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FEB. 1983

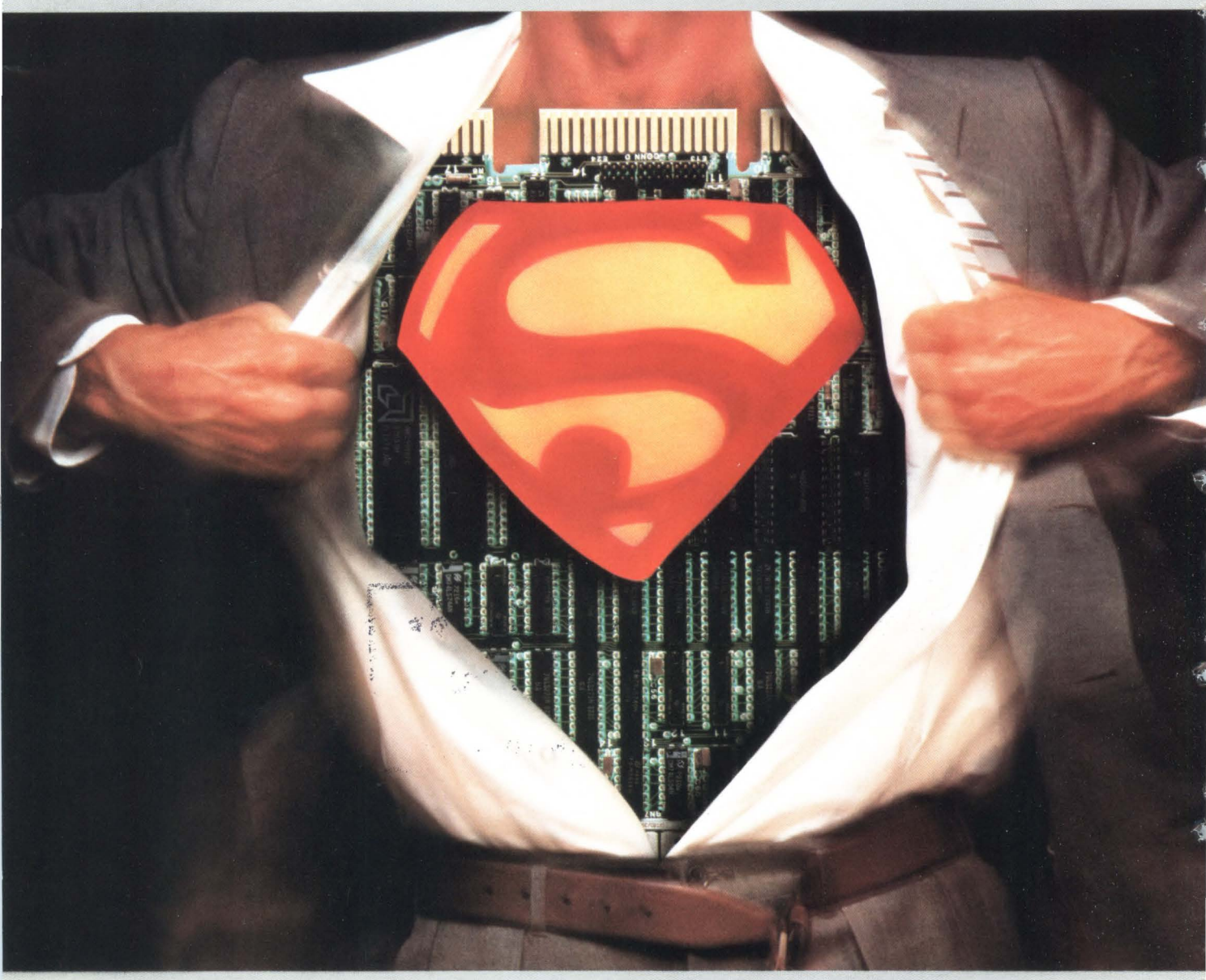
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT: ADVANCED DIGITAL ICs

CHANGING PATTERNS IN CUSTOM ICs

IT'S SUPERCONTROLLER!



It's a 6250 BPI (GCR) controller that can handle dual and tri-density drives from STC and Telex.

It's a software compatible streamer controller for today's streaming 1/2" drives.

It's a TS11* emulator.

It's a 6250 BPI streamer controller for tomorrow's new technology GCR streaming drives.

It's a single board imbedded controller with a 64K byte onboard memory that acts like a large buffer in start-stop mode and as a multiblock staging buffer while streaming.

It's the TS-6251 Supercontroller from Western Peripherals, the company that has put more magnetic tape on DEC Unibus computers than any other independent supplier. Call or write us for technical details.

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*Trademark Digital Equipment Corporation

CIRCLE 1

Kennedy is making good even better.

The 6170 Series 8″ Winchester disk drives have always provided unmatched performance for the lowest unit price in the industry.

Now, Kennedy engineering has made the product line even better. And, it still remains the lowest price unit available.

Models 6172 and 6173 have capacities of 24.5 and 40.9 megabytes respectively. They feature a linear voice coil positioner and a brushless DC spindle motor located outside of the sealed head/disk assembly to avoid inducing heat into the HDA, which yields high reliability and extends component life. Interface options allow the OEM to select between SMD, ANSI, and our inexpensive Disk Bus.

The 6170 Series has all the essentials: reliability, high performance, low cost, and immediate availability.

If you have never evaluated one of the 6170 drives, we suggest that you do so today, and if you have, we think the product warrants another look. We believe you'll like what you see. We know you'll like the price.

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For those who think a quality 8-inch disk drive has to be expensive...

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For example, our 47-Mbyte, 8-inch Winchester disk drive is competitively priced. Without any compromise in the performance you'd expect from an advanced disk drive—or in the quality you'd expect from Fujitsu.

MODEL	M2301B	M2302B	M2302BE	M2303BE
CAPACITY (MB)	11.7	23.4	23.7	47.5
AVG. POSITIONING TIME (ms)	70	70	70	70
TRANSFER RATE (KB/s)	593	593	1,200	1,200
INTERFACE	SA4000			
AVERAGE LATENCY (ms)	10.1	10.1	10.1	10.1
RECORDING DENSITY (BPI)	6,100	6,100	12,360	12,360
TRACK DENSITY (TPI)	195	195	195	195
NUMBER OF CYLINDERS	244	244	244	244
NUMBER OF DATA HEADS	4	8	4	8
POSITIONING METHOD	Buffered Stepper			
DIMENSIONS (HxWxD in.)	4.4x8.5x14.0			

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CIRCLE 3

UP FRONT

Three agreements on standard size microfloppies

Atari, Athani, BASF Systems, Fuji Photo Film, Memorex, Media Systems Technology, Shugart Associates, Sony, TDK, 3M, Verbatim, Wabash, Datatech, and Xidex have agreed to support a mutually compatible 3½" microfloppy disk format. Specifications accepted by the 14 companies for the hardcovered disks include 3.54" x 3.70" size, 80 tracks, 135 tpi, 8187-bpi maximum density, MFM recording format, 0.5M-byte/side recording capacity, 86.00-mm disk diameter, and 90- x 94-mm disk cartridge of 3.4-mm thickness. When remaining specifications are agreed upon, Sony will grant nonexclusive manufacturing licenses to qualified media manufacturers.

Concurrently, in a recent study International Resource Development Inc predicts that the 3½" microfloppy will soon become the primary storage medium for the personal computer market. The report states that the Sony-designed version and compatible 3½" disks will totally displace the more common 8" disk and sharply reduce the market for 5¼" versions. By the beginning of 1984, U.S. manufacturers will be selling 3½" drives in OEM quantities for about $225; however, by the end of the decade, competition will force the prices down sharply.

After its own evaluation study, Brown Disc Manufacturing joined Seagate Technology, Tabor, and Dysan in formally endorsing the 3¼" size microfloppy disk media as the product format the company will manufacture for use in microcomputer data storage systems. The Brown 3¼" disks reportedly provide sufficient media rigidity to operate comparably to a cartridge device. Among the reasons for choosing the 3¼", 500k-byte/side disk were cost and manufacturability. Brown feels that it can manufacture the 3¼" disks at a lower price than for the 3½" size. Further, it has not been possible to obtain a manufacturing license to provide the 3½" Sony cartridge device.

Independently, the American National Standards Committee X3, Information Processing Systems, announced project approval for standardization of a nominal 3" flexible disk cartridge. The project will cover mechanical, magnetic, and electrical features of the removable cartridge.

Proposals for streaming tape drive standards

Separate committees are planning to forward proposals for standardizing streaming tape drives to the American National Standards Institute (ANSI) and the European Computer Manufacturers Association (ECMA). The Advanced Computer Tape Standards Association (ACTSA) will propose standards for two classes of high capacity, high performance half-inch streamers to ANSI at its meeting this month. Included in the proposals are manufacturing materials; general packaging recommendations; mechanical, electrical, and magnetic characteristics for the media; and environmental specifications. One class of tape will cover a 295-Oe media that can operate between 8000 and 12,000 fcpi, the second will be for the 650-Oe tape that will store data at densities of 16,000 to 32,000 fcpi.

Proposals to ANSI and ECMA by the Working Group for Quarter-Inch Cartridge Drive Compatibility (QIC) will specify 4- and 9-track formats, a unique address for each written block, and a track reference burst on track zero between beginning of tape and load point. Members of QIC include Archive, Cipher Data Products, Data Electronics, Irwin/Olivetti, Qantex Division of North Atlantic Industries, Sanyo Seiki Mfg Co, Tandberg Data A/S, and Wangco. Observer companies include ADES, Basic Four, BNR, Kennedy, Nortronics, Rosscomp, Sysgen, and TEAC.

UP FRONT

Pretriggers

A sophisticated local area network system, made up of interfacing products designed to address the complex needs of a factory, engineering plant, or office, will be introduced by Concord Data Systems at Interface '83 next month. Especially qualified for use in a multiple computer facility environment, Token/Net operates on CATV compatible broadband cable at extended distances. The system complies with the IEEE 802 standards for LANs and utilizes the access mechanism known as "token passing" with a bus topology. Compared to alternative access mechanisms such as carrier sense multiple access/collision detection (CSMA/CD), token passing is claimed to be superior in large or realtime data network environments.

Communications controller architecture links multiple national and local systems in centralized attendant main/satellite, electronic tandem, and electronic mail networks. Just two weeks after deregulation went into effect, American Bell's Advanced Information Systems has announced the Dimension 85 PBX. Its digital communication protocol allows multiplexing of voice, data, and control information into a single digital transmission stream up to 19.2k bps, and integrated voice/data switching up to 64k bps.

Configuration flexibility that puts multiple processors to work on the problem at hand enables Burrough's B7900 to handle large volumes of data at high speed. The asynchronous system combines parallel and pipeline processing techniques with extended memory.

Managing, multiplexing, and maintaining mixed data, voice, FAX, and video networks that share 1.5M-bps transmission facilities, Timeplex's LINK/1 solves emerging needs. Implementation is both more economical and easier, since the unit handles total network control from a single point.

Entry into the gate array business by Siliconix has been achieved through a technology license with Universal Semiconductor. The nonexclusive agreement covers Universal's ISO-5 (5-micron) and ISO-3 (3-micron) silicon-gate CMOS arrays.

Performance can be increased from 3 to 16 MIPS, without software modification, through a multiprocessor system from Polycomputers, Inc. The Supramini processors can be dedicated to handle multiple batch streams or multiple terminals under a system operator's control.

Communications network problems are identified and solved through use of Hewlett-Packard's 4955A protocol analyzer. Features include easy menu-driven operation, data-stream storage that enables post-processing, seven display formats, speeds to 72k bps, 63 triggers, and a selection of interface pods.

Capacity of 72 channels with speeds up to 100 MHz enables users of Tektronix's 1240 logic analyzer to examine complex, multiprocessor systems in which separate portions operate from different clocks.

Intelligent peripheral controllers for Multibus applications have been introduced by Xylogics, Inc. One device is for control of SMD compatible disk drives, the other for streaming and start/stop tape drives.

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More speed: Ability to perform match cycles reduces access/cycle times by allowing immediate reading of data registers when adjacent words/bytes are accessed.

Advanced error handling: The DR-680 provides an on-board control and status register (CSR) which allows program control of ECC functions and contains the diagnostic information required for error analysis. The CSR can be read or written via the VERSAbus. Additionally, the DR-680 greatly increases reliability by performing error "sniffing" and error "scrubbing" during refresh operations.

Availability: Best of all, the 1.0 MB DR-680 is available now. And it comes with Dataram's standard one-year warranty.

For more information, send in the adjacent coupon or, for faster response, call Dataram today at (609) 799-0071.

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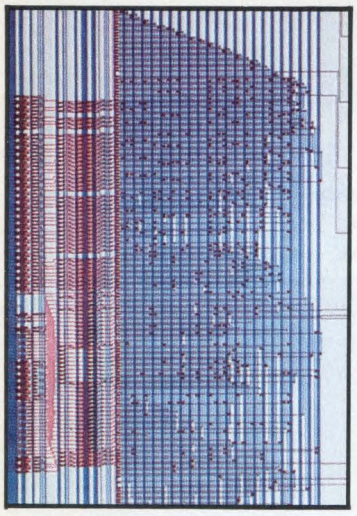
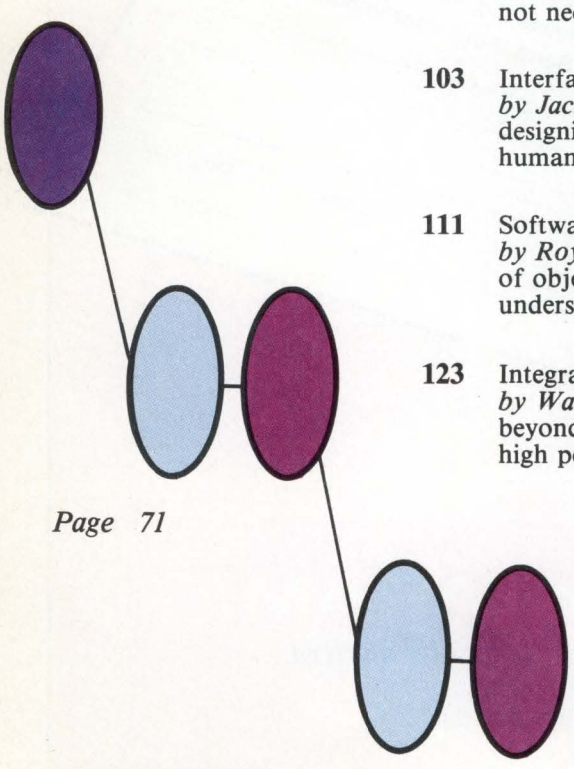
CIRCLE 4

System technology



Page 26

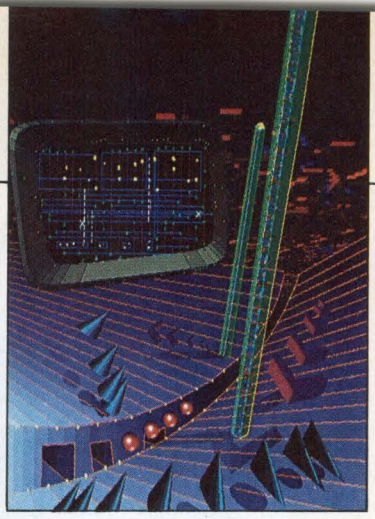
System design



Page 71

Vol 22, No 2
Feb 1983

Special report on advanced digital ICs



This month's cover, an artist's impression of a gate array design as viewed from within a CAD terminal, was created by Mark Lindquist and Robert C. Hoffman III on the Digital Effects Video Palette III. Special software was written by Henry Velick. Logic array plots courtesy of LSI Logic Corp, Milpitas, Calif.

System components

Departments

Designers' preference survey*

Editorial reviewers for parts of this issue:

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Rex Rice
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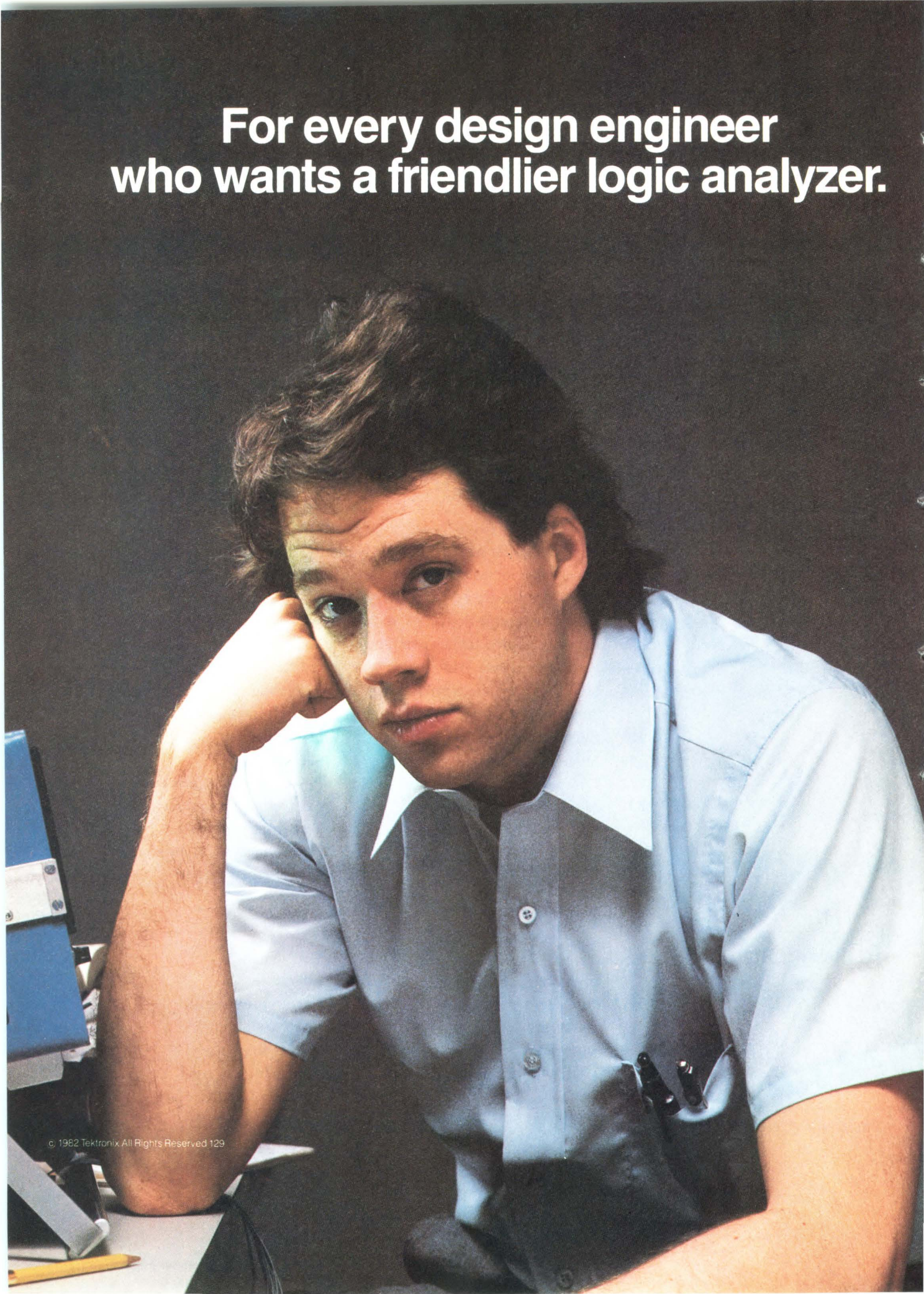
*Appearing in Domestic issues only

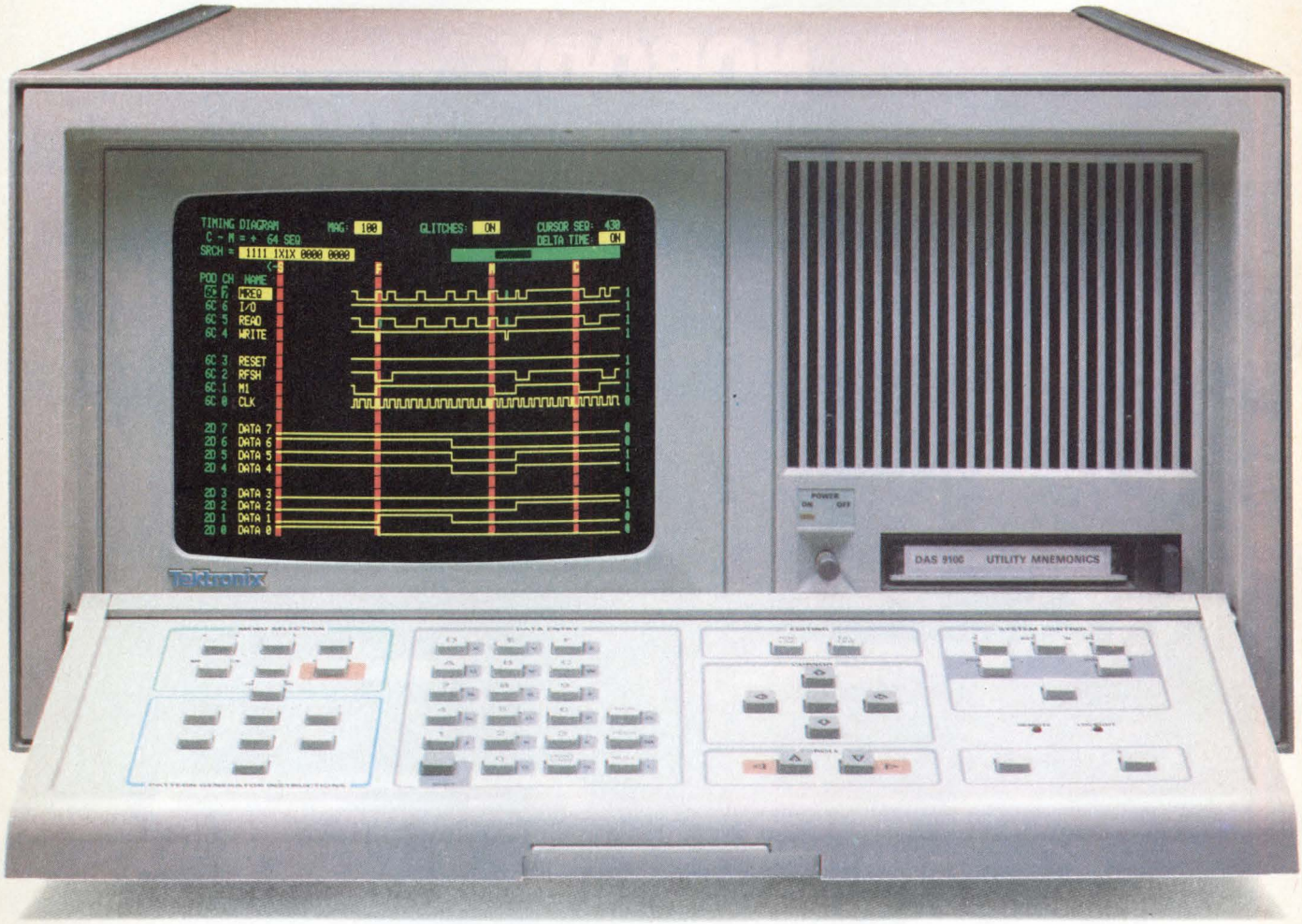
For every design engineer who wants a friendlier logic analyzer.



TEK DAS 9100 DIGITAL ANALYSIS SYSTEM

FLEXIBLE SOLUTIONS
FOR A FUTURE OF CHANGE

Tek introduces the Color DAS.



Isolating a digital fault can often be a bigger problem than the fault itself. Especially if your logic analyzer isn't as friendly as it could be.

To turn the tables, Tektronix offers the Color DAS with a new standard of friendliness for digital test instruments.

Color DAS makes the difference.

Independent research studies show color makes a significant improvement in user speed and accuracy. For example, test results showed color coding in logic analyzers reduces errors by up to 81%.

The research provided valuable information on the best use of color in the man/machine interface. So Tek developed the Color DAS with a special red-green-yellow display optimized for human interaction in logic analysis.

Not least of all, color alleviates visual fatigue and boredom, so productivity increases.

Quick to learn, easy to use.

The human engineering achievements of the Color DAS go far beyond color display.

Menu-driven keyboard entry makes the Color DAS a snap to use.

A built-in tape drive stores set-ups and user-defined mnemonics for recall when needed.

A new delta time feature gives an instant readout of time between selected stored events.

Modular Packaging gives unsurpassed performance.

Through modular design, you get the best logic analyzer performance anywhere. With data widths to 104 channels. Acquisition to 660 MHz. Pattern generation to stimulate your test circuitry and acquire the results. Simply combine the right modules and expand when you're ready.

And optional GPIB and RS-232 communications provide full remote programmability.

Color the DAS into your design picture.

For more information on the Color DAS contact your nearest Tek Sales Engineer.

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- MC68000 16-bit processor.
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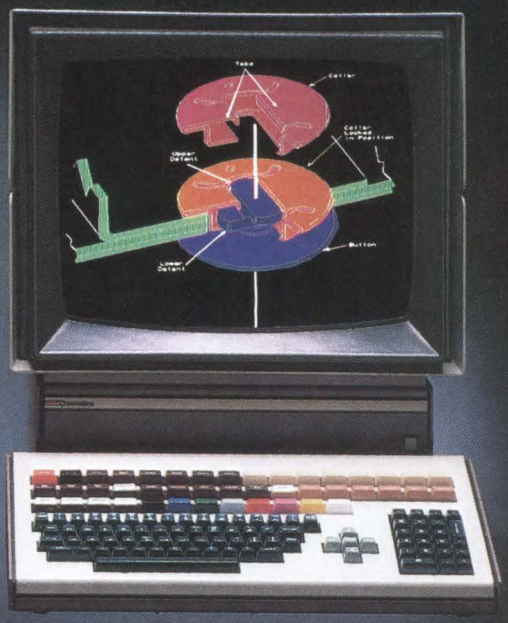
- Dual 500K byte flexible disk drives.
- 10MB or 40MB fixed disk drives.
- Up to 8MB user addressable RAM.
- IDRIS, C, PASCAL, FORTRAN.



- 512 X 512 resolution.
- Z-80 8-bit processor.

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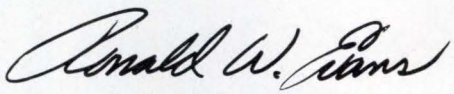
CIRCLE 7

New dimensions in system design

One tends to date oneself with such clichés as "the only engineering constant is change." In this issue, however, our editorial staff discovered that while the expression itself may no longer be in vogue, the changes certainly haven't slowed down. This issue on advanced ICs focuses on some important alternatives in system design.

While preparing this Special Report, the editors found that the impact of custom semiconductor design promises to be as forceful as the introduction of the microprocessor itself. To cut design cost and shorten turnaround time, the computer based system designer is going to become more involved with computer aided design and silicon foundry production. In approaching dedicated system applications, the designer will need to select one of three alternate approaches: complex but off-the-shelf ICs, custom fabricated advanced IC chips, or software solutions using a microprocessor.

As covered in the Special Report Introduction, we are not talking about a few isolated system designs. It is estimated that by 1990, over 50% of the ICs used in computer based systems will be custom circuits. Based on past technological advances, I have a hunch that it won't take that long. In any case, look closely at what our editors have put together, and let me know what you think.



Ronald W. Evans
Publisher

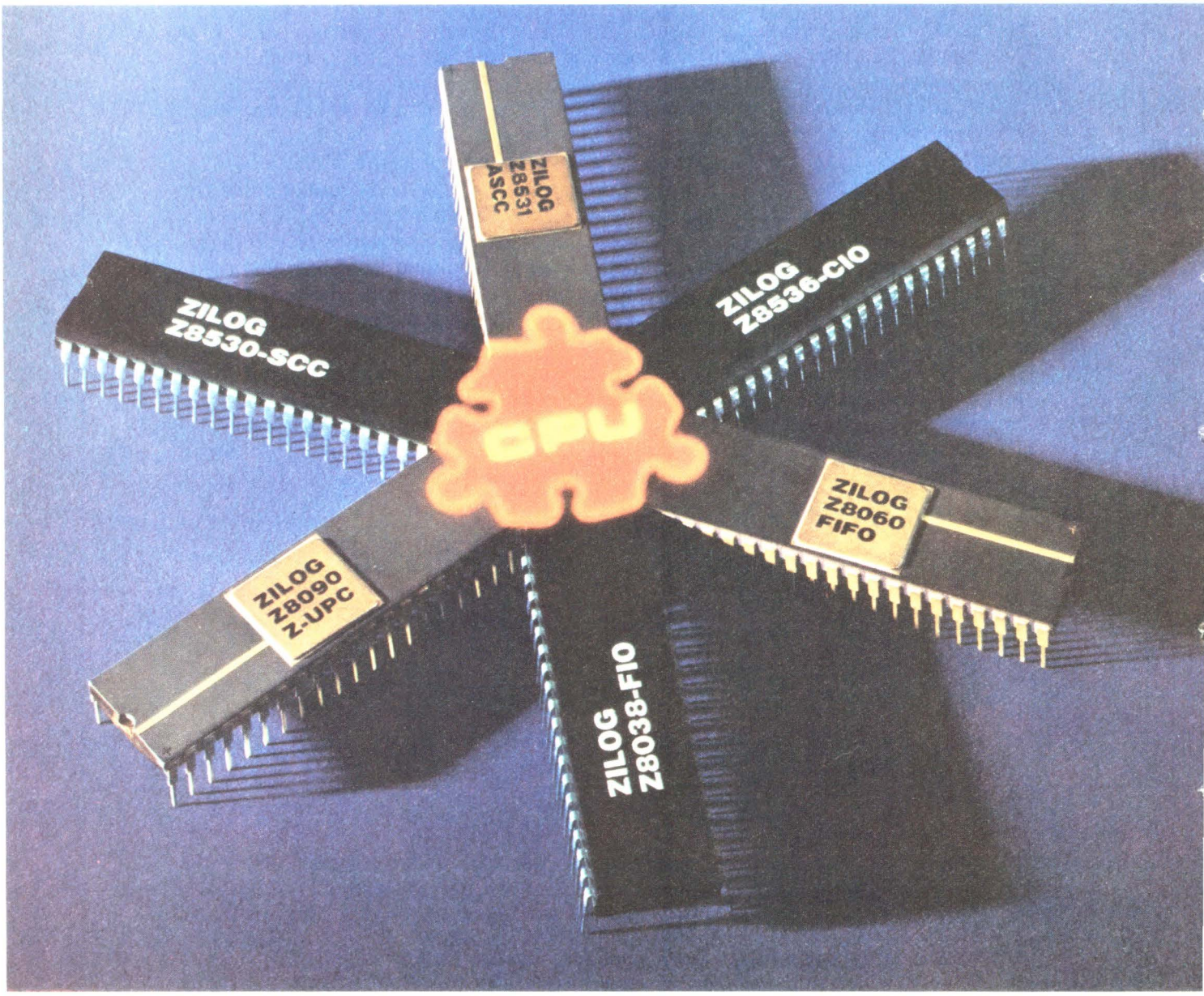
MARCH PREVIEW

Special Report on Data Communications System Design
Availability of inexpensive small computers, terminals, and workstations is making distributed processing economically feasible and desirable in a growing number of situations. Therefore, data communications systems in general, and especially local area networks (LANs)—whether for a single office building or for a manufacturing complex—are becoming essential architectural tools. Editorial emphasis of the March Special Report will be on the design of LANs and other data communications subsystems.

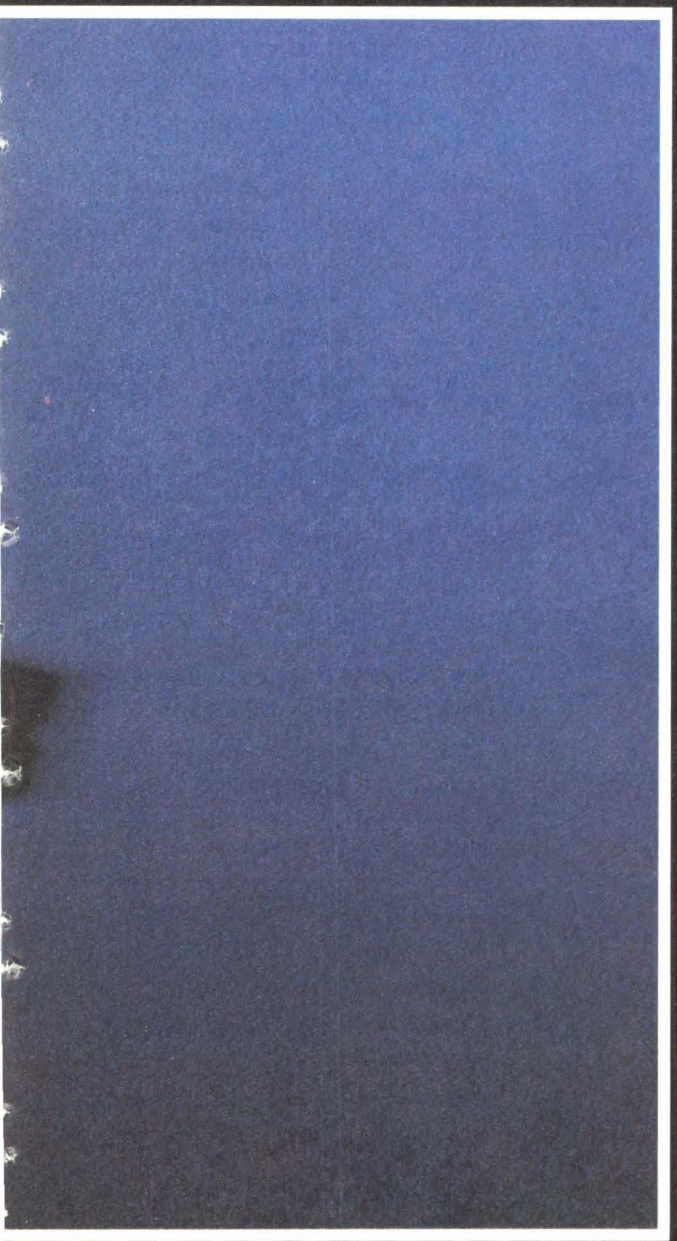
Local area networks untangled: A staff report on LANs will look at issues in the debate over baseband versus broadband systems. Also, it will examine other alternatives such as enhanced public automatic branch exchanges. Both design techniques and emerging international standards will be covered.

Other major articles on data communications: Bit oriented data link controls. . .Issues and answers on broadband network design. . .Single-chip modems. . .Ring architecture for LANs. . .

In the Microworld, Motorola and Intel CPU's



turn to Zilog peripherals for outside help.



Now, no matter whose microprocessor you choose, you can design a better system by surrounding it with Zilog's architecturally-advanced universal peripherals.

We put more functions on every chip, so you need fewer parts and less space. For example, our CIO gives you three on-board 16-bit counter/timers, 20 programmable I/O lines, and vectored interrupt control.

Advanced architectural features sharply reduce CPU overhead and increase system throughput. The SCC, for example, includes most of the frame-level protocol implementation requirements for Bisync and SDLC, including SDLC Loop Mode. And, it's the only serial controller with on-chip clock recovery logic. For asynchronous—only applications, there is also Zilog's ASCC which offers all of the benefits of the SCC at lower cost.

We also have circuits that can simplify your multiprocessor designs. Our FIO provides an easy-to-use asynchronous FIFO interface between any two CPU buses. Our UPC gives you a complete single chip microcomputer with a built-in host bus interface for distributed processing applications.

Find out today how Zilog peripherals can make your product more competitive in the Microworld—no matter which CPU you've decided on. Call Zilog TOLL FREE 800-272-6560. Or mail the coupon to: Zilog, Inc., Components Tech. Publishing, 1315 Dell Avenue, Campbell, CA 95008.

In addition to working with Zilog's CPUs, Zilog peripherals help these processors.

Supplier	16-bit	8-bit	Single-Chip
Intel	8086/8088	8080/8085	8051
Motorola	68000	6800/6809	6801
Rockwell		6502	
Texas Instruments	9900/99000		

Zilog's Universal Peripherals are available now: SCC, Serial Communications Controller; ASCC, Asynchronous Serial Communications Controller; FIO, FIFO Input/Output Interface Unit; FIFO, FIFO Buffer Unit and FIO Expander; CIO, Counter/Timer and Parallel I/O Unit; UPC, Universal Peripheral Controller. The Z-SCC (Z8030), Z-ASCC (Z8031), Z-CIO (Z8036), Z-UPC (Z8090) work with multiplexed address and data bus CPUs. The SCC (Z8530), ASCC (Z8531), CIO (Z8536), UPC (Z8590) are non-multiplexed address and data bus versions. The FIO (Z8038) and the FIFO (Z8060) work with either bus versions.

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CIRCLE 8

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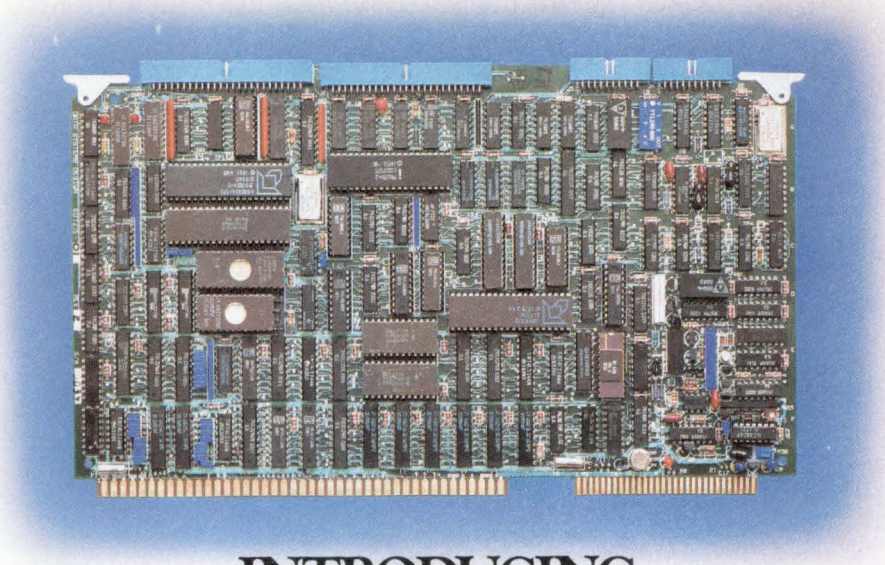
CIRCLE 11

ONE SLOT SHOPPING.



INTRODUCING THE WINCHESTER/FLOPPY/TAPE THREE-IN-ONE MULTIBUS CONTROLLER.

Try this on for size.

DSD's new 7215 single-board Multibus® controller/interface handles two SA1000-type 40Mb Winchesters, a ¼" streamer, and two 8" floppies.

Plus on-board data separation, 32-bit ECC, and self-diagnostics. All on the same board.

There's also a version for 5¼" drives, the 5215, with similar capabilities.

And both are very, very quick.

Thanks to a pipelined architecture that moves data at non-interleaved speeds.

Top-of-the-line performance.

The 7215 and 5215 are the highest performance controllers on the market for 8" and 5¼" drives.

And that makes them ideal for multiuser and UNIX™ applications.

They also emulate Intel®iSBC® 215 and iSBX™ 218 controllers so you can run RMX 86 anytime.

And with 24-bit addressing support, you can take advantage of high performance microprocessors like the 68000 and the new inexpensive memory chips to address larger physical RAM memory.

To tune system performance, both boards offer four alternatives for bus arbitration. As well as having the capability to boost system performance by performing overlapped seeks and multisector operations.

Plus the convenience to match.

The best part about all this performance is that it comes on one board. So it only takes up one backplane slot. And there are no extra boards to fool with.

As easy as that sounds, there are those of you who'd rather not do-it-yourself. For you, the 7215 controller is also available in our 770 storage systems.

And like all DSD products, our Multibus boards and systems are supported by our exclusive Rapid Module Exchange™ and regional service centers.

Shop around.

Compare our incomparable Multibus boards and systems to anything else you like. To make it easy, just send your business card to DSD Corporate Headquarters, Marketing Communications Department, for a free copy of "The Multibus Buyers Guide."

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. **Eastern Region Sales and Service:** Norwood, MA, (617) 769-7620. **Central Region Sales and Service:** Dallas, TX, (214) 980-4884. **Western Region Sales:** Santa Clara, CA, (408) 727-3163. **International Sales:** San Jose, CA, (408) 946-5800.

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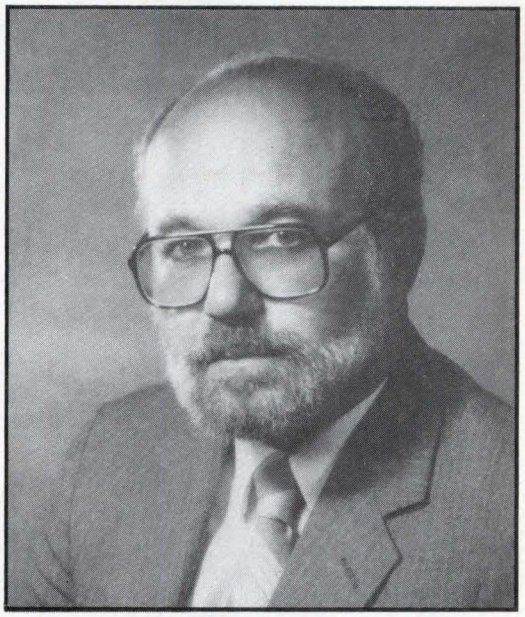
™UNIX is a trademark of Bell Laboratories.
™Rapid Module Exchange is a trademark of Data Systems Design, Inc.

DATA SYSTEMS DESIGN

CIRCLE 12

THEY WHO ALSO SERVED



On behalf of the entire staff at *Computer Design,* I thank you, our readers, for the many comments about our December 20th Anniversary issue. I feel compelled to respond to these comments, and, in particular, to Mr Currie's letter (see Letters to the Editor, p 22).

In April 1982, we asked you to select the founders and principals behind technological breakthroughs in our industry. These individuals were to be featured in our December Hall of Fame section. As I watched the responses come in, I was initially pleased that you chose many contemporaries still actively involved in today's technology. This is not to denigrate the contributions of the venerable founders of our technology back in the ENIAC, MANIAC era, for they certainly deserve to be honored.

Unfortunately, fortune and fame are related and I was—and was not—surprised to see many of our industry's pioneers missing from the list. The names of cofounders, partners, and other principals who did not appear next to an elected "Hall of Famer" were not oversights—they were simply not elected by *you*. Although the company bears both names, you chose David Packard, not William Hewlett (note, however, that Mr Packard does credit Mr Hewlett as a founder and contributor). Similarly, Bill Gates gave abundant credit to his coprincipal, Paul Allen, although the latter was not chosen.

When a company attains international recognition, it is often after one or more (or perhaps all) of the original entrepreneurs and technical contributors have departed. As the company grows, the spotlight falls on those who have remained. The information we collected on the Hall of Fame nominees came from their companies or from nominee interviews. In order to keep the Hall of Fame in its original perspective, we did not feel it was our right to embellish the Hall of Famers or add other names to the list. Whatever contributions the elected nominees and others have made—whether marketing and organizational or technical—they are all permanently linked with the companies and technologies that have made significant impacts on all of our professional lives.

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—July
"The ABCs of Simplifying Logic Equations, Simply"
Edward Glenn McCoy, Advanced Computer Systems

This article will now compete with other monthly winning articles for the 1982 editorial excellence award.

The Part

Most second-source agreements go something like this: "Here's the mask, you figure it out."

Then there's the "I'll-show-you-mine-if-you-show-me-yours" kind.

The Partnerchip is something else.

AN ALLIANCE DEFINED IN TERMS OF TIME, NOT PARTS.

For the next ten years, Intel and Advanced Micro Devices will develop, expand and support the iAPX86 family together.

The key word there, is "together."

We'll exchange masks, technology, R&D, ideas, test tapes. Everything we need to make sure our parts are identical.

Only the Partnerchip guarantees

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you two responsible domestic sources for an entire 16-bit CPU family.

ONE HUGE, HAPPY FAMILY.

Together, Intel and Advanced Micro Devices have more ways to enhance system performance than anybody. There's the 8086, the highly integrated 186, the ultrahigh performance 286 CPU's. We've got DMAs, Counter Timers, Interrupt Controllers, Clocks. The works.

And when you order our parts they're available today. Now. Not next year.

But that's only the beginning.

Because we're working together, we'll be able to work faster. You'll see a steady stream of CPU upgrades, peripherals and support for the iAPX86 family over the next ten years.

You'll see new products for high-speed encryption. Products for high-speed communications. State-of-the-art hard disk controllers and graphic controllers. Everything you need to keep you at the leading edge.

If you thought the iAPX86 family was good before, take a look at the Partnerchip.

It's twice as good.

The iAPX86 People.

Intel and Advanced Micro Devices.

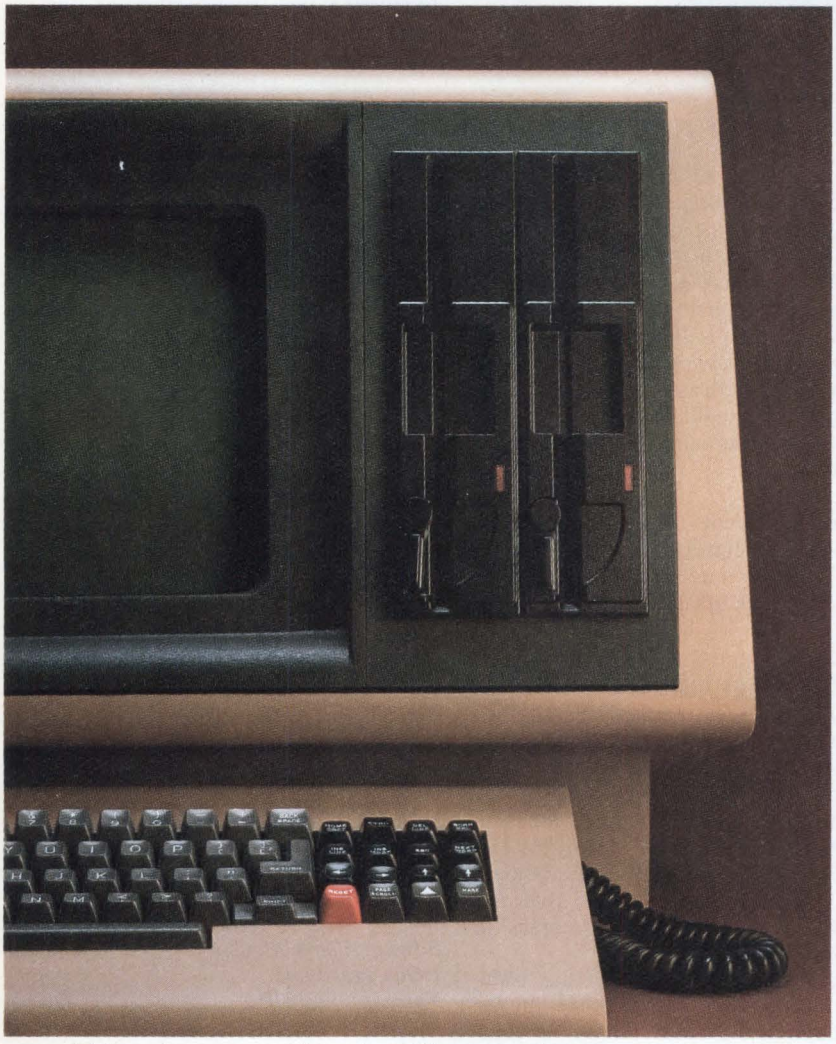
Advanced Micro Devices, 901 Thompson Place, Sunnyvale, CA 94086 • (408) 732-2400

OUR NEW 8" DRIVES PUT US IN A TIGHT SPOT.

They're half the height of a conventional 8-inch floppy.

The exact depth of a standard 12-inch CRT terminal.

And actually capable of squeezing 8-inch drive performance into desktop systems that haven't room for full size 8-inch drives.



What's more, they're Shugart's newest family members—our SA810 single-sided and SA860 double-sided floppy disk drives.

These half-height 8-inch drives offer the OEM more design flexibility, while providing an attractive new alternative to today's minifloppies.

Unlike other reduced height drives, only Shugart's SA810/860 series eliminates the need for major redesigning of hardware. And software. And controllers.

Because they're compatible with our industry standard SA801/851 8-inch drives. Same mounting holes. Same internationally recognized DC power supply. Same controller interface. And all the jumper options you need to build in the features you need.

They're also compatible with the existing user base of over 200 million 8-inch diskettes.

And the SA810 and SA860 offer distinct advantages over 5¼-inch drives, including more capacity. In the case of the SA860 (1600 kilobytes), 60 percent more than a double-sided 96-TPI minifloppy. With faster access times (89 msec versus 158 msec average). And faster transfer rates (500 versus 250 kilobits per sec).

They also offer a bundle of features not found in conventional 8-inch drives.

The rapid start DC motor, for example, eliminates the need for belts, pulleys, and head-load solenoids. So reliability is substantially increased. Media wear is reduced. And overall operation is much quieter.

All of which makes our new SA810/860 drives the smart solution for a wide range of high performance desktop applications—from word processing to distributed network systems.

All backed by the industry's largest and most experienced engineering, sales and service organizations.

For more details, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, CA 94086, (408) 733-0100 (Hamilton/Avnet, authorized distributor).

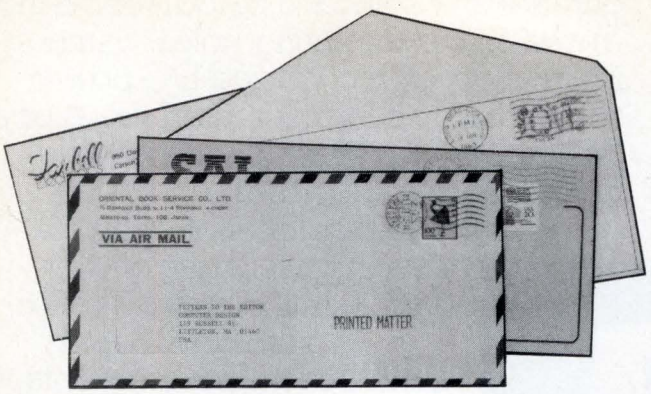
And see if you can squeeze us in.

Shugart

Right from the start.

CIRCLE 14

Milpitas, CA 408/263-2600; Costa Mesa, CA 714/979-1935; Thousand Oaks, CA 805/496-5388; Minneapolis, MN 612/574-9750; Richardson, TX 214/234-3568; Framingham, MA 617/879-1700; Saddle Brook, NJ 201/368-8445; Atlanta, GA 404/955-8968; Toronto, ONT 416/475-2655; Paris, France (1) 687-31-41; Munich, West Germany (89) 78-60-21



Missing names in the Hall of Fame?

The 20th anniversary issue of *Computer Design* held some interesting surprises, as well as a fair share of paradoxes. Hall of Fame section began with an impressive, albeit heterogeneous, list of names well known in various segments of the computer industry. Then followed a number of profiles of the newly elected Hall of Famers, with the last page entitled Meritorious Nominees.

The profiles lacked a certain degree of consistency. While Dennis M. Ritchie and Kenneth L. Thompson, and Steven Jobs and Stephen G. Wozniak shared their respective marquees, William Gates appeared without Paul Allen, David Packard without William Hewlett, and Gary Kildall without people like Dorothy McEwan, Larry Alkoff, and Anthony Gold.

Equally puzzling is the mixing and mismatching of the type of contribution, and the degree of significance and impact. Marketeers, promoters, hardware and software engineers, and historical figures are all interspersed within the section.

Including individuals such as Harold Garland (Cromemco) "for spearheading the personal computer industry by designing and marketing bus compatible microcomputers" is very distressing. While this might constitute a worthwhile activity, it certainly isn't any significant pioneering or design effort. Cromemco did little more than market recast versions of the MITS Altair.

Henry E. Roberts, founder of MITS and designer of the Altair and S100 bus, is deserving of a lasting place in the Hall of Fame. He is the visionary who recognized that BASIC was an important language for microcomputers, and had as his primary motivation, the idea to bring computers to the masses. The world's first computer store, microcomputer conference, and publishing company for microcomputer applications, were all the products of his fertile mind.

The account of Microsoft's 8080 BASIC Interpreter is appalling. From its first execution by the Altair, this product was under exclusive license by MITS. The 4K BASIC did not come into being in 1976, as claimed in *Computer Design,* but rather in 1975. The significant work beyond the first primitive version was the result of efforts largely provided by Paul Allen while employed by MITS as Director of Software. Specifically, he was responsible for all the enhancements until version 4.0, and was employed by MITS until its release.

Edward H. Currie
Lifeboat Associates
1651 Third Avenue
New York, NY 10028

Solution defies logic. . .

I am somewhat surprised to see *Computer Design* publish an article before thoroughly investigating the ideas and methods proposed by it. This was obviously the case in the July 1982 issue (pp 99-102). Edward G. McCoy's "The ABCs of Simplifying Logic Equations, Simply" is the fairy tale I am referring to. There are three primary areas in which the article fails:

Terminology: Mr McCoy has obviously forgotten or ignored the proper definition of the word "binary" in coining the term binary logic number (BLN) to represent the variables in logic equations. He repeatedly refers to numbers such as 202, 440, etc, as BLNs. Binary numbers consist of only 1s and 0s.

Lookup tables: Mr McCoy insists that no lookup tables are necessary in reducing logic equations using his arithmetic method. However, on the second page of the article, in plain black and white is the BLN conversion table. His method uses this table to convert final BLNs back to logic variables.

It doesn't work: Mr McCoy chose only to present examples that happen to reduce down to his specified solutions. How about the equation $ABC + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$? It is obvious that an arithmetic method fails to reduce this equation completely. Mr McCoy treats this situation as a trivial solution, leaving it up to the "logician" to select the best form of the solution for the particular application. I believe that upon discovering such trivial solutions, logicians will not use the arithmetic method since the method itself is trivial!

Ronald L. Guerrero
International Laser Systems Inc
3404 N Orange Blossom Trail
Orlando, FL 32804

. . .Or does it?

My referral to decimal coded numbers 220, 440, etc, as BLNs evolved quite naturally because the logic variable equivalent of ABC is, after all, 111_2. What is that other than a binary representation of a logical literal equivalent? Additionally, the TI-59 calculator treats this input as a decimal number. Tables were included to illustrate and clarify the method. Any first year engineering student examining a table that shows only a partial list of code should be astute enough to discern a pattern and write a program to serially scan the numeric output code and convert it to its literal equivalent. Hence, lookup tables are not required.

Nowhere in this article does it state that the method I evolved will always produce a minimal solution. It will always produce a correct solution—sometimes not minimal—but always correct.

Edward Glenn McCoy
1 Oak Hill Lane
Nashua, NH 03062

A star is reborn

I read Edward G. McCoy's article "The ABCs of Simplifying Logic Equations, Simply" and found it very interesting since I had never come across the Star algorithm. Using Mr McCoy's method, I wrote a program in BASIC for my Motorola 6809 EXORciser.

Richard M. Beard
Johns Hopkins University
Johns Hopkins Rd
Laurel, MD 20707

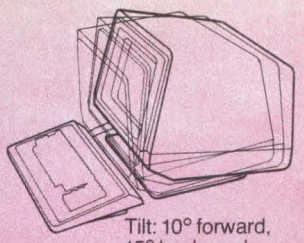
See the article "Minimal Solutions to Logical Dilemmas" on p 89 for an elaboration of the fundamentals upon which Mr McCoy's article is based.

The VISUAL 100 video display terminal is 100% compatible with the DEC VT 100 terminal from identical software right down to the layout of the keys and the sculpturing of the keyboard.

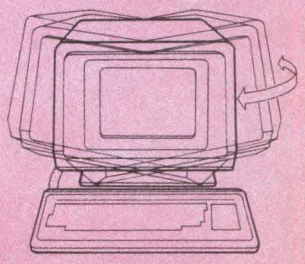
But when it comes to ergonomics, the VISUAL 100 is something else! For example, the VISUAL 100 is designed in lightweight plastic that can easily be swiveled and tilted for maximum operator comfort. A detached, low profile keyboard, and 12″ or 14″ non-glare screen are just a few of the other human engineering advantages of the VISUAL 100.

The Advanced Video package and current loop interface that are optional with the DEC terminal are standard with the VISUAL 100. Plus we've added an optional Buffered Printer Interface with independent baud rate, independent parity and printer busy via "XON-XOFF" protocol. And although the VISUAL 100 is a step up from the DEC VT 100, it is priced a step below. Only $1,345 Call or write for full details.

Service available in principal cities through Sorbus Service, Division of Management Assistance, Inc.



Tilt: 10° forward, 15° backward



Swivel: 270°

VISUAL 100.

Combines VISUAL'S ergonomic excellence with DEC VT 100® performance.

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VISUAL See for yourself

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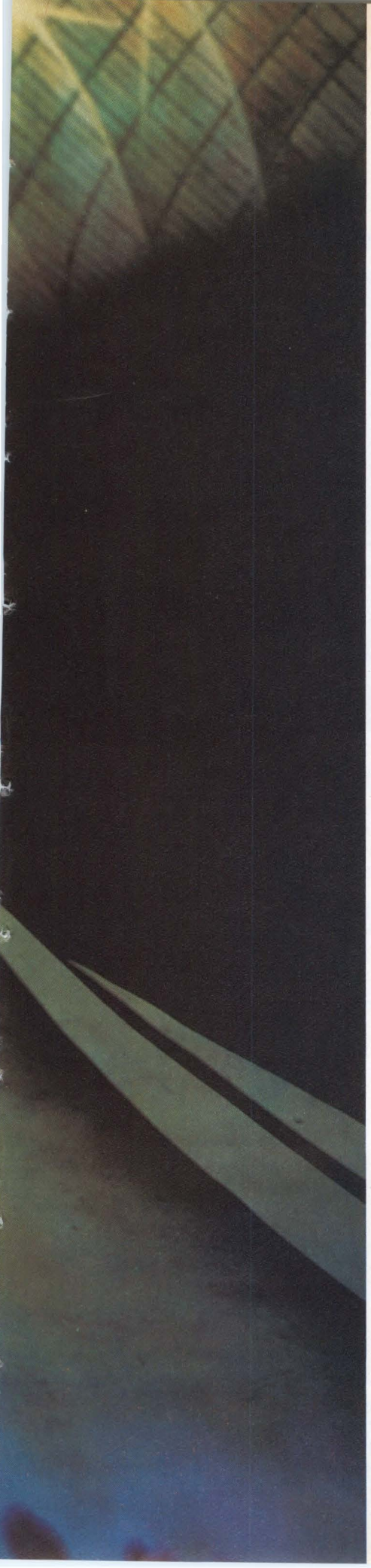
CIRCLE 15



New 64K DRAM...

"Nibble Mode" gives effective cycle time under 85ns

Here's another first in VLSI from INMOS. It's a 64K x 1 DRAM with a feature called "Nibble Mode". By providing the on-chip equivalent of 4-way interleaving, the IMS2600 allows high-speed serial read/write access to 2 bits, 3 bits or a nibble, allowing effective cycle times below 85 ns.

Two high-speed versions of the IMS2600 are available:

	Access Time	Cycle Time	"Nibble Mode" Cycle Time
IMS2600-10	100ns	160ns	55ns
IMS2600-12	120ns	190ns	65ns

But that's not all. The part operates at cycle times down to 160ns and dissipates only 303mW max at 350ns cycle time (standby power is only 22mW). In addition, this advanced 64K DRAM offers "$\overline{CAS}$ before $\overline{RAS}$," a refresh-assist function that frees pin 1 for future 256K use.

The IMS 2600 is a direct plug-in replacement for other 64K DRAMs in existing designs. And it's the 64K standard for new designs. Available now, the IMS2600 is packaged in a 16-pin, 300-mil DIP with the industry standard pinout.

For a low-cost evaluation kit, "Nibble Mode" application note, or for technical assistance, complete the coupon and mail it today.

inmos

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CD2/83

Byte of 100ns 64K DRAMs $100

☐ Please send ____ set(s) of the IMS2600-10 Evaluation Byte kit and complete technical data. Limit 3 kits per customer. Offer expires Mar. 31, 1983 Send check or money order ($100/kit) to address below, or order through your local INMOS distributor.

☐ Send IMS2600 "Nibble Mode" application note and technical data.

☐ Have a salesman call.

Name _____ Title _____

Company _____

Address _____

City _____ State ____ Zip _____

Telephone ( ) _____

Return to: 64K DRAM Offer
INMOS Corporation, P.O. Box 16000, Colorado Springs, CO 80935

CIRCLE 16

Color raster plotters use different high resolution plotting techniques

Two recently introduced color plotters aimed at producing rapid hard copy of high resolution color raster data, approach the color screen copying problem from different angles. A 4-color ink jet plotter from Tektronix, Inc uses a single-pass plot, and an electrostatic color plotter from Versatec uses a pass for each primary color plotted.

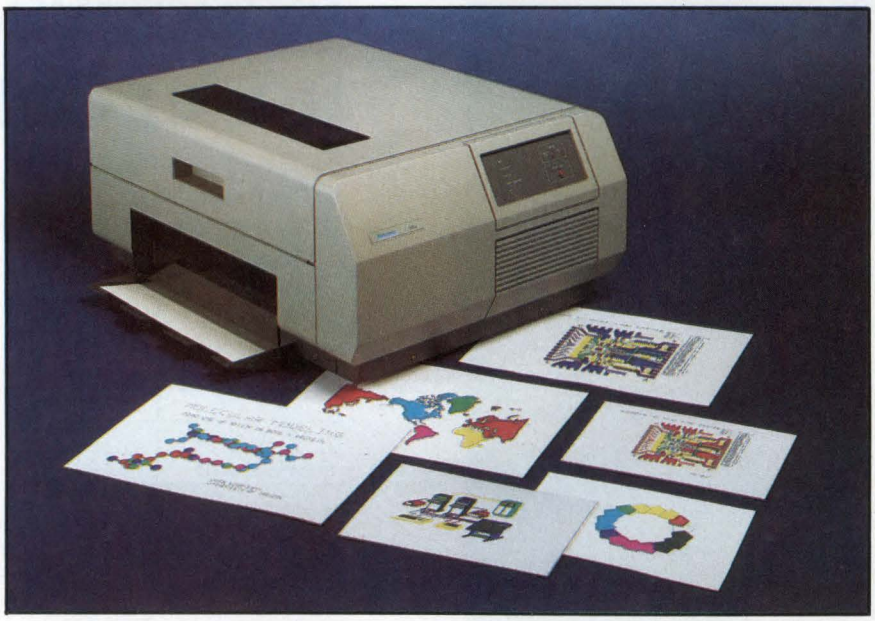
Versatec's 4-color electrostatic plotter has a 200 dot/in resolution and can produce a full-color 34″ x 44″ (86- x 112-cm) E-size drawing in 8 min; it can also provide color or monochrome plots of any length. This plotter uses translucent toners in magenta, yellow, cyan, and black, and plots on 42″ (107-cm) wide roll paper. Using raster data, the plotter makes five passes over the writing head assembly to produce a full-color plot, rewinding the paper at 10 ips between passes.

Since the high resolution demands exact registration, the first pass is devoted to writing servo and registration information along the paper's two edges. This registration pass also allows the paper to undergo any stretching or temperature and humidity effects so that it is relatively unaffected on subsequent passes.

Registration information is written as two lines down each edge of the paper with tiny cross marks through them. For horizontal registration, optical sensors track the lines, and for any deviation less than 10 mils, they cause the writing assembly to shift to compensate. If registration deviates beyond 10 mils, the entire spool assembly is shifted. For vertical registration, optical sensors count the cross marks on the registration lines in groups of 16 and compute their average position. This positional information is fed back to the paper advance mechanism to maintain registration within 3 mils; horizontal registration is likewise accurate to within 3 mils. A full-color plot then requires four more separate raster plots.

This plotter is a default monochrome device that takes black and white data for standard Versatec interfaces with no modification, but at twice the speed. Color raster image data must be separated at the host and sent to the plotter, with a header on the data stream telling the plotter both the plot's length and the color to plot.

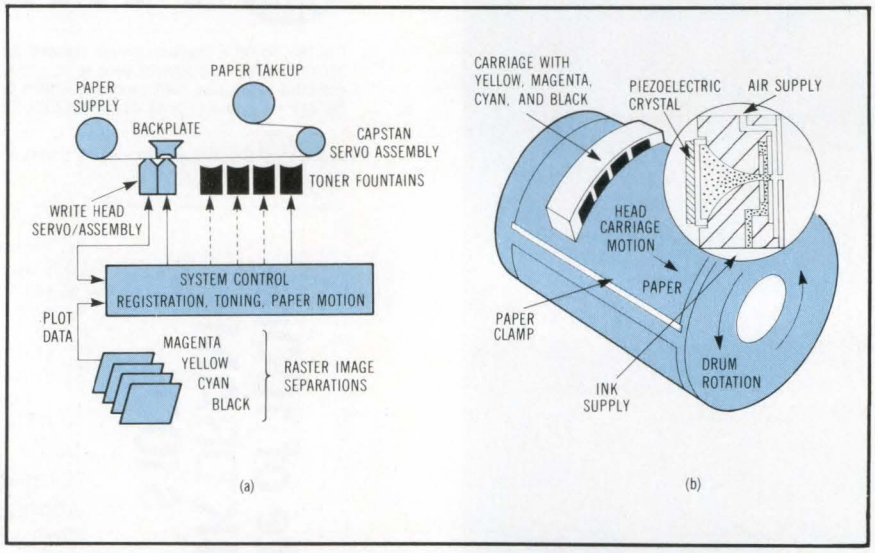
The writing array is a densely spaced (200/linear in) assembly of writing nibs embedded in a stationary writing head. Nibs receive voltage according to information in image memory and can form colors either by overlaying a limited number of translucent dots or by juxtaposing dots so that the eye perceives a variety of hues. This information must be supplied to the plotter by host software or by an intermediate processor between the plotter and the host. Several integrators of CAD and geophysical systems are claimed to be developing color plotting software.



Tektronix's color graphics copier produces either 8.5″ x 11″ or 11″ x 17″ 8-color output in either horizontal or vertical format under program control.

Tektronix's model 4691 copier uses a drop-on-demand color ink jet process in which ink droplets are deposited on a rotating drum as the printhead moves

(continued on page 30)



In Versatec's electrostatic process (a), array of densely packed writing nibs in stationary writing head selectively creates minute dots on paper passing over head. Tektronix's process (b) uses ink jets and rotating drum; four colored inks produce full-color copies in a single pass of heads along paper.

It's not Magic, it's NEC.

The Spinwriter™ handles any business form you can conjure up.

No matter what your business forms, no matter what size, shape or format, the NEC Spinwriter printer can handle them. Automatically. We have eight forms handlers. All quickly and easily user changeable. There's a single-sheet feeder with an add-on second bin or envelope feeder. There's also a cut-sheet guide, a bi-directional tractor, demand document tractor with tear bar and copy separator, manual inserter and bottom feed. With some of our forms handlers, you get functions unavailable anywhere else—like bi-directional paper movement and ultra-fast ribbon cartridge changing with forms handlers in place.

Of all printer companies, *only NEC* designs and manufactures its own comprehensive family of forms handlers. We built them especially to go with our printers, so they give you the same reliability that has made our Spinwriters a legend.

Our Spinwriters have the industry's most remarkable uptime standards. More than *two years* between failures! They need no preventive maintenance or routine lubrication. Ever. And, with only three major spares, they usually can be fixed in only 15 minutes.

Whatever the size or shape of your business form, a Spinwriter can handle it, quickly and reliably. It's not magic, it's NEC.

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CIRCLE 17

16000 WAYS TO OVERCOM THE LIMITATIO OF YESTERDAY MICROPROCESS

E
NS
S
ORS.

THE NS16000 MICROPROCESSOR FAMILY INCREASES SOFTWARE PRODUCTIVITY AND MAKES OTHER MICROS LOOK ARCHAIC.

Software productivity has become a major issue in computer-related product development. In microprocessor-based systems, software productivity centers around the capability of the microprocessor to maximize software utility relative to shorter development cycles, improved software reliability, and extended software lifecycles.

The degree to which the microprocessor can maximize software utility directly affects the cost of a product, its reliability, and time to market. It also eliminates future software modification for product enhancement or because of rapid advances in hardware technology.

The NS16000's architecture effectively addresses these software issues.

EFFICIENT MEMORY MANAGEMENT.

This microprocessor family combines 32-bit performance with demand paged virtual memory for efficient management of large address space. It facilitates high level language program development and efficient program execution. Floating point is also integrated into the architecture.

This combination gives the user large system computing power at a lower cost. Two orders of magnitude lower, in fact.

WE WEREN'T SATISFIED WITH THE "BOTTOM UP" APPROACH.

When we began designing the NS16000 microprocessor family, we decided on a radical departure from existing architectures—designs that date back more than a decade.

While others extended 8-bit component technology upward to the system level, we weren't satisfied with that "bottom up" approach. Instead, we anticipated the computing needs of the '80s and '90s and took the time to extend sophisticated mainframe and minicomputer technology downward to the chip level.

The result is an advanced and efficient family of microprocessor hardware, software and development support products. Our entire NS16000 family offers everything you'd expect from powerful 32-bit machines and is easier to program and use than 16-bit "bottom up" micros.

Everyone who has evaluated the NS16000 recognizes its advanced architecture. We appreciate that response. Because it proves that the NS16000 family is exactly what we designed it to be—a solid foundation from which we can build solutions for your future designs while satisfying your needs for today.

NS16000. THE PROGRAMMERS' MICROPROCESSOR.

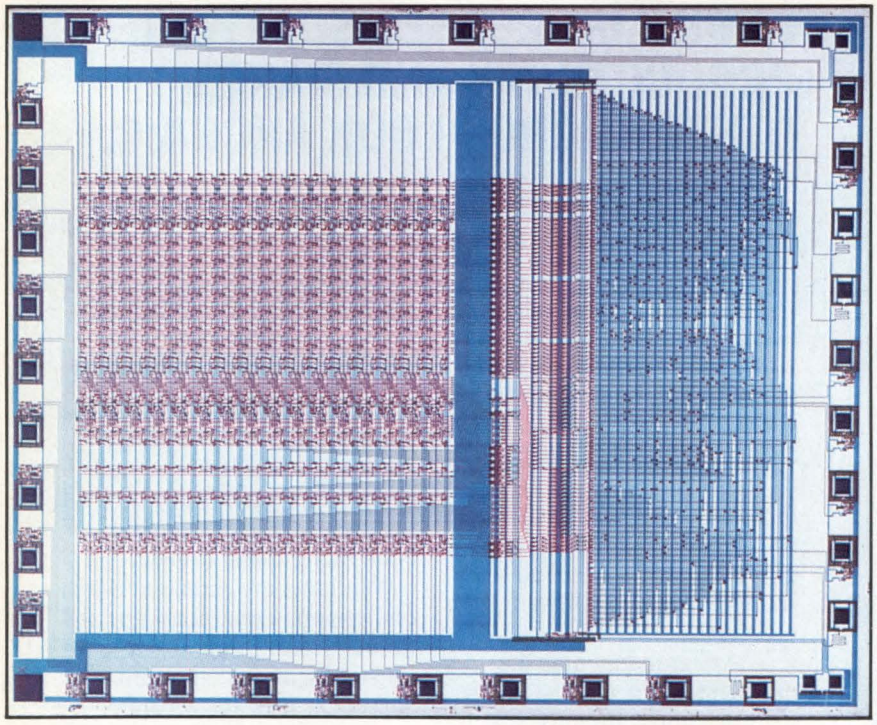
National Semiconductor

MICROCOMPUTER SYSTEMS DIVISION

CIRCLE 18

Color raster plotters

(continued from page 26)



IC mask produced by Versatec's electrostatic color plotter is constructed from four translucent toners. Electronically produced drawing can be of any length.

along its length. Air flow stabilizes the ink droplets ejected from the printhead by impulses applied to a piezoelectric crystal. Four ink cartridges containing yellow, cyan, magenta, and black can also be used to mix red, green, and blue. For a broader range of colors, droplets can be juxtaposed through a technique called dithering.

This copier has a resolution of 150 dots/in and can reproduce color CRT raster data at a 1 to 1 dot to pixel ratio or up to 3 to 1 dots/pixel for large copy. Copies can be made in either A (8.5″ x 11″) or B (11″ x 17″) sizes in 2.5 to 4 min; images can be produced in either horizontal or vertical format under program control. Host connection via a parallel interface not only allows the 4691 to act as a host resource, but also allows plotting at host resolution by using host rastering software.

Preliminary unit pricing for the Versatec color plotter is $98,000; for the Tektronix 4691 a price of $12,500 is projected. **Versatec, a Xerox Co**, 2710 Walsh Ave, Santa Clara, CA 95051; **Tektronix, Inc**, MS 63-635, PO Box 500, Beaverton, OR 97077.

Versatec—Circle 240

Tektronix—Circle 241

Color graphics terminal applies shiftable cell concept to achieve high interactivity

Graphos™, a desktop color graphics terminal, marks Ithaca Intersystems' expansion into the peripherals area from its microcomputer systems base. Selling for under $8000, the terminal supplies 640- x 480-pixel resolution and works as an intelligent workstation, distributed workstation, or standalone computer. It combines the ability to simultaneously display and manipulate 16 windows independently with smooth scrolling pages that can be larger than the windows, a menu choice of colors from a palette of 32,768, and a device independent segmented display file software system.

Based on shiftable cell™ concept the system's design combines features of alphanumeric and bit-mapped architectures. The architecture allows pages to be smoothly scrolled horizontally or vertically under the windows. Since more than one window can be assigned to a page, different parts of a large image may be compared. The system's 64k-byte memory permits full exploitation of this capability.

A compromise between the one to one correlation of screen location and

(continued on page 32)

10 years ago your boss was buying Ball.

Now you have 6 new chances to look just as smart.

We've introduced five new products designed to keep your manufacturing and service costs low, your product reputation high, and your sales picture bright. It just goes to show that buying Ball is just as smart as it was ten years ago when we introduced our first high quality data display. And even that wasn't the beginning. Twenty-five years ago we introduced our first broadcast video monitor. Now, we're putting that 25 years of experience into a whole new generation of Ball monitors.

The BC-200/300 Series gives you advanced CRT technology at high volume and low price. Available with 12 or 14 inch CRT.

S-200 Series Power Supply provides high reliability DC power for both monitor and logic power.

The HD Series gives you the elevated line rate, regulated low voltage and dynamic focus that your customer's high-density display applications demand.

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The BC-500 Series provides a high quality, cost effective, 15 inch data display monitor.

The CD-100 gives you a choice of a 5, 9 or 12 inch composite signal input, general purpose remote display.

Call one of our sales offices for a good look at our whole new generation. . . or ask your boss about us. After all, we grew up together.

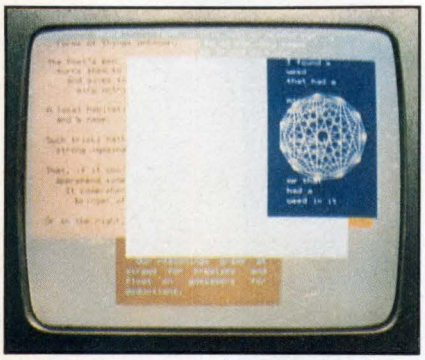
The new wave from Ball.

Ball Electronic Display Division

Ball Electronic Display Division, St. Paul, MN 55164 (612) 786-8900

CIRCLE 20

Color graphics terminal
(continued from page 30)



Display on low cost Graphos desktop color graphics terminal from Ithaca Intersystems can show and manipulate up to 16 windows using shiftable cell concept. Text and graphics in up to 16 different colors can be combined in each window, and can be smoothly scrolled under any fixed window.

display memory address used for bit-mapping and the fixed cell character descriptions of alphanumeric terminals, the shiftable cell concept has certain advantages. It requires only a single copy of each character to be stored in memory; this copy can be referenced by an arbitrary number of pointers. Since only the pointers need be changed, the display can be modified quickly; rapid color changes are also easily accomplished.

Each of the 16 displayable windows offers individual scroll, pan, and zoom with graphics overlay. Segment retention eliminates the need for retransmission from the host computer. Windows also supply 2-dimensional segment transformations; high level primitives; full 2½-dimensional polygon rendering with shading, crosshatching, and textures; and horizontal smooth scroll. Up to 16 displayable colors within each window are menu selectable from a palette of 32,768 colors.

Windows can be moved independently of one another without rewriting display memory, resulting in highly interactive operations. Applications software can create and delete windows for host computer dialogue, command menus, or data presentation. Text and graphics can be mixed in any window. Users can move windows within the screen, stack or restore them, and direct keyboard, graphic tablet, or other device input to any window.

An MC68000 microprocessor within the unit permits firmware implementation of a device independent graphics subsystem. Multitasking device independent software resident in the 112k bytes of EPROM within the terminal as firmware features local segmented display list processing, symbols, 2-dimensional transforms, full picking correlation, polygon rendering, and floating point world coordinates. This provides a high level interface for applications programs with output directable to supported peripherals or the screen. The microprocessor performs all local graphics processing. Since graphics processing is done in the terminal, the host is freed for other tasks. Details of presentation are of no concern to the host, leaving it free to support more users in an interactive environment.

Plug-in I/O function units, one for host I/O and two for local peripherals, permit a variety of protocol options without hardware redesign. These 2″ x 5″ adapters plug in to supply 110- to 9600-baud RS-232 or current loop, dual RS-232, 8- or 16-bit parallel, or RS-170 interfaces. An optional 9-slot IEEE-696 D4 expansion bus accommodates S-100 cards. **Ithaca Intersystems, Inc**, 1650 Hanshaw Rd., Ithaca, NY 14850.
Circle 242

CONTROL & AUTOMATION

High performance measurement and control system plugs into low-end microcomputer

Software sampling rates to 20k data points/s; conversion accuracies of 12, 14, and 16 bits; and the capacity for hundreds of analog and digital I/O channels are key features of Data Acquisition Systems' 4-member Series 500 measurement and control family. The modular, integrated system puts high speed signal analysis, precision measurement, and industrial process control formerly reserved for minicomputers within reach of microcomputer budgets.

Designed for the Apple II computer, Series 500 systems expand through a library of 14 plug-in I/O modules. Single-system capacity can reach 336 channels of 12- or 14-bit analog to digital, single-ended input; 168 channels of differential input; 60 channels of 12-bit digital to analog output with 2.5-μs conversion time; 24 channels of digital to analog output with 16-bit precision; 192 channels of digital input or output; or 192 channels of ac and dc power control. Beyond that, two or more Series 500 systems can interface to the same computer for commensurate leaps in performance.

Analog input modules are available in isolated and nonisolated versions. Choice of single-ended and differential inputs accommodates direct connection to all transducer types. Together with the analog input modules, analog to digital modules provide multiplexed conversion to eliminate redundant hardware.

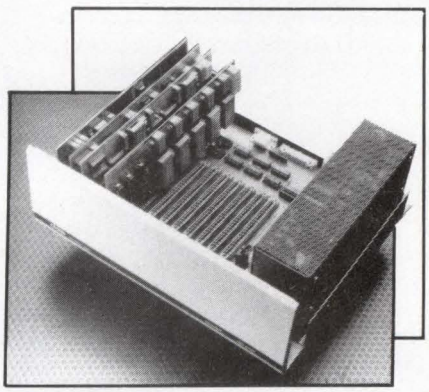
Digital input and output modules give isolated channels for reading and controlling digital devices. Applications include sensing and controlling digital devices, reading switches, controlling relays, and interfacing to all TTL signals. Solid state power control modules directly monitor and control ac and dc devices with full optical isolation.

Moreover, modules are fully supported by the Soft500 integrated software package, an extension of AppleSoft BASIC that functions in both floating point BASIC and Pascal language environments. It consists of an operating environment and over 40 language statements for direct control of data acquisition and measurement/control devices, as well as for statistical analysis, integration/differentiation, array control, and screen graphics.

Commands operate as host language statements, obviating assembly language programming for common analysis and I/O routines. Signal conditioning, noise reduction, and protocol conversions are handled as optional parameters to statements.

Soft500's realtime, interrupt-driven architecture supports foreground/background processing and multitasking for concurrent analysis, display, and

(continued on page 38)



Inside view of DAS Series 500 measurement and control system. Each frame accepts 12 modules in any combination to meet wide range of digital, analog, or power control requirements.

EXPAND YOUR MULTIBUS SYSTEM'S OUTER LIMITS.

XYLOGICS HAS SOLD MORE HIGH PERFORMANCE MULTIBUS PERIPHERAL CONTROLLERS TO MORE MAJOR OEMs THAN ANYONE.

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Yet for Multibus™ systems employing 68000, 8086 or Z8000 class microprocessors with large capacity disk and tape drives, no other Multibus controllers offer better performance or more advanced features.

NEW 450 AND 472 CONTROLLERS JOIN POPULAR XYLOGICS 440.

For the past three years, the Xylogics 440 peripheral controller – the industry's first Multibus SMD controller – has offered the highest peripheral control performance in Multibus benchmark tests and customer installations.

Now Xylogics has developed two new advances in Multibus peripheral control: the 450 and 472. Together, they set the standard for price, performance and size for IEEE-796 Multibus applications.

The new Xylogics 450 peripheral controller provides even more performance for Multibus disk control applications. The 450 can address up to 16MB of memory and control up to four SMD disk drives at data rates of up to 1.8 MB/sec. non-interleaved.

The new Xylogics 472 is a high performance, single-board tape controller for streaming and start-stop tape drives. It can address up to 16MB of memory and control up to four tape drives – running at speeds from 12.5 ips to 125 ips and at densities of 800 bpi NRZI, 1600 bpi PE, 3200 bpi, or 6250 bpi GCR.

The 440, 450 and 472 feature advanced channel control techniques and are designed to work together for system optimization. For Multibus users, this means low bus usage, non-interleaved disk operation and true high-speed streaming with no repositioning. All three work with any 16, 20 or 24 bit address Multibus system.

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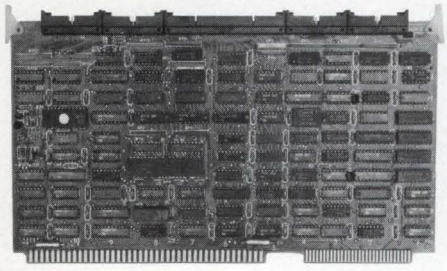
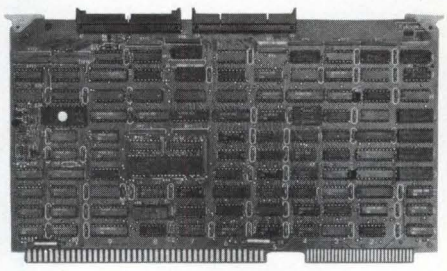
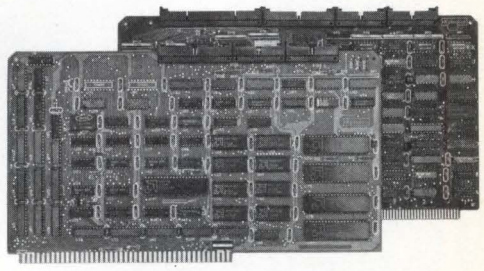


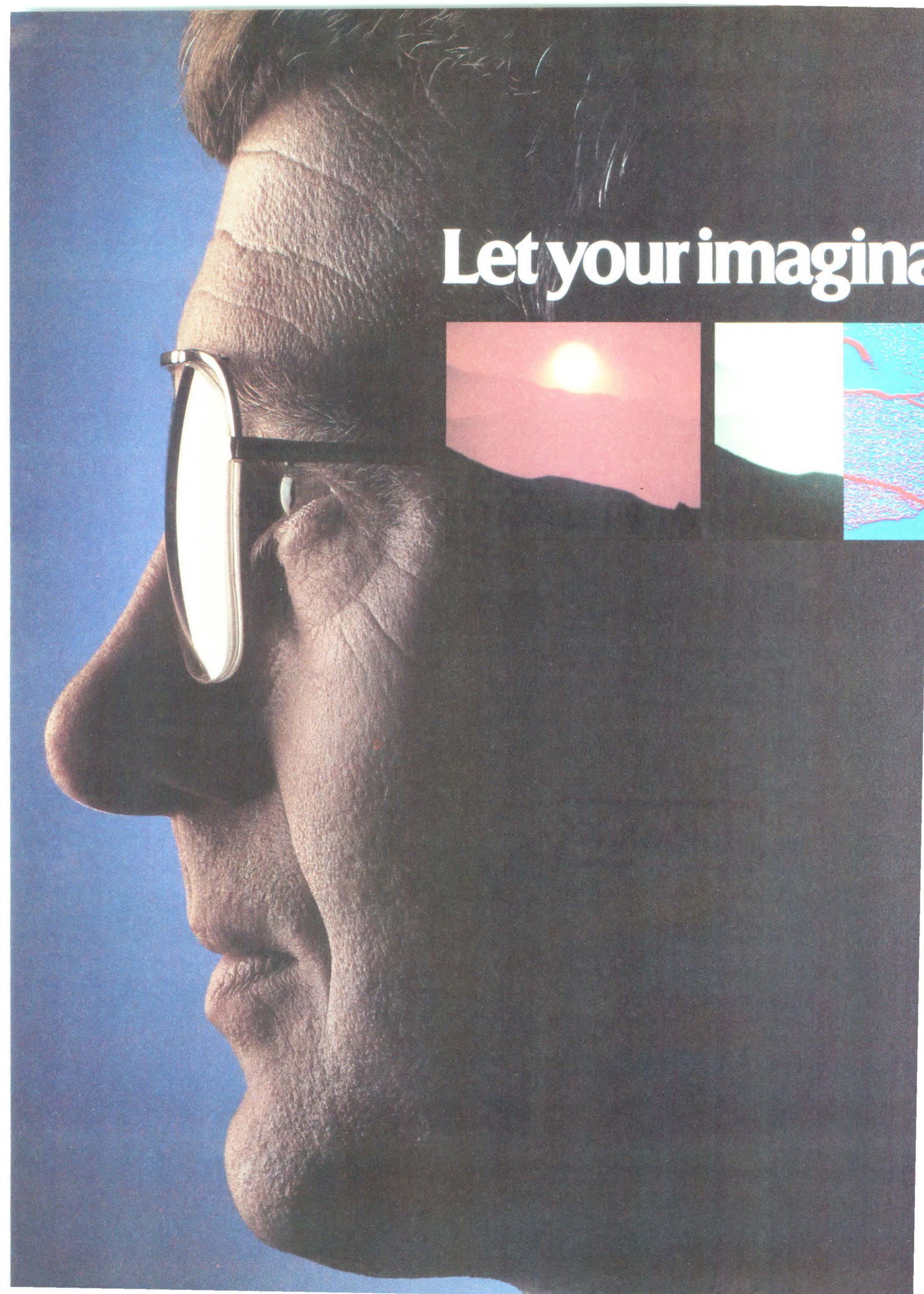
Xylogics 450 Multibus Disk Peripheral Controller.



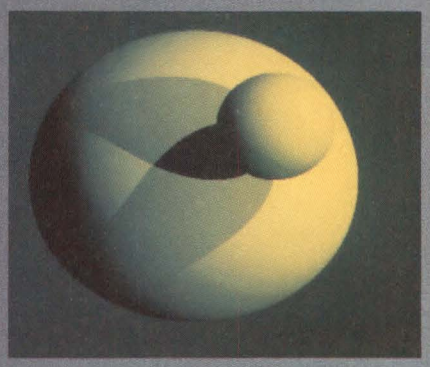
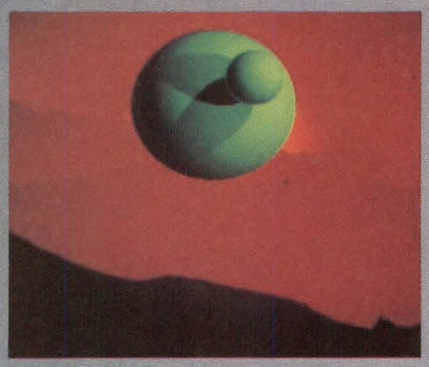
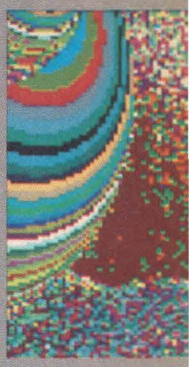
Xylogics 472 Multibus Tape Peripheral Controller.



Xylogics 440 Multibus Disk Peripheral Controller.


Let your imagina

tion run wild, not your budget.

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Because of its unique, modular design, the 2800 System can be sized to your specific needs without sacrificing performance, allowing for multiple, modular processors and controllers for parallel, multi-spectral processing. And each processor is individually programmable, letting you manipulate input, graphics and imaging for simplified operation and maximized throughput.

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GRINNELL SYSTEMS

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CIRCLE 22

WHY MULTIWIRE® THAN MULTILAYER CIRCUIT

Instead of using etched foil for signal conductors, we use computer-generated patterns of insulated wire, laid down by CNC wiring machines to form permanent interconnections.

This difference makes a Multiwire board better than multilayer in four important ways: It permits greater packaging densities. It has better electrical specs. It shortens your design cycle. And it makes board revisions less expensive.

ACHIEVE GREATER PACKAGING DENSITIES AT REDUCED COST

Because our insulated wires can be placed very close together, and even crossed, without problems, Multiwire routinely accommodates component densities of 2.0 IC's per in^2 and greater.

Increased packaging densities reduce the need to interconnect between cards. Fewer cards improve system reliability, and reduce total system costs.

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Multiwire boards require less in-house design time. Our Design Center will design your boards from as little input as a schematic or a net list.

And when you make revisions, you'll get new designs back in days instead of weeks, because the Multiwire CAD system simplifies changes by storing designs on computer tape.

GET SUPERIOR ELECTRICAL PERFORMANCE

Multiwire is superior to etched circuitry for applications that require tight-tolerance, controlled impedance transmission lines.

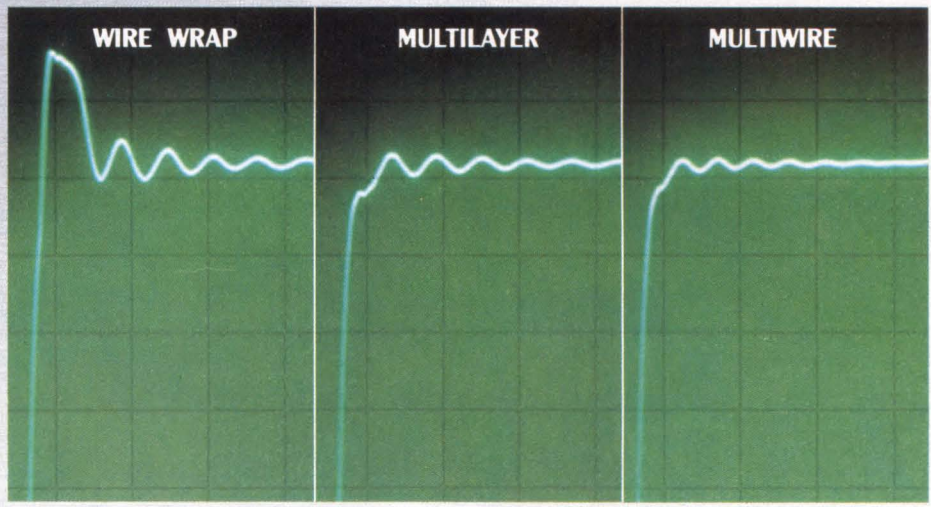
In high-speed, ECL circuits, Multiwire boards outperform multilayer and wire wrap® boards. Greater packaging densities and excellent electrical performance from Multiwire will reduce costs and increase your flexibility in design.

For military applications, Multiwire boards meet IPC-DW-425 (DoD).

SAVE THOUSANDS OF DOLLARS ON REVISIONS

Revising a multilayer board can cost a fortune, because elaborate artmasters must be redrawn for each affected signal level.

Revising a multiwire board, however, is fast. We just key the change into our computer. And save you thousands of dollars.



As these traces show, Multiwire can handle the high speeds of emitter-coupled logic better than multilayer or wire wrap.

IS 4 WAYS BETTER FOR HIGH-DENSITY BOARDS.

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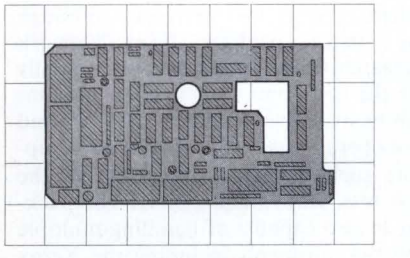
Multiwire technology provides the most advanced high-density, high-performance circuit design. And Multiwire Division is the leader in this technology, serving customers out of its three regional design and manufacturing centers.

But sometimes even our leading edge designs are not enough for your requirements. That's why we have the Advanced Manufacturing Group–a new facility with design and manufacturing specialists dedicated to solving the interconnection problems for your next generation of products.

We'd like to send you our color brochure. It explains the advantages of Multiwire circuit boards in more detail. To receive your free copy, just fill out and return the coupon.



This 4" by 6.8" Multiwire board accommodates a component density of 2.1 IC's per in².

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CD283

CIRCLE 23

Measurement and control system
(continued from page 32)

execution. The host program can perform complex data manipulations while up to 20 realtime measurement and control routines are processing. Switching to single-ground mode clears the processor for very high speed execution. To back this compute power, the package supports transparent memory expansion to 768k bytes of RAM.

Direct transducer connection removes the need for external signal conditioning. Signal integrity is ensured through private analog pathway architecture for vectored analog signal processing and independent digital bus structure. Global signal conditioning and conversion attributes are selected by oncard DIP switches. A precision, high gain instrumentation amplifier with switch-selectable gains to 1000 V/volt provides differential input for low level signals.

Other features include a realtime clock/calendar for time-stamping events, three programmable interval timers, and internal power supplies. Cold-junction reference and amplification allow direct connection of thermocouples.

The complete system integrates hardware and software in a single 12″ x 4.4″ x 10″ (30- x 11.2- x 25-cm) aluminum enclosure, and connects to the Apple computer via standard cable and interface card. Base price for the general purpose System 500, which can be arranged for most combinations of analog and digital input or output, is $2700 (I/O modules priced separately); the other three systems come preconfigured.

System 510, targeted for high performance data acquisition, costs $2900; System 520, for measurement and control, is $4100; and System 530, for high speed, high resolution digitization and generation of complex analog signals, is $4400. **Data Acquisition Systems, Inc**, 349 Congress St, Boston, MA 02210.
Circle 243

SOFTWARE

Ethernet software handles file transfer, remote program execution

A communications package capable of process to process data transfer rates in excess of 100k bytes/s supports file transfer, remote program execution, and electronic mail across any 10M-bit Ethernet local area network. Although the FUSION package from Network Research Corp was developed originally for the UNIX operating system, versions will be available to run on DEC VMS and RSX operating systems as well as to support such disparate processors as the 6800, 8086, VAX-11, and PDP-11. The package is also capable of handling multiple network protocols including the Xerox Network Support (XNS) and DoD's Defense Advanced Research Projects Agency's Transmission Control Protocol/ Internet Protocol (TCP/IP).

A modular architecture implements each of the seven required network levels (physical, link, network, transport, session, presentation, and application) with a socket driver handling the Ethernet board interface (link), network protocol

(continued on page 40)

IEEE-488

Meet the newest members of our family.

The 1720A Instrument Controller has found a home in a wide range of industrial, factory automation and OEM applications. This powerful microcomputer comes complete with floppy disk, touch-sensitive interface, dual IEEE-488 compatible and RS-232-C interfaces along with our FDOS operating system and enhanced BASIC language.

Since then, our family's grown to include a wide range of new products. All designed to complement the 1720A in your instrumentation system.

Here's a look at what's new.

1780A InfoTouch Display.

This RS-232-C compatible touch-sensitive display allows you to fashion a more effective man-machine interface. Use it as a remote display for the 1720A or integrate it into any kind of computer-based system.

External Floppy Disk.

Additional file storage memory is now available for the development of larger programs and extended data acquisition storage. Store up to 800k bytes on double density doublesided disk drives in either a single or double disk unit.

Bubble Memory.

For higher density mass storage, you can't beat bubble memory. And when you add our new Bubble Memory Module to the 1720A, you have up to 512k bytes of non-volatile file storage that operates in a temperature range of 0°C to 50°C. Helpful when working in hostile industrial installations.

We're speaking your language.

The 1720A's getting smarter with the addition of *Compiled* BASIC, Assembly, FORTRAN and now PASCAL software languages. Our software is file-transfer compatible, so you can link Assembly, FORTRAN and BASIC routines into one program using our BASIC call feature. Increasing your programmer's productivity in developing software for ATE systems. And to help document it, we added a new printer and plotter.

We won't stop here.

Fluke has committed a large staff of skilled engineers to developing future enhancements to our Instrument Controller line. So when you choose us, you can be sure we'll continue to expand our capabilities and still stay compatible with what you're planning for the future.

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For technical data circle no. 25

Ethernet software

(continued from page 38)

for data grams and virtual circuits, and operating system interface. The file transfer program handles the session, presentation, and application levels. All that is needed to implement the package is a C compiler with a complete standard I/O library, an operating system capable of task scheduling and interrupt handling, and an available Ethernet interface.

The socket driver is available separately from the file transfer program if a user already has proprietary software to implement on Ethernet. Portability between protocols and operating systems is maintained with separate modules written for each protocol's specific requirements. These requirements pertain to packet encapsulation and decapsulation, establishment of virtual circuits for reliable communications, and operating system requirements for read/write and store operations. Gateways between different networks can be created when a process has access to the sockets (XNS and TCP, for example). The process receives packets from the virtual circuit established on the XNS network and reencapsulates the packets for retransmission on a virtual circuit established with a TCP network.

Because the socket driver handles all network and operating system dependent functions, the file transfer program needs no modifications when moved to different processors. Users execute file transfers, remote program execution, and electronic mail utilities with a command shell similar to that used in UNIX. This specifies the local and remote hosts, the specific commands to be executed, and the local and remote files to be manipulated. For example, the command "cdl dir" changes the local working directory to the home directory on the local computer (used when the working directory is other than that normally associated with the home computer).

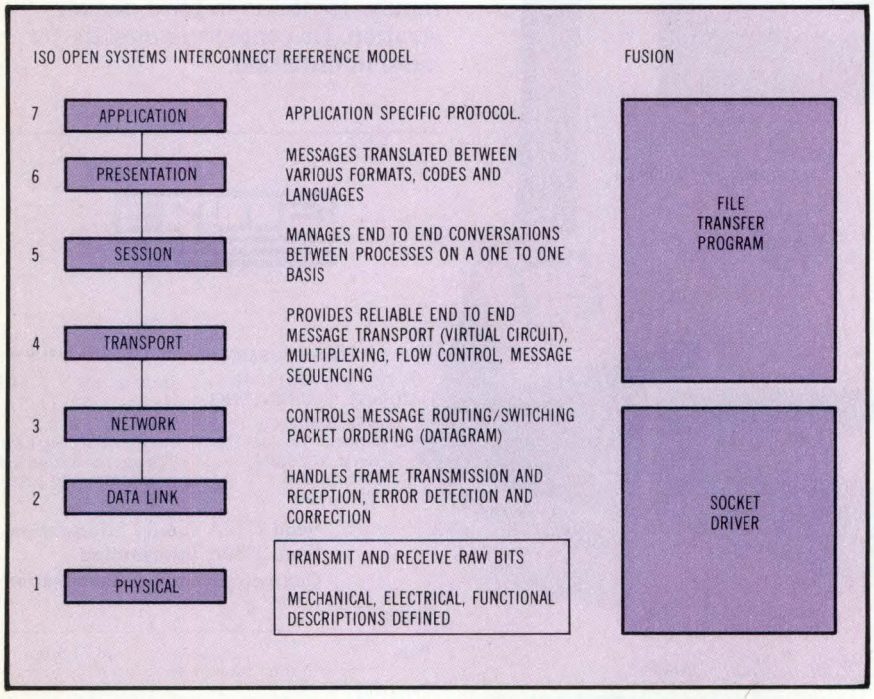
FUSION has two modes of remote program execution, "execr" and "pipe," that allow for the result of the remote command to be the output of the local process, or the output of the remote command can be treated as the input for a local process. During execution of an "execr"command, variable names, environment names, path names, and wild cards (sort keys) are evaluated on the remote host. All characters are typed on the standard input device and passed to the remote host to be provided as input to the remote command. The output of the remote command is then passed back to the standard output device (a printer or plotter, for example).

Pipes, on the other hand, specify local and remote commands to be executed in parallel. Users can specify that the output of the remote command be used as the input of the local command, or that the output of the local command be used as the input of the remote command. The company envisions such capabilities being used to implement distributed parallel processing, with array processors handling matrix manipulations for VAX-11 programmed for electronic logic simulation. Ethernet was selected because of its ability to handle high processor to processor data rates needed for parallel processing.

The FUSION file transfer program is currently available in binary license form at prices ranging from $500. The socket driver is priced from $375 for UNIX versions running on the 68000, to $1750 for VAX-11 systems running VMS. **Network Research Corp,** 1964 Westwood Blvd, Los Angeles, CA 90025.

—Joseph Aseo, Field Editor

Circle 244



Portability for FUSION file transfer program is assured with modular architecture of socket driver that separates code. Network protocol is implemented from board-level interface and operating system interface.

Users design own logic arrays in-house with portable software

To allow logic array customers to specify logic design without concerning themselves with actual circuit layout, Texas Instruments has made available a transportable design utility (TDU) that includes design description languages, high level function libraries, simulators, testability analyzers, and design rule checkers. Initially, the multi-user system will run on DEC VAX-11/780 and IBM 4341 computers, but a version for Data General MV/8000 systems is also planned.

The TDU allows designers to supply a logic description and test vectors without also specifying the actual circuit configuration. This contrasts sharply with other logic array vendors that rely on the customer to generate circuit and logical design. Such vendors usually supply designers with plastic overlays, automated place and route software, or schematic capture packages to help generate masks used to fabricate the desired circuits. In addition, breadboard emulation often serves as the basis for logical and circuit design, as well as a design verification tool when prototypes are fabricated for evaluation. TI claims that such an approach is ineffective when designs reach a complexity in excess of 500 gates, or when more than three circuits are designed in a year, because the extended prototype manufacturing cycle usually involves three to five passes. The company also claims that reliance on discrete breadboards to verify circuit

(continued on page 43)

"Everybody talks about microprocessor support; here's what we're doing to deliver."

Al Carlson,
Engineering Manager,
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INTERFACE PODS FOR FLUKE 9000 SERIES MICRO-SYSTEM TROUBLESHOOTERS

Type	8-Bit	16-Bit	Date Available
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8085	x		Now
Z80	x		Now
6502	x		Now
6800	x		Now
6802 (6802NS/6808)	x		Now
9900		x	Now
8048 (8035/8039 8040/8041/8041A 8042/8049/8050/8741 8741A/8742/8748/8749)	x		Now
8086		x	Now
8088		x	Now
1802 (1804/1805/ 1806)	x		Now
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For technical data circle no. 26

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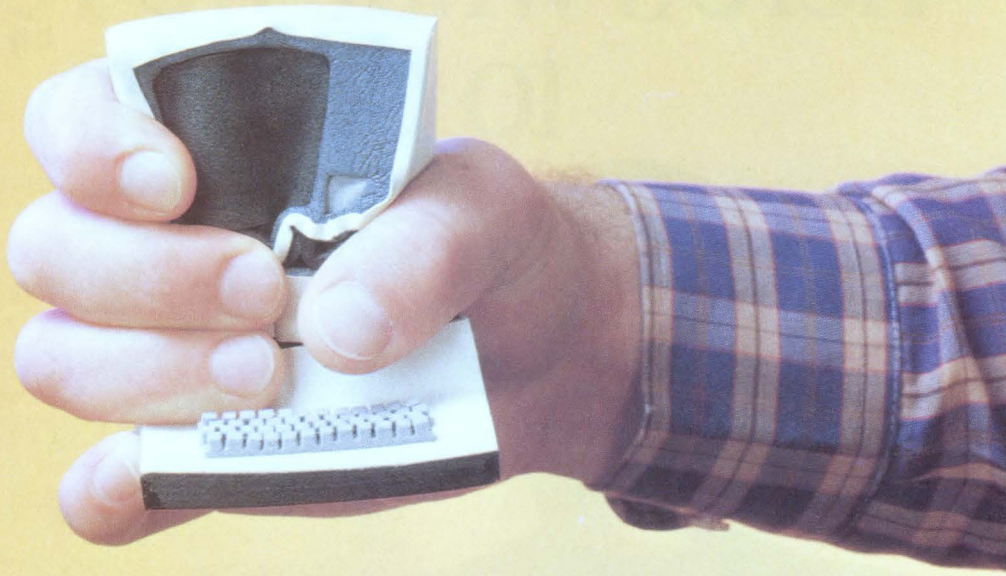

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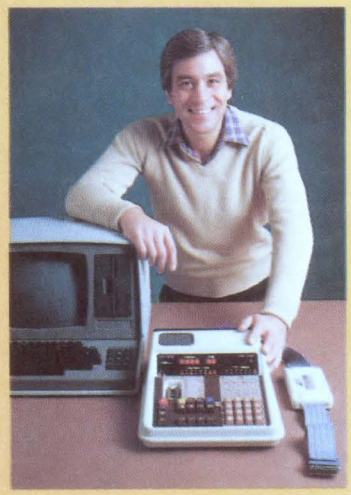
Next time you plug in your CP/M-80 based computer, plug in Applied Microsystems' powerful microprocessor development support. Adding our new Em-Pac* software to one of our EM-Series Diagnostic Emulators will turn your personal computer into a powerful microprocessor development system. With many of the features you'd expect from a system costing three times as much.

Symbolic debugging saves time.

Em-Pac software lets you download and debug software using the same labels and symbols used in the program. Any values, like the one defining breakpoints or memory addresses, can be referenced against the symbol names. This speeds up debugging and reduces the time you spend integrating hardware and software



Microprocessors Supported:

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8039	Z80A
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8049	MK3880A
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	8080A-2

Greater flexibility shortens the engineering schedule.

English language commands simplify the programming process. You can also define a long string of commands for the emulator to execute with only one command. And Applied Microsystems can provide support for the 8048, Z80, 8080 and 8085 familes of microprocessors. So you don't have to learn a completely new system next time you want to change microprocessors.

Find out more . . .

Contact Applied Microsystems for more information on our new CP/M-80 or ISIS-II compatible software. Call us **TOLL FREE** at **800-426-3925,** or write Applied Microsystems, 5020 148th Ave. N.E., P.O. Box 568, Redmond, WA 98052.

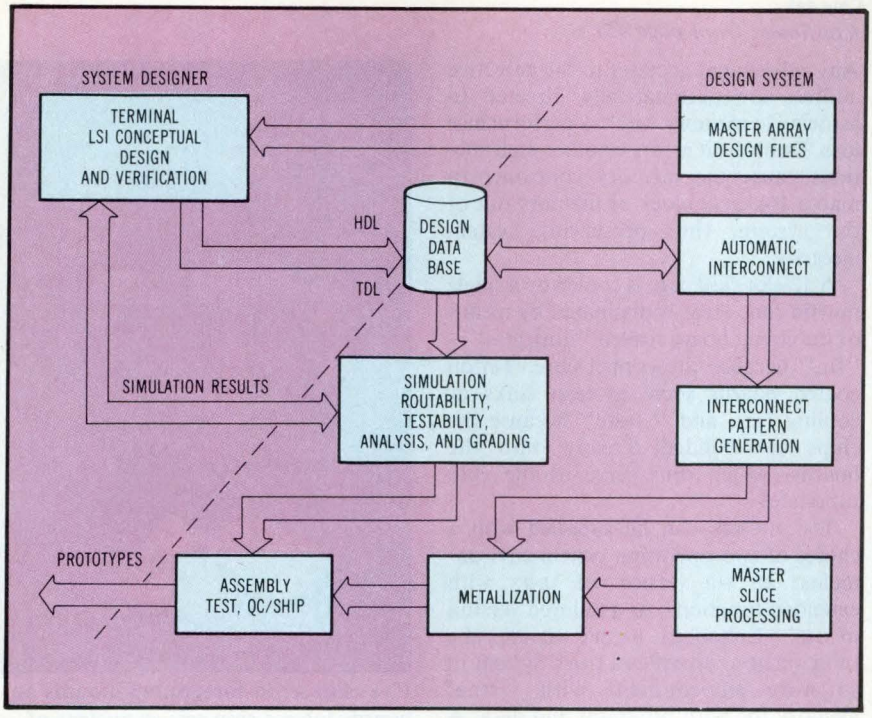
Applied Microsystems

*Em-Pac is a registered trademark of Applied Microsystems Corporation.

CIRCLE 27

Transportable design utility

(continued from page 40)



Common design data base using TI's transportable integrated design automation language (TIDAL) and test description language (TDL) eliminates need for breadboard emulators and extensive prototype fabrication.

design is often troublesome because of the difficulty in duplicating MSI functions and the inability to compare propagation delays across multiple discrete packages with those encountered on a single chip.

Instead, the TDU relies on the transportable integrated design automation language (TIDAL) that serves not only as the hardware description language, but also as the language of many other utilities. TIDAL is written in Wirth-standard Pascal as a hierarchical, block-structured language that allows description in terms of individual system elements (such as transistors and resistors), gate-level functions, MSI functions, or complete systems. A common design data base is created so that both the company and the customer can transfer layout data; electrical, functional and logical descriptions; package requirements; and test data without the fear of conflicting standards.

Besides defining the structure of the design using TIDAL, the designer also specifies test vectors with a test description language, checks that basic design rules are met for the process technology with which the arrays are implemented, and simulates the design by exercising the hardware description. A logic-level simulator used with the software function library describes popular MSI parts in STL logic. Designers can examine the performance of the design, complete with timing data extracted from signal propagations of the test vectors described in test description language (TDL). A simulation control language (SIMCL) provides high level language control of test vectors. A testability analyzer identifies potential problem areas within the design.

When the TIDAL logic design is verified by the customer, the data base can be shipped or transmitted as a remote job entry to the company for automated layout, routing, mask generation, and prototyping. The designer can then resimulate the design, using the actual layout delays for final verification, after place and route have taken place. This eliminates prototype fabrication and breadboard emulation.

The TDU currently supports designs for the TAT004 and TAT008 400- and 800-gate Schottky gate arrays, TAT010 and TAT020 1000- and 2000-gate advanced Schottky arrays, and the TAL002 and TAL004 low power Schottky arrays. Initial price for a 1-year lease is $65,000 with onsite installation, software updates, and user support supplied. Quantity discounts are available. **Texas Instruments,** PO Box 202129, Dallas, TX 75220.

Circle 245

COMPUTERS

Chip set packs power of a mainframe computer

When Hewlett-Packard Co at the 1981 International Solid State Circuits Conference introduced a 5-chip set of super-dense ICs using its NMOS III process, the company gave no hint that the chips had been designed with a specific end product in mind. The ICs have now surfaced in the form of a 32-bit single-user computer, the HP 9000, which is available as a completely integrated desktop workstation, as a rackmounted module, or in a standalone cabinet for building industrial and multi-user systems. Internally, it can be configured with up to three of the 32-bit CPU cards, as well as with one or more I/O processor cards, all of which can be plugged into the system's card cage.

The set includes CPU and clock chips, both on the CPU board; a 128k-bit RAM chip and a memory controller used in the 256k-byte memory boards; and an I/O processor chip. The I/O processor provides eight I/O channels per card with direct memory access (DMA) transactions supported between all channels and the memory processor bus. This chip is microprogrammed with 4.5k 38-bit words of resident control store. In addition to the DMA transactions, it simultaneously handles CPU I/O and generates CPU interrupts.

The 450k transistor CPU chip is a stack oriented processor with 32-bit address and data buses. It handles pipelined data transfers at 36M bytes/s, which is also the bandwidth of the memory processor bus or system backplane. The clock chip generates two nonoverlapping 18-MHz signals to drive the CPU at a 55-ns cycle time. At these speeds the processor is able to execute 1M instructions/s. The 230-opcode instruction set includes instructions for IEEE math formats, multiprocessing, and multiple processors. A typical execution time for a 64-bit floating point multiply is 10.34 μs.

Memory is provided on boards using HP's 128k-bit RAM chip in increments of 256k bytes for a maximum system main memory of 2.5M bytes. Each memory address contains 32 bits for data plus 7 for Hamming codes used by the memory controller to detect and correct single-bit errors and to detect double-bit errors. In addition, the memory controller has a 32-word associative memory for "self-healing" error correction. When it detects single-bit errors, it stores the correct contents in an associative word.

(continued on page 44)

Chip set

(continued from page 43)

Any subsequent accesses to the defective address are automatically directed to associative memory with no performance loss. Double-bit errors or other malfunctions cause the memory controller to map a 16k-byte block of memory out of the system, thus preserving system integrity.

A 12-slot card cage is cooled by a single muffin fan. Heat is dissipated by means of the circuit boards called "finstrates"—"fin" because the copper-core, Teflon coated boards serve as heat sinks or cooling fins, and "strate" because the chips are bonded directly onto the boards, which thus serve as the chip substrate.

The HP 9000 can be supplied with a choice of two operating system environments: an HP version of UNIX with extended functions, or a tailored version of HP's Enhanced BASIC. HP-UX, the UNIX version, provides a UNIX System III software environment with virtual memory for both programs and data. A maximum virtual address space of 1G byte can be allocated per process with up to 500M bytes of that space available for local code and data, and up to 500M bytes for shared system code. In addition to FORTRAN and Pascal, HP-UX supports the Graphics/9000 family of display and design graphics.

A device-independent graphics language provides fundamental graphics functionality, output primitives, and color modeling. An advanced graphics package incorporates ACM Siggraph Core compatibility, 2- and 3-D viewing, and clipping. Picture segment support with an "operator pick input" function allows interactive manipulation of graphics images.

An Enhanced BASIC language system provides a single-user operating system environment with multiprogramming and job scheduling. BASIC includes both an interactive editor and extensions aimed at engineering activity. BASIC is implemented as a runtime compiler. Running a program in source code initiates line by line compilation, and only the first iteration of a loop is compiled—thereafter, the loop's source code is executed. After compilation both source and object code remain in memory so that the user can interactively debug the program. Source and object can then be separately stored, and the object code alone can be later loaded and run if desired. The BASIC system also supports a 3-D color graphics system as well as the same IMAGE/QUERY database management system that runs on HP 3000, 1000, 250, and 9845 computers.

Five-chip set in foreground mounts on boards (above chip set) as nucleus of 32-bit HP 9000 computer. Module in center is rackmounted version; background unit is standalone workstation.

The HP 9000 system is designed to put 32-bit mainframe computations into an individual workstation. It is also configurable within the card cage for CPU, memory, or I/O intensive applications. In addition, the card cage can be packaged in the OEM desktop model 20, which includes keyboard, floppy and/or hard disk storage, and monochrome or color CRT, and is priced starting at $28,250. The card cage can also be packaged in the OEM rackmounted model 30 and the minicabinet packaged model 40. A model 40 with 1M-byte RAM, single CPU, and multi-user HP-UX operating system is priced under $45,000. Contact local **Hewlett-Packard** sales offices.

—Thomas Williams
West Coast Managing Editor

Circle 246

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

MAKING THE LEADING EDGE WORK FOR YOU

Introducing a brainy new solution from the Wizards of Winchester Disk Controllers.

A new Winchester controller. Plus floppy controller. On one low cost board. Small enough to mount atop a 5¼" drive. And ST500/SA1000 compatible. "Smart," you say? What did you expect from the Wizards of Winchester Disk Controllers?

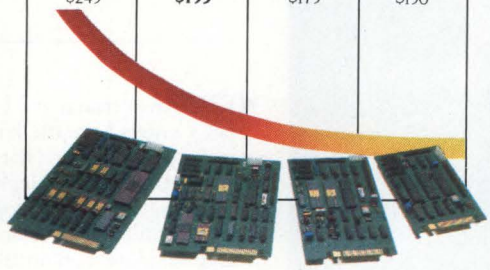
We promised you more for less. Our new WD1002 delivers. At $195 (U.S. OEM quantities) it's $50 less than its predecessor, the WD1001.

The big news, though, is that we've made the WD1002 the brainiest disk controller yet, with an abundance of new LSI innovations. Such as our WD1010 single-chip Winchester controller device. It replaces the microprocessor on our earlier boards. And about 25 other devices. Plus we've added the new WD1014 Error Correction device and the WD1015 Buffer Manager device.

Because just about every system with a Winchester has a floppy nearby, we included our new WD279X single chip floppy disk controller, too. So you get a complete, powerful solution on one reliable 5¾" x 8" board. And you're on the upgrade path to our upcoming WD1003 and WD1004 boards.

U.S. OEM Quantities

WD1001	**WD1002**	WD1003	WD1004
Summer '82	**NOW**	Summer '83	Fall '83
$245	**$195**	$175	$150

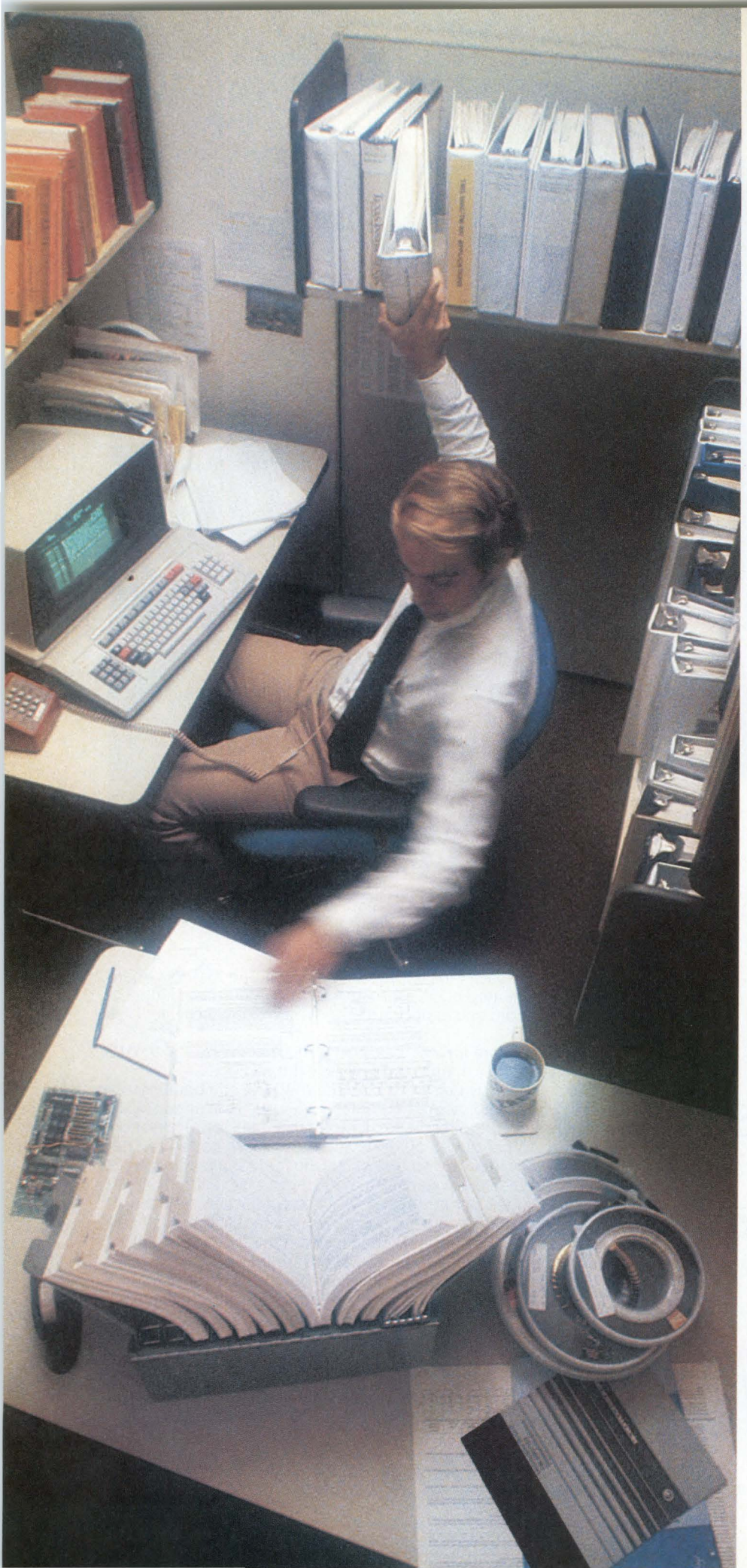


To make our disk controllers even more irresistible, we'll customize them to your bus and form factor. Or sell you our LSI, along with everything you need to build a controller yourself.

It doesn't take too much brains to see that it's safe, smart and simple to commit your disk-based systems to WD. Call our controller hotline, 714/966-7827 and we'll arrange to sit down with you and get into the details you need.

WESTERN DIGITAL
CORPORATION

Components Group, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550



No. 1 in a series:

When are

Whenever you need highly specialized logic structures at near-standard prices. At Texas Instruments, off-the-shelf master logic arrays — a collection of uncommitted gates — can be rapidly and economically transformed into your specific interconnect pattern by an advanced design automation system.

In determining when and if logic arrays are feasible for your needs, many questions, like the following, will require answers. From whom? The Answermen at TI's Regional Technology Centers (RTCs). Expert. Experienced. And conveniently accessible by telephone or in person.

Texas Instruments Worldwide Regional Technology Centers

ATLANTA (404) 452-4686	3300 N.E. Expressway, Bldg. 8 Atlanta, GA 30341
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HANNOVER, WEST GERMANY 0511/643021	Kirchhorsterstr Str 2 3000 Hannover 51
TOKYO, JAPAN 03 - 498 - 2111	Aoyama Fuji Bldg. 6-12, Kita Aoyama 3 Chome Minato-Ku, Tokyo

◀**RTC Answermen** at TI Regional Technology Centers have the knowledge as well as resources at hand to handle many logic array questions by telephone. The strategically located technology centers are also your readily available access to the courses and seminars, demonstrations, laboratories, development systems, and consultation that will help you find the right TI semiconductor solution for you.

Ask the RTC Answermen at Texas Instruments

Logic arrays logical for me?

What major factors determine whether fully custom logic or logic arrays is the best way for me to go?

Early in your deliberations, two factors will indicate whether or not you should proceed. One is how quickly you need to get to market. If you want to move fast, TI logic arrays can cut your design cycle by as much as 25 percent. TI currently delivers prototypes 12 to 14 weeks after the design is initiated.

Another factor is the size of your run. If your volume requirements will not bring the cost of a totally custom design within reason, logic arrays from TI can cut your design costs by as much as 30 percent.

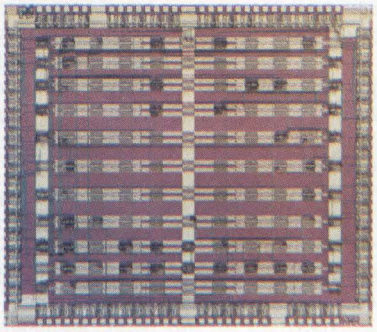
The key to these savings is TI's comprehensive design and layout automation system that allows you quickly and accurately to specify your logic and completely simulate the design in advance of production.

Before I get in too deep, can I get an advance idea of how many gates I'll need to do the job I want?

Yes. TI's software library of macro functions is available to help you estimate the number of gates you'll need.

If you want a more precise estimate, you can send us a schematic for evaluation at no charge.

We'll get back to you with a recommendation of which TI logic array best fits your needs (see table below) and a suggestion for the type of package.



Newest addition to TI's logic array family is the high-performance TAT020 master array. Fabricated using Advanced Schottky Transistor Logic, the TAT020 offers an outstanding combination of power, speed, and density.

Can I determine if my design will perform correctly before prototyping?

At Texas Instruments, our goal is first-pass success. Our integrated design automation system minimizes the need for redesigns by eliminating many manual, error-prone design techniques. Using our Hardware Description Language (HDL) and Test Description Language (TDL), you can describe your logic and build a computer model. You can run a simulation routine as a test, and check the design for timing and functionality, even apply a set of inputs and watch them propagate through the entire model. Once you give an okay, we'll partition the logic and make all the routing interconnects automatically. Then we run verification software comparing a schematic analysis against your model — actually a transistor-by-transistor, resistor-by-resistor verification.

What help are you prepared to supply in getting me to the point of a computer model?

We're on your team, and we make our design automation capability convenient and simple to use.

We hold a five-day technical design course where you'll learn the performance characteristics of our master arrays. You'll also learn how to use the various design software tools. These tools, which screen out most problems, include HDL and TDL as well as a design for testability. Other tools available to you include advanced simulation, design rule checking, design verification, and test pattern grading.

Where can I get this help?

At TI's Regional Technology Centers. That's where each RTC Answerman is located and where you'll find the applications engineers who will assist you with your logic arrays. The technical design course is taught at these centers. And each has terminals where you can input your design description directly into our software system.

If more convenient for you, you can come to our plant for logic array design and applications help, or we'll come to yours.

For fast answers to more of your technical questions about logic arrays, call the Answermen at the Hot Line numbers on the opposite page. Or visit the Regional Technology Center nearest you, or call your local TI sales engineer. For our Logic Array brochure, write Texas Instruments, P.O. Box 202129, Dallas, Texas 75220.

Fast, Efficient TI Logic Array Family

Array	Gates**	Technology†	Gate Delay	Gate Power	I/O Signals
TAL002*	280	LPS	5.0 ns	1.25 mW	29
TAL004*	400	LPS	5.0 ns	1.25 mW	42
TAT004	400	STL	2.5 ns	600 μW	76
TAT008	800	STL	2.5 ns	600 μW	104
TAT010	1000	ASTL	1.0 ns	300 μW	88
TAT020	2000	ASTL	1.0 ns	300 μW	120

*TAL Series Arrays are manually routed by you and schematically verified by TI with your software HDL model prior to prototyping.

**Usable gates

†LPS — Low-power Schottky

†STL — Schottky Transistor Logic

†ASTL — Advanced Schottky Transistor Logic

MIL versions of all these logic arrays are available from Texas Instruments.

TEXAS INSTRUMENTS

27-5605A

CIRCLE 30

Entry level 32-bit minicomputer fills industrial automation needs

Striking a competitive stance in the low end 32-bit market, Data General's Eclipse MV/4000 supplies performance of 600k Whetstones to best comparably priced systems. The system runs under AOS/VS for multi-user applications or under AOS/RT32 for dedicated realtime jobs, and supports 8M-byte main memory with up to 4.7G bytes of online storage.

Made up of a 2-board CPU, memory, I/O controllers, and power supply, the computer is housed in a compact 1-m high cabinet or in a rackmount chassis. Its 32-bit microprogrammed architecture provides a 4G-byte logical address space, segmented memory with ring protection, and the Eclipse instruction set with 32-bit data manipulation and self-diagnostic features. Implemented using gate array and programmed array logic technology, the unit supplies additional features while retaining compatibility with existing 16- and 32-bit systems and software.

The design puts system control unit (SCU) and system processor unit (SPU) on two boards. The microsequencer within the SCU contains control store and logic to control program flow through the CPU. The SCU also handles memory refresh and error correction. The SPU contains arithmetic logic unit, address translation unit, scratchpad, and input/output controller. Basic arithmetic functions, translation between logical and physical addresses, and I/O implementation are done here. Also on the processor boards are ROM-based powerup diagnostics. Providing the functionality of the system control processor and diagnostic bus used on larger MV/8000 and /6000 systems, diagnostics and error logging are controlled by a microcoded soft console.

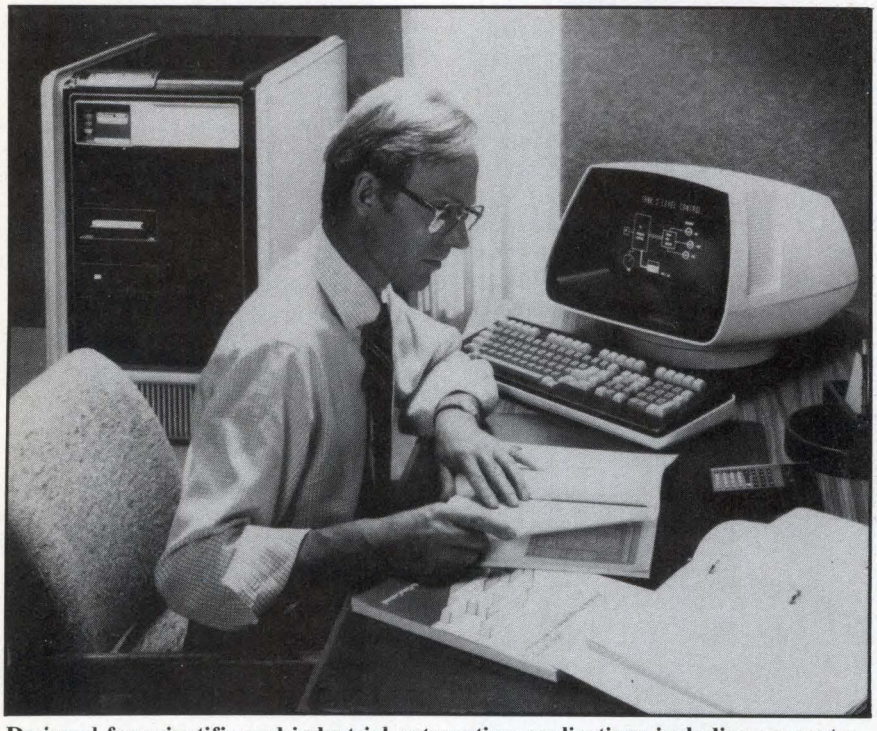
Transfers between CPU and memory occur at 10M bytes/s. A high speed burst multiplexer channel provides direct memory to device transfers at 5M bytes/s and a medium speed data channel carries data to and from intelligent network and communications interfaces. Intelligent synchronous and asynchronous controllers improve system performance by offloading the CPU. With nine available I/O slots, systems can be configured to meet specific needs.

The system's optional floating point unit accelerates both single- and double-precision calculations, performing up to 600k Whetstone instructions/s. A microcoded processor within this unit operates serially with the CPU to increase performance. 16k bytes of writable control store speeds commonly used software routines. It can also be used to define additional instructions and further enhance the instruction set, adding performance in dedicated applications.

An intelligent synchronous communications controller (ISC/2), introduced concurrently, incorporates a micro-Eclipse microprocessor with 128k bytes of onboard memory. This board makes RS-232, -449/-432A, and -422A interfaces hardware selectable. It provides two synchronous lines supporting binary synchronous communications, synchronous data link control, or high level data link control. Asynchronous line control is provided by intelligent asynchronous controllers.

A basic MV/4000 with 1M-byte main memory sells for $27,500 in single units. Quantity discounts are available. **Data General Corp,** Rt 9, Westboro, MA 01581.

Circle 247



Designed for scientific and industrial automation applications including computer aided design and manufacturing, supervisory control, and medical instrumentation, Data General's 32-bit Eclipse MV/4000 runs under AOS/RT32 realtime operating system or compatible AOS/VS multi-user virtual operating system.

DATA COMMUNICATIONS

Ultrafast data transmission outfit operates full duplex with 95% transfer efficiency

A multihop satellite data transmission system sends bulk data point to point over terrestrial, satellite, or mixed communication media at rates to 6.3M bps. Bunker Ramo's BR 1720 has overcome database and distribution problems usually associated with the 45,000-mi satellite signal path delay at speeds over 56k bps with a proprietary communication protocol. By cutting bit error rate to under one in 10^{12}, the protocol makes it possible for distant computer sites to communicate as if they are adjacent.

The satellite link protocol (SLP) was developed specifically for long-haul communications at multimegabit rates. Continuous-class characteristics provide efficiencies that are independent of both round-trip delay and data rate. SLP also provides high efficiency over noisy terrestrial circuits and over high-band satellite links that are sensitive to heavy rain and snow conditions. In clear conditions with bit error probabilities of one in 10^{-7}, SLP achieves over 95% transfer efficiency.

The protocol supports full-duplex transfer rates for 2- and 3-hop satellite

(continued on page 54)

METHEUS OEM GRAPHICS

392 FEWER THINGS TO GO WRONG

The Metheus Ω400 Display Controller gives you 1024 × 768 pixel resolution, one million pixels/second vector drawing speed, choice of 4 or 8 bit planes, plus a full complement of graphics features.

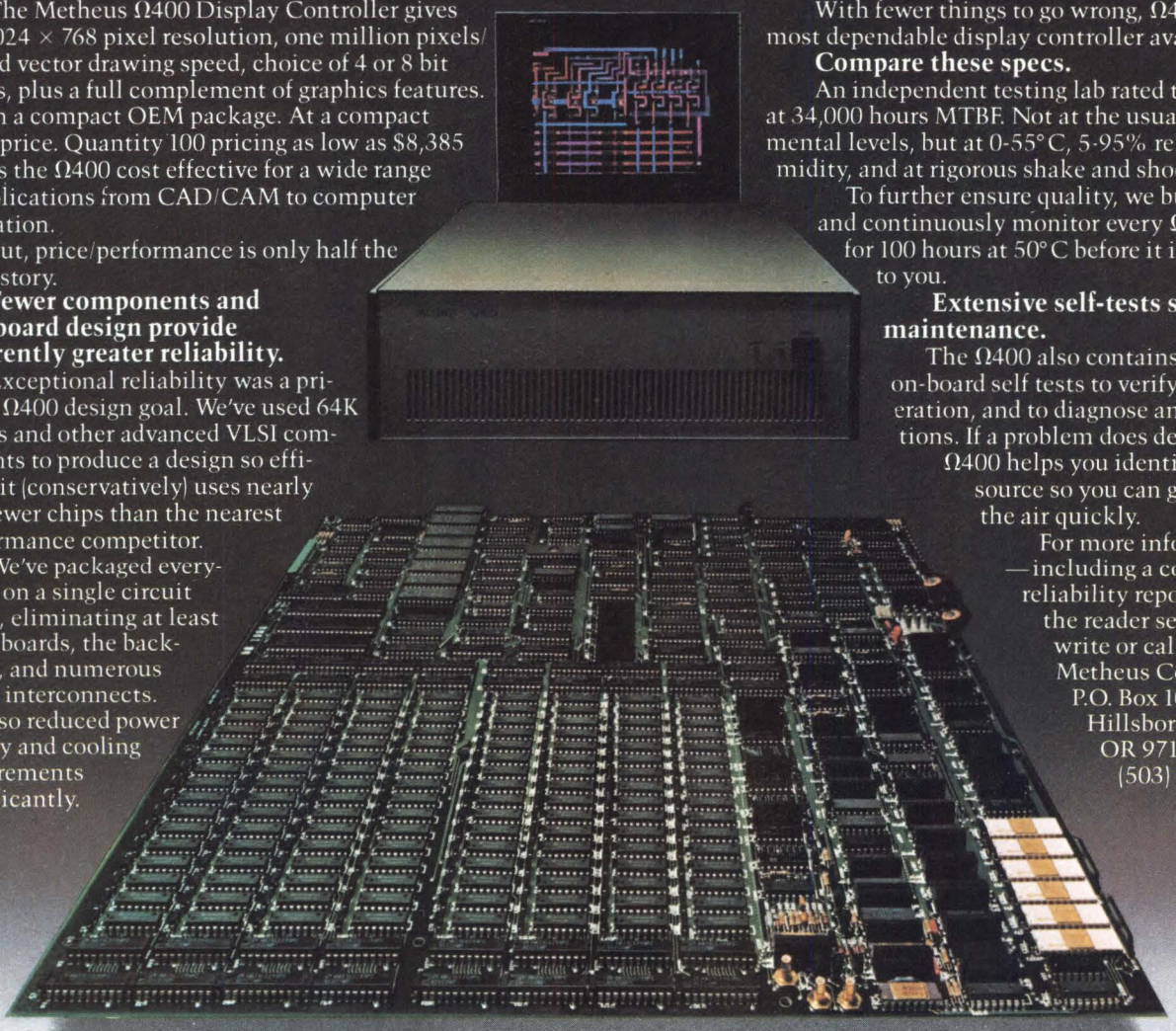
In a compact OEM package. At a compact OEM price. Quantity 100 pricing as low as $8,385 makes the Ω400 cost effective for a wide range of applications from CAD/CAM to computer animation.

But, price/performance is only half the Ω400 story.

Fewer components and one-board design provide inherently greater reliability.

Exceptional reliability was a primary Ω400 design goal. We've used 64K RAMs and other advanced VLSI components to produce a design so efficient it (conservatively) uses nearly 400 fewer chips than the nearest performance competitor.

We've packaged everything on a single circuit board, eliminating at least three boards, the backplane, and numerous board interconnects. We also reduced power supply and cooling requirements significantly.



With fewer things to go wrong, Ω400 is the most dependable display controller available.

Compare these specs.

An independent testing lab rated the Ω400 at 34,000 hours MTBF. Not at the usual environmental levels, but at 0-55°C, 5-95% relative humidity, and at rigorous shake and shock levels.

To further ensure quality, we burn-in and continuously monitor every Ω400 for 100 hours at 50°C before it is shipped to you.

Extensive self-tests simplify maintenance.

The Ω400 also contains extensive on-board self tests to verify proper operation, and to diagnose any malfunctions. If a problem does develop, the Ω400 helps you identify the source so you can get back on the air quickly.

For more information —including a copy of our reliability report—use the reader service card, write or call.

Metheus Corporation,
P.O. Box 1049,
Hillsboro,
OR 97123.
(503) 640-8000.

METHEUS

Dependable by Design

CIRCLE 31

YOU CAN'T CO
YOU'VE GOT NO

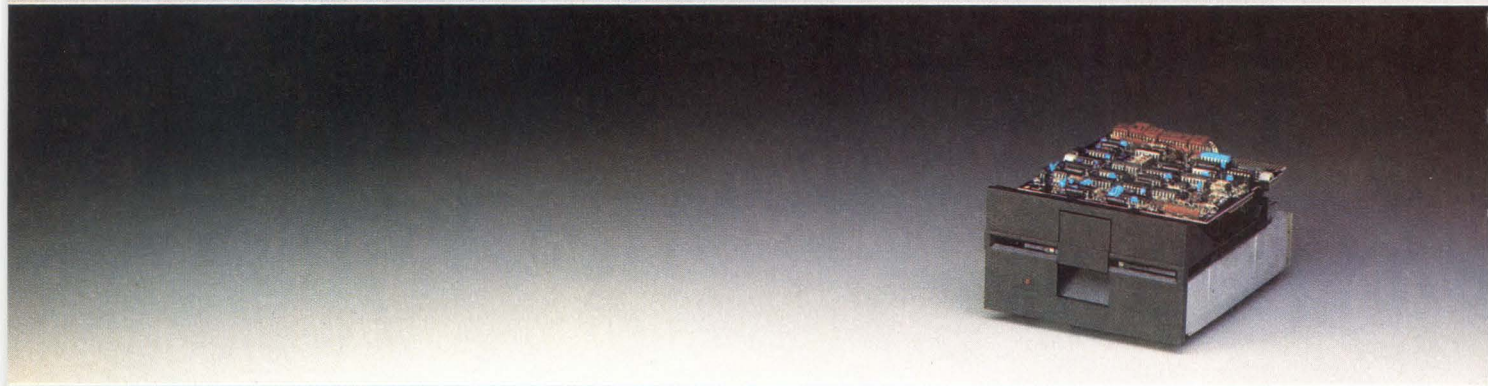
That's quite a claim. How can we make it? Quite simply, because no one else is trying to do what we've set out to do.

In the words of our President, Sirjang Lal Tandon: "Tandon Corporation has been built on a strategy of producing high performance microcomputer peripherals at prices so low that they increase the markets for the computers themselves. If we can help the computer industry create a reliable

To start with, we make more of what goes into our drives than any other manufacturer. 80% of the cost of every drive consists of parts we actually make ourselves.

This assures that we can control the quality of each critical component to our own high-level specifications.

It also allows us to engineer advanced designs from the start that lend themselves to more efficient mass production and higher overall performance.



$200 or $300 'home' system with meaningful capacity—not just a game or toy—most households will be able to afford one. Then we will see a real mass market.

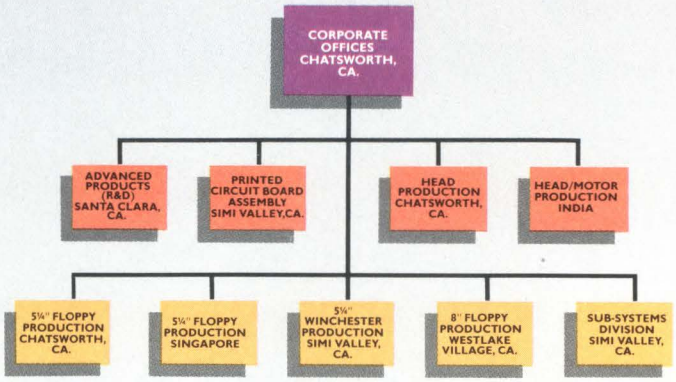
"At the upper end, if we can give small business and personal computers 10 to 50 times their current memory/storage capabilities at a practical cost, we will enlarge the market for more sophisticated desktop systems, and of course, our own market as well."

To accomplish this, we have designed and organized our business unlike all other disk drive manufacturers' businesses.

How?

We make sure that our production capabilities exceed our orders by at least 50% so we are always in a position to deliver.

And we use separate production facilities for each of our product lines,



Tandon Corporation. 20320 Prairie, Chatsworth, CA 91311, (213) 993-6644, TWX: 910-494-1721, Telex: 194794. Regional Sales Offices: Woburn, MA (
(312) 530-7401 · Plano, TX (214) 423-6260 · Irvine, CA (714) 675-2928 · Sunnyvale, CA (408) 745-6303 · Kelsterbach, West Germany (6107) 2091, Te

MPETE WHEN COMPETITION.

keeping their individual priorities distinct to further increase productivity and, ultimately, throughput.

We also offer our customers the most generous guarantee in the industry, to back up the reliability we've achieved.

And finally, we offer our customers a very broad line of drives—16 models in all. So we're the single source that can meet almost any need.

Has it worked?

You decide. In three short years we've become the world leader in small disk drives, shipping more 5¼" floppies, high capacity Winchesters and 8" ThinLine™ floppies than anyone else.

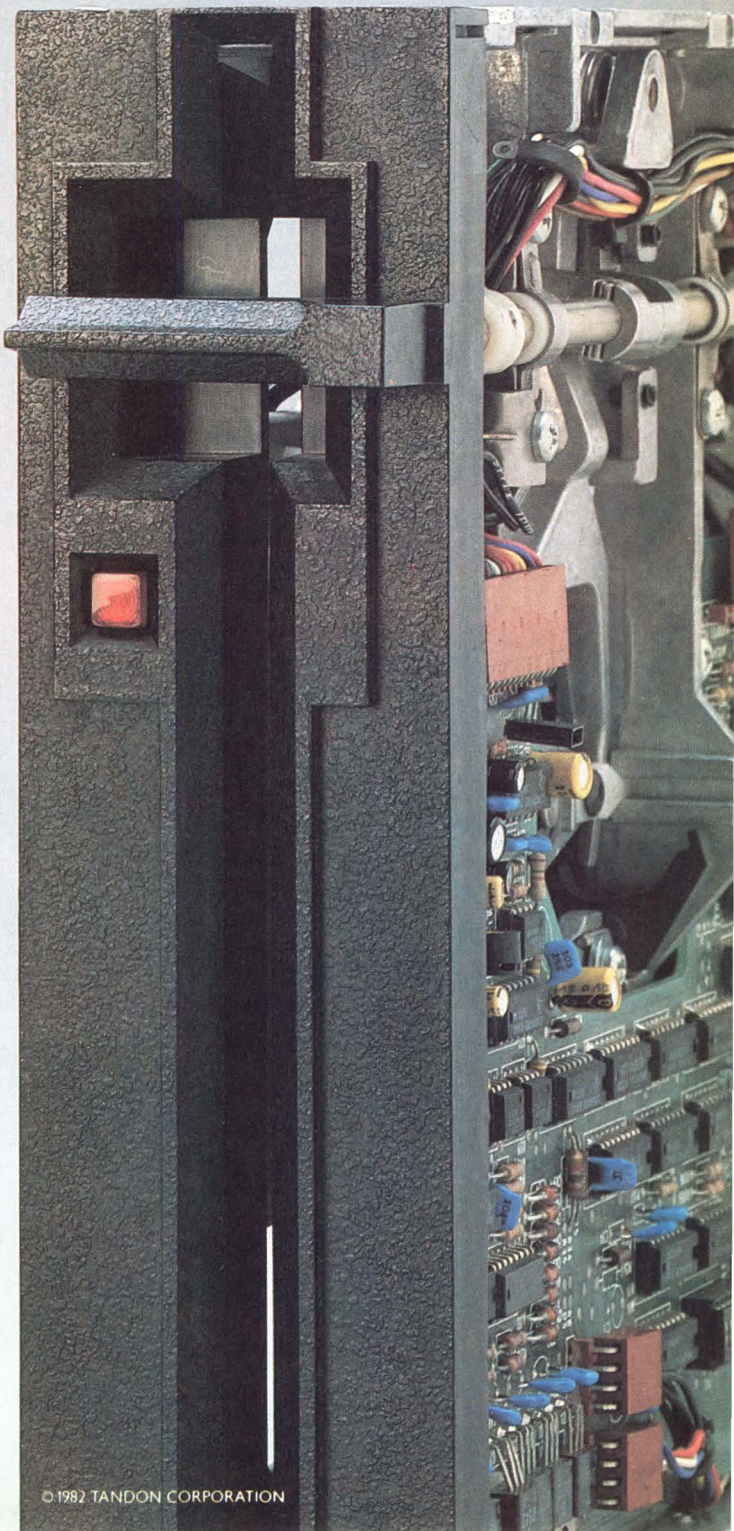
And now we're introducing five new floppy and Winchester drives that push prices lower and capacities higher than the industry has ever seen.

That's why we say we're not competing in the disk drive business.

Times have changed. Three years ago, Tandon wasn't considered competition.

Now we don't consider the competition.

ThinLine is a trademark of Tandon Corporation.



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THE MOST SUCCESSFUL DISK DRIVE COMPANY YOU EVER HEARD OF.

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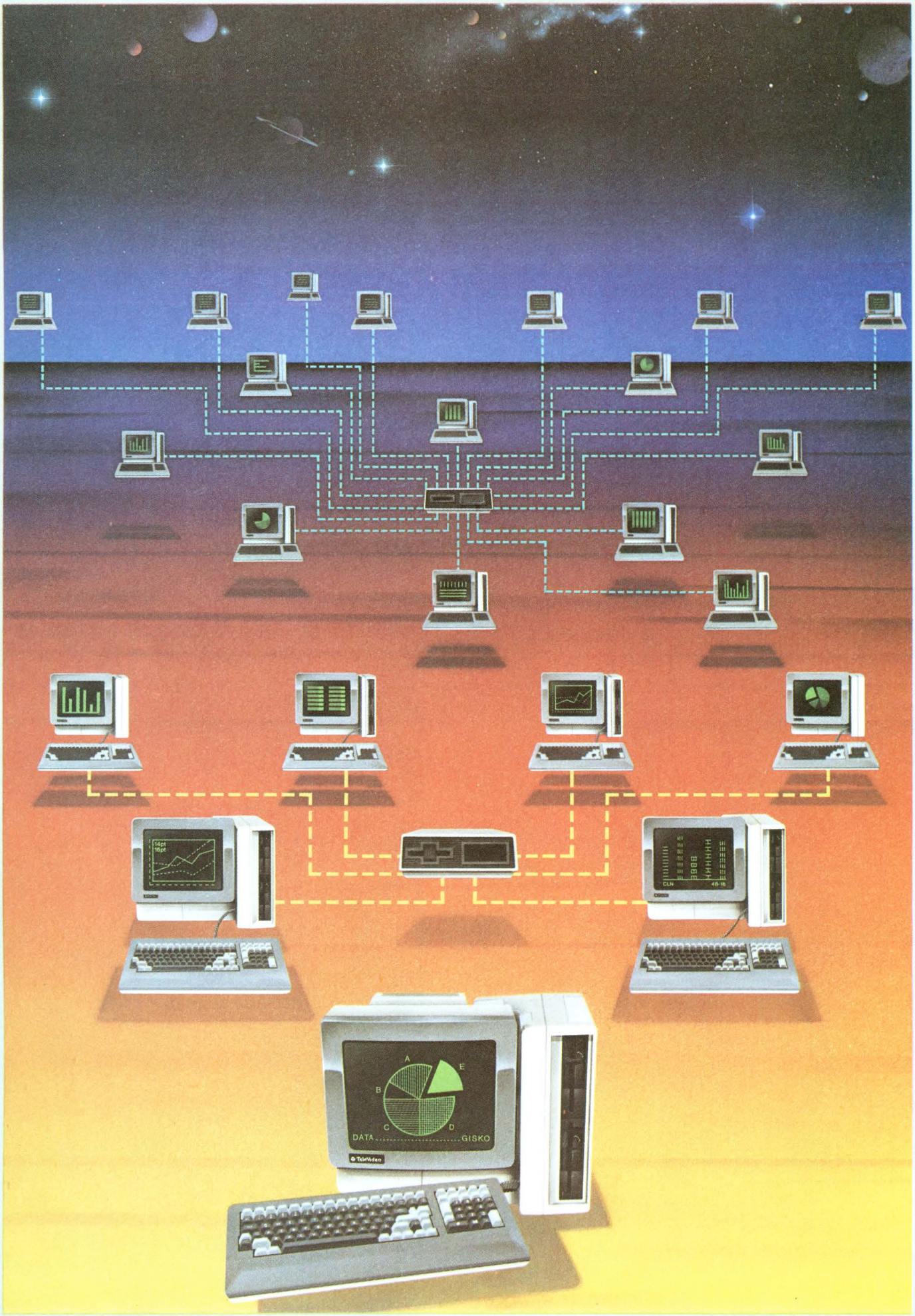
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TeleVideo

Of all the small business computers you can choose today, Televideo gives you more choices for tomorrow.

Any TeleVideo desktop computer can be used as a single-user, stand alone computer. Then, when you want to expand its professional performance capabilities, you have a choice of ways to grow into a multi-user system of up to sixteen TeleVideo computers. You can use our 8 or 16-bit computers, or any combination, starting with your original unit.

TeleVideo also gives you more choices of professional CP/M® software, including advanced graphics. And, thanks to TeleVideo's unique MmmOST™ executive program, the software used on your single-user computers will run on any TeleVideo multi-user system without modification. So if you want a small business computer that gives you professional performance, it's obvious that you have a lot of choices for today.

But there's only one with choices for tomorrow. TeleVideo.

For more information, write TeleVideo Systems, Inc., 1170 Morse Ave., Sunnyvale, CA 94086, call toll-free 800-538-1780 (in California call 408-745-7760), call one of our authorized distributors or dealers, or contact one of our regional sales offices, listed below.

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Eastern Region, 212-308-0705.
Southeast Region, 404-447-1231.
Midwest Region, 312-969-0112.
South Central Region, 214-258-6776.
Northwest Region, 408-745-7760.
Southwest Region, 714-752-9488.
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TeleVideo Systems, Inc.

CP/M is a registered trademark of Digital Research, Inc

CIRCLE 33

MmmOST is a trademark of TeleVideo Systems, Inc

Data transmission system

(continued from page 48)

links at up to 1.544M bps, and 1-hop links up to 3.152M bps. Simplex transmissions race up to 6.312M bps over a 1-hop link. Auto-dial and auto-answer with password protection function on switched wideband circuits or links.

Large amounts of data are called into play to attain the system's remarkable speed and efficiency, however. Up to 768k bytes can be consumed to store transmitted data while waiting for acknowledgment that it accurately reached the receiving data station. For example, there is about 0.33 s of delay each time a data block is transmitted from an earth station to a satellite 22,300 mi away, then back to another earth station. Another 0.33 s is spent getting the "received OK" message back to the sending BR 1720. At 6.3M bps, this 0.67 s stacks up 4.2M bits, or about 500k bytes of memory.

The BR 1720 operates in four modes: tape to tape, tape to CPU, CPU to tape, and CPU to CPU. During online computer operations, the transmission system appears to the host computer as an IBM 3803-2 tape controller with up to seven IBM 3420-8 tape drives. Alternately, the host can use standard copy utilities to transfer data from its local mass storage devices through the BR 1720 system to a remote computer and its devices or directly to remote offline tapes.

For completely automated communication, one of the seven drives is dedicated to host control as a command port; the other six can be used for the data transfers. In addition, the system can provide standalone tape to tape transfers of multivolume, multifile IBM standard labeled tapes at 6.3M bps. At that rate, the BR 1720 will copy 2400′ (732 m) of magnetic tape in 4 min; the same job takes a 19.2k-bps system 22 h.

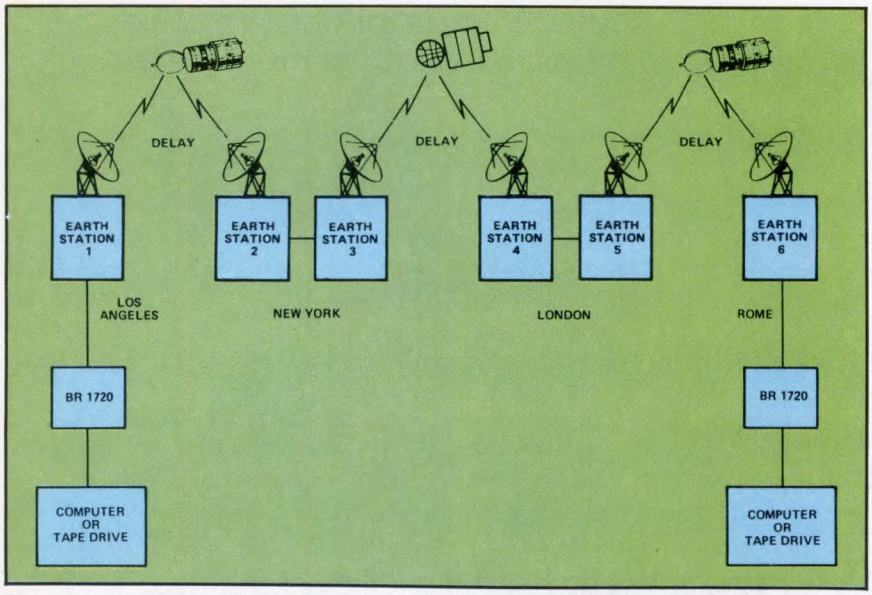
When acting as a communication multiplexer, the BR 1720 furnishes six simplex data paths and one full-duplex priority subpath through a single wideband communication link. All ports can be assigned independently as send or receive. The full-duplex subpath, permanently assigned port zero in each unit, supports transfer of control information and operator to operator messages between units.

Accuracy and speed of the system bring several attractive earthbound applications to mind. One is load leveling, to prevent underutilization of one computer center while another's work load exceeds capacity. Another is the role of intercomputer gateway, to transmit data locally or remotely at computer room speeds between two incompatible computers. In addition, the BR 1720 can raise design productivity in high speed transmission of dense graphics files; it will transfer a 1k- x 1k-pixel file in 1 s, with remote or local database access.

The complete outfit consists of an operator terminal with cassette loader for the proprietary software that loads into a 5.5″ (13.9-cm) high data exchange controller, the nucleus of the system. A statistical printer records data transfer details. The data exchange controller provides the hardware link between computer equipment and the local ground satellite station via RS-449/422, CCITT V.35, or Bell 306 interface. Host computer/high speed peripherals connect via an IBM 360, 370, 303X, or 43XX CPU block multiplexer interface.

Commands entered through the operator's console initiate, perform, and terminate a bulk data transmission. When transmission completes, the system automatically disconnects the data link for rapid reallocation to waiting calls. The system hooks up to a host CPU without altering existing software. One BR 1720 system costs $96,500; delivery is 45 days ARO. **Bunker Ramo Electronic Systems, an Allied Co**, 31717 La Tienda Dr, Westlake Village, CA 91359.

Circle 248



Two-site installation of Bunker Ramo's BR 1720 satellite data transmission system. A data block flows from computer or tape drive to first BR 1720, where it is stored until accurately received at the other end. Two- or 3-hop situation is treated as a single hop with longer delay.

Hardware interface links RS-232 ports to Ethernet networks

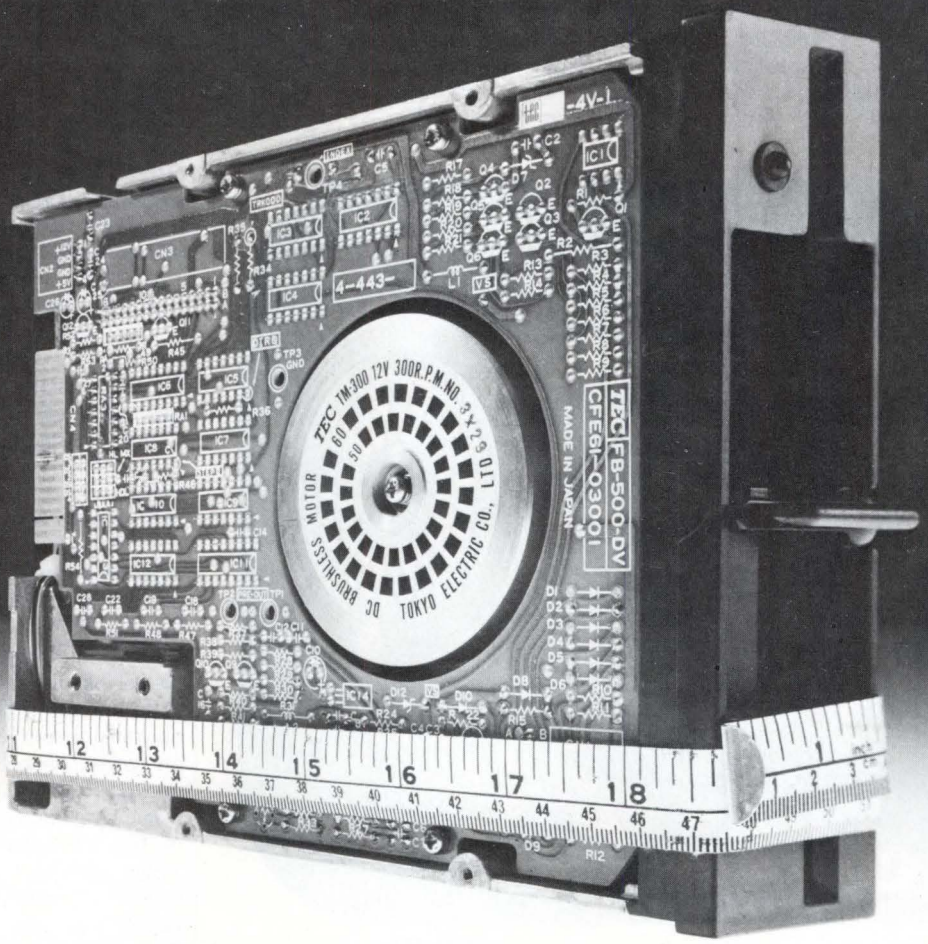
An inexpensive gateway to Ethernet local networks, the TNS-1 Microserver from Texas Network Systems uses an RS-232 port of a host computer to implement data link and physical layer specifications required for serial communications such as data encapsulation and decapsulation, collision recovery, and link error recovery. A 12-MHz 8031 microprocessor handles system timing, packet buffering, and the asynchronous serial port for the host system interface.

The hardware link, configured as a data communications equipment (DCE) modem-like interface, has a default transmission rate of 9600 bps for attaching workstations to Ethernet without modifications. Transmission rates can be altered from either the host or Ethernet transceiver to 300/600/1200/2400/4800 bps via command packets. Data terminal equipment (DTE), for terminal-like serial communications for dialup service, is a hardware option. A separate Ethernet transceiver is needed to signal transmission and reception for the attached station.

Besides defining the interface to the transceiver, Ethernet specifications also describe the data link operations needed

(continued on page 56)

HALF-SIZE 5¼ INCH FLOPPY DRIVES FROM NSA



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London (Tel. 01 427-5612)

CIRCLE 34

Hardware interface

(continued from page 54)

to manage the data link and data encapsulations. Specific operations that the TNS-1 performs include bit-wise data reception and transmission, carrier sense detection and deferring, collision detection and automatic retransmission, CRC handling (including generation for transmit packets and checking for receive packets), as well as automatic preamble generation and stripping.

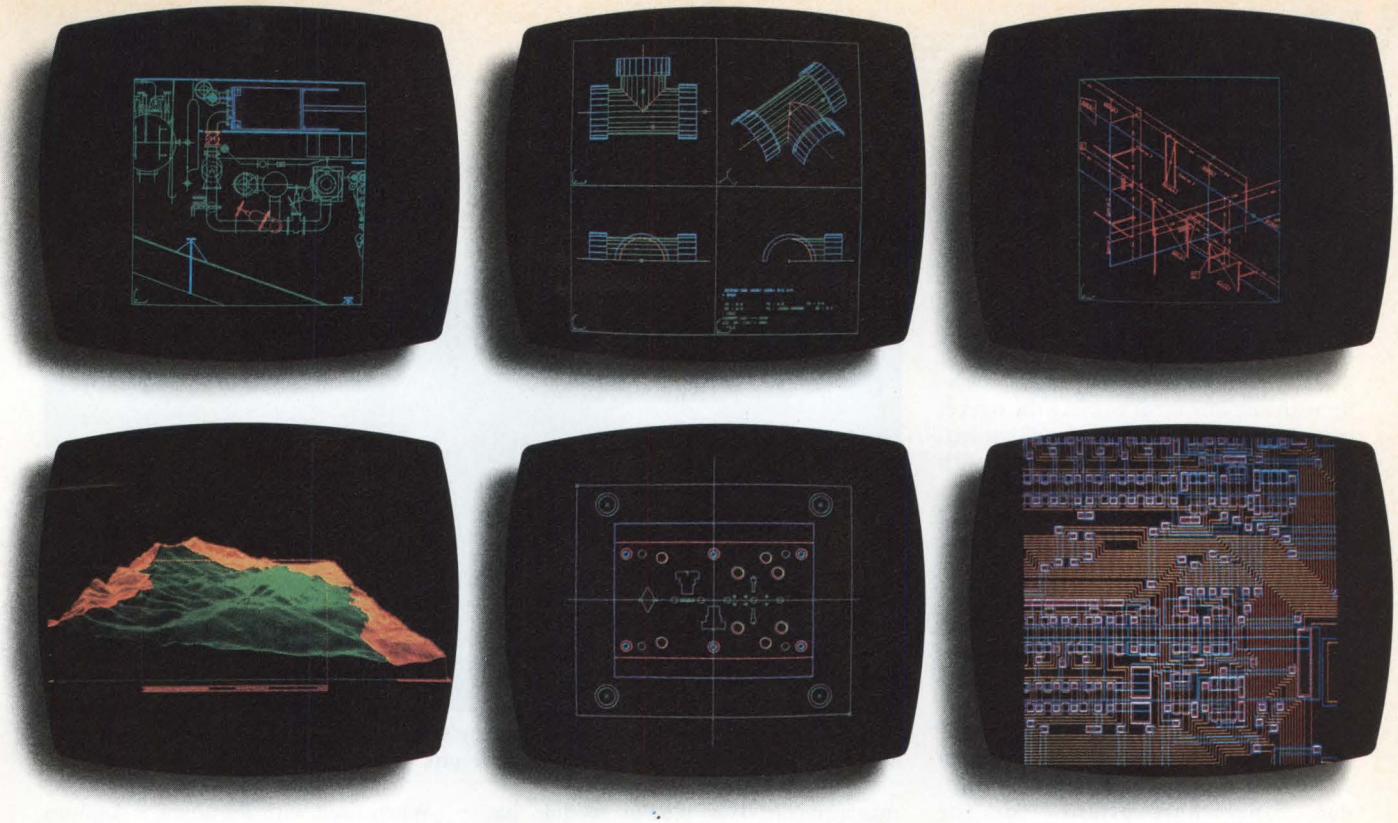
The 8031 microprocessor provides any logic necessary to generate and receive the serial bit stream between the host system. It also enforces rules on minimum and maximum packet size (64 bytes and 1518 bytes, respectively) by buffering incoming packets before they are sent to the host and buffering outgoing packets before they are sent along the network. Packets that fail to meet these rules are rejected. To cope with worst-case timing specifications, the TNS-1 can receive a deferring packet immediately after a transmitted frame within the minimum interpacket gap time of 9.6 μs. Beyond the physical and data link layers laid out in the Ethernet specification, the TNS-1 will also support the ECMA72 and Xerox transport layer protocols.

Using a protocol similar to modem control, the TNS-1 uses the RS-232 interface to pass transmission packets from the host system over Ethernet, as well as receive packets from Ethernet for host processing. When the host has a packet to send, the host issues a request to send (RTS) signal, acknowledged with either a clear to send (CTS) signal or carrier detect (CD) signal indicating an incoming packet. If CTS is returned, the host sends the packet over the interface, dropping the RTS signal after the last byte of the packet has cleared the transmitter. The TNS-1 automatically inserts the preamble on transmission, and strips the preamble on receive packet. A CD signal is transmitted after some finite delay, with a single-byte status representing the result of the transmission request following. Values indicate normal transmission (0), receiver overrun during reception of the packet due to an unexpected delay (1), the packet was too short (2), the packet was too long (3), or the packet was never transmitted over the Ethernet because of excessive collisions (4).

Packets received for host processing also follow a similar protocol. A CD signal is asserted (except when the TNS-1 returns a CTS during a host transmit operation); the packet is transmitted serially to the host after an established settling time with CRC bytes. The CD signal is also asserted when the status byte is returned. Possible values for the receive status byte include packet received with no CRC or alignment errors (0), alignment error caused improper number of bytes and invalid CRC bytes (1), and CRC error (2).

Users can also configure the system with command packets that alter the serial data formats (8-bit with no parity or 9-bit with or without parity), serial interface baud rate, and settling time before recognizing RS-232 control lines. Replies indicate configuration underwent

(continued on page 58)



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CIRCLE 36

Hardware interface

(continued from page 56)

a fatal flaw (other than 0), as well as the 6-bit network address stored in ROM for reference by the host computer. RS-232-C error detection occurs on power-up with any link error causing the packet traversing the interface to be discarded, and the event reported to the host with other network statistics. Other statistics that can be accessed with a command packet include number of packets sent and received since power-up, CRC errors detected, alignment errors detected, total collisions detected, and excessive collisions (after 16 tries) detected. Except for command packets, all other packets are passed on as received.

The TNS-1 requires host interface software to be supplied by the user, with an example provided in the reference manual. Single-unit pricing for the Microserver is $795, with quantity discounts available. Multiport interfaces are also planned. **Texas Network Systems,** 3001 Padre Court, Plano, TX 75075.

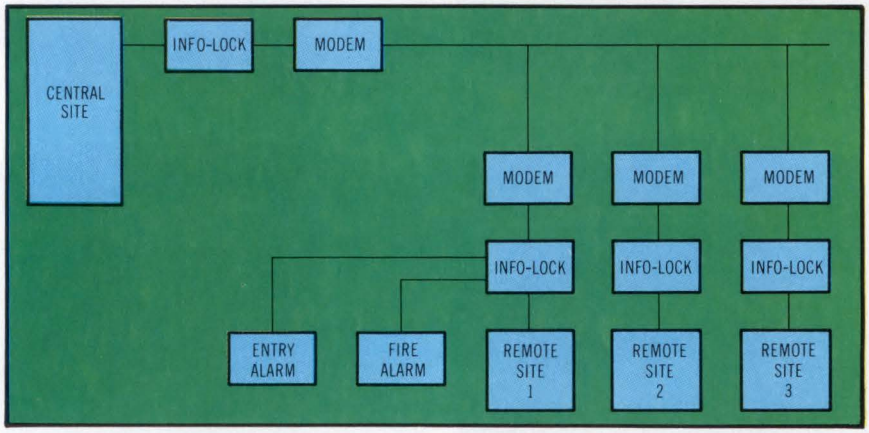
Circle 249

Protocol transparent data encryptor conforms to FED-STD 1027 for data link security

Designed for compliance with Federal Telecommunications Standard FED-STD 1027, Paradyne's Info-Lock™ is a drop-in link encryptor that can be inserted between any data terminal equipment (DTE) and data communications equipment (DCE) having an RS-232-C interface. The device uses the Federal Information Processing Standard 46 (FIPS-46) data encryption standard (DES) algorithm and operates on point to point or multipoint circuits independently of link protocol. Data rates on synchronous links are up to 64k bps; an asynchronous option allows operation at common async rates from 50 to 19.2k bps.

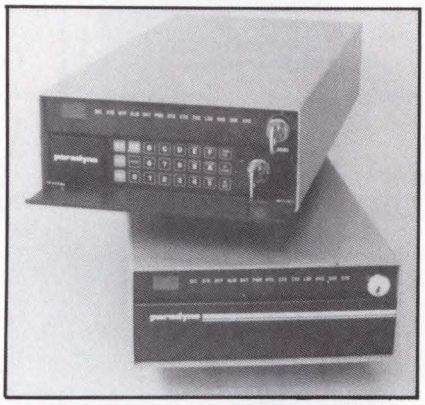
Flexible key management alternatives, selected via the front panel keyboard (see Photo), suit the encryptor to various applications. An automatic key management feature, using a 2-key hierarchy, allows the device to operate for long periods without attention or manual key transfer. For secure key management, master keys are never sent over the communication link; the encryptor is thus protected against impersonating tactics that may be applied against some public key transfer methods.

An optical key transfer module minimizes human involvement in key management. This plug-in module has electrically erasable nonvolatile memory and provides a secure means of transferring key encryption key and data encryption key variables, as well as Info-Lock attributes between encryptors in the network. Since the module randomly selects the encryption keys, no one knows the particular key currently being used.



Typical encryptor configuration. Paradyne's Info-Lock operates half- or full-duplex in point to point or multipoint circuits with up to 127 drops.

Built-in self test automatically performs DES S-box and checkword tests as specified in FED-STD 1027. Also, plain text and corresponding cipher text are continuously compared. If these data are found to be identical for 64 continuous bits, the crypto alarm operates and transmission stops. Several available manually initiated tests include end to end test of both encrypt and decrypt functions.



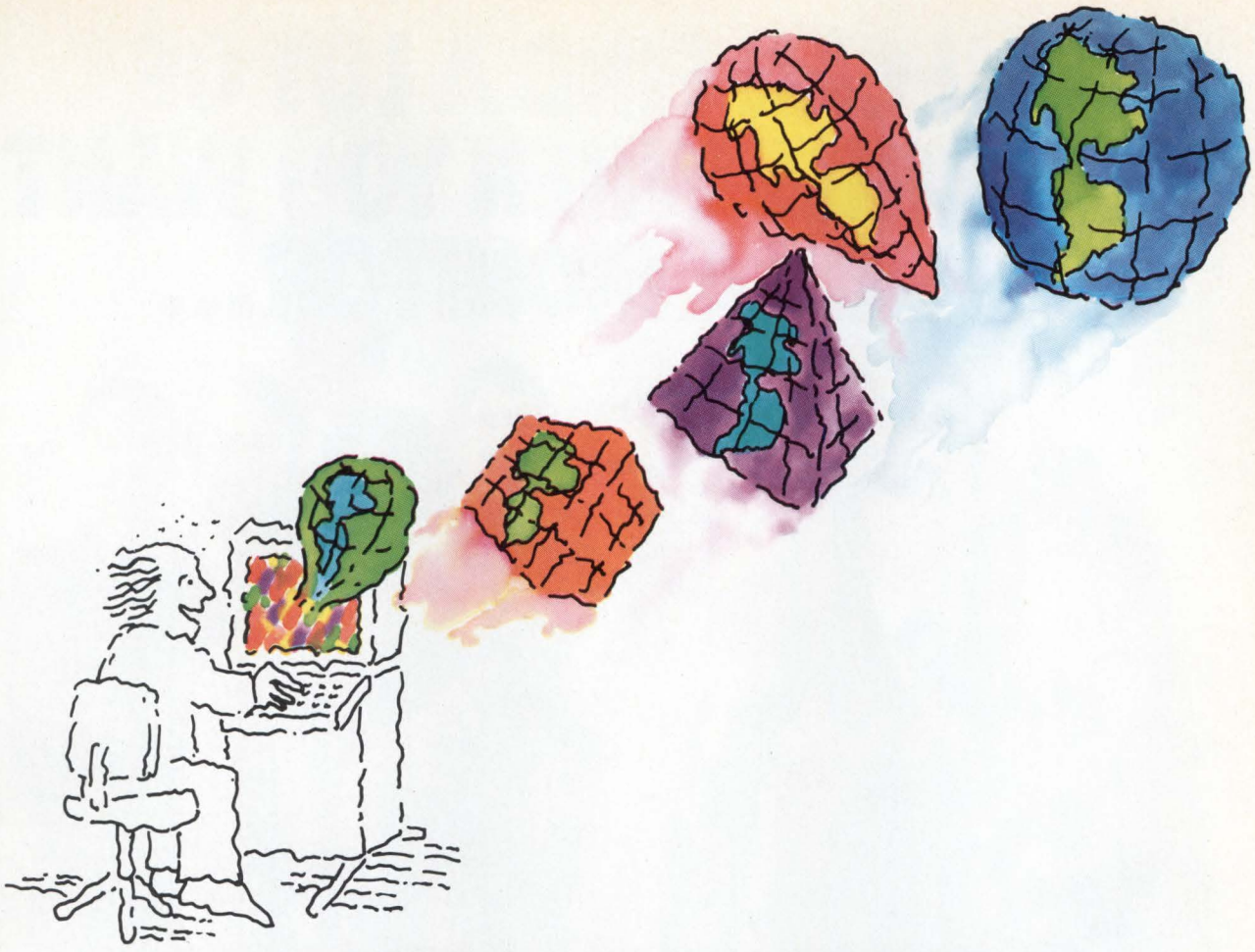
Info-Lock protocol transparent link encryptor. Lower unit is secured; upper unit shows control panel accessed after opening both protective locks. Panel indicators display encryptor status and states of EIA interface lines on DTE side of encryptor.

When used with Paradyne's Analysis Diagnostic Microcomputer option, numerous security and diagnostic functions and tests can be carried out at the central site Analysis console. Such security functions as tampering or key insertion are automatically monitored. Diagnostic tests such as EIA interface monitoring, bit error rate measurement, and data encryption self tests are also performed, in addition to DTE and data encryptor digital loopback tests. With the Analysis option, diagnostic functions are extended past the remote modem to the data encryptor and the encryptor/DTE interface.

For physical protection, all controls are covered by a steel door that is secured by a pick-resistant lock. A second such lock must be enabled in order to operate the controls associated with key management. This arrangement of control protection conforms to FED-STD 1027 requirements. Tampering, or attempts at unauthorized physical access activate the crypto alarm, alert the control site, and zeroize the key variable storage. An option provides four external alarm inputs for remotely reporting building security, fire, and other alarms (see Figure).

Among other options are a rack-mounting kit, RS-449 adaptor, motion detector, and secure mount and cable lock. Power requirement is 30 W at 110-120/220-240 Vac, 47-62 Hz. The device measures 3.5″ h x 8.5″ w x 17″ d (8.9 x 21.6 x 43 cm) and weighs 10 lb (4.5 kg). Unit cost is $2900; quantity discounts are available. **Paradyne Corp,** PO Box 1347, 8550 Ulmerton Rd, Largo, FL 33540.

Circle 250



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CIRCLE 37

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CONRAC

CIRCLE 38

The data

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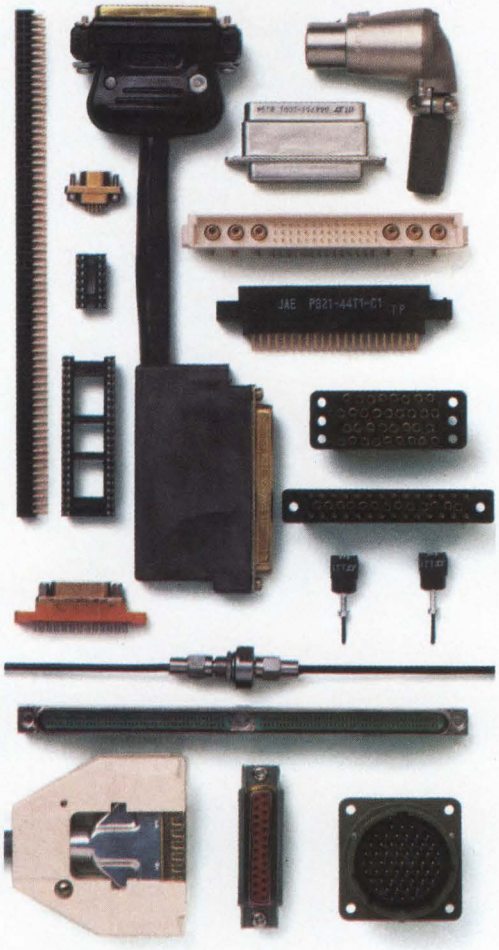
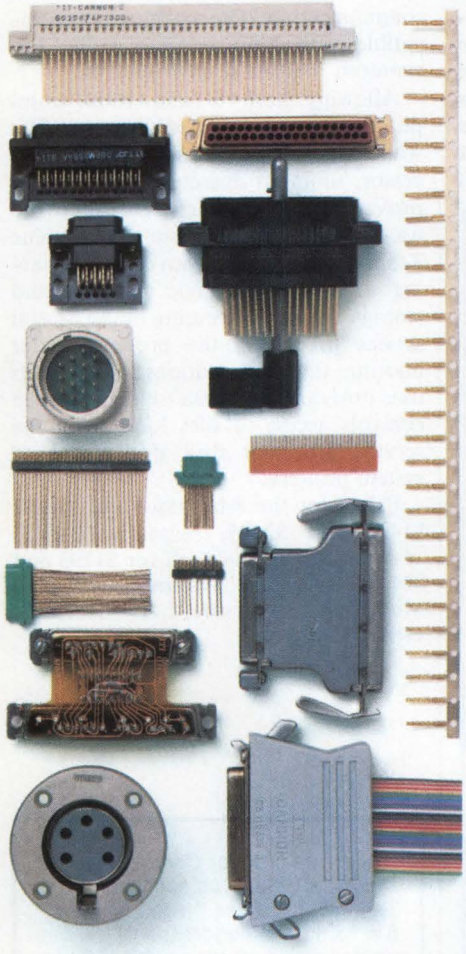


connection.



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CANNON ITT
The Global Connection

8/16-bit microcomputers serve standalone or in mixed network

Growth from single-user system to multisystem network without obsoleting any computer in the system is promised by Televideo Systems' latest microcomputers. The CP/M based machines range from 8-bit workstations to 16-bit standalone systems with graphics capability, and serve to bridge the gap perceived between existing personal computer and minicomputer offerings.

The 8-bit TS803 with two vertically mounted 500k-byte slimline floppy disk drives serves not only as a standalone system but can connect into a service processor to use the company's multitasking, multiprocessor, multi-user operating system technology (MMMOST) network manager. Its companion, the 8-bit TS800, serves up to 15 additional users as a satellite station. The 16-bit TS1603 with two 500k-byte floppy disks stands alone or integrates into data sharing 16-user networks of 8- and 16-bit machines. A second 16-bit unit, the TS1600, is a low cost intelligent workstation that connects into the MMMOST network.

Both 8- and 16-bit machines are based on the design of the company's 970 smart terminal. All units have 14″ green on black built-in CRT screens with 640 x 240 resolution and detachable Selectric style keyboards.

Based on Zilog's 4-MHz Z80A microprocessor, both 8-bit units have 64k bytes of RAM, expandable to 128k bytes. The 803 provides 32k-byte screen memory for use with both text and graphics and 8k bytes of EPROM. Standard interfaces include an RS-232 serial port, a parallel Centronics-compatible printer port, and an RS-422 port capable of 800k-bps communication.

The 16-bit single board computers are designed around Intel's 8088 microprocessor and expand from 128k bytes of RAM to 256k bytes with the addition of a memory board. The TS1603 includes a 50-pin connector that allows a graphics board to be added. Each has two RS-232 ports plus an RS-422 port for 800k-bps communication. The machines are compatible with 8-bit systems within the MMMOST multi-user environment.

Televideo's TS1603 mounts two 5¼″ slimline disk drives vertically in adjacent enclosure. Silent cooling system vents through top of enclosure to reduce heat accumulation in terminal and increase reliability.

Allowing both 8- and 16-bit computers to share output devices and files while connected to the same service processor, MMMOST operates under CP/M to provide an environment for up to 16 user stations. Each system can combine 8- and 16-bit stations with each user having its own local CPU, memory, and storage devices. Executing in the central service processor, the program, after booting the user stations, downloads user programs and data to them. It then controls access to files located on the service processor disk drives and to system printers.

Prices for the 8-bit TS800 and 803 are $1495 and $2495, respectively. The 16-bit TS1600 and 1603 sell for $1795 and $3495. **Televideo Systems, Inc,** 1170 Morse Ave, Sunnyvale, CA 94086.
Circle 251

For a free copy of *Computer Design*'s "1982 Subject Index of Technical Articles," send an 8½″ x 11″ self-addressed, postage-paid envelope (54¢ U.S.) to Index Editor, *Computer Design*, 119 Russell St, Littleton, MA 01460, U.S.A. For addresses outside the U.S., enclose a self-addressed mailing label, and International Reply Coupons to cover 3-oz (85-g) airmail postage.

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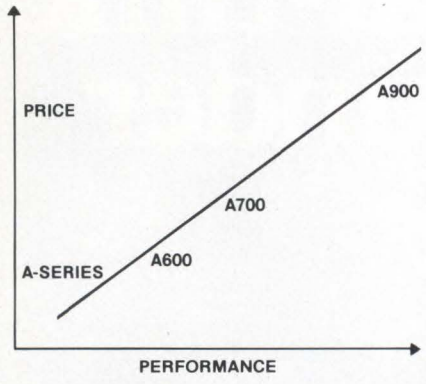

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implementation and 3.7 megabytes per second I/O bandwidth, this made it comparatively simple to reach a CPU speed of 3 MIPS. As well as 560,000 floating point operations per second. All for an astonishingly low $14,818.

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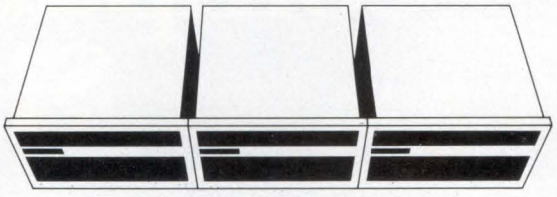

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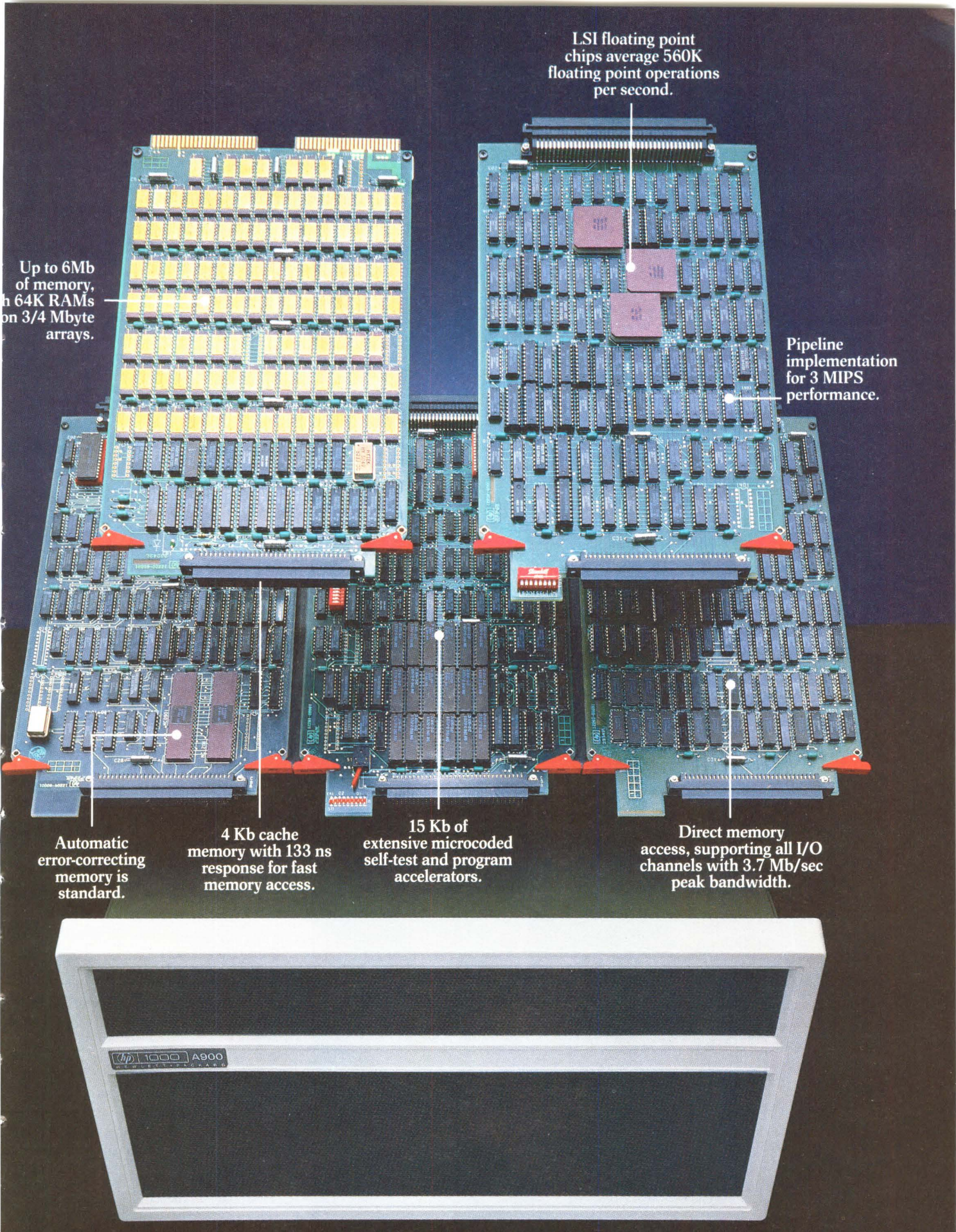
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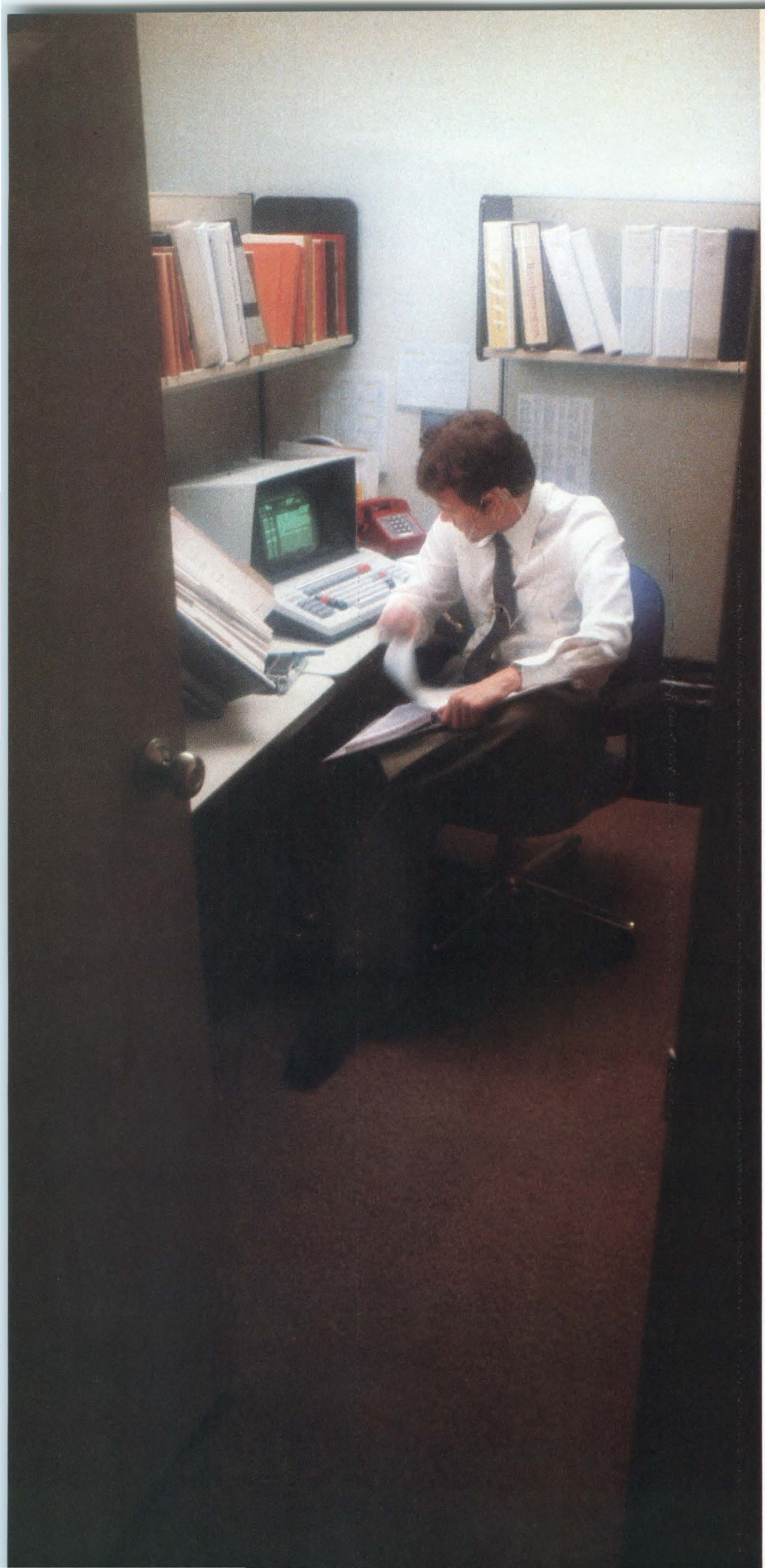

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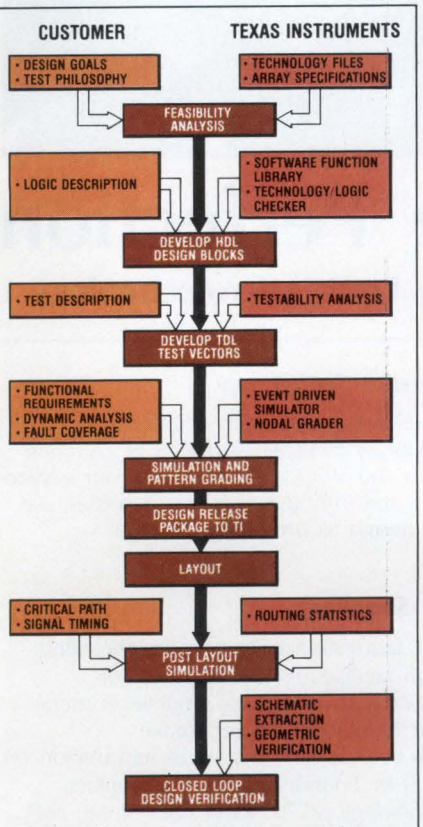

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TAT008	800	STL	2.5 ns	600 μW	104	C/M
TAT010	1000	ASTL	1.0 ns	300 μW	88	C
TAT020	2000	ASTL	1.0 ns	300 μW	120	C/M
STL700	560	STL	3.0 ns	300 μW	61	M
SBP96700	1120	I^2L	11/15 ns	100 μW	96	M
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CIRCLE 59

GROWTH OF PROCESSOR FAMILY BOOSTS SYSTEM OPTIONS

Expansion of the 68000 family to include other processor and peripheral chips frees system designers from application limitations.

by John F. Stockton

Since its introduction in 1979, the MC68000 microprocessor has been widely used in applications ranging from low end microcomputers to large, multi-user nonstop mainframes. The 16-bit exterior/32-bit interior design of the MC68000 supplies high performance at a reasonable price. A typical problem is that the latest designs must always offer either higher performance or lower cost. To make matters worse, redesign efforts must be minimal. The ultimate solution to this design dichotomy lies with the microprocessor vendor that offers object code compatible products that meet both requirements.

The family tree of the M68000 microprocessor was planned with this strategy in mind. (See Fig 1.) Recently introduced family members extend features both upward and downward in terms of performance and cost. As an example, because the MC68008 processor is compatible with the MC68000, programs written for entry level systems can be ported to the MC68008 without any change. This processor establishes the bottom end of the M68000 processor family and is basically identical with the MC68000, except that it has been redesigned to work with an external 8-bit data bus and reduced address space.

John F. Stockton is currently the business manager for the mid-range microprocessor group at Motorola Corp, 3501 Ed Bluestein Blvd, Austin, TX 78721. Previously, he was the manager of technical marketing for the M68000 family. Mr Stockton has a BSES from the University of Texas, Austin.

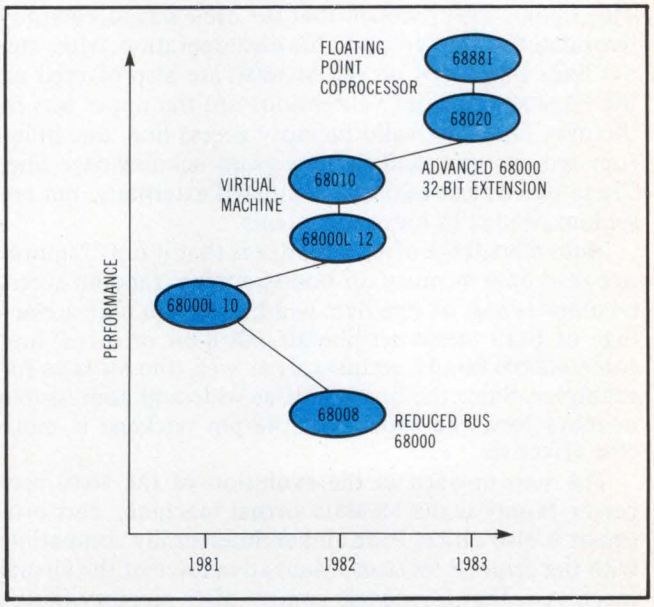

Fig 1 Genealogy of the 68000 family. By extending the family offerings both upscale and down, the manufacturer offers designers performance and cost-effectiveness.

Multiplexing the address and data was considered, but the traditional problems of lower performance tipped the decision toward a nonmultiplexed implementation. By maintaining a nonmultiplexed bus structure, the MC68008 automatically has a 30% to 50% performance edge over competing processors. The address space supported by this processor is limited to 1M bytes—consistent with the needs of low end systems.

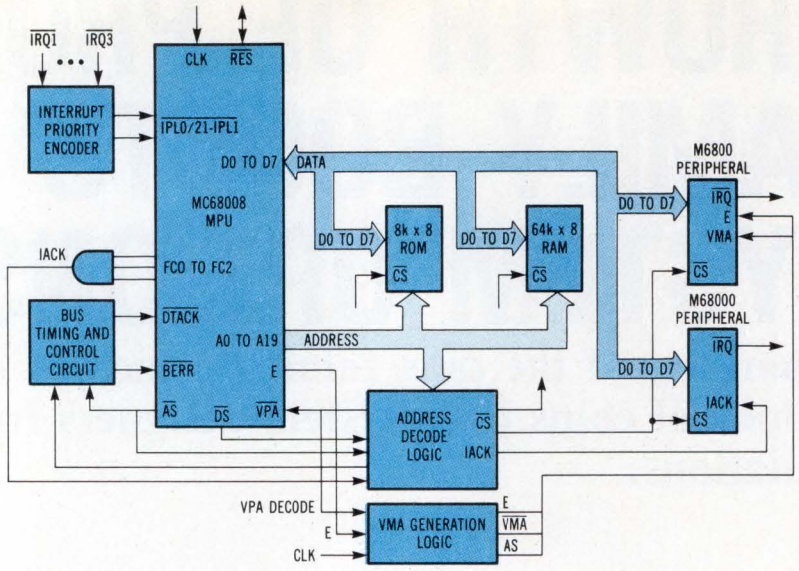

Fig 2 MC68008 processor minimum system configuration requires only one boot read only memory. The 8-bit data bus and reduced address space (1M byte) allow a compact 48-pin package.

Fig 2 shows a minimum system configuration MC68008. Handshake signals operate exactly the same as for the MC68000—an address is output onto the address bus, the address strobe is asserted, data are output, and the data strobe is asserted. When the operation is complete, as a write cycle would be in this example, the data transfer acknowledge signal is asserted back to the processor. This signals the processor that the cycle has successfully terminated and to go on to the next operation. Most signal lines supported on the MC68000 are also offered on the MC68008. The only exceptions are the upper bits of the data lines, the valid memory access line, one interrupt request line, and the bus grant acknowledge line. These signals can be easily simulated externally, but are seldom needed in low end systems.

Main advantage of the MC68008 is that it only requires one read only memory for bootstrapping, random access memory (RAM) of one byte width, and can take advantage of both M6800 peripherals (all 8-bit oriented) and some M68000 family peripherals as well (the MC68230 for example). Since the bus is half as wide and addressable memory less, the processor's 48-pin package is more cost-effective.

The step upward in the evolution of the 68000 processor family is the MC68010 virtual machine. This processor is also object code and architecturally compatible with the original MC68000. Main advantage of the virtual machine is that it recovers control after memory faults. Thus, the processor can be used in demand paged environments and as a virtual machine with multiple operating systems running concurrently.

This virtual memory machine allows programs that exceed the address space of the basic machine to run without the conscious intervention of the applications programmer. All of the shuffling of the program pieces happens transparently, so the user never knows that the machine has less memory than the program required. This ability allows systems based on the MC68010 to offer features common on larger mainframe machines, at a fraction of the cost.

The MC68010 is designed on the assumption that the trend in small computer systems is toward greater mass storage capacities. This approach is possible because most programs are small enough to be completely resident in primary storage. Luckily, those that would fully occupy RAM, occur in small proportion to the overall code.

A working set of memory pages can be resident in primary storage, while other portions of the program reside in secondary storage (disk). When a reference is made to a portion of the program that is not in primary memory, the required page can be located on and removed from secondary storage. Then, the bus cycle can continue. As far as the user is concerned, the processor has a very large physical address space, although the amount of memory that is actually present is quite limited.

Ability to support virtual memory requires that the processor stop an instruction reference in the middle of a bus cycle, be redispatched to make the page resident, and come back and continue the execution of the interrupted instruction at some later time. The sequence of events during the handling of a page fault is as follows: after a page fault is detected, the MC68010 copies the contents of its internal registers to the supervisor stack. This operation cleans out the machine and, after a minor amount of housekeeping, may be redispatched to another task.

When the previously faulted task is ready to continue, the supervisor again does some housekeeping, and then executes a return from exception (RTE) instruction. The MC68010 RTE instruction is more intelligent than that of its predecessor since it allows control to be returned from page faults as well as interrupts. Upon execution of this instruction, the processor reloads all of its temporary registers from the supervisor stack, and then tries to rerun the bus cycle that caused the page fault. When the instruction completes successfully, the program continues to run as if nothing had happened.

Obvious advantage of virtual memory support is that, in multi-user systems, very large programs can run in

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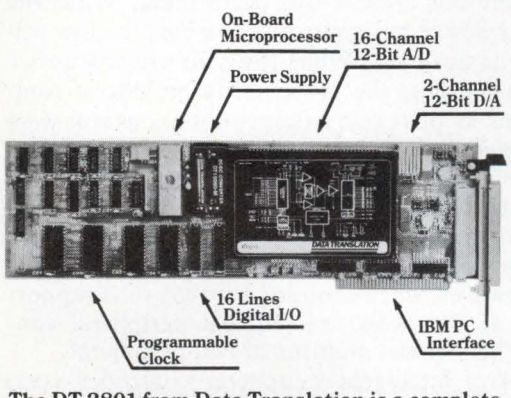

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CIRCLE 43

low cost environments. Another benefit is that applications programmers can write very large programs without worrying about memory limitations. This eliminates headaches caused by artificial memory segment bounds or program overlays, and simplifies software development.

The next step beyond the virtual machine is the MC68020, a 32-bit version of the MC68000 processor. This processor allows programs written on the MC68000 to run between two and four times faster. This increase in performance is due to the 32-bit wide data bus on the MC68020. Since processor performance is closely tied to memory bus bandwidth, by offering twice the bandwidth, the performance doubles. Another feature that increases performance is an instruction cache scheme. Once a loop is trapped in the cache, the execution rate is considerably higher than it would have been if external memory references were required.

An MC68020 companion is the MC68881 floating point coprocessor (FPCP). This architectural extension of the MC68020 processor allows very fast execution of floating point instructions: roughly 50 times faster than a software program when emulating IEEE 80-bit floating point multiply operations. The FPCP will execute approximately 120,000 80-bit floating point operations per second. The instruction set of the MC68881 also offers many arithmetic and transcendental operations, all with equally impressive performance.

Processor architecture extensions

Peripheral support chips directly influence hardware and software design. Included in the 68000 family are the MC68451 memory management unit, the MC68450 direct memory access controller (DMAC), and the MC68452 bus arbitration module (BAM). Each of these peripheral chips contribute to how the ultimate system will be configured. As a result, it is very important that systems designers fully understand the philosophy behind the most recently introduced member of this family, the MC68452 bus arbitration module.

The bus arbitration module is a controller that arbitrates conflicts between multiple bus masters when all controllers request to use the bus at the same time. These controllers can be any combination of processors, DMACs, or other bus masters that need to take control of the address and data bus to perform their operations. The MC68452 does not lower system performance, since the arbitration takes place concurrently with the bus cycle operation. The BAM can be used in other configurations, since the chip completes arbitration in less than 50 ns. The M68000 family of bus masters supports overlapping of arbitration and bus operation. Before the end of a bus cycle, the next bus master knows that the next bus cycle will be available for use, without waiting for the arbitration sequence to occur.

Signals responsible for arbitration are the bus request (BREQ), the bus grant (BGNT), and the bus grant acknowledge (BGACK). During any cycle the BREQ can be asserted by a peripheral and, shortly afterward, the processor will send back BGNT. This informs the peripheral that at the end of this current bus cycle it can take control of the bus. The peripheral monitors the address strobe signal of the processor and when it is negated, knows that the processor has released the bus. At this time, the peripheral asserts BGACK to indicate it has control of the bus. The release of the BREQ signal allows the peripheral to give bus control to other peripherals if it is requested. When the peripheral is finished with the bus, it negates the BGACK signal and the processor continues with its bus operations. Fig 3 illustrates the interconnection between the BAM, the central processing unit, and the DMACs.

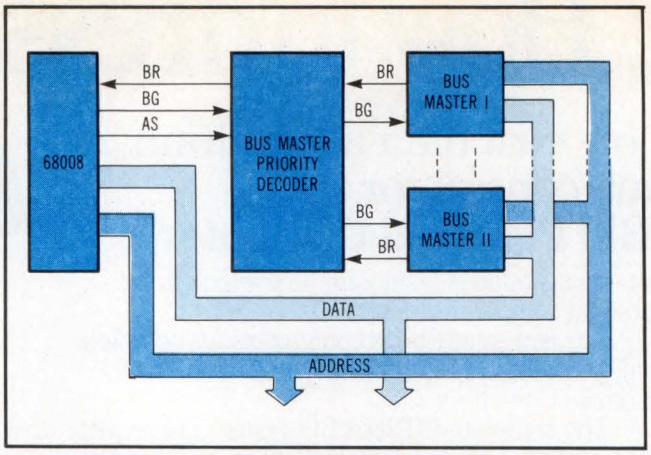


Fig 3 Bus arbitration module can prioritize requests from up to seven bus masters, based on a physical priority scheme.

When two peripheral bus masters simultaneously request bus use, the conflict is resolved quickly since the system performance degrades as a result of time spent in arbitration. In less than 50 ns the BAM can resolve the conflict and assign a priority based on physical location. Additionally, the BAM issues a bus clear signal, which can be used to disable lower priority peripherals from using the bus.

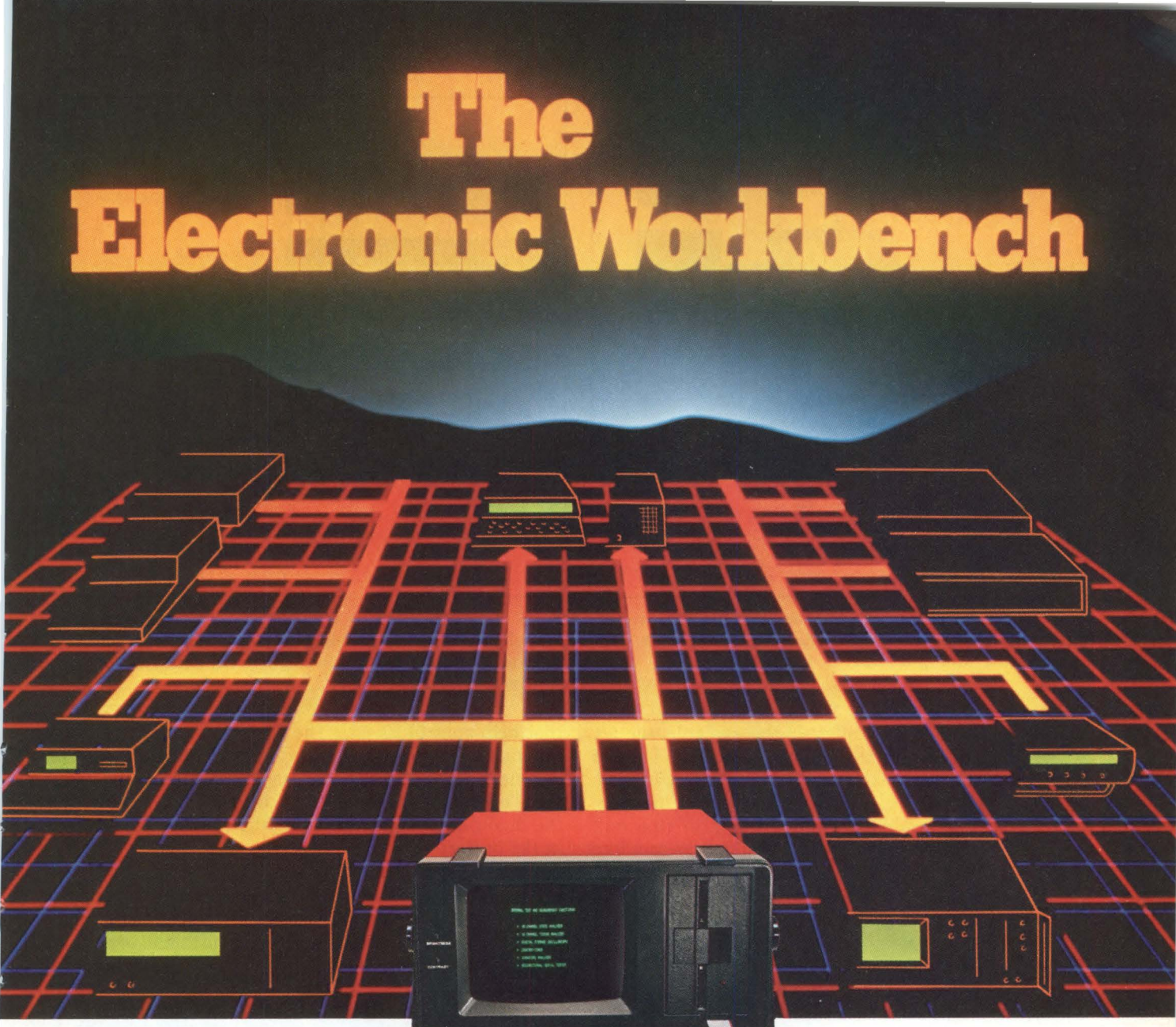
The M68000 family of bus masters all support the concept of rerunning a bus cycle. If a low priority device insists upon hogging the bus, a higher priority device can take control of the bus before the selfish device has completed the bus cycle it was performing. While the high priority device has control of the bus, the low priority device is dormant. When the high priority device relinquishes the bus, the low priority peripheral completely reruns its bus cycle and it continues as if it were not interrupted.

Fortunately, not all peripheral parts have as great an impact on the design of the central processor hardware and software as the MC68452 bus arbitration has. There are a number of considerations that must be carefully weighed, however, when choosing between such support peripherals as the MC68120 intelligent peripheral controller and the MC68901 multifunctional peripheral.

The MC68120 intelligent peripheral controller (IPC) brings input/output (I/O) processor capability to the M68000 family. IPC supports a local address/data bus that connects the system to peripherals such as disk controllers or communications interfaces. The local bus is synchronous, runs with a one microsecond cycle time, and works with M6800 family peripherals. This style of I/O allows interface to very cost-effective peripherals that are supported by many vendors. Additionally, the separate I/O bus allows I/O operations to overlap with computer operations, thus increasing the system throughput.

An example of the MC68120 IPC working as an I/O processor is illustrated in Fig 4. Here, the IPC is being used

The Electronic Workbench



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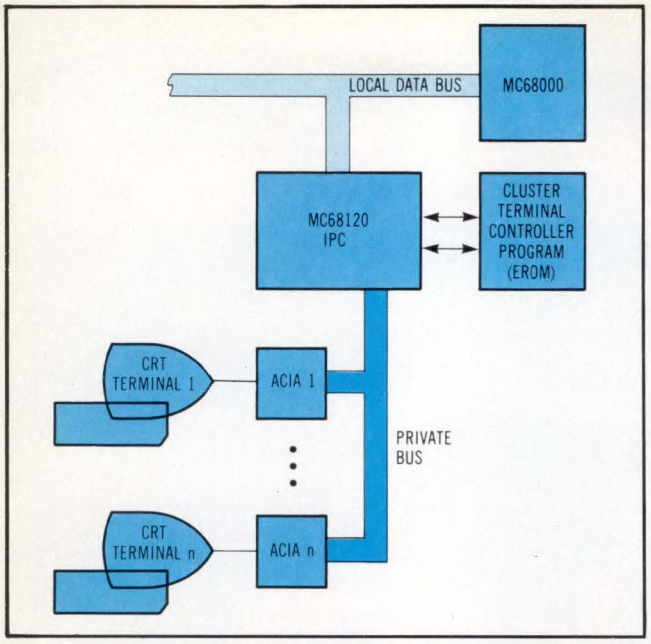

Fig 4 Intelligent peripheral controller (MC68120) can oversee cluster terminal operations and greatly reduce interrupt overhead of central processor.

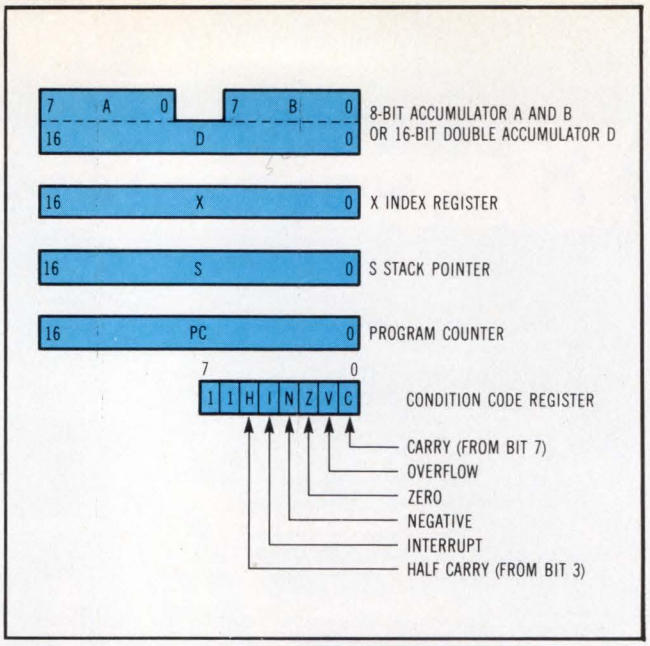

Fig 5 User programming of intelligent peripheral controller is straightforward. Several data types and addressing schemes are supported with semaphore registers used for control and status checking.

as a cluster terminal controller. In this example, the IPC connects to multiple serial I/O ports on the local bus and to the M68000 instruction bus on the host processor side. The function of the IPC is to effectively buffer the serial I/O ports and to act like a multiport first in/first out. Messages being sent by the host to terminals are put into a buffer. The IPC then takes the messages out of the buffer and outputs them, in a serial fashion, to the serial I/O ports. Messages from the terminals are buffered by the IPC, again in a serial fashion, and are then sent to the host through the dual-port RAM buffer.

Having the IPC act as a cluster terminal controller reduces the number of interrupts that the host has to service from an interrupt per character, to an interrupt per message. If the average message is 20 characters long, this decreases the interrupt request rate by a factor of 19.

The architecture of the IPC is related to the MC6800 and the MC6801 single-chip microprocessor and is optimized for control oriented applications. The 8-bit processor is upward compatible with both the source and object code for the MC6800, and features the user programming model shown in Fig 5. The register set consists of two 8-bit accumulators, A and B, that can be linked to a single 16-bit accumulator D. Additionally, the processor has a 16-bit index register, a 16-bit stack pointer, and a 16-bit program counter. The condition code register has bits for carry/borrow, overflow, zero, negative, interrupt, and half carry.

The instruction set of the MC68120 includes support bit, byte, binary-coded decimal, and 16-bit word data types. The addressing modes include inherent, immediate, direct, extended, relative, and indexed. The address space supported is 16 bits, corresponding to 64k bytes of memory. The MC68120 internal processor interfaces to the MC68000 instruction bus through a dual-port RAM buffer. This 128-byte buffer has six semaphore registers that help control its use. The semaphore registers contain bits that show when a specific portion of the buffer is in use and which processor was the last to use the buffer. This eliminates the need to check if the IPC has read the dual-port RAM by rereading the message that it left in the buffer.

For designers wanting a more flexible approach to peripheral support, the MC68901 multifunction peripheral (MFP) is a combination of miscellaneous interface devices that are commonly found in small systems designs (see Fig 6). These elements include four timers,

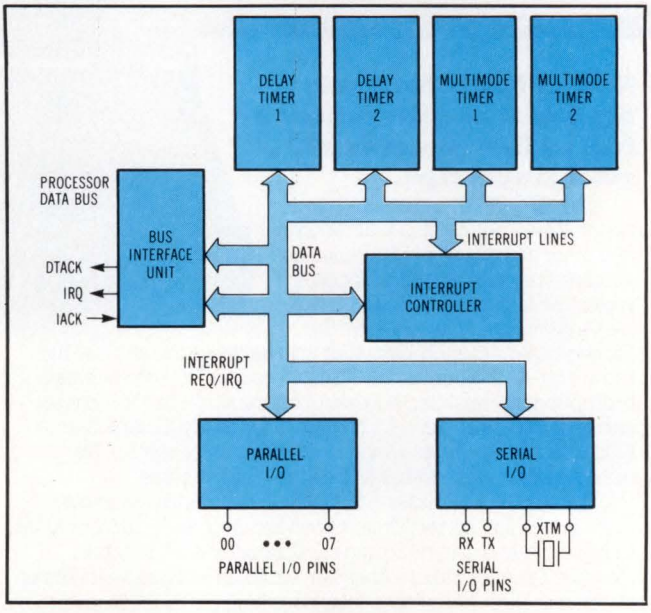

Fig 6 MC68901 multifunction peripheral chip can prioritize 16 interrupt sources. Parallel and serial ports allow synchronous and asynchronous communications to take place within this 48-pin package.

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MOC5007	1.6	0.4	0.75	50	4.0/4.0 0.1/0.1	$2.80
MOC5008	4.0					$1.65
MOC5009	10					$1.30

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an interrupt controller that will support up to 16 sources, an 8-bit parallel I/O port, and a single-channel universal synchronous/asynchronous receiver/transmitter (USART) for serial communications. The four timers consist of two that are presettable, and two that are simply countdown timers. Each timer is individually prescalable.

The interrupt controller can prioritize up to 16 sources of interrupts from eight external sources (via the parallel I/O port) or eight internal sources (internal timers or the serial port). The parallel port allows each bit to be individually programmed to be an input or an output. Each pin can also be an interrupt source and can generate an interrupt on either a leading or trailing edge transition. The USART serial port supports full-duplex asynchronous communications at rates up to 62.5k bps. It also works in a synchronous mode, where it will support data rates of up to 1M bps. The baud rate can be either internally or externally generated, and the USART has both full modem and DMA controller handshakes. The MFP 8-bit data bus allows it to be packaged in a 48-pin dual-inline package.

Data communications interfaces

An area of increasing importance for system manufacturers is data communications and local area networking. As more distributed systems are connected together with high speed data links, very large scale integration solutions to specific circuit problems must be found. The present trend in distributed office computer systems locates intelligence in low cost workstations that depend heavily on intelligent file servers. These systems, which must be interconnected in a loosely coupled fashion, use some form of serial data communications. With this trend in mind, the M68000 family peripheral line has been oriented heavily toward data communications. Table 1 compares bit rates and protocols supported with the parts that are available to support those requirements. Included in this table are the older M6800 family parts, which also work with the MC68000, but are not discussed. Following is a closer look at some M68000 data communications family members.

The MC68562 is a 2-channel universal communications controller that supports commonly used asynchronous and synchronous protocols. These protocols include advanced data communications control procedure, synchronous data link control (SDLC), higher data link control (HDLC), X.25, bisynchronous, and digital data communications message protocol. The MC68562 will operate at data rates of up to 4M bps, and will directly interface to data lines carrying any of nonreturn to zero, nonreturn to zero inverted, or Manchester encoded data. No external data/clock separation is required, since the chip contains internal phase locked loop and baud rate generators. Both the receive and transmit data paths are quadruply buffered to lower the interrupt latency requirements for high data rate operation. Additionally, the chip contains a programmable timer that can be used for interrupt generation for either periodic ticks, or timeout functions. The interrupt interface supports either a vectored interrupt scheme, similar to the rest of the M68000 family, or the autovectored interrupts used in the M6800 peripheral family. The data interface to the device offers full modem control line handshakes and DMA handshakes for direct serial to memory move operations. The parallel interface of the chip has an 8-bit parallel data path, and offers support for the M68000 family handshakes. These lines are used for cycle termination, interrupt requesting, and interrupt acknowledgment, respectively. This part, currently under development by Signetics, will be second sourced by Motorola.

TABLE 1

M68000 Datacom Devices

Device	Protocol	Speed
MC6850 ACIA MC68562 MPCC MC68564 SIO MC68661 EPCI MC68681 DUART	Asynchronous	0 to 1M bps
MC6852 SSDA MC68562 MPCC MC68564 SIO MC68652 MPCC MC68661 EPCI	Bisync - bit oriented protocol	
MC6854 ADLC MC68562 DUSCC MC68564 SIO MC68652 MPCC	SDLC/HDLC - byte control protocol	
MC6852 SSDA MC68562 DUSCC MC68652 MPCC	byte control protocol	1 to 2M bps
MC6854 ADLC MC68562 DUSCC MC68652 MPCC	bit oriented protocol	
MC68562 DUSCC	byte control protocol	2 to 4M bps
MC68562 DUSCC	bit oriented protocol	

The MC68590 local area network controller for Ethernet (LANCE) completely supports the blue book definition of the Ethernet standard, and both transmission and access mechanisms. It operates with a data rate of 10M bps, and includes a DMAC on the processor side of the interface to help support high data rates. The DMAC covers the entire 24-bit address space offered by the MC68000. In addition, DMA transfers into multiple receive buffers from multiple transmit buffers are also supported.

The LANCE handles the carrier sense multiple access/collision detection serial bus arbitration, by using an algorithm incorporating listen before talking, listen while talking, and retransmit on collision after a random wait. On successive collisions, the mean value of the random wait is increased to lower the probability of another collision, and to provide load leveling on the serial bus. Also included in the LANCE is support for the lower levels of the Ethernet protocol by performing packet framing, preamble and cyclic redundancy check insertion and extraction, and address filtering and detection. The internal DMAC handles all data transfers once the LANCE has been initialized, so communication to and from the part all takes place through a RAM buffer.

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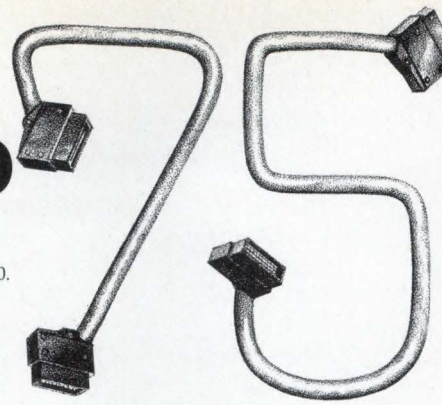

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Part Number	Description	Regular Price	Sale Price**	% Off
BC01V-25/BF	Cable Assy DP8-EA 25 FT	$126.	$82.	34
BC02M-25/BF	WO21-WO22 Ribbon, 25FT	150.	39.	74
BC02S-05/BF	Cable, WO23-WO23 TU55 5FT	180.	45.	75
BC03L-05/BF	EIA Cable, H856 TO RS232C MAL	250.	110.	56
BC03M-A0/BF	100' Null Modem Ext Cable	140.	95.	32
BC03N-A0/BF	Coax Cable 100 Foot	140.	80.	42
BC03N-A5/BF	Special Built Cable 150FT	200.	100.	50
BC03P-A0/BF	Null Modem, 2 Fem Ends, 100FT	150.	90.	40
BC04R-10/BF	Special Built Cable 10FT	32.	22.	31
BC04R-12/BF	Mate-N-Lok to 4 Rings, 12FT	34.	24.	29
BC04R-A0/BF	Special Cable 100FT	100.	70.	30
BC04R-B0/BF	Mate-N-Lok to 4 Rings, 200'	200.	130.	35
BC04Z-01/BF	H856,40 Conductor Flat (1')	48.	26.	45
BC04Z-06/BF	H856,40 Conductor Flat (6')	50.	30.	40
BC04Z-10/BF	H856,40 Conductor Flat (10')	52.	35.	32
BC04Z-15/BF	H856,40 Conductor Flat (15')	80.	40.	50
BC04Z-25/BF	H856,40 Conductor Flat (25')	90.	45.	50
BC05C-09/BF	Cable Modem 9FT	112.	80.	28
BC05C-25/BF	BC05C-25 Cable Modem	120.	90.	25
BC05D-15/BF	RS232 Male-Fem, 25 Cond, 15FT	125.	90.	28
BC05D-20/BF	RS232 Male-Fem, 25 Cond, 20FT	130.	95.	26
BC05D-25/BF	RS232 Male-Fem, RS232 Fem 25'	140.	100.	28
BC05D-50/BF	RS232 Male to Female, 50FT	150.	110.	26
BC05D-75/BF	RS232 Male-Fem, 25 Cond, 75FT	225.	160.	28
BC05F-A0/BF	Cable Interface LA30S	150.	75.	50
BC05J-06/BF	Line Cord Set 240 V 6 FT	100.	65.	35
BC05L-15/BF	H855 TO H855 Flat Reverse 15	80.	40.	50
BC05M-04/BF	Cable H856 to Mat-N-Lok 4'	42.	20.	52
BC05M-20/BF	Special Cable 20FT	62.	40.	35
BC05M-25/BF	Cable H856 to M-N-Lock 25'	65.	45.	30
BC05M-50/BF	Cable H856 to M-N-Lock 50'	90.	60.	33
BC05W-10/BF	50 Conductor Signal Cable 10'	85.	45.	47
BC05W-25/BF	50 Conductor Signal Cable 25'	160.	85.	46
BC06F-25/BF	M908 TO Compstar 191, 25 FT	425.	225.	47
BC06K-10/BF	H885-H885, Mirror Conn, 10 FT	100.	50.	50
BC06S-25/BF	Round Massbus Cable, 25 FT	1,040.	425.	59
BC07A-10/BF	Cable H856 1-End 20 TW PR 10'	130.	70.	46
BC07A-25/BF	Cable H856 1-End 20 TW PR 25'	154.	120.	22
BC07B-25/BF	Cable H856 1-End 11 TW PR 25'	200.	90.	55
BC07D-15/BF	H856 2-20 COND Ribbons 15'	140.	85.	39
BC07D-25/BF	H856 2-20 COND Ribbons 25'	160.	100.	37
BC08A-02/BF	M903 to M903 Dual Mylar 2'	150.	40.	73
BC08A-05/BF	M903 to M903 Dual Mylar 5'	200.	50.	75
BC08A-07/BF	M903 to M903 Dual Mylar 7'	220.	55.	75
BC08A-09/BF	(M903-M903) 1.25" Mylar (9')	235.	60.	74
BC08A-10/BF	M903 to M903 Dual Mylar 10'	250.	65.	74
BC08A-15/BF	Cable, BC08A	300.	75.	75
BC08A-25/BF	M903 to M903 Dual Mylar 25'	350.	90.	74
BC08F-06/BF	Cable Module	300.	100.	66
BC08J-06/BF	H856 to M953 40 CND 3M 6'	125.	80.	36
BC08J-10/BF	H856 to M953 40 CND 3M 10'	180.	90.	50
BC08J-15/BF	H856 to M953 40 CND 3M 15'	215.	100.	53
BC08J-25/BF	H856 to M953 40 CND 3M 25'	250.	110.	56
BC08J-50/BF	Cable IO PDP8E	300.	135.	55
BC08K-06/BF	H856 to M955 40 CND 3M 6'	250.	100.	60
BC08K-15/BF	H856 to M955 40 CND 3M 15'	300.	125.	58
BC08M-0M/BF	H807 to H807 Mylar 11"	250.	120.	52
BC08R-08/BF	H856-H856 3M REV 8'	68.	35.	48
BC08R-20/BF	H856-H856 3M Cable (20')	90.	55.	38
BC08S-05/BF	H856-H856 3M Strait, 5 FT	60.	30.	50
BC08S-06/BF	H856-H856 40 Cond, Cable 6 FT	62.	32.	48
BC09B-07/BF	Cable M912 12FT	1,936.	800.	58
BC09B-10/BF	I/O Bus M912 Cable 10 FT	1,963.	825.	57
BC09B-12/BF	I/O Bus M912 to M912, XXFT	2,000.	875.	56
BC10K-05/BF	Cable 5 FT., Quick Latch	2,373.	1,400.	41
BC10K-10/BF	10 MEM BUS Cable 10 FT.	2,551.	1,500.	41
BC10K-15/BF	10 MEM BUS Cable, 15 FT	2,725.	1,650.	39
BC10K-25/BF	PDP 10 MEM BUS Cable	3,073.	1,875.	38
BC10K-35/BF	PDP 10 MEM BUS Cable	3,443.	2,100.	39
BC10L-35/BF	AMP Quick Latch to (5) W021 Cable	2,750.	800.	70
BC11A-02/BF	External Unibus 2'	135.	90.	33
BC11A-05/BF	External Unibus 5'	155.	110.	29
BC11A-06/BF	External Unibus 6'	160.	115.	28
BC11A-08/BF	External Unibus 8'	170.	125.	26
BC11A-10/BF	External Unibus 10'	182.	130.	28
BC11A-15/BF	External Unibus 15'	210.	160.	23
BC11A-17/BF	Special Cable 17FT	215.	170.	20
BC11A-20/BF	External Unibus 20'	220.	175.	20
BC11A-25/BF	External Unibus 25'	230.	180.	21
BC11A-35/BF	External Unibus 35'	400.	300.	25
BC11A-50/BF	External Unibus 50'	450.	350.	22
BC11K-25/BF	H856 1 End 20 Pair 25'	180.	90.	50
BC11S-25/BF	H856 TO H856 18 TW PR 25'	138.	90.	34
BC11S-50/BF	H856 TO H856 18 TW PR 50'	173.	125.	27
BC11S-A0/BF	H856 TO H856 18 TW PR 100'	277.	190.	31
BC20Y-25/BF	TU58 Cable, 25 FT.	120.	45.	62
BC20Z-25/BF	TU58 Cable, 25 FT.	120.	45.	62
BC21S-25/BF	VK170 10 Pin Comm Cable	120.	40.	66
BC22A-10/BF	Null Modem RS 232 C 10'	48.	30.	37
BC22A-25/BF	Null Modem RS 232 C 25'	55.	40.	27
BC22A-35/BF	Null Modem RS 232 C 35'	65.	50.	23
BC22A-50/BF	Null Modem RS 232 C 50'	80.	60.	25
BC22B-10/BF	RS232C Male to Fem 14 CND 10'	55.	30.	45
BC22B-25/BF	RS232C Male to Fem 14 COND 25'	65.	40.	38
BC22B-35/BF	RS232C Male to Fem 14 COND 35'	75.	55.	26
BC22B-50/BF	RS232C Male to Fem 14 COND 50'	90.	60.	33
BC24C-10/BF	Null Modem Cable	75.	50.	33
BC24C-25/BF	25PIN Fem-10PIN Null Modem 25'	100.	85.	15
BC24Z-A0/BF	Long Line Cable Kit: 100 FT	500.	350.	30
BC24Z-E0/BF	Long Line Cable Kit: 500 FT	1,350.	975.	27
BC24Z-H5/BF	Long Line Cable Kit: 750 FT	1,750.	1,325.	24
BC26B-01/BF	VK100 Y-Cable 1 FT	85.	50.	41
BCV1A-06/BF	6 Foot Cable Ass. (2-3)	250.	160.	36
BCV1B-06/BF	6 Foot Cable Ass. (1-2)	350.	175.	50

Part Number	Description	Regular Price	Sale Price**	% Off
4A-LOTCB-AA/BF	Lot of 5, BC01V-25 (25'Cable)	540.	375.	30
4A-LOTCB-AB/BF	Lot of 10, BC01V-25 (25' Cable)	899.	695.	22
4A-LOTCB-AG/BF	Lot of 5, BC03M-A0 (100' Cable)	616.	425.	31
4A-LOTCB-AH/BF	Lot of 10, BC03M-A0 (100' Cable)	1,116.	750.	35
4A-LOTCB-AJ/BF	Lot of 25, BC03M-A0 (100' Cable)	2,748.	1,695.	38
4A-LOTCB-AK/BF	Lot of 50, BC03M-A0 (100' Cable)	4,997.	3,195.	36
4A-LOTCB-AQ/BF	Lot of 5, BC05C-25 (25' Cable)	543.	425.	21
4A-LOTCB-AR/BF	Lot of 10, BC05C-25 (25' Cable)	1,015.	795.	21
4A-LOTCB-AS/BF	Lot of 25, BC05C-25 (25' Cable)	2,363.	1,895.	19
4A-LOTCB-AT/BF	Lot of 25, BC05C-25 (25' Cable)	4,375.	3,595.	17
4A-LOTCB-BC/BF	Lot of 5, BC05D-25 (25' Cable)	648.	475.	26
4A-LOTCB-BD/BF	Lot of 10, BC05D-25 (25' Cable)	1,197.	895.	25
4A-LOTCB-BE/BF	Lot of 25, BC05D-25 (25' Cable)	2,742.	2,175.	20
4A-LOTCB-BF/BF	Lot of 50, BC05D-25 (25' Cable)	5,152.	3,950.	23
4A-LOTCB-BG/BF	Lot of 5, BC05D-50 (50' Cable)	695.	525.	24
4A-LOTCB-BH/BF	Lot of 10, BC05D-50 (50' Cable)	1,318.	995.	24
4A-LOTCB-BJ/BF	Lot of 25, BC05D-50 (50' Cable)	3,115.	2,375.	23
4A-LOTCB-BK/BF	Lot of 50, BC05D-50 (50' Cable)	5,750.	4,495.	21
4A-LOTCB-CG/BF	Lot of 5, BC11A-02 (2' Cable)	626.	435.	30
4A-LOTCB-CH/BF	Lot of 10, BC11A-02 (2' Cable)	1,186.	850.	28
4A-LOTCB-CJ/BF	Lot of 25, BC11A-02 (2' Cable)	2,800.	1,995.	28
4A-LOTCB-CK/BF	Lot of 50, BC11A-02 (2' Cable)	5,272.	3,895.	26
4A-LOTCB-CL/BF	Lot of 5, BC11A-10 (10' Cable)	846.	625.	26
4A-LOTCB-CM/BF	Lot of 10, BC11A-10 (10' Cable)	1,603.	1,200.	25
4A-LOTCB-CN/BF	Lot of 25, BC11A-10 (10' Cable)	3,785.	2,925.	22
4A-LOTCB-CP/BF	Lot of 50, BC11A-10 (10' Cable)	7,125.	5,595.	21
4A-LOTCB-CQ/BF	Lot of 5, BC11A-15 (15' Cable)	996.	775.	22
4A-LOTCB-CR/BF	Lot of 10, BC11A-15 (15' Cable)	1,886.	1,495.	20
4A-LOTCB-CS/BF	Lot of 25, BC11A-15 (15' Cable)	4,454.	3,650.	18
4A-LOTCB-CT/BF	Lot of 50, B11A-15 (15' Cable)	8,384.	6,995.	16
4A-LOTCB-DB/BF	Lot of 5, BC22A-10 (10' Cable)	228.	140.	38
4A-LOTCB-DC/BF	Lot of 10, BC22A-10 (10' Cable)	436.	260.	40
4A-LOTCB-DD/BF	Lot of 25, BC22A-10 (10' Cable)	1,038.	600.	42
4A-LOTCB-DE/BF	Lot of 50, BC22A-10 (10' Cable)	1,925.	1,095.	43
4A-LOTCB-DF/BF	Lot of 5, BC22A-25 (25' Cable)	262.	190.	27
4A-LOTCB-DG/BF	Lot of 10, BC22A-25 (25' Cable)	498.	360.	27
4A-LOTCB-DH/BF	Lot of 25, BC22A-25 (25' Cable)	1,181.	850.	28
4A-LOTCB-DJ/BF	Lot of 50, BC22A-25 (25' Cable)	2,235.	1,495.	33
4A-LOTCB-DK/BF	Lot of 5, BC22B-10 (10' Cable)	257.	145.	43
4A-LOTCB-DL/BF	Lot of 10, BC22B-10 (10' Cable)	487.	270.	44
4A-LOTCB-DM/BF	Lot of 25, BC22B-10 (10' Cable)	1,151.	650.	43
4A-LOTCB-DN/BF	Lot of 50, BC22B-10 (10' Cable)	2,166.	1,150.	46
4A-LOTCB-DP/BF	Lot of 5, BC22B-25 (25' Cable)	307.	195.	36
4A-LOTCB-DQ/BF	Lot of 10, BC22B-25 (25' Cable)	580.	380.	34
4A-LOTCB-DR/BF	Lot of 25, BC22B-25 (25' Cable)	1,367.	900.	34
4A-LOTCB-DS/BF	Lot of 50, BC22B-25 (25' Cable)	2,568.	1,650.	35
4A-LOTCB-DT/BF	Lot of 5, BC04R-12 (12'Cable)	161.	110.	31
4A-LOTCB-DU/BF	Lot of 10, BC04R-12 (12' Cable)	307.	199.	35
4A-LOTCB-DV/BF	Lot of 5, BC04Z-10 (10' Cable)	243.	165.	32
4A-LOTCB-DW/BF	Lot of 10, BC04Z-10 (10' Cable)	452.	299.	33
4A-LOTCB-DX/BF	Lot of 5, BC04Z-25 (25' Cable)	419.	215.	48
4A-LOTCB-DY/BF	Lot of 10, BC04Z-25 (25' Cable)	777.	410.	47
4A-LOTCB-EB/BF	Lot of 5, BC05F-A0 (Cable In)	915.	350.	61
4A-LOTCB-EC/BF	Lot of 10, BC05F-A0 (Cable In)	1,708.	650.	61
4A-LOTCB-ED/BF	Lot of 5, BC05M-04 (4' Cable)	200.	95.	52
4A-LOTCB-EE/BF	Lot of 10, BC05M-04 (4' Cable)	378.	175.	53
4A-LOTCB-EK/BF	Lot of 5, BC06S-25 (25' Cable)	4,875.	1,995.	59
4A-LOTCB-EL/BF	Lot of 10, BC06S-25 (25' Cable)	9,176.	3,750.	59
4A-LOTCB-EP/BF	Lot of 5, BC07A-25 (25' Cable)	641.	575.	10
4A-LOTCB-EQ/BF	Lot of 10, BC07A-25 (25' Cable)	1,128.	1,095.	2
4A-LOTCB-ET/BF	Lot of 5, BC07D-15 (15' Cable)	649.	395.	39
4A-LOTCB-EU/BF	Lot of 10, BC07D-15 (15' Cable)	1,198.	775.	35
4A-LOTCB-EV/BF	Lot of 5, BC07D-25 (25' Cable)	758.	495.	34
4A-LOTCB-EW/BF	Lot of 10, BC07D-25 (25' Cable)	1,397.	950.	31
4A-LOTCB-EZ/BF	Lot of 5, BC08S-06 (6' Cable)	298.	140.	53
4A-LOTCB-FA/BF	Lot of 10, BC08S-06 (6' Cable)	566.	275.	51
4A-LOTCB-FD/BF	Lot of 5, BC11S-25 (25' Cable)	647.	425.	34
4A-LOTCB-FE/BF	Lot of 10, BC11S-25 (25' Cable)	1,204.	795.	33
4A-LOTCB-FF/BF	Lot of 5, BC11S-50 (50' Cable)	811.	595.	26
4A-LOTCB-FG/BF	Lot of 10, BC11S-50 (50' Cable)	1,510.	1,095.	27
4A-LOTCB-FH/BF	Lot of 5, BC11S-A0 (100' Cable)	1,297.	925.	28
4A-LOTCB-FJ/BF	Lot of 10, BC11S-A0(100' Cable)	2,415.	1,795.	25
4A-LOTCB-FK/BF	Lot of 5, 70-11212-25 (Cable)	900.	475.	47
4A-LOTCB-FL/BF	Lot of 10, 70-11212-25 (Cable)	1,626.	895.	44
4A-LOTCB-FM/BF	Lot of 5, 70-11212-50 (Cable)	1,134.	625.	44
4A-LOTCB-FN/BF	Lot of 10, 70-11212-50 (Cable)	2,130.	1,195.	43
4A-LOTCB-FX/BF	Lot of 5, BC10K-05 (5' Cable)	11,076.	6,750.	39
4A-LOTCB-FY/BF	Lot of 10, BC10K-05 (5' Cable)	20,570.	12,750.	38
4A-LOTCB-FZ/BF	Lot of 25, BC10K-05 (5' Cable)	46,150.	29,875.	35
4A-LOTCB-GA/BF	Lot of 5, BC10K-10 (10' Cable)	11,905.	7,250.	39
4A-LOTCB-GB/BF	Lot of 10, BC10K-10 (10' Cable)	22,109.	13,995.	36
4A-LOTCB-GC/BF	Lot of 25, BC10K-10 (10' Cable)	49,604.	33,125.	33
4A-LOTCB-GD/BF	Lot of 5, BC10K-25 (25' Cable)	14,365.	9,125.	36
4A-LOTCB-GE/BF	Lot of 10, BC10K-25 (25' Cable)	26,679.	17,900.	32
4A-LOTCB-GF/BF	Lot of 25, BC10K-25 (25' Cable)	59,856.	39,750.	33
4A-LOTCB-GG/BF	Lot of 5, BC10K-35 (35' Cable)	16,066.	9,995.	37
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TABLE 2

68000 Family

Device	Function	Availability
68000	16-bit MPU	now
68008	8-bit 68000	now*
68010	VM processor	now*
68020	32-bit 68000	4 Q 1983
68120	IPC	now
68121	IPC – NR	now
68200	MCU	2 Q 1983
68230	PI/T	now
68430	DMAI	4 Q 1983
68440	DDMA	4 Q 1983
68450	DMAC	now
68451	MMU	now
68452	BAM	now
68454	IMDC	3 Q 1983
68459	DPLL	3 Q 1983
68561	MPCC-II	now*
68562	DUSCC	3 Q 1983
68564	SIO	now*
68590	LANCE	3 Q 1983
68652	MPCC	now
68653	PGC	now
68661	EPCI	now
68681	DUART	now
68881	FPCP	4 Q 1983
68901	MFP	now*

Acronym	Definition
MPU	Microprocessing unit
VM	Virtual machine
IPC	Intelligent peripheral controller
NR	No ROM
MCU	Micro control unit
PI/T	Parallel interface/timer
DMAI	Direct memory access interface
DDMA	Dual direct memory access controller
MMU	Memory management unit
BAM	Bus arbitration module
IMDC	Intelligent multiple disk controller
DPLL	Disk phase lock loop
MPCC	Multiprotocol communications controller
DUSCC	Dual channel universal communications controller
SIO	Serial input/output
LANCE	Local area network controller for Ethernet
PGC	Polynomial generator and checker
EPCI	Enhanced programmable communications interface
DUART	Dual universal asynchronous receiver/transmitter
FPCP	Floating point coprocessor
MFP	Multifunction peripheral

*Devices made available in fourth-quarter 1982. May still be in sampling quantities.

To conserve pins on the LANCE, addresses and data are multiplexed, thus allowing the interface to be housed in a 48-pin package.

Intelligent multiple disk controller (IMDC) is a disk controller intended for use with Winchester drives currently available at reasonable costs. This part supports the SA-1000/ST506 type of interfaces, as well as SA-800 floppy disk drives. Any combination of up to four disk drives can be interfaced to the controller at one time, allowing both hard and floppy disks to be controlled simultaneously. This flexibility makes it easy to back up hard disks since, to the controller, the floppy disk appears hard. In such a case, the backup operation becomes simply a sector to sector copy operation.

The back end of this controller is built around an intelligent DMAC. As a result, it has the ability to do file transfers to and from buffers that are at arbitrary locations in memory. The IMDC is scheduled for introduction in third-quarter 1983.

Another disk oriented support chip that can be expected in 1983 is the MC68459 disk phase lock loop circuit (DPLL). The MC68459 is a very fast digital phase locked loop that performs data/clock separation on the incoming data stream from a Winchester disk. The input provided to the DPLL is the composite data/clock signal from the disk drive. The output is a separated data signal with a synchronized clock signal. These two signals are important to the IMDC chip since it requires separate data and clock inputs. The DPLL is built in high performance metal oxide semiconductor technology, and will synchronize and separate a data stream of up to 20M bps. Its introduction is scheduled for third-quarter 1983.

The MC68440 dual DMA (DDMA) controller is the smaller, lower cost version of the MC68450 DMA controller. It is identical to the MC68450 with the exception of its support for only two channels of operation. It does not support the exotic chaining modes that the MC68450 does, either. The MC68440 is plug compatible with the MC68450, but does not have active signals that correspond to the third and fourth DMA channel handshakes. The DDMA can be expected in fourth-quarter 1983.

By expanding the 68000 family of chips, both upscale and down, the scope and depth of the product line is extended (see Table 2). This results in a chip family with such advantages as increased peripheral support and cost-effectiveness. Further, because of the broad spectrum of sophistication existing within the family, alternative choices are available to the designer.

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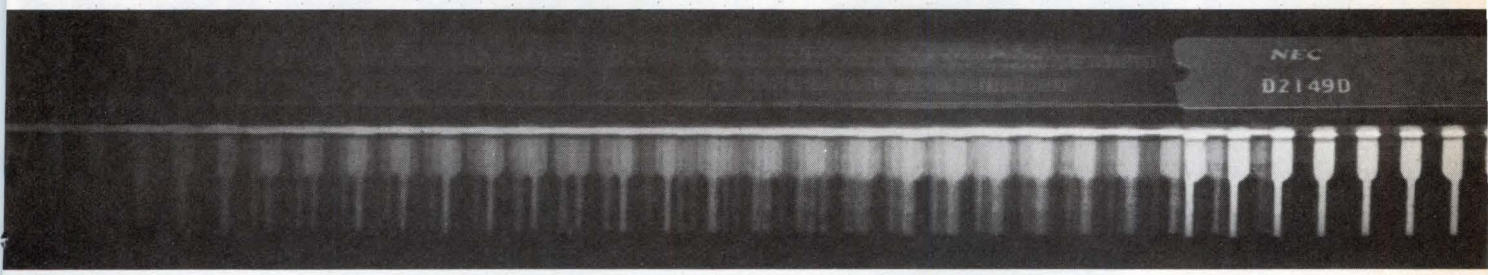

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CIRCLE 46

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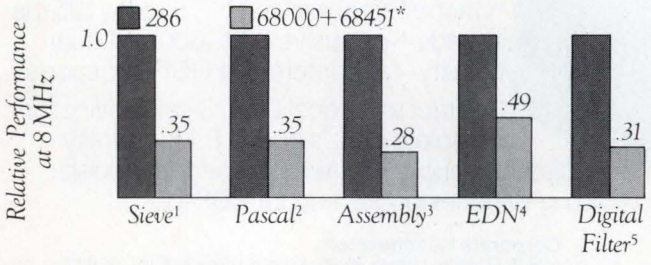
Performance Comparisons



*Performance adjusted to reflect indicated system configuration. Details available from Intel. [1]"A High Level Language Benchmark," Byte. Sept., 1981. [2]"A Performance Evaluation of the Intel iAPX 432," Computer Architecture News. June 1982. [3]"16 Bit Microprocessor Benchmark Report," Intel Corporation, 1981. [4]"16 Bit Microprocessor Benchmarks," EDN, Sept., 1981. [5]"Digital Filter Implementation on 16 Bit Microprocessors," IEEE MICRO, Feb., 1981.

And to simplify sophisticated system development even further, there's an integration of performance-critical functions. Such as task switching, interrupt handling and O.S. call.

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System Comparisons

	iAPX 286 System	*68000 + 68451* System*	*Advantages of Integrated Memory Management & Protection*
Typical System (16 Users)	*1 CPU*	*1 CPU 1-4 MMU's 2 Transceivers 1 MMU Selector*	*Less Board Space*
Wait States Required 8 MHz	*0. W.S.*	*2. W.S.*	*Higher Performance*
Task Switch Overhead	*22 μS*	*>120 μS*	*Faster Response*
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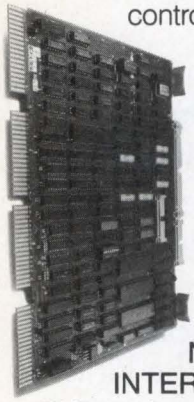

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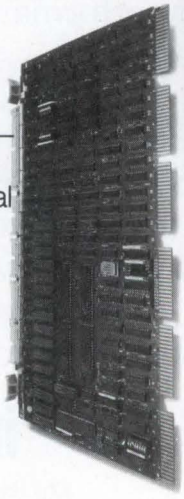

NEW—SMD INTERFACE COMPATIBLE—Model DU218—Full RM02/RM05/RP06 media compatibility—interfaces PDP-11/04 through 11/60 computers with up to four Winchester, or CDC9762/9766 equivalent disc drives employing industry standard SMD interface, as well as Memorex 677/RP06 type drives—includes three sector buffering, 32-bit ECC and dual port capability.

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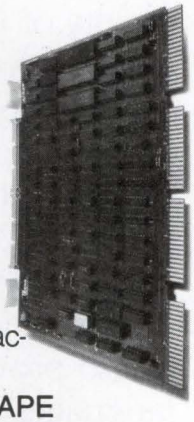

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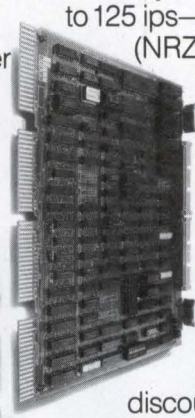

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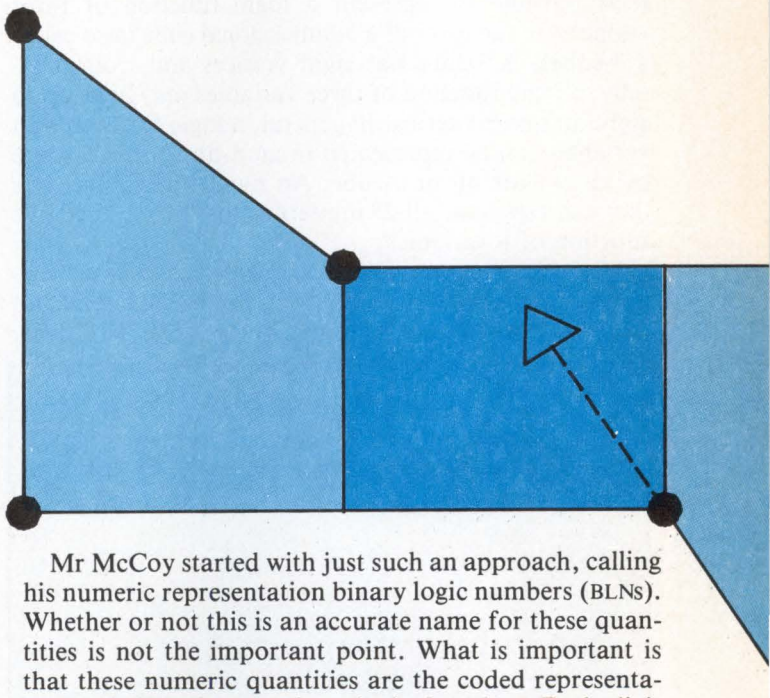
MINIMAL SOLUTIONS TO LOGICAL DILEMMAS

While there is more to simplifying logic equations than ABC, designers must remember that minimized logic functions do not necessarily imply minimal hardware configurations.



by Saul B. Dinman

*In the panel entitled "Genesis" that accompanied Edward Glenn McCoy's article, "The ABCs of Simplifying Logic Equations, Simply" (*Computer Design, *July 1982, p 99), I stated the theoretical basis for a topological algorithm that can be realized by numerical methods on a computer. Mr McCoy's article presented just such an implementation, although no such direct support was offered either by Mr McCoy or by myself. Reader response (see this month's Letters to the editor, p 22) prompted me to offer some mathematical basis for Mr McCoy's technique.*

To deal adequately with the operations and results in a 2-valued logic system requires at least a 3-valued system. That is, a variable may exist in asserted or true form, in negated or false form, or it may have been eliminated altogether from a logical expression. Thus, in the following function of three variables

$$f(A, B, C) = \overline{A}B\overline{C} + \overline{A}\overline{B}C + A\overline{B}C$$

a logical choice of numeric representation for the minterms might be 3-digit decimal numbers with a digit 0 representing a negated variable and the digit 1 representing an asserted term.

Saul B. Dinman is editor in chief of Computer Design, 119 Russell St, Littleton, MA 01460. In 1968 Mr Dinman founded GRI Computer Corp in Newton, MA, where he worked as an engineering executive. He has a total of 25 years of systems hardware and software experience. Mr Dinman has a BSEE from Pennsylvania State University.

Mr McCoy started with just such an approach, calling his numeric representation binary logic numbers (BLNs). Whether or not this is an accurate name for these quantities is not the important point. What is important is that these numeric quantities are the coded representations of the minterms in a logic function. Each digit position corresponds to a different variable, and the use of a 1 or a 0 as the digit value represents the variable's logical state. Thus, the terms in this function would be represented by the numeric list

010, 001, 101

Whether or not you deal with these representations as decimal or even binary quantities depends upon the implementation of the basic algorithm chosen.

Before looking at the algorithm in more detail, consider the logic function

$$f(A, B, C) = A\overline{C} + \overline{B}C + A\overline{B}\overline{C}$$

Obviously, some method of representing the missing variables B and A in the function's first two terms is needed. If a binary system were chosen to represent the function, problems would now surface. There is no convenient way to maintain the representation of the three variables or their logical states. In addition, some variables are or may be missing from the function's

terms, making it necessary to resort to a second list of numeric quantities. These quantities would represent, for example, those variables that have dropped out of the terms.

With the decimal system, other digits beyond the 0 and 1 are available. For example, you can represent the function just described by using the digit 2 to represent an asserted variable in a function that has two out of three terms present. A digit 1 can be used to indicate that a variable has disappeared (if a digit 2 is present anywhere in the term), while the digit 0 continues to represent a negated variable. Thus, the numeric list representing the sample function becomes

210, 102, 100

The choice of any such representation is obviously dependent upon the numeric method developed to implement the algorithm.

Representing a logic function in space

It is possible to represent a logic function of three variables in the form of a 3-dimensional cube (also called a 3-cube). A 3-cube has eight vertices and, coincidentally, a logic function of three variables may have up to eight unique minterms. In general, a logic function of n variables can be represented in an n-dimensional space by all or part of an n-cube. An n-cube has 2^n vertices that can represent all 2^n minterms possible in any logic function of n variables.

Fig 1 is a representation of the logic space for a function of three variables and indicates both the logical and numeric representations of all eight possible minterms.

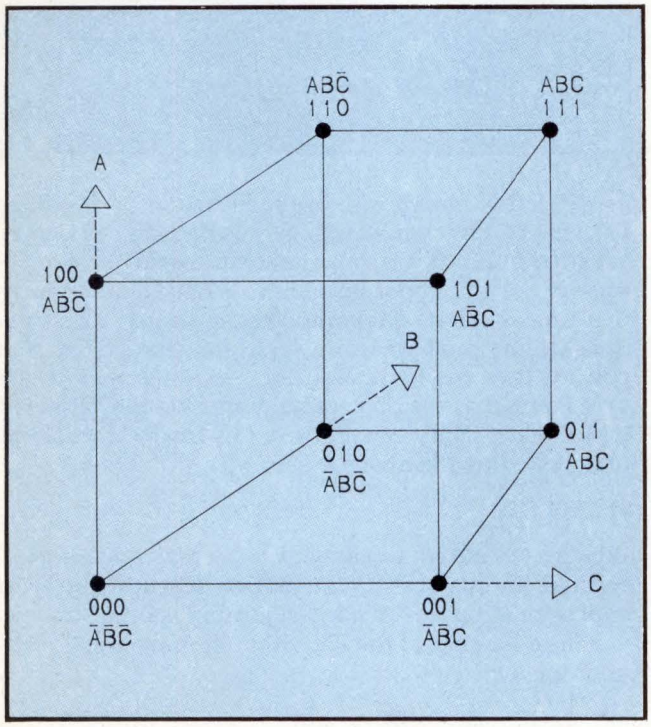


Fig 1 Three-space representation of all eight minterms of a logic function of three variables.

The topological algorithm for simplifying logic functions, termed the Star algorithm, states that two minterms (vertices of the n-cube) can be covered by a 1-cube if they are adjacent or colinear. In other words, colinear vertex pairs can have a line drawn between them, which represents the function's next higher level of simplification. Closer examination of Fig 1 shows that any adjacent or colinear vertex pair differs from another pair only by one logic variable. As shown by the numeric representations of these minterms, colinear vertex pairs have a decimal arithmetic difference of 1, 10, or 100 in a function of three variables. In a function of four variables (4-space), colinear vertex pairs have decimal arithmetic differences of 1, 10, 100, 1000, and so on. The 1 in the difference term represents the logic variable that disappears in the next level of simplification—the line constructed between the vertex pairs according to the simplification algorithm.

Now, an arithmetic representation for the next higher order cube (the 1-cubes) must be determined. In the colinear vertex pair (110, 111), the difference term is 001 and the sum term is 221. Having now moved to the next level of simplification, and also to the next higher dimension in the 3-space, the digit 2 is appropriate to represent the asserted variables on this level. It is also appropriate that a digit 1 represent the missing variable. Thus, the term 221 translates into ABX, where the X merely indicates that the variable C has disappeared in the simplification. Similarly, the numeric representations of 1-cubes in Table 1 can be directly determined by examining the sums of their component vertices.

TABLE 1

Numeric Representation of
$f(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

Vertex Pair	Difference	Sum	Logic Representation
(100, 110)	010	210	$A\bar{C}$
(001, 011)	010	012	$\bar{A}C$
(000, 001)	001	001	$\bar{A}\bar{B}$
(000, 010)	010	010	$\bar{A}\bar{C}$

Fig 2 shows the numeric and logical representations of all of the 12 possible 1-cubes that can be constructed from the 8 vertices in a 3-space. Note that it is now

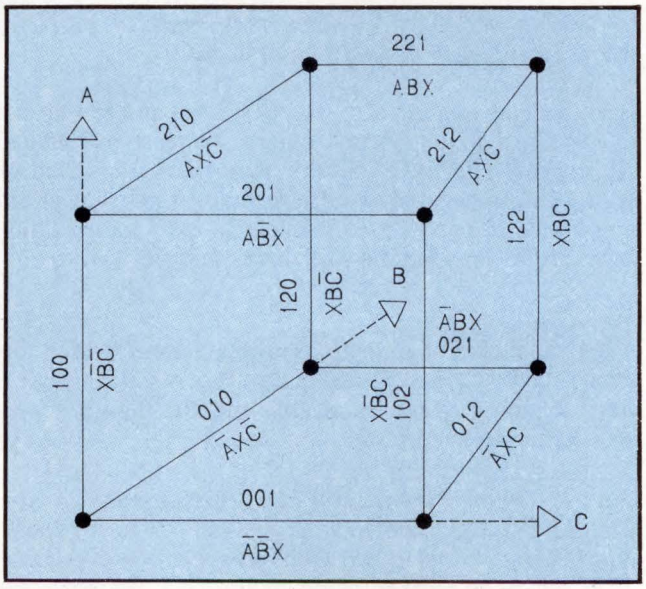


Fig 2 Three-space representation of all twelve 1-cubes that can be formed from the eight possible minterms of a logic function of three variables.

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Circle 51 for Literature

Circle 52 for Demonstration

necessary to keep track of the dimensional level of simplification to which you have moved. In other words, the sum terms of the last two entries in Table 1,001 and 010, are indistinguishable from minterms and 0-vertices. You know only that the term was generated from the combination of two vertices and therefore must be a 1-cube representation. Part of the algorithm implementation, therefore, must include maintaining separate lists of cubes generated in each dimension.

In the next level of algorithm simplification, you must search sets of 1-cubes and look for coplanar pairs—pairs of 1-cubes lying in opposite sides of the same plane that might be opposite sides of the same surface. Two coplanar pairs of 1-cubes—four in all—are necessary to allow construction of a surface or 2-cube that covers all four of the 1-cubes.

Fig 3 shows several selected 1-cubes and two constructed surfaces or 2-cubes. The 1-cube pairs (210, 212) and (201, 221) are coplanar and form a surface. Similarly, the 1-cube pairs (001, 201) and (100, 102) are coplanar and form another surface. The 1-cube pair (010, 012) is also coplanar, but forms only half of a surface. The difference and sum technique previously described can also be used here to discover coplanar pairs of 1-cubes, as shown in Table 2.

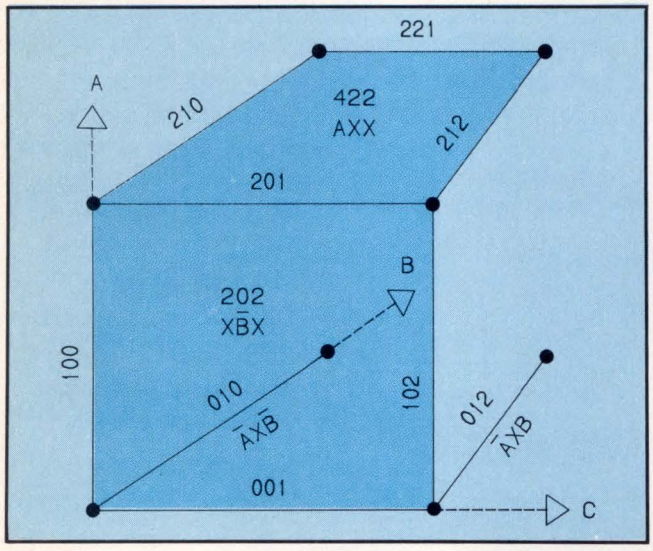


Fig 3 Three-space representation showing combination of coplanar 1-cubes to form surfaces.

TABLE 2

Numeric Generation of 2-cubes from 1-cubes Discovered in Table 1

Vertex Pair	Difference	Sum	Logic Representation
(210, 212)	002	422	A
(201, 221)	020	422	A
(001, 201)	200	202	$\overline{B}$
(100, 102)	002	202	$\overline{B}$
(010, 012)	002	022	$\overline{A}$

The difference terms that indicate coplanar 1-cubes are 002, 020, and 200, respectively. Similarly, differences in a 4-space between coplanar 1-cubes would be 0002, 0020, 0200, and 2000. The sum terms of coplanar pairs of 1-cubes are the same if it is possible to form a surface or 2-cube from them. Thus, two surfaces can be formed

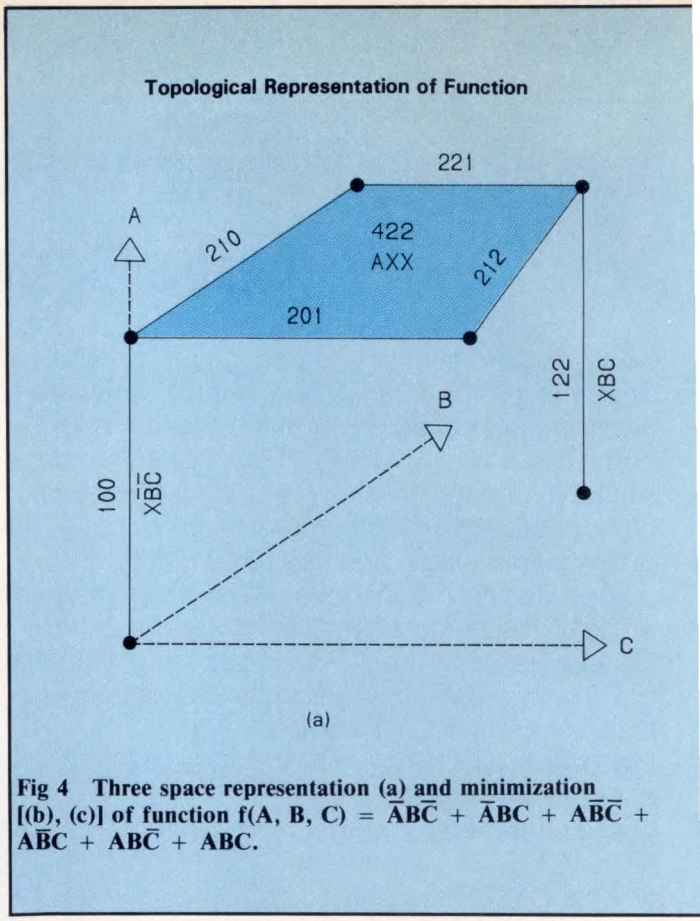


Fig 4 Three space representation (a) and minimization [(b), (c)] of function f(A, B, C) = $\overline{A}\overline{B}\overline{C}$ + $\overline{A}BC$ + $A\overline{B}\overline{C}$ + $A\overline{B}C$ + $AB\overline{C}$ + ABC.

from the 1-cubes in Table 2: 422 and 202, respectively. The appearance of a digit 4 indicates a move to the next level or dimension, and now represents the asserted variable. Of course, the digit 0 still represents a negated variable, and 2s represent variables that have been eliminated from the term. The 1-cube pair (010, 012) can be used to generate the surface 022, if the corresponding coplanar pair (001, 021) is present. Since it is not, the 1-cubes 012 and 010 represent the best simplification possible for those particular terms.

Implementing the algorithm

In expressing a numeric method to implement the algorithm, the first step is to find a scheme that permits easy discovery of n-cubes that can be covered by constructing (n + 1) cubes from them. Fig 4(a) represents a logic function of three variables around which to develop the implementation. If the vertices are structured in ascending numeric order, all adjacent pairs can be discovered by simply subtracting each higher order vertex from the lower order ones in turn and watching for the differences 001, 010, 100 that indicate adjacent vertices as shown in Fig 4(b). Hence, the ordered list of 0-cubes is

0-cube	Minterm
000	$\overline{A}\overline{B}\overline{C}$
011	$\overline{A}BC$
100	$A\overline{B}\overline{C}$
101	$A\overline{B}C$
110	$AB\overline{C}$
111	ABC

No uncovered 0-cubes are found when scanning the list of covered 0-cubes in Fig 4(b). Therefore, you must move to the next level to search for coplanar 1-cube

Discovery of 1-cubes in Function

Pair	Difference	Sum (1-cube)	Covered 0-cubes
		Vertex 000	
(000, 011)	011	not colinear	
(000, 100)	100	100	000, 100
(000, 101)	101	not colinear	
(000, 110)	110	not colinear	
(000, 111)	111	not colinear	
		Vertex 011	
(011, 100)	089	not colinear	
(011, 101)	090	not colinear	
(011, 110)	099	not colinear	
(011, 111)	100	121	011, 111
		Vertex 100	
(100, 101)	001	201	100, 101
(100, 110)	010	210	100, 110
(100, 111)	011	not colinear	
		Vertex 101	
(101, 110)	009	not colinear	
(101, 111)	010	212	101, 111
		Vertex 110	
(110, 111)	001	221	110, 111

(b)

Discovery of 2-cubes in Function

Pair	Difference	Sum (2-cube)	Covered 1-cubes
		Vertex 100	
(100, 122)	022	not coplanar	
(100, 201)	101	not coplanar	
(100, 210)	110	not coplanar	
(100, 212)	112	not coplanar	
(100, 221)	121	not coplanar	
		Vertex 122	
(122, 201)	079	not coplanar	
(122, 210)	088	not coplanar	
(122, 212)	090	not coplanar	
(122, 221)	099	not coplanar	
		Vertex 201	
(201, 210)	009	not coplanar	
(201, 212)	011	not coplanar	
(201, 221)	020	422	201, 221
		Vertex 210	
(210, 212)	002	422	210, 212
(210, 221)	011	not coplanar	
		Vertex 212	
(212, 221)	009	not coplanar	

(c)

pairs. Ordering the list of discovered 1-cubes in ascending sequence results in

1-cube	Logic term
100	$\bar{B}\bar{C}$
122	BC
201	$A\bar{B}$
210	$A\bar{C}$
212	AC
221	AB

The same technique is used to search for coplanar pairs of 1-cubes as shown in Fig 4(c). Reviewing the results in Fig 4(c) reveals one 2-cube, 422, that has covered the 1-cubes 201, 221, 210, and 212. This leaves the 1-cubes 100 and 122 uncovered. The final form of the function is therefore represented by the lists

0-cubes	1-cubes	2-cubes
none	100 ($\bar{B}\bar{C}$)	422 (A)
	122 (BC)	

Translating the lists back into logic terms

$$f(A, B, C) = \bar{B}\bar{C} + BC + A$$

Guaranteeing a minimal function

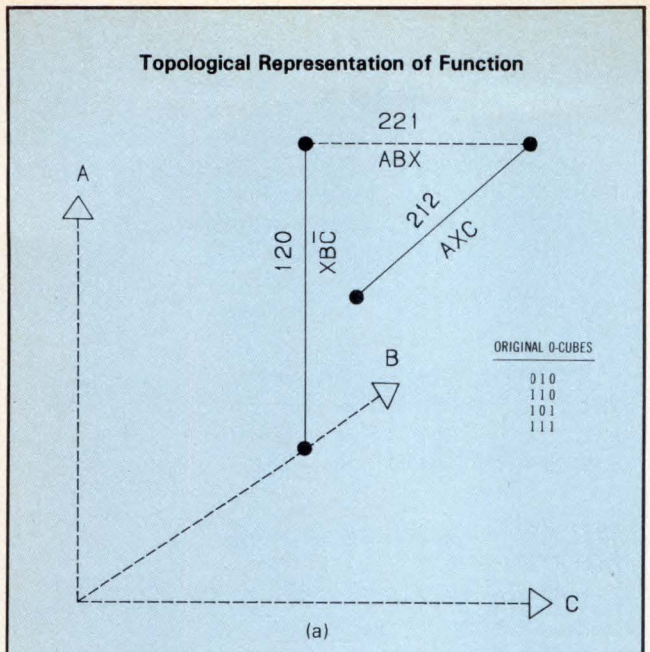
In response to Mr McCoy's article, Mr Guerrero selected an example that he claims does not work with Mr McCoy's algorithm. In response to Mr Guerrero's claims, Mr McCoy pointed out that he did not state that the algorithm produces an absolute minimal function. As evidenced in the preceding examples from which the implementation was developed, the method finds *all* higher order cubes that can be constructed from lower order cubes, even if the lower order cubes were already covered. Yet, the algorithm's topological nature requires that all of the higher order cubes be constructed in order to discover if further minimization is possible.

A final step is required to select the minimal solution after all possible higher order cubes have been constructed. The solution must be chosen from the lists of cubes, highest order first, and selection must stop if all of the (n − 1) cubes have been covered by the selection of n-cubes. Inclusion of (n − 1) cubes in such a case merely adds redundant terms that are already expressed by the n-cubes. This is not necessarily a bad or improper minimization strategy. The fact is, minimization of a logic function in a design environment is a strategy that does not always result in the absolute minimum.

The function that Mr Guerrero posed as a nonworkable case is expressed in the 3-space shown in Fig 5(a). Note that three 1-cubes can be constructed from the three vertices. This is indeed a minimized version of the function, but only the 1-cubes 120 and 212 are required to cover all three of the vertices and produce an absolute minimal function. To build absolute minimization into the algorithm necessitates a search for covered 0-cubes [see Fig 5(b)].

There are no more higher order cubes that can be constructed from the collection of remaining 1-cubes; the end of possible minimization has therefore been reached. In attempting to choose a minimal representation of the function, the final list of 1-cubes must be scanned along with the list of 0-cubes covered by the 1-cubes. The 0-cubes are crossed off the list of original 0-cubes until there are none left as shown in Fig 5(c).

The first two 1-cubes cover all of the original minterms and are a minimal representation of that function. If this step had been performed by the calculator program



(a)

Minimization Passes

First pass

Pair	Difference	Sum (1-cube)	Covered 0-cubes
(010, 101)	091	not colinear	
(010, 110)	100	120	010, 110
(010, 111)	101	not colinear	

Second pass

(101, 110)	009	not colinear	
(101, 111)	010	212	101, 111

Third pass

(110, 111)	001	221	110, 111

(b)

Final pass

1-cubes	Covered 0-cubes	Remaining 0-cubes
		010, 101, 110, 111 (original 0-cubes)
120	010, 110	101, 111
212	101, 111	none
221	110, 111	redundant solution

(c)

Fig 5 Three-space representation (a) and minimization [(b), (c)] of function f(A, B, C) = $\overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C} + ABC$.

offered by Mr McCoy, the result would have been a truly minimal solution. The minimized function then is

$$f(A, B, C) = B\overline{C} + AC$$

Programs always have bugs

Someone once said that no program is ever completely debugged; it only approaches a bug-free state. Although Mr McCoy intended to show that a minimization technique can be developed for a programmable environment, his method has some bugs in it. His program does indeed produce the correct results for his own samples and even for the redundant term mentioned by Mr Guerrero. It does not, however, work for the cases where the minimum function has cubes of different orders in the final result. For example, feeding the data from the example in Fig 4 to the program will produce only the single 2-cube A as an answer. The method completely loses the two 1-cubes not covered by the 2-cube A—because Mr McCoy did not account for the covered cubes as he moved to the next level of minimization (the next higher order dimension). His program replaces all of the (n − 1) cubes with the n-cubes generated from them. Thus, if all of the (n − 1) cubes are not covered by the n-cubes, part of the final result is lost. In short, the concept proposed by Mr McCoy does work, although the program lacks the logic necessary to complete the implementation.

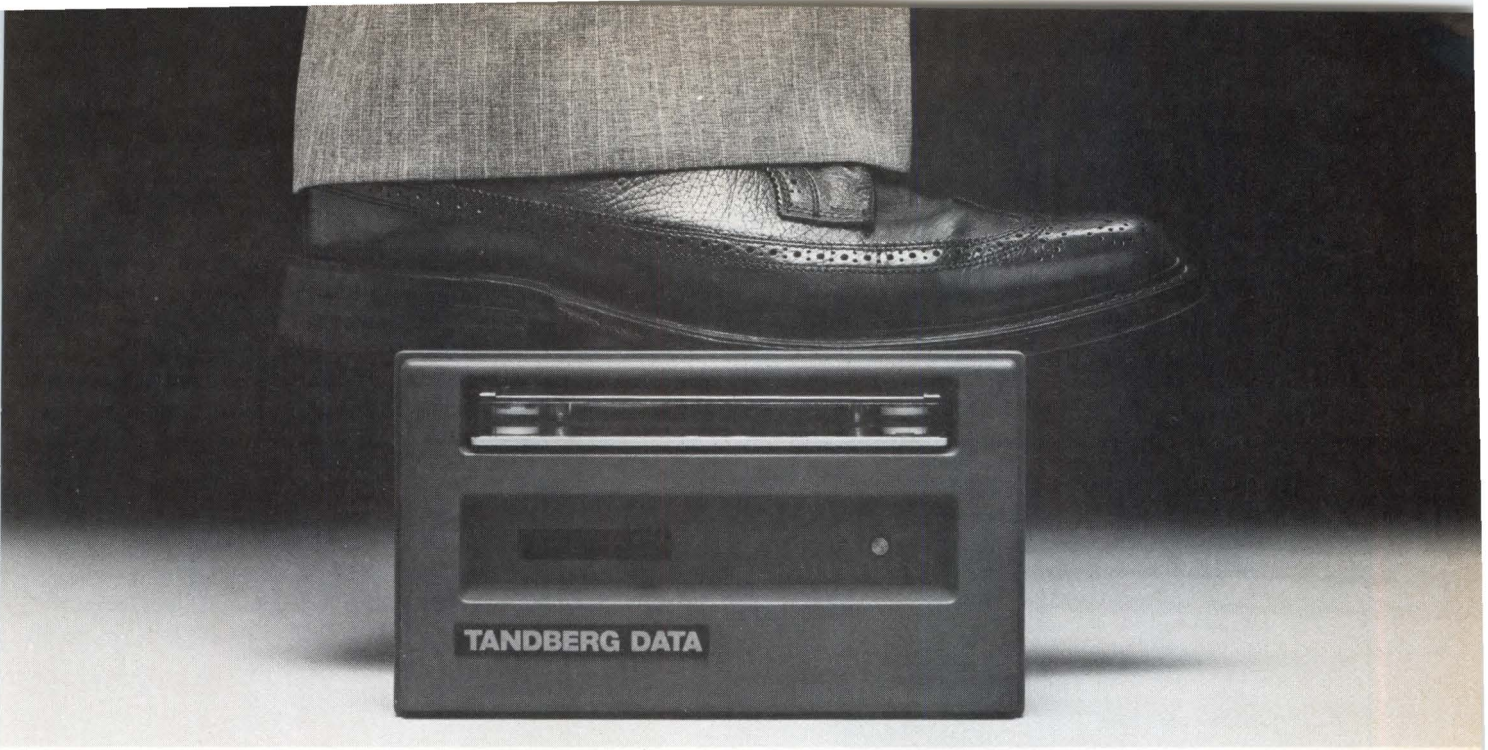
To correct the program, additional cube lists must be maintained so that (n − 1) cube coverage can be checked and uncovered cubes can be retained after each minimization level. The 0-cubes are already stored on entry, and an additional list of covered 0-cubes must be generated along with the 1-cubes list. After a complete list of 1-cubes has been formed, the list of covered 0-cubes must be compared to the list of original 0-cubes, and all 0-cubes not in the covered list must be retained on a separate list. The newly generated 1-cubes list becomes the new "input list" to be searched in order to discover 2-cubes that can be formed, and the list of covered 0-cubes can be discarded. Again, a list of covered 1-cubes generated from the list of 2-cubes must be maintained, and after the process is complete, a remainder list consisting of uncovered 1-cubes is formed and retained. Providing a working version of the program is unfortunately beyond the scope of this article.

The minimum is not always the minimum

To assume that the minimization of a logic function always produces a minimal hardware implementation is not always valid. Back in the days of discrete component logic implementations, minimization techniques were held in high esteem because of never-ending efforts to reduce overall hardware costs. With the advent of the integrated circuit and the small, medium, and large scale integration progression that rapidly followed, almost every complex function that a logic designer might need for a given design became available in chip form. The need for any serious minimization techniques rapidly decreased and was all but killed with the appearance of programmable logic arrays. However, with the advent of gate array technology, silicon foundries, and do-it-yourself computer aided design/computer aided manufacturing systems, all of which enable the logic designer to again participate at the gate level of logic design, it is quite certain that interest in minimization techniques will be revived.

When practicing the art of minimization, the absolute minimum solution in logic function terms is not always desirable. Indeed, Mr McCoy's assertion that a competent logician should be able to recognize a minimal solution is partially correct. Sometimes, an intermediate solution—one that deliberately contains redundant terms—is actually the simplest one from a hardware point of view.

Consider, for example, the two versions of the solution to the function in Fig 6. If the absolute minimum is employed, three gates are required. If part of the not-so-minimum function is already available as a logic signal, however, a 2-gate implementation results. Even worse is



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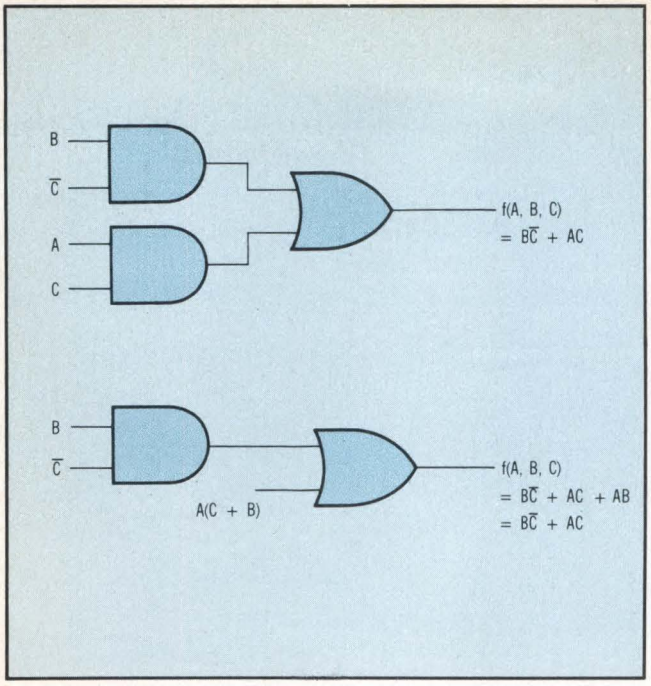

Fig 6 Implementation of function in Fig 5.

the case where the sample function is implemented on a board that has only the signals B, C, and the composite signal A(C + B) available on the board inputs. In this case, to force the implementation of the minimum function would require the presence of the signals A, B, and C on the board inputs, which in turn requires an additional board input as well as attendant backplane path for the extra signal.

Since most complex logic design at the gate level is done by function partitioning, you must consider all of the possible intermediate minimizations of a given function to ensure that the resultant total hardware implementation is, in fact, minimal. If the concept of using one or more redundant terms in an implementation is employed, this may lead to a more economical configuration, particularly since board and backplane pin connections can become a significant part of the cost.

Acknowledgment

I wish to thank J. Paul Roth for his work on the use of topological techniques to minimize logic functions found in "The Star Algorithm," a monograph from the former IBM Applied Mathematics Research Group, Lamb Estates, NY.

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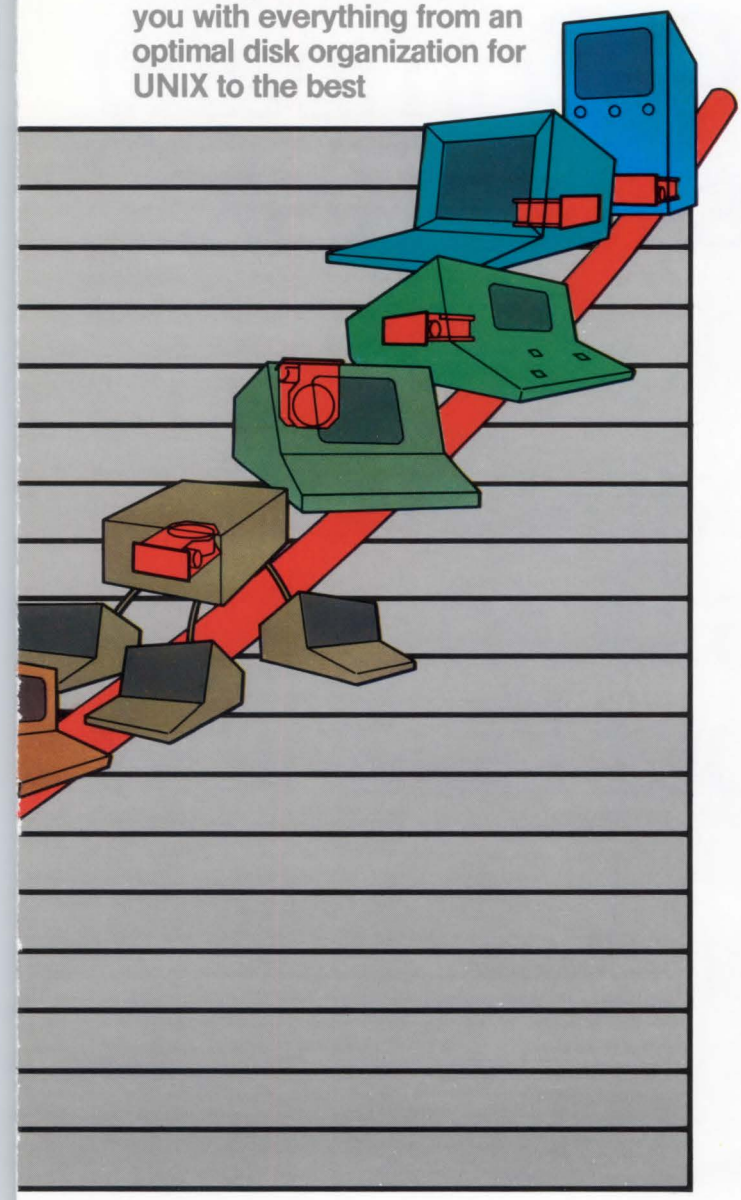

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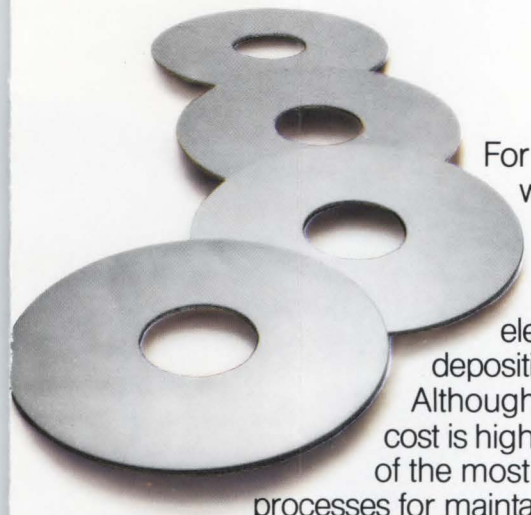

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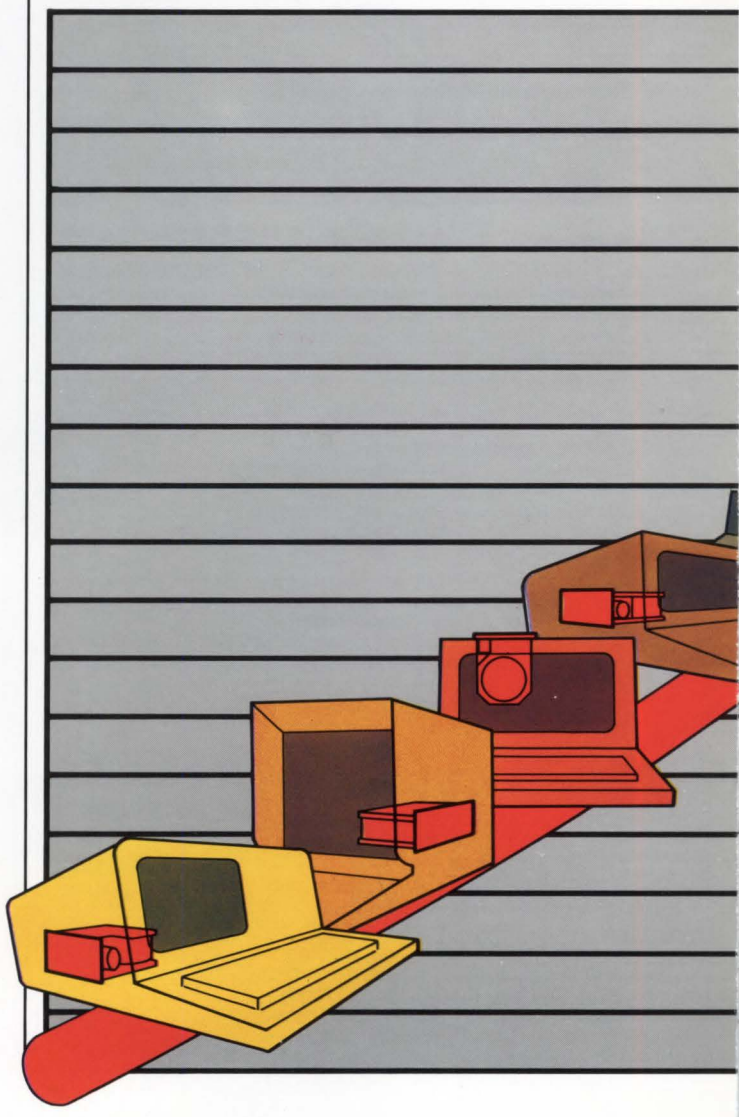

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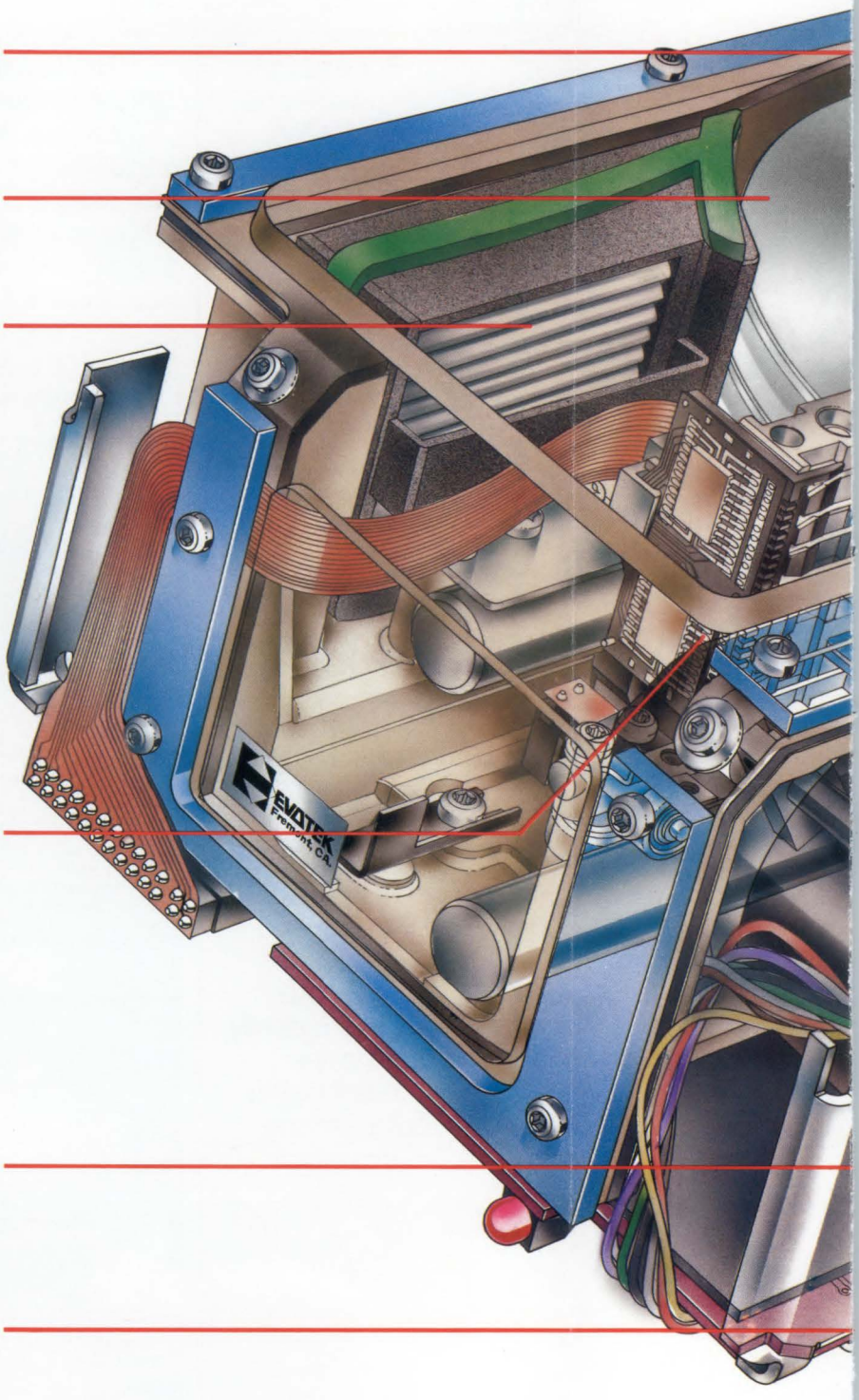

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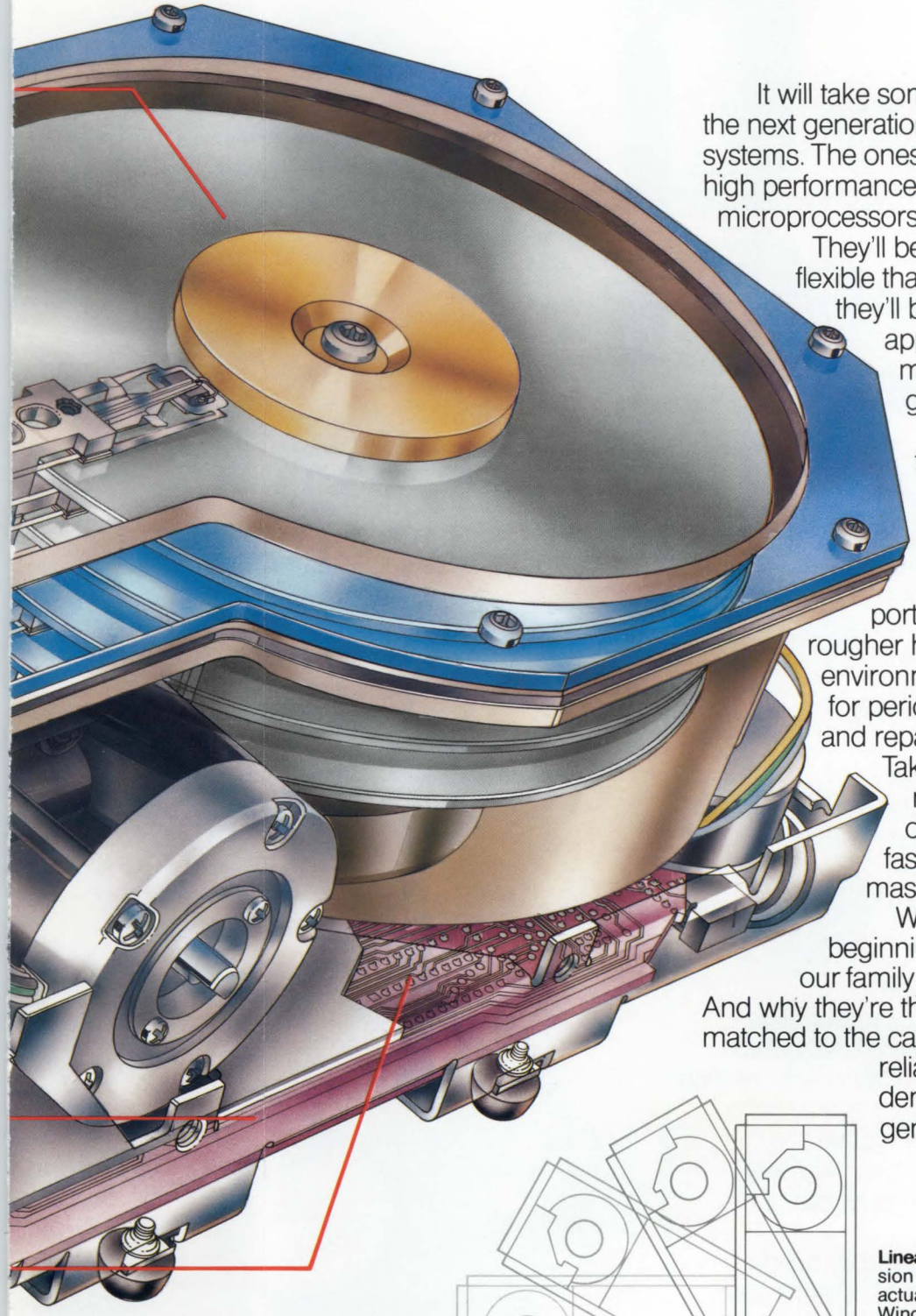

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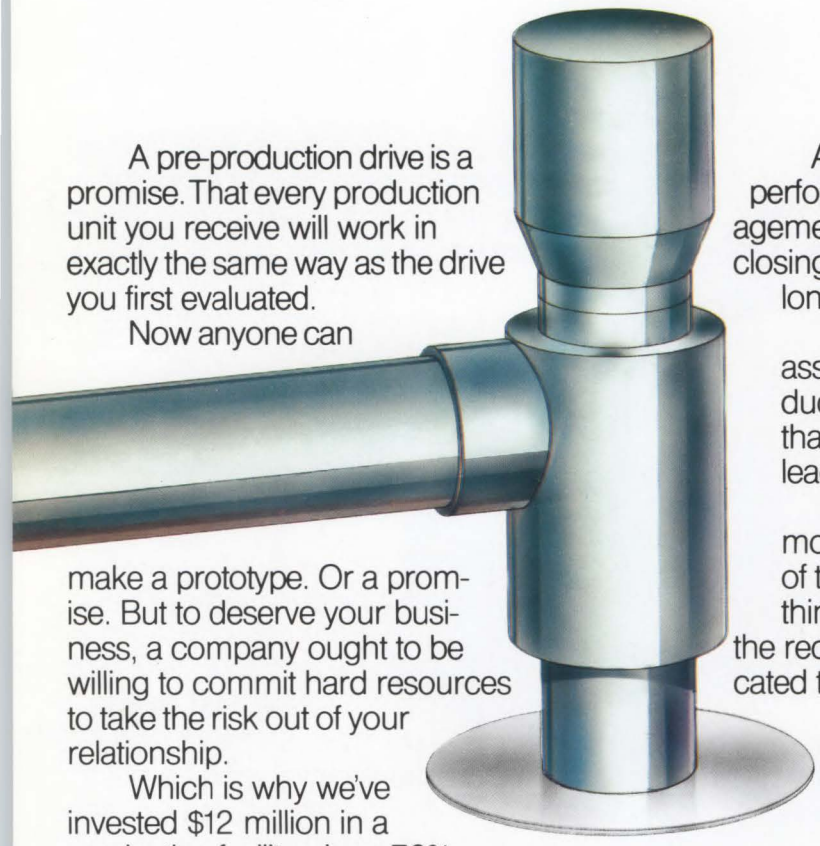

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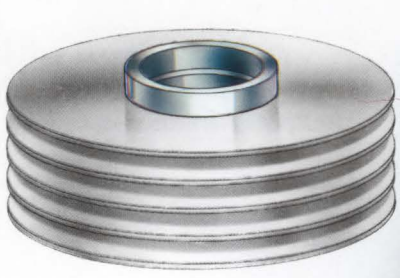

CAN COMPUTERS REALLY BE FRIENDLY?

Determining the criteria for designing user friendly computers requires examining the foibles of human behavior.

by Jack W. Crenshaw and Joseph Philipose

In any discussion about computer support environments, the term "user friendly" invariably arises. But what does user friendly mean? Can user friendliness be measured? Moreover, can a friendly environment help to improve programmer productivity? It can if today's designers of operating systems meet certain criteria. "Friendly," as it is used here, is a kind of barometer that indicates how easily an operator can interact with a computer. If the conditions of friendliness were analyzed carefully, perhaps software environment designs would more closely reflect the desires of the human community that uses them.

Although most experienced programmers have forgotten their initial frustrations, most new users still see today's operating systems as unfriendly. The reasons for the present unfriendliness can be traced to the early days of operating system design. In the beginning, market pressures on the vendor and the attitude of the vendor's customer—the data processing manager—resulted in an operating system design that accommodated the needs of everyone but the user. Even today, vendors develop their operating systems primarily to sell hardware. Development schedules are tight and pushed tighter by hardware delivery dates. The programmers who typically develop operating systems software without a user orientation may even have an anti-user bias. Their motivating force is to meet schedules, not to consider user needs.

Another consequence of this high pressure situation is the degree of traditionalism in operating system design—surprising in a field as young and dynamic as this one. As an example, consider the following syntax for an assembler:

```
< label >":"< op-code >[argument]
```

This syntax, together with the traditional 3-letter operating codes and the names of the pseudo-operation codes, was laid down in 1952 for the IBM 650. Though the form was designed for card formats and internal word lengths in the 650, it is still used 30 years later—without good reason.

Most operating systems are large and complex. Because they evolve only as minor improvements made to previous systems, many characteristics, including the anti-user orientation of the early operating systems, have survived to the present day. To purge these early influences may require some drastic departures from traditional practice.

The advent of the personal computer, however, provides an alternate model, primarily because the customer is also the user. Not surprisingly, personal computer operating systems are more user oriented and seem to be more friendly than commercial systems. Compare, for example, the log-in message of the early TRS-80 from Tandy Corp's Radio Shack—<READY—with Honeywell's MULTICS log-in session reproduced in the Figure. Also compare the clarity of Radio Shack's error message

```
WHAT?
10 for I = 1 TX?  100
```

with Honeywell's

```
SYNTAX ERROR IN REGULAR EXPRESSION
```

Of course TRS-80s cannot replace all MULTICS systems, but the larger systems can emulate the friendly characteristics of personal computers. Designers can achieve a reasonable degree of friendliness on their systems by

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```
please type your terminal identifier
-1066-027-
please log in: <control h> ABCDEFGH;< password >
P14
HOST IS ON LINE

MULTICS MR9.0: Honeywell CNO; Minneapolis, MN
Load = 81.0 out of 160.0 units: users = 81,02/17/82 1016.2 cst
Wed
hoenocheoc
1 Crenshaw
Password:
You are protected from preemption until 1116.
Crenshaw ADVS logged in 2/17/82 1016.6 cst Wed from ASCII
terminal "none"
Last log in 02/15/82 1514.5 cst Mon from ASCII terminal "none."
```

MULTICS log-in session. Compare complex display of user interaction that precedes each session with simple <READY.

simply identifying five system characteristics that tend to be perceived as friendly by users.

Identifying a friendly environment

A computer environment is the combination of hardware and software within a computer, with which a user interacts. It is this combination that ultimately determines user effectiveness and productivity. A friendly computer environment can be viewed in human terms. According to Webster, a "friendly" environment is one that exhibits "kindly interest and goodwill" and is "not hostile." No one responds well to people or machines that either will not or cannot cooperate. When computer systems will not or cannot cooperate, users become ineffective and inefficient. For example, while editing a large source file, the user reaches for the "a" key but strikes "q" instead. Hitting "q" causes the editor to terminate, and the source file is lost. The user's reaction does not need to be described; rage is a universal emotion. This unfriendly act has violated some fundamental human needs that have been ably chronicled by Bach.[1]

- *The need to have our expectations met.* A good portion of users' responses to a situation revolves not around what happened, but what they expected to happen. The degree of reaction depends largely on how justified they feel in their expectations. An unexpected change in the weather evokes little response because, by its nature, weather is unpredictable. On the contrary, machine performance should not be unpredictable.
- *The need for clear information.* Most people feel uncomfortable when they lack information. When the information is available, they use it. When it is unavailable, they do what they have to do to get it. If, however, they feel that the information exists but is deliberately being withheld or obscured, they become hostile or perceive a lack of friendliness.
- *The need to succeed.* Programmed learning courses are premised upon immediate and frequent positive reinforcement. Skinner,[2] in his early experiments on behavior, observed that an action followed by a reward is likely to be repeated in the future, while an action followed by a punishment is less likely to be repeated. For the reward to be effective, it must follow the action within about two seconds. Dwyer[3] developed an interactive algorithm based upon this concept.
- *The right to fail.* As hard as it is to admit, everyone makes mistakes. As a matter of fact, the process of trial and error is a time-honored and effective method of learning. Where computers are concerned, the right of the user to fail implies that errors they may make are tolerable and do not cause catastrophic problems.
- *The need for individuality.* Most people treasure the right to make their own choices. Everything being equal, they prefer to have options. An environment that offers no options, even though it meets all other needs, is a prison.

In other words, interactions with other people or things are perceived as friendly to the extent that they meet, rather than violate, these fundamental needs. A computer environment is no exception.

The man-machine interface

Surprisingly, little research has explored the human reaction to the computer. Studies on programming environments[4,5] concentrate on the functions of programming tools. While it is necessary to have tools that perform well, their functions have nothing whatsoever to do with friendliness. Studies on man-machine interaction, such as Benbasat and Dexter,[6] tend to concentrate on productivity. Few researchers, however, have thought to ask, "How do you feel about this system?"

In the absence of direct information concerning the user's perception of the system, designers are forced to observe the ways users deal with systems to garner information on how users cope. This electronic anthropology can yield surprising observations. The tacit assumption here is that, given options, users will select those approaches that tend to make them the most comfortable or will, at least, minimize their pain. Certain observations are based upon the preceding definition of friendliness.

The average person has a vocabulary of a couple of thousand words. Experiments and observation, however, suggest that far fewer are used in everyday conversation. Similarly, most computer operating systems have a large number of useful commands, yet users regularly work with only a small portion of those commands, as few as twenty. Apparently, there is a definite and fairly small limit to the number of commands that average users can remember. Further, in practice, users stick to those they are sure of. This number increases when the commands are simple and their functions transparent. The users' working vocabularies may also depend on their own tendencies to take risks and their attitudes toward failure. As Dwyer[3] points out, users typically react in one of two ways to too many failures: they either retreat to a familiar subset, or they get off the system altogether.

One of the most interesting and potentially significant observations made in the course of Dwyer's study relates to extensibility. Given a choice, users prefer a system that they can modify and tailor to their needs. Because IBM's System/360 is known as a rigid system, it has few fans. On the other hand, Forth and Smalltalk, two language operating systems specifically designed for extensibility, have wildly partisan supporters.

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CIRCLE 56

Forth, for example, employs a set of primitive commands represented by "words." These words form phrases that combine a number of commands. Typically, Forth words are short—and lend themselves to nested routines. Users can easily check Forth words for errors and also conjoin them to build more complex terms. As this building process proceeds, user vocabulary grows, thus personalizing the program.

Notice how well this process meets the fundamental human needs as defined. Able to rapidly check small commands, users receive the immediate positive reinforcement that encourages further progress. These short, simple commands with simple, reliable functions readily fulfill expectations and, in the process, meet the equally important need for individuality.

This same phenomenon is observable in other more conventional operating systems. Both MULTICS and Bell Labs' UNIX feature command files with executive and shell commands, respectively. Though both sacrifice some performance by using such a user friendly approach, Kernighan[7] reports that over 70% of the programs that are run on UNIX employ shell commands. Many MULTICS users also rely heavily on executive commands.

Current environments require different command syntaxes depending on context. In MULTICS, the command syntax is

<command>["b"<argument>]

However, in PL/1, the base language of MULTICS, it is

"call"<command>"("<argument>","<argument>");"

and in the editor QEDX, it is

<argument>[","<argument>]<command>.

To an expert, these differences in syntax are normal and natural. To a beginner, however, they are confusing and arbitrary.

Ease of syntax is one area in which both Forth and personal computers generally shine. Neither makes any distinction between a command in the command line and one embedded in a program. It may be argued that since different operations are done in a command line, the syntaxes need not necessarily be the same. But, in the face of the success of a language like Forth and the growing use of UNIX's shell commands, this argument has little to support it.

Generally, communication between two people is quite free. Even though a thought can be worded in many different ways, there is a reasonable assumption that the message will be understood. The average computer system, on the other hand, typically has required a rigid and precise format. This is no longer necessary. The computer game "Adventure" pointed the way to a free syntax that, though limited by a 2-word format, gave surprisingly human-like responses. Recent adventure games have an even broader range of input and, correspondingly, exhibit a more human-like behavior.

Another desirable characteristic of human communication is the ability to consider the message's context. A word or phrase may be meaningless or ambiguous when isolated, but by using the context and the direction of the conversation, the communicators can resolve uncertainties. By contrast, communicating with a computer can be like trying to talk with someone who can only remember one sentence at a time.

But again, improvements are possible. Most current systems possess a limited ability to use context; for example, when not specified by the user, the name of a file called up for editing may default to the name of the last file edited. Extension of this ability to retain context, even between separate log-in sessions, is straightforward. Hayes, Ball, and Reddy[8] even suggest that the operating system can be programmed to remember the common spelling errors a given user makes and automatically correct them.

Friendly design factors

By observing the following criteria, the operating system designer can virtually guarantee that the system he authors will be perceived as friendly by its users.

Tools. The friendly computer environment should consist of small, independent tools rather than large, interrelated ones. Each tool should carry out one and only one well-defined function. Discourage the use of "control arguments." Name the tools using common words that describe their functions. Avoid industry jargon. Tools should provide clear default values for all input aguments, as well as make possible errors obvious to the user.

Input commands. A single interface should control all input to a computer's operating system. This will ensure a uniform command syntax. The command language syntax should correspond, as closely as possible, to that of the primary programming language. The command interface should include flexible parsing to accommodate individuality. Specifically, an operating system should permit optional delimiters, interjection of prepositions, and optional positioning of verbs and subjects. A friendly operating system should allow users to edit command lines or correct errors, either prior to entry or after detection of the error.

Output interface. All programming tools should communicate with the user through a single output driver and, to the extent possible, make all output formats uniform. Commands from the user should be answered within the recommended two seconds. The response should indicate the status of the command: completed, working, or error. For commands with several phases, the system should indicate when each phase is completed, and the user should be able to suppress these computer responses.

Extensibility. A friendly operating system should allow users to collect groups of command lines into "command files," which can be invoked by a single command. From the users viewpoint, there should be no distinction between the response required to invoke a command file, like an editor, and the response required for simple commands within system programs. Further, an operating system should have a mechanism for passing data between tools so that the output from one tool may be used by another. The system should process these commands within a command file exactly as though the user had input them from the console.

Context memory. A friendly operating environment should maintain a record of user options and a program's status. This data should be shared by all tools and should conform to user preferences. For example, the mode and options set for a tool should be those set by the user on the previous invocation of that tool, unless the user specifies otherwise. Default values in the

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CIRCLE 57

command line should be taken from the last applicable value used. The command line should be retained for editing and/or repetition, until a new one is output.

Error handling and documentation. No combination of user input should cause an unrecoverable error. The system should report all errors to the user through the same output driver in a uniform format. The system's error messages should be printed clearly and tell the user what is wrong. When an error is reported, the system should display the command line with the error highlighted.

Any error encountered while executing a command should be reported by that command (via the user interface) with an appropriate error message. When the system encounters an error, it should attempt to correct it, if possible. Any such correction should be reported to the user. Any change that could result in irreversible damage to user files should not be executed without user confirmation.

Extensive online documentation and learning aids are necessary. Written documentation should be regarded only as a secondary source of information. In fact, a good measure of friendliness is the extent to which a new user can use the system without the aid of accompanying manuals.

In certain areas, the preceding criteria may appear to require radical departures from current practice, but this is not true. Although most of today's operating systems include carry-overs from earlier systems with limited friendliness, none of these suggestions would require totally scrapping any existing operating system. Designers can meet most of the criteria by using existing systems and developing additional software that serves as a buffer between users and operating systems. While such an approach might sacrifice something in machine efficiency, evidence seems to indicate that the ease of a system's use improves productivity.

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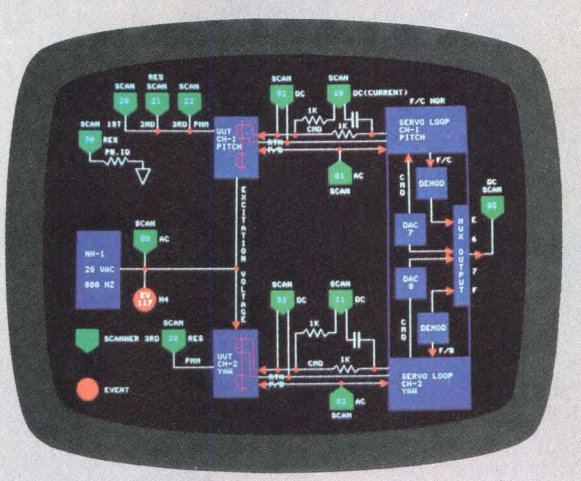

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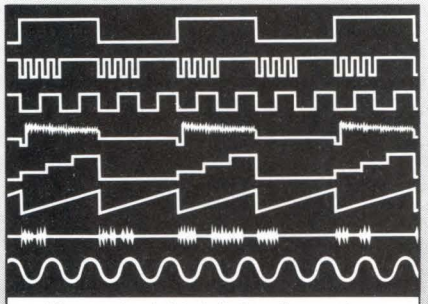

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CIRCLE 60

THE COMMON SENSE OF OBJECT ORIENTED LANGUAGES

Languages like Ada that rely on the manipulation of objects need not be hard to grasp. In fact, most of us already understand the principles upon which they are based.

by Roy S. Freedman

One of the more popular phrases on today's computing scene is "object oriented." The trade press and technical journals have made this a magic term; hardly a month goes by without some proud manufacturer touting his latest object oriented architecture, program, or design.

As might be expected, object oriented means vastly different things to different people. An illustration often used to depict object orientation concepts presents the viewer with a confusing series of items linked by a web of interconnecting arrows. Illustrations such as these, try as they might to inform, usually further obscure the notion of object oriented structures.

In the world of language development, Ada is the most recent example. Where languages and programming are concerned, a certain degree of abstraction is required to understand object orientation. Here, consider an object as any entity that can be abstracted, classified, or categorized by its type. This being the case, objects can belong to and be grouped in abstract or semantic classes. Going one step further, assume each class has an allowable set of operations. These class determined operations can be performed only on the objects that are members of the particular class. Thus, there is a collection of objects belonging to given classes upon which certain operations can be performed, depending on the class affiliation of the object.

No one need be put off by these abstract notions of objects, classes, and operations. They have all been seen before in various scientific and mathematical guises. For instance, early school lessons that pounded the concepts of real, signed, complex, and integer numbers into our consciousness dealt with abstractions similar to those required by object oriented programming languages. Each of these numerical classes contains objects (numbers) that are manipulated by different, allowable operations.

The concepts of object and class can also be illustrated by a simple example from taxonomy—the classification of plants and animals according to their presumed natural relationships. Enter Citation, Fido, and Spot. Specifying "HORSE" and "DOG" as the objects to consider, note this specification as

```
type HORSE is EQUUS_CABALLUS;
type DOG is CANIS_FAMILIARIS;
```

Define horse and dog objects by

```
CITATION:      HORSE;
FIDO,SPOT:     DOG;
```

In this notation, these definitions are read "CITATION is an object of type HORSE," and "FIDO and SPOT are objects of type DOG." Other people may wish to read these definitions as "CITATION is an instantiation (a particular instance) of class HORSE," and "FIDO and SPOT

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are instantiations of class DOG." In other words, CITATION is simply a HORSE object, and FIDO and SPOT are DOG objects. Also, note that associated with the types HORSE and DOG are certain implicit operations that can be performed on HORSE objects and DOG objects. For example, mate two DOG objects with the procedure

```
MATE (FIDO,SPOT);
```

and also mate two HORSE objects with a similar operation or procedure. According to 18th century botanist Linnaeus, however, peforming the operation

```
MATE (CITATION,FIDO);
```

is not allowed because CITATION and FIDO are from different classes and thus are different types. The MATE operation cannot be performed because of class incompatibilities.

Actions and abstractions

Obviously, the act of abstraction consists of two separate actions: first, specifying a particular semantic class of the object; second, defining who or what the object is or does. Abstracting the properties of objects into classes (or types) requires common sense—the only thing confusing about abstraction is the notation dealing with these concepts. As mentioned earlier, mathematicians long ago evolved a notation similar to what has just been shown for specifying objects and types. For example, let NAT denote the set of all natural numbers, and define the "squaring function" as

```
SQR:NAT→NAT
SQR(N) = N*N
```

The first line specifies that SQR is an object of the class of all functions from the natural numbers to the natural numbers. The second line defines what the object is and how it is implemented in terms of the implicitly defined multiply operation (*). In this notation specify SQR by

```
function SQR(N:NAT) return NAT;
```

and define what SQR is and how it is implemented by

```
function SQR(N:NAT) return NAT is
begin
  return N*N;
end SQR;
```

Sometimes it is semantically unnecessary to define the "second line" (the definition or implementation) in an abstraction process. For example, a function that returns a random number given a particular argument can be described by

```
RANDOM:NAT →NAT
```

The second line can either be presented later, if it contains many complex or confusing details, or not at all. That is, if it contains some "trade-secret" formulas, the inventor would not want them to be seen or modified.

Developed in the more traditional branches of mathematics, these concepts of object and type are increasingly being used in computer science and software engineering for the development of programming methodologies. These methodologies are influencing the design of new programming languages. The principal benefits of these concepts of object, class, and operation include

- The improvement of program readability. A human, who wishes to, can determine what is going on.
- The enforcement of "compatibility checks." These can eliminate many semantic errors.
- The ability to create "templates" of program entities. Semantic classes can be used to make general statements and prove properties about the objects they represent.
- The separation of the object's abstract class specification from the object's actual definition. This separation improves readability by avoiding confusing details, for the moment. It also provides some protection against unwanted access or unwanted modification.
- The simplification of the storage allocation issue in shared systems. This occurs if objects of different classes are implemented in different structures instead of the same structure.

Using common sense

The first language and notation that explicitly recognized the object oriented concepts of type and objects was the theory of types developed by B. Russell and A. Whitehead over 70 years ago. Russell and Whitehead observed that their theory has "a certain consonance with common sense which makes it inherently credible." They also felt it to be helpful in resolving many paradoxes and ambiguities that were present in the logical foundations of mathematics.[1] The theory of types survives today in the form of high order predicate logic and is the basis for many of the object oriented concepts found in programming languages.

Another object oriented language that is extremely popular among mathematicians and theoretical computer scientists is category theory, developed about 40 years ago.[2] A category consists of a family of mathematical objects and a set of "morphisms" (allowable operations explicitly defined on the objects). Category theory has strong object oriented properties: the relations between abstract class, allowable operation, and object are precisely specified. Category theory provides the first three benefits listed for the working mathematician. It also provides a mechanism for transforming one category into another. The programming analogy of this would be in the explicit conversions from one object of a given class to another object of a different class.

Programming languages have been rapidly becoming object oriented since the introduction of ALGOL 60[3] and the idea of "type." Many descendants of ALGOL 60 (notably SIMULA[4] and the Smalltalk family[5]) are frequently referred to as object oriented. Unfortunately, this adds to the confusion.

In SIMULA, object and class have particular meanings. A SIMULA class is an abstract program entity that allows for the definition (instantiation) of SIMULA objects (instances). These objects are used for all the benefits listed (with the exception of enforcing compatibility checks), especially for the semantic demands of simulation or concurrent programming.

The Smalltalk language family is based on SIMULA. One interesting property exploited by Smalltalk objects is the ability to pass messages to one another. This is very useful for multitasking applications. Dubbed message passing, this facility has developed into a programming style in its own right. In the Smalltalk vernacular object oriented usually refers to message passing.

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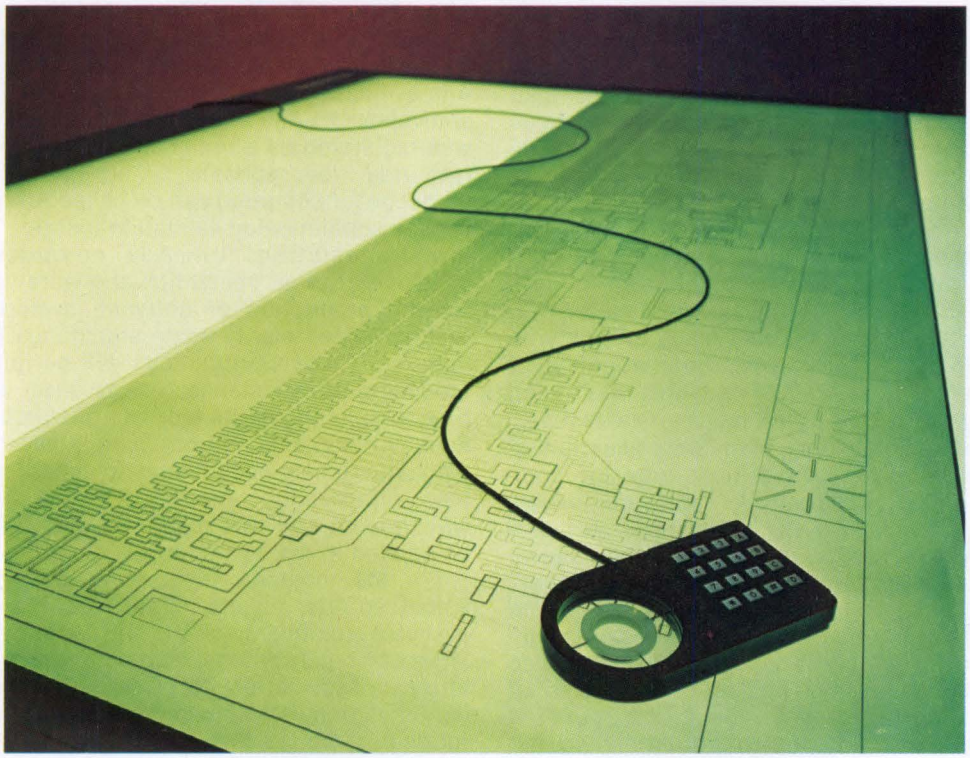

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CIRCLE 61

As mentioned, the most confusing aspect of abstraction is the notation. Fido and Spot have illustrated various object oriented concepts using a particular notation. That notation is the Ada programming language. Various programming and data structures are realized in terms of the objects and abstract classes in the Ada language.

The abstract objects in Ada are called Ada objects, and the abstract semantic classes in Ada are called Ada classes. Ada objects consist of constants and variables, procedures, packages, and tasks. Ada classes consist of types, generic subprograms, generic packages, and task types. These Ada objects and Ada classes were specifically developed to provide programmers with all the

The story behind Ada

By 1974, the U. S. Department of Defense (DoD) realized it had a software problem. The problem was not in the "number-crunching" domain, where FORTRAN was king; nor was it in the business or accounting domain where a language called COBOL (developed and standardized by the DoD) was omnipresent. The DoD's software problem was in "embedded" computer systems—systems that use a minicomputer or microprocessor as a small, but important, part of the whole. Programs for such systems were primarily written in machine or assembly language for a plethora of noncompatible computers. By 1975, the major cost of these embedded computer systems was in software, and those costs were increasing exponentially.

At the same time, it was realized that because of computer noncompatibility, the same computer programs were being rewritten. Transportability of computer programs, and programmers, was virtually nonexistent. The Army alone estimated that it used 58 different computers made by 29 manufacturers in 250 systems: these were programmed in 43 different languages. The wheel was being constantly reinvented at the taxpayer's expense.

To make matters worse, many were questioning the reliability of these assembly language computer programs. Reliability of software is very desirable (especially if the software is part of a weapon system). Software technology had shown that computer programs written in a "high order" language tended to be more reliable and easier to maintain than programs written in "lower order" machine or assembly languages. This was also reflected economically. The cost of newly created embedded software was about one hundred dollars per instruction; the cost of modifying that same instruction in an already implemented system approached several thousand dollars. Something had to be done.

In 1975, the High Order Language Working Group (HOLWG) was formed from DoD representatives with the goal of establishing a single high order language for new DoD embedded computer systems. It was felt that a single language would reduce noncompatibility and increase transportability of both computer programs and programmers. A high order language would reduce maintenance costs and increase reliability. Also, at that time no existing language satisfied the DoD's needs (but Pascal was a good start). A language was then designed from scratch. The technical requirements for the new language evolved in the Woodenman, Tinman, Ironman, and finally Steelman (1978) documents. An international competition was held to design what was called DoD-1 from the Steelman requirements. The semifinalists were color coded into red, yellow, blue, and green. Green won in 1979, after intensive review by 80 teams from industry, academia, NATO, and the DoD. DoD-1 was renamed Ada in honor of Ada Augusta (1815-1852), the programmer of the Babbage Analytical Engine.

In July 1980 the "proposed standard" *Ada Language Reference Manual* was published and distributed. Interest in Ada snowballed. The DoD formed the Ada Joint Program Office (AJPO) to coordinate Ada developments in December 1980. One of the first acts of the AJPO was to announce Ada as military standard (MIL-STD-1815) on the 165th anniversary of Ada Augusta's birth. The name Ada was registered as a trademark of the AJPO to protect Ada from subsets or supersets. No Ada language (or compiler) can be called Ada unless it passes sophisticated validation testing.

Many existing full Ada compilers were developed to test semantics and were not meant for the production of software systems. Such testing helped clarify some ambiguous language features. These clarifications will be reflected in the new reference manual (MIL-STD-1815A), which will be available soon. The lack of suitable compilers does not stop anyone from using Ada as a design language to help specify and document a system. Many organizations are finding that this is a good way to learn Ada. The results of this learning can be applied to real systems.

For the moment, the rest of the world has embraced Ada, despite the fact that there are few available compilers for the full language. Newsletters of organizations such as AdaTEC, a special interest Association for Computing Machinery (ACM) subgroup that has more corporate and institutional sponsors than any other ACM subgroup, demonstrate the tremendous interest in Ada.

Ada will not be required until full production compilers and software tools in the form of an Ada Program Support Environment (APSE) are available (*Computer Design,* Dec 1982, p 196). These Ada environments are necessary to support Ada programs throughout their software life cycles. This need was recognized by HOLWG; requirements for an APSE evolved (with the language) through Sandman, Pebbleman, and Stoneman (1980) documents. (The first APSE was released to the Army in late August 1982.) The AJPO is coordinating APSE developments in conjunction with a DoD team called the Kernel-APSE Interface Team (KIT) and an international team of 30 industry and academic consultants called the Kernel-APSE Interface Team Industry/Academia (KITIA). KIT and KITIA will ensure that the original goals of transportability and interoperability of Ada computer programs and programmers are met. The main beneficiaries of all this may actually be the taxpayers.

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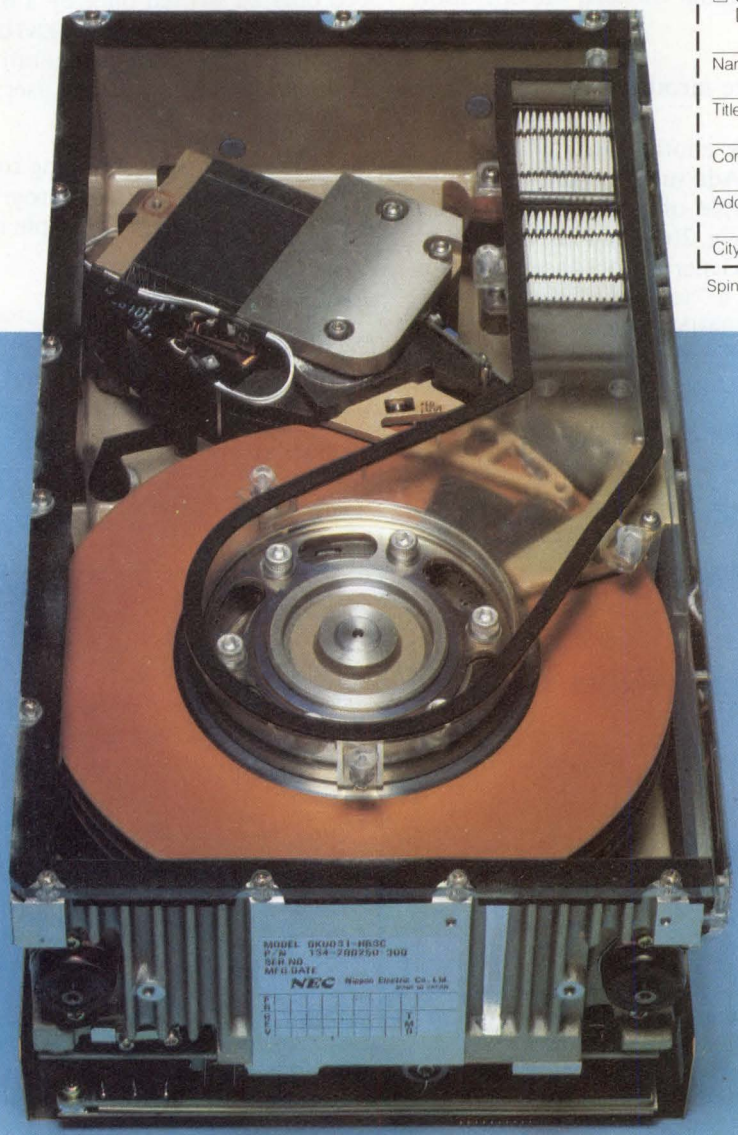

CIRCLE 62

```
--declaration
  type QUATERNION is array (1..4) of REAL;
  type VECTOR is array (1..4) of REAL;
  X, Y, Z: VECTOR;
  W, T   : QUATERNION
```

Fig 1 Method of specifying type in Ada language. Both VECTOR and QUATERNION are types of Ada objects, each subject to different allowable procedures.

benefits mentioned earlier. A detailed discussion of the semantics is found in Reference 6.

A standard example of the use of the Ada class type and its associated Ada object is seen in a specification of two abstract semantic classes (Fig 1). Objects of semantic class (type) VECTOR (objects X,Y,Z) have a certain set of implicit operations allowed to them. Similarly, objects of type QUATERNION do as well. However, while the operation

X:= Y;

is allowed since these are similar objects, the operation

W:= Y;

is not because W and Y are members of incompatible semantic classes.

The generic procedure is another Ada class whose objects (instantiations) are Ada subprograms (functions and procedures). An example of a generic procedure specification is shown in Fig 2(a), and its implementation is shown in Fig 2(b). Generic procedure SWITCH is an Ada class that describes a "template" for switching objects of (arbitrary) type THING whose only allowed operation is assignment (denoted by ":="). Objects of semantic class "generic procedure SWITCH" are defined as

procedure SWITCH_VECTOR is new SWITCH (VECTOR);
procedure SWITCH_COORD is new SWITCH (QUATERNION);

The Ada objects SWITCH_VECTOR and SWITCH_COORD are Ada procedures; SWITCH is not a procedure; it is a semantic class. These Ada objects can be used in the following way: if X = (1,2,3,4) and Y = (4,5,6,7), then after the call

SWITCH_VECTOR (X,Y);

the value of X is (4,5,6,7) and the value of Y is (1,2,3,4).

The Ada generic package is one of the Ada language's most powerful features. Much of Ada's input/output is defined in terms of Ada generic packages. An example of a generic procedure specification is shown in Fig 3. The Ada class specified by generic package BUSINESS is a software template for a business: a business buys and sells objects from an inventory. The actual implementation of the generic procedures BUY and SELL are separately provided in what is called the package body. Ada objects of this Ada class are specified as

package FRUIT_STAND is new BUSINESS (FRUIT);
package CAR_DEALER is new BUSINESS (CARS);

In these definitions, FRUIT and CAR belong to the Ada class of "enumeration types"; these are passed as arguments for the generic formal parameter type GOODS. These two Ada objects create two software packages for a fruitstand business and a car dealer: each of these packages can be used for its particular purposes, but the actual software implementation (the package body) need only be written once by a programmer. Note also that Ada objects of type INVENTORY in Fig 3 are private and thus protected. Implementation of INVENTORY may be hidden from the package user.

Bodies as objects

The Ada object corresponding to the Ada class of task types is used to describe program entities that may operate in parallel. An example of the declaration of a task type is

task type BOY;

The actual definition of what objects of semantic class BOY do is contained in the task body. A task body in Ada might look something like

task body BOY is
begin
--some actions
end BOY;

```
generic
     type THING is private;
procedure SWITCH (A,B: in out THING);
```

(a)

```
procedure SWITCH (A,B: in out THING) is
     C: THING;
begin
     C: = A; A:=B; B:=C;
end SWITCH:
```

(b)

Fig 2 Example of Ada generic procedures used in much of Ada's input/output operations. SWITCH is a generic procedure that exchanges the object THING. Specification for exchange is shown in (a), template for exchange in (b).

```
generic
     type GOODS is (<>);
package BUSINESS is
     type STORAGE is range 1..1000;
     type INVENTORY is private;
     procedure BUY (ITEM: GOODS; QUANTITY: STORAGE;
                    CURR_INV: in out INVENTORY);
     procedure SELL (ITEM: GOODS; QUANTITY: STORAGE:
                     CURR_INV: in out INVENTORY);

private
     type INVENTORY is array (GOODS) of STORAGE;
end BUSINESS;
```

Fig 3 Ada generic package specification. Generic package BUSINESS incorporates procedures BUY and SELL. Ada object INVENTORY is specified as private, limiting user access.

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CIRCLE 63

```
task body BOY is
      .
      .
      .
   GIRL.TALK (WITH=>ME);
      .
      .
      .
end BOY;
```

```
task body GIRL is
      .
      .
      .
  accept TALK (WITH: HIM) do
     -- do something in this rendezvous
  end TALK;
      .
      .
      .
end GIRL;
```

Fig 4 Rendezvous of Ada tasks accomplishing message passing. BOY task initiates communication with GIRL task. GIRL task has been specified to accept such communication at appropriate times.

Ada objects of Ada class BOY can be created in the following way:

```
GEORGE:BOY;
```

This task object creates one BOY object called GEORGE. Similarly,

```
CROWD:array (1..100) of BOY;
```

creates 100 BOY objects arrayed as a crowd. The following is used to dynamically create a BOY object:

```
type BOY_SPIRIT is access BOY;
JOHN:BOY_SPIRIT;
```

Dynamic allocation is accomplished by

```
JOHN: = new BOY;
```

All these Ada objects of Ada class BOY will operate in parallel with each other.

Ada tasks and task types can also be used for message sending (similar to Smalltalk). The message sending protocol in Ada in called a rendezvous. A simple example of this mechanism is shown in Fig 4. Here, parts of the task body for BOY and parts of another task body (from a task type GIRL) are shown. As in real life, BOY initiates a message to GIRL with the "entry call" to GIRL

```
GIRL.TALK(WITH =>ME);
```

If GIRL is not ready to accept his advance, BOY patiently waits. On the other hand, in the task body of GIRL is an "accept statement"

```
accept TALK(WITH:HIM) do
          .
          .
          .
end TALK;
```

If GIRL reaches this point (in the state of computation) before BOY issues his call, then GIRL must wait. If the BOY is calling and the GIRL is ready to accept the offer to TALK, then BOY and GIRL tasks have a rendezvous. In this denouement, both tasks now are synchronized and all action occurs in the "accept statement" of task body GIRL. For example, a message can now be passed. After the rendezvous (following the line "end TALK") both tasks split up once more to live independently.

These examples of object oriented Ada operations are presented with one intention: to illustrate the innate common sense implicit in object oriented languages. Such languages are simply not that hard to learn. Granted, the adoption of such languages by the programming community will involve changing the way some programmers solve problems. Remember, however, that object oriented languages are not impossibly complex or beyond the ken of most working software authors—including those comfortable in their use of COBOL and FORTRAN. In addition, the use of abstract objects belonging to an abstract semantic class has a long and familiar history in mathematics.

The various object oriented languages that have evolved over the years have developed their own idiomatic object and class structures for their own particular purposes. Ada programming structures exemplified by boys and girls and Fido and Spot provide a large set of object oriented features for a general purpose language. The most difficult aspect of using them is likely to be abandoning old programming habits in favor of common sense approaches to everyday coding dilemmas.

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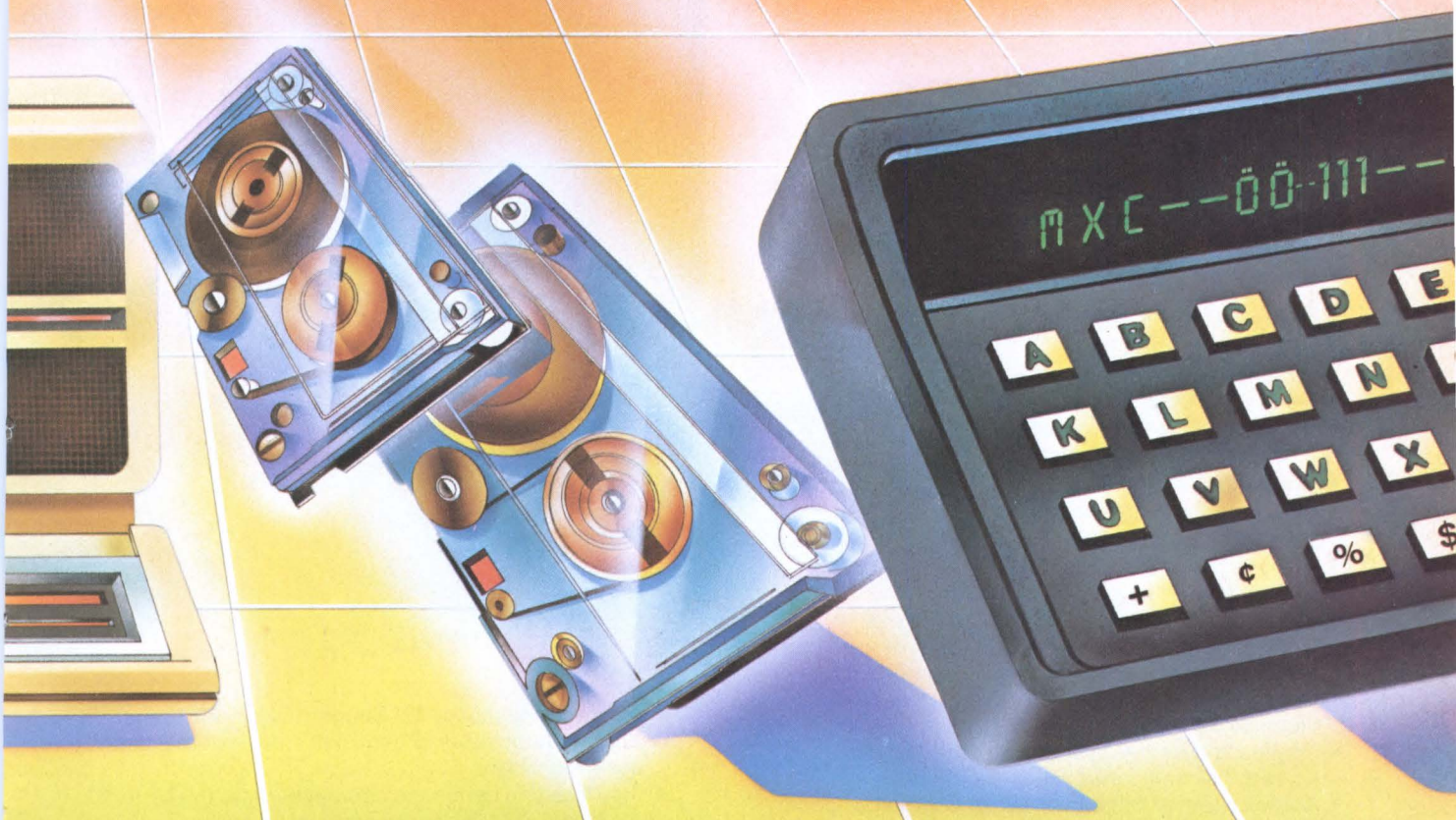

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I_{OH}/I_{OL}	.44/1.1mA	0.16/0.44mA	0.4/8.0mA	0.4/8.0mA
V_{CC} Range	2-8v	3-18v	4.75-5.25v	4.5-5.5v
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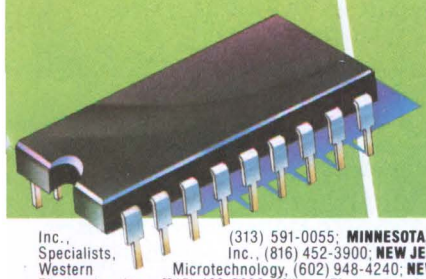

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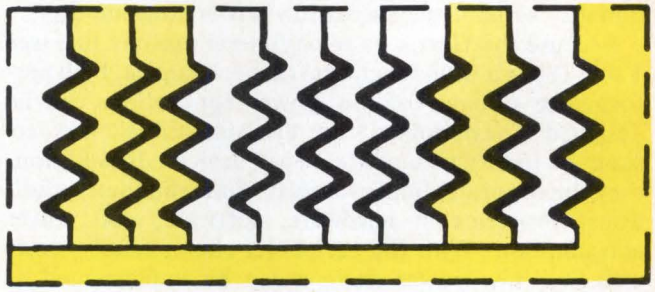
Today's complementary metal oxide semiconductor microprocessors have evolved in differing ways—some through direct hardware/software emulation of existing N-channel metal oxide semiconductor microprocessors, others by the merging of several architectures and instruction sets. In both cases, performance improvement and low power operation result.

In order to take advantage of these microprocessor advancements, logic and memory also had to improve. For example, an entire second generation of high speed small scale integration/medium scale integration (SSI/MSI) logic appeared in the 74HCXX/74SCXX products. These logic devices offered low power Schottky transistor-transistor logic (LS/TTL) equivalent propagation delays at complementary metal oxide semiconductor (CMOS) operating power levels and provided the necessary high speed "glue" for advanced CMOS microprocessor systems.

Similarly, higher density CMOS memories are now available at much greater speeds. Functional options include both synchronous and asynchronous memory operation to meet specific system requirements. Synchronous 16k CMOS random access memories (RAMs), for example, have a guaranteed operating current of 10 mA/MHz maximum for low power or battery operated systems. In addition, asynchronous 16k CMOS RAMs, with the same configuration, have access times as low as 70 ns.



CMOS nonvolatile memory support is available with both erasable programmable read only memory (EPROM) and fuse link programmable read only memories (PROMs). CMOS PROMs offer the greatest benefits in nonvolatile applications where low power and reliable data retention are critical. Present CMOS fuse link PROMs store data in programmed polysilicon fuses. Fuse link technology yields permanent, stable storage characteristics for the life of the device. Polysilicon fuses, combined with the low power of CMOS, provide an excellent alternative to EPROMs or bipolar PROMs for battery operated and other low power systems.

For high performance, low power 2716-type memory applications, 16k CMOS synchronous fuse link PROMs

Walter J. Niewierski is a technical marketing engineer at Harris Corp, Semiconductor CMOS Digital Products Div, Melbourne, FL 32901, where he is responsible for technical support of CMOS digital products. Mr Niewierski has a BSEE from the University of Michigan.

TABLE 1

CMOS 80C86 Family Peripheral Support Chips

Part	CMOS device type/function	Comments
82C82	octal latch	T_{PD} = 35 ns max at C_L = 300 pf
82C84A	clock generator/driver	8-MHz system clock frequency
82C88	bus controller	Status decode function
82C54	programmable interval timer	10-MHz count frequency
82C55A	programmable peripheral interface	Control word read capability
82C59A	priority interrupt controller	8 user defined priority interrupt requests

provide a low 13-mA/MHz operating current with 175-ns access times. Moreover, performance upgrades to 125-ns access times will soon be possible. In nonvolatile memory, CMOS has a significant speed advantage over N-channel MOS (NMOS), while showing a large power reduction.

Improving peripheral support

Although sophisticated CMOS microprocessors have brought high performance to low power designs, they cannot reach their full potential without equally high performance, low power consumption support chips. For the most part, CMOS peripheral circuit design efforts have lagged. This has limited the development of systems attempting to use CMOS devices exclusively. A new family of microprocessor peripheral circuits fills this void by providing increased performance and functionality without sacrificing low power consumption.

Because the Harris 80C86 peripheral product line (see Table 1) has a wide functional range, complex, high performance systems for low power applications can be designed. The peripherals are TTL compatible CMOS versions of industry standard NMOS devices. In addition, they incorporate improvements that eliminate traditional problems in hardware, software, and power consumption. With the peripheral circuit family, cost-effective, low power designs can be implemented at superior performance levels.

Drop-in replacements for their NMOS equivalents (see Table 2), the 80C86 peripheral family offers equal or greater performance. The peripheral family's architecture is fully compatible with 80C85- and 80C86-type microprocessors. However, the popular 2-line control method for data movement, using read (RD) and write (WR) lines, allows interface to almost any recent generation microprocessor.

In addition, consistent family specifications make system design easier. All peripheral product ac and dc specifications are guaranteed over the industrial (−40 °C to 85 °C) or military (−55 °C to 125 °C) temperature range and 5-V ±10% voltage range. Timing specifications for peripheral circuits allow full speed operation with a CMOS 80C86 central processing unit (CPU) at 5 MHz, with no wait states.

Dual specifications for the logical 1 output voltage (VOH) ensure interface compatibility of the peripherals with both CMOS and TTL devices. Even in an all-CMOS design, there may be the need for circuit functions available only in NMOS or bipolar. In this case, the peripherals allow direct interface without pullup resistors or additional buffers. For future system enhancements with circuits of other technologies, the retrofit problems that occur with non-TTL compatible devices are eliminated.

Several techniques used to design the peripherals improve CMOS's natural low power operation. During normal system operation, bus signals at the latch inputs can exhibit high impedance or make transitions unrelated to latch operation. These voltage transitions cause an increase in power dissipation due to the low resistance path between V_{CC} and ground created when the input circuitry switches.

In Harris' 82C82 octal latching bus driver, gated inputs eliminate input switching current transients by turning off the inputs when data are latched (strobe pin = low). See Fig 1. The strobe pin (STB) disconnects the input inverter from the power supply by turning off the upper P-channel (Q1) and lower N-channel (Q2). No current flow from V_{CC} to ground occurs during input transitions. Invalid logic states from floating inputs are not transmitted to succeeding circuitry, thereby eliminating the need for pullup resistors.

Steering clear of high current conditions

Bus-hold circuitry used on specific pins avoids high current conditions caused by floating inputs to CMOS devices. These circuits maintain a valid logic state when

TABLE 2

Peripheral Interface Compatibility

	Logical 1 Input voltage (VIH)	Logical 0 Input voltage (VIL)	Logical 1 Output voltage (VOH)	Logical 1 Output current (IOH)	Logical 0 Output voltage (VOL)	Logical 0 Output current (IOL)
80C86 Peripherals	2.0 V/2.2 V Ind/Mil	0.8 V	3.0 V V_{CC} − 0.4 V	−2.5 mA −100 μA	0.4 V	2.5 mA
NMOS 8086 Family	2.0 V	0.8 V	2.4 V	−400 μA	0.45 V	2.5 mA
CMOS	70% V_{CC}	30% V_{CC}	V_{CC} − 0.5 V	−10 μA	0.4 V	2.0 mA
LS/TTL	2.0 V	0.8 V	2.5 V 2.7 V	−400 μA −400 μA	0.4 V 0.5 V	4.0 mA − Military 8.0 mA − Commercial

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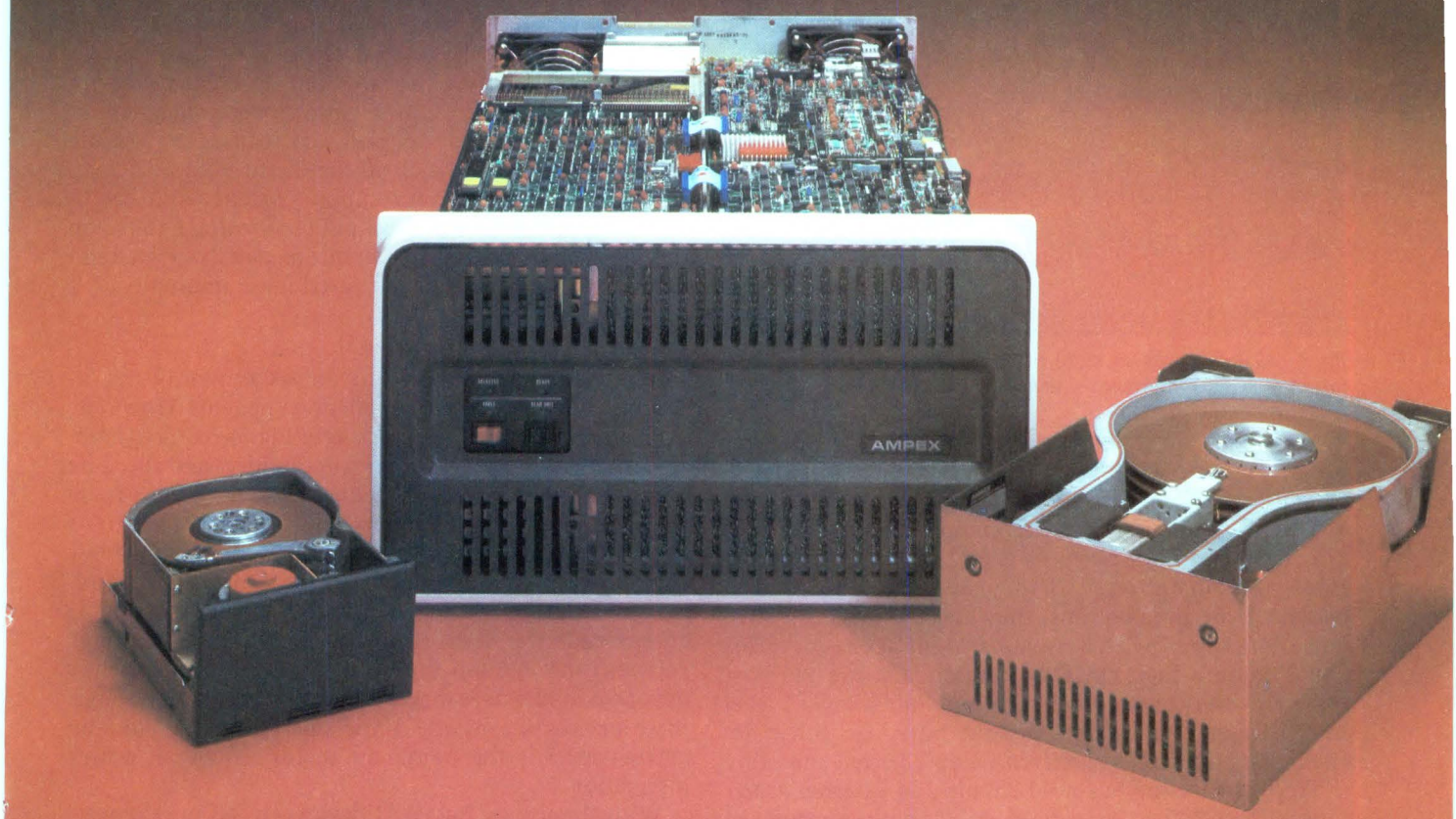

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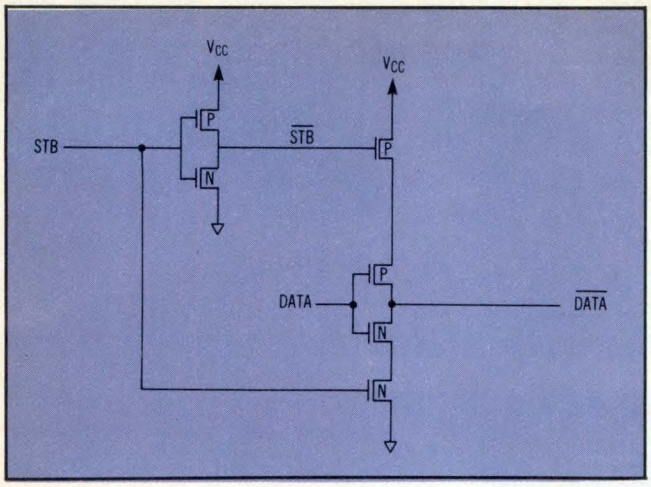

Fig 1 Gated inputs of 82C82 octal latching bus drivers. Such internal circuitry eliminates need for external pullup resistors.

no driving source is present (ie, an unconnected pin or a driving input that goes to a high impedance state). In the 82C55A programmable peripheral interface (PPI), all port pins have bus-hold circuitry (Fig 2). Port pins are defined as inputs at reset. If they are either open or will eventually become outputs, they have no driving source and are floating. With normal CMOS input circuitry, this could cause a high current situation. On the PPI port pins, however, bus-hold circuits maintain a logic 1 level internally and externally until the ports are either defined as outputs or overdriven by an external source.

To overdrive the bus-hold circuits, an external driver must supply 300-μA minimum sink or source current at valid input voltage levels. Since this bus-hold circuitry is active and not a resistive-type element, the associated power supply current is negligible. The PPI standby current specification is 10 μA maximum.

All 80C86 peripheral family devices are designed with fully static circuitry. This allows the devices to be operated from dc to their individual maximum rated frequencies. Since operating power is critical in low power applications, the user can control this parameter,

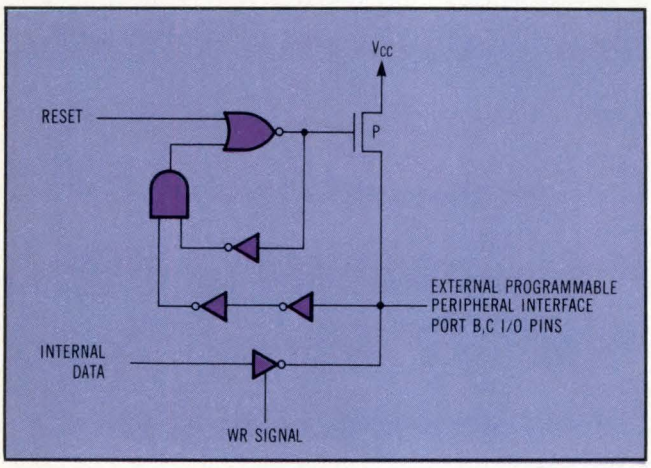

Fig 2 Bus-hold circuitry used on the 82C55A programmable peripheral interface CMOS peripheral. Logic 1 level is maintained internally on undefined port pins to keep power consumption to a minimum.

based on system operating frequencies. CMOS operating power is directly related to frequency; the lower the frequency, the lower the operating power dissipation. At a dc frequency, device standby currents are typically less than 10 μA.

Where voltage is concerned, the peripheral family maximum input voltage limit (ground $-$ 2.0 V $\leq V_{IN} \leq$ 6.5 V) essentially eliminates the problem of device latch-up. Latch-up results from an overvoltage condition on the inputs or outputs that causes a parasitic silicon controlled rectifier on the die to become active. This creates a high power supply current (ICC) condition. The increased input/output (I/O) voltage range on the peripherals offers greater protection from system-induced noise, as well as increased noise immunity.

Expanding parallel ports

Adding parallel I/O ports to an 80C48 family microcomputer using a PPI is well documented. However, designing this system in CMOS (see Fig 3) requires additional attention to the port reset condition and the state of unused port inputs. The CMOS PPI eliminates these concerns and, in conjunction with a unique feature of the 82C82 octal latch, keeps power dissipation low enough for battery operation. An extremely low standby power supply current of 10 μA maximum is guaranteed over the full operating temperature range for both the PPI and the octal latch. This is especially desirable in idle or low power modes of operation. Since these devices see mostly static operation, the standby current level is the dominant factor in overall power dissipation.

With the use of bus-hold devices on all port inputs, the PPI eliminates the need for pullup resistors to prevent undefined signal states. Upon being reset, all port (A, B, and C) pins are pulled high by internal bus-hold devices instead of the standard NMOS PPI procedure of putting all port pins into the high impedance state. The bus-hold devices also provide valid logic levels to CMOS inputs connected to the port pins prior to port initialization. Shaded areas in Fig 3 indicate where pullup resistors, normally needed for CMOS systems, are eliminated.

A low level external drive input (I_O = 300 μA) can overcome the bus-hold function. If the port input is unused, the bus-hold device maintains a high logic level and provides a valid logic input to the port pin. Since the bus-hold device is an active component on the chip and the PPI standby current is specified as 10 μA maximum, dc standby current is decreased by a factor of 1000 from the levels seen with pullup resistors.

Functional update is simplified by a readable control word on the PPI. Status of this device can be obtained by a control-word read operation. Data are transferred from the PPI control register, eliminating the need to store port configurations in system memory or internal registers.

Used in this application for address/data bus demultiplexing, the octal latch keeps power at a minimum with a specialized input circuit design. Gated inputs on the octal latch prohibit the passing of invalid input states to octal latch internal circuitry during the time data are latched. This prevents undefined logic states and high current transients due to input switching.

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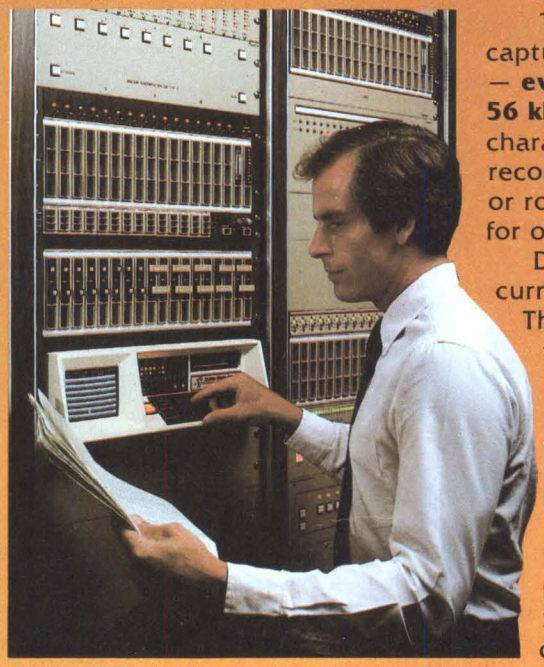

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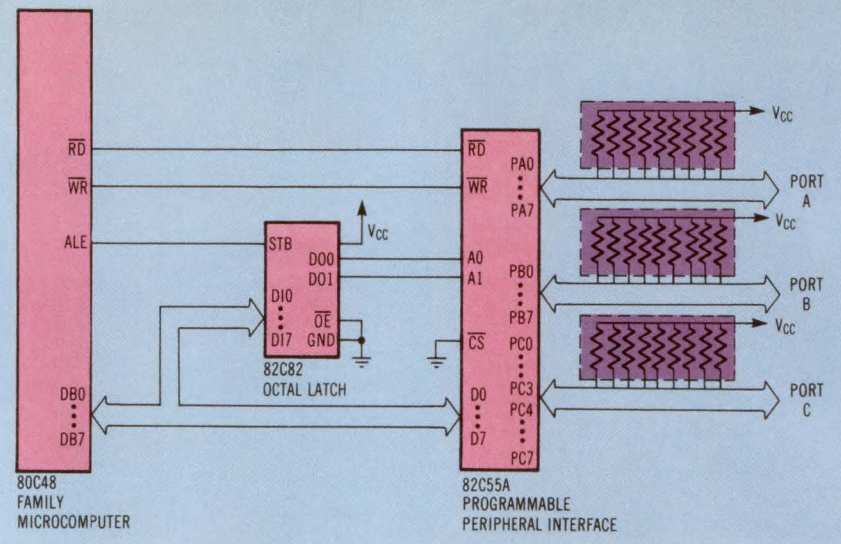

Fig 3 Parallel I/O port expansion with CMOS peripheral low power consumption and elimination of external pullup resistors (shaded areas) are benefits of CMOS techniques.

Waking up the processor

One of the most appealing features in many CMOS microprocessors is the interrupt wake-up from power-down mode. In this operation, the CPU is brought back from a low power idle mode by an external interrupt. Typically, simple interrupt schemes must be implemented since only a single external interrupt is available at the processor itself. With the 82C59A CMOS priority interrupt controller (PIC), eight separate interrupting sources can wake up the processor on a priority basis. For complex systems, 64 interrupts can be serviced via the cascaded connection of up to eight PICs.

Fig 4 shows how the PIC accommodates several interrupts in a single-chip CMOS microcomputer system. Addressing for the 82C59A PIC takes a 2-level approach—standard read/write operations and interrupt vector transfer. Since there is no interrupt acknowledge (INTA) signal available from the processor (this line is needed to transfer the interrupt vector information from the PIC), the necessary decoding for these two sets of operations must be handled elsewhere. A single HD-6440 CMOS line decoder and one 74HC00 quad 2-input NAND gate will do the job. A single bit from port B (PB1) is used to gate the microcomputer RD signal to the 82C59A PIC RD input for standard data transfers (PB1 = logic 0), or to the INTA input for vector information (PB1 = logic 1).

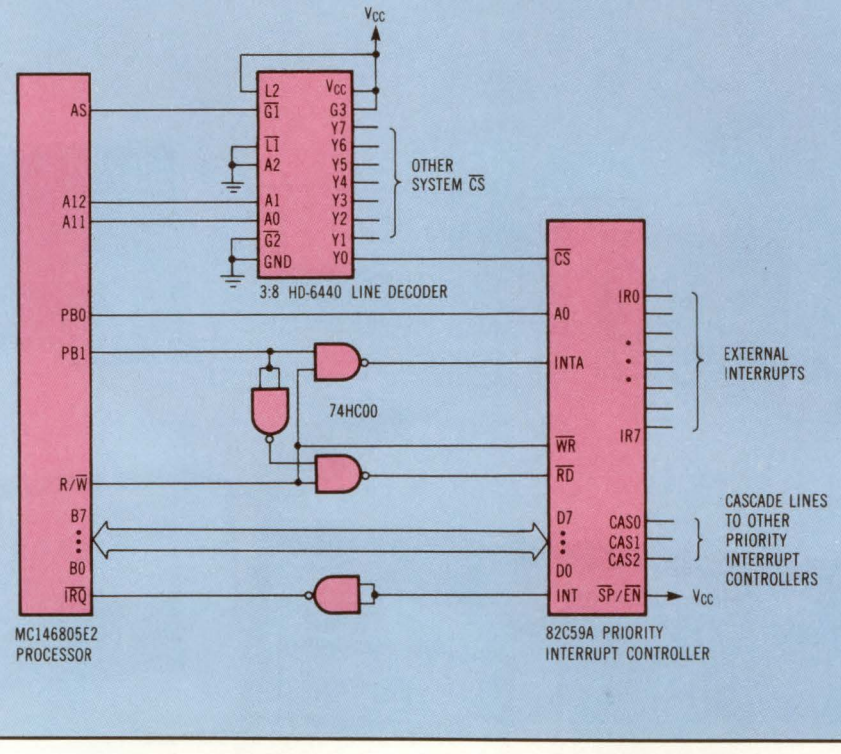

Fig 4 Multiple interrupt handling in priority interrupt controller CMOS chip. Up to eight levels of interrupts are possible, with a single 82C59A priority interrupt controller.

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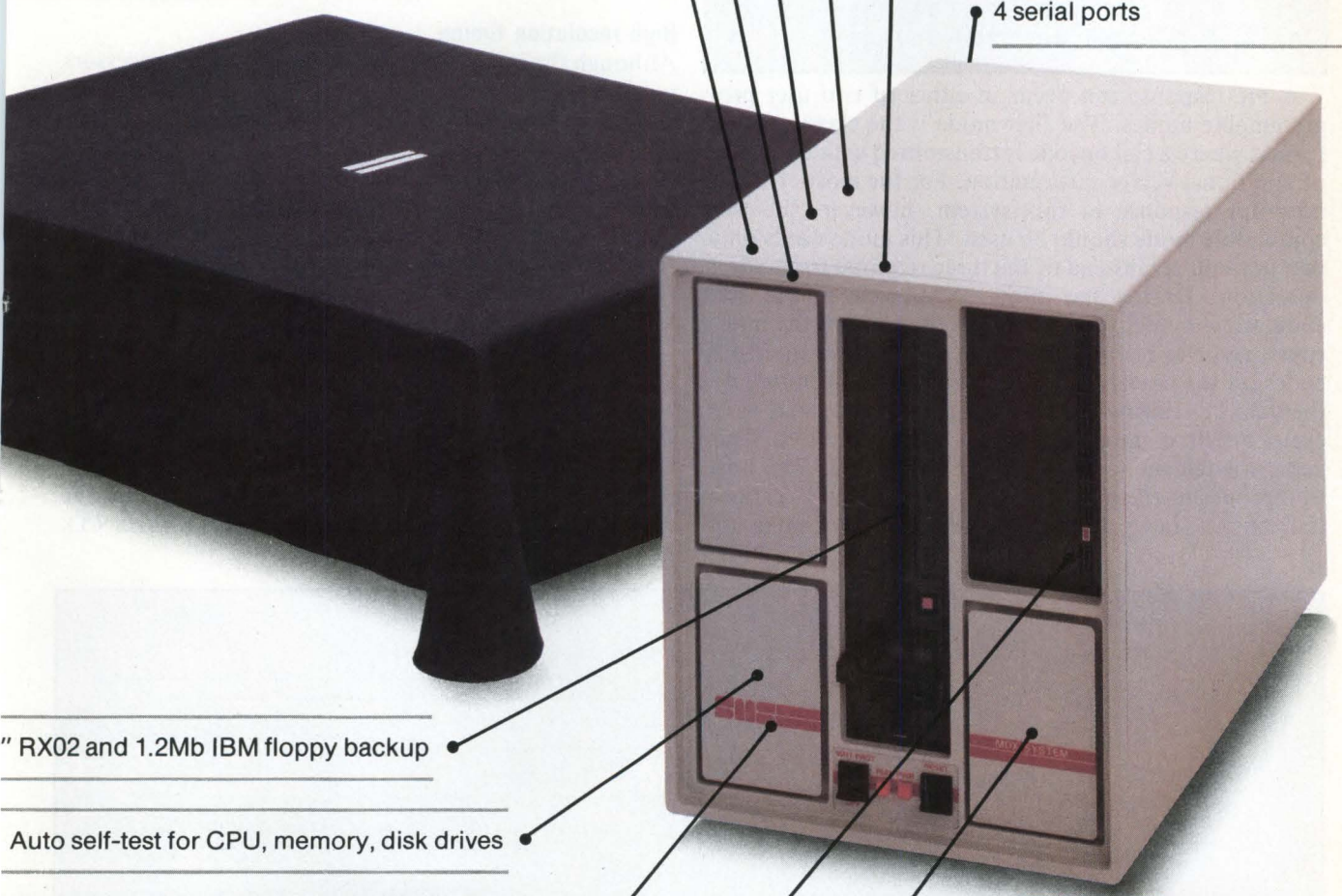

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TABLE 3

Priority Interrupt Controller Chip Interrupts

Interrupt Request Inputs	Interrupt Bit Assignments							
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

A PIC response can occur in either of two user programmable modes. The first mode is the classic 8080/85 format where a call opcode is transmitted with two bytes of additional vector information. For the most efficient interrupt response in this system, however, the 8086 compatible mode should be used. This mode needs only two INTA pulses instead of the three required for mode 1 operation. During the initial INTA cycle in the 8086 compatible mode, the PIC freezes the state of the interrupts, resolves priority, and issues the master interrupt codes on the cascade lines. No data are transmitted on the data bus during the first cycle. On the second INTA cycle, a byte of interrupt code is sent to the CPU. This acknowledgment byte is defined in Table 3. The host CPU programs the upper five bits (D3 through D7) at initialization. They provide the base address for interrupt vectoring. The lower three bits (D0 through D2) provide the offset based on the interrupting source.

INTA signals are generated by decoding specific addresses' output during load accumulator (LDA) instructions. The vector information transferred during the last INTA cycle can be used in an interrupt service routine using an indexed jump to locate the specific service program.

The timing diagram in Fig 5 shows a 146805 microcomputer's response to a wake-up interrupt, along with the necessary INTA generation and vector information retrieval from the PIC. The ability to wake up an idle CMOS microcomputer with any of several interrupting sources greatly increases single-chip system flexibility.

High resolution timing

Although the increased speeds of CMOS microprocessors meet the timing requirements of many applications, some demand a more precise reflection of time. In these situations, the 82C54 CMOS programmable interval timer (PIT) provides high frequency count capability while the 82C84A CMOS clock generator/driver (CGD) delivers, from a single input frequency, both a high frequency timer input and a lower frequency CPU clock. High resolution timing is thus accomplished with relatively low system clock frequencies.

In the system depicted in Fig 6, an 8-MHz timer frequency is used with a 4-MHz CPU clock. The CGD generates three output signals: OSC is the crystal frequency; CLK is the crystal frequency divided by three; and PCLK is the clock frequency divided by two. A 24-MHz parallel resonant, fundamental mode, AT cut crystal on the CGD results in a 24-MHz OSC frequency, 8-MHz CLK

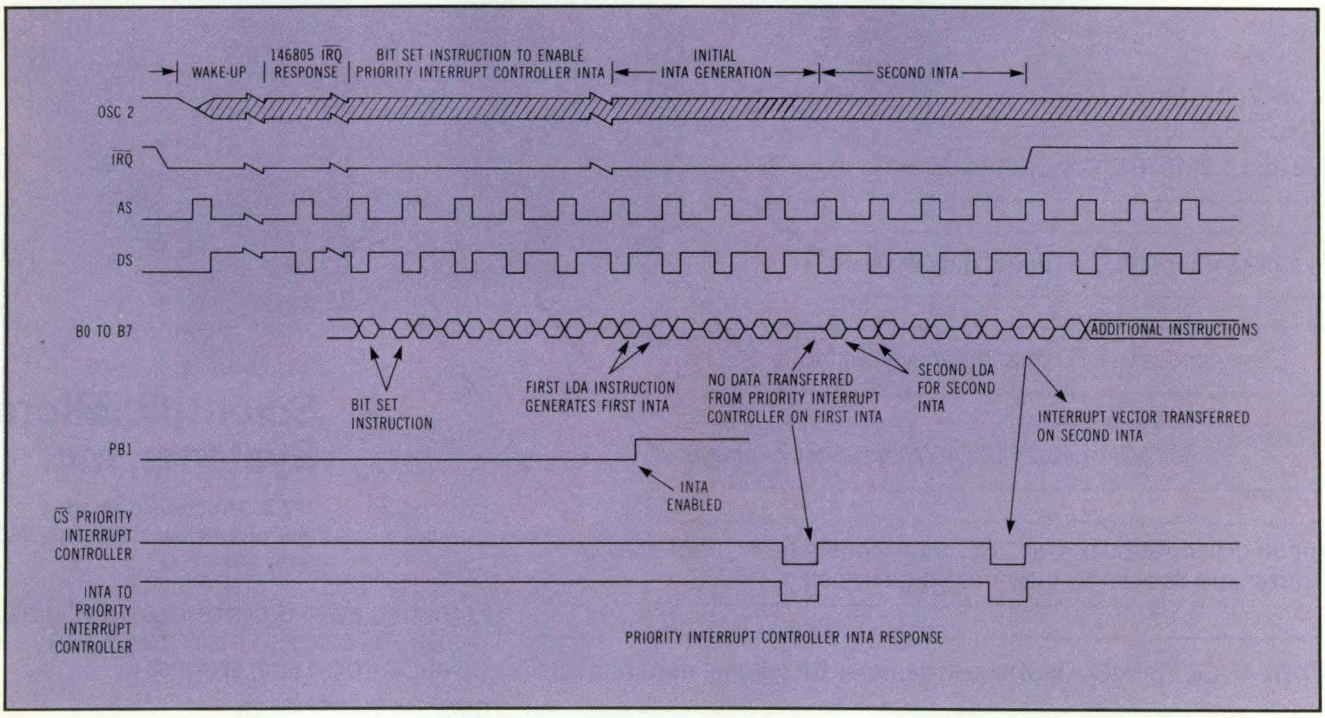

Fig 5 Timing diagram of microprocessor response to a wake-up interrupt. Any of several interrupts can initiate the wake-up response.

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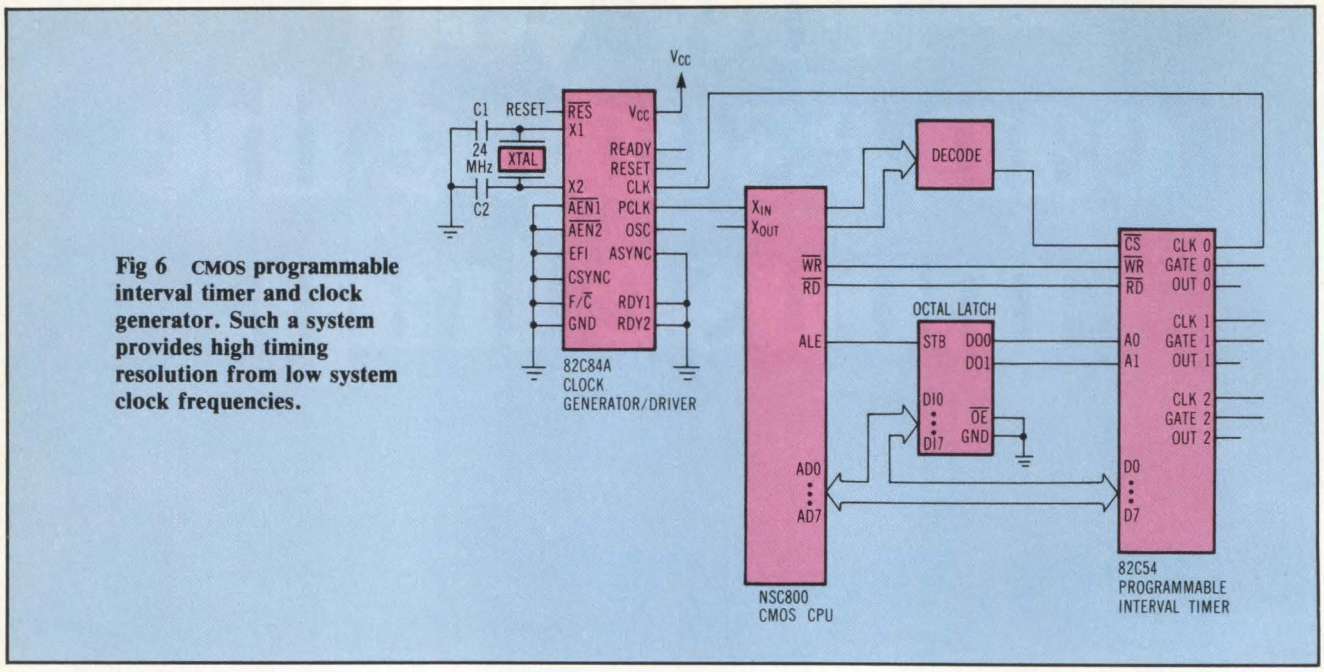

Fig 6 CMOS programmable interval timer and clock generator. Such a system provides high timing resolution from low system clock frequencies.

frequency, and 4-MHz PCLK frequency. The system thus has an 8-MHz count frequency and 2-MHz NSC800 operation. If an upgrade to 4-MHz operation is desired, the 8-MHz CLK output from the PIT can clock both the processor and the PIT. The guaranteed maximum count frequency for the PIT is 10 MHz minimum. The 8-MHz output from the CGD meets the minimum pulse width requirements for the PIT clock input. This high count frequency allows resolution of time increments down to 125 ns, even with processor T-state periods of 500 ns.

Two software features—a readable status word and realtime count indication—allow full 82C54 PIT control in high frequency applications. The status-word read capability enables the processor to get an accurate indication of device status and reconfigures the counter when necessary. For accurate realtime count readings, the PIT can be read while still incrementing. When a read count operation is initiated, the current count is held in a count register until the read is completed. The count register is then updated to the new elapsed count status. If lower system operating power is desired, or if a slower CPU speed is needed, the 82C84A CGD base frequency can be reduced. Since CMOS operating power is directly related to frequency, both CGD and PIT operating power will be lower at these reduced frequencies.

The advent of a diverse group of CMOS peripheral chips heralds a new era in system design. Applications demanding low power consumption, high performance, and portability can now be served by an entirely CMOS oriented approach. Broadening CMOS applications into areas hitherto restricted to the realm of other technologies will allow designers more flexibility in creating tomorrow's systems.

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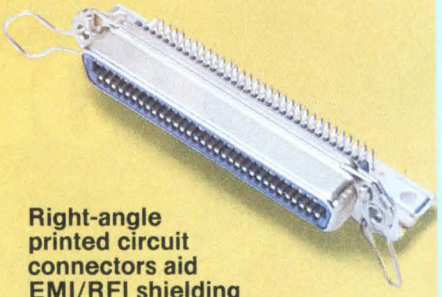

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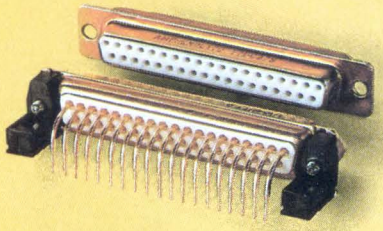

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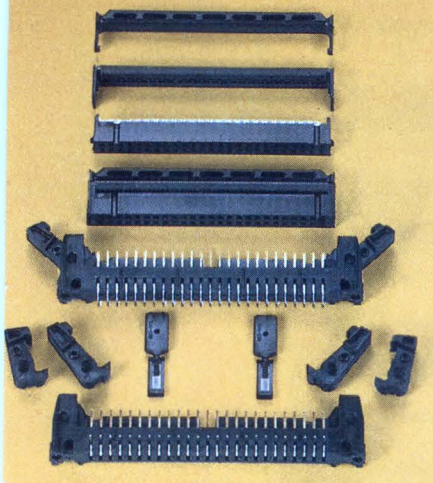

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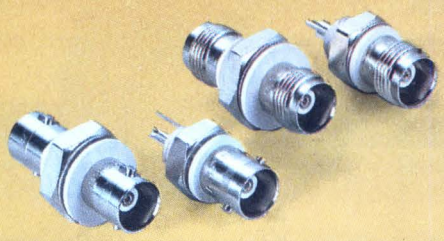

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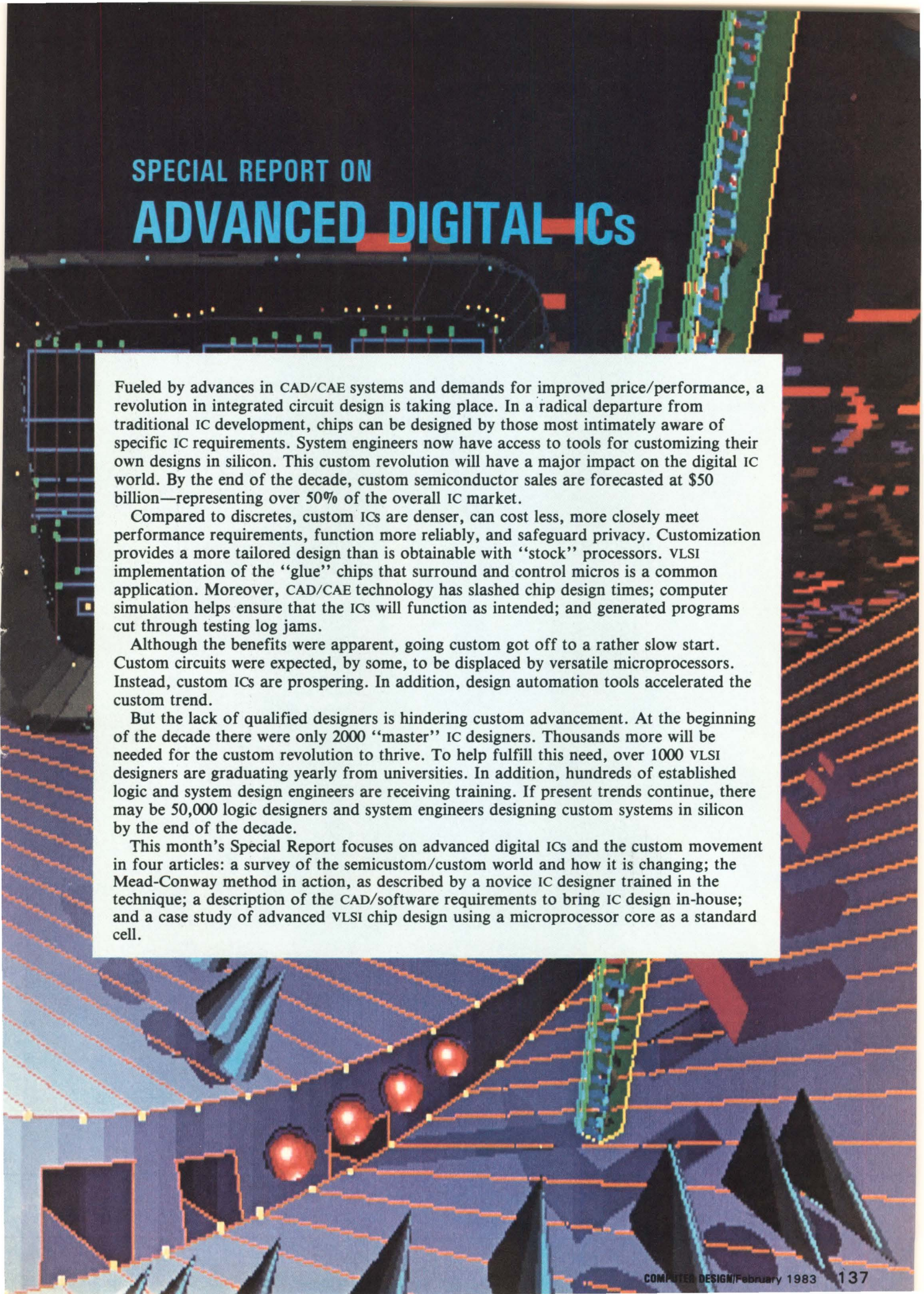


SPECIAL REPORT ON

ADVANCED DIGITAL ICs

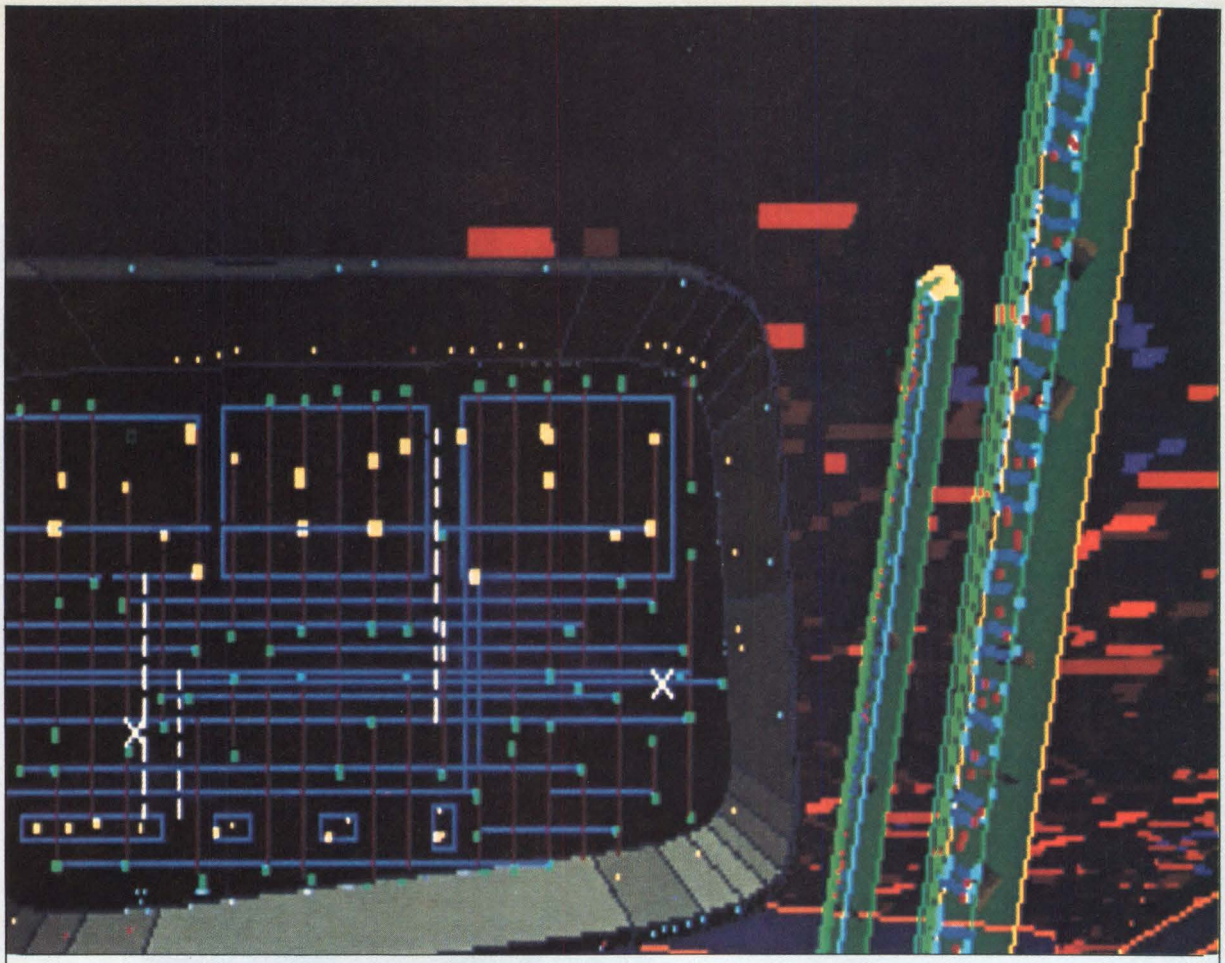
Fueled by advances in CAD/CAE systems and demands for improved price/performance, a revolution in integrated circuit design is taking place. In a radical departure from traditional IC development, chips can be designed by those most intimately aware of specific IC requirements. System engineers now have access to tools for customizing their own designs in silicon. This custom revolution will have a major impact on the digital IC world. By the end of the decade, custom semiconductor sales are forecasted at $50 billion—representing over 50% of the overall IC market.

Compared to discretes, custom ICs are denser, can cost less, more closely meet performance requirements, function more reliably, and safeguard privacy. Customization provides a more tailored design than is obtainable with "stock" processors. VLSI implementation of the "glue" chips that surround and control micros is a common application. Moreover, CAD/CAE technology has slashed chip design times; computer simulation helps ensure that the ICs will function as intended; and generated programs cut through testing log jams.

Although the benefits were apparent, going custom got off to a rather slow start. Custom circuits were expected, by some, to be displaced by versatile microprocessors. Instead, custom ICs are prospering. In addition, design automation tools accelerated the custom trend.

But the lack of qualified designers is hindering custom advancement. At the beginning of the decade there were only 2000 "master" IC designers. Thousands more will be needed for the custom revolution to thrive. To help fulfill this need, over 1000 VLSI designers are graduating yearly from universities. In addition, hundreds of established logic and system design engineers are receiving training. If present trends continue, there may be 50,000 logic designers and system engineers designing custom systems in silicon by the end of the decade.

This month's Special Report focuses on advanced digital ICs and the custom movement in four articles: a survey of the semicustom/custom world and how it is changing; the Mead-Conway method in action, as described by a novice IC designer trained in the technique; a description of the CAD/software requirements to bring IC design in-house; and a case study of advanced VLSI chip design using a microprocessor core as a standard cell.



Special report on advanced digital ICs

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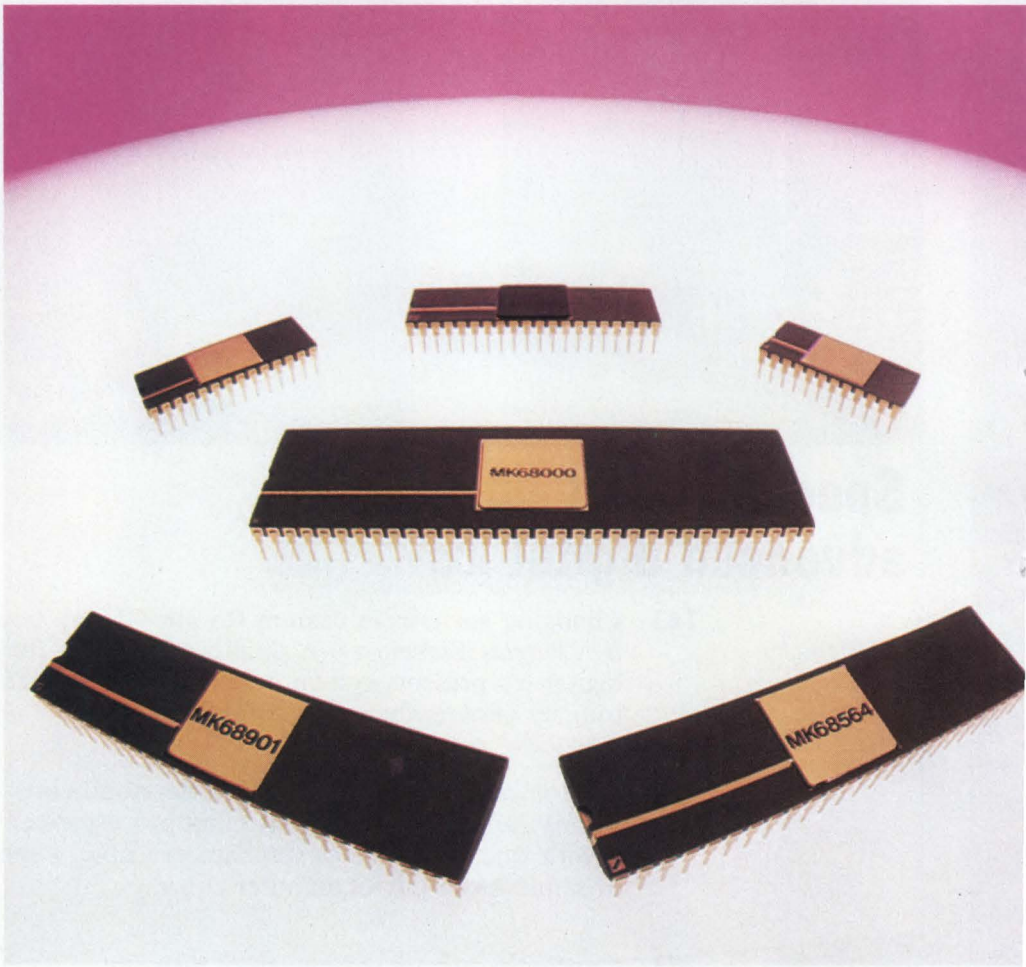

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CIRCLE 82

CHANGING PATTERNS IN CUSTOM ICs ALTER DESIGN BOUNDARIES

A wealth of schemes for customizing digital ICs presents system designers with greater freedom but tougher choices than ever before.

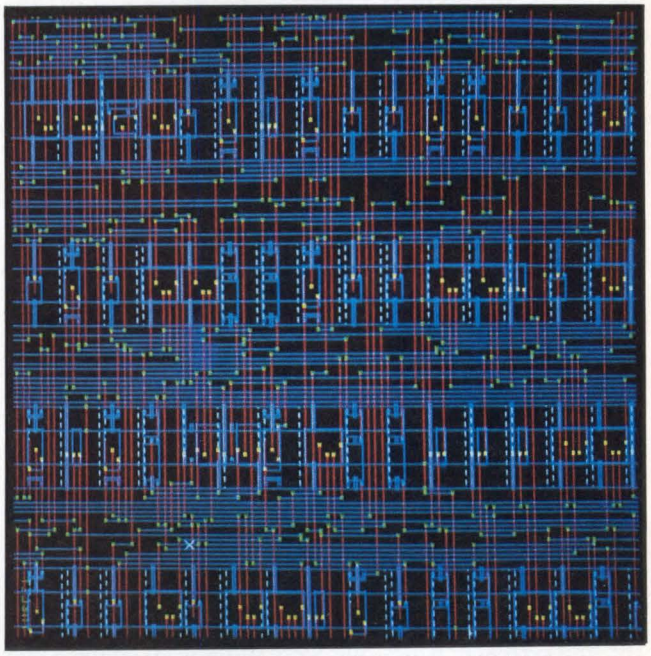
by Douglas Eidsmore, Senior Editor

Volatile and dynamic, the custom and semicustom integrated circuit market is shaking up some hitherto steadfast relationships in technology. Some people expected custom circuits to vanish from the scene with the advent of microprocessors and the versatility they brought to system design. Instead, custom integrated circuits are flourishing because of microprocessor technology. By the end of this decade, custom circuits may account for as much as fifty percent of the semiconductor business. Moreover, long-held axioms regarding custom circuit applications are fast becoming obsolete as designers find that each approach has merit. And more important, the different approaches are no longer mutually exclusive.

Tailoring to fit the need

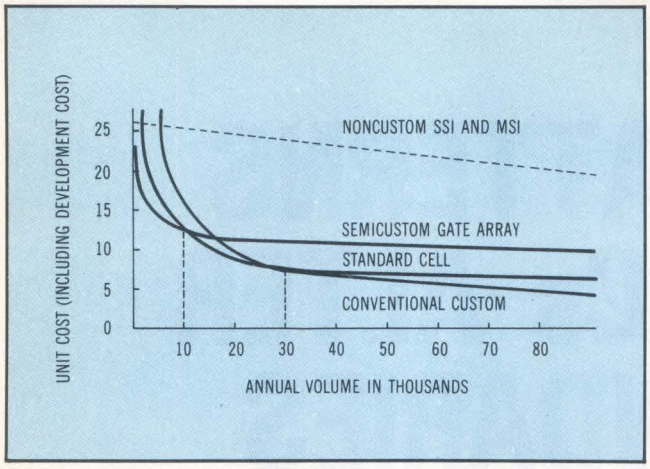
The various techniques for customizing ICs can be divided into semicustom and custom solutions. Gate arrays and fuse programmable devices are usually regarded as semicustom devices because the degree to which they can be customized is restricted.

A gate array is a matrix of predefined and preprocessed logical gate circuits on a silicon chip. Because the circuitry is already onchip, users must design within its size and organizational limits. The individual gate circuits are variously connected by one or more metal layers to obtain integrated circuits (ICs) with unique characteristics. By maintaining an inventory of preprocessed wafers, manufacturers can offer system designers a shortcut to a custom IC. Gate arrays cost $5000 to $25,000 and take a few months to develop, but they use silicon inefficiently and, in general, are relegated to applications requiring a total of under 100,000 parts for the entire production run.



The LSI5600 from LSI Logic Corp (Milpitas, Calif) is a 6000-gate array based on 3-micron, silicon gate, CMOS technology with 2-layer metal. Blue lines represent the first metallization layer; red lines the second. The small green squares are interconnection points (vias) between the first and second metal layers.

More confining than gate arrays, fuse programmable array logic ICs are completely processed and packaged ICs, with a limited number of gates. They are customized by blowing internal fuses using an off-the-shelf programmable read only memory programmer—a fine procedure for quick turnaround, but a severe constraint on volume. Programmable array logic ICs are presently limited to 250 gates and Schottky transistor-transistor logic (TTL) technology. Emitter-coupled logic (ECL) and complementary metal oxide semiconductor (CMOS)



Cost vs volume for custom alternatives from American Microsystems, Inc. Production volume is one factor influencing selection of a custom solution. Figures are based on a 1000-gate CMOS device, with development costs of $20,000 for gate array; $40,000 for standard cell; and $70,000 for conventional custom solutions.

devices with 5000 gates are being developed, which will add to the utility of the technology. Purchased off the shelf, fuse programmable devices are useful for very low quantities and limited to relatively simple functions.

Truly custom solutions consist of standard cell based or full custom ICs. Standard cells take four to six months to be completely processed and cost $30,000 to $50,000 to develop, but they use silicon more efficiently than gate arrays. Full custom circuits are for high volume and high performance, but may take as long as 18 months to develop at a cost of perhaps $50,000 to $300,000. However, they use silicon sparingly and will therefore save money in the long run.

These figures must be viewed in light of cost/volume relationships. At first glance, development costs appear to be considerably higher moving from gate arrays to standard cells and full custom. However, when the cost/volume relationship is examined, it becomes clear that each approach has merit within particular volume and timing constraints.

Moreover, the parameters of custom fabrication are still in flux due to the continuing changes in design and processing technology and the shifting requirements of the marketplace. Rules that were thought to be hard and fast may soon be broken. For example, some companies are finding that it makes sense to use gate arrays in very high volumes. Also, with the growth in complexity and flexibility of standard cells and their use in full custom designs, separating standard cells from the full custom approach may soon be just a semantic exercise.

Gate arrays—out of and in style

The earliest gate arrays were developed by Texas Instruments Inc (Dallas, Tex) and used by the company to pioneer its small calculators. Similar arrays were also offered to system integrators for quick turnaround. However, lines such as Fairchild Semiconductor's (Mountain View, Calif) Micro Mosaic were too costly and, in those pre-computer aided design (CAD) days, layout was too complex for them to be an attractive alternative to standard parts. As a result, arrays temporarily vanished from the marketplace. However, array development did not halt—it continued at system houses with captive semiconductor manufacturing facilities. By the mid-1970s this development began to pay off. When IBM Corp (Armonk, NY) introduced its 4300 series computers based heavily on gate arrays, the technology regained respectability.

Traditionally, gate arrays were the designer's choice for fast turnaround and low volume. This still makes sense for many applications. Even though standard cells have cut the development time for a custom circuit, preprocessing and inventorying of blank wafers still give gate arrays an edge in turnaround time. In the past, the excessive cost of silicon for high volume applications made gate arrays less cost-effective than standard cell based or full custom design. But now gate arrays are being used in extremely high volume applications.

The Sinclair ZX81 personal computer is a prime example. Over a million Sinclair small computers (now marketed in the United States as the Timex Sinclair TS 1000 by Timex Corp, Waterbury, Conn) were manufactured last year. The computer owes its small size to four gate arrays. One reason why gate arrays are used instead of full custom chips for such large volumes is that gate arrays allow for flexible featuring. Moreover, the product can more easily adapt to changes in the marketplace. As timing is paramount in such a competitive industry, gate arrays allow the design to be implemented in a hurry and glitches to be fixed quickly. In addition, gate arrays provide propriety and performance benefits associated with custom circuitry.

This example is not an anomaly. Interdesign Inc (Scotts Valley, Calif) has delivered three million linear gate arrays of a single type to an automobile manufacturer. In addition, International Microcircuits Inc (Santa Clara, Calif) claims it produces several unique arrays in quantities of over one million per year.

CAD systems such as VLSI Technology's integrated design system are the driving force behind growth in custom circuit design. As shown on the screen, IC designers can create stick diagrams using the STICKS graphics editor. Diffusion (green), polysilicon (red), and metal (blue) layers are easily differentiated in the color presentation.

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Technologies in vogue

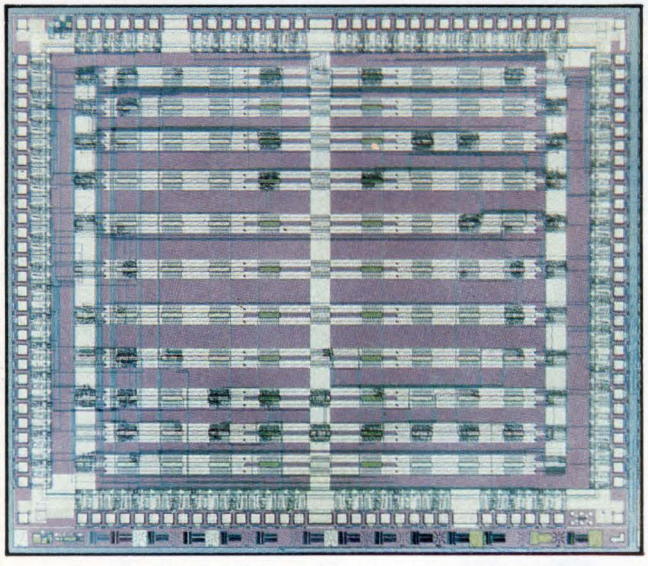
Gate arrays are available in a variety of processing technologies: CMOS; a few N-channel MOS (NMOS) arrays; and bipolar processes such as ECL, integrated injection logic (I^2L), Schottky transistor logic (STL), integrated Schottky logic (ISL), and current mode logic (CML). Presently, the trend in manufacturing processes is toward CMOS—a host of manufacturers now offers metal gate, silicon gate, and oxide-isolated CMOS. And when low power is required, CMOS is the obvious choice.

The newest 3-micron silicon gate CMOS technology beats or matches many bipolar technologies' performance without associated heat and power problems. CMOS also interfaces easily to MOS, TTL, and low power Schottky (LS)/TTL in inputs and outputs.

Several manufacturers offer this state of the art technology. In some silicon gate technologies, silicon dioxide is used for transistor isolation instead of the reverse biased pn junctions in standard CMOS. A compact circuit results, with die sizes comparable to equivalent bipolar, Schottky, or NMOS circuits. Typical silicon gate CMOS propagation delays are 3 to 5 ns/gate. American Microsystems, Inc (AMI), Santa Clara, Calif, claims 2 ns for its CMOS arrays. Power dissipation is as low as 0.00001 mW/gate.

Despite the apparent CMOS preference, there is a definite role for bipolar technology, especially ECL. For example, speed-driven applications require a process other than CMOS—ECL is the most touted. Gate delays of 0.5 ns and less are available with ECL. Signetics Corp's (Sunnyvale, Calif) ECL arrays use a 3-micron CML process with oxide isolation to attain gate delays of 0.35 ns with some functions. CML uses current switching rather than current steering, and lower thresholds for a power savings. Power dissipation is 2 mW/gate.

Another company that uses bipolar technology is Texas Instruments (TI), fabricating advanced STL arrays. Internal gate delays are 1 ns, with 300-μW typical power dissipation. In fact, Timothy John Chambers, TI's logic array marketing manager, feels that STL technology will continue to evolve. Arrays with dedicated structures such as read only memory (ROM) and random access memory (RAM) onboard will be available in the next five years. According to Chambers, input/output (I/O) cells will be designed with improved inter-array communications, probably using the JEDEC proposed 3.3-V low level TTL standard. Chambers also feels that as array densities continue to grow toward the 10k range, ECL will be limited by power requirements. He expects Schottky bipolar arrays such as TI's TATO20 ASTL series to fill the semicustom need in high performance systems.



A logic array, type TATO20, from Texas Instruments, with 2000 auto-routable gates. The array is manufactured with 2-micron design rules using advanced STL technology.

After a product is introduced, there is a time lapse before it actually appears in a design—and some of the newest high density gate arrays are no exception to this rule. First-time users are justifiably cautious designing a circuit in silicon. Most gate arrays are derived from existing circuits previously resident on printed circuit boards (PCBs). To minimize risks, users favor a limited redesign, in many cases using three or four small arrays rather than one large one. Also, large gate arrays may compete closely with standard cells. In fact, it can take less time to design a standard cell custom chip than a gate array.

Current array offerings seem to indicate that gate arrays have the most activity in larger devices. However, arrays can have tens of thousands of gates, yet the most commonly used arrays are much smaller (200 to 600 gates). High performance system manufacturers have their own reasons for using smaller arrays. Dr John Foggiatto, manager of process technology at Amdahl Corp (Sunnyvale, Calif), believes that testability is a major constraint on gate array size. The high speed ECL arrays used in the central processing unit of an Amdahl mainframe typically use 380 gates and require 1000 to 1500 test patterns to detect 90% to 95% of the faults. Increasing the number of gates increases the number of test patterns almost exponentially, according to Foggiatto.

Patterns for interconnection

Arrays are personalized through metallization, where one, two, or three masks specify the array's interconnections. In a single-level metal array, one mask is necessary for customization. Double-level arrays require three masks, one for each metal level and a third to define the interconnects between the two. Large arrays, usually more than 2000 gates, are customized with two metal levels. Because of the expanded range of interconnect options it offers, a large double-level metal array is easier to lay out than a similarly sized single-level array. Cell utilization is usually higher, especially when interconnections are automatically routed. Density gains of almost two to one over single-level arrays can be obtained. Interconnects are shorter, increasing circuit speed by minimizing parasitic delays.

To cut development time and use silicon efficiently, many manufacturers offer arrays with interconnected cells of gates or macro cells. Predefined-gate macros are connected to perform a function—they save the customer from designing the entire chip from scratch. Functionally, a macro can be a simple resistor or

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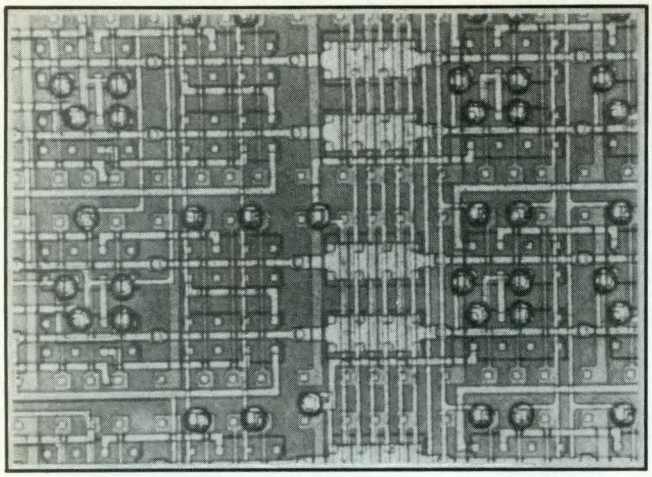


Oxide-isolated silicon gate CMOS gate array from International Microcircuits, Inc, for double-level metal interconnections. Individual logic cells can be seen, as well as via holes for connecting the two metal levels.

transistor, or a medium scale integration (MSI) complexity logical block. Macros can either be dedicated in silicon (hardwired) with a specific location on an array, or reside in a software library.

Motorola Semiconductor Products Inc (Phoenix, Ariz) is one company offering hardwired macros. The MCA 1200 ECL array consists of 106 logical macro cells—48 internal or major macros, 32 interface macros, and 26 output macros. Each logical block contains resistors and transistors interconnected to perform a logical function. Drawing from a library of 85 functions, users define the circuitry in each macro cell. One circuit pattern defines the macro cell as a multiplexer, another as a dual flipflop, another as an adder, and so on. The macro cells are then interconnected to completely personalize the chip. This requires the definition of two metal levels: the first defines the circuitry within each macro cell location, as well as the vertical routing channels; the second defines the horizontal routing and connections to I/O ports and between the two levels. Since macro cell placement is predefined, a uniform X-Y routing grid results, simplifying layout. Automatic place and route software utilizes 90% to 95% of the macro cell locations. With manual assistance, close to 100% of the possible macro cell locations can be used. Because the system uses silicon so sparingly, the company also uses it to develop standard products.

The second approach, software macros, also relies on placement of predefined macros on an array. However, the macro locations are not predefined. Macros are defined in software and individual gates are interconnected to form macros at the same time the whole array is characterized through metallization.

Design techniques—manual and automated

Designing with CAD systems, automatically placing and routing cells, and automatically generating test vectors is the trend in gate array design. Yet design and layout are still done manually on small arrays, and for high silicon usage on large ones. To facilitate manual design, many companies supply customers with design kits containing training documents and layout materials. For example, Interdesign Inc provides its CMOS customers with a 180-page CMOS design manual complete with processing information, logic conversion methods, and layout and testing guidelines. The customer then creates the schematic or logic diagram. At this point, the process could be automated to the extent that a computer based simulation can be run. Either Interdesign or the customer can then do the chip layout.

Large planning sheets are used to partition and organize an array. Adhesive functional overlays are placed on the layout sheet and interconnections are made with a pencil. Each logic cell is then listed by its alphanumeric coordinate—the design is verified and test

Technology shifts expand designers' options

In the custom and semicustom circuit design arena, there will be an increasing evolution toward standard cells and full custom solutions, according to Richard Thomas, vice president of semicustom products at American Microsystems, Inc (Santa Clara, Calif). Key factors in this evolution include a trend toward smaller geometries, increasing gate count complexity, a decrease in cycle times, and increased use of computer aided design tools.

"As the complexity of system configurations increases along with space constraints, there will be additional pressure for system designers to move toward standard cell and full custom circuits," Thomas says. "However, there will continue to be a strong market for gate arrays in the future. Gate arrays will still offer the advantages of rapid turn times, fixed size, and lower development costs. Thus, although the dynamics between the various custom and semicustom solutions may change, all of these options will continue to have particular systems applications."

Part of finding an appropriate solution among these options is evaluating the custom semiconductor vendor. "A primary concern should be the company's ability to service all of the customer's needs," Thomas stresses. "The semiconductor company should demonstrate the flexibility to work with a variety of customer inputs. The customer should be able to become involved at any stage—concept, logic description, or pattern generator tape. A full service custom vendor should have the capability of running silicon from a pattern generator tape, which is known as the customer-owned tooling approach."

After selecting a vendor, the design process begins. This can take place at the systems house, at an independent design house, or at the semiconductor company. With CAD tools, system designers can perform all or a portion of the design. For instance, they can do the frontend circuit simulation via a time-sharing system that hooks into a CAD system. The alternative is for the system integrator to license the CAD system from the IC company and perform the entire design process in-house.

Although the choices in the custom and semicustom circuit design arena may overwhelm the system designer, no one custom or semicustom approach will satisfy all integration needs. Despite the movement toward standard cells and full custom solutions, there remains room for alternative solutions based on timing, cost, and volume considerations.

Automated procedures simplify VLSI design

An automated approach to full custom VLSI circuits shortens design and manufacture time to just a few weeks, while retaining design control in the hands of the system engineer. With its roots in Mead-Conway methodology, VLSI Technology Inc's (San Jose, Calif) integrated design system has harnessed computer aided engineering to evolve from a concept to a practical reality. According to Wes Patterson, director of systems marketing, and Jim Rowson, manager of VLSI software, a design project can now be completed at costs comparable to standard breadboarding or gate arrays.

The designer begins by verifying his logical design using VSIM, a logic simulator. Then with automated layout procedures that simplify VLSI circuit implementation, he creates the data base for the IC.

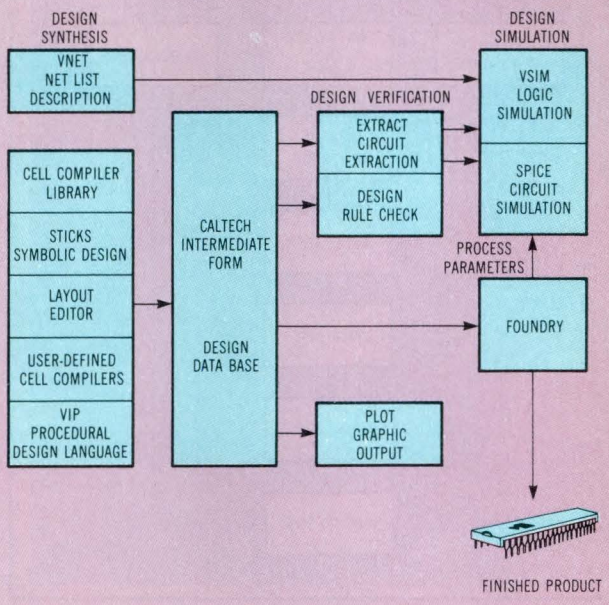
Unlike standard cell libraries, VLSI Technology's library contains cell compilers (generic cell descriptions that can be used to create cells with required performance and size characteristics). Typical compilers include those for ROMs, RAMs, latches, buffers, counters, a programmable logic array generator, decoders, I/O pads, and a pad-ring compiler. Using the cell compiler library, most of the circuit design and layout can be handled quickly and automatically. The custom cell portion of the effort is concentrated on the proprietary circuit elements.

STICKS, a graphics editor, allows designers to create and/or modify user-defined cells using symbolic stick diagrams. STICKS automatically generates layouts consistent with design rules, as specified in a technology file. STICKS can also compact these layouts within design rule constraints to minimize silicon area and reduce manufacturing costs.

To fine-tune the circuit detail, a graphics layout editor allows users to create or modify the layout data base directly. For this manual graphics editor, a design rule checker verifies that designs meet all design rules.

Users can also create their own compilers using the VLSI Implementation Program (VIP) language. All cell compilers are written in VIP. Cells created using the cell compilers, STICKS editor, or layout editor are composed into a complete chip using VIP. VIP has powerful composition features like relative cell placement, channel and routing routines, and parameterized busing. With VIP, the design layout can be adjusted automatically to design changes.

Simulation tools can check a circuit layout data base. A program called EXTRACT links the layout data base to the simulators for verification of layout accuracy and circuit performance prior to manufacture.



EXTRACT describes the chip in terms of connectivity, transistor dimensions, and parasitic capacitances. This description can be input to VSIM for logic simulation, as well as to circuit simulators that verify performance parameters. This extraction/simulation process is an important step toward guaranteeing good silicon on the first fabrication—an elusive goal with traditional hand-layout and checking methods. The end result is a full custom VLSI circuit.

inputs are described by a truth table and timing information. The completed package is then submitted to Interdesign for review. If approved, the company continues the digitizing, tooling, prototype processing, and testing. The customer then reenters the cycle by evaluating the prototypes in the system under development. Full production takes place 8 to 10 weeks later. This process works well for small arrays, but the company depends on CAD horsepower for larger devices.

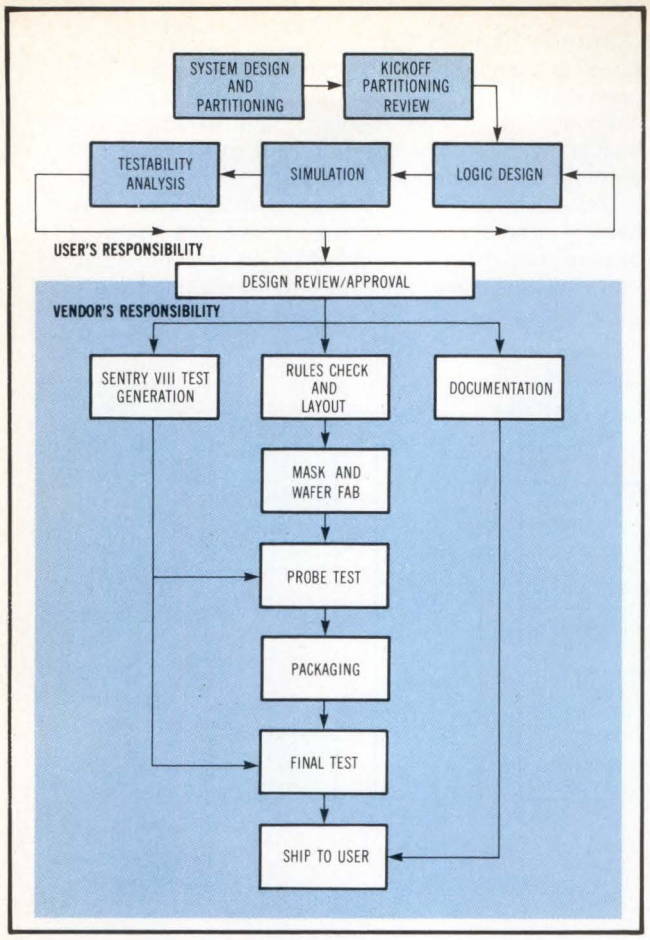
A highly automated array design system has been developed by Storage Technology Corp's (Louisville, Colo) Microtechnology Div. Its computer aided engineering (CAE) system integrates design, simulation, layout, tooling, and test generation. Customers can supply a simulation tape from their in-house system, or a schematic or logic diagram. Once the simulation is complete the data base is linked to the layout software. Circuit elements are automatically placed and routed and a delay analysis is generated. The output file goes directly to E-beam or pattern generation (PG) software and tooling is generated.

Both manual and automatic design methods offer the customer some choice regarding what he supplies the vendor and how involved he must be in the design process. Companies like California Devices Inc (San Jose, Calif) allow the customer to jump in just about any place. Although the customer can lower development cost by doing more design, he also assumes a greater risk.

Preference in vendors

Selecting a gate array vendor may be as crucial as creating the logic diagram, especially for the novice. Gate array vendors provide a service—the type and quality of that service is as varied as the products. With so many startups and established standard product manufacturers moving into the gate array market, the buyer should consider several manufacturers before making a choice. A company's possible gate array offerings include macro availability, design process and support, CAD or CAE systems, customer support, and training programs. Production capability, including testing and inventory control, should also be scrutinized.

One system integrator, DMA Systems (Goleta, Calif), believes that a gate array vendor should assume the majority of the design responsibility. The company uses gate array technology for its fixed/removable disk



A typical gate array design cycle from Storage Technology Corp's Microtechnology Div. The development process is divided into user and company responsibilities.

drives. Unless specialists are available in-house, the company recommends that integrators find a vendor who will be responsible for the logic conversion, circuit design, and layout.

This recommendation is in sharp contrast with another semicustom trend—vendors are opening their doors to customers, developing regional design centers, linking customers to their computers via remote terminals, and selling hardware and software packages—all in an effort to get customers to participate in the design of their own gate arrays. Most vendors invite customers in to be trained or to design arrays. Others, such as TI, Motorola, Fujitsu Microelectronics Inc (Santa Clara, Calif), and Storage Technology Corp's Microtechnology Div have established regional design centers to support their gate array products. Both approaches offer the customer handholding support that would not be available if the design were done in-house. Training usually takes three to five days and involves learning array design techniques and using the company's CAD system.

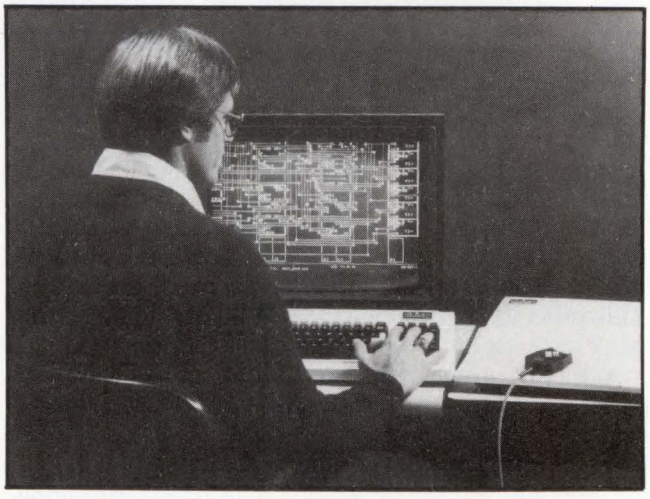
A more recent development is the lease or sale of vendor designed gate array CAD software or hardware. TI recently announced a transportable design automation software package to run on a customer's computer. The software includes design description languages, a high level function library, simulation, test analysis, and design rule verification. The multi-user system is written in Pascal and runs under VAX 11/780 and IBM 4341 operating systems. Similarly, Interdesign will soon be selling its Designer CAD hardware and software system, designed around the DEC PDP-11/23. Included in the system's peripherals are a high resolution graphics terminal, digitizer, plotter, and DECwriter console.

Controlling inventory at a semicustom or custom manufacturing facility can be problematic. A gate array vendor may help design and produce as many as 200 to 300 unique circuits a year, with 150 to 200 chips in process simultaneously. Newcomers to the gate array market, particularly companies that have formerly produced only standard parts, have to develop a system to control the material and information flow.

Despite the benefits of gate array technology and the predictions of phenomenal growth, there are some drawbacks. For example, testing arrays can be a bottleneck in the production cycle. Achieving test sequences that can detect over 90% of potential faults requires many man-hours and extensive computer assistance. Arrays with more than 2000 gates may require test circuitry onchip. Testing times can be cut by adding logic or I/O pads for access to internal nodes (eg, a line running into the chip to reset storage cells).

Moreover, the lack of standard design languages may eventually limit the technology's growth. Each manufacturer has a different customer interface, documentation, and design language. Therefore, using two or more manufacturers (or technologies) becomes extremely difficult. Although multiple sourcing of arrays is a well-documented problem, little has been done in the way of solutions. Standard hardware and test description languages would be a step in the right direction.

Semicustom and custom development, especially standard cell based, are not mutually exclusive. Some manufacturers recommend developing a gate array to test the market and then following up with a custom design if the product "flies." AMI has worked with customers on the parallel development of gate arrays and custom circuits. The gate array gets the product on



The GATEMASTER™ from Daisy Systems Corp (Sunnyvale, Calif) is the first gate array development system to unify the design process from an engineer's conception to the finished layout. Using a portable, standalone design system that draws from a single design data base, the designer can develop a design interactively, switching from the functional level to schematic, simulation, or layout levels without having to recreate the entire design. The GATEMASTER also represents a significant cost reduction from external placement and routing programs.

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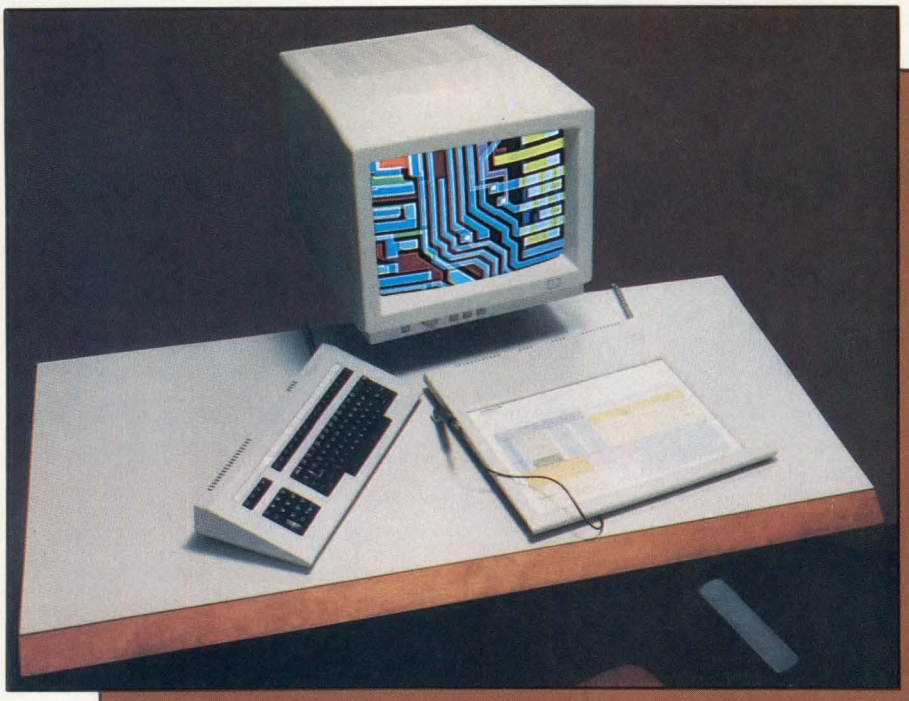

Series 4000 CAD/CAM systems from Applicon (Burlington, Mass) improve productivity by bridging the gap from design to production. Addressing every phase of IC development, these systems automate repetitive and time-consuming tasks. Application-specific software speeds and simplifies the complex layout, placement, and routing of ICs.

the market quickly and the custom circuit, with a higher integration level, cuts costs later on. Much of the gate array design can be transferred to the custom circuit, including the test program and schematic.

Custom fit for size

System integrators will have to look beyond gate arrays and programmable array logic if large size, high density, super performance, or all three are required in a custom circuit. Fortunately, advances in CAE, standard cells, training, and foundry sources make custom circuitry feasible for many integrators.

One custom solution, standard cell technology, uses silicon more efficiently than gate arrays. For a standard cell, the silicon cost is often half of what it would be for a functionally equivalent gate array. Like macro cells, standard cells can be keyed to small scale integration/MSI functions. Theoretically, an engineer familiar with PCB design should be able to design with standard cells.

State of the art design automation tools—key components in the standard cell concept—shorten design time, reduce development cost, and help ensure that a design works after processing. Standard cell based circuits are available in CMOS, NMOS, and several bipolar technologies.

Standard cells are designed by IC designers who understand silicon device physics, topological logic, and semiconductor processing. William Loesch, marketing manager at ZyMOS (Sunnyvale, Calif), describes standard cells as "a link between the expertise of the IC designer and the system designer." Designed to use silicon efficiently, standard cells do not have the redundant logic cells that characterize gate arrays. Also, designers are not restricted by a limited number of gates or by chip organization. Some system designers have found that with fewer restrictions, a standard cell design can take less time than a gate array.

The ZyMOS ZyP system is an example of one standard cell application. It uses standard cells the same way a mathematical transform maps parameters from one coordinate system to another—a description of logical functions is transformed into photolithographic masks. The system is available to subscribing designers and can either be accessed through a timesharing network or installed on a computer at the customer's facility.

There are several ZyP design steps. First is the logic/circuit design. The designer selects standard cells from the applications library and enters an alphanumeric listing that specifies the desired standard cell interconnections. Second, the designer must verify, using an event-driven logic simulator, that the selected interconnection meets the required circuit timing and logic specifications. Third, the cell network listing is input to the artwork generation software module after functional and performance requirements are verified. The module then produces an initial cell placement and routing diagram. If changes in the cell placement are required at this point, they can then be relocated. Finally, the test program generation software module processes the output from the logic simulator to generate a functional test pattern compatible with the Fairchild Sentry VII tester.

Another company, AMI, uses a symbolic interactive design system (SIDS) for standard cell design. Like other standard cell systems, the cells have 4000 CMOS series or 74 LS/TTL equivalent structures. Customers can use the SIDS system to create new cells or modify existing ones. Functions such as analog elements or RAM and ROM can be designed and merged with standard cells. This standard cell system is a bridge to full custom design. AMI also licenses its software systems and NMOS and CMOS cell libraries, allowing customers to design circuits at their own facility.

Full custom ICs, another custom solution, are sometimes called handcrafted circuits. (At one time, custom

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ICs were designed by hand to attain the highest possible density and performance.) Smaller circuits can still essentially be designed by hand. The Mead-Conway method is very useful as a handcrafted IC design method. (See "Crafting a Custom Sorted Access Memory," p 173, this issue.) The technique not only brings system designers into the IC design process, but it is also easy to learn. For very large scale integration (VLSI), however, designers need CAE.

Interweaving techniques

Full custom IC design and standard cell based design are often viewed as competing techniques. However, a great deal of standard cell technology is used in full custom chips. Full custom houses such as VLSI Technology Inc (San Jose, Calif), SynMos Corp (Mountain View, Calif), International Microelectronics Products (San Jose, Calif), and AMI offer standard cell libraries for use in designing custom circuits. If the library's standard cells are not appropriate, the designer can design non-standard cells for repetitive use in his circuit.

One example is Hewlett-Packard's (Palo Alto, Calif) design of a set of three full custom floating point processors. As commercial LSI devices were shy on performance, using discrete and low level integrated components, ECL for example, would have required a couple of PCBs and used too much power. Therefore, the company had to design three custom CMOS-on-sapphire chips. The company borrowed standard pad cells from its internal library and also created its own custom standard cell library. These cells (adders, registers, shifters, incrementers, etc) were used on all three chips.

Here, an important distinction between a standard cell based and full custom design can be made (ie, the origin of the cells). Standard cells come from a library and full custom circuits are designed especially for the custom chip. With full custom circuits, of course, the designer must bring a deeper understanding of silicon to the design.

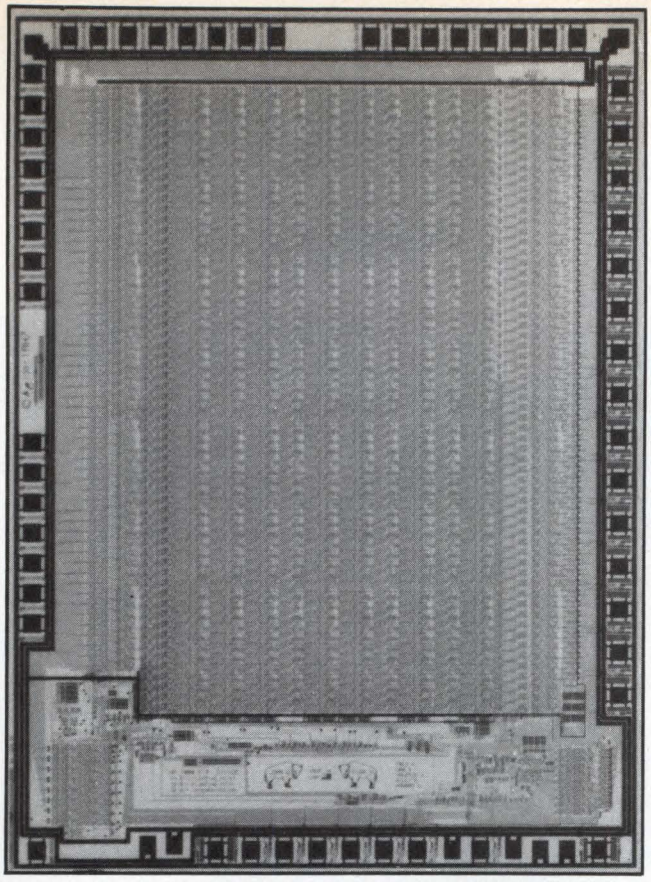
Custom VLSI circuits have now become a viable alternative for system designers due to advances in computer based design and verification automation. Computers have shortened the design cycle, reduced costs, and increased the probability of a custom IC working as intended. VLSI Technology Inc, a strong Mead-Conway devotee, has developed a design system linking synthesis, verification, simulation, and processing. This system goes several steps beyond basic Mead-Conway design and provides an integrated set of tools for large scale, fast turnaround custom design.

Piecing together a custom chip

While custom chip designers still need to know the basic design rules of the process they are designing in, CAE systems remove much of that burden. The same is not true of processing, however. Locating a processing source and overseeing custom chip production requires knowledge of semiconductor processing. Chip production facilities and what they provide vary. There are independent fabricators who will accept customer-owned tooling. Silicon foundries, as envisioned by Carver Mead, professor of computer science and electrical engineering at the California Institute of Technology, Pasadena, would provide standardized geometrical design rules, data interchange format, and a monitor to test chip structures and thus control the production process. By locating more than one such independent processor, a customer can create alternate sources.

Silicon brokers can assist system designers in custom chip design and production. The silicon broker interfaces between the designer and processor vendor. The goal is to minimize the designer's involvement in process

A section of a typical custom IC circuit appears on the VIA Systems, Inc (N Billerica, Mass) Model 110 color graphics screen. The Model 110 is a single-user, color, interactive graphics system for IC design. It features a high resolution 19″ color graphics screen with 16 colors, 3 computers, and over 700,000 bytes of memory.



Hewlett-Packard's full custom CMOS-on-sapphire 64-bit processor for floating point division. Note the repetitive logic that simplifies design and ensures efficient use of the available chip area.

details, allowing him to concentrate on functional chip design. The broker may also rent development tools or directly market CAD tools. In addition, the broker can provide the designer with a low cost, fast turnaround prototyping service (eg, multiproject chip fabrication).

Testing custom chips can be even more problematic than testing semicustom devices. AMI estimates that as much as 20% of a custom circuit's cost can be spent generating test parameters. Onboard circuitry can improve a chip's testability, but this circuitry can occupy up to 5% of the chip.

With custom circuit relationships still in transition, there are no foregone conclusions as to the direction of custom trends. However, there are some signs of what is to come. Standard cells, for instance, will impact both gate arrays and full custom approaches. Also, higher levels of integration mean that custom circuits will soon absorb the processors themselves, rather than the circuitry around them. ZyMOS already offers a 4-bit core processor as part of its standard cell library. Customizable processors are offered by AMI, and TI's SCAT technology allows processors to be designed to order. But in the midst of change, one thing is certain: CAE tools made custom ICs possible. Moreover, the movement toward engineering workstations should have a major impact on custom design.

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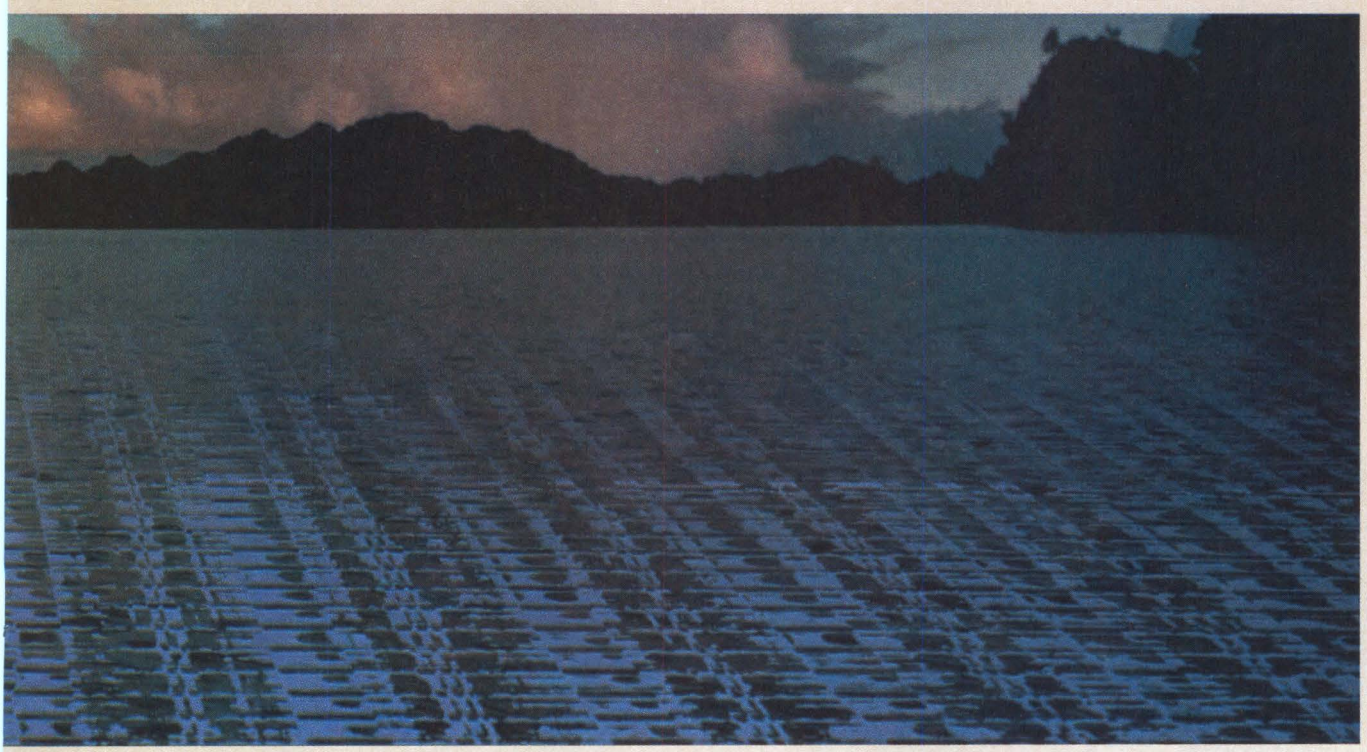

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CORE MICROPROCESSOR SPEEDS CHIP DEVELOPMENT

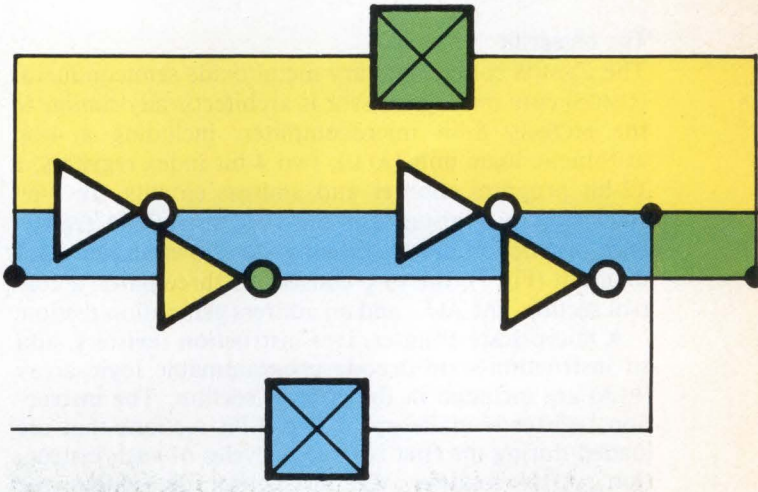
Using a 4-bit microprocessor cell and surrounding it with functions from a standard cell library speeds development of semicustom microcomputer chips.

by Jay Miner

A recently introduced design concept now extends the reach of semicustom design into microcomputer levels of system integration. Built upon the development of standard cell libraries, this "core microprocessor" adds an entire 4-bit central processing unit as a module in such a cell library. The new cell is a general purpose microprocessor without memory or input/output ports. The designer need only add appropriate random access memory, read only memory, timers, counter, and input/output modules from the same library to complete a user-defined architecture of a customized microcomputer chip.

The core microprocessor fills in the gaps that existed between the capabilities of off-the-shelf devices. Without a core microprocessor, a system designer must either use additional chips to boost the performance of a weak processor or pay for the unused performance of a more powerful device. Using full-custom or semicustom devices is a less than perfect solution to the problem.

Jay Miner designs special purpose computers, including several 8-bit CMOS designs for pacemaker applications, at ZyMOS Corp, 477 N Mathilda Ave, Sunnyvale, CA 94086. Previously, Mr Miner designed the Atari VCS video game chip logic, and was in charge of the design of the three custom chips in the Atari home computers. He has a BSEE from the University of California, Berkeley.



Although the full-custom approach yields the most efficient use of silicon, high development costs make it practical for only large production volumes. The economical advantage of semicustom design for moderate production volumes diminishes as chip complexity approaches that of a microcomputer.

Formerly, the level of cell complexities in standard cell libraries was limited to small scale and medium scale integrated circuit modules of gates and flipflops. Consequently, development costs increased significantly with mounting chip complexity. Since a central processing unit (CPU) module comprises about 5000 transistors, this level of integration in a single library cell gives the system designer a significant head start in solving complex system problems with semicustom chip design. The

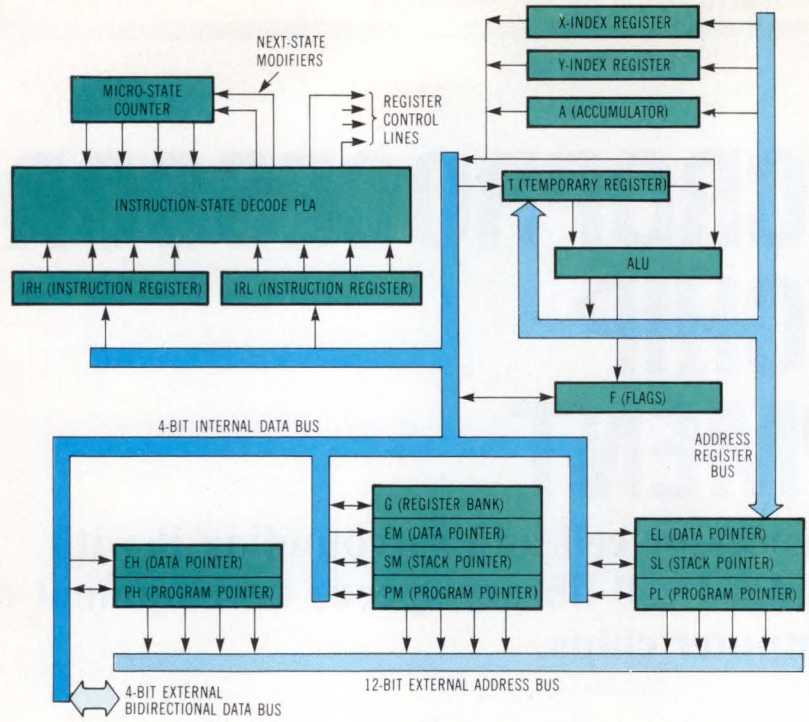


Fig 1 Core microprocessor architecture is similar to that of MCS6502 8-bit microcomputer. Combined with rich instruction set, processor has features previously unavailable in 4-bit machines.

4-bit CPU provides a module of general purpose functions that the designer can tailor by adding other standard cell functions.

The blueprint

The ZyMOS complementary metal oxide semiconductor (CMOS) core microprocessor is architecturally similar to the MCS6502 8-bit microcomputer, including a 4-bit arithmetic logic unit (ALU), two 4-bit index registers, a 12-bit program counter and address circuits, an 8-bit stack pointer register, and an 8-bit instruction register with instruction decode circuits. As shown in the block diagram (Fig 1), the CPU consists of three parts: a control section, the ALU, and an address generation section.

A micro-state counter, two instruction registers, and an instruction-state decode programmable logic array (PLA) are included in the control section. The instruction register is made up of two 4-bit sections that are loaded during the first two clock cycles of each instruction. After loading, the instruction determines the counter states and register control line activation.

Four ALU registers, a flag (status) register, and the ALU are contained in the ALU section. The ALU is basically a 4-bit adder-shifter. The X and Y registers are 4-bit index registers. Register A is a 4-bit accumulator, and register T is used for temporary storage. The 4-bit flag (status) register holds the carry, zero, negative, and overflow flags.

The address generation section assembles and outputs the addresses required for instruction fetch (program pointer), for data fetch and store (data pointer), for stack push and pull (stack pointer), and for indirect-address-register block selection (block pointer). Both the program pointer and the data pointer produce a 12-bit address; therefore, either instructions or data can reside anywhere in separate 4k memory blocks. The 8-bit stack pointer allows many levels of subroutines and interrupts to be nested. The block pointer resides in one 4-bit register, designated G. This register is used with the low nibble—4 bits—of the data pointer EL to form an 8-bit address. There are 16 registers per block (addressed by EL) and up to 16 register blocks (selectable by G) in page 0.

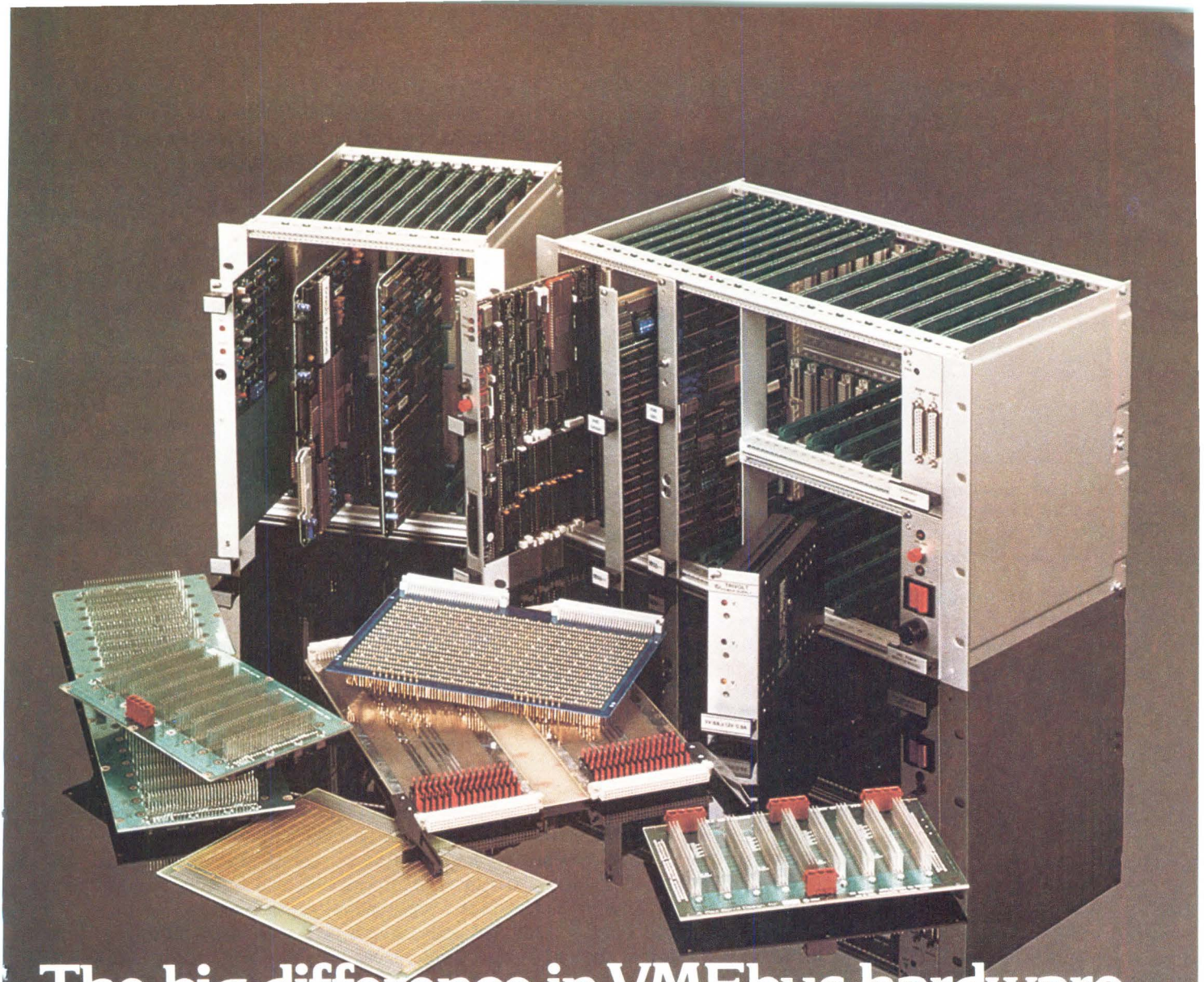
Saving power around the clock

User-defined circuits that sense a predetermined signal or combination of signals can stop the CPU clock. During this so-called "sleep state," timers continue to run and inputs continue to be sensed. But the processor conserves power by not executing program instructions until a switch is activated or some other event signal causes the clock to resume operation. This feature is useful in energy-sensitive applications that require intensive but infrequent microcomputer usage, such as pacemakers or aerospace equipment.

To retain data during periods of dormancy, the registers on the microcomputer chip must be static circuits that do not require data refresh clocking. The core microprocessor registers retain data because they use "pseudostatic" latches (Fig 2). Latches retain data as long as the phase 1 gate is at a logical 1 and the phase 2 gate is at logical 0. An external signal can command the processor clock to stop in this state, and the stop signal can be removed by a switch or timer timeout, for example.

Flexible memory expansion

Memory module cells available for user-defined microcomputer designs are all 4 bits wide. Random access memory cell options are 64, 128, and 256 x 4 bits, while read only memory (ROM) cells can be 512, 1024, or 2048 x 4 bits.



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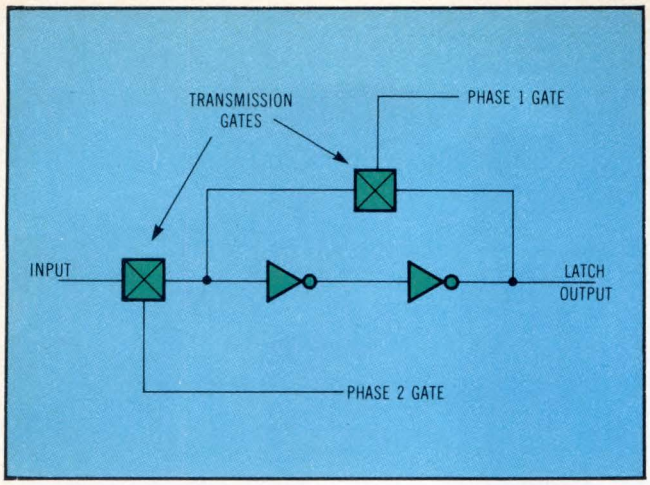


Fig 2 Pseudostatic data storage allows system clocks to be stopped during processor "sleep states" to conserve power. Registers use sample-and-hold latches like the one shown to retain data without refresh clock cycles.

The maximum amount of data or instruction memory that can be added to the core microprocessor is 4k, making a combined total of 8000 memory addresses—half for instructions and half for data. Each memory address selects a 4-bit nibble of data or instruction. Three mutually exclusive memory control lines—instruction read, data read, and data write—determine which memory type is connected to the data bus during each machine cycle.

While it is possible to combine data and instruction memory, this practice drastically reduces available memory space and has little advantage for a small, single-chip processor where instructions are usually in ROM anyway. Since each instruction requires from two to eight addressed nibbles, a 4k ROM can hold only 500 to 2000 instructions. Therefore, it is important to separate data memory from instruction memory in order to maximize program size. Lookup tables, for example, should be placed in data memory ROM instead of in program ROM.

By using latches and pad drivers from the cell library, the designer can customize a variety of input/output (I/O) ports such as serial, unidirectional, bidirectional, edge-detecting, and parallel-load serial shift. Similarly, the variety of timer designs possible includes adjustable prescale divider (for clocking other items), count-up, count-down, load-only, and read-write timers.

Because the core microprocessor is a CMOS chip, it is easier to include onchip linear functions than it is with N-channel metal oxide semiconductor devices.Therefore, linear circuits such as operational amplifiers, comparators, and even analog to digital converters and digital to analog converters can also be built into the microcomputer chip.

The instruction set of the core microprocessor is similar to that of the 6502 8-bit microcomputer. Although there are 256 instruction codes, most are addressing-mode variations on a few basic operations and are consistent and easy to learn. For example, all addressing modes apply to all memory reference instructions. As a result, the programmer does not have to remember that the direct-indexed address can only be used for add and subtract operations or that the register indirect index applies only to load and store instructions.

There are three basic types of addressing modes: implied, memory reference, and program control. The first three cycles of all modes are identical; the first two cycles of each instruction fetch the instruction opcode; the third cycle is used for opcode decoding and for fetching a third instruction nibble that may or may not be used.

The core microprocessor architecture plus the instruction set combine to provide several interrupt functions. For example, a "halt request" line stops the machine to allow external access to the address data bus, while an "interrupt" line stops program execution so that the processor can jump to and execute an interrupt service routine. The software masks this vectored interrupt, enabling the processor to ignore subsequent interrupt signals until the current one is serviced.

A power-on reset vectored interrupt executes a special power-on service routine to initialize operation each time the unit is turned on. A special test interrupt, useful for developing test programs, provides means for checking the processor, memory, and I/O. This operation includes an automatic ROM dump that dumps instruction memory onto the memory bus at the rate of one nibble per cycle. Another feature convenient for system development is a software interrupt instruction that allows a programmer to execute the program in single steps for debugging both hardware and software.

Addressing modes simplify programming

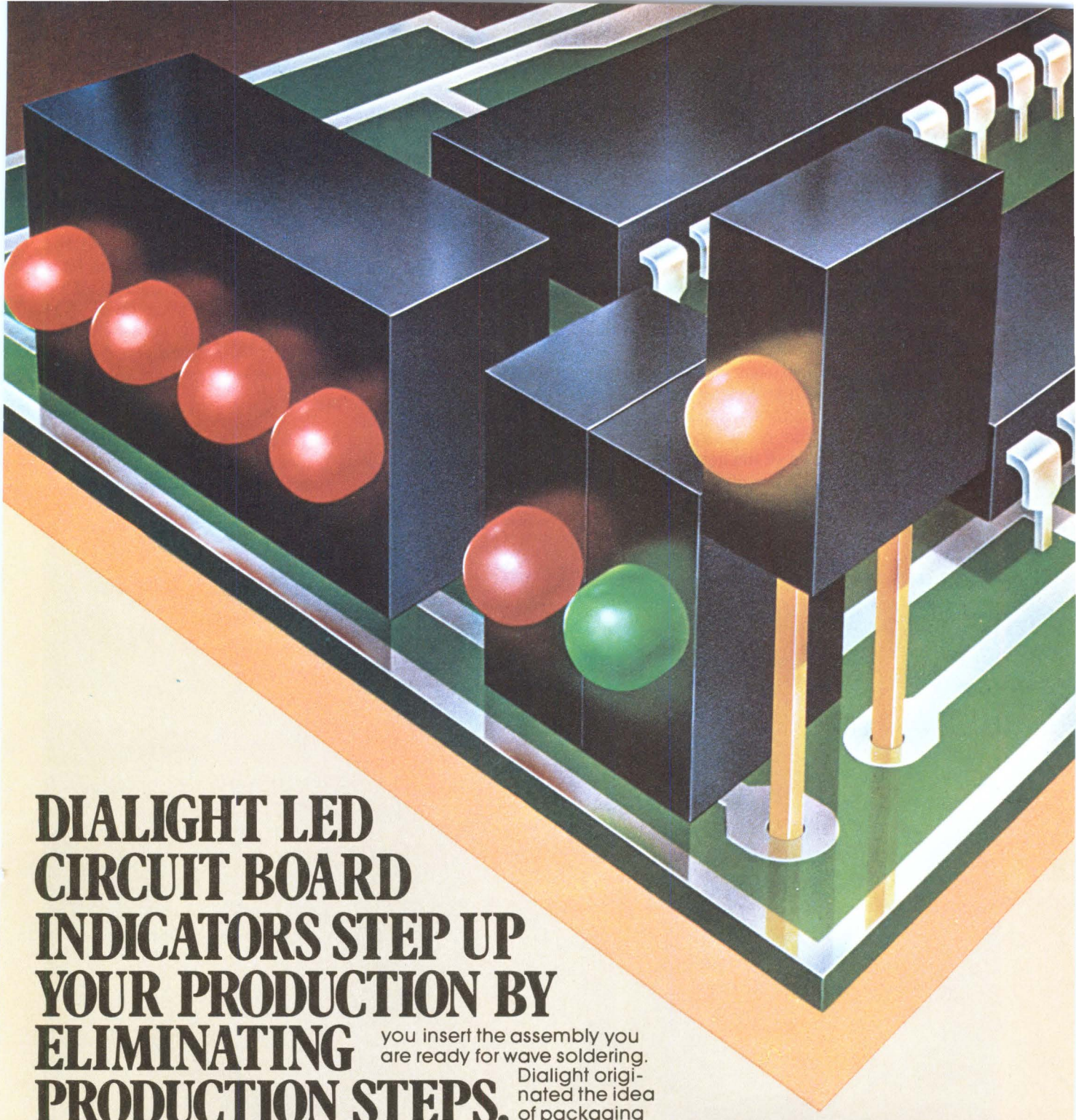
Although there are about 256 instructions in the instruction set, they are basically addressing mode variations on a few fundamental instructions and are, therefore, easy to learn. These advanced addressing modes are unusual in 4-bit processors, and include direct, direct indexed, and register indirect indexed.

Implied addressing is used with instructions requiring no memory references because their data locations are defined in their opcodes. These include instructions such as increment X register (INX); transfer accumulator to X register (TAX), and right rotate accumulator (RRA).

Memory reference addressing is used with instructions requiring fetching or storing data in memory. The last cycle of most memory reference instructions overlaps the first cycle of the following instruction and is, therefore, not counted. There are two types of memory reference instructions: single (only one memory access) and double (two memory accesses). The double types are all memory to memory operations such as right rotate memory (RRM) and increment memory if carry (IMC). These doubles are identical to the singles except for an extra memory store at the end of each instruction to return the result to memory.

The memory reference addressing modes, shown in the Table "Core Microprocessor Addressing Modes," are for single memory references (fetch or store). Double memory reference instructions (fetch and store) have two additional cycles—one to finish the operation and one to store the result in memory. The immediate mode has no doubles equivalent.

The immediate (#) mode is the simplest addressing mode since the data operand is fetched from instruction memory as one more nibble after the opcode. In the direct (D) mode, the CPU fetches two more nibbles from instruction memory after the opcode. These nibbles are used as an 8-bit direct address into memory page 0 to



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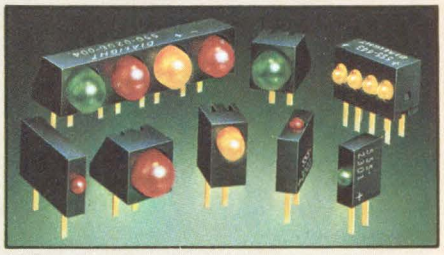

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fetch the operand on page 0. The direct indexed by X (D, X) mode is the same as direct, except the X index register is added to the low nibble of the direct address before use.

All register (R) modes require one more nibble fetched from instruction memory after the instruction opcode. This extra nibble is the address of 1 of 16 registers within the current register bank. This mode uses the contents of the register (R) as the operand. A 4-bit register bank pointer (G) identifies which of 16 register banks—all located in page 0 data memory—is currently in use. Instructions are provided to modify G.

The register indirect, indexed by X [(R), X] mode also fetches an additional nibble from instruction memory as a register address in the current register bank. The content, however, of this first register location (R) is not used as the final operand. Instead, it is added to the X index register and the sum is used as the low nibble of a new address. The content of the next location (R + 1) is used as the medium nibble of this new address. Zero is used as the high nibble. This new address points to the final operand anywhere in page 0.

Register indirect, indexed by Y [(R), Y] (not shown in the Table) is identical to [(R), X], except the Y index register is used in place of the X index register.

Absolute register indirect, indexed by X [(R), X] uses the contents of three sequential register locations—combined with the index register—to form a 12-bit address to point anywhere within the total 4k of memory. The content of the first register location (R) is added to the X index register and used as the low nibble of the address. The content of the next location (R + 1) is used as the medium nibble, and the content of the next location (R + 2) is used as the high nibble of the 12-bit operand address to access 4k of memory.

Determining design

Full-service custom houses can contribute to all phases of chip design, from system concept through prototype delivery. However, those with fabrication facilities,

Core Microprocessor Addressing Modes

Mode	Addressing Cycles	Memory	Address	Data	Comments
Immediate	1	Instruction	PC	IRH	Opcode fetch high
	2	Instruction	PC + 1	IRL	Opcode fetch low
	3	Instruction	PC + 2	Opnd	Third nibble used as operand
	*				Finish operation
Direct	1	Instruction	PC	IRH	Opcode fetch high
	2	Instruction	PC + 1	IRL	Opcode fetch low
	3	Instruction	PC + 2	DL	Operand address is
	4	Instruction	PC + 3	DM	part of instruction
	5	Data	0, DM, DL	Opnd	Fetch operand (page 0)
	*				Finish operation
Direct,	1	Instruction	PC	IRH	Opcode fetch high
indexed by X	2	Instruction	PC + 1	IRL	Opcode fetch low
	3	Instruction	PC + 2	DL	Operand address is
	4	Instruction	PC + 3	DM	part of instruction
	5	Data	0, DM, DL + X	Opnd	Fetch operand (page 0)
	*				Finish operation
Register	1	Instruction	PC	IRH	Opcode fetch high
	2	Instruction	PC + 1	IRL	Opcode fetch low
	3	Instruction	PC + 2	R	R = register number (0 through F)
	4	Data	0, G, R	Opnd	Fetch operand (page 0, Bank G, Register R)
	*				Finish operation
Register	1	Instruction	PC	IRH	Opcode fetch high
indirect,	2	Instruction	PC + 1	IRL	Opcode fetch low
indexed	3	Instruction	PC + 2	R	R = register number (0 through F)
	4	Data	0, G, R	(R)	Fetch contents of R
	5	Data	0, G, R + 1	(R + 1)	Fetch contents of R + 1
	6	Data	0, (R + 1), (R) + X	Opnd	Fetch operand (page 0)
	*				Finish operation
Absolute	1	Instruction	PC	IRH	Opcode fetch high
register	2	Instruction	PC + 1	IRL	Opcode fetch low
indirect,	3	Instruction	PC + 2	R	R = register number (0 through F)
indexed	4	Data	0, G, R	(R)	Fetch contents of R
	5	Data	0, G, R + 1	(R + 1)	Fetch contents of R + 1
	6	Data	0, G, R + 2	(R + 2)	Fetch contents of R + 2
	7	Data	(R + 2), (R + 1), (R) + X	Opnd	Fetch operand
	*				Finish operation

*Last cycle of instruction overlaps first cycle of following instruction.

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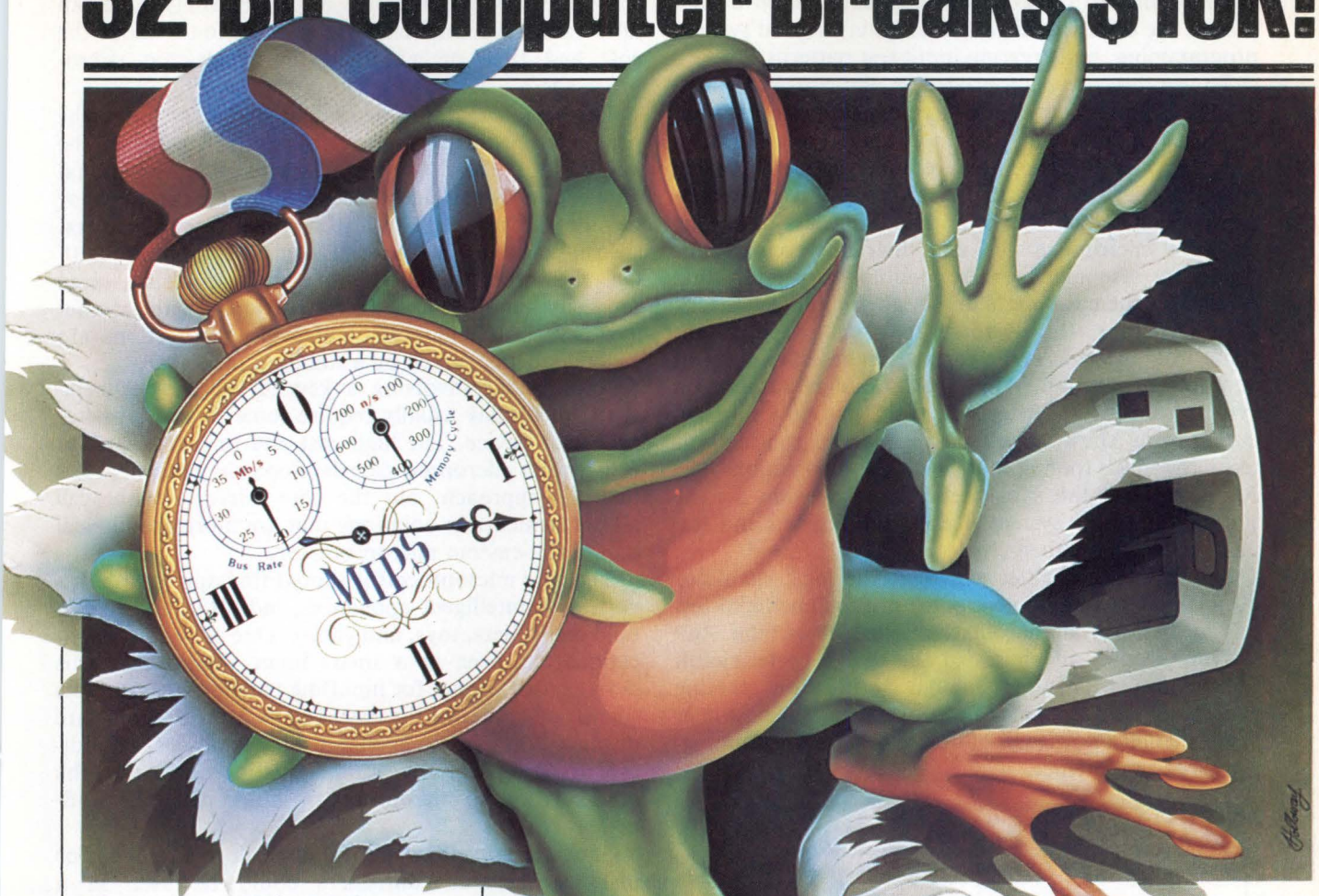

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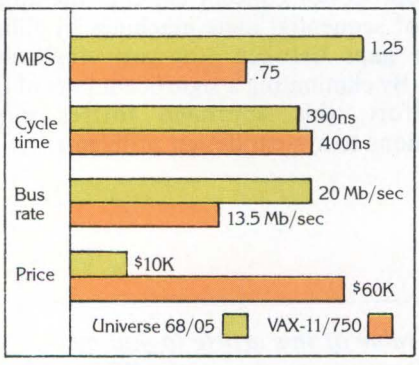

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CIRCLE 92

such as ZyMOS, are primarily interested in processing silicon to customer specifications. They are less interested in being involved in design because engineering manpower is limited. In addition, customers often do not foresee the effort required for designing a good system, programming, and creating input test patterns.

To use the core microprocessor, the customer must, at an absolute minimum, describe a system operation, including inputs, outputs, and timing relationships. This lower entry level, however, increases engineering costs significantly. The highest entry level is a chip network listing, which is a list of standard cells—including the core microprocessor—and their interconnections. There are also many other possible entry levels that depend on the customer's design ability and desires.

In any case, the customer's design specifications result in a network listing for automatic cell placement and interconnection. The ZyMOS design automation system, called ZyP, then converts this data to a chip layout drawing showing cell placement and routing patterns for mask tooling and prototype fabrication. The computer uses the same network to provide a logic simulation of the system. Design verification and test input patterns are then created.

Finally, the computer generates the logic simulator output patterns and converts them into functional test parameters for an automatic tester. Thus, the ZyP system executes all phases of the design cycle: circuit design simulation, logic design verification, tooling generation, and test program conversion. The customer needs neither knowledge of device physics nor topological design experience.

Solving problems a new way

With the addition of an entire microprocessor to a cell library, the traditional tradeoffs between standard and full-custom microprocessors no longer apply. One can now have a minimal chip system solution without the cost and time of a full-custom single-chip microprocessor.

The biggest factor in determining whether to use the core microprocessor is the size and speciality of the application. The ideal candidate is a computational application requiring a relatively small amount of memory (500 to 2000 instructions), special timers, special ports, or other special logic external to the CPU. On the other hand, applications requiring large programs—more than 2000 instructions—with external memory chips and many standard I/O functions are probably better served by a standard processor.

Applications involving a keypad, numeric calculations, or display usually require some sort of a microprocessor device. The high cost and time required for full-custom microprocessor development generally rules out this approach, but the core microprocessor cell allows semicustom solutions that are more economical than a full-custom microprocessor.

The core microprocessor should find application in a variety of intelligent appliances, industrial and household controllers, toys, and games. One of its first applications has been in a smart home thermostat. This device has a keypad for inputting temperature setpoints for various times of the day. Temperature and time are displayed on a liquid crystal display indicator. In addition to using less power than existing devices on the market, the core microprocessor should make the product easier to use.

Similar applications are not difficult to envision. For instance, several controllers could be used in a distributed-thermostat climatic control system that maintains different temperature setpoints in several areas. Such multiple processor configurations might be fitted with a battery of sensors to maintain lawn moisture levels or to control outside and inside lighting. Similarly, distributed process controllers could predict and avoid temperature over- and undershoots. Home control systems might also benefit from the use of a microcomputer. For example, whistle- or clap-actuated equipment could be designed to recognize many different commands.

The core microprocessor concept enriches the application potential of sequential logic machines by filling the performance gaps between standard single-chip microcomputers. By eliminating a significant part of the development effort, this approach invites more imaginative solutions to system design problems.

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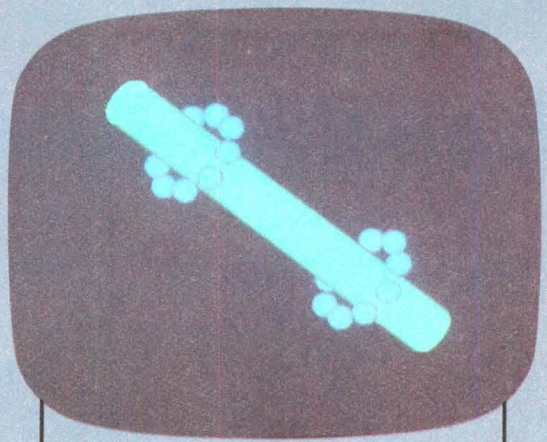

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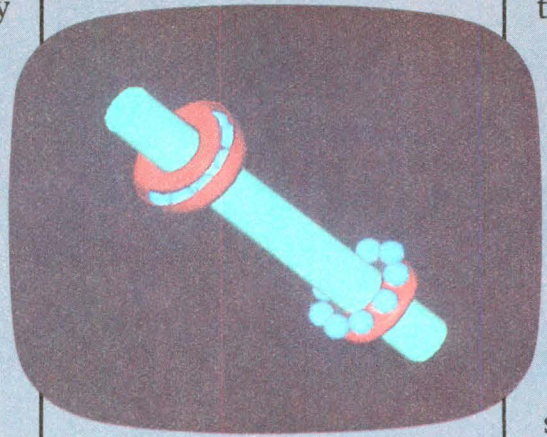

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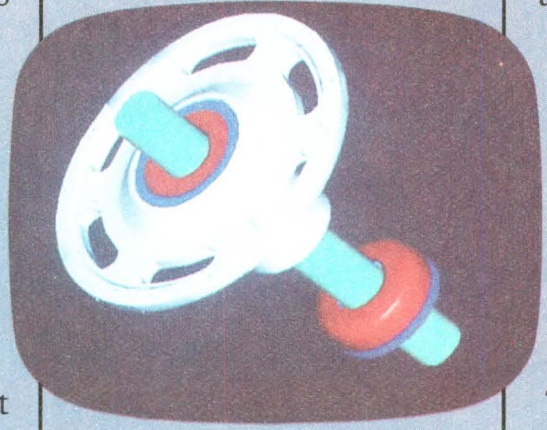

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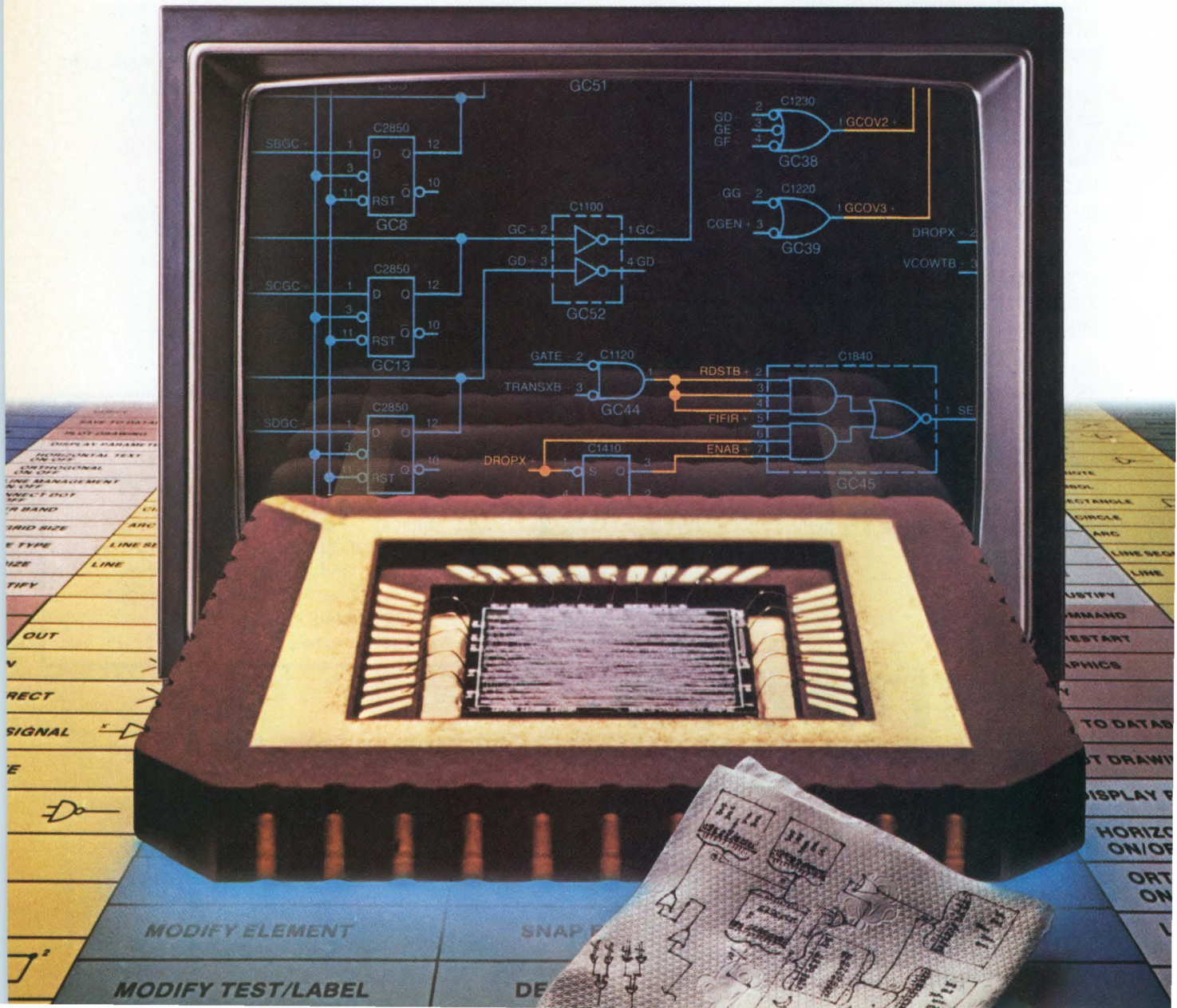

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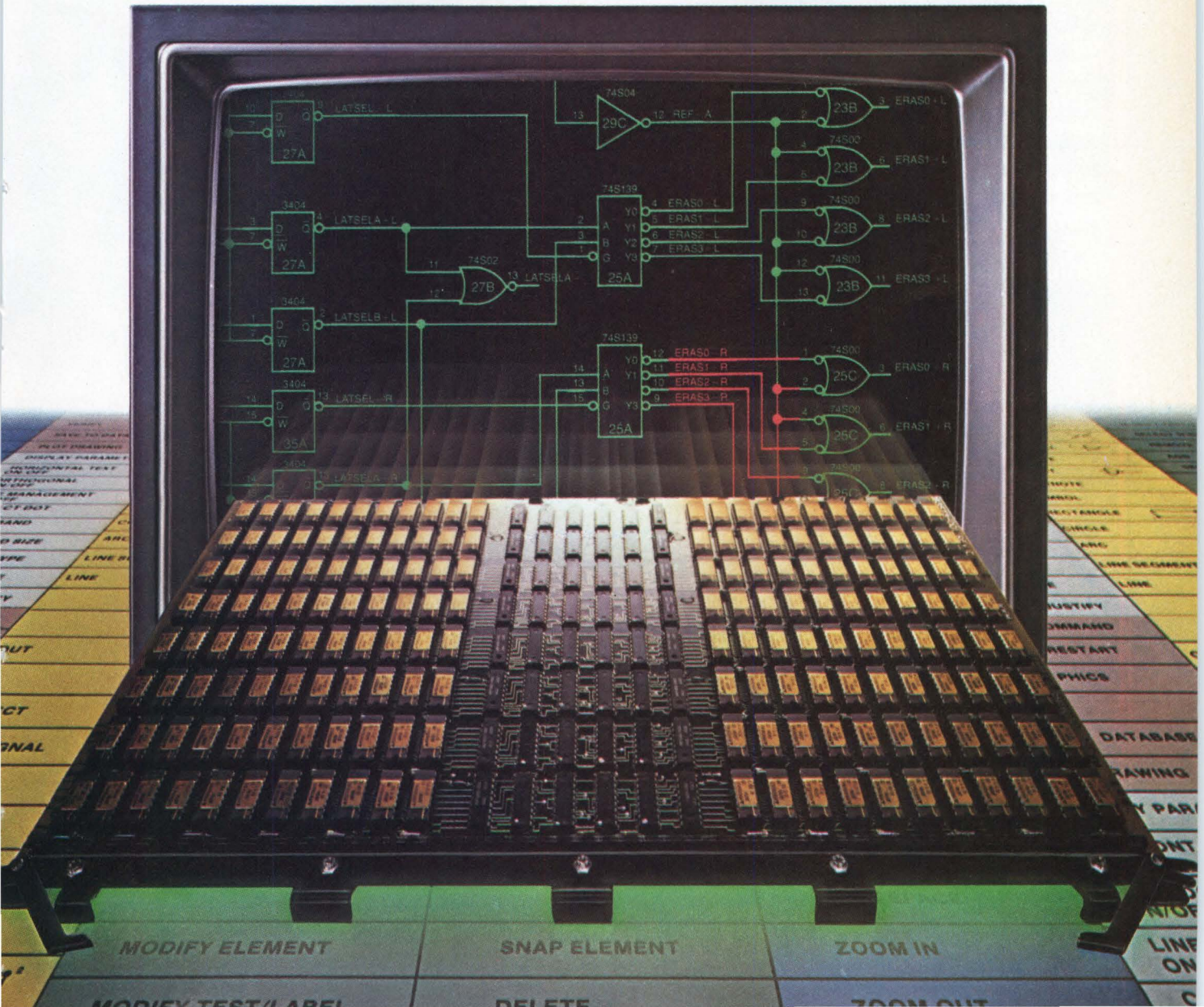

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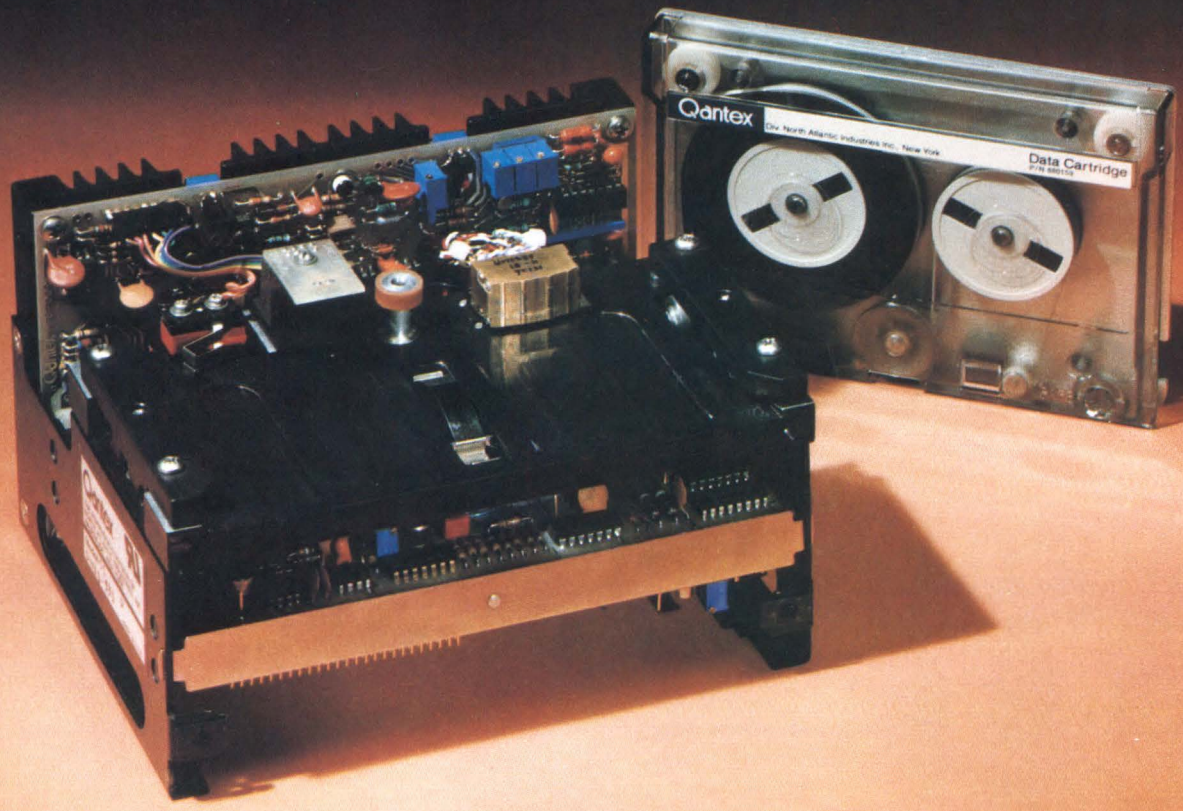

CIRCLE 97

CRAFTING A CUSTOM SORTED ACCESS MEMORY

Don't let the system software slog through sorting. Use Mead-Conway methods to design custom ICs for the task.

by Robert P. Adams

Sorting is an everpresent operation in digital logic computers. In fact, if a survey were taken on what computers spend most of their time doing, the answer would likely be sorting. Thus, the focal point of the company data processing department—the computer—spends most of its time rearranging data already stored in its memory.

Traditionally, the responsibility of directing the sorting operation has rested with the system software. Indeed, algorithms for various types of sorting are well known and often employed by programmers. Lately, however, advances in both very large scale integration (VLSI) technology and the methods used to construct custom integrated circuits (ICs) have wrested some of the sorting responsibility from the software. Now a hardware approach to specific sorting operations is possible, and better yet, practical.

By using Mead-Conway methods of circuit design, it is possible to create a sorted access memory (SAM) chip that executes sequential sorting algorithms.[1,2,3] This N-channel metal oxide semiconductor (NMOS) IC can offer powerful hardware based sorting functions to systems whose software execution burdens are already great. In addition to the time and speed advantages of hardware sorting, a SAM chip's fabrication provides an ideal exercise in the use of modern custom silicon design techniques.

Robert P. Adams is president of Adams Enterprises, 605 Hightree Rd, Santa Monica, CA 90402, where he starts high technology companies, designs custom ICs, and writes patents for others as a patent agent. Prior to this, he was founding president of Symbolics, Inc in Massachusetts. Mr Adams holds an MSEE from MIT and a BS in physics from Virginia Polytechnic Institute.

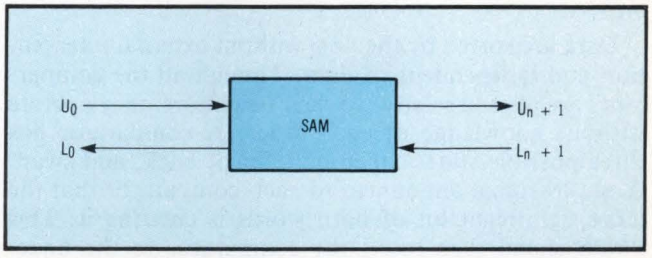

Fig 1 Black box depiction of SAM chip. Binary word entering at U_0 forces exit of smallest word stored at L_0.

Sorting with SAM

Word sequences are received, stored, and sorted by the SAM in a bit-serial manner. The smallest word is always available, and when the memory is full, the input of another word causes the smallest word to be output and lost from the SAM. Luckily, any number of SAMs can be interconnected to increase stored word capacity.

The SAM can be depicted as a black box (Fig 1). Rules governing its operation are straightforward. First, the SAM can contain n words. Second, a word entered at U_0 forces the exit of a word at L_0. The word exited is the smallest member of the class containing the SAM's

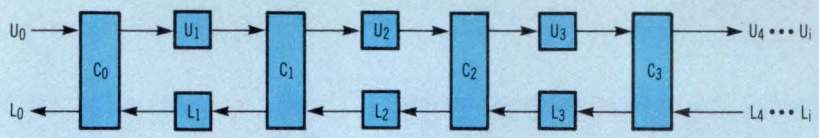

Fig 2 Simplified block diagram of SAM chip. By feeding a word composed of logic ones into C_0 at U_0, smallest word in the SAM is automatically output at L_0.

n words and the word entered. The SAM retains the rest of the class. Third, a word entered at L_{n+1} forces the exit of a word at U_{n+1}. The word exited in this case is the largest member of the class containing the SAM's n words and the word entered. The SAM retains the rest of the class. From these simple operational rules, a powerful sorting mechanism can be built.

A simplified version of the SAM is shown in Fig 2. Elements U and L are shift registers, and the Cs represent comparators. Length of U_i plus the length of L_i is n. Here, the SAM can hold three n-bit words. Key to SAM sorting lies in the fact that when words are stored in the SAM, they rearrange themselves so that the larger words are to the right of the smaller ones. Consequently, the smallest word is always at L_1. This smallest word can be accessed by feeding a word composed of all logic ones into C_0 at U_0. Since this word is no smaller than the word at L_1, it enters the SAM, forcing the smallest word in the SAM to exit (at L_0). Once the all ones word shifts through U_1, it is compared with the word shifting out of L_2. The word in L_2, which is the second smallest word originally contained in the SAM, now becomes the smallest word and shifts into L_1. If a second word consisting of all ones is shifted into C_0 at U_0, the second smallest word exits the SAM just as the smallest word did. Note that a sorted data set is output by the SAM, even though the SAM's contents may not yet be totally ordered.

Data are sorted by the SAM without external intervention and independent of data. Though all the comparators are phased relative to their neighbors, they operate without knowledge of each other. A comparator has three possible states called undefined, back, and swap. A BEGIN signal announces to each comparator that the most significant bit of both words is entering it. This BEGIN signal then resets the comparator to the undefined state, and the words at the comparator are compared bit by bit. If these bit pairs are the same, the comparator remains in the undefined state.

However, if the bit from the right word is greater than the bit from the left word, the comparator is changed to the back state and remains in this state until the next BEGIN signal. For example, if the bit from shift register L_2 is 1 and the bit from shift register U_1 is 0, comparator C_1 is changed to the back state. Similarly, if the bit from the upper word is less than the bit from the lower word, the comparator state is changed to the thru state and the comparator remains there until the next BEGIN signal. When a comparator is in either the undefined or the back state, the word remains on the same U_i, L_i pair. For example, when comparator C_i is in the back state, the output of L_{i+1} is the input of U_{i+1} and the output of U_i is the input of L_i. When the comparator is in the thru state, the output of L_{i+1} is the input of L_i and the output of U_i is the input of U_{i+1}.

On the basis of SAM operation described so far, certain conclusions can be drawn. None of the n words contained in the SAM will exit if a continuous stream of zeros enters at U_0 and a continuous stream of ones enters at L_{n+1}. In addition, a continuous stream of ones in both input ports will fill the SAM with ones in n-word time. Conversely, a continuous stream of zeros in both input ports will fill the SAM with zeros in n-word time. To enter $k < n$ words into the SAM, the lower k words must be preset to all zeros and the upper $n - k$ words to all ones. The k words can then be entered at U_0. Sorted k words can be removed immediately by entering k words of all ones at U_0.

The SAM in Fig 2 exhibits one problem. If inputs at U_0 are followed by inputs at L_{n+1} or vice versa, there must be a time delay of $n - 1$ words between the inputs. This delay is necessary to allow the words to migrate through the SAM. In many cases, this delay is unacceptable.

A solution to this problem is shown in Fig 3. Here, the comparators Z and the shift registers A are logically the same as those previously described. If a word composed of all ones is entered as A_0 into Z_0, it will be passed to A_1. The A_1 output enters comparator Z_1 and is then passed to A_2. This process continues for all A_i and Z_i inputs. Under these conditions, the SAM in Fig 3 is in effect the same as that of Fig 2, with the exception that L_{n+i} has been replaced by A_0. The important difference between these SAMs is that words entered at A_0 are available without delay for comparison at L_0, since no

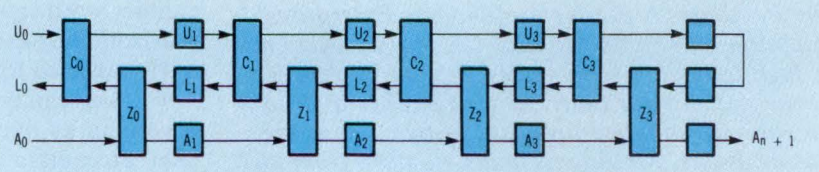

Fig 3 SAM configuration that eliminates propagation delay caused by word migration through chip. Words exited at L_0 are available immediately in sorted form.

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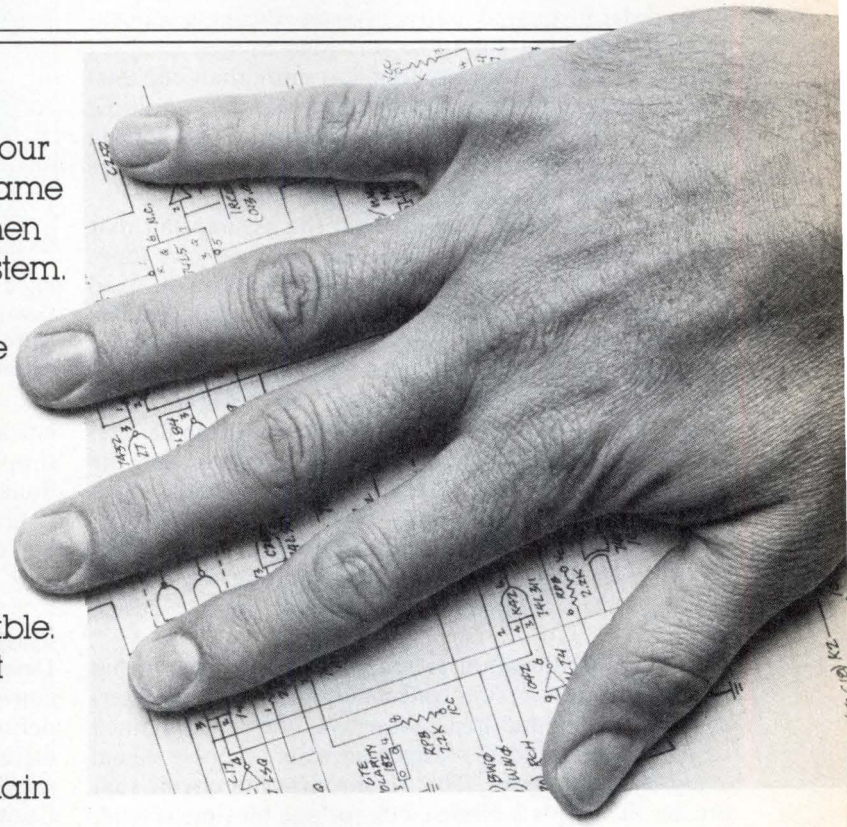

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migration time is required. Certainly, the SAM contents may not be totally ordered at any given time. However, since the access is only to the left, the smallest word present will always exit at L_0.

SAM features

The SAM design focused on two objectives: the sort capability had to be general enough to allow conventional business sorting, and the SAM had to be a building block in an order n-squared matrix inverter. Business applications demand the ability to sort long as well as short words. To satisfy this requirement, more than one SAM word is assigned to a business record, and these multiple words are sorted as if they were one word. This sorting ability is inherent to the SAM. The SAM's second use, as a matrix inverter, requires extra machinery.

SAM's word length is based on the assumption that words occur in a matrix and are each 64 bits long. Numerical data represented by such words can be fixed or floating point. The ultimate design goal requires inverting 1000 x 1000 matrices, creating a need for 10-bit indexes. Tag bits are also needed to keep track of operations during the inversion. An overall word length, including indexes and tag bits, results in 88 bits.

A counter 88 clock cycles long synchronizes the sorter. Every 88 cycles a BEGIN signal is generated. Two shift counters, 8 and 11 clock cycles long, make up the counter. The start of these two relatively prime counters is 88 cycles apart. Shift counters require no carries, making them relatively fast without heroic design efforts.

SAM synchronization is accomplished by an onchip synchronization circuit, and its 2-phase clock is generated offchip. In multiple SAM arrays, one SAM is defined as the master, and it receives an external SYNC signal every 88 clock cycles. The synchronization circuit suppresses the chip's 2-phase clock for one bit-time if SYNC is present and BEGIN is not. The SAM freezes for one bit-time and slips one bit-time relative to the external SYNC. Synchronization eventually occurs. Each SAM generates a SYNC signal delayed one bit-time, which is used as the SYNC for other SAMs.

All SAM logic was designed using Huffman's method.[4] Huffman's design methods are appropriate for MOS IC design for three reasons: pass transistor logic as well as unilateral logic is naturally represented; local asynchronous logic can be designed; and hazards are highlighted and can be easily eliminated. SAM logic is implemented as NOR logic, which is generally faster than NAND logic in NMOS. A more important design issue involves the rejection of programmable logic arrays (PLAs). On the surface, PLAs seem better by almost every measure—they are a program generated building block, making them robust and error free. Since they are canned, using them can save much design time. The PLAs' one flaw is their compactness, making it difficult to pass miscellaneous interconnects through them. PLAs complicate floor planning, and in SAM design the floor plan is the dominant issue.

The SAM chip layout shown in Fig 4 allows less replicated circuits to be at the bottom of the chip. The rest of the chip is composed of master layouts suitably repeated, reflected, rotated, and/or displaced. The chip has a 6-word capacity. A larger capacity chip's layout simply requires changing a few coefficients—no additional design is needed. Also, as the IC technology improves, smaller geometry can be used by changing one design parameter.

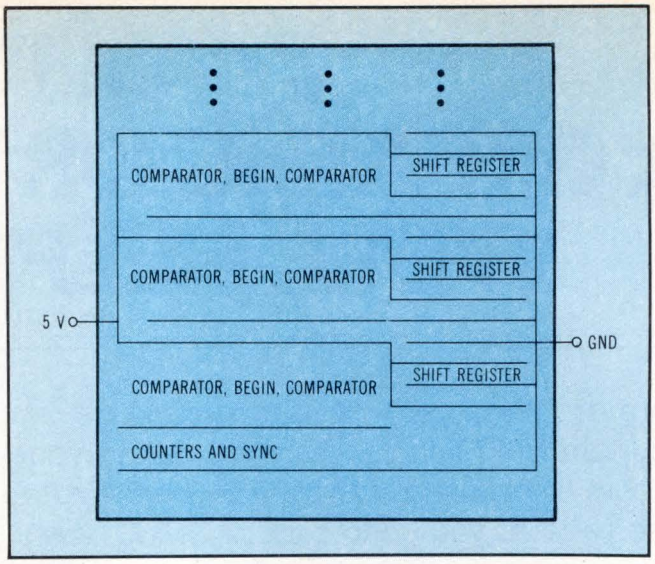

Fig 4 SAM chip layout and power and ground floor plan. Less replicated circuits for control and timing are located at bottom. Highly replicated circuits are rotated, reflected, and repeated to aid interconnects.

Designing with Mead-Conway

Design methods used in the SAM are similar to those of conventional logic design. Separable logical boxes are defined, then designed. There are some important differences, however, such as the parameters being optimized and the most appropriate design methods. Mead-Conway methods[5] used in this SAM's design are applicable to other IC designs as well. Mead-Conway's tenets are straightforward. First, the attitude is adopted that "wires are expensive—transistors are free." The chip is mostly made up of interconnects. Power and grounds should be interdigitated and the circuits organized so that the clock lines are regular and mostly perpendicular to the power and ground. If the floor plan is not defined early, an inordinate amount of silicon is wasted on interconnects and timing is compromised. The black box designs should be simulated before investing much time in detailed layout. Excellent logic simulators are available,[6] and timing simulators are maturing quickly. Also, simulation should be done locally, not globally.

A Mead-Conway method is to build a personal elements library. Parameterized instances of the elements can then be called and connected with great efficiency. These elements' integrity is assured at the lowest possible level. In addition, design time is invested to develop regular and general algorithms. Simple shapes and signal flow save space and design time. Simulation is simplified, and design bugs are easier to find. Another Mead-Conway approach is to lay out the IC on a computer and define distances relatively between elements. Often, elements must be moved about to avoid design rule errors or to improve the design. If a revision is

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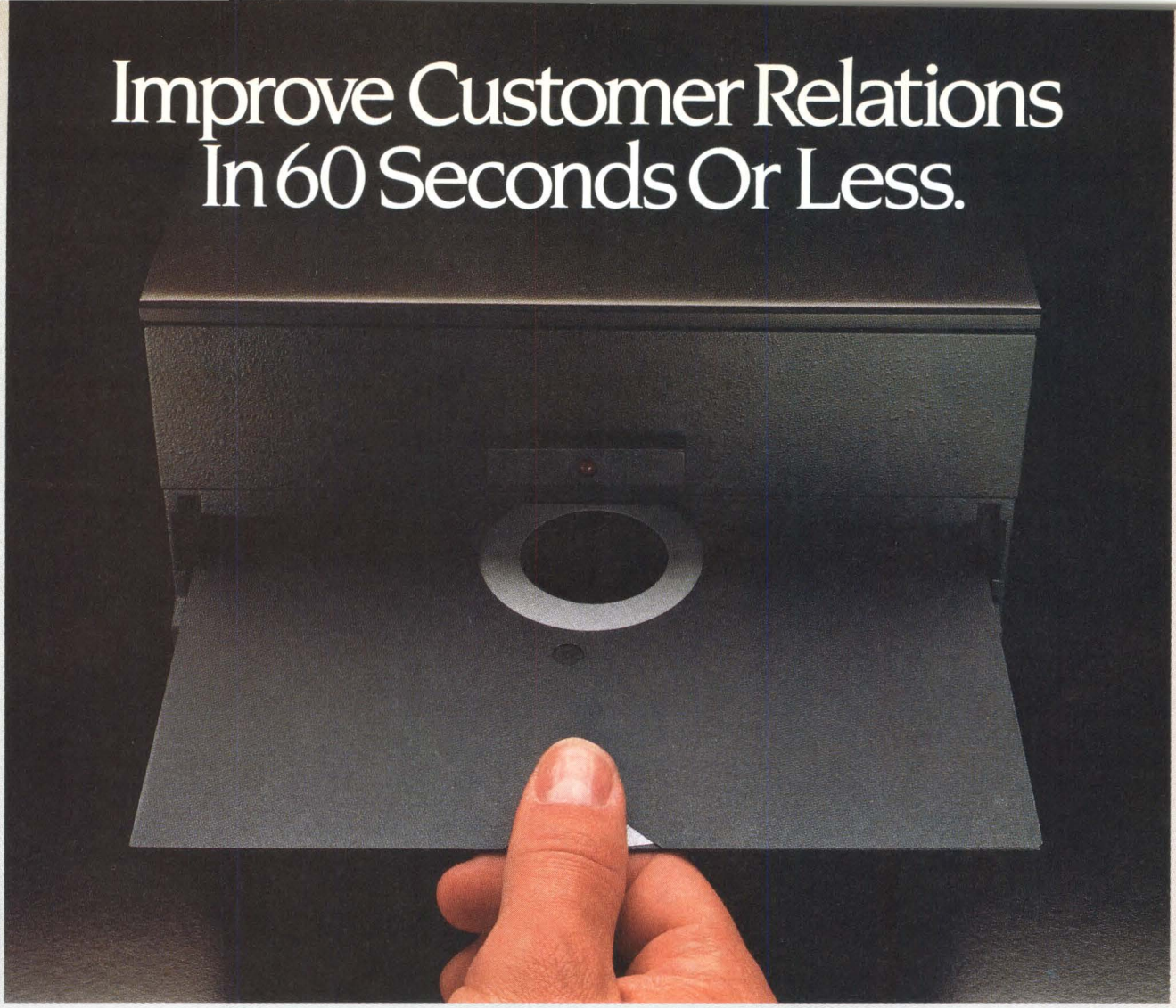

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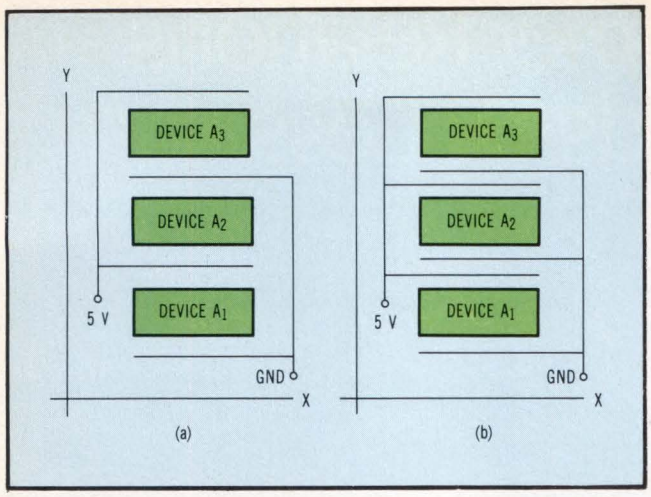

Fig 5 Power and ground routing on SAM shown in (a) is suitable for shift registers and replicated logic. Routing in (b) benefits comparator and BEGIN logic where many interconnections are required.

needed, changes can be made locally in the circuit. A final Mead-Conway technique is to check for design rule errors, both locally and globally.[6]

The Mead-Conway method is now available to the real world of logic design. Custom IC design no longer requires Silicon Valley gnomes. Sensitivity to the art of programming is central to Mead-Conway, however, since symbolic reasoning and algorithm use are both important in the design process. The entire process—architecture, logic design, and chip layout—is performed by one person with extensive help from design aids such as computers and programs. In addition, typing ability is a must—the hunt and peck method is simply inadequate for Mead-Conway purposes.

SAM architecture is a natural for Mead-Conway design. The sequential sorting algorithm provides a repetitive structure requiring only two designs—the comparator and the shift register.[1,2,3] These building blocks can be designed, then suitably located on the chip.

However, the comparators' BEGIN pulses are delayed from one comparator to the next, and the function of inserting tags in the words is conceptually complex. But with some thought, these additions are algorithmically simple, thus easily implemented. The majority of the chip is composed of comparators and shift registers. Timing and synchronization blocks are not replicated, but this is not unusual. A highly replicated part and one local control part are desirable. The local control part can be tucked into a corner, leaving the rest of the chip as a continuous, unobstructed area.

The chip layout, as shown in Fig 4, is organized so that the unique circuits are at the bottom of the chip. Local controls—counters and synchronization (sync)—are on one end. The comparator, BEGIN logic, and shift register combinations are local and can be repeated in the vertical direction to mechanize as many words as desired. Space is allocated for interconnects as needed. Interconnects in the comparator, BEGIN, and shift register blocks are embedded in the block. As previously mentioned, the comparator could be mechanized using a PLA, but the canned PLAs available are so dense that interconnects must be routed around them. For the SAM, a bus structure is better.

Routing power and ground to the replicated logic is efficient, as shown in Fig 5(a). Device A_2 is reflected about the X axis, making it upside down. Such a reflection is made with a single statement in the design program. However, in the BEGIN logic, there are many communication lines in the vertical direction, and the clean abutment of these signals for the X-reflected logic is untenable. So, power and ground lines to the comparator BEGIN logic are routed, as shown in Fig 5(b). On the other hand, the shift register cell is a serpentine structure, weaving back and forth until it has the proper logical length. The power and ground structure in Fig 5(a) is appropriate for the shift register.

Logic design and construction

The building blocks—comparator, BEGIN, counters, and sync—are structurally similar to each other. To illustrate Mead-Conway design, a logically simple block—the count-by-eight counter—must be considered in detail.

The shift counter is a 4-bit shift register as shown in Fig 6(a). Fig 6(b) shows a suitable 4-bit sequence for a count-by-eight shift counter. The Karnaugh map of this sequence, shown in Fig 6(c), generates the design in Fig 6(d). A logic term $b \sim c$ gives one output every count-by-eight sequence, and $b \sim c$ also breaks up the secondary count-by-eight sequence through the X locations of Fig 6(d). Inclusion of this term gives the final

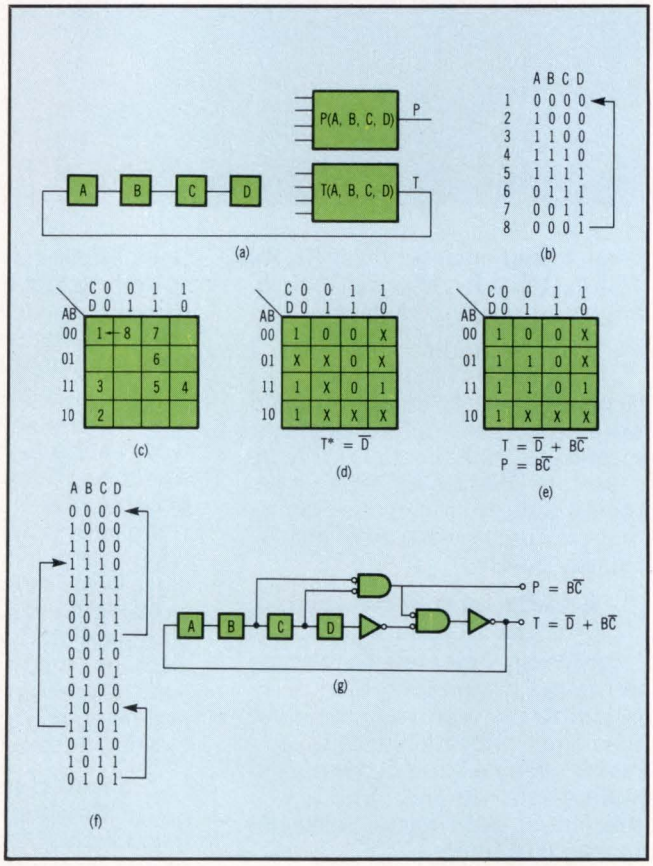

Fig 6 Design sequence used to generate a count-by-eight shift counter. Diagram (a) requires a 4-bit sequence shown in (b). Karnaugh map (c) yields logic table (d). Additional logic term $b\bar{c}$ is required for output once every count sequence. Final logic diagram (e) incorporates all bit sequences shown in (f). Final circuit diagram (g) results.

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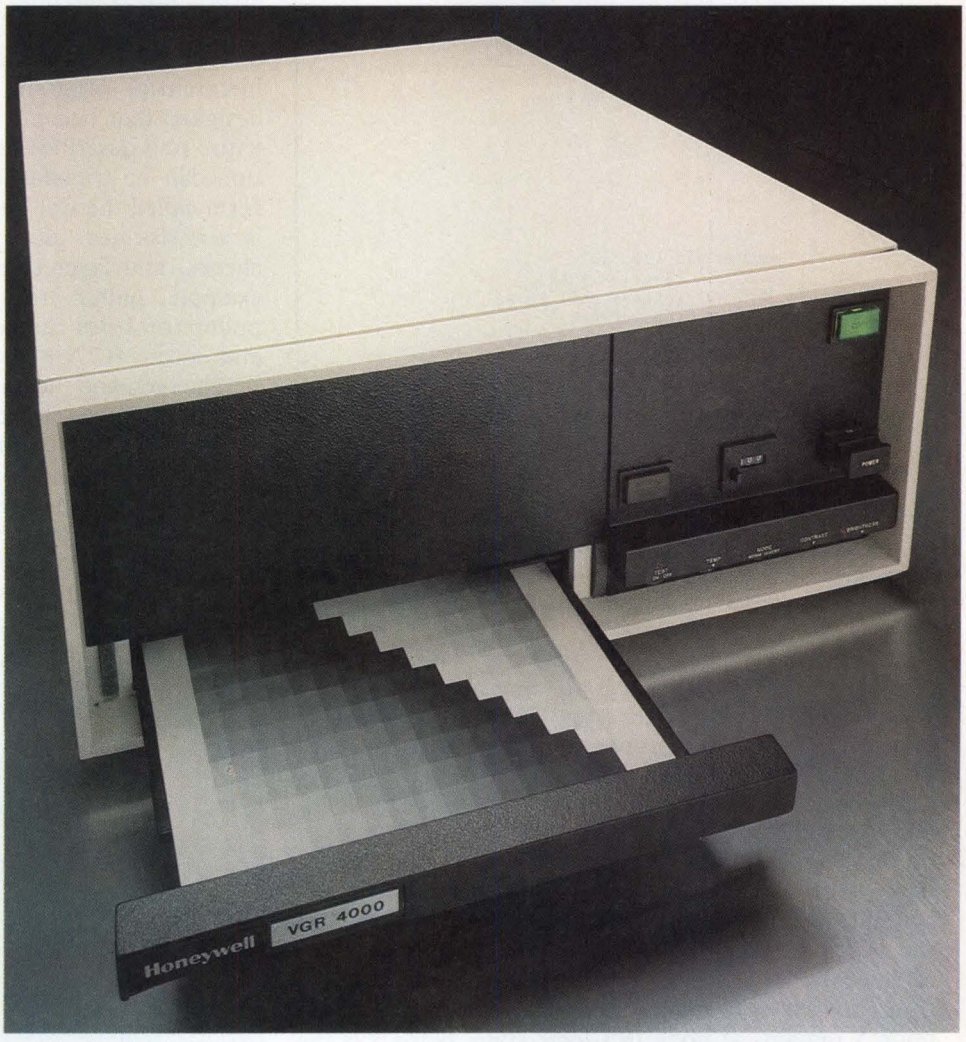

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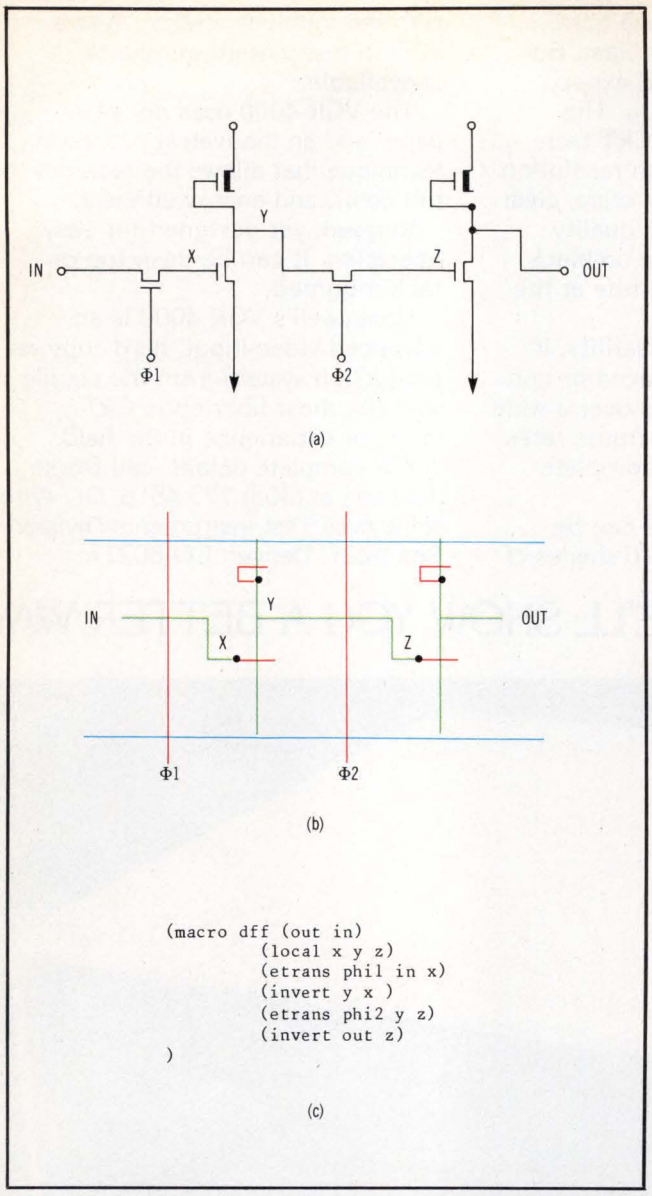

Fig 7 Basic shift cell design sequence. Schematic (a) can be represented by stick diagram (b). Metal (blue), poly (red), and diffusion (green) crossing data can be directly input to a computer via textual schematic (c).

design of Fig 6(e). Sequences for any bit combination are shown in Fig 6(f). After a few clock pulses, the shift counter locks into the proper count-by-eight sequence. The final design is shown in Fig 6(g).

The basic shift cell is a delay flipflop [see Fig 7(a)]. Φ1 and Φ2 are disjoint clock pulses—Φ1 is true, followed by Φ2 true, followed by Φ1 true, etc; Φ1 and Φ2 are never true at the same time. In this 2-phase clock system, the Φ1 transistor conducts when Φ1 is true, and the signal IN is transmitted to node X. This signal is retained by the gate to the source capacitance of the transistor whose drain is at node Y. When Φ1 goes false, node X remains at node IN's logic state. Node Y is the logical inverse of node X. When Φ2 goes true, its pass transistor conducts and node Y's logic state is stored on the gate to source capacitance of the transistor whose drain is node OUT. OUT is the logical inverse of Z. Thus, after one 2-phase clock pair, the logic state of IN is shifted to OUT.

A stick diagram of the delay flipflop is shown in Fig 7(b). Blue represents metal, red polysilicon (poly), and green diffusion. Black dots are connections, and pullup depletion node transistors are shown symbolically. Poly crossing diffusion forms an enhancement mode transistor; metal crossing poly or diffusion has no effect.

A textual schematic of the delay flipflop, in computer usable form, is shown in Fig 7(c). Various optional parameters provide the computer with information to simulate static and dynamic operation. MACRO declares that a schematic named DFF follows. DFF can be called as an element, as in the shift counter's mechanization. LOCAL declares local variables. ETRANS declares an enhancement mode transistor with gate, and interchangeable source and drain. INVERT declares a 2-transistor inverter with output and input.

The textual schematic associated with the count-by-eight counter stick diagram is shown in Fig 8(a) and (b). Note that the macroinstruction DFF for the delay flipflop is used. Before entering the stick diagram information into the computer, the textual schematic simulates the shift counter [see Fig 8(b)]. If there are logical errors, this is the time to find them. The count-by-eight counter stick diagram is entered into the computer using a VLSI Technology design program. Called VIP, this hierarchical program allows building blocks to be designed that become members of a larger block. The entire IC is described using VIP, and this textual description can be transformed into a common interchange form called the Cal Tech intermediate form. This form is transformed into plots, simulations, design rule checks, and layer data for IC production masks. For example, pullup transistors are used repeatedly. The pullup transistor can be designed once; then VIP can call and locate it. VIP programs can include modifiable parameters, and the pullup transistor program has parameters to dimension the channel. When a pullup instance is called, parameter values are given and the pullup dimensions are appropriately altered.

When the VIP program is used to lay out a count-by-eight shift counter, the power and ground rails and the pullups are placed through the use of a direct read after write (DRAW) statement in a software iterative loop. The

```
(macro dff (out in)
        (local x y z)
        (etrans phi1 in x)
        (invert y x)
        (etrans phi2 y z)
        (invert out z)
)
(dff a t)
(dff b a)
(dff c b)
(dff d c)
(invert ~b b)
(invert ~d d)
(nor p ~b c)
(nor ~t ~d p)
(invert t ~t)
```

(a)

```
abcd=0110
abcd=1011
abcd=0101
abcd=1010
abcd=1101
abcd=1110
abcd=1111
abcd=0111
abcd=0011
abcd=0001
abcd=0000
abcd=1000
abcd=1100
abcd=1110
abcd=0010
abcd=1001
abcd=0100
abcd=1010
abcd=1101
abcd=1110
abcd=1111
abcd=0111
abcd=0011
abcd=0001
abcd=0000
abcd=1000
abcd=1100
abcd=1110
```

(b)

Fig 8 Count-by-eight shift counter textual schematic (a) and resulting logic simulation (b). Logic errors can be detected early by regularly using simulation functions.

loop uses vector elements containing the separation of the pullups with respect to their neighbors. Once finished, the layout is submitted to a design rule checker program. A design rule checker raster scans the layout to verify compliance with Mead-Conway specifications, such as the proximity of two diffusion wires. When the layout passes the design rule check, the VIP file is ready for simulation.

In the second simulation (the first one used the designer generated textual schematic), the computer raster scans files generated from the VIP representation of the count-by-eight shift counter, then generates its own textual schematic. This computer generated textual schematic can be probed using the simulation program to verify that the layout actually mechanizes the desired logic. The computer is an honest critic of the layout—the same layout that is used to automatically generate the IC production masks.

System layout

The major building blocks must be located on the chip to conform to the floor plan layout. X and Y coordinates are assigned for the building block locations, the interconnects, and the pads. These building blocks are located according to the floor plan using the coordinate symbols, along with suitable displacements, rotations, and coordinate reflection. Software iterative loops can be used to successively place identical structures on the chip. This hierarchical style of relative coordinates works at all design levels.

System layout is not a trivial job—a clumsy floor plan can make it a nightmare. One truism states that "the final interconnects take more design time than the real problem." The interconnects, floor plan, and butting design are key areas, and early planning will minimize problems. When the layout is completed, a design rule check must be run on the entire chip. Though this takes a great amount of computer time, it is necessary. If any change is made, even one as trivial as the company logo, the design rule check must be rerun. At present software sophistication levels, an overall simulation is impractical. Presumably, less computing intensive simulations of both logic and circuit timing will soon be developed. While overall simulation is most desirable, it is not yet practical.

A sorted access memory chip's design using Mead-Conway techniques is no simple matter. It is, however, within most system designers' reach, provided they have the necessary design tools. Courses in Mead-Conway design—such as those given by VLSI Technology of San Jose, Calif—are becoming more frequent in both academic and industrial settings. The full-custom silicon era is just beginning, and engineers who want to be part of tomorrow's design scene should become familiar with custom design techniques.

The SAM chip is an excellent example of system design using custom ICs. It finds use in any general business environment where sorting is required, as well as in systems that solve large sets of linear equations. By accepting the challenge of custom IC design, engineers can implement, prototype, and produce VLSI chips that are more cost effective and functional—even in small quantities—than other printed circuit board or silicon alternatives.

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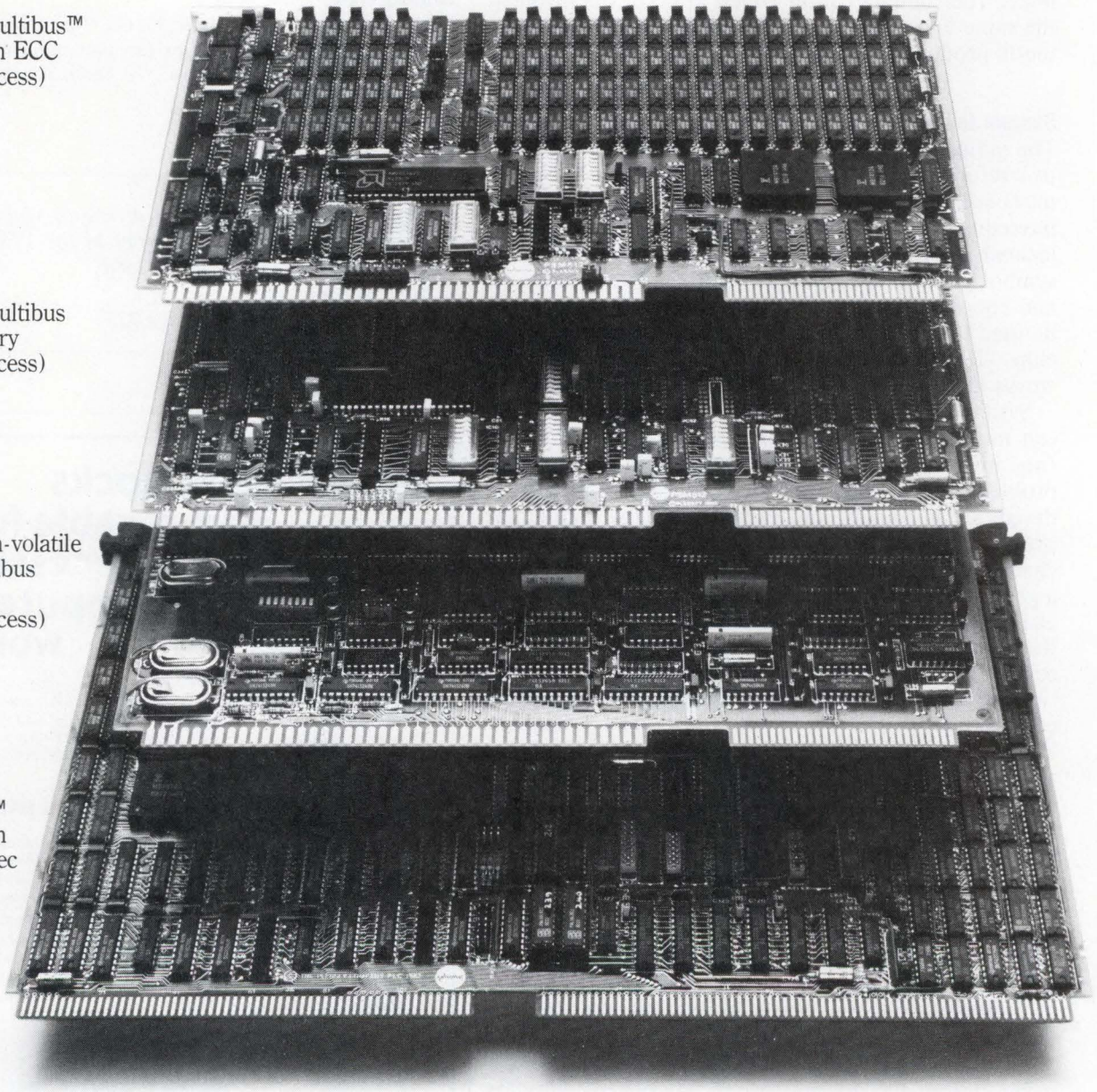

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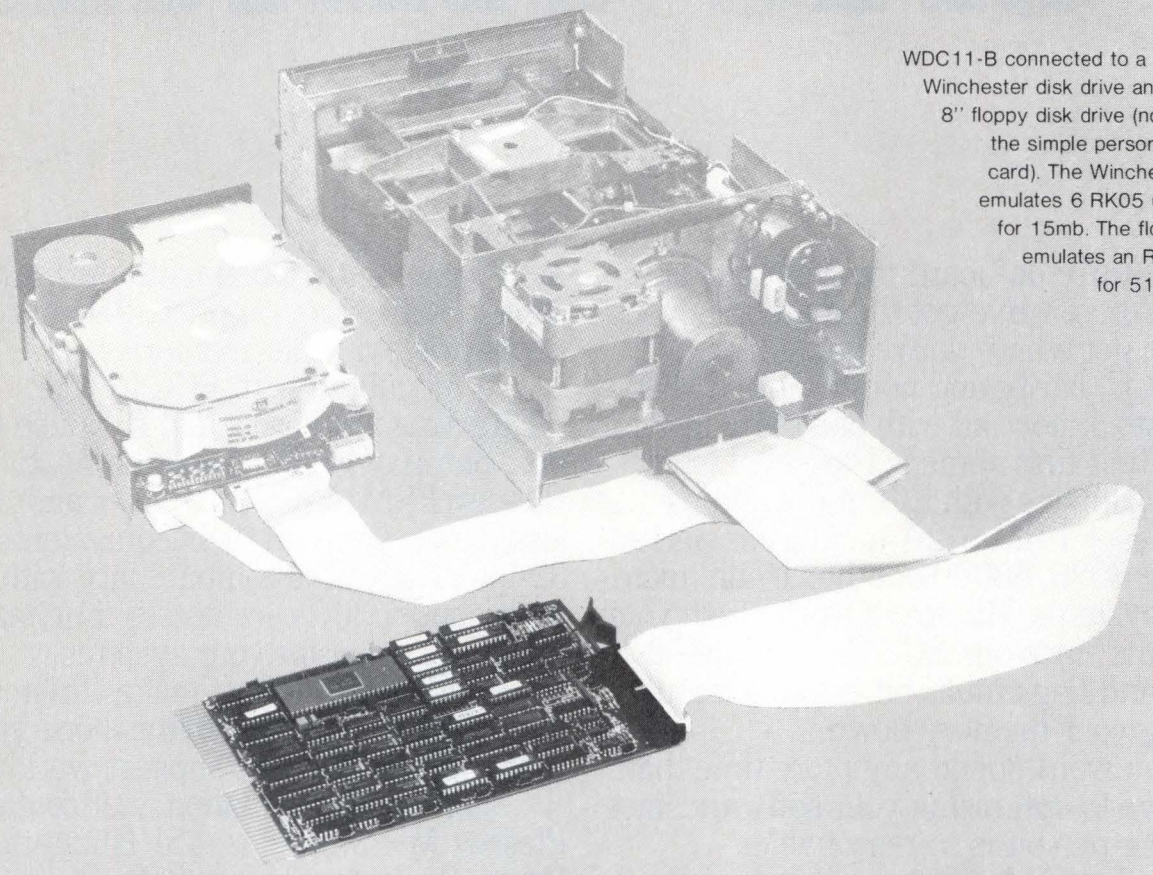

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BRINGING SEMICUSTOM IC DESIGN IN-HOUSE

As more semicustom ICs are designed in-house, cost and time have become influential design constraints. Fully automated CAD meets IC specs and cuts cost and time consumed.

by William M. vanCleemput

Until recently, the integrated circuit industry was preoccupied with the design and manufacture of high volume circuits such as memories and microprocessors. Specialized circuits were designed only for specific customers with guaranteed high production volume requirements. Most high volume custom integrated circuit houses absorbed the design cost as an overhead function.

However, when production volume drops below 50 thousand parts per year, the design cost can no longer be considered overhead. Either the design is charged separately or it must be provided by the customer. Traditional IC design cost becomes even more significant as production volume drops below 10 thousand parts per year. An IC design that minimizes chip area to increase yield and reduce manufacturing cost also makes the wafer fabrication expense less significant than the design cost. Consequently, for low production volumes, semicustom circuit design approaches that use gate arrays or standard cells become essential to cut design overhead.

Gate arrays, with common diffusion steps, can be applied to large volumes of wafers. Interconnection of the design and final metallization customize the chip, require from one to three photomasks, and are much less expensive than the rest of the fabrication cycle. Gate arrays do not merely lower fabrication cost for small volumes; they also reduce the number of fabrication steps to allow faster turnaround. With a standard cells approach, logic functions such as gates, flipflops, and multiplexers are designed, fully tested, and characterized in advance. An automated layout system can then produce a complete physical design. Standard cells better utilize the silicon chip area and permit any standard function block (eg, random access or read only memories, programmable logic array, or arithmetic logic unit) to be included in the design. Currently, electronics systems firms tend to consider gate arrays and standard cells as two parallel paths toward custom IC design.

Fully manual layout of an IC is in most cases totally uneconomical. For instance, the design of a commercially available 16-bit microprocessor required 15 man-years of design effort, of which layout related tasks comprised 10 man-years. In addition, several calendar years elapsed before an operational prototype was obtained. Conversely, a controller designed with N-channel metal oxide semiconductor technology and standard cells, with roughly the same circuit complexity as the 16-bit microprocessor (3000 vs 5000 gates), required six man-months, of which about one week was devoted to

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layout, and operation according to specification was achieved during the first test.

Design process and work hierarchies

Developments in semiconductor technology that have increased the number of logic gates put on a single chip have advanced farther than the power of human concentration. A block diagram or schematic with 10 to 50 functional blocks is usually understandable by the engineer, but a schematic with 1k logic gates, and with no logic block functionally designated, is most likely to be completely incomprehensible. Therefore, a task hierarchy is often established to complete a design. The digital logic design phase is most frequently performed in a "top-down" order, while the physical layout phase is executed from the "bottom up."

It is difficult to precisely analyze the hardware design process since it is largely dependent on the individual designer and on the specific design problem to be solved. Starting from sometimes vague and incomplete specifications, the designer goes through an iterative series of successive transformations until the system can be built within a given technology—or until it is clear that specifications such as the intended functional behavior, performance goals, or design constraints are not feasible. The functional behavior specification can be vague and incomplete, or it can be too precise. Performance goals can vary between unimportant and critical, and design constraints can often drastically reduce the size and available solution set to meet the specifications. The designer must then realign the task hierarchy to identify an alternate design, define a figure of merit, evaluate/order each design alternative according to the figure, choose a design alternative, and verify that the design specifications are met.

However, validating the functional specifications of a given system becomes more complex with increasing system size. Simulating the system gives only partial validation unless an exhaustive simulation exercises all possible combinations of inputs and internal system states. Without such care, design correctness is never proven; rather, only the absence of errors for cases considered is validated. In addition, the limits of human intellect make it impossible, in all but the most trivial cases, to simultaneously conceive and finalize the design concept. Instead, the problem is partitioned into more to less complex subproblems. This process is repeated until solutions to all subproblems are found, or until accepted procedures are applied to solve these subproblems. The converse bottom-up approach successively composes known building blocks into higher level functional blocks. In practice, both approaches are combined as a means to the completed circuit. Top-down design is often used during the initial design stages when the system is divided into functional units and the work distributed among a team of designers. Creating from the bottom up is used more frequently later during the detailed design phase.

These abstract levels of manipulating an IC design from creation to solution leads to a second task hierarchy—the physical work of chip layout. The architectural level concerns the overall system structure comprising components such as processors, memories, I/O devices, and their interconnections. Each component is analyzed according to quantitative attributes, such as the size, word length, and access time of memory. In addition to cost and functional correctness, the architectural level also involves the consideration of reliability, fault tolerance, and other system properties. Operational research, queuing theory, and simulation determine the global flow of information between various components and are used to evaluate system performance. Here the objective is to find a configuration that best satisfies the specifications at minimal cost. In some instances, system simulation is necessary to obtain a clear picture of global behavior.

The register-transfer design level typically realizes functional specifications through a sequence of information transfers between register sets. Perceiving a digital system as a large finite-state machine, the purpose of the register-transfer level design is to establish the various states, as well as the particular actions to be taken, when the system is in a given state. Simulating the operation of the entire design or subsystem often provides a better insight into the operation of the future completed system. The simulation process may also reveal design inconsistencies and errors that might otherwise go undetected.

Mapping the micro-operations and the control structure defined in the previous step into physical hardware is accomplished during logic design. This procedural level requires detailed knowledge of the technology in which the design is to be implemented, with the result perhaps being a set of logic diagrams or Boolean equations, and primitives available in the actual technology. At the physical level, the designer is concerned with partitioning the system into board-level and custom circuits, along with components and interconnection routing. This design level requires maintaining large amounts of information. In this area, design automation has been traditionally used first and most extensively.

Design tools for customizing ICs

The design processes of a relatively simple 400-gate single metal layer complementary metal oxide semiconductor (CMOS) gate array are illustrated in Fig 1. Computer aided design (CAD) limited to digitizing the original layout on an interactive graphics turnkey system is compared to extensive use of CAD tools. With CAD used for digitizing only, the system generates the control tape for a pattern-generation machine. In this manual design procedure, the use of CAD for digitizing the layout can save a substantial amount of labor once engineering changes have to be processed. A typical engineering change requires less than one day of editing on the CAD graphics turnkey system, as compared to several man-days required by manual design. The most time-consuming task, totaling 20 days, is the layout/digitize/verify cycle. As circuits become larger, the amount of time required to perform the layout task increases exponentially. The Figure also illustrates that the layout task is reduced to three days through automatic component placement, automatic interconnection routing, and interactive layout editing with online connectivity and design-rule checking. These CAD tools are available commercially or are often developed for in-house use.

In the manual design approach, logic schematics are drawn and a prototype is built out of discrete components

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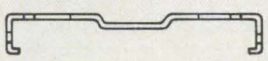

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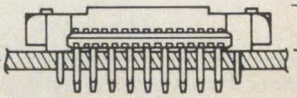

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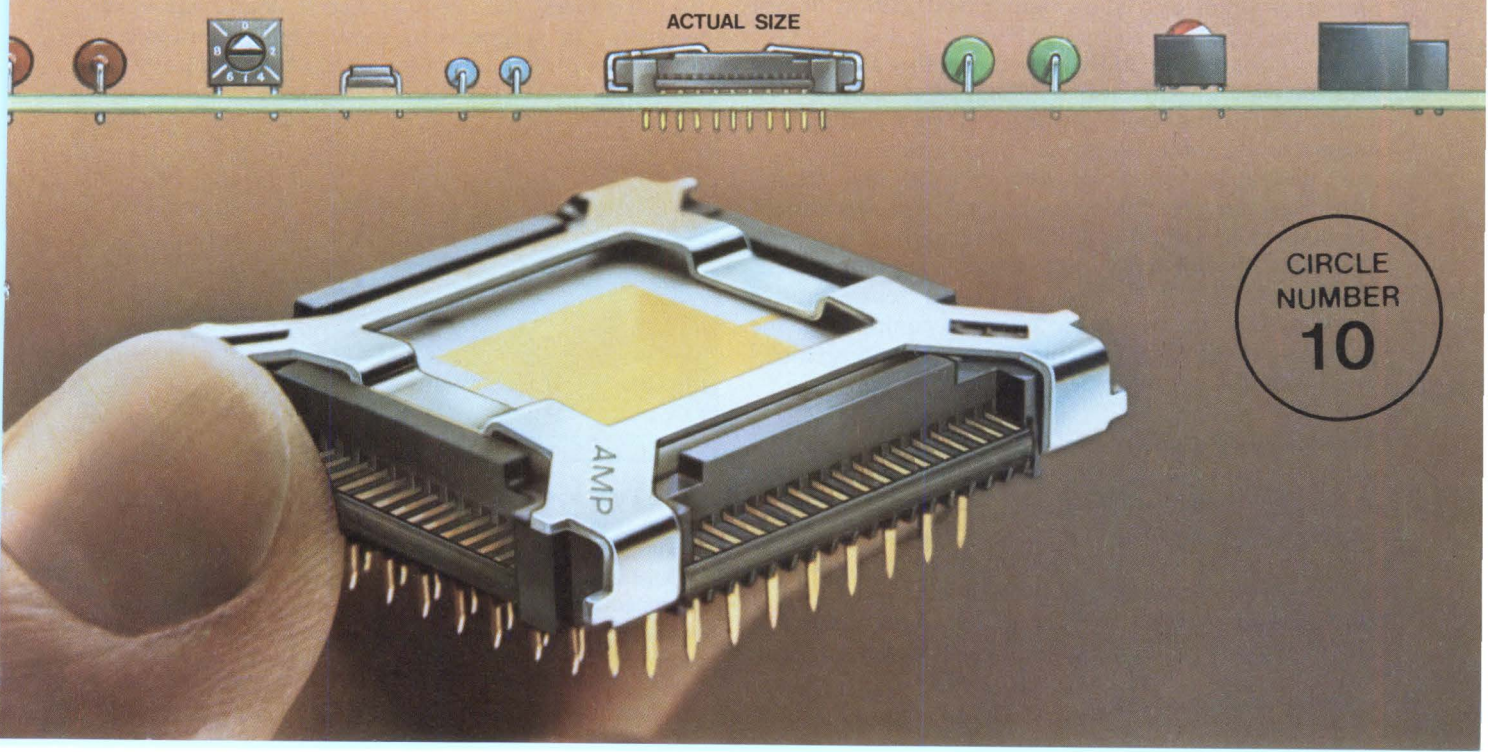

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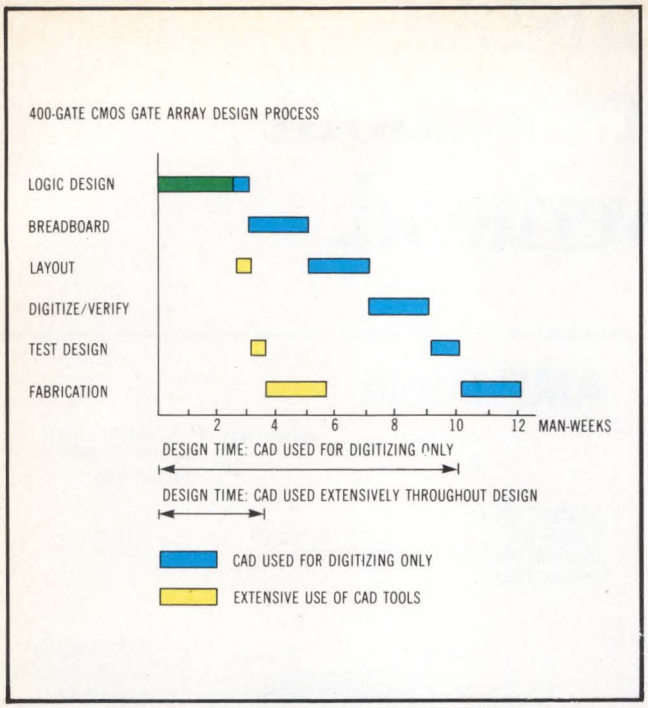


Fig 1 Limited vs extensive CAD use. Time segments used to design semicustom ICs are significantly shortened when CAD is employed for automatic placement/routing and interactive layout editing with online connectivity and design rule checking, as compared to time consumed by CAD used only to digitize specifications.

and debugged. Manual design is relatively straightforward for a 400-gate array, but it becomes very cumbersome for a 10k-gate system that may have five custom ICs. Furthermore, the breadboard cannot be used for accurate performance predictions since it is impractical to model the parasitic elements of an integrated circuit. However, an interactive schematic entry can result in an accurate version of the design. Clean documentation is also easily generated once the design is complete. Rather than building a breadboard, the designer can use a simulation program to model a parasitic effect such as capacitive loading. A fault simulation program also allows quick verification of test sequences.

Logic design is the most time-consuming task during both process approaches, totaling three man-weeks, since synthesizing logic elements is very difficult to automate. In some cases, as in programmable logic array design, it is possible to derive a full logic design from machine-readable functional specifications. Although this method is still in an experimental stage, tremendous productivity improvements are anticipated, as graphed in Fig 2. Table 1 lists a representative sampling of available CAD software to complement the various levels of design, including system and architectural level design, and logic and layout design.

Economic considerations

Setting up an in-house CAD facility for designing custom ICs has several significant benefits, including the protection of proprietary information, control over the design process, elimination of communication and queuing bottlenecks, and cost savings over manual design. Capital expenditures required for a medium-sized standard-cell or gate-array design system in 1982 ranged from $650,000 to $700,000. An average user (ie, one who works 40 hours a week) can design roughly 90 gate arrays of 1k gates each in a single year, for a total of 90k equivalent gates. For standard-cell designs, productivity is estimated at 50 custom circuit designs of an average of 5k gates each for a total of 250k gates per year. Such a design system usually supports four design stations for gate arrays and eight design stations for standard-cell designs. Two additional support personnel are required for full support of the hardware and software system.

Table 2 lists the annual cost of an IC design center, both in absolute numbers and on a cost per gate basis. It is assumed that the system is fully depreciated over a 4-year period. Yearly hardware maintenance is projected at 10% of the total hardware cost, and yearly software maintenance/support is given as 12% of the total software cost. A yearly employment cost of $60,000 per programmer/designer is used. Working at capacity, the annual cost of such a design center is approximately $350,000 for gate-array ICs and $370,000 for standard-cell ICs. However, on a design cost per gate basis, standard-cell designs are significantly less expensive than gate arrays. This difference nevertheless, is partially offset by the increased cost of manufacturing prototypes.

Comparing the time and cost savings of a full CAD approach to the digitize only method reveals even more significant variances. Most evident is that savings escalate as circuit complexity increases. This relationship results directly from the automatic features of advanced CAD software, which minimizes design errors and iterations that can occur within complex designs. Quantitatively, a CAD approach can save over 150 man-days during the design of a 5k-gate standard-cell IC, and over 45 man-days in the design of a 1k-gate array. These CAD time savings can be recalculated into dollar savings of $45,900 per 5k-gate IC and $14,000 per 1k-gate IC. Certainly such dollar and time savings are important to the designer and manufacturer, yet CAD of custom ICs has been limited to digitizing and editing purely graphic material on turnkey graphics systems. Although increasing the productivity of drafters, these CAD tools did not address the needs of circuit, logic, and system designers. In response to these needs, commercially available tools for computer aided engineering (CAE) of

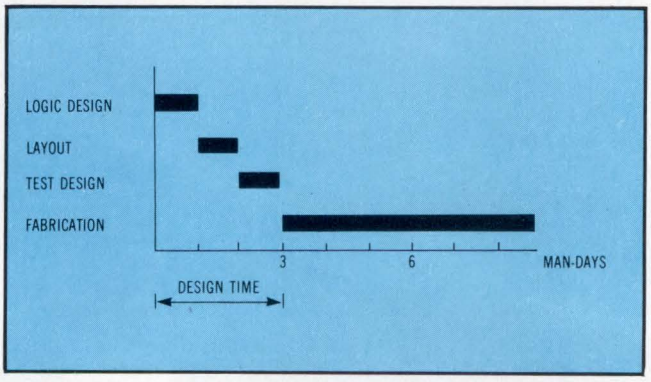
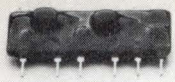
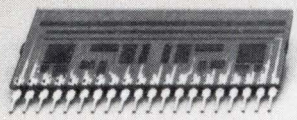


Fig 2 Fully automated CAD. A fully automated design derived from machine readable functional specifications is shown as the least time-consuming method of designing semicustom ICs. Although the approach remains in experimental stages, CAE tools and complementary software are already offsetting many previous problems.

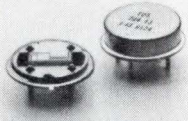


Automotive
(Conformal Coated)

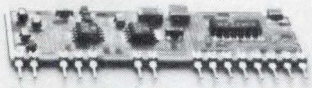
Porcelain Steel
(Pot Element)



Porcelain Steel
(Resistor Network)

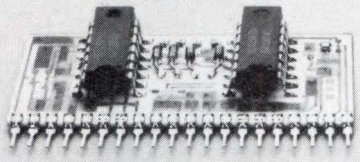


Thin Film SAW Devices (Filters)



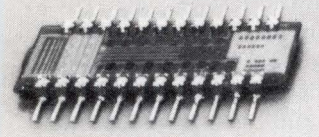
Telecommunications Interface
(Using Small Outline
Components)

Commercial Circuit
(Using Surface Mount
Components)



Telecommunications
(With PWB Components)

Precision Trimmable Resistor
(Ceramic DIP)



Porcelain Steel
(Multi-Layer)

High Speed Analog (Chip/Wire)

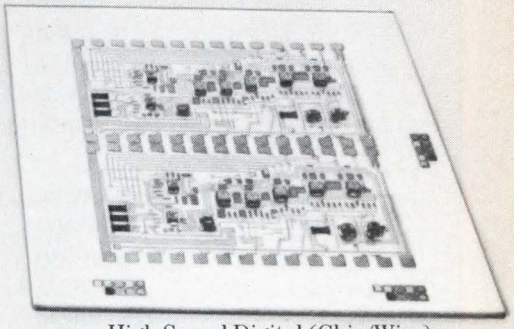


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TABLE 1

CAD Software Tools

Function	Name	Source
System/Register-Level Design		
Hardware description language	ISPS	Carnegie-Mellon University
	DDL	University of Wisconsin
	ADLIB	Stanford University
Functional simulation	TEGAS6	ComSat General Integrated System
	HELIX	Silvar-Lisco
Testability prediction	SCOAP	Sandia Laboratories
Partitioning	HIPAR	Silvar-Lisco
Hierarchical schematic entry	SDS	Silvar-Lisco
	SCALD	Lawrence Livermore Laboratories
	LOGICIAN	Daisy Systems
Logic Design		
Logic simulation	TEGAS6	ComSat General Integrated System
	SALOGS	Sandia Laboratories
	LOGCAP	Phoenix Data Systems
	LOGIS	Control Data Corp
	ILOGS	SimuTec
	HELIX	Silvar-Lisco
	BIMOS	Silvar-Lisco
Fault simulation	TEGAS	ComSat General Integrated System
	LASAR	Teradyne Inc
	FAIRLOGS	Fairchild Corp
Layout Design		
Gate-array place/route	MERLYN	V-R Information Systems Inc
	GARDS	Silvar-Lisco
	APAR	RCA/DoD
Standard cell	PR2D	RCA/DoD
	MP2D	RCA/DoD
	CALMOS	Silvar-Lisco
	CAL-MP	Silvar-Lisco
	GAELIC	Compeda Ltd
	ZyP	ZyMOS Corp
Design-rule checking	DRC/ERC	NCA Corp
	MASKAP	Phoenix Data Systems
Interactive artwork editing	860	Applicon Computer Inc
	GDS-2	Calma Co
	CADDS-2	Computervision Corp

TABLE 2

Annual Design Center Costs*

	Gate array	Standard cell
Total hardware cost	350	450
Total software cost	300	240
Hardware depreciation	88	113
Software amortization	75	60
Hardware maintenance	35	45
Software maintenance	36	29
Support personnel	120	120
Total yearly cost	354	367
Design capacity (1k gates)	90	250
Cost per 1k gates	3.9	1.5

*All cost figures are in multiples of $1000.

custom ICs have emerged. Unfortunately, because none are sufficiently integrated, designs must be individually specified for each CAE tool.

A design group will thereby often intermix such CAE tools as high level block diagrams, a functional modeling language at the specification level, and netlist descriptions as input to the design verification simulator and/or to the fault-test generation simulation system. A netlist description can be used for the automated layout (placement/routing) system and for a device level description at the low level (circuit) simulation. Artwork is used to describe cells to the automated layout system and as a final description of the layout. Designers are discouraged, nonetheless, by the amount of clerical work necessary to use a CAE design tool, and by the potential that clerical errors may not be detected until the prototype is manufactured and tested.

In an advanced CAD system, a central data base stores essentially three types of information—block/logic diagrams, functional specifications and behavioral models, and artwork of cells and of the complete design. The data base stores all information in a nonredundant manner, thereby ensuring the integrity of derived data. Furthermore, the database system allows management to efficiently exercise control over a design project.

Hierarchical design support

Hierarchical design may be the only means to increase design productivity for large designs reaching 10k equivalent gates or more. Several logic design systems have recently emerged with full support of hierarchical design and, the approach may likely be extended to layout and test generation as well. Progress has also been made in replacing the designer with automated design synthesis in severely constrained situations. It is possible, for example, to automatically generate the control logic from a high level description for a finite-state machine. A similar level of automation is possible if the underlying control mechanism is implemented as a simple microcoded engine. But synthesizing the data path for a logic design involves numerous tradeoffs between cost and performance. In such cases, human insight remains superior.

Automating layout under constraints is common for gate-array and standard-cell designs. Improvements are expected mainly in the ability to handle less regular—and hence, less constrained—shapes. The ability to place and route arbitrarily shaped rectangular blocks will become essential as the technology advances.

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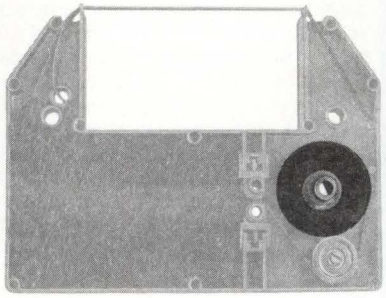

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CIRCLE 106

Automation has traditionally failed in test generation designs without constraint cases. However, a restricted approach such as the Level Sensitive Scan Design (LSSD) technique used by IBM Corp allows partitioning of the test generation problem into simple combinational subproblems, each with a few thousand gates at most. When design styles such as LSSD are incorporated into and enforced by a CAD system, automated test sequence synthesis may become a reality.

Since the introduction of the first 16-bit microprocessor, a revolution in engineering computing has occurred. Whereas engineers have had to share a large mainframe with other engineers, they now can perform some tasks on microcomputer based workstations. Although the cost of high resolution graphics workstations remains high, it is apparent that the mainframe may soon be partially replaced by a local network of engineering workstations.

However, computational needs will always exceed the abilities of most workstations for tasks such as test generation, placement, routing, and simulation. A large mainframe will still be required as a computational server and as a file server in the local network. Tasks will be divided between mainframe and workstation by such factors as size and nature of the design project, connection network, speed, relative speed advantage of the computational node, and design style of the individual engineer. Therefore, in future CAD systems the software must be able to run on both the workstation and the mainframe to create the optimal environment for solving engineering problems. These design tasks, sharing priorities and accomplished in given steps, will allow less expensive automated semicustom IC designs to be done in-house more efficiently. Resulting prototypes can then be more quickly validated according to specifications.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 725 *Average 726* *Low 727*

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CIRCLE 108

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600K-Whetstone	✓
8MB Maximum memory	✓
5MB/sec I/O	✓
Virtual addressability	✓
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Multiple I/O slots	✓
User microcode space	✓
Low Price	✓

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CIRCLE 110

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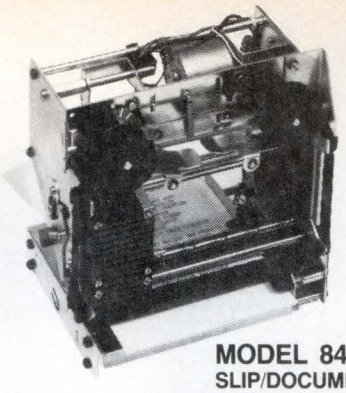

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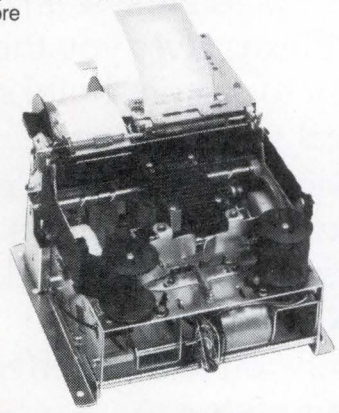

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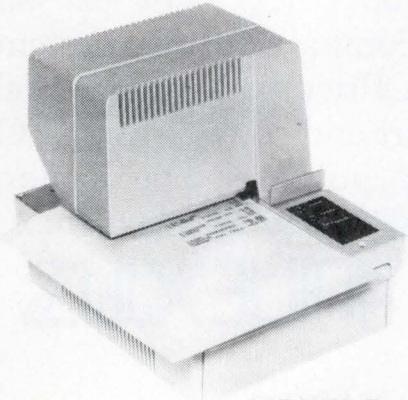

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Model 8400 and Model 8410 are complete with control and drive electronics. Serial, RS-232C or TTY and parallel interfaces are available. Both units can provide multiple print lines and carbon or pressure sensitive copy.

Model 8410 additionally features a stepping motor paper drive system which permits variable and programmable forward/reverse line spacing for applications requiring line selection and/or unique form indexing.

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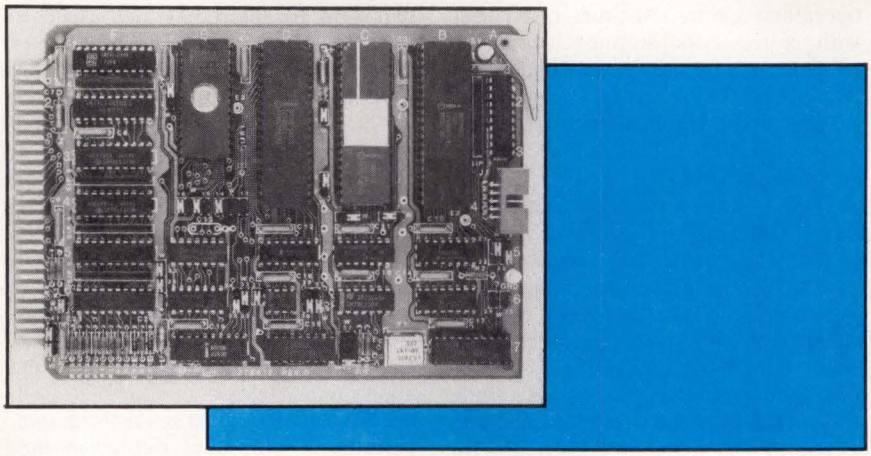
CIRCLE 111



Microcomputer boards put STD bus into realtime, multitasking arena

Ziatech's Series 8800 STD bus boards are expected to replace the STD bus' original 8-bit, light control applications with realtime, multitasking, and computation intensive functions. These 16-bit Intel 8088 CPU based microcomputer boards yield economical minicomputer processing power and a new packaging flexibility by having the CPU, math coprocessor, and silicon operating system reside on a single 4″ x 6″ (10- x 15-cm) STD bus board.

The company claims that the product family outperforms typical 8-bit units by a factor of 2:4. Also, direct main memory addressing of up to 1M byte is possible without extra overhead or loss of speed. This is made possible by four additional high-order memory address bits on the data bus that are multiplexed during what had been spare time in the data bus cycle.

Four processor boards, two memory boards, and an intelligent I/O processor board are initially included in the series. To accommodate realtime applications, each processor board supports vectored interrupts, eliminating delays incurred by software I/O polling.

The boards add innovative capabilities to the STD bus, including iRMX-86 and CP/M-86 silicon operating systems integrated on STD bus boards, a combined 8088/STD bus processor running at 8 MHz, and a 256k-byte dynamic RAM board that supports 20-bit (1M-byte) addressing.

Also featured is an integrated RAM (iRAM) supported on STD bus byte-wide memory boards. These iRAMs are interchangeable with PROM and fit into the PROM sockets. In addition, the series includes an 8088 based intelligent I/O processor board that includes memory and three types of I/O and a Multimodule piggyback I/O for tailoring the I/O processor to specific applications.

The 5-MHz ZT 8810 and 8-MHz ZT 8811 16-bit CPU based board computers are compatible with the iRMX-86 realtime and

(continued on page 200)

Series 8800 STD bus microcomputer boards

Product	Speed	PROM (bytes)	RAM (bytes)	Features
ZT 8810 board computer	5 MHz	16k		One serial port; optional development monitor
ZT 8811 board computer	8 MHz	16k		Optional development monitor
ZT 8812 integrated board computer	5 MHz	16k		Optional 8087 math coprocessor; silicon iRMX-86 or CP/M-86
ZT 8813 integrated board computer	8 MHz	16k		Optional 8087 math coprocessor; silicon iRMX-86 or CP/M-86
ZT 8820 byte-wide memory	5 MHz (no wait states) 8 MHz (one wait state)	2k to 32k	2k to 32k	Supports PROM, EPROM, EEPROM, and RAM in common
ZT 8821 dynamic RAM board	5 MHz (no wait states) 8 MHz (one wait state)		64k to 256k	Parity error generates a nonmaskable interrupt
ZT 8830 intelligent I/O controller	8 MHz	32k	32k	Onboard serial, parallel, and Multimodule I/O

Microcomputer boards

(continued from page 199)

CP/M-86 disk based operating systems. Wait states are provided for use with slower (250- to 450-ns) memories and I/O devices. An I/O port space of 64k is accessible. An onboard programmable UART for standard asynchronous communications for one RS-232-C channel is also provided by the ZT 8810. Eight vectored interrupts are maintained on both boards, and with added offboard interrupt controllers, expansion to 50 vectored interrupts is possible. One onboard 16k-byte PROM socket is allocated, and an optional debugging monitor PROM occupies this space during development. A development monitor for loading and debugging the target system is installed in the boards' PROM socket.

The ZT 8812 5-MHz and ZT 8813 8-MHz processor boards (see Photo) combine CPU, math coprocessor, and iRMX or CP/M operating systems. No licensing is required of either iRMX-86 or CP/M-86 on these boards. An onboard operating system chip socket also accepts a simple utility chip with interrupt controller/timer functions. The optional 8087 math coprocessor lets the system handle math operations up to 100 times faster than with software subroutines. Both processor boards furnish memory addressing, wait states, 16k-byte ROM, interrupt controller, and development/debug monitor PROM capabilities similar to the 8810/8811 computer boards.

Eight 20-pin sockets that accept various combinations of ROM, PROM, EEPROM, and RAM are features of the ZT 8820 byte-wide memory board. Storage choices include 2k to 32k bytes of either ROM or RAM. Selectable wait states, 1M-byte addressing, optional RAM battery backup, and no wait states at 5 MHz add to the boards' capabilities.

The ZT 8821 dynamic RAM board for 16-bit microprocessors is available in 64k-, 128k-, and 256k-byte increments. Parity checks and onboard memory refresh are provided. Like the 8820 board, highlights are 1M-byte addressing, battery backup, and no wait states at 5 MHz.

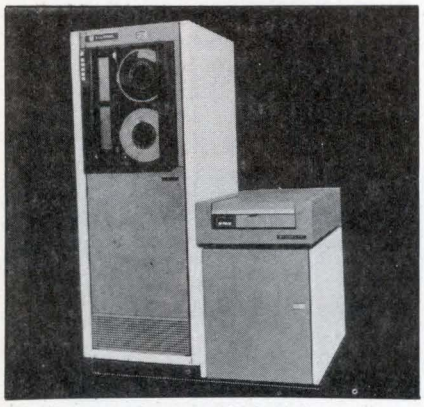
A ZT 8830 control processor can stand alone or be used as a slave I/O processor. It has 32k-byte onboard RAM, three PROM sockets, eight priority interrupts, two 8-bit parallel ports, one asynchronous serial port, and five 8-bit counter/timers, and also includes one Multimodule I/O socket.

To program/debug Series 8800 computer applications, an integrated or kit form CP/M-86 development system built around the 8800 boards is offered from Micro/Sys Inc of La Canada, Calif. The IBM Personal Computer, with an 8088 processor/CPU, can also serve as an iRMX-86 development station. Real Time Computer Systems Corp (RTCS) of Camarillo, Calif, provides software that allows Intel's iRMX-86 development packages to run on the IBM PC. A third applications development/debug method comes via Intel's Series III development system, which provides the capabilities to develop or emulate Series 8800 processor boards.

The boards have a 4- to 8-week delivery time, and a price range of $349 to $850. **Ziatech Corp**, 3433 Roberto Court, San Luis Obispo, CA 93401.

Circle 261

Superminis increase capacities while cutting costs



Challenging the capabilities of VAX 11/780, Harris Corp has added models H800-2B and H800-2BP to the 800 superminicomputer series. They incorporate a new memory board design and I/O products, greater configuration flexibility, and reduced floor space requirements. The units typically provide more basic physical memory size (768k bytes each) for their price class than other 800 series computers. Cycle time is cut to 335 ns and access time to 250 ns for 48 bits of data.

The computers are configured with the company's communications network processor (CNP). (See *Computer Design*, Dec 1982, pp 37-38.) This single-board CNP allows handling of up to 128 terminals with virtually no impact on the 48-bit CPU, and supports simultaneous communications via asynchronous, synchronous, isosynchronous, and X.25 protocols to a wide variety of networking peripherals. Up to 16 communication lines are supported for either local or remote device connection; each line can concurrently support a different protocol at different speeds.

Greater flexibility and smaller footprint features of the H800-2B/2BP are direct results of combining memory controller functions and memory arrays on the integrated memory subsystem (IMS) single board. This board has up to 1.5M-byte memory, and multiple memory subsystems can be configured for up to 12M bytes of real memory. The LSI designed PCB detects/corrects all single-bit errors, and detects all 2-bit errors and most 3-bit or more errors. Error correction is performed on a 24-bit basis, allowing 2-bit correction on 48-bit memory accesses.

As a guard against random failure due to alpha particle radiation, the IMS performs rewrite operations on all correctable errors, thereby preventing random error accumulation and possible uncorrectable errors. Memory failures are isolated down to the RAM component level. Both 2- and 4-way interleaving configurations are supported. The IMS board is offered in 384k-bit ($9000), 768k-bit ($12,500), and 1.5M-byte ($18,500) memory sizes with controller.

All 800 series models have up to 12M-byte physical memory, 48M-byte virtual memory implemented in hardware, and support 128 concurrent users and 255 devices handling interactive tasks. An integral hardware floating point processor and a 48-bit architecture with pipeline and parallel processing capabilities are also included.

H800-2B is claimed to equal the performance of the VAX 11/780 and is priced from $139,000. Fully compatible, it is field upgradable to the H800-2BP for $35,000. The H800-2BP system also packs a 6k-byte, 150-ns cycle/70-ns access time bipolar cache memory. It boasts approximately 30% more performance than the VAX system, and is priced from $164,000. Both models will be available for shipment in March 1983. **Harris Corp, Computer Systems Div**, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309.

Circle 262

THE NEW DATATEST.
NOW YOU CAN HAVE IT BOTH WAYS.

Datatest I

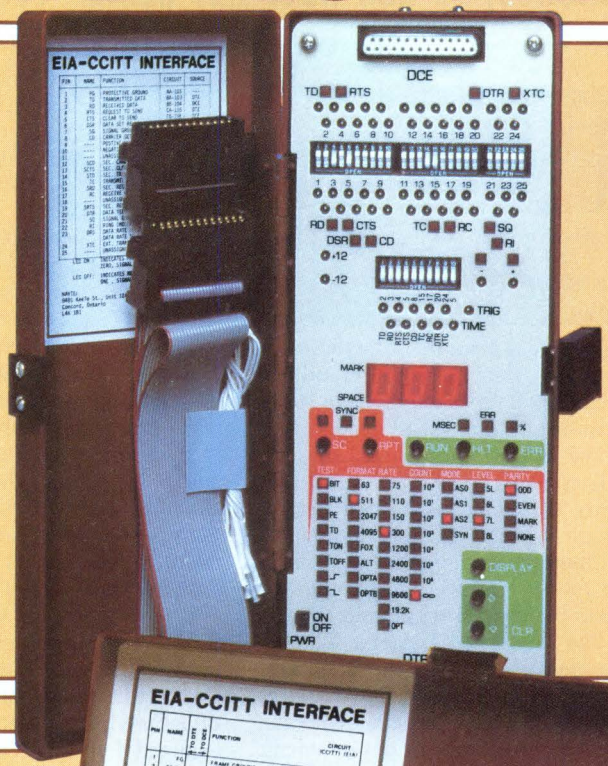
Already the standard of the industry.

This new hand-held test set is a logical extension of our successful Supertest which quickly became standard equipment at telephone companies, modem and multiplexer manufacturers, as well as major end users world-wide.

Like Supertest, Datatest I is designed for field service, but it gives you even more features. Providing more DCE testing capability and more flexible timing tests, the battery operated Datatest I still weighs less than 2 lbs. And it's easy to use with test parameters clearly marked for all phases of operation featuring colour grouped function controls and bright LED readouts.

Versatility is the key to success in the field and Datatest I has it in spades. In fact, no other test set this compact even comes close to its wide range of capabilities. And we've built it to be rugged and reliable in the field.

Datatest I. Best by any test.



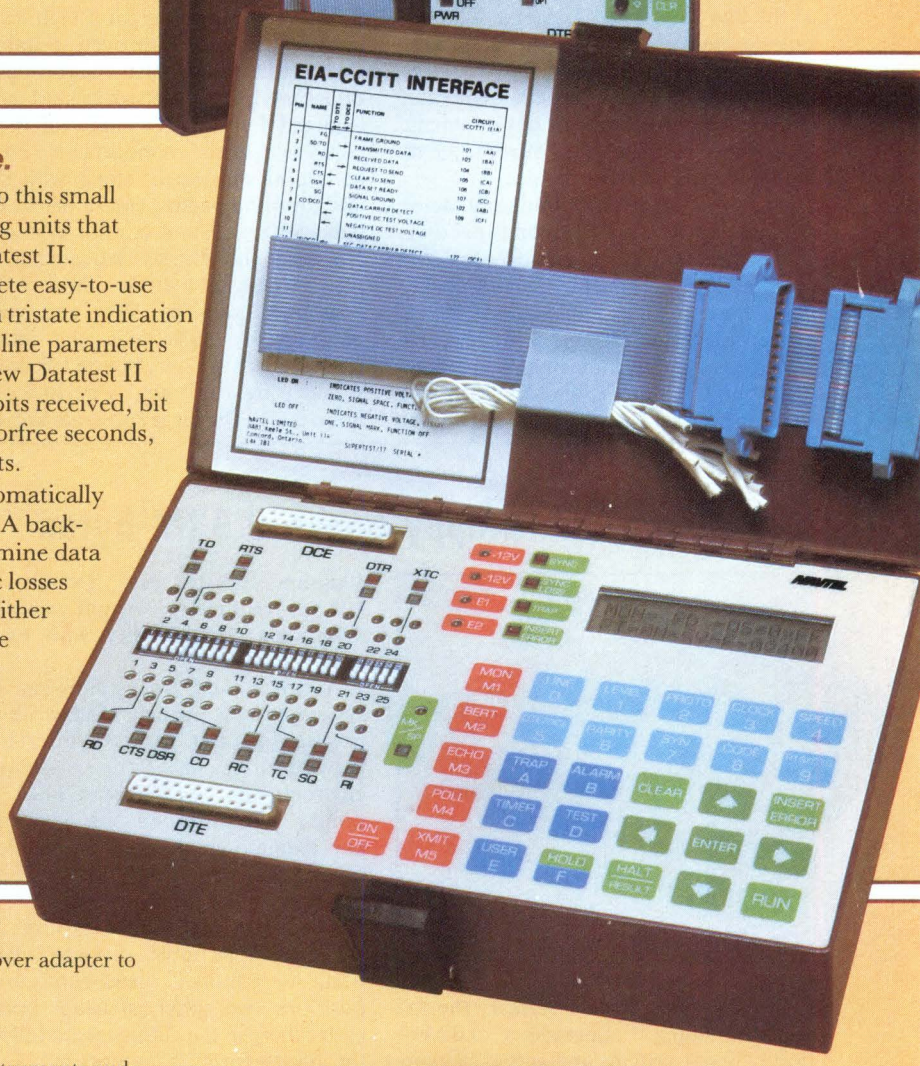
Datatest II

Test miracles in a small package.

It's hard to believe, but we have built into this small package, test set capabilities of competing units that are five times the size and weight of Datatest II.

Datatest II provides you with a complete easy-to-use integral EIA RS-232C breakout box with tristate indication of interface status. All test functions and line parameters are menu selectable. Our outstanding new Datatest II **simultaneously** measures and displays bits received, bit errors, blocks received, block errors, errorfree seconds, errored seconds, sync losses and time outs.

At the end of your test Datatest II automatically calculates both bit and block error rates. A background trap and timer allows you to examine data around errors, events, characters or sync losses or analyze response times. The user can either define his own messages or use **any of** the pseudo random or Fox patterns. Preprogrammed DCE or DTE configuration is selected electronically so that the Datatest II can test terminals, printers, point-to-point communications facilities, multi-drop networks and X.25 facilities.



Datatest I

$1,595.00 includes a leather case and a turnover adapter to facilitate terminal testing.
3⅜ in. wide x 9 in. high x 2¾ in. deep.

Datatest II

$1,895.00 with a leather carrying case for instruments and accessories.
8 in. wide x 5 in. high x 2¼ in. deep.

Send for free literature and application notes on these new pace setters in the test field.

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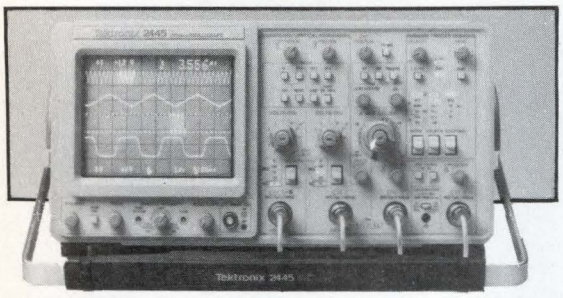
CIRCLE 112

Oscilloscopes use new CRT design for high performance at low cost



Expecting to supplant the 400 series oscilloscopes as the industry standard, Tektronix's 2400 series scopes have meshless scan-expansion (MSE) lenses with quadruple optics at the heart of their CRTs. These lenses overcome many trace problems associated with high performance CRTs, such as halo and ghost effects and high manufacturing costs.

Two models introduced are the 2445 150-MHz bandwidth scope and the top of the line 2465 300-MHz scope. With its superior performance, the 2465 is suitable for mainframe computer design, large ECL system test and measurement, and realtime control system development. Both scopes can be used for TTL, 2-ns ECL, and MOS LSI/VLSI design.

Added capabilities include scale factor readout of volts and/or seconds per division, and onscreen cursor directed movements that include delta volts, delta time, 1/delta time, delay time, phase, and ratio. Trigger voltage levels and special mode indicators (eg, bandwidth limit, hold-off, and X-Y display) also appear onscreen. An auto-level trigger gives hands-off triggering down to 20 Hz on most repetitive signals. Trigger bandwidth extends to 500 MHz in the 2465 and 250 MHz in the 2445. Independent A and B sweep trigger coupling and level/source selections allow A and B sweep triggering on dissimilar and non-time-related signals.

The MSE lens is laser cut from 1-piece stainless steel tubing. A 1-piece meander-line deflector moves the electron beam vertically. Electrons pass through three quadruple focusing lenses and then through the MSE lens, which expands and accelerates the beam. Because all active electron-optical elements are embedded firmly in the gun, the CRT withstands shocks up to 150 G.

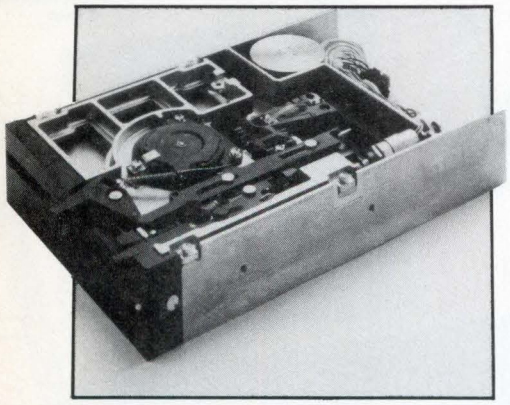
Twelve ICs were developed for and used in the 2400 series for a high level of integration and improved reliability. Calibration time is also cut through use of laser-trimmed networks and active-trimmed hybrids. Virtually all the circuitry is made of monolithic ICs bonded to hybrid substrates, along with thick- and thin-film passive components. Eight hybrid ICs and one custom MOS circuit are used for display sequencing. The active-trimmed hybrids improve horizontal accuracy by 50% and vertical accuracy by 30% over the industry standard. ICs are wire bonded to the substrate using 1-mil gold wire to 2.5-mil^2 bond pads. The large substrate is divided into individual hybrids after assembly. An epoxy sealant is the basis for the hybrid package, providing a highly reliable hermetic seal over the hybrid substrates.

Super high frequency-III (SHF-III) process and its high voltage derivative SHF-HV provide the technology for easy to use performance, low weight and small size, and reduced power requirements. The SHF-III bipolar process offers NPN structures with transition frequency beyond the 4- to 5-GHz range; its high speed stems from small geometries and shallow diffusions. Standard emitter width is 2 microns, with layer to layer tolerances of 1.5 microns. Emitter depth is only 2000 Å, and base width is 1000 Å. All dopants except the isolation region are implanted. Metallization line widths are typically 3 microns to minimize parasitics; gold is used to avoid electromigration problems.

SHF-HV provides 65 V to directly drive the oscilloscopes' CRTs. Higher voltage is obtained via the modified SHF-III process, where a thicker, higher resistivity epitaxial layer achieves the necessary breakdown voltage characteristic. A lower transition frequency results than with SHF-III, but the combined slower speed and higher voltage is ideal for driving the CRTs' deflection circuits.

The two oscilloscopes are being introduced in February, at a price of $3140 for model 2445 and $4600 for model 2465. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077. **Circle 263**

Half-height mini-floppy packs 3.33M bytes



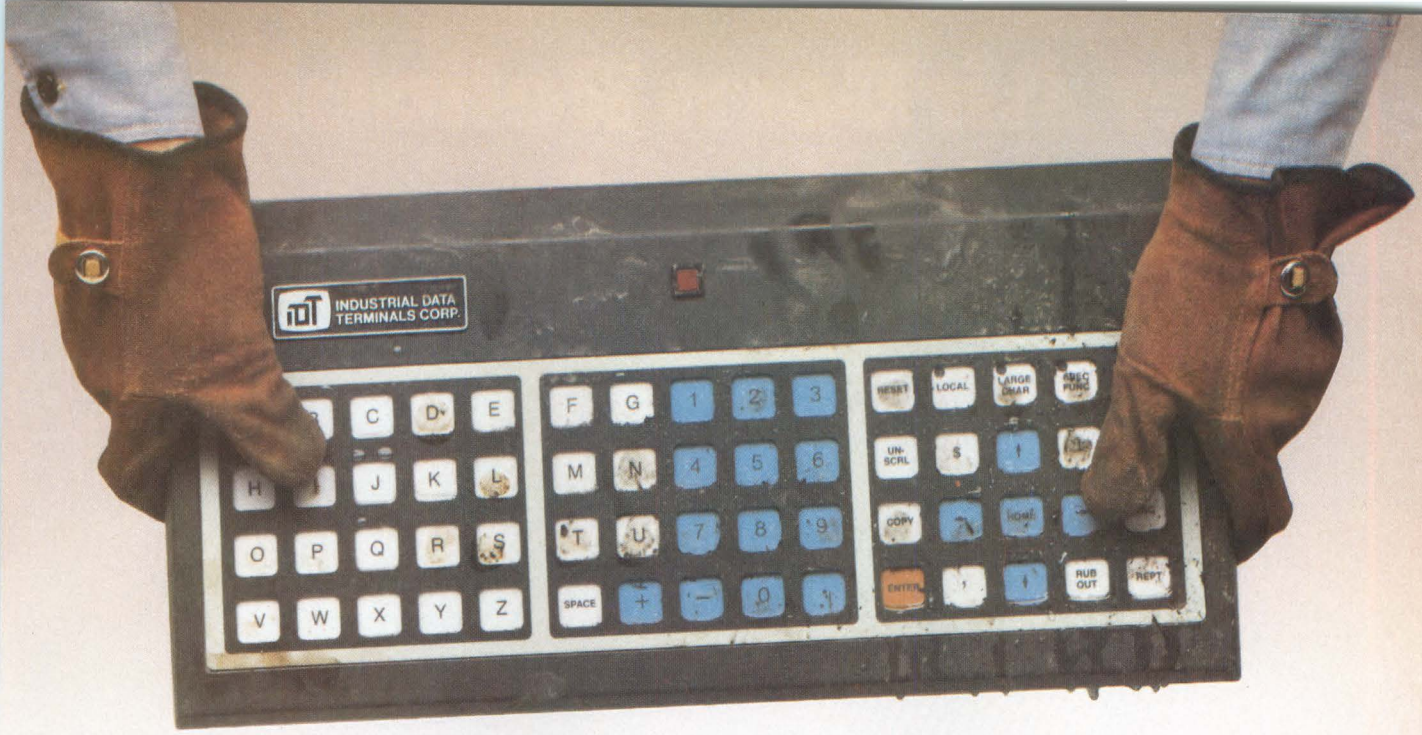
Drivetec's first product release, the 320 SuperMinifloppy™, upgrades 8″ and 5¼″ floppy based systems and acts as backup for small Winchester based systems. It has 3.33M-byte unformatted capacity, 3-ms track to track access time, and a 500k-bps transfer rate. Double-sided, 192-tpi recording format maintains downward compatibility with existing mini-diskettes.

A proprietary track-following servo system ensures ontrack read/write head positioning and diskette interchange between drives in different systems and environments. A 2-stepper head positioning system moves one head to the approximate track position, while the other adjusts the head in 200-μin increments to center it exactly.

Absolute vertical clamping gives accurate, repeatable diskette registration. A "gumball" head configuration positions two spherical heads opposite each other, so the elastic media following the heads forms a natural curve. This improves media wear characteristics over typical double-sided head configurations. Other key features include onboard microprocessor and brushless dc drive motor, buffered track seek, and door lock.

Each diskette contains 160 cylinders. There are 320 tracks (160/side), with 8192 bytes/track and 256 bytes/sector. MTBF is about 10k power-on hours. Soft read errors are approximately one in 10^9, hard read errors one in 10^{12}, and seek errors one in 10^6.

Media is a preformatted, 50-μin oxide platter that allows higher bit and track densities than conventional 100-μin media, and should cost about $3.50 as production volume grows. The desktop unit weighs 2 lb (0.9 kg) and measures 1.62″ x 5.75″ x 8.62″ (4.11 x 14.61 x 21.89 cm). SuperMinifloppy evaluation units will be shipped first quarter 1983, priced under $325 in quantity-1000. **Drivetec Inc,** 2140 Bering Dr, San Jose, CA 95131. **Circle 264**



New. Sealed. Tough. Rugged. Change key functions and legends

Flexibility. Key functions can be programmed and key legends changed, to match any plant process—again and again, whenever you wish. And, serial interface is adaptable to many systems.

Real Time Interaction. Each key can have its own programmable LED, cueing the operator to the proper process adjustment. Protect and lockout feature allows supervisory override of operator control functions.

Tactile Location. Bezel surface overlay provides positive key location, even with gloves on. Blinking optical feedback LED indicates keystrokes.

Rugged.
Reliable.
Performance-proven.

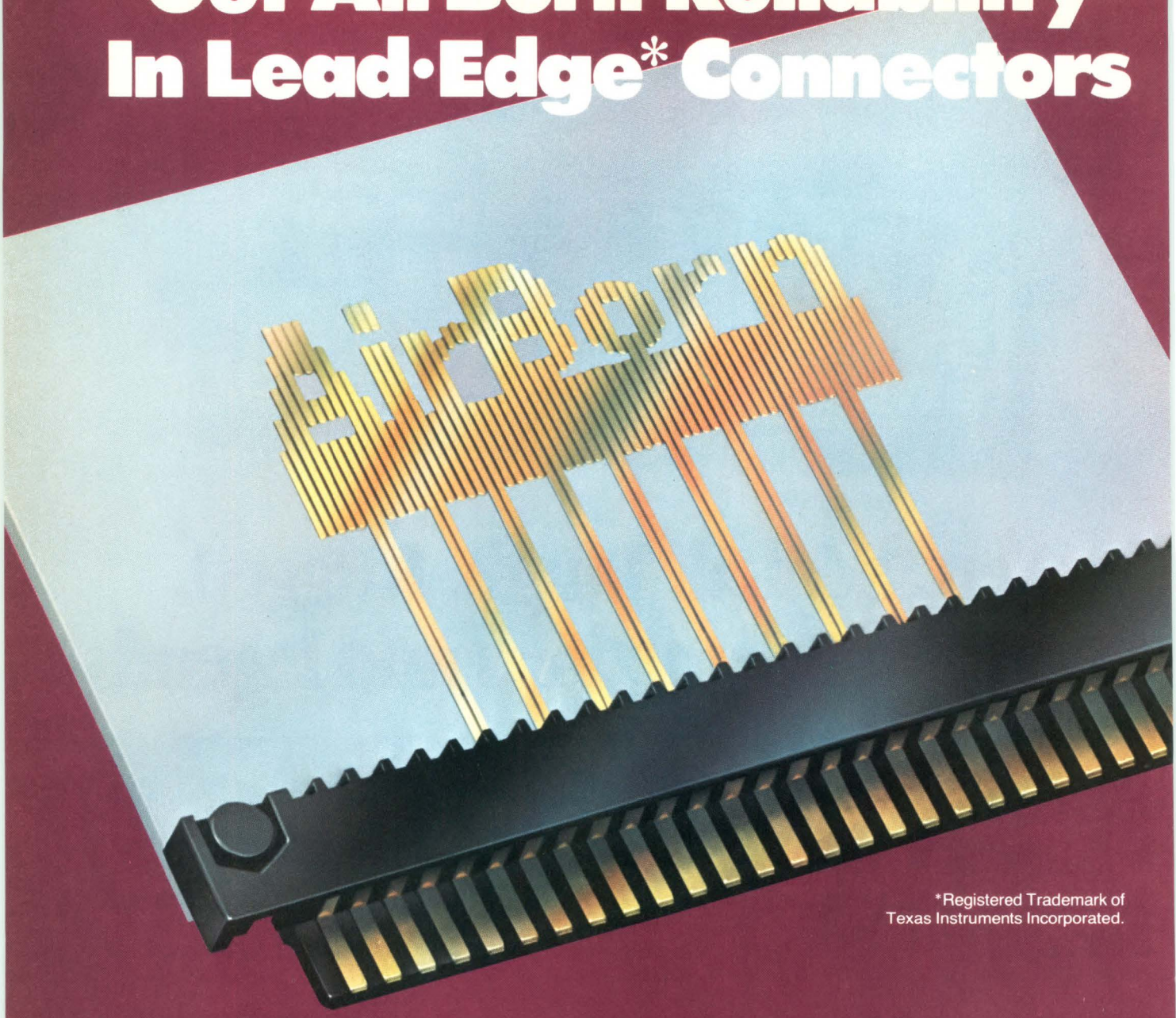
...to suit yourself.

IDT color graphics terminals are now available with this new industrial grade programmable entry panel. Easy for your operators to learn and to use, the panel can simplify and improve real time monitoring and control of your process. For more information contact IDT now.

Industrial Data Terminals Corp.
173 Heatherdown Drive, Westerville, OH 43081 (614) 882-3282

CIRCLE 113

Get AirBorn Reliability In Lead•Edge* Connectors



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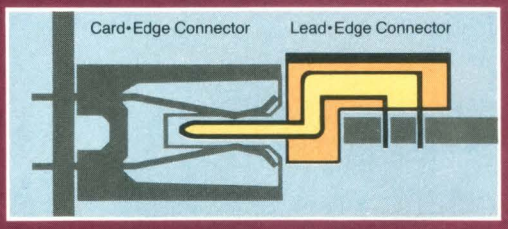
Texas Instruments Incorporated.

AirBorn's Lead-Edge* Connectors take the thickness variations out of your PC boards and insure circuit integrity, two-piece connector reliability, eliminate PC board gold plated fingers . . . and at low cost. The sturdy molded body with gold plated stamped contacts are built for controlled insertion and withdrawal forces and mate with all major edgeboard connectors. Each connector is made to the specifications and quality you have come to trust from AirBorn. Five sizes are available (from 56 to 100 contacts) and shipment can often begin within a week of the order! Call us in Dallas at 214-931-3200 . . . or TWX-910-860-5230 . . . or TELEX 794200.



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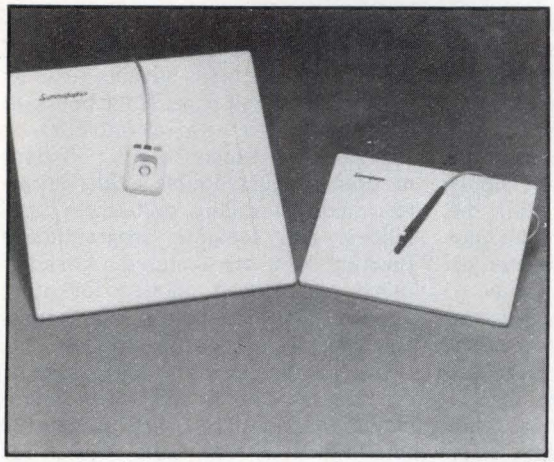
4321 AirBorn Drive / Mail: P.O. Box 519 / Addison TX 75001

CIRCLE 114

Ergonomic data tablets combine capabilities of digitizer and mouse



MM series digitizers 960 and 1200 feature a newly designed stylus and cursor. The 3-button cursor has a cross-hair sight and performs mouse-like steering and high-accuracy tracing. It outputs either delta or absolute coordinates. For free-hand drawing and menu picking, the stylus offers a solid state pen-tip switch and a user assignable barrel button.

Summagraphics has supplanted its magnetostrictive approach with no-magnet, electromagnetic technology. MM series digitizer resolution is selectable at up to 500 lines/in. Alternatively, the digitizers automatically scale output both horizontally and vertically to match CRT resolution and orientation by remote commands. The 6″ x 9″ (15- x 23-cm) model 960 has 3000 x 4500 resolution points in its active area, and the 12″ x 12″ (31- x 31-cm) model 1200 offers 6000 x 6000 points of resolution. Both tablets use the same format so that they can be interchanged for different size requirements. The coordinate origin relocates for horizontal or vertical orientation.

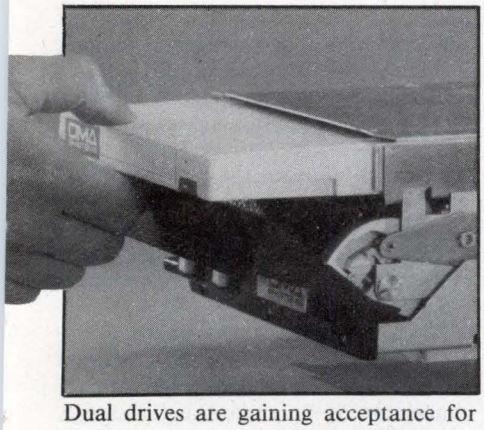
Electronics reside on a single printed circuit grid approximately 0.8″ (2.0 cm) thick within the digitizer's lightweight, tilt-adjustable plastic case. The units consume under 2 W and operate directly off terminal or workstation power supplies. Proximity of 0.5″ (1.3 cm) allows mounting under a tabletop.

Operating modes include point, stream, switch stream, delta, incremental, and diagnostic. Selectable sampling rate is 100, 50, 20, or 2 pairs/s. All functions, including modes, sampling rate, and resolution, are remote controllable from the host. Built-in diagnostics check electronics, communications, tablet, and stylus or cursor.

Serial, asynchronous, or bidirectional electronic interface matches RS-232-C or TTL output levels. Optional dual-port capability for inline operation lets the tablet be placed between the host and an additional peripheral.

Volume production of MM 960 and 1200 digitizers will begin in April 1983. Units are expected to cost under $400 each in quantity. **Summagraphics Corp,** 35 Brentwood Ave, PO Box 781, Fairfield, CT 06430. **Circle 265**

Fixed/removable Winchesters boost fixed storage



Dual drives are gaining acceptance for mass storage, I/O, and backup file generation within the 5¼″ form factor. To meet a growing demand, DMA Systems is building up fixed storage capacities in its Micro-Magnum family by reducing fixed disk track width, doubling track density, and increasing the number of cylinders.

The Micro-Magnum 5/10 cartridge drive has a 19.5M-byte unformatted storage capacity, with 13M bytes on the fixed disk and 6.5M bytes on the removable cartridge. The Micro-Magnum 5/15 holds 26M bytes unformatted, with 19.5M-byte fixed and 6.5M-byte removable storage.

A shared spindle and electronics for both the fixed and removable functions significantly improves drive reliability. In addition, the units employ embedded servo technology for reliable cartridge interchange and accurate track positioning. (See *Computer Design*, Feb 1982, pp 44-46.) Both model 5/10 and 5/15 can be used to upgrade existing systems as well for new designs; front panel dimensions are identical to those of standard 5¼″ floppy disk drives.

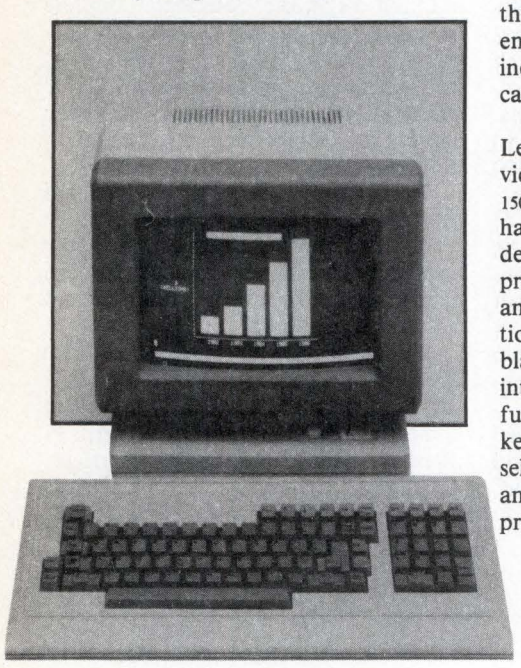
Average data access time across the family is 40 ms, and the data transfer rate is 5M bps. Each removable disk has 320 cylinders with a 454-tpi track density. The 5/10's fixed disk has 640 cylinders while the 5/15 packs 960, with densities of 908 and 1156 tpi, respectively. There are 33 sectors/track (one is spare) and each sector contains 256 data bytes. Recording density for all models is 8617 bpi.

CushionAire™ read/write heads dynamically load and unload from rotating disks without contacting the media. They retract and latch into rest position when not in use to avoid media damage. A self-sealing drive door prevents contaminants from entering the head disk assembly and ensures a class 100 clean air environment inside the assembly. When a cartridge enters the drive, a door-actuator mechanism opens head access and air filtration ports on both the cartridge and the drive. Doors automatically close when the cartridge is removed.

The Micro-Magnum cartridge is an ANSI proposed standard. Evaluation models will be released in 1983—the 5/10 in the second quarter and the 5/15 in the third quarter. In quantity-1000, the 5/10 will cost $1390 and the 5/15, $1450. Removable cartridges will be $85 each in OEM volume. **DMA Systems Corp,** 601 Pine Ave, Goleta, CA 93117. **Circle 266**

Smart CRT terminals emulate higher priced competitors

In an attempt to capture a part of the estimated half-million general purpose terminals in use during 1983, the QVT™ series of smart CRT terminals are designed to aim at timeshared database management applications. All three ergonomically designed terminals in the series feature a 12″ (30-cm) tilt and swivel display, small footprint, and low profile detachable keyboard. Menu setup mode into nonvolatile memory, green nonglare screen, 25th status line, 9 x 12 cell resolution, screen-saver timeout, self-test mode, and a switching power supply that requires approximately half the energy of comparable terminals are included. A line drawing character set can create charts, graphs, and forms.



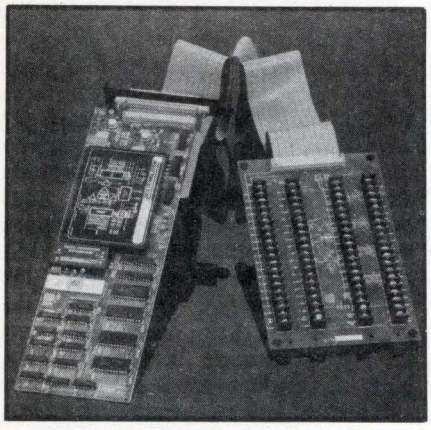
QVT 102, priced at $695, emulates the Lear Siegler ADM 3A and ADM 5, Televideo 910, ADDS Viewpoint, or Hazeltine 1500 terminals. The 80-column display has a 7- x 9-character format with descenders for easy readability. Four programmable function keys; local, line and page block transfer, and conversational modes; protected fields; blink, blank, reverse, underline, and half-intensity video attributes; full editing functions; and separate cursor control keys are provided. Sixteen baud rates are selectable, ranging from 50 to 19.2k bps, and a unidirectional RS-232-C port is provided.

QVT 103 uses ANSI X3.64 (1979) compatible codes, includes all functions of the QVT 102, and adds advanced editing features. Two full pages (four optional) of memory, CRT with selectable 80- or 132-character display format, standard or double-height/double-width characters; smooth scrolling, split-screen capabilities, and separate programmable function keys are featured. An additional card slot is allotted for other options. The $895 unit is interchangeable with DEC's VT100/132 terminals.

QVT 108, in addition to all features of the QVT 103, has 11 separate programmable function keys that provide 22 total functions with shift register for increased power and flexibility. Two pages of memory and time of day clock are included.

All three terminals are available with optional amber CRTs, 20-mA current loop, and multiple foreign character sets. Quantity volumes will be available in the first quarter of 1983. **Qume Corp, a sub of ITT,** 2350 Qume Dr, San Jose, CA 95131. **Circle 267**

Single-board I/O and computer form complete data acquisition system



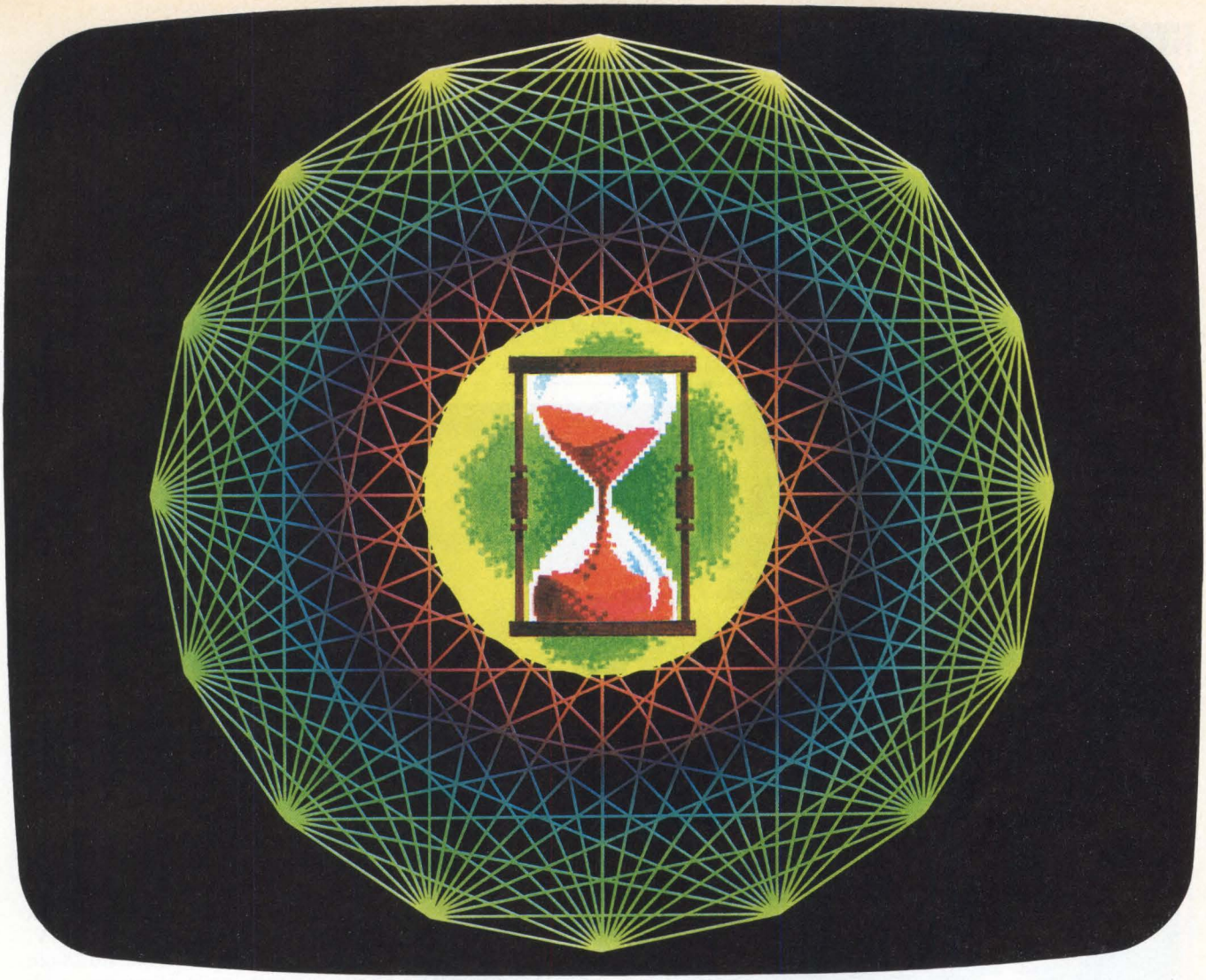
A single-board analog and digital I/O system that plugs directly into one expansion slot of the 16-bit IBM PC, the DT2801, priced at $1195, features a 12-bit ADC for 16 single-ended or 8 differential input channels with software programmable gains of 1, 2, 4, or 8. Two DACs with 12-bit resolution can be used independently or changed simultaneously. In addition, the board includes two 8-line digital I/O channels that can also be used separately or changed simultaneously. An onboard programmable clock can trigger any of the A-D or D-A commands.

Easily programmed from IBM's interpretive and compiled BASIC languages, all I/O clock functions can be accessed from three BASIC commands that read from or write to the board's command/status and data registers. The clock monitors A-D and D-A conversions, with intervals settable in 2.5-ms increments. An external clock can also be used. The external trigger control feature enables users to inhibit command execution until a pulse occurs on the external trigger line so that board operations can be synchronized with external events.

An onboard microcomputer with built-in analog I/O microcode offloads the host IBM CPU and interfaces between the DT2801 and the computer, controls all onboard analog and digital I/O operations, and performs board self-test functions. The board's architecture combines A-D, D-A, and digital I/O functions with five programmable operating modes, including DMA and programmed I/O data transfers. I/O functions can be initiated by either hardware or software control.

The A-D system can be jumper configured for unipolar or bipolar inputs of up to 10 V FSR; the two analog output channels have five jumper selectable output ranges. The entire single-board system operates from the host computer's 5-V power supply.

Also available for the board is the table-mounted DT707 screw terminal panel ($149) with integral cable for easy connection of the analog/digital signals to the host computer shown in Photo (right). The combined board and PC provide a complete data acquisition system, with computer, display, disk, printer, and analog I/O hardware for approximately $5000. The DT2801 is shipped complete with a comprehensive user's manual that includes sample programs. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 268**



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Ikegami Technology

For systems applications requiring high quality, dependable CRT display monitors, Ikegami brings you the technology of the future, today.

An innovator in video technology for over 36 years and the world's leading producer of high quality broadcast camera systems and monitors, Ikegami has applied its unparalleled experience to the design and production of display monitors for the computer industry. Put Ikegami's Emmy award-winning digital techniques for automatic setup to work for you.

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HDM Series

Ultra high resolution for your most demanding graphics systems. Ikegami's HDM Series color and monochrome display monitors utilize a delta-gun, raster-scan CRT and superb quality wide band, high speed scan, video amplifiers to provide the precision you need (up to 1280 × 1024 pixels interlace mode), plus the long life and easy maintenance you demand from a top quality graphics display. Available in 19V and 25V CRT sizes.

The CD Series (CDA/CDB)

Quickly becoming our most popular line of high resolution in-line gun color CRT display monitors. If your requirements are for high resolution (up to 1024 × 1024 pixels interlace mode), stable operation and very low maintenance, the CD Series may be your solution.

Available in 13V and 19V analog or digital models, the compact-size CD Series is perfect for simulation, medical, CAD/CAM and other high resolution applications.

The UD Series

Medium resolution, digital drive, color display monitors for business graphics systems. The Ikegami UD Series provides high performance (615 × 240 or more pixels interlace mode) at a very economical price.

The BDM Series

High performance, flicker-free monochrome CRT display units that bring Ikegami quality to word processing or on-line data entry systems. Available in green or white display and standard CRT sizes (5″, 9″, 12″, 14″ and 15″).

Easy Interface. Easy Maintenance.

Ikegami display monitors are designed to interface with your equipment, quickly and easily. There's no complex rework ... no hassle. Ikegami's sophisticated design virtually eliminates maintenance problems, so you know your Ikegami displays will continue to bring out the best in your systems, year after year.

For more information on high-performance CRT display units designed to meet your needs, today and tomorrow, write or call Ikegami today.

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(213) 534-0050

CIRCLE 115

128k-bit EPROM

MBM27128 16k-word x 8-bit EPROM provides twice the memory capacity of std 64k EPROMs without loss in access time or increase in power dissipation. The device will be available in 200-, 250-, and 300-ns access times and is completely compatible in pinout, function, and programming with the MBM2764. It is available in a 28-pin DIP or 32-pad LCC, both with std JEDEC pinouts. Using the "Quikpro" programming technique, the EPROM can be programmed within 2 min. Volume production of the 128k chip is scheduled for the second quarter of 1983. **Fujitsu Microelectronics,** 2985 Kifer Rd, Santa Clara, CA 95050.
Circle 269

3-ns access time RAM

Bipolar 64-bit ECL RAM MC10H145 has an address access time of 3 ns typ and 6 ns max. Organized as a 16 x 4 memory array, both constant current source gates and voltage regulator are included. Device is processed with the MOSAIC (Motorola oxide self-aligned implanted circuit) for smaller device geometries, improved bandwidth, and reduced parasitic capacitances. Compatible with the company's MECL 10K family and Macrocell Arrays, rise and fall times are 0.7 ns min and 2.5 ns max for both address and chip select to output. MC10H145L cerDIP is $10.65; MC10H145P plastic DIP is $9.25. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 270

64k CMOS static RAM

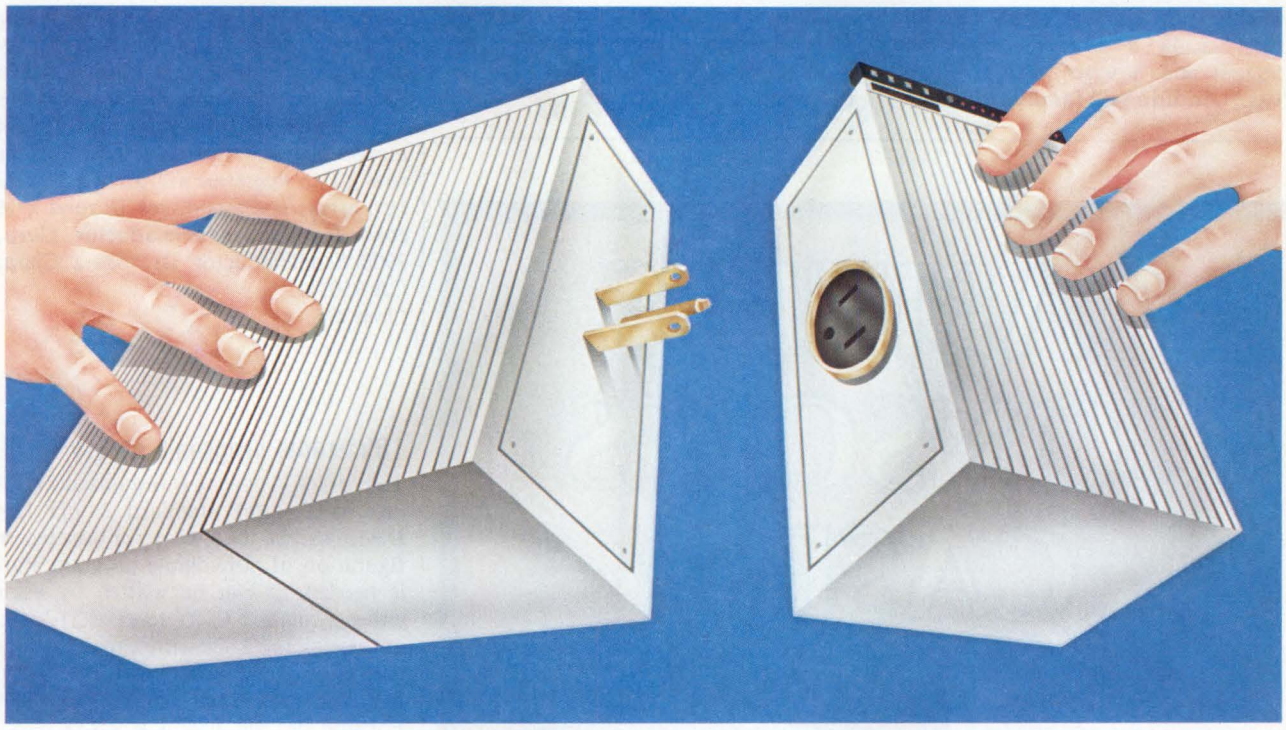
The TC5565P NMOS/CMOS RAM has 100-ns access, 5-mA/MHz operating current, and 100-μA standby current. TC5564P pure CMOS device operates with the same access time and operating current, but draws no more than 1 μA in standby mode. Both devices are configured 8k x 8, are fully static, operate from a 5-V single supply, and are directly TTL compatible. Power dissipation is 27.5 mW/MHz max operating, and data retention is 2 V. Devices are packaged in JEDEC std 28-pin plastic DIP that is pin compatible with the 2764 EPROM. **Toshiba America, Inc,** 2441 Michelle Dr, Tustin, CA 92680.
Circle 271

Low power 256k NMOS ROM

A 256k edge triggered NMOS ROM operates on a single 5-V power supply with $\pm$10% supply tolerance. Access time is 250 ns. Device draws 40 mA max power when active and 15 mA max in standby mode. A 32,768-word x 8-bit organization with std JEDEC pinout is featured. Fully TTL compatible, the device is available in ceramic (μPD23256D) and plastic (μPD23256C) 28-pin DIPS. **NEC Electronics U.S.A., Inc, Electronic Arrays Div,** 550 E Middlefield Rd, Mountain View, CA 94043.
Circle 272

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

At last, plug-in parallel processing in a 32-bit supermini system.



Perkin-Elmer announces the Model 3200 Multiple Processing System, an exciting new concept for demanding real-time applications.

Room to grow

The Model 3200MPS gives you extraordinary system expandibility. You can start with a host CPU and one auxiliary processing unit (APU). Then as your needs grow you can plug in more performance by adding as many as eight additional APUs.

Should you need even more horsepower, plug-in parallel processing lets you add exactly what you need as you need it—from a single APU to a whole fleet of multiple processing systems.

And no matter what the size of your configuration, a central point of control and management is provided by a single copy of our field-proven OS/32 operating system.

Design flexibility

With parallel-processing APUs you can take advantage of application segmentation and structured programming techniques to speed system development. You can segment your application into multiple task modules, with each APU performing a set of related functions. To further optimize system performance, you can easily re-allocate tasks among the APUs.

Your Model 3200MPS provides maximum flexibility for software development, reliability, and system maintenance. To incorporate new design changes or correct problem modules, simply work on the problem module while your system continues to operate. And the Model 3200MPS can be structured to permit continued system operation though one or multiple APUs may fail. When so structured, the APUs can receive immediate maintenance attention while the system continues to run or they can wait for routine scheduled maintenance.

And our state-of-the-art universally optimizing FORTRAN VIIZ enables you to use modular programming techniques without sacrificing real-time efficiencies.

To find out more about how you can plug into all the advantages of plug-in parallel processing minis, mail the coupon or call today: The Perkin-Elmer Corporation, Two Crescent Place, Oceanport, NJ 07757.

Tel: 800-631-2154. In NJ, 201-870-4712.

PERKIN-ELMER

3-micron Sigate CMOS ROMs

Utilizing the 3-micron Sigate CMOS process HCMOS II, ROMs with densities of 32k to 256k bits combine NMOS high speed, density, and TTL compatibility with CMOS low operating power. Products available now include SCM23C32 and SCM23C233 4k x 8 (32k) ROMs and SCM23C64 and SCM23C65 8k x 8 (64k) ROMs. Additional family members, planned for introduction in mid-1983, include the SCM23C128 16k x 8 (128k) and SCM23C256 32k x 8 (256k) ROMs. Temp range is −40 to 85 °C, with −55 to 125 °C. Full mil-std 883B screening is optionally available. Pricing in 10k quantity ranges from $4 to $7.20. **Solid State Scientific, Inc,** Commerce Dr, Montgomeryville, PA 18936.
Circle 273

CMOS multiplexed LCD drivers and 32-bit LCD display driver

MM58538, MM58539, MM58540, and MM58548 monolithic LCD devices drive a dot matrix LCD array directly under the control of an external microprocessor. Each device features an onboard oscillator and serial data I/O. 32-bit LCD display driver MM58538 drives up to 8 rows and 26 cols and is expandable to larger displays with added MM58539 that provides 34 more cols. MM58540 drives 32 cols or rows. Two MM58540s will drive a 32 x 32 LCD array. MM58548 drives 16 rows x 16 cols. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 274

16k EEROM programs at 5 V

The 5213 5-V EEROM is organized 2k x 8 bits in a JEDEC standard 24-pin DIP. Device can be used wherever user reconfiguration of nonvolatile program store is needed. It can be written by using either a single 5-V TTL level or 21-V signal. Using the 21-V write capability, the chip is plug compatible with Intel's 2816 EEROM. **SEEQ Technology, Inc,** 1849 Fortune Dr, San Jose, CA 95131.
Circle 275

16k RAM with 70-ns access

Am9128 16k-bit RAM has 2048- x 8-bit organization and is plug compatible with other industry 16k RAMs and 16k EPROMs. Housed in a std 24-pin, 0.6″ wide (1.5-cm) DIP, device uses fully static circuitry, requiring no clocks or refresh to operate. TTL compatible I/Os and operation from a single 5-V supply simplifies system design. Common data I/O pins using 3-state outputs are provided. JEDEC std pinout for byte-wide memories is used. Device is available in commercial and full mil temp ranges. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 276

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

Nothing else measures up.

Our sleek 3½″ Micro Floppydisk system is every inch a Sony. So why would one of the world's most prestigious computer manufacturers decide to make it their standard?

Because in less than half the volume of a regular 5¼″ disk drive you get twice the capacity: 437.5 KBytes.

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And because Sony offers the Auto Shutter™ disk shield system to more fully protect the media.

But most of all, Sony was chosen because our Micro Floppydisk systems are up and running—reliably. And that's the standard against which to measure all other micros.

For more input write Sony Data Products, Department A, Sony Drive, Park Ridge, N.J. 07656. Or call 201-930-6030.

SONY.

Data Products
Sony Communications Products Company

CIRCLE 119

Word alterable 16k-bit EEPROM

ER5816 16k EEPROM features remote programmability and is electrically erasable by word or block, eliminating need for circuit removal for UV exposure. Access time is 300 ns; erase and write times are 10 ms. Organized as 2048 words x 8 bits, the fully decoded EEPROM provides a min 10 years of nonvolatile data retention. Device conforms to JEDEC byte-wide pinout standards and is pin compatible with Intel's 2816 EEPROM. **General Instrument Corp, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.
Circle 277

6-bit ADC gives 100M samples/s

Model TDC1029J ADC guarantees 6-bit performance at 100M samples/s and also provides a full-scale analog input bandwidth of 50 MHz while residing in a 24-pin DIP dissipating a max 1.8 W. Utilizing TRW's Omicron-B™ process and 2-layer metalization, speed and circuit complexity are enhanced to form a commercial 1-micron VLSI circuit. The device operates from a single −5.2-Vdc supply. Digital interface is single-ended ECL compatible. MSB output is differential. The ADC will be available on DIN41612/41494 std Eurocard as the TDC1029E1C. **TRW, LSI Products Div,** PO Box 2472, La Jolla, CA 92038.
Circle 278

Dual-peripheral driver ICs with 500-mA outputs

SN75407 and SN75408 single-chip, dual-peripheral drivers with single-saturating transistors capable of outputting up to 500 mA are provided in 8-pin DIPs. High-gain, single-transistor NPN output structures are used in place of std darlington transistor driver stages. Each DIP also has a copper lead frame, allowing it to dissipate up to 1380 mW continuously in 25 °C ambient temp. The SN75407 is a NAND-logic device, and the SN75408 is an OR-logic device. Both are available for $0.90 each in 100-piece quantities. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220.
Circle 279

High reliability 8k CMOS EEPROMs

HM3008, an 8192-bit CMOS EEPROM organized 1024 x 8, is screened to Class B of method 5004 and quality conformance to method 5005. During standby, power dissipation is 5 mW, while read operations are performed at 0.05 μW/Hz. Device can be erased and byte programmed in-circuit in 1 ms/byte by raising the power supply to 16 V ±1 V and requesting an erase or program operation through TTL level inputs. Device is available in either cerDIPs or LCC packages at $84 in 1000-piece quantities. **Hughes Aircraft Co, Solid State Products Div,** 500 Superior Ave, Newport Beach, CA 92663.
Circle 280

Positive protection for personal computers.

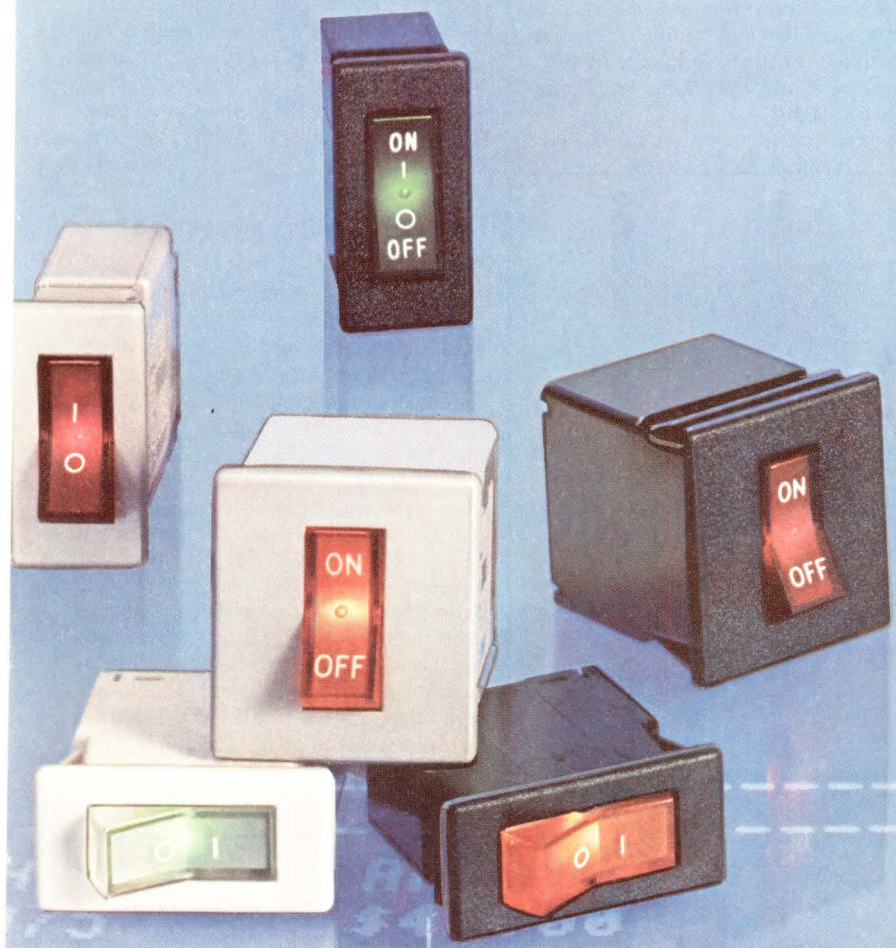
Airpax magnetic circuit breakers.

Whether the surroundings are hot or cold, Airpax magnetic circuit breakers' minimum trip current is not affected by temperature extremes, as is the case with fuses and thermal devices. These "trip-free" breakers won't stay closed on an overload even if the handle is held in the "on" position. Their built-in inertia delay avoids nuisance trip-outs due to transient surges.

Designed to conform with VDE and IEC standards 380 and 435, Airpax SNAPAK® breakers make your product ready for export markets. A wide choice of handle actuations, colors, illumination, terminals and hardware gives you the styling and selection you want. They are tested, listed and qualified under various military, UL, CSA and SEV specifications. Proven performance has made them the choice of leading manufacturers of computers, peripherals, broadcast equipment and machine controllers.

Because they combine the functions of power switching and overload protection and have zero replacement requirements, Airpax breakers are an affordable option to fuse-switch combinations.

For complete specifications, write or call Airpax Corporation, a North American Philips Company, Cambridge Division, Woods Road, P.O. Box 520, Cambridge, MD 21613. (301) 228-4600.



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CAMBRIDGE DIVISION

Logic array evaluation chip

LSI 5220Q evaluation chip for the LSI 5000 series logic arrays is based on a 3-micron double-layer metal HCMOS technology and provides 880 to 6000 gates. It is competitive in speed with ISL, TTL, and LSTTL, and can replace these families in most applications. Traditional 54/74 bipolar and CMOS SSI/MSI users can evaluate the arrays as a VLSI alternative. The chip has 22 common logic functions that include prewired gates with selectable loading conditions, flipflops, ALU, up/down counter, shift register, and I/O buffers. Evaluation kit is $125. **LSI Logic Corp,** 1601 McCarthy Blvd, Milpitas, CA 95035.
Circle 281

Dual-baud rate generators with internal crystal clock

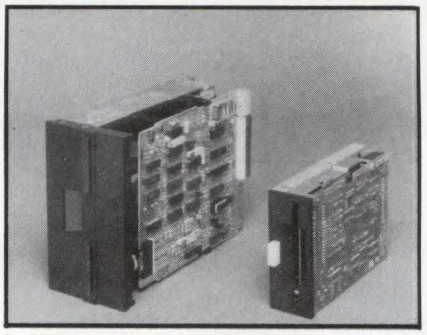
TM1135A/B/C/D are pin compatible and functionally equivalent to most std dual-baud rate generators with or without internal crystals, and are also compatible with UART/USART and ASTRO/USYCRT. Devices can be used as programmable oscillators within crystal frequency range of 3.2 to 7 MHz. Direct oscillator frequency is available along with divide-by-4 as a reference or for other system applications. Resistance weld, hermetically sealed DIP metal package can be screened to MIL-STD-883B. **Oscillatek Corp,** 5755 Foxridge Dr, Mission, KS 66202.
Circle 282

MEMORY SYSTEMS

Half-size Winchester

A reconfiguration of the MiniScribe III 5¼" Winchester disk drive is half the height of std disk drives. Up to 10M-bytes is provided in a single disk. Single-platter, 588-tpi format is used; 306- and 408-cylinder versions are available. Drive provides 6.4M bytes with 85-ms access time or 10M bytes at 120-ms access time. Volume production is scheduled for the first quarter of 1983. **MiniScribe Corp,** 410 S Sunset, Longmont, CO 80501.
Circle 283

3½" microfloppy



Standing 1.6" (4.1 cm) high, the single-sided SA300 3½" microfloppy disk drive provides 500k-byte unformatted capacity, 135-tpi density, and 6-ms track to track access time. Drive's diskette is protected by a hard plastic shell, and the shutter is spring loaded to remain closed until media are inserted. With 80 tracks/surface and 300-rpm speed, the drive achieves 125k-bps (single-density) or 250k-bps (double-density) transfer rates. Evaluation units will be available the first quarter of 1983; production units (under $200 each) are scheduled for the second quarter of 1983. **Shugart Assocs,** 475 Oakmead Pkwy, Sunnyvale, CA 94086.
Circle 284

1M-byte VERSAbus compatible add-in memory

DR-680 1M-byte memory is internally configured as 256k x 39 or as a depopulated 0.5M-byte version. Read access and cycle times are 425 and 535 ns, and write access and cycle times are 190 and 800 ns. The board conforms to the 14.5" x 9.25" (36.8- x 23.49-cm) VERSAboard. It decodes 23 address bits when used with 16M-byte max memory systems. Modules of equal capacity can be 2-way interleaved for 16- or 32-bit transfers. Board operates from 5 Vdc. Battery backup logic is provided. Onboard control and status register allows program control of ECC functions. Single-quantity prices for 1M-byte and 512k-byte versions are $4200 and $2900. **Dataram Corp,** Princeton Rd, Cranbury, NY 08512.
Circle 285

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At Recognition Concepts, Inc., when we designed our real-time image processors, we didn't follow the pack.

RCI's Trapix Series of Real-Time Image Processing Systems were designed around the capabilities of the state-of-the-art 64K RAM chip. This enables the system to be configured with up to 4M bytes of image memory in a compact 10½" chassis. It dramatically reduces storage costs. Many image processing capabilities that were only available in the laboratory are now affordable. And you get the bonus of 4 times the storage.

The Trapix digitizes video signals in real-time: to 8 or 10 bit accuracy for a single frame. Add the optional phase locked loop and time base corrector modules and the system is able to digitize directly from virtually any video source — including video tape and CCD sensors. Add the optional high speed memory interface and data may be read directly into image memory at video rate. Up to four video input sources can share the resources of the system. You get greater flexibility in image acquisition.

The Trapix features a new and unique video rate Pipeline Image Processor (PIP) for full arithmetic and boolean operation between image arrays of 8 or 16 bit precision. While our cini-mode provides you with the display power of a full 2 seconds of real-time video. You get twice the processing power.

Original concepts. New technology. Low price. The Trapix Series of Real-Time Image Processing Systems have left the crowd behind. And implementing our ideas in the beautiful surroundings of Lake Tahoe certainly hasn't hurt.

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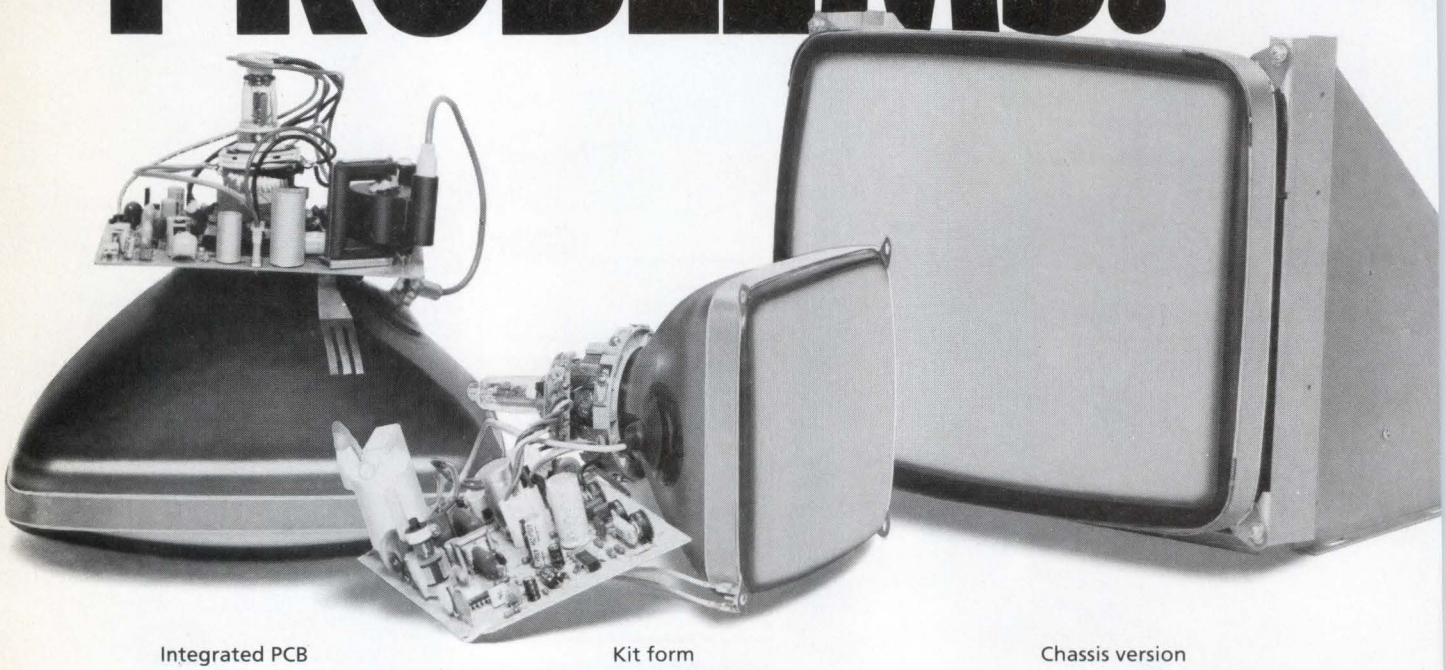
CIRCLE 123

WE SOLVE PROBLEMS!



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CIRCLE 124

SYSTEM COMPONENTS/ MEMORY SYSTEMS

DEC compatible microsystem

RLX1001B DEC compatible microsystem allows a complete LSI-11 system to be built, including processor, 256k-byte memory, and 2 disk drives, for less than $10,000. The system has a 10.3M-byte 5¼" Winchester, a 1M-byte 8" RX02 compatible floppy, a built-in Q-bus card cage with 8 quad-height slots, and a 7" (18-cm) desktop or rackmountable enclosure. LSI processor, memory, and interface cards are available. LSI-11 users can swap programs/data directly between existing systems and the RLX1001B through the RX02 floppies. Base price is $7500. **Charles River Data Systems, Inc,** 4 Tech Circle, Natick, MA 01760.

Circle 286

Streaming tape drive

EMISTREAMER 9800 half-inch (1.3-cm) open-reel IBM compatible tape drive is autoloading and comes with power supply and formatter. Features include 25-ips and 100-ips streaming speeds, 15.3M-byte max unformatted capacity, and a capstanless tape path that eliminates contact with the oxide coating—except at the R/W head and the sapphire tape cleaner. Suitable for desktop use or for mounting side by side with Winchester disk subsystems, the tape uses IBM/ANSI 1600-bpi PE format. **THORN EMI Datatech Ltd,** Spur Rd, Feltham, Middlesex, England, TW14 OTD.

Circle 287

Q-bus compatible Winchester with tape backup

DSD 890 31.2M-byte Winchester system with 1/4" tape backup emulates 3 DEC RL02 cartridge disks and a TSV05 1/2" tape. System takes up 80% less rack space and utilizes a 16.25M-byte 1/4" tape for low cost archival storage. Fully compatible with DEC LSI-11 Q-bus minicomputers, system operates with RT, RSX, TSX, RSTS, and UNIX operating software. It supports 22-bit addressing and all DEC backup utilities. Onboard bootstrap, 32-bit error correction, and simultaneous Winchester and tape operation without throughput degradation are featured. Price is $9895 in single quantity. **Data Systems Design, Inc,** 2241 Lundy Ave, San Jose, CA 95131.

Circle 288

VERSAbus compatible 128k add-in memory

MM-68000C add-in memory for VERSAbus microprocessor systems provides 128k bytes of storage and realtime calendar. Board comes with rechargeable batteries with 2-week data retention or with non-rechargeable batteries having 1-yr data retention. Cycle and access times are 220 ns with no refresh delays. Module selection is on 1000 (hex) boundaries that are switch selectable in the 16M-byte address field. Switch-selectable write protect is included with 8k-byte boundaries. User can substitute a 32k-byte block of CMOS RAMs with 2716 EPROMS. Price is $2350. **Micro Memory, Inc,** 9436 Irondale Ave, Chatsworth, CA 91311.

Circle 289

Closed-loop servo 5¼" drive with 40-ns access

Three 5¼" Winchesters are configured as triple-disk 40M-byte model 5640, dual-disk 26.68M-byte model 5426, and single-disk 13.34M-byte model 5213. A closed-loop servo positioning scheme positions to within ±25 μin. A rotary torque dc motor servo is also used. Onboard microprocessor controls all electromechanical operations and functions. Track density is 690 tpi. Each track has 32 sectors, and each sector holds 256k bytes of formatted data. Rotational speed is 3600 rpm. Recording density is 9650 bpi. Transfer rate is 5M bps. Average latency is 8.3 ms. **Computer Memories Inc,** 9216 Eton Ave, Chatsworth, CA 91311.

Circle 290

Half-inch magnetic tape subsystems for small computers

Series 1012 tape subsystems allow small computers to read/write half-inch (1.3-cm) 9-track magnetic tape. Data format meets IBM/ANSI/ECMA and ISO standards. The tapes combine "TMS Virgo" IDT model 1012 tape transport with an intelligent formatter controller. System operates at 12.5-ips, start/stop, 1600-cpi density, and provides 20k-byte/s average data transfer rate, and 250k bytes during buffer load. A 2400' (732 m) 10.5" (26.7-cm) reel accommodates over 40M bytes of data. Price is $6995. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.

Circle 291

High density tape subsystem

"Avalanche" 2920 dual-density 1600/6250-bpi, 50-ips, start/stop tape subsystem integrates both tape drive and formatter/controller into 1 std rack-mountable package. It features a CAD/CAM modeled tape transport, microprocessor adaptive controls, and extensive LSI. Motion is tightly controlled for reliable GCR recording. A mechanical tape buffering system handles both high density GCR and auto-threading. Subsystem uses one-third the card space typically found in similar GCR devices. MTBF is 5k h. Evaluation units will be available in April 1983. **Storage Technology Corp,** 2270 S 88th St, Louisville, CO 80028.

Circle 292

0.5M-byte MULTIBUS memory card with ECC

BLC-0512B 512k-byte RAM card for MULTIBUS or BLC series computers provides ECC with check bit generation and storage, syndrome bit generation, and error correction. Card utilizes 64k dynamic NMOS RAMs and is available in 128k- and 256k-byte versions. It plugs directly into any IEEE 796 backplane. The card requires 5 Vdc; jumper points are provided for battery backup. List price is $1967 for each 512k-byte board, and $1598 for each 256k-byte board. Quantity discounts are available. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 293

New Amdek 3" micro-floppydisk drive system!

AMDISK-III . . . the engineer's choice:

- New 3" hard plastic encased diskette.
- Up to 1 megabyte storage. (unformatted)
- Plug-in compatible with 5¼" drives.
- Compatible with - IBM-PC.

Specifications

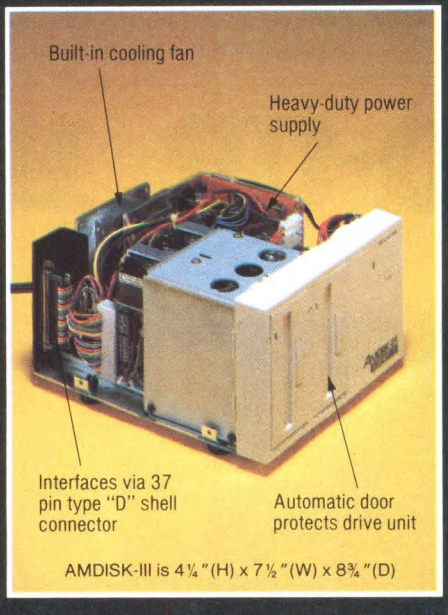
	Unit	Double Density
Capacity		
Unformatted Per Surface	Bytes	250K
Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	1
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10^{-9}
Hard Error		10^{-12}
Seek Error		10^{-6}
Media	3-inch Cartridge	
Drive Interface	Plug Compatible with 5.25 inch FDD	

External Interface

Connector: 37-pin "D" shell connector

Pin No.	Signal	Pin No.	Signal
1-5	Unused	13	Write data
6	Index	14	Write enable
7	Motor enable C	15	Track 00
8	Drive select D	16	Write protect
9	Drive select C	17	Read data
10	Motor enable D	18*	Select head 1
11	Direction	19	GND
12	Step pulse	20-37	GND

*drives are single head



AMDISK-III is 4¼"(H) x 7½"(W) x 8¾"(D)

Evaluation samples $480

Includes two-drive Amdisk unit with built-in power supply, 4 diskettes and application literature . . . Call (312) 364-1180.

The AMDISK-III Micro-floppydisk System is an engineering breakthrough in disk size, storage capacity, media protection and user convenience. Designed for microcomputers for many applications, the Amdek system is ruggedly constructed to provide years of trouble-free operation. Warranty is 90 days (parts & labor).

Put the new AMDISK-III to test . . . its recording format, data transfer rate and disk rotation speed are compatible with 5¼" floppydisk drives. Call, or write for evaluation samples at only $480.00 . . . or circle the reader service number for full technical details.

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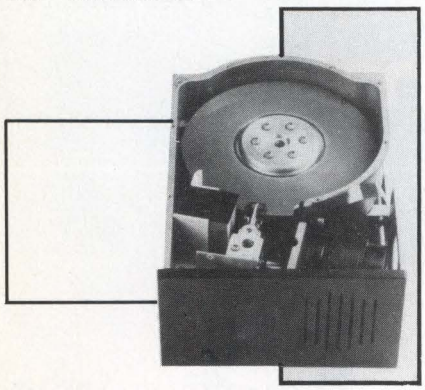
CIRCLE 127

ST400 compatible 5¼" Winchesters



5006 series 5¼" Winchesters are plug compatible with the ST400 family. They are provided as the single-platter 5006/1 ($585) with 6.38M bytes, the 2-platter 5006/2 ($695) with 12.76M bytes, and the 3-platter 5006/3 ($850) with 19.14M bytes. MTBF is 11k h; component life is estimated at 6 years. Average access time is 70 ms. A microprocessor controlled buffered seek is included. Power consumption is 25 W. **Irwin Olivetti, Inc,** 2000 Green Rd, Ann Arbor, MI 48105.
Circle 294

3.9" Winchester for IBM PC

DPR series Winchester disk drives for the IBM PC utilize SyQuest Technology's 3.9" (9.9-cm) drive, with a choice of fixed or removable cartridge. Drive provides full 5M-byte formatted storage. It consumes no more power than the IBM PC floppies, allowing the disk to be mounted in the space allotted for the second floppy. An external self-contained version with its own power supply is also available. Controller card has built-in ECC. Software includes BIOS, driver, and utilities to ensure full compatibility with existing PC DOS and CP/M-86. Prices start at $1450. **IDE Associates Inc,** 44 Mall Rd, Burlington, MA 01803.
Circle 295

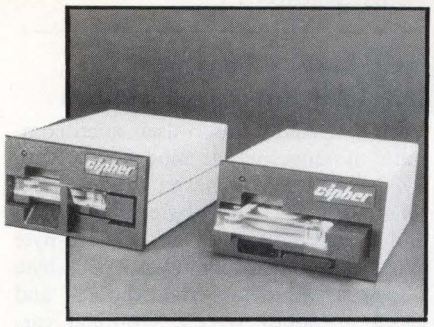
5¼" streaming cartridge tapes

Scorpion series 5¼" streaming cartridge tape drives utilizes the industry std QIC II Sidewinder interface. Power supply requirements are 12 or 5 Vdc. Both the 20M- and 45M-byte tape drive versions are available with intelligence that provides high throughput, streams at 30 or 90 ips, and eliminates inter-record gaps. Serpentine recording allows 4 (20M-byte unit) or 9 (45M-byte unit) data tracks to be written in continuous motion. Drives are priced from $800 in OEM quantities, and will be available in the second quarter of 1983. **Archive Corp,** 3540 Cadillac Ave, Costa Mesa, CA 92626.
Circle 296

Board adds 512k dynamic RAM

Error detection/correction and enhanced noise immunity are std features of the 128k to 512k dynamic RAM board. MULTIBUS compatible, board has max access of 275 ns. It corrects any single-bit error and detects all double-bit errors, and can be strapped to interrupt on any error. Input port can be read to determine the type of error and to identify the failing RAM chip. Board decodes the full 24-bit address bus for a 16M-byte system-wide memory. Onboard refresh arbitration minimizes wait states. The 100-up quantity price is $825 for 128k and $1725 for 512k. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61820.
Circle 297

Streaming cartridge tape drives

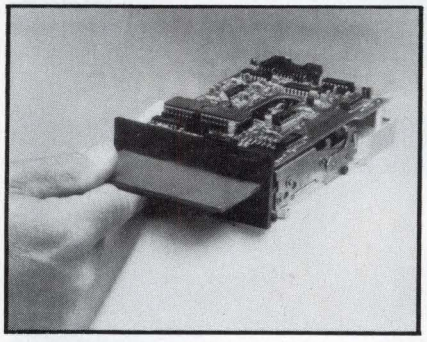


Model 540-CT 45M-byte 5¼" streaming cartridge tape drive allows front loading of a std size tape cartridge by turning the cartridge sideways for insertion. Compatible with QIC-02 interface, unit can be installed in any system using the same mounting holes and having the same physical dimensions as std 5¼" floppy or rigid disks. Model 440-CT 8" 45M-byte streaming cartridge tape drive also provides QIC-02 compatibility. Both drives (approx $850 each) will be available for volume delivery in July 1983; evaluation units will be available in February 1983. **Cipher Data Products, Inc,** 10225 Willow Creek Rd, PO Box 85170, San Diego, CA 92138.

Circle 298

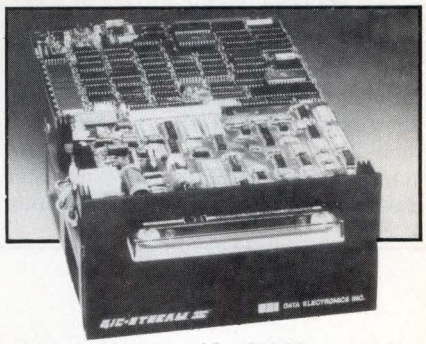
3½" microfloppy disk drive

TM35 Microline® disk drive provides 875k bytes on 2 sides of a 3½" diskette, 85-ms data access, and 3-ms track-to-track speed. TM35-2 is compatible with 5¼" std interface, and provides 40 tracks/side, double-sided recording, 250k-bps transfer rate, and 500k-byte capacity. TM35-4 is compatible with the Sony OA-D30V microfloppy drive interface, software, and diskette, and has double-sided date recording. TM35-4 features 7610-bpi recording density, 135 tpi, and 70 tracks/side. TM35-2 model features 6255 bpi and 135 tpi. Both models use FM/MFM recording. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311.



Circle 299

Streaming 1/4" tape uses QIC-02 interface standard



QIC-STREAM II provides 20M bytes of formatted data storage on a 450' (137-m) ANSI proposed std 1/4" tape cartridge (*Computer Design,* Nov 1982, p 3). Unit employs a dual microprocessor based formatter/controller, a basic drive mounted on a solid diecast frame, positive head positioning mechanism, and multiread thresholds. Either 30- or 90-ips tape speeds are available. Host protocols are via an 8-bit bidirectional bus on which command, status, and data are transferred. Data density is 8k bpi. OEM quantity price is $798. **Data Electronics, Inc,** 10150 Sorrento Valley Rd, San Diego, CA 92121.

Circle 300

3½″ microfloppy mass storage disks

Three 3½″ floppy disk systems, compatible with most HP small computers, include the HP 9121S 270k-byte single-drive system ($1200), HP 9121D 540k-byte dual-drive system ($1775), and HP 9133A single-package 4.6M-byte Winchester disk and 3½″ floppy ($4975). Rotating at 600 rpm and transferring 17.8k bytes/s from the disk to the host computer, the single-sided media provide approx the same capacity as most double-sided 5¼″ flexible disks. A 2-element media protection system and HP software packs are provided. Contact local **Hewlett-Packard** sales offices. **Circle 301**

COMPUTERS

Multi-user systems with selectable Winchester storage

Vector 5E series multi-user microcomputer systems include model 5005E with 5¼″ 5M-byte Winchester drive, model 5010E with 5¼″ 10M-byte Winchester, and model 5032E with an 8″ 32M-byte Winchester. Each system has a 630k-byte floppy drive, detached keyboard, and green phosphor screen. Optional cartridge SafStor tape drive is recommended for backup and archival storage. A 6-MHz Z80B microprocessor and 128k RAM are provided. Extended CP/M provides print spooling for simultaneous data entry and printing. A parallel and serial printer can be operated simultaneously from different terminals. **Vector Graphic Inc,** 500 N Ventu Park Rd, Thousand Oaks, CA 91320. **Circle 302**

Z80A, CP/M 2.2 based computer

AMIGO™ CP/M 2.2 based computer system uses a Z80A microprocessor with 64k-byte RAM as a CPU and I/O controller, and a 6502 microprocessor to control 44k-byte RAM handling the bit-mapped graphics and char display. System features a 12″ (30-cm) nonglare display and is available with dual 5¼″ floppy drives with up to 400k-byte formatted storage. Dual floppies with 800k bytes and a 5M-byte Winchester are optional. An 83-key low profile detachable keyboard is featured. Parallel printer port interfaces to a dot matrix, 80- or 132-col impact printer with graphics capabilities. Pricing begins at $2395. **Ontel Corp,** 250 Crossways Park Dr, Woodbury, NY 11797. **Circle 303**

Graphics/image processor

Model 2800-32 image processing system for sequential processing of RGB images has up to six 8-bit banks of 512 x 512 memory with program selectable resolutions of 512 or 480 lines and 512 or 640 pixels/line. A video digitizer and an MC68000 microprocessor card with up to 512k-byte program memory (loadable from the host computer) are included. Bit-slice processor with up to 4k of 64k-bit user loadable microcode for system control and graphics processing is provided. Pipeline image processor with extensive lookup tables, a video rate of 8 x 8 hardware multiplier, a 16 x 16 ALU, and an input stage for digitizer images are featured. Prices start at $25,000. **Grinnell Systems Corp,** 6410 Via Del Oro Dr, San Jose, CA 95119. **Circle 304**

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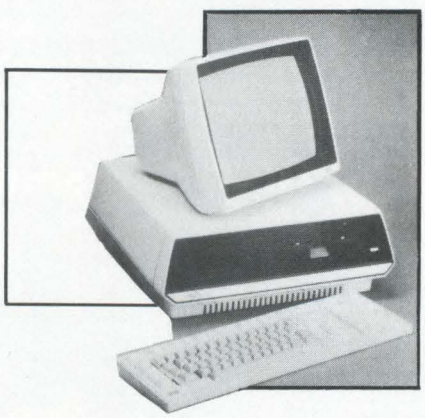
16-bit small computers

Two 16-bit IBM PC compatible personal computers—a portable or desktop system—include a 320k-byte half-height diskette drive, green phosphor monitor, 128k-byte memory, and serial and parallel ports. MS DOS, BASIC with graphics commands, and a spread sheet software package are also provided. A second half-height floppy diskette and/or a 10M-byte hard disk can be directly added. Two floppies and the hard disk can be directly installed with no external attachments to upgrade the desktop system. Memory can be expanded from 128k to 512k bytes without using

expansion slots. A 110-W switching power supply, an 8088 microprocessor, and an optional 8087 floating point coprocessor are used. Prices range from $2395 to $4495. **Corona Data Systems, Inc,** 31324 Via Colinas, Westlake Village, CA 91361.

Circle 305

16-bit micro

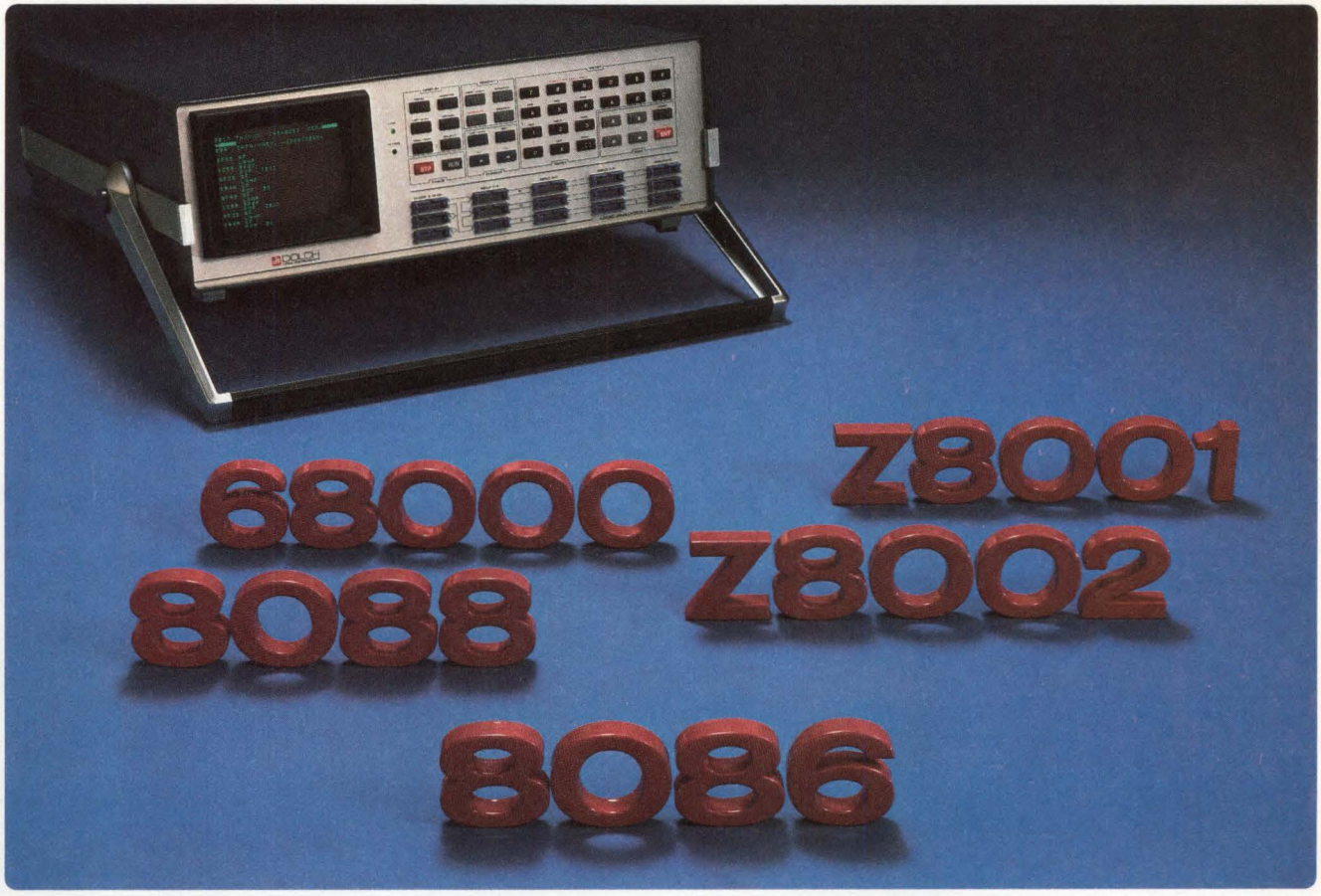


Altos 586 microcomputer has 5-user (upgradable to 8-user) capability. Interfaces to Ethernet™ and Altos-Net™ networks are provided. The 16-bit micro uses the Intel 8086 processor running at 10 MHz and has 256k or 512k RAM, expandable to 1M byte. An ergonomically designed terminal is available. Software includes XENIX/UNIX and a business software package. Battery backed clock and calendar, MULTIBUS architecture, proprietary memory management, power failure detection, and internal distributed intelligence are featured. Six RS-232 ports, upgradable to 10, are supported. Prices range from $4990 to $7990. **Altos Computer Systems,** 2360 Bering Dr, San Jose, CA 95131.

Circle 306

Dolch.

advanced logic analysis



Personality Plus for 16 bit microprocessors

The Dolch 4850A Logic Analyzer has what it takes to analyze your 16 bit microprocessor.

Friendly, yet powerful, personality

Our Trace Module connects the 4850A directly to your 16 bit operating system. Signal interfacing and clock formatting are already done. (In the 68000 and 8086/88 systems, the Trace Module separates instructions executed by the microprocessor from all of those that were "prefetched" into the instruction queue.) The 4850A then disassembles and displays the operations in assembly language mnemonics. It's that easy.

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300 MHz Sampling: Besides having 48 channels, for state or timing analysis, you can overlay 16 more at 300 MHz. The 3.3 ns resolution lets you spot short glitches and resolve critical timing sequences.

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Area Tracing: You can limit data tracing to specific areas of interest in your system's memory — there's no need to record unwanted data.

Competitive Price: Price is a real plus over *any* other analyzer.

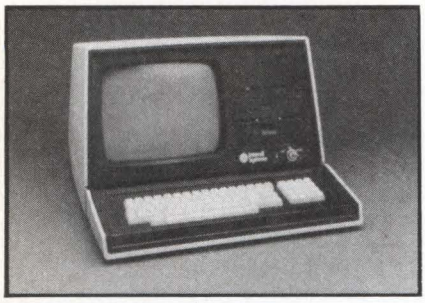
For more reasons why the 4850A is ideal for 16 bit (and 8 bit!) microprocessors see a demonstration. Call (800) 538-7506; in California, (408) 998-5730. Or write: 230 Devcon Drive, San Jose, CA 95112.

dli DOLCH
LOGIC INSTRUMENTS

Circle 132 for demonstration

Circle 170 for more information

Microcomputer with STD bus expansion



ISB 80/85 standalone microcomputer has built-in, slimline card cage that allows the STD bus based system to be user customized. System comes with either Z80 or 8085 CPU cards; 64k-byte RAM card; 12″ (30-cm) CRT; detachable keyboard; and either two 5½″ dual-sided, dual-density floppy drives or one 5¼″ floppy, and one 10M-byte 5¼″ Winchester. Up to 6 STD bus cards can be added. Fully integrated ISB-ICP/M CP/M 2.2 based OS is supplied. Unit price range is $5990 to $8990. OEM pricing is available. **Intersil Systems, Inc, a sub of General Electric Co,** 1275 Hammerwood Ave, Sunnyvale, CA 94086. **Circle 307**

CP/M and MP/M computer

QDP-300 computer features a 6-MHz Z80B CPU, cache memory for disk track buffering, a Z80A DMA processor for high speed data transfer, 128k-byte RAM, two 8″ double-sided double-density floppy drives, internal sensor, S-100 bus, and CP/M. Options include a 10M- or 15M-byte 5¼″ hard disk, 256k-byte RAM, up to 6 serial ports, and MP/M II operating system. Standard 8-bit configuration is easily upgradeable to an optional 16-bit capability that uses an 8086 processor. **Quasar Data Products (QDP) Computer Systems,** 10330 Brecksville Rd, Cleveland, OH 44141. **Circle 308**

16-bit industrial microcomputer

MB86I integrated microcomputer system is housed in an airtight aluminum enclosure that contains an 8-slot IEEE 796 card cage, 10-MHz 8086 processor with 128k parity RAM, and serial/parallel I/O. A 12″ (30-cm) alphanumeric display with 64-key alphanumeric keyboard is provided. Push/pull cooling across the card cage and thermal heat exchanger are included. Power supply is 200 W. Price is $6795; OEM discounts are available. Delivery is 30 days ARO. **Comark Corp,** 257 Crescent St, Waltham, MA 02154. **Circle 309**

16/32-bit microprocessor for virtual machine applications

MC68010 16/32-bit microprocessor can store the complete internal processor state upon receipt of a memory fault. The processor can recover this state later and continue processing after the fault condition is resolved. One operating system supervises any number of subordinate operating systems, allowing multi-users to run different operating systems and virtual I/O to be supported.

(continued on page 228)

How do Unibus* users spell peak I/O rate relief?

High speed data acquisition can be a real headache. Especially during peak I/O rates when transfer can exceed the CPU's capacity and key bits of information go off in thin air.

So we developed a DR11-W module. First for the Unibus. Now for the Q-Bus. Both feature our exclusive DMA Throttle that efficiently regulates data flow down to average rates to maximize overall CPU performance. But that's not all.

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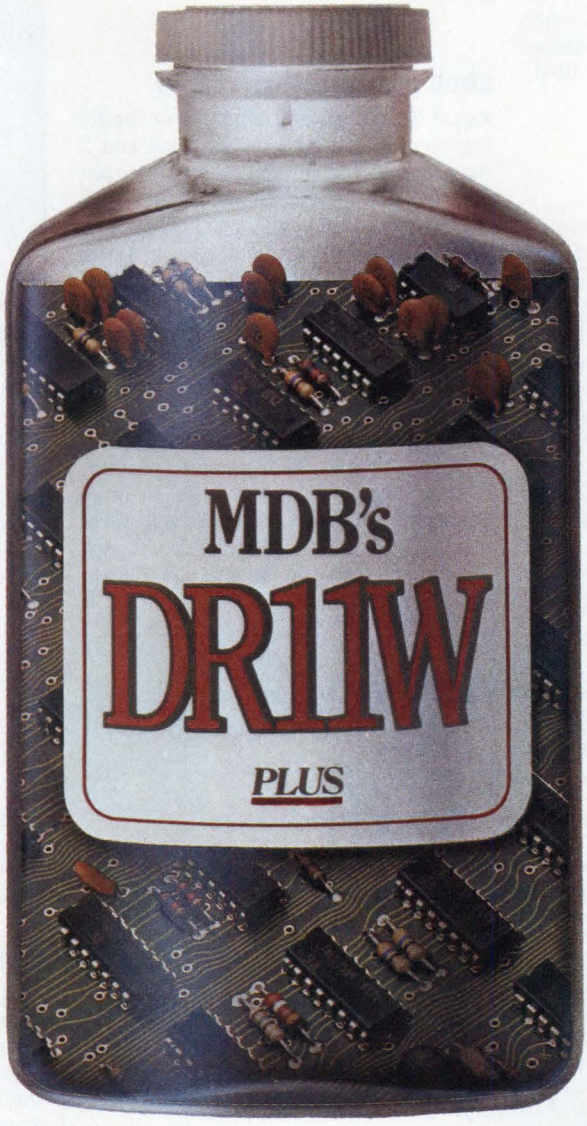
- Edge mounted LED's to illuminate performance status
- Micro-sequencer driven, self-test diagnostics
- Long lines capability
- Switch selectable 22-bit addressing (Q-Bus)



- Bus Address Extension for memory transfer throughout the 4 megabyte range (Q-Bus)
- Switch selectable, 4-level or single level interrupt arbitration (Q-Bus)
- Compatibility with 16, 18 and 22-bit backplanes (Q-Bus)

This high speed, digital input/output device is prescribed for such typical applications as:

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Circle 135 For LSI-11-171 for PDP-11

(continued from page 226)

Delayed bus error signal can also abort a bus cycle to allow error detection/correction without impacting peformance. User programming model, supervisor programming model, and 2 alternate function code registers are provided. Samples are $90 each in quantities of 100. **Motorola Inc, MOS Microprocessor Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 380

CMOS STD bus cards

A processor card based on the 80C85A CPU, a 16k-byte-wide memory card, and a general purpose interface card for the STD bus have an op temp range of −25 to 85 °C and a storage temp range of −40 to 100 °C. Gold-plated sockets, jumper posts, and plugs are included. The 78C05 processor card ($295) accommodates 8k-byte CMOS EPROM and 4k-byte CMOS RAM. 2k bytes of RAM and an edge connector are included. The 77C02 16k memory card ($175) handles 16k bytes of either EPROM or RAM, or 8k bytes of each. Its eight 24-pin sockets accept 2k-byte EPROMS or 2k byte-wide CMOS static RAMs. The 75C07 interface card ($260) features 24 bidirectional I/O lines controlled by three 8-bit R/W ports. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.
Circle 310

CMOS microprocessor family

R65C00 8-bit CMOS microprocessor family incorporates 12 new instructions and 2 new addressing modes. R65C02 is pin compatible with the std 6502 and requires an external clock; R65C102 has a self-contained oscillator; R65C112 operates with a slave clock for multiprocessing applications. Peripherals will include peripheral interface adapter (PIA), PIA with 16-bit counter/timer, ACIA, and static RAM, ROM, and EPROM. Improved bit manipulations, including set/reset memory bit and branch on bit set/reset, lead to 20% memory requirement reduction. Price is $4.90 in large volumes. **Rockwell International, Electronic Devices Div,** 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 311

PERIPHERALS

Low cost VDTs emulate 18 systems

Ampex D150 and D175 video display terminals come with a 32k-bit EPROM socket that allows modifications/additions to the std firmware. D150 ($849) provides a 256-char set that can be displayed double wide and double high; double wide; or double high. Split-screen capability with vertical scrolling, and smooth and jump scroll modes are provided. D175 ($869) provides all features of the D150, and also includes an ergonomically designed typewriter style keyboard. Both terminals provide data code, escape sequences, control codes, and emulation of 18 comparable systems. Data format is 24 lines x 80 chars; char format is 6 x 8 dot matrix in a 7 x 10 field. RS-232-C asynchronous and serial printer interfaces are included. **Ampex Corp,** 401 Broadway, Redwood City, CA 94063.
Circle 312

Digital color plotter

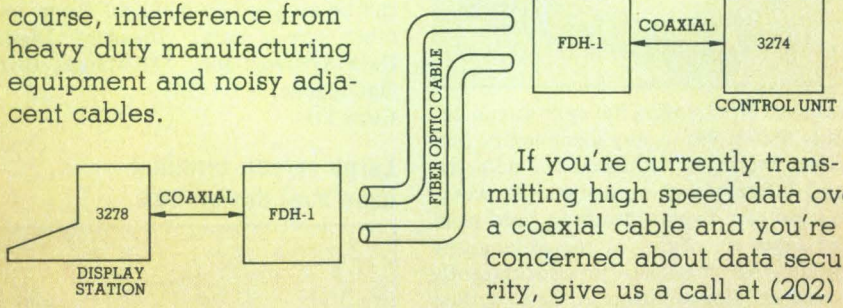
Digital color plotter model VP-6801P utilizes either 6-fiber, ball-point, or plastic tip pens to generate color impressions over a plotting area of 10″ (25 cm) along the X axis and 7.2″ (18.3 cm) along the Y-axis. Writing speed is 16 ips. Unit accepts ASCII 8-bit parallel GPIB, or RS-232-C interfaces. Price is $1995. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094.

Circle 313

Protect your sensitive IBM data with our new Fiber Optic Link

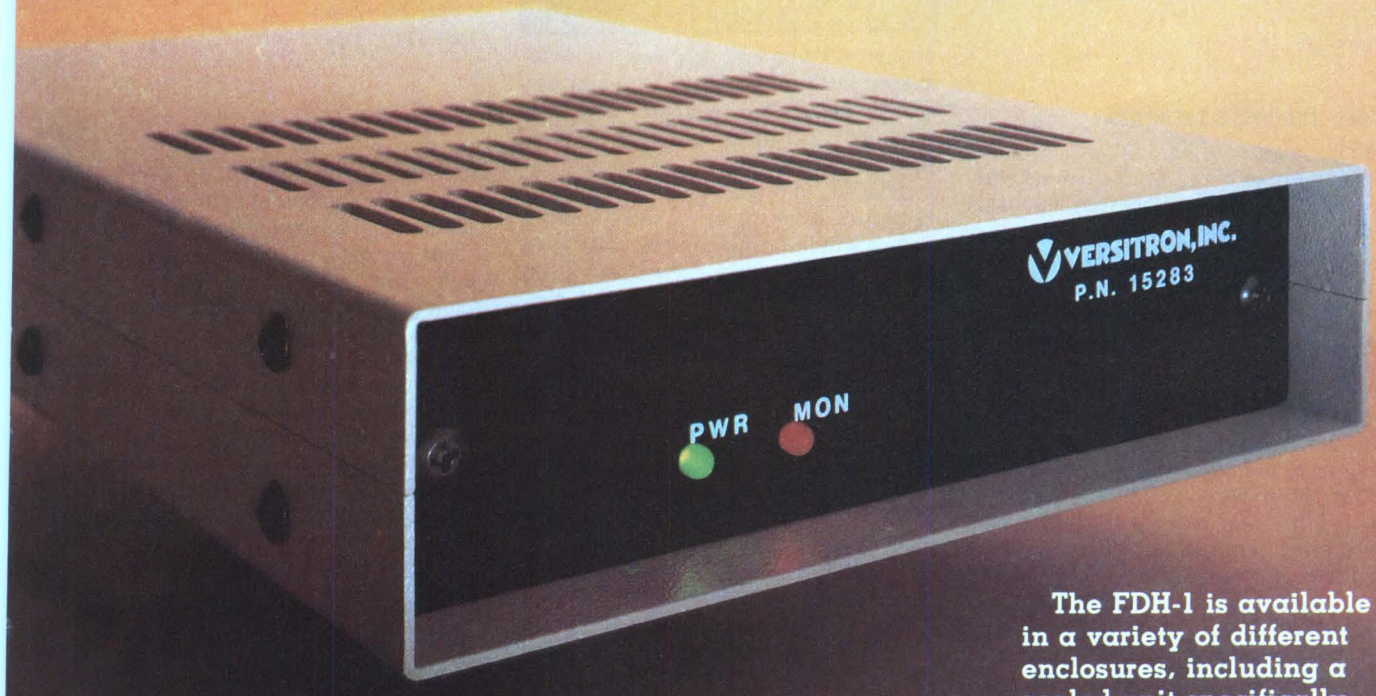
- **Plug compatible with IBM series 3250, 3270A, and 3270B equipment.**
- **Replaces coaxial cable with fiber optic cable.**
- **Up to 1 Km operating range — virtually immune to electromagnetic interference.**

Versitron's FDH-1 (fiber optic digital hybrid) was designed to replace the coaxial transmission path in systems equipped with the IBM 3250 or 3270 series equipment. The simple installation of a fiber optic link provides two very important benefits to the user. First of all, the security level of the transmission link is greatly improved since fiber optic cables are inherently immune to conventional wiretapping techniques. Secondly, the system operating capability will be enhanced since fiber optic cables are impervious to virtually all types of electromagnetic interference. This includes, of course, interference from heavy duty manufacturing equipment and noisy adjacent cables.



Versitron's FDH-1 combines the high speed capabilities of a coaxial cable with the inherent advantages of a fiber optic cable. By interfacing directly to the coaxial cable, the FDH-1 appears totally transparent to the rest of the system; thus eliminating any operating restrictions.

If you're currently transmitting high speed data over a coaxial cable and you're concerned about data security, give us a call at (202) 882-8464 and get all of the details on how our FDH-1 will not only protect your data; but may also actually increase the operating efficiency of your entire system.



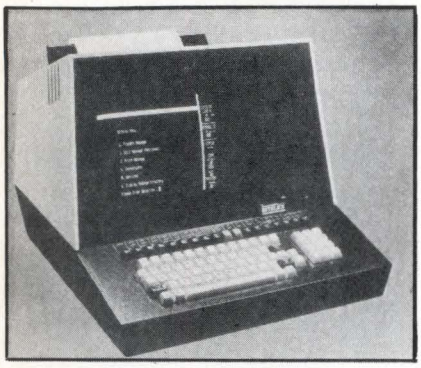
The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

VERSITRON, INC.

6310 Chillum Place, N.W., Washington, D.C. 20011, TEL: (202) 882-8464
TWX: 710-822-1179

CIRCLE 136

Communications workstation



BITELEX workstation has split-screen display that monitors any incoming or outgoing messages. Designed for domestic and international networks, the workstation can display, transmit, and print messages in single- or mixed-language mode. All messages are permanently saved on floppy diskette. Basic system ($3500) contains a 12″ (30-cm) CRT, ASCII keyboard, 80-cps impact printer, single-board control unit with 64k-byte RAM and 16k-byte PROM, 2 serial communications ports with built-in modems, a parallel interface port, and a multitasking central program. **International Digital Electronics Associates, Inc,** 6 Westchester Plaza, Elmsford, NY 10523.
Circle 314

Code loadable terminal

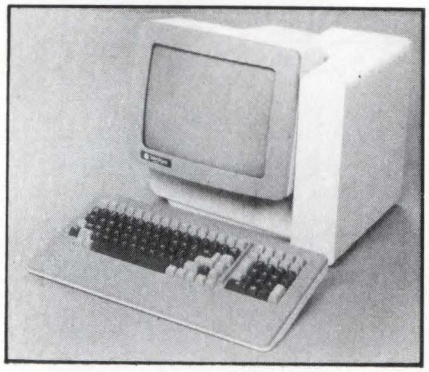
Model 7 user configurable ANSI compatible editing terminal can be loaded with over 100 alternate control sequences and up to 64 alternate key codes. The $1295 unit can emulate asynchronous terminals and is compatible with virtually all asynchronous computers or operating systems. It accepts up to 32 variable length dynamic functions and offers 68 selectable operating parameters. Two-page display memory can be expanded to 4 pages, either volatile or nonvolatile. Display format is either 48 or 96 80-col lines, up to 255 cols. Four char sets, RS-232 ports, and choice of CRT sizes and phosphors are available. **Research Inc, Teleray Div,** PO Box 24064, Minneapolis, MN 55424.
Circle 315

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Low cost color terminal

Viewpoint/Color terminal, priced at less than $1200, can run applications written for the ADDS Regent 40 and 60, and the ADDS Viewpoint/60 terminals without software modification. Similar in use to std alphanumeric terminals, the Viewpoint/Color also features variable tilt and swivel screen, glare reduction, and low profile keyboard. Red, green, blue, magenta, cyan, yellow, black, and white can be assigned to highlight forms and other screen data. **Advanced Digital Data Sytstems Inc,** 100 Marcus Blvd, Hauppauge, NY 11788.
Circle 316

Large screen terminal uses oval design box

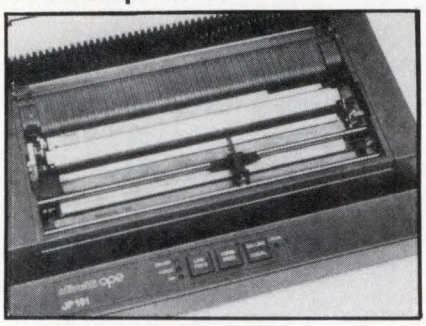


Model 970 terminal features an oval-shaped enclosure with 14″ (36-cm) CRT screen, detachable keyboard, and side-mounted electronics that include logic board and power supply. Silent air flow system in the side enclosure releases heated air at the top of the side-mount to reduce temp. Terminal meets ANSI X3.64. CRT provides black letters on green phosphor tiltable screen. Price is $1495. **TeleVideo Systems, Inc,** 1170 Morse Ave, Sunnyvale, CA 94086.
Circle 317

Low cost color printer

Model 315 color printer has a 4-hammer head design with a special rotating platen, with each of the 4 hammers printing 1 of 4 primary colors. Over 30 possible shades can be printed in a single pass of the printhead. This single-hammer/single-color design prevents color bleeding and contamination of the ribbon that can be caused by ink residue left on the hammer. The printer operates at 50 cps for both char and color graphics printing. Rated graphics throughput is 200 cps. Retail price is $599. **Transtar, div of Omega Northwest, Inc,** Box C-96975, Bellevue, WA 98009.
Circle 318

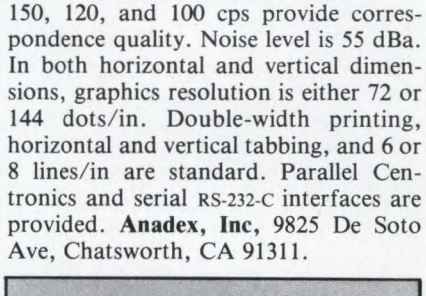
Low cost ink jet printer for desktop micros



JP101 dot-matrix printer, operating noise-free at 80 cps, consists of a single PCB, power supply, and mechanical assemblies for head and paper movement. It measures 4.5″ x 15″ x 10″ (11.4 x 38 x 25 cm). Draft quality alphanumerics are printed at 10 cpi over 80 cols in a 7 x 7 matrix, 12 cpi over 96 cols in a 7 x 7 matrix, or 18.25 cpi over 146 cols in a 7 x 5 matrix. Bit-map graphics are 110 x 110 dots/in, with 880 dots/8″ (20-cm) line. Printhead moves horizontally by dc motor and encoder, and vertically by a stepper motor. An 8-bit parallel interface, with optional RS-232-C or current loop interfaces, is provided. **Irwin Olivetti, Inc,** 2000 Green Rd, Ann Arbor, MI 48105.
Circle 319

Multimode dot matrix printer

DP-9625A, dual-pass dot matrix printer, a member of the Silent/Scribe family, has a max speed of 200 cps in data processing mode and 50 cps in near letter quality mode. Intermediate speeds of 150, 120, and 100 cps provide correspondence quality. Noise level is 55 dBa. In both horizontal and vertical dimensions, graphics resolution is either 72 or 144 dots/in. Double-width printing, horizontal and vertical tabbing, and 6 or 8 lines/in are standard. Parallel Centronics and serial RS-232-C interfaces are provided. **Anadex, Inc,** 9825 De Soto Ave, Chatsworth, CA 91311.



Circle 320

New...
Intelligent Interfaces

To your host CPU our Winchester Disk backup looks just like your Winchester Disk.

Now, costly interface designs are eliminated when you specify EPI's STR®-Stream. That's because this compact, reliable 1/4" cartridge incremental recorder has a system designed interface that emulates both the power requirements and interfacing of Winchester disks. Interfaces available include SA1000, ST506, PRIAM, and DEI Funnel* look-alikes.

STR®-Stream offers the highest data integrity (< one soft error in 10^9 bits), and unit-to-unit compatibility of any recorder in its class. To achieve this, it utilizes a wide write track, narrow read track, read-after-write circuitry and CRC verification.

The recorder stores up to 17 Mbytes (unformatted) on a DC-300XL cartridge, yet takes up no more physical space than an 8" floppy.

Each STR®-Stream comes complete and ready to plug into your compatible controller. Domestic U.S. price is less than $1,000 in OEM quantities.

EPI, with more than 10 years experience moving tape, has the technology and resources to back you and your Winchester disks.

For complete information on STR®-Stream, write to Electronic Processors, Inc., P.O. Box 569, Englewood, CO 80110. Phone (303) 761-8540.

Let EPI remember for you.

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E2/1

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CIRCLE 137

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CIRCLE 138

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If you're looking for a smart ANSI compatible terminal, the NABU 3100 is a very shrewd choice indeed. It's a surprisingly economical package, and it's packed with dozens of the most wanted features.

Features like a buffered edit mode, 4 character highlighting attributes, double-width characters, 16 user programmable string keys, host/user writeable status line and split screen are all standard.

And we haven't overlooked the consideration of operator comfort. The NABU 3100's ergonomic design incorporates a detached typewriter-style keyboard with audible key click, a time saving auto key repeat, a 14-key numeric keypad, smooth scroll and a 12-inch non-glare screen, available with black/white, green or amber display.

Also available, the NABU 3100/GX. Our smart, high performance line graphics terminal. It incorporates all the features of the NABU 3100, delivers the same excellent price/performance ratio and gives you a Tektronix™ Plot 10® software compatible graphics package as well.

These two smart terminals are a shrewd choice for anyone who wants the combination of top performance and top value. For more information on NABU 3100 and NABU 3100/GX, call us or your local NABU terminal distributor.

The NABU 3100/GX. Our new smart high performance graphics terminal.

NABU **COMMERCIAL TERMINALS**
(Formerly Volker-Craig)

NABU MANUFACTURING CORPORATION, COMMERCIAL TERMINALS

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14623
☎(716) 475-1221

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Waterloo, Ontario, Canada
N2J 3H6☎(519) 884-9300
Toronto☎(416) 456-2070
Telex: 069-55327

United Kingdom
William Olds Estate, Tolpits Lane, Watford
Hertfordshire, England WD1 8XL
Rickmansworth☎09237-71378
Telex: 895-6082
Northern Office: 50 Flixton Road, Urmston,
Manchester M31 3AB☎061-747-4613

Distributors in: Argentina, Austria, Australia, Belgium, Canada, Denmark, England, Finland, France, Germany, Greece, Hong Kong, Ireland, Israel, Italy, Japan, Korea, Mexico, The Netherlands, New Zealand, Norway, Philippines, Singapore, Spain, Sweden, Switzerland, Taiwan, U.S.A.

CIRCLE 139

Complete Protection Needed

Dedicated Power Lines Leave Computers Vulnerable.

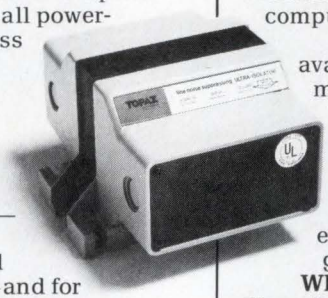
Power-line noise is a major source of computer problems; it can cause program errors, component malfunction and hardware damage. The many sources of noise include lightning, the switching of power grids and power-factor correction capacitors by utility companies, and the operation of countless electrical devices from elevators to electric pencil sharpeners. Power-line noise is so troublesome that most computer manufacturers recommend that users provide some form of noise protection in order to keep sensitive equipment operating properly.

Dedicated Lines are Ineffective Against Most Noise Transients.

Many computer users believe that the best way to provide noise protection is with a dedicated power line. But a dedicated line protects *only* against noise that originates *within* the computer facility. It provides virtually no protection against the majority of noise transients — those which originate outside the facility. This external noise enters the building through the main power feeder *and actually travels down the dedicated line to the computer.*

Ultra-Isolators Provide COMPLETE Noise Protection.

A Topaz Ultra-Isolator installed between the computer and the electrical power source blocks the only path through which noise can pass. This ensures complete protection against all power-line noise regardless of its source. (See table.)



More Ultra-Isolator Advantages.

Distribution— A dedicated line offers only limited noise protection—and for only one piece of equipment. A Topaz Ultra-Isolator offers complete protection and also offers output receptacles for as many as 21 pieces of sensitive electronic equipment. This feature allows users to distribute noise-free AC power to an entire computer system simply by plugging each piece of equipment into the Ultra-Isolator.

Convenience — Installing a dedicated power line often requires building modifications that can disrupt normal facility operations for days. A Topaz Ultra-Isolator typically can be installed in less than one hour — and with practically no inconvenience.

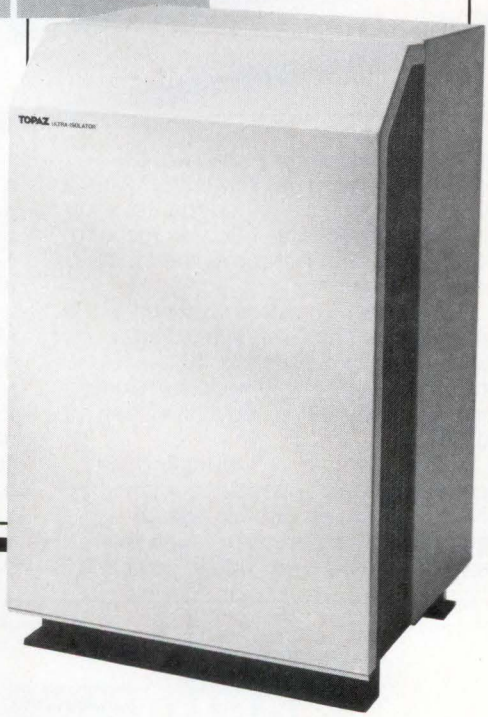
Economy — In most cases, the cost of an Ultra-Isolator will be considerably less than the cost of a dedicated power line. And unlike a dedicated line, a Topaz Ultra-Isolator can be moved if the computer is ever relocated.

Topaz Ultra-Isolators are available in 50 Hz and 60 Hz models and in styles and power ratings to suit virtually any application. Other features include UL listing, attractive computer-room styling, quiet and efficient operation and guaranteed performance.

Why install a dedicated power line when you can provide more protection for more equipment in less time for less money with a Topaz Ultra-Isolator? Contact us today for the **complete** solution to noise-related computer problems.

SOURCES OF NOISE	PROTECTION	
	DEDICATED LINE	*ULTRA-ISOLATOR*
Electrical devices within your facility	YES	YES
Electrical devices in neighboring facilities	NO	YES
Lightning	NO	YES
Power-network switching	NO	YES
Switching of power-factor correction capacitors	NO	YES

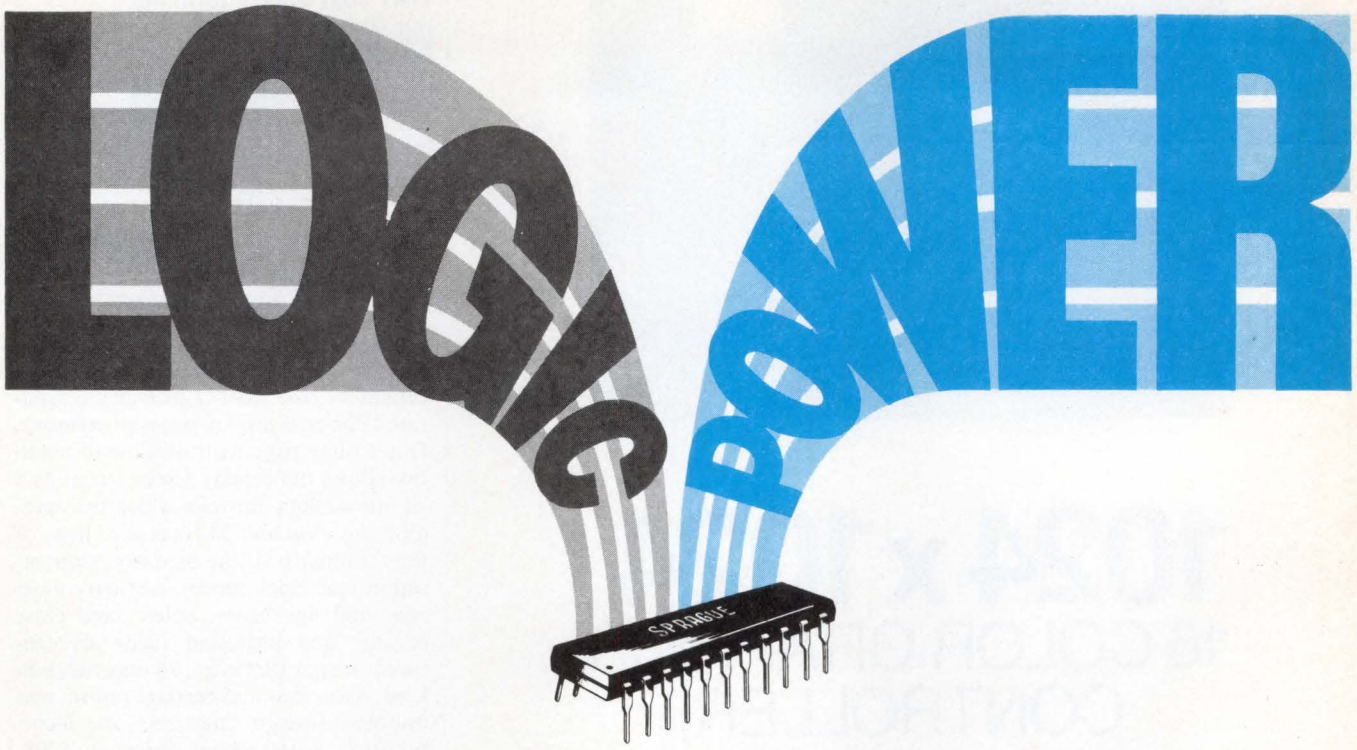
Topaz Electronics Division,
3855 Ruffin Road
San Diego, CA 92123
(619) 279-0831
TWX: 910-335-1526



TOPAZ
SOLUTIONS TO POWER PROBLEMS™

CIRCLE 140

CREATIVE MIXING OF LOGIC & POWER



Sprague BiMOS ICs Simplify Interface Designs

Sprague BiMOS Latch/Drivers can be advantageously employed in a variety of sink and source drive applications: relays, solenoids, stepping motors, LED or incandescent displays, thermal print heads, vacuum fluorescent displays, and many more.

These IC's incorporate CMOS inputs, latches, and control circuitry to provide minimum loading and compatibility with CMOS, PMOS, NMOS, and TTL. The bipolar Darlington outputs are suitable for use with a wide variety of high-voltage or high-current loads. The bipolar/MOS combination provides extremely low-power with maximum interface capability.

Type	Description	V_{OUT}	V_{DD}	I_{OUT}	Engineering Bulletin No.
UCN-4401A	4-Bit Latch/Driver	50V	18V	500mA	26180
UCN-4801A	8-Bit Latch/Driver	50V	18V	500mA	
UCN-4805A	Latched Decoder/Driver	60V	18V	−40mA	26181
UCN-4806A	Latched Decoder/Driver	60V	18V	−40mA	
UCN-4810A	10-Bit Serial-input, Latched Driver	60V	18V	−40mA	26182
UCN-4815A	8-Bit Latch/Source Driver	60V	18V	−40mA	26183
UCN-4821A	8-Bit Serial-input, Latched Sink Driver	50V	15V	350mA	26185
UCN-4822A	8-Bit Serial-input, Latched Sink Driver	80V	15V	350mA	
UCN-4823A	8-Bit Serial-input, Latched Sink Driver	100V	15V	350mA	

For the engineering bulletins of interest to you, write to: Technical Literature Service, Sprague Electric Company, 555 Marshall St., North Adams, Mass. 01247.

For further information, write or call Paul Emerald, Semiconductor Division, Sprague Electric Company, 115 Northeast Cutoff, Worcester, Mass. 01606. Tel. 617/853-5000.

For the name of your nearest Sprague Semiconductor Distributor, write or call Sprague Products Company Division, North Adams, Mass. 01247. Tel. 413/664-4481.

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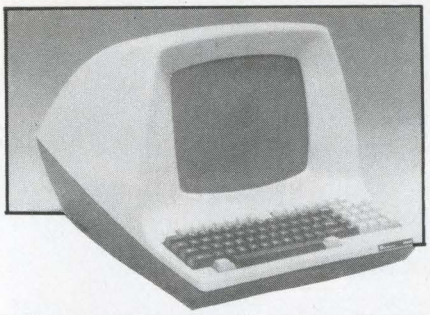
CIRCLE 141

SYSTEM COMPONENTS/ PERIPHERALS

Low cost smart terminal



Microprocessor based video display terminal featuring window to memory capability, the ADM 23 provides 2 separate 1920-char display pages of memory. One 51-line page with window to memory allows the display screen to act as a 24-line window through which the operator can view any 24 successive lines of the terminal's 51-line memory. Conversation and block modes; auxiliary port; char and line insert, delete, and erase editing; and protected fields are featured. Visual attributes, 16 max function keys, ASCII char and carriage return, and optional foreign char sets are incorporated. Commercial price is $795, quantity 1. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803. **Circle 321**

Ergonomic terminal with extensive emulation capabilities

Visual 330 microprocessor based video display terminal emulates DEC's VT52 and DG's D200 terminals. Menu selectable emulation of Lear Siegler's ADM-3A and Hazeltine's 1500 terminals is also included. Streamlined plastic housing, tilt and swivel capabilities, 12″ or 14″ (30- or 36-cm) nonglare screen, high density 7 x 9 dot matrix chars, and detached low profile keyboard are featured. Each of 12 user programmable nonvolatile function keys stores 32 chars. Standard video attributes, line drawing char set, and split-screen viewing are featured. Price is $1150. **Visual Technology Inc,** 540 Main St, Tewksbury, MA 01876.

Circle 322

Lundy graphics terminals are setting standards because we set high standards for Lundy.

Standards: no other 3D graphics vector work-station delivers more speed or a higher IQ than the UltraGraf;™ only our color raster scan display products offer resolution as high as 1,536 × 1,024 pixels. But there's still another standard you should investigate—the one we set for our company.

Be careful. The fast-paced world of high tech breeds a lot of companies that don't survive; five years from now, many graphic terminal manufacturers won't be around anymore. Which means you could be left without service, support or enhancements.

Lundy: a company as good as its products.

That's why we think it's important you know as much about our company as our products. We're a high tech company that's been able to balance standard-setting technology with solid business sense—no small achievement.

Now, don't take our word for that, take *Forbes* magazine's instead. Lundy was on *Forbes'* Up&Coming List for 1982, a select roster of companies that look good for the long term because they've paid attention to basics: low debt load, consistently good profit picture, sound management, investment in service, support and R&D.

T5680 color raster, 3D UltraGraf ™and T5470.

Lundy maintains the largest service infrastructure—52 locations.

Our graphics terminals feature the best price/performance ratios available today.

We have developed a new software subroutine package with exceptional compatibility. Its 300 functions deliver a new high in high powered productivity.

Lundy continues to invest in expanded R&D each and every year. Because R&D is the name of this highly competitive game—and we intend to *keep* setting standards.

We'll help you see more in graphics.

When you take a close look at our graphics terminals, service, support, software, systems capability, enhancements—and our company—you'll understand why Lundy can help you see more in graphics now and in the long term.

For more information, write: Lundy Electronics & Systems, Inc., Glen Head, New York 11545, or call: (516) 671-9000.

LUNDY®

Mt. Everest, symbolic of aiming high, was generated on the Lundy T5680 raster. It offers 16 colors and 136 shades from a palette of 4,096 colors.

CIRCLE 142

Check The Chart Before You Choose Your New 16-Bit Computer System.

Columbia Data Products' New Multi-Personal® Computer, Featuring IBM-PC® Compatibility, Excels In Professional, Business And Industrial Applications. Check it out.

Columbia Data Products' MULTI-PERSONAL® COMPUTER can use software and hardware originally intended for the IBM® Personal Computer . . . while enjoying the flexibility and expandability of all Columbia Data's computer systems.

Available operating system software includes single-user MS-DOS® or CP/M 86® or multi-user, multi-tasking MP/M 86® or OASIS-16®, with XENIX® available soon, providing users with a host of compatible software packages for personal and professional business and industrial applications. A large selection of higher level languages are also available, including BASIC, FORTRAN, COBOL, PASCAL and MACRO Assembler.

Our standard 16-Bit 8088 hardware configuration provides 128K RAM with parity, two RS-232 serial ports, Centronics parallel printer port, interrupt and DMA controllers, dual floppy disks with 640K storage, Winchester disk and keyboard interfaces, and eight IBM-PC compatible expansion slots . . . and lists for only $2995. Winchester hard disk configurations, featuring cache buffer controllers for enhanced disk access performance are also available, starting at $4995.

So, when you need to grow, why gamble and hassle with independent third party hardware and operating system vendors which may or may not be compatible . . . not to mention the hidden expense and frustration of implementing peripheral drivers in the different operating systems and upgrades? Who needs the finger-pointing when things don't work out?

After you review our chart, you will agree . . . for overall 16-Bit microprocessor superiority, expandability, flexibility, compatibility and real economy, Columbia Data is your *total source.*

Our Multi-Personal Computer . . . the 16-Bit system born to grow!

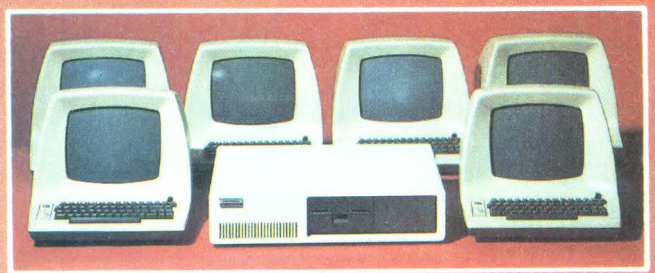
Get yours now.

MAIN FEATURES	CDP-MPC	IBM-PC*	OTHERS
Microprocessor	16-Bit 8088 8-Bit Z-80 (Opt)	16-Bit 8088	?
USER Memory	128K-1 Mbytes	16K-256 Kbytes	?
IBM-PC Compatible Expansions Slots Beyond Professional Configuration[1]	8 Slots	0	?
Resident Floppy Disk Storage	Dual 320K (std)	Dual 160K (Opt) Dual 320K (Opt)	?
Resident Cache Buffer Hard Disk Storage	5M/10M	—	?
OPTIONAL OPERATING SYSTEMS (Supported by Company)[2]			
MS-DOS (PC-DOS)	Yes	Yes	?
CP/M 86	Yes	Yes	?
MP/M 86	Yes	—	?
OASIS-16	Yes	—	?
XENIX	Soon	—	?
OPTIONAL HARDWARE EXPANSION BOARD (Supported by Company)			
RS-232 Communications	Yes	Yes	?
B/W and Color Display Controller	Yes	Yes	?
Expansion Memory	Yes	Yes	?
Z-80 CP/M-80 Board	Yes	—	?
Cache Buffer Hard Disk	Yes	—	?
Time/Calendar Board	Yes	—	?
IEEE Bus Controller	Yes	—	?
8" Floppy Disk System	Yes	—	?
8" Hard Disk System	Up to 40 Mbytes	—	?
Tape Cartridge System	Yes	—	?

[1]For comparison purposes, typical professional configurations consist of 16-Bit 8088 Processor, 128K RAM with Parity, Dual 320K 5-inch Floppies, DMA and Interrupt Controller, Dual RS-232 Serial Ports, Centronics Parallel Port and Dumb Computer Terminal or Equivalent.

[2]Columbia Data Products also supports CP/M 80® with an optionally available Z-80 CP/M Expansion Board.

*As advertised in BYTE Magazine, August 1982.



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DATA PRODUCTS, INC.

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Columbia, MD 21045
Telephone 301-992-3400
TWX 710-862-1891

West Coast:
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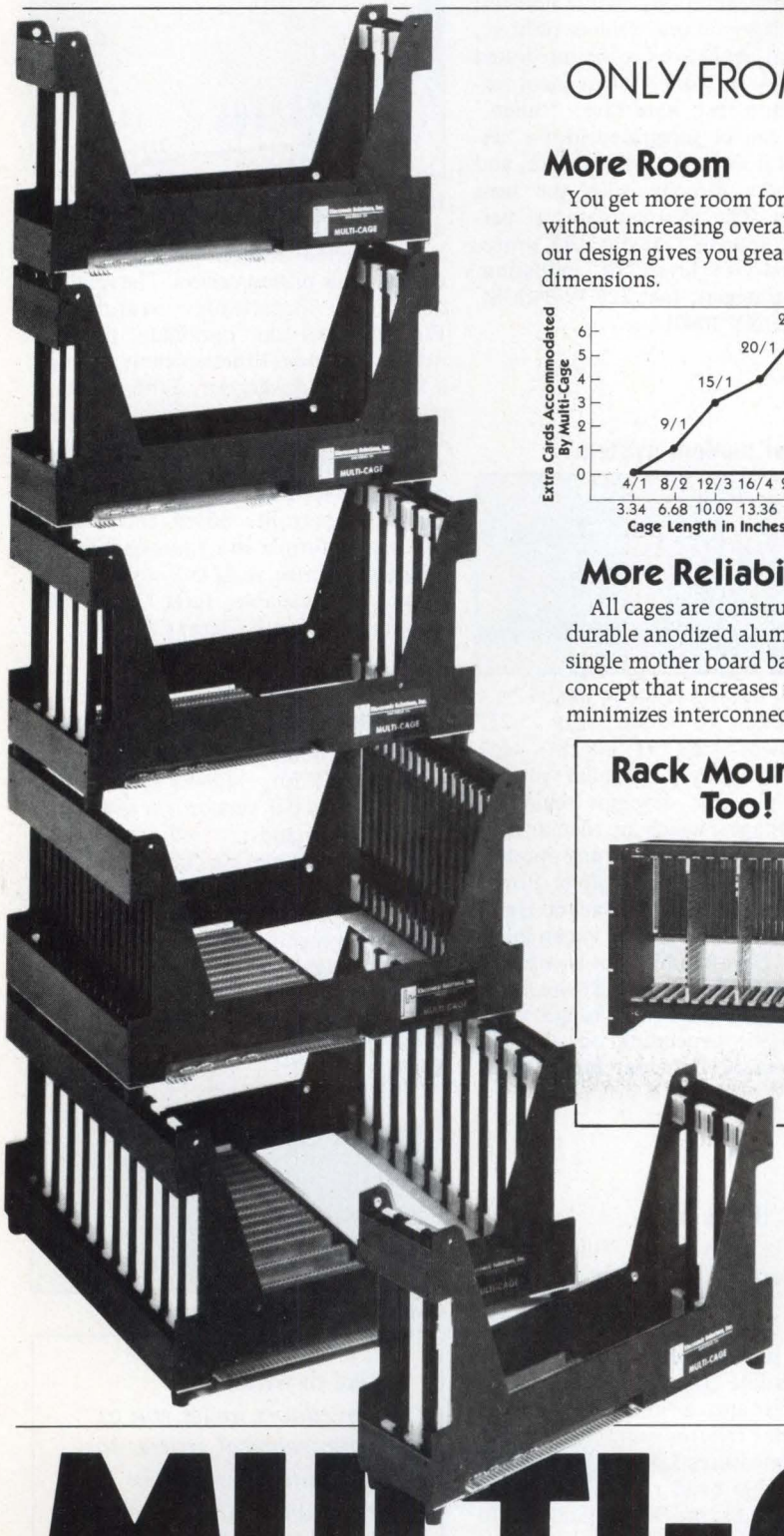

ONLY FROM ELECTRONIC SOLUTIONS!

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You get more room for extra cards without increasing overall size, because our design gives you greater inside dimensions.

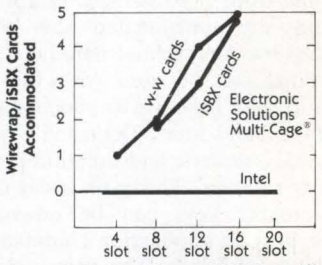
More Reliability

All cages are constructed of sturdy, durable anodized aluminum with a single mother board backplane . . . a concept that increases reliability and minimizes interconnections.

Rack Mounting Too!

More Models

We have more models than all our competitors combined. Choose a cage with 3, 4, 5, 6, 7, 8, 9, 12, 14, 15, 16, 20, 24 or 26 slots for the right solution to your problem. We have models with either 0.6" or 0.75" card centers and can even accommodate **wirewrap cards**.



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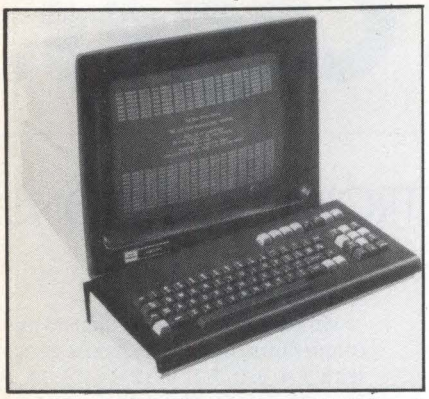
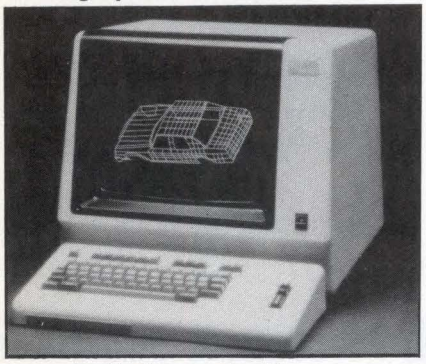
CIRCLE 144

Low cost ANSI compatible terminal



GENIE terminal features a 15″ (38-cm) nonglare screen, 60-line optional memory and zoom feature that allows user or host to reconfigure the display format from 18 to 30 lines. Editing commands are implemented with pointers and allow for decimal parameters. The terminal can be used with full-screen editors with little use of pad chars, even at high baud rates. Detached keyboard provides numeric and function keys and n-key rollover. Thirty-six levels of programmable keys can be downloaded with host or application commands for 1-stroke execution. The ANSI compatible terminal is $1195. **Ann Arbor Terminals, Inc,** 6175 Jackson Rd, Ann Arbor, MI 48103. **Circle 323**

High resolution color graphics terminal



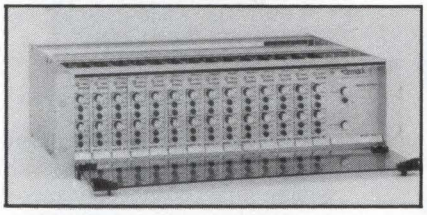
NJC-C1421 display terminal for CAD, CAM, and CAE applications combines a color monitor, graphics processor, and communications package into a desktop unit. It features a 14″ (36-cm) raster scan CRT, 1024- x 780-dot resolution, 16-color display (27-color palette), and optional zoom and pan. Serial/parallel ports, built-in lightpen interface, and video outputs for host computer and peripheral communication are included. Unit is DEC VT-100 and PLOT 10 compatible. Price is $6995. **Nippon Computer Co, Ltd,** Naito Bldg, Nihonbashi Hamacho 2-25-1, Chuo-ku, Tokyo 103, Japan.
Circle 324

DATA COMMUNICATIONS

Customized SNA device emulators for non-IBM peripherals/processors

Customized system network architecture device implementations enable non-IBM terminals, RJE stations, remote printers, and general processors to be integrated into an SNA network. When incorporated in non-IBM hardware, "alien" hardware can be integrated into a network, as if it were a true IBM device, and communicate directly with the host mainframe. The SNA emulator is perceived as comprising the physical, protocol, and device layers of emulation. **Systems Strategies, Inc,** 225 W 34th St, New York, NY 10001.
Circle 325

Short-haul modem system

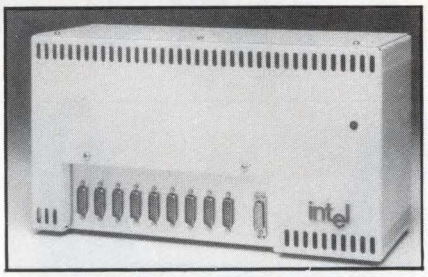


Short-haul modem system model 76-A accommodates 28 modems in 5.25″ (13.34-cm) of std 19″ (48-cm) rack space. It includes a modular plug-in power supply that develops semiregulated dc voltages, which are then distributed via PC backplane to any module installed in any of the 14 slots. Power supply operation is at 110 Vac, 60 Hz or 220 Vac; 50 Hz is selectable via an internal switch. Each module slot is wired to two RS-232 connectors and 8 wire cable termination jacks. Prices range from $556 to $795, depending on configurations. **Remark Datacom Inc,** 4 Sycamore Dr, Woodbury, NY 11797.
Circle 326

Half-size, 8-line mux

Spectrum Eleven SZV11 8-line multiplexer is compressed to half the size of the DZV11, yet has double the functionality. The asynchronous mux sells from $1150 and is compatible with all DEC and DEC compatible Q-bus hardware. Use of dual UARTs and a microprogrammed state machine reduces component count. The SZV11 measures 5.5″ (14.0-cm) high. Plug selectable baud rates allow access to rates of 19.2k and 38.4k baud and to various split receive/transmit pairs. **Webster Electronics Inc,** 333 Cobalt Way, Sunnyvale, CA 94086.
Circle 327

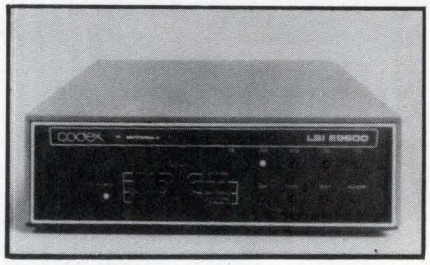
Ethernet connection eliminates transceivers, cables



Intellink cluster module DCM 911-1 allows up to nine Ethernet™ workstations to be connected without using Ethernet coaxial cable or transceivers. The resulting customer installable, standalone Ethernet LAN can optionally be connected to a main Ethernet cable through a single transceiver. Any Ethernet compatible device can be connected to the Intellink module without modification. Module acts as a std Ethernet transceiver. Device can be used with iSBC 550 Ethernet controller board and iNA 950 LAN S/W to form a MULTIBUS based LAN. Single-unit price is $2450; volume discounts are available. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 328

Economical high speed modems

E series 9600-bps modems include the LSI E9600 ($2650), LSI E9604 ($3200), and the international version LSI E9600 V.29. The LSI E9604 and LSI E9600 V.29 provide 4-channel multiplexing. The LSI E9604 is a domestic functional equivalent to E9600 V.29. MTBF is in excess of 36k h on the LSI E9600. Shipments of the series are currently available. **Codex Corp, a sub of Motorola Inc,** 20 Cabot Blvd, Mansfield, MA 02048.



Circle 381

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ROLM U.K. Limited, Catherine House, 63 Guildford Road, Lightwater, Surrey GU18 5SA, England, (0276) 76363

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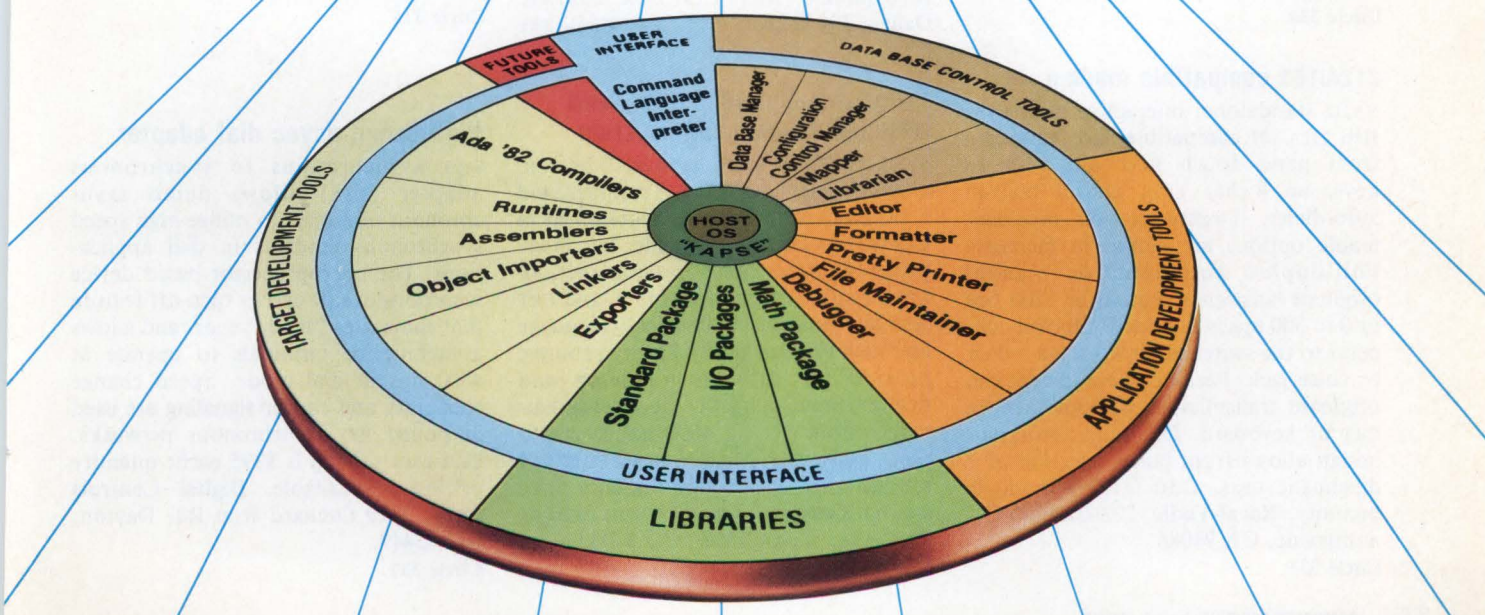
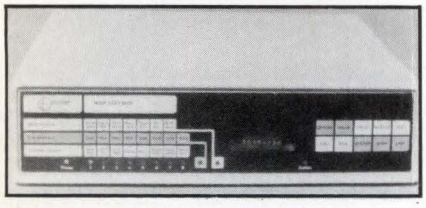
CIRCLE 145



16-channel stat mux



Stat mux model 4001 concentrates up to 16 channels over a single phone link, complementing the company's 60-channel 4220 network processor. Unit features user selectable channel priority assignment and 50- to 9600-bps speed. On the concentrated link, synchronous or NRZI asynchronous capabilities are std; no external clock source is needed. Inband and out-of-band flow controls are independently selected at each end of the channel throughout a point to point network. Pricing begins at $1690. **Halcyon Communications, Inc,** 2121 Zanker Rd, San Jose, CA 95131.
Circle 329

Data line monitor

DLM V data communications analyzer has full menu driven keyboard programmability that includes 15 instructions and 11 commands. Each test program can be up to 72 steps long. Edit/update capability allows program modifications without rewriting. Up to 10 named programs can be stored simultaneously in nonvolatile EEPROM. Stored programs can interactively test terminals or interactively emulate different segments of the communications network. An optional MSU IV dual-diskette subsystem expands storage capacity and offline diagnostic capability. Price is $5395. **Digilog, Network Control Div,** 1370 Welsh Rd, Montgomeryville, PA 18936.
Circle 330

212A/103 compatible modem

VA212 standalone, interactive modem is Bell 212A/103 compatible and features a front panel touch keyboard with 16 keys, an 8-char LCD, and a built-in auto-dialer. Twenty-six user programmable options are stored in memory. Full-duplex automatic or manual originate/answer operation at 1200 bps or 0 to 300 bps is provided. Modem connects to the switched network via a data or voice jack. Peripheral equipment can originate transmission without using a CRT or keyboard. Dual-microprocessor design allows front panel selection of 7 diagnostic tests. Cost is $795 in single quantity. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.
Circle 331

ProNET connection for MULTIBUS computers

MULTIBUS host specific board allows connection of any MULTIBUS compatible computer to the proNET™ 10M-bps local network system. The proNET systems include the host specific model HSBM and a controller board model CTLM. Using a passive wire center, controller hardware implements a token arbitrated star shaped ring network that supports several hundred host computers, terminal servers, and other high speed devices. The CTLM need not be mounted in the MULTIBUS backplane. Fully decentralized token ring transmission with guaranteed access and full throughput is provided. Fiber optic links are available. Price is $1988. **Proteon Associates, Inc,** 24 Crescent St, Waltham, MA 02154.
Circle 332

INTERFACE

Controller interfaces DRAMs to microprocessors

TMS4500A dynamic RAM controller features synchronous operation and directly addresses and drives up to 256k bytes of memory. A 16-bit multiplexer generates row, column, and refresh addresses for up to 32 DRAMs. Strobe signals for DRAM decode of addresses are provided. Onchip 8-bit refresh counter generates the 256 row addresses needed for RAM refresh while a refresh timer generates timing signals. The internal or external refresh rate is strap selectable. Device is provided in a std 40-pin plastic DIP; op temp range is 0 to 70 °C. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220. **Circle 333**

Programmable controller with onboard development system

SYS-2 controller features four 12-bit ADC channels, eight 50-V/0.5-A outputs, and 8 switch-closure inputs. Programmed in Control BASIC, the controller has interpreter, 4k RAM, EPROM programmer, 4k EPROM space expandable to 6k, and CRT terminal interface. Resident language and menu driven utility library prompts provide for easy programming and debug. Serial RS-232-C port programmable from 110 to 4800 baud, 2 CPU flags, and a high level vectored interrupt are included. Production quantity price is $285. **Octagon Systems Corp,** 5150 W 80th Ave, Westminster, CO 80030.
Circle 334

Color graphics enhancements

The act 1 interface attaches an act 1 nonimpact ink jet copier to the CGC 7900 color graphics computer system for copying raster images or ASCII text directly from the computer display memory. Hardcopy interfaces for the Versatec V80 and any RS-232 printer are also available. The ROM expander card increases ROM from 64k to a max of 512k bytes when 4 cards are used. The remote fixed disk provides portable mass storage and also extends the 7900's storage to 80M bytes. The 9-track tape interfaces to std tape drives and provides dual-disk capabilities and offline/online storage. **Chromatics, Inc,** 2558 Mountain Industrial Blvd, Tucker, GA 30084.
Circle 335

Graphics display with flicker-free resolution and screen refresh

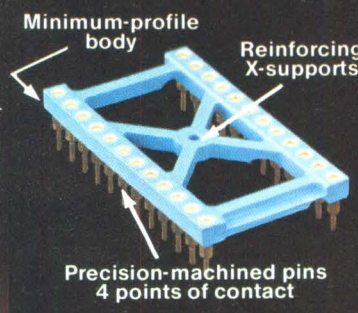
Model One/60 graphics display system combines a local command set with multiprocessor architecture to relieve the host computer from interactive menu management, graphics input device control, and other realtime tasks. Unit features a 768 x 576 displayable resolution window on a 1024 x 1024 bit map. Displayable window can pan/zoom across the nonvisible memory, which also stores text fonts and special symbols. The 60-Hz noninterlaced display can simultaneously show 64 colors from a 16M palette. Price is $11,000 to $18,500, depending on configuration; quantity discounts are available. **Raster Technologies, Inc,** 127 Dorrance St, Providence, RI 02903.
Circle 336

High speed async dial adapter

9373 asynchronous to synchronous adapter (ASA) allows dumb asynchronous terminals to utilize high speed synchronous modems in dial applications. The microprocessor based device incorporates soft carrier turn-off feature that eliminates "trash" chars and allows asynchronous terminals to operate at 4800 bps in dial mode. Speed change capability and carrier signaling are used in polled ISO asynchronous networks. End-user pricing is $395 each; quantity pricing is available. **Digital Controls Corp,** 2779 Orchard Run Rd, Dayton, OH 45449.
Circle 337

Now Ansley Electronics has you covered across the board.

On it, off it, across it and board-to-board, Ansley Electronics is now your complete source for electronic interconnection. We've gone beyond our innovative family of flat cable and IDC products, and developed an extensive line of premium quality, low profile screw-machined DIP Sockets: a full range of open frame, closed frame, solder pin and wrap post styles – all designed for optimum electrical and mechanical performance.



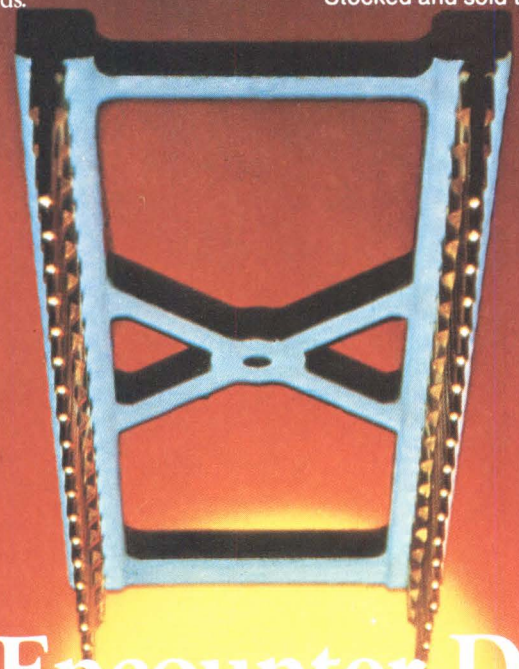
For example, many of our open-frame sockets feature exclusive "X" supports for greater strength and rigidity – and better visual access to the PC board.

Available in 6 through 64 positions, Ansley Electronics DIP Sockets offer precision screw-machined pins for high integrity, high reliability contact. Plus a minimum-profile body to maximize air flow and space between boards.

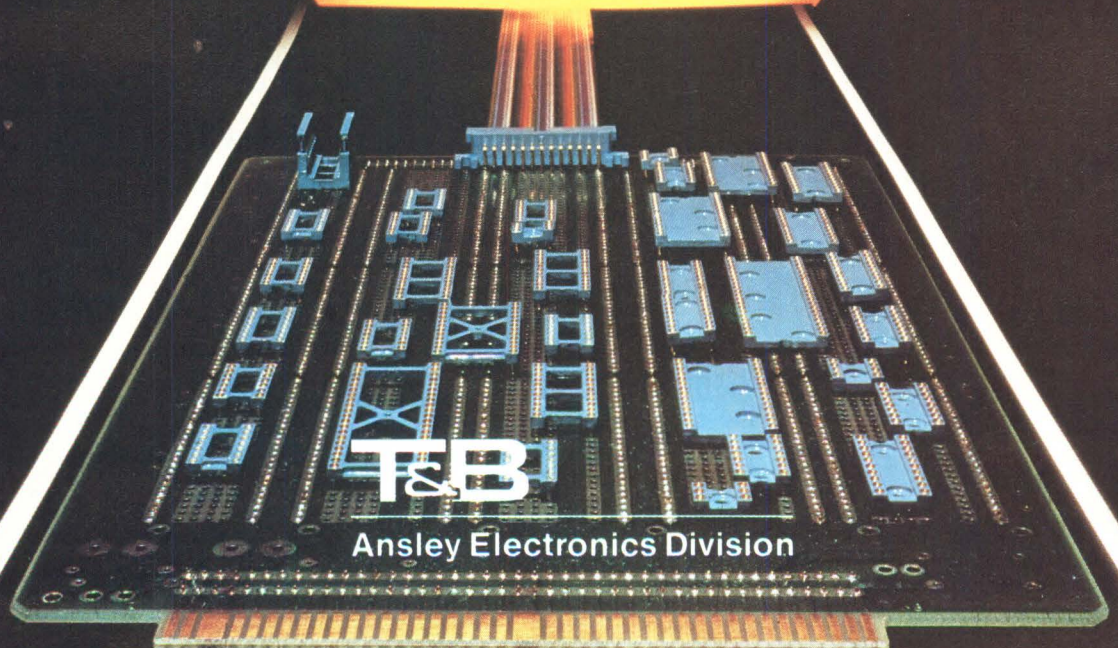
They complete a family of DIP-compatible products unparalleled in the industry. Like our Remote DIP Socket Connector, which frees DIP switches, displays and ICs from PC boards. And our innovative Stacked DIP Socket, accommodating two DIP memory or discrete devices – one above the other – to virtually double IC packaging density.

The byword is commitment. Look to Ansley Electronics as the complete across-the-board supplier for all your electronic interconnection needs. For data on our new DIP Sockets, adaptor plug assemblies, terminal carriers and socket pins, write today. Thomas & Betts Corporation, Ansley Electronics Division, 920 Route 202, Raritan, N.J. 08869. Or phone Customer Service at (201) 469-4000.

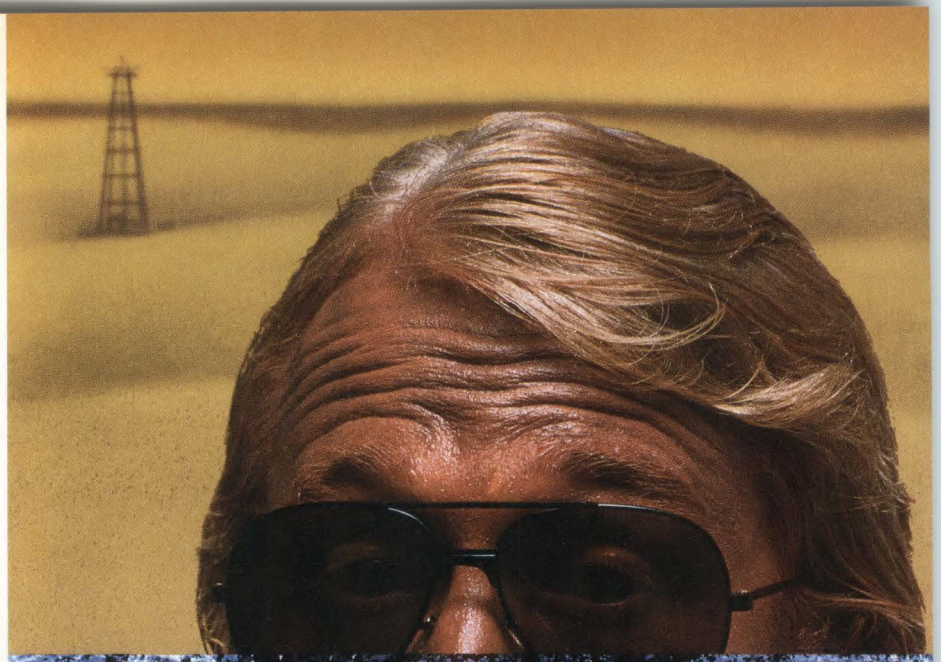
Stocked and sold through Authorized Distributors.

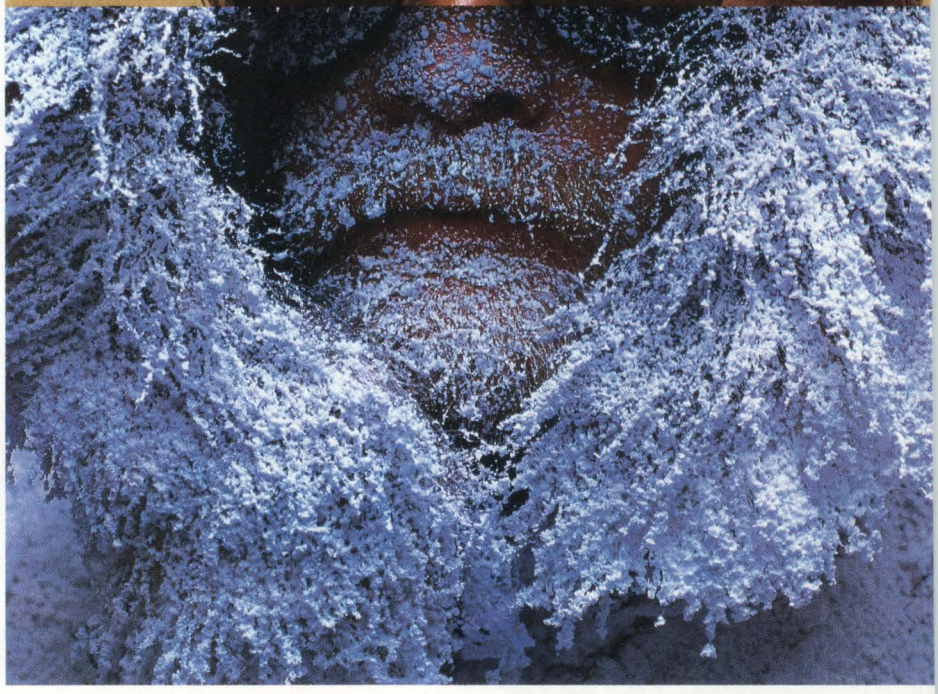


Encounter DIP Sockets of another kind.



CIRCLE 146





HE'S BEEN THERE, searching for oil. Logging drill mud temperature and viscosity at the equator. Performing seismic studies where the ground is frozen solid year round.

And he depends upon rugged Dataflux Winchesters to come through with accurate, on-line data processing – in spite of the conditions.

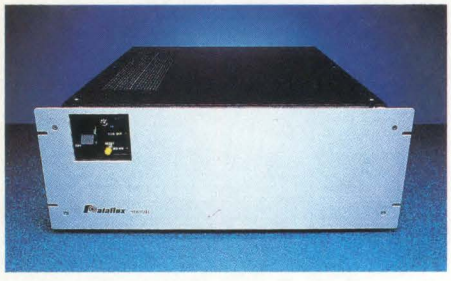
Today, in addition to oil exploration, over 400 Dataflux Rugged Winchesters with customized interfaces are being used in process plants, mining operations, and severe military applications.

As independent tests substantiate, these drives are built to take extreme temperatures. −40°C to 60°C non-operating. 0°C to 50°C operating.

They can be bounced around. 5 G's along all axes when they're not being used. 2 G's, error free, when they are.

And as for vibration, they're tested to MIL-STD 810C.

Dataflux makes two models of Rugged Winchesters. The 8" 9800R provides up to 20 Mbytes of on-line data storage (soon, up to



100 Mbytes). Plus an average access time of 35 ms. 10,000 hours of power-on MTBF. 30 minutes MTTR.

And there's our 5800R "Twinchesters" – two 5¼" drives, each with up to 21 Mbytes of storage capacity. Totally software transparent, the 5800R provides maximum infield redundancy, with serial recording, simultaneous recording, or data dumping from one disk to another under software control.

And the 5800R is removable, allowing easy replacement in the field as well as secure storage of classified information.

For test results, spec sheets, and further information on Dataflux design features and custom interfaces, please call or write: Dataflux Corporation, 1050 Stewart Drive, Sunnyvale, CA 94086 (408) 732-7070.

Our Rugged Winchesters can go from 60°C above to 40°C below.

Ask the field supervisor.

DATAFLUX

WHEN THE GOING GETS ROUGH.

CIRCLE 147

Error correcting hard disk controller for S-100 micros

Model HDC-1001 microprocessor based hard disk controller operates up to four 8″ or four 5¼″ hard disk drives within S-100 based microcomputers. A 32-bit computer-generated polynomial detects/corrects errors before they are apparent to the user. Up to 8-bit single-burst correction, multiburst detection, and programmable correction/detection span are also featured. Controller has built-in separation and 5M-byte/s max data rates, 256-sector addressing range, CRC generation/verification on ID fields, unlimited sector interleave, and automatic retries, restore, and reseek on error. Controller with CP/M BIOS diskette is $500. **Advanced Digital Corp,** 12700 B Knott Ave, Garden Grove, CA 92641.
Circle 338

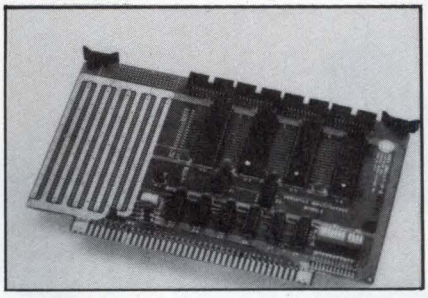
Single-chip intelligent peripheral controllers

R6500 family of single-chip, 8-bit programmable slave controllers have parallel host data bus compatible with 6500/6800 and 8080/Z80 microprocessors. Devices have onchip I/O status, control registers, and 16-bit counter with latch. Onchip 64 x 8 RAM and ROM satisfy requirements for motor and keyboard control, small printer line buffering, and other peripheral control tasks. I/O ports are software programmable to directly address up to 4k bytes (8k for 1 device) of external memory or additional I/O. Five external, 1 internal, and 2 host interrupts include 1 positive and 1 negative external edge sensitive lines. Prices range from $5.60 to $8.60. **Rockwell International,** 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660. **Circle 339**

Controller features custom LSI chips

SA1600 series disk drive controllers provide device independence via 4 custom LSI chips and microprocessor. Address chip contains control lines for SASI functions, and controls address of data buffer in RAM. Sequencer chip and microprocessor contain serializer/deserializer and main sequencer control logic for formatting, searching, reading, and writing functions. Analog data recovery system (DRS) handles data separation for FM/MFM for floppy or rigid drives. Digital DRS handles address mark generation/detection and digitizes analog data. Evaluation units will be available in the first quarter 1983. **Shugart Assoc,** 475 Oakmead Pkwy, Sunnyvale, CA 94086.
Circle 340

Interface module supports 80 I/O and control lines



GMS6501 module comes with 64 bidirectional I/O lines, 16 handshake lines, eight 16-bit programmable counter/timers, and four 8-bit shift registers. The module is fully compatible with Motorola's EXORciser/Micromodule and Rockwell's SYSTEM 65/AIM 65 bus structures. Four 6522 versatile interface adapter devices are onboard. Requiring a single 5-V supply, board includes a wirewrap section for customized I/O. All address and data lines are fully buffered, and all I/O ports are CMOS/TTL compatible. Prices range from $168 to $214. **General Micro Systems, Inc,** 1320 Chaffey Ct, Ontario, CA 91762.
Circle 341

DATA CONVERSION

12-bit, 10-MHz ADC

CAV-1210 12-bit 10-MHz ADC ($2287) includes a track and hold amplifier, an encoder, and timing/output registers. Monotonic performance is guaranteed over the 0 to 70 °C op temp range. Full-scale analog input range is ±1 V with input impedance of 1k Ω. Total error at dc, including nonlinearity, is typ ±0.0125% of FS. Typ nonlinearity vs temp is ±0.000125% of FS/°C while gain drift is typ less than ±0.005% of FS/°C. Max initial offset voltage is ±1 mV and drifts are less than ±0.02% of FS/°C. With a 500-kHz analog input, rms signal to rms noise ratio is 62 dB typ. **Analog Devices, Inc,** 7810 Success Rd, Greensboro, NC 27409.
Circle 342

EMI PROTECTION

Silicone gasketing for emi shielding

TUFEL™ semiconductive silicone gasketing—a heat cured silicone rubber compound—provides high tear strength, flex life, and elasticity. Material is durable and reliable despite broad temp swings and environmental attack. The shielding gaskets also provide a dust and hermetic seal for the system. Typ volume resistivity of 7 Ω/cm is achieved. Material meets appropriate UL flammability standards. **General Electric Co, Silicone Products Div,** Waterford, NY 12188.
Circle 343

SOFTWARE

Enhanced Series/1 software

Version 6 of the Series/1 realtime programming system (RPS), along with a multiprocessing feature, facilitates attachment of additional processors to the Series 1 without interrupting system operation. Two to 16 Series/1 systems can be configured to appear as a single computer. Two copies of data files can be made for backup. Redesigned I/O architecture improves response time and throughput and supports additional peripherals. Command language facility enhancements include full-screen menus. Also featured are SNA extended support and magnetic tape support. **IBM Corp,** 900 King St, Rye, NY 10573.
Circle 344

I/O control program development

CyberFORTH extended Forth dialect includes built-in industrial hardware I/O drivers for Cybersystems' analog and digital I/Os and communications modules, and a prioritized realtime multitasking executive. An interactive command line integrator, fully structured assembler, source code editor, interactive runtime tracer/debugger, cross compiler for generating ROMable programs, floating point math package, and links to a high level graphics utilities package are also provided. The program development package ($300) runs under CP/M on the development system and optimizes features of the CYKEY model 9990. **Cybersystems, Inc,** 7540 S Memorial Pkwy, Huntsville, AL 35802.
Circle 345

MTOS-68K

for the chips you don't want to gamble with...

The Multi-Tasking Operating System for the 68000

MTOS-68K has made its mark among 68000 micro users. It is a real-time operating system that's so beautifully simple... it's simply beautiful.

- Supports up to 16 processors on a common bus
- Written in assembler to emphasize through-put
- Run-time interfaces for Pascal, "C" and Assembler
- Extendable, configurable and provides for easy incorporation of special device drivers
- Requires only a clock interrupt and a lockable bus to operate in any 68000 environment

MTOS-68K, with all its Power and Features, requires only 11k bytes and as little as 6k bytes in certain applications.

For the chips you don't want to gamble with, look to Industrial Programming. We have produced more real-time operating systems, for more micro processors, for more years than any other source in the industry.

These MULTI-TASKING OPERATING SYSTEMS are delivered in source form and sold under a liberal licensing policy which entitles the licensee to imbed the object program in products without further charges.

- **MTOS-86** for the 8086
- **MTOS-86MP** for the 8086
- **MTOS-80** for the 8080/85
- **MTOS-80MP** for the 8080/85
- **MTOS-68** for the 6800
- **MTOS-69** for the 6809

- **MTOS-68KF*** firmware for the 68000

*Sold in object form under separate license

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100 Jericho Quadrangle, Jericho, New York 11753
(516) 938-6600 • Telex: 429808

FRANCE: CELDIS SA, 53 Rue Charles Frerot, 94250 Gentilly, Phone: 546.13.13, Tlx 842-200485
WEST GERMANY: SCS Scientific Control Systems GmbH, Postfach 62 04 80, Oehleckerring 40, 2000 Hamburg 62, Phone: 040 531030, Tlx: 841-2174113
CELDIS-ENATECHNIK-SYSTEM VERTRIEBSGESELLSCHAFT mbH Schillerstrasse 14, 2085 Quickborn (Hamburg), Phone: 041 06/612-240, Tlx 841-213590
INDIA: SARAS ELECTRONICS, 21, Perambur Barracks Road, Madras 600012, Phone: 32497, Tlx 011-3532
ISRAEL: CONTAHAL, LTD., 54 Ibn Gvirol St., Tel Aviv 64364, Phone: (03) 269 379, Tlx 922-33654
JAPAN: (MTOS-86, 80, 80MP) TOKYO ELECTRON LIMITED, Shinjuku Nomura Bldg., 1-26-2 Nishi-Shinjuku, Shinjuku-Ku, Tokyo 160, Phone: 03-344-5893
(MTOS-68K, 68KF, 68, 69) C. ITOH DATA SYSTEMS, LIMITED C. ITOH Bldg., 2-5-1 Kita-Aoyama, Minato-Ku, Tokyo 107, Phone: (03) 497-8096
SCANDINAVIA: FRONTEC MICRODATORCENTRUM AB, Box 204, Malmvagen 28, Sollentuna, Sweden, Phone: 08-359360, Tlx 854-15130
SWITZERLAND: XMIT AG, Bellikonerstrasse 218, CH-8967 Widen, Phone: 057-54656, Tlx 845-59955
UK: HAWKER SIDDELEY DYNAMICS ENGINEERING LTD., Bridge Road East, Welwyn Garden City, Herts, AL7 1LR, Phone: (07073) 31299

CIRCLE 148

Graphics software for CP/M and MP/M systems

SGPLOT graphics package supports the company's retrofit graphics enhancements for DEC VT100 and TeleVideo 925 and 950 terminals. SGPLOT enables DEC VT180/VT18X and TeleVideo TS801 CP/M systems interfaced to Selanar's graphics boards to generate graphics displays. Package ($450) is similar to the CalComp and Versatec instruction set utilizing FORTRAN subroutines. It also features high level statistical routines, automatic saving of plot files, a built-in diagnostic subroutine, program selectable display window with adjustable scale, and user specified functions. **Selanar Corp,** 437-A Aldo Ave, Santa Clara, CA 95050.
Circle 346

Software extensions to REX-80 executive

Multiprocessor extension MPX and file system extension FSX are fully compatible architectural extensions to the REX-80 realtime executive. MPX supports multiple processors with shared memory and provides for task communications, synchronization, and resource sharing across processor boundaries. MPX compatible processors are Z80, 8080, 8085, 8088, or 8086. FSX contains facilities for REX-80 tasks to create, delete, and open files, as well as for reading and writing to files. FSX conforms to CP/M and ISIS-II standards and is used with Z80, 8080, and 8085 processors. **Systems & Software, Inc,** 1315 Butterfield Rd, Downers Grove, IL 60515.
Circle 347

Easy to use Modula-2

Modula-2 version 0.3 includes a module library, a compiler that runs 25% faster than the previous version, and a tutorial to easily update Pascal programmers. Low level machine access, realtime control, concurrent processes, and type-secure separate compilation with automatic version control are featured. Interrupt handling is fully supported. Language is designed for systems based on the 6502, 8080/Z80, TI 9900, and the 68000 microprocessors and interfaces to UCSD Pascal. Std library provides console I/O, random access files, disk directory operations, format conversion, strings, decimal arithmetic, storage management, program execution, and process scheduling. **Volition Systems,** PO Box 1236, Del Mar, CA 92014.
Circle 348

Superminicomputer program generator for micros

Superminicomputer program generator software package with RIMS/MPG™ (Information & Systems Research, Inc) is available for microcomputers to create ready to use business applications and structured ANSI '74 COBOL source code without writing any code. The software carries out friendly dialog with the user to establish program parameters. The COBOL source code generator can be used to develop programs or to customize existing applications. **Micro Focus, Inc,** 1601 Civic Center Dr, Santa Clara, CA 95050.
Circle 349

C compiler for Prime computers

C compiler for Prime Computer, Inc's 50 series and 400/500 computers is compatible with UNIX CC versions 6 and 7 and is accompanied by UNIX libraries with over 100 routines. It compiles at over 5k lines/min and generates Prime 64V mode object code. The compiler has Berkeley and UNIX extensions, including enumerated types, structured arguments and assignments, FORTRAN storage class, identifiers up to 32 chars long, and UNIX style command line arguments. Package is $5000 to $7500. **Primarily Software, Inc,** 1227 Pearl St, La Jolla, CA 92037.
Circle 350

APL for the VAX-11

VAX-11 APL implementation of the A Programming Language (APL) for the VAX superminicomputers has been tested on workspaces with more than 10M bytes and has a 4G-byte theoretical limit. The mathematical formatted software runs under the VMS operating system and is file compatible with other high level languages running under VMX by using the RMS file system. Symbol table is limited only by the size of the available virtual memory. Compatible languages include VAX-11, FORTRAN, BASIC, COBOL, and C. Price is $13,800. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 351

Talk to the editors
Have you written to us lately? We're waiting to hear from you.

POWER SOURCES & PROTECTION

Auto-ranging transient protection for 480-V 3-phase lines

Model HT-4803-Y transient protection system features automatic range clamping at 20% above the voltage waveform on 3-phase, Y-connected systems. The noncurrent circuitry provides fast response time for optimum protection of MOS/TTL controlled devices, measuring systems with high impedance transducers, motor or generator insulation protection, op amps, or reduced line interference from flourescent panels. Transient dissipation power is 300 kW, 1 ms. The bipolar operating, fuse protected unit has 18″ (46-cm) leads and a 0.5″ (1.3-cm) conduit fitting. **Hi-Tech Systems, Inc,** 3985 N State Rd 39, Lebanon, IN 46052.
Circle 352

CONTROL & AUTOMATION

Simplified industrial control

RacPac 8 and RacPac 12 industrial rackmount enclosures hold the 1872+ industrial BASIC module, 1860+ Z80 CPU module, 9602 communications module, and an RS-232 cable, to allow startup of a BASIC language system. The 1872+ BASIC module provides complete support for development and execution of industrial control/monitoring programs. It contains an industrial BASIC system in EPROM ready for use. Battery backed 14k RAM (expandable to 30k) is provided for program storage. System expansion and reconfiguration are easily accommodated. **XYCOM Inc,** 750 N Maple Rd, Saline, MI 48176.
Circle 353

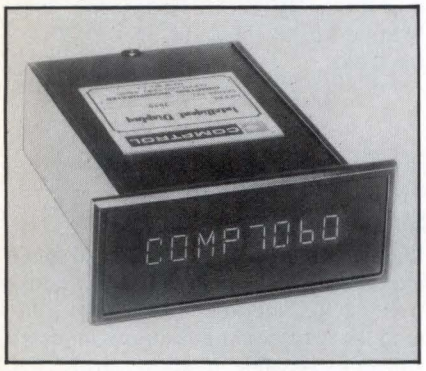
Speech synthesizer

CYBERCOMMAND™ add-on industrial control unit gives voice capability to a machine, process, or robot. Eight different speech/message channels are provided, each with a capacity for a 12-word sentence. Message priority sequence can be programmed. Memory stores vocabulary. Unit is easily interfaced to equipment via std sensors. The NEMA 4 enclosed unit has 10-W RMS audio power and requires 120-Vac 50/60-Hz, 2-A supply. Price is under $1600. **C. A. Briggs Co,** PO Box 151, Glenside, PA 19038.
Circle 354

Digital linear actuator

Digital linear actuator series L92200 provides step increments of 0.001″, 0.002″, or 0.003″ (0.003, 0.005, or 0.008 cm) in process control applications, and magnetic R/W head positioning in memory disk operations. Unit is a modified permanent magnet stepper motor that incorporates an internally threaded rotor fitted with a lead screw shaft that provides up to 4.5-lb (2.0-kg) linear force. Actuator has a max travel distance of 2.5″ (6.4 cm) and remains in position when current is removed. The units have an operating voltage of either 5 or 12 Vdc. Price is $38.40 each in quantities of 100. **AIRPAX Corp,** PO Box 768, Cheshire, CT 06410.
Circle 355

Intelligent display

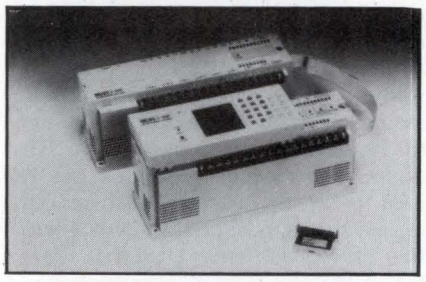


COMP7060 electronic sensing system monitors on/off status of machine pushbuttons, limit switches, motor starters, contactors, and relays. The intelligent display units enable control devices to communicate in English or other literal languages via 8-char displays/2045-char memory. When combined with COMP7580 input modules, system can monitor up to 112 on/off functions and display a user programmed message when 1 or more is activated. **Comptrol, Inc,** 9505 Midwest Ave, Cleveland, OH 44125.
Circle 356

Process control interface cards meet Eurocard specs

$M^2\pi$ memory mapped process interface meets Eurocard specs, provides M68000 compatibility, and complements VME products. The standalone cards require no I/O software drivers. CPU sees the interface as a memory mapped block of internal RAM, allowing the computer to access the realtime data base through simple read/write operations. Interleaving of multitasks is simplified by low level interrupts, and execution time becomes entirely predictable. Need for signal isolators, contact debounce, or digital filtering is eliminated. **Monitek, Inc,** 1495 Zephyr Ave, Hayward, CA 94544.
Circle 357

Compact progammable controller



F-20M programmable controller measures 25.5 x 8 x 10 cm and follows programs stored in either EPROM or RAM to handle as many as 20 I/O lines. The F-20E expansion unit doubles the number of I/O lines to a total of 24 inputs and 16 outputs. Std output has no voltage contact relay; triacs and transistors are optional. Power consumption is 11 VA. Reliability is 150k hours. Controller's microprocessor can perform up to 320 program steps at 0.1 ms/step. **Mitsubishi Electric Sales America, Inc, Industrial Products Div,** 3030 E Victoria St, Compton, CA 90221.
Circle 358

Low cost programmable CRT data logger

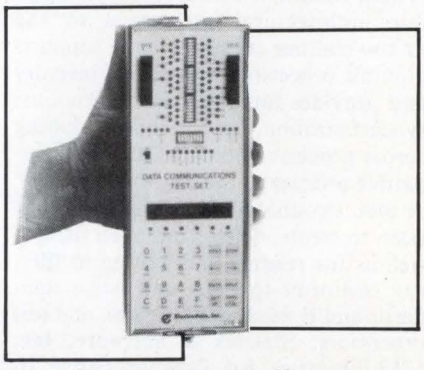
DIGI/SCAN 10C data logger with 7″ (18-cm) CRT display and printout recording provides 11-channel displays or alphanumeric display for single-channel use. Single-channel display shows process value, input type, engineering units, print interval, and channel number/time/date. Unit scans 16 channels (up to 960 channels optional) while displays are called on demand. Instant status report simultaneously shows all channels in alarm. There are no factory set limits; user sets all programs. **J & W Instruments, Inc,** 4800 Mustang Circle, New Brighton, MN 55112.
Circle 359

Digital controller for distributed/dedicated systems

Monitroller I 9-member series of single-loop digital process controllers for dedicated and distributed control environments accepts inputs from a range of sensors, transducers, and transmitters. It provides on/off or PID action on dual setpoints and communicates with peripherals via isolated data outputs. Features include 0.56″ (1.42-cm) high LED displays, solderless installation, front panel formatting of displayed process variable, and 3-key setup of operating parameters. Zero setpoint drift provides accurate process variable control. Prices start under $400, single quantity. **Analogic Corp,** 14 Electronics Ave, Danvers, MA 01923.
Circle 360

TEST & MEASUREMENT

Handheld communications test set



CTS 2 battery operated data communications test set diagnoses problems in RS-232 or V.24 systems. A combined EIA and communications tester, the unit is compatible with both full- and half-duplex synchronous, HDLC, and asynchronous systems. It can also test communications peripherals and also monitor/simulate digital data transmission anywhere in the data communications system. Receive and send buffers can hold up to 1023 chars each. Manually triggered or programmed automatic triggers can control receive data trapping and send buffer transmission. Price is $2795. **Electrodata, Inc,** 23020 Miles Rd, Bedford Heights, OH 44128.
Circle 361

Digi-Data Value Means:

FASTER DISK BACK-UP AT LOWER COST

Digi-Data's new Series 2000 Streamer will back-up your disk at up to 9.3M bytes per minute. It can record 1600 bpi densities at 125 ips, or 3200 bpi density at 62.5 ips. That means you can back-up 92M bytes on a single tape reel in under 10 minutes . . . including rewind. And the Series 2000 is ANSI/IBM compatible with start/stop speeds of 25 or 12.5 ips available.

We designed the Series 2000 for 3200 bpi from the start. Step-write . . . microprocessor controlled read electronics . . . and extended de-skew buffer are some of the unique Digi-Data features that make 3200 bpi operation more reliable. Check other streamers for comparable features.

The Series 2000 benefits from our 20 years experience in tape drive design. Microprocessor controlled calibration and power-up diagnostics are standard. Sensors are solid state and I/O lines are properly terminated. There are no loud vacuum blowers. And the number of moving parts has been minimized.

At 50 lbs and less than 19″ depth, you won't find a smaller 1/2″ streamer. Best of all, prices start at $1850. in large OEM quantities.

The Series 2000 is complemented by a full line of 1/2″ and 1/4″ tape drives for conventional start/stop operation.

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Jessup, MD 20794
(301) 498-0200 TWX 710-867-9254
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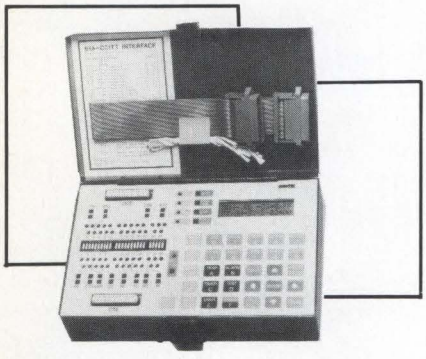
In Europe contact:
Digi-Data Ltd.
Kings House, 18 King Street
Maidenhead, Berkshire
England SL6 1EF
Tel. No. 0628 29555-6
Telex: 847720

CIRCLE 149

Dealer Inquiries Welcomed

Data communications diagnostics

Datatest 2 data comm test set provides all test functions and their parameters with dedicated keys. Parameter selections are shown in the 32-char alphanumeric display. Unit has bert, monitor, echo, poll, and Xmit test modes. Parameters include full-, half-duplex, or multidrop line; number of bits/char; asynchronous 1 or 2 stop bits, synchronous, isochronous, and SDLC protocols; internal or external clock; and user programmable speed. Circuits can be reconfigured for DTE or DCE simulation on the same connector. Accepted codes are Hex, ASCII, and EBCDIC. Price is $1895. **Navtel Ltd,** 8481 Keele St, Unit 11A, Concord, Ontario, Canada L4K 1B1.



Circle 362

Data communications tester, development tool

Chameleon data communications test tool with multiprotocol analysis and simulation capability has dual Sony 3½" floppy drives with 350k storage formatted. Max transfer rate is 500k bps. Detachable numeric keyboard with 92 keys (10 programmable function keys), 9" (23-cm) CRT with 80- x 24-char resolution, and remote I/O port are provided. Memory is 74k RAM, 40k PROM. Auxiliary I/O port for remote control or line printer support and slave printer port are provided. HDLC, SDLC, X.25, bisync, and SNA/SDLC protocols are supported. Price is $18,000. **Tekelec Inc,** 2932 Wilshire Blvd, Santa Monica, CA 90403.

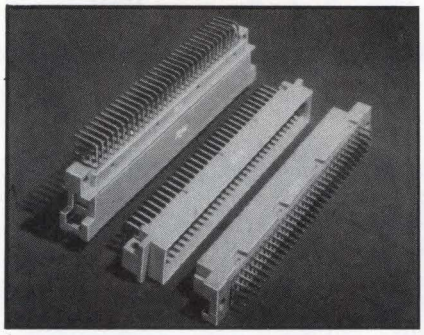
Circle 363

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? Turn to the Editorial Score Box on the Reader Inquiry Card.

INTERCONNECTION & PACKAGING

DIN connectors



RNE series DIN connectors provide up to 50% more I/O connectors per lineal foot with an installed cost approximating edge cards with gold PCB pads. Connectors come in 2- or 3-row bodies with 64 or 96 contacts. Termination styles include right angle or straight solder, wrap pin, or IDC for flat cable use. The 3-row units come in std or reverse mounting styles. Prices for mated pairs in 1k lots range from $2.56 to $3.46 each. **Robinson Nugent, Inc,** 800 E 8th St, New Albany, IN 47150.

Circle 364

Single-channel fiber optic connector

FW series single-channel optical connector has a conical plug molded directly around the fiber. The fiber is located along the cone axis for concentricity. Interconnection is via threaded-style coupling nut. Biconical sleeve mates the connectors. Since the connector is molded directly to the cable, jumpers are supplied in predetermined lengths. Pig-tail plugs are also available. **Automatic Connector, Inc,** 400 Moreland Rd, Commack, NY 11725.

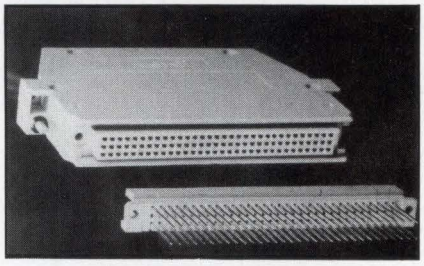
Circle 365

Mass termination for DIN 41612/41613 connectors

Two 64-position mass termination socket connectors for pluggable interface to DIN 41612 and 41613 connectors are available with either 2- or 3-row bodies, and with grid spacings of 2.54 x 2.54 mm or 2.54 x 5.08 mm. Both connectors are available with/without mounting flanges and with gold-plated contact areas. With Scotchflex manual or pneumatic presses, all connections are made in a single operation. The "U" contacts pierce the insulation and displace it from the conductors to ensure gas tight, corrosion resistant, and electrically uniform contact. The connectors can be daisy chained or endmounted on the cable. Strain relief clips and pull tabs are available. **3M, Electronic Products Div,** PO Box 33600, St. Paul, MN 55133.

Circle 366

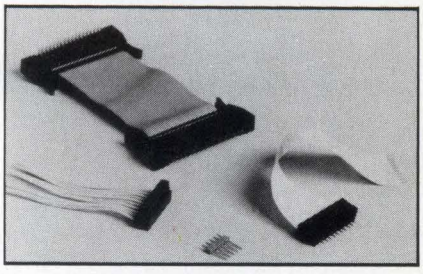
Domestically produced Eurocard connectors



DIN 41612 Eurocard receptacles and headers have 2-part design to improve typical card-edge systems through 3-row contact density and shroud that provides polarized coupling reliability. Family includes 2-row std sex and 3-row versions in std and reverse sex configurations. Glass-filled polyester 94 V-0 housings have a dielectric rating of 1000 Vac between contacts for 1 min. PCB mounting options include wrap type posts, solder tails, or compliant pins for solderless pressfit backplane construction. **AMP Inc,** Harrisburg, PA 17105.

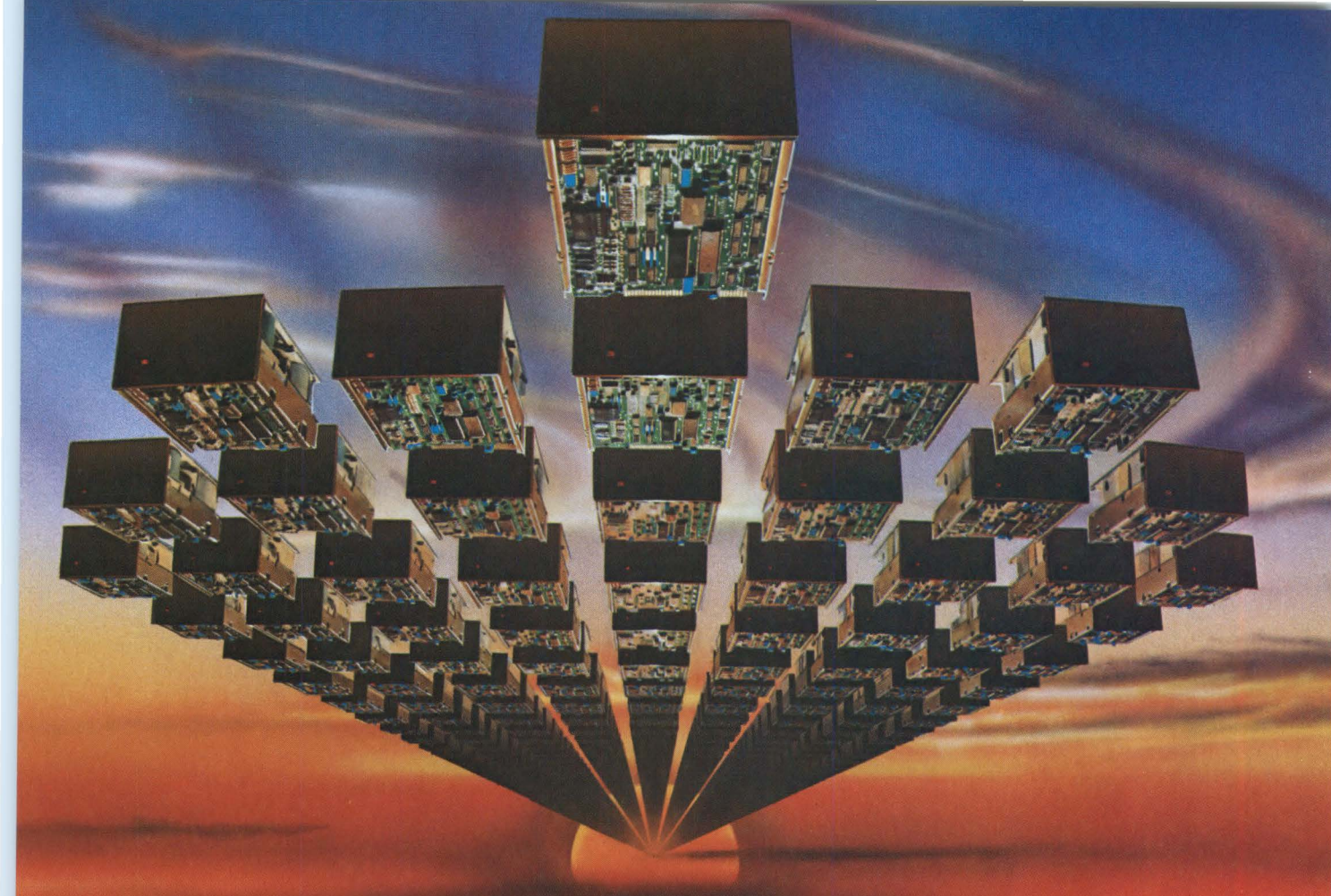
Circle 367

Cable connectors for PCBs



RA, NR, and FR insulation displacement connectors have twin U-slot parallel beams and double-leaf contact with point of contact dimples. RA and NR series features 2-die precision stamping and selective gold-plating. RA connector is used with a 0.05" (0.13-cm) center ribbon cable and meets MIL-C-83503 specs. NR connector can be used with ribbon cable or with optional 22-28 gauge discreet wires. Base assembly eliminates most flux problems. FR ZIF positive connector is used with flat flexible cable having 0.1" (0.3-cm) centers and membrane switches. **J.S. Terminal Corp of America,** 2420 E Oakton St, Arlington Heights, IL 60005.

Circle 368



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CIRCLE 150

VICOM Digital Image Processor

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The VICOM Digital Image Processor is a powerful new computing tool designed to handle a variety of image processing applications. VICOM has the capability and flexibility to help you get your job done... quickly and efficiently.

VICOM is versatile. It can operate as a real-time scene analyzer with an electronic camera input, a peripheral processor to a host computer, or a stand-alone digital image processor, complete with magnetic tape and hard disk storage units.

VICOM's internal Motorola 68000 Microcomputer can be configured as a firmware-based interactive image processing system or as a disk operating system with resident FORTRAN, PASCAL, and assembly capability — as well as interactive image processing.

Also, the VICOM image/graphics memory stores over four million sixteen-bit pixels. Internal point and array processors operate at video rates. Arithmetic, logical and convolution operations execute in a fraction of a second.

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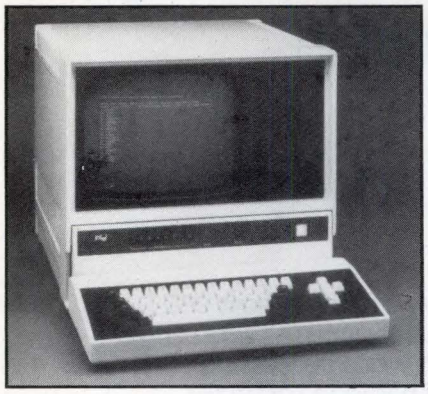
For information only 165

For immediate interest 151

Enhanced development system



Series-IIE/iMDX-225 enhanced version of the Intellec Series-II microcomputer development system features command line editing and recall, file viewing and job batching, preprogrammed soft keys, and keyboard help function. Cursor provides direct addressability. Page and line by line scrolling, along with a 1k-byte data redisplay capability are supported. The $12,500 system is upgradable to a Series-III 16-bit development system. It has a single flexible disk drive, 64k-byte RAM, detachable keyboard, 12″ (30-cm) CRT, and 8085A-2 4-MHz CPU. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 369

Cutting software costs with 6809 interface programming

Videotaped short course "6809 Interface Programming" teaches how to use the 8-bit 6809 microprocessor through a series of twelve 30-min color lectures. Programming techniques, potential gains with the 6809, and effective interface to cut costs are emphasized. Course is geared toward OEMs who design/maintain 6809 controlled equipment; use PIC, block structure, or reentrant programming methods; or build dedicated or standalone systems. **Colorado State University, Engineering Renewal & Growth Program,** Christman Field, Bldg 1000, Fort Collins, CO 80523.
Circle 370

Like to write?
The editors invite you to write technical articles for Computer Design. For a free copy of the Author's Guide, circle **503** *on the Reader Inquiry Card.*

DoD spec Ada compiler for mil computers

Fully implemented DoD ANSI 1982 spec Ada compiler and Ada development environment (ADE) coupled with a multiterminal 32-bit computer, the Ada Work Center allows from 8 to 128 simultaneous users to develop Ada language applications. The Work Center package includes hardware, software, and technical support for Ada development on a full range of ROLM 16- and 32-bit computers. The Ada compiler implements all defined Ada functions; compilation rate exceeds 1200 lines/min. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 371

SYSTEM ELEMENTS

Touch sensitive, transparent I/O panel

Model 3003 membrane touch panel mounts in front of a display, minimizes keyboard use, and allows the entire display to be used as an I/O device. Panel is a normally open transparent membrane switch that operates through a momentary contact touch sense. Available in both matrix and analog formats, custom designs can be provided. Membrane achieves 85% max transparency for use as an overlay control panel. Panels can be backlighted with a graphic display and used as a normal touch switch. They are available in either flat- or single-dimensional form. **Transparent Devices, Inc,** 756 Lakefield Rd, Westlake Village, CA 91361.
Circle 372

Speech synthesizer

"Cheaptalk" CT-200 self-contained speech synthesizer board holds up to 3 s of speech. Total playback time can be partitioned into 1, 2, 4, or 8 equal intervals to hold multiple words or phrases. Boards can be cascaded for longer continuous recordings. The 3″ x 3.25″ (8- x 8.26-cm) board requires switches or TTL control logic to operate. Signals also provide microprocessor interface. Three TTL compatible phrase select lines are addressed for multiphrase boards. Operating power is 5 V at 200 mA max. OEM quantity price is $68. **DataVoice Corp,** 2 N LaSalle St, Chicago, IL 60602.
Circle 373

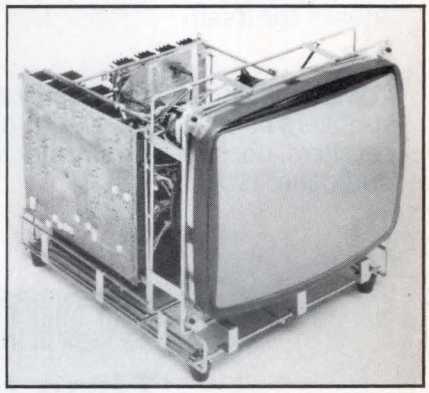
Momentary pushbutton switches

Series 581 snap action momentary pushbutton switches mount through a 0.25″ (0.64-cm) hole and have a short, pretravel plunger action for fast response time. Contact ratings are available for high and low current levels. The spdt or dpdt switches have epoxy sealed terminals in solder, PC, and wirewrap configurations that range in length from 0.75″ to 1.062″ (1.91 to 2.697 cm). Price is $1.33 each in 1k quantity. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 374

High resolution monochrome display

A 12″ (30-cm) diagonal monochrome computer display model TR120M1P features a direct etched faceplate to minimize glare and a 1100-line resolution display. Video bandwidth is 20 MHz. The display easily reproduces 80- x 25-char displays or computer graphics through green P31 phosphors. Video looping connector and an integral audio system are also featured. The UL listed unit carries an FCC class B certification. Retail price is $220. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094.
Circle 375

Color raster monitor with 1024 noninterlaced lines



KM1400 raster scan color video monitor has noninterlaced lines to display twice as much data in any given frame as a comparable interlaced monitor. This feature, combined with 0.031-cm triad spacing, eliminates jagged lines known as "stair casing." P22 screen has 60-Hz refresh rate. Video amplifier has a bandwidth of over 100 MHz; rise and fall times are 3.5 ns. **Kratos Display Systems,** 101 Cooper Court, Los Gatos, CA 95030.
Circle 376

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COMDEX means **Business** and spells **Opportunity** for you in 1983! This year you can get an early start at COMDEX/Spring '83 in the Georgia World Congress Center and The Atlanta Apparel Mart, Atlanta, Georgia, April 26-29. Don't let the competition get the jump on you. Take advantage of the earliest possible information on new products and services ... It's smart business! And COMDEX/Spring is your first **real** opportunity to see the latest industry offerings.

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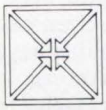

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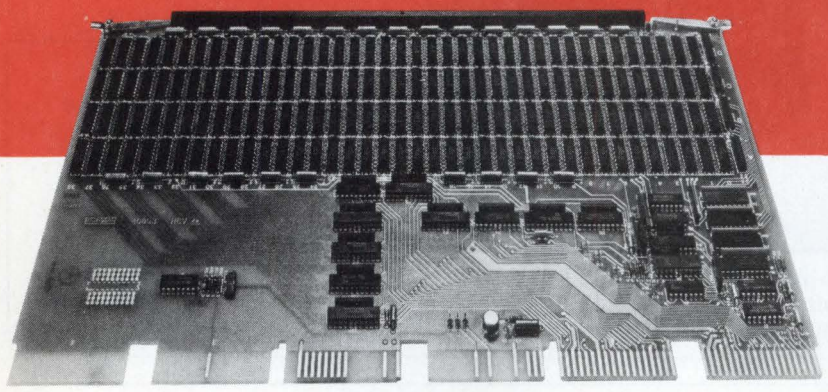
CIRCLE 163

DEC-COMPATIBLE SEMI ADD-INS

NEW!
1.0 MB VAX 730
1.0 MB VAX 750
2.0 MB VAX 780



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DEC Mini	Dataram ADD-IN	Board Size	Maximum Capacity
LSI-11®	DR-115S	dual	64 KB
LSI-11	DR-215	dual	256 KB
LSI-11	DR-213	quad	1.0 MB
PDP®-11	DR-114S	hex	256 KB
PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214	hex	1.0 MB
PDP-11	DR-144	hex	256 KB
PDP-11	DR-244	hex	1.0 MB
VAX®-11/750 PDP-11/70	DR-175	hex	256 KB
VAX-11/750 VAX-11/730	DR-275	hex	1.0 MB
VAX-11/780	DR-178	extended hex	512 KB
VAX-11/780	DR-278	extended hex	2.0 MB
DECSYSTEM 2020®	DR-120	extended hex	256 KB

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Dataram also provides core ADD-INs, core and semiconductor ADD-ONs, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

CIRCLE 153

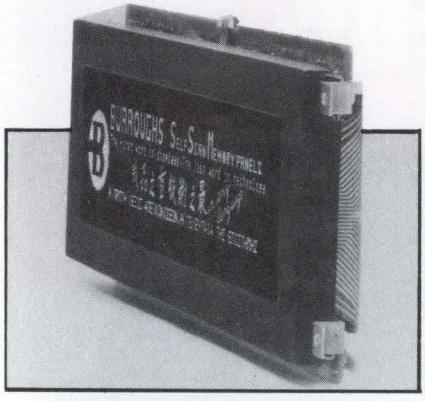
Low cost industrial encoder

ILC series encoder, priced under $100, features 0.38″ (0.95-cm) diameter double-ended stainless steel shaft and widely spaced bearings that withstand 100-lb (45-kg) shaft load. Dual-shaft ends facilitate connection to machine elements, or the encoder can be placed directly in the power train. Sealed bearings and a gasketed, heavy walled housing are used. Up to 1200 pulses per revolution, square wave TTL or CMOS complementary outputs, are provided at 5 to 15 V. Optional gated marker pulse and line driver outputs are available. **Motion Control Devices, Inc,** 80 Stedman St, Lowell, MA 01851.
Circle 377

Touch membrane switches

Textur Touch membrane switch uses a G10 glass epoxy double-sided substrate board with tin-plated conductors and plated through holes. Membrane switch assemblies with LEDs mounted onboard can be supplied. A variety of connectors can be mounted on the substrate to enable connection to the system. T/T HES series has built-in graphite static shields or silver grid emi shields. A 0.5″ (1.3-cm) between center spacing switch matrix can be provided. Smooth or glossy surface finishes can be selected from among 50 tactile textures. **CAM Graphics Co, Inc,** 145 Toledo St, Farmingdale, NY 11735.
Circle 378

CRT replacement panel



Self-Scan® gas plasma display with memory flat panel is an 80-char line width, 400-char panel that can display both alphanumerics and graphics. The dc internal address feature is combined with a technology that incorporates an ac layer for storing data in memory indefinitely. The ac memory layer eliminates need for refresh memory electronics and, with 400-char display, reduces the number of required drivers from 656 to 25. Optional touch-sensitive overlay allows direct data input. Price for the 400-char model with driver electronics is $625 in OEM quantities. **Burroughs OEM, Display Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 379

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Retro-Graphics™ and DEC.

Now GEN.II™ delivers Tek 4010/4014/4027 compatible graphics on your VT100, VT101, VT102, VT103, VT131, or VT132.

Generating cost-efficient yet sophisticated images on your DEC™ terminal first begins with your choice of VT100™-Series displays. Then add Digital Engineering's GEN.II Retro-Graphics terminal enhancement. Our plug-in upgrade transforms an otherwise "dumb" terminal into a multi-featured bit-map graphics workstation, capable of plotting complex business and technical renderings. In a raster-scan resolution of 800 by 480 and in concert with your Tektronix®-based program.

But best of all a Retro-Graphics enhancement costs only a fraction of what you'd pay for an equivalent graphics terminal: about $1200 - 1800, depending on the GEN.II model you order.

Introducing GEN.II Retro-Graphics for DEC.
More graphics power and Tek™ simulation.

An easily installed PC card assembly, our second-generation enhancement provides emulation of the Tektronix 4010 graphics terminal *plus* one-color simulation of the Tek 4027 color graphics terminal.

And for extra power — and compatibility with your existing or future Tek 4014 applications programs — *GEN.II for DEC also features one-color 4014 simulation.* With little or no software modification.

In addition, GEN.II's 32 Kb's of "local" intelligence ensures that images come up quickly — and costly terminal-host data transmissions are held to a minimum. And because GEN.II is based on industry-standard Tektronix protocol, graphics programming and operation are considerably eased. Case in point: by entering from the keyboard or computer the following command string

!PIE 100, 0, 360, 45

an eight-sided *polygon* with a radius of 100 will be plotted and its interior will be *filled* with a shading pattern (GEN.II maps 4027 colors to dithered shades).

With similar high-level command strings, GEN.II will also perform *arc* and *vector drawing. Define* and *shape text characters. Store* and *recall* graphs. And, while in 4014 mode, *perform additional graphics annotation using all four 4014 character sets.* And you get all this with no loss of existing terminal features.

Software compatibility ensures your long-term investment.

Since our GEN.II products for DEC provide 4010/4014/4027 compatibility, their use with utility and applications programs, whether now or in the future, is guaranteed. Currently, more than 20,000 Retro-Graphics products are performing successfully on graphics programs such as DISSPLA® and TELLAGRAF®, PLOT 10™, Template™, DI-3000™, and ILS®.

Graphics I/O and solid backup throughout.

Digital Engineering has built a solid foundation of "user-chosen" interactive tools for GEN.II. For instance, a crosshair cursor and light-pen port (for our optional light pen) are standard features, while optional interfaces allow you to simultaneously interact with a digitizer while outputting to an impact or non-impact serial printer and video device.

Comprehensive documentation assists at every level of operation. A worldwide distribution network assures prompt delivery and backup. And whether you tap our service network or opt for on-site service — from one of the largest field service organizations in the world — your needs will be quickly met.

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CIRCLE 154

CONFERENCES

MAR 8-10—Localnet, London, England. INFORMATION: Online Confs Ltd, Argyle House, Northwood Hills, HA6 1TS, Middx, U.K. Tel: Northwood 09274/28211; 44/9274 28211 (internat'l)

MAR 10-12—Internat'l Computer Color Graphics Conf, Tallahassee-Leon County Civic Ctr, Tallahassee, Fla. INFORMATION: Ron Spencer, 555 W Pensacola St, PO Box 10604, Tallahassee, FL 32302. Tel: 904/487-1691

MAR 14-16—Phoenix Conf on Computers and Communications, Phoenix, Ariz. INFORMATION: Gerald Fetterer, GTE Automatic Electric Lab, 2500 W Utopia, Phoenix, AZ 85027

MAR 21-24—Interface, Miami Beach Conv Ctr, Miami Beach, Fla. INFORMATION: The Interface Group, 160 Speen St, PO Box 927, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 21-24—Powercon 10 (Internat'l Power Electronics Conf and Exhibit), Sheraton Harbor Island Hotel, San Diego, Calif. INFORMATION: Ronald Birdsall, Gen'l Chmn, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/656-1890

MAR 22-23—Office Automation Conf and Expo, Holiday Inn Mövenpick Hotel, Zurich-Regensdorf, Switzerland. INFORMATION: Foreign Commercial Service, American Embassy, PO Box 1065, CH-3001, Bern, Switzerland. Tel: 031/437011

APR 4-8—Tutorial Week East (including sessions on interactive computer graphics; robotics; data communication; and software design, development, management, and testing), Orlando, Fla. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 5-8—Communications Tokyo, Tokyo Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak Internat'l, PO Box 70007, Washington, DC 20088. Tel: 301/657-3090

APR 13-20—Hannover Fair, Hannover, West Germany. INFORMATION: Hannover Fairs Information Ctr, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

APR 18-21—Internat'l Sym on Industrial Robots/Robots 7 Conf and Expo, Conrad Hilton Hotel and McCormick Pl, Chicago, Ill. INFORMATION: Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

APR 19-21—Electro, New York Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 19-21—Mini/Micro-Northeast, New York Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 27-29—Satellite and Computer Communications Internat'l Sym, Versailles, France. INFORMATION: T. Bricheteau, Secretariat du Symposium, Domaine de Voluceau, Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France. Tel: 3/954.9020; Poste 600

MAY 2-5—Test and Measurement World Expo, San Jose Conv Ctr, San Jose, Calif. INFORMATION: Meg Bowen, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

MAY 9-13—SID (Society for Information Display) Internat'l Sym, Marriott Hotel, Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

MAY 10-12—Mini/Micro-Northwest, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

MAY 10-12—Northcon, Portland Coliseum, Portland, Ore. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

MAY 16-18—Electronic Components Conf, Contemporary Hotel, Orlando, Fla. INFORMATION: Don L. Willyard, Bendix Corp, Dept 867 MF39, PO Box 1159, Kansas City, MO 64141

MAY 16-19—NCC (National Computer Conf), Disneyland Hotel and Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3624

MAY 18-20—MIPRO (Microprocessors/ Microcomputers Course/Conf), Congress Ctr, Hotel Adriatic, Opatija, Yugoslavia. INFORMATION: P. Dragojlović, MIPRO Secretariat, Trg P. Togliatti 4, 51000 Rijeka, Yugoslavia. Tel: +38 51 31 211 X424 (am); +38 51 741 494 (pm)

MAY 25—Automating Intelligent Behavior: Applications and Frontiers, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Marvin Denicoff, Trends and Applications 83, PO Box 639, Silver Spring, MD 20901. Tel: 202/696-4302

JUNE 13-16—Internat'l Conf on Computer Architecture, Stockholm, Sweden. INFORMATION: H. W. Lawson, Jr, Linkoping Univ, S-581 83, Linkoping, Sweden

SEMINARS

MAR 7-11—Computer Aided Engineering and Manufacturing Seminars and Exhibition, North Carolina State Univ, Raleigh, NC. INFORMATION: R. L. Edwards, Industrial Extension Service, North Carolina State Univ, PO Box 5506, Raleigh, NC 27650. Tel: 919/737-3470

MAR 21-23—Digital Control, Boston, Mass. INFORMATION: Hellman Assocs, Inc, Dept R, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

SHORT COURSES

MAR 21-24—Personal Microcomputer Interfacing and Scientific Instrumentation Automation, Virginia Polytechnic Institute and State Univ, Blacksburg, Va. INFORMATION: Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. Tel: 703/961-4848

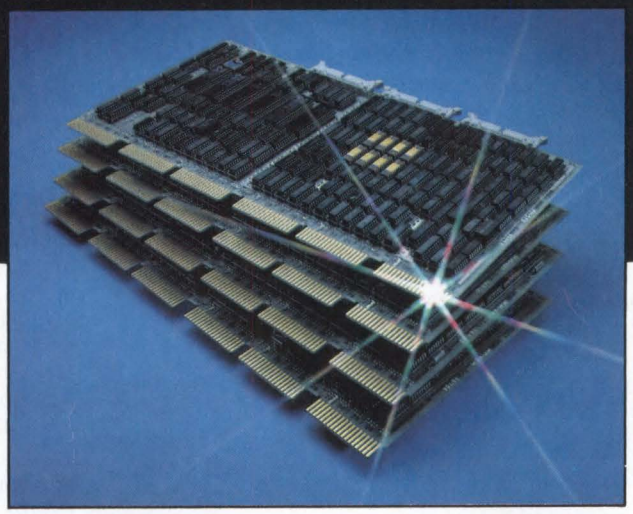
MAR 23-24—Strategic Planning for Office Automation, Watergate Mall, Washington, DC. INFORMATION: Nancy Anderson, Micronet/KSI, 2551 Virginia Ave NW, Washington, DC 20037. Tel: 202/333-4800

MAR 30-31—IEEE VLSI Test Workshop, Bally's Park Place Casino Hotel, Atlantic City, NJ. INFORMATION: Jerry Kunert, Naval Air Engineering Ctr, Code 92A32, Lakehurst, NJ 08733. Tel: 201/323-2663

MAR-APR—Digital Processing; Graphics, CAD/CAM & Robots; Microprocessors; Networks & Systems; and Software, various cities and dates. INFORMATION: Integrated Computer Systems, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/ 450-2060; 800/421-8166 (outside Calif)

MAR-JUNE—Digital Systems, Process Control, and Instrumentation, various cities and dates. INFORMATION: Administrator, Training Ctr, Instrument Society of America, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

Discover The OEM Array Processor.



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CIRCLE 155

Industrial control microcomputer
Digest describes CINCH™ microcomputer as a host working with CINCHNET™ multiple access, industrial local area network, detailing hardware specs and system applications; programming examples demonstrate CINCH BASIC language. **Control Logic, Inconix Corp,** Natick, Mass.
Circle 410

Touch-sensitive displays
Brochure gives overview of applications for touch-sensitive technology in computer display terminals and components. **Interaction Systems, Inc,** Newtonville, Mass.
Circle 411

Composite input video
Booklet highlights BHD series 5″, 9″, and 12″ monitors, which accept standard composite video signals from 0.5 to 2.5 V peak to peak, negative sync, and offer optional dynamic focus. **Dotronix, Inc,** New Brighton, Minn.
Circle 412

Audio spectrum analyzer
Booklet introduces model 7800 Digital Sona-Graph, a dc to 16-kHz spectrograph that combines features of a conventional spectrum analyzer, a 3-D display, a high resolution gray scale printer, and an oscilloscope. **Kay Elemetrics Corp,** Pine Brook, NJ.
Circle 413

Electrostatic CRTs
Brochure illustrates large screen directed-beam displays for instrumentation and design graphics, listing applications and performance specs. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 414

Heat sinks and accessories
Catalog profiles units in various configurations that slide or fasten into semiconductor packages; standard and custom extrusions for high current devices are included. **Aavid Engineering, Inc,** Laconia, NH.
Circle 415

Console and handheld trackballs
Pamphlet covers electrical, mechanical, and environmental specs for compact interface, which has 62- to 500-cycle resolution for one complete rotation. **Litton Systems, Inc, Encoder Div,** Chatsworth, Calif.
Circle 416

High voltage CRT power
Leaflet describes power supplies with high speed dynamic focus, control logic to enable high voltage and provide a delay for filament warm-up, and proprietary linear circuits for low noise. **Bertan Associates, Inc,** Syosset, NY.
Circle 417

Data acquisition
Tutorial sections complement individual data sheets for product line, including data converters, op amps, signal conditioners, computational circuits, power supplies, digital panel instruments, subsystems and systems for measurement/control, and linear component test systems. **Analog Devices,** Norwood, Mass.
Circle 418

Network diagnostics and performance
Datalyzer™ option for Analysis automated network management system is examined in booklet that cites performance with host computer traffic, response time reporting, and in-service parameters with color graphic and statistical displays. **Paradyne Corp,** Largo, Fla.
Circle 419

CMOS industrial single-board computer
Data book covers Series/800 CMOS industrial microcomputer board, based on proprietary P²CMOS process, and BLMX-80C multitasking operating system; line includes CPU, memory expansion, and digital and analog I/O boards. **National Semiconductor,** Santa Clara, Calif.
Circle 420

AC/DC industrial motors
Catalog presents variety of ac motors and dc rectified power motors with detailed engineering data, evaluating motor efficiency and performance, as well as motor selection and applications. **Reliance Electric Co,** Cleveland, Ohio.
Circle 421

Digital microcircuits
Technical and design data are given on microcircuits dedicated to the computer and communications industries, including ROM, electrically alterable nonvolatile memories, microcomputers, audio, telephony, data communications, ULA, video, and tuning. **General Instrument Corp, Microelectronics Group,** Hicksville, NY.
Circle 422

Integrated office system
Brochure explains task switching, I/O, design and expansion, and complete specs for Omny OEM integrated office system, based on Motorola's 68000. **ShareData, Inc,** St Paul, Minn.
Circle 423

RFI/EMI power line filters
Cross-reference lists general purpose and specialized filters for electronic data processing equipment, including filters for switched-mode power supplies. **Sprague Electric Co, sub of GK Technologies,** North Adams, Mass.
Circle 424

Hybrid power modules
Product guide gives descriptions, electrical/mechanical specs, and applications ideas for 12- and 15-V, 15-W modules. **Power Products, Div of Computer Products, Inc,** Pompano Beach, Fla.
Circle 425

Permanent magnet, brushless motors
Brochure examines servomotors, tachometers, general purpose brushless motors, and commutation electronics, highlighting characteristics for ferrite and rare earth magnet versions. **Honeywell Motor Products Div,** Rockford, Ill.
Circle 426

Semicustom circuit tools
Leaflet introduces HIGHLAND software system for automated semicustom gate array development; logic designer specifies data files for VLSI, then company creates masks and test tapes. **United Technologies Mostek, Microelectronics Center,** Carrollton, Tex.
Circle 427

Power supplies
Product reference gives specs and application information on wide range of general purpose and specialized power supplies, along with redundant output power systems. **Acopian Corp,** Easton, Pa.
Circle 428

High frequency ICs
Applications reference covers high speed dividers, digital signal processing, UHF and VHF synthesis, A-D conversion, power and motor control, and op amp design. Request on company letterhead (for $6.50) from **Plessey Semiconductors,** 1641 Kaiser Ave, Irvine, CA 92714.

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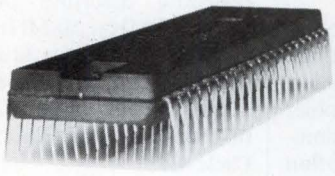

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CIRCLE 172

Flat cable connection
Catalog illustrates design features and performance characteristics of Cinch Superfast™ connector system, with type I, II, and III headers, sockets, DIP plugs, PC edges, PCB connections, and 9 standard termination sizes. **TRW Electronic Components Group, Connector Div,** Elk Grove Village, Ill.
Circle 429

Switch mode power supplies
Quad-output Cool-1 series 130-, 150-, 170-, and 200-W models are profiled in bulletin showing features, specs, and dimensional drawings. **Deltron Inc,** North Wales, Pa.
Circle 430

Precision resistor networks
Catalog describes miniature precision resistor networks using Bulk Metal® foil technology for lightweight applications. **Vishay Resistive Systems Group,** Malvern, Pa.
Circle 431

Advanced computer science
Brochure summarizes university research on VAX and PDP-11 systems in robotics, intersystem communication, database management, local area networks, language development, and VLSI processor design applications. **Digital Equipment Corp,** Maynard, Mass.
Circle 432

Electrical components
Technical data specifies pin, socket, flat flexible circuit, and 0.050″ center ribbon cable connectors; PCB interconnection systems; solderless terminals; insulation displacement products; switches; sockets; and applications tooling. **Molex Inc,** Lisle, Ill.
Circle 433

Multilayer ceramic capacitors
Bulletin tabulates capacitance values, tolerances, working voltages, various failure rate levels, and ordering information for mil-spec, molded radial-lead, axial-lead, 2-pin DIP, and chip type models. **AVX Ceramics,** Myrtle Beach, SC. **Circle 434**

MULTIBUS interconnections
Catalog profiles 6-slot version of press-fit backplanes and card frames, socket boards with continuous groundplane on wiring side, expander cards for testing and debugging, and related services from custom pinning to wirewrapping. **Hybricon Corp,** Littleton, Mass.
Circle 435

Dew point sampling
Application bulletin 3-052 discusses design factors in system development, including materials selection, effects of sample leakage on dew measurement, pressure/dew point relationship, and hygroscopic properties of various materials. **EG&G Environmental Equipment Div,** Waltham, Mass.
Circle 436

Adjustable-speed dc drives
Bulletin highlights DRIVEPAK controllers for 5- to 500-hp dc drive that incorporate SCR control technology, using 6-pulse, full-wave power conversion for cooler motor operation and improved commutation. **Contraves Goerz Corp, Motion Control Div,** Pittsburgh, Pa.
Circle 437

Color graphics
Jupiter 7 raster terminal, which offers 768- x 575-pixel resolution and 256 simultaneously displayable colors, is introduced in brochure that suggests electrical CAD and scientific applications. **Jupiter Systems, Inc,** Berkeley, Calif. **Circle 438**

Three-phase inverter
Data sheet describes 15-kW inverter system for 48-Vdc applications, with specs on I/O, environmental ratings, physical dimensions, and dc noise. **LorTec Power Systems, Inc,** North Ridgeville, Ohio.
Circle 439

RFI power line filters
Catalog examines basic filter technology and selection, in addition to product descriptions with electrical schematics, 50-Ω insertion loss data, and applications suggestions. **Corcom Inc,** Libertyville, Ill.
Circle 440

Adjustment knobs
Knurled, ribbed, fluted, notched, and scalloped knobs produced in nylon and engineering plastics for light and heavy duty applications are profiled in fold-out booklet. **Plastiglide Manufacturing Corp,** Hawthorne, Calif.
Circle 441

Proximity switches
Main parameters for flush and exposed mounting types are outlined in brochure that examines 52 inductive models for detecting metals and 12 capacitive models for solids and liquids. **Photobell Co, Inc,** Fairfield, NJ.
Circle 442

Data communications equipment and peripheral controllers
Bulletin covers computer products compatible with DEC PDP-11/LSI-11 and Data General NOVA/Eclipse systems; advanced FORTRAN IV utilities for NOVA/Eclipse; and support products. **GEN/COMP Inc,** Canton, Mass.
Circle 443

Oscilloscope line
Brochure describes performance of 15- to 35-MHz, 50-MHz, and 100-MHz models, detailing features like calibrated delayed-sweep/dual time base, alternate triggering, and variable holdoff. **Leader Instruments Corp,** Hauppauge, NY.
Circle 444

High speed thermal printhead
Leaflet sets forth features, functional operation, and performance characteristics of SM 20100, which comes in 20-column format that gangs up for 40-, 60-, and 80-column assemblies. **Gulton Industries, Inc, Hybrid Microcircuit Dept,** Metuchen, NJ.
Circle 445

Digital panel meters
Slimline series short-form catalog specifies meter line including display-only, BCD output, and serial ASCII output. **Nationwide Electronic Systems, Inc,** Streamwood, Ill.
Circle 446

Microcomputer interference control
Protective devices, line voltage regulators, and ac power interrupters are described in booklet that reviews typical problems, solutions, and applications. **Electronic Specialists, Inc,** Natick, Mass. **Circle 447**

MOS/LSI data book
Product bulletin describes function, usage specs, and essential parameters for data communication, CRT displays, floppy disk controllers, printers, baud rate generators, keyboard encoders, and microprocessor peripherals. **Standard Microsystems Corp,** Hauppauge, NY.
Circle 448

Network control modems
Product specs, applications diagrams, and functional charts for CS series high speed modems are outlined for operating environments using integrated data transportation and network management. **Codex Corp, Motorola Inc Information Systems Group,** Mansfield, Mass.
Circle 449

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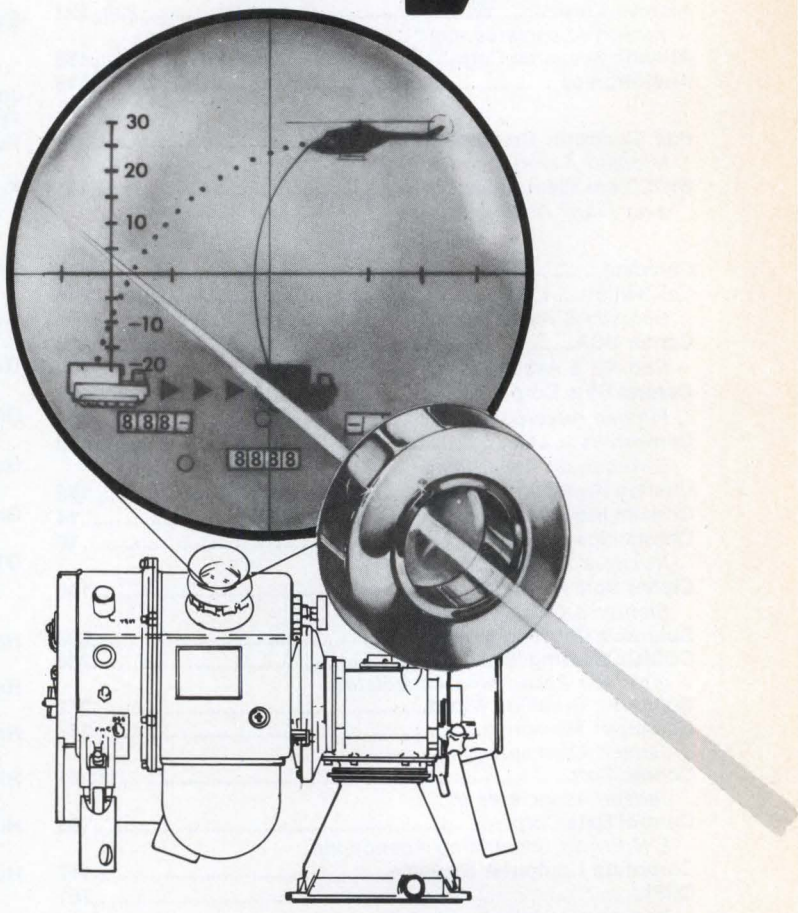

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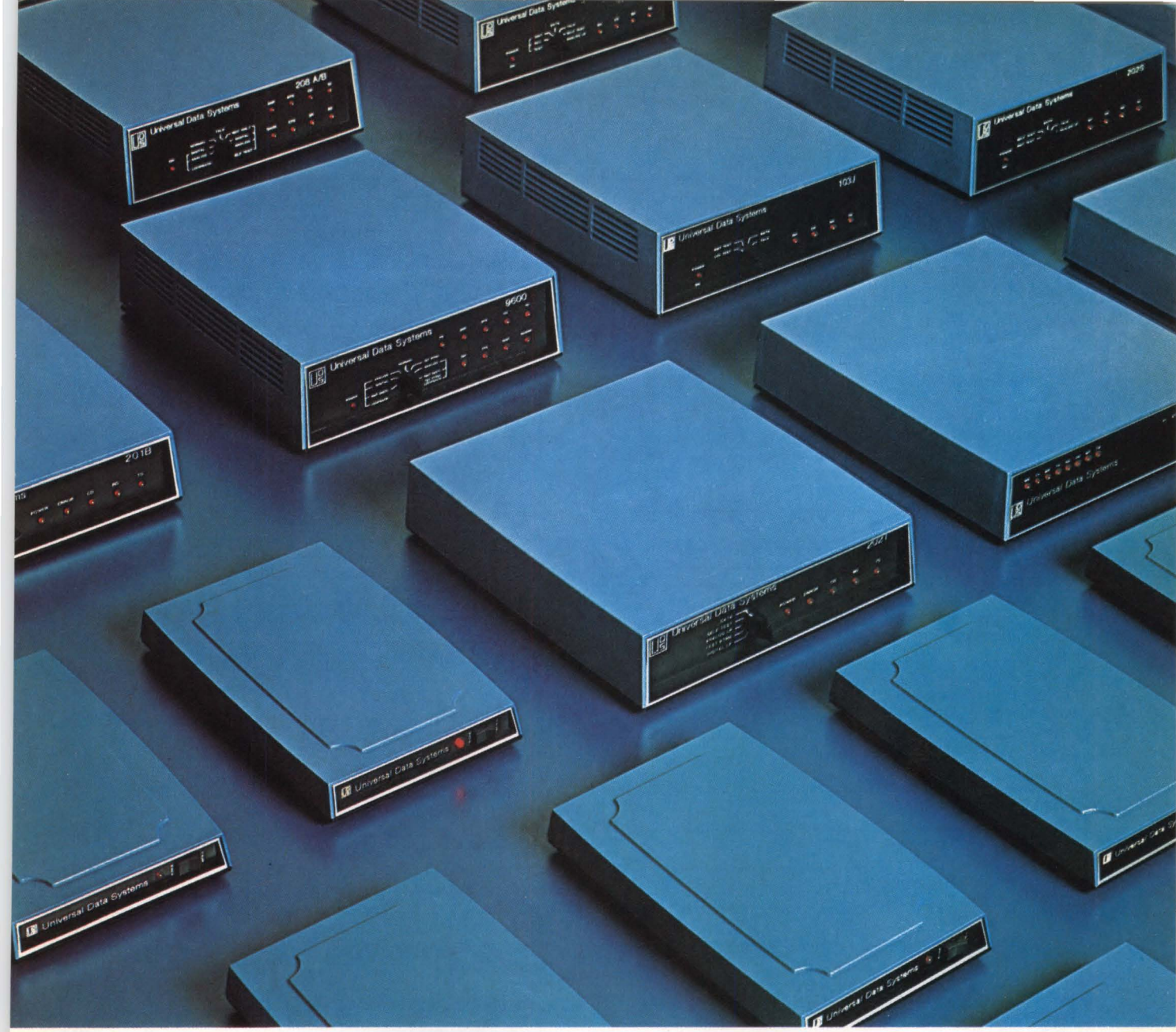

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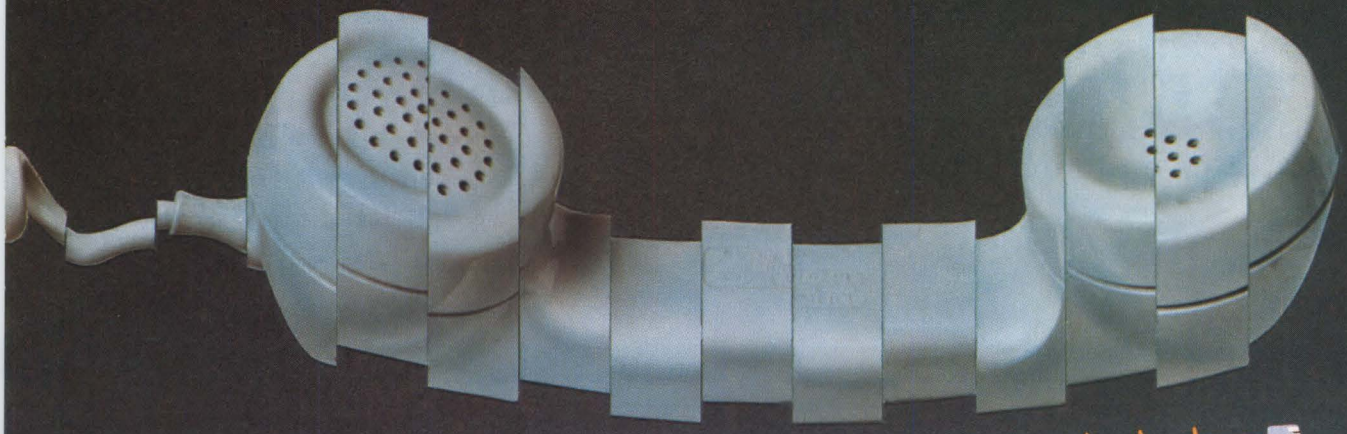
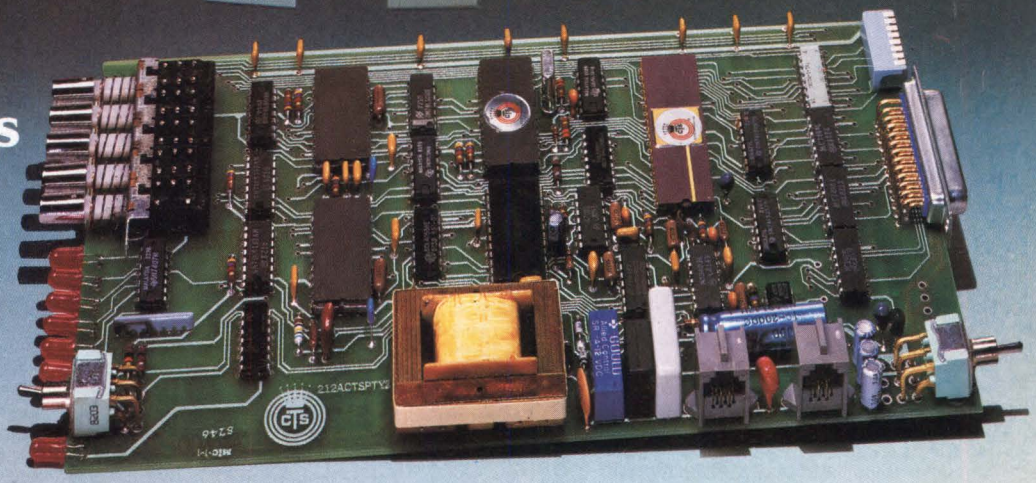
CIRCLE 158

AD INDEX

Phone lines garbling your data?



CTS 212A COMPATIBLE CUSTOM MODEMS deliver superb error-free data communication –even over poor phone lines



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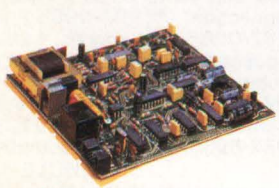
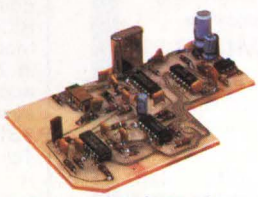


Microcomputer Integral Modem



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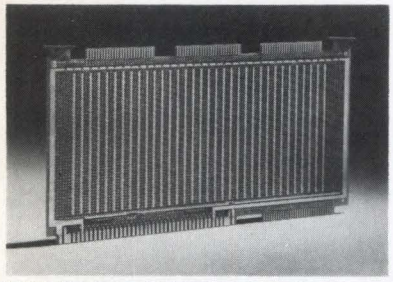

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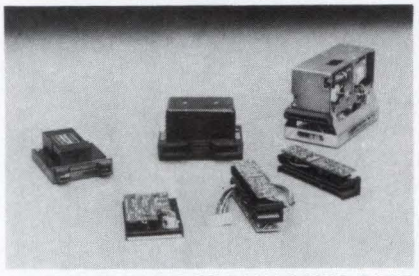

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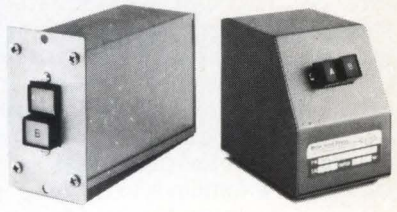

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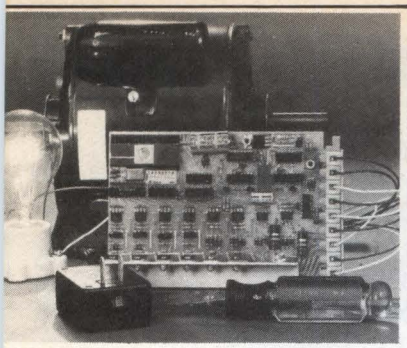

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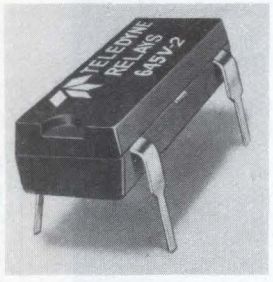

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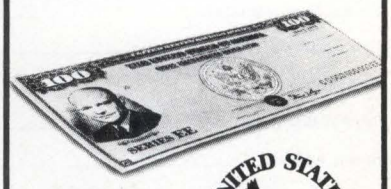

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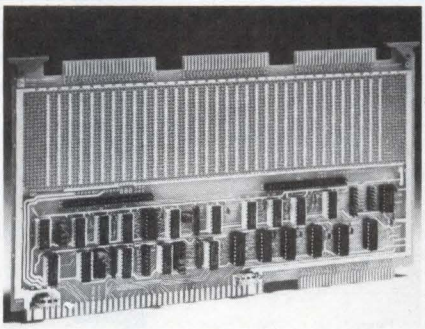

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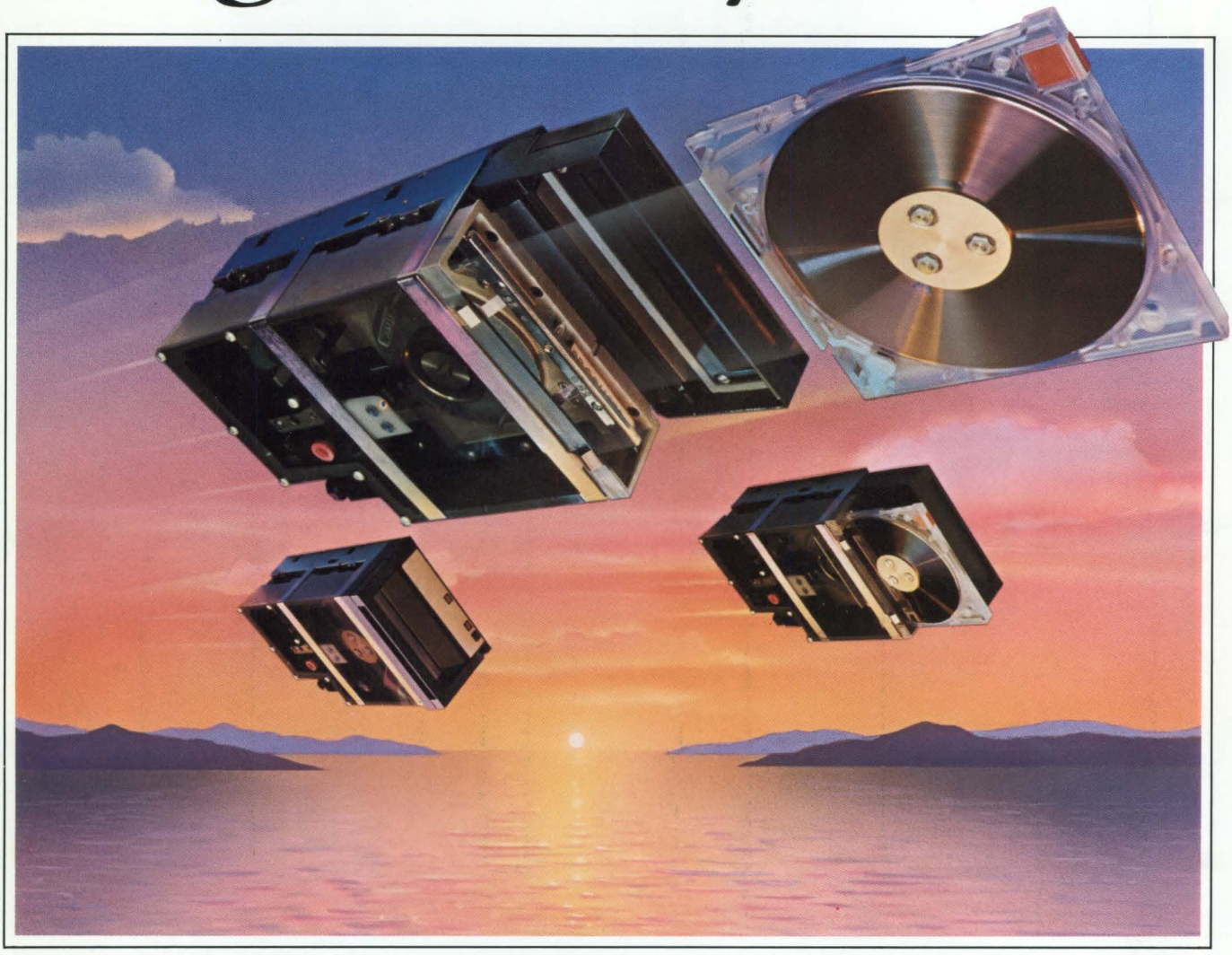

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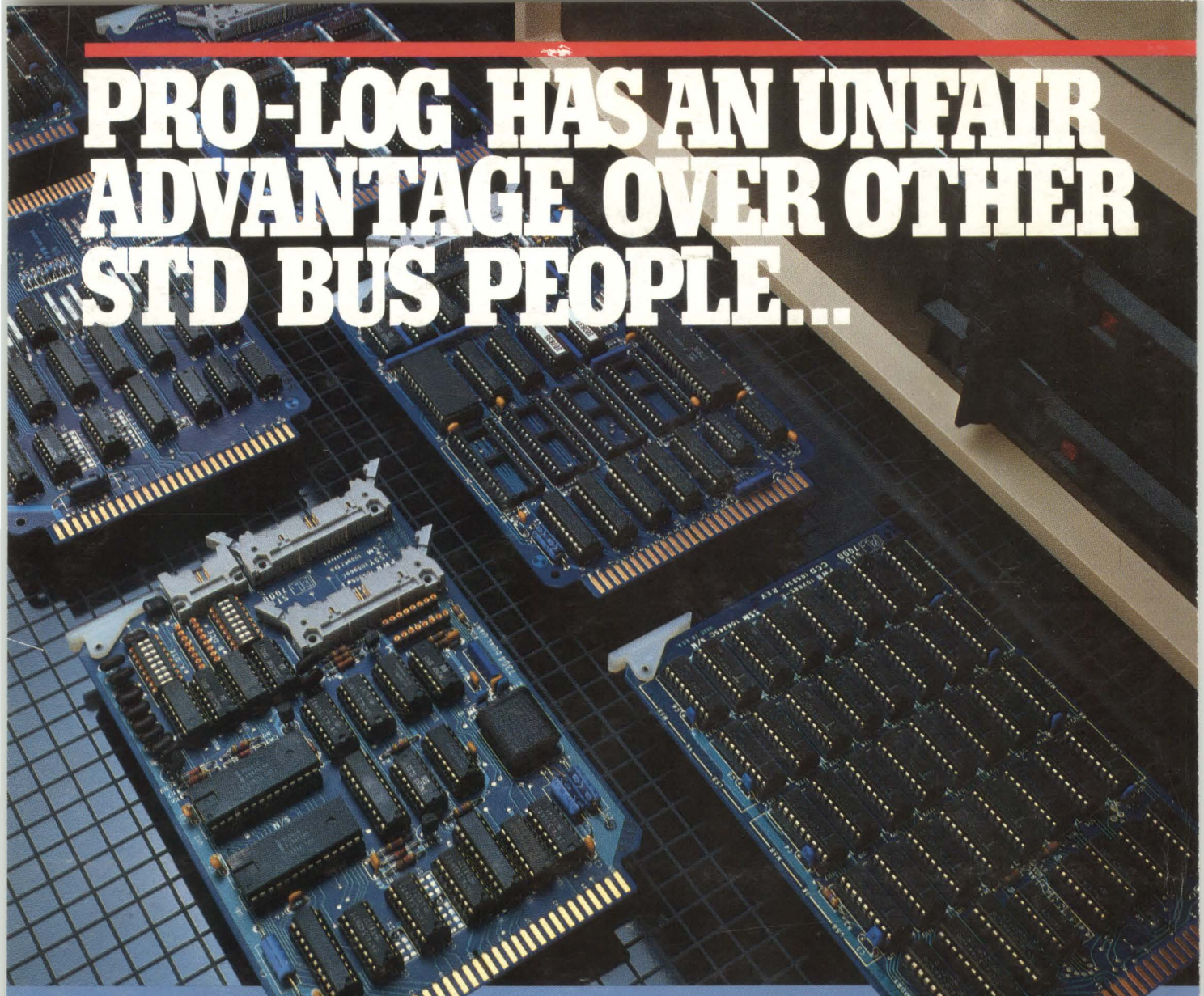

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