A PENNWELL PUBLICATION

JAN. 1982

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT: MEMORY SYSTEMS DESIGN

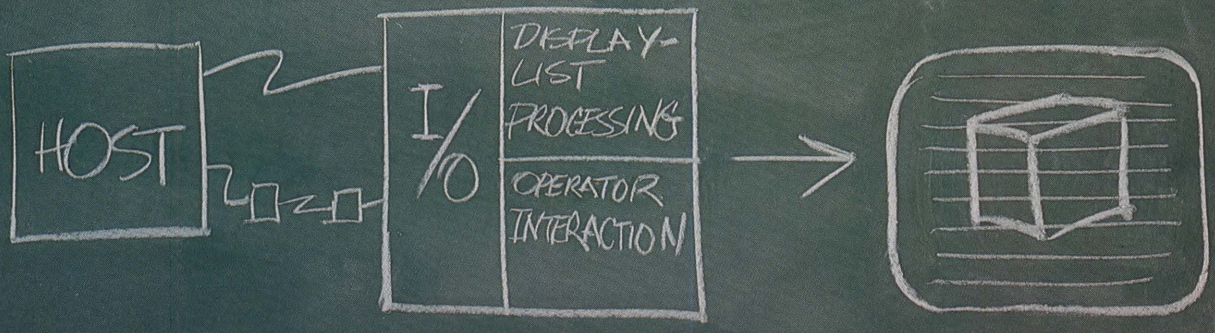
HOSTED SOFTWARE FOR MICROCOMPUTERS

SOLVING THE FIXED DISK BACKUP DILEMMA

DESIGNING FOR COMPLIANCE WITH FCC EMI REGULATIONS

THE MEGATEK DIFFERENCE:

REMOTE WORKSTATIONS



Core-compatible Fortran package which organizes graphic information for maximum communication-line efficiency. Image segments can be dynamically extended, changed to a different color or line type, scaled, translated; or blinked with just a few simple commands.

Whizzard 6200 terminals can also be programmed with hundreds of graphic subroutines (e.g., the image of a bolt head). Instead of reconstructing such "instances" each time they are needed, the host computer simply transmits a subroutine ID number.

Swiftly interacting with the host computer at the "action" end of the communication line is an intelligent Whizzard 6200 memory-management

Whizzard 6200 raster-scan, line-drawing terminals are working remote workstations – fast, interactive, intelligent.

The Megatek difference starts with host-computer software. Wand 6200 is a computer-independent, I/O interface which maps subroutines, segments, and attribute information into a 64K-byte display-list memory (expandable to 128K bytes).

The final step, from memory to screen, is nearly instantaneous. Powered by a 32-bit proprietary processor, the Whizzard 6200 "graphics engine" processes display-list data into raster images at an average rate of 200 nanoseconds per pixel. Text can be displayed in eight hardware-generated character sizes. Twelve-bit vector coordinates (4096 x 4096 virtual display space) can be scaled up to 8X with full retention of fine-line detail. Images can be "Rasterized" into full-resolution hardcopy.

Monochrome or color, 512 x 512 or 1024 x 1024, every member of the Whizzard 6200 family is a complete graphics workstation, including desk, display monitor, keyboard, joystick, and optional data tablet. And all are upwardly mobile – up to the Whizzard 7200 series of 3D rotation-and-scaling raster/vector terminals.

There is a Megatek difference. See it, believe it. Call or write: Megatek Corporation, 3985 Sorrento Valley Blvd., San Diego, CA 92121. 714/455-5590. TWX 910-337-1270. European

The more you know about graphics, the more you lean toward Megatek.

Headquarters, Megatek, S.A., Avenue du Tribunal Federal, 34, CH-1000 Lausanne, Switzerland, Telephone: 41/21/207055, Telex: 25037 MEGA CH.

MEGATEK CORPORATION
UNITED TELECOM COMPUTER GROUP

CIRCLE 1 ON INQUIRY CARD

Only one company has the complete range of disks and disk backup—Kennedy

That's right. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8″ 40 MByte disk drive (Model 7300) and an 80 MByte 14″ Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼″ cartridge recorder (Model 6450), and Model 6809, ½″ Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼″ 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

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CIRCLE 2 ON INQUIRY CARD

LETTER-PERFECT PRINTER DOUBLES AS DATA CRUNCHER.

Print two ways...correspondence quality and high speed data processing. Now priced under $2000!

The new T-1805 dual purpose serial printer uses a unique 40 x 18 matrix dot pattern for high quality correspondence printing; or, flip a switch, it uses a 7 x 9 matrix for high speed data processing printing. In the high speed mode, it generates reports at time-saving throughput rates reaching 200 lines per minute. In the reduced speed correspondence mode, its pivoting print head lays down overlapping dots to create a letter-perfect character that looks like it came from an office typewriter.

The T-1805 is the latest evolution in the popular and proven T-1000 series of serial printers. As such, the T-1805 offers the same quality construction, high reliability, ease of operation and operator conveniences. Plus, for the benefit of the office crew, the T-1805 is exceptionally quiet. Its 53 dbA noise level ranks it as the quietest impact printer on the market.

There's much more to tell, so visit or call your Mannesmann Tally sales outlet today.

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Printers for the long run.

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CIRCLE 3 ON INQUIRY CARD

UP FRONT

Memory expansion for IBM personal computer

Up to four times the amount of memory previously available for the IBM personal computer will be available in a high capacity memory expansion board announced by Datamac Computer Systems. Users will be able to directly address up to 1M byte of memory. Boards will contain 64k, 128k, 192k, or 256k bytes, with parity. The 64k-byte board is now available at $499.

Membership offered in software protection association

Applications are being accepted for 1982 membership in the Association for Software Protection (ASP), a nonprofit organization incorporated in May 1981 to reduce software piracy. Proposed ASP services include a bimonthly newsletter containing protection information, including case histories, legislative update, and responses to members' questions; an information library on international software laws and customs; research on various software protection subjects; and an education program for end users unfamiliar with proprietary software licensing requirements. There may also be conferences and seminars, practical protection assistance, referral services for end users, and educational packages for both developers and users.

ASP services will be available to participatory members at a fee of $350/year. Associate members, for $150/year, will receive copies of the ASP newsletter, a membership list, and active protection benefits; other services will be available for an extra fee. Membership applications and information are available from Ms Robin Robinson, President, ASP, 10143 Leona Ave, Tujunga, CA 91042 (tel: 213/957-2900).

Ada to run on Z8000

Zilog, Inc and Litton Systems, Inc, Data Systems Div have agreed in principle to cooperate on a program to develop an Ada compiler for the Z8000 16-bit microprocessor family. A 16-bit System 8000 will be used as the host for developing the compiler. Once the programming language has been converted, the compiler will be submitted to the Department of Defense for certification.

Acquisitions

Boards of directors of both companies have agreed in principle to the acquisition of Four-Phase Systems, Inc by Motorola, Inc as a wholly owned subsidiary, subject to the execution of a definitive agreement and its final approval by the boards of directors of both companies and of Four-Phase stockholders. The agreement is based on a stock exchange of between 0.634 and 0.763 Motorola shares per Four-Phase share.

An agreement in principle has been signed for the acquisition of Magnuson Computer Systems, Inc by Storage Technology Corp, to be accomplished by the exchange of 0.35 share of Storage Technology common stock for each outstanding share of Magnuson common stock. The merger is subject to approval of a definitive merger agreement by the boards of directors of both companies and of Magnuson shareholders.

Gould Inc and American Microsystems, Inc announced that both boards of directors have approved an agreement in principle, under which AMI would become a wholly owned subsidiary of Gould. Terms of the agreement call for 1.78 shares of Gould common stock to be issued for each outstanding share of AMI common and preferred stock.

UP FRONT

Standard chosen for 3″ floppy disk

Three companies that have been conducting research on development of a small size floppy disk—Matsushita Electric Industrial Co, Ltd; Hitachi, Ltd; and Hitachi Maxell, Ltd—have standardized a format for their own use for the 3″ "compact floppy disk." They plan to propose this format to disk and hardware manufacturers as an industry standard.

Suggested specifications include recording capacities of 125k bytes single-side and 250k bytes double-side, recording density of 4500 bpi, and data transfer rate of 125k bps for an FM recording system and double for an MFM system. Track density will be 100 tracks/in with 40 tracks/side, and rotation speed will be 300 rpm.

Pretriggers

Control & automation Automation of the design process has become the key to economic success for many companies. Recent announcements from 10 different companies emphasize that CAD/CAM systems and software are evolving into cost-effective industrial tools that enable development of more complex design and design documentation.

Computers Plans for the CRAY-2 computer under development call for a 32M-byte memory size and a CPU with a 4-ns cycle time. To help accomplish this, the design will include ECL chips housed in tightly packed modules that are immersed in an inert fluorocarbon cooling liquid.

Integrated circuits Texas Instruments Inc has broadened its offerings of voice synthesis products and introduced SDS, a speech development system for OEMs.

By adding metal interconnects to fixed component arrays, Micro-Circuit Engineering produces semi-custom bipolar linear devices within a few weeks and at lower cost than for full custom circuits. The recently introduced Uniray series contains 14 basic arrays.

Memory systems Super Sidewinder streaming cartridge tape drives from Archive Corp provide 45M-byte formatted capacity with a transfer rate of 90k bytes/s. Basic and intelligent models are available to back up both 8″ and 14″ Winchester disk storage, with streaming at 90 ips.

Either one or two Marksman disk drives of 20M to 160M bytes and up to four 30- or 90-ips intelligent tape drives can be controlled by Century Data System's Marksman T series formatter. Combining disk controller, tape controller, and host interface on a single PC card provides increased data transfer rates, offline backup and restore capability, and simplicity in the host interface.

Claimed to be the first 5.25″ Winchester drive with both fixed and removable disks, DMA Systems' Micro-Magnum 5/5 has a capacity of 6.75M bytes unformatted and 5M bytes formatted.

Data communications Two to 30 computers can be networked and up to 60 operations simultaneously performed with Zeda Computers' InfiNet. This local area networking system allows individual microcomputers to handle local tasks in parallel with other processing.

Microprocessors/ microcomputers A distributed microprocessor architecture that dedicates individual application processors to each function or task and that links each processor via a shared high speed data bus is the basis of DOSC's claim for virtually eliminating computer downtime.

Equivalent in power to a desktop computer, yet weighing less than a pound including keyboard and display, a handheld computer system from the Quasar Div of Matsushita Electric Corp of America fits into an attache case along with NiCd battery and six peripherals, including optional modem and printer.

Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept, PO Box 593, Littleton, MA 01460. (USPS 127-340)

BULK SEMI

THE BIG IDEA IN MEMORY: UP TO 32 MB/CHASSIS

Now, from the memory leader, you can get 32 MB of high-performance memory in a compact 15¾" system.

With chassis interface slots that allow you to use your own interface (our library of logic cards facilitates your designs!). Or choose a Dataram BULK SEMI interface that operates with DEC®, Data General, Perkin-Elmer, MODCOMP, or Honeywell minicomputers. SMD, MULTIBUS®, and AMPEX 4666-compatible interfaces are also available. And we have BULK SEMI for CSPI array processors too.

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BULK SEMI has been proven in seismic processing, process control, telecommunications, and array processing applications — anywhere microsecond speed, megabyte main memory or peripheral memory is required. Our 16-page BULK MEMORY brochure will tell you more. And you can have it at no charge by completing the coupon below, or calling us at 609-799-0071.

DEC and MULTIBUS are registered trademarks of Digital Equipment Corporation and Intel Corporation, respectively.

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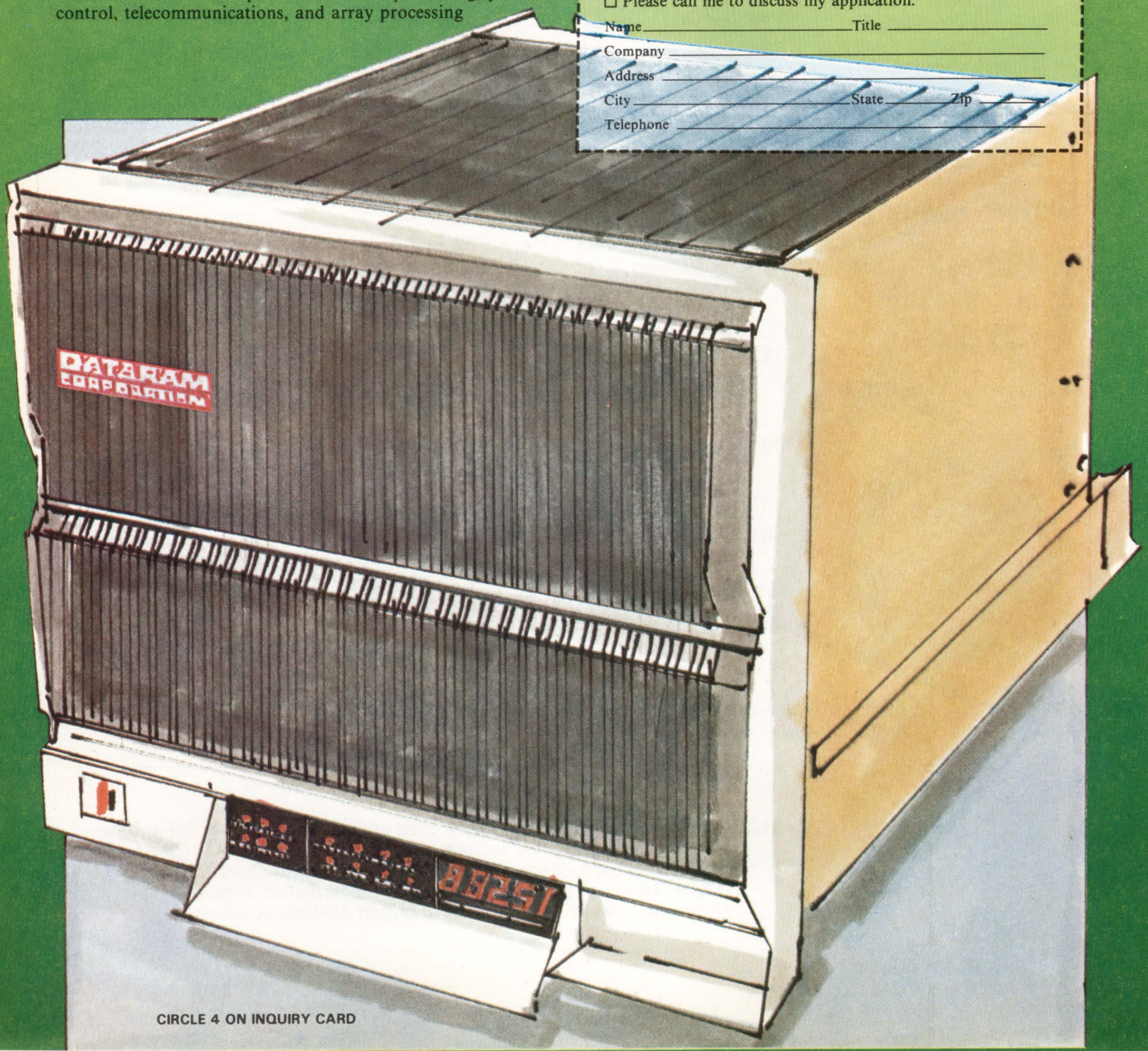
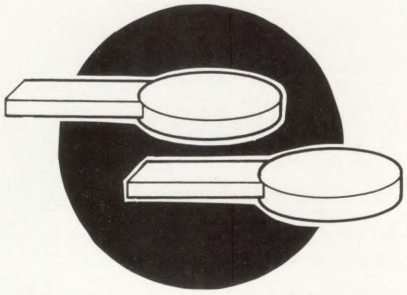


CIRCLE 4 ON INQUIRY CARD

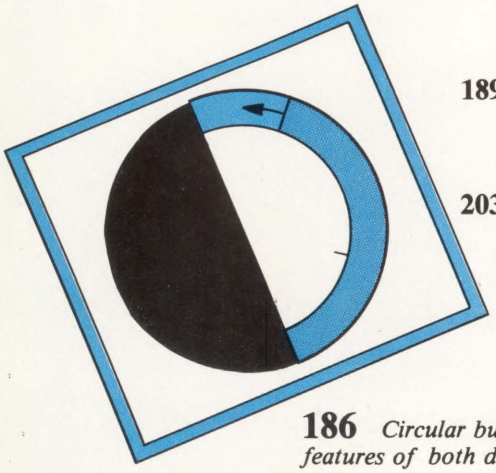
COMPUTER DESIGN®

System technology



40 *Totally independent, duplexed boards that operate in parallel and contain their own checking logic and diagnostics form backbone of continuous processing system*

System design



186 *Circular buffer in fixed disk drive combines features of both dual buffer and FIFO systems*

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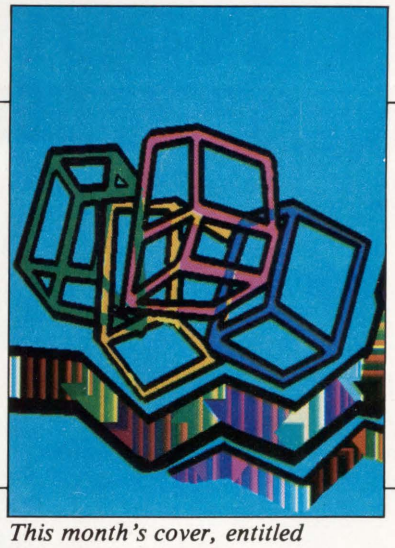
Special report on memory systems design



This month's cover, entitled "Hosted software for microcomputers," was generated using a Digital Effects VP-3 and D-48 color printer by Larry Gartel

System components

Departments

Designers' Preference Survey*

Editorial reviewer for this issue:

William G. Henrikson

*Appearing in Domestic issues only

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BPA
ABP

GOULD BIOMATION K100-D

7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

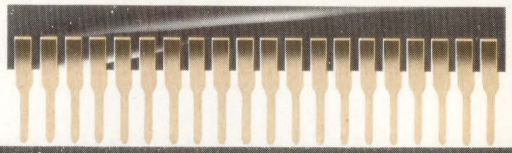
For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.

The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

Circle 5 for Comparison Guide
Circle 6 for App. Note request form
Circle 7 for T-12 communicator data

GOULD
Electronics & Electrical Products

If you need Floppy Disk Controllers immediately— come to Standard Microsystems.



Standard Microsystems announces totally pin-for-pin compatible alternate source versions of the FD 1791 family of industry-standard Floppy Disk Controllers/Formatters — and all 6 configurations are available for immediate delivery!

Our FDC 1791 family of MOS/LSI Controllers/Formatters can provide all of the functions to read or write data to any type of Floppy Disk Drive. These devices are manufactured with Standard Microsystems' patented n-channel COPLAMOS® process and are available in 40 pin plastic or ceramic packages.

If you need one of our FDC 1791 series controllers for current production, or are considering a new floppy disk system design, call or write us for detailed technical specifications and a quote. You'll be glad you came to Standard Microsystems!

SMC'S FDC 1791 FAMILY:

FDC 1791: IBM 3740 compatible, single-density; system 34 compatible, double-density. Can read/write and format a double-density diskette, including address mark detection, FM and MFM encode and decode logic, window extension and write precompensation.

FDC 1792: Operates in the single-density mode only

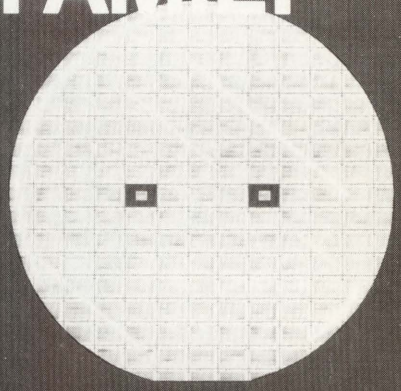
FDC 1793: Same as the FDC 1791 except data lines are TRUE

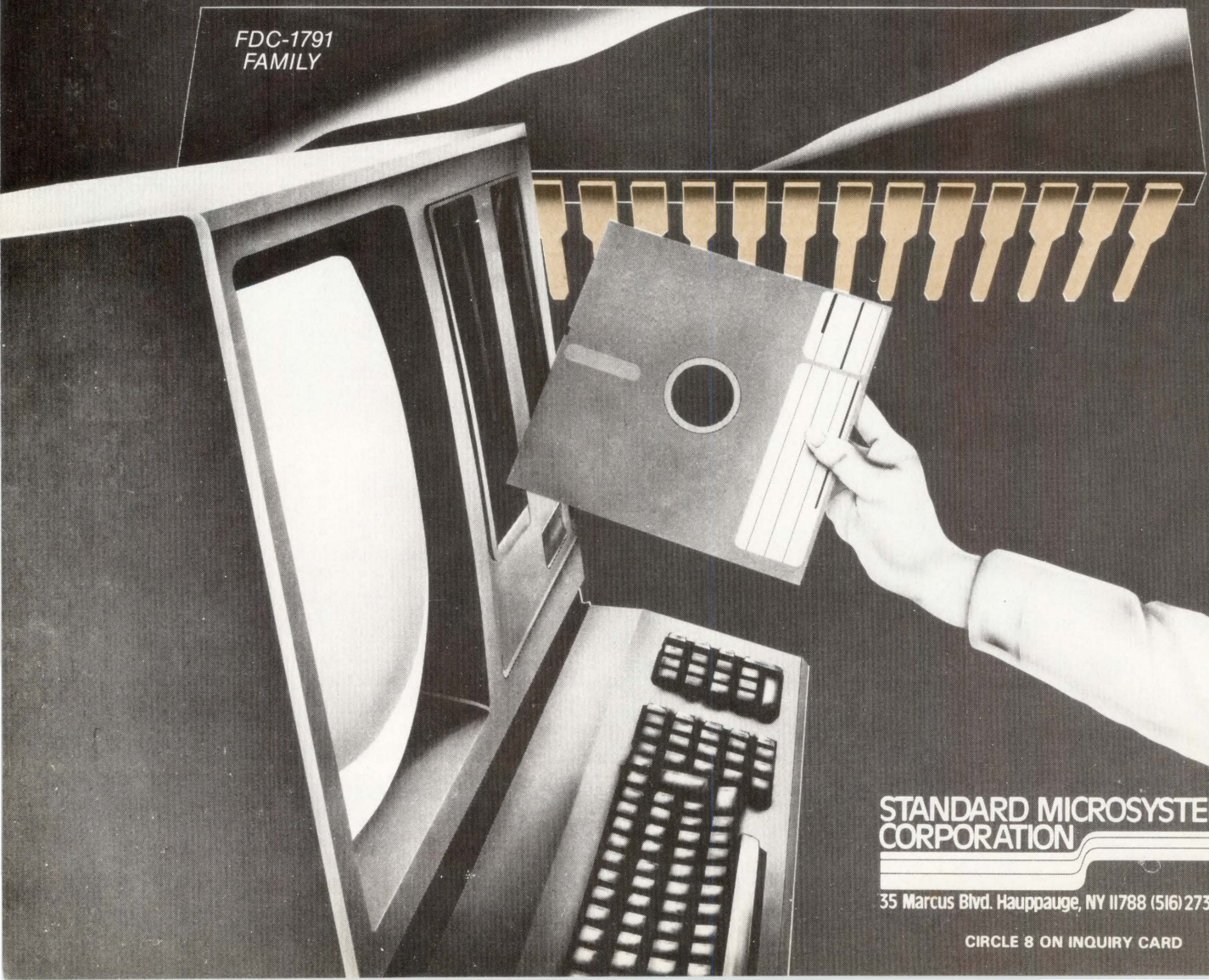
FDC 1794: Same as the FDC 1792 except data lines are TRUE

FDC 1795: All the features of the FDC 1791 plus double-sided disk drive control

FDC 1797: All the features of the FDC 1793 plus double-sided disk drive control

FDC-1791 FAMILY





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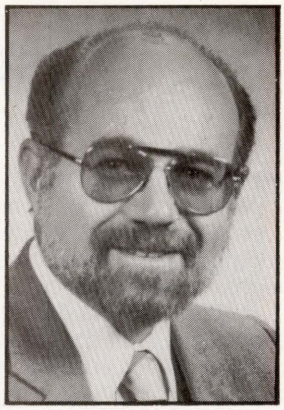
CIRCLE 8 ON INQUIRY CARD

THE YEAR AHEAD

will find a special report section in *Computer Design* every month. We have chosen the subjects of these "Design Frontier" reports to include software, systems and peripherals, and system ICs and components. System Design, our section for general interest feature articles, will continue to bring you a balanced selection of articles ranging from system software to system components. In addition, as you may have noticed already, we are broadening our scope to include articles of professional interest to senior systems designers. Coverage of legal topics in software and hardware will continue because response to the articles we published last year was high.

We plan to broaden our overseas coverage to pace some of the exciting new development work that is beginning to make its presence felt in the United States. This year will mark our first show participation abroad—we will be at the Hanover Fair this spring and Electronika in the fall. For our overseas readers, most of whom are in the EEC, we are planning a special edition of *Computer Design* starting with the March issue, which will be distributed at the Hanover Fair.

Looking back on 1981 for a moment, all of us at *Computer Design* thank you for your feedback: both the praise and the criticism.



We have diligently attempted to apply your suggestions to the redesign that appeared first in September, and will continue our efforts through 1982 to put together the best package possible. We will also try to keep *Computer Design* fluid—to be responsive to your needs and as dynamic as our rapidly evolving technology.

I would like to encourage all of you to share your technology and expertise with each other by submitting your ideas to us. If you would like to write an article for *Computer Design,* circle 503 on the reader service card and we will send you a copy of our *Author's Guide.*

On behalf of the *CD* staff, I wish you a very happy, healthy, and professionally satisfying 1982!

Saul B. Dinman

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—August

"Touch-Sensitive Screens Ensure a User Friendly Interface"
Henry H. Ng and Steven J. Puchkoff, Interaction Systems, Inc

This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.

TEK DAS 9100 DIGITAL ANALYSIS SYSTEM

Tektronix introduces 132 state of the art logic analyzers, in one.

A new concept in logic analysis.

Now you can have a single logic analysis system that is both configurable and upgradable. All with unprecedented performance and flexibility.

It's the DAS 9100. A single mainframe that houses up to six card modules. With acquisition speeds up to 660 MHz, timing resolution down to an unprecedented 1.5 ns, data widths up to 104 channels and synchronous or asynchronous operations.

And for the first time, you can combine *pattern generation with data aquisition.* Pattern generation provides stimulus data widths up to 80 channels and speeds up to 25 MHz.

Need I/O capability? There's an option that adds RS-232, GPIB and hard copy interface. And another for a built-in magnetic tape drive system.

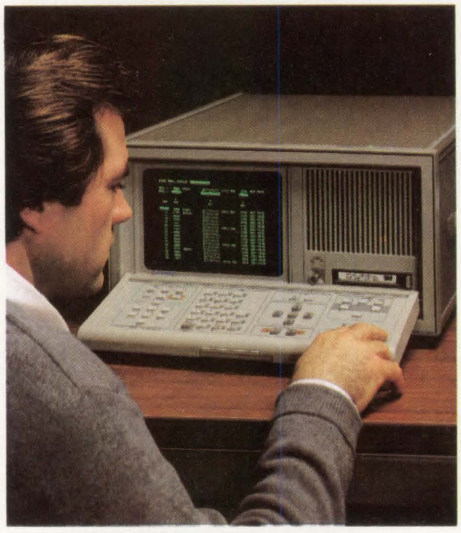
Select your own width and speed combination, for data acquisition.

DAS 9100 gives you four different data acquisition modules to use as building blocks. Each has its own data width and maximum speed: 32 channels at 25 MHz; 8 channels at 100 MHz with glitch memory; 4 channels at 330 MHz or two channels at 660 MHz. Modules can be combined to give you the performance you need.

Need high speed performance? One module can track your system clock (synchronously) at speeds up to 330 MHz or provide asynchronous sampling to 660 MHz. The eight channel module provides *both* synchronous and asynchronous sampling at 100 MHz. And the 32 channel module can be used to arm the trigger on those with higher acquisition rates.

To obtain the data width and speed your application calls for, simply select the appropriate combination of modules and add on later as your needs change.

To back it all up, there's powerful triggering, programmable reference memory and multiple clocks. Plus glitch triggering, with a separate glitch memory for



unambiguous glitch detection and our unique, new "arms mode" allows timing correlation between synchronous and asynchronous data.

DAS 9100 integrates the power of pattern generation with data acquisition.

At last, you can have a tool that covers your digital system debugging needs. By combining pattern generation and data acquisition modules, you can stimulate your prototype while simultaneously analyzing its operation. Allowing you to enter a whole new dimension of design analysis and verification.

Pattern generation capability is built around a 16 channel, 25 MHz module. Through additional expansion modules, you can raise the total to 80 channels while maintaining full system speed. The pattern generator allows interaction with the prototype through data strobe outputs and external control inputs, including an interrupt line. The generated pattern can even be changed based on the data acquired by the logic analyzer.

The DAS 9100 lets you start debugging hardware even before your software is available. Pattern generation makes it all possible.

With plenty of room for mainframe options to fit your application.

A powerful I/O option adds RS-232, GPIB and hard copy interace for full remote programmability. A built-in magnetic tape drive using DC-100 cartridges is also available, so you can save whole or partial instrument setups for recall. Pattern generation routines and reference memory data also can be stored.

DAS 9100 easy-to-use keyboard and menus tie it all together.

Operation of your DAS 9100 is simple and straightforward. Selectable menus help you set up trigger conditions, select data formats, and define voltage thresholds. You can even define your own mnemonics to fit the data under test.

How does it all go together?

In whatever combination your application calls for, or choose one of these pre-configured packages from Tektronix:

The DAS 9101. 16-channels of data aquisition at 100 MHz.

The DAS 9102. 32-channels of data aqusistion at 25 MHz plus 16-channels of pattern generation.

The DAS 9103. 32-channels of data aquisition at 25 MHz plus 8 more channels at 100 MHz. And 16-channels of pattern generation.

The DAS 9104. 80-channels of data aquisition, with 64-channels at 25 MHz and 16-channels at 100 MHz. Plus a 16-channel pattern generator with a built-in DC-100 magnetic tape drive.

Backed by Tektronix support.

You get a world-wide service organization, extensive documentation and applications assistance.

Contact your Tek Sales Engineer for more information. Or call us toll-free. 1-800-547-6711, in the U.S. In Oregon, 1-800-452-6773.

For further information, contact:

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Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

Canada, Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone: 705 737-2700

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Circle 11 for Sales Contact

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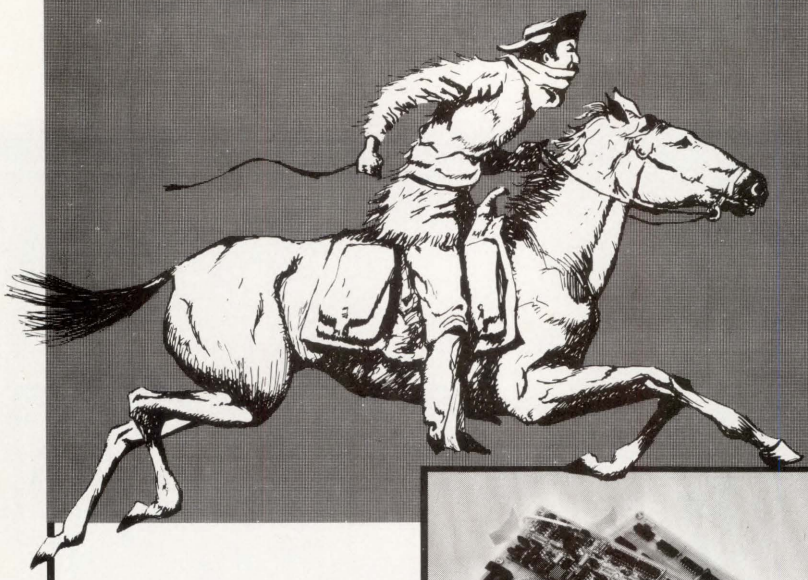

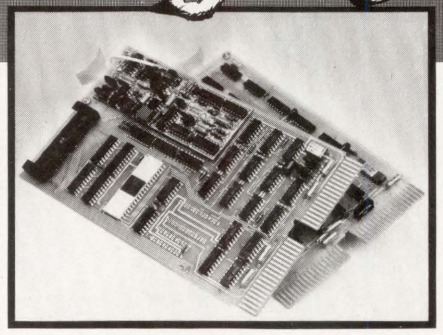

Use Megalink™ for 1 Megabit/sec DMA transfer between as many as 255 DEC and Intel processors on local networks up to 32,000 feet long.

- **Q bus, Unibus, and Multibus compatible units plug directly into DEC and Intel backplanes.***
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- **Integral 1 Megabit/sec FSK modem is immune to baseband noise.**
- **Software compatible drivers available.**
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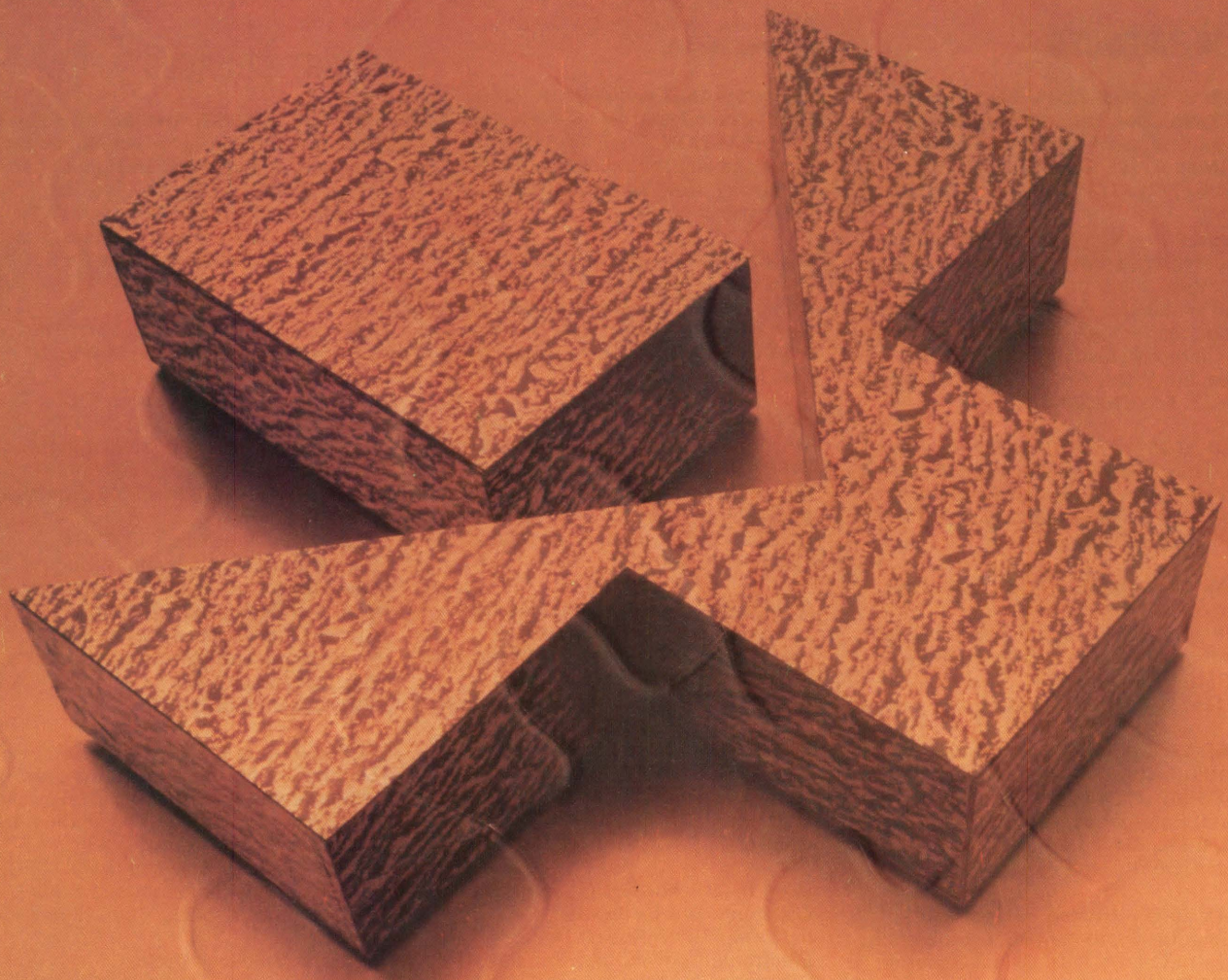

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We've become an integral part of the Gould electronics and electrical family and changed our name to Gould Inc., S.E.L. Computer Systems Division. Everything's in place and it fits perfectly.

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CONFERENCES

FEB 10-12—Internat'l Solid State Circuits Conf, Hilton Hotel, San Francisco, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 21-23—Non-impact Printing Technologies Data Base Access Meeting, Sheraton Fisherman's Wharf, San Francisco, Calif. INFORMATION: Linda M. Tempero, Advanced Technology Resources Corp, 6256 Pleasant Valley Rd, El Dorado, CA 95623. Tel: 916/626-4104

FEB 22-25—COMPCON Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 1-4—Robots VI Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: Public Relations Dept, Society of Manufacturing Engineers, 1 SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500

MAR 3—California Computer Show, Marriott Hotel, Anaheim, Calif. INFORMATION: Carol Reimer, Norm De Nardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

MAR 15-17—Human Factors in Computer Systems/NBS, Gaithersburg, Md. INFORMATION: Wilma Osborne, A265 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: 301/921-3485

MAR 19-21—Computer Faire, San Francisco Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Laurie McLean, Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

MAR 22-25—Interface Nat'l Conf and Expo for Data Communications/ DDP/Networking, Dallas Conv Ctr, Dallas, Tex. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 23-25—Southcon, Sheraton Twin Towers Hotel, Orlando Hyatt Hotel, and Holiday Inn International Drive, Orlando, Fla. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAR 23, MAR 25, AND APR 14—Invitational Computer Confs, Dallas Marriott, Dallas, Tex; Adam's Mark Hotel, Houston, Tex; and Sheraton Southfield, Southfield, Mich. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

MAR 25—ANSI and AFNOR Public Conf, Grand Hyatt Hotel, New York, NY. INFORMATION: Priscilla F. Trias, American Nat'l Stds Inst, Inc, 1430 Broadway, New York, NY 10018. Tel: 212/354-3315

MAR 30-APR 1—INFOCOM '82, Joint Conf of the IEEE Computer and Communications Societies, Las Vegas, Nev. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

APR 5-7—Office Automation Conf, Moscone Ctr, San Francisco, Calif. INFORMATION: Betty Lou Cooke, American Federation of Information Processing Societies, Inc, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

APR 21-28—Hanover Fair, Hanover, West Germany. INFORMATION: Hanover Fairs Information Ctr, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

MAY 11-13—Society for Information Display Internat'l Sym, Town-Country Hotel, San Diego, Calif. INFORMATION: L. Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

MAY 18-20—Northcon, Seattle Ctr Coliseum, Seattle, Wash. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 25-27—Electro, Sheraton-Boston Hotel, Hynes Auditorium, and Commonwealth Armory, Boston, Mass. INFORMATION: Robert Myers, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEMINARS

Data Communications for Minicomputer Users, various U.S. cities and dates. INFORMATION: Seminar Administrator, Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311. Tel: 213/998-8844

MAR 9-11—Internat'l Zurich Seminar on Digital Communications, Swiss Federal Institute of Technology, Zurich, Switzerland. INFORMATION: Secretariat 82 IZS, Miss M. Frey, EAE, Siemens-Albis AG, CH-8047 Zurich, Switzerland. Tel: +41-1-247 51 20

MAR 29-30—Robotics: Fundamentals and Technology of Computerized Robots, Marriott Pavilion Hotel, St Louis, Mo. INFORMATION: Ralph E. Lee, Computer Science Dept, Mathematics-Computer Science Bldg, Univ of Missouri-Rolla, Rolla, MO 65401. Tel: 314/341-4491

SHORT COURSES

FEB 8-10, APR 5-7, AND MAY 10-12—Data Network Design: Techniques for Systems Analysis and Design, Logan Airport Hilton, Boston, Mass; San Francisco, Calif; and New York, NY. INFORMATION: American Management Assocs, 135 W 50th St, New York, NY 10020. Tel: 212/246-0800 or 212/586-8100

FEB 16-19—Intelligent Robots: The Integration of Microcomputer and Robotic Technology, George Washington U, Washington, DC. INFORMATION: Director, Cont Engineering Ed, George Washington U, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

FEB 17-19—Practical CAD/CAM Considerations (Concept Through Operation), U of Calif, Los Angeles, Calif. INFORMATION: Sylvan H. Chasen, Univ Extension, Cont Ed in Engineering and Mathematics, 6266 Boelter Hall, UCLA, Los Angeles, CA 90024. Tel: 213/825-1047

FEB 25-27 and MAR 1-3—Digital Electronics for Instrumentation; and Microcomputer Interfacing Design and Programming, Virginia Polytechnic Inst and State U, Blacksburg, Va. INFORMATION: Dr Linda Leffel, CEC, Virginia Polytechnic Inst and State U, Blacksburg, VA 24061. Tel: 703/961-4848

MAR 15-17—Fiber Optical Communications, Arizona State Univ, Tempe, Ariz. INFORMATION: Ctr for Professional Development, College of Engineering and Applied Sciences, Arizona State Univ, Tempe, AZ 85287. Tel: 602/965-1740

MAR 22-23 AND MAR 24-26—Review of Pascal and Introduction to Ada, Univ of Wisconsin-Extension, Madison, Wis. INFORMATION: Avinash Vaidya, Program Director, Dept of Engineering and Applied Science, 432 N Lake St, Madison, WI 53706. Tel: 608/262-8592

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A FULL SPECTRUM OF CHOICES IN DEC-COMPATIBLE DISK STORAGE:

And now a new 32.2-Mb Winchester/Floppy System

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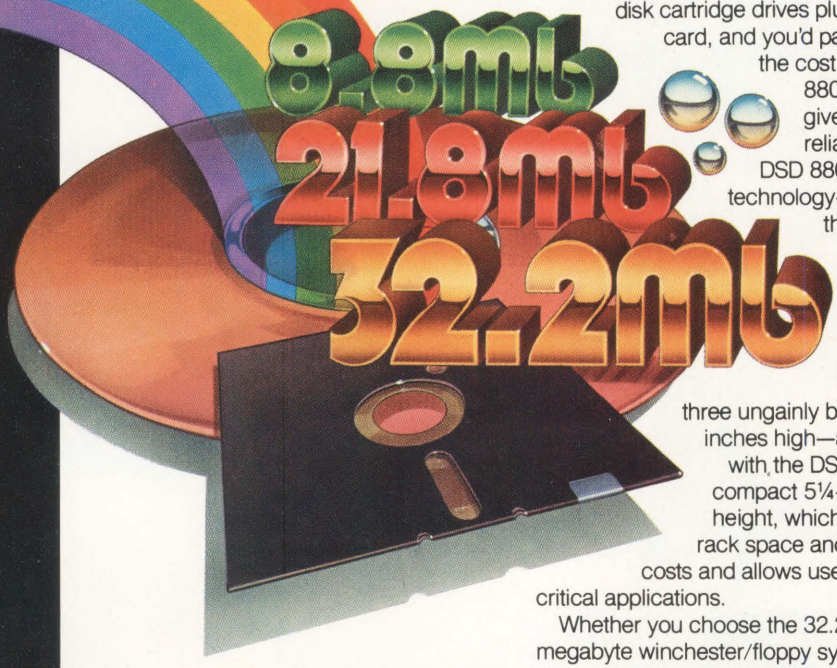
More disk storage choices than you get from DEC.



DEC designs great CPUs. Data Systems Design gives you disk storage to match.

For CPU quality, you can't beat DEC's LSI-11 and PDP®-11. But their disk storage doesn't always measure up. At Data Systems Design, data storage is our *only* concern. That's why our DEC®-compatible disk systems are more reliable, less expensive, more compact and easier to maintain than the disk systems you get from DEC.

And you get more choices of systems, too, so you can pick the exact features your product application requires.

DSD 880 gives you more megabytes per buck for your PDP-11 and LSI-11.

With the addition of a new DSD 880 version, you now have three choices in winchester disk storage: 31.2, 20.8 or 7.8 megabytes. Each with a choice of 0.5 single- or 1-megabyte double-sided floppy backup. More capacity for less cost-per-megabyte than any comparable DEC alternative.

To match the capacity of the DSD 880's 31.2-megabyte winchester disk, for example, you'd need three DEC RL02 disk cartridge drives plus bootstrap card, and you'd pay about twice the cost of one DSD 880. Plus, you'd give up the high reliability of the DSD 880's winchester technology—a state-of-the-art choice DEC doesn't even offer LSI-11 and PDP-11 users. And you'd have three ungainly boxes over 30 inches high—as compared with the DSD 880's compact 5¼-inch panel height, which saves you rack space and cabinetry costs and allows use in space-critical applications.

Whether you choose the 32.2, 21.8 or 8.8 megabyte winchester/floppy system, your disk system is more cost-effective than any comparable DEC disk drive or combination.

The hardware bootstrap is built right into the interface so you don't have to pay extra for a separate board.

The DSD 880 interfaces require 70% less backplane space than equivalent DEC configurations.

And the HyperDiagnostic™ panel simplifies troubleshooting for cost-effective remote diagnosis.

Fully compatible three ways.

The DSD 880 is hardware-compatible. It integrates with any DEC LSI-11 or PDP-11 computer-based system. Combine the DSD 880 with a VT103 containing an LSI-11/23 and you've got a complete, powerful table-top microcomputer with up to 32.2 megabytes of storage.

Software compatibility is no problem either. You can use your RT-11 or RSX-11 operating systems with RL01 or RL02 (winchester) and RX02 (floppy) handlers. With no modifications at all. And the DSD 880 runs all applicable DEC diagnostics and utilities.

It's media-compatible, too. DSD floppies can use either DEC double-density or IBM single-density formats.

With its higher capacities, smaller size, lower cost and more, the DSD 880 gives your DEC computer-based system the disk storage it deserves.

A choice of 4 floppy systems.

Pick the features you need. Data Systems Design gives you more choices in DEC-compatible floppy disk systems, too.

Each of the four floppy systems is packaged in a low-profile 5¼-inch chassis. All offer built-in hardware bootstrap and complete DEC RX02 compatibility, plus a choice of domestic or international configurations, and complete documentation for easy system integration.

DSD 480 provides double-sided floppy storage for your LSI-11 or PDP-11.

For twice the capacity of DEC's RX02, choose the DSD 480. An optional EXCHNG™ software program lets the DSD 480 transfer files between IBM- and DEC-generated diskettes.

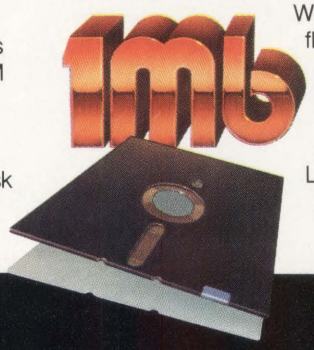
DSD 470 gives you low-cost double-sided floppy storage for your LSI-11.

The DSD 470 is software compatible and can be configured for single- or double-sided diskettes. And its single-board controller/interface * has far fewer parts than separate boards for better space utilization and improved reliability.

Choose DSD 440 for single-sided floppy storage with your LSI-11 or PDP-11.

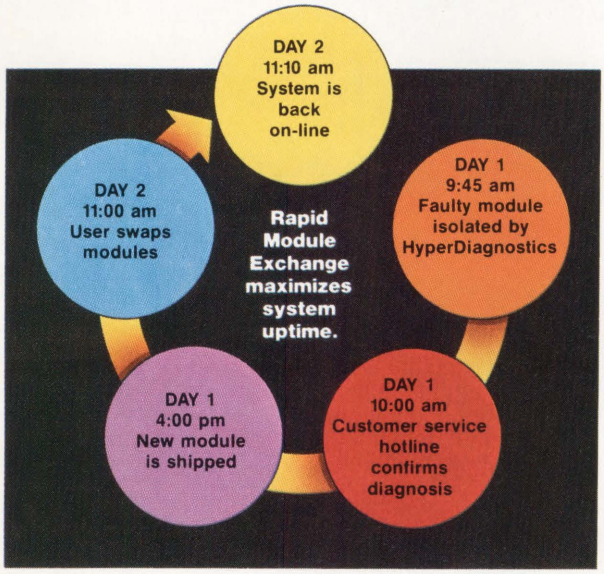
The DSD 440 is RX01 and RX02 software-compatible. It can transfer data 20% faster than DEC's RX02, and features built-in self-diagnostics for easy servicing.

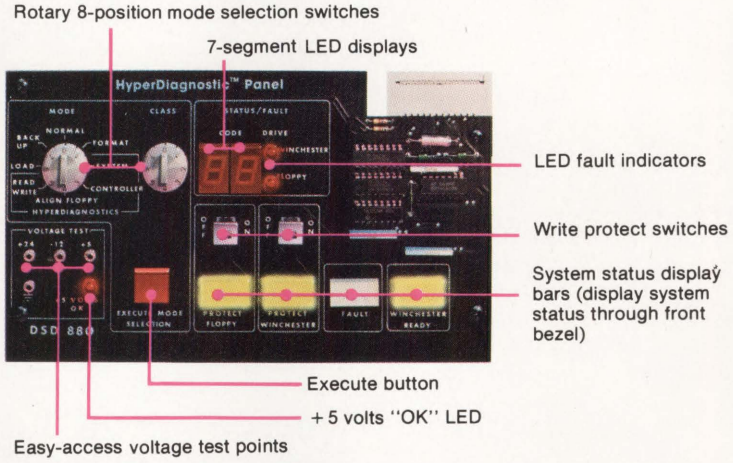
Choose DSD 430 for lowest entry cost with your LSI-11.



With 2 single-sided floppy drives, the DSD 430 gives you full RX02 compatibility and complete LSI-11/23 four-level interrupt support.

More reliable performance and easier maintenance.





DSD 880 HyperDiagnostic™ Panel

A revolutionary concept in uptime: Remote diagnosis ends costly service calls.

The true measure of a system is its ability to perform. Day after day, reading and writing data on demand. Data Systems Design units outlast any other disk system on the market. But even the most rugged system has an occasional problem. And that's when Data Systems Design really shines.

You know the usual service scenario. There's a problem, so you call the service rep. And wait for a return call. Then you wait for someone to show up. And every minute is costing money, in addition to the high cost of the service contract itself.

Data Systems Design ends all that with the service system that will soon be the industry standard: remote diagnosis.

HyperDiagnostics,™ standard on the DSD 440, 480 and 880, allow the user to test, exercise and debug without a CPU or a service call. Easy-to-use controls activate microprogrammed routines, and LED indicators designate fault status. On the 430 and 470, ODT-driven self-diagnostics and software diagnostics assist in troubleshooting.

A call to our service hotline gets instant back-up and confirmation of the diagnosis.† Our service records show that over 20% of the problems are fixed over the phone, with no service needed.

When a faulty module is isolated, **Rapid Module Exchange**™ gets the user back on-line faster than a service call. Thanks to our system's modular design, the user simply swaps modules after consultation with a hotline advisor. We usually ship out a new module the same day a failure is diagnosed in a specially-designed reusable carton for easy return of the original module.

For less than half the cost of a DEC service contract, our **HyperService**™ option extends warranty protection for one year beyond the standard 90 days and covers factory repairs and Rapid Module Exchange Service.

At Data Systems Design, we have carefully considered every step in the process to make service as easy and cost-effective as possible.

Get the disk storage you deserve for your DEC-based system.

For full technical details, write Data Systems Design, Inc., 2241 Lundy Avenue, San Jose, CA 95131, or call the sales office nearest you.

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*This controller/interface is also available separately as the DSD 4140.

†Although these services are available within the U.S.A. only, comparable service is available through our international distributors.

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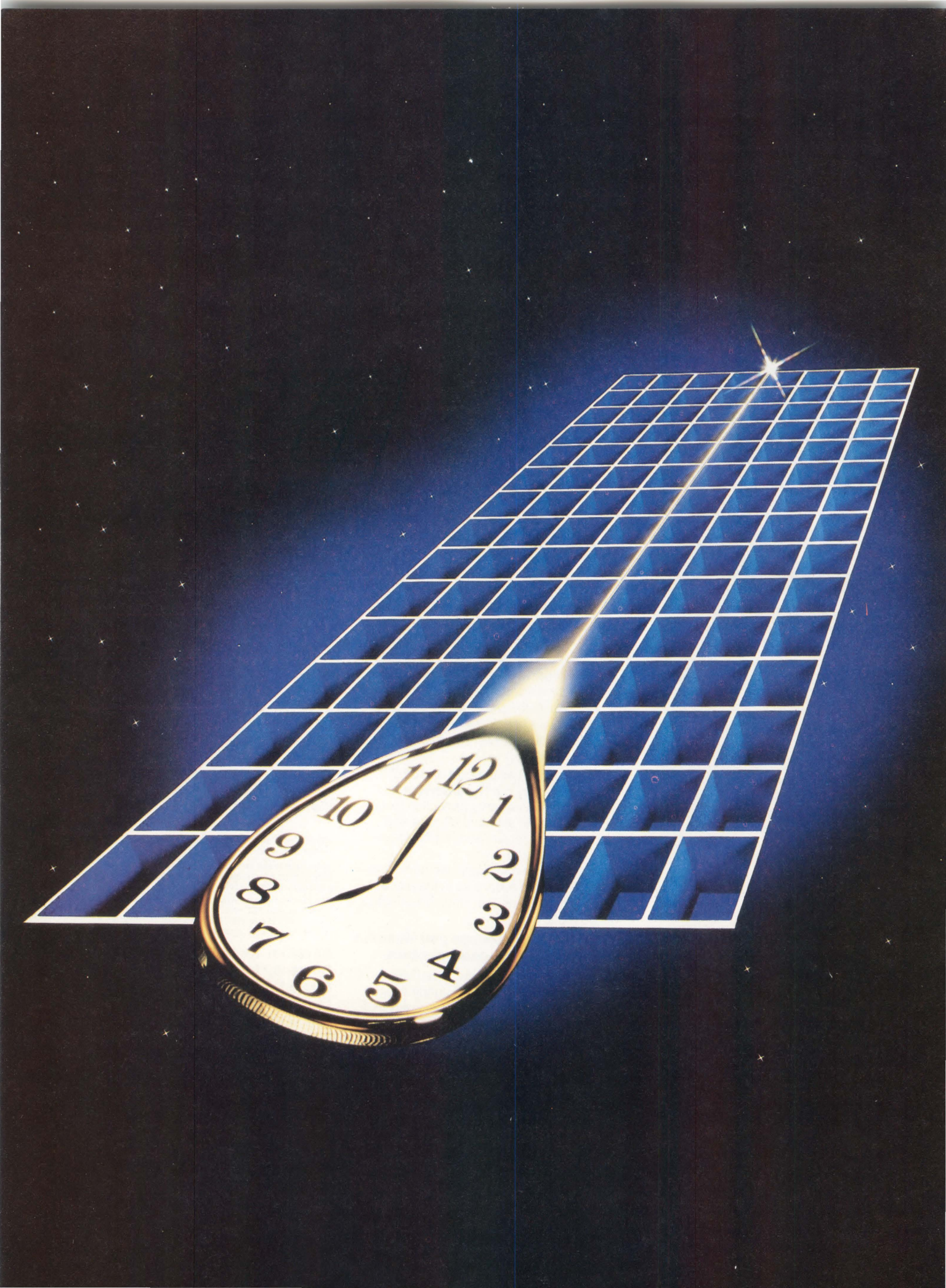
Circle 101 for DSD 880 information.
Circle 102 for DSD 480 information.
Circle 103 for DSD 470 information.
Circle 104 for DSD 440 information.
Circle 105 for DSD 430 information.

Data Systems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Introducing, for PDP-11 RSX, RSTS/E, and RT-11 users

Pascal-2™

The Time Machine

The First Dimension: Performance

Pascal-2 performs.

Pascal-2 programs run as fast as FORTRAN IV-PLUS programs—or faster. (FORTRAN IV-PLUS is Digital's fastest PDP-11 high-level language.) Pascal-2 code is as small as code generated by any Digital PDP-11 compiler or interpreter—or smaller. And Pascal-2 typically compiles at 1000 lines per minute.

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The compiler precisely reports typographic or syntactic errors. The interactive, source-level debugger helps detect deep-rooted logical errors. The profiler helps identify code that can be rewritten to speed program execution. Also included are formatters, index generators, and documentation aids— a total of 70,000 lines of Pascal code.

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The Fourth Dimension: Our Past and Future

The core of our technical group has been together more than a decade. Our Pascal-1 compiler entered commercial use in 1975. Before releasing our PDP-11 product, we delivered Pascal-2 under contract to two major computer manufacturers for three different processors. Now we're moving Pascal-2 to Motorola's MC68000, to Digital's VAX-11, and to the UNIX operating system. We're committed to Pascal for the long term.

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CIRCLE 14 ON INQUIRY CARD

The Freedom

Announcing the Freedom Generation of 5¼" thin film drives from Seagate Technology. They will bring new freedom to the designer of small, powerful computer-based systems.

Freedom ST538: 38 megabytes in a 5¼" package.

The ST538's highest memory capacity frees you to more fully utilize 16- and 32-bit processors.

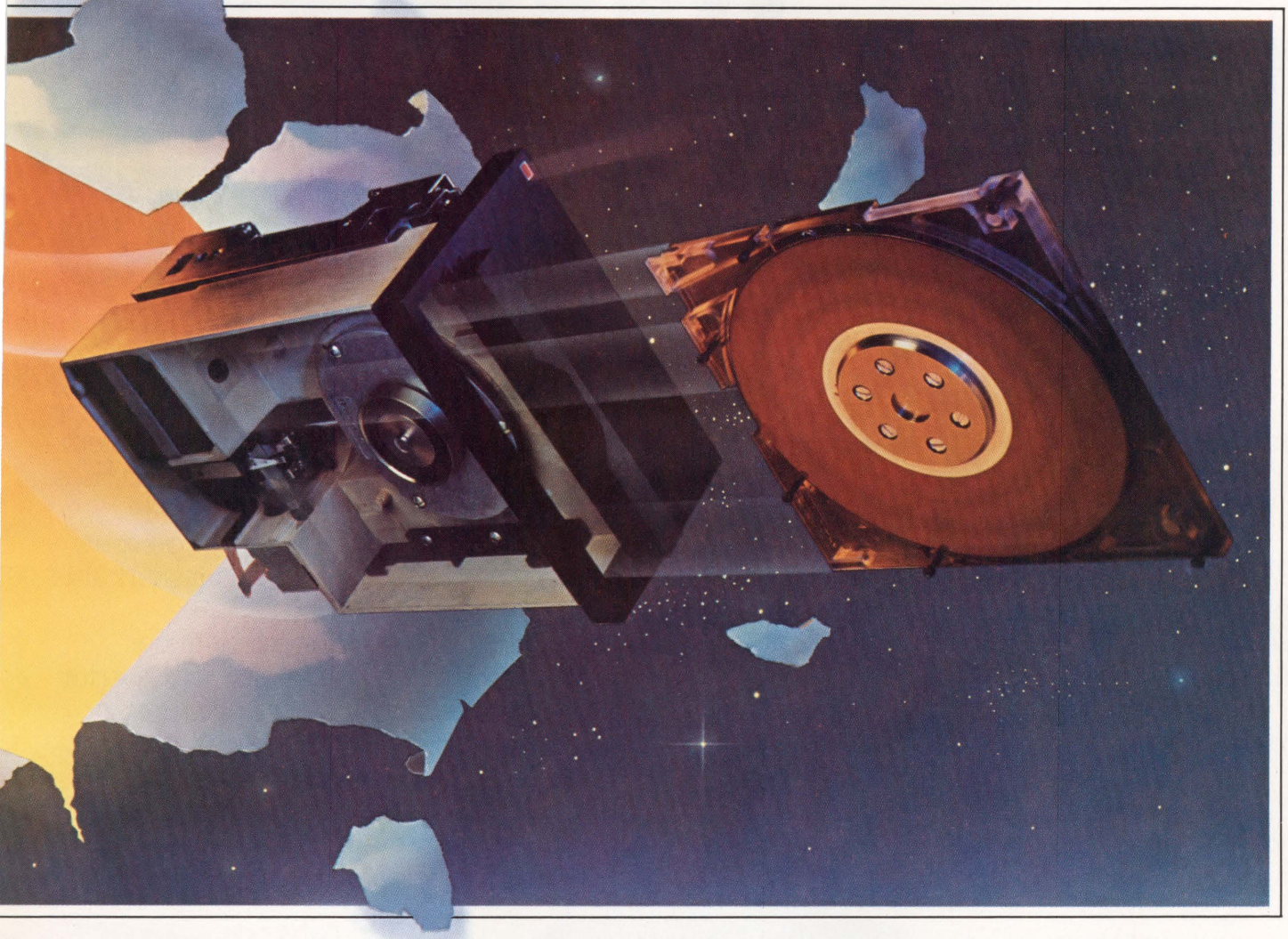
The ST538 handles larger data bases, meets the demands of transaction and query applications, and will satisfy more users in multi-tasking or multi-station networks. With the Freedom ST538, you'll be free to design bigger software programs with more comprehensive user aids and prompting.

And don't forget to consider the simplicity of integration with the ST538 when you're thinking about a 16- or 32-bit system.

Freedom ST706: the 6 megabyte MicroDisc cartridge drive.

The ST706 MicroDisc cartridge drive combines Winchester reliability and data

Generation!



access speed with the portability of a 5¼" removable disc cartridge.

It's the perfect I/O, program loading, and backup companion for the ST538 or the ST512, the first 5¼" to utilize thin film technology.

Six megabytes unformatted per ST706 MicroDisc cartridge give you more capacity than floppy or mini-floppy media.

Random access delivers faster backup than tape. Plus data integrity and system reliability are better than either floppy or tape.

Free and Easy Integration.

Each member of the Freedom Generation is designed for minimum impact on controller design, packaging, power supply requirements and software implementation.

And each is compatible with all existing products from Seagate.

Set yourself free! Consider the ST538 or ST706 for future systems designs.

For Freedom Generation product literature, circle our readers' service number.

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"Turning the tide in disc technology"

CIRCLE 15 ON INQUIRY CARD

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WITH OUR DISK INTERFACE, HAVE THIS

Used to be, upgrading a single disk drive meant sinking a heap of money and man-hours into system redesign.

The interfaces were that incompatible.

Not anymore. Now, with the help of our SA1400 intelligent controllers, every Shugart low cost drive has one common interface. Our new SASI™ (Shugart Associates System Interface).

Design it into your system once—then reap the benefits for generations to come.

Add data storage. Beef up your product line. Upgrade or modify. All virtually at will, without the fuss and colossal cost of traditional hardware or software changes.

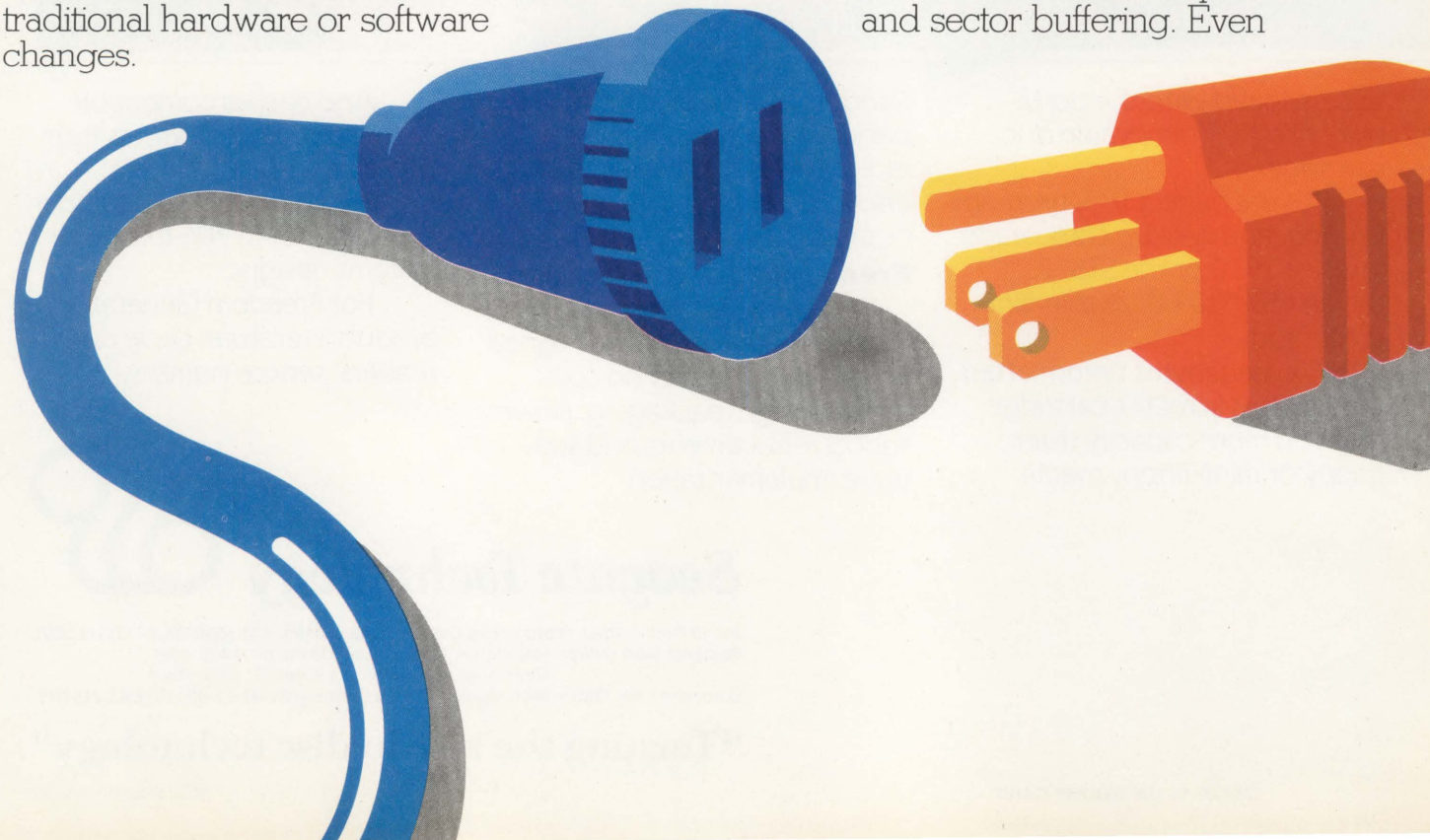
Fact is, thanks to SASI our 96-TPI Minifloppy™ looks the same to your system as our 14-inch Winchester. Same status lines. Same controls. Same commands.

But don't forget, at the heart of our new standard interface is something remarkable in itself.

A Shugart SA1400 series controller.

It performs all the automatic, high performance functions that your CPU shouldn't have to handle.

Like error detection and correction, implied search and verify, and overlapped seek. Then there's data separation and sector buffering. Even



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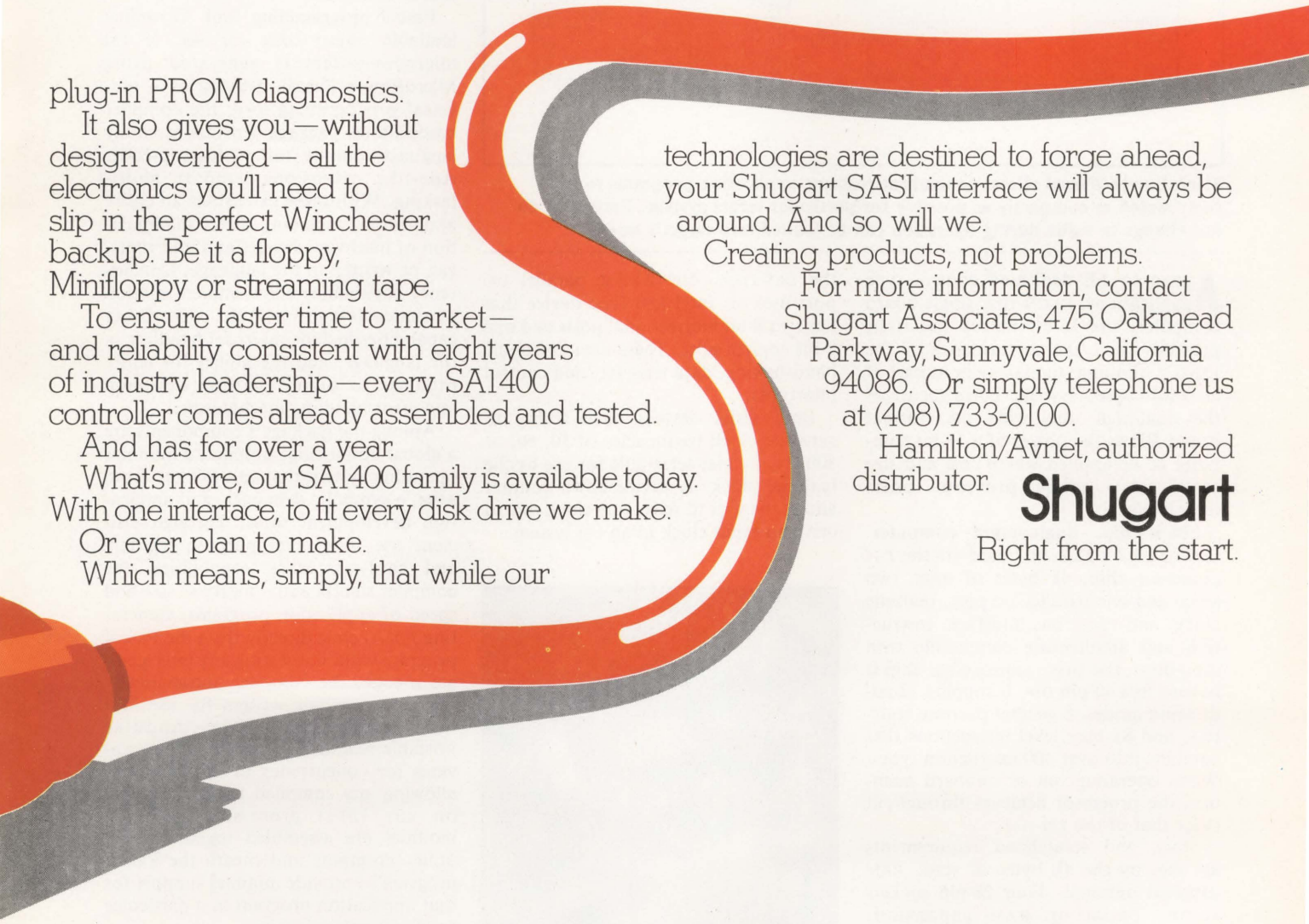

plug-in PROM diagnostics.

It also gives you—without design overhead— all the electronics you'll need to slip in the perfect Winchester backup. Be it a floppy, Minifloppy or streaming tape.

To ensure faster time to market—and reliability consistent with eight years of industry leadership—every SA1400 controller comes already assembled and tested.

And has for over a year.

What's more, our SA1400 family is available today. With one interface, to fit every disk drive we make.

Or ever plan to make.

Which means, simply, that while our technologies are destined to forge ahead, your Shugart SASI interface will always be around. And so will we.

Creating products, not problems.

For more information, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, California 94086. Or simply telephone us at (408) 733-0100.

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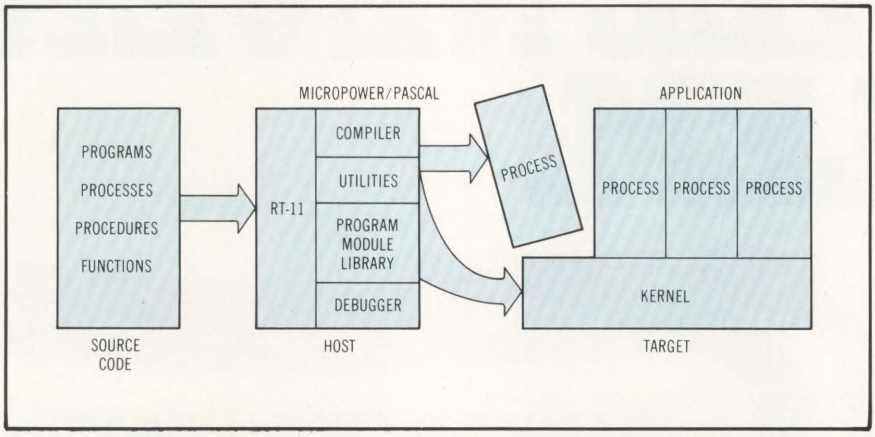
Compact single-board 16-bit computer supported by Pascal development package



MicroPower/Pascal allows concurrent realtime application programs to be constructed as compactly as possible for particular target system. Parts that do not change in value during operation can be loaded into target's ROM.

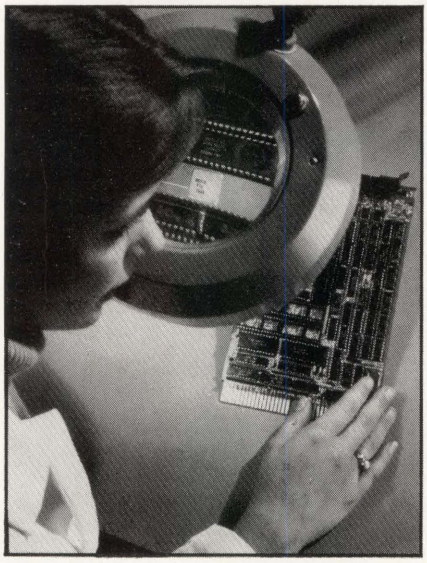
Aimed to fill dedicated control type applications, DEC's first single-board computer, the 16-bit Falcon SBC-11/21, provides twice the performance of the LSI-11/2, running standalone or as part of an LSI-11 based system. Form factor of the dual-high, dual-wide DEC format board allows the power of a 16-bit computer to be applied where cost and size restrictions made previous units impractical.

Single-chip, single-board computer. On the 13.2 x 22.8-cm board are the T-11 processor chip, 4k bytes of RAM, two serial and one parallel I/O port, realtime clock, and LSI-11 bus interface. Instruction and architecture compatible with the PDP-11, the MOS/LSI processor chip is housed in a 40-pin DIP. It supplies 12 addressing modes, 8 general purpose registers, and 82 base level instructions that combine into over 400 instruction types. When operating out of onboard memory, the processor achieves throughput twice that of the LSI-11/2.

Stack and scratchpad requirements are met by the 4k bytes of static RAM supplied onboard. Four 28-pin sockets accept PROM or RAM expansion. Onboard memory capacity expands to 32k-bytes PROM with 4k RAMs, or 16k PROM with 8k RAMs. Battery backup for 4k static RAM is supplied by socket set A.

Two serial interfaces, asynchronous EIA RS-423 and RS-232-C ports, are provided using single-chip DLV-11F equivalent devices. These devices support transfers at rates from 300 to 38.4k baud. Support for 20-mA communications requirements is offered through the DLV-11KA. The 24-line parallel I/O port uses an Intel 8255 type device that has two 8-bit bidirectional ports and one 8-bit control port. These devices handle handshaking, data transfer, and control interrupts.

Both serial devices have ability to generate clock frequencies of 50, 60, or 800 Hz, jumper selectable for use by the realtime clock. A divide-down counter allows the user to select one clock rate to drive an event clock in an LSI system.



Single-chip T-11 processor is heart of Digital's Falcon SBC-11/21 16-bit single-board computer. Instruction set compatible with PDP-11 line, computer fills dedicated control application.

The board's LSI-11 bus interface allows direct memory access between devices on the bus and onboard memory. This makes onboard memory appear as external memory to the system. Single-level interrupt service like that of the LSI-11/2 is provided to the bus; onboard, however, there is a multilevel structure, like that of the 11/23.

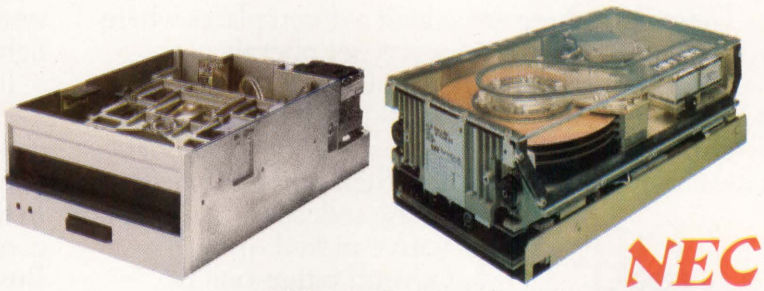
Pascal programming tool. Downline loadable object code for SBC or LSI microcomputers is generated using MicroPower/Pascal. Serving as a universal programming tool, the compiler based Pascal package provides assembly language output rather than p-code. Ada-like extensions support multitasking. With these extensions an entire application, including direct manipulation of hardware devices and interrupts, can be written in the language. Concurrency capabilities allow implementation of shareable and reentrant code. Other capabilities include interrupt handling in the language, and the ability for entire products to supply uniform exception and error handling mechanisms.

Among the package's components are a global optimizing compiler, a modular operating system that can execute from ROM, a symbolic debugger, and application development tools. Through efficient use of general purpose registers and hardware stack capabilities, the compiler significantly improves size and speed of application programs. Generating PDP-11 code directly from the Pascal program without creating any intermediate p-code, the compiler automatically segments anything written for use in a ROM environment. The modular ROMable realtime operating system provides for concurrency in the language, allowing any compiled program to run on any LSI-11 processor. Software modules are assembled together using utility programs underneath the Pascal program to provide minimal support for that application program in a particular hardware environment.

In addition, PASDBG, the symbolic debugger, downline loads and remotely controls execution of applications in the prototype hardware configuration. Accomplished without in-circuit emulation hardware, this not only allows full program debugging in the original Pascal language terms, but also enables the programmer to view the underlying opera-

(continued on page 30)

Fatten your profits with NEC disks.



NEC

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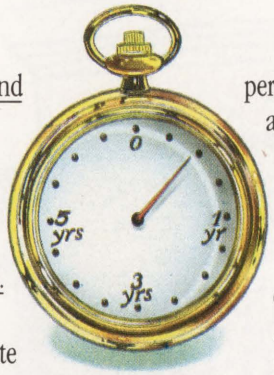

Our Soft-Touch 8-inch diskette drive has a mean time between failure of 15,000 hours. That's nearly 5 years of normal use.

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Our 15 years of disk-building experience pays off.

We know disks, we know how to build them, and we know how to keep them running. As a result, we've got features in our disks that give you, and your customers, years of hassle-free service.

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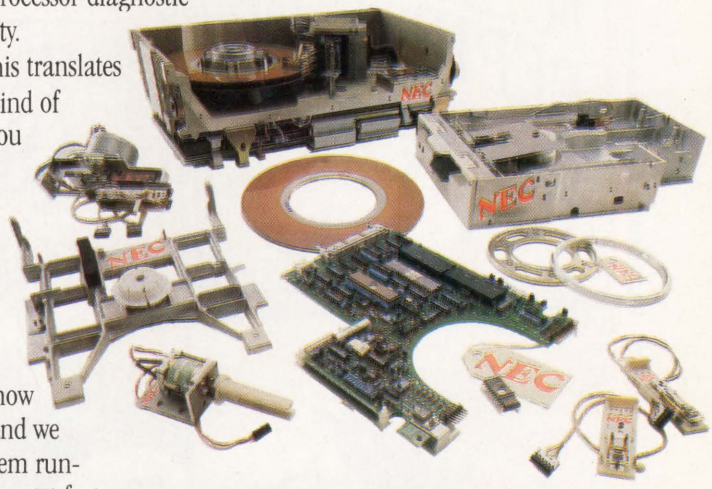
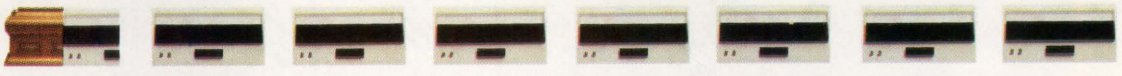


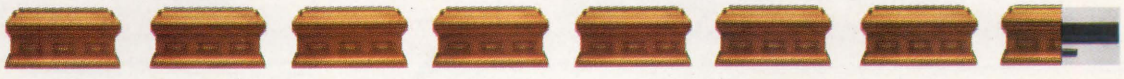
Because we manufacture almost every part in all our disks, we can assure the high tolerance engineering, rigid quality control in selection of raw materials, and attention to production details that guarantee you years of trouble-free operation.

Our significantly better diskette drive DOA rate reduces test and inspection time, saving you hundreds of dollars.

NEC Soft-Touch™ DOA rate: practically nil.



Other diskettes' DOA rate: as much as 10%.



BELIEVE IT OR AN EASIER WAY TO

These days, there are at least a dozen places where you could buy microprocessor peripherals.

A number cruncher here, a CRT controller there, a bus clock somewhere else.

That's great. If you feel like spending half your time shopping around. And then trying to breathe life into the collection of spare parts you've picked up.

But if you'd rather build a system where all the pieces work together as one tight unit, then you've only got one real choice.

Intel.

Because we give you more LSI peripherals to choose from than anybody else. 56 at last count. For 8-bit applications. 16-bit applications. Or both. In five different product areas. Memory control. CRT control. Slave processing. Data communications. Bus support. And over 1982, we'll be introducing 8 new peripherals. Which is more than the total line a lot of companies can give you.

NOT, THERE'S BUY PERIPHERALS.

Obviously, there's a much better chance you'll get exactly what you need from us. But that's only part of the story. Thanks to our common bus interface, each one of our peripherals is perfectly compatible with all the others. And with all our CPU's. Past, present, and future.

Design your whole package with our building blocks, and you'll push your system integrity to the max. While you're cutting your development time down to the minimum.

We can make your life a lot simpler from a strictly business standpoint, too. By ordering all your peripherals in one kit, you'll get all the technical support you'll ever need. All from one source. In a totally coordinated package. We'll coordinate your deliveries, too. So you can count on a nice smooth production flow.

Of course, some of you would rather look for high performance. And easy upgrades. That's fine with us. Because those are just a few more of the things we give you.

So no matter what you need, get in touch with us now. We'll send you a 36-page microprocessor peripheral guide. And show you how simple it is to find the right peripherals.

When you know where to look.

Just ask your local distributor. Or write: Intel Corp., Attn: Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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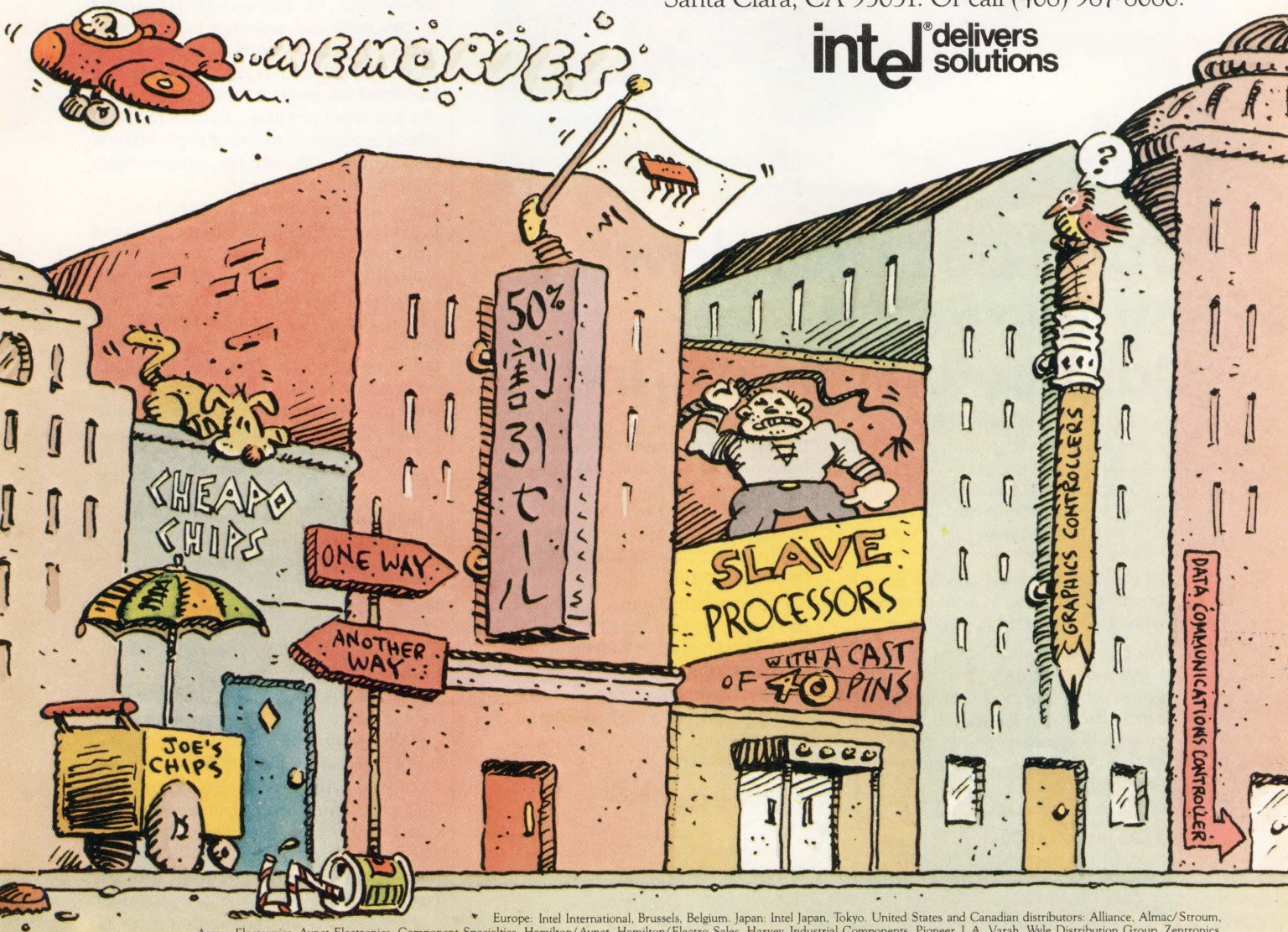

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L A. Varah, Wyle Distribution Group, Zentronics.

CIRCLE 18 ON INQUIRY CARD

ting system and other concurrently executing processes.

Pascal application programs are developed on a PDP-11 system, with minimum 128k byte memory running the RT-11 version 4 operating system. The final program is transported to the target microcomputer by writing it into PROM, downline loading it over a serial line, or recording it on floppy disk or tape cartridge.

Since the software's modular architecture minimizes memory requirements without sacrificing the ability to build large, full function configurations, designers can use the SBC-11/21 for low cost realtime applications implemented in EPROM.

The Falcon SBC-11/21 lists for $790 in single units, and $521 for quantities of 100. Volume deliveries are scheduled for the third quarter. MicroPower/Pascal is licensed at $8500 for the development system in quantity; runtime copies are $30 each. Deliveries are scheduled for March. **Digital Equipment Corp**, 146 Main St, Maynard, MA 01754.

Circle 240 on Inquiry Card

Don't get shot down by the FCC!
Call Dayton T. Brown, Inc.

The FCC rules and regulations are specific about the correct method of conducting a test program. The incorrect approach to your FCC testing can lead to poor results and added cost. You do not have to take any chances.

At Dayton T. Brown, Inc. we perform FCC testing in accordance with the rules and regulations.

We use calibrated receivers and tunable antennas for radiated emissions testing. Conducted emissions are measured with specially designed line impedance stabilization networks and EMC receivers.

All FCC testing at Dayton T. Brown, Inc. is performed on FCC approved, indoor all weather field sites.

Dayton T. Brown, Inc., delivers test results you can rely on. We have the distinction of providing the test data for some of the first units ever certified by the FCC to meet part 15, subpart J, for digital electronic products, the new requirement!

To be sure call Dayton T. Brown, Inc., to perform your FCC engineering and testing. We have been assisting manufacturers to meet government regulations for more than 30 years. We can help you too!

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For a free poster of this ad, send us your business card, attention, FCC

New bus standard takes wind out of Futurebus effort

In a joint announcement, a new 16- and 32-bit microprocessor bus standard has been defined by three U.S. manufacturers—Mostek, Motorola, and Signetics/Philips—and subsequently supported by a major European company, Thomson-CSF of France. Called the VME bus, the new standard conforms to DIN 41612 and 41494 mechanical standards, popularly known as the Eurocard. Both single- and double-size Eurocard formats are supported, as is the Eurocard pin and socket connector, which is accepted as being more reliable and immune to adverse environments than the edge connector.

The asserted aim of the VME bus is to provide a 16- and 32-bit interconnect structure that will serve the needs of multiprocessor and distributed intelligence systems. The single-card, measuring 160 x 100 mm, contains all the primary signals needed by 16-bit systems, in addition to 16 pins each for data and address. The doublesize format, with its P2 connector, provides 16 additional pins for both data and address to accommodate architectures having up to 32-bit data words and 32-bit address spaces, and measures 160 x 233.4 mm. Also available on the P2 connector are 64 additional I/O lines. These lines are located on the outer rows of connector pins so that systems requiring 32 or fewer extra I/O lines can select less expensive connectors.

The VME bus is asynchronous, supporting multiple processors, and positively acknowledges every bus transfer. VME is nonmultiplexed to reduce timing penalties and bus noise. Four levels of bus arbitration with BUS BUSY and BUS CLEAR controls permit sharing by multiple processors; arbitration allows daisy chain priority within levels and user selectable priority between levels. To permit optimal utilization of the bus bandwidth in a multiple processor

(continued on page 32)

CIRCLE 19 ON INQUIRY CARD

Designing your own datacomm black box?

If your data communications problem seems to require an intelligent "black box," put your software into an OrangeBox™ instead. MICOM did, and produced the world's most popular data concentrators.

If you've looked into building your own, you'll find that the OrangeBox™ is just the kind of package your own designers would want to put together, given the time—and money—to "do it right." MICOM did it right—we *had* to—since the hardware was to become the base for many of our best known products, including the new Micro800/2 Data Concentrator. As a result, the OrangeBox™ is as esthetically pleasing and as simple to operate as it is functionally efficient. And thanks to MICOM's very large production volume, it comes *at a price that may surprise you.*

Neatly integrated into its injection-molded case are an up-to-date set of very efficient components, including a fast Z80A, RAM, EPROM, SIO chips, programmable DIP switches, LED's, up to 18 I/O interfaces, and even matched integral modems. Since its programming characteristics will be immediately familiar to most communications designers, your application can be implemented in very little time, using the OrangeBox™ either as an intermediate step toward an in-house design or as a base for continuing product development.

Protocol conversion? Node processing? Terminal cluster control? Front-end processing? Packet Assembly/Disassembly? Network security monitoring? The OrangeBox™ is the right hardware for all of them. Call or send today for a set of brochures describing the OrangeBox™ and MICOM's other OEM products.

What could you do with an "empty" OrangeBox™?

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CIRCLE 20 ON INQUIRY CARD

VME BUS SIGNALS

P1 Primary Signals†

Address bus	A01 to A23	Primary Address Range = 16M bytes
Data bus	D00 to D15	Primary data width = 16 bits
Address control	AS	Address strobe
	AM0 to AM5	Address modifiers (extended address, short I/O address, block transfer, supervisor/user, program/data, user definable functions)
Data control	DS0, DS1	Data strobes (upper/lower byte, word select)
	WRITE	Read/write data direction
	DTACK	Data transfer acknowledge
	LWORD	Long word (32-bit) data transfer
Interrupts	IRQ1 to IRQ7	Interrupt request—7 levels
	IACK, IACKIN, IACKOUT	Interrupt acknowledge and daisy chain
Bus arbitration	BR0 to BR3	Bus request—4 levels
	BG0 to 3IN/BG0 to 3OUT	Bus grant daisy chains
	BBSY, BCLR	Bus busy, bus clear
Interprocessor serial link	SERDAT	Serial data
	SERCLK	Serial clock
Error signals	SYSFAIL	System failure
	BERR	Bus error
	ACFAIL	Power failure
Power	5, ±12	Includes standby power line for battery backup
	5 Standby, gnd	
Miscellaneous	SYSCLK	16-MHz clock
	SYSRESET	System reset

P2 Expansion Signals††

Extended address bus	A24 to A31	Extended address range = 4G bytes
Extended data bus	D16 to D31	Extended data width = 32 bits
Power	5, gnd	Additional power and ground lines
Input/output	User I/O	64 pins in the two outside rows A and C available for I/O functions

†Primary signals are available on both single- and double-size Eurocard formats. All signals are active low or low true except SYSCLK, SERDAT, SERCLK, and Address and Data.

††Expansion signals are available only on double-size Eurocard format. P2 may be used entirely for I/O when expansion bus is not required.

system, a separate serial link with lines for serial clock and data, independent of the bus, is provided for message passing between boards. The indivisible READ/MODIFY/WRITE cycle also allows the use of semaphores to synchronize the multiple processors with each other or to lock out other processors. Seven levels of interrupt can be centralized or distributed among various processors on the system; any processor can service any interrupt level.

High speed data transfers are possible at rates up to 5M 32-bit transfers/s, or 20M bytes/s. Because of the asynchronous timing of the VME bus, processors, memories, and peripherals of varying speeds can reside in the same system, and any module can be upgraded to higher performance without affecting option, which mounts on the board. RAM is accessed by the 8088 CPU with no that can transfer large blocks of data by supplying a starting address to a slave device, followed by multiple data transfers.

The VME bus has been placed in the public domain and also placed before the IEEE as a proposed standard; other vendors are being encouraged by the originating firms to design cards for the bus. The joint announcement may circumvent the current P896 "Futurebus" standardization effort, now before the IEEE committee. According to a Mostek representative, the P896 effort was potentially leading to many special circuit requirements. Mostek, which previously participated in that effort, announced it will withdraw support.

Circle 241 on Inquiry Card

8-bit single board computer based on 5-MHz CPU

The iSBC™ 88/25 computer includes a CPU, system clock, read/write memory, nonvolatile ROM, I/O ports and drivers, serial communications interface, priority interrupt logic, and programmable timers on a single 6.75″ x 12.00″ board. (See Photo.) In addition, this device from Intel Corp is well suited for control oriented applications including process control, instrumentation, and industrial automation. Included in the 5-MHz 8088 CPU are four 16-bit byte addressable data registers, two 16-bit memory base pointer registers, and two 16-bit index registers, all accessed via 24 operand addressing modes.

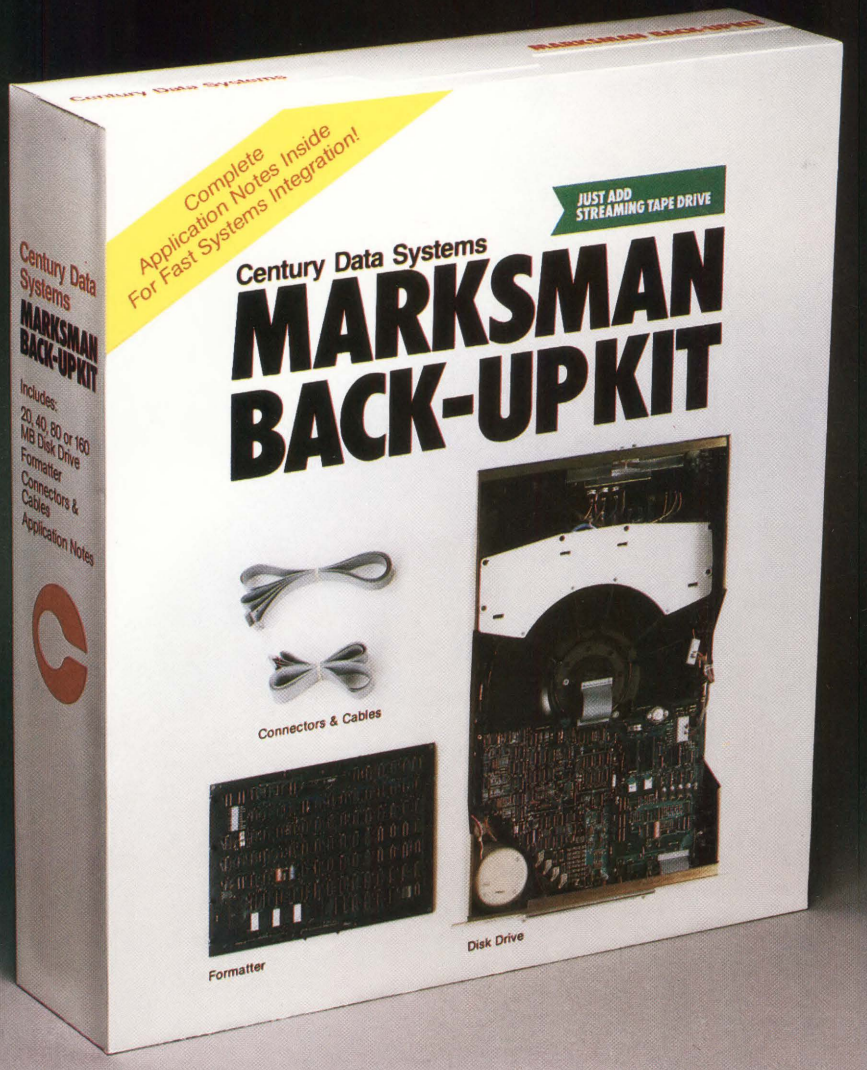
Variable length instruction format (including double operand instructions); 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD, and unpacked ASCII data; and iterative word and byte string manipulation functions are included in the CPU instruction. For enhanced numerics processing capability, the company's iSBC 337 MULTIMODULE numeric data processor extends the architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic, and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. 4k bytes of high speed static RAM are onboard expandable to 16k bytes through 4k-byte component expansion (2 x 2168 RAM) and/or 8k-byte MULTIMODULE expansion with the iSBC 302 MULTIMODULE RAM

(continued on page 37)

Century Data Systems
A Xerox Company

Drives for the 80's

Finally, an off-the-shelf answer to Winchester back-up.



Introducing the Intelligent Marksman Back-Up package. And the solution to the chronic problem of Winchester back-up.

And what a solution it is. Our new formatter is specially designed to control 20, 40, 80 or 160 MB Marksman Winchesters—and the Archive Sidewinder, Cipher Quarterback, or DEI Streamer ¼-inch tape drive for back-up.

A simple host adapter and software I/O drivers are all you need to tie into word and data processors utilizing interfaces such as S-100 or Multibus, and running operating system environments such as CP/M, MP/M, UNIX and others.

If that isn't enough, just one formatter will control two Marksman Winchesters, providing a system with a storage potential of 320 MB, in a minimum of space.

Continued on next page

Century Data Systems
A Xerox Company

Century Marksman drives: Because it's a jungle out there.

In the world outside the computer room, computer data faces constant danger.

The people out there smoke cigarettes and spill coffee. They raise dust and trip over power cords and do everything else no one would do inside the computer room.

Earlier generation disk drives just can't protect data from that kind of abuse.

But Winchesters can. A Winchester's sealed design makes it the perfect choice for any outside-the-computer-room application: Word and data processing, computer graphics, networked data storage, data entry, computerized numerical control and any other hostile environmental applications you can think of.

But ruggedness isn't the only advantage you get with a Winchester. There's also the massive storage capacities ranging up to hundreds of megabytes per drive. Which means you can build in a system's capacity to grow.

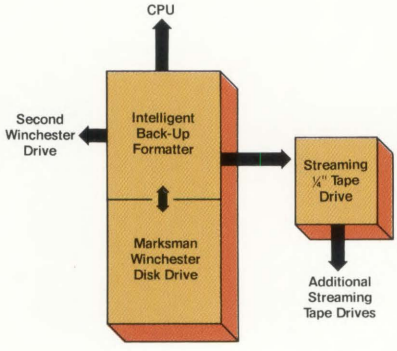
And finally, there's the Century Data Marksman Winchester. It combines all of these advantages with the lowest cost per megabyte in the industry.

So before you send any system out into the world beyond the computer room, be sure it's equipped with a Century Marksman Winchester.

back-up. *Continued from first page*

A storage system independent of the CPU.

But back-up isn't nearly all our new formatter offers. You also get an independent data storage package that doesn't tie up valuable CPU time.

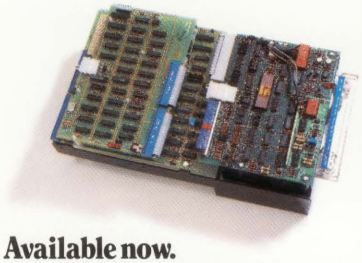


The formatter permits independent communication among all its interconnects: From disk to tape. Tape to disk. Or either drive to and from the CPU.

Which means operators can continue to use the CPU during back-up, and even interrupt the Winchester-tape intercommunication to pull out or insert data from the disk. Without specifically shutting down and restarting the back-up functions.

The advantages of streaming tape.

Compatibility with streaming tape back-up is another big plus of the new Century formatter. As a removable media, ¼-inch streaming tape is ideal for archiving data. It's also a low-cost, high-performance, no-maintenance tape option perfectly matched to the speed and capacity of a Winchester.



Available now.

Best of all, our new formatter isn't just a promise of something to come. It's available now, right along with our full line of Marksman Winchesters and full application notes.

So if you're an OEM, systems integrator or distributor, let's get together soon. And get the problem of Winchester back-up off your back once and for all.

Sidewinder is a trademark of Archive Corp.; Quarterback is a trademark of Cipher Data Products; Streamer is a trademark of Data Electronics Inc.; CP/M and MP/M are registered trademarks of Digital Research, Inc.; Unix is a trademark of Bell Laboratories; and Multibus is a trademark of Intel.

Century Winchesters don't crash, they land.

You've heard of crashed disks before. But you've probably never heard of one in a Winchester.

That's because Winchesters rarely crash. And at Century Data, we take special pains to make sure of it.

In addition to the standard protection of disk lubrication and feather-light heads, we've designed a unique braking system and special head landing zones where no data is stored.

During a power failure or reduction, the brakes automatically slow the disk in seconds rather than minutes. And the head is programmed to seek out it's special data-free landing zones.

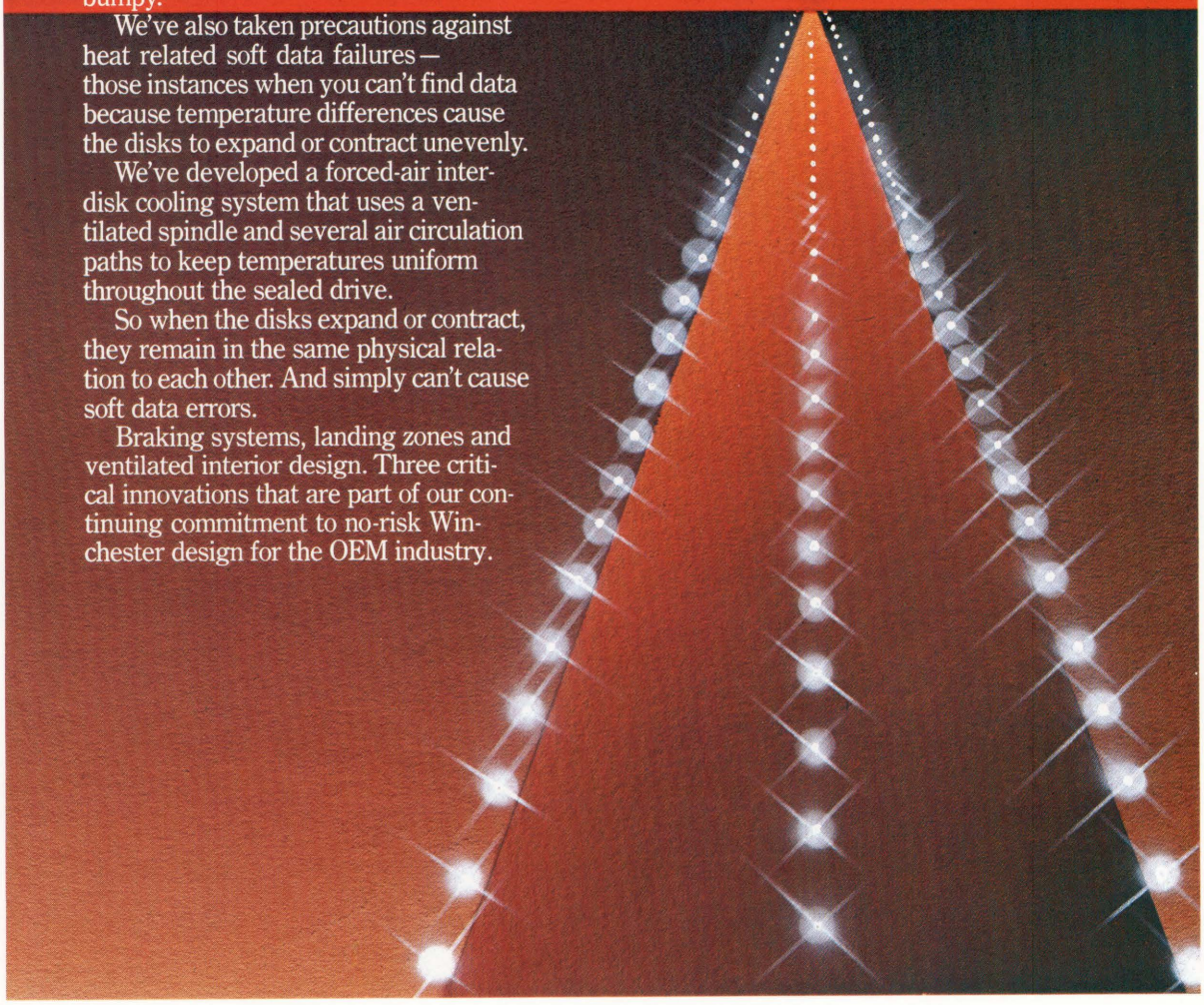
The combination not only prevents crashes, it virtually insures the data's integrity even if the landing is a little bumpy.

We've also taken precautions against heat related soft data failures — those instances when you can't find data because temperature differences cause the disks to expand or contract unevenly.

We've developed a forced-air inter-disk cooling system that uses a ventilated spindle and several air circulation paths to keep temperatures uniform throughout the sealed drive.

So when the disks expand or contract, they remain in the same physical relation to each other. And simply can't cause soft data errors.

Braking systems, landing zones and ventilated interior design. Three critical innovations that are part of our continuing commitment to no-risk Winchester design for the OEM industry.



Q: Why have you chosen Trident removable-pack drives for Japan, Mr. Kato?

A: Because of Century's design and commitment to quality.

Mr. Atts Kato is U.S. Manager for NELCO, the electronics subsidiary of Nissho Iwai—one of the largest international trading companies in Japan. The following is excerpted from an interview with Mr. Kato:

Q: After reviewing other manufacturers of removable-pack drives, what has brought you to Century?

A: Frankly, I've never seen such advanced facilities as Century's.

I've been involved in the computer business for twenty years, and have visited many U.S. computer companies. Century Data facilities for engineering, manufacturing and testing all indicate a serious commitment to disk drives.

This was a very important factor for me in selecting a manufacturer—one that can make hundreds of drives like Century has done for me.

Q: How are these drives being used in Japan?

A: We often sell the Trident drives to OEMs and systems houses, but we have other large end-users that buy quite a few. For example, Tokyo Electric Power, which is the largest utilities company in the world, and many Japanese broadcasting companies.

You see, the Japanese market situation is very similar to that of the U.S. Removable-pack drives are seen as having many desirable features, particularly storage capacity and removability. Winchesters are just now seen as becoming a good product to integrate into systems.

We see our disk business changing to Winchesters over the next few years, and this was another key reason why Century capabilities were so important to us.

As our demand for Winchesters grows, we will look upon Century to fill this need—particularly with their new products becoming available now and in the near future.

NELCO covers the entire Japanese computer market, offering individual components as well as totally integrated systems with extensive technical support capabilities for both hardware and software. And NELCO has chosen Trident removable-disk drives from Century Data Systems.

Now media compatible.

Our 300 MB Trident now provides full plug and media compatibility with other SMD-interface removable-pack disk drives. Now, Tridents can be integrated into systems without losing access to existing disk libraries.

If you would like to find out more about our proven drives and these attractive features, contact us at our address below, or feel free to give us a call.

For the full Story of the Century, please indicate the information you want, and we'll send it right away.

- ☐ Intelligent Marksman Backup Package
- ☐ Marksman Winchester Disk Drives
- ☐ Trident Removable-Pack Disk Drives
- ☐ I would like an evaluation unit of the above.

Name_____ Title_____

Company_____

Street_____

City/State_____ Zip_____

Phone (_____)_____

Send to: Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806

CD

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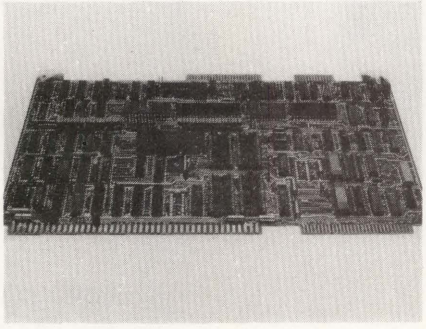
A Xerox Company

Century Data Systems
1270 N. Kraemer Blvd.
Anaheim, CA 92806

North American Headquarters
(714) 632-7500

wait states, yielding a memory cycle time of 800 ns.

In addition to the RAM, the board has four 28-pin sockets, configured to accept JEDEC 24/28-pin standard memory devices. Up to 32k bytes of EPROM are supported and up to 16k bytes of EPROM with 8k-byte increments are provided. Other JEDEC standard pinout devices are also supported, including bytewide static and integrated RAMs. The addition of the iSBC 341 MULTIMODULE EPROM option doubles the onboard capacity for these devices so that up to 64k bytes of EPROM are provided.



The computer contains 24 programmable parallel I/O lines, which are configured in combinations of unidirectional I/O and bidirectional ports by the system software. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector. The programmable communications interface is based on a company USART, provided with common communication frequencies by a software selectable baud rate generator. Mode of operation (ie, synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The USART provides full duplex, double buffered transmit and receive capability, parity, overrun, and framing error detection.

Three independent, programmable 16-bit interval timers/event counters are provided. Each counter is capable of operating in either BCD or binary modes, while two timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the programmable interrupt controller, and to the I/O terminators associated with the programmable peripheral interface, to allow external devices or a port to gate the timer or to count external events. For the RS-232-C USART serial port, the programmable baud rate generator is provided by the third interval timer.

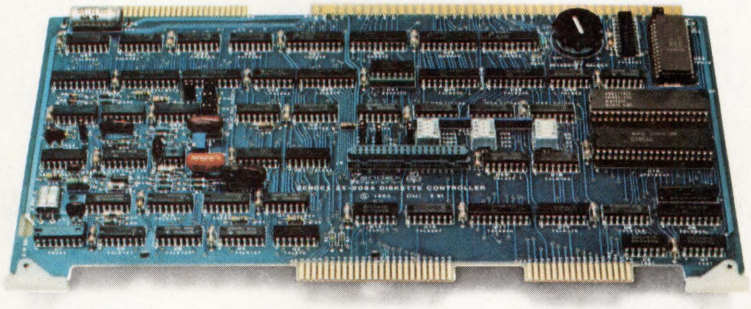
In addition, two 8-bit iSBX MULTIMODULE connectors are provided on the microcomputer. Through these connectors, additional onboard I/O functions may be added. **Intel Corp**, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

Circle 242 on Inquiry Card

THE ZENDEX Model ZX-208A DISKETTE CONTROLLER

FOR THE OEM USING THE MULTIBUS*

Single or Double Density IBM Formats for standard and Mini FDD Interfaces. Controls up to 4M Bytes of on-line storage. Use instead of Intel SBC-208.
For use by the OEM systems designer who demands the maximum in speed and efficiency with a minimum of hardware costs. Features NEC UPD765A FDC chip, DMA Controller, PLL Data separator and BUS Arbitrator. 5 volts only. Optional CP/M** System Disk available.



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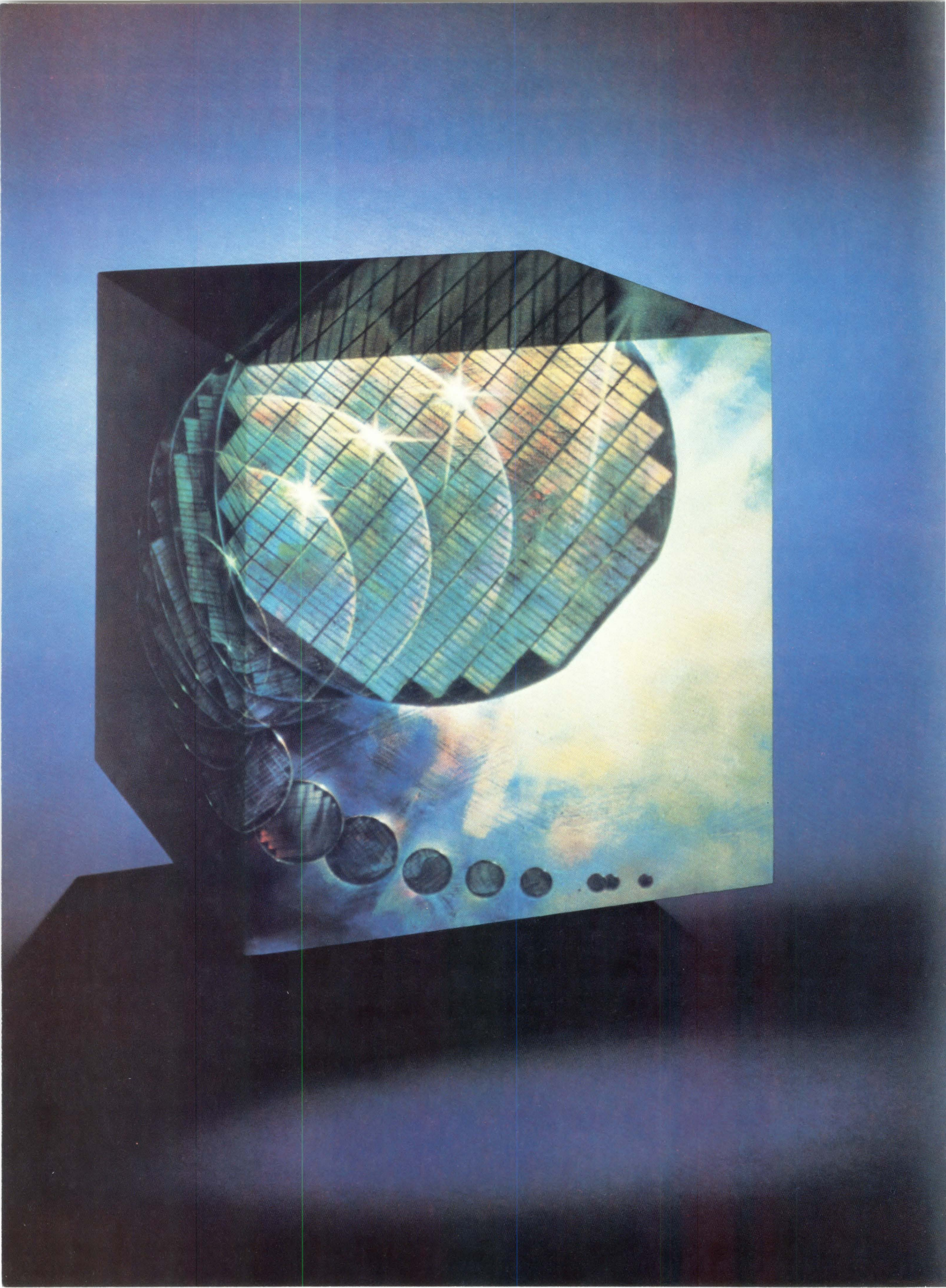

Another new standard from INMOS.

4K x 4/16K Static RAM

The IMS1420: High Speed. Low Power. Available Now.

The VLSI technology leader in 16K static RAMs introduces another industry first. Organized 4K x 4, the IMS1420 offers a chip enable access time as fast as 45ns.

Lowers System Cost

The low entry level price of $38.00 (100's) for the IMS1420-55 makes this new 4K x 4 a viable alternative to 4K x 1 and 1K x 4 fast static RAMs. It matches their speed, saves board space and reduces power consumption by at least a factor of four. Trade off your 4K designs today and lower your system costs.

Need Higher Speed?

The companion IMS1421 delivers even more performance where higher speed is a must. With a chip select access time as fast as 30ns, the IMS1421 sets a new speed record for 16K memories.

Naturally, both new RAMs operate from a single +5V (±10%) supply and are fully TTL compatible. They're packaged in industry standard 20-pin, 300-mil dips and also industry standard 20-pin chip carriers.

Application Note Tells You How

Check your current 4K static RAM designs today. Chances are good that one of the new INMOS 4K x 4 RAMS offers a better system solution. Call or write for our new application note that tells you how to make the switch - and save.

INMOS 16K STATIC RAMS					
Static RAM Family	Organization	Max. Access Time		Max. Power Dissipation	
		Chip Enable/Select	Address	Active	Standby
IMS1420-45*	4K x 4	45ns	40ns	600mW	165mW
IMS1420-55	4K x 4	55ns	50ns	600mW	165mW
IMS1421-40*	4K x 4	30ns	40ns	600mW	NA
IMS1421-50	4K x 4	40ns	50ns	600mW	NA
IMS1400-45	16K x 1	45ns	40ns	660mW	110mW
IMS1400-55	16K x 1	55ns	50ns	660mW	110mW

*Available 1Q 1982

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CIRCLE 23 ON INQUIRY CARD

Continuous processing system performs error checks in hardware to eliminate complex software

In answer to increasing demands for nonstop processing, Stratus Computer has developed a fail-safe business computer system that cuts costs by relying on hardware instead of software for error checking. The Stratus/32 continuous processing system eliminates the complex software task of checkpointing an online program between two or more computers, along with the unproductive processing overhead required for it.

Basic computational unit of the system, the processing module, contains a 20-slot chassis, dual 16M-byte/s system buses, dual power supplies, and battery backup. Each circuit board has automatic checking logic for immediate fault detection. The processor board holds four Motorola 68000 processors that are paired for self-checking operation, presenting two CPUs to the operating system. One of these is used for handling I/O interrupts and page faults, the other for user applications. Memory boards use 64k-bit memory chips; each board holds 2M bytes of error correcting memory. Moreover, intelligent controller boards all have their own processors, which offload much of the I/O processing from the processor board.

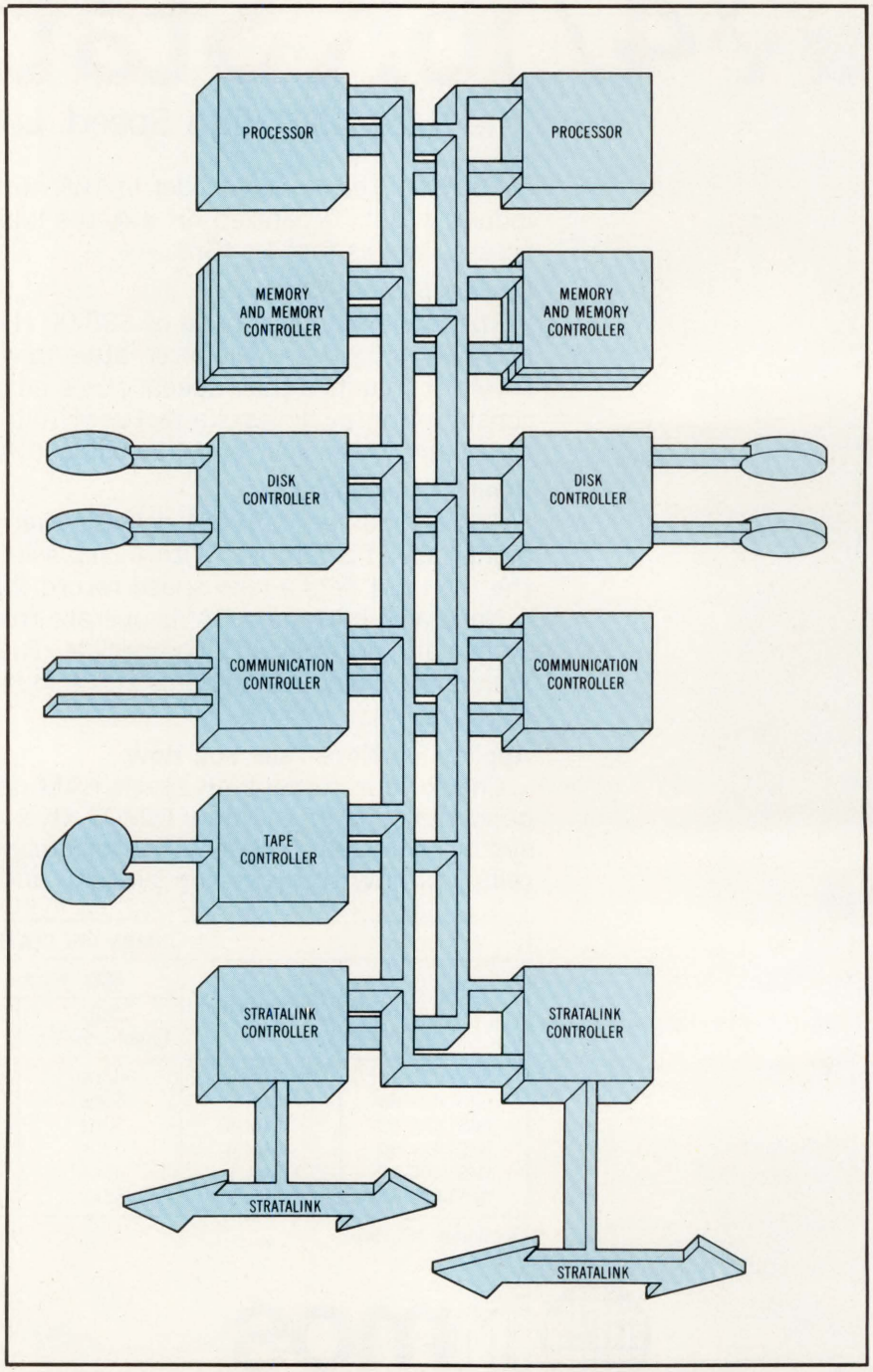
The module's dual CPUs function independently and process both the operating system and user programs in parallel. Additional microprocessors in the peripheral controllers further enhance performance. The communication controller, for example, offloads line protocol and character processing from the CPU. Other significant performance features are 16M-byte/s 4-level pipeline system bus, 375-ns 4-way interleaved memory, prefetching of memory references, I/O command chaining, multiple command chains for each controller, and 6 concurrent user memory translation maps in high speed memory.

The proprietary design uses hardware, not software, to detect hardware errors and recover from them. Errors are trapped and stopped the instant they occur. Parallel hardware in the system continues to operate on the problem uninterrupted, with no performance loss. In addition, complex error detection and recovery software typical of other failsafe implementations are not needed. Each operation is self-checked 8M times/s so that user data bases are never corrupted by bad data.

All boards are self-checking and can be replaced while the system is running; no service interruption occurs. A red light on each board automatically pinpoints the failing board. These features permit maintenance to be priced below that of IBM, the industry maintenance price leader.

Each processing module supports up to 8M bytes of duplexed memory, up to 64 terminals, and up to 16 disk drives; each storing 30M, 60M, or 143M bytes.

(continued on page 42)

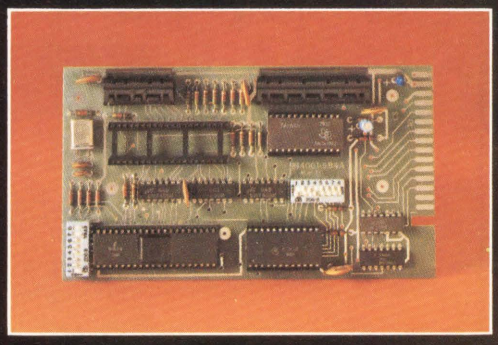


Duplexed components form the backbone of the Stratus/32 continuous processing system. Boards are totally independent and contain their own checking logic and diagnostics. Continuous processing is achieved by having two identical boards operating in parallel. Checking logic immediately detects malfunctions and failures. Failed boards are automatically removed from service before erroneous processing occurs or data are corrupted.

Oak puts E^3 up against the world's fastest typists.

In a keyboard market clogged with claims and confusion about "N-key-rollover," look to Oak's FTM® keyboard for the practical answer. It provides E^3-Entry Error Elimination. And that means precisely what it says. We challenge the fastest typists in the world to make it error. They can't.

Yet E^3 makes its real contribution to Oak's Full Travel Membrane (FTM) keyboard—and to you—in the cost column. You get the Entry Error Elimination and 100-million-cycle-plus performance you've got to have in a keyboard at prices far below those of keyboards with comparable performance. That's practical. Entry Error Elimination is a remarkably sensible microprocessor based N-key-rollover and phantom key lockout system developed by Oak engineers. Without the cost and complexity of Hall Effect and capacitive technologies.



And that's not all. Beneath the FTM keyboard is Oak's proven, industry-leading membrane switch technology. So you get all the good things of membrane switching—reliability, durability, RFI and EMI resistance, design flexibility, and—of course—low cost. All without sacrificing the qualities you demand in a keyboard, right down to human engineered industry standard feel and touch.

Call or write us today for the data and details to prove it. You can't afford not to call Oak.

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Circle 150 for Salesman to Call

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Versatility and durability at a low price... you'll find all that and more in RCA's rugged VP-3300 series Interactive Data Terminals. Computer applications include data entry, data and graphic display, process control and time-sharing. And they are compact. Perfect for use as remote or portable terminals.

- RF or Video output. Designed to work with standard TV sets or monitors.
- Unique color-locking circuitry for sharp color graphics and rainbow-free characters.
- 128 resident and dynamically redefinable character set.
- 20- and 40- character formats.
- Selectable data rates up to 19.2 kilobaud.
- Standard ASCII encoding with RS-232C and 20 mA current loop interfaces.
- LSI video and microprocessor control.
- Spillproof, dustproof unitized keyboards.

Plus much more.

For more information write RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604, or call 717-291-5848. To order, call toll-free, 800-233-0094.

*OEM quantity price. Model VP-3301 (video/audio output).

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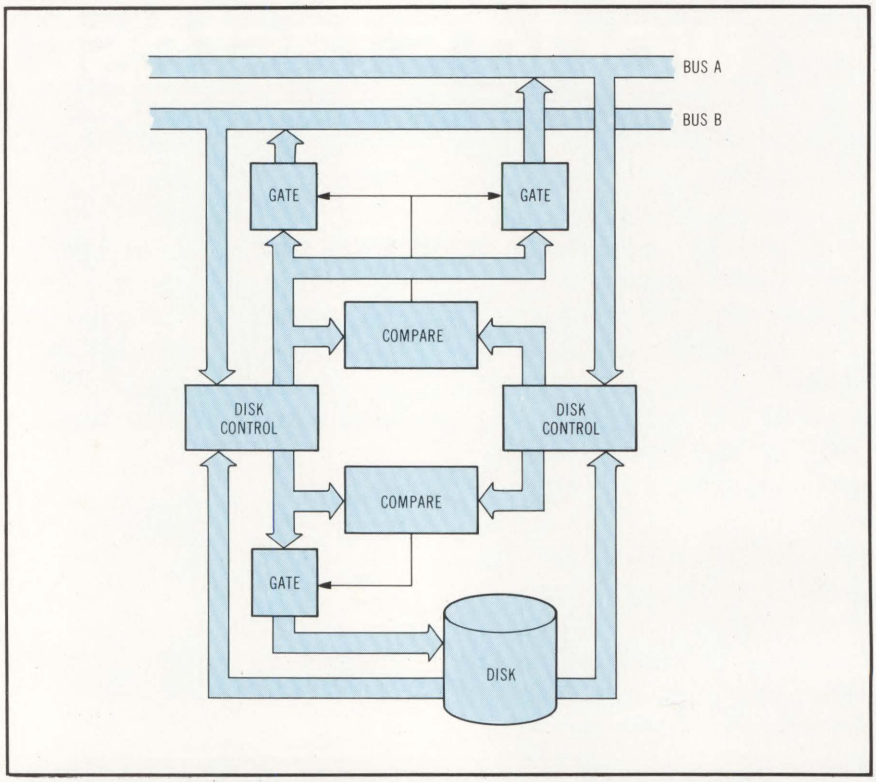

Compare logic within disk controller of Stratus/32 checks results just before data are sent, and if comparison fails, data are not transferred. Instead, controller instantaneously disconnects itself from bus, turns on its red light, and sends maintenance interrupt to CPU.

Other peripherals include line printers, letter quality printer, and magnetic tape.

A distributed processing system, Stratus/32 connects to existing networks via IBM communications capabilities. StrataNET, the networking system, uses public networks via the X.25 communications protocol. The system has a built-in ability to access any other like system at a remote site as if that system were local. Thus, operating a network of computers is no more difficult than operating a single local system.

A system is formed from 1 to 32 processing modules. Multiple modules are connected with the high speed StrataLINK, which operates as a ring network to transfer data at up to 2.8M bytes/s. Modules can be located as far as several miles apart.

In addition, VOS, the Stratus Virtual Operating System, is self-configured during initialization and requires no system generation. The virtual memory based system supports multiple users on multiple processing modules and network configurations, such that it appears as a single virtual computer system. Users have up to 12M bytes of virtual memory available for each program. Capitalizing on the system's 32-bit architecture, the operating system emphasizes high level languages, with the initial release including COBOL 74, BASIC, and PL/1, supported by a high level interactive symbolic debugger. A multikey data manager, IBM and X.25 communications facilities, word processor, and general utilities complete the initial release.

An entry configuration costs $123,350 and includes CPU, communication controller supporting up to 32 asynchronous lines or 16 synchronous lines, 2M bytes of memory, 60M-byte disk, terminal, remote maintenance modem, streaming tape drive, VOS operating system, and COBOL execution. This configuration offers protection against all hardware failures. Any component can fail without the user experiencing loss of capability or performance. **Stratus Computer, Inc,** 17-19 Strathmore Rd, Natick, MA 01760.

Circle 243 on Inquiry Card

Multifunction computers offer 0.5M-byte mass storage in desktop units

To provide 0.5M bytes of mass storage in a desktop unit, Convergent Technologies has mounted both mini-floppy and miniWinchester disk drives in the same enclosure with the processor and display. Designated AWS™ Workstation to indicate the target market—application workstations—each unit consists of an Intel 8088 processor, up to 512k bytes of RAM (based on 64k RAM chips), an 80-character by 28-line video display unit, and mass storage.

Use of VLSI components and innovative packaging condenses all minicomputer elements into the desktop unit. The processor, RAM, input/output, and video control logic are on a single printed circuit board. An optional board contains disk controller electronics. Elements are packaged together with the disk units in a simple lectern, mounted on the pedestal that carries the adjustable display unit. Floppy disks are simply dropped into the top of the lectern "toaster style." The keyboard detaches from the unit and can be placed anywhere within reach of the 5′ (1.5 m) coiled cable.

The units can either stand alone or be interconnected into a local network via a high speed data link, sharing peripherals and data buses but not processing power. High responsiveness is the result, with the ability to support diverse applications operating on the same data base simultaneously. Workstations can serve independently in a standalone mode, as master stations controlling a cluster and providing resources such as disk storage and printer services to other workstations, or as cluster stations that use the master stations' resources. Moreover, a standalone system can be upgraded to a local network without software modifications.

The CTOS™ operating system supports realtime, multitask operation, and supports COBOL, FORTRAN, BASIC, and Pascal, plus assembly language. In addition to the multitasking operating system, software components include a selection of program development tools, four standard programming languages, communications protocols, and text and data management facilities. Data management facilities include multikey ISAM, a forms facility, and a sort-merge facility. In addition, 3270 terminal emulator, 2780/3780 remote job entry terminal emulator, asynchronous terminal emulator, and X.25 emulator communications protocols are supported. Two RS-232-C communications channels can be programmed for a variety of tasks, with software selectable baud rates from 110 to 19.2k. An RS-422 channel operates at up to 615k baud, and all three channels can be programmed to support a number of synchronous and asynchronous protocols, including BiSync, ADCCP, SDLC, and HDLC.

There are four members in the AWS family. The AWS-210 supports 128k- to 512k-bytes RAM with no mass storage, and can only be used as a cluster station. AWS-220, which supports 128k- to 512k-bytes RAM and one mini-floppy, can be used as standalone system or cluster station. Supporting 128k-bytes RAM with two minifloppy units, the AWS-230 can be used as standalone system or as cluster station with local mass storage. AWS-240 supports 256k- to 512k-bytes RAM, has a mini-floppy and a miniWinchester, and can be used as standalone system master station or as cluster station.

In single units, prices range from $3990 for a -210 cluster station to about $11,500 for a -240 with 512k RAM and a combination of floppy and Winchester drives. **Convergent Technologies,** 2500 Augustine Dr, Santa Clara, CA 95051.

Circle 244 on Inquiry Card

16-bit small business systems extend performance with memory management

Up to eight users can share processing power of the 16-bit ACS8600 microcomputer systems. Based on Intel's 8086 microprocessor, Altos' latest systems provide up to 1M bytes of main memory plus online floppy and Winchester hard disk storage from 1M to 80M bytes. The systems are compatible with a variety of operating systems and business application software programs, and feature error detection and correction along with a memory management system.

Organized around three processors, the 8086 for system and applications control, the 8089 for DMA and I/O processing, and the 8087 for optional fast floating point arithmetic, the ACS8600 addresses up to 1M byte of memory directly, in blocks of 64k. Memory management is organized as 256 pages of 4k bytes and provides both position independence

(continued on page 44)

ASCII Encoded Keyboards.

Where can you buy as much keyboard for as little as $49?*

Feature for feature, no keyboards offer you more value and durability for the money than the RCA VP-600 series.

58-key typewriter format, or typewriter plus 16-key calculator-type keypad. Both versions available with parallel or serial output. These keyboards are particularly suitable for hostile environments.

- Spillproof, dustproof, unitized keyboards.
- Flexible membrane switches with contact life rated at greater than 10 million operations.
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- Low power, 5V DC operation.
- Three serial output modes: RS-232C, 20 mA current loop and TTL.

For more information, write RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604, or call 717-291-5848. To order, call toll-free, 800-233-0094.

*OEM quantity price. Model VP-601 (parallel output).

RCA

CIRCLE 26 ON INQUIRY CARD

and protection for the contents of the memory. The physical location of each page, plus 13 flag and control bits, are stored in the 256- x 21-bit memory management RAM, which maps logical addresses to physical addresses in memory so that data may be stored in random, noncontiguous sectors and fewer disk swaps are required.

The 8086 CPU provides some memory management through the use of segment registers. The 8086 logical address is generated by appending four 0 bits to the 16-bit segment number and adding the 16-bit offset specified by the instruction. Of this 20-bit logical address, 8 bits specify a logical page. The 256- x 21-bit memory management RAM substitutes an 8-bit relocation value that specifies a physical address when it is recombined with the 12 offset bits. At the same time, 11 attribute bits are examined by the comparator to test the validity of the access.

Main memory is organized in 16-bit words plus six bits for error detection and correction. When a word is written into memory, the error correction circuitry uses a modified Hamming code to generate six check bits for each word; when the word is read out of memory, these check bits are compared with a new set of check bits generated during the read process. If both check bit sets are alike, no error has occurred.

The Hamming code is chosen so that the pattern generated by comparing the two sets of check bits will have an odd number of 1s if a single error has occurred. Each pattern is associated with a particular memory or check bit, so that the error correction circuit can then correct the error by inverting the bit in error.

If the pattern has an even number of 1s, more than one bit is in error. The CPU can "scrub" the error by reading and rewriting the reported memory location. The error correction system cannot correct more than one error; it will, however, report both single and multiple bit errors to the CPU which can take corrective action. The CPU can also log the error for diagnostic and maintenance purposes.

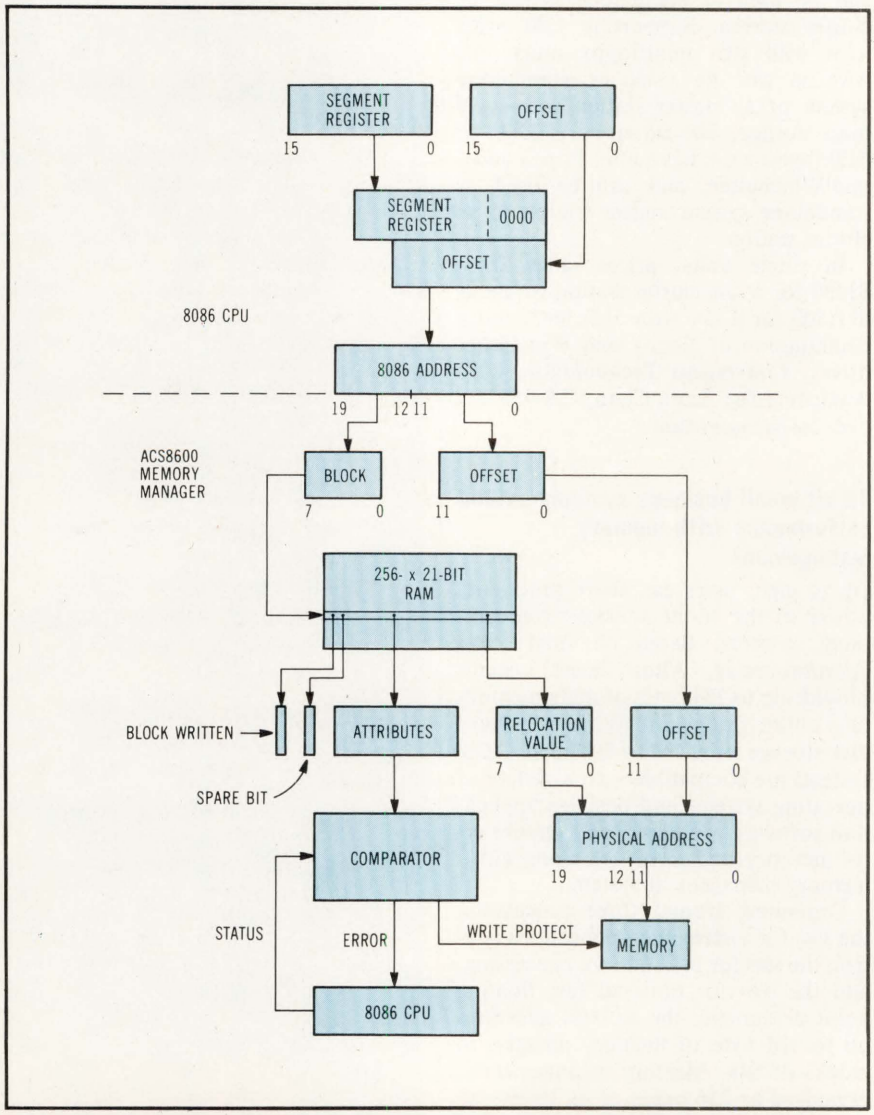
The operating system allocates memory to each user or task. The amount of memory allocated depends on the memory available and the size of the operating system. For operating systems that can swap memory out to disk, a task can use more memory than is available in RAM.

The family supports four operating systems, including the XENIX operating system, Bell Labs' UNIX V7 adapted by Microsoft. It also supports CP/M-86, MP/M-86, and OASIS-16 operating systems.

In addition to eight terminals and other peripherals, the system supports expansion through a MULTIBUS port and accepts both synchronous and asynchronous communications protocols. It can handle network data rates up to 800k baud for high speed networking.

The basic system, with 512k bytes of main memory, 10M-byte hard disk, and floppy backup, lists for $12,990; the same system with 1M dual floppy storage, no hard disk, and 128k-bytes main memory sells for $8,990. **Altos Computer Systems**, 2360 Bering Dr, San Jose, CA 95131.

Circle 245 on Inquiry Card



Memory management circuitry in ACS8600 maps memory in high speed RAM, thus allowing system to support multiple users while maintaining high performance.

Engineering workstation reduces electronic design time using traditional methods

Time required to design complex electronic equipment can be substantially reduced using the LOGICIAN™ engineering workstation. Designed to give engineers the power and flexibility of a personal computer without requiring them to change their design methods, the system allows engineers to communicate with a computer in efficient graphics language. Based on familiar concepts and procedures, the workstation combines traditional design methods with computer-derived benefits to improve productivity.

(continued on page 46)

Perfect for any occasion.

Whatever your business or application, there's a TermiNet® 200 printer to fit it perfectly.

From mini/micro computer output to transaction processing, General Electric TermiNet 200 printers deliver the high performance you want. Like outstanding throughput, excellent print quality for up to nine-part forms, reliable operation, minimum downtime, and low operating costs. Choose the one to match your exact needs. A basic line printer with serial or parallel interfacing. A forms access printer with precise alignment and no paper waste. A split platen printer that does two different jobs at the same time. Plus a highly versatile KSR.

For more information on TermiNet 200 printers, contact your local GE distributor. Or send in the coupon today.

Quality that will make a lasting impression

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Mail today to: General Electric Company, TermiNet 794-57, Waynesboro, VA 22980. Telephone: (703) 949-1474.

☐ Send me more information about TermiNet 200 printers.
☐ Have a sales representative contact me.
☐ I'm also interested in a TermiNet 200 printer demonstration.

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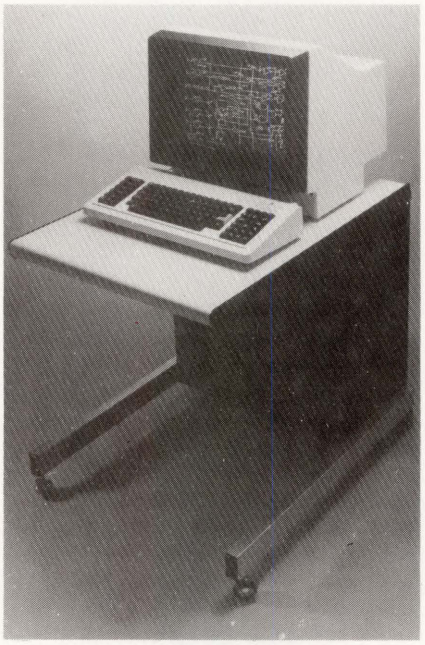
An advanced form of computer aided design, the system addresses the critical front end of the design cycle—system architecture, logic design, data management, local analysis, and documentation. Moreover, it acts as a preprocessor that provides a single window into the elements of electronic design. Thus, the engineer can address RTL simulation, logic simulation, circuit simulation, connectivity verification, and test generation from a single terminal in either interactive or automatic mode.

The unit is suitable for design of both complex electronic systems, and very large scale integrated subsystems used to implement these systems. It operates on the principle of hierarchical design, which allows engineers to conceive an overall architecture, then move through the design via block diagrams. Within these block, logic, and schematic diagrams, the engineer creates symbolic representations of transistor or integrated circuits. An electronic data base serves as a single source of block and schematic diagrams, simulation modes, connectivity specifications, and design documentation. Because the system database manager maintains the integrity of the block interfaces between levels of the design hierarchy, the design task can be partitioned among multiple designers and even design groups.



Daisy Systems' engineering workstation captures design details with schematic editor and provides modeling system to interface with simulation programs.

Password protection is available to prevent unauthorized use of system information. Privileged users can designate individual file access to be "read only" or "read/write."

For accurate release control, the system keeps full archival records of what versions of the design have been released. The configuration control facility also provides accounts of what portions of the design hierarchy have been partitioned, who is responsible for them, and when they were assigned. In addition, the workstation facilitates the definition of design standards. These standards, which can be partially or completely controlled by a "data base administrator," are stored in the workstation's component library. The libraries are then used by the engineer as he designs his circuit.

When an engineer is ready to submit a design for simulation—RTL, logic, circuit, and so on—the integrated modeling system extracts the relevant connectivity description and modeling statements from the data base; characterizes these data for a specific target simulator; and submits the file to the user's mainframe computer. This modeling can have a major impact on the design cycle by eliminating the tedious and error prone task of manually coding simulator input files. Once the simulation is complete, the results can be transferred back to the workstation for review, plotting, and storage.

The workstation supports both automatic and interactive physical design approaches. If automatic placement and routing programs are being used, the workstation will extract the formatted logical network description from the electrical database for input to the placement and routing system. In interactive design environments, a complete hardcopy documentation set can be generated on an optional printer/plotter. Once the physical description of the circuit has been compiled, the modeling system then compiles the connectivity specification necessary to verify the interconnect integrity.

A schematic editor, the primary user interface, captures design and detail of all logic elements necessary for implementation. Instructions are executed in an English-like language that is forgiving to the novice or infrequent user. The unit's modeling system provides an interface to different simulation and analysis programs.

The multiple processor system is interconnected via the standard Intel MULTIBUS. System processor is a single-board computer based on an Intel 8-MHz 8086 microprocessor with 512k bytes of RAM. This processor and its resident UNIX-like operating system allocate system resources and execute application programs. A proprietary graphics processor interfaces to a 1022 x 826 pixel, 17″ (43 cm) diagonal display, providing a high level of graphics performance.

All system software and user files are stored on an internal 10M-byte Winchester disk, with a 1M-byte floppy disk unit for archival storage and data transport. A parallel port facilitates optional hardcopy output.

A serial RS-232-C port connects to a host mainframe at rates to 19.2k baud and a high speed serial interface supports future network expansion at data rates to 615k baud. **Daisy Systems Corp**, 2118 Walsh Ave, Santa Clara, CA 95051.

Circle 246 on Inquiry Card

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At last, there's a multi-user microcomputer system designed and built the way it should be. The CompuStar™. Our new, low-cost "shared-disk" multi-user system with mainframe performance.

Unlike any other system, our new CompuStar offers what we believe to be the most practical approach to almost any multi-user application. Data entry. Distributed processing. Small business. Scientific. Whatever! And never before has such powerful performance been available at such modest cost. Here's how we did it . . .

The system architecture of the CompuStar is based on four types of video display terminals, each of which can be connected into an auxiliary hard disk storage system. Up to 255 terminals can be connected into a single network! Each terminal (called a Video Processing Unit) contains its own microprocessor and 64K of dynamic RAM. The result? Lightning fast program execution! Even when all users are on-line performing different tasks! A special "multiplexor" in the CompuStar Disk Storage System ties all external users together to "share" the system's disk resources. So, no single user ever need wait on another. An exciting concept . . . with some awesome application possibilities!

CompuStar™ user stations can be configured in almost as many ways as you can imagine. The wide variety of terminals offered gives you the flexibility and versatility you've always wanted (but never had) in a multi-user system. The CompuStar Model 10 is a programmable, intelligent terminal with 64K of RAM. It's a real workhorse if your requirement is a data entry or inquiry/response application. And if your terminal needs are more sophisticated, select either the CompuStar Model 20, 30 or 40. Each can be used as either a stand-alone workstation or tied into a multi-user network. The Model 20 incorporates all of the features of the Model 10 with the addition of two, double-density mini-floppies built right in. And it boasts over 350,000 bytes of local, off-line user storage. The Model 30 also features a dual drive system but offers over 700,000 bytes of disk storage. And, the Model 40 boasts nearly 1½ million bytes of dual disk storage. But no matter which model you select, you'll enjoy unparalleled versatility in configuring your multi-user network.

Add as many terminals as you like - at prices starting at less than $2500. Now that's truly incredible!

No matter what your application, the CompuStar can handle it! Three disk storage options are available. A tabletop 10 megabyte 8" winchester-type drive complete with power supply and our special controller and multiplexor costs just $4995. Or, if your disk storage needs are more demanding, select either a 32 or 96 megabyte Control Data CMD drive with a 16 megabyte removable, top loading cartridge. Plus, there's no fuss in getting a CompuStar system up and running. Just plug in a Video Processing Unit and you're ready to go . . . with up to 254 more terminals in the network by simply connecting them together in a "daisy-chain" fashion. CompuStar's special parallel interface allows for system cable lengths of up to one mile . . . with data transfer rates of 1.6 million BPS!

Software costs are low, too. CompuStar's disk operating system is the industry standard CP/M*. With an impressive array of application software already available and several communication packages offered, the CompuStar can tackle even your most difficult programming tasks.

Compare for yourself. Of all the microcomputer-based multi-user systems available today, we know of only one which offers exactly what you need and should expect. Exceptional value and upward growth capability. The CompuStar™. A true price and performance leader!

INTERTEC DATA SYSTEMS®

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CIRCLE 29 ON INQUIRY CARD

Broad range of CAD/CAM systems spans needs of small to large organizations

A family of CAD/CAM systems has been introduced and demonstrated in conjunction with the recent announcement of the acquisition of Redac Interactive Graphics, Inc, Littleton, Mass, by Racal Electronics Ltd. The U.S. company will henceforth be known as Racal-Redac, Inc.

CAD/CAM products range from a microprocessor based system for firms which design as few as ten PCBs annually, to larger multiterminal systems for companies with heavy CAD/CAM workloads. All systems employ auto-interactive design that allows skilled designers to interact with the computer's automatic design power using high speed graphics displays.

Lowest cost system in the line, CADET II is a 16-bit microprocessor based system supplied with a raster refreshed CRT and 9-track magnetic tape drive for photoplotting. It generates artwork for 1- to 4-layer PCBs with dimensions up to 25″ x 25″ (64 x 64 cm) with ±0.001″ (0.025-mm) registration accuracy and repeatability, and offers a choice of 511 components.

Design aid repertoire includes component placing, track routing, design rules checking, and post-processing. Among the routing options are a power and ground bus router, memory router, and orthogonal channel router. These routers are reentrant, allowing the designer to interactively define critical signal paths. An automatic aid called Reconnect ensures that, for a given net of connections, the path between net points on the PCB is the minimum possible length.

Several facilities achieve error-free design. A redundancy check on input data guarantees correct starting data. During the router phase the data base is secured; the system will not allow routing to incorrect pads or to the wrong side of single-layer pads. A design rule check finds shorts or violations of minimum clearances as defined by the user.

Standard outputs include artwork, drill drawings, silkscreen drawings, solder masks, pad masters, and assembly drawings. A printer/plotter is optional. The CADET II system is priced at $76,000 with 30-day delivery.

Designed for firms or departments with two to four designers and draftsmen, RACAD is a CAD system for mechanical design, 2-D drafting, plant facilities planning, PCB design, schematics, and logic diagrams. The self-prompting system creates drawings using a combination of lines, arcs, fillets, and circles. Among the features are automatic dimensioning, crosshatching, pattern generation, symbol library, mirroring, and variable text.

RACAD hardware includes a Tektronix 4054 microprocessor based high resolution graphics computer, and a Tektronix 4663 interactive digital plotter. For larger formats there is a choice of CalComp plotters. A 1.2M-byte floppy disk drive is provided for storage of drawings, and multiple terminal system configurations are available. Supplied complete with hardware, software, and a one-week

(continued on page 50)

Protect critical electronic equipment from power fluctuations with a Deltron Line Regulator

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- ☐ Latched inputs.
- ☐ 192 power I/O points per station.
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Remote process control through SAMUX II.

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CIRCLE 31 ON INQUIRY CARD

CADET II low cost PCB CAD system. All commands are designer friendly. Functions are available via keyboard or stylus selection. CRT Prompter reviews what has been done and directs to next procedure.

training course, a single-station system is priced at $65,000, with delivery in 30 days.

CADENCE is a multi-user, multi-applications CAD/CAM system; it consists of a PDP-11/34 CPU with two or more designer terminals attached, one or more alphanumeric terminals, and associated output plotters and peripherals. The CPU runs under the RSX-11 multi-user operating system.

Each designer terminal has local processing, graphics control, and data storage for distributed processing capability. Up to six remotely located designer terminals can be added with no degradation in system performance. System CPU handles database control, data inputting, editing, and verification. It also acts as the host/driver to a variety of plotters, paper tape punches, and mag tape drives. Schematic, PCB, and assembly drawing libraries are held in the central PDP-11/34. The central library makes data available at individual designer stations.

CRT stations with full editing facilities can be used for preparing and checking initial data for circuit analysis, logic simulation, schematics drawing, and PCB designs. Circuit data compiled during simulation can be transferred to the schematic and PCB design programs, providing automatic data transfer facilities from logic design to the final PCB. Expansion of the system can be accomplished at low cost by using CADETS, which can communicate freely with the CADENCE system via RS-232-C asynchronous serial links. Price of a basic 2-terminal CADENCE system is about $300,000. **Racal-Redac, Inc**, One Redac Way, Littleton, MA 01460.

Circle 247 on Inquiry Card

Range of factory control computer and communications products announced

The HP 1000 automation system, a low cost microsystem for automation workstation tasks requiring computer graphics, and the enhanced DATACAP/1000 factory data collection software package were recently announced by Hewlett-Packard Co. Moreover, the company has developed less expensive ways to interconnect its computer products within a manufacturing facility.

These products emphasize expanded data communications and computer networking capabilities. For example, the Data Link has been redesigned to become a general purpose communication link. Initially offered as the connection between the 1000 computer and factory data collection terminals, the Data Link can now accommodate the company's 1000 computer systems, 9826/35/45 desktop computers, a range of CRT terminals, data capture terminals, and data couplers.

In addition, Data Link has a new multidrop capability that lowers the cost of creating local computer networks. 1000 computers can now communicate with each other using the company's DS/1000-IV networking software over twisted pair cables. The multidrop scheme provides store and forward message handling, automatic message rerouting, and message integrity assurance, and requires only one interface board for each node.

Data Link is typically used with a master 1000 computer and up to 128 slave devices. With the company's desktop computers and terminals as subordinate equipment, data can be communicated at 9600 bps. Multidrop DS/1000-IV on the Data Link also uses a 1000 as the master system, but subordinate computers can communicate at a faster 19,200 bps. Either method is suitable where computers and data capture devices require low volume, occasional transfer of data; involving applications such as supervisory control, reporting summary information, sending end of shift reports, and factory data collection.

Also introduced were the 1000 automation processor and the 2250 measurement and control processor. These processors form a system suitable for a range of industrial automation applications such as machine monitoring and control, process supervision and control, and automated electromechanical product testing.

Packaging for the 1000 automation system can be a standard computer cabinet or a sealed NEMA-12 enclosure, for operation in harsh industrial environments. Although the system is capable of standalone operation, it is primarily configured to operate as a node in the company's computer network using either DS/1000-IV high speed, point to point or DS/1000-IV multidrop communications over the Data Link.

Concurrent with these announcements was the introduction of the 1000 model 5 graphics microsystem. Manufacturing applications include use as a management information system, where the graphics capability can convert data into line graphs and bar and pie charts. As a realtime computer, it can control instruments or machines and graphically display status information to operators. The model 5 may also be linked in DS/1000-IV point to point or multidrop networks.

A number of major enhancements also were announced for DATACAP/1000, the company's factory data collection software package. With a 1000 computer system and multiple data capture terminals, the software forms a DATACAP/1000 factory data collection system. These systems support up to 92 data capture terminals. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 248 on Inquiry Card

Dr. Robert Smithdas is blind, nonhearing, and nonverbal. He is a published poet.

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It's the first DI CMOS switch that's μP compatible.
Our new AD7590 series of protected (latch-up proof) switches is the perfect solution to the microprocessor to data latch to analog switch design problem.

They're designed with the data latches built in, so you get a clean, simple, "all-in-one" design that saves time and precious board space. These new switches also feature overvoltage protection up to ±25V above the power supply, low R_{ON}: (75Ω), and buffered switch logic. And they're TTL and CMOS compatible.

It costs no more to go state-of-the-art.
Available in plastic for only $4.95, or in a hermetically-sealed ceramic package for $8.95, these superior new switches are not only a better alternative, they're a cost-effective one.

And it's available in three different configurations.
Our AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP.

ANALOG DEVICES

They differ only in that the switch control logic is inverted. Our AD7592DI comes with two independent SPDT switch packages in a 14-pin DIP.

For more information on the first analog switches designed to turn on designers, contact Doug Grant or Don Travers at (617) 935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

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CIRCLE 32 ON INQUIRY CARD

Multi-user development system supports design team approach

Developed specifically for microcomputer design teams, the 8560 is the third member of Tektronix's 8500 series of development systems. Other members of the family are the 8550 single-user system and the 8540 host integration unit. The 8560 system supports large scale microcomputer development efforts by supplying tools such as text processing and documentation tools, a team oriented file system, and utilities for automating the construction and alteration of program modules.

Each member of a design team also has access to standard development tools. Assemblers and compilers for 8- and 16-bit chips, loader/linkers to combine object files into executable object code, and editors (including an advanced screen oriented version) are accessed from software workstations. Pascal compilers will soon be available. Integration and debug tools, including emulators and a trigger trace analyzer, are available in the 8540 integration unit, which functions as a hardware workstation.

The 8560 hardware is based on an LSI 11/23 CPU that operates with frontend I/O processors (one for every four ports), which results in over 90% of the terminal I/O being off-loaded from the main processor. In addition to supporting programmable baud rates up to 9600 bps for RS-232 and remote communication, the I/O processors support the Tektronix high speed interface (HSI) operating locally at 153.6k baud up to 2000'.

System memory can be expanded from the standard 128k bytes to 256k bytes. Mass storage includes a 1M-byte flexible disk and a 35.6M-byte Winchester hard disk. An intelligent disk controller works in conjunction with the main processor to optimize disk I/O functions. Up to eight workstations and two spooling line printers are supported, while standard RS-232 CRT terminals can be used as software development workstations. Access to the system's software development capability can be expanded by adding terminals.

The 8540 integration unit is recommended as the integration/debug workstation. To add flexibility, the 8540 can be configured with the 8560 in different communications modes. One mode allows a single terminal to serially communicate with two 8540s to simultaneously emulate two processors in a single prototype. Debug information from both processors can be formatted using TNIX commands to suit the user's needs. The integration unit provides the user with realtime, transparent emulation for many 8- and 16-bit processors, along with a maximum 128k-byte emulation memory capacity, memory mapping, symbolic debugging, trace, and service requests for I/O simulation. Assemblers are currently available for the Z8000, 8086, 6809, Z80A, MCS 48 family, 8080, and 8085. In addition, the 6800/01/02 and 68000 will soon be supported. Emulators for use with the 8540 integration unit are available for the Z8000, Z80A, 6809, and 8085; emulators for the 68000, 6800/01/02, 8086, 8080, and MCS 48 will be available early this year.

(continued on page 54)

Now you can use the intelligent sonic digitizer.

Here's a whole family of high precision sonic digitizers from Science Accessories Corporation, all pre-programmed for the calculations you need to make right now. Most GP-6 models are microprocessor-based; they automatically perform mathematical computations previously requiring external processors or hand calculation. Four additional non-μp models are also available. And if we don't offer a GP-6 with the programming you need, we can develop firmware for your specific requirements.

Standard GP-6 Programs
Model 6-30
Origin offset
Incremental mode
Menu capability
Model 6-40
All the above
Area calculation
Line length calculation
Variable scaling
Model 6-50
All of the above
Axis rotation
Slope calculation
Polar or cartesian coordinates
Angle calculation

Although the customer shown here requested a clear acrylic work surface on which to attach the menu, two dimensional digitizing employing our L-frame sensor assembly requires no fixed data tablet. An unencumbered, active work area of up to 5' x 6' allows direct interaction with a variety of images, including CRT and plasma displays, projections from x-rays and films, maps, drawings on drafting tables . . . any two dimensional graphic material.

Either a stylus, a cursor with cross hairs, or both may be supplied with GP-6 systems to take data or to make menu selections. As easy to use as a ball point pen, the stylus contains both sonic energy generating gap and a ball point ink cartridge available in a choice of ink colors. Alternately, a pushbutton controlled cursor may be substituted for the stylus; pushbutton switches can permit the user to control program selection. Output for these GP-6 digitizers is in BCD Cartesian (X-Y) coordinates and is available compatible with RS-232 or IEEE 488-1975. We even offer optional resolution to 0.005".

There may be lower cost digitizers available (like our GrafBar GP-7, for instance), but you can't find more capability than a μp-based GP-6. Let us tell you all about it: Your GP-6 technical bulletin awaits. We're Science Accessories Corporation, 970 Kings Highway West, Southport, CT 06490, (203) 255-1526.

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CIRCLE 33 ON INQUIRY CARD

MULTI BUS MEMORIES
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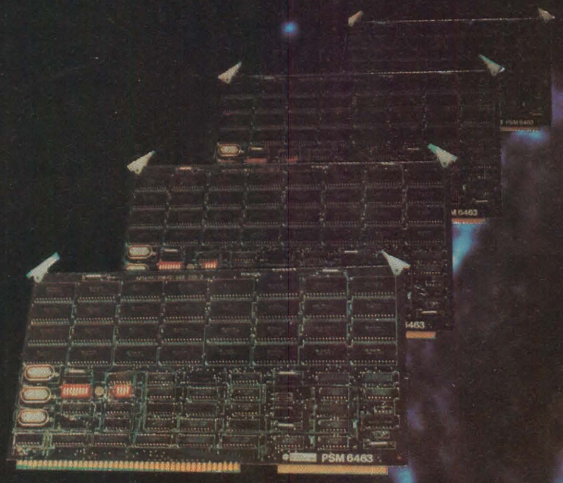

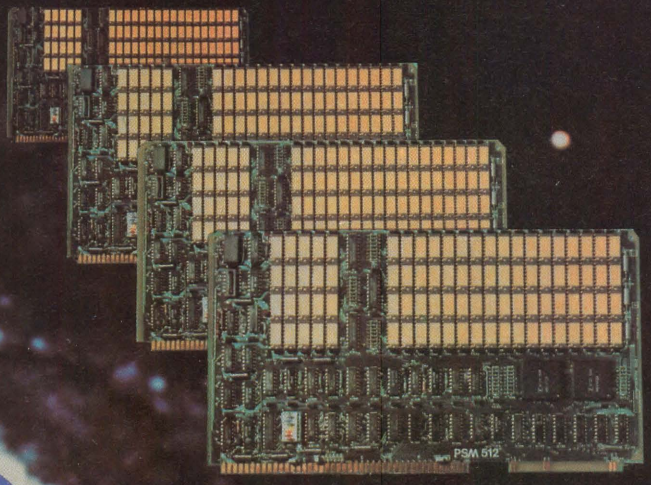

PSM 6463
64K of Non-volatile Static RAM

The combination of CMOS RAMs and high power-density batteries enable us to offer a memory system that doesn't get amnesia when the power fails! The batteries and the charging and changeover circuitry are all on-board and fully automatic. It gives over two weeks of data retention without power. You can even unplug the board and move it to another system without loss of data — it's a carefree memory!
But behind all this is real performance

- *Access and cycle times of 220 nS*
- *Single static operation*
- *8 or 16 bit operation*
- *Single +5 volt operation*
- *Low active power consumption-1.5A max*

With the PSM 6463 many applications can eliminate PROM EPROM and DISK for enormous cost savings. Field update of software is greatly simplified. This is a powerful addition to your system design that will reap benefits for you and your customers!

PSM 512
1/2 MByte of error correcting DRAM

Now the users of 16 bit CPU's need only take up one card slot and one PSU voltage for 512K Bytes. On-board error and correction circuitry extends the MTBF to over 20 years! It's fast too with an access time of 350 nS and a cycle time of 500 nS. For those who really need to get the most out of their 8MHz 16 bit CPU, even faster versions are available. It can support both Byte and word modes of operation plus many other user selectable options and is availabe depopulated to 256K and 128K. 24 bit addressing allows the full 16 Mbyte of the IEEE p796 bus to be used. This is an ideal memory for 86/12 and 68000 systems.

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We have been a highly regarded supplier of computer memories for as long as they have existed. Plessey offers the very best in Quality of design and manufacture. Since we don't make the devices, we are free to choose the best in price, performance, quality and delivery and pass those benefits on to our customers in the form of very competitive prices and a 1 year warranty.

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1641 KAISER AVENUE, IRVINE, CA 92714

*Multibus is an Intel trademark

CIRCLE 34 ON INQUIRY CARD

In addition, the optional trigger trace analyzer can be used with the 8540 to debug 16-bit chips. It can capture real-time execution of code on a prototype's bus, using four independent channels that monitor prototype software execution and logic transactions, along with a high speed acquisition memory for capturing the data. The trace analyzer can be used for software performance analysis, hot spot detection, and interrupt timing.

TNIX, the 8560's OS, is based on Bell Lab's UNIX®. The TNIX hierarchical file system allows programs and directories to be logically grouped into subdirectories. Files are given time/date attributes so that users can easily determine the latest version of a file. Provided that the file owner has not restricted access, the OS allows users to access each other's files. TNIX user passwords, via file access modes, allow files to be either shared or kept private.

With TNIX, the user is allowed to run concurrent tasks. For example, a user may initiate an assembly and a listing, then detach them and immediately begin editing. If the assembly or listing is not immediately needed, the user could lower its priority so it would consume fewer system resources.

A flexible command structure permits effective programming at the expert as well as the novice user level. GUIDE (guided user-interactive development environment), a frontend menu, lets the user concentrate on software design instead of command syntax. GUIDE does not limit the user, however, for the user can modify the menus or can employ standard TNIX commands for more sophisticated operation.

One operation, pipelining, allows commands to be combined and permits the output of one command to act as the input to another. At a higher level of refinement, the OS permits the construction of intelligent command files that can be called by the user and executed as a single unit.

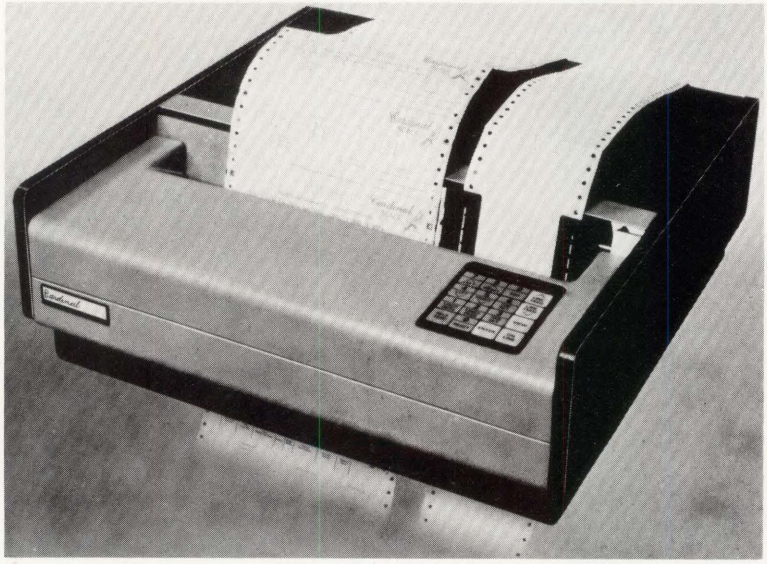
Within files, a number of high level control structures can be employed to automatically supervise the command flow. These include FOR loops to control the number of iterations; CASE statements that present alternative courses of action based on the value of a certain expression; IF...THEN...ELSE statements that permit conditional branching of the command flow; and WHILE loops that execute command sequences as long as a certain condition is present.

The MAKE utility program controls the creation and modification of programs which are made up of many modules. Using a control file that specifies file dependencies, MAKE issues the commands needed to ensure that the end program is correctly made from the current version of the modules. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077.

Circle 249 on Inquiry Card

Cardinal® 2170

High Speed Dot Matrix Data Printer



- O Five paper drive combinations including top or bottom tractor drive and individual forms handler.
- O 200 cps.
- O 9-pin ballistic print head, 650 million character life.
- O Near letter-quality print at 100 cps.
- O Heavy-duty industrial design.
- O Five-input interfaces available.

Cardinal's new 2170 is a rugged performer, tough enough to take anything a factory environment can dish out... yet sophisticated to the point of engineering genius.

Unlike many of today's data printers, the 2170 is available with bottom tractor feed. This enables an operator to remove a form immediately after the last line is printed.

Self diagnostic and signature analysis are built right into the 2170 too. This makes troubleshooting as simple as flipping a switch.

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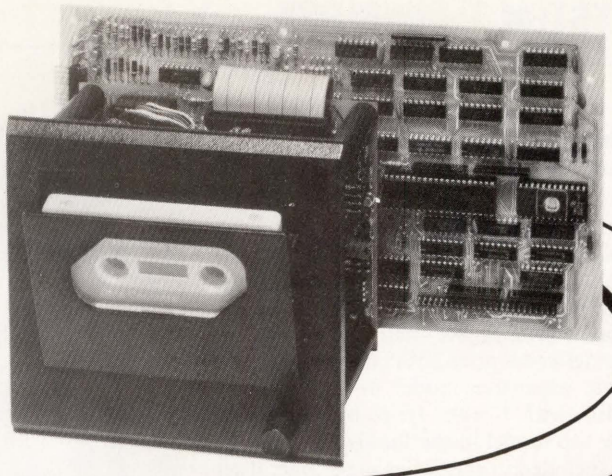
CIRCLE 35 ON INQUIRY CARD

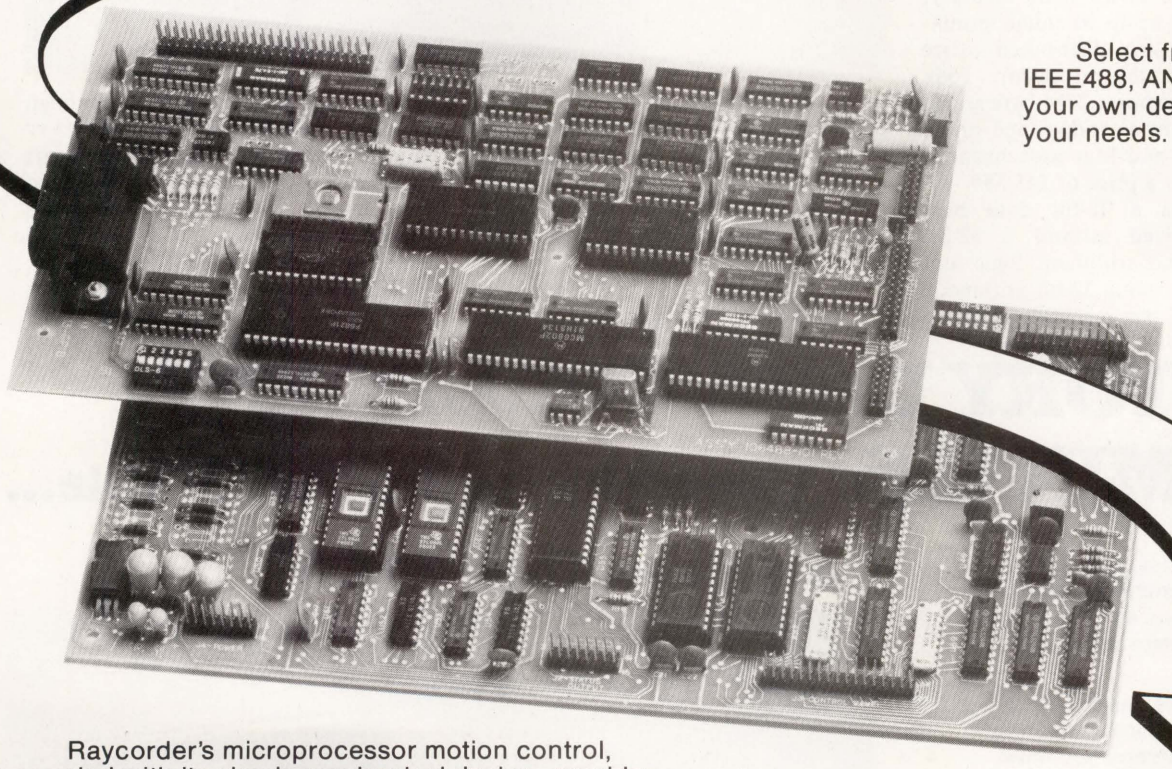
Raycorder II...

the intelligent connection!



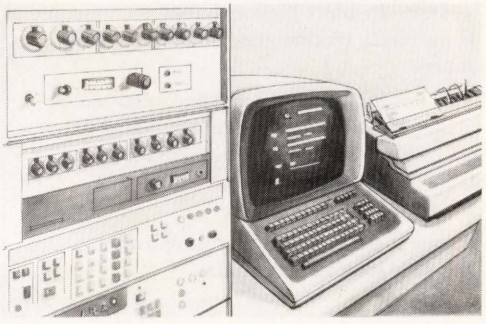
Whether your application calls for an OEM tape drive or an intelligent operating system, Raycorder has the interface you can use.

The Raycorder II Model 6440 offers not only maximum reliability and performance in a low-cost cassette tape drive, but also the versatility and convenience of intelligent controller interfaces.



Select from RS232, IEEE488, ANSI Parallel, or your own design, based on your needs.

Raycorder's microprocessor motion control, coupled with its simple mechanical design, provides such features as constant tape speed and uniform tape tension. Precision head alignment assures cassette interchangeability. Optional features, such as read-after-write and 1600 BPI packing density, make the Raycorder even more versatile.



Features

Versatility
Intelligent interfaces
Maximum reliability and performance
Low price
Constant tape speed
Simple mechanical configuration
Uniform tape tension
Precise head alignment
Ease of loading/unloading cassette

Applications

Process control
Automated test equipment
Data logging
Store and forward
Program loading
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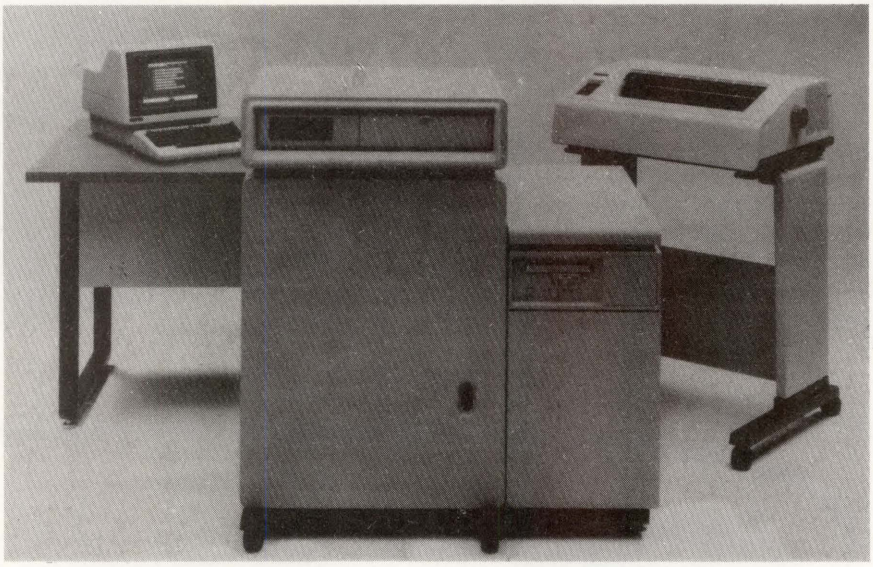
CIRCLE 36 ON INQUIRY CARD

More powerful and lower cost computers introduced



Two new versions of Hewlett-Packard's 3000 general purpose business computer were recently announced. Series 40 is the new entry level computer in the family, with a performance level higher than that of the top model and a price 30% below that of the least expensive model of a year ago. Also, with 1 MIPS, series 64 is currently the top model in the family.

Included in the Series 40 peripheral set are a 27M-byte sealed disk, an integrated cartridge tape drive, and a compact video terminal that can serve as a system console. Moreover, series 40 can be expanded to 2M bytes of main memory, and can support up to 56 online terminals. The Series 40SX distributed office system includes the processor, 256k bytes of main memory, 27M-byte sealed disk with built-in cartridge tape drive, system console, and four asynchronous terminal ports at a price of $45,559.

Series 64 has a 32-bit data bus, memory organized around a 32-bit word, and a dual arithmetic logic unit capable of performing 32-bit arithmetic in a single cycle. Yet it retains compatibility with the other 3000s. Its hierarchical memory system has 8k bytes of high speed cache memory, and 2- to 8M bytes of main memory implemented with 64k RAMs. Effective memory access time is 145 ns, while expansion is in 1M-byte increments.

An advanced terminal processor (ATP) for the 64 provides communications over 4000′ with RS-422 connections. Through its own microprocessors, the ATP reduces system overhead and augments system processing power. When used with RS-232-C connections, terminals operate at speeds up to 9.6k baud with cables up to 50′. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 250 on Inquiry Card

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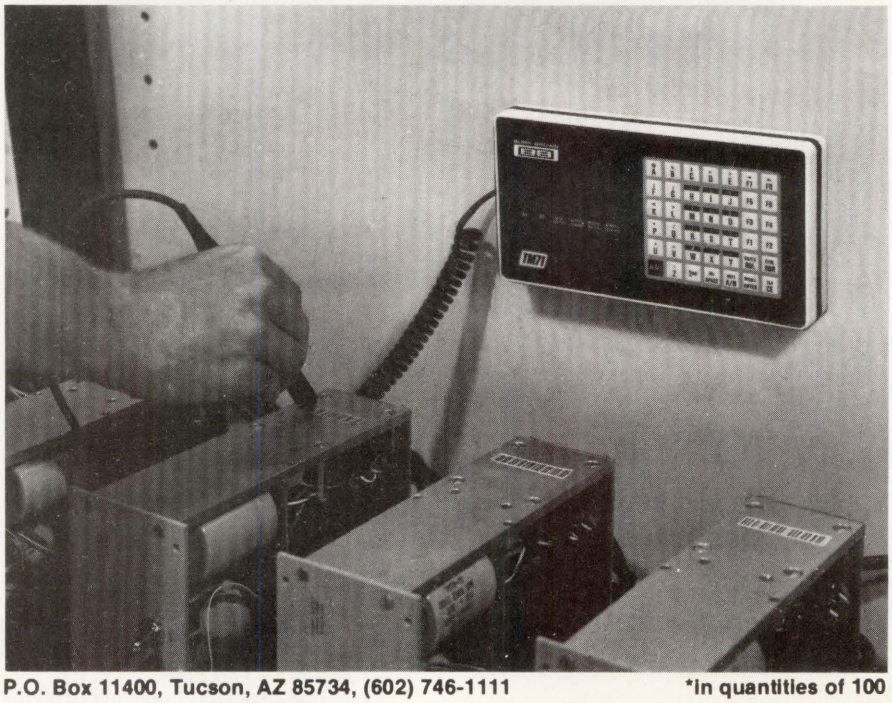

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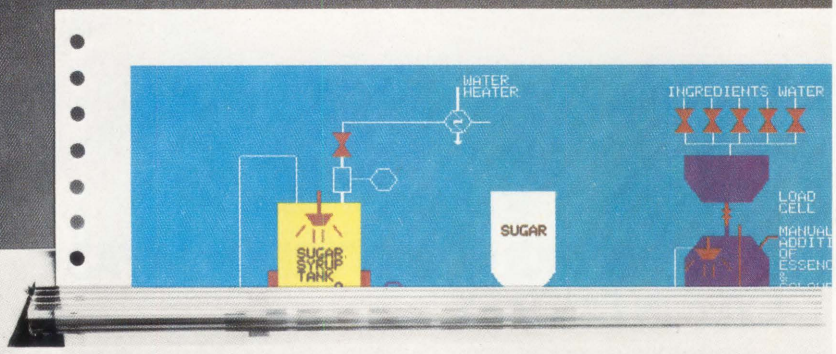

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CIRCLE 39 ON INQUIRY CARD

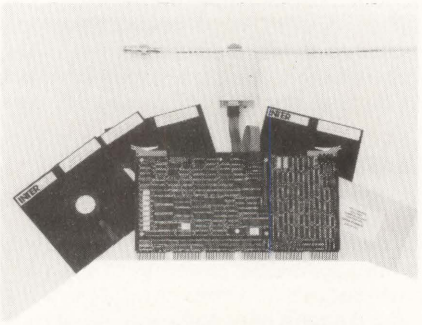
Product family interfaces DEC systems to Ethernet local area network

Two controller boards in conjunction with an Ethernet protocol module allow direct connection of Digital Equipment Corporation's family of VAX-11, UNIBUS based PDP-11, LSI-11, and Q-bus based PDP-11 systems to the Ethernet local area network. The Interlan products perform data link and physical channel functions per the Xerox/Intel/DEC V1.0 specification and allow 10M-bps data communications between stations up to 2500 m apart. Device drivers for DEC RSX-11, RT-11, and VMS operating systems are also provided.

Key to the design approach is the plug-in NM10 Ethernet protocol module. This is combined with appropriate interface boards to produce controllers for specific bus systems. The module has an onboard microcomputer that controls the Ethernet interfaces, manages data buffers, filters multicast addresses, and runs diagnostic checks to verify correct operation of the module.

Implementing Ethernet version V1.0 specifications, the module performs data link layer functions of data encapsulation/decapsulation and CSMA/CD transmit and receive data link management. Physical link functions supported include a 10M-bps data rate, data encoding/decoding, channel access, and transceiver cable interface. Network statistics, such as number of transmissions, receptions, errors, and collisions, are collected.

The module contains a 16k-byte FIFO buffer for back-to-back frame reception and a 2k-byte FIFO for frame transmission. Diagnostics include internal and external data loopback operation, CSMA/CD network state signals, power-up confidence test, and a pass/fail LED indicator.



UNIBUS interface. Products shown include NI1010 UNIBUS Ethernet controller board, software drivers for RSX-11M and RT-11 operating systems, comprehensive diagnostic program, and user manual. Ethernet transceiver model NA1010 is also shown. These products provide complete Ethernet compatibility for DEC UNIBUS based computer systems.

Mounted on a 6.25″ x 10″ x 0.41″ (15.87 x 25 x 1.04-cm) board that fits 0.5″ (1.3-cm) backplane space, the protocol module interfaces to popular 8- and 16-bit microprocessor families by combining with one of Interlan's bus adapter boards and driver software. Two system interface boards are now available to form complete Ethernet controllers for DEC system families: NI1010 for UNIBUS and NI2010 for LSI-11 Q-bus systems.

UNIBUS controller NI1010 occupies one backpanel slot as a standard UNIBUS SPC. It contains all data communications logic needed to interface DEC's family of VAX-11 and UNIBUS based PDP-11 systems to the Ethernet. NI2010 Q-bus controller comes as a quad-height board set that occupies two quad slots on the back panel but represents only one bus load. It interfaces to LSI-11 and PDP-11 Q-bus based systems.

Both controllers have full DMA capability. Onboard buffer memory for transmitting a maximum sized Ethernet packet allows chaining of noncontiguous buffers in user memory to create a single packet. The extensive onboard buffering allows the controllers to be installed on the UNIBUS or LSI-11 Q-bus in a position determined by the anticipated traffic through the controller. It is not necessary to give either unit a high priority position on the bus. Controllers can operate at the full Ethernet data rate with minimum CPU overhead penalty.

NS2010 RSX-11M/S and NS2020 RT-11 V4.0 device drivers are available for both controllers, providing standard DEC RSX and RT driver functions.

In quantities of 25, prices are: NM10 Ethernet protocol module, $1725; NI1010 UNIBUS controller, $2940; and NI2010 Q-bus controller, $2625. Delivery is scheduled for early 1982. The company also provides a complete line of products required to install an Ethernet: transceivers, transceiver cables, Ethernet coaxial cables, and cable terminators. **Interlan, Inc,** 160 Turnpike Rd, Chelmsford, MA 01824.

Circle 251 on Inquiry Card

Melissa Berman, 9 years old is deaf. She studies ballet at the Joffrey Ballet School.

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All systems are available in both U.S. and European versions, with plug-compatible interfaces to most minicomputers (including DEC, Data General and PRIME). Proven system designs ensure reliability, and an expanded FORTRAN library and driver package makes operation easy.

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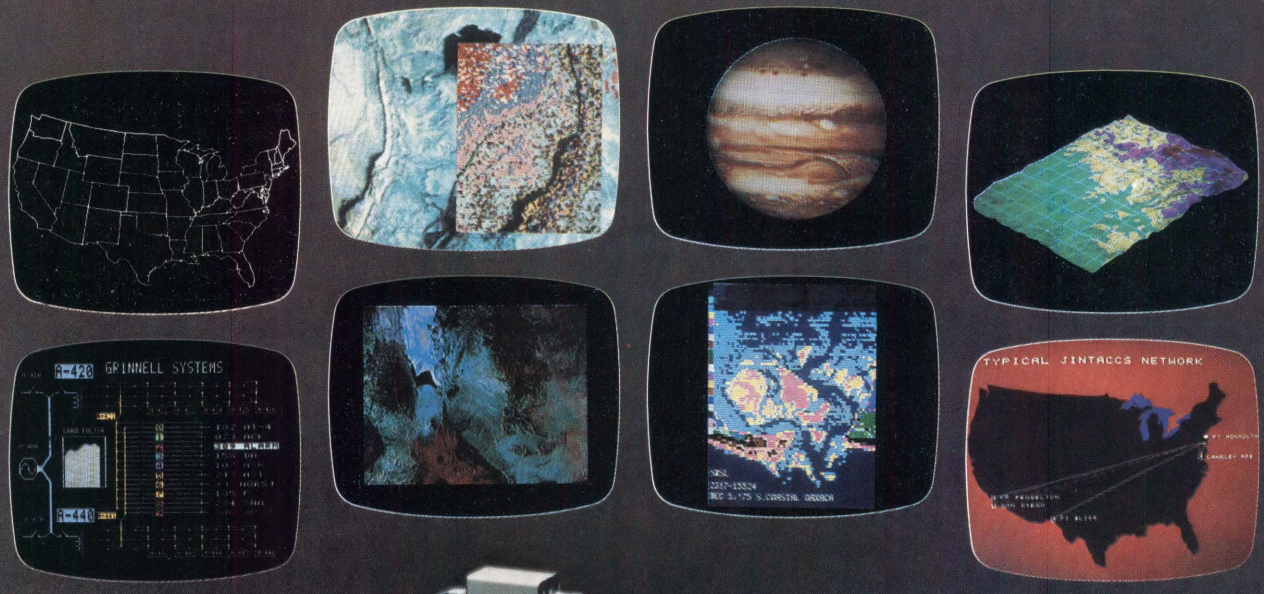

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CIRCLE 40 ON INQUIRY CARD

Ethernet controllers plug into Q-bus and UNIBUS minis

Two controllers provide Ethernet control functions at 10M bps for DEC computers ranging from the LSI-11 to the VAX. 3C200, compatible with the DEC LSI-11 Q-bus, and 3C300, which interfaces with the DEC UNIBUS, are both manufactured by 3Com Corp. Also released to support the products was the enhanced UNET, the company's UNIX based networking software.

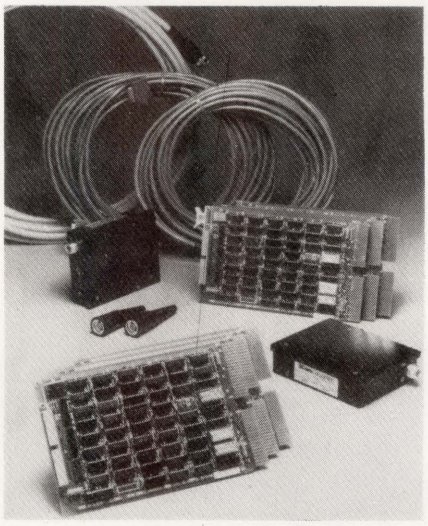
Paired with the company's 3C100 Ethernet transceiver, either of the controllers will support the physical layer (layer one) and data link (layer two) of the International Standards Organization System Interconnection Reference Model. A DEC computer running the UNIX operating system, equipped with the company's enhanced UNET, new controller, and transceiver, can become a complete Ethernet local computer network station. Such a system provides communication through all seven levels of the ISO model, with UNET providing file transfer, virtual terminal, electronic mail transfer, and process to process communication capabilities via the five upper layers.

Both controllers have 32k bytes of dual-ported RAM, permitting the controller and host CPU to access the controller memory space. To support back to back handling of packets at the 10M bps transfer rate, a portion of the memory is used by the controller for send and receive buffers. Memory is allocated in 2k-byte segments, each of which has enough space to store the maximum packet size of 12,144 bits. Since most Ethernet applications require no more than four buffers, much of the memory can be used for storing programs or data. Minimizing move operations, the host CPU can process packets within this memory. Packet processing occurs concurrently with the Ethernet transmission activities of the controller. On a practical level, the user gets an additional 24k bytes of memory along with an Ethernet controller.

Contained on three double-height boards, the 3C200 is plug compatible with DEC Q-bus computers including the LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. For this controller, software drivers are provided for the RT-11 and RSX-11 operating systems, as well as UNET.

DEC UNIBUS computers use the single, hex-sized 3C300 controller, compatible with the PDP-11 UNIBUS machines, including VAX. The company provides software drivers for VMS, RSX-11, and RT-11 operating systems, as well as UNET, for use with the system. 3C300 differs from the 3C200 by providing hardware address recognition.

First-time Ethernet users are encouraged to begin with starter packages that include two controllers, two transceivers, two transceiver cables, one coaxial cable, and two 50-Ω terminators. Each package includes all the hardware to implement a 2-station Ethernet network. (See photo.) Additional controllers, transceivers, and cables can be purchased to build larger operational networks. **3Com Corp**, 1390 Shorebird Way, Mountain View, CA 94043.



3C240 Q-bus Ethernet starter package. Package contains all required hardware for full, 2-station Ethernet based local computer network. Pair of 3-board controllers is designed to plug directly into DEC computer equipped with Q-bus. One of two 3C100 transceivers is connected to each of two controllers. Transceivers are then connected directly to 50-Ω Ethernet coaxial cable.

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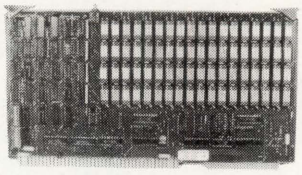

512KB SINGLE BOARD MULTIBUS® MEMORY
First to Offer 512KB on One Board

- Pin-to-pin MULTIBUS compatibility for both 8-bit and 16-bit systems.
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SINGLE QTY. PRICE: 128K x 9 $795. 512K x 9 $1,995.

256KB LSI 11/23® SINGLE DUAL WIDTH BOARD
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- Addressable as a contiguous block in 4K word increments through 4 Mega Bytes.
- On-board parity generator checker.
- Power requirements are +5V 1.2A.
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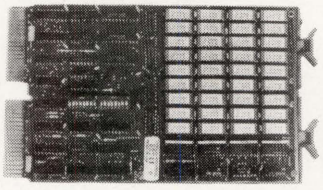

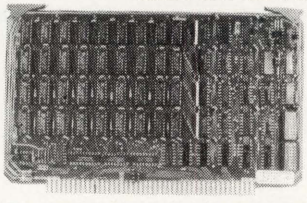

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Single Board Memory.

- Addressable as a contiguous block in 4K word increments with respect to VXA or VUA.
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- Functions with on-board hidden refresh up to 1.5 meghz clock rates.
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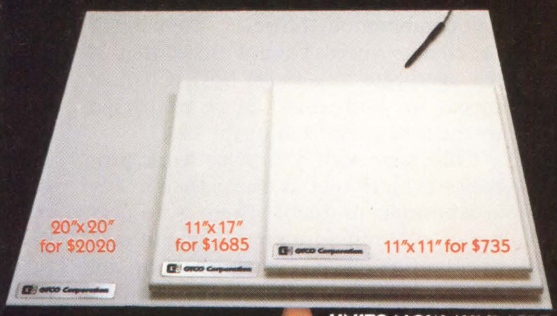
Input Graphic Data With A Digi-Pad

WITH 0.001 INCH RESOLUTION

Just plug one of our new DIGI-PAD 5s™ into your graphic terminal or computer I/O port and you can input precise graphic coordinates without a keyboard or light pen. Use the DIGI-PAD to control a cursor for CRT display analysis... or to enter commands by menu... or to precisely digitize graphic information.

The DIGI-PAD 5 digitizer tablets and stylus or cursor measure and transmit X-Y coordinates with 1 mil resolution over the active tablet area. Coordinates are transmitted at up to 200 X-Y points per second. The DIGI-PAD has an integral microcomputer that computes stylus X-Y coordinate location from GTCO's proprietary electro-magnetic ranging array, built into the tablet's surface. From local or remote commands, the microcomputer also controls data transmission and protocol for compatibility with your terminal or computer. That compatibility allows us to emulate Bit Pad™ and other more expensive or lower performance tablets you may have used before. And due to its manufacturing simplicity, DIGI-PAD 5 costs less... even though it is built for rugged commercial environments.

SIZES UP TO 42"x 60" AVAILABLE



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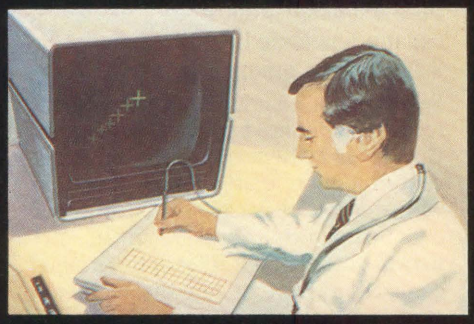
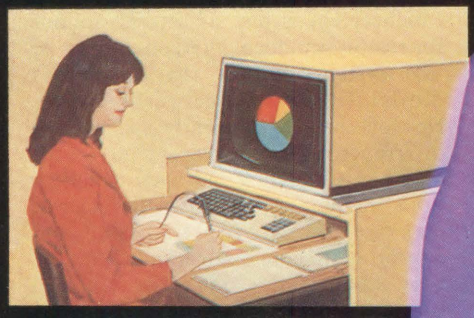
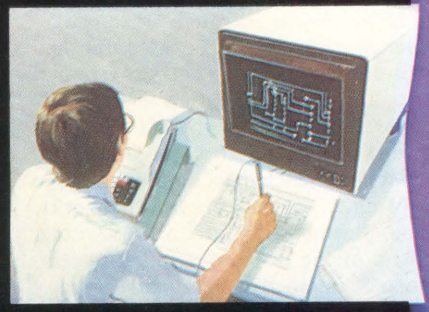
GTCO has pioneered development of a comprehensive range of digitizer products. Our electromagnetic absolute ranging technology was patented in 1975 and has set the standard for our industry. So whether you need a special OEM digitizer, the DIGI-PAD, a larger digitizer, or an interactive digitizing system, call us at (301) 279-9550 and talk with one of our digitizer specialists.

™Bit Pad is a trademark of Summagraphics Corporation.







GTCO Corporation

1055 First Street/Rockville, MD 20850
(301) 279-9550 Telex 898471

CIRCLE 42 ON INQUIRY CARD

Channel option unit allows independent synchronous channels to share one line

Two-channel bit-interleaved synchronous time division multiplexer synchronous channel option (SCO) allows two independent synchronous data streams to share one telephone line. It can be plugged into a free card slot in any DCA network processor. The SCO allows remote synchronous terminals such as IBM 3270s or 3780s to share a single line with multiplexed asynchronous terminals.

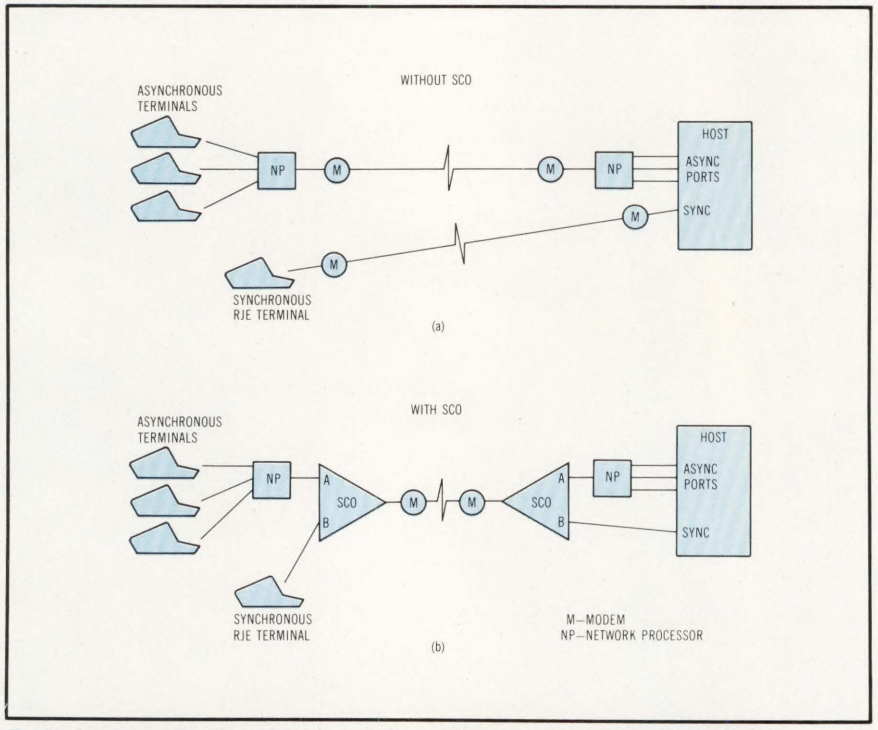
Used in pairs, the SCOs are connected by a full-duplex synchronous data stream (aggregate link). The SCO splits the aggregate data stream, coming from a modem or data coupler, into two secondary streams, channels A and B. These in turn are connected to two independent synchronous devices.

Each SCO unit has a thumbwheel switch that programs the SCO to allocate 100%, 75%, 50%, 25%, or 0% of the aggregate link bandwidth to channel A. The remaining aggregate bandwidth is assigned to channel B. Channel data stream speeds can be programmed to any combination; however, the sum of the channel speeds cannot exceed that of the aggregate link (9600 bps). Channel speeds for both ends can be controlled by the SCO at one end of the link.

Colocated with a DCA network processor (NP), the SCO is transparent to any synchronous protocol. There is no degradation in response time. The unit may operate unattended, or an operator can change speeds or test both channels from one end of the aggregate link without manual intervention at the other.

Bandwidth for channel B stream can also be allocated automatically. In response to a DTR signal from a synchronous terminal, the SCO automatically assigns a portion of the aggregate bandwidth to channel B. When the synchronous terminal goes offline, its previously used bandwidth is reallocated to channel A.

The SCO is accommodated on a 6″ x 9″ (15 x 23-cm) plug-in card and a 2.25″ x 3.5″ (5.72 x 8.9-cm) cable adapter card.



Typical SCO application. In (a), one line and two modems are dedicated for synchronous data stream and one line and two modems are dedicated to multiplexed asynchronous data stream. In (b), SCO pair allow one line and two modems to handle both multiplexed asynchronous and synchronous data streams. Normally connected to DCA equipment, channel A may also connect to other colocated data terminal equipment such as terminal or host computer ports. Channel B is connected to colocated synchronous data terminal equipment.

Frame size is switch-selectable at 1024 or 2048 bits. There are eight synchronizing bits/frame plus command and status bits. A 3-position loopback test switch allows checking of aggregate link status or troubleshooting channel data paths both locally or remotely at either end of the link. Eight LEDs indicate troubleshooting results and two additional indicators show operational status of the system. The SCO is compatible with all DCA units and synchronous data terminal equipment. Both channel and aggregate links have EIA RS-232-C interfaces. Price for each unit is $500, with delivery in 30 days. **DCA**, 303 Technology Park/Atlanta, Norcross, GA 30092.

Circle 253 on Inquiry Card

Data communications capabilities including SNA and X.25 support announced

Several data communications products recently announced by Hewlett-Packard Co include an HP 3000 network communications option that allows connection with CCITT X.25 packet switched public data networks (PDNs), 3000 to SNA network capabilities, fiber optic terminal connections, and an auto dialing intelligent network processor. The X.25 enhancement is one of several options for remote and local interconnections of 3000 systems within the company's distributed systems networks (DSNs). Network services currently available to distributed systems users are now obtained by connecting 3000s with X.25 PDNs including network file access, database access, file transfers, and interprogram communications. With the new X.25 facilities, the 3000s can also support remote, interactive character-mode terminals through the packet switched network. This is accomplished by implementing the CCITT X.29 terminal connection standard within the DSN.

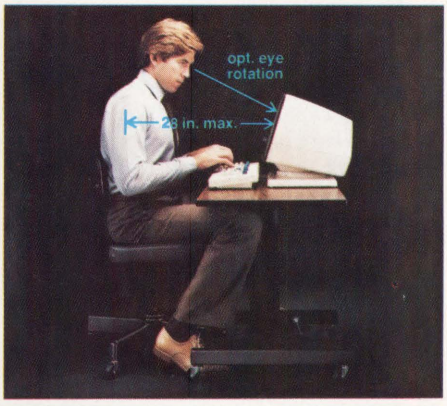
Now compatible with IBM's systems network architecture (SNA), the 3000s can interactively exchange data with large mainframe systems in SNA networks, through emulation of an SNA/SDLC verison of the IBM 3270 terminal system. The DSN/interactive mainframe facility (IMF) emulates IBM's 3270s and provides physical unit type 1 capability.

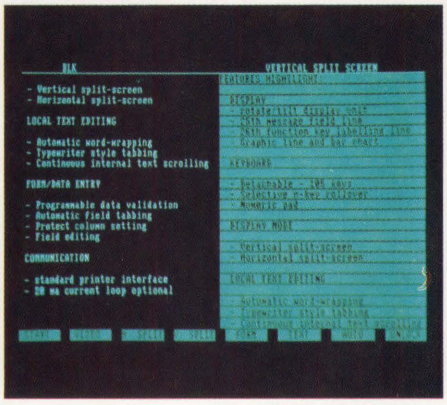
In addition, a new advanced terminal processor for use with the 3000 series 64 computers supports communication

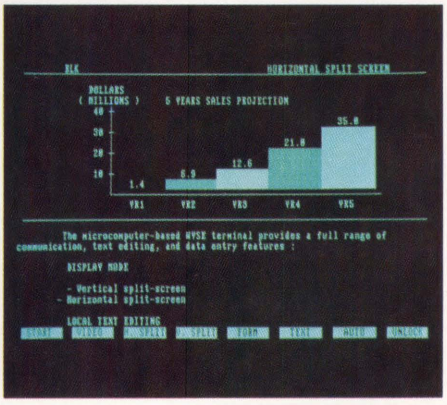
(continued on page 64)

Introducing the $995 Smart Terminal

ERGONOMICALLY ENGINEERED







Ergonomics. The science of designing machines for the humans who must use them. OEM's take note. Because ergonomics is fast becoming the determining factor in end-user selection of smart terminals. End-users are, after all, only human.

Enter the WY-100. The most ergonomically sound smart terminal for an economical price, list $995/unit.

The WY-100 is designed for that unpredictable species, Homo sapiens. Its fully tilting/rotating display and detached keyboard accommodate different working conditions and preferences. The green screen pampers eyes. Horizontal and vertical split screen capabilites with independent scrolling help a person do the impossible, be in two places at once. Why the WY-100 even understands that to err is human, ergo, screen editing and protected fields with data validation.

And there's more. Each WY-100 undergoes 96 hours of rigorous testing. So you can be sure that it will blink, dim, reverse, underscore and blank when you want. Plus you get 128 characters with upper and lower case, line drawing and graphics. And a keyboard with 105 keys including cursor pad, numeric pad, special modes and function keys.

The WY-100 knows that OEM's are human, too. Their needs are often different. So it's customizable. A systems programming manual is available.

Think economical. Think ergonomical. Think Wyse.

For complete specifications and an eye-opening ergonomical comparison chart, circle our reader's service no. or contact Larry Lummis at Wyse headquarters.

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726 Charcot Ave.
San Jose, California 95131
408/946-3075

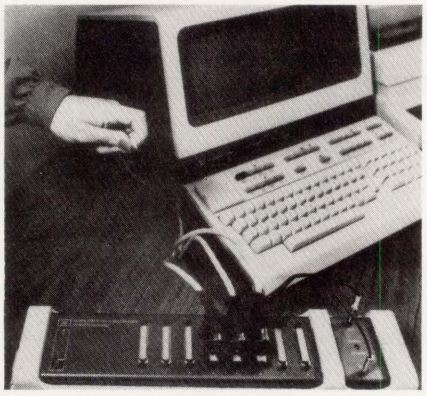
CIRCLE 43 ON INQUIRY CARD

speeds up to 9.6k baud, at distances up to 4000′, through RS-422 connections. When used with RS-232-C connections, terminals operate at speeds up to 9.6k baud with cables up to 50′ long.

An 8-channel fiber optic multiplexer, 39301A was also announced. A pair of these multiplexers, interconnected by the company's fiber optic cable, allows a remote cluster of eight RS-232-C devices to be connected to a computer at distances up to 3280′. Each of the eight full-duplex channels can run asynchronously at rates up to 19.2k baud.

Also unveiled was a new version of the intelligent network processor (INP), which is lower in price and incorporates automatic telephone dialing as a standard capability. The INP serves as the hardware interface between 3000s and multipoint terminals, and between 3000s and mainframe systems.

Finally, the company announced its support of one configuration of the emerging IEEE 802 standard for local area networking. It also defined the direction it will follow in evolving toward open systems. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.



Circle 254 on Inquiry Card

SOFTWARE

Operating system kernel enables realtime microprocessor operation

A realtime multitasking executive kernel for the Z8002™ microprocessor, placed in 4k bytes of PROM, VRTX™ is designed for embedded microprocessors in control and instrumentation environments where processors may have to deal with a wide variety of onboard devices. The OS kernel provides a common core of mechanisms to coordinate multiple tasks in an event-driven realtime system.

VRTX makes no assumptions about its hardware environment other than the presence of a microprocessor and memory. All other functions, including interrupt handling and realtime clock, are handled by 22 system calls to VRTX. Thus, a character I/O call to get a character from a peripheral device would be SC_GETC in the application program. The call would send VRTX to a user written configuration table that would then vector execution to the proper I/O handling routine contained in RAM or ROM.

The main logical unit controlled by VRTX is the task. VRTX has calls to create, delete, suspend, resume, and change the priority of tasks; 256 tasks can compete for system resources at any one time under VRTX. In addition, tasks can create other tasks, change their own priority or priorities of other tasks, and send and receive messages among tasks. Intertask communication in VRTX is accomplished by two task-named commands: SC_POST and SC_PEND; neither predefined mailboxes nor semaphores are needed. Separate stack areas are maintained for each task. VRTX likewise supports static and dynamic allocation of memory with two system calls—SC_GBLOCK and SC_RBLOCK to get and release blocks of memory.

A configuration table connects VRTX and its environment, specifying all parameters for VRTX to access specific devices or areas of memory. The configuration table can be contained in ROM or RAM, and in some allocations can be dynamically loaded with different values in RAM for even greater flexibility. Up to 128 user-defined system calls can be added to VRTX thus making it possible to add device dependent interrupt handlers, as well as such complex logical functions as a file structure. **Hunter & Ready**, 445 Sherman Ave, Palo Alto, CA 94306.

Circle 255 on Inquiry Card

Resident SPICE software system eases implementation of DEC's single-board Falcon microcomputer

A resident software system for Digital Equipment Corp's 16-bit Falcon SBC-11/21 single-board computer, SPICE (stack oriented procedural interactive computing environment) combines an operating system, high level programming language, assembler, file system, and multitasking executive within an integrated ROMable framework. It has been designed specifically for system integration and controller applications.

SPICE encourages top-down design of an application system, with bottom-up implementation. Its interactive nature, based on an incremental compiler, allows rapid development and debugging of software. In contrast to other programming languages, it offers direct access to the machine's resources, making it ideally suited to hardware familiarization and debugging.

By supporting mixed high level and assembler code, the software ensures that critical routines can execute at full processor speed. A multitasking executive simplifies the implementation of complex processes, and includes a variety of tools for intertask communications and synchronization. Even interrupt service routines can be coded directly in the high level language.

DEC's Falcon with SPICE supplies an added level of integration for controller systems by allowing OEMs to use a target system as the development system. Systems can be implemented in a matter of days, rather than weeks or months.

The software is contained in two 2764s and supports both ROMed software for dedicated systems and RAM loaded programs for development and changing environments. Single-user Class A supports starts at $750. **Nortek Inc,** 2432 NW Johnson St, Portland, OR 97210.

Circle 256 on Inquiry Card

Computer aided design/analysis programs run on minicomputers

Developed for DEC/VAX and PRIME minicomputer systems, computer aided design and analysis packages provide mainframe functions on small systems. SUPER*SCEPTRE significantly advances the original automatic analysis program. I-G SPICE, a special interactive graphics version of SPICE2, retains all capabilities while adding flexibility, online speed, and convenience.

Capable of determining initial conditions, transient, and steady-state responses of linear, nonlinear, or digital networks, SUPER*SCEPTRE uses a free-format engineering oriented language. Its defined parameter mode allows direct solution of state equations written to describe any type of system. Additions include an implicit integration routine for faster solutions of "stiff" systems, ability to perform ac (frequency domain) analysis, and sensitivity, optimization, worst case, and Monte Carlo analysis dc options. The preprocessor adds capabilities to analyze not only electronic circuits, but also mechanical systems, logic, transfer functions, and interdisciplinary problems. The program automatically reacts with user provided FORTRAN subprograms.

I-G SPICE supplies ac (frequency domain) analysis, transient (time

(continued on page 66)

MACSYM 10.

The first 16-bit stand-alone minicomputer designed for harsh industrial environments.

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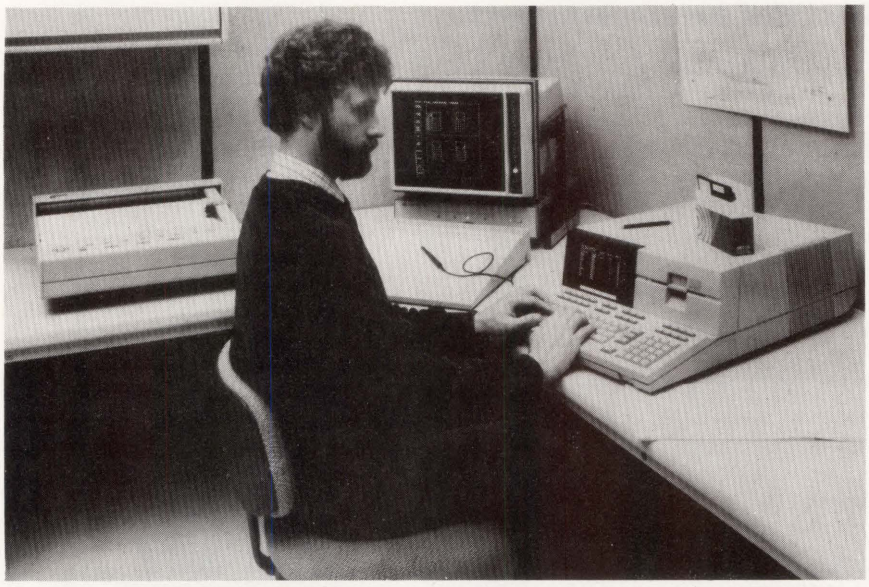
domain) analysis, dc, noise, sensitivity, driving point impedance, Fourier, temperature, distortion, transfer characteristics, and transmission line analysis. It allows users to easily change any or all of the circuit or solid state model parameters of a given circuit and to quickly see the modified output curve on the graphics display, making comparison of various responses for tolerances or changes straightforward.

The solid state model library provided with the program contains SPICE compatible computer models for bipolar, JFET, MOSFET, PWRFET, diodes, Zeners, SCRs, and macro models for FET and bipolar IC op amps. Graphics package is designed for the HP2648A, Tektronix 401X series, or other compatible graphics terminals. **AB Associates**, 1348 Eckles Dr, Tampa, FL 33612.

Circle 257 on Inquiry Card



Based on HP 9826A desktop computer, interactive graphics system from Hewlett-Packard uses graphics tablet as primary input device and provides Pascal procedures for easy application development.

PERIPHERALS

Interactive graphics system supplies Pascal procedures for application development

Created for the single-user design graphics area, the 1360 Graphics System, a low cost, high performance, interactive graphics station, supports plotter/printers for hardcopy and mass storage devices for program development. The system offers users realtime interactivity with the display through the graphics tablet or other supported input devices, such as digitizers.

A 9826A desktop computer, 1351A graphics generator, 1311B large screen display, 9111A graphics tablet, InteGraL/60 interactive graphics library, and necessary connecting cables make up the system. Serving as the computational element and system controller, the desktop computer, under direction of the graphics library, controls all major system functions such as I/O, calculations, and information storage.

The graphics generator receives picture data from the computer through a 16-bit parallel interface, stores it in its internal memory, and displays it on the CRT. It refreshes the display from memory, keeping current picture data on screen until it is modified or erased. When the picture is changed and instruction given to redisplay, the new picture is stored in the generator's memory and displayed on the screen. The unit also displays data with different intensities and blinking on command.

The graphics tablet is the human/computer interface for the system. It enables users to interactively draw lines, pick elements for editing, and position text on the CRT display. These functions are implemented by the computer and graphics generator to provide realtime interaction with the CRT.

InteGraL/60 model 52113A is composed of a set of 81 Pascal procedures that can be divided into three basic segments: device handling, graphics functions, and data base. The device handling portion takes care of I/O functions associated with I/O devices. This frees the applications programmer from the responsibility of writing code to deal with specifics of each particular device. Programmers can define objects in terms of a logical device that is device independent. To output graphic objects to a specified device, the object is redefined in terms of an actual physical device.

The graphics functions portion of the library provides the programmer with high level building blocks for constructing an interactive graphics application program. From these, objects can be created for mechanical drawings, schematics, printed circuit board artwork, and other specialized applications. The system supports several fonts with user specified size and spacing, depending on the plotter used. Procedures control orientation, direction, justification, and slant of text. Editing features permit users to modify any object previously created. All aspects of appearance and style of basic elements can be changed, inserted, or deleted after creation.

The third, data base, part is a collection of objects or subobjects that can be moved, displayed, or otherwise acted on. Each primitive in the data base is stored with specific output attributes like contrast, line style, polygon style, text style, slant, text size, spacing, rotation, and justification. Each object is stored in device independent fashion.

The 1360 graphics system with 9826A desktop computer is a user's system. For program development, the system is configured with a 9836A with 12″ screen and two 264k-byte flexible drives instead of the 9826A. Price for the 1360S is $14,750. The 9826A option 715 sells for $13,450; the 9836A option 715 for $16,450. Graphics tablet 9111A has a tag of $2050. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 258 on Inquiry Card

Controller allows ten users to share disk resources

A multi-user file management system, developed by Tektronix, allows shared access to large capacity mass storage by up to ten series 4050 desktop computers. The 4909 file management system, available in either 32M- or 96M-byte versions provides backup and information portability by incorporating a 16M-byte disk cartridge. In addition, up to eight drives can be supported by the 4909 controller

(continued on page 68)

Made in USA

Aydin Patriot™ Color Monitors

Aydin Controls introduces its American-made, in-line gun, high resolution Patriot Series of Color Monitors.

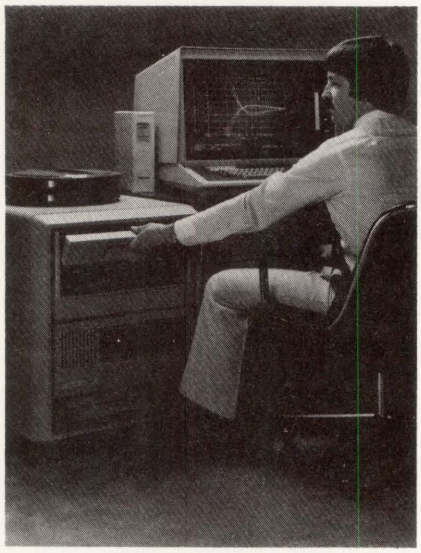
Aydin Controls, a leader in high resolution color display terminals, now manufactures Patriot™, its own in-line gun series of color monitors. The Patriot series will supplement Aydin's well known family of delta and in-line gun monitors.

Patriot's 13-inch Model 8810 and 19-inch Model 8830 both offer the latest state-of-the-art features plus all of the advantages of American technology and manufacturing. Patriot features high video bandwidth, wide horizontal line rates, fixed convergence, excellent high voltage regulation, modular construction, analog or TTL inputs and rack mountability. The Patriot Series can be customized to fit special needs.

Patriot monitors provide outstanding performance at an attractive price coupled with an 18-month OEM warranty; off-the-shelf availability; quick delivery of spare parts; and fast, reliable service. For more information contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel: 215-542-7800 (TWX 510-661-0518).

AYDIN CONTROLS

CIRCLE 45 ON INQUIRY CARD



for a maximum of 768M bytes of local storage.

Expansion of the system is accomplished using eleven plug-in slots that can support either eight disk drives or desktop computer/terminal interfaces, depending on requirements. Interfaces use the IEEE-488 GPIB standard in conjunction with a mass storage ROM pack to interface to the 4050 series desktop computers. Since access to the 4909 is via English commands over the GPIB, various types of computers and controllers using the GPIB can also be attached to the system.

The 4909 incorporates, in addition to shared access, certain intelligent file management features designed to offload routine tasks from desktop computers using the system, including private and public workspaces. Private workspaces can be accessed only by a user-defined password and access code, while public workspaces contain files accessible by all users of the system. Workspaces can be allocated to fit the needs of system users.

Other features that ensure flexibility in system configuration are indexed files with variable length records and dynamic file allocation, and volume concatenation. Indexed file capability allows quick file retrieval for database systems development. Concatenated volumes make expansion easier by permitting multiple drives to appear as one, thus allowing a file to expand to the physical limits of the totally configured system. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077.

Circle 259 on Inquiry Card

Graphics preprocessor provides intelligent input

Designed for preprocessing of graphic information, the DIGIKON system combines a choice of accurate graphics measuring tablets with firmware program modules for geometric analysis in any coordinate system. DIGIKON consists of a tablet with resolution of 0.025 mm in a range of sizes from 28 x 28 cm to 100 x 150 cm; cursor and stylus; measurement and evaluation electronics package; and keyboard with display.

Digitization of X-Y coordinates, the basic function of the DIGIKON, can be done in either point or continuous (streaming) mode. In continuous mode, coordinates can be set according to time and distance; this mode can use a "manual close" option which will assume straight lines between points where the continuous trace of the stylus has been interrupted. The coordinates, once measured, can be either displayed on the DIGIKON keyboard or sent directly to the host computer. Coordinates can also be subjected to preprocessing by six firmware modules currently available for the system. One module performs scaling and transformation of linear coordinates by tapping one to four points on the tablet; scaling can be done either by tapping two points or by keyboard entry. It is thus possible to easily compensate for slight skewing of paper on the tablet. The coordinate transformation module allows transformation between Cartesian and polar coordinates; conversion to curved line coordinates; conversion of logarithmic to linear coordinates; and conversion of Gauss-Kruger coordinates.

Other firmware modules include a programmable measuring raster for definition of a variable raster with selectable equidistant intervals in X and Y directions, and for output of coordinates according to raster points. A module for geometric length and area measurements in either point or continuous mode, and a module for diagram evaluation including integration of curves, height and base-width of a curve line, slope, and radius of curvature are also featured. **Kontron Electronic, Inc**, 630 Price Ave, Redwood City, CA 94063.

Circle 260 on Inquiry Card

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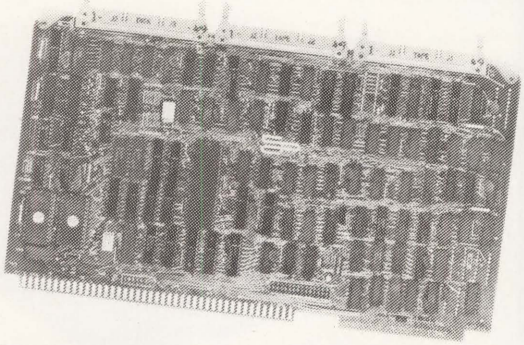
1/4 INCH MAG TAPE



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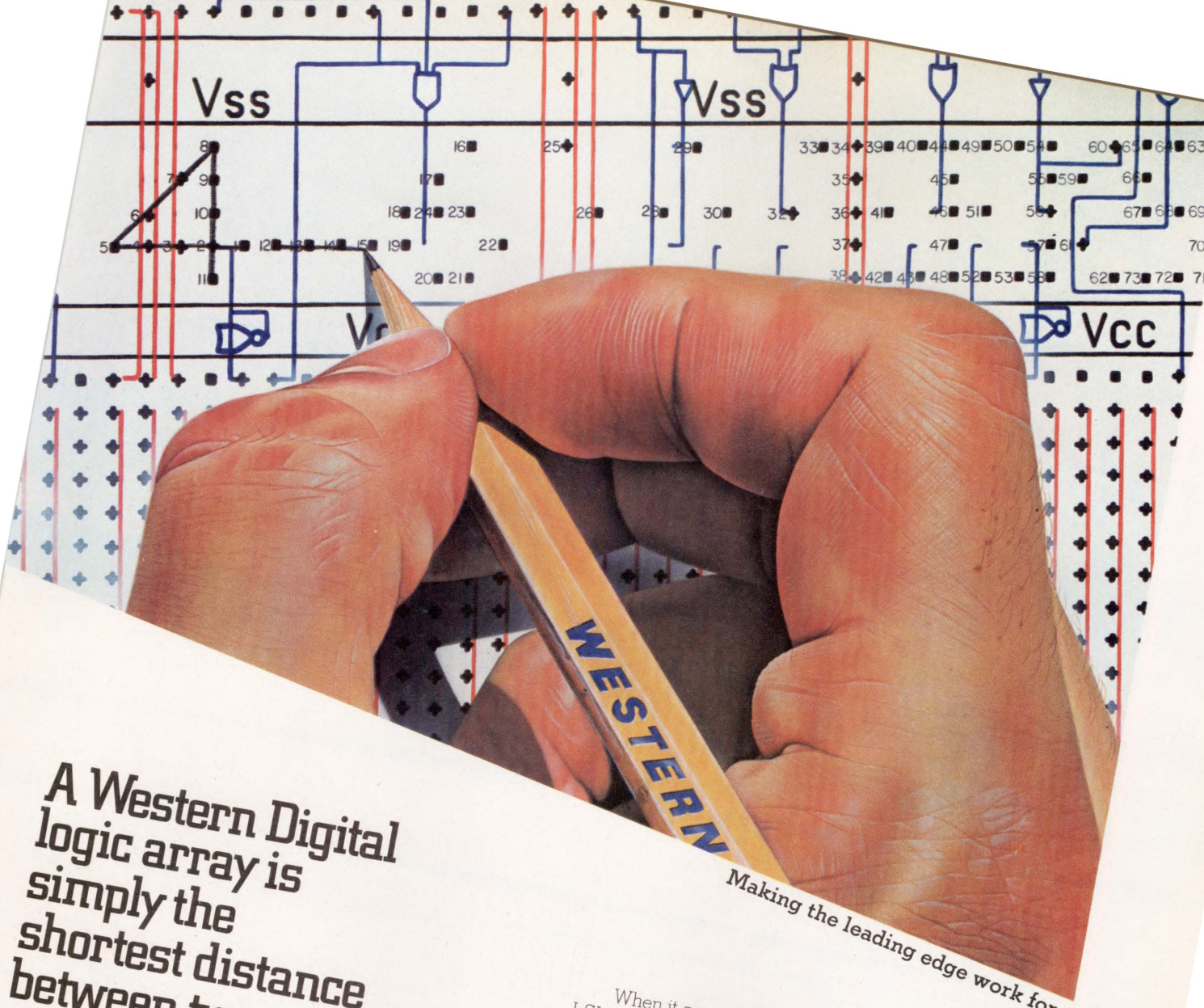

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CIRCLE 48 ON INQUIRY CARD

Manufacturing/quality control procedures combine to produce interchangeable diskettes

As floppy disk drives increase in density, needs for higher precision and greater accuracy in the media and its housing become more demanding. Extreme precision and superior performance in electromagnetic properties, physical properties, and dimensional accuracy combine to insure reliability, accuracy, dependability, universal compatibility, and long term performance with no deterioration.

To fulfill these requirements, Maxell Corp has imposed a complex series of manufacturing standards that mandate stringent production tolerances. Ensuring complete compliance with standards by carrying out extensive testing and inspection procedures, Maxell designates these products "Gold Standard" to call attention to the quality control. Among the steps taken to guarantee product quality is limiting deviation from normal industry standards (such as ANSI, Shugart, and IBM) to much tighter tolerances. Thickness, deformity, or the potential for deformity are checked piece by piece. As a result, diskettes are within tighter physical tolerances than published standards.

A specially developed, extremely stable, computer grade gamma hematite magnetic powder is used to ensure uniformity, consistency, and compatibility with a variety of disk drives. Coating thickness is maintained at an extremely uniform 2.5 μm and 0.2 μm.

A proprietary binder system results in durability. Samples are continually tested through an accelerated life test of 10M passes. Products using the binder system show no sign of deterioration, drop outs, abrasion, or distortion throughout the test. A special lubricant maintains the friction factor at the lowest possible level. Reduced friction reduces wear and provides stable output for a longer time.

All diskettes are manufactured in a dust-free, temperature and humidity controlled, clean room environment. All disks and all tracks are certified. Zero defects are guaranteed. Available "Gold Standard" products include double-density/double-track diskettes, and 10-hole hard sector and soft sector single- and double-sided minidiskettes. **Maxell Corp of America**, 60 Oxford Dr, Moonachie, NJ 07074.

Circle 261 on Inquiry Card

INTEGRATED CIRCUITS

1024 x 8 PROM well suited for pipelining

The Am27S35 PROM has been designed to reduce the cost and size of systems that temporarily store PROM data in a register. Well suited for pipelined microprogrammed systems, this device from Advanced Micro Devices, Inc, has 8-bit onchip edge triggered registers (Fig 1). The 1024-word by 8-bit part also provides synchronous and asynchronous output enables for simplified word expansion. Address setup is 35 ns and the clock to output is 20 ns.

The Am27S35 has an asynchronous initialize ($\overline{\text{INIT}}$) input. This function, useful during power-up time-out sequences, is common to all registers and is a programmable word which may be set into the output registers under single pin control. $\overline{\text{INIT}}$ may be programmed to any 8-bit word from 00_{16} ($\overline{\text{CLEAR}}$) to FF_{16} ($\overline{\text{PRESET}}$).

When V_{CC} is applied, the synchronous enable ($\overline{E}_S$) flipflop will be in the set condition causing the outputs, Q_0 to Q_7, to be in the OFF or high impedance state. Reading data is accomplished by first applying the binary word address to the address inputs, A_0 to A_9, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data are accessed and loaded into the master flipflops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW to HIGH transition of the clock, data are transferred to the slave flipflops, which drive the output buffers. Providing the asyncronous enable $\overline{E}$ is also LOW, stored data will appear on the outputs, Q_0 to Q_7. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. Outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level.

The onchip edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing race conditions. Other register timing requirements are similar to those of standard Schottky registers.

Manufactured with a conductive platinum-silicide link at each bit location, the output of the memory with the link in

(continued on page 74)

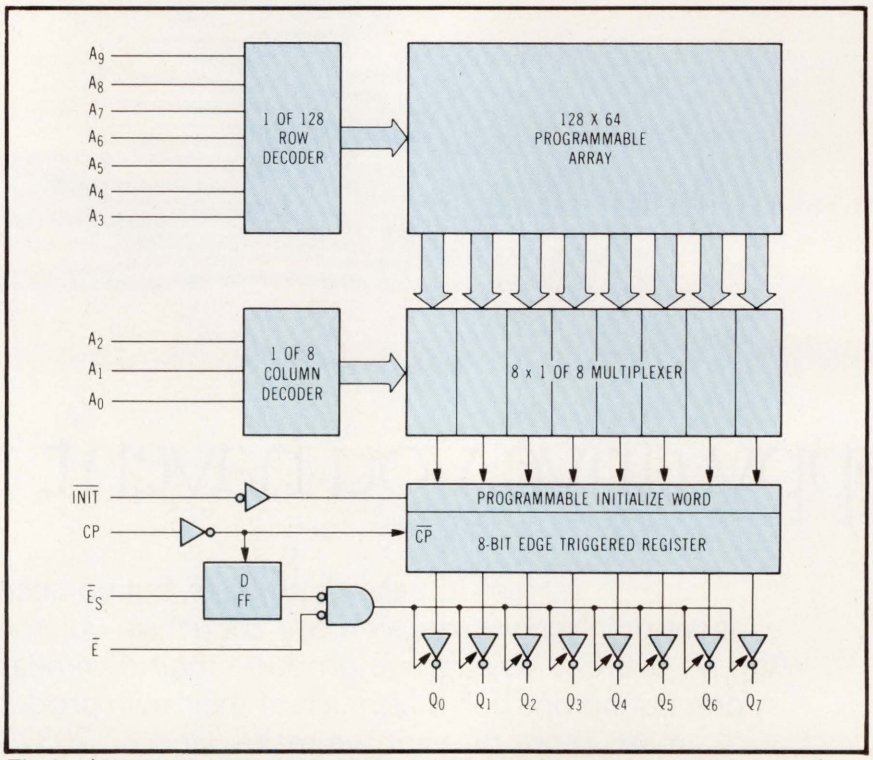

Fig 1 Am27S35 block diagram. PROM provides onchip registers making it well suited for pipelined systems. Asynchronous $\overline{\text{INIT}}$ input is programmable. Word may be set into output registers under single pin control.

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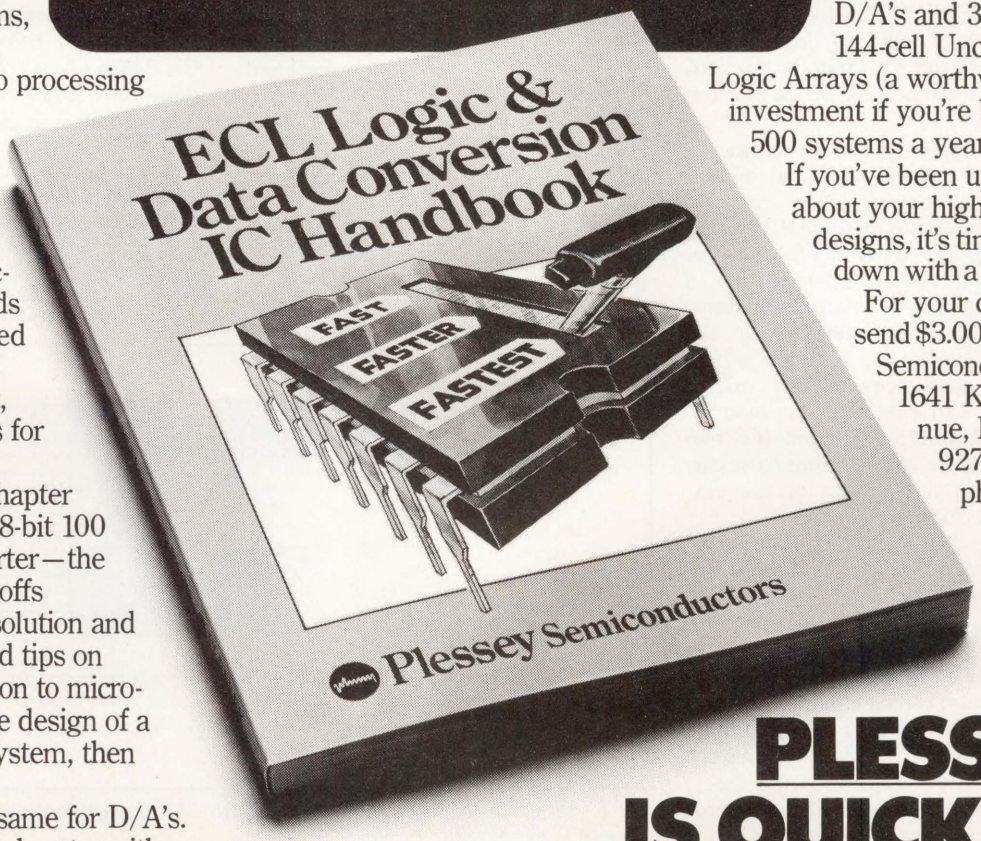

PLESSEY IS QUICKER.

CIRCLE 49 ON INQUIRY CARD

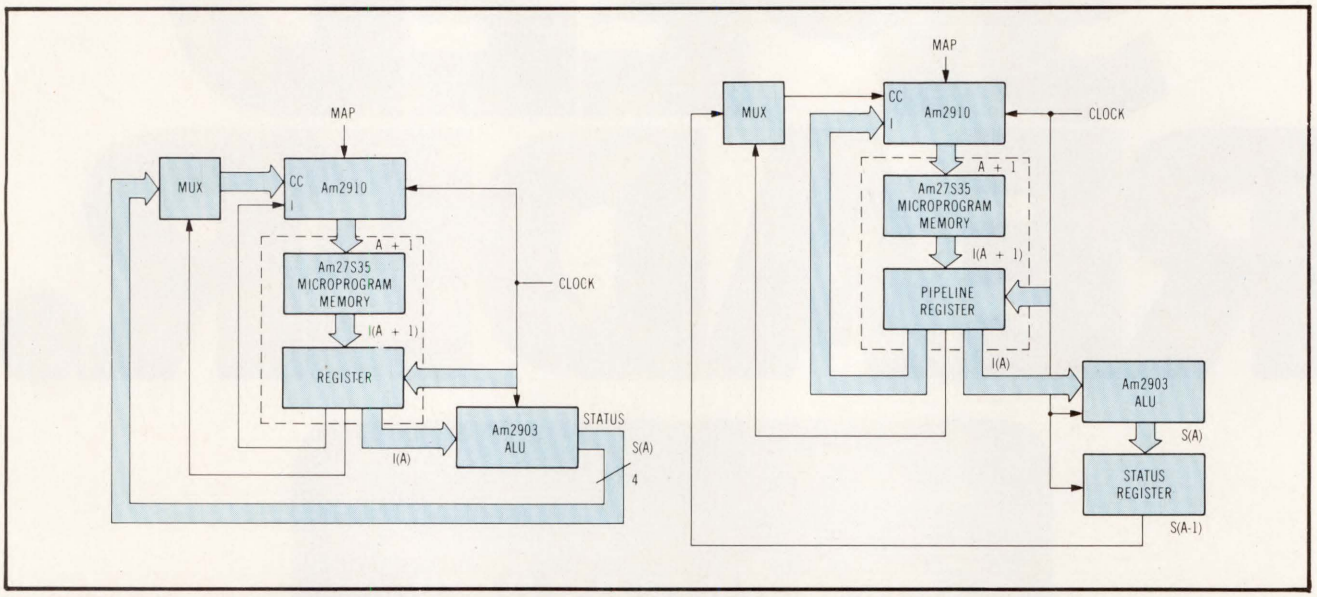

Fig 2 Pipelining example using Am27S35 microprogram memory. Register at microprogram memory output contains microinstruction being executed. Microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as ALU operation. One level pipeline provides better speed than architecture on left. Microprogram memory and Am2903 array are in parallel speed paths instead of in series.

place is LOW. The fusible links are opened one at a time by passing current through them from a 20-V supply, which is applied to the memory output after the $\overline{E}$ input and $\overline{INIT}$ input are at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 V. After 50 μs, the 20-V supply is removed, the chip is enabled, and the CP input is clocked. The part is implemented in a 24-pin slim cerDIP.

When applied with the company's 4-bit microprocessor slices and bipolar microprogram sequencer, the registered PROM can be used to upgrade the performance of existing systems. These devices are designed to be operated by a coherent sequence of microinstructions, termed "microprogramming" by the company. (See Fig 2.) In the case of a computer, each sequence of microinstructions can execute a machine instruction. A microinstruction has two parts; the elemental operations to be carried out, and the address of the next microinstruction to be executed.

Usually included in the definition of the micro-operations to be carried out are ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are distinguished from non-microprogrammed machines. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flipflops, connected in a somewhat random fashion, in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are more highly ordered, particularly with regard to the control function field, and use high speed PROMs for control definition. Most simply defined, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction. **Advanced Micro Devices, Inc**, 901 Thompson Pl, PO Box 453, Sunnyvale, CA 94086.

Circle 262 on Inquiry Card

64 x 4 and 64 x 5 FIFOs guarantee 15-MHz shift out rate

Two first in, first out (FIFO) memories from Monolithic Memories are well suited for digital signal processing applications and as low cost buffers in high speed minicomputers and peripherals. The 67401A and the 67402A are organized as 64 words x 4 bits and 64 words x 5 bits, respectively. Data can be written

(continued on page 76)

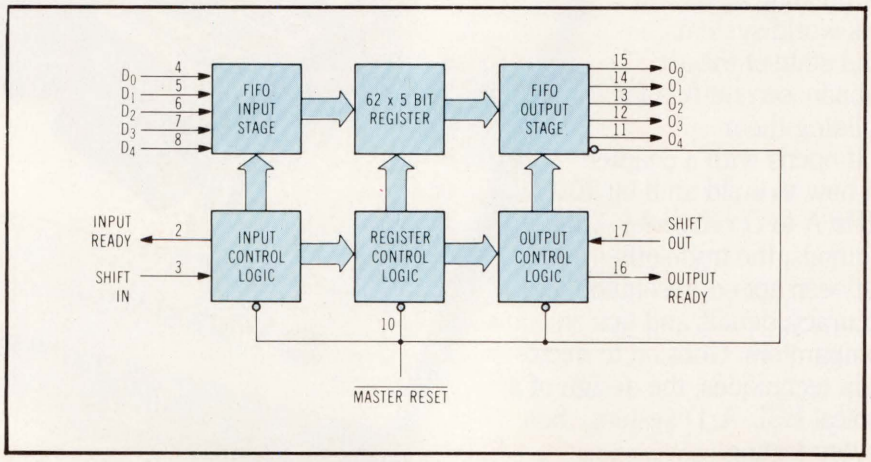

Fig 1 Block diagram of 67402A FIFO. With 64 x 5 organization, device has extra bit and is expandable in word dimension.

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CD1/82

CIRCLE 50 ON INQUIRY CARD

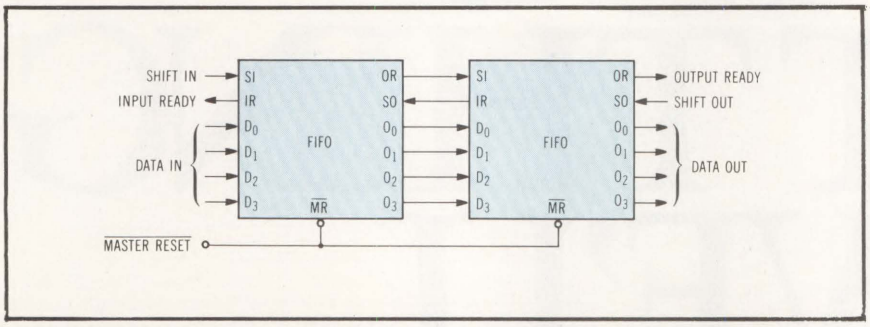


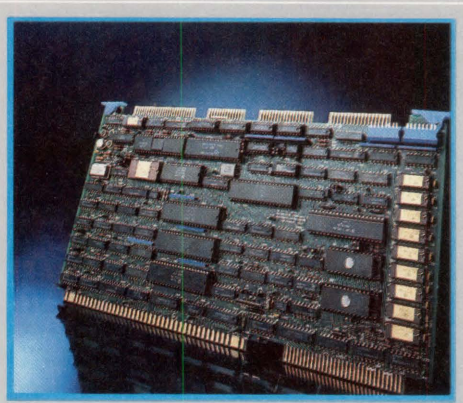
Fig 2 Cascading FIFOs form 128 x 4 FIFO. FIFOs can be cascaded to any desired depth. Handshaking and associated timing between FIFOs are handled by FIFOs themselves.

into the FIFOs at one rate and read out in the same sequence at a different rate. As long as the FIFO memory is not full, writing and reading are independent operations. Both FIFOs guarantee a data rate of 50 MHz. The 67402A provides four bits plus one bit for parity checking or end of frame marking (Fig 1). This enables designers to use two FIFOs to build a 9-bit (8 bit plus parity) system instead of three FIFOs.

If the user wishes to increase memory capacity, 67401A and 67402A FIFOs designated by the letter C can be expanded in both word and bit dimensions. These devices, C67401A and C67402A, can be connected serially (cascaded) to form a memory of 128 words or more, or they can be connected in parallel to form word widths of 8 bits or more (Fig 2). Devices all have TTL inputs and outputs, with input pins located directly opposite corresponding output pins. Series is capable of asynchronous operation. 67401A is housed in a 16-pin, 300 mil wide ceramic DIP, while 67402A is housed in an 18-pin ceramic DIP. All are available in commercial (5V ±5%, 0 to 70 °C) as well as military (5V ±10%, −55 to 125 °C) versions. **Monolithic Memories, Inc**, 1165 E Arques Ave, Sunnyvale, CA 94086.

Circle 263 on Inquiry Card

MAKE IT EASY



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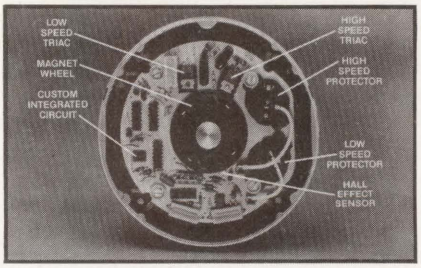
SYSTEM ELEMENTS

Solid state digital switch leads to high reliability motor

A UL recognized digital solid state switch, the result of 3 years research by Gould's Electric Motor Division, makes an electric motor a smart motor. Operating life and resulting reliability are essentially infinite, thereby eliminating a major cause of motor failure. Use of the switch eliminates the nearly 27% of motor failures that are traceable to the switch or governor.

The solid state switch uses a custom IC and contains more than 1200 transistors on a 0.084″ x 0.082″ (0.213 x 0.208 cm) silicon chip. The switch is either on or off; there is no indecision or stuttering. Unlike mechanical devices, with nine moving parts to wear out, the switch consists of a circuit board and a magnetic wheel. Its operation is based on true motor speed.



Solid state switch has been adapted to 1- and 2-speed motor (shown) design. Based on a custom integrated circuit and speed sensing technology, Gould's switch can eliminate 27% of motor failures traceable to switch or governor.

Motors equipped with the switch will be of particular value to users faced with environmentally difficult locales—places where mechanical switches are threatened by dust, dirt, salt spray, water, or other potentially harmful materials. Applications where the motor is frequently started, or where long acceleration times are encountered, such as machine tool and computer disk drive applications, are ideal candidates for the design. Motors equipped with the switch will be delivered on a first-come, first-serve basis in 1982. **Gould Inc, Electric Motor Div**, 1831 Chestnut St, St Louis, MO 63166.

Circle 264 on Inquiry Card

CIRCLE 51 ON INQUIRY CARD

For Higher Reliability, Try Doing Things The "Hard Way."

VRC MODEL 8520... 8" CARTRIDGE DRIVE WITH 22.1 MEGABYTES OF DATA CAPACITY

Performance and reliability are the key features of the Model 8520. A standard ANSI 8-inch removable cartridge stores 11 megabytes of data with track-to-track access time of 14 msec. On the same spindle, in a one-over-one configuration, a fixed disk doubles the capacity to 22 megabytes. All within a compact 7" x 15" x 8½" cabinet. Cross-copying between disks makes it easy and economical to create back-up files. More important for communications, process control, or any application requiring a memory device of the highest reliability, the 8520 is resistant to thermal and physical shock.

The Model 8520 has a MTBF of 8,000 hours and a service life of 30,000 power-on hours, in a temperature range of 0° to 45°C. A proprietary microprocessor-controlled servo positioning technique provides high tolerance to shock, low seek error rate and high data reliability. Unlike conventional Winchester drives, the 8520 features non-contact start/stop heads that never ride on the media during startup or stop or shipping. Heads are positioned by a high performance linear actuator to take advantage of the embedded servo. And a closed loop air filtration system uses the disk as a centrifugal pump to enhance overall reliability and eliminate contamination. The 8520 has an ANSI interface as standard, and other interfaces are available.

For more information, call or write:
Vermont Research Corporation,
Precision Park, North Springfield,
VT 05150. Tel: 802/886-2256.
TWX: 710/363-6533.

In Europe call or write:
Vermont Research Ltd.
Cleeve Road, Leatherhead,
Surrey, England
Tel: Leatherhead 76221
TLX: 23280

- 22.1 Megabytes of Data Capacity
- Non-Contact Heads
- Resistant to Thermal and Physical Shock

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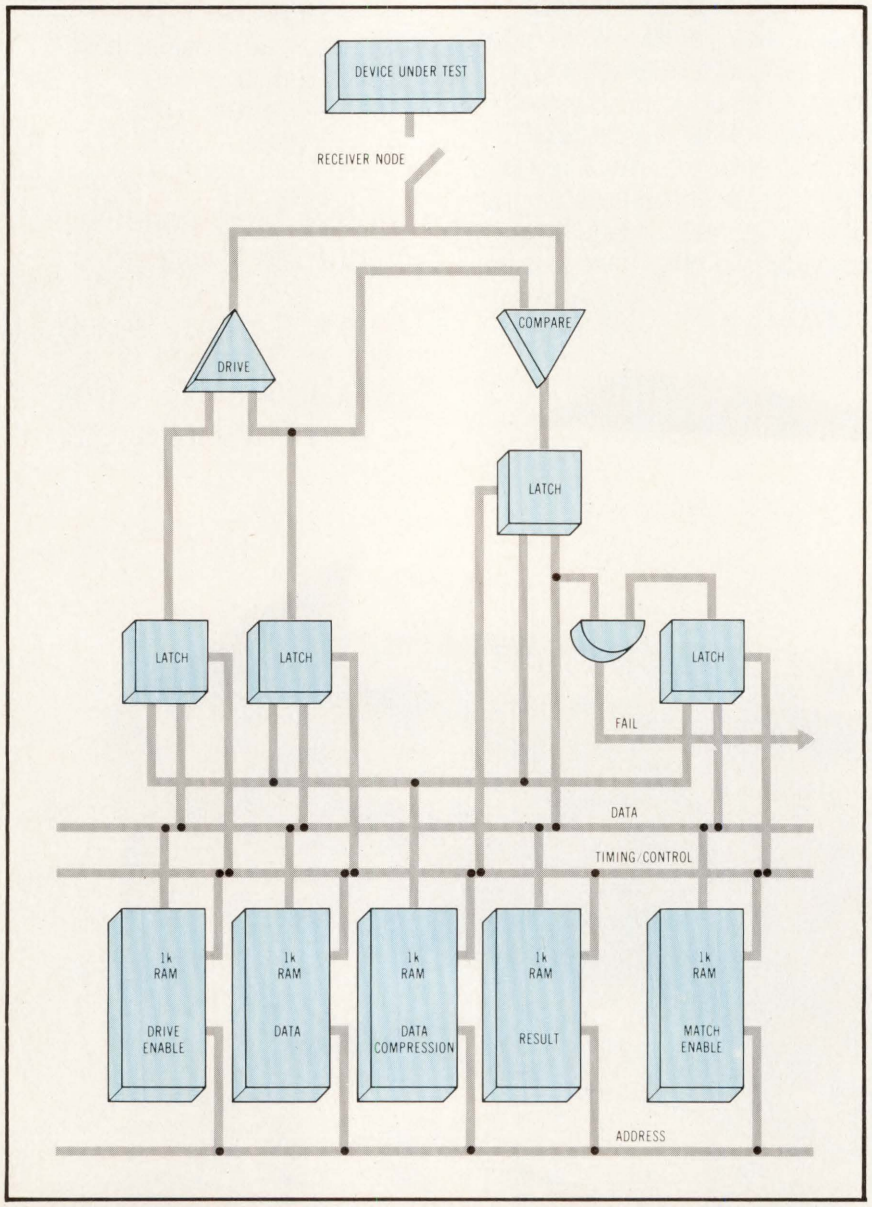
CIRCLE 52 ON INQUIRY CARD

Automatic test systems respond to escalating demands by combining in-circuit and functional test capabilities

In their attempts to meet test requirements of high density VLSI components and PC boards without exacting a price penalty, manufacturers are supplying modular systems that derive computing power from minicomputers. Becoming more important are such features as multiple test heads, more accurate timing functions, and faster clock rates to meet those of current and upcoming microprocessors.

Another result is the merging of in-circuit and functional test systems that allow such systems to be reconfigured to meet requirements for both engineering and production environments. The synthesis of these two functions also promises simpler test program generation, plus the ability to determine the nature of a problem once a faulty component has been isolated. Among the improvements evident in in-circuit testers are higher pin counts, higher speed, and the ability to handle mixed logic families. Functional testers show improved simulators and fault isolation capability.



Providing 2-MHz pin change rate, each FAST-TEST point is backed by 1k RAM, 5 channels wide. Sequence processor controls RAMs and performs test looping and subroutine implementation.

Combination functional/in-circuit test system

For isolating faults on large and complex analog, digital, and hybrid printed circuit boards, Fairchild's Series 30/333 supplies cost saving capabilities and provides both functional and in-circuit testing in one economical system. The system features 2207 digital test point capacity with ECL capability—each point with its own driver. A full capability analog test section includes 959 points, with enhanced guarding techniques for accurate component measurements.

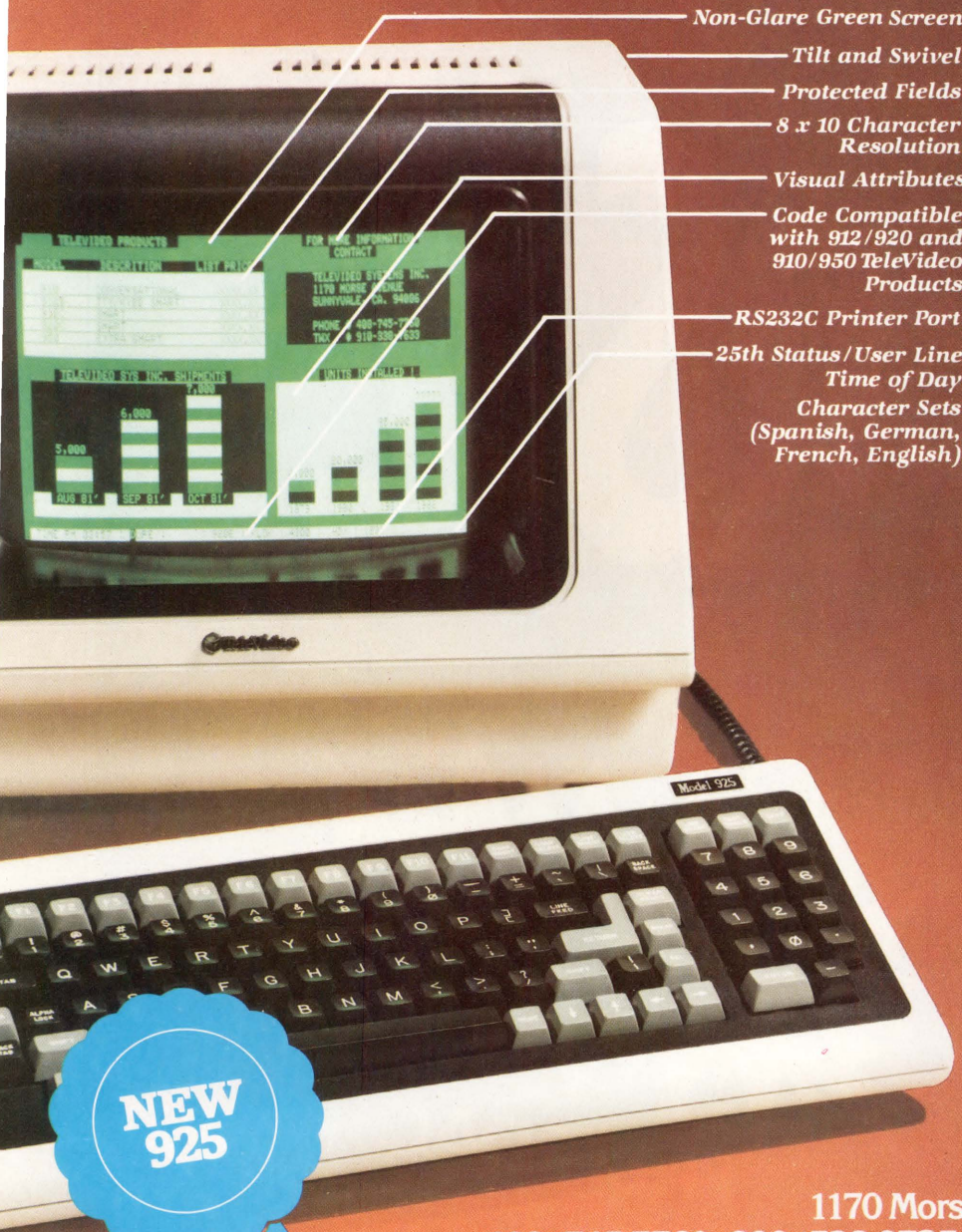
Key to the increase in fault isolation capability is the system's high speed digital test section. An optional 256-pin high speed section, FAST-TEST™ uses the company's FAST™ semiconductor technology. It not only allows the user to test dynamic parts with parallel patterns at up to 2 MHz, but also permits high speed functional exercise of LSI devices. FAST-TEST comes with a built-in sequence processor that provides efficient RAM control for test looping, subroutine implementation, and DUT initialization. More than ten times the number of vectors can be introduced at a 2-MHz data rate with this technique. Thus, a complete functional checkout of a device can be achieved: registers are tested bit by bit, and key modes and instructions are exercised. Each test pin is backed by 1k RAM, 5 channels wide. This configuration provides efficient test data and pin function control, and together with maximum data compression and minimum memory reloading techniques, achieves the high effective test rate.

Software improves in-circuit testing performance and significantly reduces test program preparation and maintenance times. The device library is included with the automatic test program generator, FAULTS™. Digital testing routines include bus disable and feedback loop disable algorithms, as well as initialization problem detection software and automatic test pattern generation. WIREGEN™, an automatic fixture wiring program, adds another tool to the program generation package. It uses test program input data to develop a fixture wiring scheme. Moreover, UUT circuit designs and the system's test pin matrix are matched during wire assignment, resulting in an

(continued on page 82)

The Performance Leader....

Model 925



Now you can have it all with TeleVideo's new 925. Code compatible with our 910 and 950 terminals, the 925, with its 6502 microprocessor-based control board can emulate our 912/920 models while operating at speeds up to 19.2K baud. This allows you to grow within the TeleVideo family of terminals, from the conversational to the smart.

The 925, a modular designed unit that uses the same power supply, monitor, and keyboard as the rest of TeleVideo's family, has built-in *proven* reliability and quality from beginning to end. TeleVideo's P31 non-glare, tiltable, green screen and detached selectric style keyboard make the 925 a comfortable, low stress terminal to use.

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CIRCLE 54 ON INQUIRY CARD

A 14-BIT DAC AT

A 12-BIT PRICE.

Now you can get the Digital-to-Analog conversion accuracy you require. At a price you can afford. Intersil's new ICL7134 is the world's first monolithic microprocessor-compatible DAC with true 14-bit accuracy. And prices start at what you'd expect to pay for a 12-bit DAC: an incredibly low $19.95 (in 100's).

TECHNOLOGY BREAKTHROUGH PROVIDES TRUE 14-BIT ACCURACY.

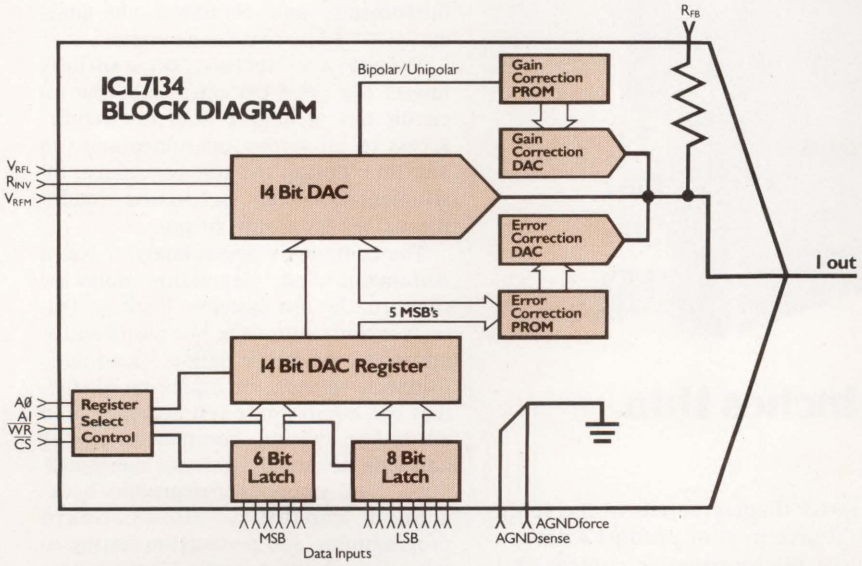
The ICL7134 is the first DAC to replace conventional, costly laser trimming techniques with on-board PROMs for linearity and full-scale correction. The result? True 14-bit endpoint linearity (.003% max.). And an ideal DAC for applications in CRT display systems, process control, instrumentation, telephony, communications, and digital audio.

PRE-ADJUSTED FULL SCALE.

Say goodbye to costly, time-consuming full-scale tweaking. The ICL7134 is factory set to 0.006% max. An on-board PROM corrects full-scale, eliminating trimming potentiometers. So labor is reduced, reliability is increased, and long-term accuracy assured.

LOW POWER CMOS TECHNOLOGY. AND MORE.

The ICL7134 uses the low-power CMOS technology (10mW typical) that you've come to expect from Intersil. Its other specs are impressive, too: an extremely fast settling time (typically 900 ns.), extraordinarily low temperature drift (5 ppm/°C), full four-quadrant multiplying capability, and a single +5 volt power supply. It all adds up to the best price/performance DAC you can buy.



DIRECT MICROPROCESSOR INTERFACE.

Double buffered inputs provide a direct interface between the ICL7134 and standard 8- and 16-bit microprocessor buses. Data can be latched in as a single 14-bit byte or dual bytes, or go directly to the output switches under software control.

NOW IN VOLUME PRODUCTION.

Now you can give your DAC applications the accuracy they deserve. Call your nearest Intersil sales office or franchised distributor, or send the coupon for full details and delivery information. The CMOS innovators at Intersil are making it a 14-bit DAC world. At a price you can't resist.

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Dear Intersil:

I'm ready for 14-bit DAC accuracy.

_____ Please rush me your data sheet on the ICL7134.

Name_____

Company_____

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City/State/Zip_____

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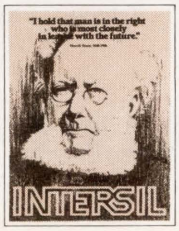


☐ Also, please send me an Henrik Ibsen poster from your "famous quotations" ad series.

CD182

efficiently wired fixture that minimizes program debug and simplifies future wiring changes. **Fairchild, Subassembly Test Systems Div**, 299 Old Niskayuna Rd, Latham, NY 12110.
Circle 265 on Inquiry Card

High pin count hybrid test systems

Supplying hybrid test capability for boards ranging up to 960 nodes (3584 pins on the 2272), GenRad's 2271 and 2272 depend on system architecture to substantially lower the price per pin. The units perform high quality comprehensive tests over a wide range of board sizes and complexities and device technologies.

For digital testing, each point has a driver/sensor backed by local memory. The resulting parallel stimulus/response testing eliminates the need to repeatedly scan a single sensor for each output, a cost reducing technique used by many systems. The local driver/sensor memory provides constant, controllable timing necessary for testing sequential devices. Having a sensor at each point also allows the system to automatically verify that the proper input stimulus level has been achieved for each test step.

Dual programmable positive/negative logic levels permit testing of ECL, TTL, MOS, and mixed logic boards and devices. Drive voltage is monitored locally for tight control of logic levels, and current is monitored to ensure system and device protection.

Precision 14-bit instrumentation provides high accuracy for analog measurements. A quadrature reactance bridge makes possible combined phase and magnitude measurements to differentiate between parallel wired components. A 4-line instrument switching matrix gives each pin programmable access to both system and external IEEE instruments, and eliminates the inaccuracy of 3-line switching systems.

System architecture substantially lowers the price per pin. Since the in-circuit test technique does not require access to all system instrumentation at any time during the test procedure, instrumentation can be shared (multiplexed) across groups of pins.

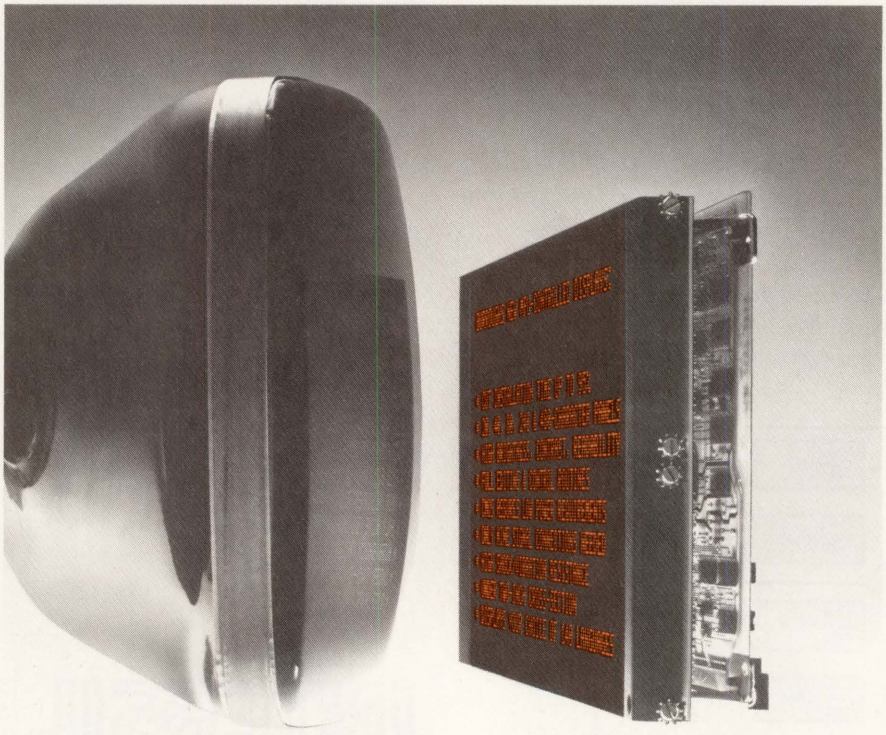
The company's circuit analyzer based Automatic Test Generation software supports the test systems. Package features include automatic bus disabling for improved device isolation, automatic feedback squelch for inhibiting glitches that can compromise test accuracy, and automatic wiring compensation for handling nonstandard device configurations. An optional foreground/background capability allows board programming and production testing to take place simultaneously. **GenRad, Inc**, 170 Tracer Ln, Waltham, MA 02254.
Circle 266 on Inquiry Card

Graphics display highlights detected faults to speed repair

An option to GEC Marconi's Autotest System 80 circuit card test station is a computer driven color graphics repair station. Model 1924 Repair Station immediately pinpoints the location of any detected faults to cut repair time.

System 80 measures each component mounted on a board under test to its true value or function in isolation from surrounding circuitry, thus establishing the

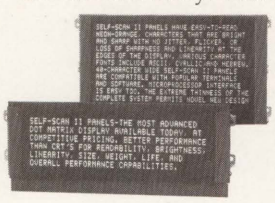
(continued on page 84)



12 inches fat...1½ inches thin.

You could fit nine Burroughs 240 or 480 character display panels in the space of one CRT. Imagine the bulk and weight you'll save in your product's design.

What's more, they're available with built-in microprocessor control and memory. All you do is feed in 8-bit signals and you've got one of the brightest, easiest-to-read displays yet. Plus savings of 50% or more in size and weight. Get the full story. Call or write for the name of your nearest representative.



Burroughs OEM Marketing, Burroughs Place, Detroit, MI 48232. (313) 972-8031. East Coast: (201) 757-5000. Central U.S.: (612) 932-3800. West Coast: (714) 835-7335. In Europe, Langwood House, High Street, Rickmansworth, Hertfordshire, England. Telephone Rickmansworth (09237) 70545.

Burroughs

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SPUR!

70 megabytes of fast Winchester Database to make systems respond

Systems respond faster, more powerfully, with PRIAM's DISKOS 7050 Winchester disc drive. As compact as a floppy disc drive, the 7050 packs 70 megabytes of database to make systems take off like a quarterhorse. A smaller-capacity, mustang version is also available in the 35-megabyte DISKOS 3450.

Shared-processor and multiprocessor systems react faster to user demands when spurred by the quick voice-coil data accessing of the DISKOS 7050. Pure and simple in design, the advanced technology 7050's use brushless DC motors to drive their discs. So they operate anywhere in the world with superb reliability.

PRIAM's interface permits you to groom your systems to user requirements, using PRIAM Winchester drives with capacities from 11 to 158 megabytes. ANSI and SMD interface options extend your systems integration freedom, and PRIAM's SMART and SMART-E interfaces can help to get your systems out of the gate more quickly.

Find out now how the DISKOS 7050 can get better performance out of your systems. Call or write to:

PRIAM

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CIRCLE 55 ON INQUIRY CARD

integrity of the entire unit under test, prior to subsequent functional testing. The system is capable of testing analog, digital, and hybrid circuit boards. Components can include passive components, discrete semiconductors, analog and digital ICs, and SSI through VLSI, in addition to circuit opens and shorts. Faults are printed as a list of faulty components and shorted/open tracks, providing diagnostic information for repair purposes.

Color graphics display on repair station augments capabilities of in-circuit tester by displaying board layout with faults highlighted. This allows operator to repair board without consulting schematic or other diagrams.

Faults detected by System 80 are transmitted via a data link to the repair station and stored there on disk. When the circuit board appears at the repair station, the stored data are consulted. The graphics display on the repair station produces a color drawing of the board with the faulty component or circuit highlighted in a contrasting color. Repair information including component type, value, stock, code, and other data are displayed with the fault summary for the card.

Source data for the repair station are provided by the operator, who uses a cursor with integral crosshair and keyboard to trace the outline drawing of the board on a digital pad. Whenever a component is encountered, it is numbered to correspond to the component number in the test program and automatically drawn to scale. This information is easily retrieved for comparison with any board needing repair. **Marconi Instruments, Automatic Test Systems Div**, 292 Gibraltar Dr, Sunnyvale, CA 94086.

Circle 267 on Inquiry Card

Test-sharing segments test and support functions

Marathon™ combines independent computer based modules into a coordinated resource that accommodates most automatic test requirements. Computer Automation's system can handle prefunctional and functional testing of loaded circuit boards, test program development, and simulation, as well as functions not previously available such as paperless rework, centralized data storage, and management information reporting.

As implemented in the system, the test-sharing concept provides modularity and configuration flexibility. The concept segments production and production support functions. High performance test stations perform only production needs, while all other functions are handled by the resource manager. Because of task segmentation, overall test environment reliability is improved. Since all operate independently, failure of a single test station or even the resource manager has no effect on the rest of the operation. Task segmentation also eliminates the conflict in the test environment between production and production support activities.

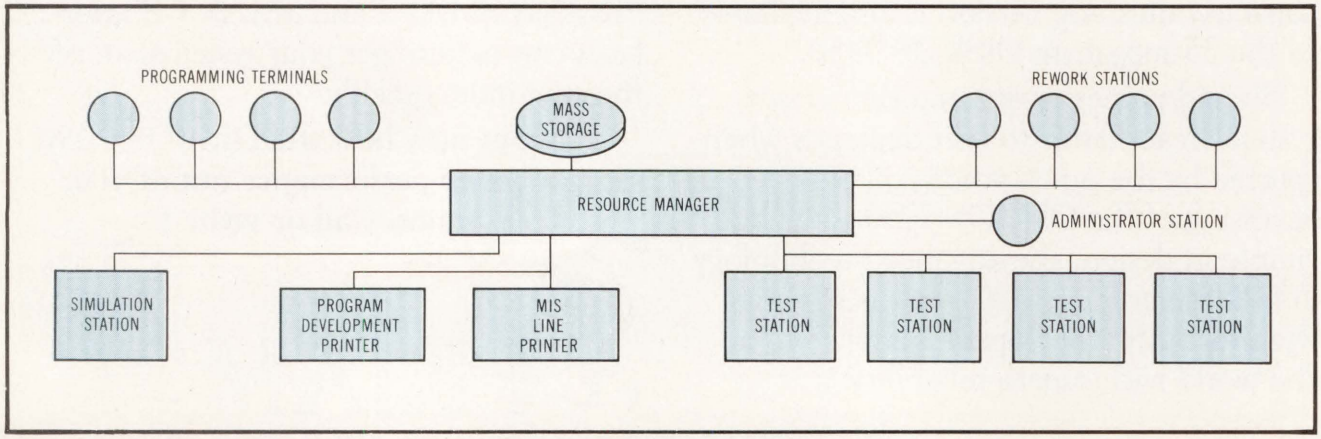
In its simplest form, the system consists of a single test or program development station, closely coupled by a high speed communications link to a resource manager, both running independently. Users can add test stations and simulation capability to accommodate increases in volume or changing test requirements. The resource manager can be augmented by adding up to four test program development stations, four paperless rework stations, 600M bytes of data storage, and management reporting.

Test stations themselves are dedicated to function, offering test pattern speeds of 16 MHz, a 4-MHz test cycle rate, and up to 1024 pins with interchangeable high speed programmable interfaces.

Prefunctional test stations pretest for manufacturing process related faults using in-circuit testing techniques. With pin capacity to 4096 pins, these stations can accommodate boards of medium to high complexity with analog and TTL, CMOS, and ECL logic.

The system's simulation capability accommodates boards using 400 or more LSI or VLSI components. **Computer Automation Inc, Industrial Products Div**, 2181 Dupont Dr, Irvine, CA 92713.

Circle 268 on Inquiry Card



Independent computer based modules of Marathon combine with test-sharing concept to accommodate most automatic test requirements and increase productivity in loaded circuit board testing.

DILOG NUMBER 1 FOR DEC 11*

With LSI 11/PDP 11 Software Compatible Disc/Tape Controllers Offering Single Board Low Power μP Based Design and Low Cost... Plus Many Other Good Reasons!

The reasons start with DILOG'S (Distributed Logic Corp's.) full time engineering and design staff. *Not outside suppliers.* That means when you contact DILOG for product selection or after sale service, you'll get "first hand" assistance...along with years of experience manufacturing μP based controllers that interface with DEC 11 CPUs.

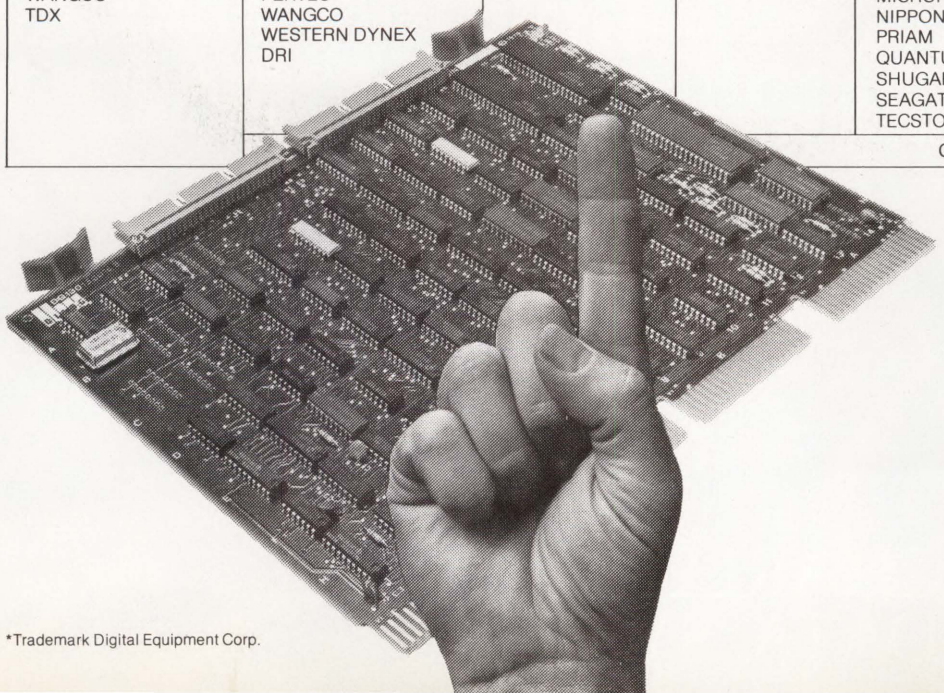
The intelligent products you'll discuss all utilize common proprietary architecture and DILOG automated design techniques—products with exceptional reliability and cost efficiency...mostly available from stock. And when you plug a DILOG controller into your DEC CPU it's ready-to-run because it's *fully operating system software compatible.*

These high performance data storage interface products also feature • minimum bus/space requirements • up to 60% less power • 10 to 50% lower cost • automatic self-test...and numerous other features for easy system integration.

Consult the DILOG/disc-tape compatibility table for your needs. Then ask for detailed data on existing, or future products from DILOG...#1 in single board DEC 11 compatible disc/tape controllers. Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643, Phone: (714) 534-8950 • 64-A White Street, Red Bank, New Jersey 07701 Phone: (201) 530-0044

DISC/TAPE DRIVE MANUFACTURER COMPATIBILITY CHART

MAGNETIC TAPE	DISC					
½" REEL-TO-REEL STD. & STREAMER	2315/5440/RK05 CARTRIDGE CLASS	CMD CARTRIDGE MODULE	SMD STORAGE MODULE	WINCHESTER 5¼", 8" OR 14"	¼" TAPE CARTRIDGE	FLOPPY DISC DRIVE
AMPEX CIPHER CONTROL DATA DIGI-DATA KENNEDY MICRODATA PERTEC TANDBERG DATA (IDT) WANGCO TDX	AMPEX CAELUS CENTURY DATA CONTROL DATA DEC DIABLO IOMEC MICRODATA PERTEC WANGCO WESTERN DYNEX DRI	AMPEX CONTROL DATA	AMPEX CENTURY DATA CONTROL DATA BALL COMPUTER MITSUBISHI	AMPEX BASF CENTURY DATA CONTROL DATA FUJITSU IMI KENNEDY MEMOREX MICROPOLIS NIPPON PER. LTD. PRIAM QUANTUM SHUGART SEAGATE TECSTOR	DEI KENNEDY PEREX QUANTEX	BASF DECITEK MICROPOLIS PERTEC REMEX SHUGART
	CAPACITIES 2.5 TO 300 MB					



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DILOG

CIRCLE 56 ON INQUIRY CARD

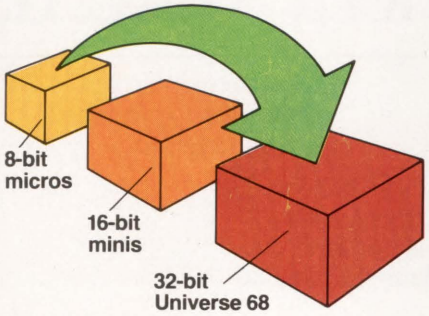
*Trademark Digital Equipment Corp.

Universe 68 leapfrogs the 16-bit minis.

CHARLES RIVER
DATA SYSTEMS

Introducing the first 32-bit supermicro for OEMs

Our new Universe 68 computer system offers powerful 32-bit architecture, a microcomputer price, the programming efficiency and portability of a UNIX-like operating system, and the refreshing experience of working with a computer supplier whose business practices are actually designed to make life easier for OEMs.



Jumping over outmoded 16-bit architecture

Built around the Motorola 68000 microprocessor, the Universe 68 system is a 32-bit supermicro that leapfrogs conventional 16-bit minicomputer technology. It has directly addressable, non-segmented address space of 16 million bytes, compared to the 64-kbyte limitation imposed by 16-bit architectures.

That means greater functionality per dollar, increased program development efficiency, and power to tackle demanding new applications.

The Universe 68/10 computer system

Outhopping supermini prices

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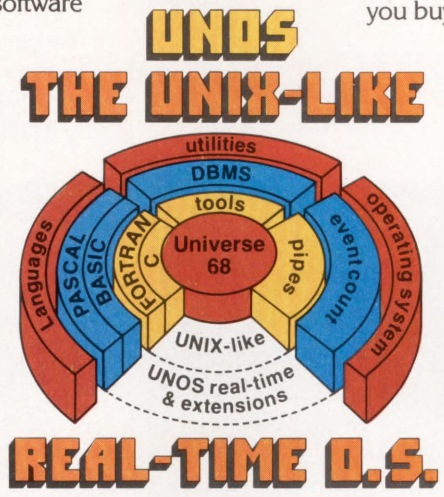

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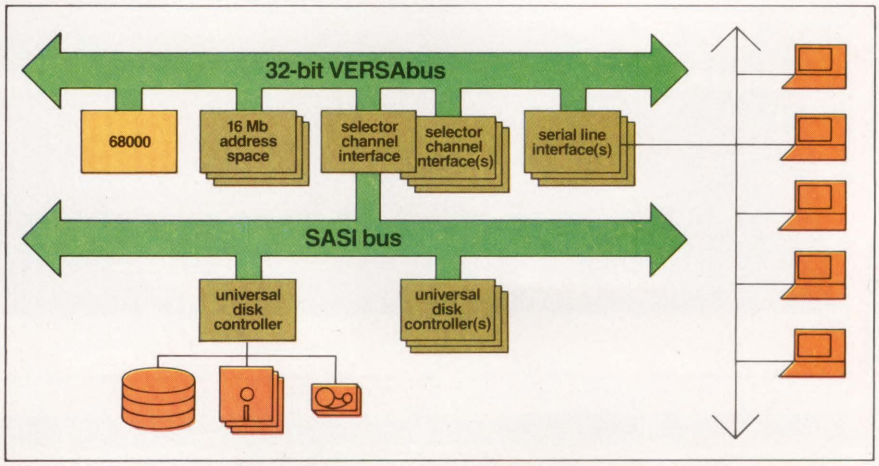

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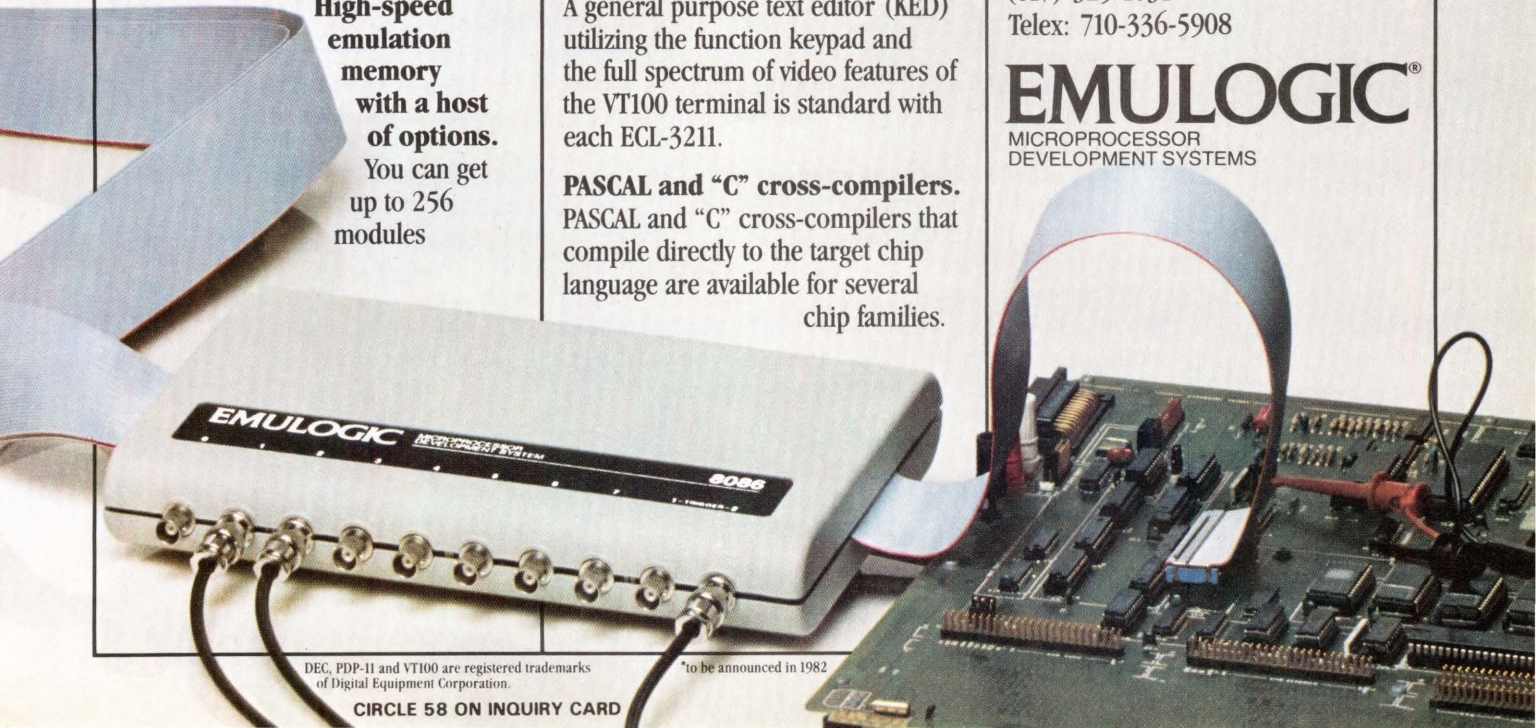

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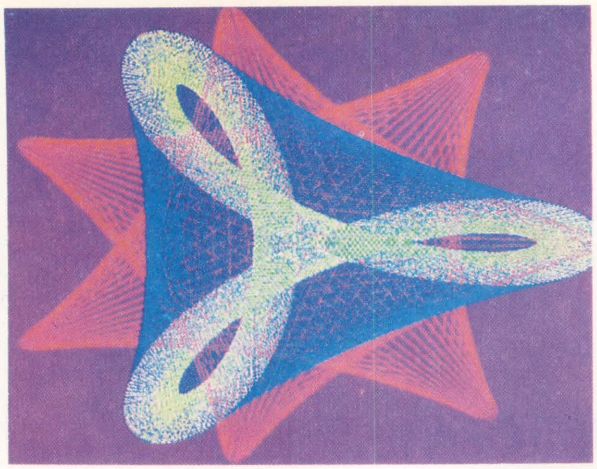
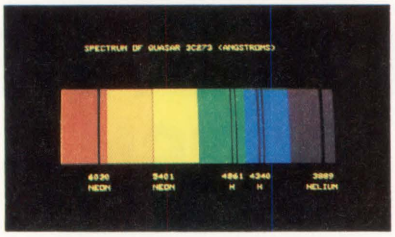
SPECIAL REPORT ON

MEMORY SYSTEMS DESIGN



"...stands well above other S-100 graphics displays in its price and performance range."
BYTE, Product Review



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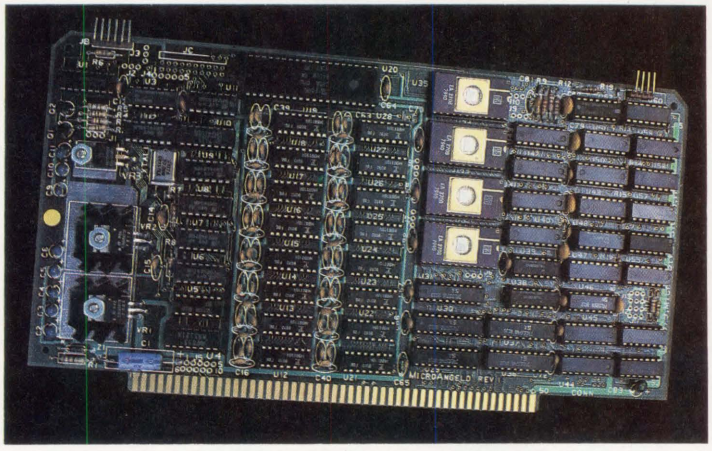

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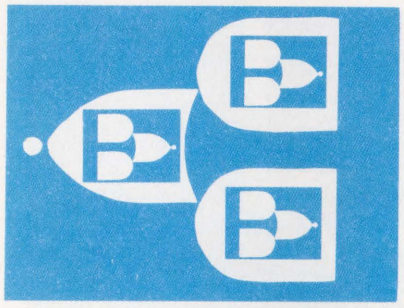

Output of 36-MHz oscillator, asymmetrically divided by three, is then divided by two to deliver a symmetrical 6 MHz **97**

Special report on memory systems design

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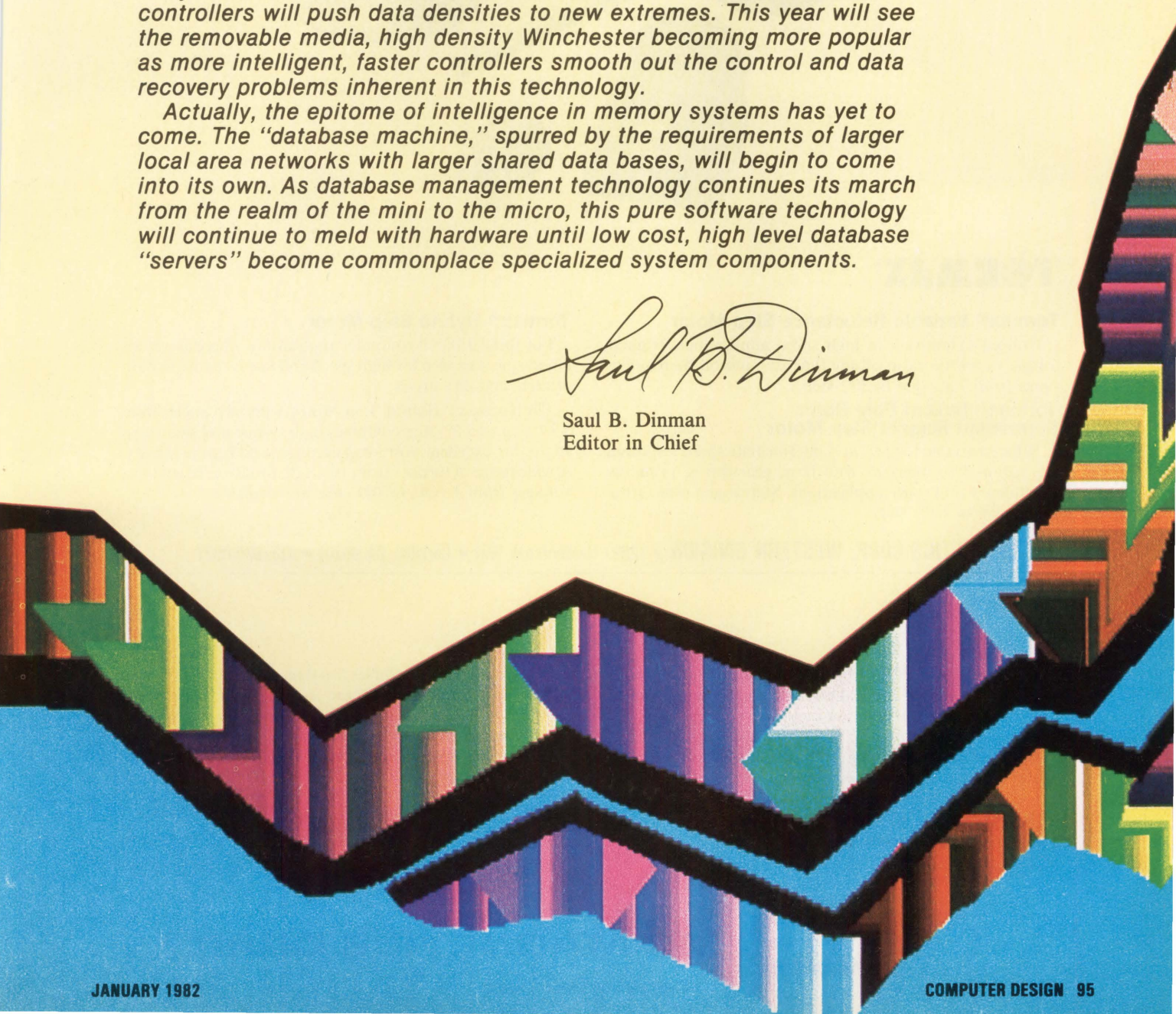
INTRODUCTION

From 2k-byte static RAM to 4M-bit dynamic MOS RAM on a chip is a long way in terms of technology, yet this has come about in only a few years. As memory chip costs have plummeted and producing more bytes per dollar has become the rule, the needs for foolproof error detection/correction and for extended memory mapping schemes have also become common. Once handled by many discrete chips and considered the domain of high cost, "High Rel" systems, LSI offerings in the coming year will probably perform these functions at costs consistent with commercial requirements. The drive toward the silicon disk will also become more feasible, and it will not be long before price competitive, "no moving parts" disks will proliferate at the same rate as their mechanical counterparts do now.

By the same token, Winchester disks, thin film heads, and smarter controllers will push data densities to new extremes. This year will see the removable media, high density Winchester becoming more popular as more intelligent, faster controllers smooth out the control and data recovery problems inherent in this technology.

Actually, the epitome of intelligence in memory systems has yet to come. The "database machine," spurred by the requirements of larger local area networks with larger shared data bases, will begin to come into its own. As database management technology continues its march from the realm of the mini to the micro, this pure software technology will continue to meld with hardware until low cost, high level database "servers" become commonplace specialized system components.

Saul B. Dinman
Editor in Chief



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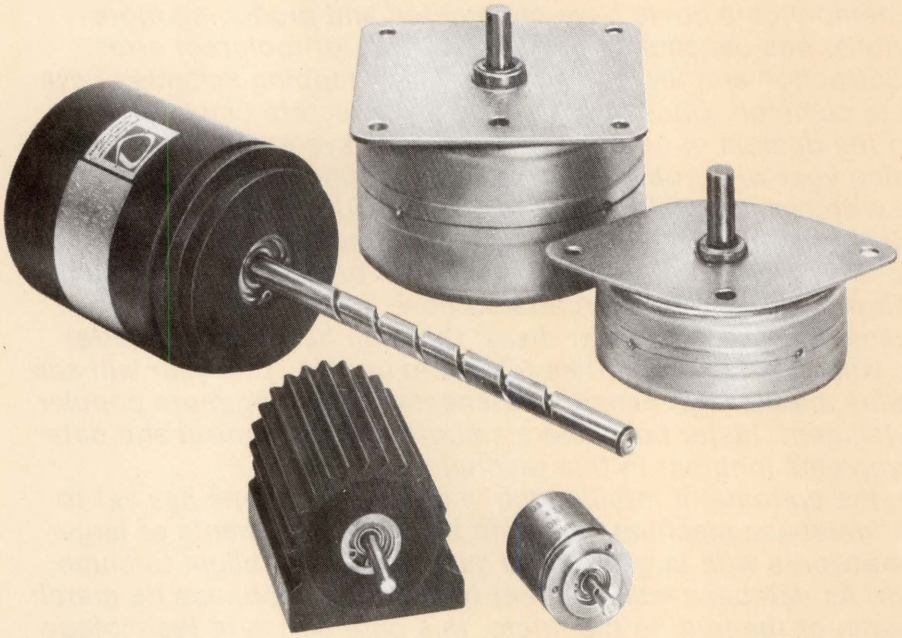

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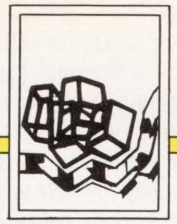

ELASTIC CLOCK PERMITS MIXING MEMORY ELEMENT SPEEDS

Better price/performance ratios can be achieved by mixing memory elements of different speeds

by David McCracken

Advanced microprocessors provide large address spaces and fast execution. To meet a particular cost/performance level, a memory system approaching the 48M-byte range of the Z8000, for instance, should include both high speed elements for locations most often accessed and lower speed memory for data storage. Slower memory can increase a microprocessor's effective bus cycle time by requesting wait periods. This requires only simple circuitry but produces lower system performance than can be achieved by cycle stretching through control of the microprocessor's clock.

One reason why wait request cycle stretching degrades performance is that it must execute in increments of full clock periods, regardless of actual memory access times. For example, the Z8000 microprocessor discussed in this article, operating at 6 MHz, will grant a 165-ns minimum wait even if the wait requesting memory needs only a 50-ns delay.

Another problem with wait requests is that they must be asserted one clock period before data are strobed into the central processing unit (CPU). While the addressed memory may be fast enough to avoid delay, the wait request generator may not be. This can happen if memory management circuitry, such as in the Z8010 memory management unit (MMU), delays valid address output in order to translate input addresses. Although this analysis is based on a read cycle, write cycle timing characteristics are similar.

The Z8010-2 6-MHz MMU uses the Z8001's A8 to A15 lines to help form a translated address. Considering worst-case delay of valid A8 to A15 input to the MMU and subsequent translation, the output address will be valid 5 ns *after* wait must be asserted—210 ns vs 205 ns. In other words, while the MMU significantly enhances many aspects of system performance, it also exacts a speed penalty of at least one wait period, especially when buffer delays are included. Unless all memory has an access time of 170 ns, including buffer delays, this wait period must be automatically included in every memory cycle. Furthermore, this problem is not unique to the Z8000 CPU/MMU combination; it is characteristic of any extensive address-manipulating circuitry.

However, the elastic clock solves both problems inherent in the wait based cycle stretch by tailoring the exact delay needed to ensure valid data transfer to each physical block of memory. Operating at a nominal 6 MHz, the elastic clock allows a delay of from 1/6 to 15/6 clock periods (0 to 417 ns in increments of 28 ns) to be defined for each of 16 memory blocks. At system initialization, the operating system tags each memory block with its stretch time. Accepting clock stretch information at the last possible moment avoids mandatory wait caused by MMU delay. It must be valid only 28 ns before the CPU operating clock edge that normally strobes in data, leaving an additional 168 ns for cycle stretching circuitry to make decisions. Although the hardware penalty exacted by the elastic clock is approximately 11 integrated circuits—which is considerably more than the one integrated circuit usually used for a clock—overall system cost and performance are improved.

The principle behind the elastic clock is that either phase of the Z8000's operating clock can be stretched,

David McCracken is a microprocessor applications consultant and principal engineer at Thera Institute, PO Box 1090, Aptos, CA 95003. His design work includes automated laboratory equipment for biochemical research, multiprocessor controlled test environments, and miniature computerized field data acquisition systems. Mr McCracken studied civil engineering at the University of California, Berkeley.

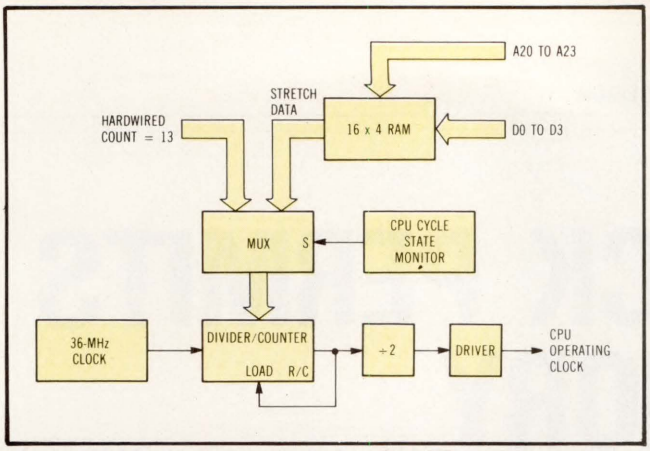

Fig 1 Divider/counter, clocked at 36 MHz, can be loaded with alternate initial counts to deliver varying CPU operating clock.

regardless of resulting asymmetry. As with many microprocessors, the Z8000's dynamic internal memory requires minimum clock activity, resulting in a maximum stretch of 2000 ns; this is much longer than the stretch needed for interfacing to most memory. Basic circuit function is outlined in Fig 1.

A divider/counter divides the 36-MHz oscillator by three. For a normal 6-MHz CPU clock, when the count reaches 15, the carry output feeds back to the synchronous load input, causing a reload of 13 on the next input clock. The resulting ripple/carry (R/C) output represents 36 MHz asymmetrically divided by three, which is then divided by two to deliver a symmetrical 6 MHz. Either phase of the output clock can be stretched by reloading the counter with a number less than 13, thus requiring more input counts to reach maximum. A reload of 12, for example, would add one count or 28 ns to the output clock half-period, while a reload of 0 would add 417 ns.

Since deviation from a uniform 6 MHz is required only at a specific time in the Z8000 memory cycle, the circuit monitors the CPU cycle status to determine the point at which the counter should be reloaded with stretching data. At that point, the multiplexer feeding the input count is switched to select a value determined by the speed of addressed memory. All other CPU clock half-periods are formed by a hardwired reload of 13.

Clock stretching reload values are then delivered to the multiplexer by a 16- x 4-bit random access memory (RAM). The RAM is addressed by A20 to A23 from the computer system address bus while stretch data are written by the Z8000 at system startup. Each of the sixteen 1M-byte memory blocks is assigned a stretch of 0 to 417 ns. With increments of 28 ns available, cycle delay and memory response times can be precisely tailored to

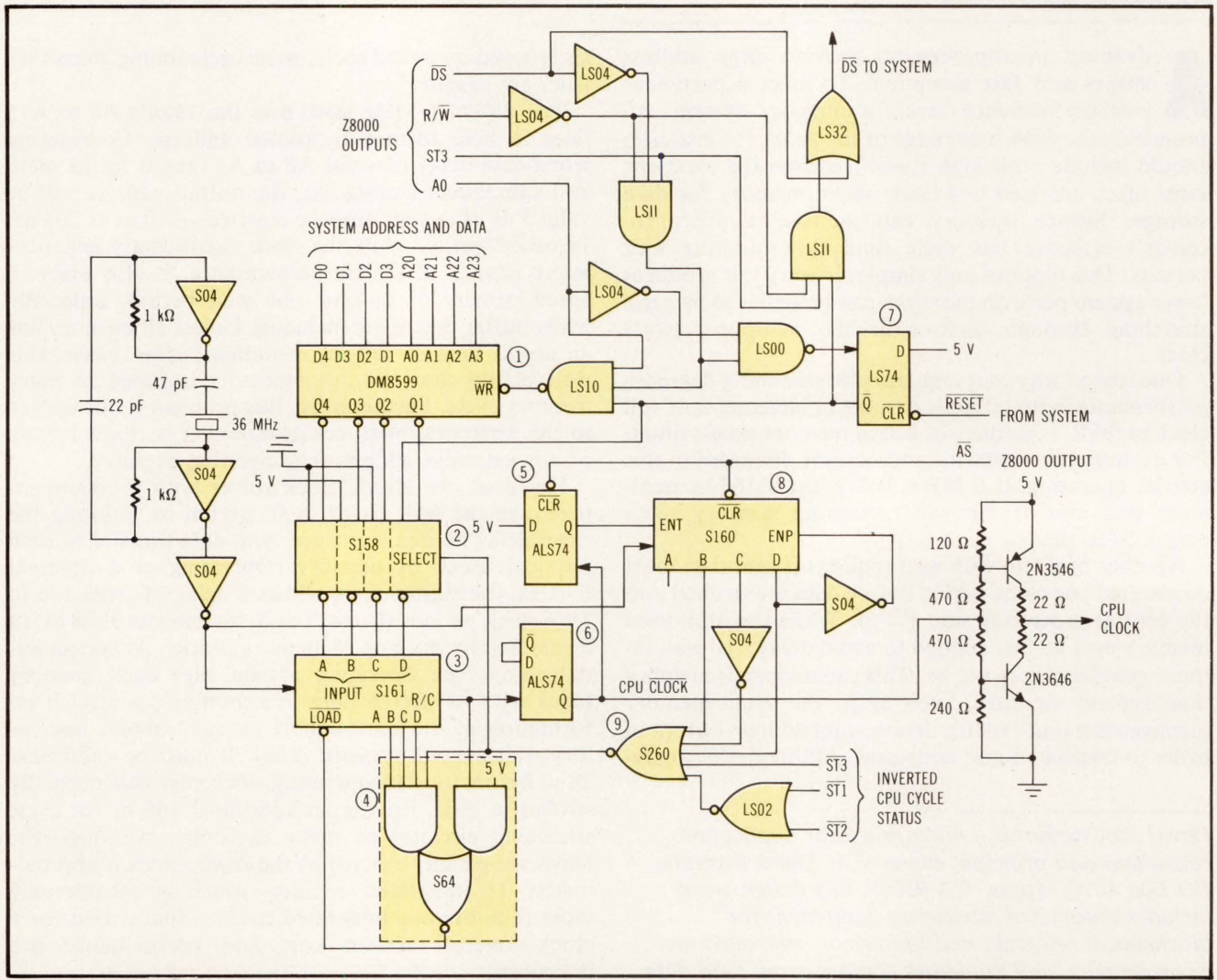

Fig 2 Counter (3) divides 36 MHz while counter (8) keeps track of CPU cycle state to synchronize source control of divider's initial count input.

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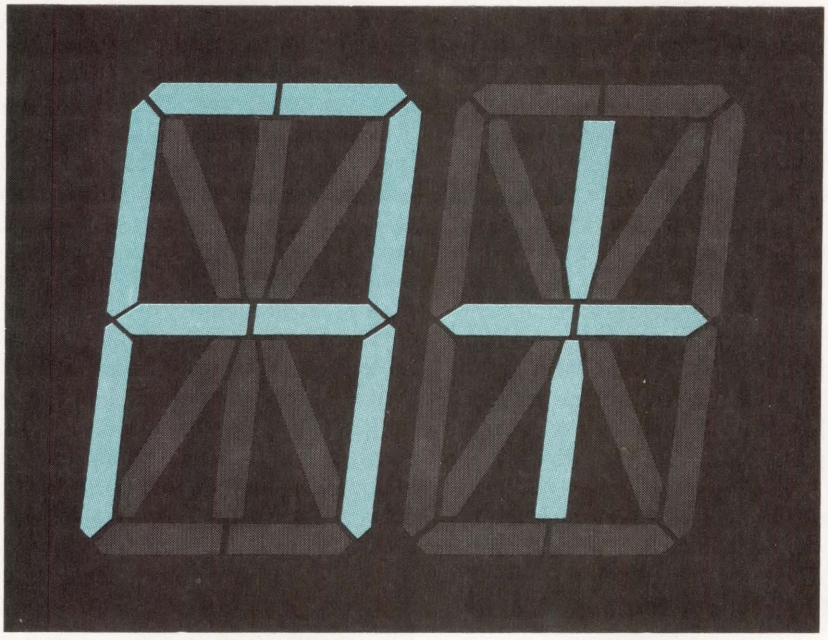

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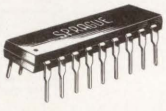

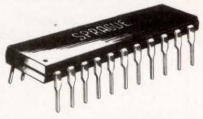

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deliver the highest performance per cost of components. Also, the stretch load occurs at count 14 of the final operating clock half-period before the CPU strobes in data. This allows 160 ns from MMU output address valid to stretch input required valid, thus eliminating a mandatory wait.

Fig 2 shows the complete schematic which, in addition to the functional blocks in Fig 1, shows how to write data into the stretch RAM. System $\overline{\text{reset}}$ clears flipflop ⑦, establishing several conditions for initialization. First, a 0 is fed to the most significant bit input of divider/counter ③, creating a 3.3-MHz CPU operating clock that relaxes memory response requirements throughout the address space. Flipflop ⑦'s $\overline{Q}$ output also combines with the CPU's read/write (R/$\overline{W}$) and status output, ST3 (1 = memory access cycle), to disable the system data strobe ($\overline{DS}$) on memory writes. At the same time, $\overline{Q}$ enables write to stretch RAM, provided that A0 from the CPU is 1 (ie, odd addresses only). Under these conditions, the Z8000 can write to any odd address in a memory block and store data (D0 to D3) at the corresponding stretch RAM address without affecting actual system memory.

After tagging each of the 16 blocks with its characteristic delay, the Z8000 writes to any even address, causing flipflop ⑦ to toggle without affecting any other circuit elements. When initialization is complete, divider/counter ③ usually reloads itself with 13 to yield a symmetrical 6-MHz operating clock after division by flipflop ⑥.

Normal reload occurs at the end count because load is controlled by the R/C output. Since R/C also provides the clock input to the divide-by-two flipflop, a stretch reload must occur before the end count to delay the operating clock transition. Count 14 is combined with the CPU cycle state to determine the stretch load time.

Fig 3 shows a typical memory access cycle. Ideal time for clock stretch is the high phase of period T3, just before the CPU strobes in data on falling clock edge Ⓑ. Cycle state counter ⑧ (Fig 2) is cleared by address strobe ($\overline{AS}$), which the Z8000 asserts in every T1 to indicate address output on the multiplexed address/data lines. Flipflop ⑤ (Fig 2), also cleared by $\overline{AS}$, inhibits counting until it is toggled by operating clock edge Ⓐ.

On each subsequent 36-MHz clock low/high transition, state counter ⑧ advances, as shown in the expanded timing diagram in Fig 4. Output count is combined with CPU status information ST1 to ST3 (Fig 2) so that at counts 4 and 5 on memory access cycles, NOR gate ⑨ output goes high. This selects stretch memory as input to divider/counter ③ through multiplexer ② and also enables divider count output of 14 to activate the load input. Thus, final count is not reached at the usual time unless the selected stretch memory location contains 15 (ie, no delay is needed). Because stretch memory reloads the divider/counter with 11, the cycle illustrated in Fig 4 is delayed by two 36-MHz clock periods. Non-memory cycles such as input/output, indicated by ST1 to ST3, disable clock stretching. During these cycles the normal wait request is still functional.

Microprocessors other than the Z8000 require changes only in the cycle state monitor to take advantage of the elastic clock. Future memory management devices could include onchip R/W memory to supply the clock with delay information characteristic of every memory segment. Thus, external circuitry would be simplified and a finer division of memory space would be provided.

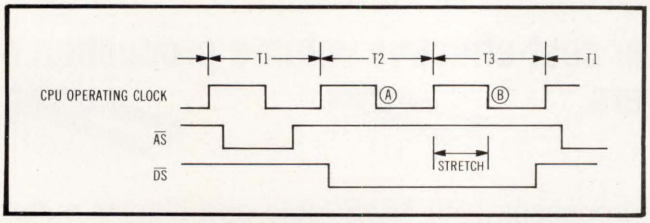

Fig 3 T3 clock high is ideal half-period for stretching because it allows longest time for address delays before falling edge Ⓑ, used by the CPU to strobe in data.

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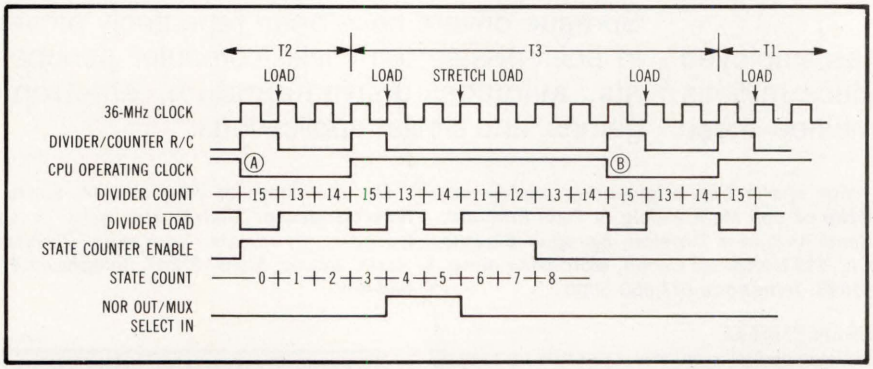

Fig 4 Divider/counter is normally reloaded at count 15 by its own carry output, but stretch load occurs on count 14. Data loaded at this time determine length of stretch in increments of 28 ns/count.

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X.25

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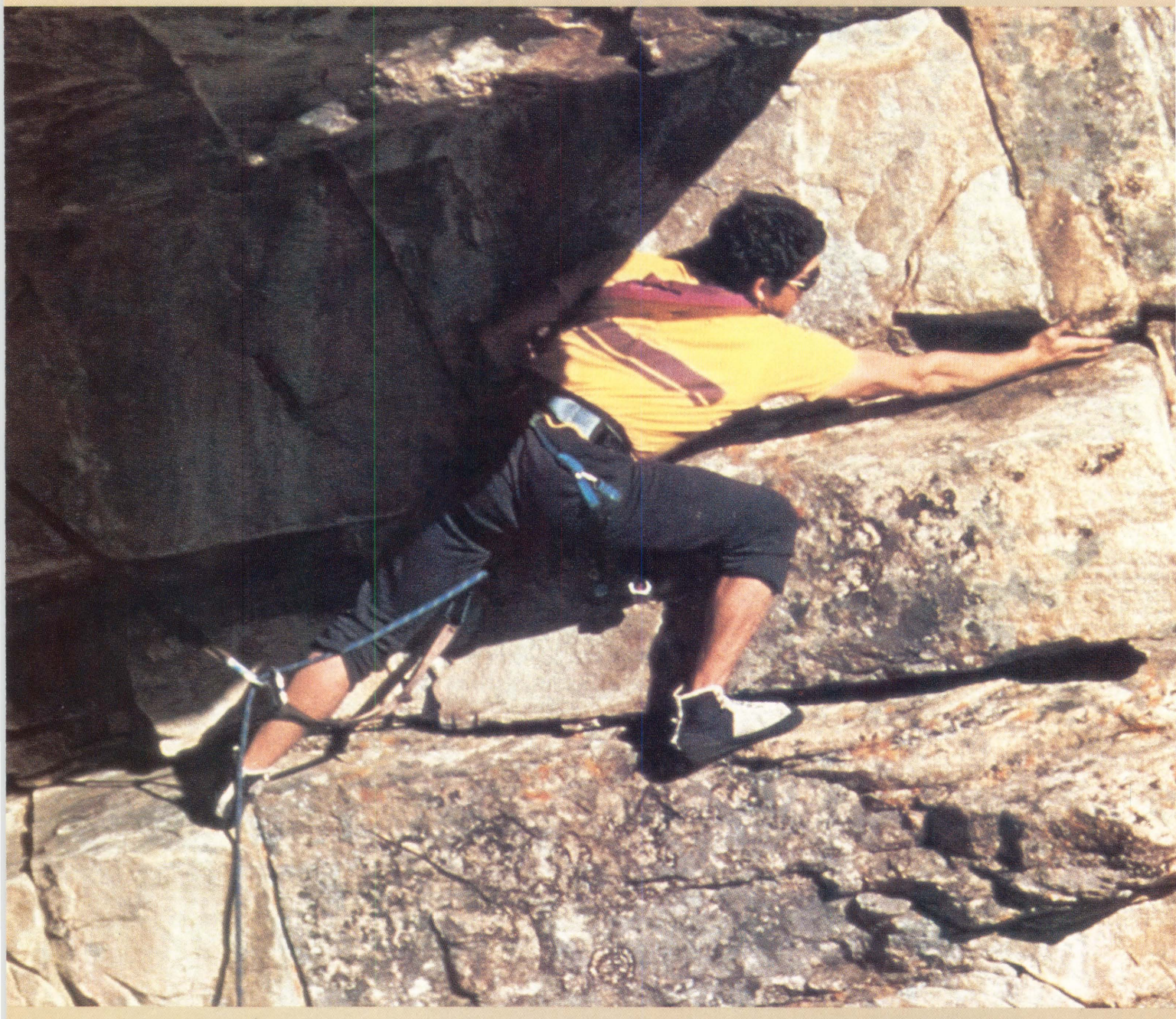

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MB8116	Dynamic RAM	16K x 1	150ns	NMOS
MBM2764	EPROM	8K x 8	200ns	NMOS
MBM2732A	EPROM	4K x 8	200ns	NMOS
MBM2716	EPROM	2K x 8	350ns	NMOS
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MBM2148	Static RAM	1K x 4	55ns	NMOS
MBM2149	Static RAM	1K x 4	45ns	NMOS
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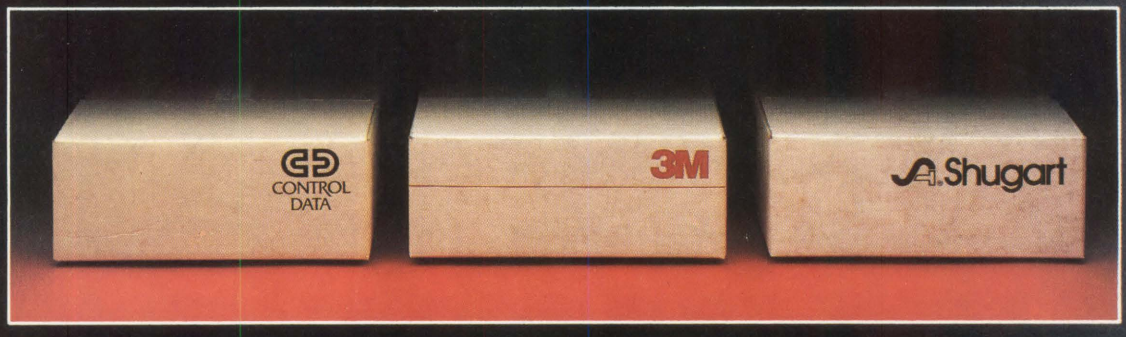

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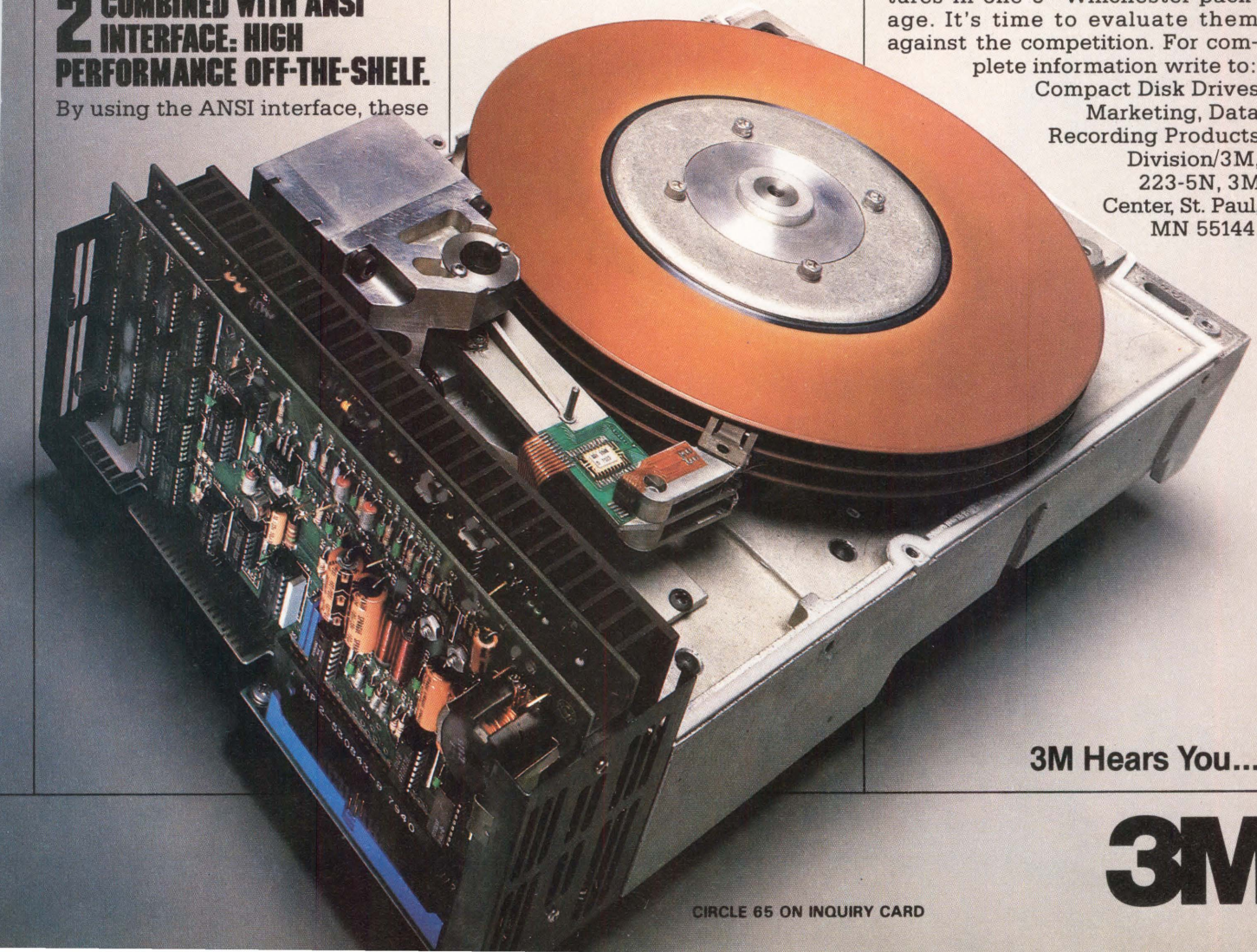

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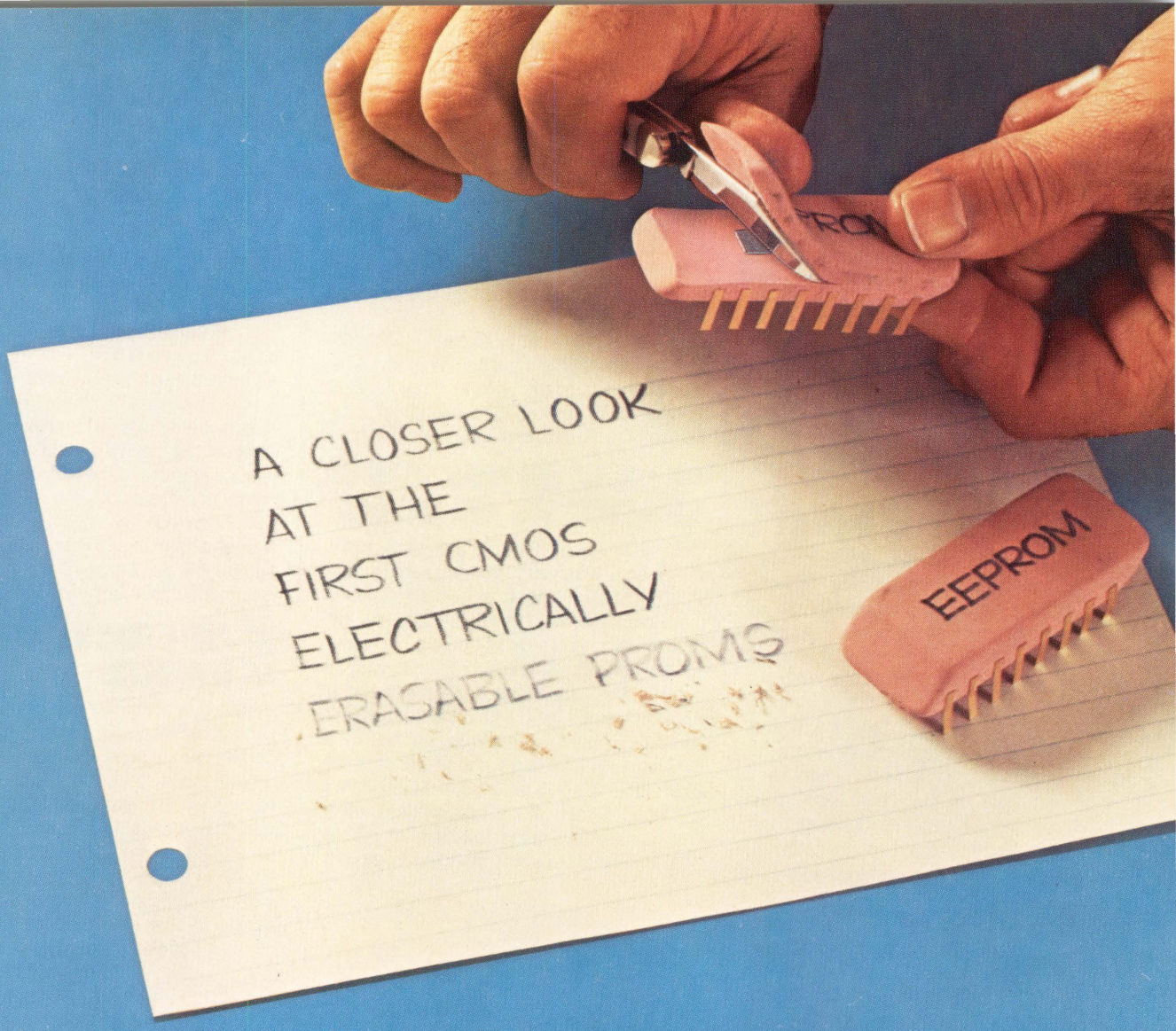

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The HNVM 3004 (512 x 8) and the HNVM 3008 (1024 x 8) EEPROMs can be written 10,000 times and retain information for 10 years at 125°C or 20 years at 70°C. Naturally, the Hughes HNVM 3000 series are compatible with all major logic families.

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SEMICONDUCTOR MEMORY UPDATE: DRAMS

Dynamic random access memories are one of the most dynamically changing component areas in the business. The current state of the DRAM art is reviewed here.

by Eugene R. Hnatek

In 1981, prices for 16k dynamic random access memories dropped to such low levels that the device became a commodity item with marginal profitability. This caused many suppliers to cease production and gear up for the 64k version. The past year has witnessed the 64k dynamic random access memory rise to production status. Because of the large potential market for this device (said to exceed $1 billion by 1985) and the impending war of competition, prices have dropped rapidly as participants have jockeyed for market share. At present two U.S. suppliers, Texas Instruments and Motorola, are in volume production, as are about six Japanese suppliers—Fujitsu, Hitachi, Nippon Electric Co, Toshiba, Mitsubishi, and Oki. However, many users are waiting for major U.S. suppliers (Intel, Mostek, INMOS, National) to bring their products to market before making a commitment. These suppliers are introducing redesigned versions of earlier designs.

The issue of redundancy for large memories cropped up at the 64k level and will most certainly apply to 256k dynamic random access memories (DRAMs). In the area of quality, however, U.S. suppliers have pulled even with the Japanese at the 16k level. The battle over quality at the 64k level has yet to be fought.

Random Access Memories

Dynamic and static characteristics have been merging, and both dynamic and static random access memories (RAMs) have adopted the single 5-V power supply. Another shared feature is power-down, previously offered only by DRAMs, which are now being designed with hidden or transparent refresh, making them look static to the user. One factor that is instrumental in this merging is the reduction in the cell size of static RAMs (SRAMs). Although the dynamic cell is still considerably smaller than the static cell, the latter has decreased in size at a rapid rate. The cell for a static 16k device is as small as 100 μm^2 (or 1.5 mil^2), with smaller cells yet to come.

As device densities increase, device geometries dwindle. As the line widths and associated oxide thickness decrease, so must the operating voltage to avoid punch through and oxide breakdown. The standard 12-V power supply for 4k and 16k dynamics has already given way to 5 V for 64k and 16k devices. Although 5 V may

Eugene R. Hnatek is vice president and general manager of Viking Laboratories, 440 Bernardo Ave, Mountain View, CA 94043. Prior to this, he held management positions at several other companies in the semiconductor industry. An authority on ICs, Mr Hnatek has published six books and more than 100 articles on the subject. He received BSEE and MSEE degrees from Bradley University.

In December 1981 *Computer Design* published one chapter of Mr Hnatek's upcoming book on semiconductor memories, "Semiconductor Memory Update: EEPROMS." Next month *CD* will publish a third chapter, which examines gallium arsenide integrated circuits.

still be used for the 256k dynamic RAM, the voltage will be reduced to 2 or 3 V, as line widths fall below 2 μm.

The by-one configuration has been the dominant choice for DRAMs for device densities of 1k and 4k, but starting with the 16k device, other organizations (bytewide) are appearing. The dilemma posed by the by-one organization for very large densities is memory size modularity. At the 256k device level, the smallest memory system increment will be 256k; the next occurs at 512k. For many systems a by-four or by-eight alternative may be more attractive than by-one in that they still allow the new greater device density to be utilized. These organizations are forthcoming as will be discussed.

Dynamic RAMs

1980 witnessed the first major test for the dynamic RAM (DRAM) market since its inception about 10 years ago. This was due to the combined effects of the general downturn in the economy, the magnitude of the DRAM market, the changes that have occurred in the supply-demand relationship for the 16k dynamic RAMs, the high degree of technological change involved, and the huge capital investment required for the evolution from 16k to 64k dynamic RAMs. Further, overseas manufacturers, mainly Japanese, achieved major penetration into the world memory market over the last few years as a result of the supply shortages of 1979 and early 1980; and the overall quality and reliability of the products supplied by these firms are high.

Dynamic and static characteristics have been merging, and both dynamic and static...RAMs...have adopted the single 5-V power supply.

The severe price erosion of the 16k DRAM has adversely affected the later entries into the market, as well as those manufacturers who have not been able to achieve a competitive cost status. The flight of suppliers from the marketplace accelerated in 1981. In particular, this will reduce the semiconductor industry's ability to react to short-term increases in demand. Both the manufacturer and user of dynamic memories must face two major challenges over the next few years. One is to insure an adequate supply of the workhorse 16k DRAM. The other is to make the transition to the next generation of dynamic RAMs, the 64k version, in a way that does not confront the industry with any disruptive financing or design and manufacturing problems.

16k DRAMs. The 16k dynamic RAM achieved mature product or commodity item status in 1980 and is believed to be the most important semiconductor device, to date, from an economic viewpoint. High volume production is expected for the next several years until the 64k DRAM achieves high volume product status (about 1985). Currently there are about 12 suppliers (7 American and 5 Japanese) of 16k DRAMs. However, this number is expected to dwindle because of the serious price erosion that has been taking place since about November 1980. Manufacturers are turning to products with higher profit margin potential. Of the 200 million or so 16k DRAMs sold in 1980, 40% came from Japanese suppliers. Typical 16k DRAM performance was shown in Table 5 of Reference 1 (*Computer Design*, Jan 1980, p 124). Address access times of 100 to 120 ns are at the leading edge, and the device is supplied by a number of manufacturers. In terms of power dissipation, Mostek and National are the leaders.

32k DRAMs. Occupying an intermediate position between 16k and 64k DRAMs is 32k, an unusual bit density that seems to have been fostered by several manufacturers. As occurred at both the 4k and 16k levels, many manufacturers were realizing economic returns from selling partial memories for less demanding applications. For example, a faulty 64k device can be sold as a 32k DRAM once the faulty cells have been identified and isolated. This represents a small volume of memory usage and sales, but, if shortages occur, a large market could develop because for each good 64k DRAM produced there will be several rejects which may be good at the 32k-bit level. Table 1 summarizes unit 32k DRAM products.

64k DRAMs. As with previous generations of metal oxide semiconductor (MOS) RAMs, price-performance divisions are expected among manufacturers and customers alike. Some will be concerned with the speed, others with the power dissipation. Consequently, different products will be optimized for these parameters. The bulk of 64k DRAMs is expected to be the 120-ns version, which is currently producible only by the Japanese. Further, it is now believed that the 64k DRAM is the "end-of-the-line" for the present generation of processing and photolithographic techniques, which are being pushed to their limits. At the next density level (256k), conventional projection printing equipment will be replaced by a direct step on wafer process or some other more exotic photolithographic process. Then, too, the technology required to produce the 256k DRAM is still in development as is its fabrication equipment. All of this points to increased technological problems and enormous capital equipment costs, much as was incurred at the 64k level, that will certainly slow the introduction of new DRAMs.

In 1978 and 1979, several manufacturers made premature product announcements. The parts appeared later than planned because mass producing prototypes of the 64k DRAM was more difficult than had been anticipated. The 64k DRAM's complex nature may have been underestimated in the original product announcements. It is not a natural evolutionary product. Also, the manufacturing processes are expensive. Some of the technical advances (detailed in the technical literature) that were made in order to develop producible 64k DRAMs are as follows: reducing memory cell size, using polysilicon or metal bit word lines, using folded bit lines, reducing the number of cells per bit line, using thick dielectric, increasing storage capacitance by using different capacitor construction techniques or bootstrapping word lines, addressing the issue of substrate bias, and providing a means of alpha particle protection.

The 64k DRAM, along with the 16k SRAM and the 16k electrically erasable programmable read only memory (EEPROM), is the focal point of the most frenetic activity in the semiconductor industry. Strong focus is on this device because of severe price erosion at the 16k level.

Latest Edition

Remex Times

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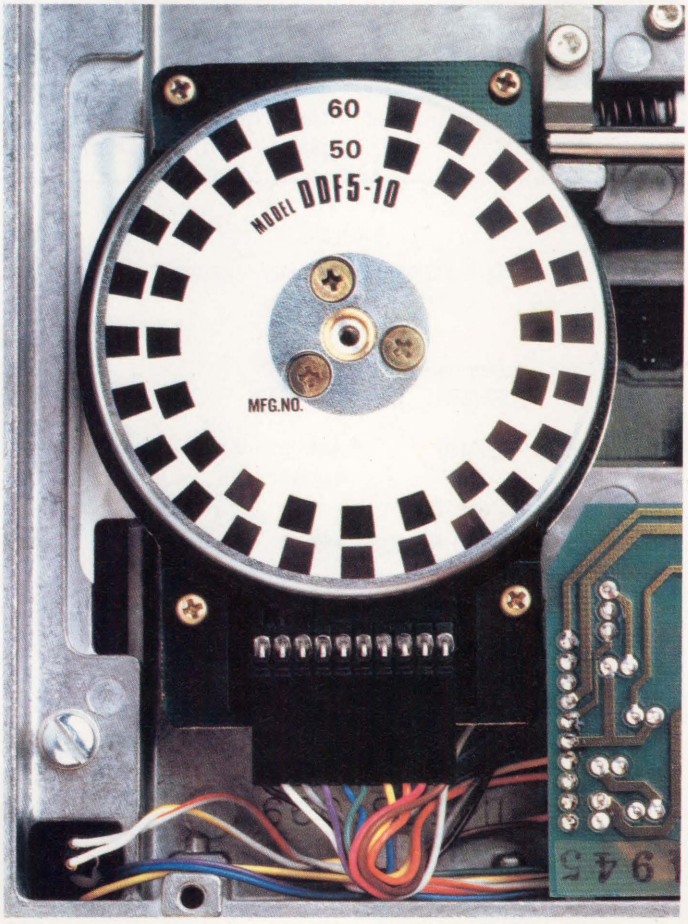
THE HIDDEN TRUTH ABOUT 5¼ INCH FLOPPYS

Belts and Brushes Murder on Life Span

The bad news for mini floppy disk drive buyers is that 5¼ inch drives are designed with belt and brush type AC motors . . . and they suffer the consequences. The good news according to high level authorities is that there is an exception. The Remex PICO™ 48/96 tpi, 5¼ inch flexible disk drive has no belts or brushes because it is the first mini-sized floppy with a direct drive DC motor. Direct drive means that improper belt seating is nonexistent so variations in speed and friction-producing side loading are eliminated. Motor life is also extended. A reliable industry source indicates that the MTBF of the PICO motor is 5 years—typically ten times that of most brush type motors. The President of the United States, in his comments, stated (continued on Page 5).

Trouble Maker Eliminated

"Tap-tap wear is a thing of the past" according to design engineers evaluating the Remex PICO 5¼ inch flexible disk drive. This major cause of media damage and wear on mini floppy drives, the loading and unloading of the head on the media, has been eliminated with the Remex PICO because the PICO has no head load solenoid.This design innovation also reduces magnetic leakage which may result in data errors. Rumors that PICO will receive an award from the Association for the Preservation of the Sanity of Systems Designers were not confirmed by Remex.



Direct drive DC motor saves life of 5¼ inch floppy.

Designers Spellbound by Interchange

Reliable interchange of media between Remex PICO drives is enhanced by the precise speed control of the motor's closed loop servo. Speed is regulated to 1% on Remex PICO versus typically 2¼% on other small drives, therefore read/write errors caused by speed variation are not a major factor with PICO. The drive's speed control may also simplify controller design because phase lock loop requirements are less demanding. Vast crowds of cheering engineers stood outside the office of (continued on Page 11).

Drives Embezeled!

A choice of bezel sizes on the Remex PICO 48/96 tpi, 5¼ inch floppy makes this drive the appropriate choice for a wide variety of system configurations according to sources. Among the sizes available is a 2¼ inch low bezel which is ideal for space limited micro-systems. An "industry standard" bezel is optional.

Proud Parent Praises PICO

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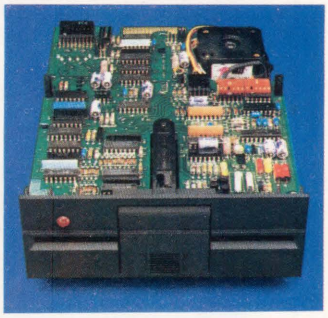

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TABLE 1

Available 32k Dynamic RAMs

Manufacturer	Part No	Org	TAA (ns)	PDISS (mW) Active/Standby	Power Supply (V)	Pins
Mostek	MK4332	32k × 1	200	482/40	12, ±5	18
TI	TMS4132	32k × 1	150/200/250	380/18	12, ±5	18
Motorola	MCM6632[a] MCM6633[b]	32k × 1	150/200	250/25	5	16

Notes:

[a] Partial of 64k MCM6664 with pin 1 refresh

[b] Partial of 64k MCM6665 without pin 1 refresh

Address 15 is held either high or low on pin 9 to select usable half of chip.

Pin 1 — automatic refresh control

Most Japanese semiconductor manufacturers are shifting their capacity from the 16k toward the 64k DRAM and the 16k SRAM area. They are counting on an edge they believe they possess for each of these part categories to gain market dominance and thus market control.

The 64k DRAM is just beginning its production cycle and is projected to peak between 1985 and 1987. Currently there are 17 announced commercially available sources of the 64k x 1 DRAM (Table 1). Of these, 5 are in the production stage, 3 to 4 are in the product sampling stage, and the remainder have no parts that are

TABLE 2

64k × 1 DRAM Availability Summary

Manufacturer	Part No	Die Size (mil^2)	Access Time (ns max)	PDISS (mW) Active/Standby	Pin 1 Function	Refresh Cycle 128-Cycle (2 ms)	Refresh Cycle 256-Cycle (4 ms)	Onchip Redundancy
IBM	Internal-NCA	62,500	330-440	360/20	N/A		X[a]	Yes
Bell Labs	Internal-NCA	61,800	170	440/NA	N/A	X[b]		Yes
TI	TMS4164	33,000	150, 200, 250	200/27	No Connection		X	No
Motorola	MCM6664	39,000	120, 150, 200	275/30	Refresh	X		No
Motorola	MCM6665	39,000	120, 150, 200	275/30	No Connection	X		No
NEC	UPD4164D	50,650	150, 200, 250	250/28	No Connection	X		No
Hitachi	HM4864	45,460	150, 200	330/20	No Connection	X		No
Fujitsu	MB8264	34,300	150, 200	303/28; 248/28	No Connection	X		No
INMOS	IMS2600	34,520	100	300/10	No Connection		X	Yes
Mostek	MK4164	40,750	120, 150, 200	300/22	Refresh	X		No
Mostek	MK4564	40,750	120, 150, 200	300/22	No Connection	X		No
Intel	I2164	36,100	150, 200, 250	N/A	No Connection	X		Yes
Mitsubishi	M5K4164S	41,750	150, 200	250/275	Refresh	X		No
National Semiconductor	NMC4164	29,000	120	200/22	No Connection		X	No
Toshiba	TMM4164C	38,600	120, 150, 200	250/275	No Connection	X		No
Oki Semi	MSM3764	N/A	120, 150, 200	N/A	No Connection	X		No
Fairchild	F4164	36,450	120, 150, 200	200/75	No Connection		X	No
Siemens	HYB4164	39,000	150, 200	150/20	No Connection		X	No

Notes:

All parts are in industry standard 16-pin DIP except IBM (40-pin) and Bell Labs.

All parts operate from single 5-V supply except IBM (8.5, 4.25, -2.2) and Bell Labs (8, -5).

[a] 2- to 3-ms refresh rate

[b] 4-ms refresh rate

NCA — Not commercially available

N/A — Not available

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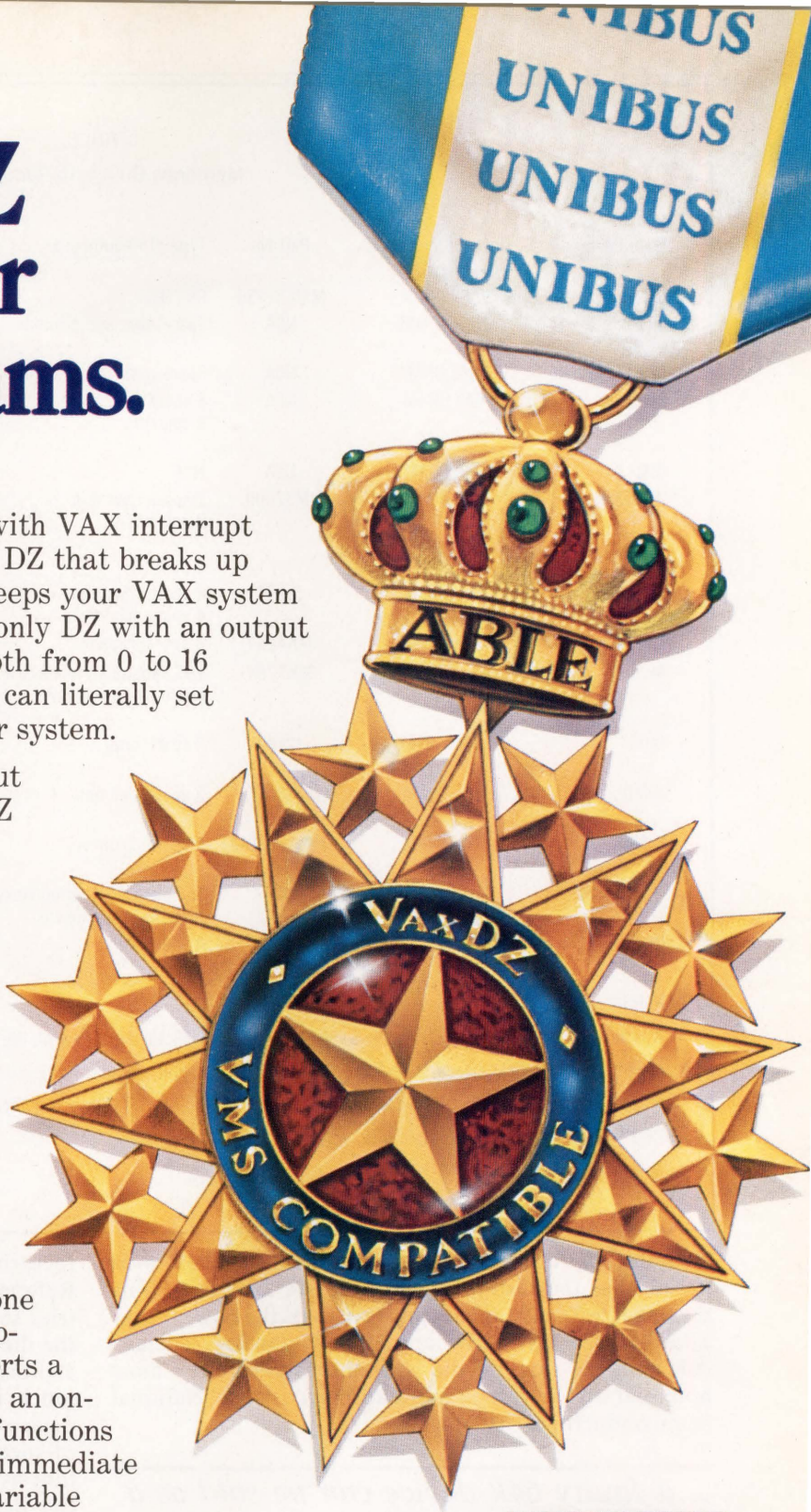

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TABLE 3

Memories Built with Redundancy

Manufacturer	Type of Memory	Part No	Type of Redundancy	Programming Techniques	Note
Oki Electric	256k DRAM	MSM37256	6k cells		
Siemens AG	256k DRAM	NCA	Spare rows and columns	High voltage pulses at wafer test, poly fuse	
NTT Musashino	256k DRAM	NCA	Spare rows and columns	Mode register	
Bell Labs	64k DRAM	NCA	8 spare rows and 8 columns	YAG laser pulse	Requires critical mechanical positioning
IBM	64k DRAM	NCA	N/A	N/A	
INMOS	64k DRAM	IMS2600	2 spare rows and 2 columns	High voltage(12-V) pulses at wafer sort, poly fuse	Requires main decoder inhibiting — extra gate delay
Intel	64k DRAM	I2164	4 spare rows and 4 spare columns	High voltage pulses at wafer sort, poly fuse	Same as above
Mostek	64k DRAM	MK4164	8 spare columns	Laser pulse at wafer sort	
Mostek	64k UVEPROM	MK2764	25% redundant memory Matrix — 2 columns	High voltage(25-V) laser pulse, pulses at wafer sort, poly fuse	
Intel	16k SRAM	I2167	3 spare rows	High voltage pulses at wafer sort, poly fuse	
INMOS	16k SRAM	IMS1400	2 spare columns	High voltage pulses at wafer sort, poly fuses	
INMOS	16k SRAM	IMS1420/1421	8 spare columns	High voltage pulses at wafer sort, poly fuses	
NTT Musashino	4M-byte ROM[a]	NCA	Complete ROM redundancy — four 1M-byte modules		
Intel	32k bipolar PROM	3632	4 spare rows		

Notes:

It is said that redundancy increases the yield by a factor of 56.30, depending on the maturity of the Fab line.

Most magnetic bubble memories also use redundancy to increase manufacturing yields by means of a "boot loop."

[a]See M. Y. Kitano et al, "A 4M-byte Full Wafer ROM," 1980 IEEE ISSCC Digest of Technical Papers, Feb 13-15, 1980.

NCA — Not commercially available

N/A — Not available

commercially obtainable. As Table 2 shows, the INMOS IMS2600 has the fastest speed of all 64k DRAMS (100 ns max), while Texas Instruments (TI) holds the power miser award at 125 mW active and 28 mW standby. The circuit with the smallest die size, and therefore the most potential for lowest manufacturing costs, is National Semiconductor's NMC4164.

...a faulty 64k device can be sold as a 32k DRAM once the faulty cells have been identified and isolated.

The 64k DRAM is upward compatible with the 16k DRAM and encased in the industry standard 16-pin DIP using address multiplexing. In changing from a 3-power supply 16k DRAM to a single 5-V power supply 64k DRAM, pin 1 changes from V_{DD} to either refresh or no connection; pin 8 is the primary power supply (V_{CC}) pin; and pin 9 becomes A7.

At the 64k x 1 DRAM level, devices with onchip redundancy to increase yields and maintain reasonable manufacturing costs are beginning to appear, as predicted in Reference 2. As memory density increases and geometries shrink (via device scaling and circuit innovations), the die size must remain constant for producibility and yield considerations. As such, defect density becomes a much more important factor than with lower density devices since a single defect can wipe out a major section of memory. Process cleanliness becomes more important as well. To offset this, built-in redundancy allows the defective words/bits to be switched out of the memory array and the redundant circuitry to be switched in according to the results of the bit mapping procedure at wafer sort. Table 3 summarizes the memories that currently have a built-in redundant circuitry. The list includes several 16k SRAMs, one ultraviolet erasable programmable read only memory (UVEPROM), a large MOS ROM and a bipolar PROM. Look for this trend to continue and accelerate as higher density memory devices appear. All commercially available magnetic bubble memories also contain redundant circuitry.

Even though the 64k DRAM has a standardized pinout (remember the problems with 4k DRAMs), two other

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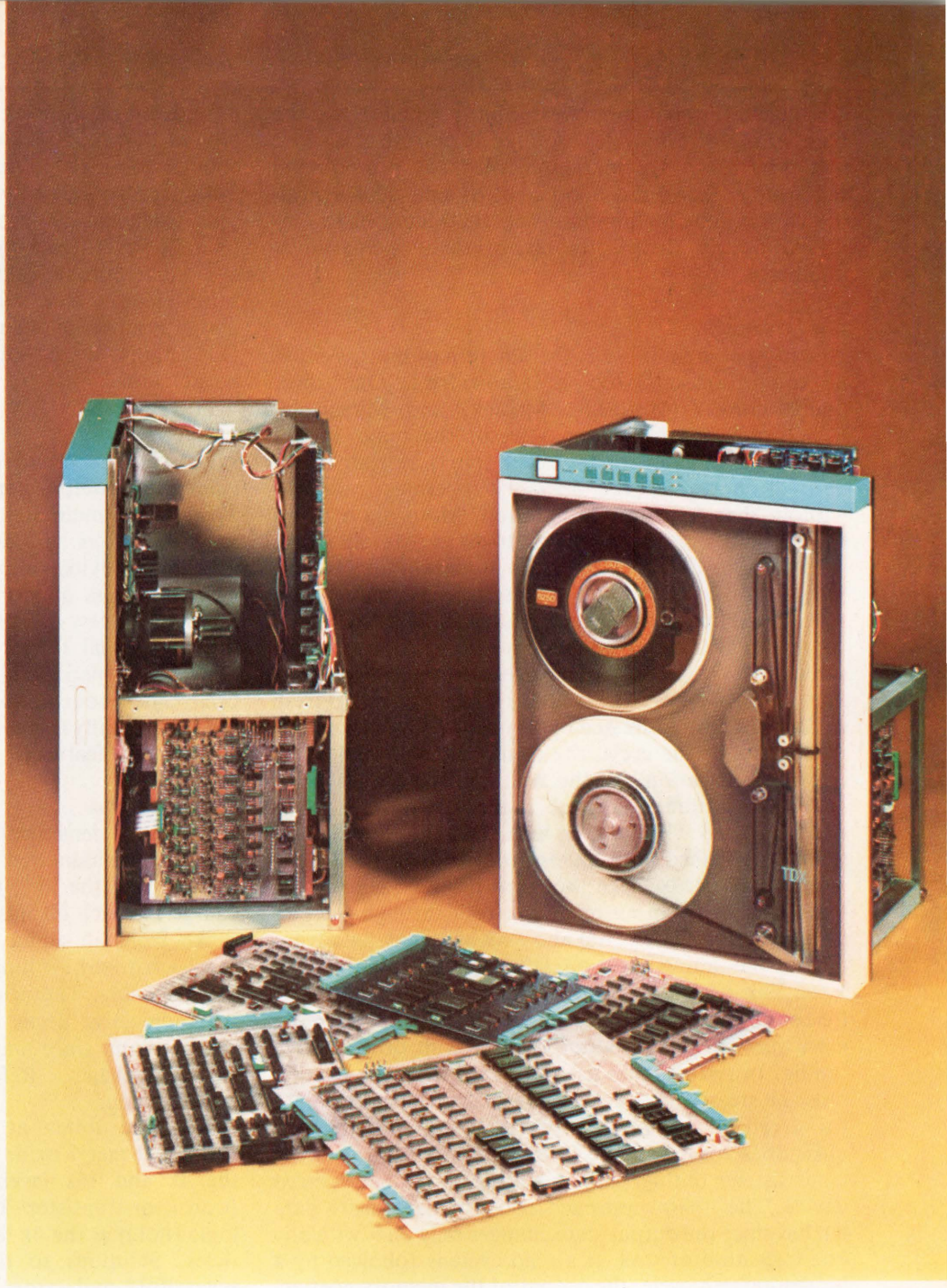

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areas have fostered controversy: pin 1 function and the number of refresh cycles required to refresh the entire memory.[3] Both are marketing ploys or promotional fancy aimed at gaining acceptance of a particular product as the industry standard 64k DRAM and have very little to do with facts or the ease of use of one part over another.

Pin 1 function

As can be seen in Table 2, the function of pin 1 is either no connection or a self- or auto-refresh. Only three manufacturers (Motorola, Mostek, and Mitsubishi) have opted for automatic refresh; the majority has chosen no function on pin 1. If pin 1 refresh is not desired, however, the memory operates normally without that function. In addition, Motorola offers a 64k automatic refresh part (MCM6664) to cover all bases. This part has two onchip refresh modes: automatic and self-refresh. Mostek's 4164 has a self-refresh mode and a special test mode to ensure operation of the internal counter. The self-refresh modes of both devices operate similarly. When row address strobe (RAS) is high, pin 1 must be pulsed low. The memory then executes a refresh cycle at the row addressed by its onchip refresh counter. At the end of the cycle, the counter is incremented by one in preparation for the next refresh cycle. In the MCM6664's automatic refresh mode, the refresh line is double pulsed while RAS is high, and the RAM is continually refreshed until RAS is brought low.

INMOS's IMS2600, even though it has a no connect on pin 1, performs an automatic refresh through the column address strobe (CAS) and RAS lines, taking advantage of the timing edges already available in a dynamic RAM. This design is upward and downward expandable (to the 256k RAM), easy to implement, does not require extra power, and does not conflict with other system timing. In systems that use pin 1 refresh, the RAS pulse must be steered to RAS for a normal cycle and to pin 1 for a refresh cycle. With the INMOS circuit, the RAS pulse does not have to be steered and thus utilizes fewer gates in the timing path, resulting in a higher speed device. The INMOS approach also eliminates extra data latches since the output state changes only once with any one transition of CAS. If a read cycle is followed by a hidden refresh cycle, the output of the memory goes active, reflecting the contents of the addressed cell. CAS can be held low indefinitely, holding the output valid. Since CAS is already low, the only other requirement for refresh is to pulse the RAS line again. When CAS goes high, the output returns to its high impedance state. The IMS2600 RAM functions like any other RAM in systems designed with RAS only refresh or in systems that perform error correction during refresh.

Number of refresh cycles

In addition to the definition of pin 1, the other incompatibility between 64k DRAMs is the number of refresh cycles: 256 refresh cycles over a 4-ms period or 128 cycles over a 2-ms period. The lineup of 128- vs 256-cycle refresh manufacturers is found in Table 2, which shows that the majority has opted for the 128-cycle, 2-ms approach. The key is that neither the 128-cycle, 2-ms part nor the 256-cycle, 4-ms part can be directly plugged into 16k DRAM 3-power-supply sockets (which account for the majority of 16k DRAM sockets) without circuit modification. In addition, refresh circuitry for either type of 64k DRAM is the same, consisting of a clock, a counter, and an address multiplexer. (The 128-cycle, 2-ms part requires only seven of the counter's eight outputs while the 256-cycle, 4-ms part requires all eight bits. However, since counters come with eight bits, this is a moot point.) Thus, the matter of the number of refresh cycles is a subjective decision of the system design engineer and is not based on technological facts. One should not be misled by marketing ploys of the participants.

Timing features

A new feature found with the 64k DRAM is called extended data output control, and is controlled by $\overline{\text{CAS}}$. This feature maintains valid data on the output for as long as 10 μs. In addition, page mode operation (Mostek) provides improved access and cycle times in random access of any column address with a row by strobing the row address into the chip, and maintaining the $\overline{\text{RAS}}$ signal low. Nibble mode operation (INMOS) allows high speed serial access four bits at a time, with cycle time about one-half that of the traditional page mode. Presently there is no industry standard for any of these timing features.

Alpha particles

As memory densities have increased beyond 16k bits, with the attendant new circuit design techniques, device scaling, and the like, the capacitance needed to store charge for each bit has decreased to such a level that a strike from an alpha particle would be sufficient to cause a soft error if it occurred in the cell areas or on the bit/sense line. The primary cause of alpha particles is the radioactive decay of naturally occurring uranium and thorium, trace amounts of which are found in ceramic packages. References 4 and 5 detail this phenomenon.

Dynamic RAMs at the 64k density level, static n-channel metal oxide semiconductor (NMOS) RAMs at the 4k and 16k levels, and, recently, bipolar RAMs [transistor-transistor logic (TTL) and emitter-coupled logic (ECL)] at the 4k level are susceptible to alpha particles. Solutions to the alpha particle problem are severalfold and center on packaging materials, device design, die coatings, and system design techniques. Susceptibility to alpha particles can be decreased by the following specific means.

Packaging: Using cooler packaging material to eliminate as many trace radioactive elements as possible; using plastic packages

Device design/construction: Using an epitaxial layer during device manufacture; increasing memory storage cell capacitance; using metal—not diffused—bit lines; using folded bit lines; minimizing the duration for which the bit lines are floating; using an organic die coat

System design: Incorporating error detection and correction methods

Semiconductor manufacturers are currently using all of these techniques. The following manufacturers of 64k DRAMs are now employing an organic die coat: IBM, Hitachi, Motorola, TI, Toshiba, Mitsubishi, and Fujitsu.

The 256k RAM will be even slower in coming than the 64k version. Even though announced by Nippon

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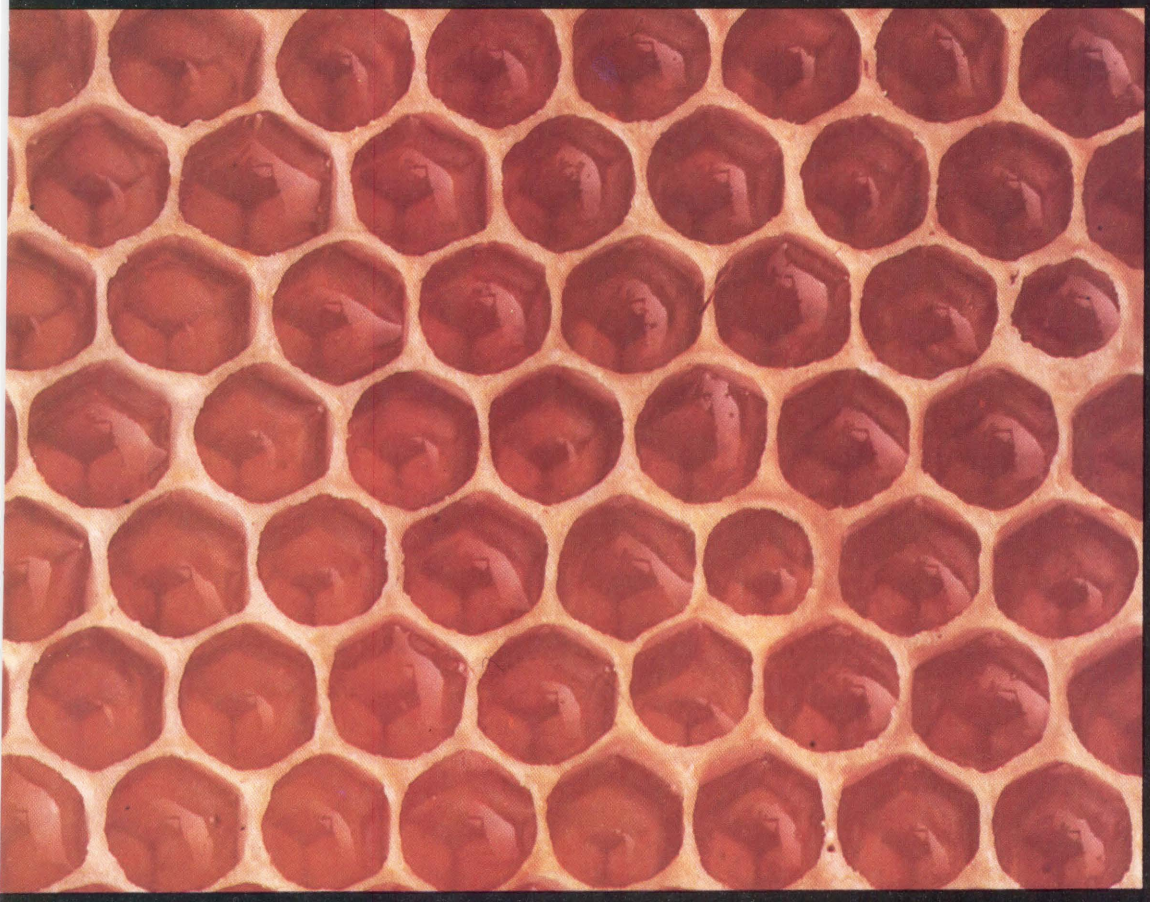

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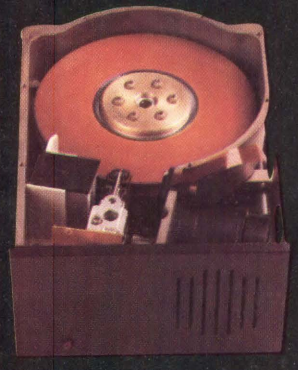

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TABLE 4

Bytewide Dynamic RAMs

Manufacturer	Org	TAA/T Cycle (ns)	PDISS (mW) Active/Standby	Refresh	Die Size (mil^2)	Pkg
TI	8k × 8	100/250	200/NA	128-cycle 2 ms	34,000	16-pin
Hitachi	8k × 8	120/300	170/NA	256-cycle 4 ms	45,003	16-pin

Electric Co (NEC)-Toshiba and the Musashino Laboratory of Nippon Telegraph and Telephone Public Corp (NTT) at the 1980 International Solid State Circuits Conference, and recently by Oki and NEC Semiconductor, the 256k RAM will not be available for several more years, probably not till 1983 or 1984, and even then in sample quantities. The reasons are technologic development, cost and development of line patterning, and placement in production. Production quantities will not be available until the last half of the 1980s.

The aspect ratio (die length/width) will present a problem during attempts to package the 256k DRAM into a 16-pin dual-inline package (DIP). In all probability, it will be encased in a 28- or 32-pin leadless chip carrier (LCC) package. Furthermore, 256k and future generations of RAMs will contain redundant cells for yield improvement, reduction in processing steps to keep costs down, folded bit lines for noise reduction, low resistance silicide for reduced delay, epitaxial layer for alpha particle protection, and direct step on wafer writing or E-beam writing. A deviation from the traditional adherence to by-one output organization for dynamic RAMs—a trend that continues to prevail through the 64k level—may take place soon. Although page mode operation with DRAMs has not been widely used to date, there is a growing use of block transfer of data, particularly in large memory systems.

Bytewide DRAM structure offers simplified bus operation through the use of 3-state data input/output (I/O) lines. However, these lines are complex in design and require more real estate—8 buffers, 8 data latches, and 8 bonding pads—thus deviating from the standard 16-pin DIP package. Also they have longer access times and consume more power (than the by-one organization) but offer greater data throughput since all I/Os are in parallel and have UVEPROM, read only memory (ROM), and EEPROM pin compatibility and interchangeability. As a result, several manufacturers are investigating alternative memory organizations, including a straightforward 8k x 8 structure (Table 4), an onchip cache memory or memories in which page mode is replaced by a successive address mode. At the 256k-bit level, these alternative organizations are even more desirable. Memory systems that can take advantage of these different structures will begin entering the market in the early 1980s.

Japanese DRAM reliability

In late 1978, Hewlett-Packard informed the electronic industry that Japanese 16k DRAMs were of a significantly higher quality than those from U.S. manufacturers. This triggered the heated debate, which still continues today, over Japan's "unfair" competitive advantage. At the heart of the matter are basic differences between the two countries in the following areas: economic and corporate structures, management philosophies, values and work ethics, personnel policies, government protectionist policies, government funding of conglomerate research projects, job mobility, and import-export tariffs. All Japanese semiconductor houses are subsidiaries of computer firms, which also own the lending institutions and support their own subsidiaries first. Moreover, one of Japan's worldwide goals is computer dominance. It will therefore require time and compromises by both countries to resolve these matters to mutual satisfaction. (See References 6, 7, and 8 for further details.)

Several key points must be made. If we unite as manufacturers and address the problem squarely and objectively, instead of resting on our past laurels, we will succeed in competing against the Japanese. U.S. semiconductor manufacturers, by nature, are an innovative group, whereas the Japanese are extremely adept at applying those innovations to quality high volume production. The Japanese are good learners; they obtained most of what they have by observing U.S. manufacturers because of our open policy regarding information transfer and by applying the results to their "system." Both sides have changed; the Japanese are becoming innovative, and we are learning quality from them. And it is paying off.

The quality edge that the Japanese have held for the past 24 months or so for the 16k DRAM (and this is also directly applicable to the 64k DRAM) no longer exists in toto. Independent Test Laboratory results of incoming inspection testing and burn-in of large volumes of 16k DRAMs have shown that several U.S. manufacturers of this device, as of fall 1981, produced devices with quality levels *equivalent* to those of Japanese suppliers. This dramatic turnaround has been due to an enormous concentration of efforts and willingness to learn by many people. However, we cannot become complacent with these preliminary results but must push ahead vigorously with our newly adopted quality plans.

The Japanese are not standing still but are pushing for market domination in the following categories of devices in both the United States and Europe: 64k DRAMs, 2k x 8 SRAMs, complementary metal oxide semiconductor (CMOS) RAMs, EEPROMs, and, to a lesser extent, 16k DRAMs, as well as advanced microprocessors. Moreover, they are active in the research and development of GaAs integrated circuits.

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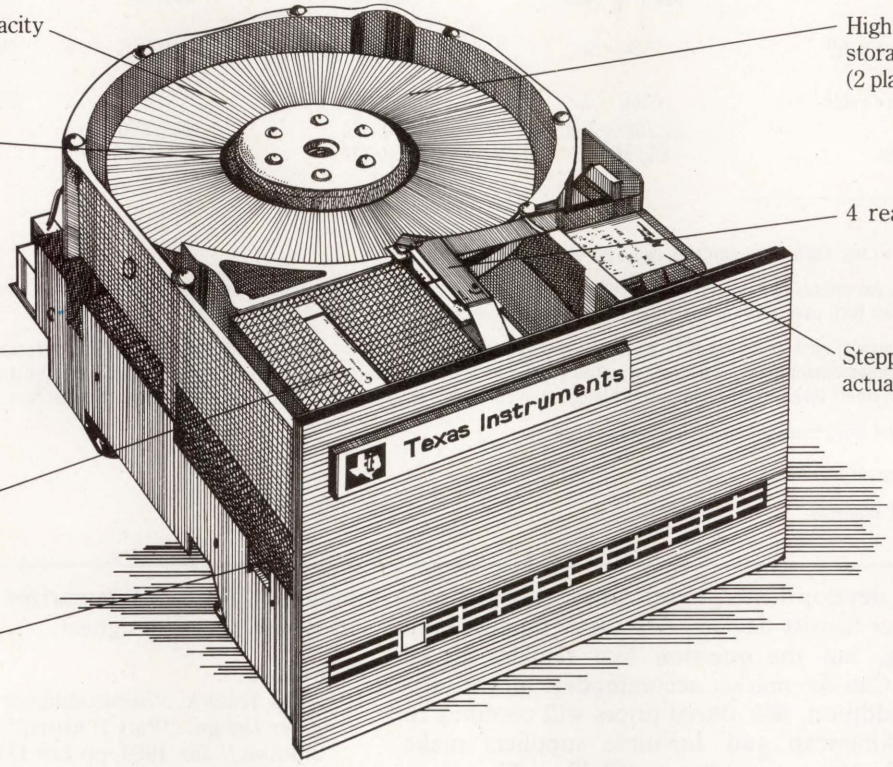

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TABLE 5

New DRAM Developments

Manufacturer	Org (Part No)	TAA/T Cycle (ns)	PDISS (mW) Active/Standby	Refresh	Pkg
Intel	4k × 8	200/400	250/50	128-cycle, 2 ms	28
TI	16k × 4 (TMS4416)	150 (read)/360	125/17.5 (typ)	256-cycle, 4 ms	18
Siemens[b]	256k × 1	N/A	N/A	N/A	18
NEC-Toshiba[a]	256k × 1	160/350	225/25	256-cycle, 4 ms	16
NEC	256k × 1	100/270	300/20	256-cycle, 4 ms	16
NTT Musashino[c]	256k × 1	100/200	230/15	256-cycle, 4 ms	N/A
Oki Electric	256k × 1 (MSM37256)[e]	100/200 (typ)	300/20 (typ)	256-cycle, 4 ms	16
IBM	32k × 9, 288k	800/NA	200/NA	N/A	N/A
Japan's Cooperative Lab[d]	256k × 2	170/NA	N/A	256-cycle, 4 ms	N/A
Japan's Cooperative Lab[d]	256k × 4	170/NA	N/A	256-cycle, 4 ms	N/A
General Automation	32,768 × 4 or 65,536 × 2	150/320 150/320	1848/160 924/160	N/A N/A	28

Notes:

[a] Two 128k arrays; each array contains two 512- × 128-bit sections.

[b] Device has pin swapping mode in which address lines will be expanded to allow 8-bit data transfer; onchip redundancy mode register allows both user and manufacturer to replace bad memory bit with good from a bank of 5120 cells.

[c] Two 128k arrays; each array has a 2k block of redundant cells and a dummy sense circuit. Redundant cells are replaced by electrically programming polysilicon resistors during wafer sort. Devices are built with E-beam direct writing, dry processing, and 3 interconnect levels; molybdenum word lines, aluminum bit lines, and polysilicon are used for storage capacitors.

[d] Experimental using tantalum oxide for storage capacitor.

[e] Pin 1 is designed as A8.

N/A — Not available

share and to develop faster, lower power (high performance), higher density devices. 64k DRAM qualification is continuing, but the question that remains to be answered is, Can the market accommodate all the latecomers? In addition, 64k DRAM prices will continue to decline as American and Japanese suppliers make greater production quantities available. The large market shares will go to suppliers with higher performance parts. In fact, prices have eroded to such an extent that Advanced Micro Devices is seriously considering not participating in the 64k DRAM market. Also, look for nibble (16k x 4) and bytewide (8k x 8) dynamic RAMs to appear on the scene beginning in 1982.

...the Japanese are becoming innovative, and we are learning quality from them.

Work is proceeding at a frantic pace on 256k DRAM development, most suppliers having made several design iterations already. These devices, which should appear in sample quantities in 1983, will make greater use of vertical structures, metal silicides, and redundancy to achieve high performance operation and yet be producible (provide a reasonable yield). Also look for CMOS to be a prime technology for 1M-bit and larger DRAMs (as well as for all memory types) for reasons of high performance, reduced noise disturbance, and alpha particle immunity. Table 5 summarizes the development efforts of dynamic RAM designers.

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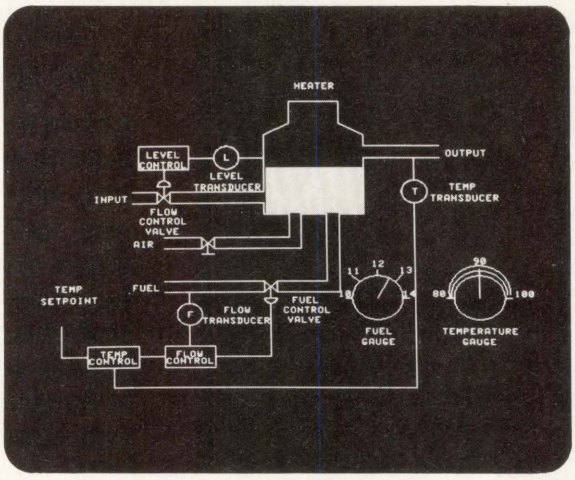

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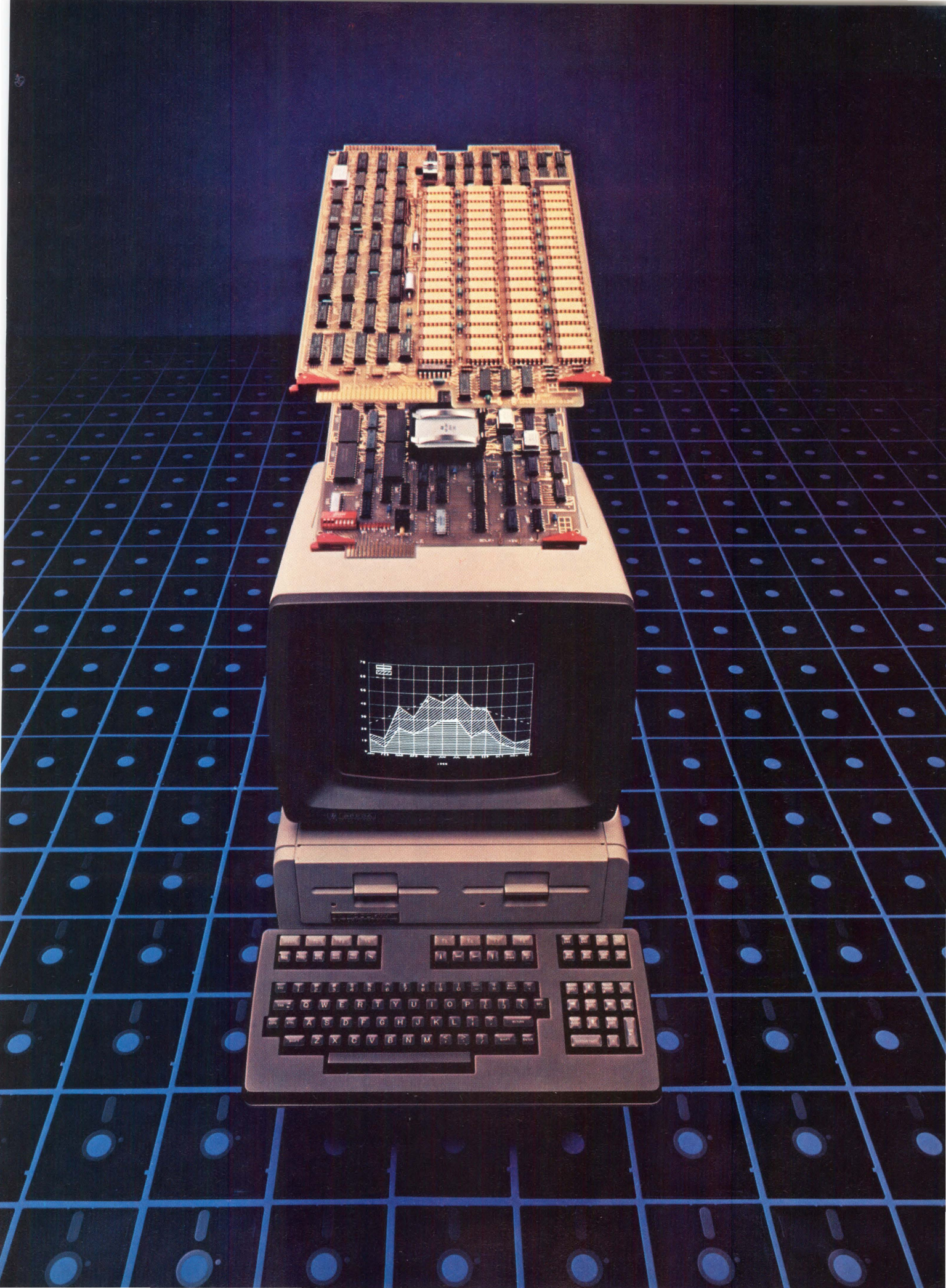

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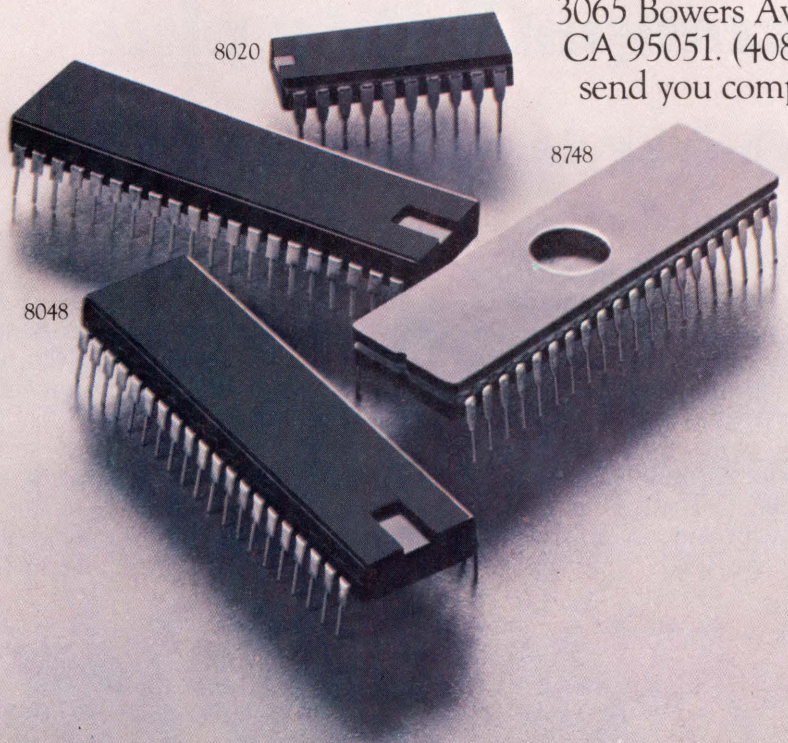

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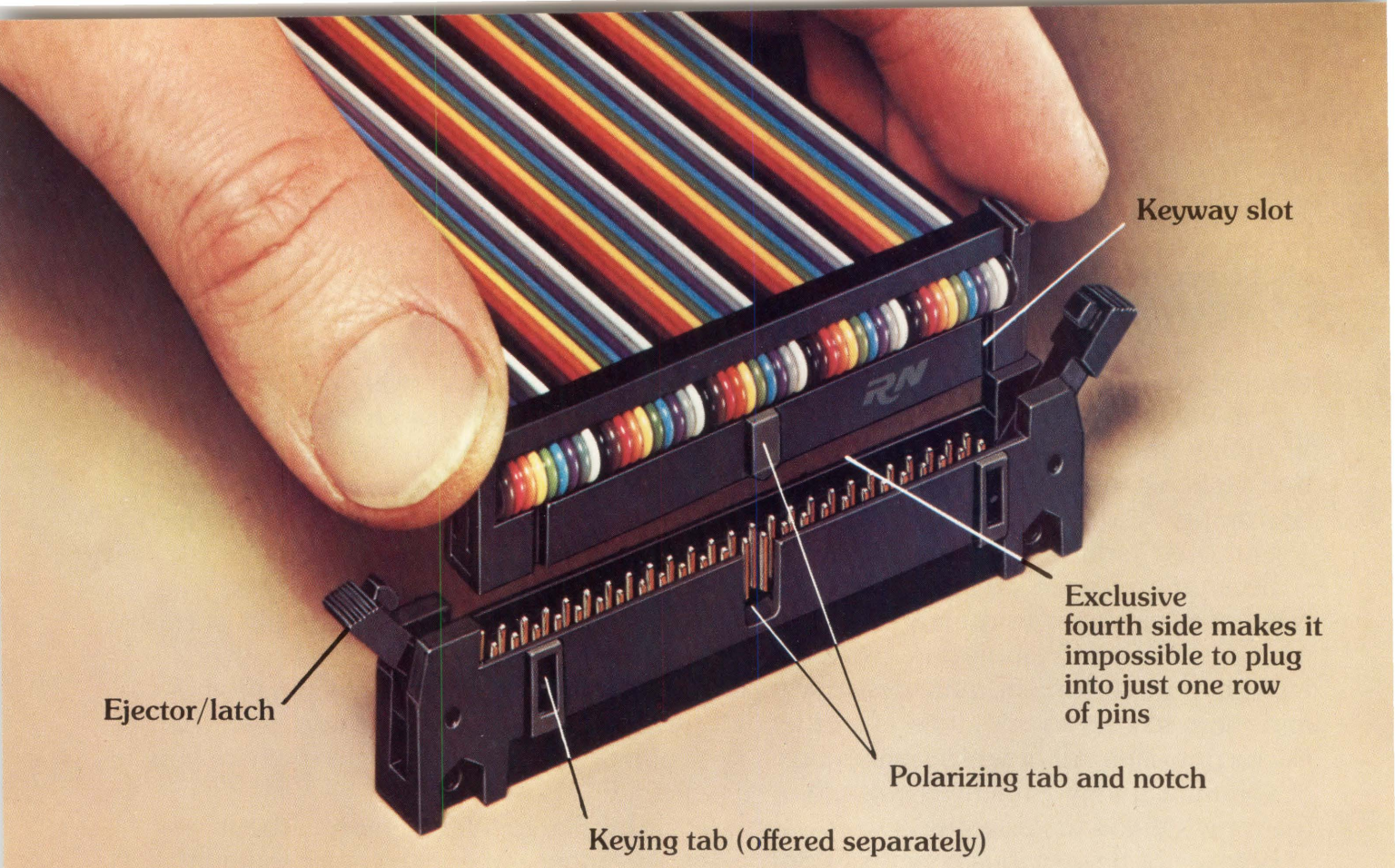

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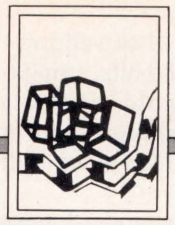

SIMPLIFICATION OF 2-BIT ERROR CORRECTION

Bit by bit, errors can be detected and eliminated through the use of an error matrix

by Bob Nelson

A computer-generated code, which generally obeys the rules attributed to the Hamming code and many of its variations, can be used to extend error detection and error correcting efficiency in an error checking and correction system. Such a code has been implemented by National Semiconductor on the DP8400, an expandable error checking and correction device packaged in a 48-pin dual inline package. The DP8400 can be used in a minimum hardware implementation of a 2-bit error correction system which will serve as an introduction to the rotational syndrome word generator, and also lead the way to expanding the error correcting capabilities even further.

Syndrome words

The code used in an error checking and correction (ECC) system designed to correct 1-bit errors and detect 2-bit errors for 16-bit data words may be viewed as a 16 x 6 matrix (Fig 1). The matrix describes the error locations and the syndrome bit positions so that the upper left bit of the matrix defines the least significant bit (LSB) for both the error locations and the syndrome bit locations. Each vertical column of the matrix contains the syndrome word (syndrome bits) for that error location in the data word. For any number of errors, the syndrome word generated by presenting the data word to the matrix is the exclusive OR (XOR) of the syndrome words defined by the error positions. To correct an error, the location of the error must be uniquely identified, and thus the 16 vertical columns must each be unique. A modified Hamming code generates a unique syndrome word for every possible data bit error location and hence may be referred to as a syndrome word generator.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code. By ensuring that the syndrome words (vertical columns in the matrix) contain either three or five 1s, all applicable error conditions may be defined by counting the syndromes. The absence of a syndrome (ie, a syndrome containing all 0s and no 1s) indicates no error; an odd number greater than one (3 or 5 in this case) defines the location of a single-bit error. Any simultaneous double error will provide a syndrome word containing an even number of 1s greater than zero, while a single 1 in the syndrome word is indicative of a failure in the check bit portion of memory.

The rotational syndrome word generator described here also contains an odd number of 1s in each syndrome word. One additional characteristic common to both the Hamming code and most of its modified versions is that byte parity is an integral part of the matrix itself. However, the code implemented in the DP8400 ECC device and discussed here does not consider byte parity, or word parity, as a part of the code itself.

A 2-bit error correction system may be implemented in either of two ways. A code designed to allow 2-bit error correction may be used, or an existing single-bit error correct code may be extended by adding a second, different code which will ensure that each syndrome

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											1	1	1	1	1	1		
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5		
LSB	←						error locations									→	MSB	
	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	LSB	0
	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	|	1
	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	syndrome	2
	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	words	3
	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	|	4
	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	MSB	5

Fig 1 DP8400 generates unique syndrome word to indicate single-bit error position. Generated syndrome word containing all 0s means there is no error in data word.

word generated for any two error locations will be unique. Thus, a secondary, and different, 16 x 6 matrix connected to the primary matrix to form a 16 x 12 matrix will allow double-bit error correction if the XOR of the two 12-bit syndrome words produces a unique word for any two error locations.

Second matrix

The definition of an ECC matrix requires specifying a correspondence between error locations and syndrome words that defines the error location for each set of single-error syndromes. If a matrix is resequenced such that any error location corresponds to a syndrome word different from the original (primary) matrix, a second matrix has been created. For a 16-bit ECC matrix, 16!, or 2.092279 x 10^13, different codes exist. If a second code exists such that when it is combined with the first code (each containing the same syndrome words, but in a different sequence), a unique, larger syndrome word is generated for any two error locations, then an expandable code has been created (Fig 2).

The matrix, or code, used in the DP8400 device is defined such that if a second matrix, identical to the first but shifted by one bit position, is combined with the first, it would form just such a larger matrix. This matrix is fully rotational in that the secondary matrix need only be rotated, or shifted one error bit position to the left or right with respect to the primary matrix, to form larger, unique syndrome words regardless of the assigned correspondence of the primary matrix.

											1	1	1	1	1	1		
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5		
LSB	←						error locations									→	MSB	
	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	LSB	0
	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	|	1
	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	|	2
	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	|	3
	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	|	4
	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	syndrome	5
	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	words	6
	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	0	|	7
	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	1	|	8
	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	|	9
	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	|	10
	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	MSB	11

Fig 2 Code in DP8400 can be expanded by adding second device with code shifted by one bit position. Note that bottom six bits of each column are identical to top six bits in column to immediate right.

Implementation of this code in the DP8400 allows the data word size to be extended beyond 80 bits, using one device for each additional 16-bit word or portion thereof. The code function as a rotational syndrome word generator exists for all these defined word widths (Fig 3).

In addition to the rotational syndrome word generator, the DP8400 has two important features that permit an easy implementation of a 2-bit error correction system. During a memory read, the error indicating syndromes can be accessed directly by outputting them to the syndrome input/output (I/O) ports; syndrome can also be presented to the syndrome I/O ports to be XORed with the internally generated syndromes inside the DP8400. The internal syndrome decoder is provided with the result.

Error locations ⟶ 0 and 1
produce
HEX syndrome word ⟶ E34 (+) A78 = 44C
but
Error locations ⟶ 2 and 4
produce
HEX syndrome word ⟶ 1E9 (+) C65 = D8C

Fig 3 Unique syndrome is produced for each pair of error locations which is XOR of the locations. That syndrome can be decoded to identify pair in error.

If, for example, the internally generated 2-bit error syndromes are XORed with externally provided syndromes, representing one of the bits in error, the resulting syndromes representing the unknown error will be presented to the internal syndrome decoder. Once the unknown error is corrected, the data can be output to the data bus. The apparently correct data return zero syndromes (those containing all 0s) which, when XORed with the syndromes being injected, produce the syndromes representing the unknown error and present them to the syndrome decoder. This second error can then be corrected.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code.

As described, the DP8400 is implemented for a 16-bit system. This "primary" ECC device will provide at its syndrome I/O pins the primary, or least significant six, syndrome bits of an extended matrix ECC system. A "secondary" ECC device is interfaced to the memory system with the data pin-to-system data bit correspondence rotated by one bit position, thus producing the extended matrix just described. The second device requires a second set of check bits; these secondary, or most significant six, syndrome bits are provided by the second DP8400.

The resulting 12-bit syndrome word can be externally decoded to provide the syndromes to be injected to effect 2-bit error correction. In system use, the externally decoded syndromes will be stored in a register. After the syndrome I/O port of the primary ECC device has been "turned around," the register outputs are enabled to allow syndrome injection.

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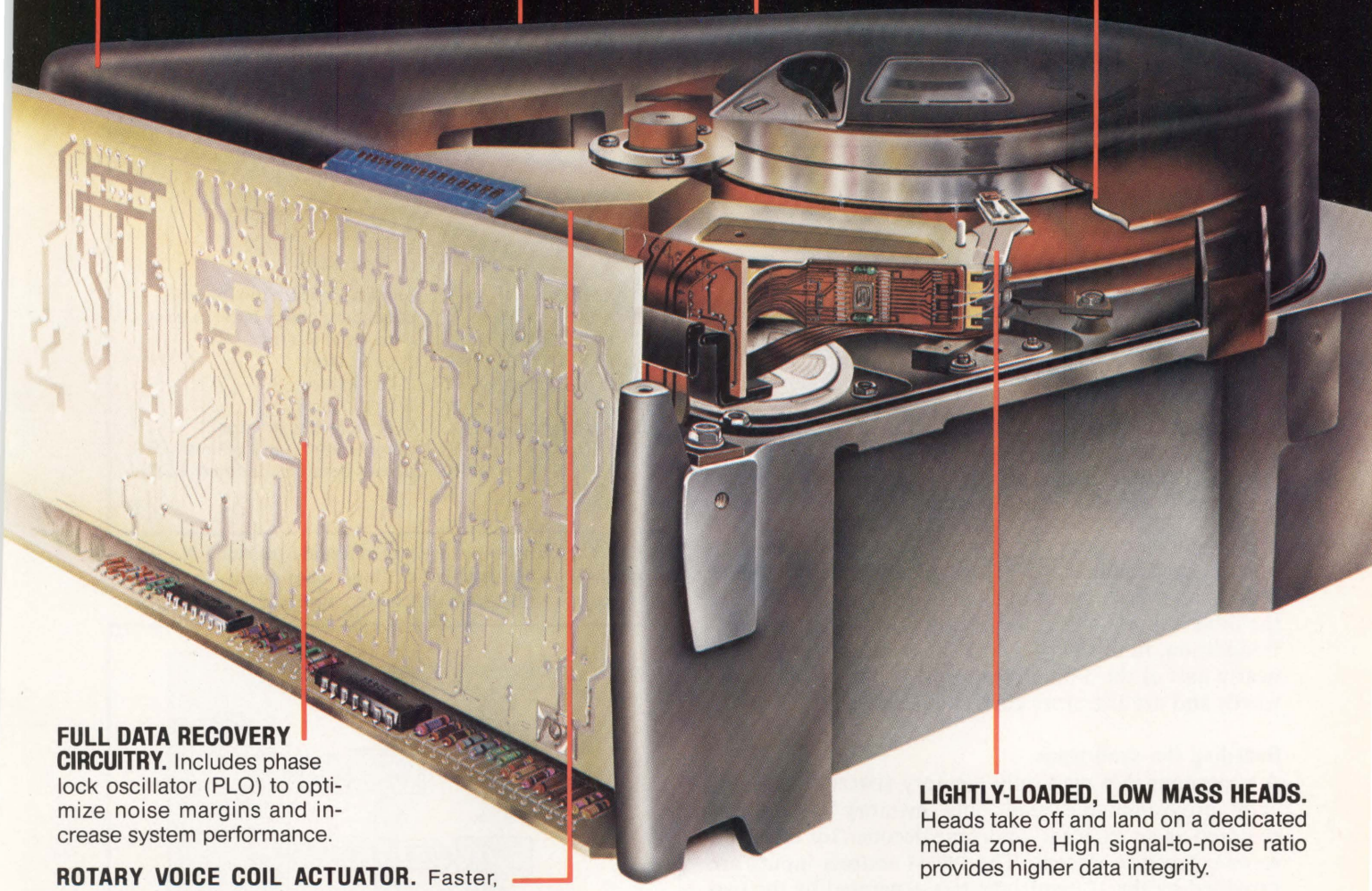

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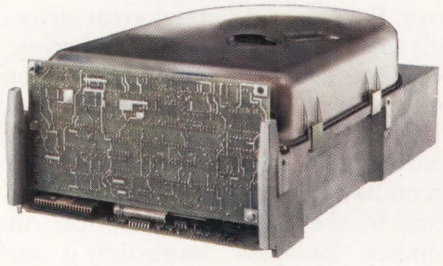

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Each of the DP8400 devices provides a set of error flags. Since each device maintains an independent check bit field in memory, errors occurring within a given check bit field are easily and quickly determined. If the errors, regardless of number, are confined solely to the check bit field of one of the devices, a no-error condition will be indicated.

The syndrome word generated by this system is unique for any combination of 2-bit data errors; both devices see an even number, greater than zero, of 1s in the syndrome word (Fig 4). For 2-bit errors involving one data bit and one check bit in either the primary or secondary check bit fields, the DP8400s report an even, greater than zero, and odd number of 1s in the syndromes; again, the syndromes are unique. The remaining type of 2-bit error, that in which both errors occur in either the

Location/Error			Syndromes		Location/Error			Syndromes	
Data	Sec	Prim	Sec	Prim	Data	Sec	Prim	Sec	Prim
2	0	0	even	even	1	0	1	odd	even
1	1	1	even	even	2	1	0	odd	even
1	0	0	odd	odd	0	1	2	odd	even
0	1	1	odd	odd	1	1	0	even	odd
3	0	0	odd	odd	2	0	1	even	odd
1	0	2	odd	odd	0	2	1	even	odd
1	2	0	odd	odd					

Fig 4 Number and type of errors can be determined by looking at combination of even or odd numbers of 1s in the primary and secondary check bit fields.

primary or secondary check bit fields, produces its own unique syndrome word. However, since one DP8400 reports an even number of 1s in its syndrome word and the other reports all 0s, the data are known to be valid. In addition, in this particular 2-bit error correct system, nearly half of the 3-bit errors result in unique syndrome words and are therefore correctable as well.

Decoding the syndromes

A programmable read only memory (PROM) or electrically programmable read only memory (EPROM) is required as an external syndrome decoder for this 2-bit error correction system. The PROM address inputs are provided by the 12 syndrome bits generated by the two ECC devices. The least significant six bits of the PROM output byte provide, when required, the syndrome bits for subsequent injection into the primary DP8400. The remaining two bits of the PROM output byte provide flags defining the type of error and the contents of the six LSBs of the PROM output byte [Fig 5(a)].

The DP8400's error flags provide initial error determination; if an error that is not a single-bit error occurs, the external syndrome decoder will provide further error determination. Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors. An example of such an error is one with a data bit and a secondary check bit in error. This type of error is corrected by the primary ECC device. An error type that requires "one-pass" correction is one with two data bits in error. In this case, syndromes representing a known error are injected into the DP8400, allowing correction of the unknown error. The remaining single error is then corrected.

The remaining error type, the "two-pass" error, can sometimes be a correctable 3-bit error. The syndromes representing a 2-bit error condition are injected, allowing correction of one error. The remaining 2-bit error produces a new set of syndromes which requires external (second-pass) decoding to produce a set of

(continued on page 136)

MSB 7	6	5	4	3	2	1	LSB 0	
0	0	X	X	X	X	X	X	1 pass correctable
0	1	X	X	X	X	X	X	2 pass correctable
0	X	X	X	X	X	X	X	bits 0 to 5 = syndromes
1	0	X	X	X	X	X	X	not correctable
1	1	X	X	X	X	X	X	0 pass correctable
1	X	X	X	X	X	X	X	bits 0 to 5 < > syndromes

(a)

MSB 7	6	5	4	3	2	1	LSB 0	
1	X	X	X	X	X	X	1	primary check bit(s) in error
1	X	X	X	X	X	1	X	secondary check bit(s) in error
1	X	X	X	X	1	X	X	data bit(s) in error
1	X	X	0	0	X	X	X	1 bit in error
1	X	X	0	1	X	X	X	2 bits in error
1	X	X	1	0	X	X	X	3 bits in error
1	X	X	1	1	X	X	X	4 or more bits in error
1	1	0	X	X	X	X	X	output data from secondary ECC
1	1	1	X	X	X	X	X	output data from primary ECC

(b)

Fig 5 When a PROM is used as external syndrome decoder, its output byte can supply additional data about the error and how it is to be most efficiently corrected.

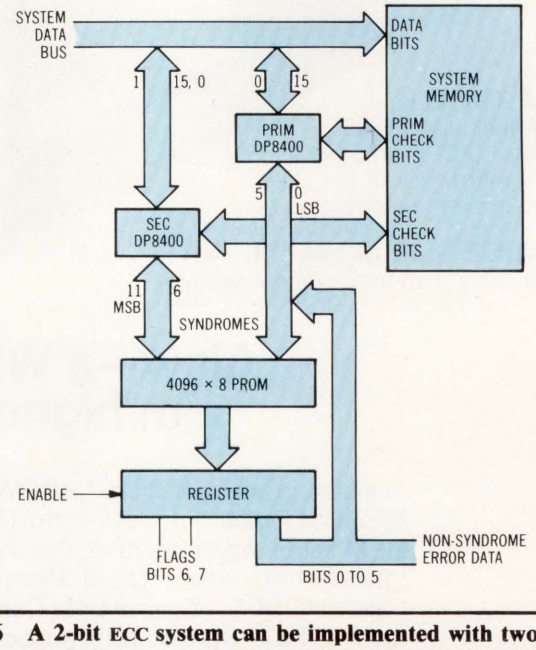

Fig 6 A 2-bit ECC system can be implemented with two DP8400s, a 4k-byte PROM for external syndrome decoding, and a register for temporary storage of syndromes error data. Note that the altered sequence of the lines from the secondary DP8400 reflects the bit rotation needed to expand the unique matrix.

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```
3000 '*************************************************************************
3010 '***     'DC16AROM.BAS'        Bob Nelson - Sunnyvale CA - 9/15/81     ***
3020 '***     This program generates the syndrome decoder ROM code  for     ***
3030 '***     use in implementing a primary syndrome injection two  bit     ***
3040 '***     correction code generated by a single bit left   rotation     ***
3050 '***     of the secondary matrix.      The primary is a  Rotational     ***
3060 '***     Syndrome Generator as defined by National   Semiconductor     ***
3070 '***     in the DP8400.  The LPRINT routine may be replaced with a     ***
3080 '***     FILE generator or OUTP routine to facilitate the use of a     ***
3090 '***     PROM/EPROM programmer.....................................     ***
3100 '*************************************************************************
3110 '
3120 DEFINT A-Z:DIM SYND(16), PRI(16), ROM(4096,1)
3130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
3140 NEXT:SYND(15)=B*64+A:PRI(15)=D
3150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
3160 ROM(0,1)=224:FOR A=1 TO 4095:ROM(A,1)=184:NEXT
3170 FOR A=0 TO 13:FOR B=A+1 TO 14:FOR C=B+1 TO 15                  '300 - 560
3180 AD=SYND(A) XOR SYND(B) XOR SYND(C):AE=PRI(A) XOR PRI(B)
3190 IF ROM(AD,1)=184 THEN ROM(AD,1)=AE+64 ELSE ROM(AD,1)=183
3200 NEXT:NEXT:NEXT
3210 FOR A=0 TO 14:FOR B=A+1 TO 15                                  '200 - 120
3220 AD=SYND(A) XOR SYND(B):ROM(AD,1)=PRI(A)
3230 FOR C=0 TO 5:P=2^C                                             '201 - 720
3240 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3250 IF (PRI(A) AND P)=0 THEN AF=PRI(A)+P+64 ELSE AF=PRI(A)-P+64
3260 IF ROM(AE,1)=184 THEN ROM(AE,1)=AF ELSE ROM(AE,1)=183
3270 NEXT
3280 FOR C=0 TO 5:S=64*2^C                                          '210 - 720
3290 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3300 IF ROM(AE,1)=184 THEN ROM(AE,1)=PRI(A) ELSE ROM(AE,1)=183
3310 NEXT:NEXT:NEXT
3320 FOR A=0 TO 15:AD=SYND(A):ROM(AD,1)=228                         '100 -  16
3330 FOR B=0 TO 5:P=2^B                                             '101 -  96
3340 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3350 ROM(AE,1)=205
3360 FOR C=B+1 TO 5:P=2^C                                           '102 - 240
3370 IF (AE AND P)=0 THEN AF=AE+P ELSE AF=AE-P
3380 IF ROM(AF,1)=184 THEN ROM(AF,1)=213 ELSE ROM(AF,1)=183
3390 NEXT:NEXT
3400 FOR B=0 TO 5:S=64*2^B                                          '110 -  96
3410 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3420 ROM(AE,1)=238
3430 FOR C=B+1 TO 5:S=64*2^C                                        '120 - 240
3340 IF (AE AND S)=0 THEN AF=AE+S ELSE AF=AE-S
3450 IF ROM(AF,1)=184 THEN ROM(AF,1)=245 ELSE ROM(AF,1)=183
3460 NEXT:NEXT
3470 FOR B=0 TO 5:P=2^B:FOR C=0 TO 5:S=64*2^C                       '111 - 596
3480 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3490 IF (AD AND S)=0 THEN AE=AE+S ELSE AE=AE-S
3500 FOR D=0 TO 5:E=2^D
3510 IF ROM(AE,1)=D THEN ROM(AE,1)=183:GOTO 3540
3520 IF ROM(AE,1)=184 THEN ROM(AE,1)=P
3530 NEXT D
3540 NEXT C:NEXT B:NEXT A
3550 FOR A=0 TO 5:FOR B=0 TO 5                                      '011 -  36
3560 AD=2^A+64*2^B:ROM(AD,1)=235
3570 FOR C=A+1 TO 5:AE=AD+2^C                                       '012 -  90
3580 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3590 NEXT
3600 FOR C=B+1 TO 5:AE=AD+64*2^C                                    '021 -  90
3610 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3620 NEXT:NEXT:NEXT
3630 FOR A=0 TO 5:AD=2^A:ROM(AD,1)=225                              '001 -   6
3640 FOR B=A+1 TO 5:AE=AD+2^B:ROM(AE,1)=233                         '002 -  15
3650 FOR C=B+1 TO 5:AF=AE+2^C                                       '003 -  20
3660 IF ROM(AF,1)=184 THEN ROM(AF,1)=241
3670 NEXT:NEXT:NEXT
3680 FOR A=0 TO 5:AD=64*2^A:ROM(AD,1)=226                           '010 -   6
3690 FOR B=A+1 TO 5:AE=AD+64*2^B:ROM(AE,1)=234                      '020 -  15
3700 FOR C=B+1 TO 5:AF=AE+64*2^C                                    '030 -  20
3710 IF ROM(AF,1)=184 THEN ROM(AF,1)=242
3720 NEXT:NEXT:NEXT
3730 B=0:C=0:FOR A=0 TO 4095:H$=HEX$(ROM(A,1)):       'LPRINT ARRAY
3740 B=B+1:C=C+1:IF LEN(H$)=1 THEN H$="0"+H$
3750 LPRINT USING "\   \";H$;:IF C<>16 THEN 3770
3760 C=0:LPRINT"  ";HEX$(A)
3770 IF B<>256 THEN 3790
3780 B=0:LPRINT:LPRINT
3790 NEXT
```

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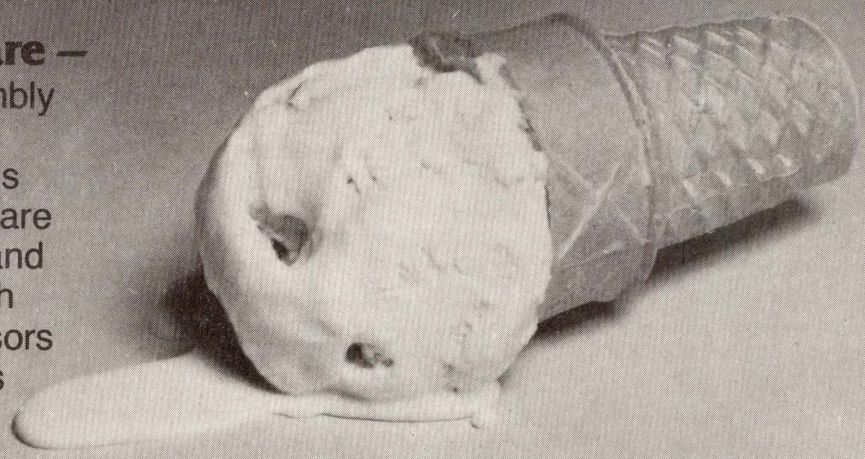

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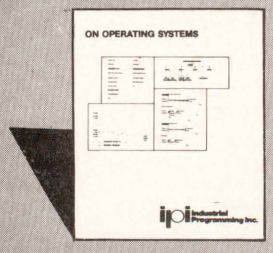

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IPI-1

CIRCLE 77 ON INQUIRY CARD

```
1000 '*************************************************************************
1010 '***    'DC16AMAP.BAS'       Bob Nelson - Sunnyvale CA - 9/15/81     ***
1020 '***    This program generates the syndrome maps for  a  primary     ***
1030 '***    syndrome injection implementation of a 16 bit  word  two     ***
1040 '***    bit error correct system utilizing a Rotational Syndrome     ***
1050 '***    Word Generator as implemented in the DP8400 by  National     ***
1060 '***    Semiconductor.   These maps are based on single bit left     ***
1070 '***    rotation of the secondary matrix.  The 'c' and 'd' notes     ***
1080 '***    in the maps denote  non-correctable  and  non-detectable     ***
1090 '***    three bit error conditions.............................      ***
1100 '*************************************************************************
1110 '
1120 DEFINT A-Z:DIM SYND(16),PRI(16),ROM(1132,1):P$="PRIMARY":S$="SECONDARY"
1130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
1140 NEXT:SYND(15)=B*64+A:PRI(15)=D
1150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
1160 LPRINT "ONE DATA ERROR SYNDROME MAP":LPRINT
1170 FOR A=0 TO 15:LPRINT USING"##";A;:LPRINT"  ";:NEXT:LPRINT:LPRINT
1180 FOR A=0 TO 15:LPRINT HEX$(SYND(A));" ";:NEXT:LPRINT
1190 FOR A=1 TO 4:LPRINT:NEXT
1200 LPRINT"TWO DATA ERROR CORRECT SYNDROME MAP":LPRINT
1210 FOR A=1 TO 15:LPRINT USING"##";A;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1220 FOR A=0 TO 14:FOR B=A+1 TO 15:AD=SYND(A) XOR SYND(B)          '200 - 120
1230 ROM(X,1)=AD:H$=HEX$(AD):IF LEN(H$)=2 THEN H$="0"+H$
1240 LPRINT H$;"  ";:X=X+1:NEXT B:LPRINT USING"###";A
1250 LPRINT TAB((A+1)*5+1);:NEXT A:FOR A=1 TO 4:LPRINT:NEXT
1260 FOR A=0 TO 5:S=64*2^A:FOR B=0 TO 5:P=2^B:FOR C=0  TO 15       '111 - 576
1270 AD=SYND(C):IF (AD AND P)=0 THEN AD=AD+P ELSE AD=AD-P
1280 IF (AD AND S)=0 THEN AD=AD+S ELSE AD=AD-S
1290 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT:A$=" "
1300 LPRINT"ONE DATA, ONE PRI, ONE SEC CHECK ERROR SYNDROME MAPS":LPRINT
1310 LPRINT:X=120:FOR A=0 TO 5:LPRINT"SECONDARY CHECK BIT";A:LPRINT
1320 FOR F=0 TO 15:LPRINT USING"##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1330 FOR B=0 TO 5:FOR C=0 TO 15:FOR E=0 TO 119
1340 IF ROM(E,1)=ROM(X,1) THEN A$="d":E0=E0+1:GOTO 1370 ELSE NEXT E
1350 FOR D=120 TO 695:IF D=X THEN D=D+1
1360 IF ROM(D,1)=ROM(X,1) THEN A$="c":E2=E2+1 ELSE NEXT D
1370 H$=HEX$ (ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1380 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING"####";B
1390 NEXT B:LPRINT:LPRINT:NEXT A
1400 LPRINT"576 ONE DATA, ONE PRI, ONE SEC CHECK errors are possible."
1410 LPRINT E0;"TWO DATA errors are not detectable.":LPRINT E2;
1420 LPRINT "ONE DATA, ONE PRI, ONE SEC CHECK errors are not correctable."
1430 LPRINT 100*((576-E0)/576):"PERCENT DETECT - ";
1440 LPRINT 100*((576-E0-E2)/576;"PERCENT CORRECT"
1450 FOR A=1 TO 4:LPRINT:NEXT:EA=E0:E0=0:EC=E2:E2=0
1460 X=0:FOR A=0 TO 15:AD=SYND(A):ROM(X,1)=AD:X=X+1:NEXT           '100 -  16
1470 FOR A=0 TO 5:P=2^A:FOR B=0 TO 5:S=64*2^B                      '011 -  36
1480 AD=P+S:ROM(X,1)=AD:X=X+1:NEXT:NEXT
1490 FOR A=0 TO 15:FOR B=A+1 TO 15:FOR C=B+1 TO 15                 '300 - 560
1500 AD=SYND(A) XOR SYND(B) XOR SYND(C)
1510 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1520 FOR A=0 TO 5:P0=2^A:FOR B=A+1 TO 5:P1=2^B                     '102 - 240
1530 FOR C=0 TO 15:AD=SYND(C):IF (AD AND P0)=0 THEN AD=AD+P0 ELSE AD=AD-P0
1540 IF (AD AND P1)=0 THEN AD=AD+P1 ELSE AD=AD-P1
1550 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1560 FOR A=0 TO 5:S0=64*2^A:FOR B=A+1 TO 5:S1=64*2^B               '120 - 240
1570 FOR C=0 TO 15:AD=SYND(C):IF (AD AND S0)=0 THEN AD=AD+S0 ELSE AD=AD-S0
1580 IF (AD AND S1)=0 THEN AD=AD+S1 ELSE AD=AD-S1
1590 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1600 LPRINT"THERE DATA BIT ERROR SYNDROME MAPS":LPRINT:LPRINT
1610 X=52:A$="  ":FOR A=0 TO 13:LPRINT"DATA bit";A:LPRINT
1620 FOR D=A+2 TO 15:LPRINT USING"##";D;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1630 FOR B=A+1 TO 14:FOR C=B+1 TO 15:FOR E=16 TO 51
1640 IF ROM(E,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 1690 ELSE NEXT E
1650 FOR F=612 TO 1091
1660 IF ROM(F,1)=ROM(X,1) THEN A$="c ":E1=E1+1:GOTO 1690 ELSE NEXT F
1670 FOR G=52 TO 611:IF G=X THEN G=G+1
1680 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1 ELSE NEXT G
1690 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1700 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING "###";B
1710 LPRINT TAB((B-A)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
1720 LPRINT"560 THREE DATA BIT errors are possible.":LPRINT E0;
1730 LPRINT"ONE PRI, ONE SEC CHECK errors are not detectable.":LPRINT E1;
1740 LPRINT"ONE DATA, TWO PRI or TWO SEC CHECK errors are not correctable."
1750 LPRINT E2;"THREE DATA BIT errors are not correctable."
1760 LPRINT 100*((560-E0)/560);"PERCENT DETECT - ";
1770 LPRINT 100*((560-E0-E1-E2)/560);"PERCENT CORRECT"
1780 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC=EC+EC+E2
1790 LPRINT"ONE DATA, TWO PRIMARY CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
1800 A$=" ":E0=0:E1=0:E2=0:FOR A=0 TO 4:LPRINT"PRIMARY check bit";A:LPRINT
1810 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1820 FOR B=A+1 TO 5:FOR C=0 TO 15:FOR E=852 TO 1091
```

```
1830 FOR F=52 TO 611
1840 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 1860 ELSE NEXT F
1850 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1-E1+1 ELSE NEXT E
1860 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1870 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
1880 NEXT B:LPRINT:LPRINT:NEXT A
1890 LPRINT"240 ONE DATA, TWO PRIMARY CHECK errors are possible."
1900 LPRINT E1;"ONE DATA, TWO SECONDARY CHECK errors are not correctable."
1910 LPRINT E2;"THREE DATA BIT errors are not correctable."
1920 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
1930 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:E1=0:E2=0
1940 LPRINT"ONE DATA, TWO SECONDARY CHECK ERROR SYNDROME MAPS":LPRINT
1950 LPRINT:FOR A=0 TO 4:LPRINT"SECONDARY check bit";A:LPRINT
1960 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1970 FOR B=A+1 TO 5:FOR C=6 TO 15:FOR E=612 TO 851
1980 FOR F=52 TO 611
1990 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 2010 ELSE NEXT F
2000 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1=E1+1 ELSE NEXT E
2010 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2020 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
2030 NEXT B:LPRINT:LPRINT:NEXT A
2040 LPRINT"240 ONE DATA, TWO SECONDARY CHECK errors are possible."
2050 LPRINT E1;"ONE DATA, TWO PRIMARY CHECK errors are not correctable."
2060 LPRINT E2;"THREE DATA BIT errors are not correctable."
2070 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
2080 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:A$="  ":C0=1:C1=64
2090 IF W=1 THEN P$="SECONDARY":S$="PRIMARY":C0=64:C1=1
2100 X=0:FOR A=0 TO 15:AD=SYND(A):FOR B=0 TO 5:P=C0*2^B        '101/110 -  96
2105 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
2110 ROM(X,1)=AE:X=X+1:NEXT B:NEXT A
2120 FOR A=0 TO 5:S=C1*2^A:FOR B=0 TO 15:FOR C=B+1 TO 15       '210/201 - 720
2130 AD=SYND(B) XOR SYND(C):IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
2140 ROM(X,1)=AE:X=X+1:NEXT C:NEXT B:NEXT A
2150 FOR A=0 TO 5:AD=C1*2^A:FOR B=0 TO 4:AE=AD+C0*2^B          '012/021 -  90
2160 FOR C=B+1 TO 5:ROM(X,1)=AE+C0*2^C:X=X+1:NEXT:NEXT:NEXT
2170 A$="  ":LPRINT"TWO DATA, ONE ";:LPRINT S$;
2180 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2190 X=96:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2200 LPRINT" check bit";A:LPRINT
2210 FOR F=1 TO 15:LPRINT USING"##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2220 FOR B=0 TO 14:FOR C=B+1 TO 15;FOR D=0 TO 95
2230 IF ROM(D,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 2280 ELSE NEXT D
2240 FOR G=96 TO 815:IF G=X THEN G=G+1
2250 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1:GOTO 2280 ELSE NEXT G
2260 FOR E=816 TO 905
2270 IF ROM(E,1)=ROM(X,1) THEN A$="c ":E1+E1+1 ELSE NEXT E
2280 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2290 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"####";B
2300 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
2310 LPRINT"720 TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2320 LPRINT" CHECK errors are possible."
2330 LPRINT E0;"ONE DATA, ONE ";:LPRINT MID$(P$,1,3);
2340 LPRINT" CHECK errors are not detectable.":LPRINT E1;"TWO ";
2350 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2360 LPRINT" CHECK errors are not correctable."
2370 LPRINT E2;"TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2380 LPRINT" CHECK errors are not correctable."
2390 LPRINT 100*((720-E0)/720);"PERCENT DETECT - ";
2400 LPRINT 100*((720-E0-E1-E2)/720);"PERCENT CORRECT"
2410 FOR A=1 TO 4:LPRINT:NEXT:EA=EA+E0:EB=EB+E1:EC=EC+E2
2420 LPRINT"TWO ";:LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2430 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2440 X=816:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2450 LPRINT" check bit";A:LPRINT
2460 FOR F=1 TO 5:LPRINT USING "##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2470 FOR B=0 TO 4:FOR C=B+1 TO 5
2480 FOR D=96 TO 815:IF ROM(D,1)=ROM(X,1) THEN A$="c ":E1=E1+1 ELSE NEXT D
2490 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2500 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"##";B
2510 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A:LPRINT"90 TWO ";
2520 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2530 LPRINT" CHECK errors are possible.":LPRINT E1;"TWO DATA, ONE ";
2540 LPRINT MID$(S$,1,3);:LPRINT" CHECK errors are not correctable."
2550 LPRINT"100 PERCENT DETECT - ";100*((90-E1)/90);"PERCENT CORRECT"
2560 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC=EC+E2
2570 IF W=0 THEN W=1:GOTO 2090
2580 FOR A=1 TO 4:LPRINT:NEXT
2590 LPRINT"3290 THREE BIT ERRORS (all types) are possible."
2600 LPRINT EA;"of these errors cannot be detected."
2610 LPRINT EB+EC;"of these errors cannot be located."
2620 LPRINT 100*((3290-EA)/3290);"PERCENT DETECT - ";
2630 LPRINT 100*((3290-EA-EB-EC)/3290);"PERCENT CORRECT"
```

single-bit error syndromes. The error status at this point is that of a "one pass" error, and correction proceeds accordingly.

When a zero-pass error or a noncorrectable error occurs, the six LSBs from the PROM provide additional information. For example, a hexadecimal coded output from the PROM [Fig 5(b)] defines a 2-bit error in which one bit in error is a data bit and the other a primary check bit. The primary ECC device detects a 2-bit error while the secondary device detects only the data bit in error. Bit 5 of the PROM output directs the secondary device to output corrected data to the system. In most cases, bit 5 is a 1, and corrected data are output from the primary ECC device. Bits 0 through 4 of the PROM output define the error type and the number of bits in error (Fig 6) when the MSB (bit 7) is a 1. When the MSB is a 0, syndromes are required for correction, and bits 0 through 5 represent those syndromes.

Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors.

The first of the two programs provided here is called "DC16AROM.BAS," and is a listing in hexadecimal representing the contents of the syndrome decoding PROM. The file may be presented to an output port for loading a PROM programmer if minor program changes are made. The second program, called "DC16AMAP.BAS," generates all the required syndrome maps, which include flags for all correctable 3-bit errors. These programs were written in Microsoft Basic and are compilable.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 707 *Average 708* *Low 709*

This is the second of a 3-part series. The conclusion, "Effortless Error Management," will be published next month. Part 1, "Error Correction the Hard Way," was published in December 1981.

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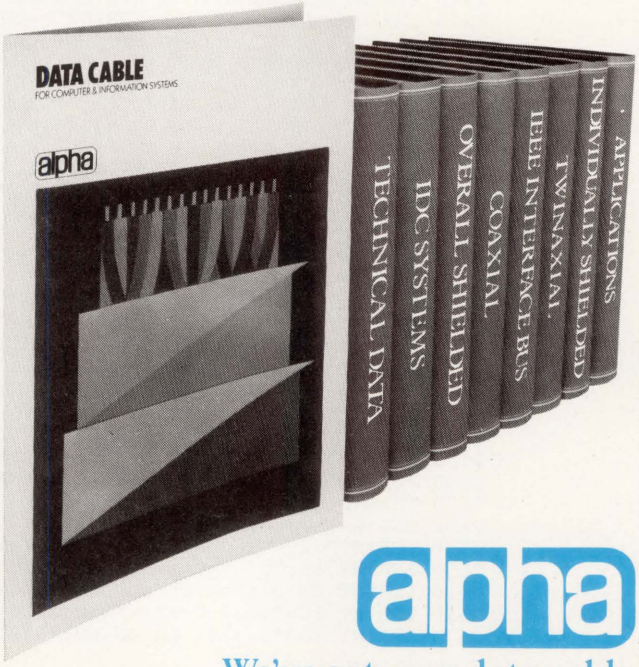

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CIRCLE 78 ON INQUIRY CARD

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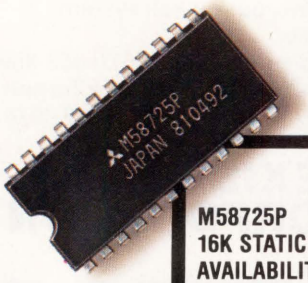

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AVAILABILITY: From Stock
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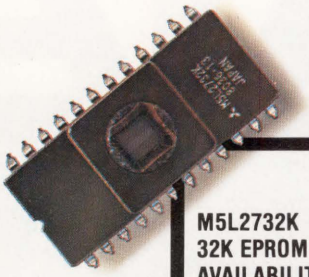

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M5K4164S
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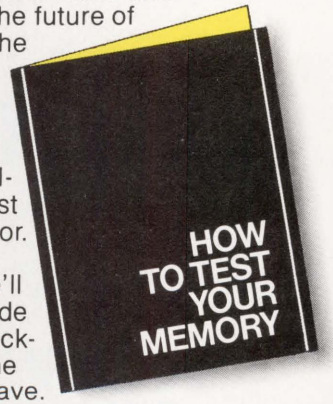

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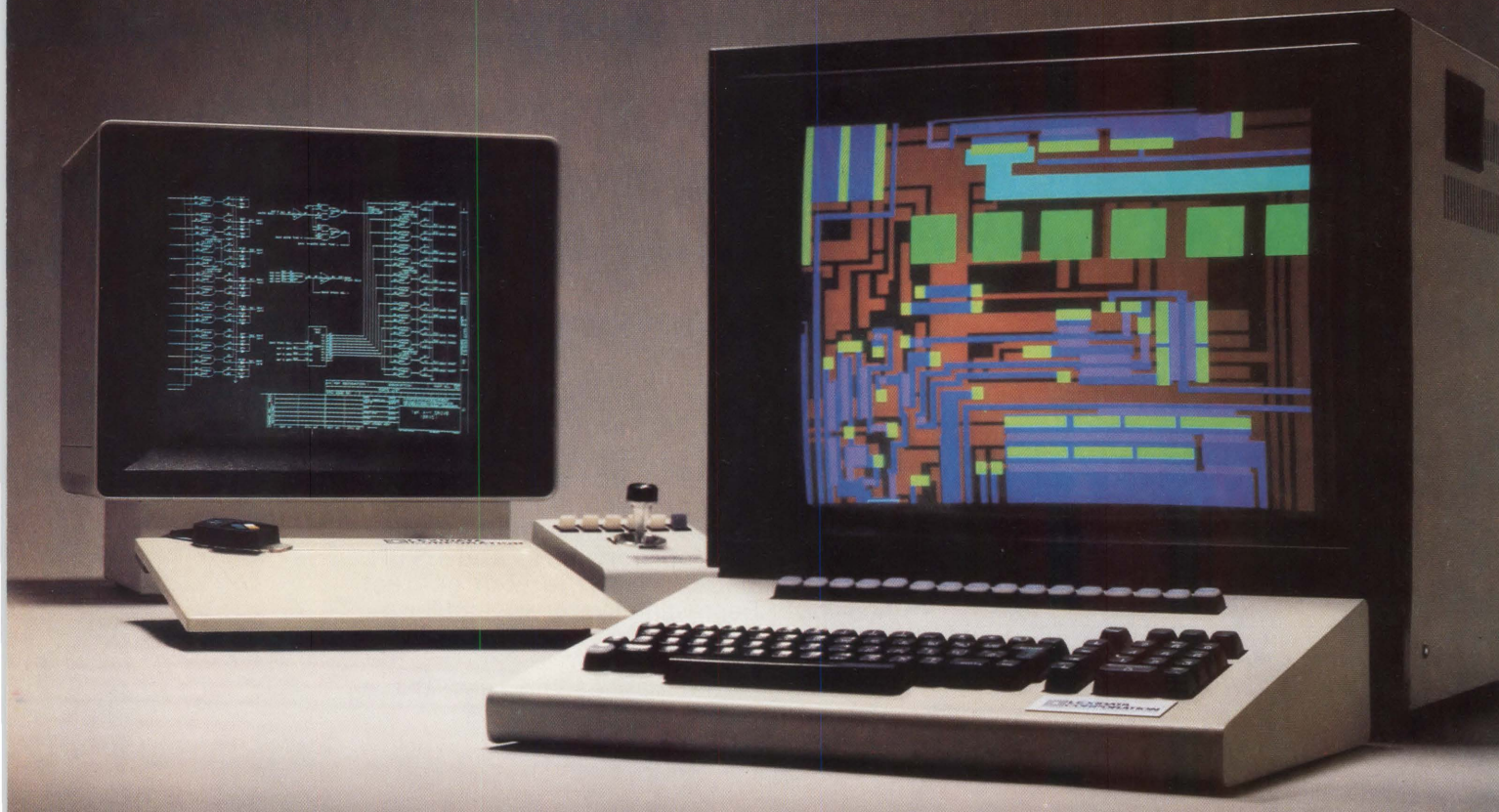

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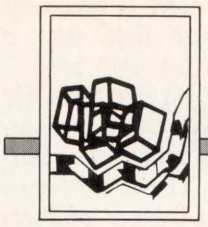

MAINFRAME MEMORIES FOR MICROCOMPUTERS

Memory management puts mainframe system capabilities within reach of the microprocessor

by John F. Stockton

Typically reserved for larger CPUs, 16-bit microprocessors will be used in applications that include multi-user and multitasking systems demanding heavy memory management support. Some specific requirements of hardware needed to support memory management (a feature not necessarily included in previous microprocessor families) are the abilities to translate addresses for dynamic memory allocation, to support dynamic address relocation, and to provide memory protection. Since it is not always known exactly how much memory a task will require when a task is started, the operating system must dynamically allocate memory while the task is running. If memory provided for the task is not located in contiguous memory, the processor must support address translation, so that physical memory can be mapped to appear logically contiguous.

It is desirable to support dynamic address allocation in hardware. When a task is suspended for a long time, and a request is made for more space in primary storage (eg, for a new program) the task suspended longest should be swapped to disk until it is again ready to run. It can then be reloaded at runtime into primary memory and restarted. But it is extremely unlikely that a task can be reloaded at exactly the same physical address at which it had been previously loaded. Relocation hardware allows the program to be relocated at exactly the same logical address, while not necessarily at the same physical address in memory.

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One of the most important requirements of a multiprocessing system is the need for system security. It is important that one task not inadvertently wipe out another task or interfere with its operation. Illegal memory operations by both processors and peripherals, such as with direct memory access (DMA) devices, should be preempted before the contents of memory are changed. Protection of this sort is particularly important in realtime process control applications. It is also important that one task not be able to access another task's data. A mechanism must be available that allows some processes to access privileged data, while keeping other tasks out. This is imperative in applications involving sensitive or private information.

While it is necessary to ensure privacy of data, sometimes data must be shared with other tasks. In this case, one task can be allowed to read, but not alter, the contents of the buffer. Read only protection accomplishes this, and is necessary for applications in which user tasks need to access a system resource, such as a realtime clock, but should not be able to change it. Resource protection also guarantees proper operating system functioning. If a task can alter the operating system's tables, there is no way to guarantee its functioning. Protective features of the memory management unit (MMU) discussed in this article allow for all of these design considerations.

Binary buddy system

A fast and efficient algorithm for dynamically allocating and deallocating storage, called the "buddy system," was first applied by Bell Laboratories in the L-Sixth computer. The basic concept of the buddy system is that when memory is requested, a search is made of the memory buffer available tables to determine if an appropriately sized buffer is available for a task. If one is not available, a search is made for the next larger sized buffer. When a larger buffer is found, it is split into two sections—one allocated to the

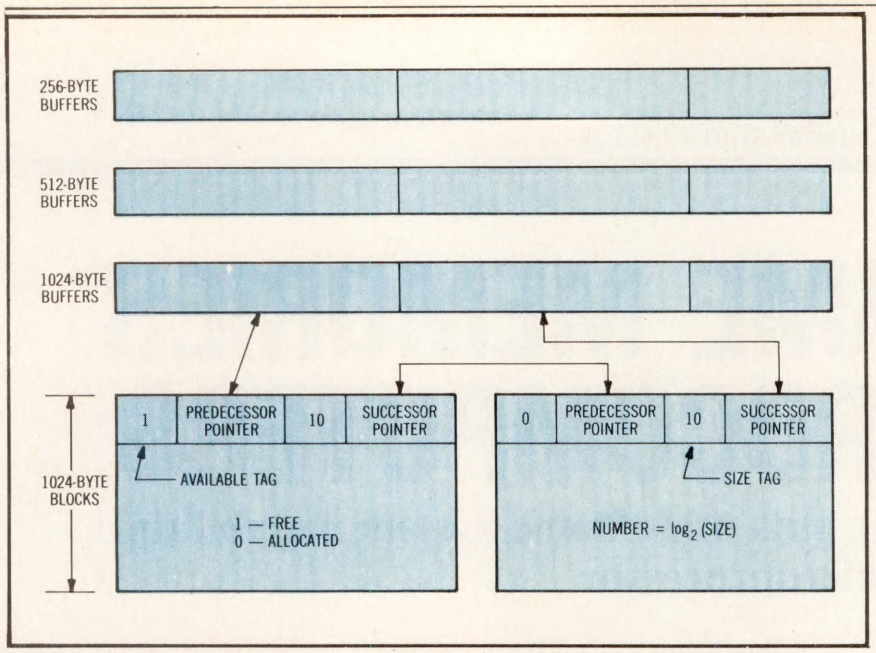

Fig 1 Arrangement of memory available tables. Predecessor pointer of each buffer points to its "buddy" successor, and vice versa, allowing buddies to be recombined into larger buffers. Buffer's buddy starting address can be easily calculated using size tag.

requesting task, and the other placed on the memory available list. If a larger buffer is not found, the process continues until either the largest sized buffer is split into multiple sections and the request honored, or the request is put in a queue to wait until sufficient memory is released to honor the request. The task returns the memory block when it is finished; if the buddy corresponding to that block is available, they are joined together to make the next larger sized block.

The binary buddy system has a distinct advantage over other allocation algorithms by knowing the starting address and length of any one buffer; one buddy is thus able to calculate the address of the other buddy by XORing the address with the buffer length. The result is an address that points to the first buffer's buddy. For example, if a buffer is at 1000H and is 100H long, then its buddy would be at 1100H. With this definition, address calculations can be carried out simply, adding to the efficiency of the alogrithm. In addition any one buffer is always located on a memory boundary that is a power of two multiple of its size; if a buffer is 100H long, it will always be located on a boundary of 100H in memory (eg, 1000H, 1100H).

The conceptual layout of memory available tables is shown in Fig 1. In this application, a separate table is maintained for each possible buffer size that might be requested. Possible buffer sizes are typically limited to a reasonable range to simplify operation of the storage algorithm. A typical range that is well supported by the MC68451 MMU is 256 bytes to 256k bytes. The MMU will support buffers up to the entire address space of the MC68000, but empirical data suggest that buffer size should be limited to about one-tenth of the total memory space available, (16M bytes typical for the MC68000). Each entry in the memory available tables consists of two links, successor and predecessor pointers. A free buffer count may be provided to lower the search time when no buffers are available.

In each memory block, the first five words consist of system information, including both a free/allocated bit, a predecessor pointer, a successor pointer, and a size field that is typically encoded as the base 2 logarithm of the field size. [See Fig 2(a).] As illustrated, there are currently no 256-byte or 512-byte buffers available. The respective predecessor and successor pointers point to themselves to indicate a null list, and the free buffer count is set to zero. After a 256-byte buffer request is made, the memory available table for 256-byte buffers is scanned and found to be empty. The 512-byte buffer table is scanned next, and also found to be empty. The routine continues to scan the next higher binary sized buffer table until an entry is found [Fig 2(b)]. In this example, a 1024-byte buffer is available. It is then removed from the 1024-byte buffer available list, and split into halves. The 512-byte half is added onto the 512-byte buffer available list, and the remaining 512-byte buffer is again split to honor the request for a 256-byte buffer. One half of the 512-byte buffer is allocated for the request, and the other 256-byte section is added to the 256-byte buffer available list. Adding a buffer to a list is simply a matter of rewriting four pointers, a free/allocated bit, and a size field.

Since buffer sizes are powers of two, the binary buddy system operates most efficiently when buffer requests are in powers of two. Requests not made in binary must be treated as if they were larger than they actually are so that more memory is allocated to a task than was really needed. The result of all requests between 257 and 512 bytes being treated as a request for 512 bytes is approximately 1.3 to 1.5 times greater than the memory requested and that actually being used.

Binary restrictions of buffer size that cause inefficiency is measured as the fraction of memory allocated greater than that which is actually requested. Since this waste occurs inside a buffer, it is called internal fractioning, and is the primary cause of inefficiency in the buddy system [Fig 3(a)]. However, a modification of the binary buddy system (eg, the Fibonacci system) can reduce this internal fractioning from an average of 38% excess memory to 25%, at the expense of a slightly more complicated allocation algorithm.

By definition, all memory allocation schemes suffer from these innate inefficiencies to some degree. Although two buffers of a given size exist and could be combined to create a buffer large enough to satisfy a request, they might not be buddies and therefore could not be combined. Fig 3(b) shows an example of a memory map illustrating external fractioning, which occurs outside the buffers. External fractioning typically is not as great a problem as internal fractioning, since enough memory will be freed in time to honor the request.

In comparison, Fig 4 shows a typical memory map that would result from use of the buddy system. Note that the entire map is considered as one buffer, and that it is broken into two equal size sections, each buddies.

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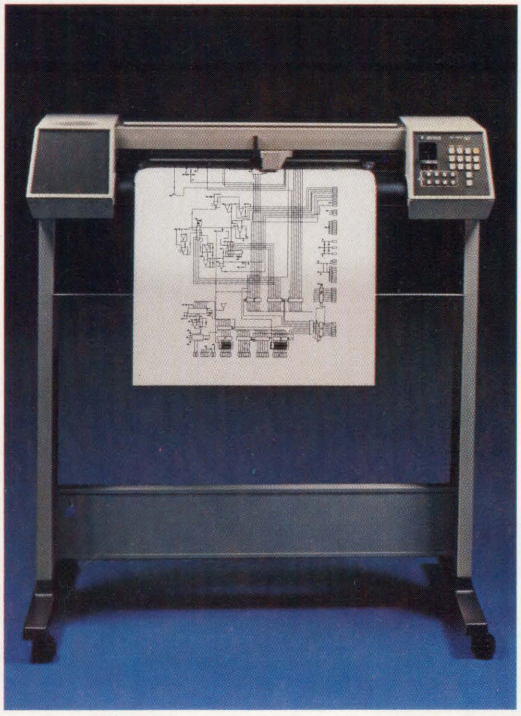

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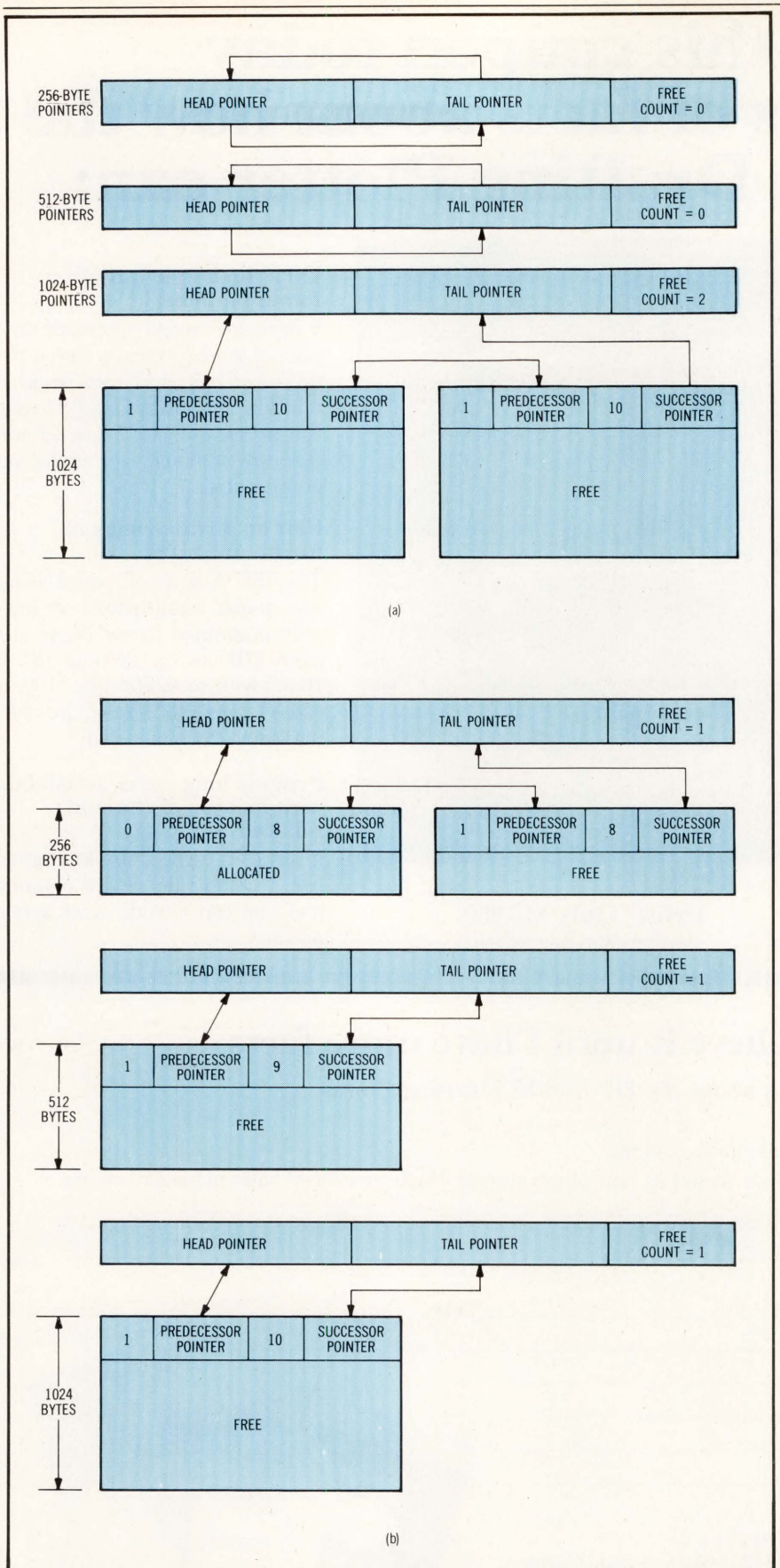

Fig 2 Before (a), and after (b) a 256-byte buffer request. If request is made for buffer size not currently available, the next higher buffer table is scanned until one is found. In this case a 1024-byte buffer is divided into two 512-byte buffers. One is tagged available and one is divided again into two 256-byte buffers. One 256-byte buffer is then allocated and remaining 256-byte buffer is tagged available.

These sections are in turn broken into smaller sections, and so on. Two available buffers might also exist on the same level (being of equal size), and yet they cannot be combined since they come from different "parents."

Algorithms

The algorithm for allocating a memory block is relatively straightforward. The procedure starts by checking if a segment size is available within a power of two of the request. If so, the segment is removed from the available list and tagged as being in use. At this time, a descriptor is loaded into the MMU to describe the segment. If no segment is available, then the tables of the next larger size segments are scanned to check for an available segment. If no segment is available to fill the request, the available list continues to be checked for the next higher size segment until the maximum segment size is reached. Typically, this is one-tenth the total memory size. The requesting task must then be suspended until memory becomes available, or other descriptors must be swapped to make room for the request.

When a larger segment is available, it is broken in two, a left half and a right half. One half is used to honor the request, and is tagged and entered into the MMU. The other segment is entered into the available list of the smaller size segment. Fig 5 charts this operation. Note that if the second power of two segment size is not available, then the next one, if available, will be broken into three sections: one-quarter for the request, and one-quarter sized segment and one-half sized segment which are available for other requests.

The algorithm for deallocation is also relatively simple, and is charted in Fig 6. When a buffer is returned to the pool, the segment descriptor in the MMU is immediately freed, and the segment is added to the available table. At the same time, its buddy is checked for availability. If both buddies are available, they are removed from the available list, and recombined to become a larger segment. Recombination prevents the accumulation of numerous small segments that tend to choke the system.

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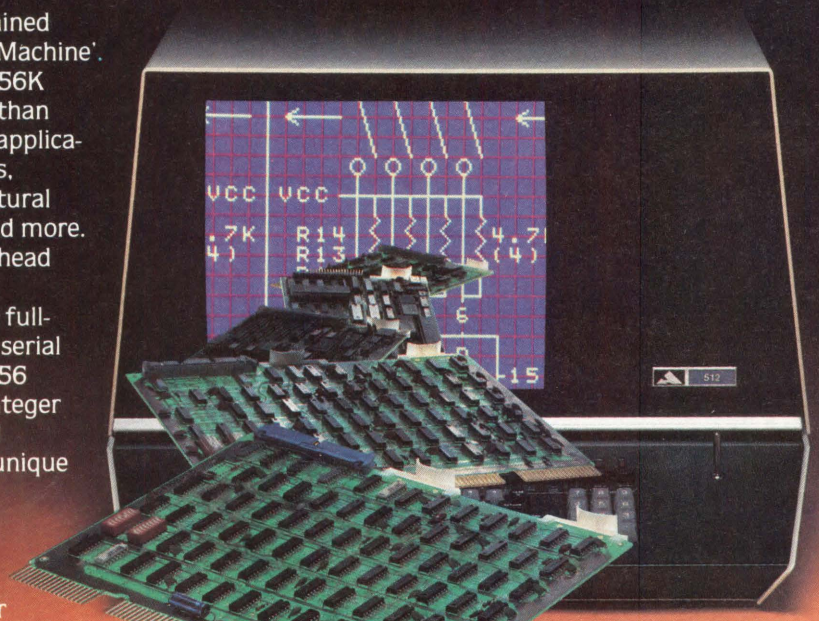

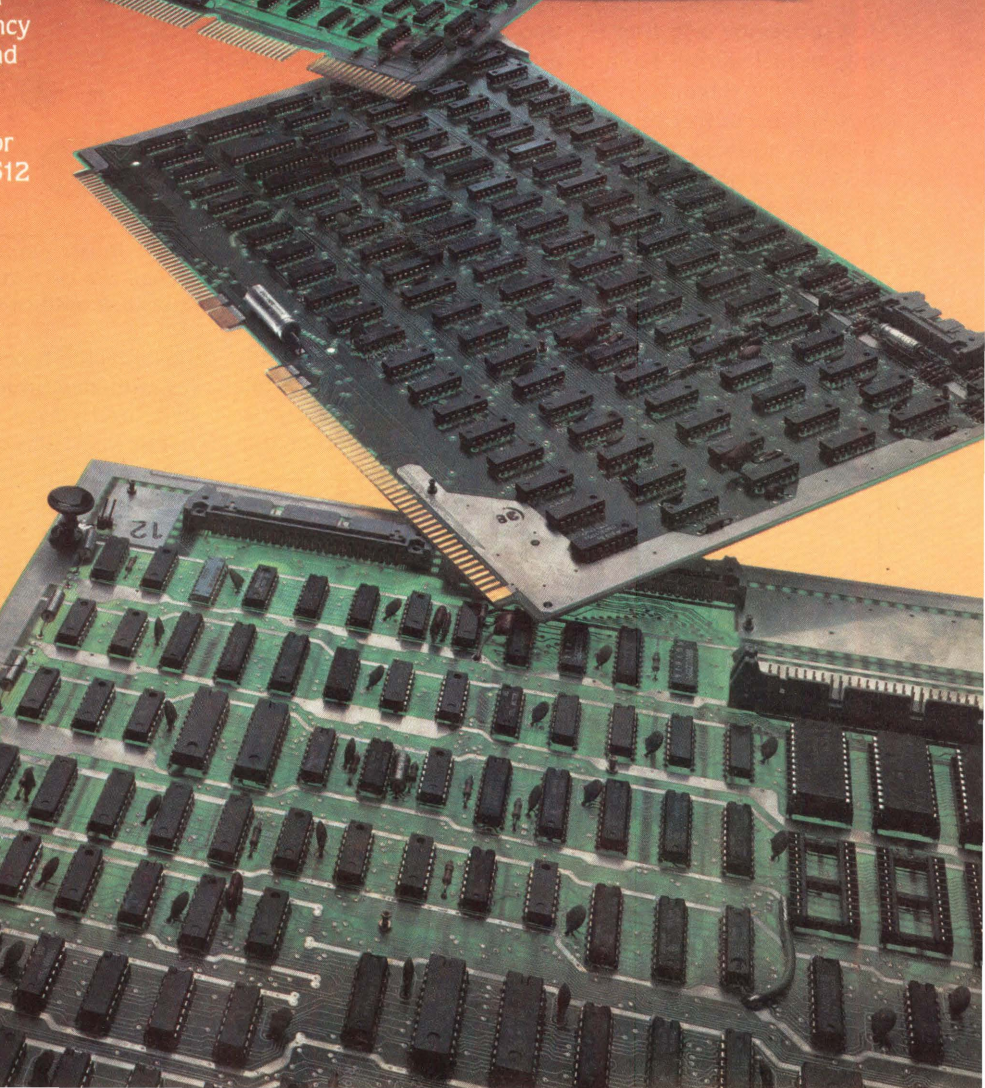

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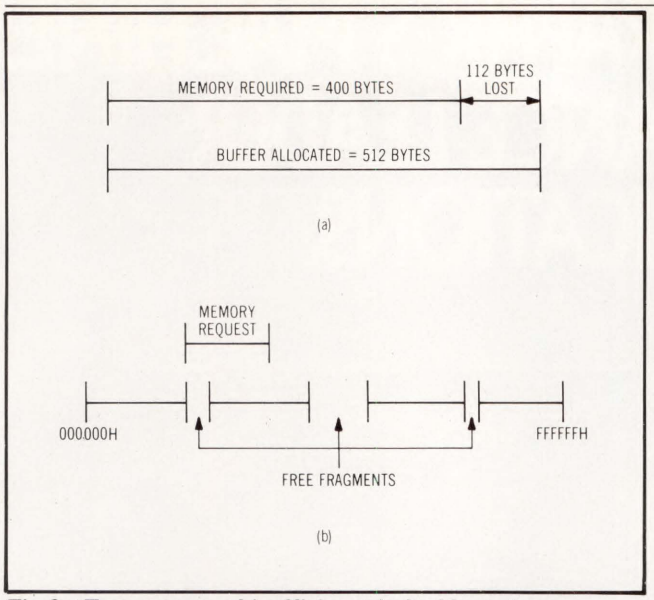


Fig 3 Two sources of inefficiency in buddy system. Internal fractioning (a) stems from allocating more memory to buffer than is actually used. External fractioning (b) can leave 3 segments of memory unused. External fractioning is, however, a transitory problem.

translation mechanism, and virtual memory support are also important design considerations of the MMU. The central processing unit (CPU) provides four lines to indicate the type of bus cycle currently executing. These lines, consisting of three function code lines (FC0 to FC2) and the bus grant acknowledge line (BGACK), specify if the processor is in user or supervisor mode, if it is making an instruction fetch or a data fetch, and if the processor or a slave device (such as a DMA controller) currently has control of the bus. Each condition specifies a unique address space; thus the function codes and BGACK are regarded as address space modifiers. The MMU uses them to provide a fast context switch, and to allow user data areas to be shared without necessarily forcing the program areas to be shared as well.

A 16-byte address space correspondence table within the MMU is depicted in the Table. Function codes associated with each memory cycle are used as an address in the Table, where they effectively point to a tag that will be used for that address reference. Eight processor fetch types, along with eight DMA or other bus

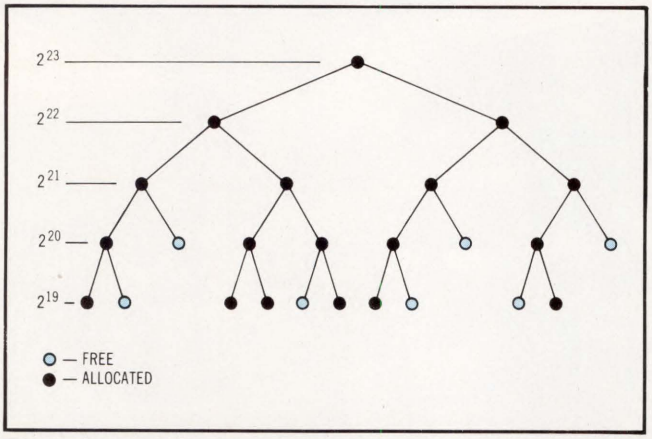


Fig 4 External fractioning memory map. Three buffers on the second level cannot be used unless their exact size is requested, since buddies that are currently free cannot combine with non-buddies.

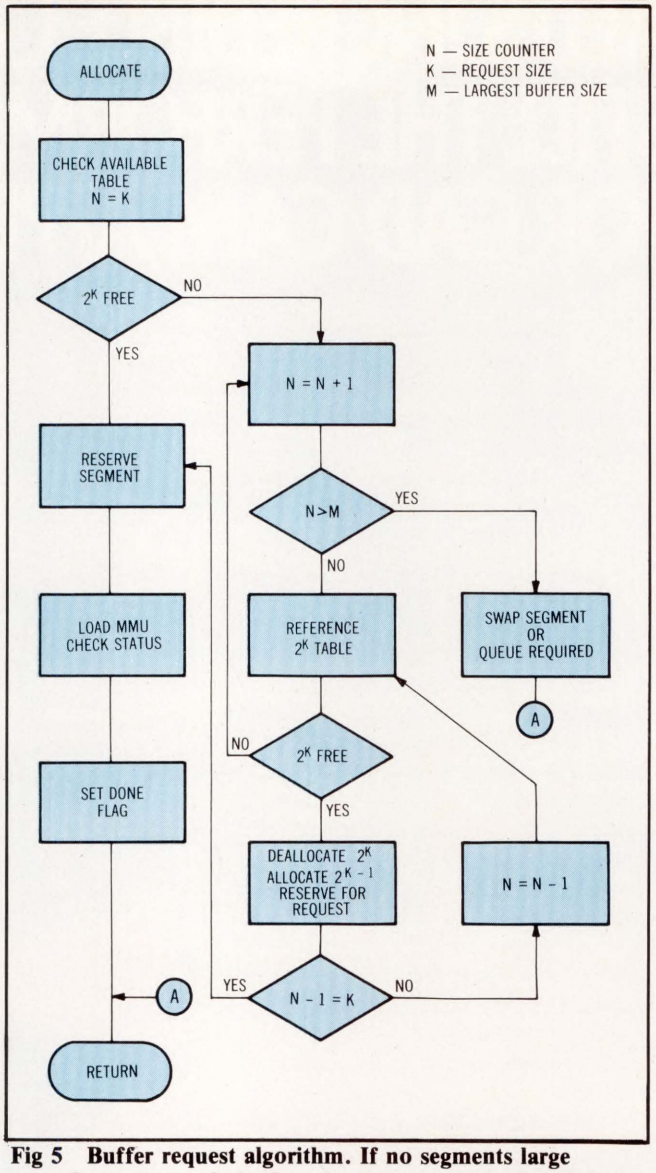
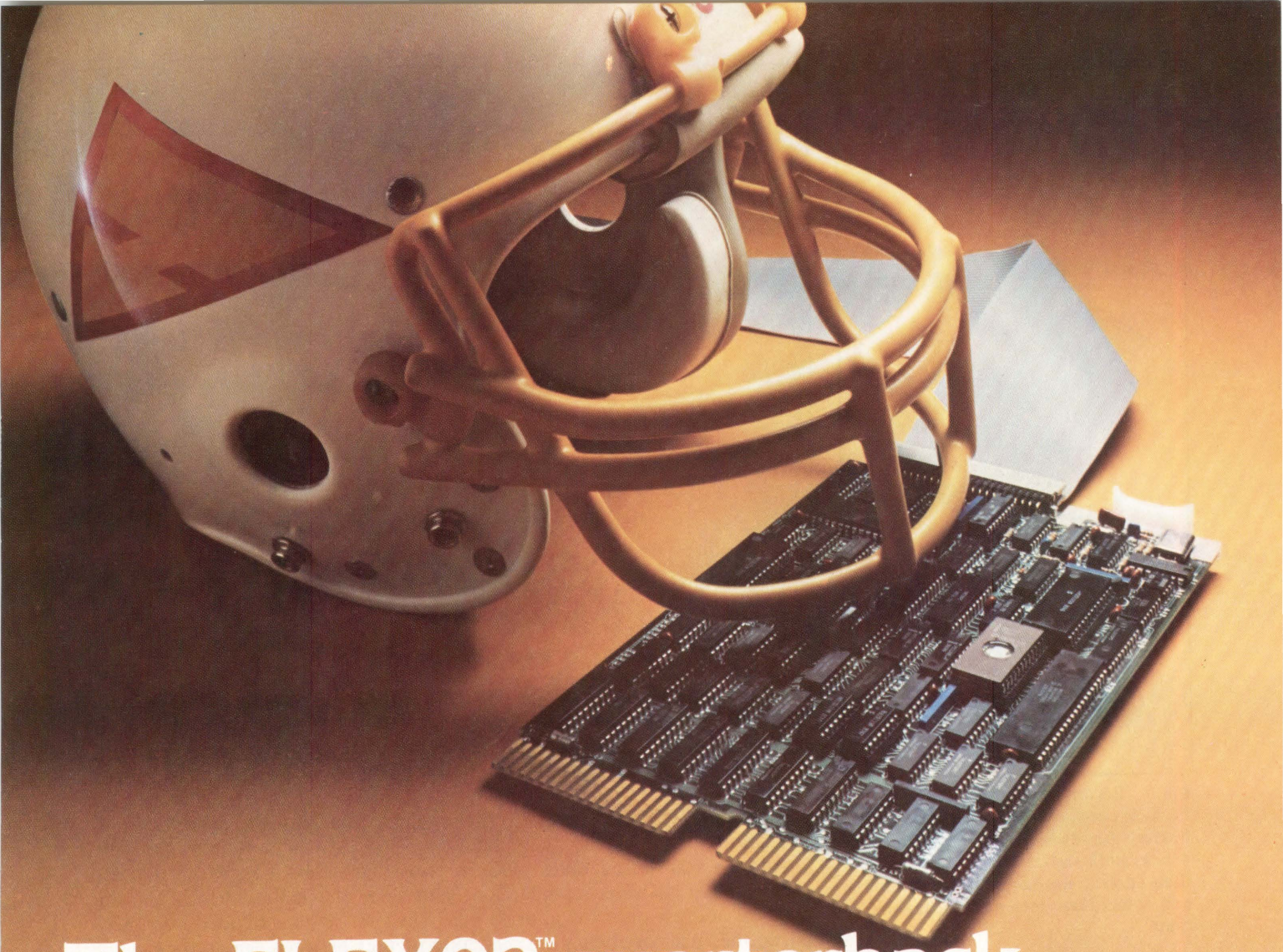


Fig 5 Buffer request algorithm. If no segments large enough can currently be found, request is queued and task suspended until enough memory becomes available.

master fetch types are supported. An address space correspondence table is primarily used to speed up context switches by associating the tags in a lookup scheme.

The MMU allows for a fast context switch by changing a program and a data descriptor tag in the address space correspondence table of the MMU. Bytes are used on a cycle basis to determine the segment descriptors that should be considered for an address and privilege match; each segment descriptor has a tag associated with it that is considered for a match only when the tags match. By changing two bytes in the address space correspondence table, it is possible to have a completely different set of segment descriptors used for address translations. A very fast context switch can therefore be made, but at the expense of needing all segment descriptors resident at the same time. The MMU context switch time equals 2 write cycles at 500 ns each $\geq$ 1.0 μs. However this is not a limitation, since each MMU has 32 segment descriptors, and up to 8 MMUs can be configured in a system. One distinct advantage of lowering context switching time is that the processor can spend less time taking care of overhead and have more time to run user tasks.



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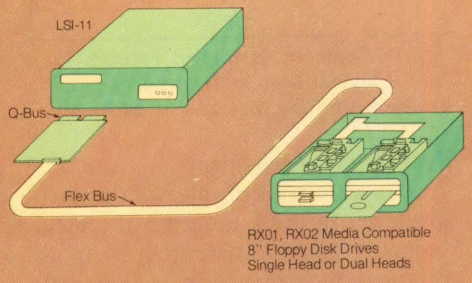

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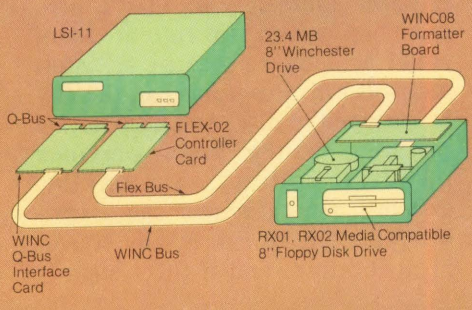

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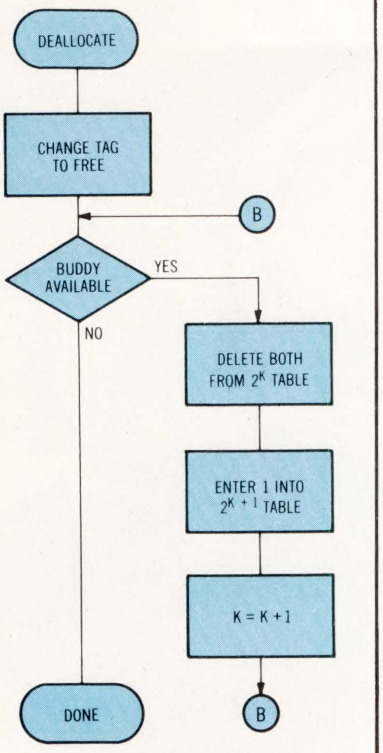

Fig 6 Recombination algorithm. Process checks tables to see if freed buffer's buddy is available. It then deletes both buffer and buddy from their current size table, and recombines and enters them into next higher size table.

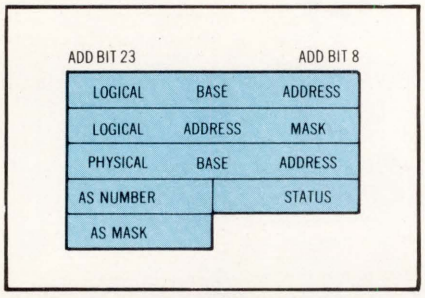

Fig 7 Segment descriptor format. 16-bit logical base address corresponds to the beginning of segment address.

Translation mechanism

Address translation allows the programmer to think in terms of logical memory allocations rather than in physical memory terms. The MMU translates logical addresses into physical addresses, so that a program assembled to run at 2000H could actually be located at 2A00H and still run. Programs can thereby be swapped to disk, and need not be restored to the exact previous physical address. In smaller systems, a programmer can assemble programs to run at any convenient location, and if the system is reconfigured, programs can be relocated without reassembly. The MMU can map both program and data segments so that they are shared or kept as private segments. Since function codes are used in the mapping function, segments can only be executed by making them available to the processor during instruction fetches. Segments can also be defined so that an interrupt will be generated upon access to the segment, thus allowing dynamic stack allocation.

Address space correspondence table

BGACK	FC2	FC1	FC0	Address correspondence table
0	0	0	0	Reserved
0	0	0	1	User data
0	0	1	0	User program
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Supervisor data
0	1	1	0	Supervisor program
0	1	1	1	Interrupt acknowledge
1	0	0	0	DMA and other bus masters
1	0	0	1	DMA and other bus masters
1	0	1	0	DMA and other bus masters
1	0	1	1	DMA and other bus masters
1	1	0	0	DMA and other bus masters
1	1	0	1	DMA and other bus masters
1	1	1	0	DMA and other bus masters
1	1	1	1	DMA and other bus masters

Address translation takes place in two stages consisting of an address range and a privilege comparison, and later the actual driving of the physical address onto the address bus. The first stage is divided into three parts, the first part being the matching of tags between the address space correspondence table and the tag associated with each segment descriptor. Second, an address match is made, in which the logical address must be checked to ensure that it is in the range of the addresses that should map into that particular segment. The third part checks the privilege status to verify that a write operation is not being attempted into a read only segment. If all three parts of the address comparison execute successfully, the physical address associated with that segment descriptor is driven onto the address bus. Fig 7 illustrates the format of a segment descriptor, which comprises six parts: a logical base address, a logical address mask, a physical base address, an address space number, an address space mask, and a status register. Each MMU holds 32 segment descriptors.

The 16-bit logical base address can be treated as the beginning address of a segment. Since the 8 least significant bits of the address from the processor are wrapped around the MMU, only the most significant address bits are modified. Combining the logical base address and its mask forms the end address of a segment. The mask effectively turns bits into "don't cares," and they are then passed through the MMU unmodified. If all bits in the mask were "cares," the size of the memory segment would be 256 bytes, since the 8 least significant bits are not reviewed by the MMU. If the least significant bit of the mask is set to be a don't care bit, then address bit 8 is passed directly through the MMU, effectively bypassing it. The segment size is therefore 512 bytes. When segment size becomes 512 bytes, the segment must fall on a 512-byte boundary because lower bits of the logical base address are treated as don't cares. One segment descriptor can describe any block of memory ranging in size from 256 bytes to 16M bytes, increasing in size by powers of two.

When the logical address is in the range of a defined segment, a match occurs within tags and privileges. The physical base address then is driven onto the bus for all address lines that were cares as defined by the mask. Address translation is now complete.

The address space number is the tag used for context switching. In the address space correspondence table (which is considered to be a global table), there is a tag for the machine cycle currently running. Tags that are part of a segment descriptor must match with the address space number before the segment descriptor can drive out its physical address. Since every segment descriptor has a tag, it is easy to alternate between different sets of segment descriptors if each set has a different number in the address space registers of its descriptors. By changing one byte in the address space correspondence table, the set of segment descriptors can be efficiently modified.

Segments of memory may need to be shared among different tasks, as is the case with a common resource. The address space mask register allows bits of the address space number to effectively become don't cares, so that a segment descriptor can respond to multiple tags that differ only in the don't care positions. Common memory therefore can exist as a uniquely defined segment, and can keep other tasks out of private memory. Segment status registers also contain the used and modified bits that are commonly used in virtual operating systems for efficient swapping routines and least recently used routines. In addition, the status register includes bits that allow an interrupt to be generated whenever an access is made into the segment. These bits are particularly useful for stack overflow detection and benchmarking applications. One bit also defines a segment to be read only, and another bit flags a fault if an access is made into this segment.

Status and control registers give the programmer access to the MMU for such operations as programming segment descriptors, finding out which segment has a fault in it, setting up interrupt vectors, reading the status local to the MMU, and reading the status of the system when multiple MMUs are involved. The global status register allows the programmer to determine if any illegal conditions occurred during MMU setup, such as segment descriptors that describe overlapping segments of memory. Sharing an area in memory via a common segment is the proper way, and the MMU will detect segment descriptors that were accidentally programmed to overlap.

Accumulator

Looking exactly like a segment descriptor, the accumulator is used to program the segment descriptors in the MMU. Initially, it is set up to look exactly as the desired segment descriptor; and a control bit and destination pointer are set up in the status register. The accumulator is then loaded into the descriptor and the appropriate error condition bits are set. Another use for the accumulator is for direct address translation. If the logical address and user number is given to the MMU in the accumulator, the physical address, as the MMU would map it, will be returned in the accumulator. Operating system time is saved, since the MMU can do the conversion and return the value rather than having the operating system duplicate the calculation.

Conclusion

Future CPU versions will support virtual memory, and in designing the peripherals, it makes sense to now include features that will be required in the future. Important to virtual memory systems are the abilities to indicate through the fault line that a page fault has taken place, and to indicate either that a segment has been written into, or that it has not been recently used. By using the MMU and dynamic memory block allocation techniques, designers will be able to satisfy the increased memory requirements of 16-bit CPUs in multi-user and multitask environments.

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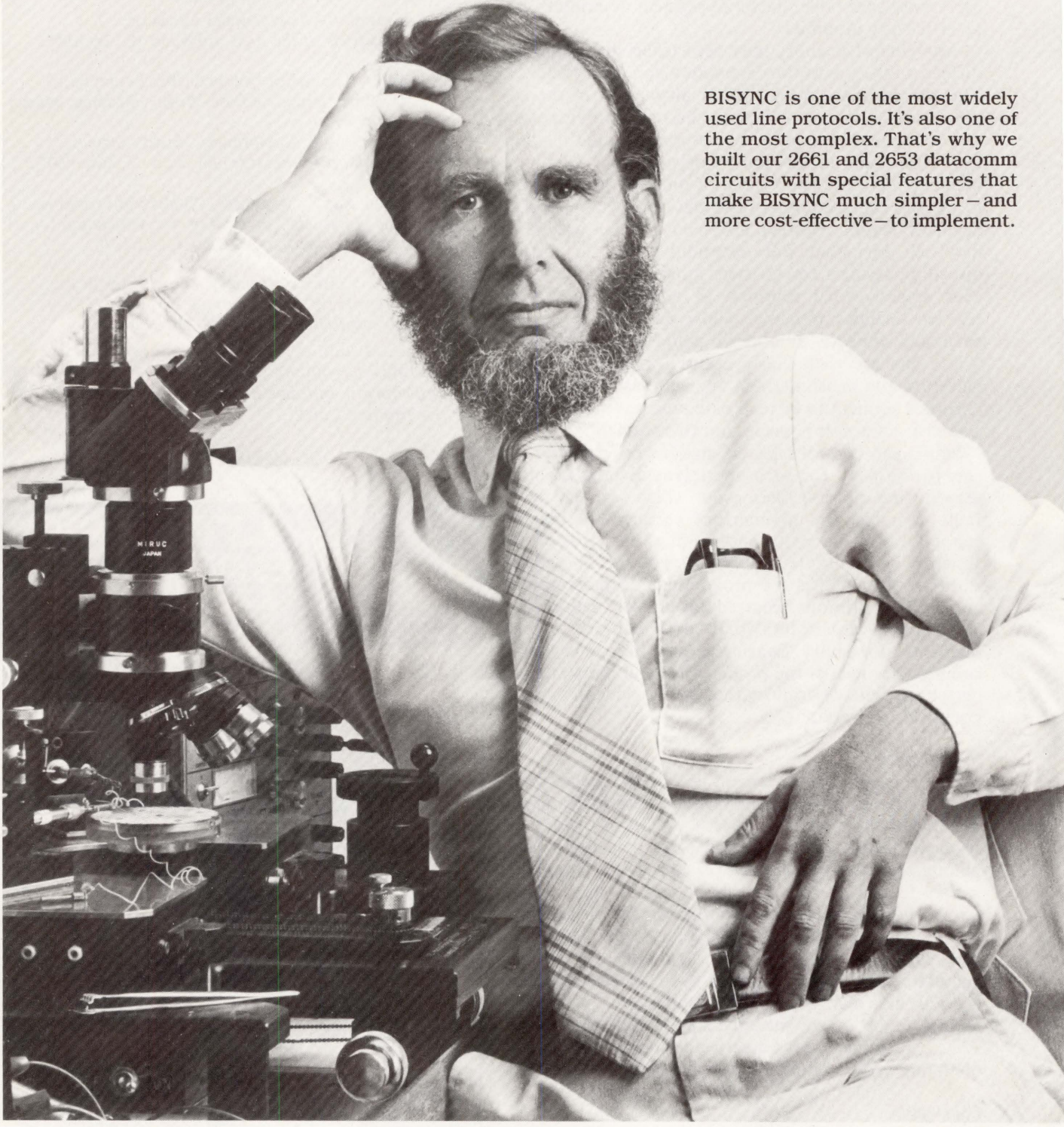

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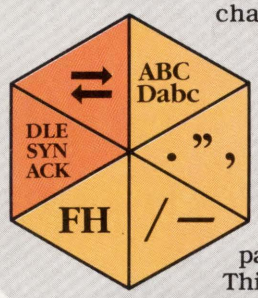

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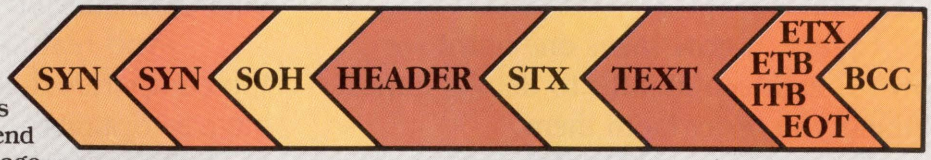

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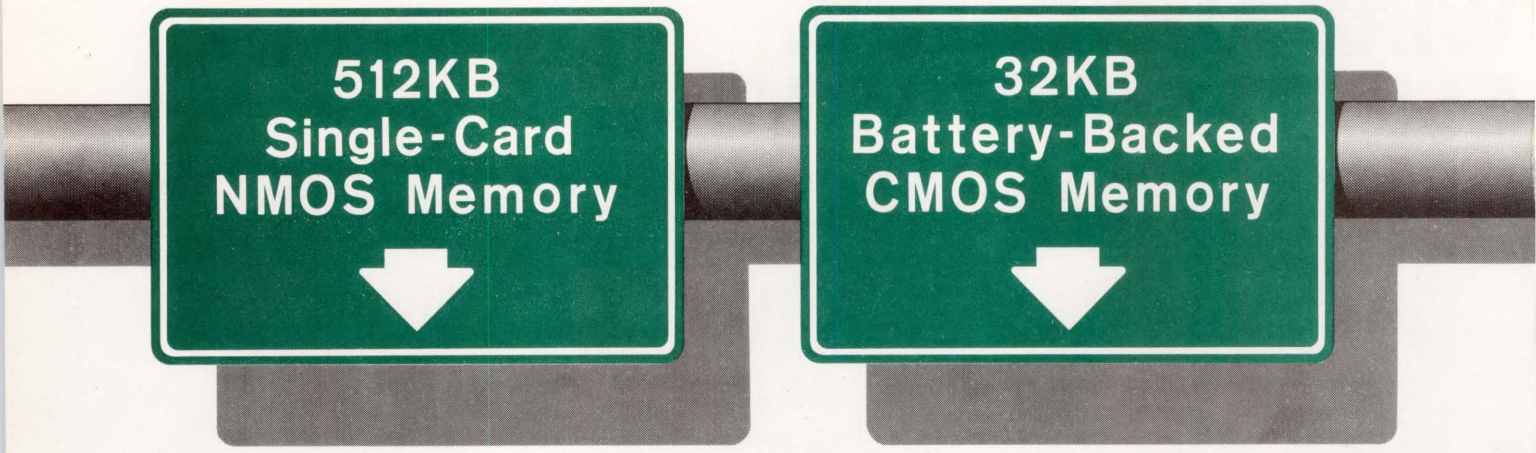

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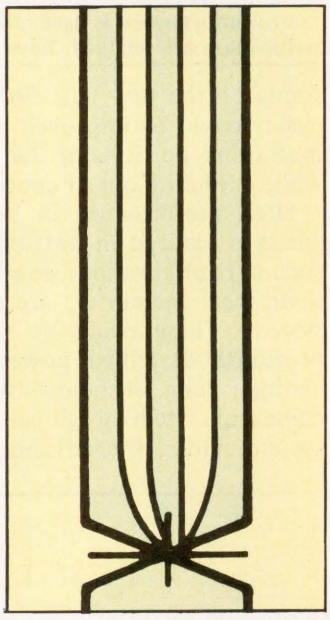
BETTER PROCESSOR PERFORMANCE VIA GLOBAL MEMORY

Wait states are eliminated by joining global and local memories through five TTL components

by Joseph P. Altnether

At least 60% of today's designs incorporate microcomputers, which have become one of the most widespread components in a variety of electronic equipment ranging from video games to navigational flight computers. Microcomputers comprise several elements. One of the more important of these is the memory. In early systems (and even in some of today's low performance microcontrollers), the memory is interfaced and accessed exactly like any other peripheral. Such an architecture is shown in Fig 1. For this type of application, data store (random access memory), control store (electrically programmable read only memory/read only memory), and input/output reside on a single bus connected directly to the central processing unit. This kind of application is usually a dedicated system performing only one function, such as control of a vending machine.

Memory consists of control store and data store. The former occupies most of the memory and contains about 16k bytes of program; the latter is small and contains less than 4k bytes. A major design goal is simplicity, which can be best achieved when the components of control store and data store are compatible. It is much simpler and certainly more efficient to use the same set of address decoders and drivers, as well as data transceivers, for both control and data store. This is achieved with common pinout and functionality between random access memory (RAM) and electrically programmable read only memory/read only memory (EPROM/ROM). Therefore, the memory should be an 8-byte wide RAM. Several disadvantages are inherent in such a system: the address space is limited; and because all elements—including the central processing unit (CPU)—reside on a common bus, the CPU, as the bus controller, suspends processing to control bus operations.



Enhancing the system

The performance of this system can be enhanced by upgrading to a microprocessor and storing a variety of programs in permanent bulk memory. In this kind of system, control store consists of a RAM containing up to 64k bytes (Fig 2). This memory is much larger because it serves a dual function: data store and control store. Programs to be executed are downloaded via a boot program residing in EPROM. The system overcomes the memory addressing space deficit of the previous system but still retains the disadvantage of having all memory

Joseph P. Altnether is technical marketing manager for memory products at Intel Corp, Aloha, OR 97005. Before that, he worked as an applications engineer at Intel and a memory system designer for nuclear/medical instruments at G. D. Searle. Mr Altnether has a BSEE from St Louis University.

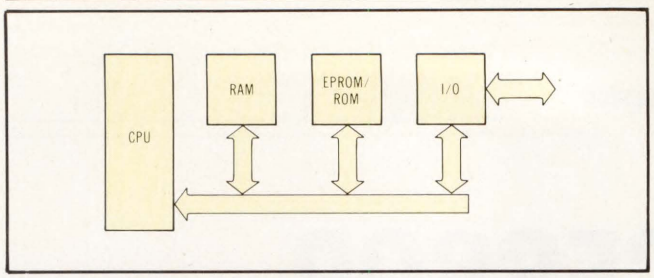


Fig 1 Single-bus architecture of dedicated microcontroller. Though inexpensive, this configuration limits available address space and requires that CPU suspend processing when controlling bus.

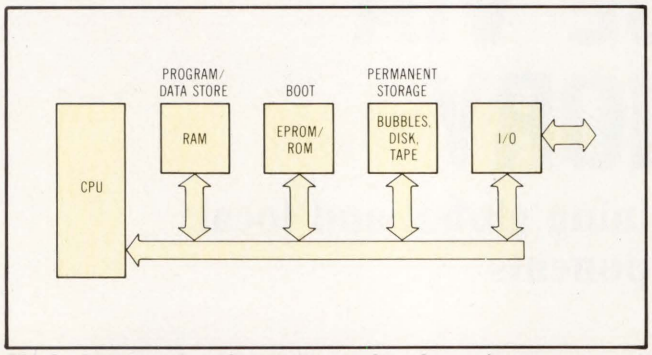


Fig 2 Improved performance results when microprocessor using RAM program storage for up to 64k bytes of data and control information is used. Disadvantages of common bus architecture are retained, however.

reside on the CPU bus. For example, throughput efficiency could be improved if it were possible to download other portions of the program into control store while executing out of control store (dual porting).

High performance in both processing power and speed is realized in distributed processing systems. In such a configuration, several processors, together with their local memories, are distributed throughout the system. These could be structured like the systems previously described; however, they have an important distinguishing element—multiple local buses with a common system or global bus. Fig 3 depicts such a system. Here, the advantages of dual porting, error checking and correction, and direct memory access all become cost effective.

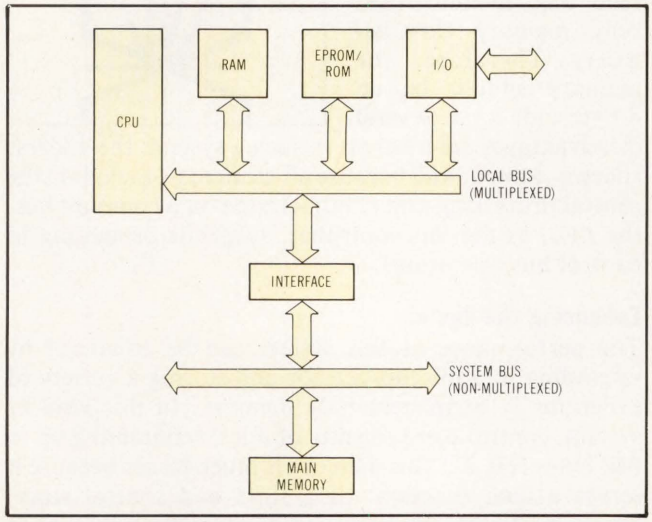


Fig 3 Distributed processing system using several processors with local memories and common (global) bus provide high performance. Each processor in system has access to large (1M-byte) global memory.

...because the global memory is so large, the RAM used must be as dense as possible to reduce the number of components.

Residing on the system bus is a global memory to which every processor has access. This memory can be very large—even greater than 1M byte. Consequently, it could be disk, tape, magnetic bubble, or RAM. If built with RAMs, the type used would be dynamic RAMs (DRAMs) for several reasons. First, because the global memory is so large, the RAM used must be as dense as possible to reduce the number of components. Lower component count reduces system cost and increases system reliability, which is inversely proportional to the number of components in the system. Second, the components should consume minimal power. Even a small amount of power per device multiplied by hundreds of devices will require a large power supply. In addition, as the power requirements increase, so do the cooling requirements, which again add to the overall system cost and operating cost.

Finally, the RAM must be low cost to be competitive and provide ample operating margins. DRAMs meet these requirements quite adequately as they provide the lowest cost per bit and also consume the lowest power per bit of RAM devices. Unfortunately, designing with DRAMs has long been considered esoteric and difficult. In fact, some designers still believe that DRAMs do not even work. The first of these beliefs was based on fact in earlier days, but the second is based on an emotional

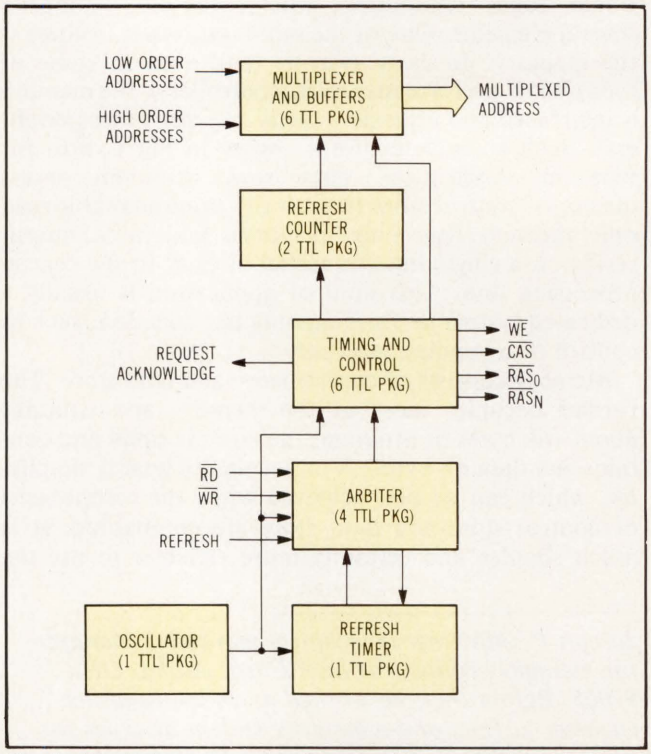


Fig 4 Typical DRAM controller. Oscillator provides timing and control logic for refresh timer.

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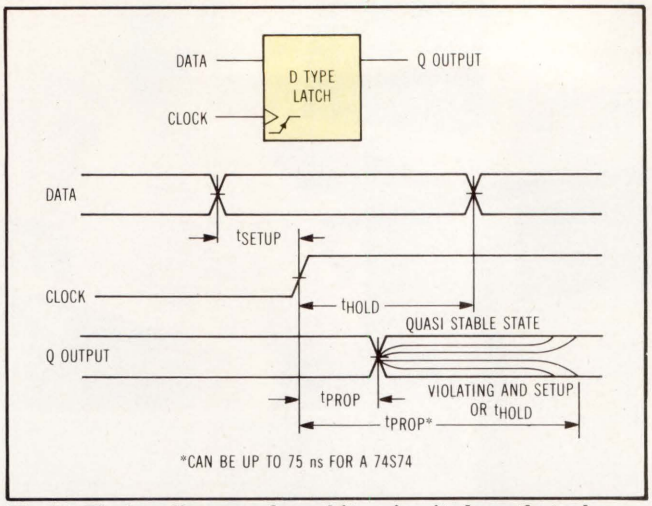

Fig 5 Timing diagrams for arbiter circuit show that when certain conditions exist, output is analog signal floating between TTL levels 1 and 0. During this 75-μs period, no decisions can be made and refresh failure occurs.

reaction to a memory that forgets unless it is periodically told to remember. DRAMs do not lose data if they are properly refreshed. This can be easily accomplished by a memory interface controller.

Designing a DRAM system

Although it is more difficult to design a DRAM system than a static RAM (SRAM) system, it is not impossible. Shown in Fig 4 is a typical DRAM controller. At the heart of the controller is an oscillator which provides timing and control logic for the refresh timer. Because DRAMs are clocked, they need signals like row address strobe (RAS), column address strobe (CAS), and write enable (WE), which come from the control logic. The refresh timer will periodically time out, typically every 15 μs, to request a refresh cycle asynchronously with respect to CPU memory requests. To decide which request (CPU or refresh) is granted first, an arbiter circuit is required. The arbiter is the most complicated controller element to design. In theory, a D type flipflop could be an arbiter (Fig 5). If refresh request is set asynchronously with respect to the system clock, a decision on the Q output can be made. If Q is true, the refresh cycle is granted; if false, the CPU is given access. Timing relationships of data and clock indicate that normal operation of the flipflop will occur if setup and hold times of data with respect to the clock are met.

If the setup or hold times are violated, however, the Q output is no longer a transistor-transistor logic (TTL) level 1 or 0. The output becomes an analog signal floating between TTL levels somewhat like a 3-state output device with the output in a high impedance state. This condition can persist for as long as 75 ns, during which it is impossible to make a decision. At the system level this appears as a refresh failure. Lastly, the controller requires multiplexers and drivers for the memory addresses. The total system is built with 20 TTL components (Fig 4).

The...DRAM controller...includes an arbiter which synchronizes the refresh and memory cycle requests to eliminate the arbitration problem....

Another consideration is design time. About four weeks are usually required for design, two weeks for worst-case analysis, six weeks for printed circuit board layout, four weeks for building and debugging, and another four weeks for redesigning to add features or correct errors. And this does not include a possible second iteration effort. In any case, the task could consume up to six man-months.

A simpler solution

Intel's dynamic RAM controller, the 8203, is contained in a single 40-pin package that incorporates the entire DRAM controller (Fig 6). It includes an arbiter which synchronizes the refresh and memory cycle requests to eliminate the arbitration problem previously described. Compatible with the 8080A, 8085A, iAPX88, and iAPX86 family of microprocessors, the device directly addresses half a megabyte of memory composed of 64k RAMs (eg, the Intel 2164). All the refresh functions are provided: timer, 8-bit address counter, and multiplexers for addresses. Because refresh is usually performed asynchronously with the CPU cycles, provision is made for performing synchronous refresh if required. At times the controller will be providing refresh when the CPU requires access. Consequently, the CPU must be placed in a WAIT mode. This is accomplished with a signal from the 8203 called SACK. In addition, the signal XACK can be used to clock data into the latches during a read cycle.

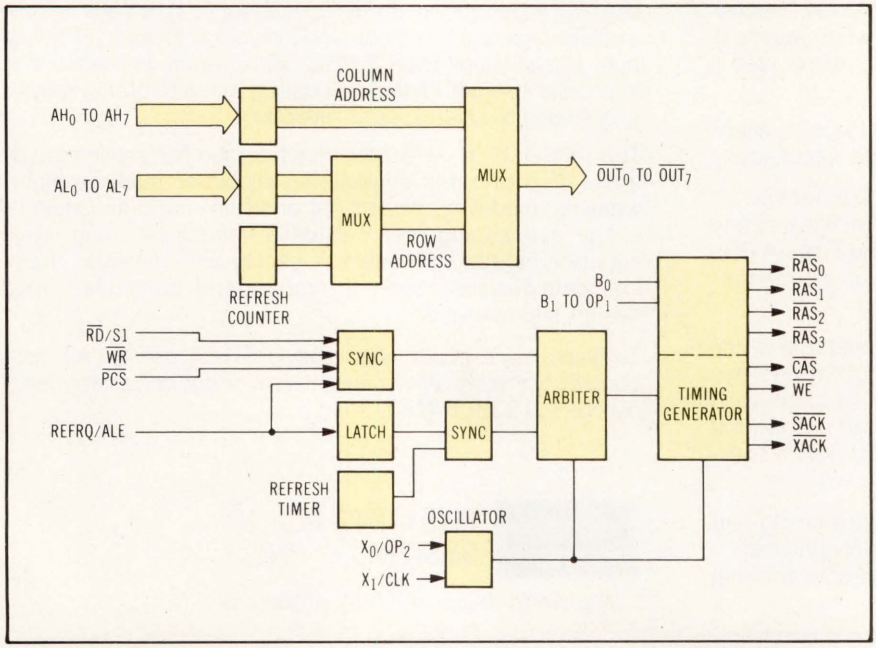

Fig 6 40-pin, 8203 DRAM controller includes arbiter that synchronizes refresh and memory cycle requests eliminating indecisive condition of Fig 5. Chip directly addresses 0.5M byte.

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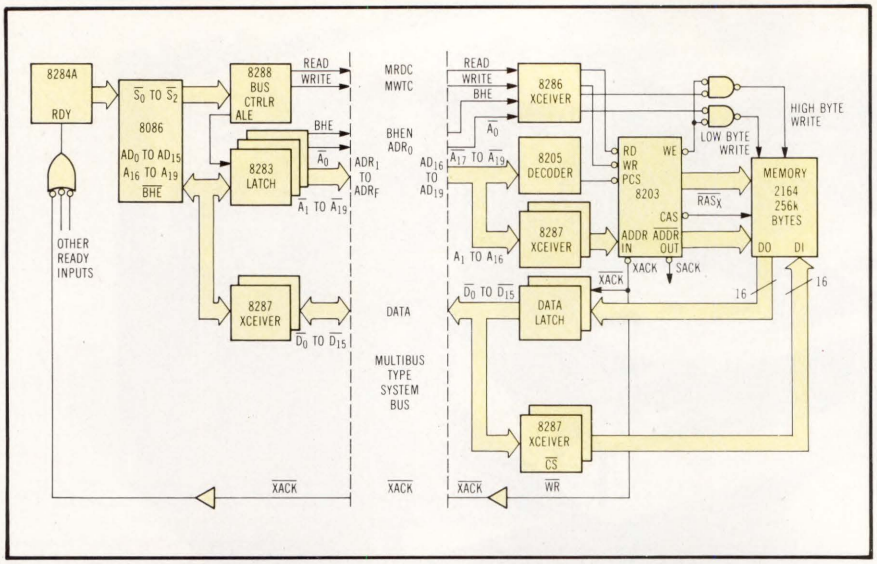

Fig 7 Typical global memory interface for microprocessor. Multiplexed address/data bus serves as local bus and demultiplexed address/data bus serves as global bus. Minimum or maximum mode operation is possible.

To illustrate the ease of interfacing global memories to the microprocessor, an iAPX86 system using an 8086 is shown. The multiplexed address/data bus is normally thought of as the local bus, and the demultiplexed address and data bus as the global bus. In much larger systems, it would be possible for the local bus to be demultiplexed immediately at the processor and for another bus that services the entire system to be the global bus. The system described works on either demultiplexed bus. The iAPX86 can be operated in either of two modes, minimum or maximum (Fig 7). In the former mode, the microprocessor generates the read and write commands directly, whereas in the latter mode, a bus controller such as the Intel 8288 is required. In this case, the iAPX86 outputs status bits S_0 to S_2 that are interpreted by the bus controller. Commands for read and write are now generated by the bus controller. Independent of the mode, the 8203 and memory interface identically to the microprocessor.

Ease of use or simplicity of design have been balanced against performance. The simple system shown (Fig 7) typically operates with one to two WAIT states required. For the minimum mode operation, the read (RD) and write (WR) commands occur too late in the memory cycle to allow the DRAM controller to generate a ready signal early enough to avoid WAIT states. Operation without WAIT states can be accomplished by transmitting advance RD or WR commands to the memory. This is a non-trivial task in the minimum mode because the iAPX86 produces the RD and WR signals in a fixed relationship after address latch enable (ALE) occurs. For maximum mode operation, the iAPX86 outputs status bit information ahead of ALE. With proper logic circuitry, these status bits can be decoded and the information used to initiate the advance RD and WR commands.

With a small amount of additional logic, it is possible to combine ease of use of the DRAM controller with high performance. As a result, the iAPX86 can operate at 5 MHz and requires no WAIT states unless the memory is

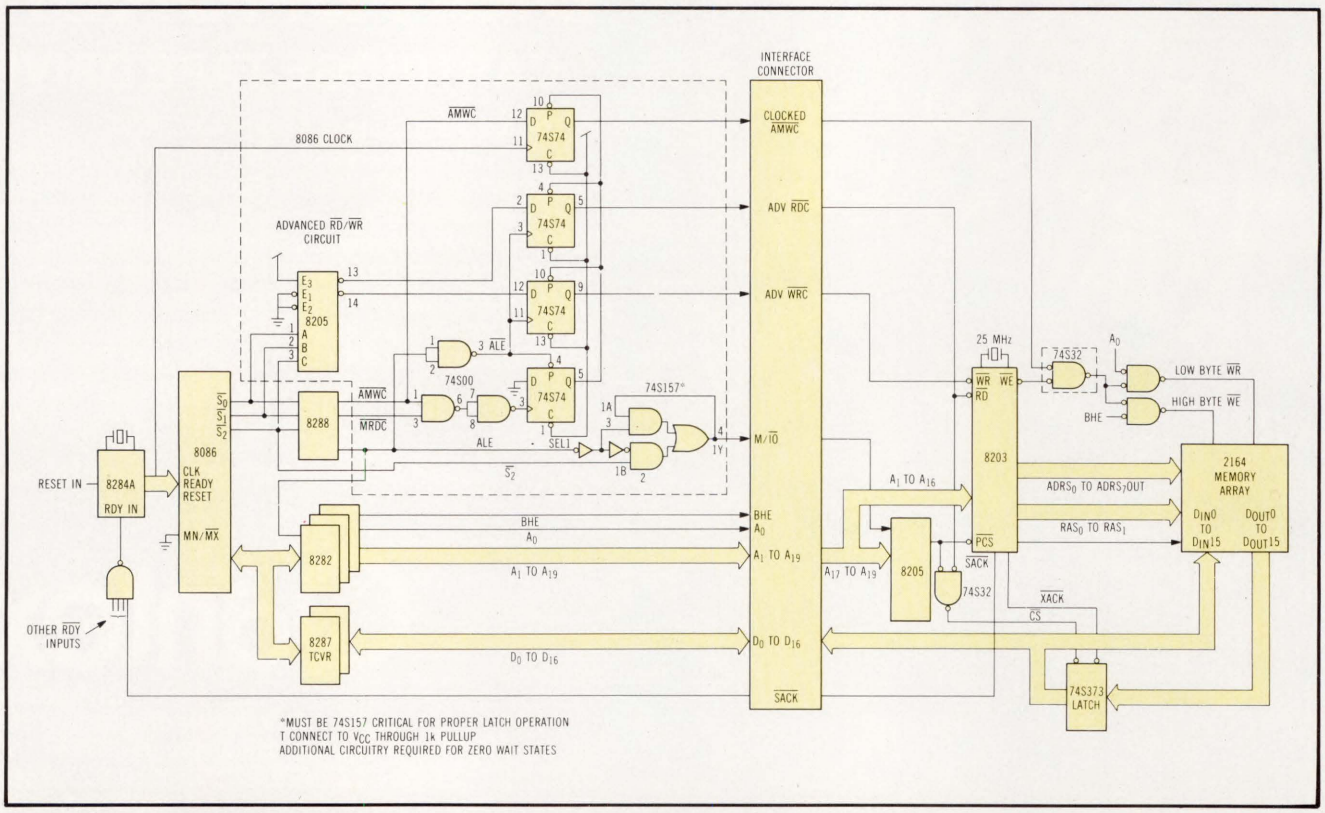

Fig 8 To achieve 5-MHz operation with no WAIT states, additional circuitry (dashed lines) must be added.

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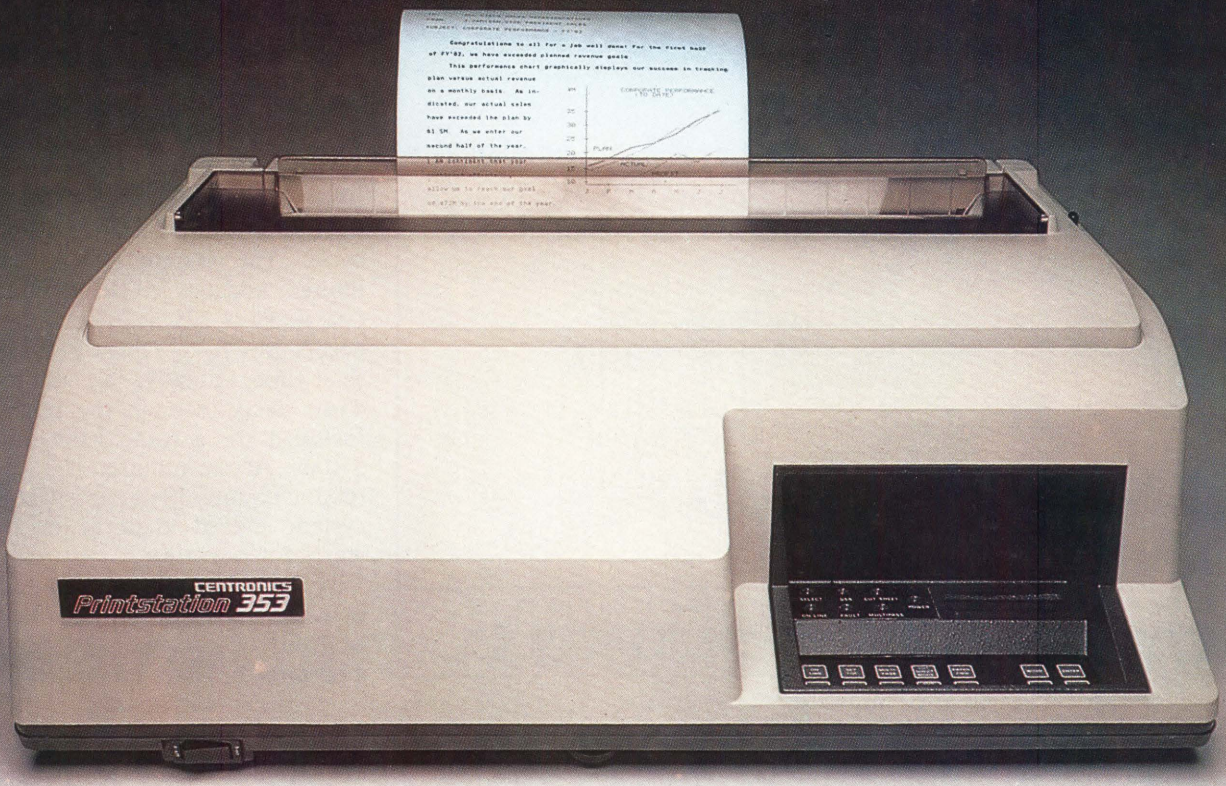

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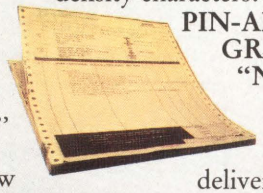

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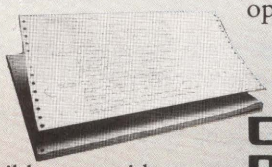

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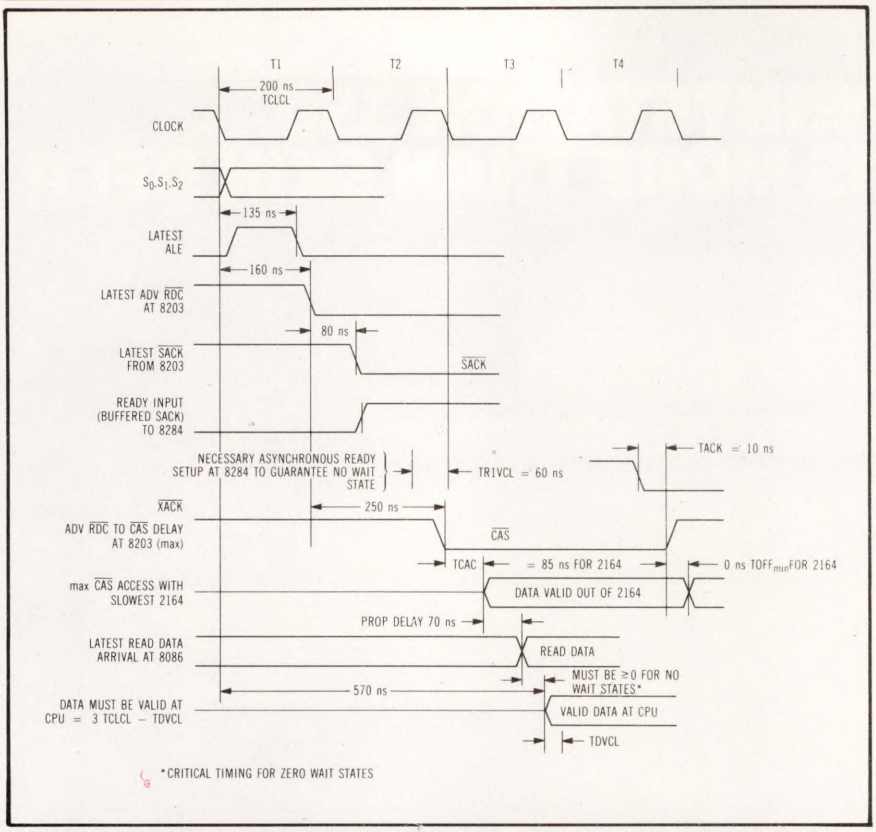


Fig 9 Read cycle worst-case analysis. Processor T states T1 through T4, are shown. For read without WAIT states, valid data must reach processor 30 μs before end of T3.

being refreshed. The circuitry added to the system is shown inside the dashed lines in Fig 8. The 8205 is a 3:8 line decoder which monitors the status lines. With the proper combination of status lines S_0, S_1, and S_2, an advanced RD command (ADV RDC) or an advanced WR command (ADV WRC) will be output on pin 13 or pin 14, respectively.

The RD or WR command, whichever is true, is latched by the corresponding 74S74 on the falling edge of ALE from the 8288 bus controller. Latch outputs at pins 5 and 9 (ADV WRC and ADV RDC) are entered into the 8203A WR and RD inputs directly. The two latches are cleared later on the trailing edge of either the memory read command (MRDC) or memory write command (MWRC) through the two 74S00 gates. System acknowledge (SACK)—used in place of (XACK) because it occurs sooner—is ANDed with protected chip select (PCS) and returned to the

Global memory can be easily built using only DRAMs and the... DRAM controller.

8284A, which provides a synchronous ready signal to the iAPX86. The S_2 status bit (memory operation) is latched by the 74S157 on the trailing edge of ALE. The 2:1 multiplexer is configured as a high speed flow-through latch by feeding the output back into the input. Propagation delay time is only 7.5 ns. The advanced memory write command (AMWC) is ANDed with WE to provide WE to the DRAMs.

Read cycle worst-case analysis (Fig 9) considers the maximum time delays. The four processor T states are indicated by T1 through T4. To read without WAIT states, valid data must reach the processor by the end of T3 minus 30 ns. The latest read data arrival at the processor does indeed fall within this time frame. The memory read cycle begins with ADV RDC (Fig 9), which is latched by the falling edge of ALE. ADV RDC reaches the 8203 at 160 ns into the cycle and begins access. Within 80 ns, SACK is valid and ANDed with PCS to be returned to the 8284A clock as READY. As a result, no WAIT states are required unless the DRAM controller is performing a refresh cycle. The system is CAS access limited, and as such the ADV RDC to CAS delay is 225 ns. The 85-ns CAS access time (t_{CAC}) must be added to this time. Finally, an additional 45-ns delay through the buffers is included for a total delay time of 510 ns. Access required is 3 T times (600 ns) minus 30 ns, or 570 ns. The system indeed requires no WAIT states for operation.

In the write cycle, the relationship between data and WE and the relationship of CAS and WE must be guaranteed. Data are written into the DRAM on the falling edge of WE. Consequently, data must be valid prior to the falling edge of WE. The skew of data from the processor and WR from the 8203 is such that it is possible for the data to be valid after the falling edge of WR. In this event, invalid data would be written into the memory as shown in Fig 10(a). In addition, DRAMs have a timing constraint, t_{CWL}, which is the overlap between CAS and WE. If CAS were early and MWTC were late, t_{CWL} would be violated as shown in Fig 10(b). Both of these requirements are satisfied by ANDing AMWC with WR.

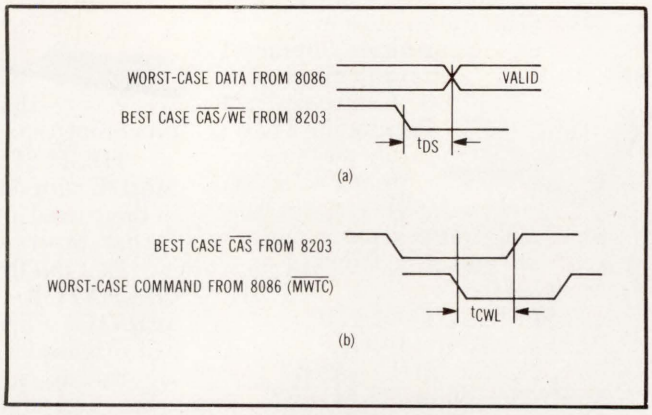
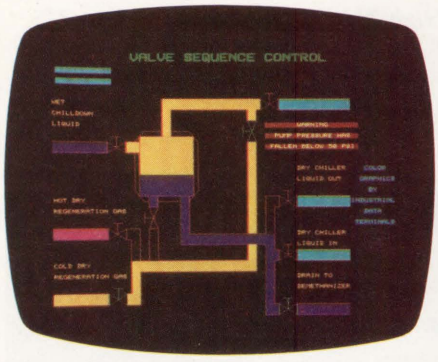
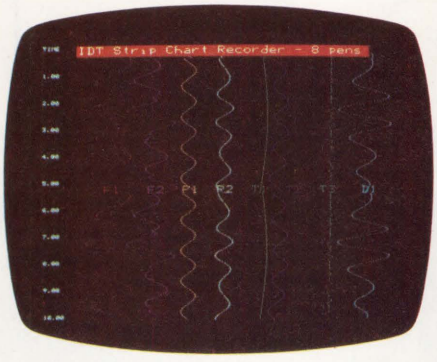


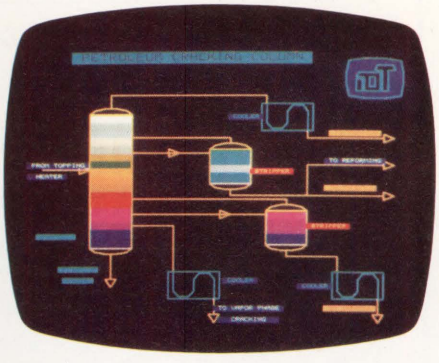
Fig 10 Required WE delay timing to memory

Fig 11 depicts the worst-case timing analysis for a write cycle, which is similar to that for the read cycle with a few exceptions. The ADV WRC is latched on the falling edge of ALE. The earliest that CAS can occur is 105 ns after ADV WRC starts the write cycle. Valid data are output from the CPU within 210 ns and reach the memory 35 ns later. By ANDing the AMWC with WR from

Bubble Breakthrough







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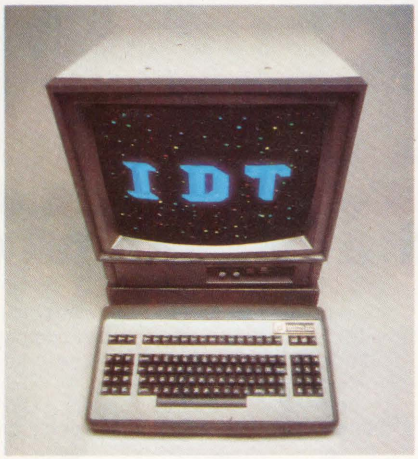

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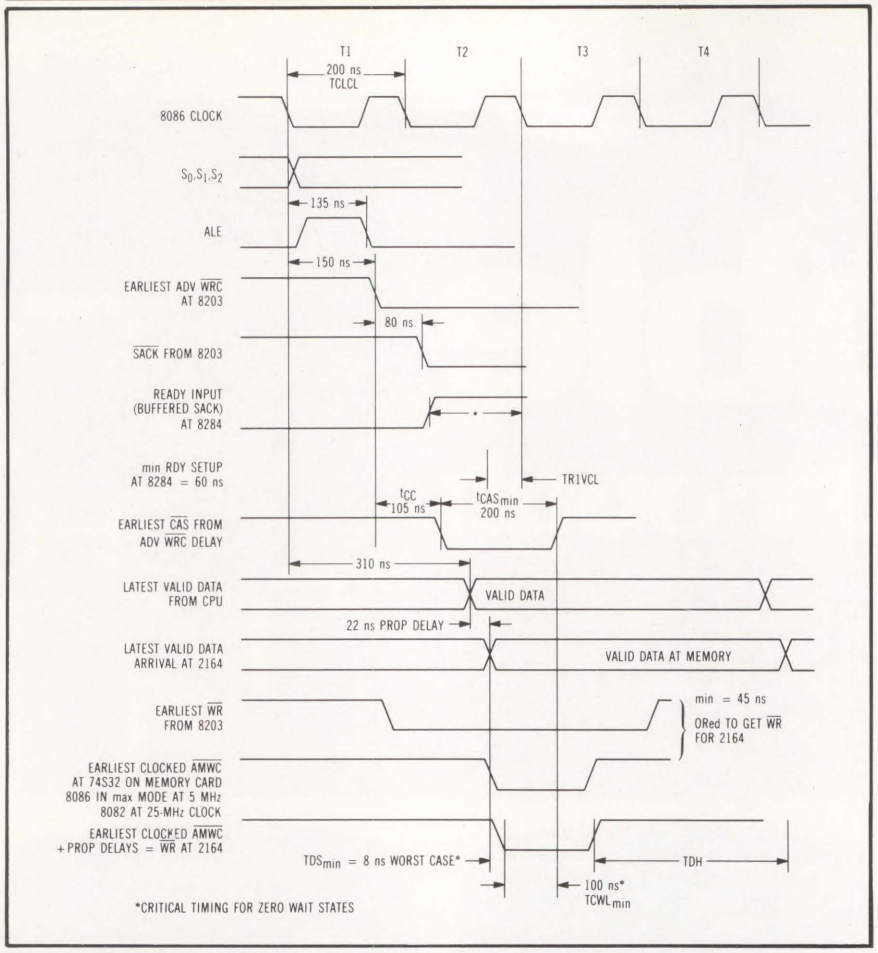

Fig 11 Worst-case timing analysis for write cycle

the 8203, WE falls a minimum of 8 ns after data are stable and valid at the memory. In addition, this ANDing guarantees a minimum t_{CWL} of 100 ns.

Overall system performance is improved by using global as well as local memories. Global memory can be easily built using only dynamic RAMs and the 8203 dynamic RAM controller. Performance, together with ease of use, is achieved by adding just five TTL components. The design of a 5-MHz system that runs without WAIT states is a good example of this approach.

Acknowledgment

The author would like to thank Bill Righter and David Chamberlin for their help in preparing this article.

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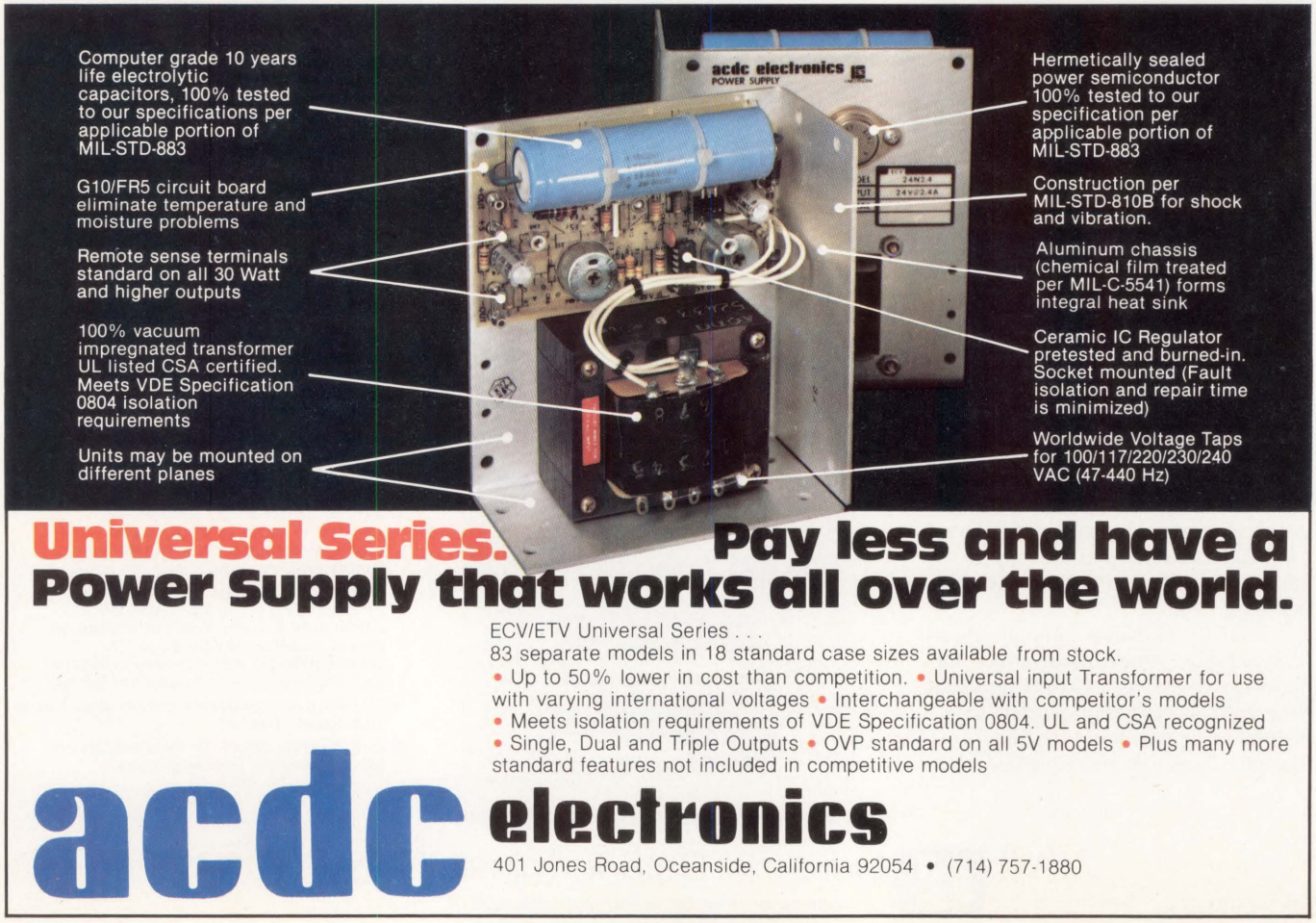

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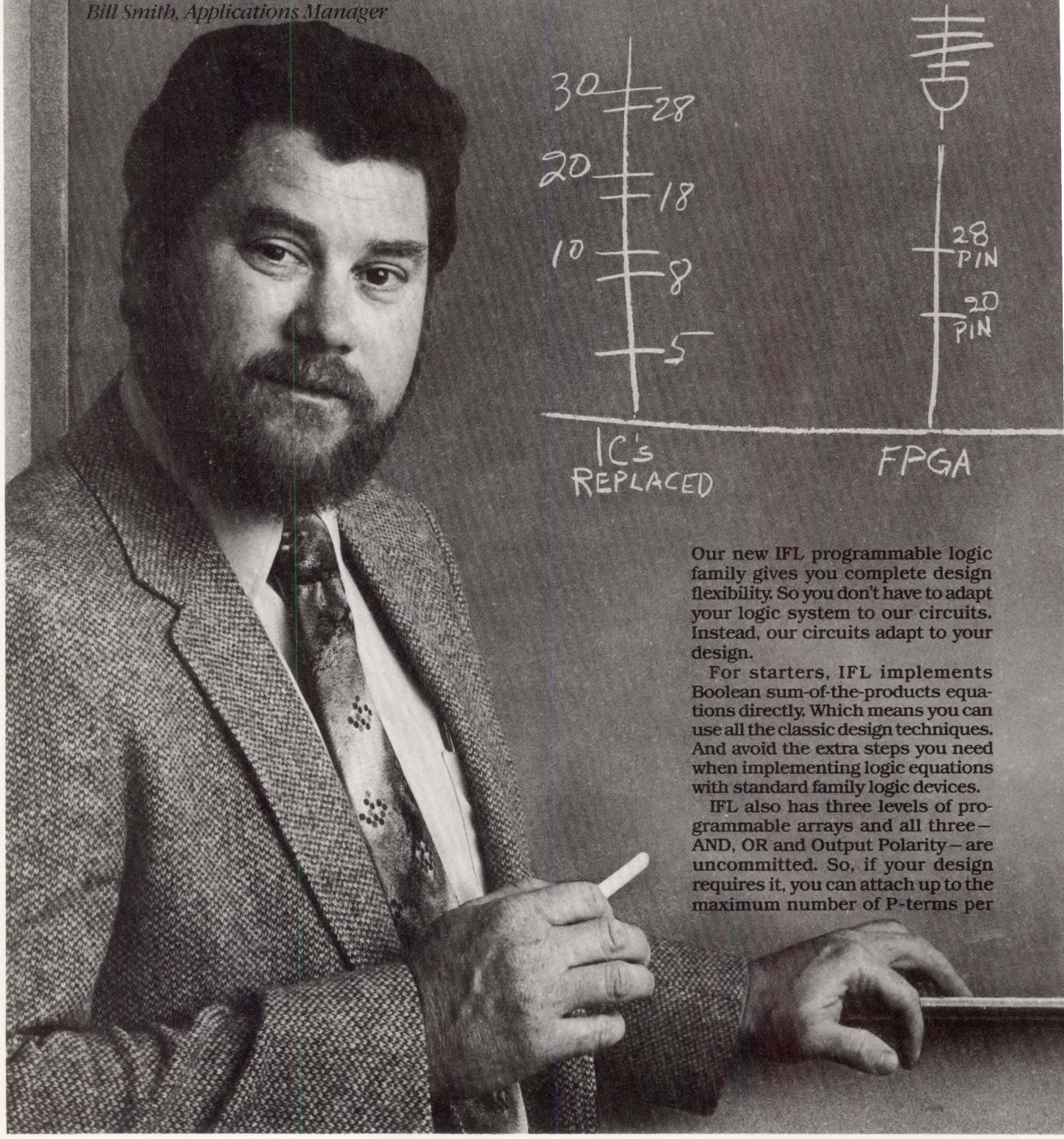

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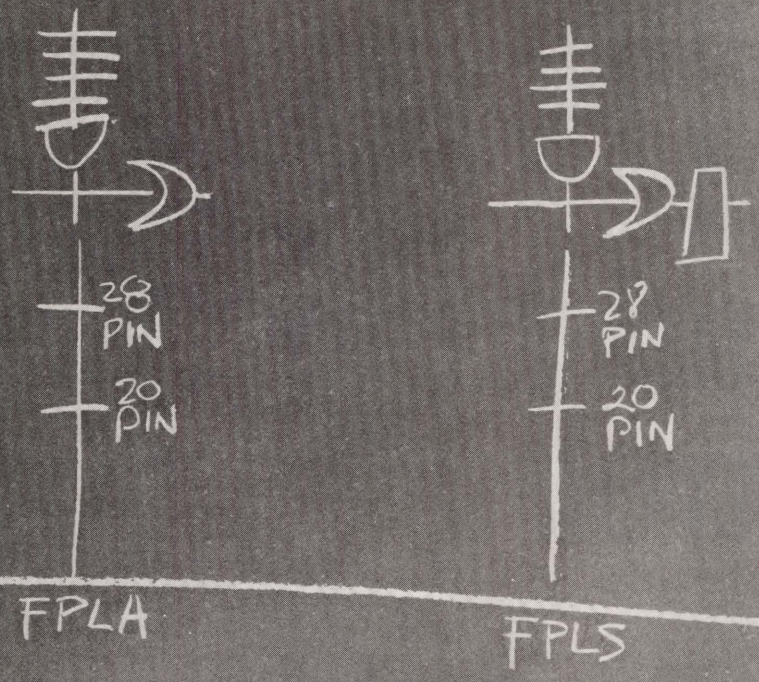

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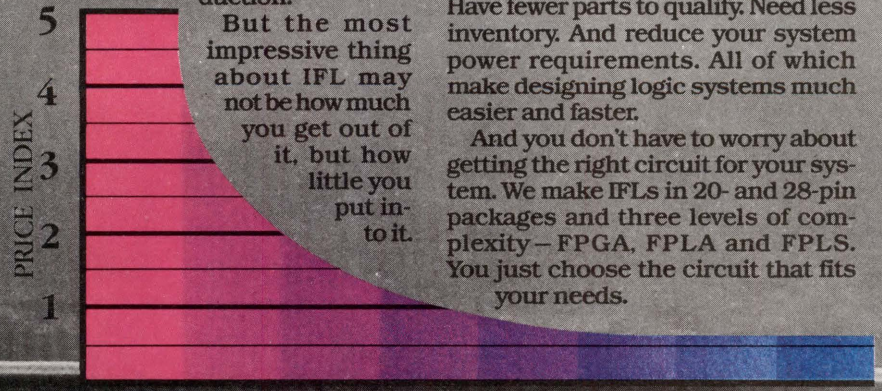

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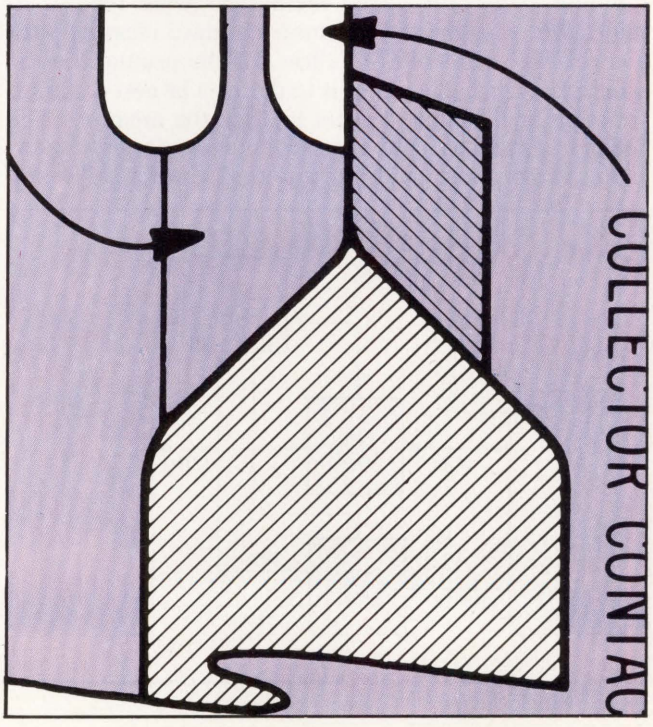
A VLSI APPROACH TO CACHE MEMORY

The push for large cache memory products will soon be satisfied by VLSI building blocks

by Bruce Threewitt

Development of a memory hierarchy establishes use of faster, more expensive memories in smaller data buffers—called cache memories—while slower, less expensive devices are used in the mainframe. Cache memory technology assumes that data next required by the CPU are near current program or data activity. Thus, whenever required information is not in the cache, references to slower main memory load a block of data surrounding the required location. Fig 1 illustrates the cost/performance tradeoffs confronting memory system designers, which gave rise to use of a memory hierarchy.

One measure of a cache memory performance is the so-called hit ratio, which is the percentage of data references found in high speed memory. In this technique, the hit ratio weights an average performance in favor of the cache memory. At the same time, the average memory cost per bit is weighted in favor of the slower, lower cost mainframe memory. Unfortunately, approaches to cache memory designs have not been standardized. Microcode implementations for the various functions differ significantly. For example, the associative tag buffer can be fully associative (any block in main memory mapped to any block in cache) or set-associative (any block in main memory mapped to a specific "set" of blocks in cache). With a slight performance penalty, a set-associative algorithm simplifies the tag buffer hardware; the data cache can be simplified in the same way. Another difference involves whether or



Bruce Threewitt is responsible for product planning and applications engineering of memories and interface products at Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94086. His experience in the semiconductor industry has ranged from design engineering to strategic marketing. Mr Threewitt holds a BSEE from Oregon State University.

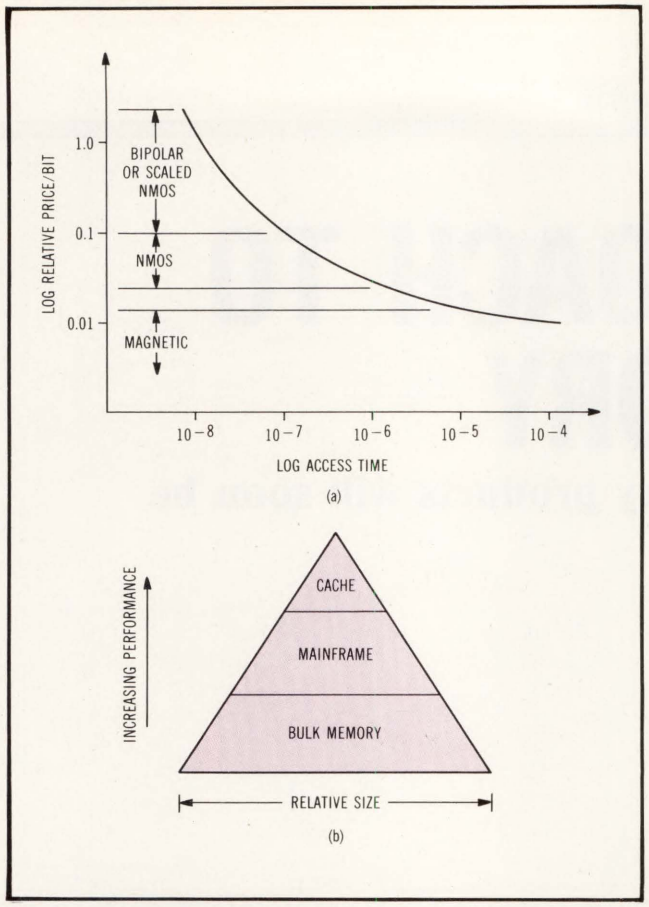


Fig 1 Cost/performance curve (a) confronting memory system designers encourages use of memory hierarchy (b).

not the main memory is to be updated when a cache write operation occurs. Such options make defining a common cache building block a difficult task. Fig 2 diagrams one typical approach.

VLSI semiconductor solutions to these problems will become economical only when system approaches are standardized. Two approaches to defining a common building block for cache memories come readily to mind. One is to build a common standard memory with a specialized controller to allow for the peculiarities of specific designs. The other is to define a largest common function and include control logic in the memory. The former approach offers cost advantages, possibly sacrificing performance and pin count. The latter solves the

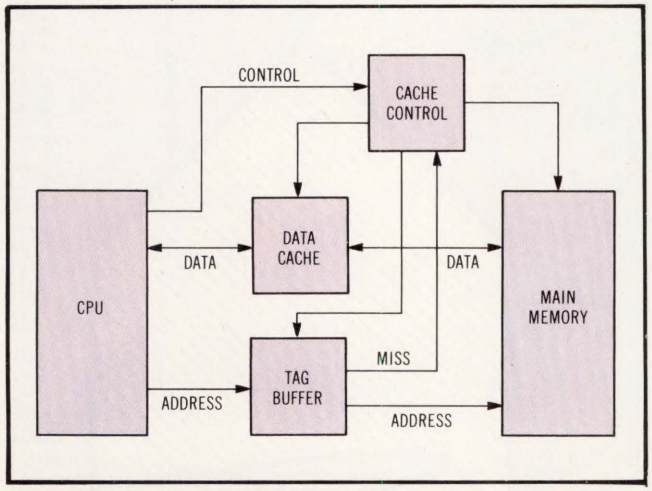


Fig 2 Block diagram of typical cache memory

speed and pin count problems by trading off cost and universality.

Packaging imposes another constraint upon cache memory systems. Cache environments generally require long word structures. In a standard memory with a cache controller, the controller requires many pins to handle both address and data paths. Integrating memory and control functions on the same chip alleviates this problem somewhat, as do denser packages with higher pin counts (eg, leadless chip carriers).

Cache memory systems already share some common features. Cache memory depth is usually in the 1k- to 8k-word range, and word lengths range from 16 to 64 bits. Since present memory capacities easily meet these requirements, additional complexity can be devoted to control logic. Pin constraints will probably limit the devices to 4-bit organizations.

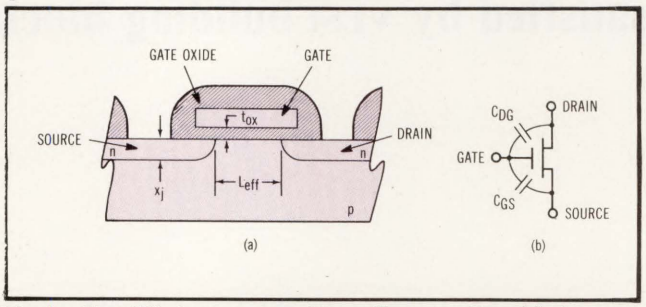


Fig 3 Simplified NMOS transistor. Cross-section (a) shows where enhancements increase density by shrinking transistor's horizontal dimension (effective gate length, L_{eff}) and vertical dimension (oxide thickness, t_{ox}; and junction depth, x_j). Schematic for device is in (b).

Characteristics of VLSI memory technology

Memory technologies concentrate on small transistors because memory cell area is dominated by active devices requiring relatively few interconnections. When an integrated circuit design combines memory and logic functions, such as in a cache memory, interconnections must be minimized—even if this means duplicating functions at various locations onchip. All memory technologies share this characteristic. Memory efficiency, the ratio of total memory cell area to total chip area, increases with density. Thus, additional control functions have less impact on the chip size of denser devices. These factors make memories with integrated control functions more attractive. Three technologies are candidates for cache memory devices: scaled NMOS, bipolar, and scaled CMOS.

Scaled NMOS. During the past decade, n-channel silicon-gate metal oxide semiconductor (NMOS) technology has become the workhorse for VLSI memories. Until recently, however, performance of cache applications for this low cost memory technique have been limited. Fig 3 shows a simplified NMOS transistor. Generally, NMOS enhancements are aimed at higher density and lower cost; in addition, scaled NMOS technique improves performance. Shorter channel lengths, lower threshold voltages, and reduced parasitic load capacitance increase speed. Scaled NMOS RAMs with 45-ns access times are currently available with densities in the 4k- to 16k-range. Designs of the next generation are targeted at 35 ns, with even higher densities. Scaled NMOS memories are generally transistor-

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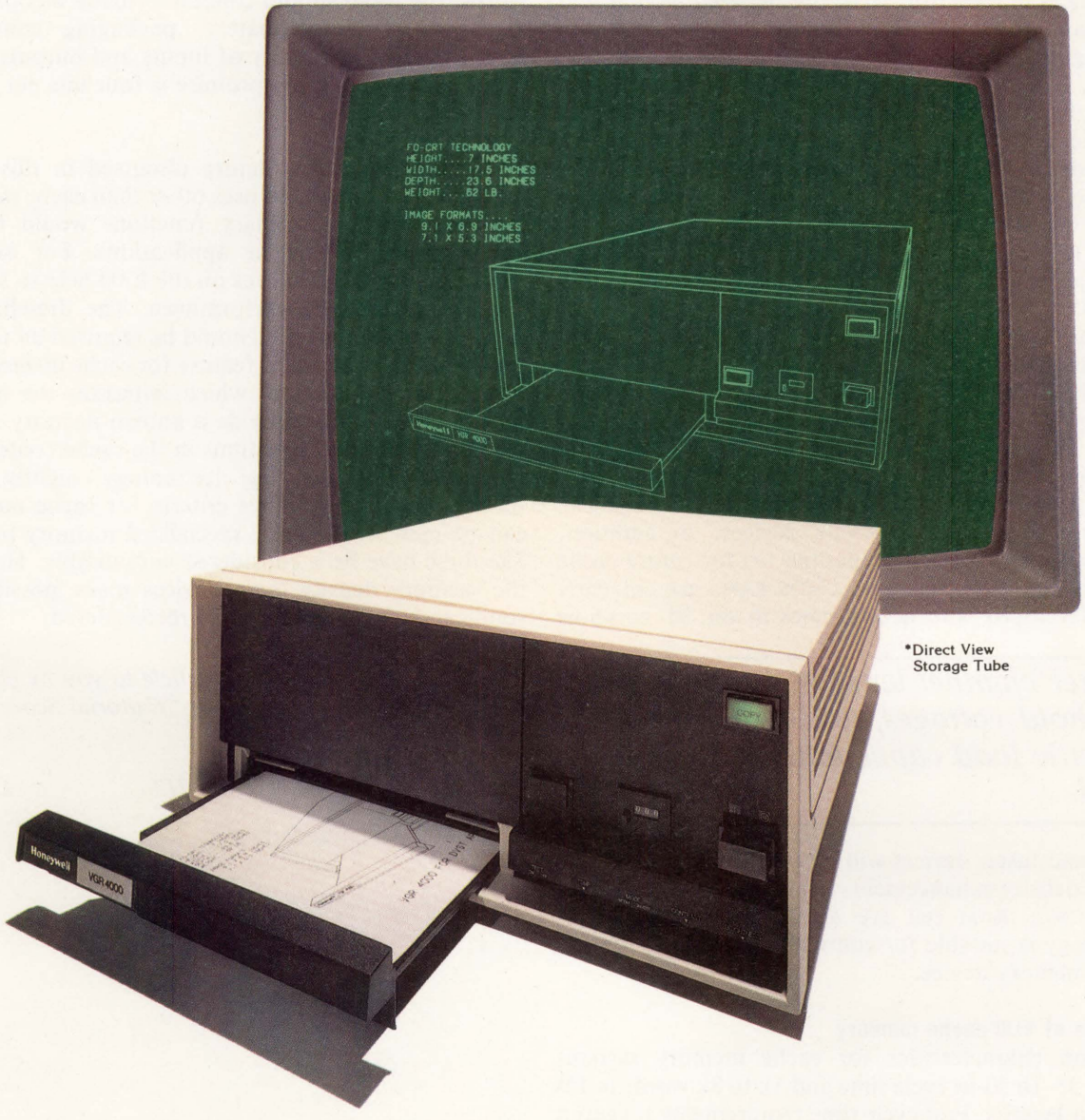

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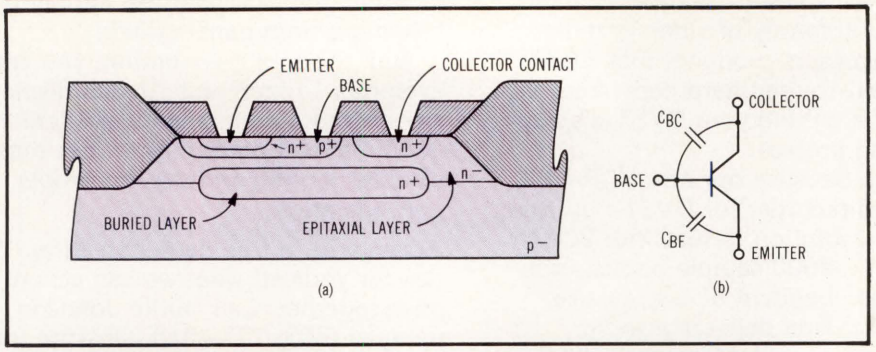

Fig 4 Simplified bipolar transistor. Cross-section is diagrammed in (a). Schematic (b) shows where reductions in parasitic impedances (such as C_{BC}, the so-called Miller capacitor) can improve performance in bipolar memories.

transistor logic compatible at the inputs and outputs. As cache speed requirements increase, a transition to emitter-coupled logic (ECL) compatible I/O is likely. Unfortunately, NMOS does not easily provide ECL levels.

Bipolar. Until recently, high speed memories have been the sole province of bipolar memory technologies. Differences in transistor structure between bipolar and NMOS can be seen by comparing Figs 3 and 4. As design rules tighten, scaling can also be applied to bipolar devices. Unlike NMOS memories, bipolar memories are inherently ECL compatible. In fact, many bipolar memories use ECL internally and translate to transistor-transistor logic levels only at the interface. This technology will provide a ready solution as ECL compatible caches become necessary. As is the case with NMOS RAMs, pin constraints will probably limit organization to 4-bit words per device, with access times in the 35-ns range. ECL RAMs are heading toward 25 ns in the next generation, and faster devices are currently being studied.

Scaled CMOS. Complementary metal oxide semiconductor (CMOS) technology offers improved performance, noise margin, and power dissipation over NMOS, with some increase in process complexity. The same scaling techniques applied to bipolar memories result in similar performance of CMOS devices. In addition, CMOS can provide ECL compatible I/O for future cache performance enhancements. CMOS RAMs are currently being developed with access times in the 35- to 45-ns range, and faster devices will be available in the future. Several density enhancements to reduce the area penalty for a CMOS RAM cell are also being studied. This technology is suitable for control logic implementation on the memory device.

Shorter channel lengths, lower threshold voltages, and reduced parasitic load capacitance increase speed.

Features of VLSI cache memory

Optimum characteristics for cache memory systems feature 35- to 50-ns cycle time and 1k to 8k words in 16- to 64-bit lengths. Fast cycle time requirements suggest a static RAM implementation. Lower cost, dynamic RAM approaches are inadequate because they require longer cycle times. Since the ratio of cache memory bits to main memory bits is small, cache memory cost per bit does not contribute significantly to overall system cost. In other words, a less dense technology would be appropriate—such as bipolar NMOS (using static RAM circuitry) or CMOS—as long as the speed targets can be met.

Since sufficient address space for the entire cache may be contained on one RAM device, power-saving features, such as power-down from chip enable, are not useful for cache oriented RAMs. Thus, although word length is assembled from several RAMs in parallel, cascading RAMs for additional address space is seldom necessary. Considering how few cache memory chips are needed for each system, the cache does not contribute significantly to the overall power requirement for the system.

To facilitate a memory comprising 16- to 64-bit words, the RAMs should contain as many bits per word as possible. Unfortunately, packaging constraints quickly limit the number of inputs and outputs on the RAM. A reasonable compromise is four bits per word.

Conclusion

The standard RAM structure discussed in this article might also be applied to uses other than cache memory. However, certain ancillary functions would be particularly useful in cache applications. For example, separate inputs and outpus on the RAM help to simplify the peripheral logic performance. The drawback, of course, is that more pins would be required on the RAM package. Another useful feature for cache memories is a memory clear function, which initializes the memory during power-up to provide a known memory content for the associative algorithms in the cache controller.

By extending existing technology slightly, these features and performance criteria for cache memories can be met. In the past, specialized memory products like these have been considered unfavorably. However, the memory density these devices make possible will soon cause that position to be reconsidered.

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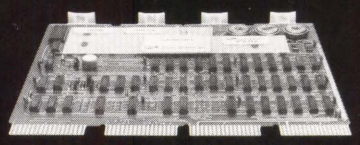

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3608						X	X	X	X	X	X	X	X		X	X	X	X		X	X	NONE
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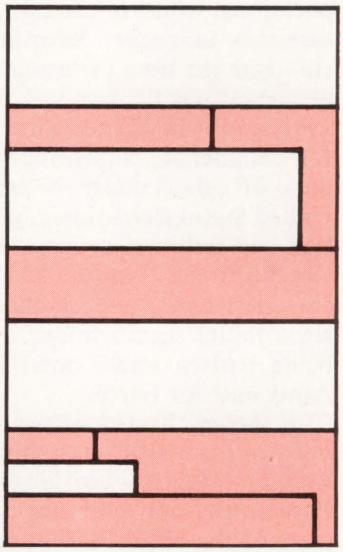

by Douglas E. Wrege

Sharp reductions in hardware cost over the last few years have led to great expansion in microcomputer applications. While many microcomputers retain their identity as small general purpose computers, others have become special purpose devices that are permanently embedded in products; users are often unaware that these devices contain computing capability. Microcomputers are appearing in countless products that formerly used either hardwired logic or no logic at all, and are vastly enhancing their performance—often at a significantly lower cost.

Since software development goes along with hardware application, however, the steeply rising cost of software will be a severe problem in the 1980s. For special purpose microcomputers, moreover, there seems to be direct conflict between the two major objectives of software development: minimizing program cost and maximizing program efficiency. In the first objective, the idea is to equip programmers with software development techniques and tools that will minimize programming time. In the second objective, applications are programmed in a manner that will produce the fastest execution time and require the least space in memory. Conflict arises because conventional methods are not able to achieve both objectives in microcomputer software: the programmer must shoot for one or the other.

Conventional methods are based on writing programs for microcomputers with the software tools that are available on the microcomputer itself, just as is done routinely for larger computers. Although using a high order language (HOL) saves the programmer's time, the program usually executes more slowly and requires more main and secondary memory. Conversely, programming in assembly language improves program efficiency, but is painstakingly slow and therefore very expensive.

Assembler coding provides the fast execution time that is essential in most realtime applications; if the volume is large enough, a saving of even one read only memory chip in the microcomputer's central processing unit can be worthwhile. Also, if the program is embedded in thousands of units, the high programming cost is not critical. Now, at least in part because programmers have more confidence in the process, almost all special purpose programs are written for microcomputers in assembly language, whether or not program efficiency is critical.

As microcomputer applications expand, however, minimizing program cost and achieving adequate

Douglas E Wrege received his BS in physics from the University of Rochester, and his MS and PhD in physics from the Georgia Institute of Technology. This article was written while the author was senior research scientist at the Systems Engineering Laboratory, Engineering Experiment Station, Georgia Institute of Technology, Atlanta, Ga. Mr Wrege has specialized in developing embedded realtime software systems, and is now at work on an Ada programming support environment.

program efficiency will become crucial. Hosted software development offers the most effective technique for meeting both demands. Although it is a well-known programming concept, hosted software has been developed in limited applications. Until recently, the urgency of the need was not fully recognized, and so the necessary software tools have been unavailable.

In hosted software development, application programs are written and debugged in an HOL on a large machine, then cross-compiled for running on a microcomputer or small minicomputer. Programming time is substantially less than with microcomputer based HOLs because of the superior software (including the HOL itself) on the large machine. In addition, the machine code that is generated by a host based HOL translator (a compiler) can be more efficient and more maintainable than code written in assembler on the microcomputer itself.

Fortunately, hosted software development will receive a big boost within the next several years with the advent of the Ada language. Ada, a powerful HOL, was designed specifically for realtime embedded military applications, which historically have depended heavily on assembly language. Revolutionary constructs in Ada eliminate the need for assembly language. The first implementations of Ada will be in the public domain in 1983, and Ada will be available (and equally applicable) for commercial/industrial systems. Ongoing development of Ada is under the technical management of the United States Department of Defense, with the cooperation and technical support of the defense ministries of Great Britain, France, and Germany. Ada has been fully designed, a process that has taken over four years since initial specification, and the first compilers are being written under contract with the United States Army and Air Force.

In theory, hosted software development can be applied with any HOL, even though it is most advantageous with a strongly typed language like Ada (or perhaps Pascal), the only currently available language that has most of the required features. But the choice of HOL, host computer, and target microcomputer will be limited for some time by the availability of software tools.

Application programming on microcomputers

Programmers use a variety of tools in writing application software on a microcomputer: operating system (OS), editors, assembly languages, HOLs, and debuggers. The major steps involved in using software tools for programming on a microcomputer in an HOL or assembly language are preparation, translation, linking, and debugging.

First, the program is written in the form of a series of instructions (in an HOL) or operational codes (in assembler), then entered into the microcomputer with the help of editor software. Editors are OS dependent utility routines that vary widely in function from machine to machine, but are limited in microcomputers. The program can be written in modules or as an integrated whole, depending on its size and the capability of the language. Next, the machine translates program modules from instructions (HOL) or operational codes (assembler) into binary machine code and assigned memory locations. Errors are detected in the translation process, program changes implemented by the programmer, and code is retranslated until it is correct as far as can be determined at this stage. After translation, two or more program modules are linked into a complete, integrated program by special software or firmware. Then the program is run in an application environment, and debugging software is used to identify problems. Problems are solved by revising the program at the preparation stage and proceeding through the remaining stages. Because bugs are often interdependent, the programming cycle may have to be repeated several times before the affected modules are discovered.

The main advantage of an HOL over assembly language is the significantly lower cost of application programming. The cost of a single software statement is largely independent of whether the statement is programmed in assembly language or in HOL. Furthermore, an HOL written program is likely to have only from one-fifth to one-tenth as many statements as an assembler written program for an equivalent computing task.

A major problem in writing assembler code is poor maintainability. Generally, the longer a program is used, the more frequently it will be changed. Modification tends to be a corrupting process, and successive enhancements make code more obscure. Ultimately, the code cannot be understood at all—the program has become enhancement-proof—and further modifications can be made only with a fresh start. An HOL program, since it consists of far fewer statements, is inherently more understandable and easier to modify than an assembler equivalent. The longer a program is expected to last, the more important superior maintainability becomes.

The difficulty with programming a microcomputer, either in assembly language or in HOL, lies in the limitations of the software tools at each stage. For example, the microcomputer's OS cannot offer the variety of data management tools (eg, methods of file access, intertask communication constructs, and spoolers) that are available on larger machines with richer OSs. Microcomputer editors are not as versatile, and the HOL, which may be only a subset of the full language, is simply unable to generate the most efficient code.

Application programming on large computers

Application programming on a computer with substantial memory and an extensive assortment of software tools provides a superior environment for programming in an HOL. For instance, Digital Equipment Corporation's VAX-11/780 has 2G bytes (2000M bytes) of address space, many times the 2M bytes that might be needed for a production quality optimizing compiler. Because of its comprehensive virtual memory system, the OS permits many programmers to work simultaneously (24-port capacity at present) in several languages

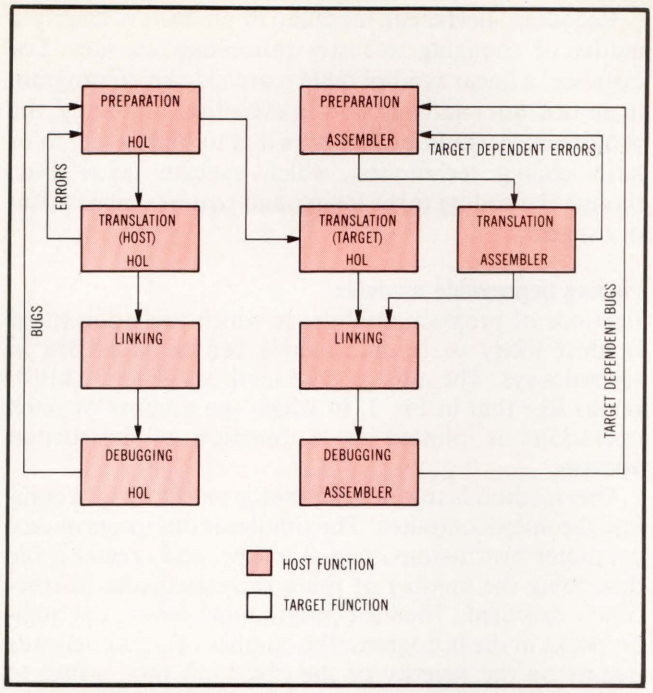

Fig 1 Initial steps in writing application program for target machine on host computer in HOL (left) are identical to major steps in programming a microcomputer, either in assembly language or in HOL. Retranslation and linking of debugged program modules follow (right). Finally, debugging in target machine may be necessary to meet application conditions.

(FORTRAN, COBOL, and Pascal, among others). Its program development tools include an excellent HOL debugger and such system utilities as cross-reference listing, source compare, and versatile editor assortment. Human orientation and a high degree of interactivity in the system software enhance programmer productivity.

Programs that are written to run on a large machine are developed with a procedure that is identical to the procedure for programming a microcomputer. The difference is that mainframe software at each stage does a great deal more for the programmer. In translation, a strongly typed language like Pascal or Ada checks ranges and variable usage (FORTRAN does not); consequently, program modules are "cleaner" before they are linked for debugging.

If certain variables have been defined, such as A = integer and input, B = real and output, and C = real and input/output, a mainframe translator will check that a call of SUBR (A, B, C) always has integer, real, and real in sequence. If this routine is called in another module with (X, Y, Z), then X, Y, and Z must agree in type or the error will be flagged in translation. If the translator does not have this ability, the error will not turn up until the debugging stage, when it will be much more difficult to correct.

After linking, the debugging process is simplified in a large machine, both because there are far fewer bugs to handle and because the HOL based debugger program provides more specific analysis information than an assembly language debugger. A programmer can ask the VAX-11/780 debugger, for instance, to print out specific values in selected variables in the source language. When programming in assembly language on a microcomputer, on the other hand, the specific addresses for printout must be stated, even though the programmer may not be sure about what they are. When programming in an HOL on a microcomputer, the programmer needs an assembly language listing to find out what debug lines are equivalent to what HOL instructions.

Application programming on a host for microcomputers

Hosted software development begins with the complete procedure shown at left in Fig 1. After translation and debugging, the now-correct program modules are retranslated in a cross-compiler designed for the particular microcomputer that is the target machine. The hosted linker integrates the software modules and produces the bit patterns for an executable program in the target.

Since the host usually cannot run the linked microcomputer program, it is downline-loaded by wire or magnetic tape to the target machine. There, it may be necessary to debug certain modules with regard to application needs, such as special interfaces or realtime data loading. Target debugging involves revising and retranslating program modules, as well as relinking the module into the program on the host.

Target debugging of hosted software is normally handled in assembly language. If the target microcomputer is linked to the host, however, the target can communicate with a host program that has access to data generated by the compiler and linker. Then, since the target debugger can recognize HOL constructs, the

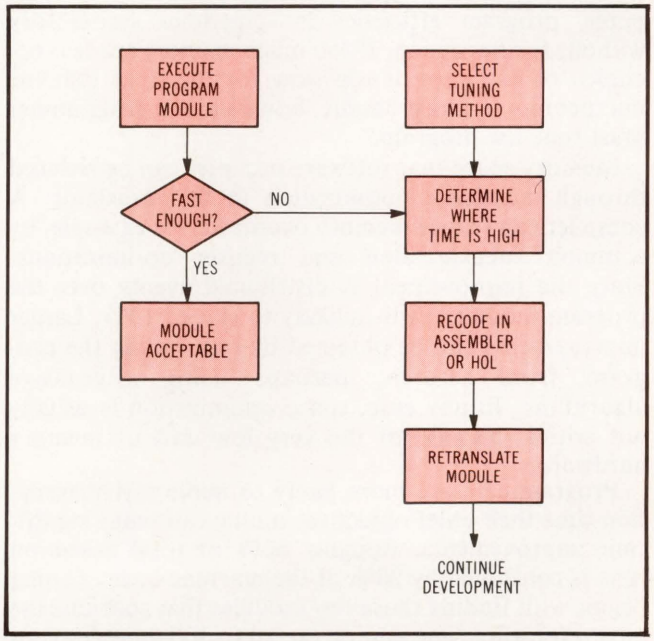

Fig 2 Microcomputer program is tuned by selecting modules in which execution time seems to be high; then unacceptable modules are identified and subroutines recoded.

Fig 3 Histogram that gives number of fetch operations as function of instruction address in memory will identify subroutines that consume a large proportion of total execution time.

programmer can debug in the HOL. Although limited, the target debugger can still be effective because host debugging software provides the functions that the target program cannot handle.

Program tuning

In running host developed software on a microcomputer, program efficiency is sometimes satisfactory without further action. If too much memory space is occupied or execution is too slow for the tasks that the microcomputer must handle, however, the programmer must tune the program.

Memory space that software occupies can be reduced through automatic optimization in the translator. A compiler can reduce memory overhead, for example, by common subexpression and register optimizations. Since the improvement is distributed evenly over the program modules, it is unlikely to exceed 10%. Larger improvements can be obtained by redesigning the program from scratch, perhaps using alternative algorithms. In any case, space optimization is usually not critical because of the very low cost of memory hardware.

Programmers are more likely to make faster execution time their chief objective; tuning can make significant improvements. Roughly 80% of total execution time is consumed by 20% of the machine code. Tuning begins with finding those few modules that consume the most execution time among the 10 to 100 modules constituting the complete program. As shown in Fig 2, each program module is executed and its speed determined as acceptable or unacceptable in terms of what the computer must accomplish. Time-heavy portions of the modules are recoded in assembler or HOL on the host, retranslated, and debugged.

Writing the original program in an HOL on the host and recoding only the few sluggish modules—even in assembly language—is substantially faster than coding the entire program in assembler. As a matter of fact, total execution time might often be shorter with hosted development because the programmer's efforts are concentrated on assembly coding only where the return on investment is highest.

Recoding inefficient modules in an HOL is largely a matter of changing to faster processing schemes. For instance, a linear symbol table search is easy to program in an HOL but relatively slow in execution. In tuning, the programmer would probably switch to binary search or hash coding techniques, which execute faster even though the coding takes longer and requires more memory space.

Finding improvable modules

Portions of program modules in which execution speed is most likely to be improvable can be identified in several ways. The most precise methods generate histograms like that in Fig 3, in which the number of fetch operations is plotted as a function of instruction address.

One method is to run a simulator on the host to emulate the microcomputer. The simulator interprets microcomputer instructions, one at a time, and creates a file describing the number of times each particular instruction is executed. Then the programmer selects the highest peaks in the histogram (the number of peaks depends mainly on the severity of the execution time problem) and takes programming steps to reduce them. If a peak's instruction addresses indicate that a symbol table search routine is the offender, for example, the programmer can reduce the number of instructions involved in the symbol table subroutine (make the peak narrower) and/or reduce the number of times that particular instructions are used in the subroutine (cut down the peak height).

Another way of generating such a histogram is to provide an extra clock to introduce random interrupts in the program as it runs on the target machine. An asynchronous control transfer routine interprets and stores the instruction that is executing at the time of each interrupt. Advantages of this method are that a control transfer routine is much easier to write than a simulation program, and that the tuning is done on the target machine itself (provided that there is enough space in the target's memory for the histogram file).

A third method is to build a histogram file in a separate machine by monitoring the program counter on the microcomputer. The histogram run is faster than in the interrupt clock method, the target memory is not involved, and the programming time is about the same. However, it may not be convenient to link the microcomputer to another computer.

One of the simplest methods of identifying the most frequently executed instructions is to tie a storage oscilloscope to the internal instruction bus between the program counter and main memory. In tuning a program for a 16-bit microcomputer, one oscilloscope probe is linked to one byte of the program counter and the other probe to the other byte through a digital to analog converter. The spot on the screen will be deflected rapidly as the bit patterns change in the two bytes of the program counter. The several brightest spots on the screen represent memory addresses that are being accessed most frequently by the central processing unit.

A software approach that is far less precise than a simulator, but which is often effective, involves no special hardware or software. The programmer first makes educated guesses about which subroutines are at

fault. A NOP (no operation) instruction is then inserted into one routine at a time, and the program module is run to see whether the total execution time has been appreciably changed. Even when virtually certain that a particular subroutine can be significantly improved, the programmer should confirm that assumption with the NOP method because it can be completed quickly.

The missing tools

Without question, hosted software development will eventually be used widely. How long that will take depends on the availability of cross-compilers for the numerous microcomputers that are finding their way into military devices and commercial products.

The missing software is actually only part of a cross-compiler, which can be constructed as shown in the diagram in Fig 4. The front end of a cross-compiler comprises a syntax analyzer and an HOL dependent optimizer, both of which are language dependent but identical for any target machine. The back end of a compiler comprises a target dependent optimizer and target dependent code generator, sometimes referred to jointly as a code generator. The code generator must be customized for each microcomputer whose software is being developed on the host.

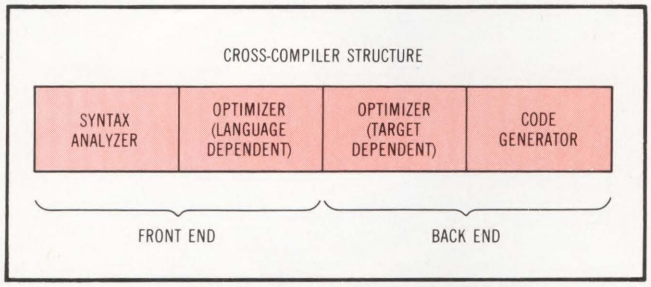

Fig 4 Cross-compiler includes some software elements that are applicable to all target machines (front end) and others that are target dependent (back end).

Pending the release of Ada host and cross-compilers, hosted software development will be used most advantageously with the Pascal language. However, Pascal does not permit independent compilation of program modules, a characteristic of Ada that is assumed in the hosted development procedure described in this article. While this is not serious in small programs, larger microcomputer programs can be written more effectively by several programmers working independently. In addition, Ada has more inherent realtime capability than Pascal and is easier to use in the multitasking mode.

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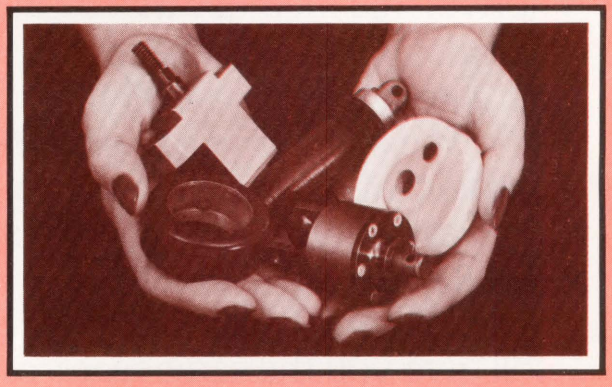

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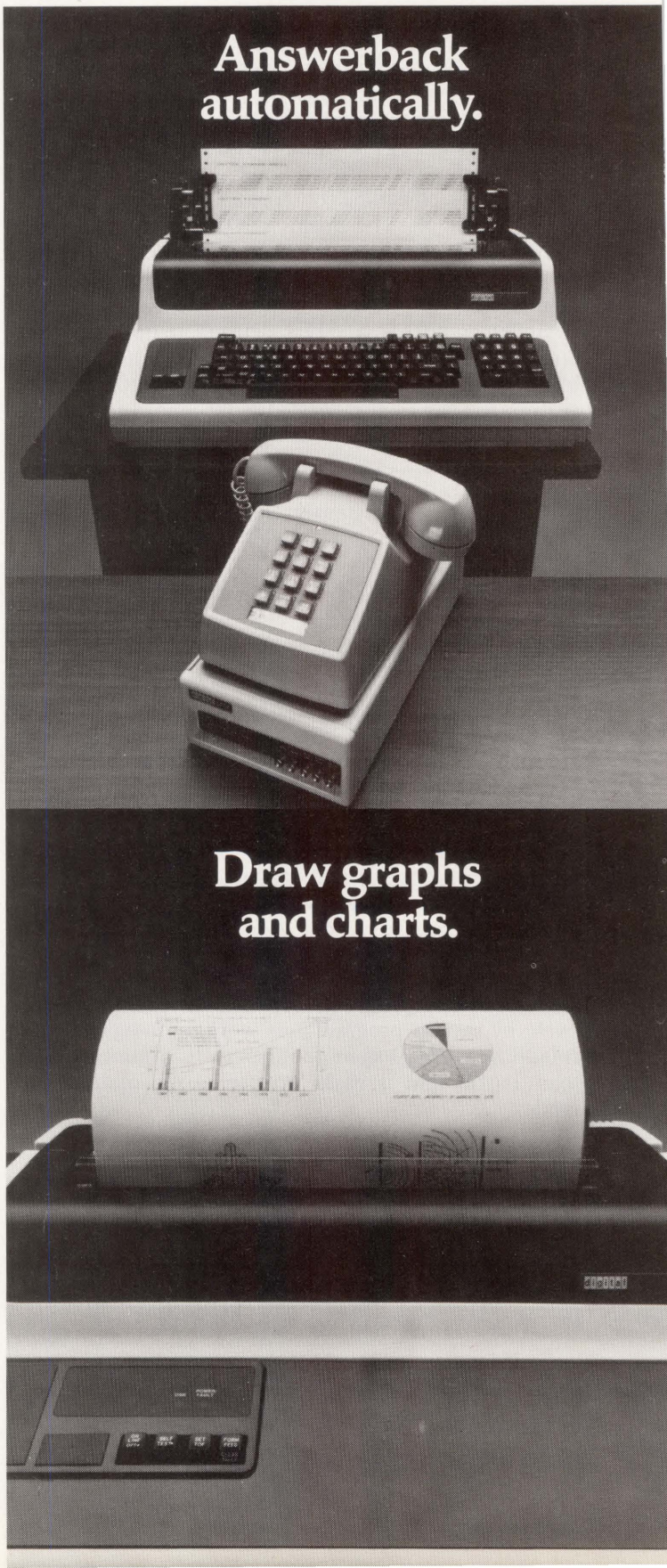

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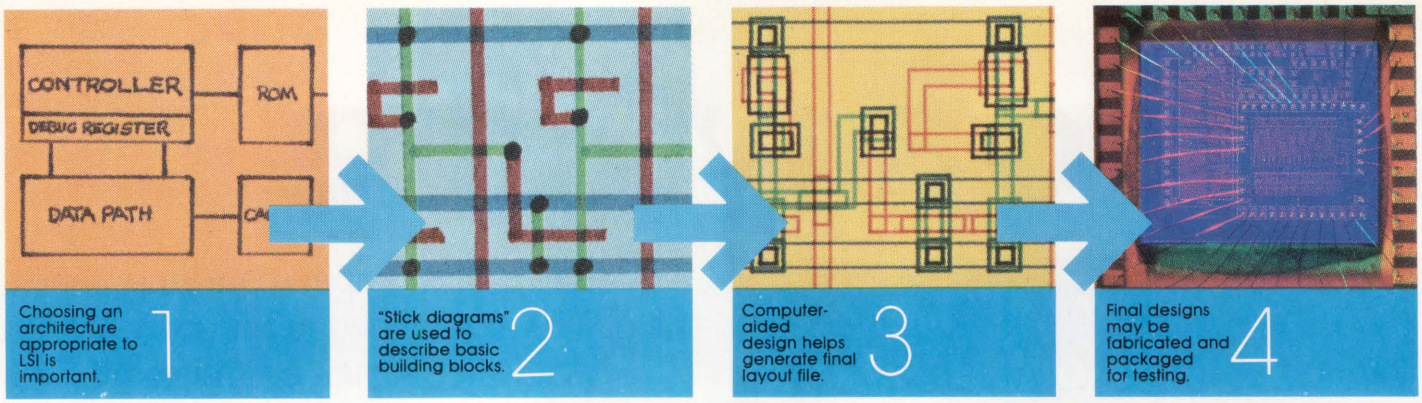

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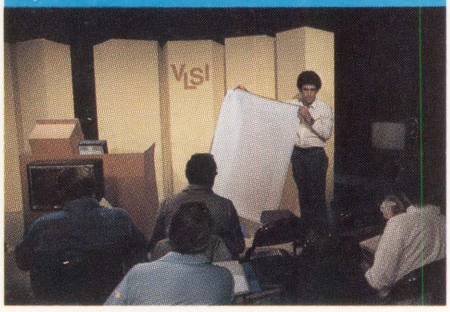

The instructors for this course have debugged the material over the past two years while teaching LSI/VLSI design courses at M.I.T., Caltech, Stanford, and U.C. Berkeley. Similar courses based on the Mead/Conway design methodology are now being taught at **DEC, Xerox, Varian, Bell Labs, and Hewlett-Packard,** as well as at over 30 major universities in the U.S. and Europe.

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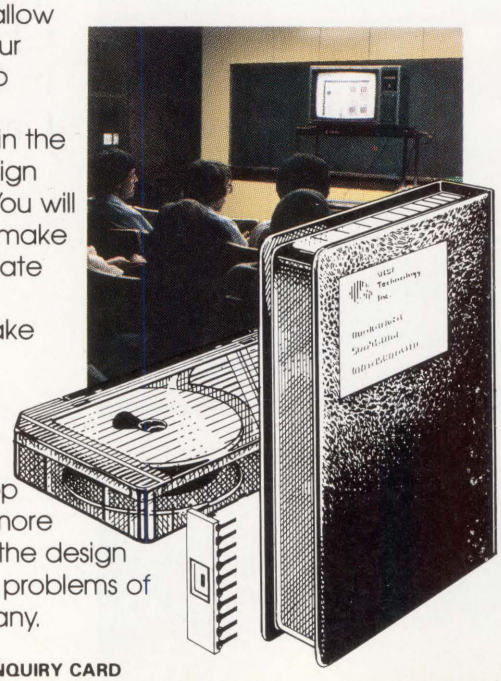

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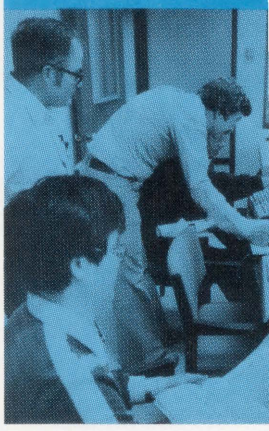

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CIRCLE 98 ON INQUIRY CARD

SOLVING THE FIXED DISK BACKUP DILEMMA

When using series streaming of tape cartridge drives for Winchester backup, compatibility with the proposed ANSI standard interface is an extra benefit

by Erik Solhjell

The new generation of small fixed disk drives has much to offer the designers of data equipment requiring large amounts of secondary storage. However, the question of backup or security copy for these devices is often a major obstacle to introducing the fixed disk concept in the system. Although new backup devices that solve this problem are now coming to the market, designers must still make many decisions and sometimes compromise before reaching the final solution to their application.

Some disk parameters

This new generation of disks uses Winchester technology, and maximum capacities range from approximately 5M bytes to more than 60M bytes. The maximum will probably increase to 100M bytes within the next two years. Formatted track capacity goes from 8k to 15k bytes, and the disks perform one complete revolution in 16 to 20 ms. Maximum data transfer rate is 6M bps. Power requirements also vary considerably. Most disks, however, require at least 24 V, 5 V and either −5 V or −12 V. Only a few drives require ac power.

Backup requirements

With the preceding numbers in mind, a list of the most important requirements for the backup system can be made. The list is not presented in any order or priority, as the importance of each requirement will vary according to the type of application.

Erik Solhjell is development manager for Data Storage Products at Tandberg Data, Oslo, Norway, where he is responsible for all development work concerning data storage. His work at Tandberg has largely involved designing tape and floppy disk controllers. Mr Solhjell has a Diplom (equivalent to an MS degree) in electronic engineering from the Technical University of Norway.

Ability to store data reliably
Adequate capacity, normally at least 20M to 30M bytes
Low total system cost
Low media cost
Backup time of less than 30 min
Small physical volume
Easy interfacing
Ease of making a common disk/backup device controller
High data transfer rate
Ease of use
Possibility of archival storage at a low cost
Immediate read verification of written data
Low power requirements
Voltage requirements similar to disk drive
Possibility of future capacity expansion

Backup methods

Two basic methods are employed for backing up small disks: partial and total. In the partial method only those parts of the disk contents that have been changed during the day are transferred to the backup device. Thus dumping time and the requirements for backup storage capacity are reduced. System overhead (software) may increase considerably, and a restore operation is more complicated. Data are transferred either as they are generated throughout the day, or during a backup operation at the end of the day. In the former case, a removable cartridge drive or a 0.5″ tape drive with normal start and stop facilities may be the best choice, whereas a streaming tape drive may be more suitable in the latter case. A streaming tape drive runs the tape continuously without the normal start and stop operations between the data blocks.

Total backup means that the complete contents of the disk are copied onto the backup device in one operation. This is normally done at the end of the day. The method requires a backup device with a larger capacity, but operation is very simple and system overhead low. Disk restore operation is simple. A streaming device is normally used to reduce dumping time, and the system

Relative Performance of Backup Devices

	Removable Disk Cartridge	Floppy Disk	Std 0.5″ Tape Drive	Stream 0.5″ Tape Drive	Std 0.25″ Tape Drive	Stream 0.25″ Tape Drive
Max capacity	5	6	3	1	4	2
Backup drive size	1	4	6	5	3	2
Error rate	1	5	4	1	6	2
Total system cost	3	1	6	5	4	2
Media cost, 20M-byte storage	5	4	1	1	3	2
Data transfer rate	1	5	4	2	6	3
Read-after-write capability	6	6	1	1	1	1
Cost of common controller	1	3	6	6	3	2
20M-byte archival storage cost	6	4	1	1	2	1
Voltage/power requirements	1	4	6	5	3	2
Future capacity expansion	6	5	4	1	3	2
Easy media handling	1	1	4	2	1	1
Total score	37	48	46	31	39	22
Total relative performance	3	6	5	2	4	1

transfer rate should be high to avoid slowing down the backup drive. Preferably one backup medium should take the complete contents of the disk.

Backup devices

Six different types of backup devices are available today: removable disk cartridge (built into a fixed disk), floppy disk, standard 0.5″ tape drive, streaming 0.5″ tape drive, standard 0.25″ tape cartridge drive, and streaming 0.25″ tape cartridge drive. The Table lists typical relative performance for each of these devices. Numbered from the best rating of 1 downward to 6, the list is based on a study of a typical 20M-byte backup application. Other types of applications, special system requirements, or different vendor specifications may change some of the numbers.

Removable disk cartridge. The removable disk cartridge offers the highest transfer rate, minimum size (built into the disk), and easy interfacing. However, capacity is limited, medium cost is high, and it remains to be seen if the technology is reliable enough to be used in ordinary office environments. Available capacity on the fixed disk portion is fairly low. To avoid long backup time, care should be taken when the transfer hardware and the backup algorithm are designed.

Floppy disk. Low cost and low capacity characterize the floppy disk. System cost is low because many systems already use floppy disks and it is possible to make a common fixed disk/floppy controller. However, the low capacity, the lack of a read-after-write test, and reliability problems with the double-sided, double-density devices make them suitable only for low capacity noncritical applications.

Standard 0.5″ tape drive. The standard 0.5″ tape drive has a fairly high transfer rate, can store more than 30M bytes, and generates IBM compatible tapes. However, the system cost is high, a common disk/tape controller (9-channel parallel recording) is difficult to make, and the physical size is large compared with the fixed disk. Thus it is not a suitable backup device except in those applications where the tape drive is already used for other reasons.

Streaming 0.5″ tape drive. Compared with the standard 0.5″ tape drive, the streaming version is faster and cheaper and can be made physically smaller. Still it is a fairly big, high priced device. A common disk/tape drive controller is complicated (9 parallel tracks). The generation of IBM compatible tapes may be important in some applications requiring data interchange, but transfer speed is so high that a large buffer is required for many applications. Capacity can be increased considerably. With non-IBM compatible recording formats, it should be possible to store 100M to 250M bytes on one tape at a reasonable cost.

Standard 0.25″ tape cartridge. Employing the 3M tape cartridge, the standard 0.25″ tape cartridge has a density of either 1600 or 6400 bpi. The low transfer speed, the long gaps, and a maximum formatted capacity of 3.75/11M bytes make it suitable mainly for the low end of the backup market.

Streaming 0.25″ tape cartridge. Probably the best solution for most disk backup applications, the streaming 0.25″ tape cartridge is fast, small, and reliable, and carries a low price tag. Because of the similarity in operation, it is easy to design a common disk/backup drive controller. Its capacity now ranges from 20/30M bytes to 67M bytes. Within a few years, this could increase to 100M bytes. The cartridge is rugged and easy to handle, ideal for archival storage. Transfer speed is not as high as for the fixed and removable disks or the 0.5″ tape drives, but it is well within the requirements for most systems, and the necessary buffer requirements are much lower.

Optimizing backup time

Backup time is important in most systems, whereas restore time is less critical because restore operations are rare. To achieve a short backup time, the backup device should be fast, but this is only a part of the solution. The two systems (disk and backup device) have an asynchronous relationship. Data cannot be transferred from the disk to the backup drive directly, even when both systems have the same transfer speed. A buffer is required as shown in Fig 1. During backup, data are

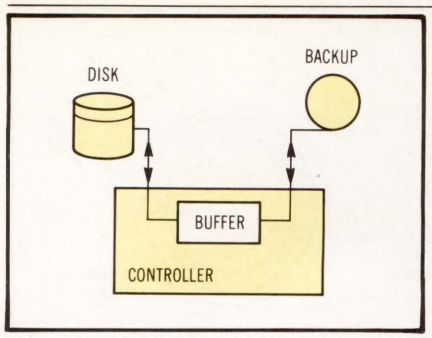

Fig 1 Backup system with one buffer. Data are transferred from disk to buffer, then from buffer to backup device.

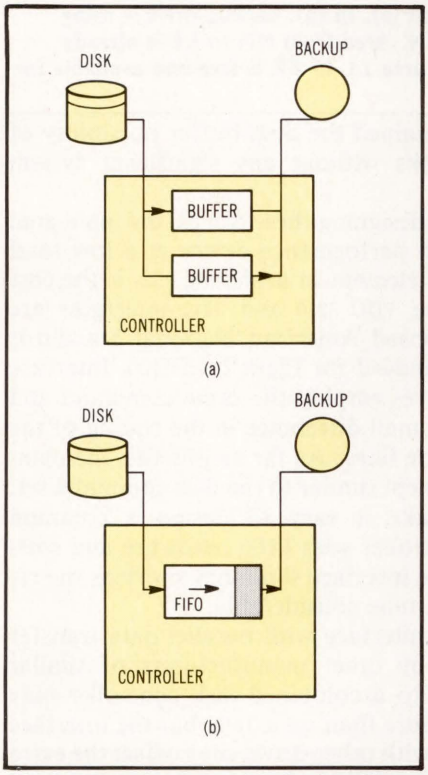

Fig 2 Data backup with dual buffer (a) and with FIFO (b). When dual buffer is used, disk loads data into one buffer while backup device reads from other buffer. With FIFO, performance slows down when read-after-write circuit in backup drive detects error.

loaded from the disk to the buffer and then from the buffer to the backup device. Buffer capacity requirements may be high, especially for high speed streaming 0.5″ tape drives. A one-buffer system, however, is not a good solution, since one of the devices has to wait while the other is either loading or unloading the buffer. Worst-case transfer time may increase to many times the theoretical minimum.

To avoid these problems a dual buffer or a first in, first out (FIFO) buffer should be used (Fig 2). With dual buffers, the disk loads data into one buffer while the backup device reads from the other one. To achieve a short backup time, it is important that data transfer to the backup device take place without interruptions. Minimum buffer capacity depends upon the disk speed, the speed of the backup device, and the particular backup algorithm employed. The algorithm can be a sector by sector transfer in an evenly increasing order (sector 1, sector 2, sector 3, etc), or any mix of reading and skipping sectors. One easy method is to have a buffer capacity larger than the amount of data written by the backup device during one or two disk revolutions. The buffer is then filled up for each disk drive revolution, which makes it possible to back up the sectors in an evenly increasing order. Single disk read errors should normally not be a problem.

The FIFO solution can use the same types of backup algorithm as those used by the dual buffer system. However, the FIFO solution has one major drawback. Suppose that the read-after-write circuit in the backup drive detects an error. The data must then be rewritten, but because with a true FIFO the data are already lost, they need to be read once more from the disk. This slows down performance considerably.

A solution

Tandberg Data's series of streaming 0.25″ tape drives, called Backer drives, has been designed with disk drive backup in mind. The mechanism involves a moving serpentine read-after-write head with eight tracks on the tape. A serpentine head can operate in read-after-write mode in both tape directions so that a rewind operation is no longer needed after a track has been written. The mechanism for moving the head employs a stepper motor and a screw system to achieve a high motion resolution at a low cost. Once installed, it requires no adjustments and is designed to be highly tolerant of mechanical wear. The capstan motor has an infrared optical tachometer.

Speed is controlled in two ways—short-term by an analog feedback circuit and long-term by the microprocessor. A three point locking mechanism keeps the cartridge in place. Mounted just below the cartridge door opening is a manual ejection arm. The locking mechanism, the capstan motor, and the head mechanism are mounted on a sturdy casting. The electronics are mounted on two boards, one read/write board and one digital board. A microprocessor is used to control the capstan motor, the head motor, and the drive interface. A self-test program is included, and may be activated either with a command from the controller/host or by shorting a test pin to ground. Operating speed is 90 ips and maximum flux density is 10160 frpi. Maximum capacity on a 450-ft (137-m) tape cartridge is 40M bytes.

Drive. The drive comes in three versions. TDC 3210, the basic drive, has servo and read/write circuits. TDC 3212 is the same drive with a built-in buffered formatter. Buffer capacity is 4k bytes maximum. Read and write data are transferred serially between host and drive. TDC 3214 is identical to TDC 3212 except that the interface is industry standard with read and write data transferred in parallel.

Formatter buffer. 3212 and 3214 employ a buffer design that combines the features of both the dual buffer and the FIFO systems described earlier. It is called a circular buffer. In Fig 3, its total capacity is represented by the circle. When the backup operation starts, data are loaded from the disk into the buffer from (internal) address 00 and upward. Writing begins when a minimum of 512 bytes have been loaded [Fig 3(a)].

In Fig 3(b), data have been written to the tape from (internal) address 00 and upward. Now the backup drive is using data from location NN. The buffer area from NN to LL has already been filled with disk data. The area from LL to KK is free and can be loaded with new disk data. When detecting a read error, the formatter automatically rewrites the bad block further down the tape. The data are still in the KK to NN field. Address KK is 512 bytes less than address NN to ensure that the complete block has been read by the read circuit before new data are loaded into that buffer area. Except for the last 512 bytes written to the tape, the total buffer area is always available for data loading from the disk. The system has the flexibility of the FIFO but has retained the dual buffer possibility of rewriting bad blocks without any significant system degradation.

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2	30B-020	30W-020	30Y-020	30R-020	30BLK-020
2.5	30B-025	30W-025	30Y-025	30R-025	30BLK-025
3	30B-030	30W-030	30Y-030	30R-030	30BLK-030
3.5	30B-035	30W-035	30Y-035	30R-035	30BLK-035
4	30B-040	30W-040	30Y-040	30R-040	30BLK-040
4.5	30B-045	30W-045	30Y-045	30R-045	30BLK-045
5	30B-050	30W-050	30Y-050	30R-050	30BLK-050
6	30B-060	30W-060	30Y-060	30R-060	30BLK-060
7	30B-070	30W-070	30Y-070	30R-070	30BLK-070
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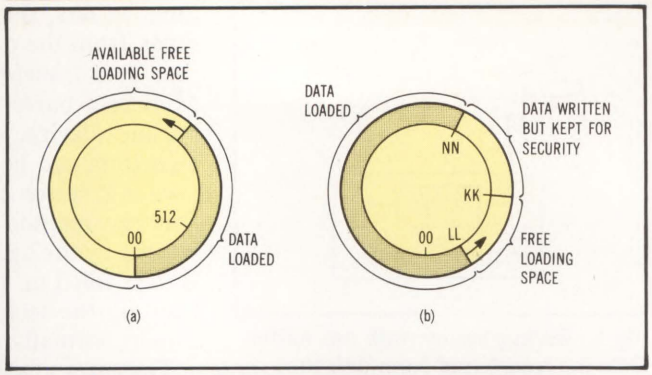

Fig 3 Operating principle of circular buffer. Circle represents total capacity. Data are loaded into buffer from address 00 and upward. Writing starts when minimum 512 bytes have been loaded (a). In (b), backup drive is using data from location NN. Area from NN to LL is already filled with disk data; area LL to KK is free and available for new disk data.

the FIFO but has retained the dual buffer possibility of rewriting bad blocks without any significant system degradation.

Interface. When designing these drives, the main goal was to offer a high performance device at a low total system cost. A key element in achieving this is the cost of interfacing. The TDC 3210 and 3212 interfaces are based on the proposed American National Standards Institute (ANSI) Standard for Eight Inch Disk Interface (X3T9/143). The drives employ the same command and status lines with a small difference in the coding of the serial read and write lines. As far as possible the command set has been kept similar to the disk command set. These features make it easy to design a common disk/cartridge controller with little hardware and software overhead. The interface similarity shortens the required extra design time considerably.

The 3214 has an interface with parallel data transfer that is also used by other manufacturers of similar drives. Interfacing to a combined disk controller may require a few ICs more than on a 3212, but the interface plug compatibility with other drives may offset the extra cost for many system designers.

Conclusion

For most applications, the streaming 0.25″ cartridge drive with its high capacity, high data reliability, small size, and low cost offers the best solution to the disk backup problem. To achieve a short backup time, care should be taken when designing the data transfer hardware and software. The buffer system employed is especially important. The series of streaming 0.25″ drives described here simplifies system integration and offers high capacity at a low total system cost.

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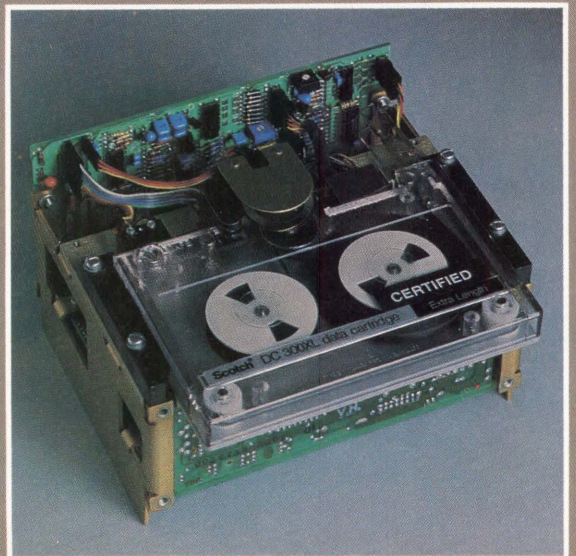

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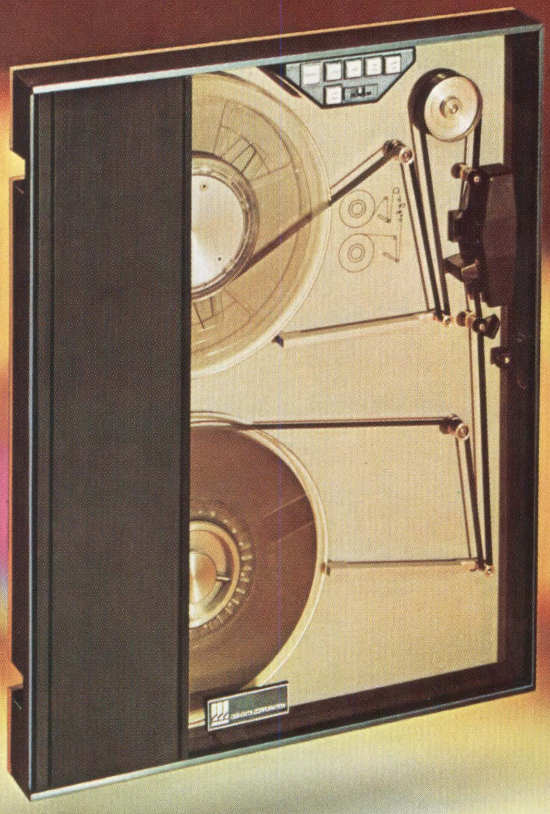

*LSI-11, PDP-11, Nova Eclipse, and HP 2100/21MX.

CIRCLE 106 ON INQUIRY CARD

DESIGNING FOR COMPLIANCE WITH FCC EMI REGULATIONS

Early planning to meet the latest FCC requirements on conducted and radiated emission is essential to cost-effective engineering of computer related products

by Eric VanderHeyden
Jerry H. Bogar

To meet the FCC's requirements for regulating electromagnetic interference from computing devices, engineers must limit conducted and emitted energy through careful circuit, component, and system design. The FCC rules cover radio frequency emissions from circuits employing digital or switching rates of over 10 kHz. Included in the mandate is energy radiated directly from equipment, as well as energy conducted into alternating current power lines. FCC Docket 20780, as it is known, will alter the design procedures followed by most computer, peripheral, and related equipment engineering groups. Vigilance over the FCC rules must begin with product design, from conception to production, and through field installation.

Circuits and systems covered

In general, designs containing switching or digital circuit frequencies of over 10 kHz must comply at least with the FCC's Class A requirements for regulating electromagnetic interference (emi). If, in addition, any market for the product includes use in the home, then it may have to comply with the more stringent Class B rules.

For the present, some equipment has been excluded. It is most likely, however, that a system that employs a binary clock, is driven by a reference source in excess of 10 kHz, and/or is sold to the average computer market is covered. Components and systems covered include mainframes and central processing units with clock frequencies of over 10 kHz, cathode ray tube terminals, discs, tape drives, printers, communication interfaces, and modems employing microprocessors or clocks. Also covered are systems using all or parts of the devices just mentioned, including dedicated products such as private branch exchanges, business computers, and data concentrators. Furthermore, it is important to remember that interconnection cabling can radiate more interference than the equipment itself. Often the primary source of radiation the system integrator must deal with is the interconnecting cables.

How much radiation is critical?

To engineers and designers suddenly confronted with the need to meet them, these requirements may seem mysterious. One seldom thinks of digital circuits as interference culprits. Most designers do not know what

A development engineer in the research division of AMP Inc, Harrisburg, PA 17105, Eric VanderHeyden is involved in the emc related aspects of shielded connector design. Before this, his work involved development of filters and filtered connectors, electronic instrumentation, and components. Mr VanderHeyden holds a BS in electrical engineering from the Pennsylvania State University.

Jerry H. Bogar is manager of emc/transmission systems research at AMP, where he has designed digital magnetic circuits using multi-aperture ferrite cores, investigated discontinuities in coaxial transmission lines, analyzed miniature emi filters, and studied the emi properties of shielded cables and connectors. Mr Bogar earned a BA at Yale and a BSEE at the Pennsylvania State University.

levels of radiation and conduction to expect from various binary/digital sources. Energy to be conducted or radiated at a specific frequency must initially be present at the frequency that represents a source of interference. If a switched signal is generated, the amount of energy available at any given frequency depends upon the signal amplitude (A), the repetition frequency (PRF or 1/T), the pulse width (t_w), and the pulse rise time (t_r).

Signal parameters are identified in Fig 1. Note that point X shows the energy level available at frequencies up to f_1. It is proportional to the signal amplitude A and the pulse duty cycle (t_w/T or $t_w \cdot PRF$). Signal energy reaches a maximum at $(t_w/T) = \frac{1}{2}$, the equivalent of a clock signal. At frequency f_1, the radiation envelope begins to drop off (20 dB/decade) at the frequency determined by $1/t_w$. As t_w gets shorter, the frequency of the f_1 breakpoint moves up. This represents a bit duration that is directly related to system baud or data rate. At frequency f_2, the envelope drops off even more rapidly (40 dB/decade). The new breakpoint is determined by the inverse of the pulse rise and fall times, when t_r and t_f are assumed to be equal. As pulse transition speed decreases, producing slower rise and decay rates, this point lowers in frequency and the Fourier harmonics at higher frequencies are reduced in amplitude. Since circuits have lower potential for radiating rf energy, if they do not require fast rise and fall times it is best not to use them.

Fig 2 illustrates a practical situation. It shows the energy available for radiation from a typical 5-V transistor-transistor logic (TTL) gate driving six loads (9.6 mA), at a 1-MHz frequency with a 50% duty cycle. Rise and fall times are assumed to be 6 ns. What may seem astonishing in this situation is that even if only

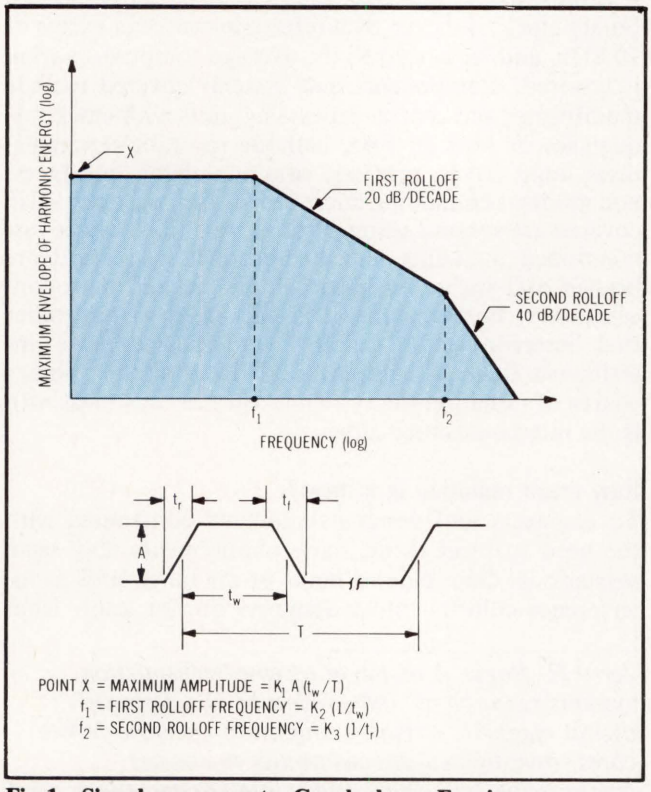

Fig 1 Signal components. Graph shows Fourier components of signal vs frequency. Envelope of maximum energy amplitude spectrum generated by trapezoidal signal pulse, with equal rise and fall times, is plotted.

1×10^{-3} of the power available at the TTL gate were radiating energy into space, the radiated level would exceed FCC specifications. Fig 3 illustrates an analogous situation for conducted interference. When power levels are much higher than those contained in TTL circuits, such as in a switching power supply, the situation becomes more acute.

Modification of an existing design vs progress of an emi proof design

Apart from the inability to modify emi sources significantly and the impracticality of reconfiguring system interconnection board layouts or enclosures radically, the process of modifying an old design is very similar to that of developing a new one. One advantage to modification of an old design is that measurements can be performed on an existing system, so that problem sources, levels, and frequency bands are not merely hypothetical. The drawback is that retrofit requires skilled emi control engineers who must also minimize changes to a system that is already in production to keep the per-unit cost down.

A new design is not constrained by as many forces as one that is already in production. An emi controlled design starts with a careful selection of the basic circuit elements. For example, this can include the choice of logic families from least energy spectrum (most desirable) to most energy spectrum (least desirable), as outlined in the Table, "Logic families." Power driven circuits should switch the minimum energy to accomplish the task. Pulse rise times should be selected to minimize the harmonics generated by the circuitry, while other circuit parameters are traded off. Very high harmonics, the seventh through the ninth, often are not useful for realizing the required circuit performance, and can be troublesome as interfering rf emissions. Circuits that carry signals with components in the rf spectrum should be physically close to one another, to minimize interconnections that can behave as antennae radiating unwanted emi.

Direct current circuits that are bypassed with large capacitors should be bypassed by smaller ceramic or tantalum capacitors. This nullifies parasitic inductances and resistances inherent in large value capacitors that tend to make them ineffective filters at the higher frequencies. As a rule of thumb, bypass capacitors should keep stray currents isolated in small loops to minimize radiation. Thus, a 100-μF/A capacitor should be located at the printed circuit board power input; a 1.0-μF/A unit at the circuit main current branches; and a 0.01-μF/A unit at each integrated circuit. These current loops are illustrated in Fig 4.

By no means is all the energy generated in a pulse circuit radiated or conducted as emi, however. Much of

Logic families

Logic family	Maximum useful bandwidth
CMOS	5 to 12 MHz
TTL	10 to 25 MHz
TTL (LS)	15 to 30 MHz
TTL Schottky	30 to 100 MHz
ECL	50 to 500 MHz

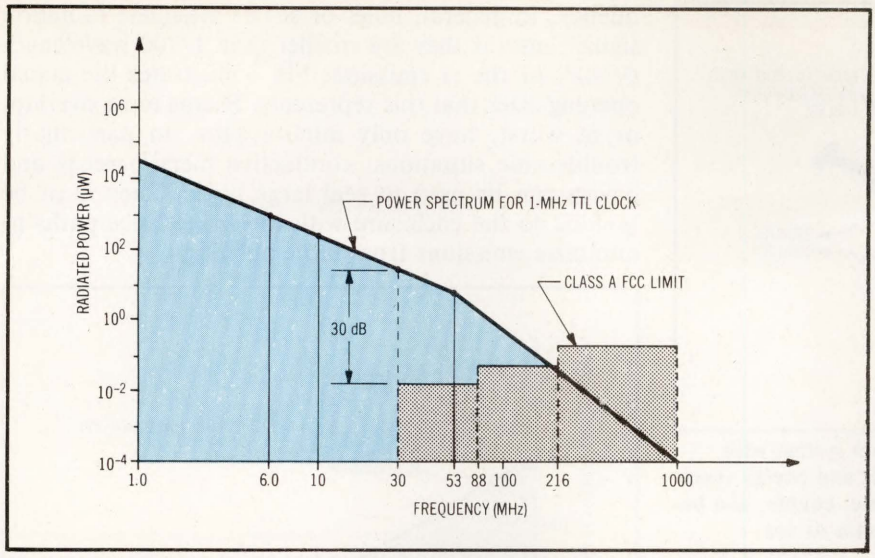

Fig 2 Emission levels. Shown are both energy available from 1-MHz TTL gate and emission levels allowed by FCC specification. Graph compares radiation available to that of theoretical isotropic radiator emitting energy equally in all directions at FCC limits.

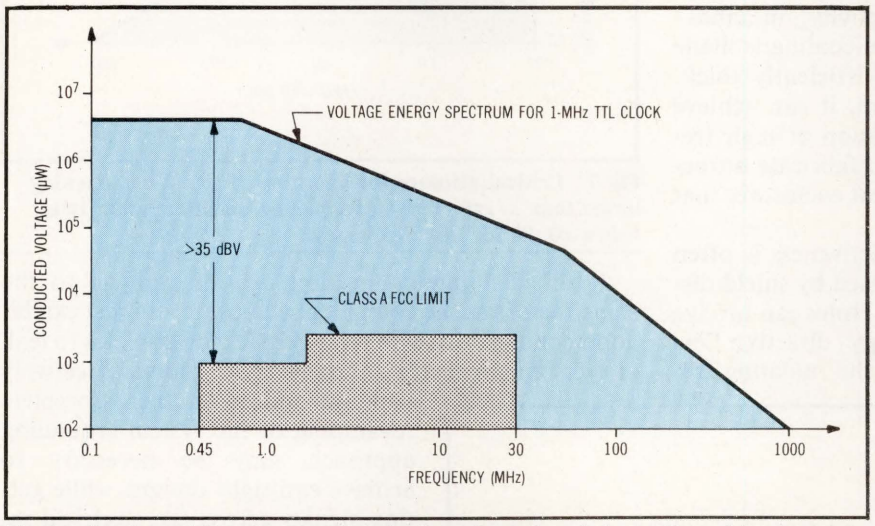

Fig 3 Conducted interference. Level of conducted emissions allowed by FCC specifications is compared to rf voltage available from TTL gate. Here, even 10^{-3} of power available at 2 MHz, conducted into power line, would exceed FCC limits.

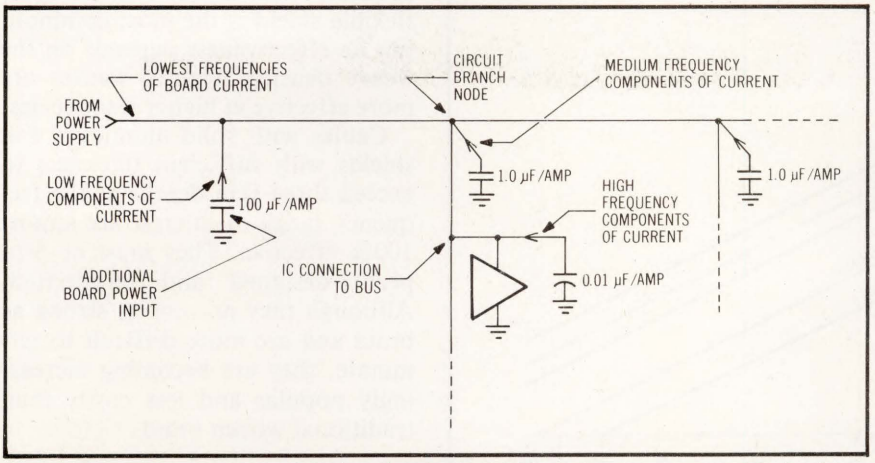

Fig 4 Bypass capacitors minimize circuit rf emissions from power supply leads. High frequencies are bypassed closer to integrated circuit source, medium frequencies at circuit branches, and low frequencies at board input. Overall, this minimizes high frequency current spikes in long interconnection paths back to power supply.

the energy is employed usefully and thereby absorbed by the circuits themselves. The rest is radiated by interconnecting lines between circuits (an antenna effect), coupled via capacitive or magnetic coupling, or conducted via uncontrolled ground paths to other portions of the circuits. (See Fig 5.) Design engineers must prevent excessive amounts of emi energy from leaving the equipment, the interconnections between equipment, or the primary power circuit. Suppression measures combine shielding the radiation adequately and filtering the conducted energy.

Enclosing the source in a shield

Shielding is essential in controlling emi. Shielding reflects energy, absorbs it, or both. Shields may enclose portions of a system, the entire system, or the interconnection system by encircling them with a conductive surface at ground potential. When an electromagnetic plane wave strikes a conductive surface, it suffers a loss of energy due to reflection and absorption. In assessing the effectiveness of a shield, both types of losses must be considered.

Reflection losses are related to discontinuities in characteristic impedances at media boundaries through which the wave travels as it enters and leaves a shield. For a thin metallic shield in an electric field, the primary loss is caused by reflection at the metal surface. Absorption losses are ohmic and simply transform the rf energy into heat. Consequently, as the electromagnetic wave passes through the shield, the amplitude of the wave decreases exponentially. Distance required for the amplitude to decay to $1/e$ of its original amplitude is defined as the skin depth, δ, in inches

$$\delta = \frac{2.6}{(f\,\mu_r\,\sigma_r)^{1/2}}$$

where f is the frequency of the wave, μ_r is relative permeability, and σ_r is conductivity relative to copper. To be effective in all applications, a shield should be at least three skin depths thick. Shown in Fig 6 are thicknesses of five metals for three skin depths versus frequency.

Plastic enclosure designs employ two approaches. One confines

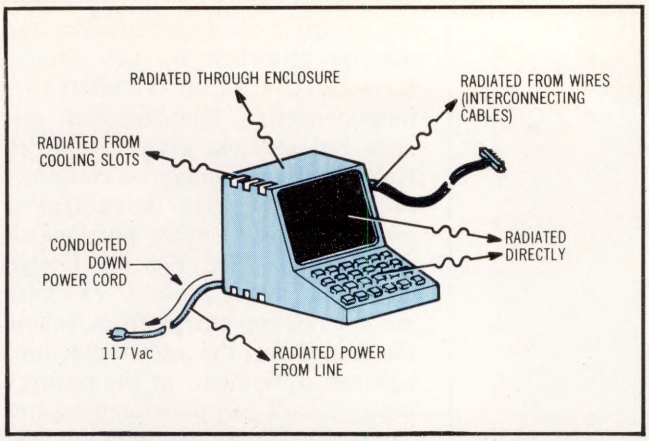

Fig 5 Energy conducted and radiated from system with conducted enclosure. Once spurious signals and energy reach other portions of circuitry, they may radiate, couple, and be conducted until they finally radiate into space or are transmitted via power line.

critical portions of the circuitry in a metal enclosure, such as aluminum; the other applies conductive materials to the inside of a plastic case. Such coatings are selected on the basis of conductivity, in mhos/square, and cost of application. If the coating is made from appropriate materials and is sufficiently thick, usually on the inside of the enclosure, it can achieve results that effectively suppress radiation at high frequencies. Thus, product designers can fabricate attractive yet relatively inexpensive equipment enclosures that fulfill emi suppression requirements.

A material's intrinsic shielding effectiveness is often of less concern than is the leakage caused by shield discontinuities, such as seams and holes. Holes can behave as slot antennae and radiate energy directly. The amount of radiation is a function of the radiating frequency. In general, holes or seams attenuate radiation significantly if they are smaller than 1/100 wavelength ($\lambda/100$) of the rf emission. Fig 7 illustrates the actual opening sizes that this represents. Seams must overlap, or at worst, have only minute gaps. In particularly troublesome situations, conductive metal screens and covers can be used to seal large holes. They must be bonded to the enclosure with low impedance paths to minimize emissions from large openings.

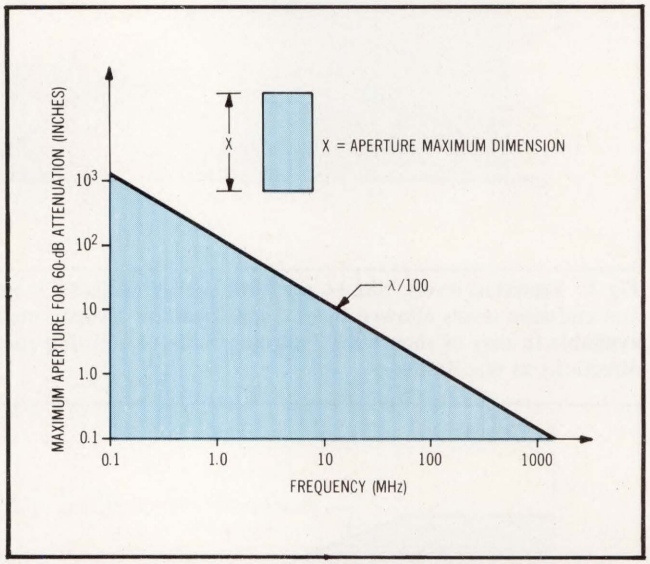

Fig 7 Critical distance for aperture. If shield has opening larger than $\lambda/100$ at given frequency, its attenuation falls below 60 dB for that frequency.

A shielded interconnection cable is subject to the same factors as the equipment enclosure. It must exhibit good conductivity with relatively few or no holes to leak rf, yet remain flexible enough to be routed effectively from one unit to another. Complete revamping of the system grounding approach may be necessary to achieve emi-tight designs while getting signals across the electrical interface. (See Fig 8.) Material commonly employed for cable shielding is metal braid, flexible conduit, rigid conduit, and metal foil. Braided flexible shield is the most common, but its effectiveness depends on the weave density. Tighter weaves are more effective at higher frequencies.

Cables with solid aluminum foil shields with sufficient thickness to exceed three skin depths at the frequency range of interest are almost 100% effective. They must be properly designed and terminated. Although they are not as strong as braid and are more difficult to terminate, they are becoming increasingly popular and less costly than traditional woven braid.

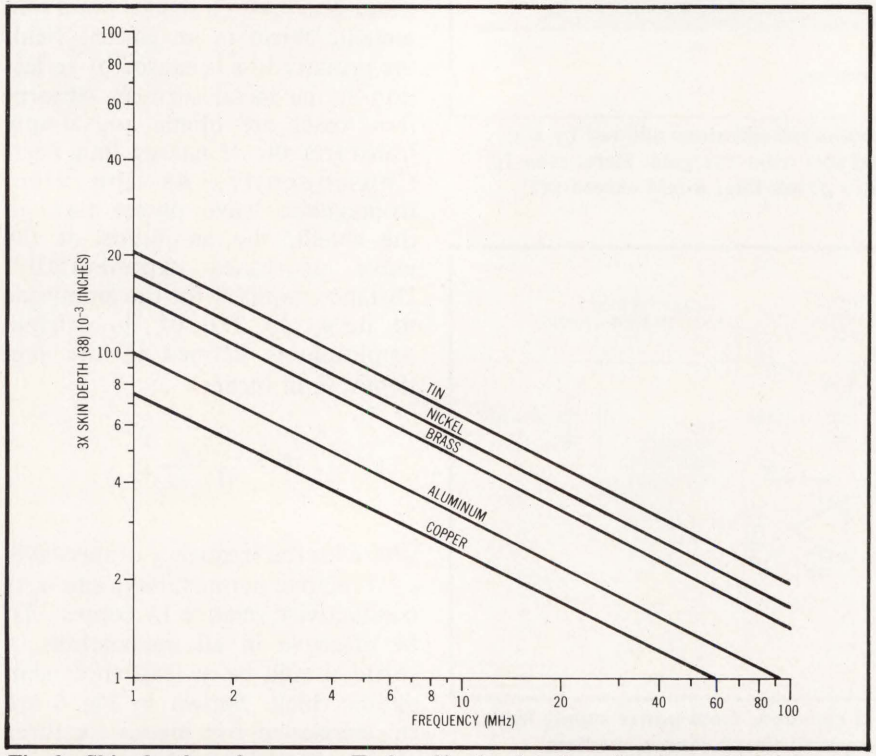

Fig 6 Skin depth vs frequency. To be effective in all applications, shield should be at least three skin depths thick. Thicknesses of five metals for three skin depths vs frequency are plotted.

Filters

Filters used for emi control are of the "low pass" type, and isolate unwanted electrical noise generated in

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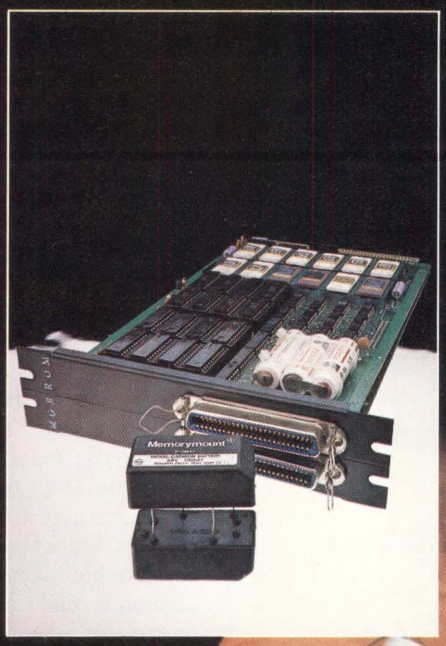

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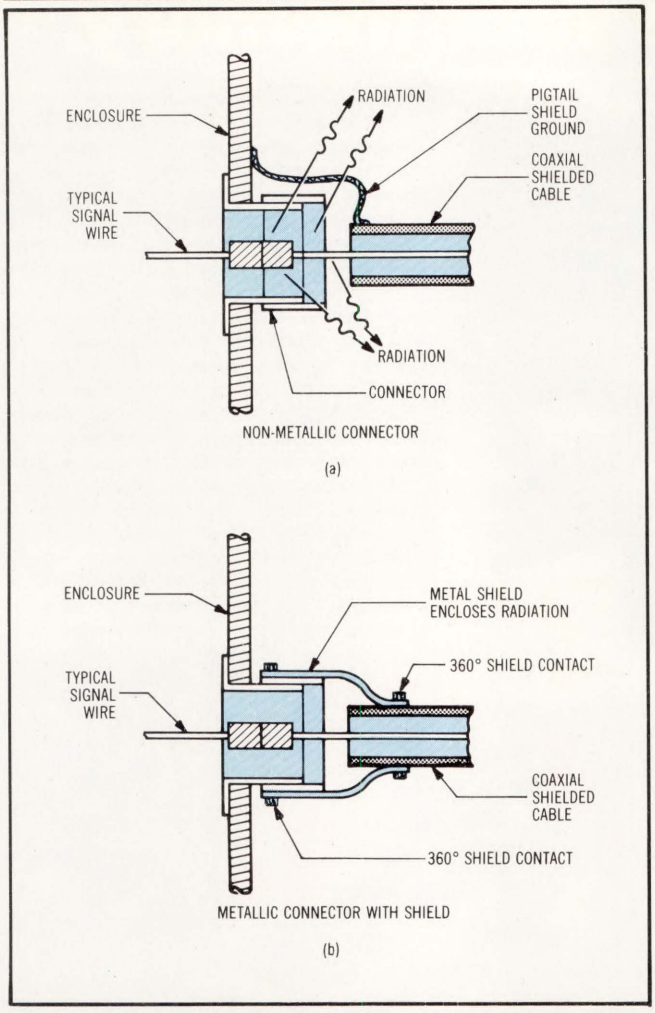

Fig 8 Conductive shield termination. At high frequencies, shields that surround interconnecting cables must extend metal surface from enclosure to cable shield. When used to ground shields to cables, conventional pigtails have same effect in enclosure as apertures, and allow radiation to escape (a). Conductive shield termination encloses conductors and extends enclosure shield to cable shield (b). For rf, shields must be grounded at both ends.

one part of a circuit or system and keep it from being conducted to other parts of the circuit or system. They are particularly important in regard to power supply leads and primary power input leads. If a broad bandwidth is not required for signal transfer, signal lines can be filtered to minimize radiation from interconnection lines. When combined with shielding, filtering can be particularly effective for inter-equipment cabling.

Electromagnetic interference filters are divided into three broad categories: those comprising "lumped elements," those acting as special "feedthrough capacitors," and those employing high frequency, lossy ferrites. Lumped-element filters (Fig 9) isolate conducted interference from the primary power line. They can have one or more sections, and additional sections improve performance. Many kinds of lumped-element filters, packaged in emi-shielded enclosures, are available. Components must be selected carefully for each design situation. Since lumped-element filters are actually LC circuits, they can create problems stemming from multiple resonances, especially when connected to switching power supplies. Therefore, these filters should be chosen carefully for such applications.

Fig 10 illustrates the straight feedthrough filter. It depends on the capacitor to bypass high frequency energy to ground and to isolate input and output by the enclosure wall. Its equivalent circuit contains a series inductor that limits this effect at high frequencies. The simplest high frequency lossy ferrite filter is a ferrite bead on a wire (Fig 11). The ferrite bead appears as a 1-turn toroid with an approximate inductance of 1 to 10 μH. The ferrite is lossy at high frequencies, producing a resistance, R(f); at low frequencies, the impedance diminishes to that of the wire. Series impedance of a ferrite bead is low at low frequencies, then rises and stabilizes for a wide range of frequencies, after which it begins to rise further. Hence, ferrite beads can effectively block passage of high frequency energy.

A very effective filter is the distributed element type, shown in Fig 12. In this case, distributed capacitance and ferrite material coaxially surround the signal wire and provide a uniform radial path to ground, improving filter characteristics significantly. Filter elements in high density connector pin configurations of special connectors enable every pin to act as an emi filter. These filter elements can also take the place of feedthrough capacitors. (See Fig 13.)

Testing

Testing is an integral part of the emi design procedure. According to FCC compliance requirements, a limited amount of radiation is permitted from any direction at a specified distance from the equipment. All testing must be performed in "open field" test sites. Equipment sold as a system can be tested either as a complete system or in place, as installed.

Most initial testing is performed in an emi shielded room, which blocks out external rf to localize the source with test equipment. Otherwise, both measuring equipment and the operator would have to select the emitted signals under test from those already present from other sources. Besides being emi tight, shielded rooms are often built to allow for automated measurements that move calibrated equipment and/or sensor antennae to locate maximum radiated field strengths. Receivers are automated to digitize data and speed location of significant radiations.

Even if only 1 x 10^{-3} of the power available at the TTL gate were radiating energy into space, the radiated level would exceed FCC specifications.

Initial tests are often made on circuitry with packaging as identical as is practical to the final configuration. Such tests are performed on circuits, subsystems, entire systems, and interconnections. The true level of radiation can be determined by performing emi tests on circuits; by testing subsystems, the effectiveness of enclosure shielding and filters can be determined. Measuring interconnecting cables and connectors discloses their shielding effectiveness.

The final prototype is tested as a system with simulated interconnection wiring to peripheral and host equipment, as appropriate. Frequencies of the highest

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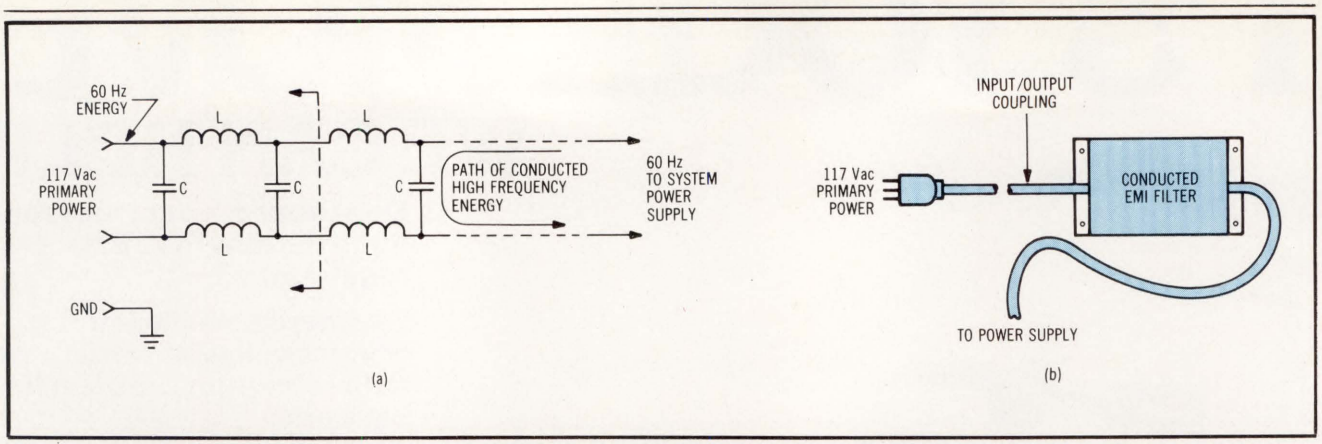

Fig 9 Lumped-element filter. Two-section filter blocks conducted interference from 117-Vac, 60-Hz primary power circuit (a). Capacitor provides short circuit path and inductor provides high impedance while 60-Hz primary power passes virtually unimpeded. Improper installation is potential problem area (b); placing filter input wiring too close to output wiring creates coupling path for conducted interference that nullifies effect of filter.

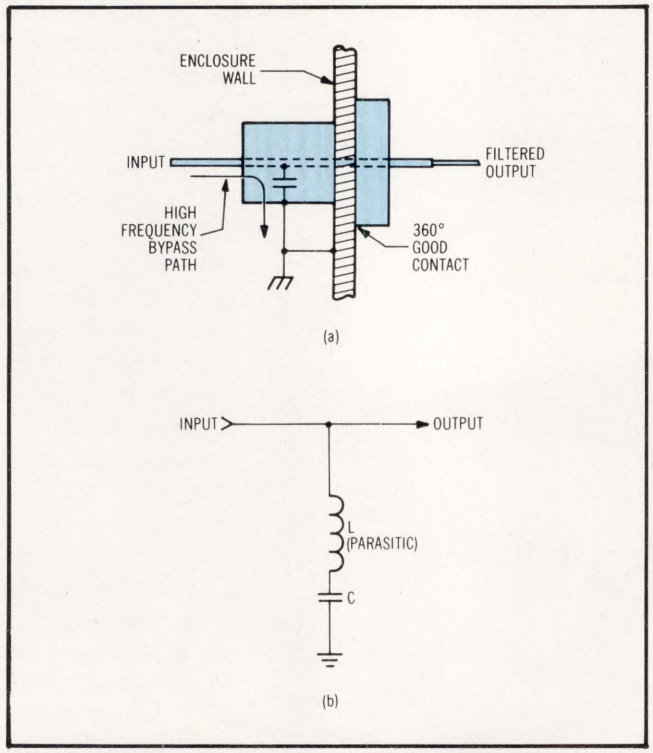

Fig 10 Feedthrough capacitor. Effective bypassing of rf currents depends chiefly on capacitor (a), but parasitic inductor in equivalent circuit hinders effective bypassing at high frequencies (b).

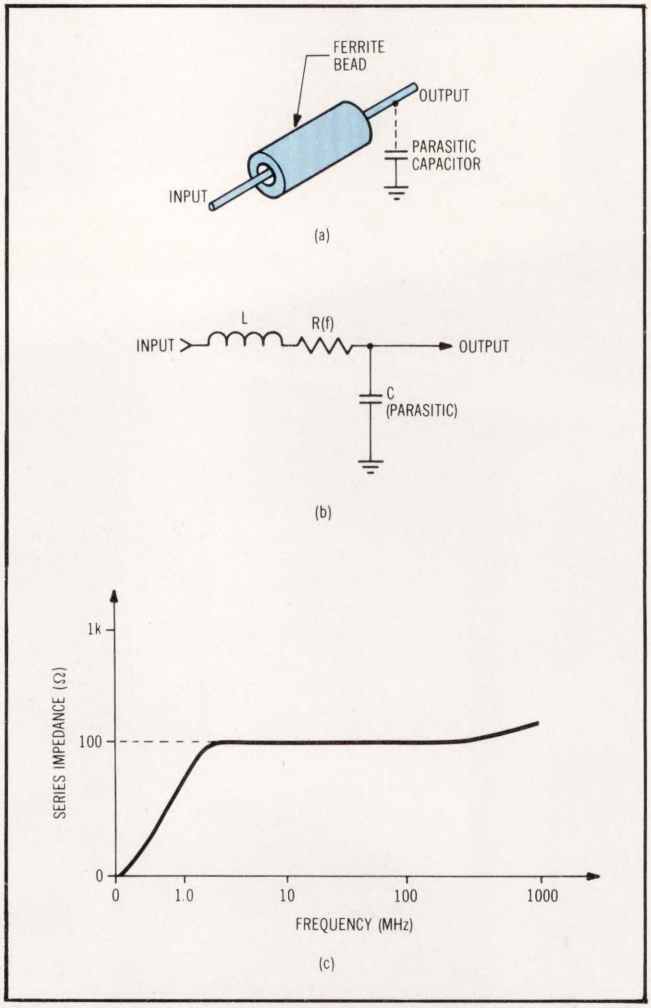

Fig 11 Ferrite bead filter. Simplest unit is one bead on wire (a). In equivalent circuit (b), resistor R(f) is function of frequency. Series impedance curve of typical ferrite bead (c) is very low at low frequencies, but stabilizes over wide range of frequencies.

emissions are then noted. After this, tests are performed at these values in an "open field" test site. Although these sites are unable to screen out external rf emissions, they simulate the equipment's normal operating situation. Test sites are elaborate and require specialized grounding systems. In addition, they must supply filtered power to the test equipment and the unit under test. Test sites rely upon automation to rotate the test unit and to position antennae, speeding up the data-gathering task considerably. A system too large or too complex to be tested as a whole may be tested after installation. In this case, the testing can be laborious, since use of automated equipment to position equipment and sensor antennae is restricted.

It is important to remember that interconnection cabling can radiate more interference than the equipment itself.

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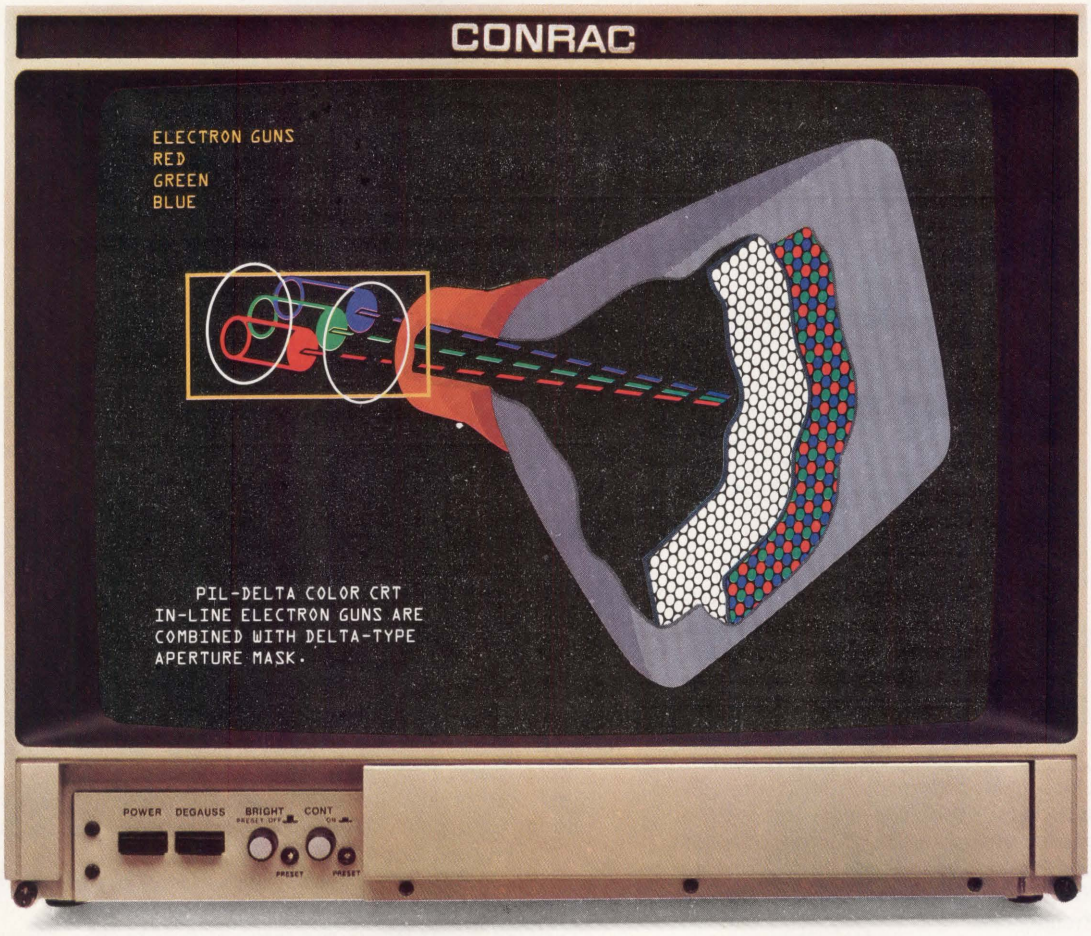

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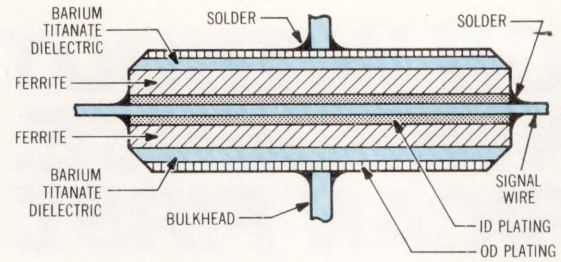
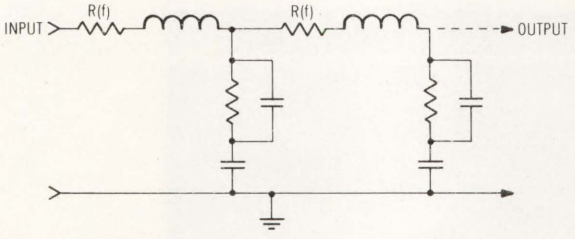


(a)



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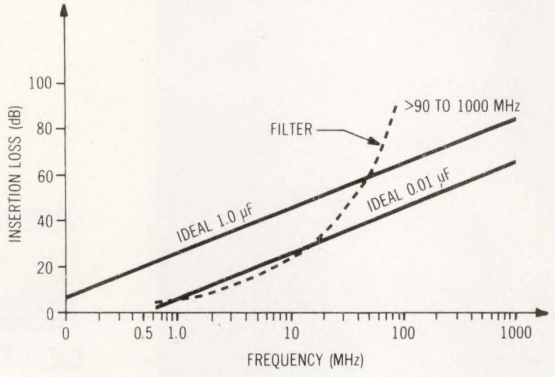

(c)

Fig 12 Distributed element, absorptive filter. Longitudinal cross section (a) takes form of lossy, coaxial transmission line; equivalent circuit is shown in (b). Filtering effect of coaxial filter is compared to ideal capacitor of same value in (c). This filter performs more effectively than conventional capacitor at high frequencies.

Test failure

If a unit fails under test, it probably will not fail by much. A new design that fails the test reenters the process as if it were an "old" design, and the search for the lowest cost redesign to meet the requirements begins. At this point, the sources causing the excessive emission are readily identified and appropriate measures can be taken to reduce the radiation that reaches the outside environment. This will be accomplished with additional shielding and filtering. After the redesign, the testing must be repeated on the modified prototype to ensure compliance. Since the FCC requires compliance of each unit manufactured, it is advisable to set up a sample lot control program to guarantee that all future units continue to meet the requirements.

Filter elements in high density connector pin configurations of special connectors enable every pin to act as an emi filter.

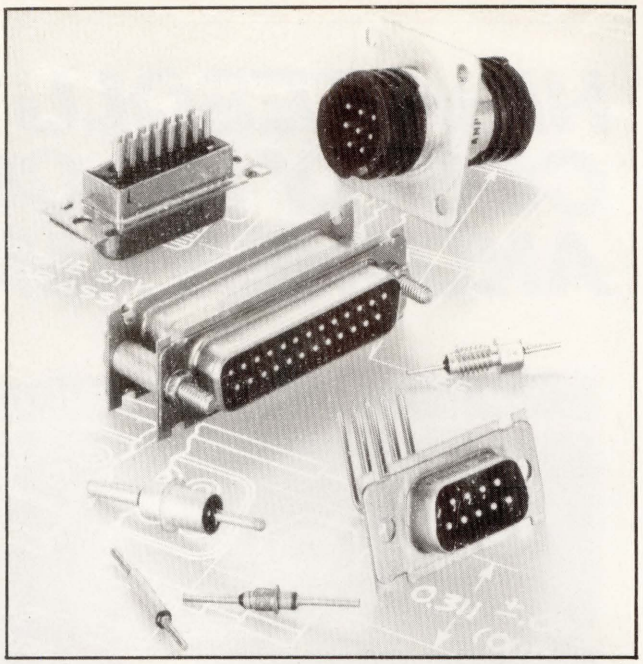

Fig 13 Miniature coaxial feedthrough filters. Filters are assembled into connectors, which trap interference that might otherwise leave enclosure.

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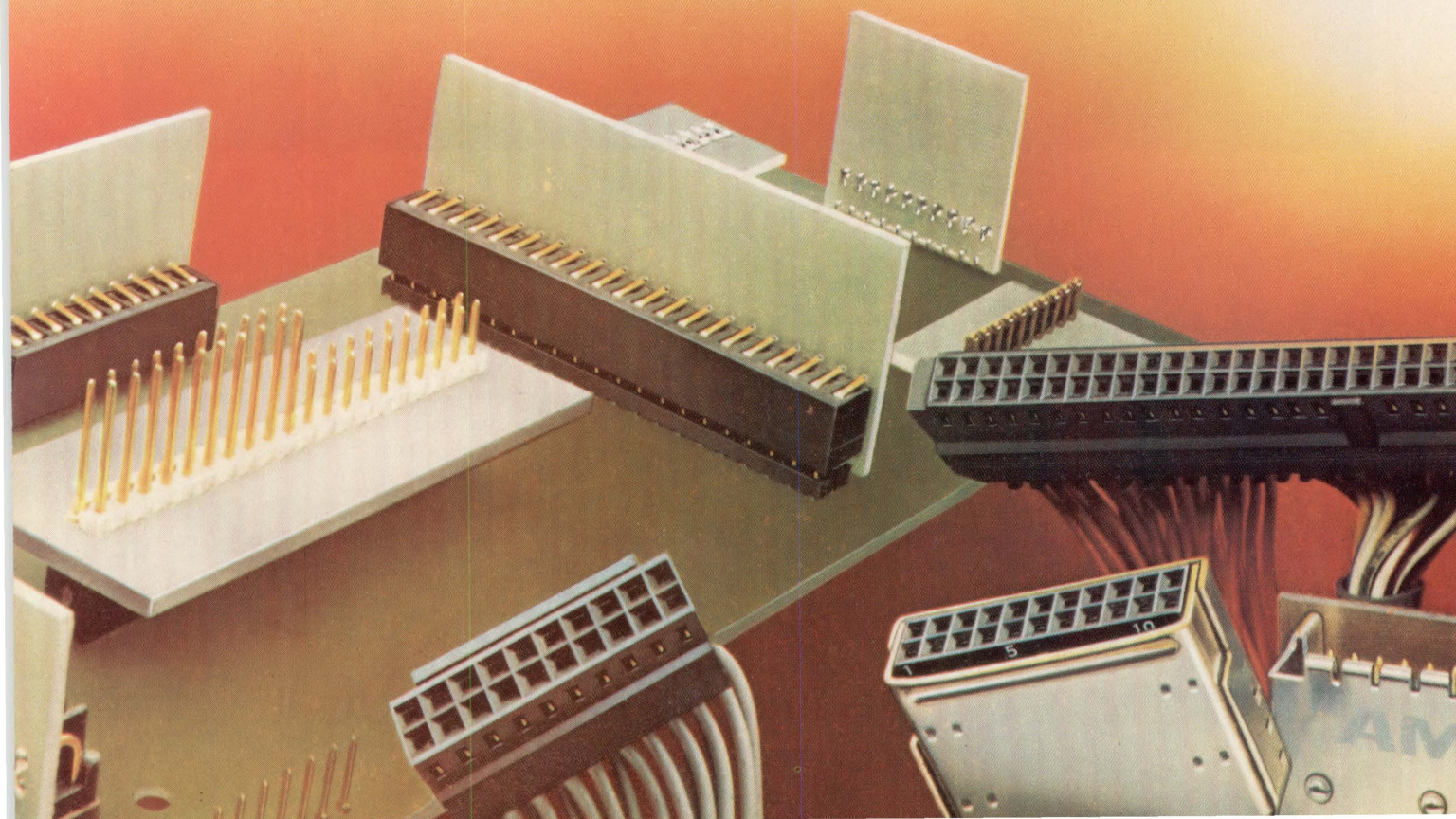
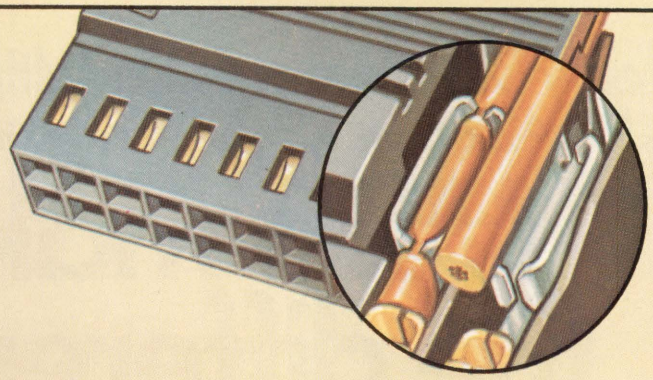
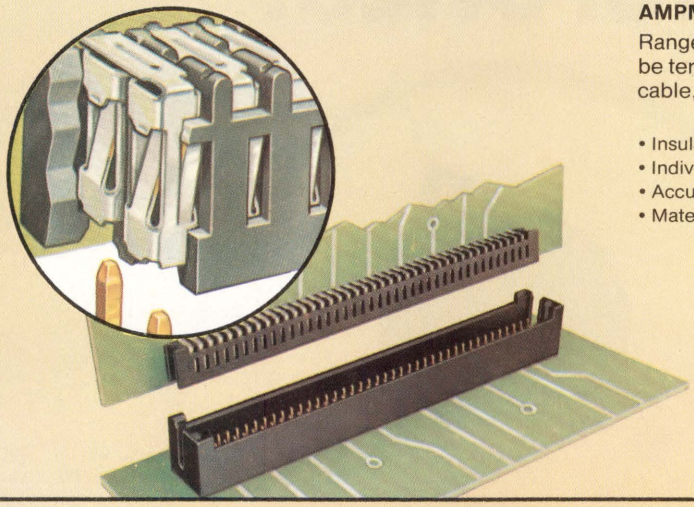


AMP Facts



AMPMODU 2-piece connectors:
High density interconnection, with up to 300 positions per connector

- Two-piece design eliminates gold pc edge fingers
- Proven receptacle design
- Solderless compliant pin insertion in motherboard
- Molded-in polarization and daughter card guides



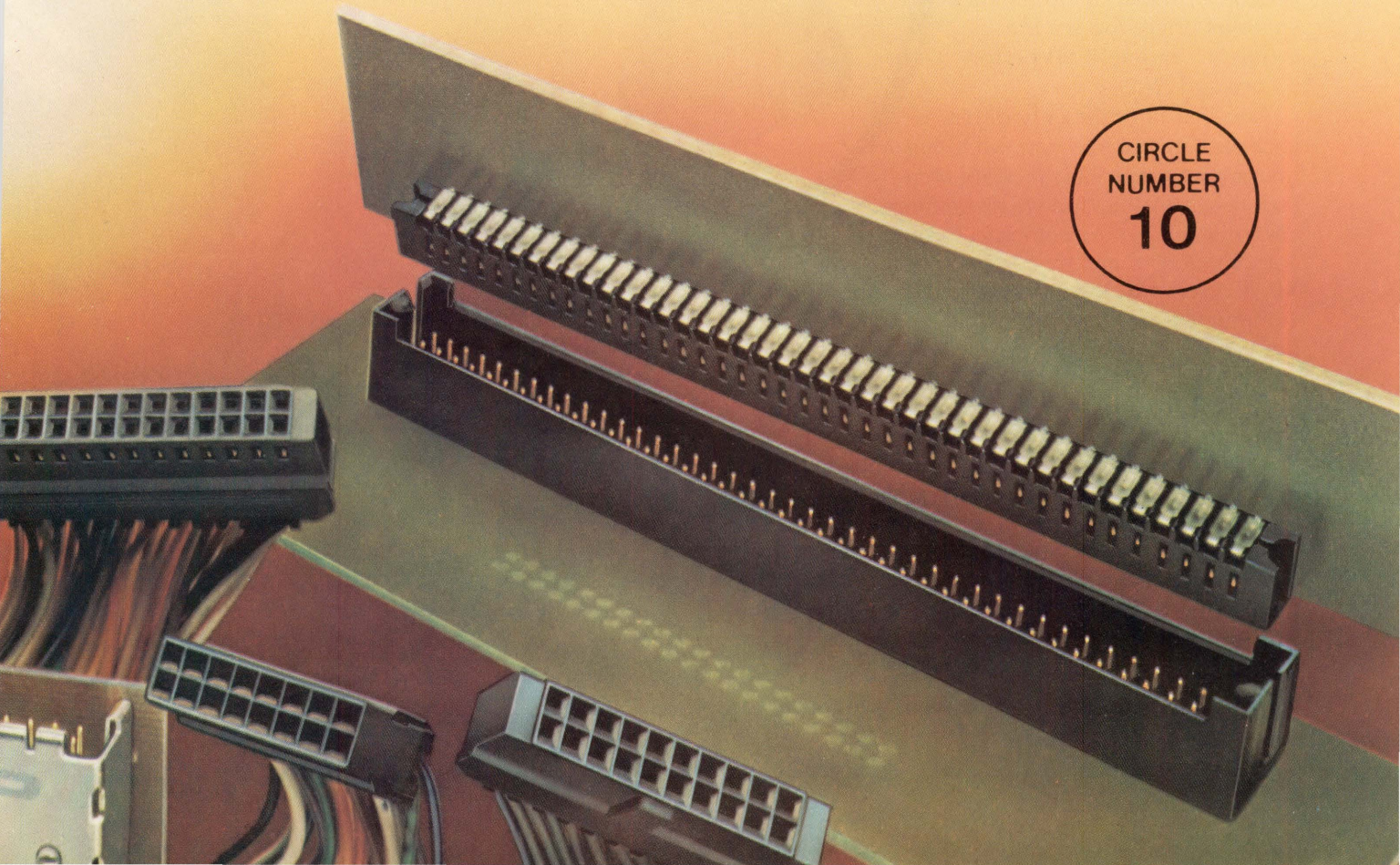
AMPMODU MT Connectors:
Range from 6 through 72 positions and can be terminated to discrete wire, jacketed cable, twisted pair cable, and ribbon cable.

- Insulation displacing contacts
- Individual wire strain reliefs
- Accu-plate precision plating
- Mates with quick-eject headers

For more information, call the AMPMODU System Desk at (717) 780-8400.
AMP Incorporated, Harrisburg, PA 17105.

AMP and AMPMODU are trademarks of AMP Incorporated.

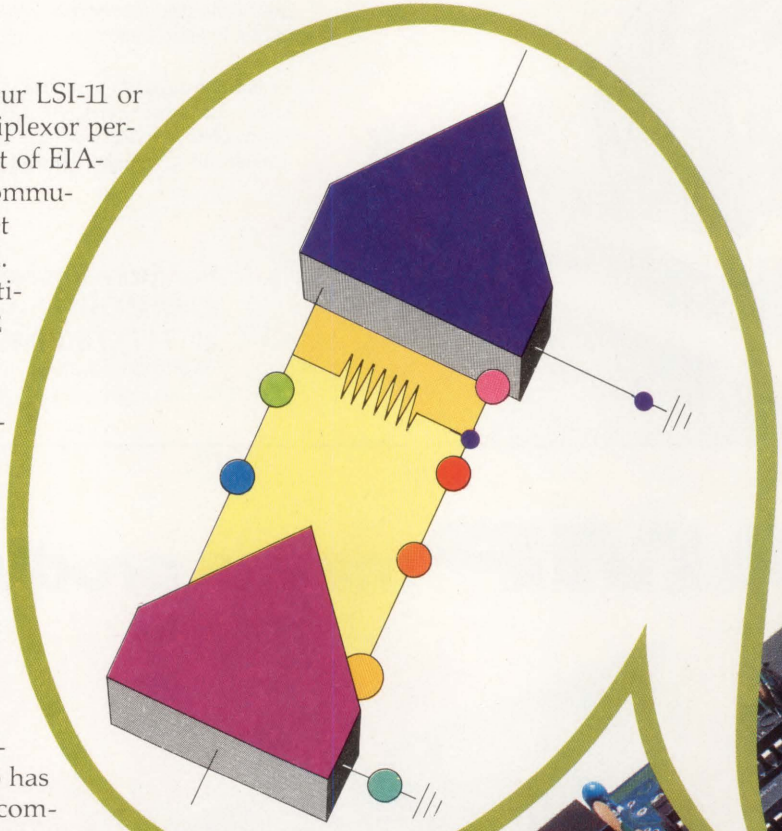
AMP means productivity.



CIRCLE NUMBER 10

The only DZ11 Compatible Multiplexor for LSI-11. And it has RS-422 plus RS-232 and current loop capability-

MDB makes the difference!



Now you can have it all for your LSI-11 or PDP* 11 system! Full DZ11 multiplexor performance with the added benefit of EIA-RS-422 long line capability—communicates at distances to 3000 feet (914.4m) at rates to 19.2K baud. What's more, MDB's DZ11 multiplexors let you combine RS-422 with EIA-RS-232 in any combination up to a total of eight lines on a single board. Or combine RS-232 with current loop in the same way. Eight and sixteen channel RS-232 DZ11 multiplexors are also available. No more doubling up on boards, distribution boxes, rack space or price. You see the results in your system's performance and cost.

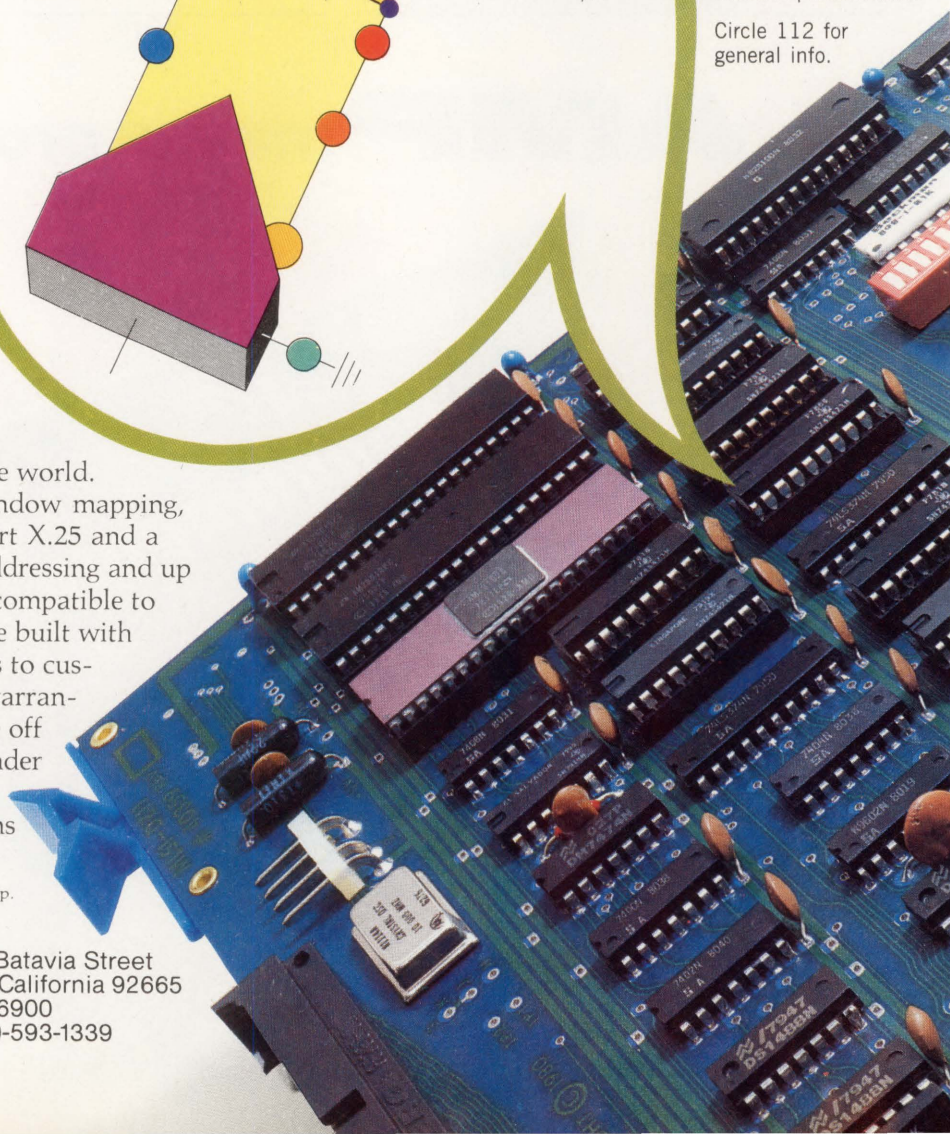
And that's not the only difference we can make to you. MDB has line printer controllers that are completely self-testing and we make more controllers for more computer/printer combinations than any company in the world. MDB offers PROM modules with window mapping, communications interfaces that support X.25 and a unique LSI-11/23 system with 22 bit addressing and up to 4 Mbytes of memory. From purely compatible to purely incredible all MDB products are built with exceptional quality and responsiveness to customer requirements. Our boards are warranteed for a full year, many are available off the shelf and they can be purchased under GSA contract #GS-OOC-02423.

Call or write for all our specifications —the MDB differences that make a difference.

*Trademark Digital Equipment Corp.

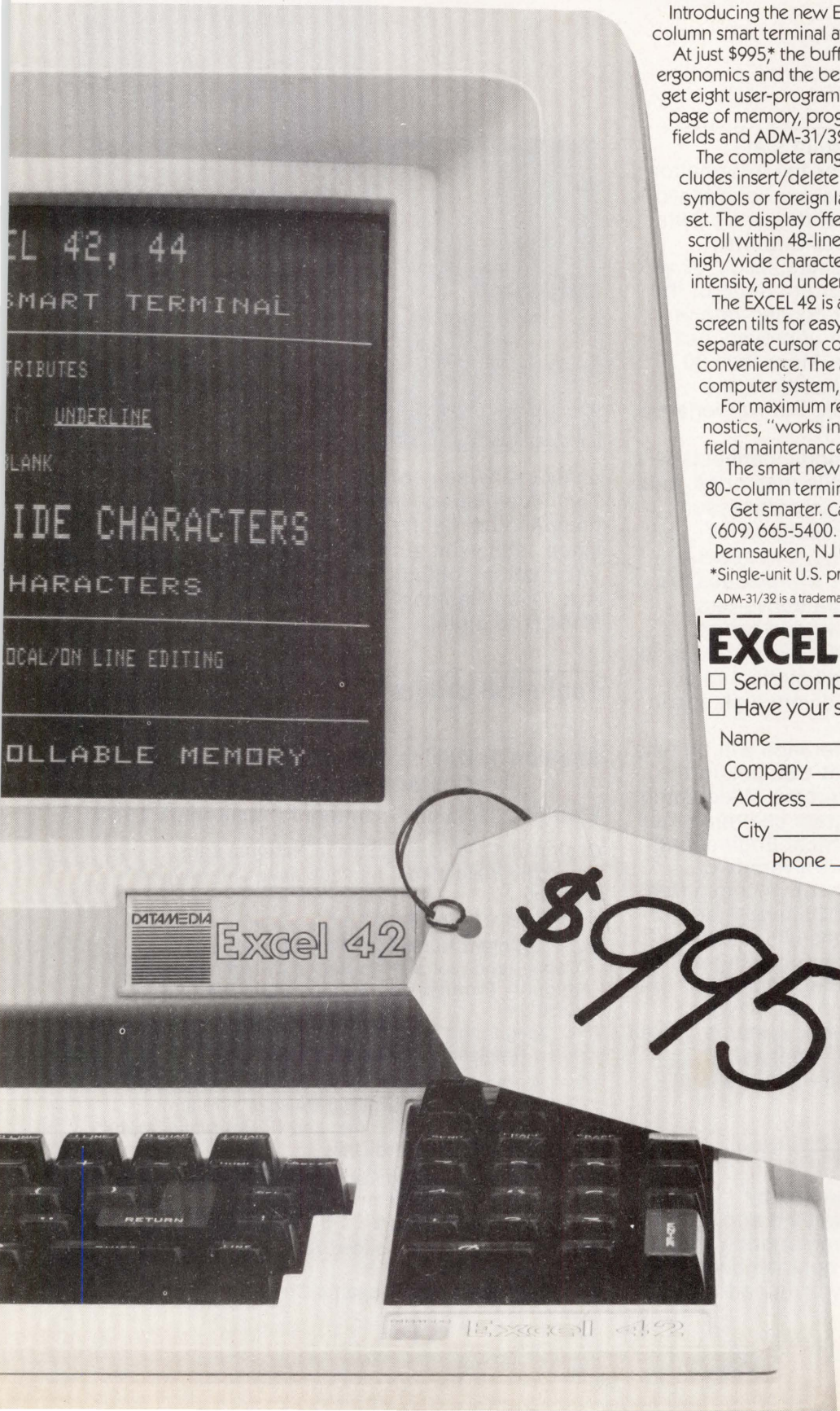
Circle 111 for featured product data.

Circle 112 for general info.



MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX: 910-593-1339

We've just put our smart new terminal on sale.



Introducing the new EXCEL 42, the first fully-featured 80-column smart terminal at a bargain price.

At just $995,* the buffered EXCEL 42 boasts state-of-the-art ergonomics and the best performance in its price range. You get eight user-programmable function keys, a standard second page of memory, programmable status mode, even protected fields and ADM-31/32™ compatibility.

The complete range of EXCEL 42 editing capabilities includes insert/delete in field, line or page. For special graphic symbols or foreign languages, add your own 128 character set. The display offers smooth scroll, split screen/regional scroll within 48-line memory, double-wide and double-high/wide characters, blink, blank, reverse video, dual intensity, and underline.

The EXCEL 42 is also smartly designed. Its non-glare screen tilts for easy viewing. Its detachable keyboard with separate cursor control/numeric pad guarantees operator convenience. The attractive cabinetry will enhance any computer system, plus a larger screen is optional.

For maximum reliability, the EXCEL 42 features self-diagnostics, "works in a drawer" logic boards, and a national field maintenance program.

The smart new EXCEL 42. Everything you need in an 80-column terminal and on sale for just $995.

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CIRCLE 116 ON INQUIRY CARD

1982 IEEE International Solid State Circuits Conference

San Francisco Hilton Hotel,
San Francisco, California
February 10 to 12

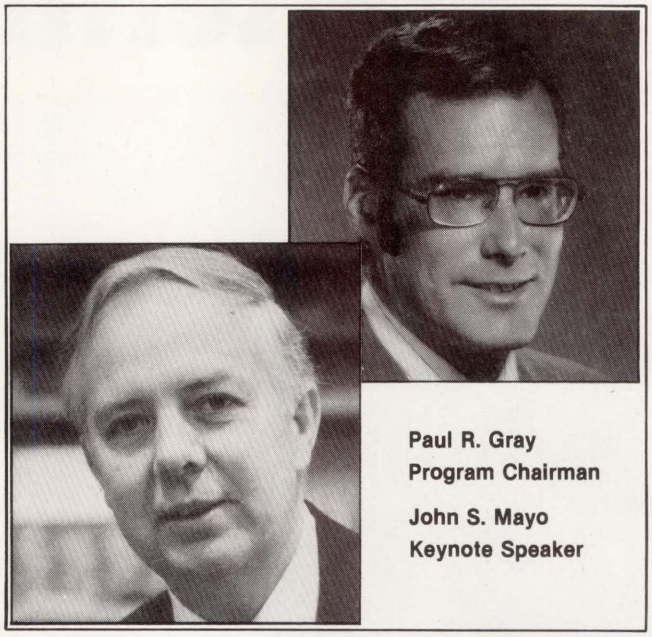
The technological impact of solid state electronics—the "workhorse of the information age" according to keynote speaker John Mayo—is again the prime emphasis of the IEEE's 29th annual International Solid State Circuits Conference. Like its predecessors, ISSCC '82 will include discussions on the current state of the art, and evening sessions will concentrate on design aspects that are as yet unproven, but likely to be used in the future. More than 80 panels will be led by over 300 authors and coauthors from the U.S., Japan, the Netherlands, England, Germany, and Italy.

During the 19 daytime sessions, panelists will cover topics such as nonvolatile memories, data acquisition and conversion, microprocessor system circuits, data communications ICs, device structures and modeling, and speech processing. Evening panelists will discuss the future of high speed logic, data converters exceeding 12 bits, the status of and future trends in computer design aids, expectations for memories larger than 64k, semi-custom logic, local data bus technology, and very high speed ICs.

Formal opening of the conference will be held on Wednesday, February 10, at 1:30 pm, in the Continental and Imperial Ballrooms. Welcoming remarks will be made by program chairman Paul Gray, professor, Dept of Electrical Engineering and Computer Science of the University of California at Berkeley and executive committee chairman John A. A. Raper of General Electric Co. Formal award presentations will also be made at this time. Immediately following will be the keynote address, "Technology Needs of the Information Age," given by John S. Mayo, executive vice president network systems at Bell Laboratories. His address will emphasize technological impacts on both industrial and home environments.

Registration

Advanced registration (postmarked by January 29) is $50 for IEEE members and $70 for nonmembers. At-conference registration will be $60 for members and $80 for nonmembers. All registrants will receive a copy of the edited 25th anniversary issue of the *ISSCC Digest of Technical Papers*, including a 48-page compendium listing over 2000 papers published since 1958, with authors and affiliations. For information contact Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134; tel: 305/446-8193 /8194 (1 to 5 pm).



Paul R. Gray
Program Chairman

John S. Mayo
Keynote Speaker

Technical program

Session 1: Device Modeling and Characterization

Wed 9 to 11:45 am, Continental Ballrooms 1 to 4

Chairman: C. W. Gwyn, Sandia National Labs

1/1 "The Yield Model for 256k RAMs and Beyond" (9 am)
C. H. Stapper, IBM Corp

1/2 "Efficient Numerical Simulation of MOS Capacitance for a Wide Range of Temperatures, Impurity Profiles, and Surface State Distributions" (9:30 am)
R. C. Jaeger and S. E. Diehl, Auburn Univ, and F. H. Gaensslen, IBM Corp

1/3 "A Recombination Model for the Low Current Performance of Submicron Devices" (10 am)
R. B. Lefferts, Tektronix, Inc, and R. M. Swanson and J. D. Meindl, Stanford Univ

1/4 "Alpha-Generated Carriers and Implications to RAM Design" (10:45 am)
C. Hu, Univ of California

1/5 "Alpha-Particle Induced Soft Error Modeling" (11:15 am)
G. A. Sai-Halasz, IBM Research Center

Session 2: Digital Signal Processors

Wed 9 to 11:45 am, Continental Ballrooms 5 to 9

Chairman: P. J. Verhofstadt, Fairchild Camera/Instrument Corp

2/1 "A 64-bit Floating Point Processor" (9 am)
F. A. Ware, Hewlett-Packard Co

2/2 "A 2-μm CMOS/LSI 32-point Fast Fourier Transform Processor" (9:30 am)
B. L. Troutman *et al*, TRW Electronic Systems

2/3 "A Monolithic CMOS Maximum-Likelihood Convolutional Decoder for Digital Communication Systems" (10 am)
R. D. McCallister and P. E. C. Hoppes, Motorola Government Electronics

2/4 "A Digital Signal Processing LSI" (10:45 am)
T. Nakamura *et al*, Matsushita Electronics Corp

2/5 "A Microcomputer with Digital Signal Processing Capability" (11:15 am)
E. R. Caudel *et al*, Texas Instruments, Inc

Session 3: Linear Circuit Techniques

Wed 9 to 11:45 am, Imperial Ballroom

Chairman: G. Erdi, Linear Technology Co

3/1 "A 4-Quadrant MOS Analog Multiplier" (9 am)
D. Soo and R. G. Meyer, Univ of California

3/2 "Differential NMOS Analog Building Blocks" (9:30 am)
D. Senderowicz *et al*, Intel Corp

3/3 "A 4-Quadrant Cosine-Synthesis Circuit" (10 am)
E. Seevinck, Philips Research

3/4 "A Universal Trigonometric Function Generator" (10:45 am)
B. Gilbert, Analog Devices, Inc

3/5 "A Monolithic Balanced-Modulator-Demodulator for Instrumentation" (11:15 am)
M. Gerstenhaber and A. P. Brokaw, Analog Devices Semiconductor

Session 4: Formal Opening of Conference

Wed 1:30 to 2:10 pm
Continental and Imperial Ballrooms

Welcoming Remarks: P. R. Gray, Univ of California, and J. A. A. Raper, General Electric Co

Award Presentations: J. H. Mulligan, Jr and P. R. Gray, Univ of California

Session 5: Keynote Address

Wed 2:15 to 3 pm
Continental and Imperial Ballrooms

Chairman: P. R. Gray, Univ of California

5/1 "Technology Needs of the Information Age"
J. S. Mayo, Bell Labs

Session 6: Testing and Design Automation

Wed 3:15 to 6 pm, Continental Ballrooms

Chairman: F. H. Hewlett, Jr, Texas Instruments, Inc

6/1 "An Automatically-Designed 32-bit CMOS VLSI Processor" (3:15 pm)
S. Horiguchi *et al*, NTT Musashino Lab

6/2 "Custom Macro Design in VLSI Bipolar Technology" (3:45 pm)
J. J. Coleman *et al*, IBM Corp

6/3 "A High Density PLA Macro and Its Layout Generator" (4:15 pm)
W. Fung *et al*, IBM Corp

6/4 "A Self-Testing PLA" (5 pm)
G. Grassl and H-J Pfleiderer, Siemens Research Labs

6/5 "Test/Characterization Procedures for High Density Silicon RAMs" (5:30 pm)
P. D. Gangatirkar *et al*, IBM Corp

Session 7: Dynamic RAMs

Wed 3:15 to 6 pm, Continental Ballrooms 5 to 9

Chairman: H. J. Boll, Bell Labs

7/1 "A Storage-Node-Boosted RAM with Word Line Delay Compensation" (3:15 pm)
K. Fujishima *et al*, Mitsubishi Electric Corp

7/2 "A 288k-bit Dynamic RAM" (3:45 pm)
B. F. Fitzgerald and E. P. Thoma, IBM Corp

7/3 "A 72k-bit Bipolar DRAM" (4:15 pm)
R. J. Houghton *et al*, IBM Corp

7/4 "An NMOS DRAM Controller" (5 pm)
M. Bazes *et al*, Intel Corp

Session 8: Data Acquisition and Conversion

Wed 3:15 to 6 pm, Imperial Ballroom

Chairman: A. P. Brokaw, Analog Devices Semiconductor

8/1 "A Monolithic 12-bit 3-μs DAC" (3:15 pm)
G. McGlinchey, Advanced Micro Devices

8/2 "A Differential Switched Capacitor Instrumentation Amplifier" (3:45 pm)
R. C. Yen and P. R. Gray, Univ of California

8/3 "A Pin-Programmable Instrumentation Amplifier for 12-bit Resolution Systems" (4:15 pm)
S. A. Wurcer and L. Counts, Analog Devices Semiconductor

8/4 "A 14-bit PCM DAC" (5 pm)
W. Mack *et al*, Signetics Corp

8/5 "A 16-bit Monolithic Bipolar DAC" (5:30 pm)
T. S. Guy and L. M. Trythall, Harris Semiconductor

Wed 8 pm, Informal Discussion Sessions

1 "Monolithic Signal Processors"
Continental Ballrooms 1 to 3
Moderator: C. R. Hewes, Texas Instruments, Inc
Panel members: J. R. Bodde, Bell Labs; J. M. Hughes, Texas Instruments, Inc; J. A. Feldman, MIT Lincoln Lab; R. E. Owen, Fairchild Advanced R&D Lab; and T. Nakamura, Matsushita Electronics Corp

2 "The Future of High Speed Logic in MOS, Bipolar, GaAs, and Josephson Junction ICs"
Continental Ballroom 4
Moderator: C. A. Liechti, Hewlett-Packard Co
Panel Members: H. J. Boll, Bell Labs; B. Dunbridge, TRW; T. R. Gheewala, IBM; J. Magarshak, Thomson-CSF; D. L. Peltzer, Fairchild; and H. G. Sachs, Cray Labs

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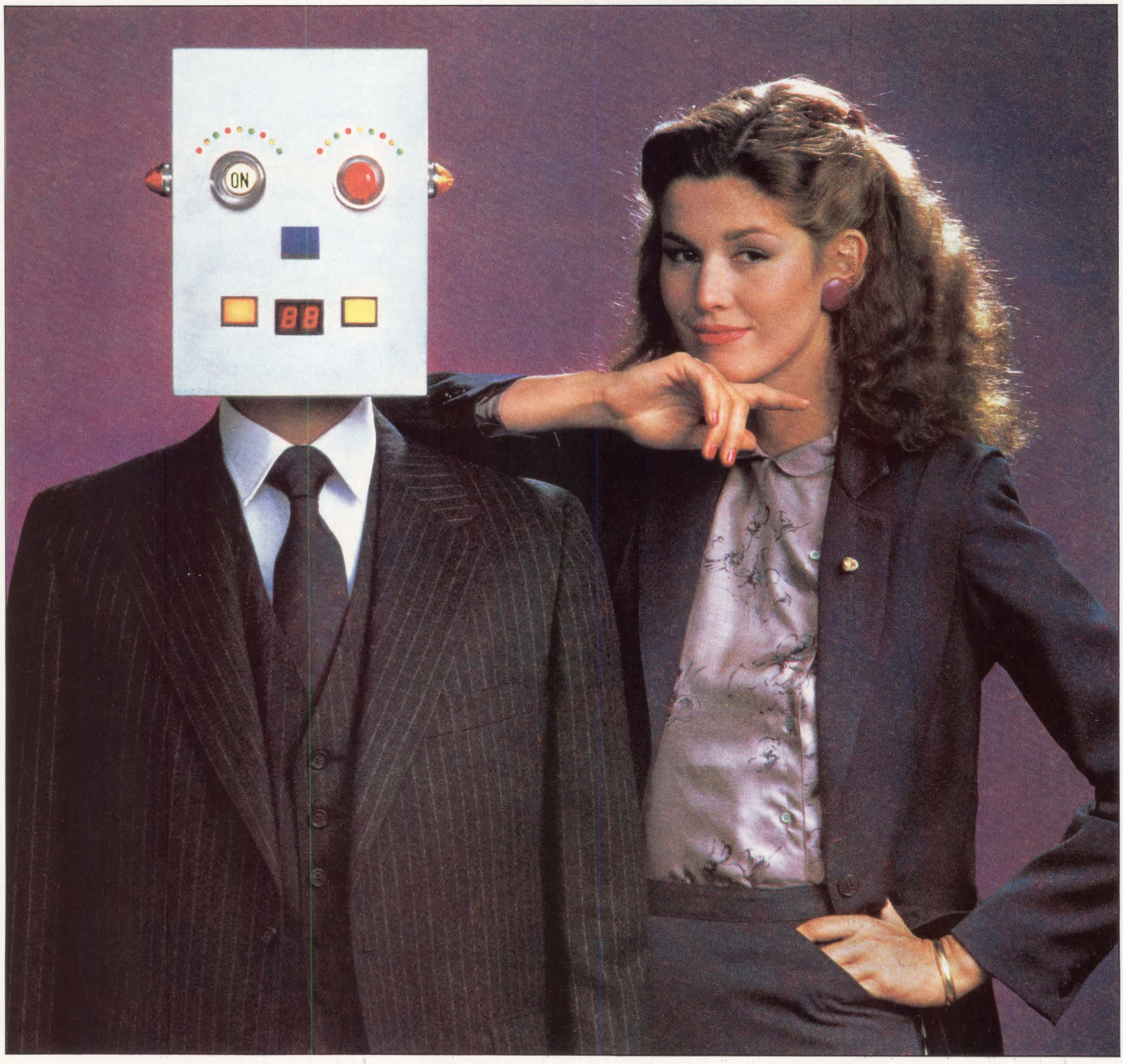

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When it comes to optoelectronics, Dialight offers an enormous selection plus some exclusive advantages. For example, we now package LED indicators singly and in arrays for mounting on PC boards. As soon as you insert them into the board, they're precisely positioned. Installation is far faster. Wave soldering can be done in a single pass. All these features reduce production costs.

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CIRCLE 117 ON INQUIRY CARD

3 "The Data Converter World above 12 Bits"
Continental Ballroom 5
Moderator: J. A. Schoeff, Antron Systems
Panel Members: Z. Boyacigiller, Intersil; P. Burton, Analog Devices, NV; S. Wilensky, Hybrid Systems; B. Gordon, Analogic Corp; J. Memishian, Analog Devices, Inc; J. Sitkewich, Harris Semiconductor; and M. Nagata, Hitachi Central Research Labs

4 "Status and Future Trends in Computer Design Aids"
Continental Ballroom 6
Moderator: D. O. Pederson, Univ of California
Panel Members: S. Domenik, Intel Corp; D. Fairbairn, VLSI Technology, Inc; W. J. McCalla, Hewlett-Packard Co; R. Newton, Univ of California; D. Schweikert, United Technologies Microelectronics Center; and N. Weste, Microelectronics Center of NC

5 "Approaches for Monolithic GaAs ICs"
Continental Ballrooms 7 to 9
Moderator: A. E. Podell, Podell Assocs
Panel Members: D. Hornbuckle, Hewlett-Packard Co; R. Pucel, Raytheon Co; H. Ishikawa, Fujitsu, Ltd; D. Maki, Hughes Research Center; E. Strid, Tektronix, Inc; R. S. Pengelly, Plessey Research; and Y. Takayama, Nippon Electric Corp

6 "Is There Life After 64k?"
Imperial Ballroom
Moderator: R. C. Foss, Mosaid, Inc
Panel Members: R. Gossen, Texas Instruments, Inc; J. Moench, Motorola Semiconductor; W. Sander, Apple, Inc; R. Chew, Tektronix, Inc; K. Itoh, Hitachi Central Research Labs; and J. B. Atkins, IBM Corp

Session 9: Nonvolatile Memories

Thurs 9 am to 12:15 pm
Continental Ballrooms 1 to 4

Chairman: R. H. Dennard, IBM Research Center

9/1 "A Sub-100-ns 32k EEPROM" (9 am)
C. Kuo *et al*, Motorola, Inc

9/2 "A 16k EEPROM" (9:30 am)
G. Yaron *et al*, National Semiconductor Corp

9/3 "A 40-ns CMOS EEPROM" (10 am)
R. G. Stewart and D. Plus, RCA Labs

9/4 "A 128k EPROM with Redundancy" (10:45 am)
W. Spaw *et al*, Intel Corp

9/5 "A 64k Bipolar PROM" (11:15 am)
R. M. Fisher, Harris Semiconductor

9/6 "A Nitride-Barrier Avalanche-Injection EAROM" (11:45 am)
S. Hijiya *et al*, Fujitsu Labs, Ltd

Session 10: Circuits for Microprocessor Systems

Thurs 9 am to 12:15 pm
Continental Ballrooms 5 to 6

Chairman: P. H. Buffet, Digital Equipment Corp

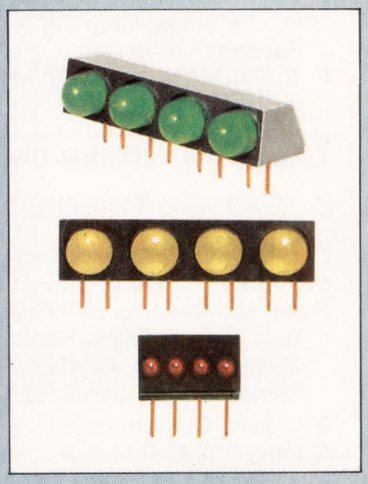
10/1 "16-bit Microprocessor with 152-bit Wide Microcontrol Word" (9 am)
J. F. Sexton *et al*, Texas Instruments, Inc

10/2 "An Adaptive Array Processor LSI" (9:30 am)
T. Sudo *et al*, NTT Musashino Lab

DESIGN IN DIALIGHT LED CIRCUIT BOARD INDICATORS.

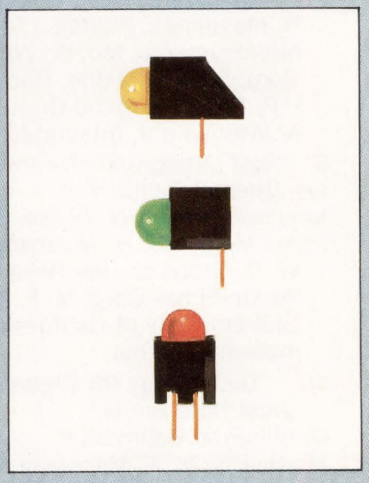
QUAD-LED CIRCUIT BOARD INDICATORS

Series 550 and 555 QUAD-LED™ are 4-element LED arrays. Single packages provide 4-line logic status indication. TTL compatible; separately accessible leads for each element; facilitates PCB mounting and wave soldering. Compatible with respective 550 and 555-2000 series individual units.



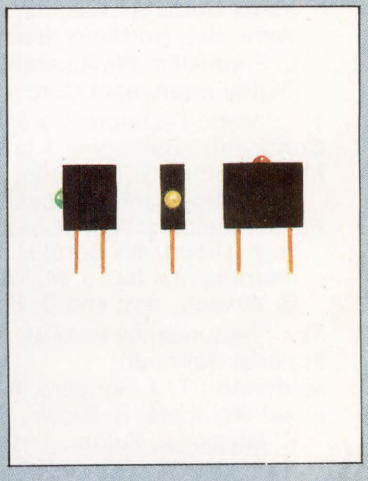
LED CIRCUIT BOARD INDICATORS

Series 550 are LED circuit board indicators with green, yellow, red or bicolor LEDs. Available with or without integral resistor. In standard and high efficiency T 1-3/4 LEDs in choice of 3 configurations to meet all designs and space requirements.



LED CIRCUIT BOARD INDICATORS

Series 555-2000 and 555-3000 are available in red, yellow, green in a range of voltages and currents. Suitable for dense packaging on PC boards, these low cost indicators have applications in logic status troubleshooting, binary display or as circuit board indicators.



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16/4 "A Programmable Speech Circuit Suitable for Telephone Transducers" (3:15 pm)
P. Consiglio and M. Siligoni, SGS/ATES Electronic Components

16/5 "Integrated Active Speech Network for Subscriber Set Application" (3:45 pm)
M. B. Terry and C. P. LeMaire, Mostek Corp

16/6 "A Single-Chip Signaling and Dial Pulse Receiver" (4:15 pm)
P. E. Fleischer *et al*, Bell Labs

Thurs 8 pm, Informal Discussion Sessions

7 "Packaging Technology for Microwave ICs and High Speed Logic"
Continental Ballrooms 1 to 3
Moderator: S. Long, Univ of California
Panel Members: E. Belohoubek, RCA Labs; B. K. Gilbert, Mayo Foundation; R. K. Rinne, IBM Corp; T. Tsukii, Raytheon Co; R. Thorne, Hewlett-Packard Labs; and G. Kaelin, Rockwell International

8 "Semi-Custom Logic"
Continental Ballroom 4
Moderator: A. R. Sass, General Instrument Corp
Panel Members: P. Scott, Signetics Corp; H. Masunaga, Fujitsu, Ltd; M. Gooze, American Microsystems, Inc; W. Walton, Digital Equipment Corp; S. G. T. Maine, General Instrument Corp; I. R. Pearson, Micro Circuit Engineering; and A. Wainwright, Integrated Circuit Engineering

9 "VLSI Lithography for the '80s"
Continental Ballroom 5
Moderator: R. F. W. Pease, Stanford Univ
Panel Members: H. Abraham, Hewlett-Packard Co; W. D. Grobman, IBM Research Center; M. C. King, Perkin-Elmer Corp; M. P. Lepselter, Bell Labs; W. G. Oldham, Univ of California; and G. L. Varnell, Texas Instruments, Inc

10 "Technology for Digital Subscriber Loops and Local Data Buses"
Continental Ballroom 6
Moderator: H. E. Mussman, Bell Labs
Panel Members: J. Huggins, Intel Corp; W. C. Lynch, Xerox Corp; M. Stieglitz, Western Digital Corp; J. B. Terry, Bell Northern Research; A. Boleda, BNR, Inc; L. Freimanis, TSS-Alcatel Corp; and T. Ermolovich, Digital Equipment Corp

11 "VHSIC Technology Approaches"
Continental Ballrooms 7 to 9
Moderator: C. G. Thornton, U.S. Army Electronics Technology and Devices Lab
Panel Members: A. M. Chester, Hughes Aircraft Co; H. A. Cloud, IBM Corp; H. D. Toombs, Texas Instruments, Inc; J. M. Walker, Westinghouse Corp; B. Whalen, TRW; and D. Prestholdt, Honeywell

12 "Redundancy in RAMs...How and When?"
Imperial Ballroom
Moderator: T. J. Rodgers, Advanced Micro Devices
Panel Members: R. Brown, Burroughs Corp; K. Miyasaka, Fujitsu, Ltd; R. Pashley, Intel Corp; R. Proebsting, Mostek Corp; R. Smith, Bell Labs; R. C. Smith, Intel Corp; A. R. Strube, IBM Corp; and S. Matsue, Nippon Electric Co

Session 17: Device Structures and Technology

Fri 9 am to 12:15 pm
Continental Ballrooms 1 to 4

Chairman: J. D. Shott, Stanford Univ

17/1 "Device Applications of Beam Crystallized Silicon-On Insulators" (9 am)
J. F. Gibbons, Stanford Univ

17/2 "HMOS III Technology" (9:30 am)
S. S. Liu *et al*, Intel Corp

17/3 "Signal and Power Distribution for Josephson Technology" (10 am)
M. B. Ketchen *et al*, IBM Research Center

17/4 "A Binary-Analog Correlator" (10:45 am)
W. E. Engeler *et al*, General Electric Research/Development

17/5 "Measurement of Intrinsic Capacitances of MOS Transistors" (11:15 am)
J. J. Paulos *et al*, Massachusetts Inst of Technology

Session 18: Static RAMs

Fri 9 am to 12:15 pm
Continental Ballrooms 5 to 9

Chairman: R. Pashley, Intel Corp

18/1 "ECL Compatible 4k-CMOS RAM" (9 am)
E. L. Hudson and S. L. Smith, Intel Corp

18/2 "A 35-ns 16k NMOS Static RAM" (9:30 am)
K. Anami *et al*, Mitsubishi Electric Corp

18/3 "32k- and 16k-MOS RAMs Using Laser Redundancy Techniques" (10 am)
R. J. Smith *et al*, Intel Corp

18/4 "An NMOS 64k-Static RAM" (10:45 am)
S. S. Liu *et al*, Intel Corp

18/5 "A HICMOSII 64k-bit Static RAM" (11:15 am)
O. Minato *et al*, Hitachi

18/6 "A 64k-bit CMOS RAM" (11:45 am)
S. Konishi *et al*, Toshiba Corp

Session 19: Speech Processing

Fri 9 am to 12:15 pm, Imperial Ballroom

Chairman: R. Brodersen, Univ of California

19/1 "A Monolithic Voice Recorder" (9 am)
T. Takamizawa *et al*, Texas Instruments Japan Ltd

19/2 "C^2MOS Speech Synthesis Systems" (9:30 am)
F. Tanaka *et al*, Toshiba Corp

19/3 "A Single CMOS Speech Synthesis Chip" (10 am)
K. Inoue *et al*, Sharp Corp

19/4 "A Single-Chip Sound Synthesis Microcomputer" (10:45 am)
T. Oura *et al*, Nippon Electric Co, Ltd

19/5 "A Monolithic Audio Spectrum Analyzer for Speech Recognition Systems" (11:15 am)
L. T. Lin *et al*, EG&G Reticon, and R. Runge and D. Conrad, Interstate Electronics Corp

19/6 "A Systolic Processing Element for Speech Recognition" (11:45 am)
N. H. E. Weste *et al*, Bell Labs

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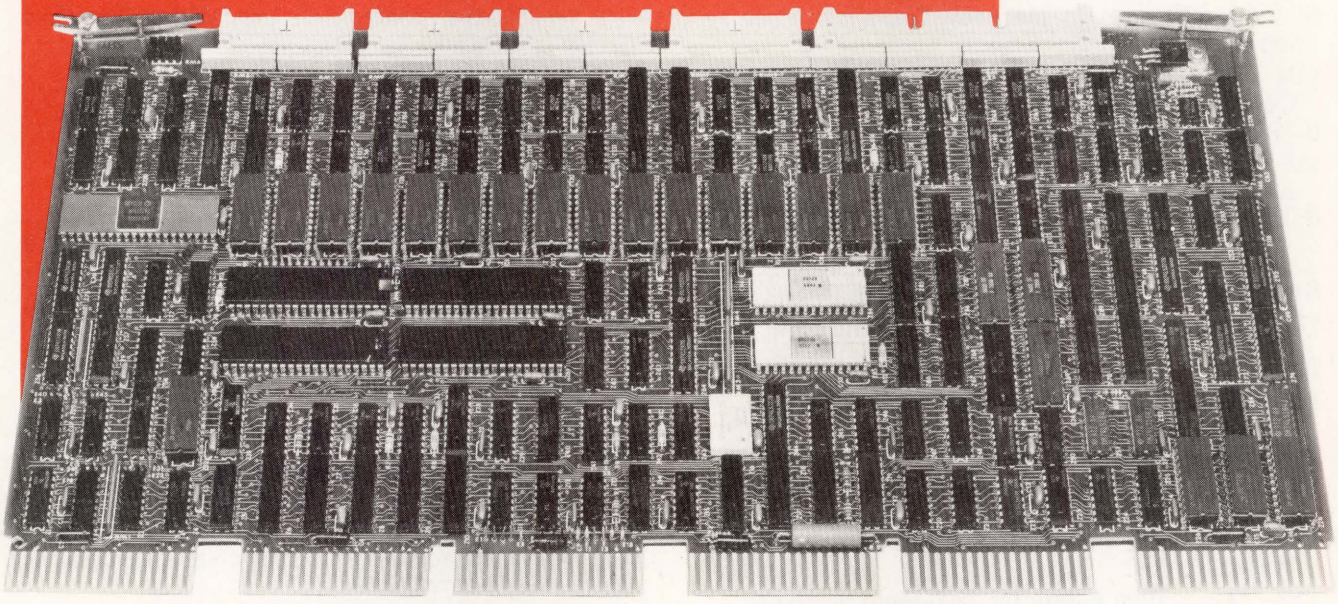

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PDP-11	S33/A	S33/B	S33/C	S33/D
LSI-11	S03/A	S03/B	S03/C	S03/D

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CIRCLE 118 ON INQUIRY CARD

10/3 "A CMOS LSI 16 x 16 Multiplier-Accumulator" (10 am)
R. A. Allen *et al*, TRW Microelectronics Center

10/4 "An Intelligent Hard Disk Controller for Winchester Disks" (10:45 am)
T. Ohtsuka *et al*, Nippon Electric Co, Ltd

10/5 "A 32-bit VLSI System" (11:15 am)
J. W. Beyers *et al*, Hewlett-Packard Co

Session 11: Monolithic Microwave Circuits

Thurs 9 am to 12:15 pm
Continental Ballrooms 7 to 9

Chairman: E. D. Cohen, Naval Electronic Systems Command

11/1 "SOS MESFETS for Monolithic Microwave ICS " (9 am)
S. P. Yu *et al*, General Electric Co

11/2 "S-Band Phase Shifter Using Monolithic GaAs Circuits" (9:30 am)
C. W. Suckling *et al*, Plessey Research

11/3 "A Monolithic GaAs Power FET Amplifier for Satellite Communications" (10 am)
H. Q. Tserng and H. M. Macksey, Texas Instruments, Inc

11/4 "X-Band GaAs Monolithic Voltage Controlled Oscillator" (10:45 am)
B. N. Scott *et al*, Texas Instruments, Inc

11/5 "10-GHz 3-Stage Monolithic Low Noise Amplifier" (11:15 am)
R. E. Lehmann *et al*, Texas Instruments, Inc

Session 12: Data Communication ICs

Thurs 9 am to 12:15 pm, Imperial Ballroom

Chairman: B. T. White, Silicon Systems

12/1 "Echo Canceller for an 80k-bit Baseband Modem" (9 am)
O. Agazzi *et al*, Univ of California

12/2 "A Single-Chip NMOS Analog Front End LSI for Modems" (9:30 am)
Y. Kuraishi *et al*, Nippon Electric, and T. Kimura, NTT Musashino Lab

12/3 "Monolithic Filters for 1200-Baud Modems" (10 am)
L. T. Lin and H-F. Tseng, EG&G Reticon, and L. Querry, Penril Corp

12/4 "Adaptive Equalizer for Digital Communication Networks" (10:45 am)
T. Enomoto *et al*, Nippon Electric Co, Ltd

12/5 "A Differential Phase Shift Keying Modem for Data Transmission Over Power Lines" (11:15 am)
Y. A. Haque *et al*, American Microsystems, Inc, and G. C. Cagle, Rockwell International

12/6 "A Carrier Current Transceiver IC for Data Transmission over ac Lines" (11:45 am)
D. Montcelli and M. Wright, National Semiconductor Corp

Session 13: Optoelectronic Circuits

Thurs 1:30 to 5 pm, Continental Ballrooms 1 to 4

Chairman: G. Baldwin, Hewlett-Packard Labs

13/1 "A Bar Code Reader IC (1:30 pm)
R. H. McCharles, Hewlett-Packard Labs

13/2 "Dynamic Range Fiber Optic Receivers" (2 pm)
G. F. Williams, Bell Labs

13/3 "A Monolithic Laser Driver for Optical Communications" (2:30 pm)
R. G. Swartz *et al*, Bell Labs

13/4 "A Linear Bipolar Optically-Coupled Isolation Amplifier" (3:15 pm)
H. L. Skolnik, Burr-Brown Research Corp

13/5 "A CCD Linear Image Sensor" (3:45 pm)
N. Suzuki *et al*, Toshiba Corp

Session 14: Array and Gb Logic

Thurs 1:30 to 5 pm, Continental Ballrooms 5 to 6

Chairman: R. A. Pederson, Bell Labs

14/1 "GaAs Logic for Multi-Gb Data Generators" (1:30 pm)
C. Liechti *et al*, Hewlett-Packard Labs, M. Namjoo, Stanford Univ, and A. Podell, Podell Assocs

14/2 "A 6k Gate CMOS Array" (2 pm)
T. Kobayashi *et al*, Toshiba R&D Center

14/3 "A 6k Gate CMOS Gate Array" (2:30 pm)
T. Itoh *et al*, Hitachi, Ltd, and S. Horiguchi and H. Yoshimura, NTT Musashino Lab

14/4 "A 2500-Gate Macro Cell Array With 250-ps Gate Delay" (3:15 pm)
S-C Lee and A. S. Bass, Motorola, Inc

14/5 "Logic-in-Memory VLSI for Mainframe Computers" (3:45 pm)
M. Odaka *et al*, Hitachi, Ltd

Session 15: Microwave GaAs FET Oscillators and Amplifiers

Thurs 1:30 to 5 pm, Continental Ballrooms 7 to 9

Chairman: J. W. Gewartowski, Bell Labs

15/1 "An X-Band Dielectrically Stabilized FET Source" (1:30 pm)
J. M. Seligman, Itek

15/2 "GaAs Switched Geometry Oscillator for X and Ku Bands" (2 pm)
B. N. Scott, Texas Instruments, Inc

15/3 "A 5-W Microwave Pulsed Oscillator Using Power GaAs FETS" (2:30 pm)
N. Furutani and Y. Arai, Fujitsu, Ltd

15/4 "A Wideband Monolithic GaAs IC Amplifier" (3:15 pm)
D. B. Estreich, Hewlett-Packard Co

15/5 "Performance Characteristics of Lossy Match vs Feedback Amplifiers in S-C Band" (3:45 pm)
K. B. Niclas and R. R. Pereira, Watkins-Johnson Co

Session 16: Telecommunication Circuits

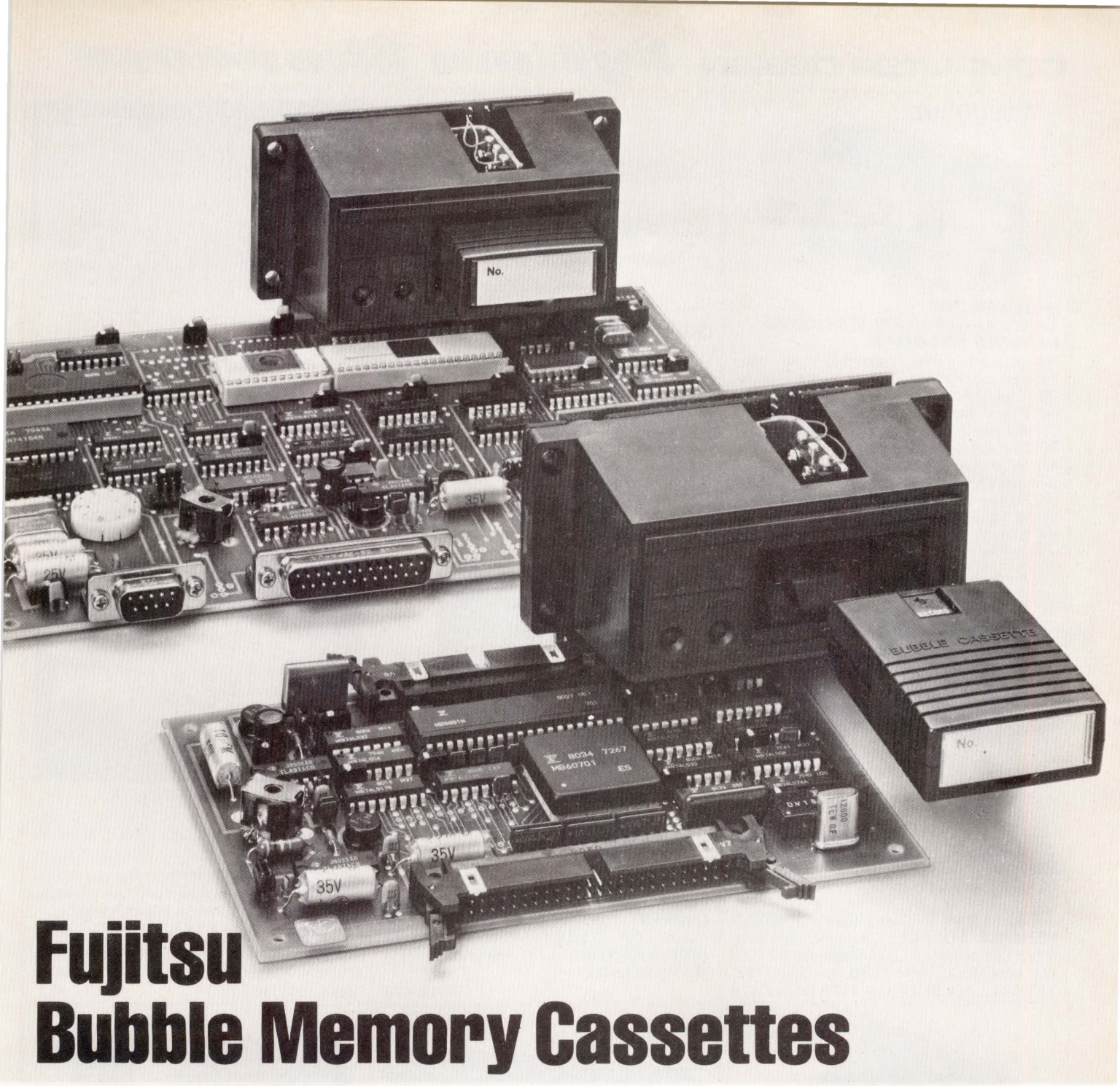
Thurs 1:30 to 5 pm, Imperial Ballroom

Chairman: P. J. Schwarz, Plessey Telecommunications/Office Systems

16/1 "High Voltage Subscriber Line Interface LSIS" (1:30 pm)
K. Kawarada *et al*, NTT Musashino Lab

16/2 "A Hybrid Integrated Trunk and Subscriber Interface" (2 pm)
P. C. Davis *et al*, Bell Labs

16/3 "A 256-Channel Digital Switch Module IC" (2:30 pm)
D. R. Parker *et al*, Plessey Research, and A. N. Morgan, Stentor AS □



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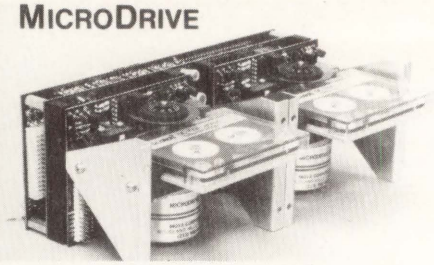
CIRCLE 119 ON INQUIRY CARD

MICRODRIVE



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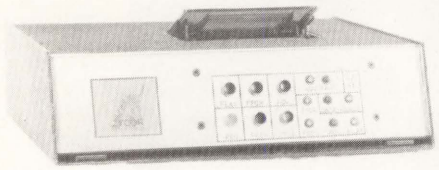
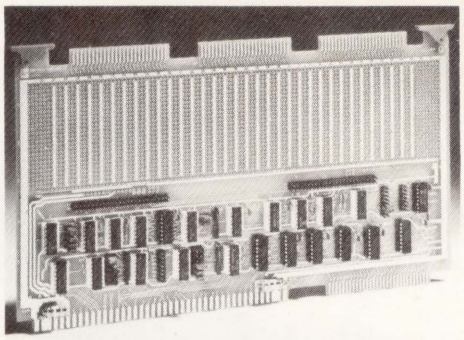


DIGITAL RECORDER

Digital storage capability can be added to terminals, printers, modems etc. by connecting the CA-11 cassette recorder in series with RS-232C, 20 ma current loop or TTL communication lines. No hardware modifications are needed other than matching connectors. The CA-11 can also be used as a stand alone digital recorder. Buad rates from 110 to 1200. $395/Singles. **ZYCOR DATA SYSTEMS**, PO Box 90020, Dept 210, Houston, TX 77090. Tel: (713)363-3261. **CIRCLE 478**



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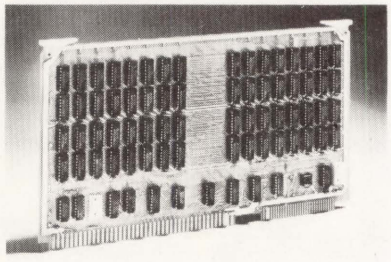

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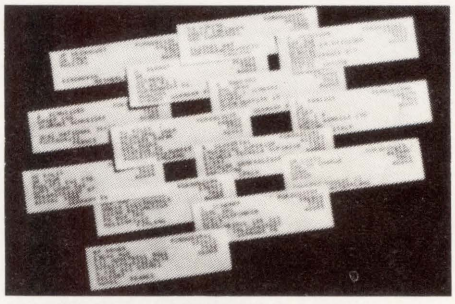

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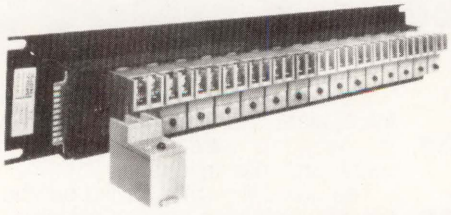

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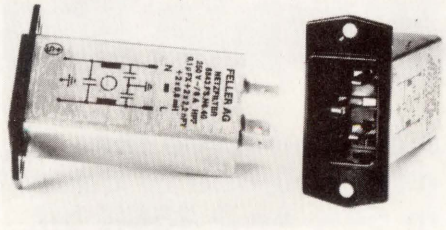

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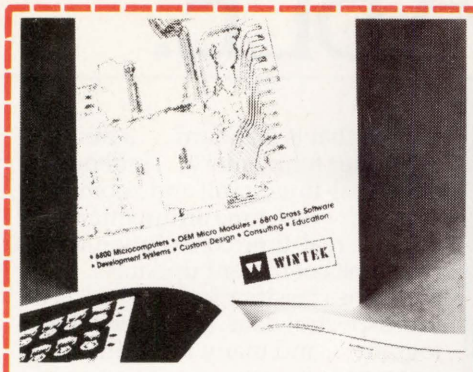

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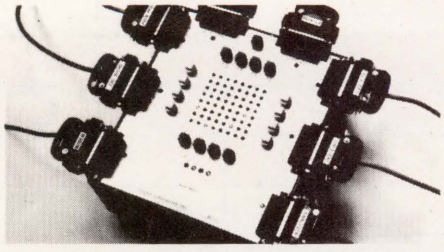

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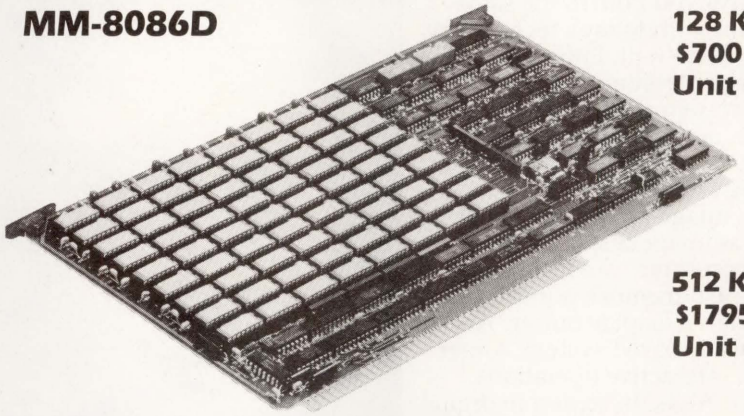

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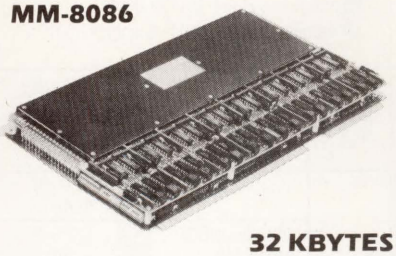
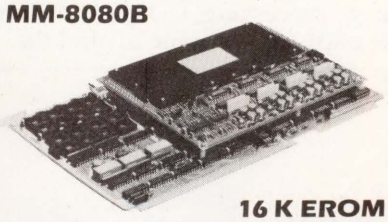


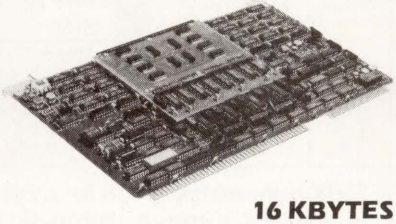
32 KBYTES

MM-8080B



16 K EROM
& 8 K CORE

MM-8086/16



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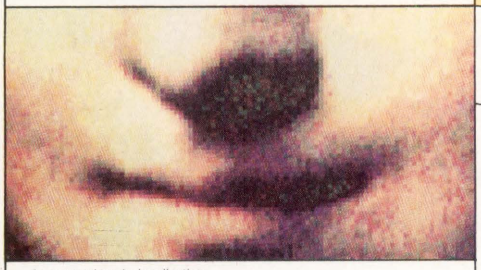

4x zoom using pixel replication.

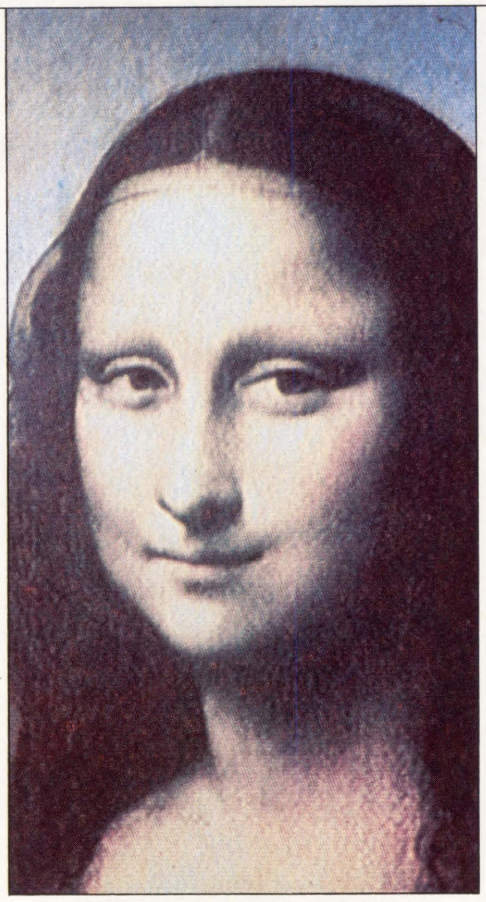

Image of Mona Lisa processed by Combined Logic Research, Hollywood, CA, on a COMTAL Vision One/20 using histogram equalization and function memory modifications for brightness, contrast and color correction.

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COMTAL

■ Image Resolution and Bit Depth ■ Number of Images (i) & Graphics (g) In Typical Configuration				Function Memory Processing	Small Area Processing	Real-Time Arithmetic	Dual User Capability
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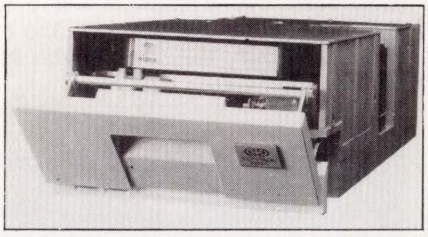
	8000-R Model 65	■ ■	1024^2 x 8 3i, 4g	■			
Stand-alone Image Processing	VISION ONE/10	■ ■	512^2 x 8 4i, 4g	■	■	■	
	VISION ONE/20 Model M8	■ ■	512^2 x 8 7i, 8g	■	■	■	■
	VISION ONE/20 Model M10	■ ■	512^2 x 8 15i, 8g	■	■	■	■
	VISION TEN/24	■ ■	1024^2 x 8 4i, 8g	■	■	■	■
	VISION ONE/12	■ ■	$256^2/512^2$ x 12 3i, 12g/1i, 4g	■			
Image Input	Digital Video Input Processor	Acquires and digitizes filmed images illuminated by a light table; integrates as many as 256 frames; images can be transferred to a VISION ONE/20 or host computer.					

CIRCLE 121 ON INQUIRY CARD

Rigid disk drive provides 16M bytes of storage

9454 Lark™ Micro Unit 8″ (20-cm) rigid disk drive provides 8M bytes of storage on a removable cartridge and 8M bytes on a fixed disk, for a total storage of 16M bytes. It uses the company's 92108 Lark module and compatible cartridges that are top loading for stable alignment of removable media to the drive; however, the cartridges are inserted from the front of the drive for operator convenience. The device's Lark micro interface includes an 8-bit bidirectional bus and LS TTL single-ended transmitters. Its asynchronous bus characteristics allow multiple commands in the same bus transfer. The interface is not SMD interface compatible and depends upon the host system to provide a power source.

Features include a 9.67-MHz transfer rate, low power requirement of 100 W, microcomputer based controller logic, internal fault monitoring, and independent manual write, protection of cartridge and fixed media. An internal recirculating air system eliminates the need for an external air flow system. A linear voice coil actuator provides max accuracy and reliability, and rapid positioning. No electrical adjustments or preventive maintenance is required.



The unit's low mass, lightly loaded flying read/write heads are attached to a precisely controlled linear head positioner. No dedicated servo surface is required for head positioning control, index and sector pulse generation, or the phase locked oscillator reference clock. Embedded servo information is factory written on each data surface in those areas not occupied by header or data blocks. No head alignment or adjustments are required. Two units mount horizontally, or 3 vertically, in a std 19″ (48-cm) Retma rack. Price is $2665 each in OEM quantities. **Control Data Corp,** PO Box O, Minneapolis, MN 55440.

Circle 270 on Inquiry Card

Memory and serial I/O module

MLV-11 dual height module provides 128k bytes of memory and 2 serial I/O ports. With 22-bit addressing capability, memory can be configured at 64k-byte boundaries using DIP switches. The memory uses 64k-bit RAMs, with access times of 300 ns. Serial I/O ports are DLV11-J compatible with 10-pin connectors. Address/vector configuration, UART parameters, and baud rates are switch-selectable. Standard RS-423/232 interface signals are provided. **General Robotics Corp,** 57 N Main St, Hartford, WI 53027.

Circle 271 on Inquiry Card

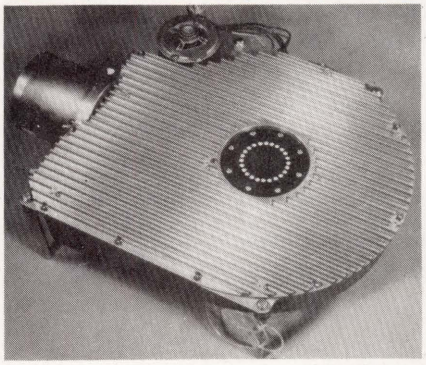
Nonvolatile RAM board

Providing full MULTIBUS compatibility, NVR8010 uses battery-less semiconductor technology and has 8k bytes of high speed static RAM and 1k byte of battery-less nonvolatile "shadow RAM." The nonvolatile RAM is fully speed compatible with the static RAM, and totally transparent to programs in all operating modes. Via jumper straps on the board, the 1k-byte nonvolatile memory block can be logically inserted into the addressing decode structure to occupy any of the eight 1k-byte memory blocks implemented on the board. Nonvolatility is then provided transparently to all other system operation. No special power detection circuits or interrupt processing is required. The board supports both 8-and 16-bit data transfers, and can be used with all the popular 8- or 16-bit microprocessors available in MULTIBUS board format. **Stynetic Systems, Inc,** Flowerfield, Bldg 1, St James, NY 11780.

Circle 272 on Inquiry Card

Winchester disk drives

Advanced Marksman Series (AMS) 190 and 380 drives offer 190M and 380M bytes of fixed storage, respectively, in drives with the same form/fit as the company's 20M-, 40M-, 80M-, and 160M-byte units. Using a linear motor



positioner, the drives provide 25-ms positioning time, claimed to be the fastest positioning time available for any 14″ (36-cm) Winchester drive. Features include a spin motor brake, carriage lock for use during shipment, and a ventilated spindle to provide uniform cooling of the disks. The AMS 190 has a data transfer rate of 960k bps, 24,000 bytes/track, 480 tracks/in, and 7545 bpi; the AMS 380 offers a 1280k-bps transfer rate, 32,000 bytes/track, 712 tracks/in and 10,000 bpi. Avg latency time for both units is 12.5 ms. SMD interface is std. **Century Data Systems, A Xerox Co,** 1270 N Kraemer Blvd, Anaheim, CA 92806.

Circle 273 on Inquiry Card

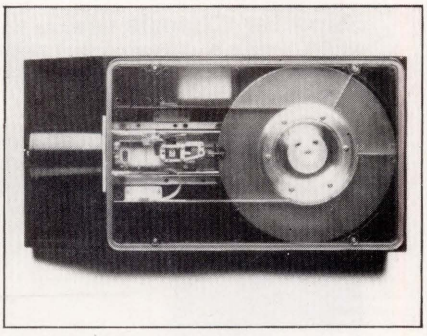
Winchester hard disk subsystem with streaming tape backup

DART-MS1 subsystem for Data General NOVA, Eclipse, and emulating computers includes a 14″ (36-cm), 34M- or 68M-byte Winchester fixed disk drive; a 0.25″ (0.64-cm), 20M-byte streaming tape cartridge drive for backup; DART controller board; chassis; and high performance power supply. It also includes four ports of MUX, master console support, a realtime clock, and a parallel printer. The subsystem's controller accommodates up to four daisy chained disk drives for a total storage capacity of 272M bytes. Price for the 34M-byte subsystem is $8700. **Microtech Business Systems,** 3180 Pullman St, Costa Mesa, CA 92626.

Circle 274 on Inquiry Card

40M-byte, 8″ fixed disk drive

40M-byte member of 6170 series incorporates 3 disks and features a data transfer rate of 800k bytes/s and an avg seek time of 27 ms. Actuator and drive motors are located outside of the sealed air flow environment, preventing heat buildup and lengthening motor life. A brushless dc motor directly drives the disk spindle. The drive has an MBTF of 10,000 h and requires no scheduled maintenance. **BASF Systems Corp,** Crosby Dr, Bedford, MA 01730.

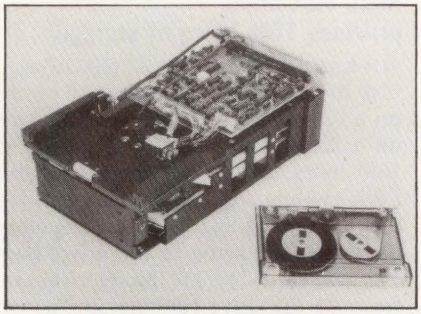


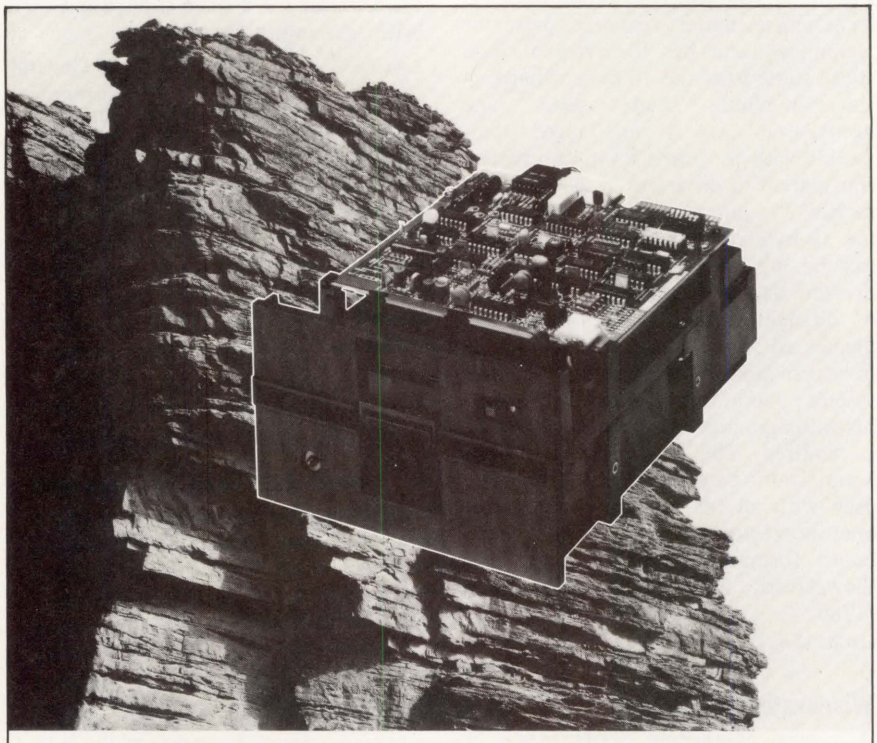
Circle 275 on Inquiry Card

0.25″ cartridge magnetic tape drive

STR^R-Stream offers Winchester disk users high capacity backup with an interface that is identical to a Winchester; alternative interfaces include ANSI, 9-track tape, and DEI funnel look-alikes. Using a std DC-300XL cartridge, the device has a capacity of 17M bytes (unformatted) and can transfer 1.4M bytes/min in the streaming mode. Its form factor is identical to an 8″ (20-cm) floppy disk. Soft error rate is <1 in 10^9. An incremental mode of operation allows online, active file editing and data logging. Priced at $1115 in quantities of 100, the std system deck includes read after write circuitry, NRZ to MFM encode/decode, infrared tape position sensing, formatter, command and status lines, 4-track read after write head, optical encoder, CRC circuitry, and interface electronics. **Electronic Processors, Inc**, 1265 W Dartmouth Ave, Englewood, CO 80110.

Circle 276 on Inquiry Card





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Superior Chassis features fiberglass reinforced polyester (FRP) which, unlike aluminum, won't stretch with heat. Extra-rugged and precision molded, the unit also has a shield to insulate the head from outside interference.

25 Years of Leadership in all magnetic recording technologies is your assurance of a quality product you can rely on. For complete information on all TEAC Rock-Solid Floppy Disk Drives (FD-50 Series) — including our one-year warranty and full technical support and service — just write:

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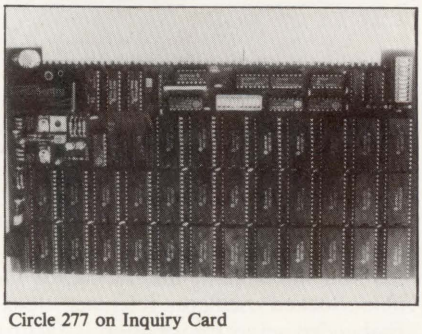
TEAC Corporation of America
Industrial Products Division
7733 Telegraph Road, Montebello, CA 90640
(213) 726-8417

64k-byte CMOS static RAM board

Offered for the SS50/C bus and including battery backup, board is fully compatible with 6800/6809 DMA techniques. It is guaranteed for 2-MHz operation with no wait states or clock stretching. The board requires less than 0.25 A at 8 V and is nonvolatile using an onboard nickel-cadmium battery; with the battery fully charged, memory contents remain intact for a min of 21 days. The entire board can be hardware write protected by a switch located at the top of the board. **GIMIX Inc**, 1337 W 37th Pl, Chicago, IL 60609.



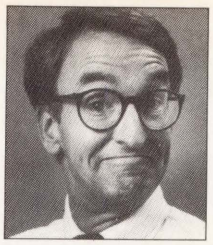
Circle 277 on Inquiry Card

Quad-density memory board

Offered for Hewlett-Packard's 9826 series desktop computer, WKBP-4, with 256k bytes of RAM, provides four times the capacity of the 64k-byte boards that HP offers for the 9826. The user can plug in an ample amount of RAM for any purpose, without tying up more than a few of the computer's 8 card slots, leaving most of the 9826's interface slots available for connection of peripherals, ROM based BASIC, etc. The board is priced at $1995. **Eventide Clockworks, Inc**, 265 W 54th St, New York, NY 10019.

Circle 278 on Inquiry Card

CIRCLE 122 ON INQUIRY CARD

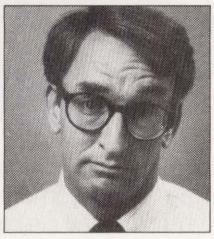


Barney Stevenson just spent two years programming and de-bugging a process control system in assembly code.

Now Barney thinks he deserves some congratulations for his efforts.

Sorry Barney,

NO CIGAR.



Barney Stevenson thought he deserved a pat on the back. As project manager at Smart Widgets, Inc., he had taken on the biggest real-time process control headache of his life. And after 24 months he'd finally succeeded in programming and de-bugging Smart's newest product.

We think Barney missed the boat.

Barney figured the choice was simple. High level languages like Pascal and Fortran could program quickly, but would run too slowly and take up too much memory. Assembly code would take longer to program and de-bug, but was the only answer for real-time applications.

Wrong.

Real wrong.

Barney didn't know about FORTH: a language that runs nearly as fast as assembly, is just as compact (if not more so), yet can cut development time by a factor of 10 over assembly language.

He also didn't know about FORTH, Inc.

They're the people who invented this remarkable tool, evolved it, and for 10 years have seen it used in thousands of applications . . . from running an observatory to sorting baggage, from video games to industrial robotics. Virtually every real-time application imaginable.

The latest evolution of FORTH is called polyFORTH:™ An incredible programming environment available for just about any mini or micro processor.

For Barney? Still no cigar. But for *you*, FORTH offers a software tool that in speed, compactness and extensibility, simply has no match.

So call us at (213) 372-8493. Or write FORTH, Inc., 2309 Pacific Coast Highway, Hermosa Beach, California 90254. We'll rush you the latest on polyFORTH,™ and tell you where you can see it in action.

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...the real-time saver.

CIRCLE 123 ON INQUIRY CARD

LS-TTL gate array features 2000 gates on a single chip and 1-ns/gate delay time

Supplied in a 135-pin plug-in square package, B2000 gate array is processed with a double-layer metal gate, low power Schottky process. Die size is 7.7 x 7.7 mm². The array has 2108 internal 3-input NAND gates with clamp diodes on the output, and contains 112 I/O buffers. Two power supplies are required: 5 V (V_{CC1}) and 2.3 V (V_{CC2}). The V_{CC1} supply is LS-TTL compatible and is utilized for the I/O buffer gates; V_{CC2} power is used to bias internal gates and results in 0.95-ns delay time (fanout = 1) and 0.65-mW/gate power consumption.

With the application of a customized double-layer metal mask, gates and buffers can be interconnected to form a variety of random logic configurations. To facilitate error-free implementation of the metal interconnection routing, a CAD system interfaces customer specifications with the manufacturing function. This CAD software provides the physical layout of the array, line routing, mask pattern data generation, and test programs, as well as computer simulation of the final circuit. To speed design time and to improve layout efficiency, 21 predesigned logic cell combinations are contained in the computerized cell library. Typ development time is 16 weeks. **Fujitsu Microelectronics,** 2985 Kifer Rd, Santa Clara, CA 95051.

Circle 279 on Inquiry Card

Radiation hardened 4k CMOS static RAMs

HS-6504RH 4096 x 1 RAM and HS-6514RH 1024 x 4 RAM are fabricated using the company's radiation hardened, self-aligned silicon gate technology. The units offer functional total dose capability of 5 x 10^5 rad silicon, latch-up free operation to greater than 5 x 10^{11} rad silicon/s, 500-μW standby power, 25-mW/MHz operating power, and typ access times of less than 250 ns. Typical applications include satellites, nuclear instrumentation, and weapon systems (both tactical and strategic). **Harris Corp, Semiconductor Group,** PO Box 883, Melbourne, FL 32901.

Circle 280 on Inquiry Card

Industrial quality memory components and microprocessors

MKI family offers extended temp operation over the −40 to 85 °C range, with complete electrical testing to verify functionality to ac and dc parameters. Each device also receives MIL SPEC 125 °C burn-in to improve system reliability. Military 100% screening criteria are applied and AQL levels tighter than MIL-STD 883B are guaranteed. The family currently includes 16k x 1 dynamic RAMs, 2k x 8 static RAMs, 2k x 8 EPROMs, and the Z80/Z80A 8-bit microprocessor. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 281 on Inquiry Card

Our message is clear!

We're dedicated to innovative CRT display design, quality production standards and complete customer satisfaction. Whatever your display needs, we have the experience and talent to design it, or improve it. Contact us today!

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CIRCLE 124 ON INQUIRY CARD

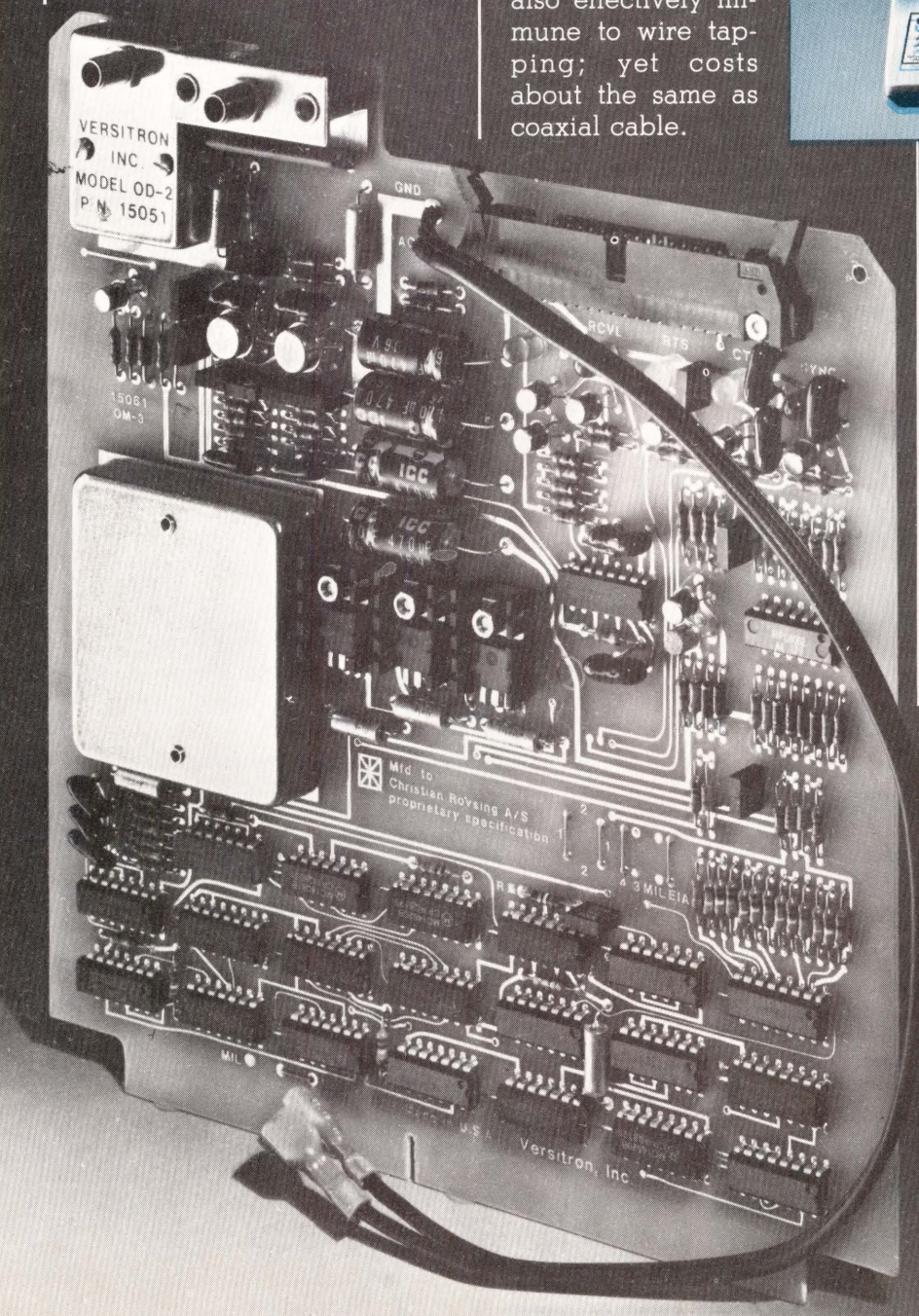
Plug-in Fiber Optic Modem Expands Capabilities of OEM Units

Equipment manufacturers can now integrate a powerful, new Fiber Optic Modem directly into their equipment; resulting in a device that will provide exceptional data throughput performance in any local distribution environment.

The Case for Fiber Optics: The use of fiber optics for local data distribution assures that your end product will perform as it was designed to; regardless of the environment in which it is used. Unlike conventional wire cables, optic cables are totally unaffected by rfi, adjacent noisy cables, or heavy duty electrical equipment. A big plus is that it is also effectively immune to wire tapping; yet costs about the same as coaxial cable.

The Reasons for Using Versitron: In addition to the inherent advantages of fiber optics, Versitron's OM series of plug-in modems offers an impressive list of performance specifications. These include: operating range up to two kilometers (6500 feet), synchronous or asynchronous operation at data rates up to 38.4 KBPS, true EIA handshaking (three separate control signals in each direction are multiplexed along with the data), and an optional alarm circuit that will shut down all traffic if the cable is tampered with.

For details on how our optical modem can help you to significantly improve the marketability of your end product, give us a call at (202) 882-8464; or write Versitron, Inc., 6310 Chillum Place, N.W., Washington, D.C. 20011



VERSITRON, INC.

CIRCLE 125 ON INQUIRY CARD

8k CMOS EPROMs

IM6657 (2048 x 4) and IM6658 (1024 x 8) EPROMs are fully decoded and erasable by exposure to UV light. Access time is 300 ns at 10 V for the IM6657/58A, and 450 ns at 5 V for the IM6657/58. Power requirements are 100 μA standby current and 138 mW max operation power, with a single 5-V supply. Inputs and 3-state outputs are TTL compatible and allow for direct interface with popular common system microprocessor bus structures. Onchip address registers and chip select functions simplify system interface requirements. Devices are available in std 24-pin DIP packages and are priced at $24 each in 100-unit quantities. Military versions are also available. **Intersil, Inc,** 10710 N Tantau Ave, Cupertino, CA 95014.

Circle 282 on Inquiry Card

20-V linear semi-custom array

Pin for pin compatible with the A20M, A20MS features a collector current of 400 mA and contains 812 components on a die measuring 10.1 x 15.1 cm. Replacing the A20M with this array provides higher operating current at the same saturation voltage (400 mA at 1.5 V_{sat}) or lower saturation voltage and lower power dissipation at the same operating current (200 mA at 0.75 V_{sat}). The array contains a wide range of linear components that the designer can interconnect via specifying the final mask. Onchip components include npn and pnp transistors, base and pinch resistors, Zener and Schottky diodes, etc. **Micro-Circuit Engineering Inc,** 1111 Fairfield Dr, West Palm Beach, FL 33407.

Circle 283 on Inquiry Card

64k dynamic RAM

MCM6665A second generation version of the MCM6664A dynamic RAM, offers improved performance and high reliability at lower cost. The device preserves the address strobe ratios (ASRs) of $t_{RAC}/t_{CAC} = 2$ that provide a $t_{CAC} = t_{RCD}$ specification for 64k dynamic RAMs. Extended t_{RCD} provides additional switching time for the high capacitive load on the column address drivers, and the reduced t_{CAC} provides for faster page mode operation. The part offers industry std soft error performance of 0.1% per 100 h, improved row access time, lower input capacitance, wider operating margins, and exceptional tolerance to V_{CC} slew. Prices start at $19.40 for a 200-ns device in quantities of 100 or more. **Motorola Inc, MOS Integrated Circuits Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 284 on Inquiry Card

ISL gate arrays

8A1260 and 8A1542 integrated Schottky logic (ISL) gate arrays offer gate delays of 4 ns, allowing direct replacement of std LST^{2}L devices in any application. The 8A1260 has 1200 gates, 60 I/Os, and replaces up to 65 LS devices; 8A1542, with 1500 gates and 42 I/Os, can replace more than 80 LS devices. Both have a power dissipation of 168 μW/gate and a temp range of -55 to 125 °C. Available packages include plastic and ceramic DIPs and leadless chip carriers. Nominal prices in 5k quantity range from $28 to $40 for the 8A1260 and from $26 to $36 for the 8A1542, depending upon package type and pin count. **Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94086.

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FOR YOUR CARD & BADGE DATA COLLECTION NEEDS

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- Manual-Fed Card Readers
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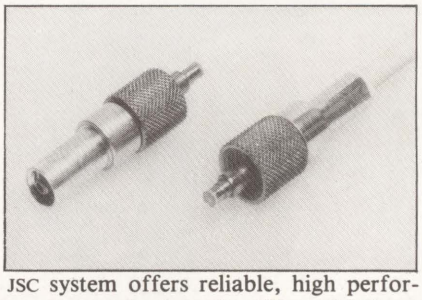
CIRCLE 126 ON INQUIRY CARD

INTERCONNECTION & PACKAGING

Fiber optics connector system



JSC system offers reliable, high performance terminations for 125- and 140-μm cables. Mateable with certain SMA types, the system provides cable attachment by means of a crimped back shell approach, offering an epoxy free method, with cable retention equivalent to the cable's recommended max tensile loading. The only adhesive required is a drop of rapid curing epoxy that is applied at the ferrule tip. Polishing is performed using the 698-JSC-T301 polishing tool. Cable to cable connections are achieved with the 698-JSC-INI interconnect device that features a captivated bushing for a precise alignment. Low loss of 0.9 dB is typ (90% probability) with 100-μm core/140-μm clad fibers. **Augat Inc,** 40 Perry Ave, Attleboro, MA 02703.

Circle 286 on Inquiry Card

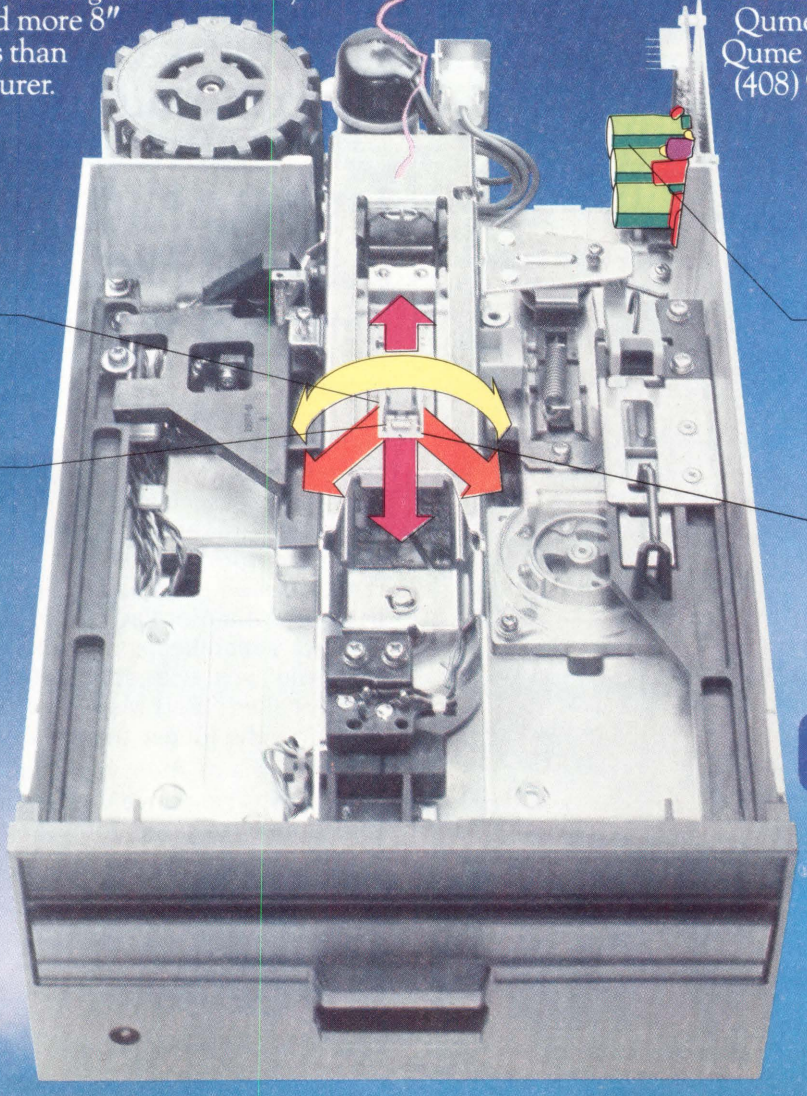
QUME

AC

For standard AC floppy drive applications, nothing beats QumeTrak 842. Our exclusive TriGimbal™ design heads glide smoothly over the disk surface for the gentlest media ride in the business. That's one good reason why QUME has installed more 8" double-sided drives than any other manufacturer.

DC

For special battery-backup or overseas installations, you get the same smooth media treatment from the QumeTrak 842DC drive. For more information about the gentlest, most reliable floppy disk drives in both AC and DC, call or write Qume Product Marketing, Qume Drive, San Jose, CA 95131. (408) 942-4000



ROLL, PITCH and YAW: TriGimbal head rotates on three axes for smooth ride.

TAP TEST: Qume beats industry standard 100,000 impacts to 25,000 impacts.

TWO VOLTAGES: +12 and +5 volts DC. No negative voltage required.

CONTINUOUS CONTACT TEST: Qume beats industry standard 10 million passes to 3 million passes.

Qume®
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CIRCLE 127 ON INQUIRY CARD

IEEE 488 molded cable assemblies

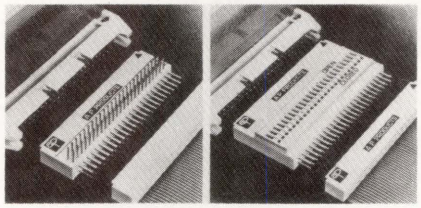
Assemblies feature the company's 5900 or 5910 interface bus cable and IEEE 488, 24-pin connectors. A male/female back to back connector configuration at each end allows piggyback interconnects to facilitate multi-instrument stacking. Each molded cable assembly ensures environmental protection throughout the cable length. Field replacement of damaged cable or changes in system configuration can be effected without downtime. In addition, the 5910 series meets the rfi/emi requirements of FCC Docket 20780. **Alpha Wire Corp,** 711 Lidgerwood Ave, Elizabeth, NJ 07207.

Circle 287 on Inquiry Card

Flat cable connection devices

Allowing immediate access to previously inaccessible lines, Intra-Connector is interjected between mating system connectors to provide the external pin contacts that can either be probed individually or connected to another cable assembly. The pins also act as a "cube tap," allowing an existing system to daisy chain into new areas.

With the Intra-Switch, any number of lines can be individually opened or closed at system interconnection points, saving time spent testing flat ribbon cable systems. Applications include switching command signals to control boards as well as switching I/O signals to or from test equipment and for programming optional preset logic functions. An Intra-Switch in conjunction with two Intra-Connectors forms a complete test assembly for probing signals under no load and full load conditions. Both devices are available in 20-, 26-, 34-, 40-, and 50-contact versions. **A P Products Inc,** 9450 Pineneedle Dr, Mentor, OH 44060. Circle 288 on Inquiry Card



POWER SOURCES & PROTECTION

Switching power supplies

MF series semicustom supplies feature output power levels of 150 W, open frame construction, dual input, and multiple outputs. The lightweight, 13″ x 2.56″ x 5.12″ (33- x 6.5- x 13-cm) supplies offer 75% typ efficiency; wide input line variations of 15% to −26% for a total 41% range; modular construction; short circuit and overvoltage protection; high frequency operation (50 kHz); conformity to UL-478, BS, and VDE; holdup time of over 20 ms; and inrush currents of 40 A. Up to 5 outputs are available with customer specified voltages and currents within the overall 150-W limit. Differential ripple and noise is less than 1% plus 75 mV, pk-pk. Op temp is up to 50 °C without derating, and rise time is within 100 ms. **Panasonic Co, Electronic Components Div,** One Panasonic Way, Secaucus, NJ 07094.

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24-28-40 position on .600 centers
64 position on .900 centers

COMPLETE ARIES CAT. IN EEM— VOL. 1 : 1635 to 1670

CIRCLE 128 ON INQUIRY CARD

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"THANKS for the MEMORY"

Belting Industries makes belts for use on common shafts and equipment where there is no allowance for take-up, especially computer disk and paper transport drives.
What puts Binco ahead in belting technology is their use of a more advanced style of weave — a weave which keeps the belts' basic dimensions the same even after constant stretching pressure. That's called "Belt Memory", and the better the memory, the longer the life of the belt.
Binco — one of the nation's largest suppliers of belts, with five convenient locations throughout the country to serve you.
You'll be thanking them for the memory.

BINCO "It Gets Around"
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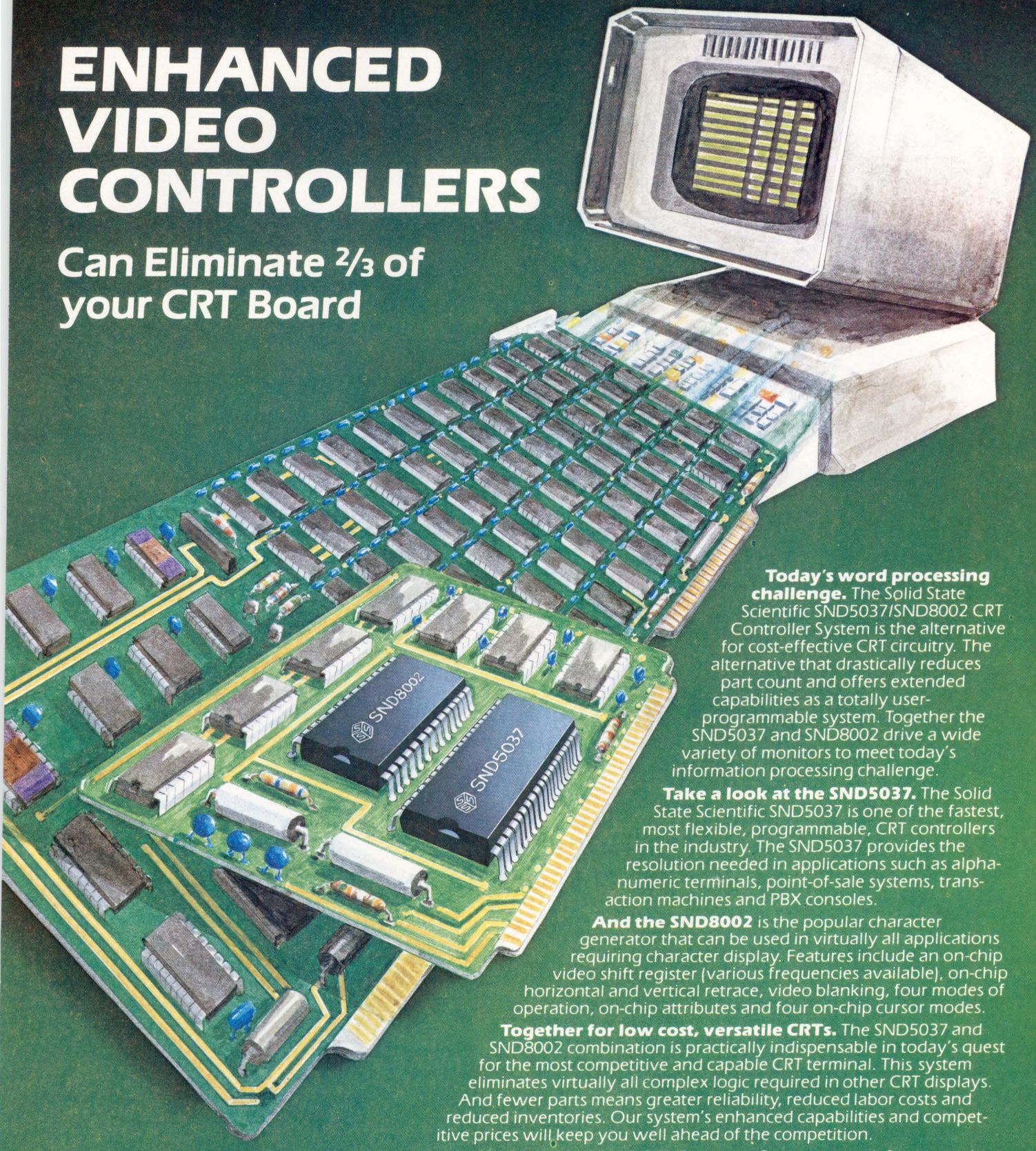
20 Boright Ave., Kenilworth, N.J. 07033, (201) 272-8591

CIRCLE 129 ON INQUIRY CARD

ENHANCED VIDEO CONTROLLERS

Can Eliminate 2/3 of your CRT Board



Today's word processing challenge. The Solid State Scientific SND5037/SND8002 CRT Controller System is the alternative for cost-effective CRT circuitry. The alternative that drastically reduces part count and offers extended capabilities as a totally user-programmable system. Together the SND5037 and SND8002 drive a wide variety of monitors to meet today's information processing challenge.

Take a look at the SND5037. The Solid State Scientific SND5037 is one of the fastest, most flexible, programmable, CRT controllers in the industry. The SND5037 provides the resolution needed in applications such as alpha-numeric terminals, point-of-sale systems, trans-action machines and PBX consoles.

And the SND8002 is the popular character generator that can be used in virtually all applications requiring character display. Features include an on-chip video shift register (various frequencies available), on-chip horizontal and vertical retrace, video blanking, four modes of operation, on-chip attributes and four on-chip cursor modes.

Together for low cost, versatile CRTs. The SND5037 and SND8002 combination is practically indispensable in today's quest for the most competitive and capable CRT terminal. This system eliminates virtually all complex logic required in other CRT displays. And fewer parts means greater reliability, reduced labor costs and reduced inventories. Our system's enhanced capabilities and competitive prices will keep you well ahead of the competition.

Put the SND5037/SND8002 CRT Controller System to work for you today by calling your local Solid State Scientific sales office. Application support is available by writing to our Applications Department, Solid State Scientific, Montgomeryville, PA 18936 or by calling Marketing, at (215) 855-8400.

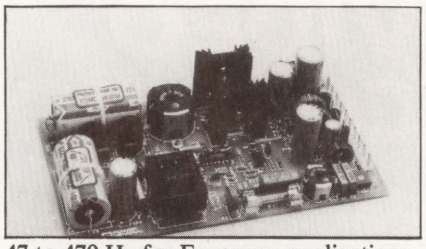
Solid State Scientific

CIRCLE 130 ON INQUIRY CARD

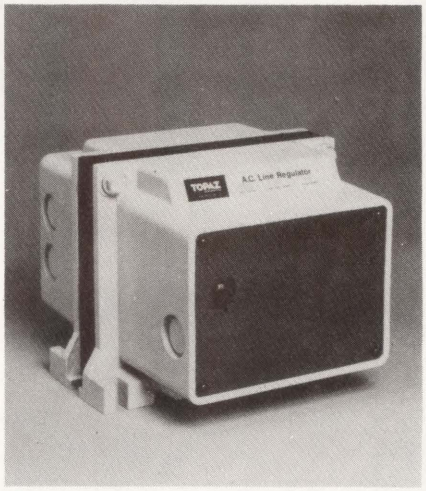
50-W, multiple-output switching power supplies

Series 4050 power supplies are true off the line switchers with up to 4 output voltages on a single PCB. Full rated output is provided over an ambient temp range of 0 to 50 °C with a 2%/°C derating to 71 °C. Four models are offered: 4050-1 (5 V at 6 A, −5 V at 1 A, 12 V at 1 A, and −12 V at 1 A); 4050-2 (5 V at 6 A, −5 V at 1 A, 15 V at 1 A, and −15 V at 1 A); 4050-3 (5 V at 6 A, 12 V at 1.5 A, and −12 V at 1 A); and 4050-4 (5 V at 6 A, 15 V at 1.5 A, and −15 V at 1 A). The power supply input offers pin strappable voltage ranges of either 85 to 130 Vac, or 170 to 260 Vac at 47 to 470 Hz for European applications. Ripple and noise equal 50 mV pk-pk or 15 mV rms. Other basic specs include line regulation of ±0.1%, load regulation of ±0.2%, temp coefficient of ±0.02%/°C, transient response of 300 μs to 1% of final value, and input to output isolation of 1000 Vac. Holdup time is 32 ms, with input surge current at 10 A. Overvoltage protection is set at 6.25 Vdc; relative humidity range is 5% to 80% non-condensing. Current limit, input fusing, soft start, and rfi filtering are std. **Power General,** 152 Will Dr, Canton, MA 02021.

Circle 290 on Inquiry Card



Voltage regulators



Series 77000 line regulators are 98% efficient and provide significant energy savings compared to ferroresonant and other types of regulating devices. They feature low output impedance, eliminating the need to oversize circuit breakers and associated hardware, and provide a narrow ±7% voltage regulation band for input voltages from 85 to 125 Vac. Ac voltages that drop as low as 82 Vac or climb as high as 130 Vac are controlled to within ±10% of nominal. The regulators eliminate short term voltage drops caused by rapid load changes, operate over a frequency range of 47 to 63 Hz, and are available in single- and 3-phase models. **Topaz, Inc, Powermark Div,** 3855 Ruffin Rd, San Diego, CA 92123.

Circle 291 on Inquiry Card

READ-OUT
OR
SQUINT-OUT

The difference is the clear competitive edge you gain with Glasflex "Non-Glare" matte finish cell-cast acrylic.

Because it offers superior optical and surface qualities, Glasflex "Non-Glare" reduces glare better than continuous cast sheet.

Its "instant readout" capability makes Glasflex "Non-Glare" ideal for use on CRT screens, instrument panel faces, microfiche readout screens, rear view screens, instrument dials, gauges, and digital instrument readouts.

Offered with different degrees of light diffusion, Glasflex "Non-Glare" acrylic is available in clear or color sheets fabricated in sizes, shapes and thicknesses to suit your requirements.

And you can rely on Glasflex's over half-century's expertise in acrylics to clear up your most glaring "instant readout" problems. See what we mean.

Phone or write today.

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When you're down to the wire™:

Nobody can support you with mass termination products like Spectra-Strip can.

We make more variations of flat cable than any one: laminated, extruded and bonded, grey and color coded. Jacketed cable for inter-cabinet runs. Ground plane cable to reduce cross-talk. Even a twisted-pair flat cable that can be mass-terminated, so you get the performance you want and the lower costs you need.

Our connectors are more of the same: high quality, high performance and low prices. Choose from a range of pin headers and receptacles, DIP plugs and sockets, PCB transitions, and card edge connectors built to the relevant portions of MIL-C-83503 and MIL-C-21097. And IDC D-Subminiature connectors with metal shells (fully intermateable and intermountable with any of the other real D-Sub's).

We can also lower your capital investment, inventory and labor overhead. Let us prepare your jumpers for up to 20% less than you're paying now. Call your nearest Spectra-Strip value-added distributor for economical, fully-tested flat cable and IDC connector assemblies. Or call Garden Grove for custom assemblies that combine flat cable with the other kinds of interconnects you need. Whatever your applications, if you're down to the wire on price, performance or delivery, there's one simple solution:

Spectra-Strip, 7100 Lampson Ave., Garden Grove, CA 92642, telephone (714) 892-3361 and 720 Sherman Ave., Hamden, CT 06514, telephone (203) 281-3200.

In Europe, Spectra-Strip Ltd., Romsey, Hampshire, England, telephone (0794) 517575.

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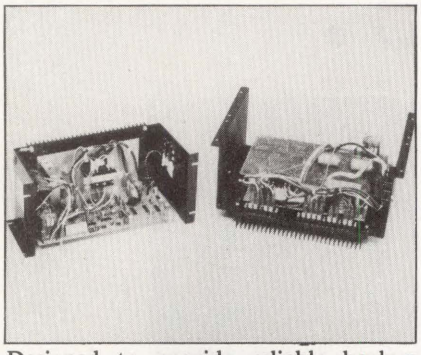
CIRCLE 132 ON INQUIRY CARD

Open frame standby power supply units

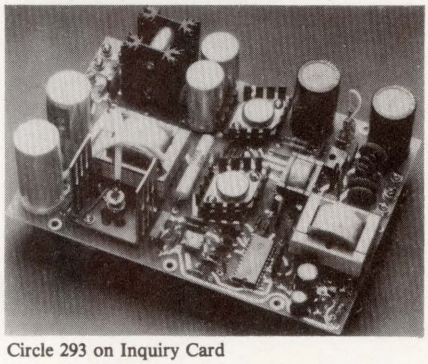


Designed to provide reliable backup power for use in brownouts or blackouts, both SPS 1-250-12E and SPS 1-500-24E have ac output voltages of 120 Vac ±5%, 60 Hz ±5% from inverter. The 250 has output power of 200 Wac continuous, input voltage of 12 Vdc normal, and input current of 21 Adc; the 500 has output power of 400 Wac continuous, input voltage of 24 Vdc, and input current of 21 Adc. Both have overload short circuit protection. Battery charger for both units has 120-Vac ±10%, 60-Hz input voltage. Model 250 has input current of 0.2 A max, output voltage of 13.8 ±0.1 Vdc, and output power of 18 W max; model 500 has input current of 0.3 A max, output voltage of 27.6 ±0.1 Vdc, and output power of 35 W max. Overload protection for battery charger is rated at 1.5 A max. **Welco Industries, Inc,** 9027 Shell Rd, Cincinnati, OH 45236.

Circle 292 on Inquiry Card

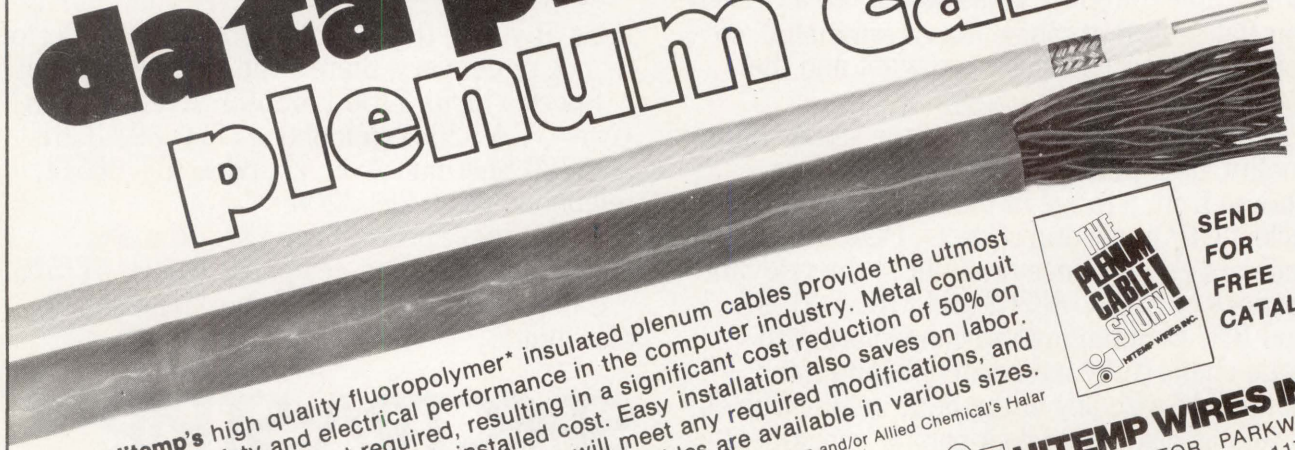
Switching power supply

OPS-50 features a user selectable 120/240-Vac input and 3 fully regulated outputs. Standard dc outputs include 5 V at 8 A, 12 V at 1 A, and −12 V at 1 A; or 5 V at 8 A, 15 V at 1 A, and −15 V at 1 A. Standard features include free-standing PCB construction, soft start input, full overcurrent protection, input emi filtering, 5-V overvoltage protection, 65% typ efficiency, and full brownout protection. The supply measures 2.5″ x 8″ x 5.65″ (6.35 x 20 x 14.35 cm). Primary applications include VDTs, monitors, small computers, and floppy disk systems, as well as process control equipment. **General Instrument Corp, Computer Products Div,** 1401 Lomaland Dr, El Paso, TX 79935.



Circle 293 on Inquiry Card

HITEMP WIRES INC.
THE SOURCE FOR ALL YOUR
data processing
plenum cable



Hitemp's high quality fluoropolymer* insulated plenum cables provide the utmost in safety and electrical performance in the computer industry. Metal conduit is not required, resulting in a significant cost reduction of 50% on the installed cost. Easy installation also saves on labor. Hitemp will meet any required modifications, and the cables are available in various sizes.

*DuPont's Teflon and/or Allied Chemical's Halar

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516 234-3020
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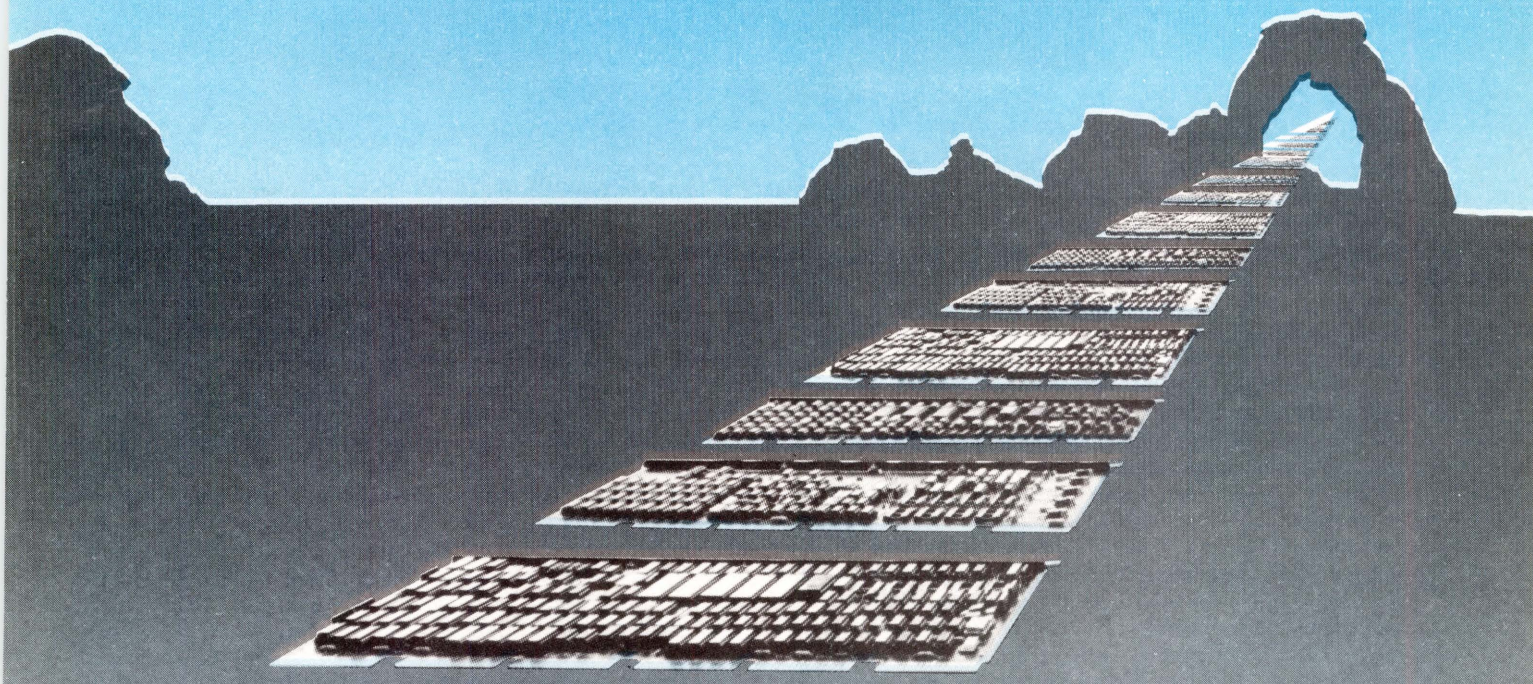
CIRCLE 133 ON INQUIRY CARD

UNLEASH THE POTENTIAL



use ACC's protocol packages for DEC systems

X.25 Link your PDP-11 to today's X.25 packet-switched networks with our IF-11/X.25. Send messages to remote sites over Telenet, Tymnet, PSS, Datapac, Transpac and others.

Our IF-11/X.25 supports X.25 Levels 1, 2 and 3. To a PDP-11, it looks like a peripheral device with 33 data paths. One path serves supervisory functions while the 32 other full-duplex paths are available for your data transfer.

We offer the IF-11/X.25 in two versions. One, with LAP and BSC control characters, operates up to 9.6 Kbps. Another, using LAP-B and HDLC standards, operates up to 56 Kbps.

ACC's User Mode X.29 software package is offered separately. It interfaces 32 PDP-11 terminals to our IF-11/X.25, making your message sending direct and simple.

3270 Our IF-11/3270 allows you to link a PDP-11 or VAX to one or two remote IBM 370-type mainframe computers. You can cluster up to 31 DEC VT-100 (or other ANSI-compatible) terminals with your DEC computer, or have a stand-alone configuration without it.

From a terminal, you can access the DEC processor, access either of the remote 370 mainframes, or transfer data between them. Under your control, our IF-11/3270 can switch display from normal DEC operation in an RSX environment to emulation of a standard intelligent IBM 3270 terminal.

A typical installation entails a centralized IBM database with DEC minicomputers at remote field sites. Since the IF-11/3270 does the BSC processing, it's especially advantageous where DEC resources would be strained by the imposition of protocol processing.

3780 Our IF-11/3780 attaches to your DEC PDP-11 or VAX, emulates IBM 2780 or 3780 Remote Job Entry stations, and sends data to one or two remote IBM 370-type mainframes. Since you'll transfer data to our IF-11/3780 by fast DMA, and process the 2780/3780 protocols with it, your DEC resources are virtually unaffected.

The vast array of available UNIBUS peripherals gives you great flexibility. You can input a job from a peripheral, process it on the DEC computer, then queue it for input to the 370s. Output from the 370s can be stored on disc, processed if desired, then printed or otherwise handled at your, not the system's, convenience.

U200 Link a PDP-11 or VAX to two remote Sperry Univac 1100 mainframe computers with our IF-11/U200. It enables you to cluster up to 31 DEC VT-100 display terminals or small printers with the DEC computer. Or you can cluster them in a stand-alone configuration without it.

Since protocol processing is handled by the IF-11/U200, and since computer access is on a high-speed Direct Memory Access (DMA) basis, the unburdened DEC computer continues to be available for everyday tasks.

Users at their terminals can access the PDP-11 in a normal RSX-11M environment, switch at will to a remote Univac 1100 mainframe under Uniscope 200 emulation and, when needed, can initiate data transfer between the two computers.

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FOR EUROPEAN REPRESENTATIVE, CONTACT: DACI, ROSKILDEVEJ 398, DK-2610 RØDOVRE, DENMARK. PHONE (01) 41 51 33. TELEX 15080.

CIRCLE 134 ON INQUIRY CARD

AC line conditioners

Plug-in Voltector[R] series 6 conditioners protect minicomputers, microcomputers, and microprocessor controlled equipment against destructive voltage spikes, surges, and transients, as well as against rfi. Units protect against 500-A surges with 10-μs rise times and 1000-μs half-amplitude decay times. They also attenuate rfi between 1 and 1000 MHz in both common and transverse modes by more than 60 dB. In addition, the bidirectional units prevent disturbances created by power supplies, motors, switches, solenoids, etc, from entering the 110-V power line. When the unit is plugged into a multiple output strip, it provides positive spike protection for equipment that is plugged into the other outlets on the strip. Five models are available from 1 to 10 A. **Pilgrim Electric Co,** 29 Cain Dr, Plainview, NY 11803.

Circle 294 on Inquiry Card

DATA COMMUNICATIONS

Single-board, 4-port statistical multiplexer

CP1 communications processor provides statistical multiplexing of up to 4 asynchronous data channels on a single 11.5″ x 12.5″ (29.2- x 31.7-cm) circuit board. Composite link bandwidth is up to 19.2k baud (optionally to 56k baud); aggregate channel bandwidth is up to 38.4k baud, enabling all channels to function at 9600 baud. Standard on all models are terminal activated diagnostics, statistics, and configuration (menu driven from any attached terminal). Configurations are stored in nonvolatile memory, and any channel or system parameter can be set locally or downtime loaded. OEM volume pricing starts at $750. **Scitec Corp Pty Ltd,** 83 York St, Sydney, NSW 2000, Australia.

Circle 295 on Inquiry Card

High speed modems

SE35 and SE36 are designed for use in applications involving high data transmission speeds, such as high speed multiplexer links, disk to disk data transfer, file dumping, and load shedding. SE35 operates as a conventional baseband modem at either end of the link when transmission is required over telephone lines within a single exchange area. When communication is required over a long distance involving wideband transmission, the SE36 is used with the SE35. The SE36 translates data onto a high frequency carrier for transmission over a telephone group band channel. Data transmission is synchronous at fixed rates of 48k, 56k, 60k, 64k, or 72k bps. Both modems are equipped with CCITT V.35 interface. **SE Labs (EMI) Ltd,** Feltham, Middlesex, England.

Circle 296 on Inquiry Card

OUR SPECIAL PRINTERS SATISFY SOME VERY SPECIAL CUSTOMERS:

NCR, Eastman Kodak, Ford, Westinghouse, TRW, Honeywell, American Airlines, TWA, Amtrak, Raytheon Data Systems, N.Y.C. Off-Track-Betting.

And that's just to name a few. Major corporations — both OEM's and end-users — are sold on the quality and reliability of Computer Terminal Systems special printers.

Their confidence has made us the world's leading supplier of airline and entertainment ticket printers. Our printers interface with any computerized ticketing system on the market.

Our unique drum and hammer design, microprocessor control and precision paper movement deliver typewriter-quality printing at high speeds. We've engineered our printers with the fewest possible components for maximum reliability at a sensible price.

So if, you need ticket, label or form printers for special applications, call or write us. ***We are the Special Printer Specialists.***

CTS
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65 South Service Road, Plainview, NY 11803/516-752-1965

CIRCLE 135 ON INQUIRY CARD

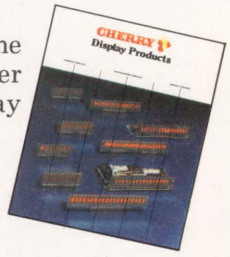
You don't need a lot of lettuce to get a Cherry

16 character display system for the OEM

The Cherry W416-1050 16 alphanumeric gas discharge display system is a lot more than "bare bones" even though it's priced at just $96 in lots of 5,000. It is equipped with microprocessor controlled circuitry including drivers, character generator, refresh memory and provides 19 control functions at a price so low it's ideal for OEM product applications.

Easy-to-read half inch high 14 segment characters, 7-bit ASCII input, adjustable brightness, fully addressable cursor, and flashing display are but a few of many outstanding features found in this display system. Comes complete with metal mounting bracket to facilitate installation. Works indoors or out from 0° C to 55° C. Best of all this bright new display system is available off-the-shelf.

FREE! Yours for the asking:
Complete information on the full line of Cherry 16, 20 and 24 character alphanumeric displays and display systems.



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Worldwide affiliates and phone numbers: Cherry Semiconductor Corp., East Greenwich, RI, U.S.A., 401-885-3600 • Cherry Mikroschalter GmbH, Auerbach, Germany, 09 643 181 • Cherry Electrical Products Ltd., Harpenden (Herts) England, (05827) 63100 • Cherco Brasil Industria E. Comercio Ltda., Sao Paulo, Brazil, 55 (011) 246-4343 • Hirose Cherry Precision Co., Ltd., Kawasaki, Japan, 044 933 3511

CIRCLE 136 ON INQUIRY CARD

In an age when new standards are constantly emerging, one disk consistently meets or exceeds them all.

Maxell. The Gold Standard.

Not all disks are created equal. Some are better than others. To find out what's best for you, look for Maxell disks. They now carry the Gold Standard symbol of quality. It's your assurance Maxell disks meet or exceed every definition of quality. No matter who establishes it. We've earned this universal superiority by never relaxing our uniquely demanding quality control. Every aspect of manufacturing is checked, then checked again.

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There is a Maxell disk for the floppy system you use, or plan to use. Check your computer's instructions. Or write for our complete, highly informative brochure.

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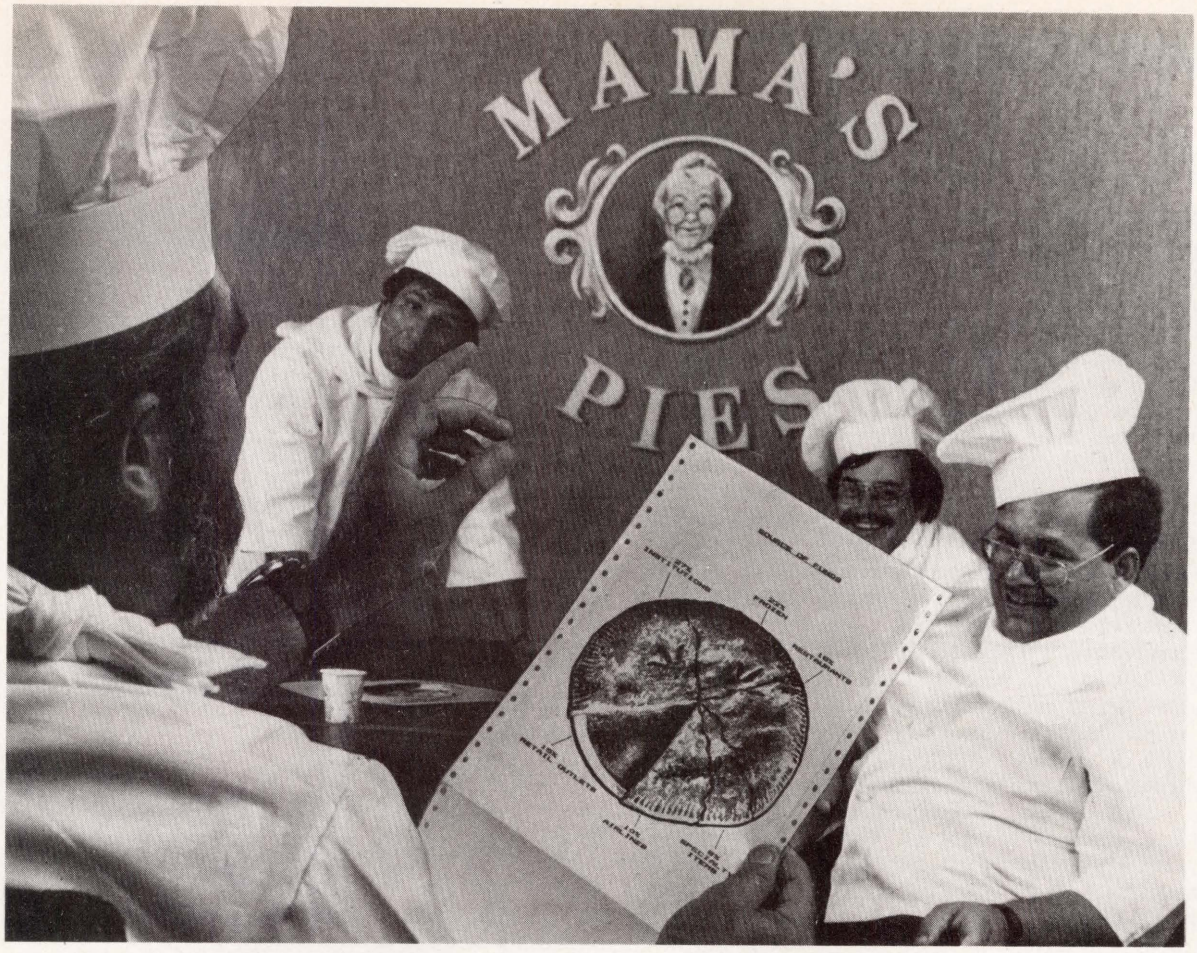
CIRCLE 137 ON INQUIRY CARD



Other printers make pie charts. Ours make pie charts you can sink your teeth into.

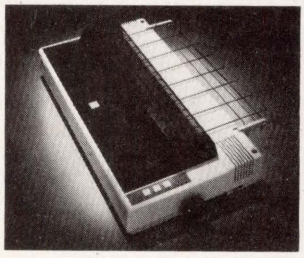
Epson.

Most printers will give you simple graphs and charts — so long as you don't want too much detail. Epson printers, on the other hand, start out with correspondence quality printing, an unequalled reputation for reliability, and a remarkably low price, and then back it up with the most precise, sophisticated and versatile graphics capabilities in their class.

So you not only get eye-appealing pie charts, you get advanced features like 12 separate type faces including compressed printing, multiple forms handling, bidirectional printing and a logical seeking function, plus a standard dot addressable graphics capability so precise that no one, to our knowledge, has yet written software that utilizes all the resolution it is capable of.

Our MX-80 Type II and 136-column MX-100 give you 60/120 dots per inch horizontally and up to 72 dots per inch vertically; our MX-82 gives you high density graphics that can precisely place up to 10,368 dots in a square inch. That's resolution enough for even the fussiest user.

So with Epson, you get better printers and better graphics. And more. You get a better price. Because we're the world's largest, we can work with you on large quantities or specialized requirements. And because we sell more printers than anybody in the world, we can afford to sell each one for a little less.



Epson. OEM. That's about as clear as we can say it in words. But we could draw you a picture.

EPSON
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OEM Products Division

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CIRCLE 138 ON INQUIRY CARD

Q-bus/UNIBUS multiplexers

Configured for Q-bus applications, the MLSI-DZ11-A/422 8-line asynchronous multiplexer offers EIA RS-422 "long line" capability in combination with RS-232-C on a line-selectable basis. Using the line-selectable feature, the user can have any combination of RS-422 and RS-232-C lines. The RS-422 lines allow terminals with corresponding circuitry to be placed up to 3000′ (914 m) from the computer. The device is composed of a quad module, an 8-channel distribution panel, test connectors, and cabling between the module and the panel, which includes a self-contained power supply. Each line of the multiplexer is programmable from 50 to 19.2k baud. The unit offers switch-selectable device addressing and interrupt vectors, and includes dataset control. Its 4-level interrupt enables prioritizing and ensures compatibility with UNIBUS operational software. A similar multiplexer for UNIBUS computers is designated MDB-DZ11-A/422. **MDB Systems, Inc**, 1995 N Batavia St, Orange, CA 92665.

Circle 297 on Inquiry Card

2400-bps modem

LSI 24C serves as a direct replacement for AT&T's 201C modem on either private leased lines or dial-up lines. The 2-wire, half-duplex modem can also be interfaced to 4-wire lines, and is fully compensated for operation over satellite links as well as land lines. Train time is 7 ms, while MTBF is greater than 30,000 h. The modem is packaged on a PC card housed in a standalone unit. Ten units can be installed in a std 19″ (48-cm) rack nest. **Paradyne Corp**, 8550 Ulmerton Rd, Largo, FL 33541.

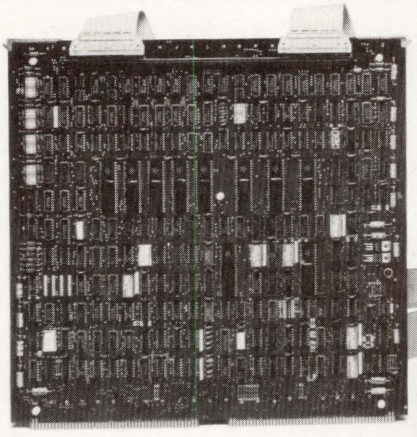
Circle 298 on Inquiry Card

Combination modem/concentrators

Series 2 Micro8000 concentrator modem combines a statistical multiplexer and a matched MOS/LSI modem in a compact desktop cabinet, eliminating the need for separate enclosures, cables, and power cords. The device supports up to 16 terminals, each running at up to 9600 bps. Its built-in modems are rated at 2400, 4800, or 9600 bps. Features include statistical multiplexing of up to 4 synchronous channels concurrently with asynchronous channels (16 total); a command port for online troubleshooting, channel reconfiguration, data collection, and other control functions; terminal activated channel test for troubleshooting telephone lines and communications from the user's terminal keyboard; terminal initiated channel configuration for changing the assignment of a channel from the user's keyboard; speed conversion for matching terminals and ports running at different rates; and data compression for greater concentration efficiency. **MICOM Systems, Inc**, 20151 Nordhoff Ave, Chatsworth, CA 91311.

Circle 299 on Inquiry Card

OUR MODEL 400 I/O CONTROLLER IS



SIMPLE but SOPHISTICATED... POWERFUL but INEXPENSIVE

IF YOU'RE A NOVA/ECLIPSE USER, you won't want to miss this!
Our new Model 400 I/O Controller actually replaces three DG boards: two ULM Muxes (4241, 4241A), and line printer controller.

Model 400 interface features include:

- 8 channels of ULM multiplexer
- 2 general purpose console controllers
- 1 parallel line printer
- Real Time Clock

All ten asynchronous ports are switchable for RS232 or current loop, and all device codes are fully selectable. All popular brands of printer are supported and the warranty is good for a full 2 years.

Single unit price (only $2100) includes a 10-port distribution panel, ribbon cables and line printer cable.

If you're interested in the Model 400 or any other Custom Systems products, call or write for more information.

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Telephone: (612) 941-9480 Telex: 290975

CIRCLE 139 ON INQUIRY CARD

Eliminate Color Hard Copy Headaches in CAD/CAM graphics.

COLORPLOT™ makes it simple.

Now you can interpret your CAD/CAM graphics quickly and accurately — in full color hard copy. It's simple with the Trilog COLORPLOT.

COLORPLOT printer/plotters employ an uncomplicated, reliable design to provide raster matrix impact printing at its best. You get all of the benefits of CAD/CAM color plotting — and none of the headaches.

Trilog's patented multicolor technology provides full color or black printing on plain fanfold paper at 100 dots per inch resolution. Additional features include flexible color mixing (up to 256 colors), 100% duty cycle, and built-in diagnostic self test.

COLORPLOT also offers text quality printing at 150 LPM or matrix quality at 250 LPM. Yes, it's a line printer too.

Best of all, COLORPLOT is economical. No toners or chemicals are required. Full color hard copy is typically less than 25¢ per copy or, if you use it as a line printer, only 1¢ per copy.

Contact Trilog today for further information on the COLORPLOT printer/plotter. It's affordable, reliable, versatile, and it's sold and serviced by a worldwide distribution network.

We make it simple
for fewer CAD/CAM headaches.

TRILOG

17391 Murphy Avenue
Irvine, California 92714
(714) 549-4079 TWX (910) 595-2798

CIRCLE 140 ON INQUIRY CARD

Bell compatible modem line

Asynchronous modems compatible with similar Bell designated models, the 103J operates at 300 bps, while the 212A operates at 300 or 1200 bps. Both units attach directly to switch networks and provide unattended automatic answer. Synchronous modems in the line operate at 2400, 4800, and 9600 bps. Model 201C operates at 2400 bps over leased or dial-up lines; 208 A/B operates over private lines or switched circuits at 4800 bps; and V.29 compatible 9600 operates at 9600 bps over private line circuits. All modems provide diagnostic test capability and self-testing. Analog, digital, and remote digital loopback tests help isolate communication problems. **ICOT Corp**, 830 Maude Ave, Mountain View, CA 94043.

Circle 300 on Inquiry Card

SYSTEM ELEMENTS

Image digitizing system controls up to 6 digitizing cameras

PERIPHICON 500 series image digitizing system includes the 521 image digitizing camera and the 502X image digitizer controller that allows the camera to interface with DEC LSI-11 and PDP-11 architectures using either Q-bus or UNIBUS. The system controls up to 6 digitizing cameras and is available in 3 configurations: 5022, controlling up to 2 cameras; 5024, controlling up to 4 cameras; and 5026, controlling up to 6 cameras.

For each camera, exposure time and gray scale level rendition (up to 15 gray scale levels) are software programmable. Sensitivity is equivalent to ASA 200 emulsion and field of view is 14 cm at 1 m. An f 1.6/16-mm lens, with C mount and focus from 0.2 to infinity, is std. A full range of lenses and optical systems is available. Camera measures 8.2 x 4 x 2.5 cm (excluding lens and connector).

Each controller channel is completely independent of every other channel. For max data throughput, acquisition channel pairs can share one digitizing camera; one channel acquires the image from the camera and the other communicates with the host processor using two 16-bit registers. An image can be acquired in less than 2 ms. Max pixel interrogate rate is 110,000 pixels/s for the Q-bus. Consisting of one camera and an interface card, a basic system is priced at $2500. **Hinds International, Inc, Instruments Div**, PO Box 4327, Portland, OR 97208.

Circle 301 on Inquiry Card

Precision op amp

OP-37 features pk-pk noise of 80 nV in the 0.1- to 10-Hz bandwidth, and spot noise of 3 nV/$\sqrt{Hz}$ at 1 kHz. Offset voltage is 10 μV, slew rate is 17 V/μs, gain bandwidth is 63 MHz, and long-term drift is 0.2 μV/month. The device is compensated for a min voltage gain of 5 and has 1/f noise corner frequency of 2.7 Hz. Other specs include a min output swing of $\pm$10 V into 600 Ω, voltage gain of 1.8M, common-mode and power supply rejections in excess of 120 dB, and input bias current of 10 nA. The device is available in 8-lead DIPs and 8-pin TO-99 cans. It is offered with 2 temp ranges ($-$55 to 125 °C and $-$25 to 85 °C) and 3 grades of electrical specs. **Precision Monolithics, Inc**, 1500 Space Park Dr, Santa Clara, CA 95050.

Circle 302 on Inquiry Card

Isolation amplifier

Model IA194 offers a wide 30-kHz bandwidth, high linearity, 3000-V I/O/power isolation, 100-μs settling time, 90-dB common-mode rejection, externally programmable gain, a floating internal supply for powering an external transducer, and external synchronization of the internal oscillator used in obtaining the input isolation. Its 0.1% linearity ensures compatibility with 10-bit data acquisition systems, and input voltage noise is held to 3 μV, 10 Hz to 1 kHz, with 40-pA max current noise for the same range. Relative accuracy, including all effects of offset, temp, and linearity, is $\pm$0.5% over the full range of 0 to 80 °C. Device measures 3.6″ x 2.27″ x 0.55″ (9.14 x 5.76 x 1.39 cm). **Intronics**, 57 Chapel St, Newton, MA 02158.

Circle 303 on Inquiry Card

Size 8 stepping motor

Offered in VR and PM types, stepper is a 4-phase design with 100 Ω/phase. The motor has a 15° step angle and a high step accuracy of 3%. Input voltage is 28 Vdc, and holding torque is 1 oz-in (0.007 N • m). Ball bearing construction adds to the long life of the motor. A rear shaft is optionally available. **Eastern Air Devices**, 1 Progress Dr, Dover, NH 03820.

Circle 304 on Inquiry Card

Wideband monolithic op amp

With gain bandwidth of 60 MHz, AM-411 features slew rate of 50 V/μs and settling time of 1 μs to 0.1%. An uncompensated device, the amplifier is stable at closed loop gains of greater than 10 without external compensation. It has an open loop gain of 150,000 V/V; dc input characteristics include a max input bias current of 50 pA, input offset current of 50 pA max, and common-mode rejection ratio of 80 dB. Input offset voltage is $\pm$1.0 mV max and input offset voltage drift is typ 5 μV/°C. Output drive capability is $\pm$12 V at $\pm$10 mA min. The amplifier is available as AM-411-2C, operating over the 0 to 70 °C range, or AM-411-2M, covering the $-$55 to 125 °C military temp range. Both are packaged in 8-lead hermetically sealed TO-99 cases. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.

Circle 305 on Inquiry Card

Thimble fonts

Five fonts for Spinwriter™ printers, including a font that prints Arabic in its entirety, full Script-Multilingual A, Dual Gothic-Multilingual A, Courier 72-Multilingual A, and Prestige Renown 15/12, feature a durable, low mass "thimble" print element that contains up to 128 chars with an avg service life of more than 30M impressions. The Arabic font is believed to be the first font in the industry that prints every variation of the calligraphic Arabic language. Script, Dual Gothic, and Courier 72 fonts utilize 127 of the 128 char positions and offer full upper- and lowercase alphabetical chars, numerics, punctuation, and special symbols, as well as upper- and lowercase foreign accents. The Prestige Renown 15/12 font, also utilizing 127 char positions, offers additional printing capabilities to the legal and sales markets. In 15-pitch, the font contains upper- and lowercase alphabetic chars, numerals, punctuation, and special symbols such as trademark, paragraph, and copyright. In 12-pitch, the font contains uppercase alphabetic chars. NEC **Information Systems, Inc**, 5 Militia Dr, Lexington, MA 02173.

Circle 306 on Inquiry Card

Edge-abuttable membrane switches

Switches allow designers to abut any 2 or more switches while maintaining a continuous center to center key spacing. The line is available on 0.75″ and 1″ (1.9-and 2.54-cm) center to center spacings. Available switch formats include common bus and matrix in 1 x 4, 2 x 2, 2 x 3, 3 x 3, 3 x 4, 4 x 4, and 4 x 5. **W.H. Brady Co, Xymox Div**, PO Box 571, Milwaukee, WI 53201.

Circle 307 on Inquiry Card

Brilliance, Intelligence and Economy in One High Resolution Terminal.

RAISE YOUR GRAPHICS STANDARD!

Price/performance you couldn't get before in a high resolution raster terminal no matter how far up you climbed—it's yours in the Genisco G-1000.

The G-1000 high resolution (1024 x 792) desk top terminal offers extraordinary brilliance and contrast with full raster erasability, *plus* the intelligence of a Z-8001 microprocessor and 16K each of RAM and PROM. The price is less than $9,000 in OEM quantities.

What you get for your money is the industry's only true raster replacement for the Tektronix 4014-1 terminal (plug to plug and software compatible) and a no-end-in-sight expandable, fully programmable tool for CAD/CAM, plot previewing, mapping and many other present and future applications.

Expand your G-1000 capability with an optional alphanumeric overlay and memory to 512K bytes RAM and 32K PROM for distributed processing applications. Attach a graph tablet and/or one of several hard copy devices.

No matter how you look at it, it comes out on top. Raise your graphics standard. Call or write for a G-1000 brochure to Genisco Computers Corporation, 3545 Cadillac Avenue, Costa Mesa, CA 92626, (714) 556-4916.

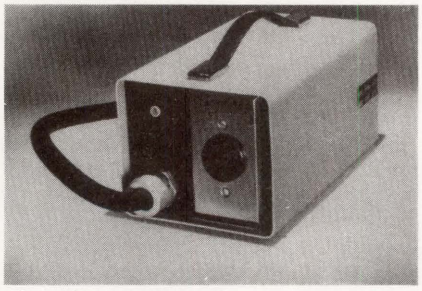
Genisco
GENISCO COMPUTERS CORPORATION

Ken Hodges

CIRCLE 141 ON INQUIRY CARD

Power line filter

IPC Powerline filter checks emi such as oscillations, radio frequency, and general random noise, in addition to blocking high and low voltage transients. Rather than attempting voltage regulation, the device specifically concentrates on attenuating high and low voltage impulses and their oscillatory decay that tend to bypass common power regulators, isolation transformers, and conventional filtering systems. It detects and removes any abnormal energy level within 10% of the instantaneous sine wave voltage. In low current applications to 30 A, it will remove any emi within 5% of the instantaneous sine wave voltage. The device removes transient energies up to 24,000 V and all rfi and microwaves within 5 kHz. It also boosts short term sags and is immune to self-oscillation. Sinusoidal output waves up to full load are maintained, while phase and neutral lines are separately filtered. **International Power Control,** 7711 N Merrimac, Chicago, IL 60648.



Circle 308 on Inquiry Card

DEVELOPMENT SYSTEMS

Development system supports 8X300 bipolar microcontroller

EZ-PRO development system provides in-circuit emulation for Signetics' bipolar 8-bit microprogrammed microcontroller. Two microprocessors, each with its own memory and control circuitry, function as master and slave. The master controls the system and provides human interface functions, while the slave executes the program the user has developed. For the 8X300 system, the slave processor is an 8X300 device. Each major functional unit of the system is attached to a central information bus. Also interfaced to the bus is an I/O bus that 2 RS-232 devices may be attached to. Typically, these are a CRT terminal and a serial printer, but the ports can also interface the system to a PROM programmer or another computer system.

The master processor is equipped with 32k bytes of RAM that store and execute software supplied with the system. In addition, 8k words (16 bits each) of high speed RAM store the 8X300 program developed by the user. Additional high speed RAM can be added to the system. Operating software and files are stored on single- or double-sided 5.25″ (13.34-cm) dual diskettes.

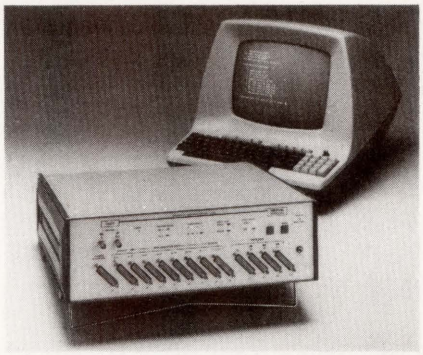
An address control board is responsible for the control of the slave processor, its memory, and its interface to the master processor. Together with the 8X300 memory and the slave processor, the control board constitutes the 8X300 in-circuit emulation feature for the system. An optional PROM programming subsystem consists of the hardware and software required to both format 8X300 object code and program various PROMs. Std system software includes a text editor, relocating macroassembler, linkage editor, debugger, and DOS. **American Automation Inc,** 14731 Franklin Ave, Tustin, CA 92680; and **Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 309 on Inquiry Card

Bit slice development system offers multiple array emulation and data break

DS270 series II Emulyzer™ bit slice development system features multiple writable control store (WCS) arrays for emulation and data break to allow break/trigger on the occurrence of up to 64-bit wide data patterns. Multi-emulation allows the user to simultaneously emulate up to 4 independent PROM arrays. Data break permits breakpoint settings based on data patterns, as distinct from address patterns. The user can specify any arbitrary breakpoint as a function of the data bits available. The data break can cause a break/trigger or can arm an address breakpoint, or an address break/trigger can arm a data break pattern.

Formatting enables the user to display the WCS word or trace word in a format that matches the user's microword format or field definitions. The user can specify any number of data fields and intermix binary, hex, octal, or quad subfields. Up to 255 chars of display headings can also be entered. Virtual in-circuit emulation offers all the features



of a true in-circuit emulator by executing some virtual emulation microcode. In addition, virtual emulation commands allow the alteration and/or display of the state of bit slice on a std CRT screen.

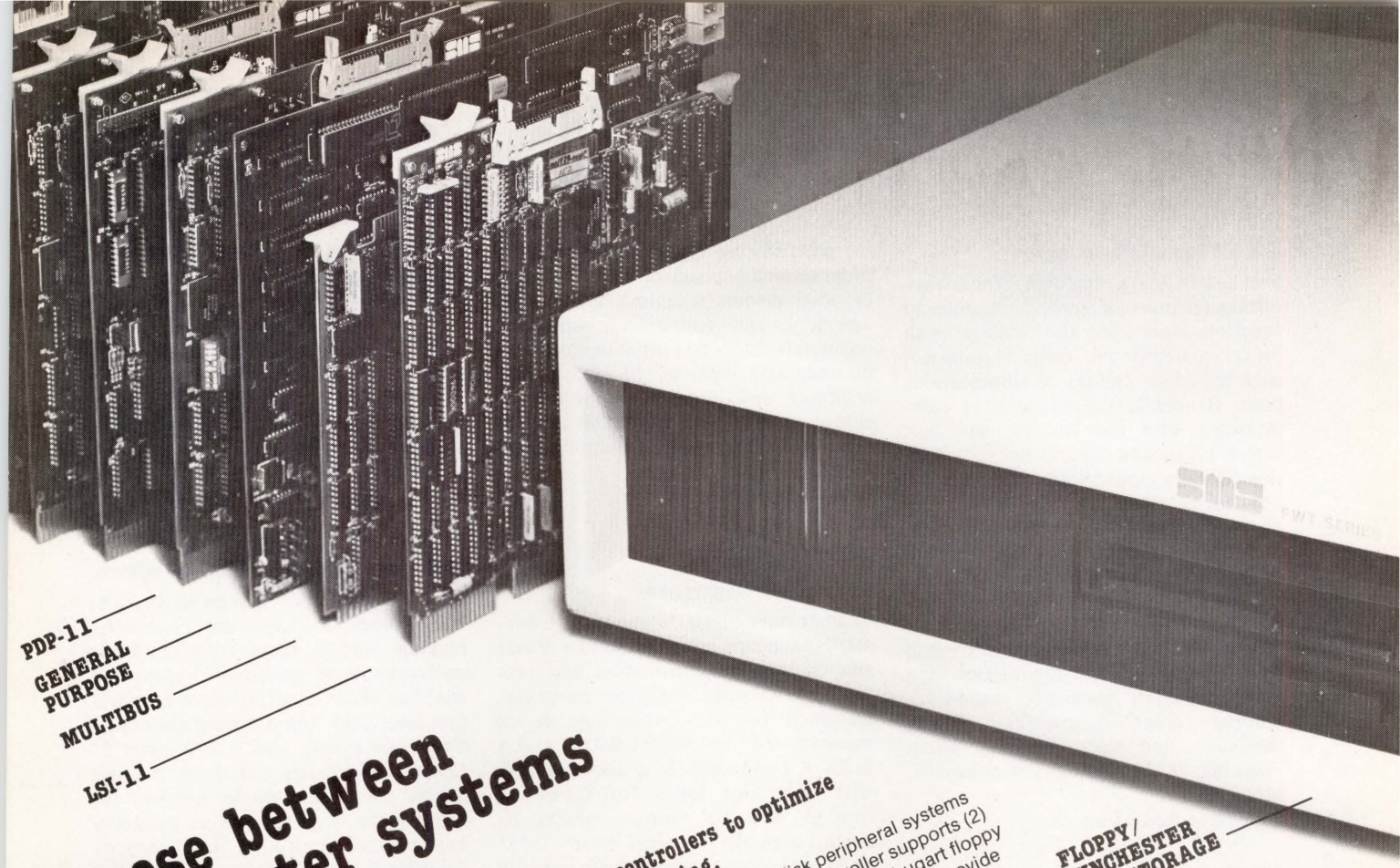
The IEEE 488 interface module provides complete instrument control in an automatic test equipment environment. The user can set up formats, set breakpoints and triggers, single-step the target under test, and read back the trace memory contents for signature analysis. Any instrument operations that can be done from the CRT keyboard can be done remotely from the IEEE 488 interface. With the 16k x 16-bit WCS memory module, any configuration from 16k x 128 bits to 64k x 32 bits can be emulated. Access time is 65 ns at the PROM sockets. Prices for the system start at $9360. **Hilevel Technology, Inc,** Park Irvine Business Ctr, 14661 Myford Rd, Tustin, CA 92680.

Circle 310 on Inquiry Card

In-circuit emulator

MICE™ emulator's resident assembler and disassembler, combined with its RS-232 interface, allows users to perform hardware debugging and minor software modification using only a CRT. The emulator features a dual-processor, 2-board design; built-in line assembler and 2-pass disassembler; built-in logic analyzer functions, including trace forward and backward up to 256 qualified cycles; realtime emulation up to the max rated speed; and RS-232-C interface to modem or terminal with band rates from 110 to 9600 baud. It measures 21.5 x 17.5 x 5.0 cm and weighs 0.85 kg. The device supports the 8085, Z80, 6502, NSC 800, and the 8048/49/50 family, and operates with any host computer or development system. Driver packages are available for the Intel MDS and the Apple II computer. **GYC, Inc,** 100 Clement St, San Francisco, CA 94118.

Circle 311 on Inquiry Card



Choose between Winchester systems or controllers

Complete systems to minimize system costs . . .

SMS FWT series disk peripherals provide up to 40M bytes of 8" Winchester disk storage and 1M bytes of floppy disk storage for DEC's* PDP-11, LSI-11, and VT103, INTEL Multibus** and other microcomputers! In only 5¼" of table top or rack space you also get the following benefits:

- Choose 8.9Mb, 17.8Mb, 26.7Mb or 35.6Mb of formatted Winchester disk storage.
- Up to 427K bytes/sec data transfer for Winchester and 63K bytes/sec for floppy.
- Supports IBM single and double density diskette formats plus DEC's RX01/RX02 formats or INTEL 202 format depending on host computer.
- Single board interfaces are compatible with PDP-11 Unibus, LSI-11 Q-Bus, INTEL Multibus or use your own adapter card for special microcomputer busses.
- Convenient Winchester backup requires only 40 seconds per 1.2M byte floppy diskette.
- Off-line and on-line system and drive tests verify correct disk and controller operation.
- Automatic error retry, ECC (Error Correction Code) and Winchester disk flaw management insure exceptional data integrity.

Or, just controllers to optimize system packaging.

All controllers used in SMS disk peripheral systems are available separately. Each controller supports (2) Shugart/Quantum Winchester and (2) Shugart floppy disk drives, utilizes patented PLL circuitry to provide maximum margins for worst case bit shifted data recovery, incorporates ECC (Error Correction Code) and includes on-board self test! Additional features are:

DEC PDP-11/LSI-11

- Single LSI-11 dual height or PDP-11 quad height interface plus formatter board.
- On board bootstrap.
- Standard RT-11, RSX-11M, UNIX,*** and SMS utility software support selective file backup and load operation.
- High performance data transfer of up to 543K bytes/sec.
- Emulates DEC RX02 floppy disk controller.
- Automatic recognition of RX01, RX02 and IBM diskette formats.

INTEL MULTIBUS

- Single Multibus compatible PC board requires only 5A (max.) @ 5 volts.
- Direct connection to (2) Shugart/Quantum and (2) Shugart floppy disk drives. Eliminates external data separator board.
- Interface and command compatible with INTEL iSBC 215A and iSBX 218 controller boards.
- Supports IBM and INTEL iSBC 202 diskette formats.

GENERAL PURPOSE

- Single board controller requires only 5A (max.) @ 5 volts.
- Interface, dimension and connector compatible with Shugart 1403D.
- Direct multi-sector disk transfer of up to 543K bytes/sec.
- Easy to use byte parallel general purpose interface.

Scientific Micro Systems
777 East Middlefield Road
Mountain View, CA 94043
(415) 964-5700 TWX: 910-379-6577
Western Regional Office (602) 978-6621
Midwest District Office (312) 966-2711
Eastern Regional Office (617) 246-2540

*Trademark of Digital Equipment Corporation
**Trademark of INTEL Corporation
***Trademark of Bell Telephone Laboratories

IBM 3270 emulator package

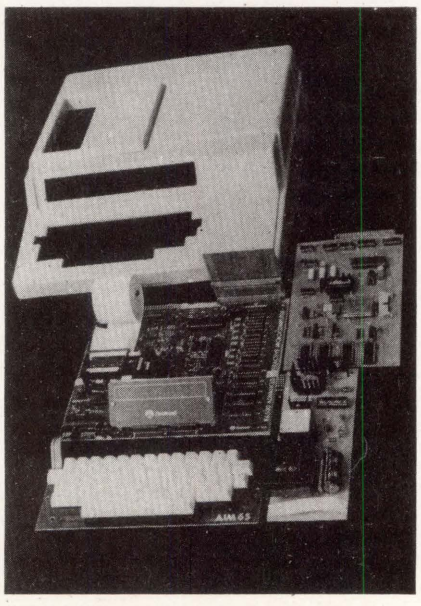
3270 EMULATOR hardware/software package permits an Apple II computer to function as an IBM 3270 terminal with binary synchronous (bisync) protocol over leased or dial-up communications lines. It enables the Apple II to communicate with IBM 360, 370, and 303X central processing units, or with any non-IBM device equipped with remote BSC3270 communication capabilities. The package includes a synchronous communications adapter plus the software on a 5.25″ (13.34-cm) floppy diskette necessary to implement the code conversion and communication protocols. It gives a 48k Apple II with disk drive and 80-col display all the capabilities of a 3270, 3271, 3276, or 3278 display station, including screen formatting, polling responses, and error checking. **Micro Plus, Inc,** 2832 LaPort Dr, Minneapolis, MN 55432.

Circle 312 on Inquiry Card

DATA CONVERSION

Precision data logger

With 16-channel ±0.012% accuracy (12 bits), DL-1001 data logger is offered in kit form for scientific and industrial users. Based on Rockwell's AIM-65 computer and expanded by 16 channels, the device includes a calendar/clock, a 20-char printer, and an LED display. Voltage input ranges can be set ±10 V, ±5 V, or 0 to 10 V. Included in the package are BASIC programs to set the clock and to read and print values at each of the 16 channels. Stored in EPROM memory, these programs can be supplemented by the user. Sixteen digital outputs can be programmed to control remote alarms or other devices accepting TTL signals. The device can communicate with other computers via RS-232 output or store data on magnetic cassette. Molded plastic enclosure and power supplies are included in the kit. **Columbus Instruments,** PO Box 44049, Columbus, OH 43204.



Circle 313 on Inquiry Card

Miniature synchro to resolver transformer

Transformer 52975 converts 11.8-V, 400-Hz synchro information to 1-V rms sine and cosine information and provides 5 arc-min nominal accuracy. Designed for PCB mounting, device measures 0.5″ x 0.875″ x 0.438″ (1.3 x 2.223 x 1.113 cm). It is also available with side exit leads for mounting through a board cutout, making its height over the terminal board 0.35″ (0.89 cm). Unit operates over the full military temp range and is priced at $27 in quantities of 1000. **Magnetico, Inc,** 182 Morris Ave, Holtsville, NY 11742.

Circle 314 on Inquiry Card

COMPUTERS

32-bit minicomputer offers 400-ns memory access time

Designed specifically for the sophisticated system integrator, model 3210/A 32-bit minicomputer has 400-ns memory access time and uses 64k RAM chips. Its architecture and I/O interfacing are fully compatible with the company's line of 32-bit minicomputers. Built-in reliability features include error checking and correcting memory, hardware error logger, power fail/auto restart, and illegal instruction trap.

The basic processor and all system components are available separately. Available components include 30″ or 56″ (76- or 142-cm) high cabinets, dc power system, air cooling assembly for the CPU chassis, floating point processor, and add-on memory up to a max directly addressable 4M-byte capacity.

In addition, a wide range of 32-bit software is available for use with the system, including the company's multitasking OS/32 operating system and 32-bit languages such as ANSI 77, FORTRAN VII, Pascal, ANSI std COBOL, BASIC, CAL MACRO, RPG II, and CORAL 66. The system is upwardly compatible with models 3210, 3220, 3230, and 3240, and other members of the company's line of 32-bit minicomputers. A basic unit, consisting of a fully functional 32-bit processor and 512k bytes of memory mounted in a chassis, together with a control panel and a 2-line communications multiplexer, is priced at $19,100 (OEM, quantity 100). Min quantity that can be ordered is 10 units. **Perkin-Elmer Corp, Computer Operations,** 2 Crescent Pl, Oceanport, NJ 07757.

Circle 315 on Inquiry Card

Multi-user business computer system

SB700-B Easy-Grow™ system serves up to 200 independent users simultaneously, making one or more complete CP/M microcomputers available to each, and enabling all of them to share a central processor pool and a central data base. The basic system uses a 20M-byte, 8″ (20-cm) Winchester disk drive; a single cabinet can house up to 6 drives for 120M bytes of disk storage. Including multiple disk controllers, total capacity for the system is 600M bytes. With 4 Z80 based processor modules, a 20M-byte Winchester disk drive, and a 1M-byte diskette drive, a minimum system is priced at $15,115. **Symcro Systems, Inc,** 7300 Crescent Blvd, Pennsauken, NJ 08110.

Circle 316 on Inquiry Card

General purpose minicomputer offered for single-or multi-user environments

68k MiniFrame™ general purpose 16-bit computer can be configured for use as a low cost single-user system, or as a high powered multi-user system with LRU demand paged virtual memory. The system uses 3 processors: a 68000 main processor, a 68000 virtual memory and number crunching co-processor, and a 6809 I/O processor. Designed for full 12-MHz operation with no wait states, it can address up to 4G bytes and handles LRU demand paged virtual memory in 16M-byte increments. Relocation and limit registers are maintained for each user to facilitate multi-user and multitasking operations.

The system operates with floppies and/or hard disks, and includes 6 RS-232 interfaces, 4 parallel interfaces, and a high speed DMA port to facilitate multi-user hookup. It runs the UNIX (version 7) operating system and supports CBASIC, Forth, LISP, APL, and Microsoft languages including BASIC, FORTRAN, COBOL, and Pascal. The computer is housed in a 19″ x 7″ x 24″ (48- x 18- x 61-cm) rackmountable metal enclosure, that also contains power supplies, fan,

circuit breaker, backplane connectors, power and reset key switches, and a power-on/fault front panel LED indicator.

Price for a single-user, desktop system with 256k RAM; 2M-byte, 8″ (20-cm) floppy disk storage; 6 RS-232 ports; 4 parallel ports; 1 high speed DMA port; and the UNIX operating system starts at under $12,000. The complete UNIX package includes FORTRAN 77, C, BASIC, text processor, and file processing utilities. A typ multi-user system handles 6 or more users and contains 512k bytes of RAM in 16M-byte virtual space, 40M bytes of Winchester disk storage, and UNIX. Future peripherals include a bus arbiter for networking systems, bus adapters for MULTIBUS, VERSABUS, S-100, and IEEE 488, and high speed cache memory. **MicroDaSys, Inc,** PO Box 36215, Los Angeles, CA 90036.

Circle 317 on Inquiry Card

INTERFACE

Minicartridge drive controller

Designed for use with the TM110 minicartridge drive, the TM210 controller consists of a PCB that mounts under the drive. The controller accepts serial data or control characters, and responds with serial status or data characters. By optional link selection, data input can be accommodated at RS-232, current loop, or TTL levels. RS-232 signals "request to send" and "clear to send" are supported to facilitate operation with a modem or microprocessor. Baud rate and character format can be selected by onboard switches. The TM210/TM110 combination has a 120k-byte formatted capacity. Data are fully buffered within the controller, and tape data format complies with ECMA or ANSI standards. The controller is priced at $197 in OEM quantities. **Burroughs OEM Corp,** Burroughs Pl, Rm 4E19, Detroit, MI 48232.

Circle 318 on Inquiry Card

Intelligent RS-232-C interface

An RS-232-C based I/O controller SCDR/BDL 3026 interfaces a TC-3000 series cartridge recorder to terminals or modems in accordance with EIA std RS-232-C type D and E, CCITT std V.24, or Teletype compatible current loop. Data are recorded in ANSI std X3.56B-1976 format. The unit responds to ASCII control character sequence from the local terminal or modem (over 30 user commands are available). It provides a 2048-byte buffer; 28 baud rates from 75 to 38,400 baud; 4000 bytes of program memory that can be customer programmed for special requirements; over 4M bytes/cartridge data storage; and a copy feature that permits cartridge duplication on a dual drive system. Two interface connectors allow the recorder to connect to a local I/O terminal and a modem for remote operation.

The unit operates in all RS-232-C environments, including transparency for binary operations. Its power-safe circuits remember the last operation of the peripheral for 24 h. One controller supports three additional daisy chained drives. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.

Circle 319 on Inquiry Card

USART/baud rate generator

Designed to interface microprocessors or microcomputers to data communication links or processor peripherals, COM 2651 combines a USART and a baud rate generator on a single MOS/LSI chip. It accommodates all std asynchronous formats and all std char oriented synchronous formats. In the asynchronous mode, features include programmable char formats and clock rates, onchip line break detection and generation, automatic serial echo, and 2 loopback modes. In the synchronous mode, char formats are programmable. In addition, the device can operate in both transparent and nontransparent modes with automatic SYNC insertion and stripping. The unit includes all the required microprocessor control lines plus the RS-232-C modem control signals. It is pin for pin compatible with the Signetics 2651 and available in 28-pin plastic and ceramic packages. **Standard Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11788.

Circle 320 on Inquiry Card

Ethernet controllers plug into DEC computer products

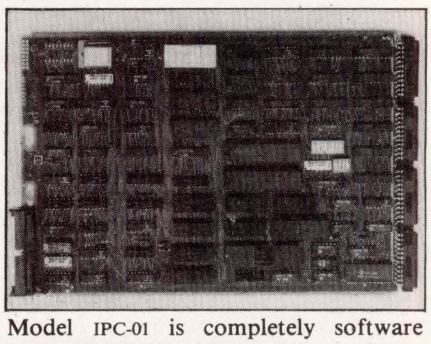
Compatible with DEC's LSI-11 Q-bus and UNIBUS, respectively, the 3C200 and 3C300 controllers provide Ethernet controller functions at 10M bps. Either controller, teamed with the company's 3C100 Ethernet transceiver, provides complete support for layers one (hysical) and two (data link) of the ISO Open System Interconnection Reference Model. Also available are enhancements to UNET, the company's UNIX networking software that provides full support for the controllers.

Both controllers provide parallel to serial and serial to parallel conversions, buffering of data during transmission and reception, framing of message packets, data encoding and decoding, plus collision and error detection. The UNIBUS controller 3C300 has additional hardware assistance for address recognition, including options to accept broadcast, multicast, or all packets. Both controllers have 32k bytes of dual-ported RAM that permit the controller and the host CPU to access the controller memory space. To support back to back handling of packets at the 10M-bps transfer rate, the controller uses a portion of the 32k memory for send and receive buffers. Allocated in 2k-byte segments, each buffer has enough space to store the max allowable packet size of 12,144 bits.

A DEC computer running the UNIX operating system, equipped with the enhanced UNET, controller, and transceiver, can function as a complete Ethernet local computer network station. Such a system provides communication through all seven ISO model levels, with UNET providing file transfer, virtual terminal, electronic mail transfer, and process to process communication capabilities via the five upper layers. **3COM Corp,** 1390 Shorebird Way, Mountain View, CA 94043.

Circle 321 on Inquiry Card

Plug compatible controller

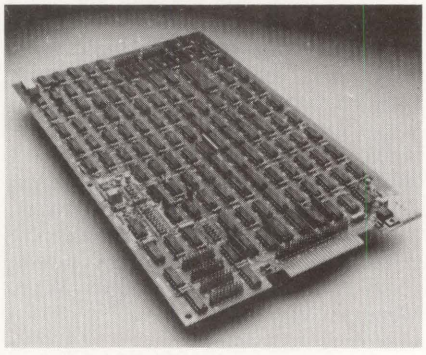


Model IPC-01 is completely software compatible with printer drive routines within the IBM RPS and EDX operating systems. Oncard 2901 bit-slice microprocessors convert EBCDIC from the Series/1 bus to printer-control signals. Measuring 7.25″ x 10.75″ (18.42 x 27.31 cm), the device is installed in one slot in the Series/1 model 4953 or 4959 expansion chassis. Extensive use of low power Schottky devices reduces power required from the system to 5 Vdc at 4 A. **BDS Corp,** 115 Independence Dr, Menlo Park, CA 94025.

Circle 322 on Inquiry Card

Intelligent disk controller

Model 20A controls up to 2 Seagate interface compatible 5.25″ (13.34-cm) disk drives or their functional equivalents. The single 5.75″ x 11.5″ (14.6- x 29.2-cm) PCB is designed for physical compatibility with the Seagate drives, and is plug compatible at the host interface level to DTC 500 series and OMTI 10 series controllers. Disk I/O operations are done via buffering to support varied host transfer rates. Powerful 32-bit ECC and transparent soft/hard drive error logging enhance the unit's reliability. The controller's command set includes a multiple sector transfer capability for reading or writing up to 256 sectors in one operation, a 512-byte sector option, fast seek capability for the ST506, and sector interleaving to optimize host throughput. **OMT, Inc,** 2165 S Bascom Ave, Campbell, CA 95008.



Circle 323 on Inquiry Card

MICROPROCESSORS/ MICROCOMPUTERS

VT100 personal computing option

Microprocessor option VT18X enables the company's VT100 video display terminals to run CP/M personal computing software; terminals can operate as an I/O device to a computer system or run standalone personal computing applications under CP/M. The $2400 single-unit price includes a Z80 based microprocessor module with 65,536 chars of internal memory for mounting inside the VT100 cabinet; a dual mini-floppy, 5.25″ (13.34-cm) disk drive with 160,000 chars of data and program storage; connecting cables; user guide and documentation; and a diagnostic disk to check system performance. A second dual mini-floppy disk drive can be added for $1275. CP/M software license and documentation are priced at $250. **Digital Equipment Corp,** 146 Main St, Maynard, MA 01754.

Circle 324 on Inquiry Card

Multiprocessor, multi-user microcompter system

ZEUS II supports from 1 to 64 users, each with a dedicated single-board computer module that includes a Z80A CPU, 64k RAM, and dual serial I/O. A 2-board module serves as a master, supervising all user requests for shared storage and peripherals. The master processor module includes an onboard floppy controller, peripheral interfaces, DMA, and realtime clock with battery backup. The CP/M compatible multi-user system executive (MUSE) op sys provides a true multi-user environment. The system operates from a UPS; in the event of a power outage, it will operate up to 20 min. **OSM Computer Corp,** 2364 Walsh Ave, Santa Clara, CA 95051.

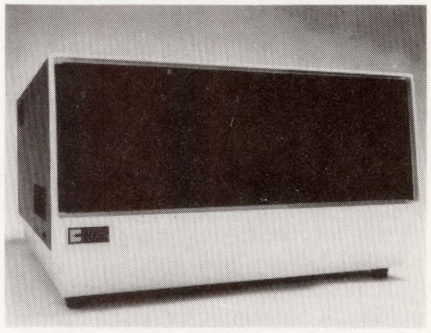
Circle 325 on Inquiry Card

Packaged computer system

Built around DEC's LSI-11/23 central processor, MH-11 offers a Winchester disk and a choice of system software. A basic system, priced at $16,000, includes LSI-11/23 central processor with 128k bytes of memory, 4-port serial interface, 20.8M-byte Winchester disk, dual double-density floppy disk drives, and 30″ (76-cm) high office style enclosure. Operating system software (either DEC's RT-11V4 or Whitesmiths Ltd's Idris, a UNIX like system that includes C and Pascal languages) is included in the base price. A cartridge tape backup unit is optional. **Charles River Data Systems, Inc,** 4 Tech circle, Natick, MA 01760.

Circle 326 on Inquiry Card

MULTIBUS microcomputers



CTW series MULTIBUS based computers are available with Z80 (CTW-100), Z8000 (CTW-200), and 68000 (CTW-300) microprocessors. Each computer accommodates a variety of storage modules, including a 10M-byte 5.25″ (13.34-cm) Winchester, a 380k dual mini-floppy disk drive, and a 17M-byte tape cassette. The series is also available with 64k to 1M-byte RAM storage. Software available for the series parallels that available for the firm's CTS series of MULTIBUS microcomputers. Model CTW-300 can process a range of FORTRAN and Pascal software, including the full ANSI std FORTRAN 77 (not a subset). These languages operate under the UNIX like operating system, MERLIN. The CTW-200 microcomputer employs the XENIX operating system from Microsoft. CTW-100 runs an extended BASIC, C, and other languages. **Codata Systems Corp,** 285 N Wolfe Rd, Sunnyvale, CA 94086.

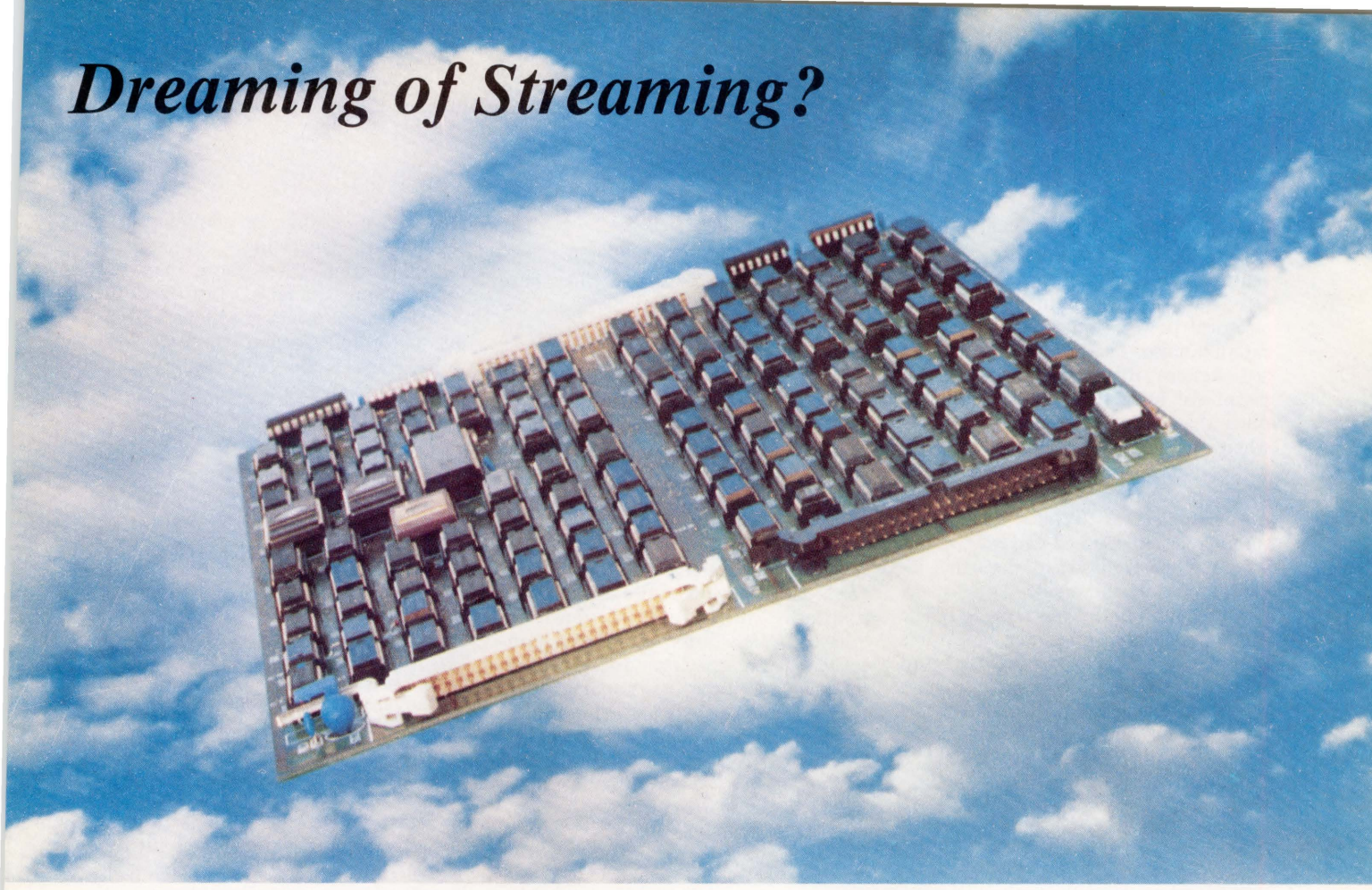
Circle 327 on Inquiry Card

6809 based single-board microcomputer

FLEXI PLUS™ features up to 56k bytes of onboard RAM, ROM, and EPROM in any combination, extensive serial and parallel I/O capability, a 20-mA current loop TTY port, and a universal cassette interface. Options include a floppy disk controller that supports up to four 8″ (20-cm) drives or three 5.25″ (13.34-cm) drives and provides IBM compatible formats; an RS-232-C communications port that is fully buffered with programmable data formats and baud rates from 50 to 19,500; and an IEEE 488 Bus controller. **The Computerist, Inc,** 34 Chelmsford St, Chelmsford, MA 01824.

Circle 328 on Inquiry Card

Dreaming of Streaming?



Introducing the GYPSY™, the first complete streaming solution

Convenient, low-cost, dependable backup solution for your Winchester disk? Probably one of the most complex questions you face. The answer is the GYPSY, the fastest, most versatile disk/tape controller on the market.

VERSATILITY. The GYPSY offers a unique set of back-up, restore, and access features including:

- Offline backup and restore functions which eliminate the need to tie up the host processor or memory
- "Transparent" tape commands, allowing continual host access of the disk during backup and restore procedures
- Backup and restore at a streaming tape rate of 90K bytes/second
- File oriented backup and tape file search capability, allowing selective backup and restore

PERFORMANCE. With a burst transfer rate of two megabytes/second and average data throughput of 450K bytes/second, the GYPSY is the highest performance disk/tape controller available. A single command allows the user to backup 20M bytes of data in less than four minutes.

ADAPTABILITY. The GYPSY offers innovative solutions to disk, tape, and host interfacing. Disk interfaces include Century Data Systems and Priam, as well as the industry standard SMD. The GYPSY supports all major 1/4" tape drives, Archive, DEI, Cipher, and TEAC. Host interfaces have been extremely simlified; the GYPSY can communicate with any host via a simple parallel interface, or by utilizing one of ADES' many economical host interface adapter boards.

SYSTEM SOLUTION. Looking for a system solution? ADES offers complete disk/tape memory subsystems, integrating the GYPSY, streaming tape, and 8" or 14" Winchester disk drives ranging from 10 to 160 megabytes. Our SYSTEM 8 and SYSTEM 14 provide the user with leading edge hard disk technology and all the performance and versatility of the GYPSY.

Make the dream a reality . . .

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ADES

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CIRCLE 144 ON INQUIRY CARD

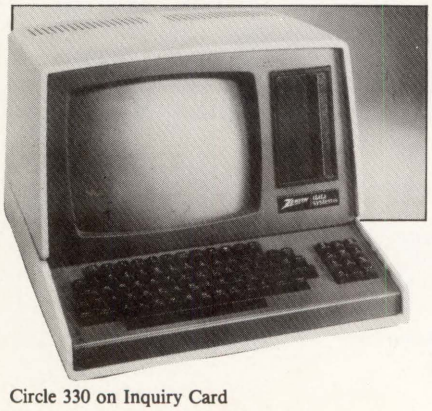
Radiation resistant microcomputer

Mk-r16 is based on a CMOS/SOS 16-bit central processor chip that features the SOS characteristics of high speed, low electrical power, and high tolerance to external noise. The 6-chip set uses other SOS devices for control storage and peripheral logic to form a microcomputer that consumes less than 750 mW when operating at 5.5 MHz. The unit will operate in a radiation environment of 10^{10} rads/s transient dose, with a total dose immunity of 10^4 rads. Its architecture is register oriented and implements a comprehensive instruction set that includes multiply and divide. Avg instruction execution time is less than 2 μs. The microprocessor interface supports priority interrupt levels and multiprocessor protocol, and provides direct addressing of 64k bytes of external memory. Full military temp range parts, tested to MIL-STD-883B, are available. **Mikros Systems Corp,** 3828 Quakerbridge Rd, Mercerville, NJ 08619.

Circle 329 on Inquiry Card

Z80 based microcomputer

Z-90 provides Z-89 microcomputer features, plus a double-density disk controller card that increases storage available on 5.25″ (13.34-cm) diskettes. It also offers 64k bytes of RAM, compared to the Z89's 48k bytes, and a third RS-232 port on the back panel. The microcomputer uses the 8-bit Z80 microprocessor and includes computer, video display, disk drive, and keyboard in a 1-piece housing. The video screen is a green, nonglare 80-char x 24-line display. A 25th line is available to show system status. Built-in terminal emulators make the microcomputer capable of replacing any ANSI or DEC VT-52 terminal. Both operating system software and Supercalc™ planning software are provided with the system. **Zenith Data Systems,** 1000 Milwaukee Ave, Glenview, IL 60025.



Circle 330 on Inquiry Card

Industrial grade 16-bit microcomputer modules

Conformal coated TM990 modules have an op temp range of 0 to 70 °C and are constructed to withstand the effects of hostile elements. All ICs are soldered in place prior to being sealed with the conformal coating, with the exception of socketed EPROMs mounted into sockets that have gold plated machined pins, as well as clamps to protect against vibration. Sockets are screened during the conformal coating process, and then lubricated with corrosive-resistant fluid. All jumper selections are wide wrapped for security. Five modules are currently available in industrial versions: TM990/C101MA microcomputer controller, TM990/C201 memory expansion module, TM990/C307 RS-232 communication expander, TM990/C308 industrial communication module, and TM990/C310 I/O expansion module. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220.

Circle 331 on Inquiry Card

CMOS microprocessors

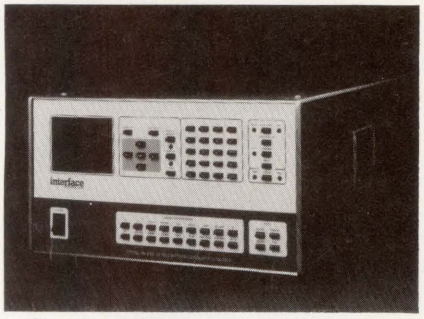
Added to the 1800 CMOS microprocessor line and similar in architecture to the 1802A, the CDP1805C microprocessor features 64 bytes of RAM, a 4-MHz clock rate, 22 additional instructions (113 total), an 8-bit presettable down counter with a divide-by-32 prescaler, and a Schmitt-trigger crystal or RC controlled oscillator. Also added to the line, CDP1806C is identical to the 1805C except that it does not include RAM. Both devices provide for memory expansion of up to 64k of combined RAM and ROM. The units have an operating voltage range of 4 to 6.5 V and are supplied in 40-lead plastic DIPs. **RCA/Solid State Div,** Rte 202, Somerville, NJ 08876.

Circle 332 on Inquiry Card

TEST & MEASUREMENT

Digital signal generator and test subsystem employs dual-microprocessor architecture

Model RS-4000 20-MHz pattern generator/analyzer uses a dual-microprocessor architecture to provide the multiple functions of a digital word generator, a comparator, and a logic recorder in a single unit. Designed specifically to provide word generator and timing simulator digital output capabilities, the device also provides digital input, compare, and record capabilities for use in complex digital testing. In addition, it is capable of generating, testing, and recording from 16 to more than 512 simultaneous channels. Test rates to 20 MHz can be achieved with parallel input and output pattern depths to 2048 words. Serial modes of input and output operation are also available.



Standard features include IEEE 488, serial ASCII, and 16-bit parallel interfaces for remote control, and a video output jack that can be used to drive a large monitor or video printer. The unit operates as either a benchtop instrument or a subsystem within an automatic test system. It is completely programmable by any operator, regardless of skill level or previous programming experience.

Users are prompted through and assisted in the programming of various modes, data tables, and control parameters by a menu driven user interface, using a keyboard and CRT display. A std LSI microprocessor aids in prompting and display formatting, and handles the programming protocol for the integral bit slice microprocessor. Programs can be pre-stored on floppy disks for call up by file name, generated in any of several high level prompted operating modes, or developed at the macro language level. In each case, users have access to all stimulus memories, expected value memories, mask memories, and record memories contained in the instrument. **Interface Technology, Inc,** 150 E Arrow Hwy, San Dimas, CA 91773.

Circle 333 on Inquiry Card

Logic analyzer traces data on up to 64 channels

Series KLA logic analyzers are available in 32-, 48-, and 64-channel versions (models KLA-32, KLA-48, and KLA-64, respectively). The instruments offer 2048 words of memory (4096 optionally), asynchronous clock speeds to 100 MHz, and extensive clocking, triggering, and display formatting facilities. A floppy disk drive that stores front panel setups

(continued on page 254)

Color Retro-Graphics.™ Our Terminal Enhancements Cross Yet Another Frontier.

For over three years now, Retro-Graphics™ terminal enhancements have transformed some of today's most popular alphanumerics terminals into impressively-featured graphics terminals. Now Digital Engineering, the pioneer in graphics upgrades and creator of Retro-Graphics, has taken its successful idea and made it a colorful one as well. An idea that makes sense to the business and scientific communities alike, by making sales and financial charts, as well as complicated engineering drawings, easy to produce—and startlingly easy to afford.

Introducing the DM800 Retro-Graphics Enhancement for the Datamedia™ Colorscan™ Terminal.

Here is a formidable tool. Eight colors, chosen from a 64-color palette, can be selected and displayed at once. And thanks to a high-quality 640 x 480 resolution, graphics images are displayed crisply and vividly. There is, of course, Tektronix® 4027 graphics terminal emulation, fully software compatible with ISSCO's® DISSPLA® and TELLAGRAF® and Tektronix PLOT 10® The enhanced Colorscan terminal does vector and arc drawing, point plotting, text generation, area fill and shading patterns, thus allowing complex graphics functions to execute with a single instruction. Graphics input options include a light pen for selecting and altering screen objects as well as a bit pad for fast entry of X-Y coordinates. And for color hard copy, the Retro-Graphics DM800 interfaces to a variety of printers, plotters and cameras.

Other Retro-Graphics terminal enhancements are available for Lear Siegler's ADM-3A and 5 Dumb Terminal® displays, TI's 940 Electronic Video Terminal and DEC's™ VT100™ and VT132™ Terminals.

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CIRCLE 145 ON INQUIRY CARD

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and known good response reference information enhances flexibility. Operating software is also stored on disk, so that new, updated, or application-specific features can be added.

In order to track down faults in multiplexed systems, up to 4 clocks and 12 clock qualifiers can be recorded simultaneously. Glitches as short as 5 ns are latched and stored in a memory separate from data so that the instrument can be triggered on glitches. Glitches are displayed as half-height lines on the 9″ (23-cm) screen.

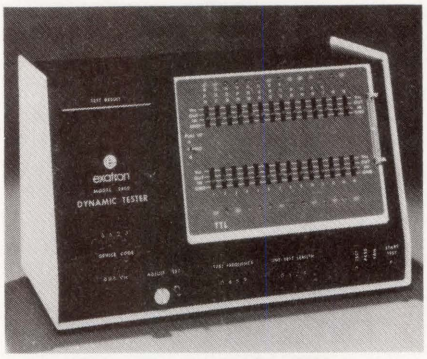
Sequential triggering offers up to 14 levels, each with pass counters, digital trigger filtering, variable trigger delays, conditional jump instructions to other trigger levels (if-then-else conditions), and ORing of trigger words. The analyzer offers transitional recording (gathering information on transitions in incoming data, not on a free-running clock) and data qualified recording. Data can be displayed in timing diagram, hexadecimal, decimal, octal, binary, ASCII, or EBCDIC formats, with optional disassemblers to display microprocessor programs in the device's mnemonics.

Options include personality probes for 8- and 16-bit microprocessors and a counter/timer board that can make timing measurement during data qualified and transitional recording modes. Prices start at $15,000 for the 32-channel version. **Kontron Electronics, Inc,** 630 Price Ave, Redwood City, CA 94063.

Circle 334 on Inquiry Card

High speed LSI test system

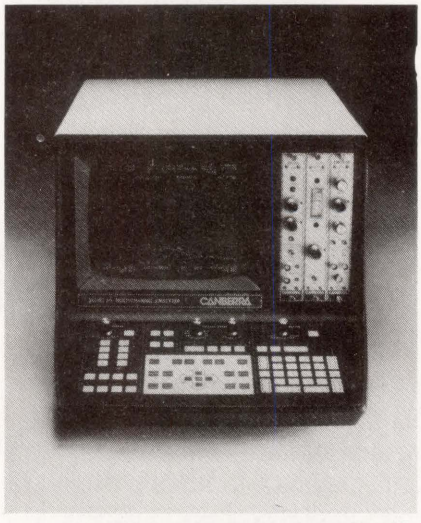
Model 2800 dynamic tester uses the signature analysis test method. By generating up to 20M test patterns/s, the unit can dynamically test a 28-pin LSI device in a fraction of a second. Worst-case propagation delay can be measured at the device's rated operating speed. Features include limited parametric analysis, dynamic refresh time testing, CMOS and TTL threshold levels, and selectable pullup resistors. Knowledge of computer programming is not required



to configure the system for different test devices. These devices are programmed into the tester by setting 4-position switches (one for each pin of the device) and a 4-digit thumbwheel code. Depending upon the device to be tested, each switch is set to be input, output, ground, or V_{CC} (device power). The thumbwheel code is a checksum "signature" produced by a known "good" device and is used as a std by the tester. **Exatron Corp,** 181 Commercial St, Sunnyvale, CA 94086.

Circle 335 on Inquiry Card

Multichannel analyzer

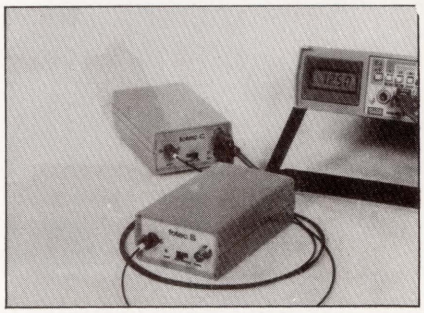


Series 85 analyzer accommodates 3 self-contained 100-MHz ADCs and features a nuclear instrumentation module (NIM) front end, enhanced analysis firmware, improved CRT quality, greater expandability, and built-in self-testing. In addition, the unit provides multitasking operation, complete peak analysis, learn/execute sequence programming, options for isotopic analysis with user definable libraries, and online Jupiter computer operation. **Canberra Industries, Inc,** 45 Gracey Ave, Meriden, CT 06450.

Circle 336 on Inquiry Card

Fiber optic test instrument

Fotec S fiber optic signal source functions as a fiber optic pulse generator, providing the optical signals required to test fiber optic cables, receivers, repeaters, or complete systems. When combined with an instrument capable of measuring fiber optic system power, it provides complete test capability for any fiber optic communication system, either in the lab or in the field. The unit offers a fast rise time pulse train output optical signal with variable frequency and amplitude. Optical output pulse frequency can be adjusted by a front panel control in the range of 5 to 100 kHz (square wave), or controlled by an external pulse generator for varying output



optical pulse width and frequency. A single BNC connector functions as both a pulse output for verifying output frequency in the internal pulse mode, and an input for using an external pulse generator to modulate the optical source. Standard source wavelengths are 700, 820, 880, and 940 nM. Peak output power depends on the fiber and connector chosen. **Fotec, Inc,** PO Box 246, Boston, MA 02129.

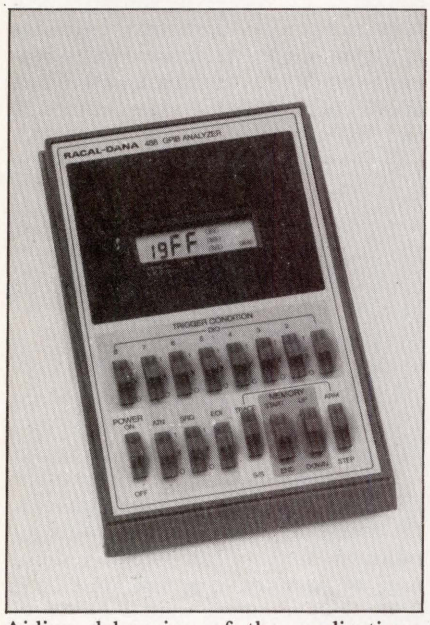
Circle 337 on Inquiry Card

Combination breakout box/ bit error rate tester

Datatest runs at speeds up to 64k bps and can be used to run loopback and end to end tests on both synchronous and asynchronous networks. In addition, the complete RS-232-C breakout box allows monitoring and cross patching of all 25 conductors on the interface. The unit transmits 5 patterns, including pseudorandom 511 and 2047. Asynchronous speeds of 75, 150, 300, 600, 1200, and 2400, or 300, 600, 1200, 2400, 4800, and 9600 baud can be selected. Housed in a metal case, the device can run on internal rechargeable batteries or ac. A VF monitor is optional. **Navtel,** 8481 Keele St, Unit 12A, Concord, Ontario L4K 1B1, Canada.

Circle 338 on Inquiry Card

IEEE 488 bus analyzer



Aiding debugging of the applications software in an IEEE STD 488 based system, model 488 features battery operation and 40-word memory, and operates in 3 modes. The passive mode monitors bus activity and displays the status of each active line on a LCD. DIO lines are displayed in hex code while handshake and housekeeping lines are individually annunciated. A single-step mode allows the analyzer to control the bus handshake and single-step activity, byte by byte. Trace mode activates the 40-word memory and allows normal bus activity. After capturing 40 words, the user can examine the previous bus activity on a handshake by handshake basis. Battery operation allows data to be retained and analyzed offline. **Racal-Dana Instruments Inc,** 18912 Von Karman Ave, Irvine, CA 92713. Circle 339 on Inquiry Card

SOFTWARE

Software package

Personal business system or engineering/development system users can communicate with a single host computer for file storage, information access, and peripheral sharing via the poly-XFR software package. Moreover, a mix of system types can use the same information and communicate with each other. The system supports DEC PDP-11S running RSX-11M or RSTS/E as a host; local systems include DEC/RT-11, Intel and Motorola development systems, CP/M based systems including the DEC VT18X, Xerox 820, and TRS-80. It supports both binary and ASCII file transfers, allowing software to be loaded from a central support site. Error detection, retransmission, and timeout protection provide integrity. System will operate on asynchronous lines, remotely via modem or in a direct wire environment, at speeds up to 9600 bps. **Polygon Assoc, Inc,** 9 American Industrial Dr, Maryland Heights, MO 63043.
Circle 340 on Inquiry Card

Multi-tasking kernel

Multi-Tasking Kernel integrates multiple realtime software tasks in a microprocessor based product. The ROMable package oversees both selection and execution of each task and provides source code for a basic multitasking organization (tasks self-schedule in a round-robin ordering). Users are guided through a series of enhancements for implementing sophisticated interrupt initiated, preemptive priority, dynamic task scheduling. Also included are descriptions of dedicated and shared resource scheduling, time-slice scheduling, intertask communication schemes, and additional tasks. Completely documented and fully tested, the package is available in source assembly form for the 8085, Z80, 6502, 6800 and 6809. **U S Software,** 5470 NW Innisbrook Pl, Portland, OR 97229.
Circle 341 on Inquiry Card

BASIC interpreters for MCPU-800 STD BUS microcomputer

2k BASIC interpreter language is a subset of std BASIC. Common arithmetic functions operate on integer numbers within the range of -32767 to 32767. There are 26 variables (A-Z) and a single array with its dimension set to the unused memory area. In addition to common editing commands, FOR/NEXT loops, subroutines, PRINT, INPUT, and IF statements are supported. PEEK and POKE allow memory location reading and modification. IN and OUT provide control of I/O ports, while CALL gives access to machine language routines. 8k BASIC is a full function BASIC interpreter. Floating point math accommodates numbers from $\pm 2.7 \times 10^{-20}$ to $\pm 5.7 \times 10^{18}$ and supports transcendental functions. Up to 286 numeric variables and 286 string variables can be defined. Matrices, user definable functions, DATA statements, and string manipulation are supported. PEEK, POKE, INP, OUT, and CALL are included as well. Both interpreters are available in development or application versions. **Miller Technology,** 647 N Santa Cruz Ave, Los Gatos, CA 95030.
Circle 342 on Inquiry Card

Realtime executive software

PROM based VRTX/8002 supports the Z8002 microprocessor with a full range of multitasking and control functions. By incorporating the system functions common to all realtime applications into one package, the need for users to write complex system software is eliminated. The software provides the common core of mechanisms necessary to coordinate multiple tasks within the framework of a responsive, event-driven system. Interrupt-driven task scheduling, intertask communication and synchronization, dynamic memory allocation, clock support, character I/O, and quick response are provided. **Hunter & Ready, Inc,** 445 Sherman Ave, Palo Alto, CA 94306.
Circle 343 on Inquiry Card

8051 microprocessor support software

With cross reference, software librarian, object format conversion, and downline loading programs, CY8051 relocatable macro assembler is offered for the Intel 8051 (including 8031 and 8751) family of microprocessors. The software is available for all DEC PDP-11 and VAX computers. Supported operating systems include RSX-11M, RT-11, IAS, RSTS, and VMS. Assembler and symbolic debugger are also available for the 8051. **Boston Systems Office,** 469 Moody St, Waltham, MA 02154.
Circle 344 on Inquiry Card

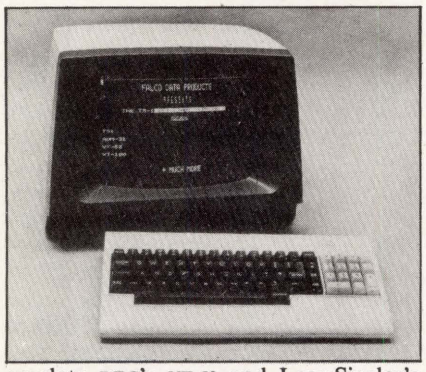
Solid font impact band printer

Model 8155 produces 450 lines/min using std 64-char band, or 375 lines/min using an optional 96-char band. The 132-col printer can be changed from uppercase print to a combination of upper- and lowercase with no software adjustments. Compatible with all of the company's series IV processors, it features a digital display panel that continuously monitors the printer's status; any malfunction is automatically displayed, enabling the operator to identify and correct many offline conditions. An operator self-test feature ensures timely problem diagnosis, minimizing service calls and maximizing uptime. Print format is 10 chars/in (4/cm) with vertical line spacing selectable to either 6 or 8 lines/in (2.4 or 3/cm). Forms handling is provided by a 12-channel vertical forms unit. **Four-Phase Systems,** 10700 N DeAnza Blvd, Cupertino, CA 95014.

Circle 345 on Inquiry Card

Smart terminal emphasizes software driven features

Providing a wide range of operation flexibility and reducing the possiblity of obsolescence by emphasizing software driven features, the Z80 based TS-1™ smart terminal can be upgraded to perform new functions by exchanging ROMs or adding PCBs. In addition to operating in its native code, it can



emulate DEC's VT-52 and Lear-Siegler's ADM-31 terminals; as an option, it can emulate DEC's VT-100. The terminal features a detached front connected keyboard, 28 user programmable function keys that can be chained together and nested, a std green P31 phosphor screen (white P4E or amber PC134 screen is optional), inductive key switches, a 256-char data buffer, 8k of ROM (expandable to 16k), 1k of data RAM (expandable to 17k), and 2k of display RAM.

Two interchangeable, bidirectional dual I/O ports with independent interface characteristics allow simultaneous connections with computers, printers, or modems. An extension port feature echoes data from the master port through the slave port. The terminal also provides a std RS-232 interface (RS-422 and current loop are optional), 16 baud rates from 50 to 19,200, 115/230-V ±20% operation at 50/60 Hz, and 50-W max power consumption. Op temp is 5 to 45 °C, with relative humidity of 10% to 90% noncondensing. External wideband monitors can be added as an option. Synch frequency is 19.2 kHz.

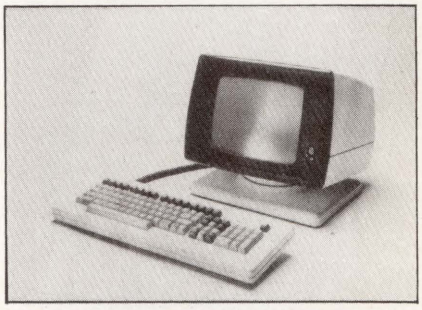
In the device's soft setup mode, software switches select word length, stop bits, parity, baud rate, word structure, transmission mode, duplex, refresh rate, master I/O port, extension port, X-ON/X-OFF and/or DTR buffer control, protocol, roll, scroll, and smooth scroll. They also add line feed to carriage return, select hour clock (12 or 24) and cursor control for model compatibility, display status line, select auto repeat and tactile feedback, and add bell 8 chars before end of line. All user selections are stored in continuous memory. The setup mode can also be downline loaded. Single-unit price is $1295. **Falco Data Products, Inc,** 1286 Lawrence Station Rd, Sunnyvale, CA 94086.

Circle 346 on Inquiry Card

Low cost intelligent terminal provides split screening overwrite protection in ergonomic package

WY-100 monochrome (green) terminal features an ergonomic configuration with a detailed keyboard and a rotating and tilting display. Graphics line drawing ability allows forms to be created on screen, while a protected field feature prevents the operator from inadvertently overwriting the form. In addition, the terminal handles horizontal and vertical split screen operation; the operator can display more than one form or group of data simultaneously. The terminal's editing features can be used in each split screen section.

Standard communications capabilities include 15 transmission baud rates from 50 to 9600 baud via a std RS-232-C or optional 20-mA current loop interface. Dialogue between terminal and host computer can occur in conversational (char at a time) or block (entire message at a time) mode. A second communications port is a local printer interface that allows data transfers at rates between 50 and 9600 baud.



Editing functions include erase-line and erase-page, typewriter style tabbing, the ability to page back and forth between the first std and second optional page of memory, char/line insert and delete, and automatic word wrap. There are two additional display lines over and above the 24- x 80-char lines the main part of the display screen comprises. The uppermost line allows the host CPU to display status information to the terminal, while the lower line provides an area for the host computer to label eight soft keys on the terminal keyboard, F1 through F8. Display attributes for screen highlighting include blink, dim, inverse video, blank, and underscore, plus combinations of these.

Keyboard features include a 14-key numeric pad to speed numerical data entry; a separate 8-key cursor control pad allows rapid display cursor movement. Six keys handle editing functions, while four others handle transmitting a line, page, or message of printing the screen contents. **Wyse Technology, Inc,** 726 Charcot Ave, San Jose, CA 95131.

Circle 347 on Inquiry Card

Touch sensitive CRT

Touch Command™ model 40 terminal has touch sensitive screen with 80 discrete 3-line x 8-char touch positions. The 12″ (30-cm) diagonal, nonglare screen has a format of 24 lines x 80 chars, and a char set with 128 displayable ASCII codes each formed by a 7 x 8 dot matrix. Its 5 display modes can be used in any combination. Moreover, the terminal uses an RS-232-C interface and has a transmission speed of up to

(continued on page 258)

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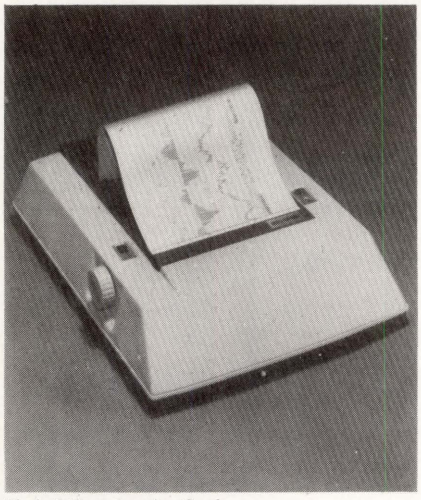
9600 bps. Software design does not require the user to learn special codes or have typing or data processing skills. Touching instruction from menu shown on the display screen lets the user retrieve and update desired information, which is then displayed on the screen. **A. R. Shaw,** 10800 Lyndale Ave S, Bloomington, MN 55420.

Circle 348 on Inquiry Card

Video printer

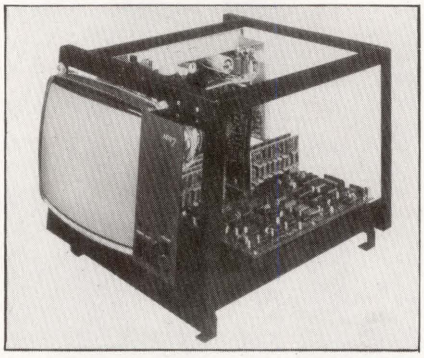
Model EX-1650 produces full-size hardcopy output directly from video input. Any displayed data including complex graphics, alphanumeric data in any size or font, foreign symbols, and hieroglyphics can be reproduced on the printer. The device operates from the composite video information displayed on the screen, and requires only a single connection to a std video jack. No external hardware or software is required. Paper width is 8.5″ (21.6 cm). Printhead is self-adjusting and requires no maintenance. **Axiom Corp,** 1014 Griswold Ave, San Fernando, CA 91340.



Circle 349 on Inquiry Card

VT100 compatible color terminal

MVI-7 13″ (33-cm) preconverged color terminal is RS-232-C/RS-422 or current loop compatible and offers a DEC VT100 emulation package designed to operate with the user's existing monochrome software. Simple instructions can enhance current software to better distinguish and relate data on user application programs. The terminal features vertical and horizontal scroll, 4 independently addressable and scrollable screens, 2 pages of screen memory, and 1280 user programmable symbols. Asynchronous protocols are used for communication between the terminal and the host or modem. Display is 80 chars x 24 col plus a status line. Memory can be configured for 80 x 56, 140 x 32, or 160 x 28 to allow for nondestructive horizontal and vertical scroll. Graphics capability is implemented via 1280 user definable chars with an effective resolution of 720 x 228. Terminal is available in desktop and rackmountable versions. **Colorgraphic Communications Corp,** Suite 105, 2379 John Glenn Dr, Atlanta, GA 30341.



Circle 350 on Inquiry Card

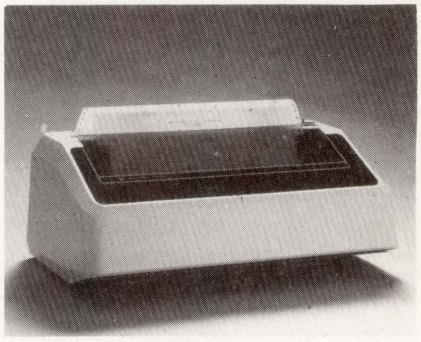
Dot matrix printer produces 8-color graphics

Prism Printer™ 132-col dot matrix printer produces 8 colors using a 4-band ribbon that carries the process colors of cyan, magenta, and yellow, as well as black. The microprocessor controlled printer offers true logic seeking look ahead capability and a high speed slew for max output. It has a std RS-232-C serial interface as well as a Centronics compatible parallel interface. Serial transmission rates are switch-selectable from 300 to 9600 baud.

The printer uses a 9-wire ballistic type printhead that incorporates 2 staggered rows of print needles to create vertically overlapping dots in a single pass of the printhead. In addition to achieving correspondence quality dot matrix print, this feature helps achieve true mixing of basic colors. In the normal (correspondence) mode, the unit prints overlapping high density (24 x 9) matrix chars at up to 150 chars/s bidirectionally. A high speed data mode enables the user to select a std density matrix and output large volumes of data at print speeds in excess of 200 chars/s.

Standard features include proportional spacing, enhanced (bold) text printing, and std print densities of 10, 12, or 16.7 chars/in (3.9, 4.7, or 6.6/cm). The unit prints a full 132 chars/line at 10-pitch; other pitches provide line lengths up to 220 col on std 15″ (38-cm) wide EDP paper. A semiautomatic cut sheet feed feature allows the operator to simply insert an 8.5″ x 11″ (21.6- x 28-cm) sheet into a slot at the bottom of the printer; it is then automatically positioned by the printer for high throughput printing.

Selectable features include automatic text justification, programmable horizontal and vertical tabbing, reverse paper feed, and fine positioning of 0.008″ (0.021-cm) chars. While the printer employs the std ASCII upper- and lowercase 96-char set, up to 4 different 96-char sets can reside within the printer simultaneously. The printer is priced at $1995. **Integral Data Systems, Inc,** Milford, NH 03055.



Circle 351 on Inquiry Card

Displays provide customized screen formats, improved data readability

To ease creation of customized screen formats and improve data readability, DASHER® D400 and D450 smart terminals can separate information into as many as 24 windows on the screen, each with independent scrolling and editing capabilities. They can also simultaneously display 80- and 135-col wide text in separate windows. Both terminals feature up to 162-col horizontal scrolling and a 256-char set that includes 7 different languages, as well as scientific and word processing symbols, and a line drawing set for simple graphs and bar

(continued on page 260)

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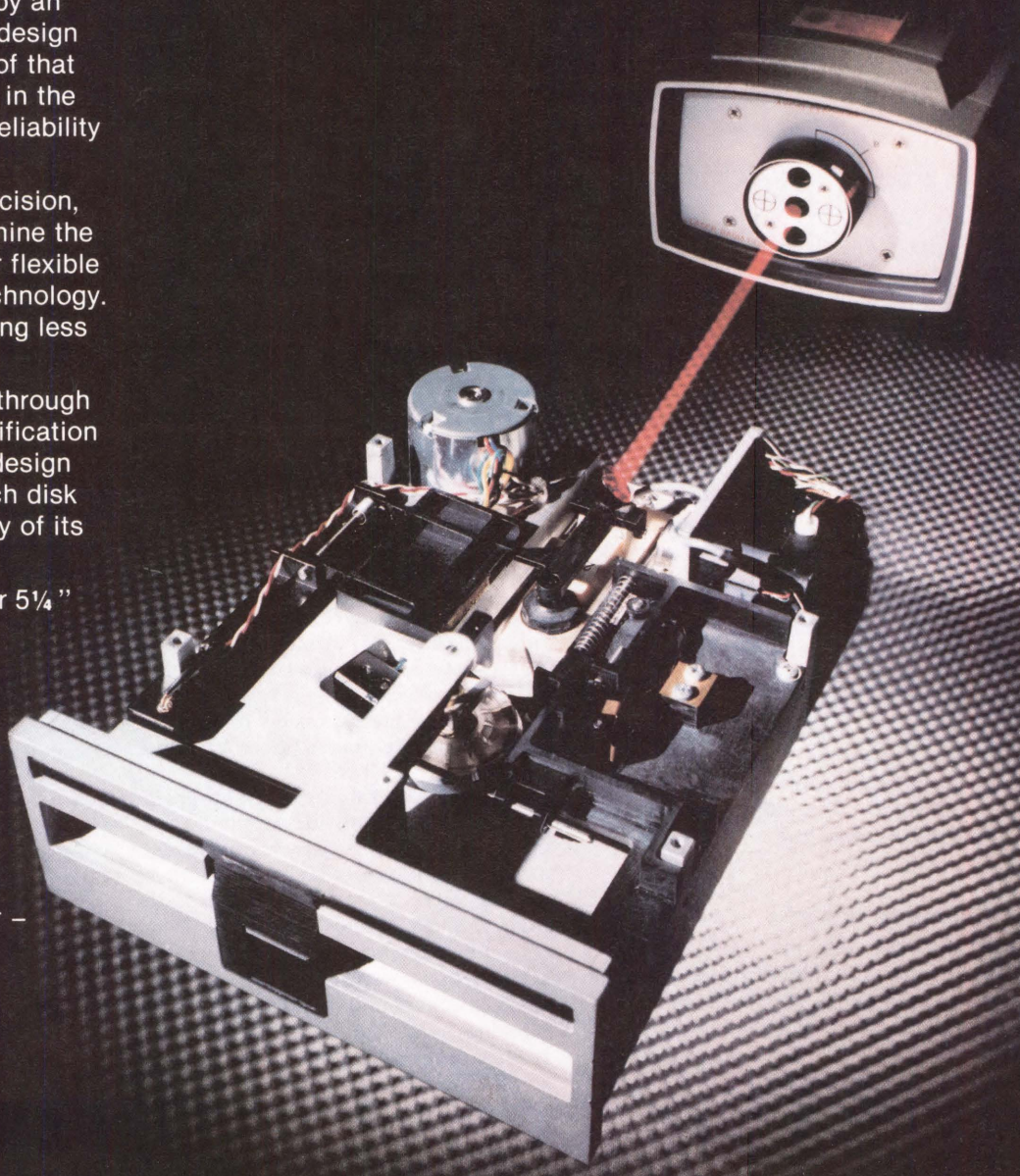
Or contact our Distributor – Diplomat Electronics, 490 S. Riverview Drive, Totowa, NJ 07512 (201) 785-1830



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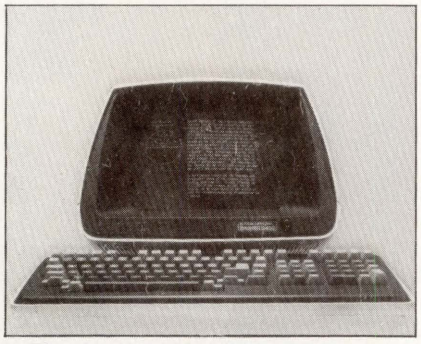
CC/3010-003 SIQ 966

CIRCLE 147 ON INQUIRY CARD

charts. Both displays also offer editing features such as insert and delete line and character. A local print capability and print pass-through mode are supported as well.

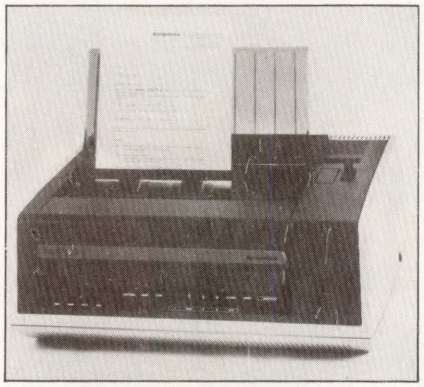
Local insert and delete capabilities reduce traffic to and from the host processor, reducing programming time in applications system development. Displays feature an ergonomic design that includes a detached, sculptured keyboard with matte finish keytops, homing keys, and a tilt and swivel green phosphor screen to reduce glare and eyestrain.



The D450's 1024-char storage capability allows the user to create and store symbols on the central processor and then load them into the terminal to display unique chars, patterns, diagrams, logos, and graphs. These can be presented alone, or intermixed with normal alphanumeric text. The terminal also supports business graphics; users can display business related information such as financial performance, sales trends, and scientific or industrial data in simple, clear tabular or graphic form. The terminals are upward compatible with the Dasher D200 display. **Data General, Information Systems Div,** 4400 Computer Dr, Westboro, MA 01581.
Circle 352 on Inquiry Card

Dot matrix printer

Performing data and word processing functions with letter quality printing, GP300 is capable of reproducing letterhead quality company logos, charts, and fixed graphics. It will also produce optical wand readable bar codes and OCR-A and OCR-B chars. Its 18-needle (9 x 9) interlaced dot matrix head permits 18- x n-char generation in 1 pass. When 36 x n chars are required for higher resolution, the printhead automatically moves ½ dot high to give full interlace on the reverse printing without moving the



paper. The head prints 9 x 9 matrix for data processing at 300 chars/s and 18 x 25 matrix for word processing at 80 to 120 chars/s. Data quality (9 x 9) and gothic (18 x 25) type fonts are std; 10 additional fonts are available. A 16k or 32k RAM is optional for storing downloaded fonts or graphics. Printer operates on 115/230 Vac at 50/60 Hz. Standard interface is RS-232-C compatible, with Centronics parallel as an option. **Amperex Electronic Corp,** 230 Duffy Ave, Hicksville, NY 11802.
Circle 353 on Inquiry Card

Interactive display functions as soft keyboard

1780A Infotouch display allows the operator to interface directly with the display screen. Functioning as a soft keyboard, the display shows the operator preprogrammed, process oriented messages. Each instruction is clearly defined on the screen. To run this software oriented system, which can be configured to meet a variety of applications, the operator need only read and touch.

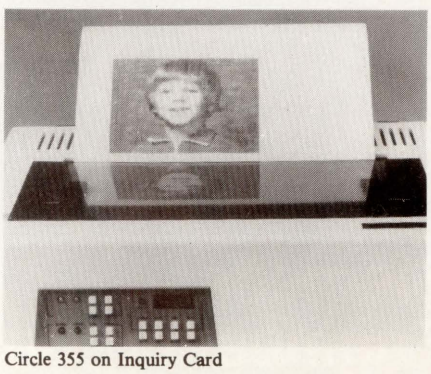
A low profile 7.6- x 19-cm wide green phosphor screen provides optimum eye comfort and incorporates a transparent switch overlay providing 60 distinct sensing areas arranged into a 6 x 10 matrix. Single touch resolution to 1 cm is combined with no-key rollover for unambiguous response. Any combination of char highlighting, including blinking, inverse video, and underlining, is available by software control. The cursor can be software selected as blinking or nonblinking reverse block, or suppressed.

Display format is selectable by program control to provide up to 1280-char capacity in the normal size (16-line x 80-char) mode, or up to 320 chars in the double size (8-line x 40-char) mode. Patterns for the std char set are stored in EPROM, providing 96 ASCII chars, 15 Greek symbols, and eleven 1720A style graphic chars. An optional alternate char mode allows for an additional 117 chars for max flexibility. All char sets are contained in 2716 or 2736 type PROMs.

Intended for international use, the display automatically selects 50- or 60-Hz operation as soon as power is applied. Std RS-232-C interface ensures compatibility with most system designs. The std display is housed in a durable industrial module designed for simple end user systems. Special OEM configurations are available. **John Fluke Mfg Co, Inc,** PO Box C9090, Everett, WA 98206.
Circle 354 on Inquiry Card

Option package for DS180 matrix printer

Package includes graphics, compressed print, display mode, and an expanded buffer. A dot addressable raster scan graphics feature allows the user to print computer generated charts, graphics, maps, and other pictorial images. Under program control, 6 individual printwires can be addressed to print high density output at a resolution of 75 dots/in (30/cm) horizontally and 72 dots/in (28/cm) vertically. Along with compressed print for variable horizontal pitch selection, print sizes include 10, 12, and 16.5 chars/in (4, 4.7, and 6.5/cm), as well as expanded modes of 5, 6, and 8.25 chars/in (2, 2.3, and 3.2/cm). Print size can be selected manually or under program control and stored in the printer's nonvolatile memory. An additional 1000 chars are available to the 1000-char FIFO print buffer, allowing the user to dump a full CRT screen of 1920 chars to the printer without interrupting normal system operation. **Datasouth Computer Corp,** 4740-A Dwight Evans Rd, Charlotte, NC 28210.



Circle 355 on Inquiry Card

TDK and ELPAC Have Combined Their Power Conversion Technology . . .

. . . To Provide the American Market with the Best Value Per Watt In DC/DC Converters

That's right . . . TDK and Elpac have combined their engineering and electronic expertise to expand their availability of DC-DC converters by over 200%. Elpac's nationwide distribution network now makes it possible for you to obtain the best value per watt in DC-DC converters from .2 to 10 watts.

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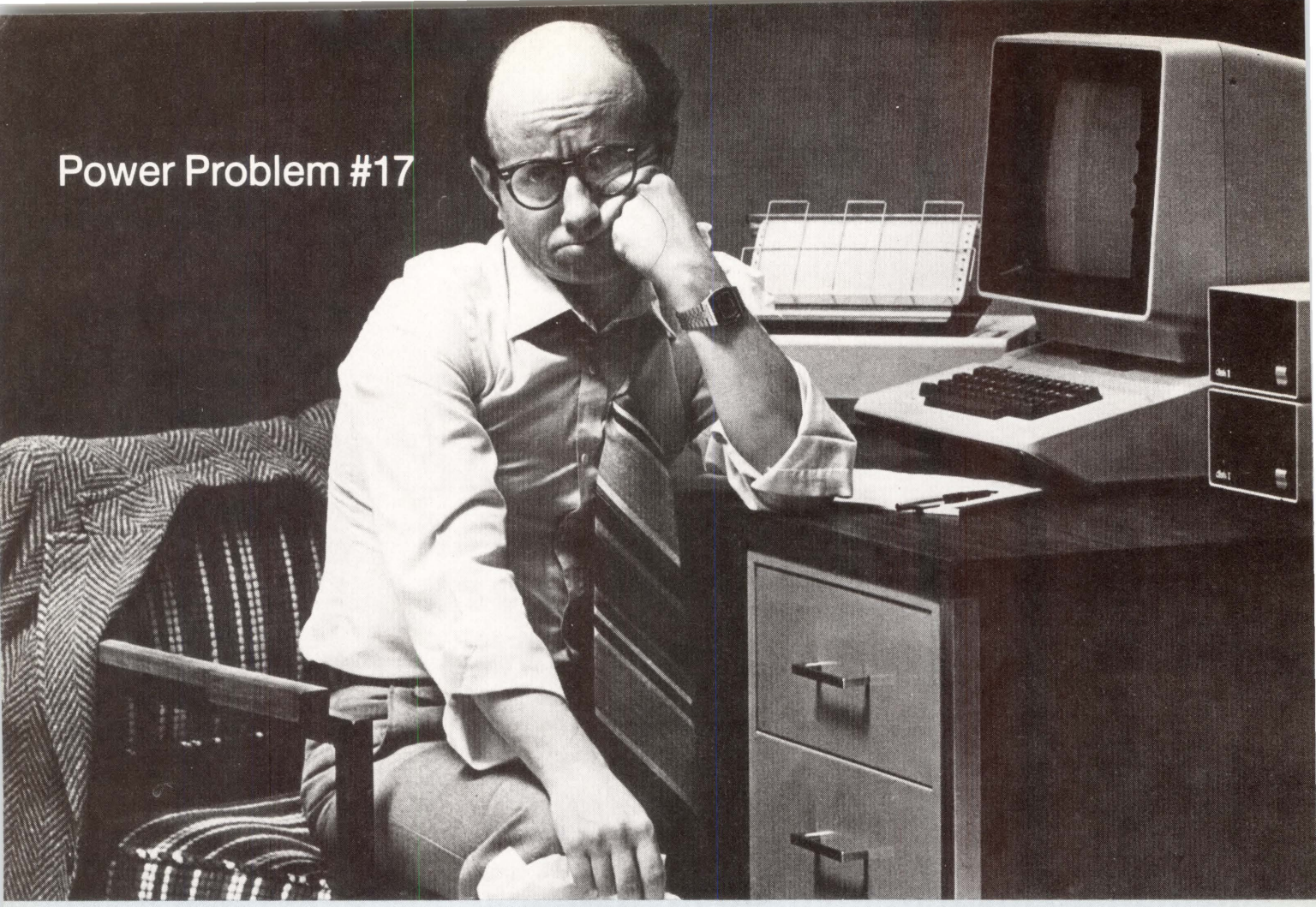

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Answer: With a Topaz Source 2® Standby Power System.

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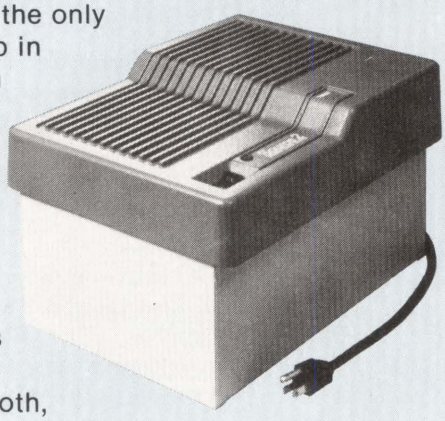

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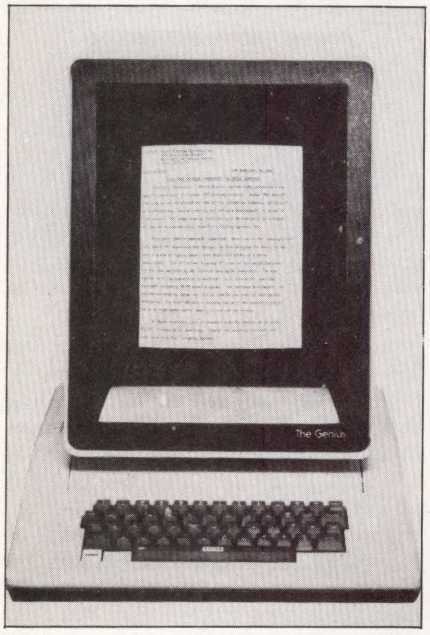
CIRCLE 146 ON INQUIRY CARD

Apple compatible, full page CRT display terminal

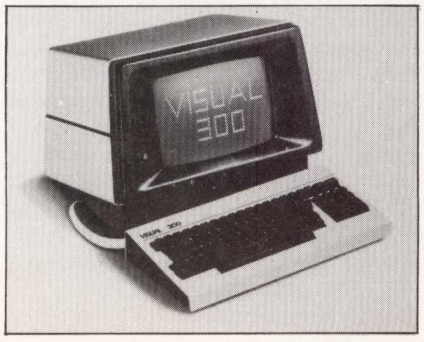


With a 15″ (38-cm) screen, The Genius™ displays 57 lines x 80 chars of text, and 66 lines x 80 chars optionally. The system is fully compatible with WordStar™, SoftCard™, and other packages, including CP/M based programs. In addition, it can display large sections of code at one time for editing and debugging. The high resolution display has an 87-MHz bandwidth and 6k bytes of high speed buffer memory to refresh the screen. An Apple interface card is std with the terminal. **Micro Display Systems, Inc,** 514 Vermillion St, Hastings, MN 55033.

Circle 356 on Inquiry Card

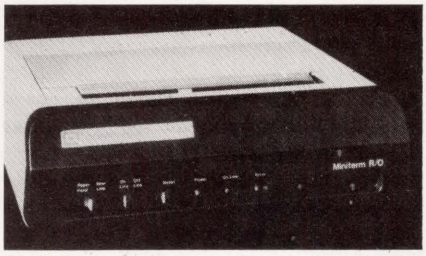
Microprocessor based video display terminal

Acting as a simple conversational TTY replacement, a multipaged text editing terminal, or a power buffered editing terminal, VISUAL 300 features block and char transmission, in addition to 12 user programmable, nonvolatile function keys, each capable of storing 32 codes. It also has blink, underline, inverse, bold, and blank video attributes requiring no display space; up to 8 pages of display memory; block graphics and line drawing char set; split screen; full editing; programmable, nonvolatile columnar tabbing; and forward, backward, and autofield tabbing. Its command set complies with the ANSI X3.64 std for display terminals. Ergonomic features include a 12″ or 14″ (30 or 36 cm) nonglare screen in either green or white phosphor; high density 7 x 9 dot matrix chars (7 x 11 on lowercase); 25th status line; detached keyboard with coil cable; sculptured nonglare keycaps; audible keyclick; 2-speed smooth scrolling; and tilt screen. **Visual Technology Inc,** 540 Main St, Tewksbury, MA 01876.



Circle 357 on Inquiry Card

Bidirectional receive-only data terminal



High speed, lightweight model 2100 is designed for online applications requiring hardcopy output, for OEM or turnkey system applications, or for use as a remote or standalone printer terminal. The 14-lb (6.4-kg), 14″ x 12.5″ x 4.5″ (36- x 31.8- x 11.4-cm) terminal offers a 2k buffer; 160-char/s bidirectional printing; 80/132-col selectability, a serial RS-232-C interface; a 5 x 10 dot matrix, full 128 ASCII char set that has upper- and lowercase chars with descenders and true over/underscore; and software controls to aid terminal configuration as std features. Eight selectable hardwire transmission speeds from 110 to 9600 baud are provided. A Centronics compatible parallel interface is optional. The terminal uses Intel's 8051 microcomputer chip and a specially designed 1 x 11 dot matrix high speed thermal printhead. **Computer Devices, Inc,** 25 North Ave, Burlington, MA 01803.

Circle 358 on Inquiry Card

80-col buffered terminal

Excel 42 12″ (30-cm) CRT terminal features a 2-page display memory, smooth scrolling within the 48-line memory, double-wide and double-high/wide characters, blink, blank, inverse video, dual intensity, underline, protect attributes, and built-in self diagnostics.

User programmable function keys, multiple transmission commands, status mode, and protected/unprotected fields are also provided. The terminal's ergonomic features include nonglare, tiltable screens with detachable keyboard and separate cursor control/numeric pad. **Datamedia Corp,** 7401 Central Hwy, Pennsauken, NJ 08109.

Circle 359 on Inquiry Card

Dot matrix line printer

Bidirectional H-25 prints at speeds in excess of 150 chars/s and up to 300 lines/min. The unit's char set has all 95 ASCII chars, upper- and lowercase, plus 33 graphics chars. Character width or pitch is operator selectable from 10, 12, 13.2, or 16.5 chars/in (4, 4.7, 5.2, or 6.5/cm). Capable of printing std edge punched or fanfold paper from 3.5″ to 17.8″ (8.9 to 45.2 cm) in width, the printer forms characters with a 9 x 9 dot matrix. "No-roller" paper feed reduces the possibility of jamming and eases reloading. LEDs on the control panel indicate if the printer is on, if it is online with the computer, or if the printer is out of paper, jammed, or has the cover open. Automatic test printing and status lights are built-in for service diagnostics. The printer interfaces with most std microcomputer systems using an RS-232-C serial interface or a 20-mA current loop. **Heath Co,** Benton Harbor, MI 49022.

Circle 360 on Inquiry Card

Graphics microsystem

HP 1000 model 5 combines the company's Graphics/1000-II software with a graphics terminal to provide high performance graphics on a low cost microcomputer system. The system handles applications

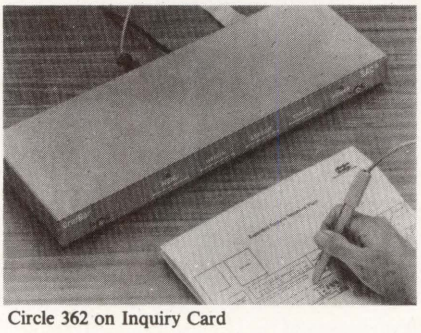
(continued on page 264)

ranging from data display graphics to the realtime graphic display of process monitoring information. It supports 16M-, 27M-, or 64M-byte Winchester fixed disk drives that may include built-in tape cartridges for loading or updating software or for system backup. Graphics/1000-II software is a high level applications tool that does not require complex coordinate conversions and provides device independence. Available software includes 2 realtime executive operating systems, IMAGE/1000 database management software, DS/1000-IV networking software, FORTRAN, BASIC, Pascal and Assembly. Optional graphics peripherals, including a built-in graphics printer, plotters, graphics tablet, and digitizer, can be used to tailor the system to specific applications. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 361 on Inquiry Card

Sonic digitizer

GrafBar™ GP-7 sonic digitizer features a large 18″ x 24″ (46- x 61-cm) active area and two point microphones to eliminate the conventional L-frame microphone assembly. Integral microprocessor converts slant ranges into absolute Cartesian coordinates. Outputs include RS-232 series ASCII, parallel 8-bit packed binary, or BCD packed. RS-232 baud rate is selectable at either 110 or 150 to 19,200 in 8 steps. Both stylus and cursor compatible, the unit has 0.01 in/cm output resolution and 125-count/s digitizing rate. A 115-Vac power supply is built-in. **Science Accessories Corp,** 970 Kings Hwy W, Southport, CT 06490.



Circle 362 on Inquiry Card

Interactive video display terminal

D81 buffered editing system, operating in either conversational or block mode, provides an alphanumeric keyboard with an IBM Selectric™ typewriter like layout and nonglare keytops, plus a nonglare display to ease eye strain.

Keyboard is also equipped with a numeric pad section and fast repeat type keys that enable rapid data entry. Separate keys control the movement of the switch selectable cursor that operates in block or underline and blinking or nonblinking modes. The terminal has an RS-232-C asynchronous interface operating at up to 19.2k baud, half- or full-duplex, as well as a std serial printer interface. Data format is 24 lines x 80 chars, plus a top status line of 80 chars, for a total of 2000 displayable positions on the 12″ (30-cm) diagonal screen; char format is a 6 x 8 dot matrix in a 7 x 10 field. The device's 128 displayable symbols include 96 ASCII chars, 21 control chars, and 11 chars to support line drawings. Editing features include erase, insert, and delete char and line functions. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.

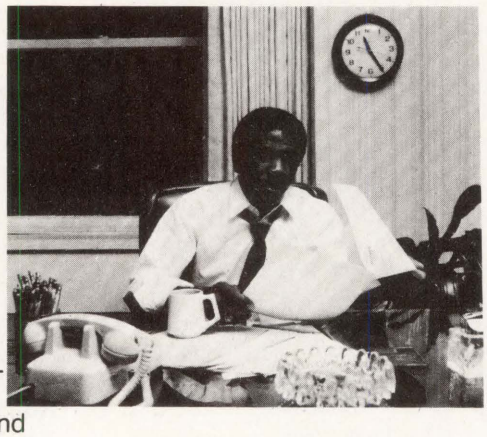
Circle 363 on Inquiry Card

General purpose 74-key alphanumeric keyboard

KS99 std keyboard features a moving plate capacitor, a tease-proof switch detection circuit, a single-piece unitized frame impervious to moisture and dust, bounceless keyswitch operation, and an advanced microprocessor. The moving plate capacitor is composed of a hinged moving plate and a single fixed plate, both attached to the PCB. Other features include numeric, function, and cursor pads, alternate action, serial or parallel output, automatic repeat keys, n-key rollover, and stepped, sculptured keytops. The keyboard is ASCII encoded and TTL compatible. An EPROM enables it to be programmed for a variety of applications. **The Digitran Co,** 855 S Arroyo Pkwy, Pasadena, CA 91105.

Circle 364 on Inquiry Card

Heart attack or stroke could knock you down on your way up.



You're working for the challenge, the satisfaction, the success. The last thing you want is a heart attack or stroke. Yet, nearly one million Americans die of heart disease and stroke every year. And 200,000 of them die before retirement age.

The American Heart Association is fighting to reduce early death and disability from heart disease and stroke with research, professional and public education, and community service programs.

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WE'RE FIGHTING FOR YOUR LIFE

OEM EUROPE MEETS AT THE INVITATIONAL COMPUTER CONFERENCES

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At these one day, regional conferences guests will have a close-up view of every type of computer and peripheral-mini/micros, disk drives, tape drives, printers, interfaces, controllers, graphic display terminals—and will be welcome to attend a program of technical seminars covering the latest state-of-the-art technology. Some of the companies associated with the series include Arsycom BV, Century Data Systems, CII Honeywell-Bull, Cipher Data Products, Control Data, Dataram, Genisco Computers, International Memories, MDB Systems, Priam, Printronix, Remex, National Semiconductor, Kennedy and Trilog.

Technical product seminars will be presented on streaming tape drives, graphic display systems, winchester disks, matrix line printers, color printer/plotters and add-in memories.

Plan to attend the conference in your area. Invitations are available from participating companies or from the ICC sponsor. For further information contact:

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Invitational Computer Conference Spring 1982 Series

London	**March 11, 1982**
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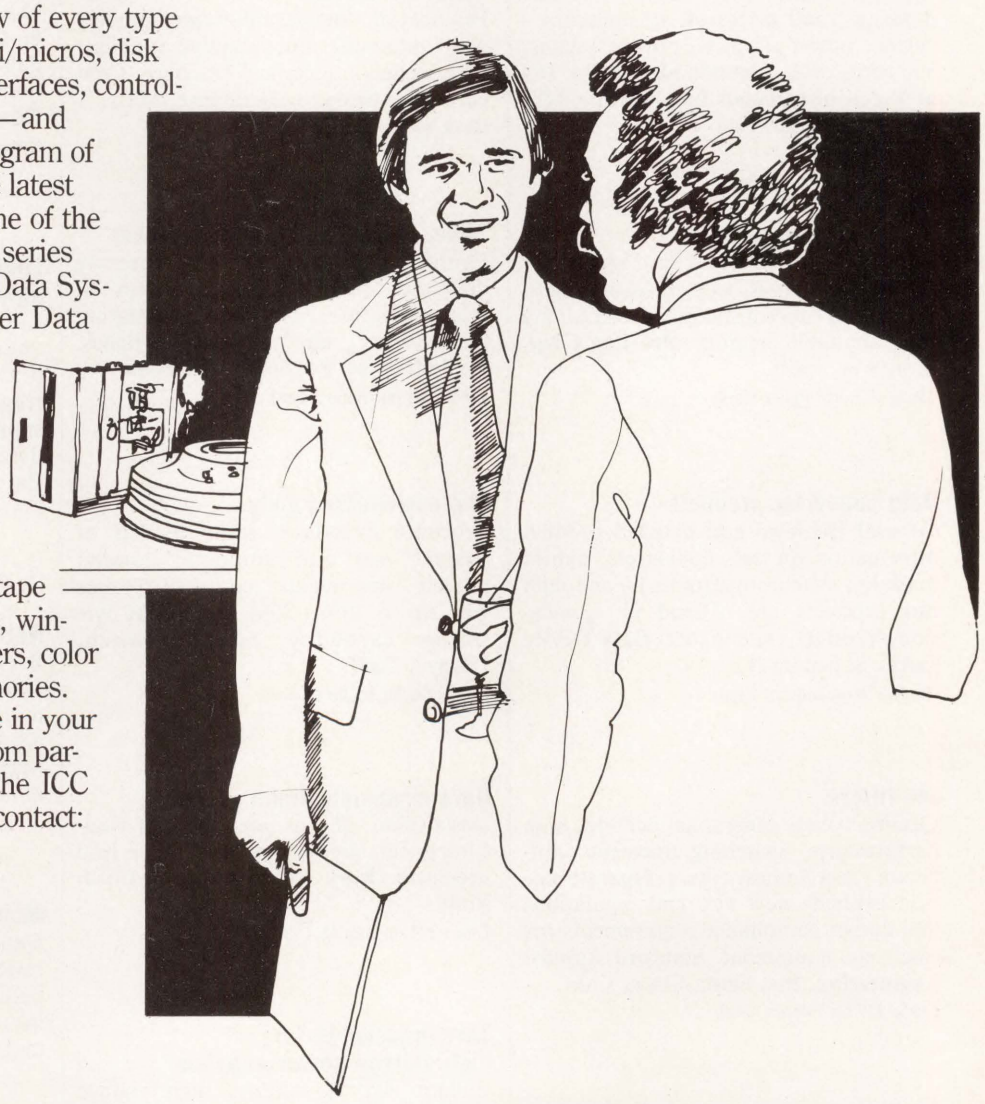


Invitational Computer Conferences

64k dynamic RAM board with transparent refresh

Application note AN-835 describes hardware required to implement a hardware refreshed 64k dynamic memory board for use with M6800 or M6809 systems. **Motorola Inc, MOS Microprocessor Div,** Austin, Tex.

Circle 375 on Inquiry Card

Power supplies

Catalog contains detailed specs, outline drawings, and prices of the company's current power supplies, power systems, and accessories. **Lambda Electronics, Div of Veeco Instruments Inc,** Melville, NY.

Circle 376 on Inquiry Card

Programmable devices

Selection guide provides data on bipolar fusible link PROMs, MOS erasable PROMs, PALs, and microprocessors containing programmable memory. **Pro-Log Corp,** Monterey, Calif.

Circle 377 on Inquiry Card

Data converter products

General technical and detailed product information on data converters, hybrid modules, synchro instruments, and data bus products are offered in applications/product catalog. **ILC Data Device Corp,** Bohemia, NY.

Circle 378 on Inquiry Card

EMI filters

Catalog covers general application, high performance, switching transient, connector, and 3-phase filters; separate section explains new FCC emi regulations and design compliance requirements for electronic equipment. **Stanford Applied Engineering, Inc,** Santa Clara, Calif.

Circle 379 on Inquiry Card

Oscilloscope measurement techniques

Application note explains keystroke programming techniques using 7854 microprocessor based oscilloscope that can streamline and improve repeatability of complex measurements. **Tektronix, Inc,** Lexington, Mass.

Circle 380 on Inquiry Card

Virtual memory computer systems

Brochure contains overview of the company's minicomputers, including throughput rates, performance measurements, and max number of interactive terminal users supported; VULCAN virtual memory operating system is also described. **Harris Corp, Computer Systems Div,** Fort Lauderdale, Fla.

Circle 381 on Inquiry Card

1200-bps modem

Features of CDS V.22 full-duplex modem with automatic and adaptive equalizer are detailed in technical brochure. **Concord Data Systems,** Lexington, Mass.

Circle 409 on Inquiry Card

Slide, rocker, and toggle switches

Found in catalog are engineering drawings, full specs, and photos of microminiature, standard, miniature Sydewynder^{R}, and miniature switches. **CW Industries,** Southampton, Penn.

Circle 382 on Inquiry Card

Microcomputer family

Brochure introduces seven models of System 2800 microcomputer family; models listed include hard disk systems with up to 10M-, 20M-, and 40M-byte storage capability. **Systems Group,** Orange, Calif.

Circle 383 on Inquiry Card

Data communications system

Description, photos, and specs of Digi-Link system are supplied in detailed 16-p brochure. **Kaye Instruments,** Bedford, Mass.

Circle 384 on Inquiry Card

Test procedures for high voltage power supplies

Bulletin STP-783 outlines high voltage power supply test setups and loading methods, output current regulation, ripple, temp coefficient, and stability checks; charts show applications and features of typical supplies. **Spellman High Voltage Electronics Corp,** Plainview, NY.

Circle 385 on Inquiry Card

16-bit microprocessor

Spec sheet provides functional description, block diagrams, ac/dc characteristics, and instruction set summary of SAB 8086 C microprocessor. **Siemens Corp,** Iselin, NJ.

Circle 386 on Inquiry Card

Common-mode emi filters

Schematic diagrams, specs, charts listing international emi filter specs, and tables of min loss and frequencies are included in selector guide for common-core or dual-function emi filters. **Genisco Technology Corp, Components Div,** Rancho Dominguez, Calif.

Circle 387 on Inquiry Card

Linear and switching power supplies

Catalog describes features, specs, voltage/current ratings, and outline drawings of switches, linear open frames, and CP series computer power supplies; options and accessories are also described. **Deltron Inc,** North Wales, Pa.

Circle 388 on Inquiry Card

Network management system

Brochure highlights capabilities, features, and options of 90/10 data communications network control and management system. **Intertel, Inc,** Andover, Mass.

Circle 389 on Inquiry Card

Multiplexer

Data sheet provides detailed technical review of PIN 9102 X.25 network interface multiplexer. **Gandalf Data Inc,** Wheeling, Ill.

Circle 390 on Inquiry Card

Data bus products

Data sheets, general specs, features, and prices of MIL-STD-1553 data bus product line are outlined in 44-p catalog. **SCI Systems, Inc,** Huntsville, Ala.

Circle 391 on Inquiry Card

CRT connectors
Dimensional drawings, illustrations, and technical data on 7-, 8-, and 14-pin units are presented in catalog. **Connector Corp,** Chicago, Ill.
Circle 392 on Inquiry Card

Tubeaxial fans
Bearing type, volts, Hz, air performance dB levels, and mounting and connecting data are furnished in catalog that describes more than 40 units with accessories. **ebm Industries, Inc,** Farmington, Conn.
Circle 393 on Inquiry Card

Laser-trimmable resistor networks
Data sheet features TRIM-PAK™ networks, listing specs, applications, tabulated performances and ranges, and packaging information; illustrations include time-stability curves, application diagrams, and dimensional drawings. **Electro-Films Inc,** Warwick, RI.
Circle 394 on Inquiry Card

Image processing system
Modular precision image processing system is introduced in 6-p brochure that configures 3 typ systems for basic and advanced image analysis, and multi-user applications. **EIKONIX Corp,** Bedford, Mass.
Circle 395 on Inquiry Card

Access control system
Illustrated 4-p preview brochure highlights functions and capabilities of D-4000 computerized access control system. **Cardkey Systems,** Chatsworth, Calif.
Circle 396 on Inquiry Card

Thick film paste
Low temp curing, filled thermoplastic dielectric thick film paste is described in data sheet that discusses printing and curing processes, as well as applications. **Electro-Science Laboratories, Inc,** Pennsauken, NJ.
Circle 397 on Inquiry Card

Microcomputer modules/accessories
Catalog describes 30 ModulasOne® boards, including microcomputer modules, memory boards, analog and digital interface boards, and special purpose boards such as floppy disk controller/formatters and IEEE 488 interface modules. **Adaptive Science Corp,** Emeryville, Calif.
Circle 398 on Inquiry Card

Data communications equipment
Descriptions plus photos and general specs of high speed test sets, data traps and monitors, and error correction systems are provided in catalog. **International Data Sciences, Inc,** Lincoln, RI.
Circle 399 on Inquiry Card

Heat sinks
Description of product line is supplied in 6-p, full-color facilities and capabilities brochure. **Jonathan Thermotek Products, Div of Jonathan Manufacturing Corp,** Fullerton, Calif.
Circle 400 on Inquiry Card

Open frame power supplies
Over 132 models of dc power supplies are described in photos and text of 12-p catalog. **Condor, Inc,** Camarillo, Calif.
Circle 401 on Inquiry Card

Voice data entry technology
Newsletter format 4-p brochure reports on capabilities of systems in applications such as manufacturing, quality control, materials handling, and numerical control programming. **Threshold Technology Inc,** Delran, NJ.
Circle 410 on Inquiry Card

Single-chip microcomputer
Technical bulletin contains specs, diagrams, functional description, instruction set, signal descriptions, addressing modes, and timing characteristics for model 6500/1. **Commodore Semiconductor Group,** Norristown, Pa.
Circle 402 on Inquiry Card

Interconnection systems
Catalog furnishes description of Alpha System line of flat cables, connectors, headers, and sockets, including part numbers, specs, operational characteristics, construction materials, dimensions, pin versions, and applications. **Alpha Wire Corp,** Elizabeth, NJ.
Circle 403 on Inquiry Card

Pushbutton switches
Expanded line of series 75, including watertight switch, is described in 16-p, updated catalog. **Ledex Inc,** Vandalia, Ohio.
Circle 404 on Inquiry Card

Jumpers, headers, and accessories
Catalog describes line of socket, PCB, card edge, DIP, D subminiature, dual-row plug, dual- and single-row boards, single-row socket, and custom jumpers. **Symbex Corp,** Chico, Calif.
Circle 405 on Inquiry Card

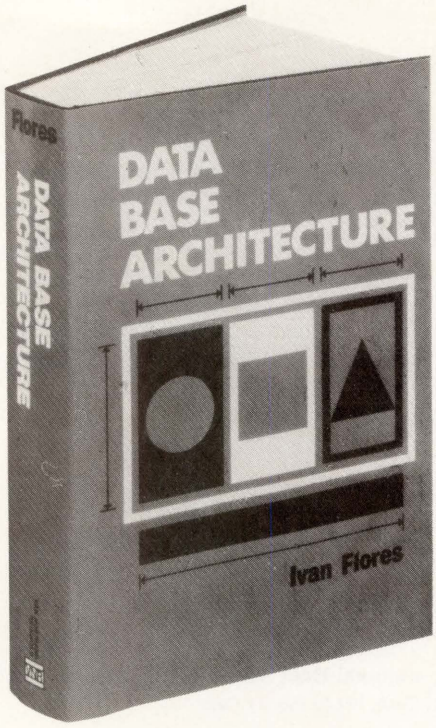
Reed relays
Complete specs; dimensional drawings; electrical, mechanical, and operational data; and pull-out design sheet feature series 100, 300, 400, 500, 700, and 800 reed relays. **Hamlin, Inc,** Lake Mills, Wis.
Circle 406 on Inquiry Card

DC motor systems
Brochure discusses low inertia, dc, permanent magnet motors/motor systems, and application illustrations, with specific attention to high speed/torque, precision control, and ms time response. **Inertial Motors Corp,** Doylestown, Pa.
Circle 407 on Inquiry Card

Edge connectors
Product bulletin outlines technical information and specs for expanded line of CARDCON™ edge connectors. **TRW Cinch Connectors, Div of TRW Inc,** Elk Grove Village, Ill.
Circle 408 on Inquiry Card

Designer's Bookcase

Data Base Architecture by *Ivan Flores, Ph.D.*



This is the definitive guide to data base organization, giving the answers to the why's and how's. It describes the structure and use of information organized into a data base, and how application programs, data structures, data base management systems (DBMS), the operating system, and hardware relate to each data base organization.

408 pages; 295 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. July, 1981.
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This book presents the fundamental concepts on which modern 16- and 32-bit microprocessor architectures are based. A boon to anyone who must select or design a microprocessor or minicomputer system, the book also illustrates the impact of computer architecture on software efficiency and reliability.

Published by Microcomputer Applications
Softbound, 5½ x 8½, 240 pp, 1980, $10.95
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Computer-Assisted Data Base Design by *George U. Hubbard.*

This book not only thoroughly explains the theoretical aspects, but also provides explicit directions on all data base design procedures. In addition to a practical design methodology it discusses the ways to automate the major portions of this methodology. However, all of the techniques can be utilized without computer assistance.

320 pages; 123 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; $24.95. August, 1981.
Circle 457 on Inquiry Card

ANDROID DESIGN: Practical Approaches for Robot Builders by *Martin Weinstein.*

A comprehensive look at the tools, materials and techniques necessary for designing an android. Examines what an android is, what you can expect it to do, and how this will translate into the design requirements. Also looks at both usual and unusual hardware and software, and mechanics and mechanisms.

Hayden Book Company, Inc., 256 pages, 6 x 9, 5192-1, $11.95 Circle 458 on Inquiry Card

DATA COMMUNICATIONS a user's guide by *Kenneth Sherman.*

A BRAND NEW quick and effective source for pinpointing and eliminating system malfunctions, discovering new, more efficient data movement, learning effective troubleshooting, ensuring strong, clear signal transmission and achieving maximum performance and value. Put these *all new* ideas and many others to work for you!

348 pages; 95 illustrations; Reston Publishing Company Inc; $21.95. 1981.
Circle 459 on Inquiry Card

MANAGING SOFTWARE DEVELOPMENT AND MAINTENANCE by *Carma L. McClure, Ph. D*

This book presents practical project management methods that focus on the management and maintenance issues of the software life cycle.

Managing Software Development and Maintenance can help solve a wide range of management and maintenance problems currently encountered in providing to industry high quality software systems within time and budget constraints.

224 pages; 42 illustrations; 6 x 9; Van Nostrand Reinhold; $16.95. Publication date: February 1981.
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AD INDEX

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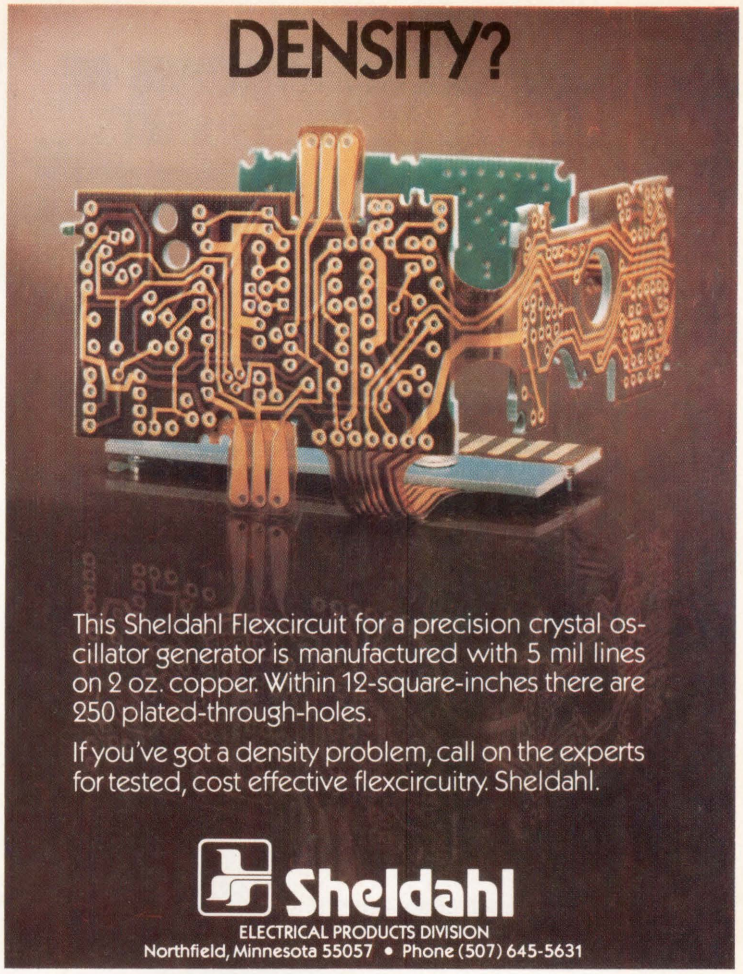

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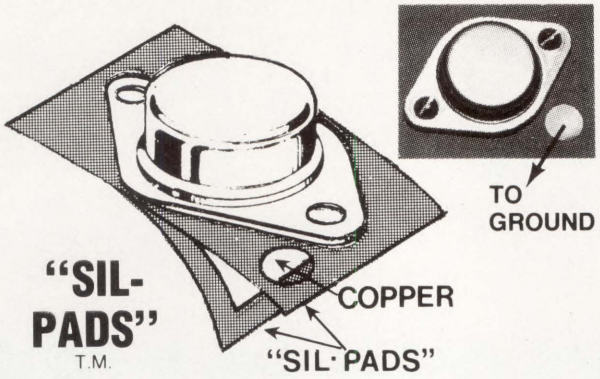

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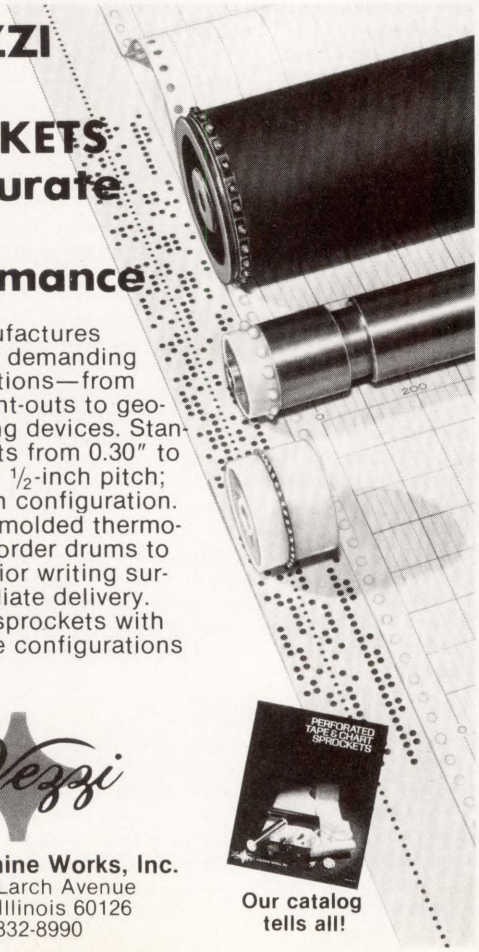

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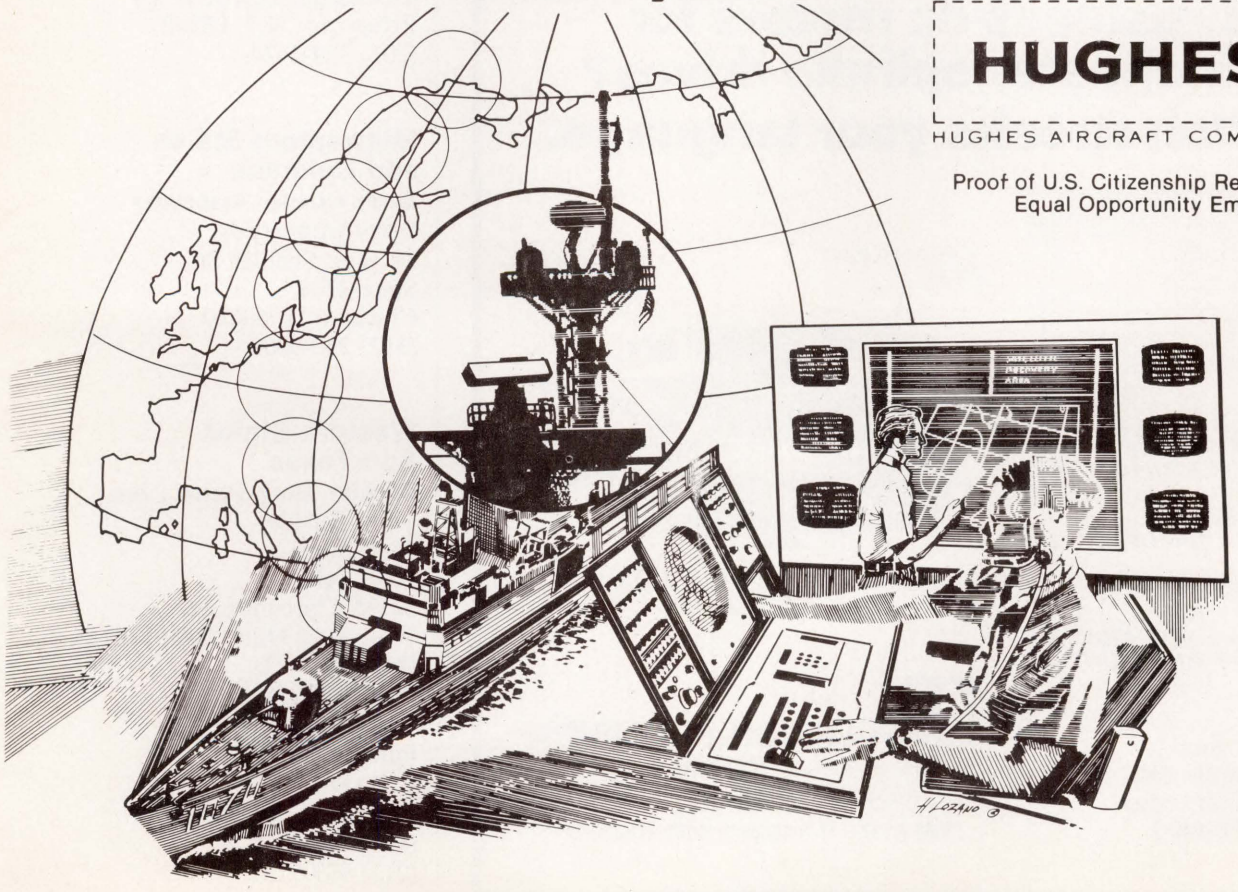

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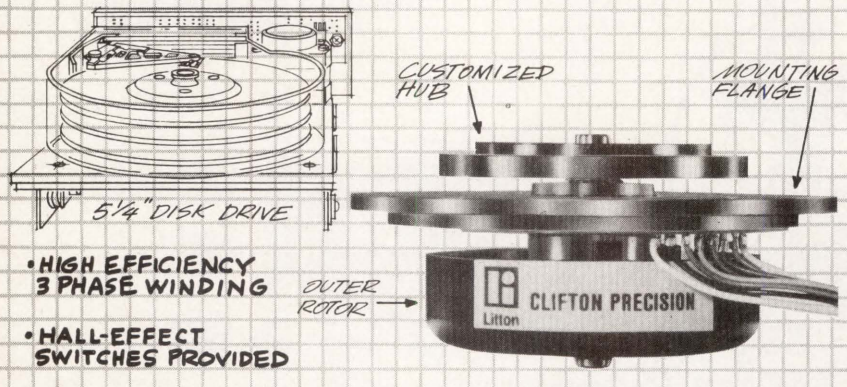

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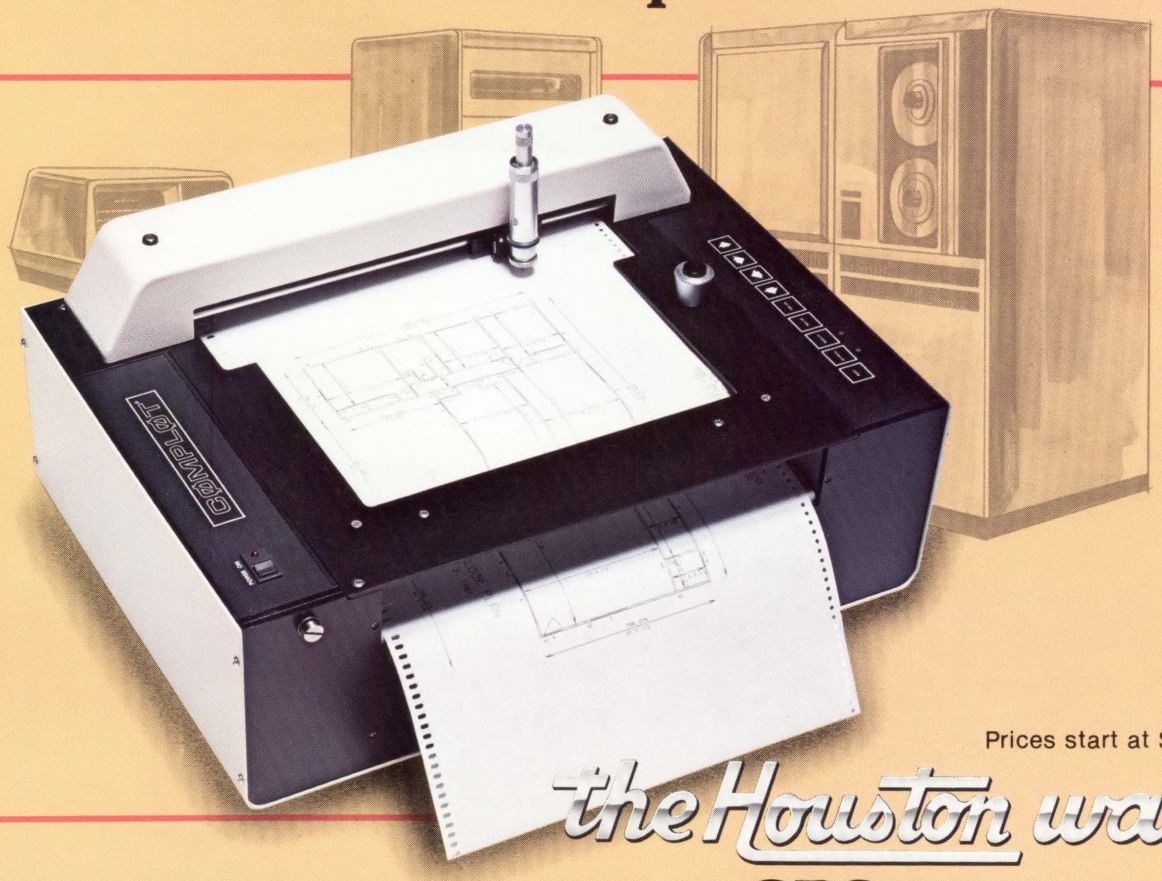

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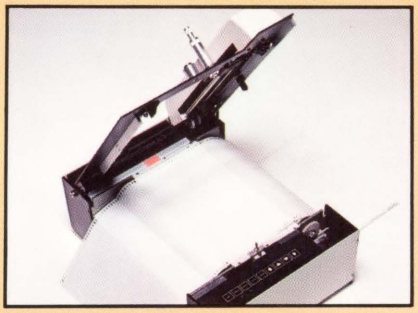

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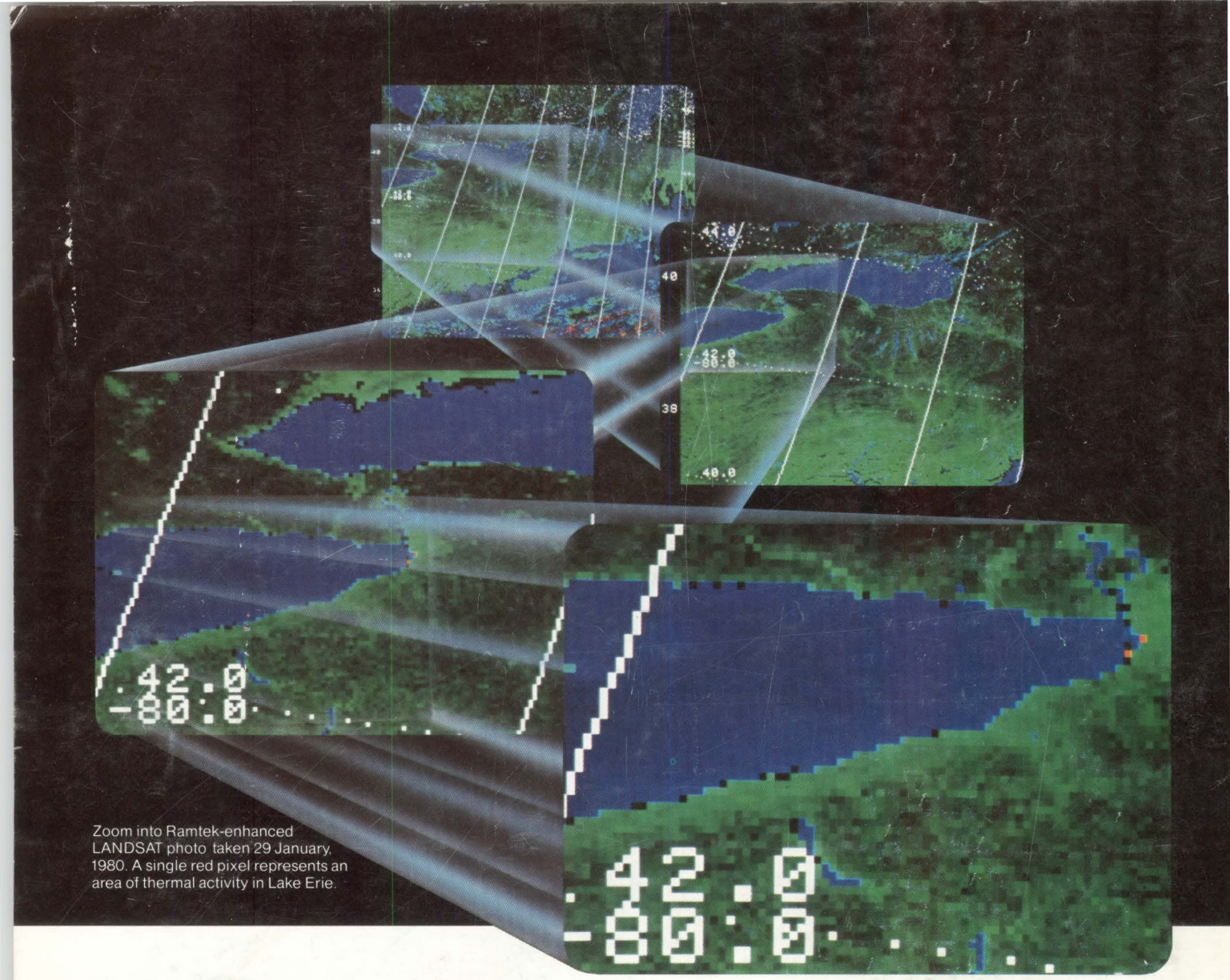

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