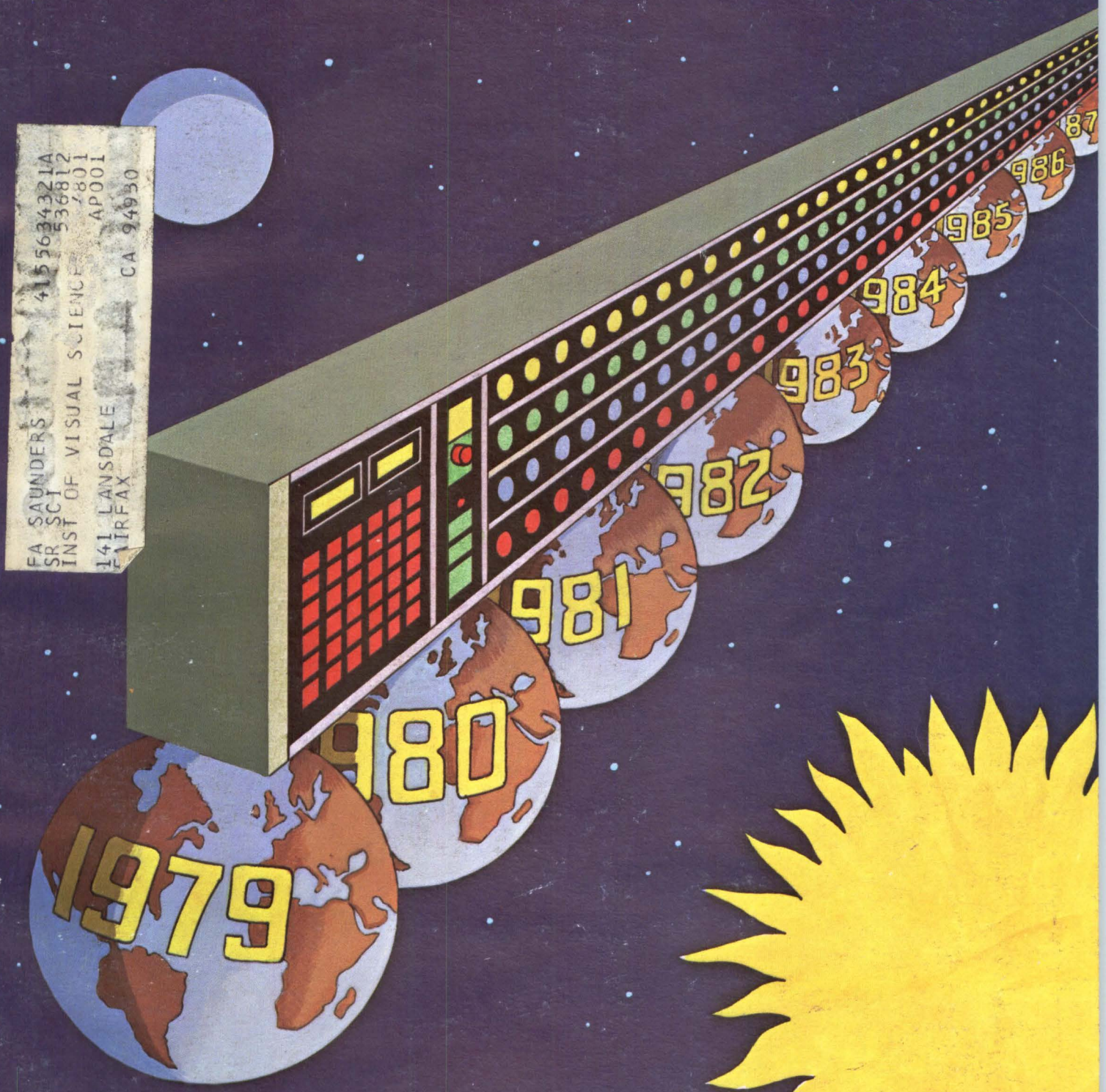
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

APRIL 1979



PROCESSOR ARCHITECTURE ANTICIPATES FUTURE PERFORMANCE REQUIREMENTS

DESIGNING A MICROPROCESSOR DRIVEN MULTIPURPOSE PERIPHERAL CONTROLLER

LOGICAL ENVIRONMENT COMPARISON TESTING HANDLES COMPLEX LSI DEVICES

OUR PDP-11* MAGTAPE CONTROLLER IS GOOD AS GOLD

every two hours of every working day somebody puts a TC-130 on a PDP-11 computer

Here are just a few of the reasons why more people put TC-130's on their PDP-11 systems than any other magtape controller:

- Software compatible – embedded design
- Mixed density – 1600 bpi PE and 800, 556, 200 bpi NRZ
- Intermix 9 track and 7 track, up to 8 drives
- Fits all PDP-11 Series Computers
- Dual speed – switch selectable, 12.5 to 125 ips

SEND FOR COMPLETE INFORMATION

western peripherals

Division of WESPERCORP

(714) 991-8700 • TWX 910 591-1687
Cable WESPER
1100 Claudina Place, Anaheim, CA 92805

Western Peripherals Service Centers located in,
Anaheim, California (714) 991-8700
Linthicum, Maryland (301) 796-2236
Lewisville, Texas (214) 436-5577
Zeist, Netherlands 03404-21344

CIRCLE 1 ON INQUIRY CARD

* Trade name of Digital Equipment Corp.

Kennedy peripheral products.

Buying is just the beginning.

There's a lot more to any company's success than just the products it sells. We know that at Kennedy. That's why we help select the Kennedy product best suited for your requirement; it's the reason we've established training seminars for people using our equipment; it's why we have virtually over-night service; complete documentation; and completely stocked service centers and parts depots in the U.S. and Europe. And always someone at the end of the phone to answer questions about service, delivery, modifications, interfacing — you name it. If you're a customer of Kennedy, you know it. If you're not, give us a call.

KENNEDY CO.

540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953

CIRCLE 2 ON INQUIRY CARD

KENNEDY- QUALITY– COUNT ON IT

IT'S THE FLEXURE THAT GIVES THE MUSCLE TO THE UNMATCHED RELIABILITY OF TALLY LINE PRINTERS.

Flexure technology—special steel couplings that support and move the print carriage. The print hammer fingers of the patented Tally print comb are also flexures.

Designed for unlimited life, a flexure has no wear points nor lubrication requirements. Adjustments are never necessary.

Thus the stage is set for a highly reliable printing technique based on low stress parts moving at low speed over short distances. For example, print hammer movement—there's a hammer for each character position—is limited to the distance of a single character. Tally has eliminated clutches, belts, timing variables, cam shafts, pivots and sliding wear surfaces. There are no preventive maintenance requirements. No duty cycle limitations.

And this is only the beginning of the benefits you get from the Tally T-2000 printer. 125 or 200 lines per minute. Superb print quality. Quiet operation. Low cost of ownership. Contact your nearest Tally sales representative for more facts.

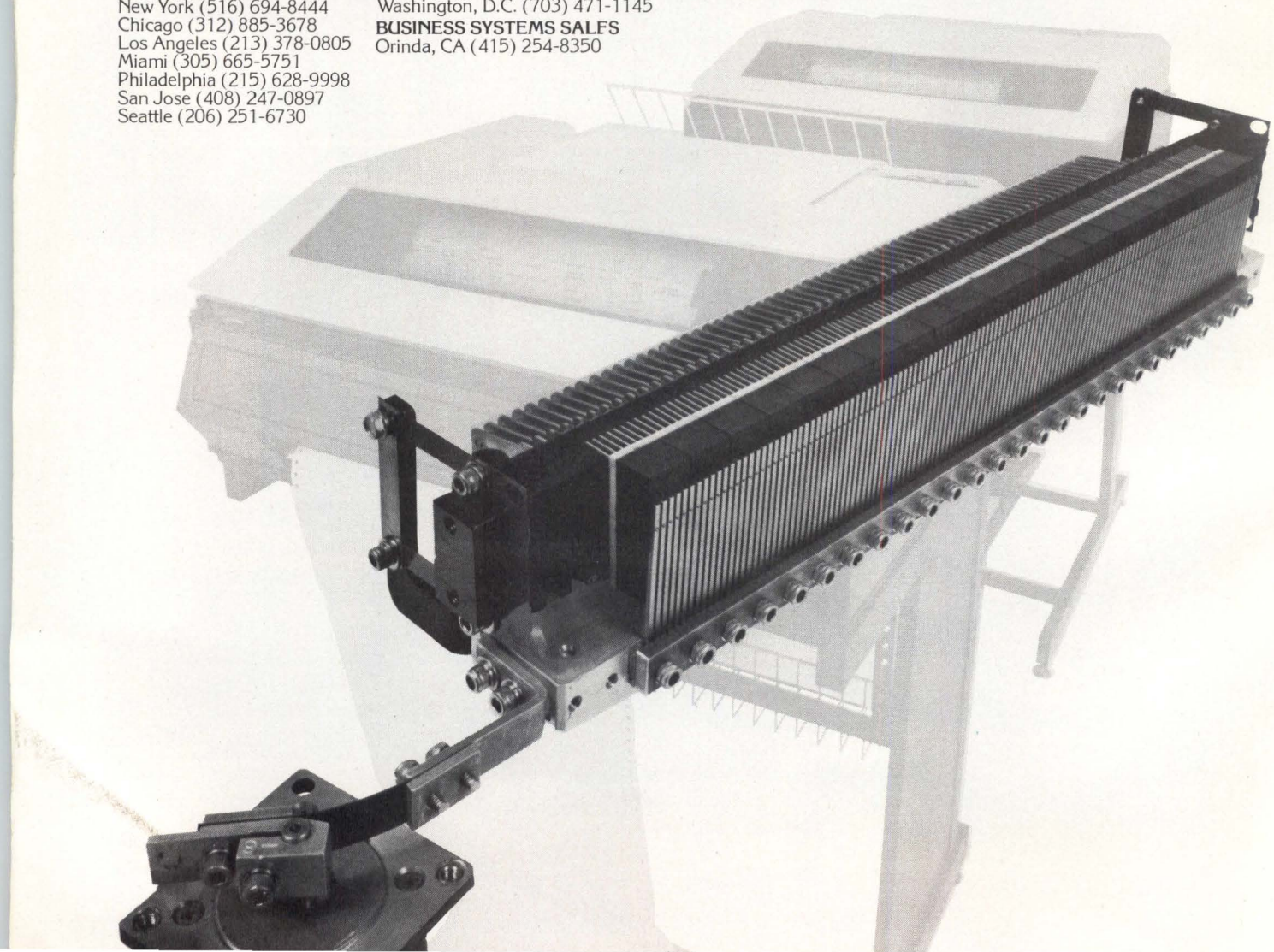
Tally Corporation, 8301 S. 180th St.,
Kent, WA 98031. Phone (206) 251-5500.

CIRCLE 3 ON INQUIRY CARD

TALLY® PRINTERS WORLDWIDE

OEM SALES OFFICES
Boston (617) 272-8070
New York (516) 694-8444
Chicago (312) 885-3678
Los Angeles (213) 378-0805
Miami (305) 665-5751
Philadelphia (215) 628-9998
San Jose (408) 247-0897
Seattle (206) 251-6730
San Antonio (512) 733-8153
Washington, D.C. (703) 471-1145

BUSINESS SYSTEMS SALES
Orinda, CA (415) 254-8350



COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

APRIL 1979

VOLUME 18, NUMBER 4

DEPARTMENTS

BPA **CIRCULATION: 67,155 (JUNE 1978)**

(USPS 127-340)

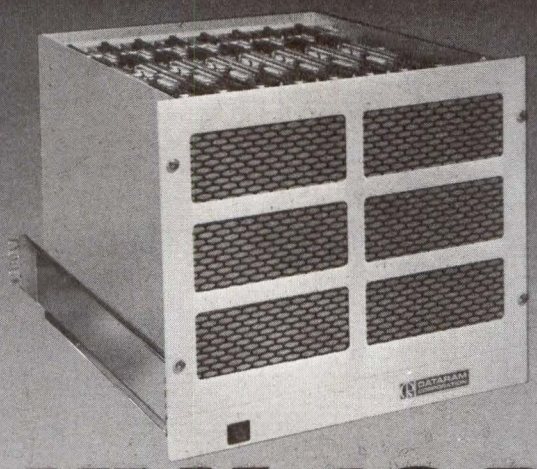
FEATURES

CONFERENCES

STAFF

Editorial & Executive Offices
11 Goldsmith St
Littleton, MA 01460
Tel. (617) 486-8944
(617) 646-7872

Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."



SEE US AT NCC BOOTH 1506

featuring dual-port capability for DEC® and Data General emulators

BULK CORE

NOW AVAILABLE WITH THE INDUSTRY'S MOST EXTENSIVE LINE OF CONTROLLERS

Now Dataram's popular BULK CORE is available with interfaces that bring all the proven features of this high-capacity, high-reliability, low-cost memory system to your minicomputer.

Use BULK CORE as peripheral storage or main memory. In either 7″ or 15¾″ chassis. With storage capacities up to two megabytes in one chassis. And with dual-port capability available for DEC and Data General disk emulators.

And in addition to offering high-capacity storage, BULK CORE has the added advantages of non-volatility and high reliability.

And all available with interfaces to these popular minicomputers (and there are more coming!):

DEC
LSI-11® RF-11 fixed-head disk emulator
PDP®-11 RF-11 single-port, fixed-head disk emulator
PDP-11 RF-11 dual-port, fixed-head disk emulator
PDP-11/70 main memory

Data General
Novadisc® (4019 compatible) single-port emulator
Novadisc (4019 compatible) dual-port emulator
AOS (6063/6065 compatible) fixed-head disk emulator

Interdata
Moving-head disk emulator

Modular Computer Systems
MEMORY +

Find out today how BULK CORE can help you get more out of your minicomputer. Contact Dataram at 609-799-0071 or send in the coupon below.

I'd like to learn more about BULK CORE for my _____ minicomputer.

☐ Please send information.
☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

☐ Please send me information about Dataram's ADD-ON/ADD-IN memory for minicomputers.

DEC, LSI-11 and PDP are registered trademarks of Digital Equipment Corporation. Novadisc is a registered trademark of Data General.

DATARAM CORPORATION

PRINCETON-HIGHTSTOWN ROAD CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

Canada: Ahern & Soper Ltd., Alberta, British Columbia, Ontario, Quebec • **Finland:** Systek OY, 90-737-233 • **France:** YREL, 956 81 42 • **Italy:** Mactronics Italia, 02/35 36 041 • **Netherlands:** Technitron b.v., 020-45 87 55 • **Sweden:** M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom/Ireland:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany/Austria:** O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 543 2076 • **India:** Industrial Electronic Instruments, 79281 • **Israel:** K.D.M. Electronics, 921513 • **Japan:** Matsushita Electric Trading Co., Ltd., 03 (435) 4501 • **Taiwan/Republic of China:** Syscom Computer Engineering Co., (02) 7022156.

CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

MAY 8-10—Society for Information Display Internat'l Sym, Chicago Marriott Hotel, Chicago, Ill. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: (305) 446-8193

MAY 11-13—West Coast Computer Faire, Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: (415) 851-7075

MAY 17—Trends and Applications: Advances in Systems Technology Sym, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Trends and Applications, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAY 18-20—Mid-Atlantic Personal and Business Computer Show, National Guard Armory, Washington, DC. INFORMATION: Mid-Atlantic Expositions, Inc, PO Box 3315, Annapolis, MD 21403. Tel: (301) 263-8044

MAY 23-25—Custom Integrated Circuits Conf, Americana Hotel, Rochester, NY. INFORMATION: Dr Andras I. Lakatos, Xerox, Webster Research Ctr, 800 Phillips Rd, Bldg 114, Webster, NY 14580. Tel: (716) 422-4354

MAY 30-JUNE 1—APL79, Rochester, NY. INFORMATION: Fletcher McTaggart, I. P. Sharp Associates, Suite 1150, 183 Main St E, Rochester, NY 14604

JUNE 4-6—Machine Tool Forum, Pittsburgh Hilton, Pittsburgh, Pa. INFORMATION: J. Vincent Hanratty, Westinghouse Electric Corp, Westinghouse Bldg, Gateway Ctr, Pittsburgh, PA 15222. Tel: (412) 255-3693

JUNE 4-7—National Computer Conf, New York Coliseum, Hilton Hotel, and Sheraton Centre New York, NY. INFORMATION: Marjorie Greimel, American Federation of Information Processing Societies, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810

JUNE 10-14—Internat'l Conf on Communications, Sheraton Hotel, Boston, Mass. INFORMATION: James J. Lanigan, Director, Public Affairs, GTE Sylvania Inc, 100 First Ave, Waltham, MA 02154. Tel: (617) 890-9200

JUNE 13-15—Computer Applications in Industry, Alpes Congres, Grenoble, France. INFORMATION: The Secretary, Computers in Industry, PO Box 354, CH-8053 Zurich, Switzerland

JUNE 17-20—Joint Automatic Control Conf, Hilton Hotel, Denver, Colo. INFORMATION: Prof T. F. Edgar, Program Chm, 1979 JACC, Dept of Chemical Engineering, U of Texas, Austin, TX 78712. Tel: (512) 471-3080

JUNE 20-22—Internat'l Sym on Fault-Tolerant Computing, Concourse Hotel, Madison, Wis. INFORMATION: Prof Charles R. Kime, Dept of Electrical and Computer Engineering, U of Wisconsin, Madison, WI 53706. Tel: (608) 262-0206

JUNE 21—Information Systems—Effectiveness for the User Sym, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Angela Turvey, 4910 Butternut Dr, Rockville, MD 20853. Tel: (301) 427-8105

JUNE 25-27—Design Automation Conf, Town and Country Hotel, San Diego, Calif. INFORMATION: Robert J. Smith, III, Electrical Engineering Dept, U of Texas, PO Box 7728, Austin, TX 78712. Tel: (512) 471-4540

JUNE 25-28—Joint Conf of the CIPS and DMAC, Quebec, Canada. INFORMATION: Conference 1979, Département d'Informatique, Faculté des Sciences et de Génie, Université Laval, Quebec, Quebec, G1K 7P4, Canada

JUNE 25-29—Internat'l Sym on Information Theory, Grigano, Italy. INFORMATION: Prof M. Pursley, Dept of Electrical Engineering, U of Illinois, Urbana, IL 61801

JULY 16-18—Summer Computer Simulation Conf, Toronto, Canada. INFORMATION: Dr A. J. Schiewe, Chairman '79 SCSC, c/o The Aerospace Corp, PO Box 92957, Los Angeles, CA 90009

JULY 17-19—Internat'l Sym on Circuits and Systems, Tokyo, Japan. INFORMATION: Kazuo Horiuchi, Dept of Electrical and Comm Engineering, Waseda U, Shinjuku, Tokyo 160, Japan

JULY 17-20—Joint Intermag/Magnetism and Magnetic Materials Conf, Statler Hilton, New York, NY. INFORMATION: Dr E. F. Luborsky, Conf Chm, General Electric R&D Ctr, PO Box 8, Schenectady, NY 12301

JULY 30-AUG 3—Computer and Peripheral Equipment Exhibition, Internat'l Marketing Ctr, Singapore. INFORMATION: Todd W. Burns, U.S. Dept of Commerce, Office of Internat'l Marketing, South Asia-Rm 4126, Washington, DC 20230

AUG 29-31—IFAC Sym on Computer-Aided Design of Control Systems, Zurich, Switzerland. INFORMATION: CAD/IFAC, Institut für Automatik und Industrielle Elektronik, ETH-Zentrum, CH-8092 Zurich, Switzerland

SEPT 5-8—INFO/ASIA, Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017

SEPT 25-29—Relcomex '79—Reliability and Exploitation of Computer Systems, Ksiaz Castle near Wroclaw, Poland. INFORMATION: Mr I. Jozwiak, Institute of Engineering Cybernetics of Wroclaw Technical U, Janiszewskiego st 11/17, 50-372 Wroclaw, Poland

SEMINARS

MAY 11-12—Microprocessor Sem, U of Pittsburgh, Pittsburgh, Pa. INFORMATION: Vincent J. Giardina, IEEE Mgr of Continuing Education, 445 Hoes Lane, Piscataway, NJ 08854. Tel: (201) 981-0060, X174

JUNE 11-15 and 18-22—Chorafas Sem on Distributed Information Systems, Radisson-Chicago Hotel, Chicago, Ill; and Breckenridge Pavilion Hotel, St Louis, Mo. INFORMATION: Richard A. Laubhan, Project Communications Inc, 333 E Ontario, Suite 2603B, Chicago, IL 60611. Tel: (312) 266-2113

JUNE 27-29—Computers in Manufacturing, Chicago, Ill. INFORMATION: AIIE Seminars, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500

SHORT COURSES

MAY 14-16—Software Design for Data Communication Systems, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington University, Washington, DC 20052. Tel: (202) 676-6106

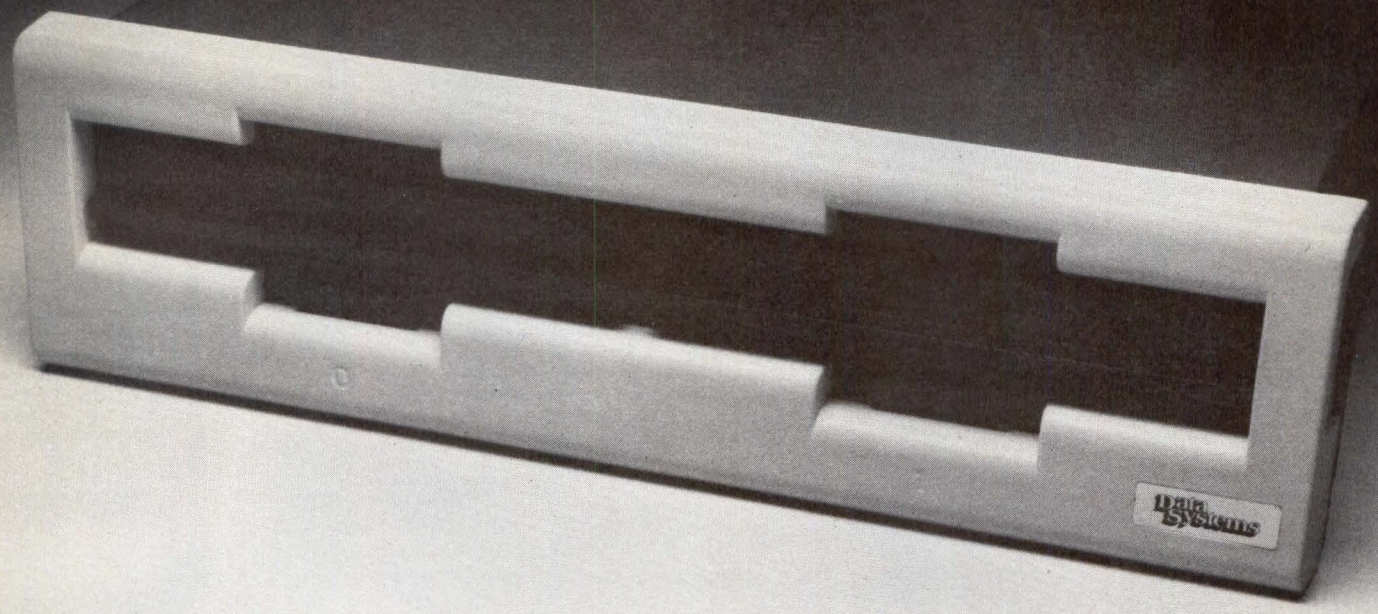
JUNE 4-6—Microprocessor Programming, Rapid City, SD. INFORMATION: Vincent J. Giardina, IEEE Mgr of Continuing Education, 445 Hoes Lane, Piscataway, NJ 08854. Tel: (201) 981-0060, X174

JUNE 19-21—Using Interactive Graphics for PC Artwork Generation and Design, New York, NY. INFORMATION: Omnimation, 2076 Elberon St, San Pedro, CA 90732. Tel: (213) 833-9637

JULY 9-20—Computing Systems Reliability, U of California, Santa Cruz, Calif. INFORMATION: Institute in Computer Science, U of California Extension, Santa Cruz, CA 95064

Announcements intended for publication in this department of *Computer Design* must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

INTRODUCING THE DSD 440. DOUBLE DENSITY, DELIVERED.



The DEC® RXO2 – Compatible Flexible Disk System with 30 day delivery.

Our new DSD 440 records data in both DEC double density and IBM 3740 single density formats. It is 100% software, hardware and media compatible with DEC LSI-11, LSI-11/2, PDP-11 and PDP-8 computers including those equipped with extended memory. The DSD 440 can be set to emulate either the RXO1 for downward compatibility or the RXO2 for increased storage capacity and throughput.

Hardware Bootstrap

A 512-word hardware bootstrap is built into the interfaces for the PDP-11, LSI-11 and LSI-11/2 systems. In addition to bootstrapping both single and double density configurations, it also performs diagnostics on the CPU memory, and the disk interface and controller.

"Hyperdiagnostics"

Microprogrammed self-diagnostics are built into the drive and controller unit. User-selectable, stand-alone "Hyperdiagnostics" simplify maintenance and alignment procedures.

The DSD 440 data storage capabilities include write protection, power loss data protection, single track and complete diskette formatting. Diskettes can be formatted using sequential or user-selected sector interleaving. Special sector interleaving schemes can be implemented during formatting to improve system throughput.

Megabyte System

This powerful megabyte flexible disk system is packaged in a low profile 5¼-inch chassis.

The DSD 440 is being shipped in quantity now. Delivery is 30 days.

To find out more about it, contact Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

Data Systems

3130 Coronado Drive, Santa Clara, CA 95051
(408) 249-9353 TWX: 910-338-0249

®Registered trademark of Digital Equipment Corporation

CIRCLE 6 ON INQUIRY CARD

How Litronix' opens a new world

Norand® Sprint 100™
Order entry terminal

Now designers have a communications peripheral perfectly matched in size and cost to the world of microcomputers.
Litronix invented the Intelligent Display* to give microcomputers a new way of "talking" to users in words, numbers or even sentences. And not surprisingly, these displays are already beginning to create a new class of microcomputer-based products.

Part Number	Features	Character Height	Horizontal Row Spacing	Vertical Row Spacing	Viewing Angle	Character Positions	Character Segments
DL-1416	Standard General Purpose Display	.160"	.250"	1.200"	±25°	4	16
DL-1414	Compact Display For Hand Held Equipment	.112"	.175"	.800"	±50°	4	16
DL-2416	Premium Display New Rugged Package	.160"	.250"	.800"	±50°	4	17

*Intelligent Display is a trademark of Litronix, Inc.

The Intelligent Display is an alphanumeric LED readout that incorporates ASCII decoder, multiplexer, memory and LED driver in a built-in CMOS IC. It interfaces simply and directly to any microprocessor bus, much like a RAM. Power is from a single +5V supply, and operating current is low enough for any battery powered device.

Litronix puts intelligent communications in the palm of your hand or anywhere panel space is limited. Three versions of the Intelligent Display are already available to fit a wide variety of applications. The smallest lets you fit 20 characters side by side in a space of only 3.5 inches.

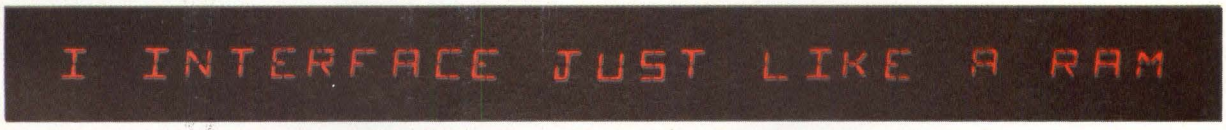
Litronix' Intelligent Displays are already being used in the portable terminal, the low cost microcomputer and electronic translator above. They're also ideally suited for applications like control panel readouts. Handheld computer

Intelligent Display™ of microcomputer applications.

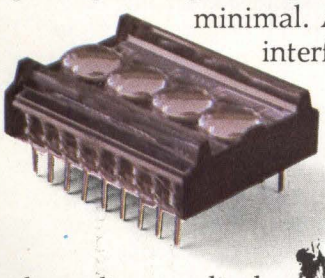
Lexicon
LK-3000™
Electronic translator

terminals. "Smart" games and appliances. Educational products, and more.

Use Intelligent Displays in any product that calls for alphanumerics. They'll reduce component count and cut costs dramatically. Since everything is encapsulated in a single package, design and production costs are minimal. And because no display interface PC board is needed, component costs are typically reduced by 25%. Typical OEM volume pricing per digit will range from $2 to $5 per digit, depending on display type. For easy breadboarding with Intelligent Displays, ask about our inexpensive, prewired Evaluation Kit. To get data sheets and a copy of our applications note



on Intelligent Displays, or for a demonstration, phone or write Litronix, Inc., 19000 Homestead Road, Cupertino, CA 95014. Telephone (408) 257-7910.



litronix
AN AFFILIATE OF SIEMENS

DATA COMMUNICATIONS TESTING OVERVIEW—ANALOG TESTING

Jeffrey R. Duerr

Hewlett-Packard Company, Delcon Division
Mountain View, California

That portion of the data communications system most out of control of the user is the carrier channel. AT&T, the largest carrier, is composed of 23 operating telephone companies across the U.S., servicing 83% of the country's subscribers. General Telephone, the next largest carrier, has about 8% of that service market. The remaining 9% is split among approximately 1550 independent telephone companies.

Standards and practices as defined by AT&T typically predominate in delineating the characteristics of these communications networks. A complete description of the properties of the analog channel as they affect data transmission is contained in the three Bell System Technical Reference publications listed in the bibliography. These documents are a basic guide to understanding the measurement requirements of the analog channel.

Carrier Facilities

There are three options when renting a voice channel from the carrier—dial-up, leased, or digital lines. While digital lines are coming into more widespread use since their inception in 1974, at the present time the first two categories are much more prevalent.

Dial-up lines, most commonly used for standard voice communication, are comparatively inexpensive, and, in a high percentage of applications, are quite suitable for basic data transmission. If such a line is unsuitable for proper data transfer because of noise or distortion, the user has the option to hang up and redial. The subscriber should be aware that he has no control over the routing of this dial-up network, and can expect widely varying transmission delays and characteristics from call to call.

Although full-duplex operation can be achieved on one dial-up line by frequency division multiplexing modems over short distances, transmission over longer distances is limited to half duplex. In this transmission mode the user will experience a delay in switching directions because circuit components in the channel take several hundred milliseconds to turn around. Also, the customer may find that the average 15 to 20 s time required to dial and obtain a line might be more than he can tolerate in an inquiry-response application.

Leased lines, though more expensive, provide the user a readily available, consistent communications path, and afford him more control over the characteristics of his channel. To further improve these lines for data transmission, the carrier will supply various types of conditioning to place more exacting requirements on channel amplitude, delay, and noise characteristics. Therefore, it would seem normal to believe that there is no need for analog test equipment to evaluate a dedicated link, since the carrier guarantees specific performance appropriate to a requested type of conditioning.

This may be true for a simple system, but as a computer communication center becomes more complex, time spent in discussing channel problems with the carrier becomes extremely costly. A better strategy is to be able to evaluate line deficiencies with procedures and equipment that are acceptable to the telephone company. Also, basic analog testing of the channel can do much to solve the finger-pointing dilemma.

Channel Parameters and Conditioning

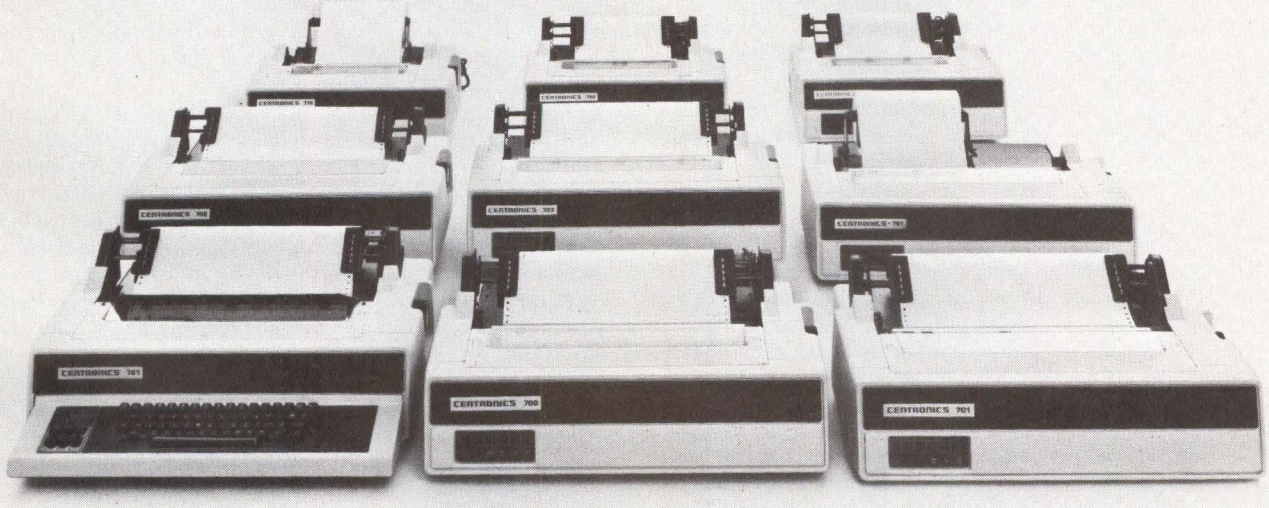
When a carrier offers a service to the user, it must have previously filed with the Federal Communications Commission (FCC) a tariff describing the service, the rates for that service, and detailed characteristics of the channel to be used. There are 11 parameters affecting data communications on an analog channel (see "Analog Channel Parameters"). In the basic channel, none of these parameters is controlled by tariff, although all except phase hits, gain hits, and dropouts are controlled to internal AT&T specifications.

(*Continued on p* 12)

Does its broad line make Centronics' matrix printer family the best?

NO. Even though the Centronics 700 series is a continually expanding printer family—currently 9 models and a range of print speeds from 60 to 180 cps—there's much more to it than just breadth of line. For example, there's a choice of 6 different types of forms handling capability; choice of uni- and bi-directional operation; and choice of 80 and 132-column formats. Why so much choice? It comes from the simple, highly flexible modular 700 series design that delivers superior reliability, exceptional parts commonality—and competitive prices.

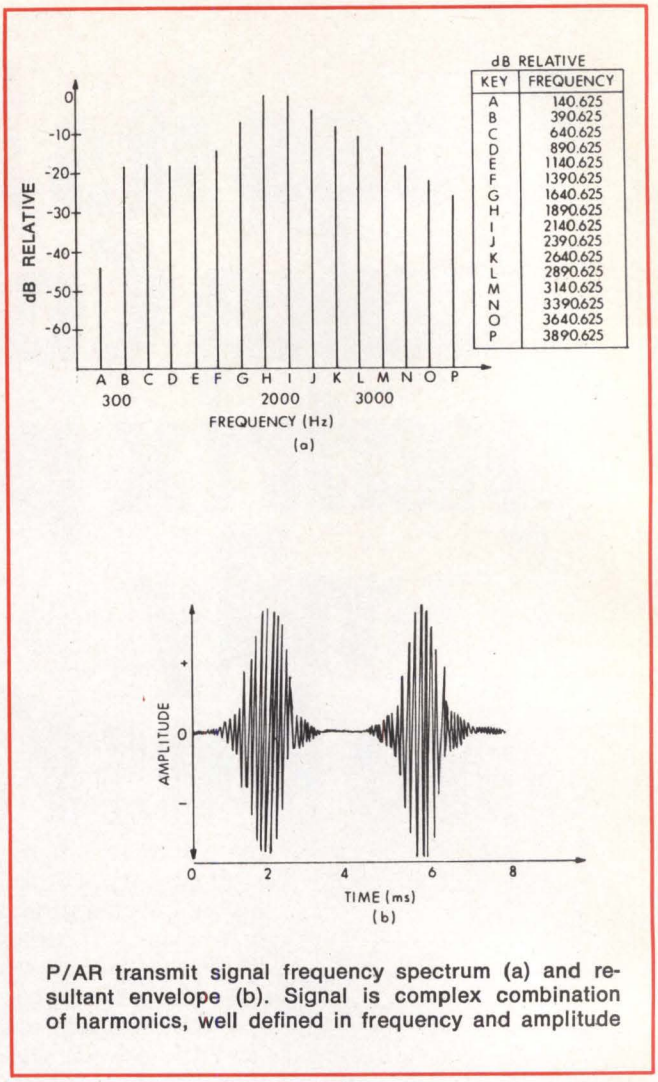
And like all Centronics printers, the 700 series is fully supported by the largest worldwide service organization of any printer company. For complete 700 series information write or call today. Centronics Data Computer Corp., Hudson, NH 03051, Tel. (603) 883-0111.



CENTRONICS® PRINTERS
Simply Better

Analog Channel Parameters

Parameter	Control
Attenuation distortion	C conditioning
Envelope delay distortion	
S/N ratio	D conditioning
Harmonic distortion	
Impulse Noise	Controlled to
Frequency shift	internal Bell
Phase jitter	specification
Echo	
Phase hits	Not controlled
Gain hits	
Dropouts	



P/AR transmit signal frequency spectrum (a) and resultant envelope (b). Signal is complex combination of harmonics, well defined in frequency and amplitude

Attenuation distortion is the variation in signal attenuation at different frequencies—the frequency roll-off curve of the network. Because the line was originally designed to transmit voice in the 300- to 3000-Hz band, severe attenuation above 2000 Hz was not critical. However, high speed data transmission has important frequency components at the higher frequencies, and this roll-off becomes a significant factor.

Envelope delay distortion is the rate of change with respect to frequency of the phase difference between transmission and reception; signal delay through the channel varies with frequency. This does not affect voice reception because the human ear is virtually insensitive to it. For this reason phase distortion was not tightly controlled in original telephone system design, but when using the voice channel for data transmission, envelope delay becomes an important parameter. The higher frequencies required for high speed data transmission systems necessitate more compatible delays across the frequency band.

Available in three levels, "C" conditioning is tariffed to give varying degrees of control in the specifications for attenuation and envelope delay distortion. The level of conditioning required depends on the bit rate transmitted, and is often defined by the modem manufacturer. Sophisticated modems having automatic equalization perform a function similar to "C" conditioning, and generally do not need it. In fact, such conditioning can prove to be detrimental to overall performance in these cases. "C" conditioning can change a normally smooth delay characteristic to a curve with steep slopes and ripple. This newer, more distorted curve will make automatic equalizer compensation more difficult.

For 9600-bit/s operation "D" conditioning has been tariffed. This specifies limits on signal-to-noise (S/N) ratio and on harmonic distortion. "D" conditioning allows higher S/N ratio and less harmonic distortion, which, although unpleasant to the human ear, is of little handicap to the modem. Harmonic distortion generates unwanted harmonics as a result of nonlinear operations combining two or more desired signals.

Although it is fairly easy to measure, nonlinear distortion measurement is a more accurate indication of this parameter. Nonlinear distortion affects reproduction of higher frequency signal components at the receive end and thus degrades fidelity of the received signal. Unlike delay distortion, the effect of nonlinear distortion is irreversible and cannot be compensated for at the receiver. Compensation must occur at the transmitter by reducing the number of distinct levels transmitted which, in turn, limits the allowable bit rate. "D" conditioning controls these parameters so that 9600-bit/s transmission is more readily obtainable on voice grade lines. It is offered to the customer in two levels and can be used with or without "C" conditioning.

Specifications for impulse noise, frequency shift, phase shift, and echo are not defined by tariff, but are controlled to internal AT&T specifications. These are published in the AT&T literature, BSP 41004, pp 13-15.

Phase hits, gain hits, and dropouts are not controlled by practice or tariff. If the user can demonstrate that his data communications are degraded by a significant number of these disturbances, the carrier company can reroute and reconfigure the communications paths. However, for credibility, the measurements made to back up such complaints should be made with equipment and to standards acceptable to the carrier. The inability to properly define line troubles is very often an obstacle to clearing them up.

Testing the Analog Channel

First level of testing on the channel can be done by simply evaluating its frequency response. Using simple equipment, the basic analog channel can be tested for continuity, signal loss at various frequencies, and noise over the bandwidth. More sophisticated equipment such as the Hewlett-Packard transmission impairment mea-

surement system (TIMS) series will make all of the measurements described. This equipment is widely used among operating companies and therefore provides a credible standard for defining line disturbances. Attachment of the equipment to the channel is done by connecting to the two or four wires of the local subscriber loop at the analog side of the modem. TIMS testing can be accomplished in looparound using one measurement set on a full-duplex system, or, using two instruments, one can test in one direction on a half-duplex system or in both directions individually on a full-duplex system. With some TIMS sets, another configuration called master-slave operation allows remote testing and feedback of results to a central station.

To define an overall figure of merit for a channel path that will describe its suitability to data transmission, AT&T has developed the peak-to-average ratio (P/AR) measurement. This technique was designed to give an overall indication of envelope delay and nonlinear distortion, and return loss. A pulse train representative of a data modulated voiceband signal is transmitted. The spectrum and envelope of this signal is shown in the Figure. At the receive end, the P/AR of the signal is measured. As the signal traverses the transmission medium, P/AR will deteriorate because of channel impairments. A perfect channel would result in a 100 P/AR reading of the received signal. Readings of 50 or higher generally indicate that 2400-bit/s or slower data rates are acceptable. P/AR is also useful as a monitor of data channel parameters. If the P/AR value changes by more than four points from an initial reading, it is likely that the channel parameters have changed significantly.

Cost Tradeoffs

How much should be invested in test equipment for a data communications channel? Basic analog level and frequency testing can be accomplished for $1000 to $2000. Test equipment that will handle all the tests described here can be purchased for $7000 to $9000.

Bit error rate (BER) testing is available in an instrument selling for less than $1000. Equipment that can perform all the digital tests described (*Computer Design*, Mar 1979, pp 12-18) will range from $2500 to $5000 per instrument.

Protocol test equipment (*Computer Design*, Feb 1979, pp 10-20) starts at about $3500 and ranges to over $15,000. The upper end of the range includes programmability in the basic instrument. At the lower end, there is monitoring capability only. As the price goes up, capability increases to include both monitor and simulation modes, plus storage cassettes to record longer periods of channel operation.

Other levels of expense involved in data communication testing center around facilities and personnel. For a simple point-to-point uncomplicated system, a data communications specialist may not be needed. As the network grows in sophistication, it will become necessary to add a resident technician and eventually a data communications staff.

In determining the actual cost of a system, the major factor should be the costs involved in the event of a system failure. Where downtime of several hours or days results in no serious loss of revenue, only a small investment in equipment is needed. However, many systems, such as airline reservation, bank charge card, and the like, start incurring heavy losses for each second of outage. Here a considerable investment in a data communications service facility, with a full range of test instruments, and redundant communications equipment and channels, becomes profitable.

The Future

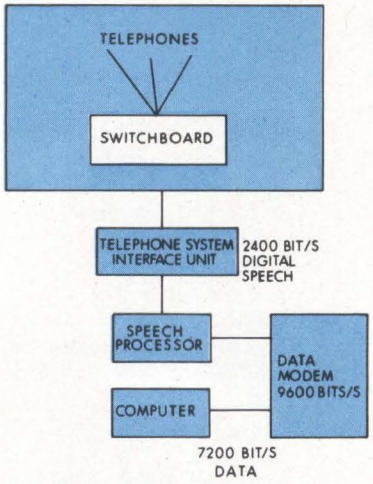
In the area of test equipment, more measurement capability for the dollar can be expected. Instruments will become programmable, be more interactive, and provide more prompting to the operator, allowing sophisticated tests on a complex network to be performed by less experienced personnel. While there is little pressure to combine digital, analog, and protocol testing in one instrument, it is reasonable to expect that programmable versions of these instruments might be combined in service and control centers for more efficient testing and system operation.

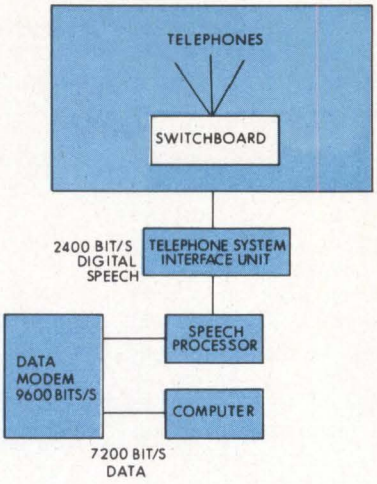
Overall, there is a dynamic growth in the need to move data quickly and accurately from point to point. Capabilities offered by public and private carriers, as well as by equipment manufacturers, are expanding to meet this challenge. Technical advances continue to offer new techniques and opportunities to meet communications needs. It is important that the expertise and facilities required to take advantage of these opportunities be maintained.

Bibliography

Bell System Technical References. Pub 41004: Data Communications Using Voiceband Private Line Channels. Pub 41008: Analog Parameters Affecting Voiceband Data Transmission—Description of Parameter. Pub 41009: Transmission Parameters Affecting Voiceband Data Transmission—Measuring Techniques. Order from: AT&T, Supervisor Information Distribution Center, 195 Broadway, Rm 208, New York, NY 10007. Price, $1.50 each.

Speech Processor Provides Simultaneous Transmission of Voice and Data on Same Channel





E-Systems LPC-24 speech processor converts audio input from telephones to 2400-bit/s digital speech for transmission simultaneously with computer data. Linear predictive coding techniques are enhanced by microprocessor control

Simultaneous transmission of digitized speech and data over the same channel is implemented by the LPC-24 speech processor through use of linear predictive coding (LPC). Telephone speech, presented to the network in a 2400-bit/s synchronized serial data stream, is multiplexed with computer data over a common circuit.

In operation (see block diagram), audio input from a conventional telephone, received through a switchboard, is sampled and analyzed in the speech processor by LPC techniques. The resultant output is a synchronous, 2400-bit/s data stream that can be manipulated in the same manner as any other data and is compatible with an RS-232 or MIL-STD-188 interface. This bit stream is fed via a modem into the satellite or telephone line circuit to a comparable modem at a remote location. There the 2400-bit/s stream is reconverted to audio form by another speech processor.

Depending on particular system implementation, digital voice can be applied in 2400-bit/s increments. For example, 9600-bit/s data are transmitted during non-overlapping working hours. Then the data are idled for the overlapping period to allow voice transmission. Application of digital voice in 2400-bit/s increments allows the data network to handle up to 7200-bit/s data and a single channel of digital voice simultaneously without idling data transmission equipment and personnel.

Speech quality remains constant, with a claimed high level of speaker recognition and intelligibility. A microprocessor-controlled voice operated gain automatically adjusts input audio. Advanced Micro Devices 2900 series microprocessors also perform the LPC techniques and are used in troubleshooting to isolate faults to PC card level.

Physical characteristics of the speech processor—made by E-Systems Inc, PO Box 226118, Dallas, TX 75266—include: size, 7 x 17 or 19 x 18″ (17.8 x 43.2 or 48.3 x 45.7 cm); weight, 36 lb (16 kg); and power, 100 W, 115/230 Vac + 10%, 47 to 63 Hz. Operating temperature range is 0 to 100 °F ambient (−18 to 38 °C), and storage temperature range is −40 to 160 °F (−40 to 71 °C).

Circle 400 on Inquiry Card

Network Processors Provide Ascending Levels of Processing Functions

A 5-member family of single and multiple data communications processors for networks of varying complexities has been introduced by Raytheon Data Systems Co, 1415 Boston-Providence Tpk, Norwood, MA 02062. Major features of the Raynet™ processors—depending on model—include line concentration, network control, virtual terminal support, and node-to-node communication.

Through line concentration, costs are lowered by reducing the number of lines required between operator terminals and host mainframe computers. Terminals installed "downline" communicate with these processors via low to medium speed lines, and messages are then transmitted from the processors to the mainframe over higher speed lines.

Network control can be maintained by using the processors to turn individual communications lines or communications controllers on and off. In addition, the processors can provide error counts and other network management statistics.

Instead of being dedicated to a single host under a single discipline, terminals now can transmit messages to as many as eight host mainframe computers under a variety of communications line disciplines. This

The Paper Tiger™ is here.

The Paper Tiger sets a new standard for low-cost impact printers. More capability. More versatility. For just $995.

You get a full upper and lower case 96-character set. Eight software-selectable character sizes. Plain paper, multiple copies. Forms length control. Parallel and serial interfaces. Multiple line buffer. Tractor feed. Automatic re-inking. 80 and 132 columns.

It's all standard with the Paper Tiger.

Unbeatable capability.

The Paper Tiger prints just about any paper form you need. From address labels to multicopy invoices and legal-size reports.

Adjust the tractor width from 1-3/4 to 9-1/2 inches. Choose from 8 switch-selectable forms lengths. Print 6 or 8 lines per inch.

Unmatched versatility.

Want graphics? Add the Paper Tiger's software-selectable full dot plotting graphics. Print illustrations, block letters, charts, graphs, and more.

Need a bigger buffer? The Paper Tiger features an optional 2K-byte memory that holds a full 24-by-80 CRT screen.

Feature \ Printer	Integral Data 440	Tally 1200	Lear-Seigler 300	Texas Instruments 810	Centronics 779-2
96-character ASCII set, upper and lower case	YES	OPTION	YES	OPTION	NO
Software-selectable character sizes	YES	NO	NO	OPTION	NO
Throughput, lines per minute @ 10 char./line @ 132 char./line	 275 42	 100 40	 Data not available	 440 64	 130 21
Parallel and RS-232 serial interfaces standard	YES	NO	NO	NO	NO
CRT screen buffer	OPTION	NO	OPTION	NO	NO
Footprint (W x D = sq. ft.)	1.37	3.45	3.18	3.58	2.44
Weight (lbs.)	20	64	50	55	45
Forms length control	YES	OPTION	YES	OPTION	NO
Full dot plotting graphics	OPTION	NO	NO	NO	NO
Unit Price	$995	$2500	$1995	$1895	$1350

Comparison data from manufacturers' current literature.

And there's more.

The Paper Tiger is small, lightweight, and compact. That's because it's designed especially to work in small computer systems.

And it's built rugged and simple. For high reliability and easy maintenance. Just like the thousands of IDS printers already in the field.

See for yourself.

Check the comparison chart. Find out why this Paper Tiger just set a new standard for low-cost impact printers.

For more information, write or call. We'll send you our free brochure. Integral Data Systems, 14 Tech Circle, Natick, MA 01760. (617) 237-7610.

CIRCLE 10 ON INQUIRY CARD

Integral Data Systems, Inc.

No one portable everyone's needs.

So we built 21.

Everyone's needs are different. Some want the same versatility in the field they get from a bench model in the lab. Others are more concerned about weight. Some require basic performance models at an economical price. Tektronix offers a selection of 21 portable scopes — 15 real-time and 6 storage models — to satisfy just about everyone.

Take your pick. You can't beat our 400 Series when it comes to high performance. Choose from 9 models ranging in bandwidth from 50 MHz to 350 MHz. All under 26 pounds (11.8 kg). Five with an optional DMM and delta time read out.

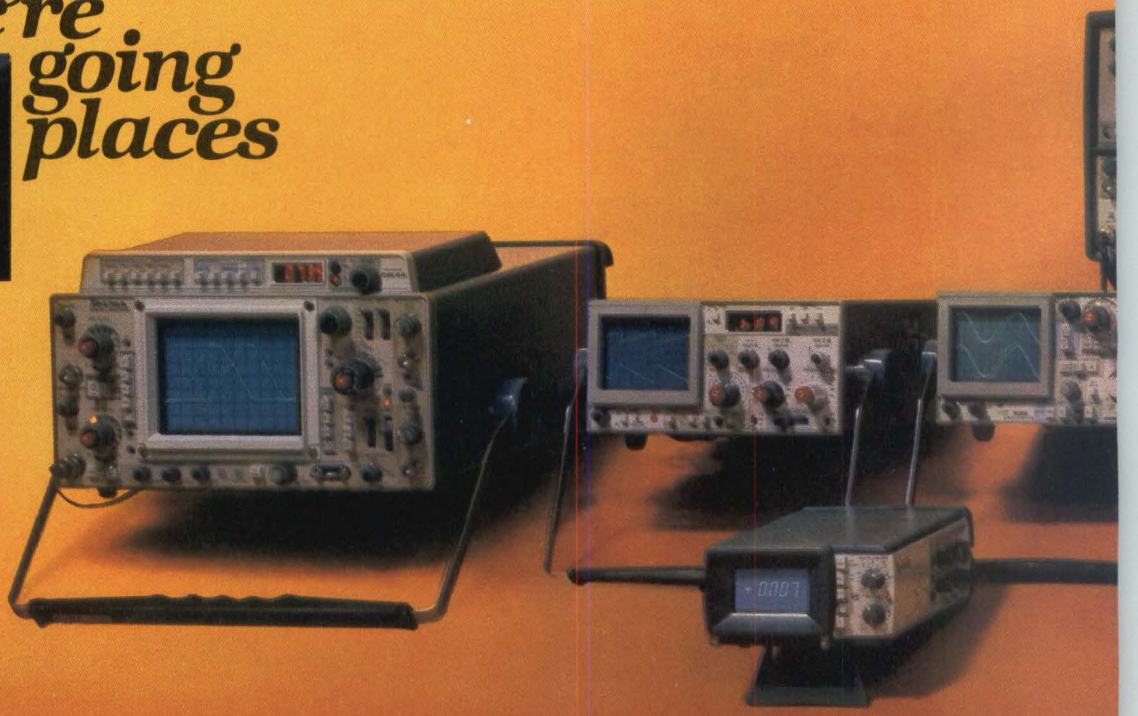
If you're looking for a battery-powered model that fits into a briefcase or toolbox, there's our 200 Series. Bandwidths to 5 MHz. Weights less than 3.7 pounds (1.7 kg).

In between, there's the compact 300 Series, with bandwidths to 35 MHz. Each scope weighs less than 11 pounds (5.0 kg). And finally, we offer the low cost T900 Series, priced from just $795.00*.

Our worldwide service team goes where you go. We're with you all the way, with more than 500 service personnel at 46 Tektronix centers in the U.S.A. and hundreds of Tektronix-supported service engineers in over 50 other countries to calibrate and maintain your Tektronix scope.

So let us show you the model that's right for you. Simply contact your Tektronix Sales Engineer. He'll arrange for a demonstration of our portable or laboratory oscilloscopes. And for our latest portable oscilloscopes brochure, write: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

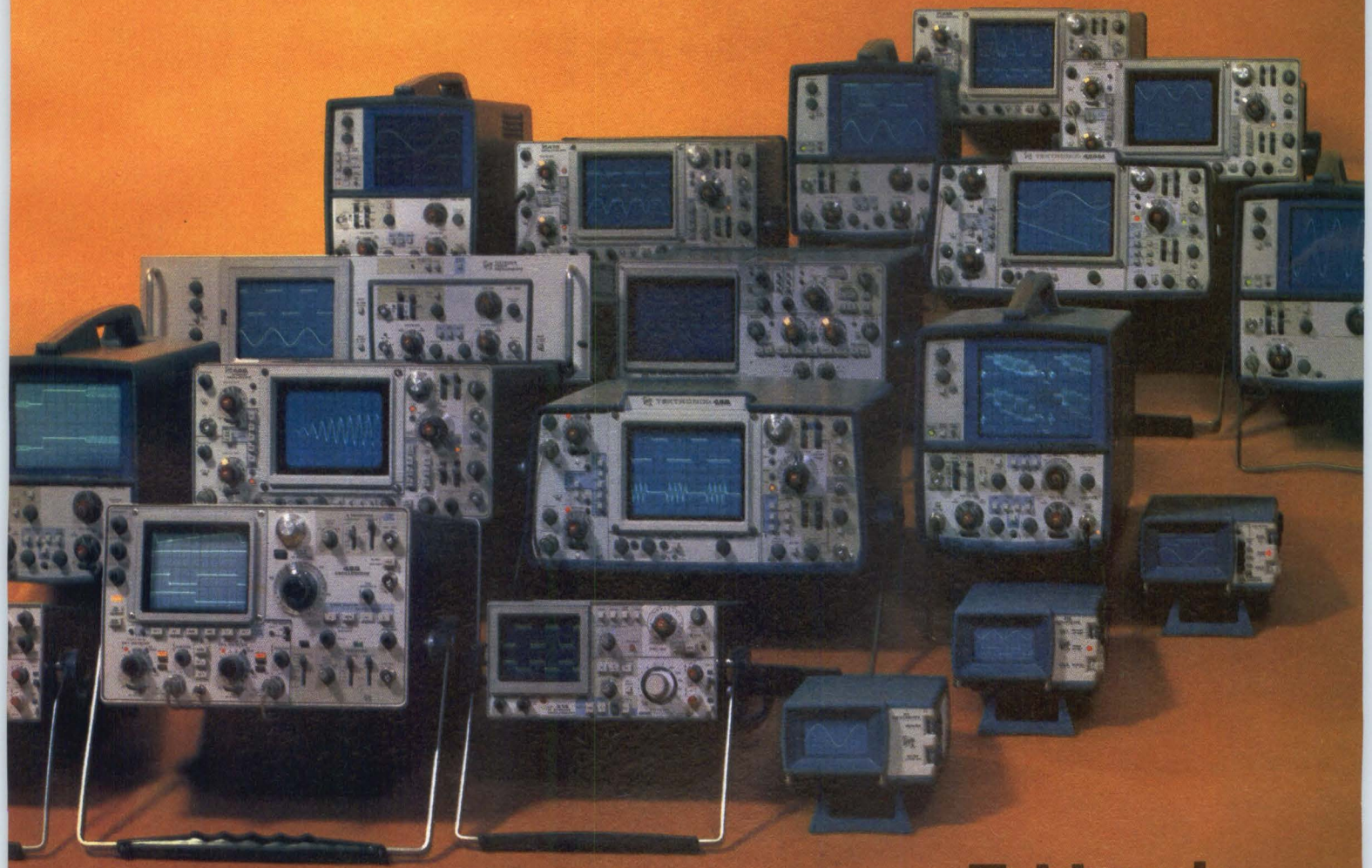
We're going places



scope meets

	Product	Bw	Dual Trace	Delayed Sweep	Fastest Sweep Rate	Other Special Features	Price*
Storage Models	466	100 MHz @ 5 mV/div	yes	yes	5 ns/div	3000 div/μs stored writing speed	$5355
	464	100 MHz @ 5 mV/div	yes	yes	5 ns/div	110 div/μs stored writing speed	4375
	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	3480
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)	2645
	214	500 kHz @ 10 mV/div	yes		1 μs/div	Only 3.5 lbs (1.6 kg)	1595
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	1545
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	5725
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable	3800
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable	3435
	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	2495
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Triservice standard 100-MHz scope	2620
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw	2055
	335	35 MHz @ 10 mV/div	yes	yes	20 ns/div	Only 10.5 lbs (4.8 kg)	2175
	305	5 MHz @ 5 mV/div	yes		0.1 μs/div	Autoranging DMM	1725
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs (1.6 kg)	1190
	213	1 MHz @ 20 mV/div			400 ns/div	DMM/Oscilloscope @ 3.7 lbs (1.7 kg)	1595
	212	500 kHz @ 10 mV/div	yes		1 μs/div	Low cost for dual trace & battery	1190
	T935A	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Delayed sweep and differential	1535
	T932A	35 MHz @ 2 mV/div	yes		10 ns/div	Variable trigger-holdoff and differential	1245
	T922	15 MHz @ 2mV/div	yes		20 ns/div	Low-cost dual-trace scope	975
	T922R	15 MHz @ 2mV/div	yes		20 ns/div	Rackmount version of T922	1345
	T921	15 MHz @ 2mV/div			20 ns/div	Lowest-cost TEKTRONIX Portable	795
Time Interval Readout	DM44	Optional, factory-installed, direct numerical readout of time intervals and DMM functions for the 464, 465, 466, 475 and 475A					445

*U.S. sales prices are F.O.B. Beaverton, OR. For price and availablity outside the United States, please contact the nearest Tektronix Field Office, Distributor or Representative. Prices are subject to change without notice.



Tektronix®
COMMITTED TO EXCELLENCE

For literature please circle # 11

For immediate action, dial our toll free automatic answering service: (800) 547-1512 (In Oregon, collect 694-9051)

For demonstration please circle # 12

For those military systems people
who have been waiting for
a "go-anywhere" twin to the
Data General ECLIPSE® Computer System

Here it is: ROLM's MSE Mil-Spec ECLIPSE Computer System

Now you can have AOS, INFOS®, COBOL, PL/1, DG/L or FORTRAN 5 in any environment. For more information write or call ROLM Corporation, 4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350. In Europe: Meuhlstrasse 19 D-6450, Hanau, Germany, 6181 15011, TWX 4-184-170.

That's Why We're #1 in Mil-Spec Computer Systems

M113A1 Armored Personnel Carrier courtesy FMC Corp.

ROLM MIL-SPEC Computers

ECLIPSE and INFOS are registered trademarks of Data General Corporation.

See our Computer and Telecommunications Products at AFCEA, Washington D.C., June 19-21, Cotillion Room, Booths 421-425.

CIRCLE 13 ON INQUIRY CARD

"virtual terminal" support provides automatic protocol conversion for "host transparency" in mixed protocol networks.

The largest configurations provide node-to-node communication to permit one processor to communicate with another. This is said to simplify design and lower operating costs on large data communications networks.

Raynet-I is a single application PARS or bisync discipline concentrator and network manager for reducing communications lines and relieving host overhead for a single host; -II, also a single discipline unit, can be used with multiple hosts; while -III combines the features of -I and -II to allow mixed protocol terminals to connect to multiple hosts for multiple applications. -IV adds over 1M bytes of local disc storage for store/forward message switching so that messages can be sent from any terminal attached to one processor to other terminals or other processors. -V processors can communicate with up to four other like processors at up to 50k bytes/s and provide internode data switching for geographically distributed mainframes and virtual terminals. Systems are upward compatible.

All configurations can include redundant processors complete with memory, appropriate peripheral devices, and operator consoles, for fail safe operation in highly critical applications. Communications disciplines currently supported include PARS/IPARS for airline passenger reservations applications, bisync (binary synchronous protocol), SDLC (synchronous data link control) protocol, and Univac U-100 protocol. The processors can be configured with an upward-expandable range of disc storage drives, magnetic tape drives, and other peripherals including CRT display/keyboard operator consoles and report printers. COS (communications operating system) software is standard on all configurations.

Circle 401 on Inquiry Card

Processor Developments Increase Speed Three to Four Times

A 16-bit minicomputer—the 1600-02 model II processor—announced by Harris Corp's Data Communications Div, PO Box 400010, Dallas, TX 75240 expands memory of the older -00 processor to 192k bytes and increases speed by three to four times, depending on application. From 1.2M to 1.4M instructions/s can be executed.

The processor is built around a chassis of 20 slots, 8 of which are reserved for processor and memory. Extra slots and larger power supply, 60 or 120 A, enable future expansion. Depending on configuration, the processor is capable of supporting up to two 1200-card/min readers; four 1200-line/min printers; two disc controllers each with a maximum of four cartridge or Winchester-type disc drives; one mag tape controller with up to four 9-track, 1600-bit/in (630/cm) tape drives; one 200-card/min punch; and as many as four concurrent communications channels. Data communications capabilities range up to 9600 bits/s for asynchronous lines and 56k bits/s for synchronous lines.

Existing company software for both 1600 remote batch and distributed data processing systems is compatible. For remote batch systems, the processor will support the memory-resident communications operating system (COS) and a complete

selection of emulation programs which communicate with mainframes manufactured by IBM, Univac, Honeywell, Control Data, Burroughs, Itel, and Amdahl. For distributed data processing systems, the processor supports the disc-resident extended communications operating system (ECOS); REGAL (remote general application language), an interactive programming language; COBOL for local batch operations; key entry processing (KEP), a keystation management system; and FORMAT/10 and FORMAT/41 for keypunch replacement with key-to-disc.

Increased power enables more keystations to be configured, which then allows traditional key-to-disc data entry functions to be executed concurrent with the more sophisticated source document entry method of capturing and processing data at the source. Larger memory and greater speed allows for larger and more flexible configurations of remote batch systems. Higher throughput volumes are achieved by increased line speeds, improved capabilities of peripherals, and the new peripherals supported in a remote batch environment. In addition, a greater number of concurrent communications jobs are possible.

Circle 402 on Inquiry Card

Fourth Earth Station Added To ARPA Network

A contract for the installation and operation of a 5-m earth station at Point Sur, California has been awarded by the Defense Communications Agency to American Satellite Corp (ASC), 20301 Century Blvd, Germantown, MD 20767. The station will be used by the Advanced Research Projects Agency (ARPA) for transmission and reception of high speed data. This installation will be the fourth land-based high speed data earth station placed in operation by ASC for ARPA since 1975. In 1976 ASC also implemented a 4.5-m station aboard a research ship stationed in the Pacific for high speed data communications to the mainland.

ASC also provides nationwide wideband data service in the 3M-bit/s range to the Air Force Meteorological Satellite program as well as data communications services to NASA in support of the space shuttle program, and a wideband secure voice link between California and Hawaii.

Circle 403 on Inquiry Card

X.25 Support Expands Network Interface

Support of the X.25 international standard packet switching protocol by DTSS Inc, 10 Allen St, Hanover, NH 03755 will allow users of that company's systems to connect to any Telenet node. In addition, through a standard X.25 interface, users will be able to access the ACS network planned by AT&T as well as Datapak in Canada and Transpac in France. □

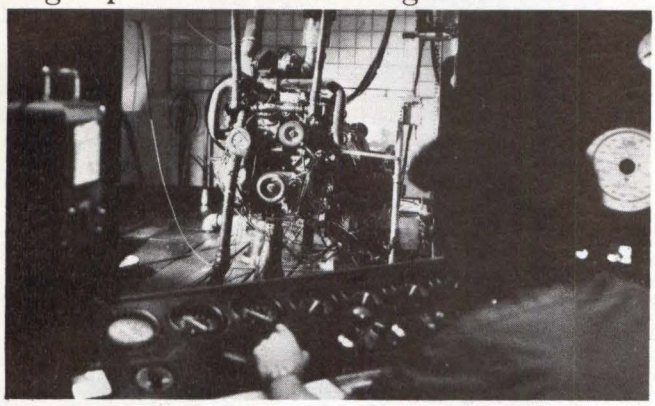
Circle 404 on Inquiry Card

"BEFORE WE COULD BUILD THE WORLD'S LARGEST INDUSTRIAL DATA ACQUISITION SYSTEM, WE NEEDED NETWORK AND SYSTEMS CAPABILITIES WE COULD DEPEND ON."

"ONLY MODCOMP HAD THEM."

Jim Springer, Director of Data Systems,
AVCO Electronics, Huntsville, Ala.

Jim Springer is building what will be the largest industrial data acquisition system in the world. This system will be used for development and testing by one of the world's largest producers of diesel engines.



To implement the system, Jim chose MODCOMP's Classic® Computers, the MAX IV operating and communications system, and the MAXNET IV network extension.

"Network software capability is the key."

"The MAXNET IV network extension integrates all 120 computers in the system. This provides us with the performance characteristics of a stand-alone system, and the economic advantages of network resource sharing.

"In a real-time environment, that's essential."

"MODCOMP gives us the high speed and performance we need — at a cost we can afford."

"The MAX IV operating system is ideal for this type of real-time multi-programming. And with the Classic's extremely fast floating-point processor, we have more than enough speed.

"This is essentially the same system we specified for testing NASA's Space Shuttle. Ordinarily, that kind of superior quality and reliability would be out of reach for industry. But because of their experience with the NASA system, only MODCOMP could meet the assigned high performance levels at a cost industry can afford."

"MODCOMP's tougher on their equipment than we are."

"Our customer was concerned about equipment reliability in their plant. And with good reason. The temperature can get as high as 120 degrees. But we've seen the Classic perform in worse places. MODCOMP's 'hot room' test facility, for instance. That's 132 degrees."

"Obviously we have a lot of faith in MODCOMP."

"We're just in the first phase of this system. But we have to know that, say, 3 years from now, the hardware will be available and that the software can be implemented or interchanged as needed.

"We recommend MODCOMP because we have a lot of faith in them. In their company, their equipment and their service.

"We know they can deliver. It's as simple as that."

At MODCOMP, we specialize in building real time computer systems and the network software capability to make them work.

Easily. Reliably. Affordably. And with the kind of performance you'd expect to find in the world's largest industrial data acquisition system.

If that's what you're looking for from a computer system supplier, do what Jim Springer did. Call MODCOMP.

MODCOMP
Dedicated to your success

Modular Computer Systems, Inc.
1650 McNab Road, Ft. Lauderdale, FL 33309
(305) 974-1380

Sales offices: Atlanta, GA • Boston, MA • Chicago, IL • Cincinnati, OH • Dallas, TX • Denver, CO • Detroit, MI • Hartford, CT • Houston, TX • Los Angeles, CA • Clark, NJ • Orlando, FL • Pittsburgh, PA • San Jose, CA • Washington, DC

CIRCLE 16 ON INQUIRY CARD

TECHNOLOGY AND ECONOMICS: IC POWER DISSIPATION VS PRICE

Montgomery Phister, Jr
Systems Consulting
Santa Monica, California

As component technology has evolved, system power requirements have changed markedly. Early small scale integrated circuits required about one-third the power of discrete silicon circuits, and medium- and large-scale integrated circuits continue to display increasing reductions in power requirements per gate.

This reduction occurs because circuits internal to the device require little power, and device power requirements tend to be proportional to the number of internal circuits that are connected to output pins rather than to the total number of circuits. The relationship that exists between device cost and power requirements on one hand and circuit complexity on the other can be useful to the designer is evaluating design tradeoffs.

Gate/Flip-Flop Relationships

Fig 1 shows the distribution of gates and flip-flops over a sample of 38 medium-scale integrated (MSI) circuits.* The average circuit (from this 38-circuit sample) contained about 2.7 flip-flops and 22 gates. The solid line, having the equation $g = 24.4 - f$, best represents the flip-flop/gate relationship for this sample.

Forty-two small-scale integrated (SSI) circuits were analyzed in a similar way, with the result shown in the lower left corner of the figure. The average circuit in this sample contained 3.5 gates and almost 0.3 flip-flops, and can be represented by the solid line $g = 4 - 2f$.

If an average system designed using these elements has 17 gates for every flip-flop, system characteristics lie on the dotted line in Fig 1. Such systems clearly must have a preponderance of gate-only circuits—circuits containing flip-flops fall far above the "average" line.

Power and Price/Gate Relationships

Fig 2 shows price vs number of gates for the sample of standard circuits (solid lines), and for a smaller sample of low power Schottky circuits (dotted line). The equations were derived from least-squares fits to mid-1978 prices. The deviation of actual prices from the equations is large—it averages 41¢, for example, for the "standard MSI" sample.

*The sample from which the equations used to generate Figs 1 to 3 were derived includes the following 74xx and 74xxx parts: Standard SSI—7400-11, -13, -14, -16, -17, -20, -23, -25, -26, -27, -30, -32, -37, -38, -40, -50, -51, -53, -54, -60, -70, -72, -73, -74, -76, -86, -107, -109, -125, -126, and -132; Standard MSI—7441-42, -45, -46, -48, -75, -83, -85, -90, -91, -95, -96, -147, -148, -150, -151A, -153, -154, -155, -157, -160A, -164, -165, -166, -173, -174, -175, -180, -181, -182, -190, -191, -194, -195, -196, -198, -199, and -251; Low Power Schottky SSI—7400-02, -03, -04, -05, -08, -10, -13, -14, -20, -26, -27, -30, -32, -40, -51, -73, -74, -76, -86, -107, and -132; and Low Power Schottky MSI—7475-83, -90, -95, -96, -151, -153, -157, -164, -181, -190, -191, -194, and -195.

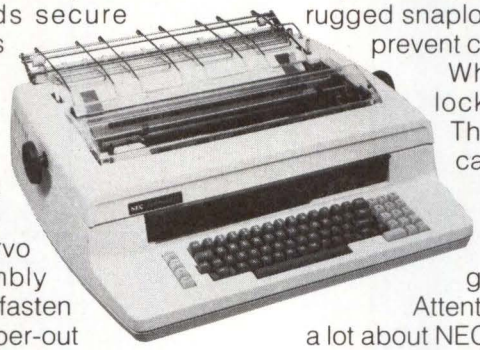
The NEC Snaplock.

A rugged little extra that makes printers more reliable.

Raise the cover of most printers and you'll find retainers that keep circuit boards secure in their connectors. NEC printers have board retainers too.

But they also have more than two dozen other locks and holddowns—far more than competitive printers.

Snaplocks, for example. NEC Spinwriter™ and Trimliner™ printers have at least 16. Six to secure servo and stepping motors, head assembly and control panel cables. Ten more to fasten the driver board, voltage regulator, paper-out switch and operator panel power switch cables.



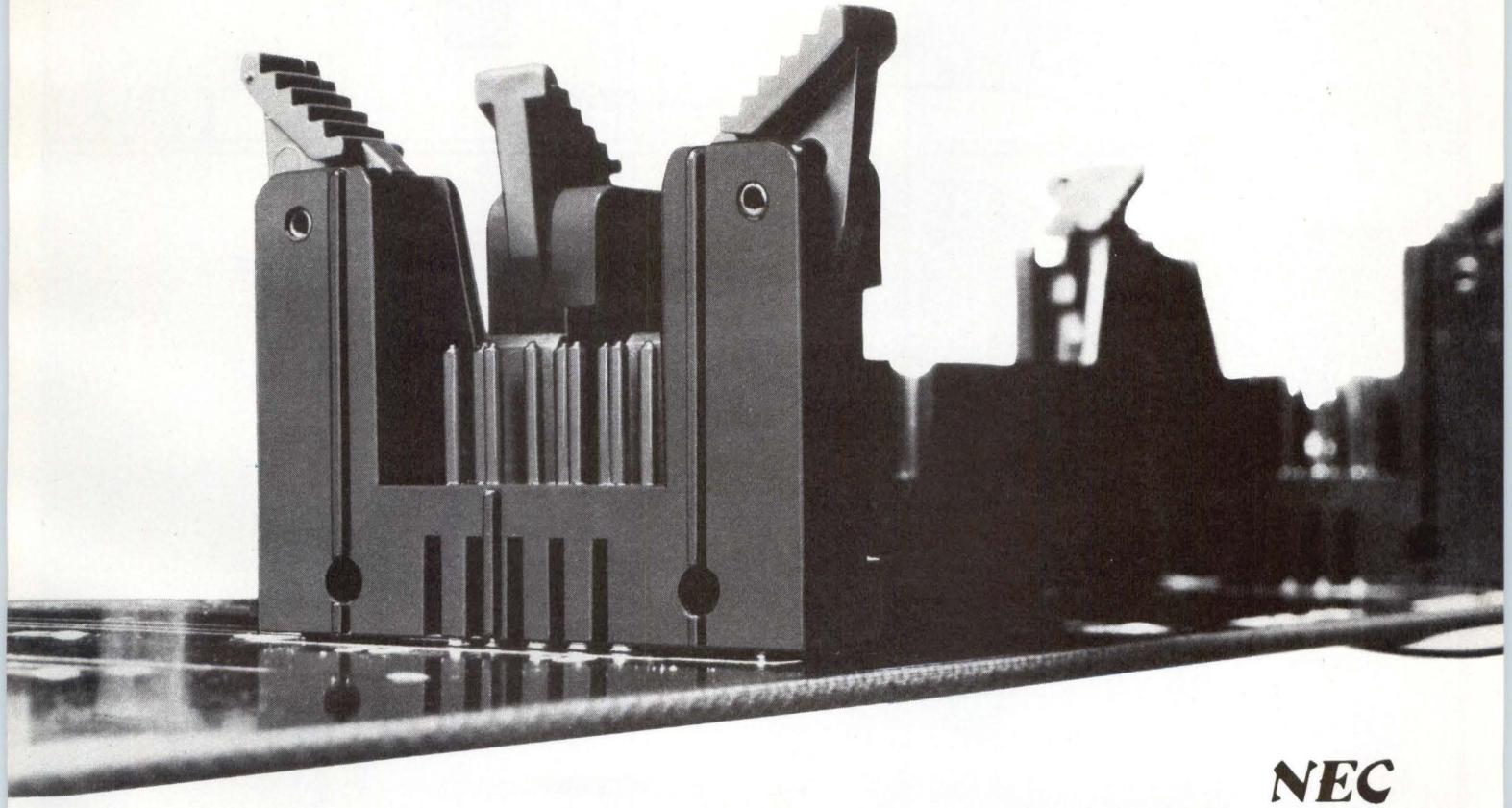
Every cable and wire connection also has its own rugged snaplock. Another 10 cable holddowns prevent cable strain and wire chafing.

What's so good about all these locks and holddowns? Reliability. They keep out the gremlins that cause printers to fail. NEC designs printers with the industry's highest MTBF. And it takes a lot of snaplocks to help us reach that goal.

Attention to the smallest detail. It tells a lot about NEC's motivation.

Send for our new printer brochures.

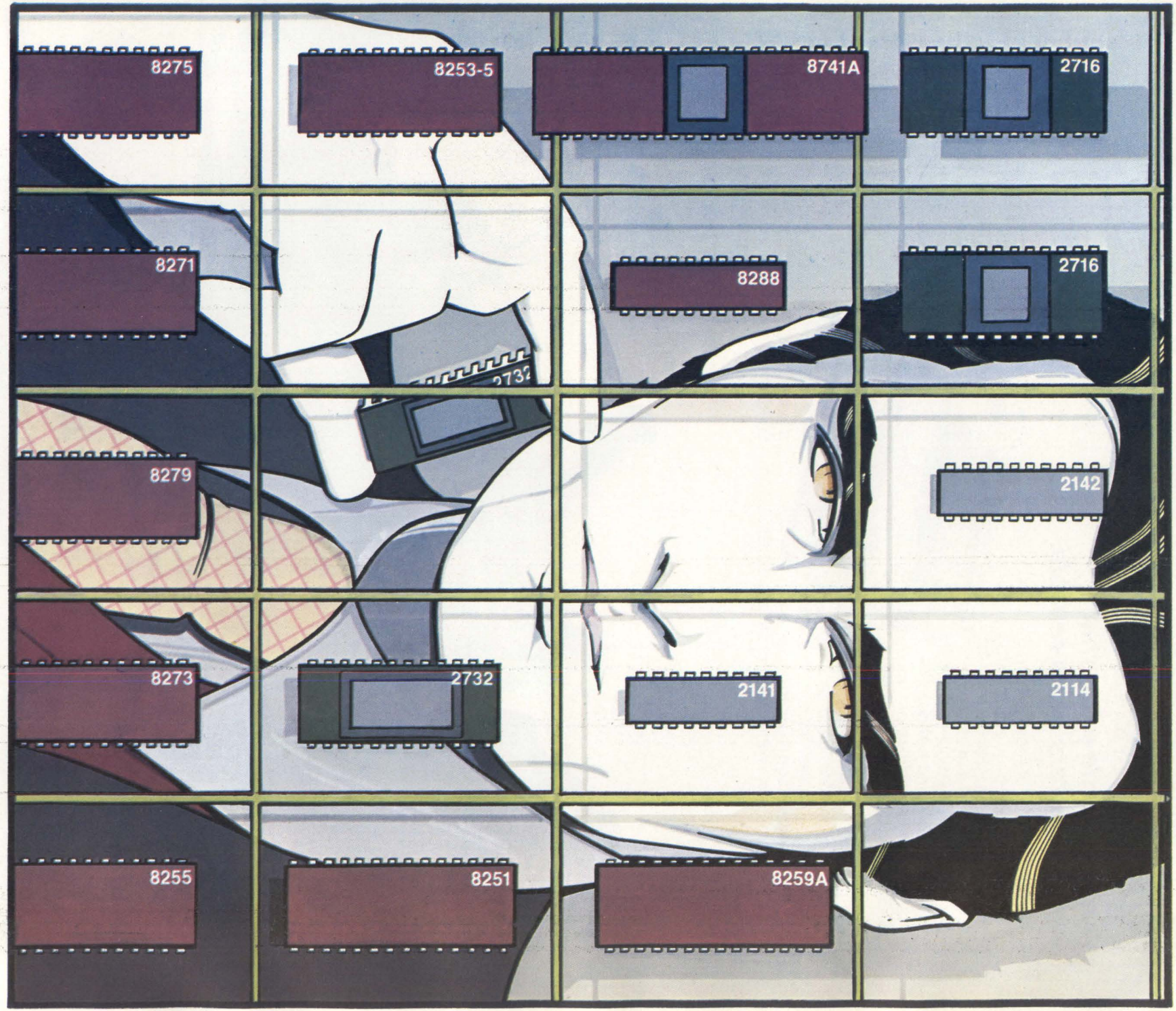
NEC. Going after the perfect printer.



NEC

NEC Information Systems, Inc.

Eastern Office: 5 Militia Drive: Lexington, MA. 02173, (617) 862-3120
Central Office: 3400 South Dixie Drive, Dayton, OH. 45439, (513) 294-6254
West Coast Office: 8939 S. Sepulveda Blvd., Los Angeles, CA. 90045, (213) 670-7346
Southern Office: 2965 Flowers Rd. South, Atlanta, GA. 30341, (404) 458-7014


8275
8253-5
8741A
2716
8271
8288
2716
8279
2142
8273
2732
2141
2114
8255
8251
8259A

8086 System Success.

Intel delivers EPROMs, RAMs and peripherals you need to start building on the Architecture of the Future.

Intel's powerful microprocessor, the 16-bit 8086, gives designers the architectural foundation to create a new generation of microcomputer solutions. The success of these system designs, though, depends on the performance and availability of compatible support components.

We understood this interdependence when, seven years ago, we invented the first microcomputer. At each step since then, our achievements in data memory, program memory and peripherals have anticipated the demands of higher performance microprocessors. Today's 8086 designs can take advantage of our full complement of compatible components to start building the systems of the future without delay.

Our EPROMs exist to support microprocessors

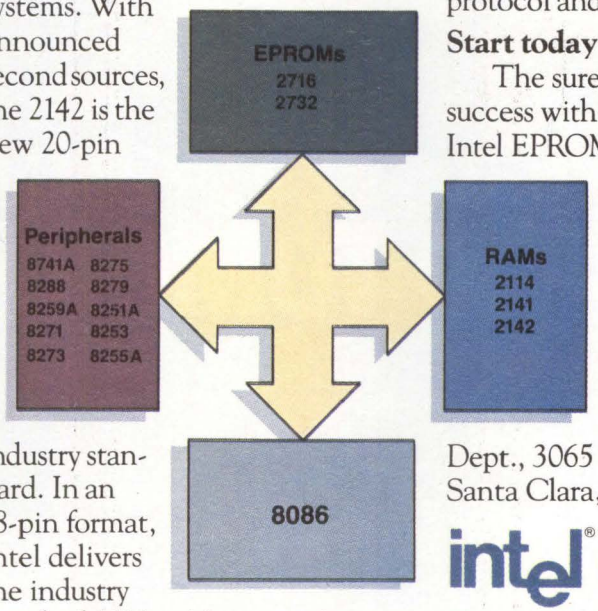
Key to practical microcomputer design is the EPROM. We invented these erasable and reprogrammable memories to make system prototyping faster and simpler. Now that the 8086 has extended the use of microprocessors to more complex data processing, the program flexibility of EPROMs is more important than ever.

Two Intel® EPROMs, the 2716 16K and 2732 32K, are ideal devices for 8086 systems. Both were designed with high speed, 5-volt microprocessors in mind. And they're the only EPROMs that give designers two independent control lines to eliminate the possibility of bus contention in multiplexed and multiprocessor systems.

A RAM for every purpose

Intel delivers a variety of components to meet the data memory requirements of 8086 systems. Whether you're working in shared or multiple memory environments, Intel's family of 5-volt static RAMs gives you a full range of speed and power solutions.

Intel's 2142 (1K x 4), for example, is an ideal RAM for high performance systems. Because it has the same two-line control as our 2716 and 2732 EPROMs, the 2142 also simplifies design in high throughput, multiprocessor systems. With announced second sources, the 2142 is the new 20-pin industry standard. In an 18-pin format, Intel delivers the industry standard 2114, with access times to 200 ns and the proven performance of the most popular 4K RAM ever. For even higher speed and lower power, use our 2141. It's the 4K x 1 bit, high performance HMOS RAM that has speed versions to 120 ns, operating current as low as 40 mA active and standby current of 5 mA.



Building on 16-bit architecture

To get started quickly with 8086 designs, you can take advantage of the family of 28 interface and control components we've developed for Intel industry standard microprocessors. They include intelligent peripheral interfaces for keyboard display, communications devices and general purpose I/O peripherals. Intel controllers give you programmable command over floppy disks, SDLC/HDLC protocol and CRTs.

Start today

The surest path to system success with the 8086 is to specify Intel EPROMs, RAMs and peripherals. They're all here now. For detailed information on any of the above products, contact your local distributor. Or write Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

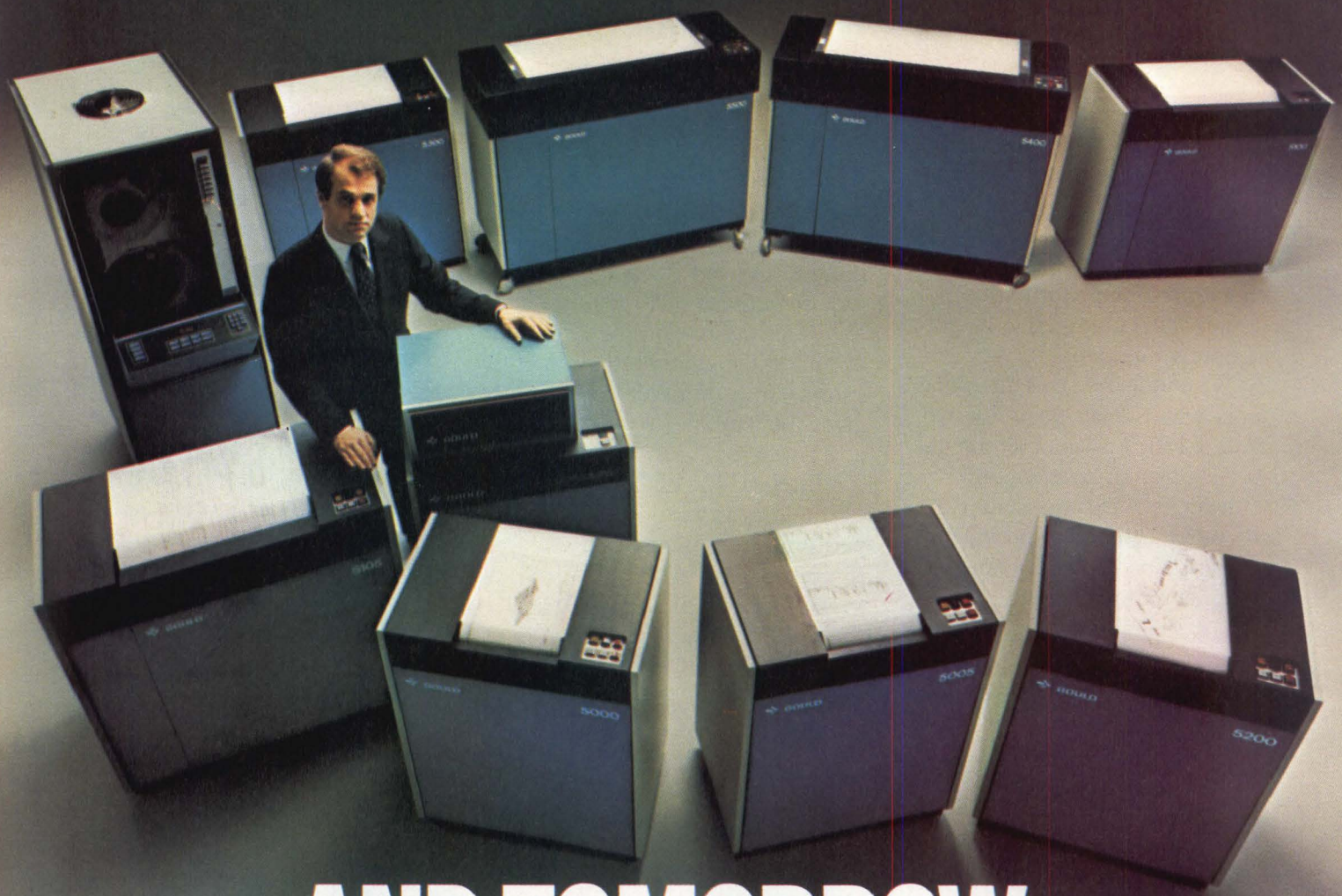
intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

See us at ELECTRO '79, New York City, April 24-26.

CIRCLE 18 FOR INFORMATION

THE BEST WAY TO SOLVE COMPUTER GRAPHICS HARDCOPY PROBLEMS TODAY.



AND TOMORROW.

Electrostatic printer/plotters from Gould. Go ahead, be choosy. Because our 5000 series of electrostatic printer/plotters gives you easy solutions for even your toughest problems. And we're also working right now to satisfy your needs for the future.

Whichever model you choose, you can count on reliability, clear and crisp graphics, high contrast and high resolution. Most models are also UL 478 listed. And even at our high plotting speeds, hardcopy is dry thanks to our exclusive, patented closed loop toning system.

We also make it easy for you in other ways. With software, intelligent and DMA interfaces, on-line, off-line and remote configurations. As well as support of popular computers such as IBM 360/370, PDP-11, HP-2100 and Data General NOVA/ECLIPSE series.

Let us tell you more about our patented designs, exclusive techniques and competitive features that can help solve your problems. For immediate help, call the toll-free number below. Or write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114.

Call toll free for brochure: (800) 325-6400, ext. 77. In Missouri (800) 342-6600.

GOULD

CIRCLE 19 ON INQUIRY CARD

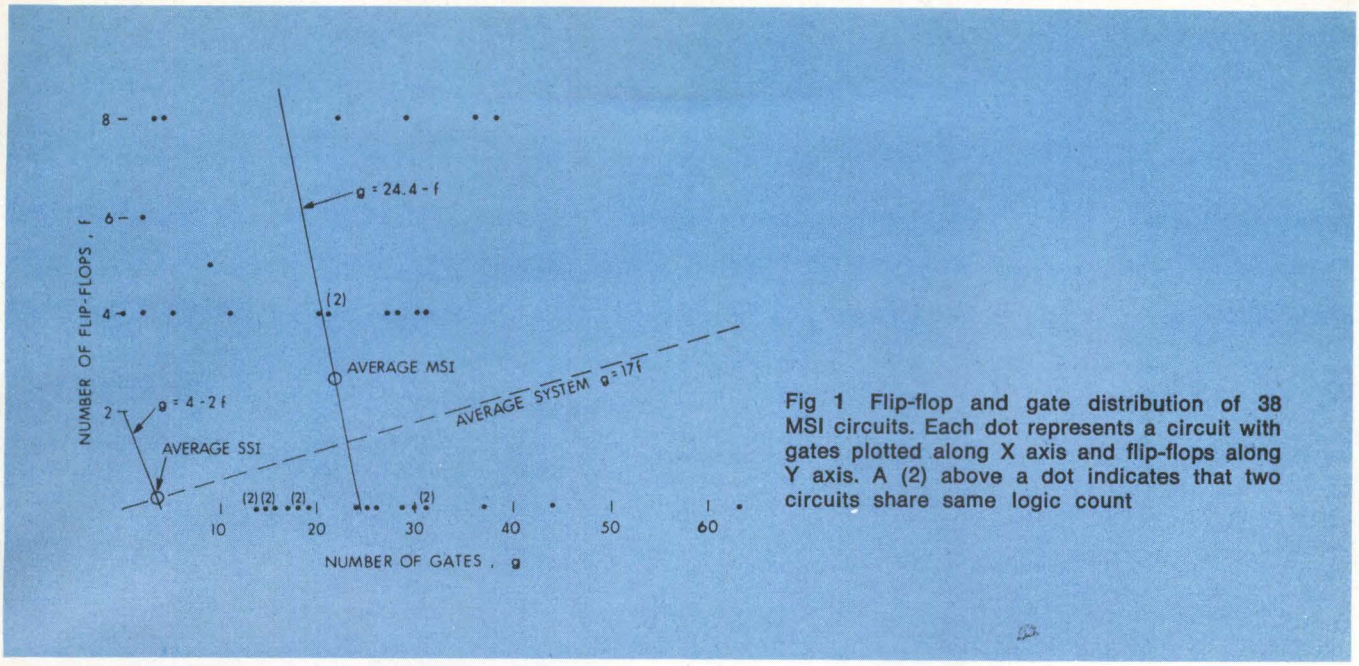


Fig 1 Flip-flop and gate distribution of 38 MSI circuits. Each dot represents a circuit with gates plotted along X axis and flip-flops along Y axis. A (2) above a dot indicates that two circuits share same logic count

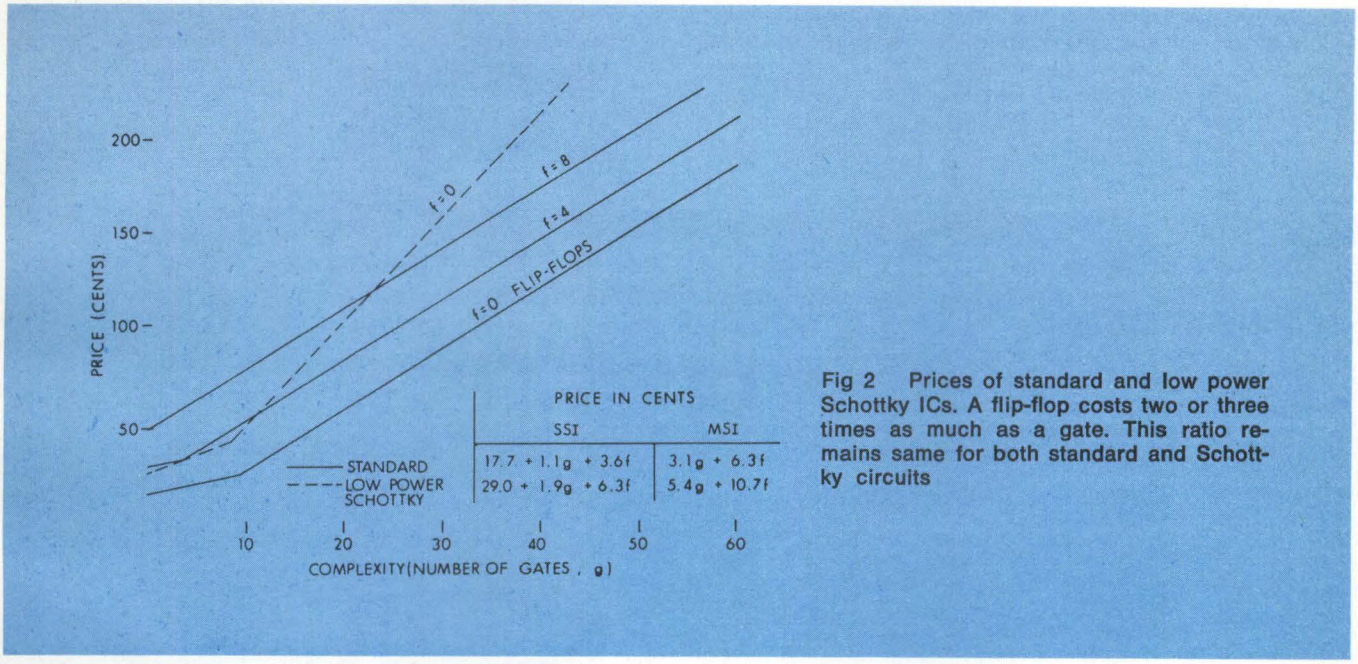


Fig 2 Prices of standard and low power Schottky ICs. A flip-flop costs two or three times as much as a gate. This ratio remains same for both standard and Schottky circuits

"Typical" power dissipation vs number of gates is plotted in Fig 3 for the same samples. Once again the least-squares equations are shown, and the deviations are again large—51 mW for the "standard MSI" sample.

Trading Off Costs and Power Savings

Suppose a module will contain 45 SSI circuits with 9 flip-flops, and 45 MSI circuits with 60 flip-flops. Further, suppose that the module averages 17 gates for each flip-flop. To estimate the cost of the SSI components, using standard circuits, use the appropriate equation from Fig 2.

$$45 \times \left[17.7 + 1.1 \times \frac{17 \times 9}{45} + 3.6 \times \frac{9}{45} \right] = 997¢ = \$9.97$$

In a similar way, cost and power dissipation of the other circuits can be estimated with the following results:

	Standard Circuits		Schottky Circuits	
	Cost	Power (W)	Cost	Power (W)
45 SSI Circuits	$ 9.97	3.04	$16.52	0.66
45 MSI Circuits	35.40	8.61	61.50	2.45
Totals	$45.37	11.65	$78.02	3.11

Note that it costs ($16.52 − 9.97)/(3.04 − 0.66 W) = $2.75/W to reduce power using SSI Schottky devices, and ($61.50 − 35.40)/(8.61 − 2.45 W) = $4.24/W to reduce power using MSI Schottky devices.

Therefore, it appears that the cheapest way to achieve a 20% reduction in module power requirements is to replace all SSI components with Schottky devices. However, in any specific application, the designer will need to examine the relative costs and power savings of both MSI and

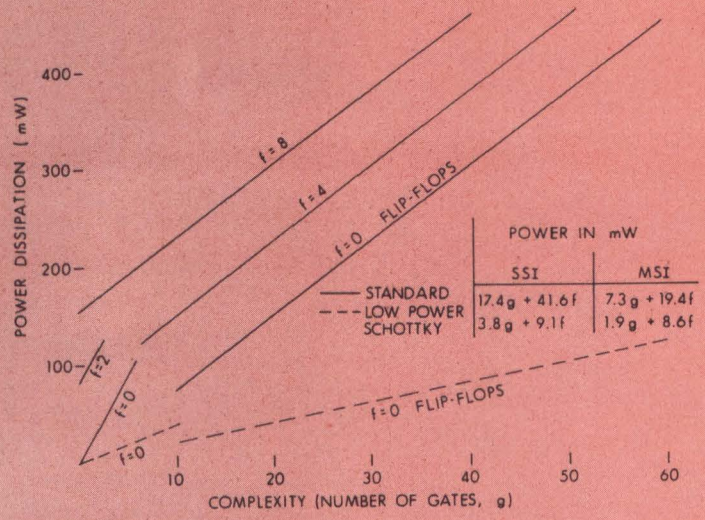


Fig 3 Power dissipations in standard and low power Schottky ICs. SSI Schottky circuits require only about 21% of the power of standard SSI circuits. MSI Schottky devices do not provide as much savings—they require 25 to 45% of the power of standard MSI circuits

SSI ICs, since the incremental cost per watt saved varies widely from one part to another. Furthermore, the designer must consider development, inventory, and other hidden costs, in addition to purchase cost, in making a choice, if the Schottky circuits chosen are not qualified part numbers at his company.

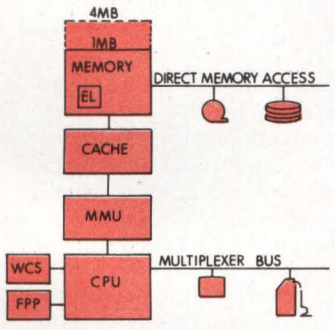
The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—**Ed.**

32-Bit Minicomputer Vies With Competitors In Price/Performance

Model 3220, a full 32-bit microprogrammed minicomputer, priced like a 16-bit machine, is claimed to outperform minicomputers in its price range and to be far lower priced than comparable machines. In this first member of the 3200 series, Perkin-Elmer Corp, Computer Systems Div, 2 Crescent Pl, Oceanport, NJ 07757 has provided full 32-bit architecture, 8M-byte direct memory access bandwidth, four external priority interrupt levels, and memory expansion to 4M bytes of MOS memory.

Directly addressing up to 4M bytes of physical memory, the processor uses 256k-byte MOS memory modules made up of 16k RAM chips. Memory has a 500-ns access cycle time and provides a 20M-byte/s bandwidth in quad-word write mode. Battery backup maintains data for 5 min at 1M byte; extended backup holds 1M byte for 80 min. Eight sets of 16 32-bit wide registers each have four levels of external interrupts. Each interrupt level has an associated register set used during interrupt handling on that level.

The standard instruction set is implemented in 2k words of fixed control store (ROM). The set has been expanded to include a subset of commercial instructions and single and double precision transfer instructions for mixed mode floating point operations.



Directly addressing 4M-bytes memory, Perkin Elmer's microprogrammed 3220 minicomputer has full 32-bit architecture. I/O paths include EMDA bus with 8M-byte/s and multiplexer bus with 400k-byte/s throughput

Error correction performed on full 32-bit words corrects all single bit errors and detects all double and most multiple bit errors. A loader storage unit with watchdog timer loads the automatic boot load program, implemented in 2k-byte P/ROM, into memory. The boot load program checks out memory and certain processor functions before loading the operating system.

An optional cache uses 1k bytes of bipolar memory to provide improved memory cycle time in some applications. With an 80% cache hit ratio, memory access time of 340 ns can be achieved. The direct mapped, write through cache is organized in 64 blocks, each 16 bytes long. Both memory and cache are updated on a memory write if the location written is stored in cache.

Implemented with a multiplexer bus and an extended direct memory access bus, the processor's I/O system supports up to 1023 devices. Slow and medium speed devices connect to the multiplexer bus, while high speed devices attach through the DMA bus. Throughput on the multiplexer bus is 400k bytes/s; the EDMA has an 8M-byte/s throughput rate.

For floating point operations, the optional floating point processor makes 46 instructions available. This option contains eight 32-bit single precision registers and eight 64-bit double precision registers. Available to implement special mathematical or scientific algorithms, an optional 2k words of writable control store can also be used to code FORTRAN or COBOL RTL routines and special functions in microcode.

All software available for previous 32-bit models 7/32 and 8/32 processors operates on the 3220. This includes realtime multitasking OS/32 operating system as well as COBOL, FORTRAN VII, ITC transaction monitor, BASIC, ITAM, and HASP.

A 256k-byte model 3220, including cabinet and power, cache, floating point processor, writable control store, and console, has a price of $46,100. With 512k bytes the price jumps to $55,600, and with 1M bytes to $71,600.

See at NCC Booth 2027

Circle 170 on Inquiry Card

Computer System Altered To Improve Reliability, Add Compactness

A redesigned HP 3000 Series III couples improvements in compactness and reliability with a reduced price. In the system Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304 has incorporated low cost power components and a redesigned system bay to cut costs while increasing system uptime. Performance of previous models is retained.

The system is fully compatible with all software written for previous Series II and III and for Series 33 machines. This compatibility allows the machine to use MPE-III operating system, languages, IMAGE DBMS, utilities, and MFG/3000 manufacturing application software.

Prices for systems now begin at $105,000, a $10,000 drop from former prices. This includes 256k bytes of 16k RAM error correcting memory, 50M-bytes disc storage, 1600-bit/in magnetic tape drive, 16 terminal ports, CRT console, and MPE operating system. This system expands to 2M bytes of memory, 960M-bytes disc storage, 8 tape drives, and 64 terminal ports.

Circle 171 on Inquiry Card

Key to Disc Systems Meet Needs for Productivity and Data Validation

Data entry Systems 3100 and 3200 combine software editing features and operator productivity aids with large storage capacities to meet user demands for data validation capability that does not degrade system throughput. Introduced by Inforex, 21 North Ave, Burlington, MA 01803, the 3100 is aimed at batch editing; the 3200 offloads validation chores from mainframe computers.

System 3100 provides 40k-bytes main memory and 2.5M-bytes disc storage. In addition to expanded program level capacity, it offers the ability to validate entries through comparison with user generated tables. The ability to generate data from tables through customer defined codes reduces key stroke requirements.

A logical upgrade, the 3200 runs 3100 programs with no modification.

It contains 64k-bytes main memory and from 10M- to 40M-bytes disc storage capacity. Provided are COBOL compiler, arithmetic capabilities, and ability to move and edit data continually. All are available as foreground or background tasks.

Both systems support 16 operator stations and various peripheral devices as well as communications options. A typical 3100 with 40k-byte processor, 2.5M-byte disc, tape drive, and eight operator stations sells for $49,240. A 3200 with 64k-byte processor, 10M-byte disc, 45-in/s tape drive, 600 line/min printer, communications interface, and eight operator stations has a tag of $89,630.

Circle 172 on Inquiry Card

Video Terminal Cuts Cost While Expanding Features

Model 1410 video display terminal supplies the advanced features necessary for efficient data entry and inquiry at low cost. Among the attributes of the terminal, available from Hazeltine Corp, Computer Terminal Equipment, Greenlawn, NY 11740, are improved visual performance and a separate numeric keypad to speed entry and reduce errors.

Priced at $580/unit in 1000 quantities, the terminal uses an advanced microprocessor to attain reduced parts count, and increased dependability. Another asset is that the cooling fan has been eliminated through the achievement of significantly cooler operating temperatures. All electronics are contained on a single PC card, eliminating all interconnections except input power and monitor connections.

The unit accommodates all 128 ASCII codes, displaying 64 characters on a 12″ (30.5-cm) diagonal screen. It operates with a standard EIA RS-232 interface and provides eight switch-selectable transmission rates up to 9600 baud.

Characters are formulated using a TV raster scan technique with a 5 x 7 dot matrix character window. Spacing of two dots between characters and three lines between rows produces a legible, well-defined character. Screen capacity is 1920 characters, displayed 80/line on 24 lines. Characters are refreshed at a 60-frame/s rate, noninterlaced.

Circle 184 on Inquiry Card

Minicomputer System Processes and Tabulates Research Survey Data

A turnkey minicomputer system designed to process questionnaire data and perform tabulation functions for market research surveys, TABMASTER™ consists of CPU with disc storage, magnetic tape drive, character printer, video display terminal, and software. Developed by Mnemonics, Inc, 280 Connecticut Ave, Norwalk, CT 06854, the system incorporates MARKETAB™, a survey tabulation system written in FORTRAN.

This system software features three processing phases: clean, tilt, and tabulation formatting. It provides multilevel parenthetical nesting; weighting; filtering; automatic stub alignment; indentation, underscoring, netting, and sorting; and statistical calculations.

System hardware provides a basic 64k-bytes memory capacity on CPU which handles 10M- to 1600M-byte disc storage subsystems. The video display terminal has a 1920-character display and detached 64-character keyboard with 11 programmable function keys. The printer produces hard copy at 30 or 60 char/s. The tape unit stores 6M bytes/tape, operating at 800 bits/in, 75 in/s.

Circle 185 on Inquiry Card

Disc Storage Subsystem Offers Plug Compatibility With Massbus Controller

Disc storage subsystems MSC-05 and -06 are plug compatible replacements for DEC RP-04/05/06 disc drives used on DECsystem-10 and -20, PDP-11 and -11/70, and VAX-11/780 systems. Designed by Microcomputer Systems Corp, 432 Lakeside, Sunnyvale, CA 94086 to avoid the complex engineering implementation of the DEC units, the subsystems can be added to an installation without changes to the operating system.

Architecture of the subsystem centralizes data transfer management functions, rather than using both disc drive control and disc storage control unit circuitry. While both systems perform the same functions, the use of microprocessor control logic provides more efficient execution of functions. As changes are made to the operating system to achieve higher throughput, the disc system will accommodate the changes.

Plug compatibility of the systems with the MASSBUS controllers allows them to be added to an installation without changes to the existing operating system. After the addition disc packs can be interchanged freely between the added drives and RP-04/05/06 units. The subsystems remain compatible when the operating system is upgraded.

All operating system and device level diagnostics are supported with the systems, facilitating maintenance. In addition, extensive inline and off-line subsystem diagnostics have been implemented to test microprocessor control logic as well as drive function. Inline diagnostics may be executed on any attached drive while the others continue normal operations. A front panel diagnostic display on each drive in the subsystem, allows monitoring of registers in the drive register set.

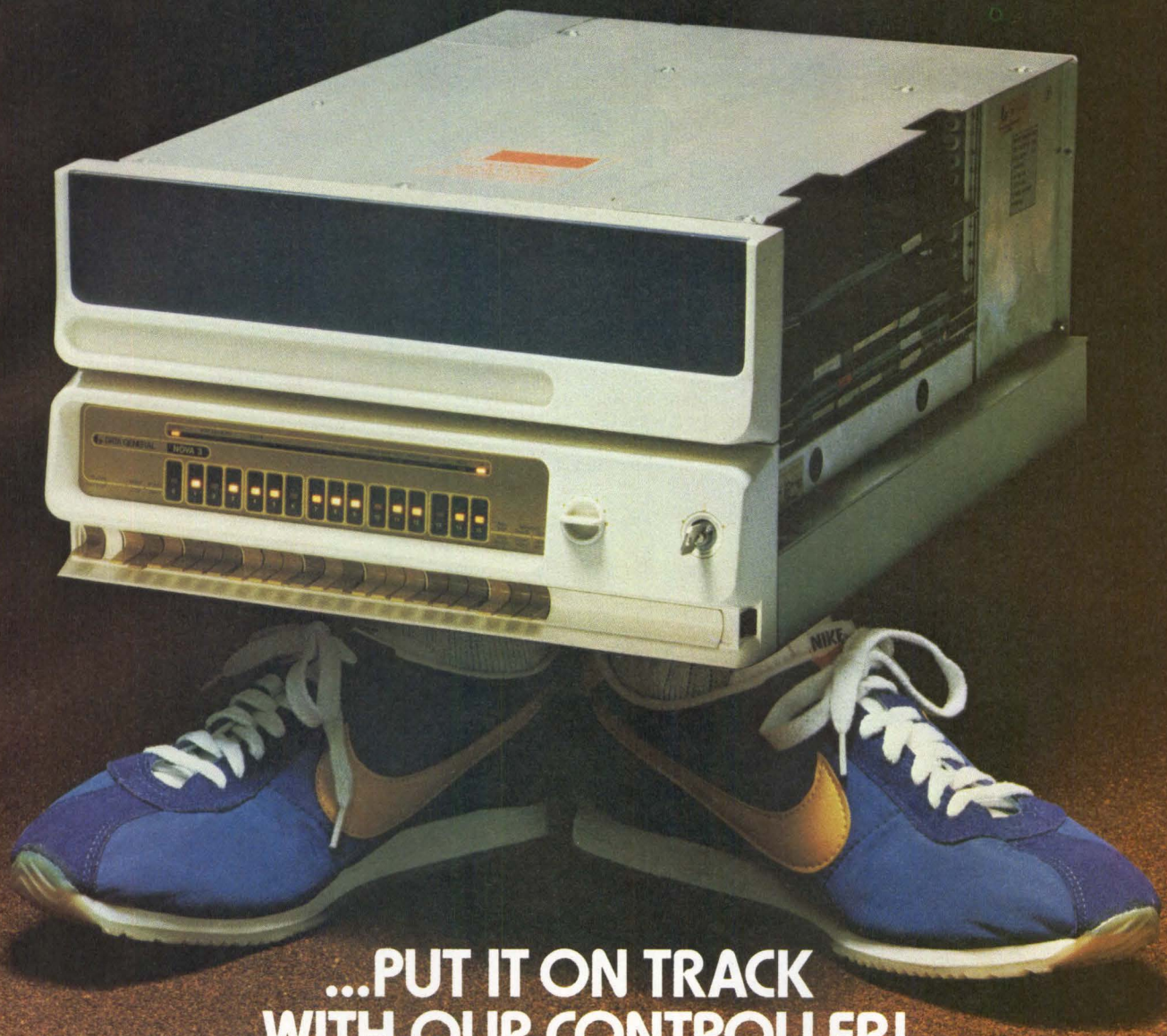
A dual port option to the subsystem permits access by two computers simultaneously. Subsystem operation in dual port mode is functionally transparent to both computers regardless of the number of disc drives attached. The subsystem dual port option supports MASSBUS reservation, request, and interrupt protocols for all drives in the subsystem. More than one subsystem can be attached to the same MASSBUS, providing the potential for dual data paths to multiple drives in a dual port system.

Circle 173 on Inquiry Card

12-MHz Dual Trace Scope Offers 15-mV Sensitivity In Compact Portable Case

A practical 3″ (7.6-cm), 12-MHz oscilloscope, the series 1020 single and double trace scopes provide 15-mV sensitivity, TTL/CMOS operat-

WANT TO SEE YOUR NOVA RUNNING FULL SPEED?



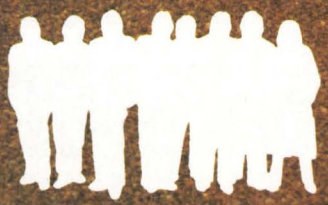
...PUT IT ON TRACK WITH OUR CONTROLLER!

With the revolutionary new Model N6010 Nova Compatible Disc Controller from Quentin Research, your Nova can for the first time perform at its full potential (handling information at the maximum disc speed of 9.67 MHz or 1.2 MBytes per second) and match more expensive computers stride for stride.

By eliminating the "bells and whistles" you probably won't need and don't want to pay for, Quentin's crack team of Advanced Technology Specialists has created the fastest, most efficient controller on the market . . . at a price you can afford, even on a shoestring budget. And they've made it so reliable that we're able to sell it with the industry's only "no strings" Lifetime Guarantee.

But in designing the N6010 for speed, low cost and reliability, we haven't left off the important features: overlap seek, compatibility with RDOS, IRIS, and BLIS/COBOL operating systems, and the capability to interface up to four CDC or other storage module disc drives with any Nova or Eclipse computer.

Call us for more information, or make a date to visit our modern new Research Center and watch the N6010 zip around the track. Find out how we're putting tomorrow's technology into today's computers.

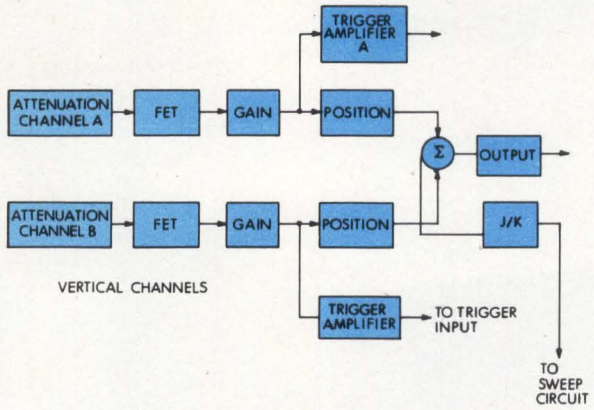


QUENTIN RESEARCH, INC.,
610 Hawaii St.
El Segundo, California 90245
(213) 322-2912

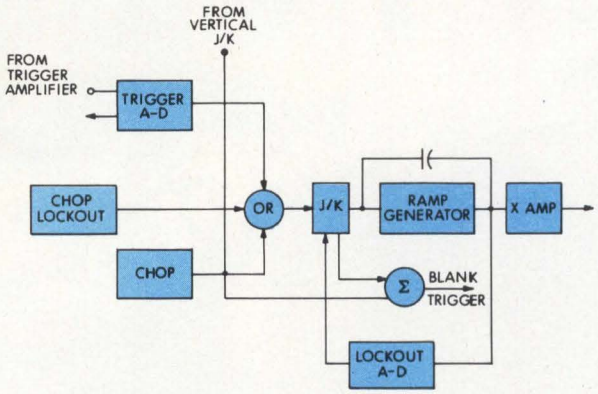
CIRCLE 21 ON INQUIRY CARD

QUENTIN
Research, Inc.

What will they think of next?



Dual vertical deflection amplifier section of Ballantine's miniscope has no appreciable dc drift with time, after a short warmup, and over full voltage range. Temperature drift is only 0.1 division zero shift for full 0 to 50 °C swing



Sweep and trigger circuits in series 1020 are all drift-free digital beyond analog threshold input of trigger binary until sweep generating op amp ramp generator is reached. Unblanking during sweep interval and blanking at all other times lowers power drain, improves available display brightness, and prevents flyback ghosts

ing efficiency, and shock and vibration resistant CRT, along with rugged construction which allows its use in any environment. Measuring 8 x 7.375 x 3.25" (20 x 18.7 x 8.25 cm) and weighing 5 lb (2.25 kg), the unit operates on 12 Vdc at 1 A obtained from battery pack or with plug-in converter from an ac power line.

Sweep rates range from 100 ns to 100 ms/div in 12 calibrated steps plus a continuously variable X10 magnifier. Use of standard TTL and CMOS circuits allows low quiescent current drain and low dissipation in operation. The high light output CRT has a 1-kV accelerating potential to minimize dissipation in the high voltage power supply and CRT control circuits. As a result the unit requires less than 10 W with a nominal temperature rise of only 7 °C, thereby eliminating the need for a cooling fan.

Short length of the CRT provides high immunity to shock and vibration. Its P31 phosphor screen is shaped to a radius that assures constant sharp focus and an integral black graticule minimizes parallax effects. Screen area is 8 x 10 divisions (1 div = 5 mm).

In order to provide all these functions within the package constraints, designers at Ballantine Laboratories Inc, PO Box 97, Boonton, NJ 07005 first minimized internal dissipation by using a high efficiency, high frequency PWM switching regulated power supply fed either by battery dc or by dc from an external line pluggable transformer rectifier module. To prevent conducted emi from entering the instrument, the filter for the transformer rectifier is located in a shielded compartment at the rear of the scope, providing broadband line attenuation for the battery cable circuit.

Selection of a short curved face mono-accelerator CRT met the size constraints and provided vibration and shock resistance, and a sharp round spot that stays in focus because of the uniformity of the glass face. To obtain a bright trace a 1-kV total accelerating supply is used with a much higher beam current that is concentrated into a small controlled spot. Screening the graticule directly onto the CRT's face virtually eliminates graticule-parallax errors or distractions.

In operation there is no beam searching. If there is nothing to trigger on an automatic bright line sweep trigger allows positioning of the traces. To add speed and simplify use an extra section on the sweep rate selector switch makes the transition from chopped to alternate mode automatic. Logical crossover from chopped to alternate is at 1 ms/div. Trigger sensitivity is 0.25 div, dc to 5 MHz and 0.5 div, 5 to 10 MHz internal; and 100 mV rms, dc to 5 MHz and 150 mV rms, 5 to 10 MHz external. The unit can synchronize on a glitch that is equivalent to a 20-MHz, 2-mV signal, as easily as it can on the leading edge of a 2-MHz clock. Accuracy is ±3%.

The unit is capable of operating from 0 to 50 °C; in transit or storage it survives −55 to 75 °C ranges. While not explosion proof by UL standards it is dust and dirt proof in use and will operate dependably at altitudes to 10,000 ft (3 km) without corona or arcing. The durable case can withstand rough handling, and yet is light enough to be hung from a neck strap. Since no ac voltage enters the unit it can be safely operated from this position.

Circle 174 on Inquiry Card

WHO CAN MEET YOUR GREATEST NEEDS IN D SUBMINIATURES?

ITT CANNON CAN!

THE CANNON® D SUBMINIATURE CONNECTOR STORE KEEPS GROWING.

CANNON connector shipments in the millions. Broad product line is key.

Flash. The ITT Cannon Electric store keeps expanding. In size and product selection. And it's no puzzle to figure out why. Key facts in the news give you the story.

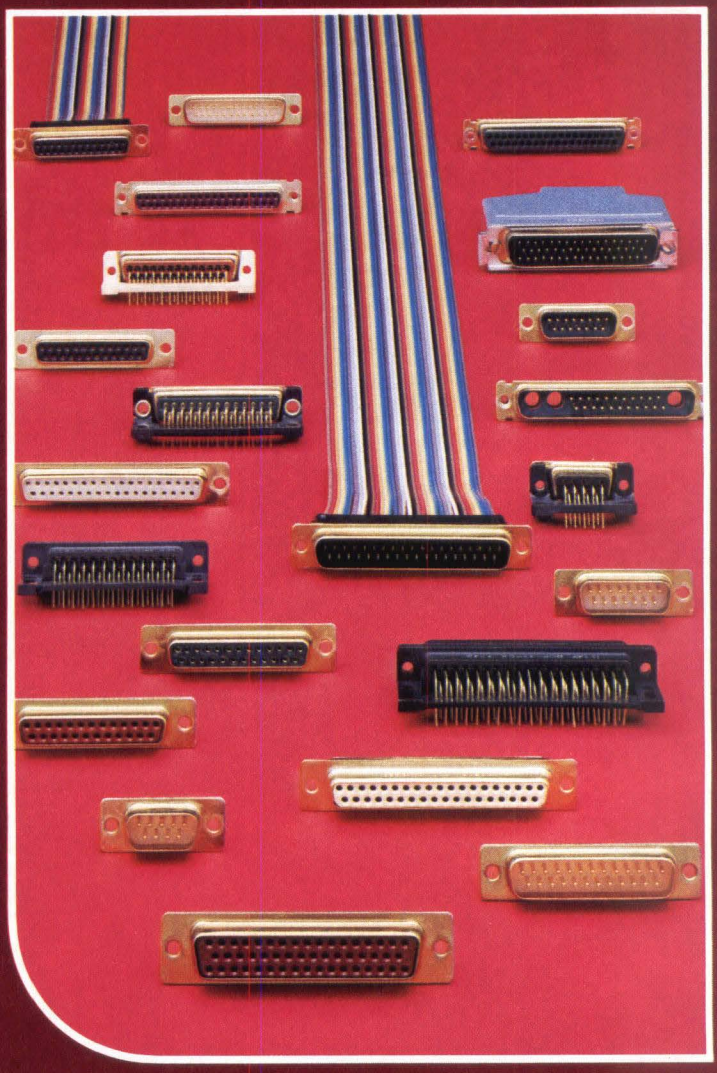
Cannon D Subminiature store thrives for over 60 years. • Millions of connectors and contacts in service worldwide. • Industries served. Military. Automotive. Electronic. Aerospace. Industrial. Commercial. • High quality. High reliability. Meeting the toughest design criteria.

And now the results from page two. Satisfied customers and repeat business for D Subminiature connectors. How can we say that? Again the facts.

ITT Cannon receives numerous customer awards for excellence. • D Subminiatures meet tough job challenges where space and weight are concerns. • All D Subminiature connector types except 2D are fully intermateable. • Each connector can handle up to 50 contacts in standard and twice the density in Double D arrangements. • Available for coaxial, power, high voltage, filter and printed circuit and Wire-Wrap contacts.

These are just the headlines of the Cannon D Subminiature Story. Get the details by writing Cannon. We'll tell you where to write later in this report.

But now, for additional facts, tune into the rest of the ITT Cannon Story. Beginning with the product line summary. An availability report. And a technical support feature. You'll see why when it comes to D Subminiature connectors...ITT Cannon's got it!

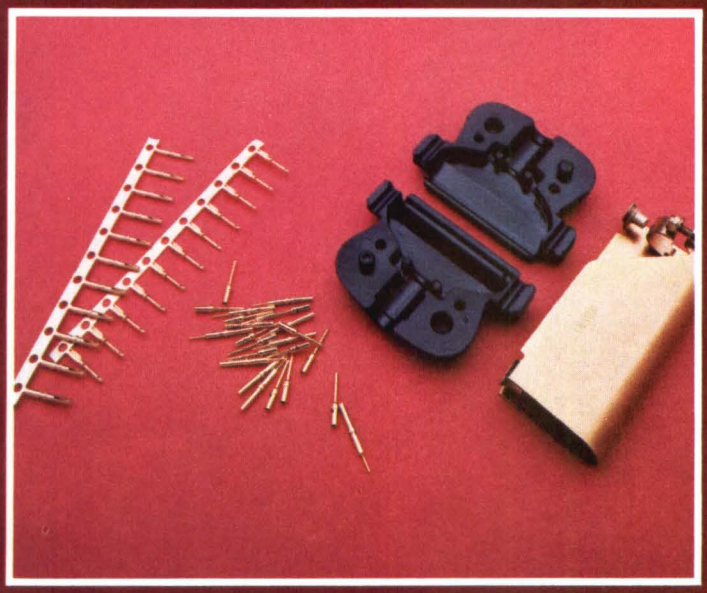


PRODUCT LINE SUMMARY

SERIES	DESCRIPTION	DESIGNATION	INSULATORS	CONTACTS
D*	D Subminiature connector, low cost	ORIGINAL-D	Two-piece white Nylon	Solder, Wire-Wrap† and printed circuit.
D*C	D Subminiature connector, low-cost for commercial applications	BURGUN-D (Mark IV)	Two-piece, burgundy glass-filled Nylon	Crimp snap-in rear release and printed circuit. Plastic cone retention.
D*U	Flame-retardant D Subminiature	BURGUN-D (Mark IV)	Two-piece, black glass-filled Nylon (UL rated 94V-O)	Crimp snap-in rear release and printed circuit. Plastic cone retention.
D*P	All plastic 90° PCB D Subminiature	BURGUN-D (Mark IV)	Black glass-reinforced thermoplastic. (UL rated 94V-O) (flame retardant)	Stamped printed circuit.
D*M	D Subminiature connector for more critical applications conforms to MIL-C-24308	GOLDEN-D (Mark I)	Monobloc, dark green. Diallylphthalate glass-filled	Solder, printed circuit. Wire-Wrap† coaxial, high power and high voltage.
D*MA	D Subminiature with LITTLE CAESAR* contact retention system conforms to MIL-C-24308	ROYAL-D (Mark III)	Monobloc, dark green. Diallylphthalate glass-filled	Crimp snap-in rear release coaxial and/or high voltage.

†Wire-Wrap is a registered trademark of Gardner Denver Corp.

SERIES	DESCRIPTION	DESIGNATION	INSULATORS	CONTACTS
D*SP	Mass Terminated D Subminiature pin and socket connector	MAS/TER™-D (Mark V)	Black glass-reinforced thermoplastic, UL rated 94V-O (flame-retardant)	Non-removable insulation displacement termination.
2D*	D connectors with double the density of crimp snap-in contacts in monobloc insulators in a standard D shell	DOUBLE DENSITY D	Monobloc, glass-filled nylon, dark green	Crimp snap-in rear release.
D*H	Hermetically-sealed D connectors for applications with extreme pressure differential	HERMETIC D	Compression glass	Eyelet or solder pot.
D*J	Filter connectors for improved control of radio frequency and electro-magnetic interference	FILTER D	Diallylphthalate	Solder and printed circuit.
D*D	Environmental D connectors, vibration-proof and moisture resistant	ENVIRONMENTAL	Diallylphthalate	Solder non-removable and crimp snap-in rear release.



From sea to shining sea. That says it all about Cannon availability.

And now the story behind the headlines. ITT Cannon worldwide capability is supported by more than 200 distributors. To meet your interconnect requirements fast. When and where you need connectors.

In the United States look to your CAPS® distributors. Cannon Authorized Plug Specialists. They keep a large off-the-shelf inventory of connectors. And operate local assembly centers for your special connectors. All meeting Cannon's strict quality control standards.

It all adds up to fast and easy access to the Cannon storehouse of interconnect products. In quantity. And at competitive prices.

ITT Cannon technical support helps lower total installed cost.

A major part of the ITT Cannon growth story is wrapped up in this simple statement:

Cannon doesn't leave you alone. You get expert technical help from design to installation. The service that's necessary to meet changing requirements and produce cost-effective interconnects.

That goes for termination tooling too. While design people specify connectors, production specialists work up handling systems... putting together the best tooling group for your product. What customer tooling does Cannon provide? Name your job. You get everything from simple hand tools to semi-automatic and fully automatic strip-and-crimp machines. Capable of terminating up to 2400 contacts per hour.

These are just some of the reasons why when it comes to D Subminiature connectors ...ITT Cannon's got it! But the story doesn't end here. For interesting reports on other Cannon rectangular connectors, stick with us. We'll also tell you how to get all the fact-filled reports you need on D Subminiature connectors.

The next report, rack and panel connectors ...just turn the page.

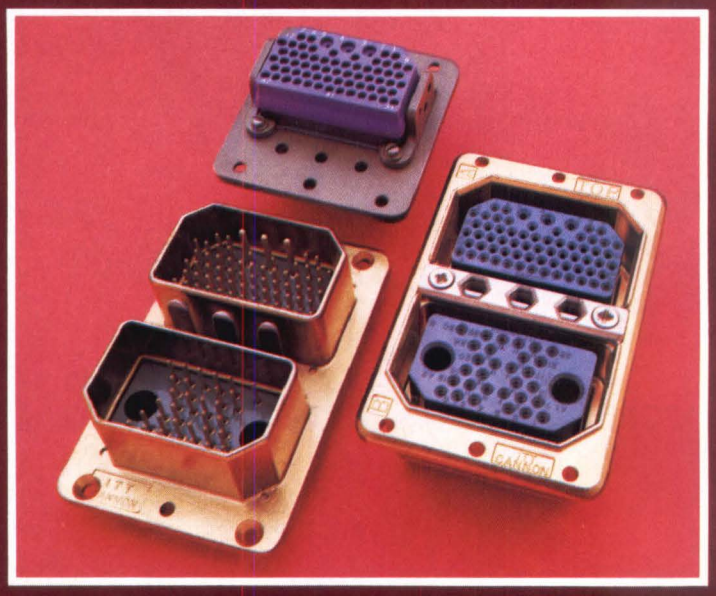
RACK AND PANEL CONNECTORS.

DPK racks up performance in tough environments.

..High performance. MIL-C-83733 qualified.
..Environment resistant. Temperature ranges −65°C to 200°C.
..Sturdy die-cast aluminum alloy construction with nickel finish.
..Insulators made of glass reinforced, thermo set plastic.
..Available in two shell sizes with a variety of mounting configurations.
..13 contact arrangements accommodate 18 to 185 signal contacts. Shielded, coaxial, and filter versions also available.
..Dependable Little Caesar® rear release contact retention system.

DPX helps you gang up on space limitations.

..Your choice of non-environmental or environmental versions.
..Both meet or exceed MIL-C-81659, Revision B.
..Operating temperature ranges from −65°C to 200°C.
..Available in single, 2, 3 and 4 gang configurations.
..12 contact arrangements accommodate sizes of 12, 16, 20 and 22 contacts.
..Coaxial, high power and filter versions available.
..Dependable Little Caesar® rear release contact retention system.



GET THE FULL ITT CANNON STORY.

For more information on the full range of products available from the Cannon D Subminiature Store, write: Marketing Manager, Rectangular Division, ITT Cannon Electric, 666 East Dyer Road, Santa Ana, California 92702. For 24-hour service, call toll-free (800) 854-3573; in California (800) 432-7063. In Canada, contact Marketing Manager, ITT Cannon Electric, Canada, a Division of ITT Industries of Canada Limited, Four Cannon Court, Whitby, Ontario, LIN 5V8. (416) 668-8881.

Six decades on the leading edge of interconnect technology.

CANNON ITT

Modular Terminals Offer Flexibility Through Virtual Machine Design

BMT™ series modular electronic terminals are described as being "based on a virtual machine design that leads to lower overall cost and provides maximum flexibility." The display based MT 200, printer based 300, and user programmable display based 600 terminal systems introduced by Burroughs Corp, Detroit, MI 48232 consist of separately packaged display screens, keyboards, printers, magnetic card readers, and memory subsystems which combine in a variety of ways to meet specific requirements.

Each terminal is built around a microprocessor that can be programmed to drive all terminals in the family. This virtual machine technique eliminates the need for separate controllers and provides cost savings as well as long range protection from equipment obsolescence by allowing future elements to be added to the terminals without software revisions or equipment replacement.

The microprocessor supplies processing intelligence for displays, printers, keyboards, and for application programs, data storage, and peripheral control. It enables terminals to operate online to a host or as independent units for offline applications. Terminals provide a choice of standard data communications protocols, with data transfer rates from 600 to 9600 bits/s.

Another element common to all terminals is an I/O subsystem that acts as interface between the microprocessor and memory and peripheral components. This subsystem contains its own single chip microprocessor and controller.

Preprogrammed display based MT 200 terminals offer a choice of 5, 9, or 12″ (12.7, 22.9, or 30.5-cm) CRT display screens. Each screen has capacity of 15 lines, each up to 40 char long, and features a 96-char ASCII set. The system can be equipped with alpha, numeric, or alphanumeric keyboard.

MT 300 units are based on a 90-char bidirectional matrix printer that offers either 4.5 or 8.5″ (11.4 or 21.6-cm) wide printing format, accepts variable width documents for single line validation, and prints a continuous form journal. Buffered for sustained operation, the unit can print reverse images (white against black) for emphasis. A numeric keyboard with 40-char Self-Scan® display is included.

Versatile standalone systems, MT 600 user programmable display based terminals provide 12″ (30.5-cm) display with capacity for 28 lines of 80 char each and alphanumeric keyboard. Up to 96k bytes of memory is included, and basic arithmetic functions (add, subtract, multiply, divide) plus positive and negative sign values are supplied. The unit offers a microprocessor controlled diskette subsystem that can store up to 160k bytes of data or control instructions.

In an interactive data entry application, the host computer causes a blank form to be displayed on the 600's CRT screen. Data entered through the keyboard are positioned automatically on the screen where they can be verified by the operator prior to transmission to the computer or printer. The unit can also perform forms creation and forms completion programs offline, or can function online as a conventional data entry station.

Circle 175 on Inquiry Card

Processors Capitalize On LSI/Packaging Technology To Raise Speed, Drop Price

Two 4300 series processors announced by IBM Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604 offer increased memory capacity and improved internal performance over comparable intermediate size processors currently in use. While maintaining compatibility with System/370, the 4341 offers 2M characters of main memory and up to 3.2 times the instruction execution speed of a 1M-char model 138. A 4331 with 0.5M-char memory offers four times the execution rate of a model 115 with 64k char at a lower price.

Advanced LSI and packaging technologies used in the processors reduce size and power dissipation. Dense packaging of memory chips and logic chips contributes to reliability and size reduction as well as significantly reducing power, cooling, and space requirements. Power and cooling requirements for the 4331 are said to be 70% less than those of a model 138, allowing the machine to operate in an office environment. The 4341 reduces requirements by about 50% compared to the model 138.

A multichip carrier that holds up to nine LSI logic chips (see *Computer Design*, Jan 1979, pp 170-172) is credited with space savings in the logic package. The module's multilayer ceramic structure and large number of I/O pins permit it to accommodate a large number of logic circuits. Fabricated from up to 23 ceramic layers in which up to 10 m of wiring are deposited during the manufacturing process, to interconnect logic circuits and distribute electrical power, the modules measure either 35 or 50 mm square. The smaller one has 196 I/O connecting pins; the larger has 361 pins.

Improved PC technology, including closer tolerances for circuit wiring and a greater number of internal planes for cards and boards, also plays a part in reducing size of the logic package. Wiring line width is held within a tolerance of ±0.001″ (0.025 mm) to permit precise fabrication of wiring lines. Wiring patterns are formed on thin epoxy glass sheets using both a subtractive etch process and an electroless copper plating process for signal planes. These sheets are lacquered together to form cards and boards. The process allows use of 8 planes in cards and 16 in boards, significantly increasing wiring flexibility. Logic modules are soldered onto the cards, with module pins connecting to wiring on various planes.

Processor memory uses previously announced 64k-bit chips. These chips contain redundant bits to enhance productivity and integrate timing and addressing functions. Two 8-bit high speed buffers on the chip are capable of a 100-ns data rate. This data rate coupled with ability to read 72 chips at one time results in increased memory access speeds.

Density at the module level has been doubled over that of the 8100 and System/38 by stacking two 2.5-cm square ceramic substrates, each holding four 64k-bit chips. Using this module allows more than 0.5M bytes of memory to be obtained on a single 12.4 x 19-cm card.

Each processor is available in two models: the 4331 has 0.5M or 1M

characters of main storage; the 4341 has either 2M or 4M. Both use the 3278 model A display console for operation and maintenance. The 4331 can operate as a standalone unit, linked to other 4300s, or attached to a central System/370. An integrated communications controller eliminates the need for a separate communications controller.

Announced for use on the 4331 processors were 3310 direct access storage providing up to 64.5M char. 3370 direct access storage for both processors offers storage for 571M char with a data transfer rate of 1.859M char/s. Two separate data paths into the 4341 are provided by the 3880 storage control. Central to this unit is an LSI bipolar microcontroller chip that can execute 5M instructions/s and has 94 I/O signal lines, and built-in error detection.

Prices for a 4331 with 0.5M and 1M char of main memory are $65,000 and $72,500, respectively. A 4341 with 2M- or 4M-character memory is priced at $245,000 or $275,000. Deliveries are scheduled for second and fourth quarter of this year, respectively.

Circle 176 on Inquiry Card

Interactive Design System Offers Graphic Networking Capabilities

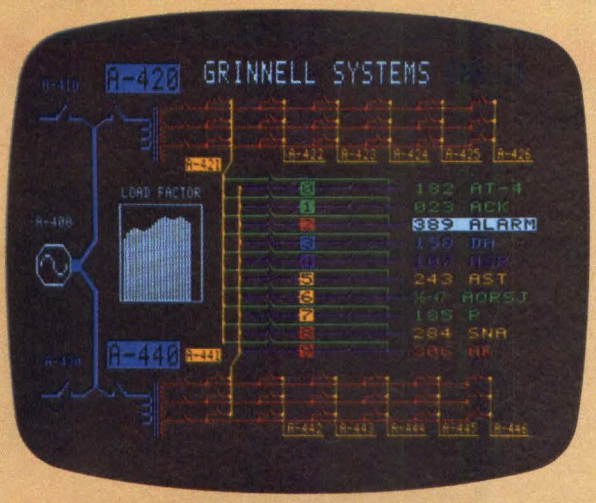
A small graphics system, the Dual Processor System introduced by Gerber Scientific Instrument Co, 83 Gerber Rd, South Windsor, CT 06074 provides production capabilities of interactive design systems, and programming, security and communication features of data management systems to users in computer aided design and manufacturing areas. The system, designed to insure productivity at low cost, provides the advantages of the company's graphic networking architecture in a smaller system. Among these are CAD/CAM capabilities, tutorial user interaction, queued plotting and communications, multiple levels of data file security, automated archiving and backup, distributed process performance and availability, and graphic network expandability.

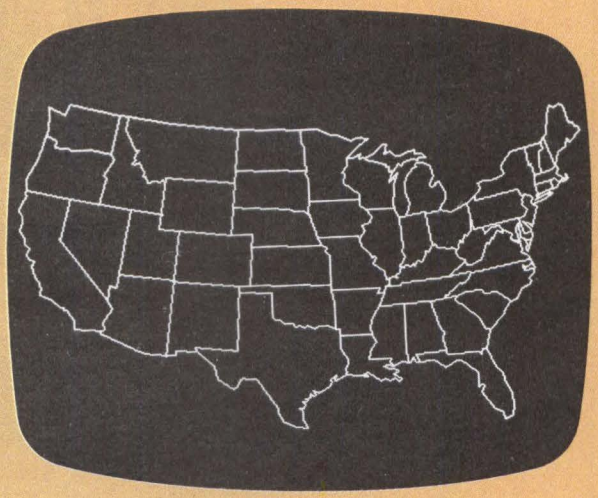
System hardware includes two HP 2113 E series computers with 64k of core memory. The two computers work in parallel to improve throughput. The two processors share a single high performance disc that provides 50M bytes of storage and a 25-ms average seek time. Featuring a fail safe head retraction system that retracts heads in event of a power failure, the disc is driven by a microprocessor based controller which handles access to the disc from both the DMS and IDS computers.

Each system supports up to four graphic workstations and peripheral devices including drafting systems, remote communications options, programming terminals, printers, and magnetic tape units. Systems expand to 2M bytes of main memory and 800M bytes of disc storage.

Circle 177 on Inquiry Card

Grinnell has your display....





from low cost imaging and graphics to full color image processing

Our modular, solid state systems can meet your computer display requirement, easily and economically.

And, they're intelligent. Every system has a complete alphanumerics and graphics package, and a powerful instruction set that simplifies programming—no need for complex macro-instructions and high order programming languages.

There's also a choice of standard resolutions: 256 x 256, 256 x 512, 512 x 512 (30 Hz or 60 Hz refresh) and 1024 x 1024. Plus plug compatible interfaces for most minis.

Options include overlays, function memories, pseudo-color tables, zoom and pan, independent cursors with trackball and joystick controls, split-screen, image toggling, and real time digitizers that grab and store images and sum consecutive frames.

Grinnell displays are already used for tomography, ERTS imaging, process control, image processing, animation and much more. All systems drive standard TV monitors.

So before you choose a display system, let our experts show you how to maximize performance and minimize cost. For details, and/or a quote, call or write.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

CIRCLE 24 ON INQUIRY CARD

"It's As Different From Other Systems As The Steam Shovel Is From The Shovel."

Mark Levi
General Manager, Microcomputer Systems

Starplex™ Development System

"Right now, what's holding back new developments in microprocessing are the existing development systems.

The Starplex System is going to change all that.

And as of this moment, if you're in the business of designing or programming 8080/8085 based products, this is the tool that can make your life infinitely less tedious.

So sophisticated is the Starplex System, it can virtually take you by the hand and walk you through its own operation.

Where other systems require scores of individually typed instructions, the Starplex System can do the same job at one stroke of a key.

Where other systems offer you blood, sweat, and repetition, the Starplex System offers HELP, PAUSE, EDIT, DEBUG, CONTINUE. To name a few of the unique functions on our keypad.

Where other systems leave you fumbling

	STARPLEX	INTEL	TEKTRONIX
SIMPLE KEYSTROKE CONTROLS	EDITOR SYSTEM UTILITIES	NONE	NONE
SYSTEM OPERATING MODES	FORMS OR COMMAND DRIVEN	COMMAND DRIVEN ONLY	COMMAND DRIVEN ONLY
CRT-ORIENTED EDITOR	YES	NO	NO
HIGH LEVEL LANGUAGES	2	2	NONE
ISE CAPABILITY	MULTI-PROCESSOR	SINGLE PROCESSOR	SINGLE PROCESSOR
PROM PROGRAMMER	INTE-GRATED OPTION	SEPARATE	SEPARATE
PRINTER	STANDARD	OPTIONAL	OPTIONAL
TOTAL PRICE (Exclusive of PROM Programmer and ISE)	$13,800	$21,870	$21,230

through thick manuals looking for escape clauses, the Starplex System guides you through your work path with a series of menus, prompts, lights, and audible signals.

And while some systems can communicate only in assembly, ours is fluent in BASIC and FORTRAN. Languages which can be loaded – as usual – with one keystroke.

Now others may have claimed their systems were "easy" before. But we've got the software to prove it. Which is why we do not hesitate to publish here a comparison chart which will show at a glance where things really stand.

The Starplex System is designed to be used with current and future National microprocessors, as well as BLC/SBC Series/80 microcomputers.

It's fully expandable, with four chassis slots allowing the addition of standard Series/80 boards. Plus a programming station which accepts optional personality boards for 2708 and 2716 PROMs.

Integrated into the Starplex package are five microprocessors, 64K bytes of memory, dual 256K byte floppy discs, a 1920 character CRT, a 50 CPS printer, and standard ASCII keyboard in addition to the special function keypads.

All the software you'll need is included in the package. A powerful operating system, macro assemblers, editor, debugger, and other key software modules.

We also offer the In-System Emulator (ISE), an extremely valuable option for hardware development. It works through an easily understood command interface. ISE uses its own memory for memory mapping – a time-saving feature which also allows true real-time debugging.

Because Starplex ISE incorporates symbolic debugging, you can debug code in the same assembly mnemonics in which it was written. And it's the only system emulator capable of debugging two microprocessors simultaneously in a multi-processor system.

By any standard of comparison, the Starplex Development System represents a colossal leap-frog over the field in every category, save one: Price. And so, while others ask in excess of $20,000 for the privilege of unnecessary toil, our price is just $13,800. On the theory that not only is less more, but more should cost less.

We would jump at the chance to tell you the whole story in detail. Write or call me for a complete brochure on the Starplex Development System. Address your request to Mark Levi, General Manager, Microcomputer Systems, National Semiconductor Corporation, Drawer 28, 2900 Semiconductor Drive, Santa Clara, California 95051. Or dial these toll-free numbers: 800-538-1866; 800-672-1811 in California.

In Europe, write National Semiconductor GmbH, Industriestrasse 10, 8080 Fuerstenfeldbruck, West Germany."

Computer Products Group
≈ National Semiconductor Corporation

The WHIZZARD™ will amaze you.

Graphics magic you never had before.

Fast, interactive computer graphics. Unequaled refresh vector quality. Astonishing performance at unbelievable prices. The best in the industry.

Buy a WHIZZARD refresh terminal. Connect it to your computer. Buy a WHIZZARD intelligent terminal. With built-in computing power. Or, buy a stand-alone graphics processing system. With the WHIZZARD's powerful FORTRAN-based graphics software, you're up and running fast.

Add an RS-232-C interface for remote or distributed processing. Up to four monitors for shared graphics processing. Plus all the graphics peripherals you may need.

Two WHIZZARD families. It's your choice.

Choose the WHIZZARD 7000 for unmatched graphics throughput and versatility. With features like hardware rotate, zoom, and multiple viewports. And easy interfacing to any 16-bit or 32-bit computer. Or, the WHIZZARD 5000 for the lowest-cost, high-performance graphics possible. Every 5000 system includes its own NOVA/ECLIPSE computer.

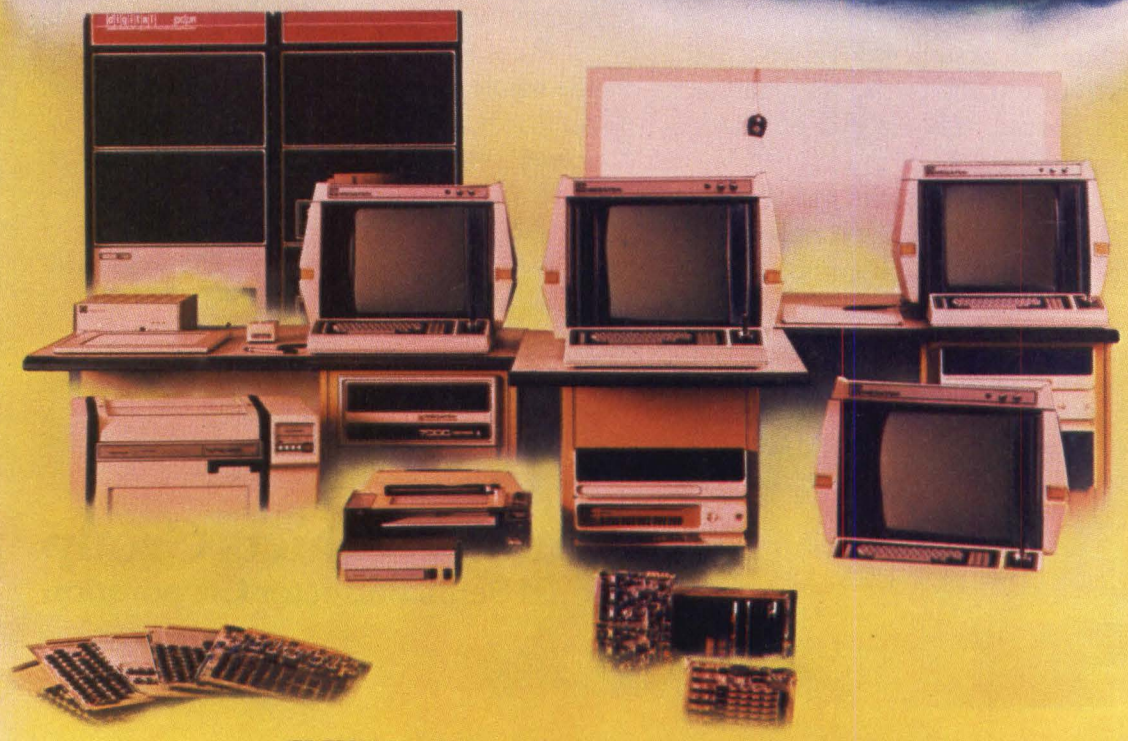
Plus, TEKTRONIX® users can get complete 4014™* compatibility with our Emutek™ software. It's the easy, economical way to upgrade from storage tube graphics.

For the whole WHIZZARD story, write or call Pat Burke, MEGATEK, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590. TWX: 910-337-1270. (European office: 14, rue de l'Ancien Port, 1201 Geneva, Switzerland. Phone: (022) 32.97.20. Telex: 23343.)

The Visible Difference

MEGATEK
CORPORATION

CIRCLE 25 ON INQUIRY CARD



*TEKTRONIX® and 4014™ are registered trademarks of Tektronix, Inc., use of which in no way constitutes endorsement.

Single Board, 64-Channel Analog I/O Systems Plug Into Unibus Backplane

Channel capacity of 64 analog inputs and choice of high or low level signal capability with 12-bit A-D conversion are standard performance features of DT 171X series analog I/O systems. Mounted on standard hex-height boards, the single card systems plug directly into a hex SPC slot in the Unibus backplane of DEC's PDP-11 minicomputers and are powered from the computer's 5-V supply.

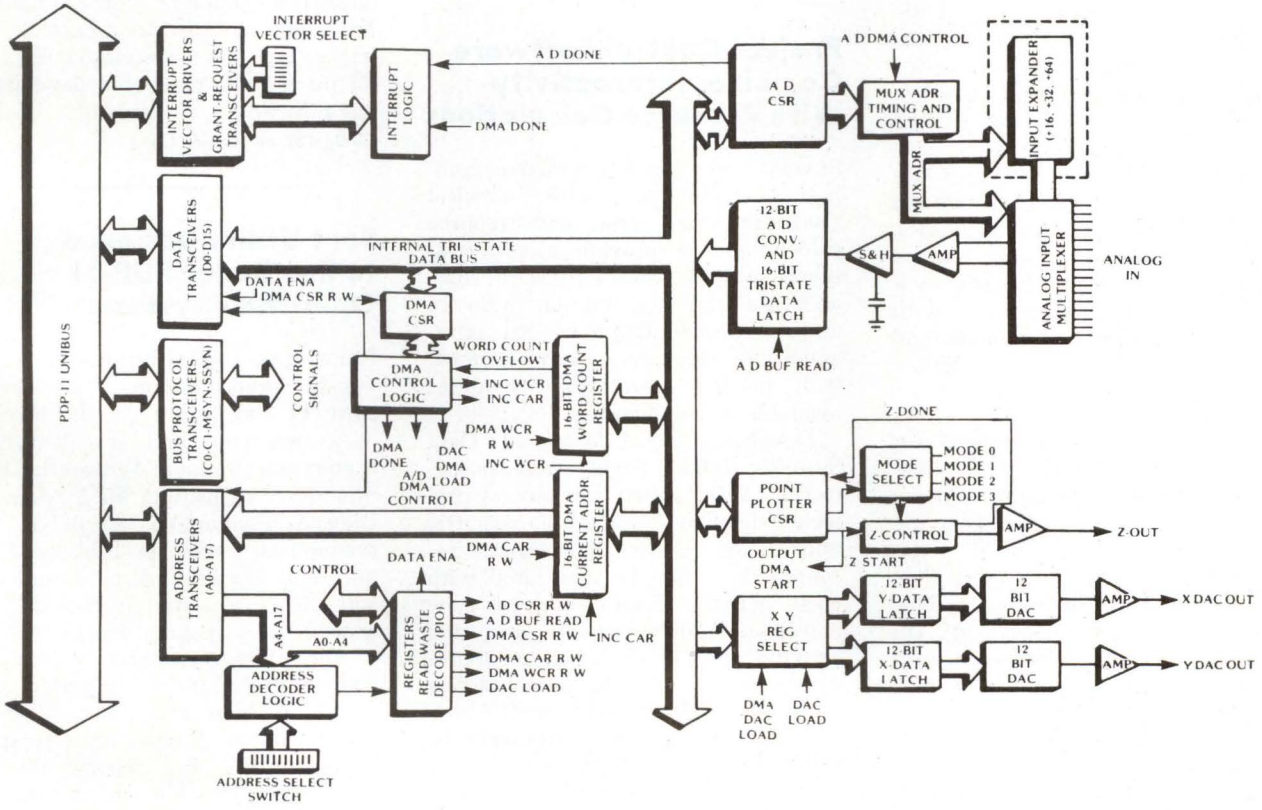
Additional features offered on these single card systems by Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760 are logic controlled 3-axis point plotting capability, signal inputs down to 10 mV full scale either isolated to ±250-V common mode or nonisolated, and direct program compatibility with DEC models. Optional are full board DMA interface for both input and output channels, programmable gain amplifier to extend dynamic range, and 100-kHz throughput.

DT 1711 is a realtime analog I/O system designed for high level applications. Its input section accepts full scale unipolar inputs of 0 to 5 and 0 to 10 V as well as bipolar inputs of ±5 and ±10 V. The on-card 12-bit A-D converter is jumper connectable for corresponding data outputs that are binary coded for unipolar inputs and either offset binary or 2's complement for bipolar. Throughput is 35 kHz with 100 kHz optionally available. For point plotting under program control, the output section contains two D-A converters and Z-axis pulse output.

Channel capacities are 16 single ended or 8 differential inputs, 32 single ended or 16 differential, or 64 single ended or 32 differential. A 14-bit A-D converter is available as is a programmable gain amplifier option for gains of 1, 2, 4, and 8.

An input system only, the DT 1712 is identical except that it has no point plotting converters or related output section circuitry. The DT 1715 is a low level I/O system that accepts full scale inputs from 10 mV to 10 V; in other respects it is identical to the 1711.

Another low level I/O system, the 1719 has an isolated analog input section that withstands and rejects common mode voltages, to ±250 V. This unit uses a reliable and expandable reed relay flying capacitor technique that provides 126-dB common mode and 90-dB normal mode rejection at 60 Hz. Available with four differential input channels and an optional programmable gain amplifier with digitally set gains of 1, 10, 100, and 500, the device can take up to 20 samples/s in random channel select mode or 40 samples/s in sequential mode.



DT 1711 series analog I/O systems provide 16- to 64-channel, 12-bit data acquisition with optional point plotting capability. Single board systems from Data Translation plug directly into Unibus backplane of PDP-11 minicomputers

Circle 178 on Inquiry Card

SOFTWARE

Software Packages Allow Graphics Hardcopy From Minicomputers

Software packages offer plotting capability for various printer/plotters on Data General, DEC, and Sperry Univac computers. Written in FORTRAN, the packages are designed to run under the minicomputers' operating systems to provide graphic hardcopy on Versatec, Printronix, and Gould printer/plotters.

To give Sperry-Univac® users the speed and reliability of electrostatic plotting, Versatec, 2805 Bowers Ave, Santa Clara, CA 95051, has integrated Versaplot version 07 plotting software subroutines for use on 1100 computers under the EXEC-8 operating system. The package consists of FORTRAN and assembly language source code and a batch job stream to compile and assemble the source and build libraries.

Level E FORTRAN-V callable subroutines are compatible with basic pen plotter routines and commercial software packages. Enhancements include programmed grid overlay, area shading, and solid or dashed curved line generation.

Provided on 9-track, 800- or 1600-bit/in tape, the package allows user adjustable plotting windows, automatic stripping of plots wider than plotter paper width, and multiple line widths. Complete with graphics programming manuals and operating manual, price is $5,500.

Circle 179 on Inquiry Card

A device driver and support for PLOT 5000 software under Data General's advanced operating system allow Eclipse users to generate graphic hardcopy on Gould series 5000 printer/plotters. Available from Gould Inc, Instruments Div, 3631 Perkins Ave, Cleveland, OH 44114, the package includes user oriented features such as ERASE, multiple and fractional weight lines, and a plot monitor program (PLT). PLT features allow users to set global and local program switches at run time, enter number of copies to be produced, produce trace messages as the monitor executes, and direct error or trace messages to files.

Both a graphic and alphanumeric handler, the AOS driver allows suspension of spooling output from disc files, providing direct output of buffers from main memory. In alphanumeric mode the driver allows the printer/plotter to simulate a standard line printer.

Circle 180 on Inquiry Card

Written in machine independent FORTRAN, a software plotting package for Printronix printers is available in versions that run under Data General's RDOS and DEC's RT-11 without modification. Replacing the standard subroutines in an existing plotter program, the package developed by Rhintek, Inc, PO Box 220, Columbia, MD 21045 produces an output plot with 60 x 72 points/in resolution.

The package includes all source code on a 9-track, 800-bit/in magnetic tape in RDOS DUMP, RT-11, or card image format. Cost is $950.

Circle 181 on Inquiry Card

Project Control Software Combines Interactivity With Resource Calculations

READINET combines interactive computing techniques with classical PERT/CPM time, cost, and resource calculations to provide a conversational project control system suitable for the construction industry and large manufacturers. All interaction is through a CRT terminal with printed reports and analyses available on command.

Developed by Educational Data Systems, 1682 Langley Ave, Irvine, CA 92714, the system can process projects with any number of activities and events. Up to 16 different resource types can be associated with each activity. Each resource type may have its own unit cost, and each activity may be assigned a nonresource linked cost to cover factors such as materials and rentals.

Weeks of 5, 6, or 7 days may be selected and an unlimited number of holidays may be specified at run time, providing the flexibility to experiment with the effects of changing work weeks. Multiple starts and finishes are allowed, and scheduled dates may be assigned to any event. Critical situations may be represented by allowing ending events to float.

Progress is reported as a percentage completed of each activity; when an activity is completed, the completion date is printed. Up to nine tabular reports are included in the reporting menu, as well as ad hoc reports, bar charts, and resource allocation/finance reports. Reports can be printed out directly or can be displayed on the CRT screen.

Using one optional module allows time card data and real costs to be reported. An optional interrogator module permits use of the CRT to investigate the status of any activity or event in detail. With it the network can be searched for activities or events that satisfy a complex selection criterion based on descriptors connected with .AND. and .OR. operators.

The system is written in Business BASIC under the IRIS operating system and uses random access file structures. It can automatically create or delete files, and allows multiple projects to be processed simultaneously from different online terminals. Provided on diskette, cassette, or paper tape, the system consists of 23 programs. Price for a basic package is $2900.

Circle 182 on Inquiry Card

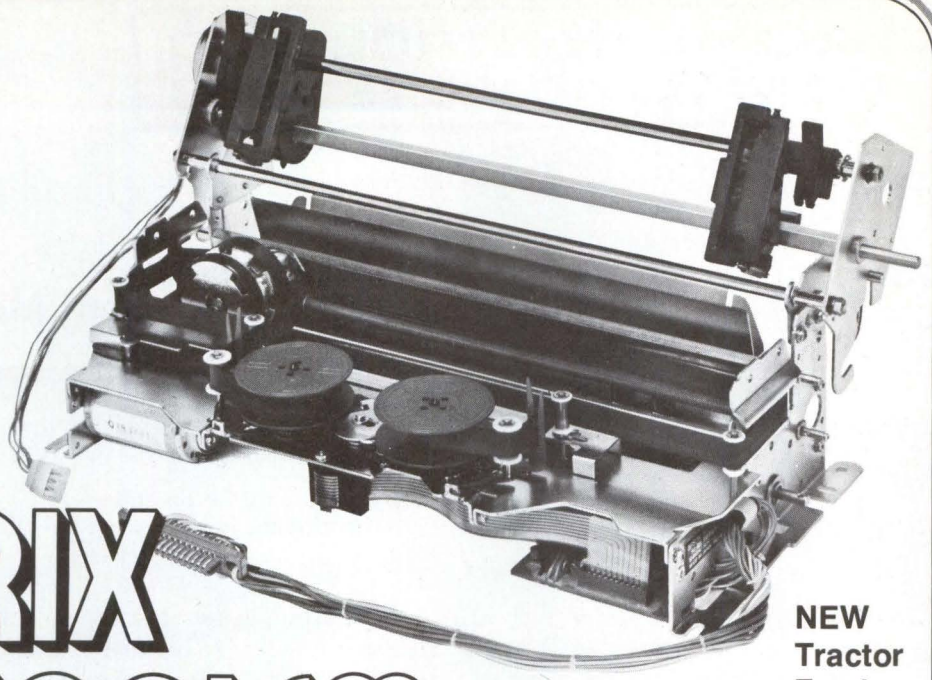
Sort Utility Designed to Run Under PDP-11 Operating Systems

Running on Digital Equipment Corp's PDP-11 minicomputers, the SPEEDSORT/11 sort utility can be invoked as a user command or called from a FORTRAN program. Written by Pennington Systems Inc, 65 S Main St, Bldg A, Pennington, NJ 08534, the system runs under RSX-11D, RSX-11M, and IAS operating systems and can sort fixed or variable records and spanned or unspanned blocks.

The utility accepts two levels of command files, including partial command. A high speed second order "verify" mode permits users to specify sort keys and reports whether records in the file are already in order. Sort keys may be integer (16- or 32-bit signed), floating (32 or 64 bit), character (8-bit unsigned), or word (16-bit unsigned). □

Circle 183 on Inquiry Card

OEM'S... USE THE LEADING DOT MATRIX MECHANISM



NEW Tractor Feed Type

EPSON MODEL 3110 WITH 80 COLUMN FORMAT

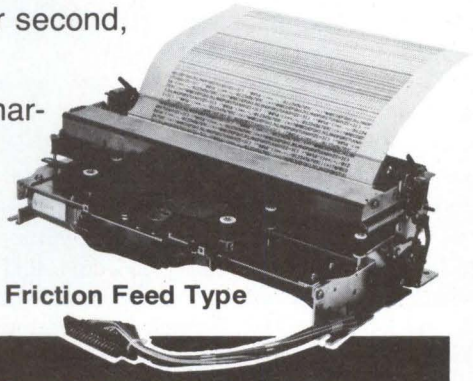
AS PART OF YOUR SMALL BUSINESS AND PERSONAL COMPUTER SYSTEMS

Now available for both tractor feed and friction feed type applications, the Epson Model 3110 Dot Matrix Printer Mechanism features a 100 million character head, with exceptionally clear printing.

Long life of the head with ruby-jeweled support comes from the mechanism's precise alignment and pin movement . . . using techniques developed by Shinshu Seiki Co., Ltd., Epson's parent in Japan.

The Model 3110 prints 80 columns at 150 characters per second, with a 5 × 7 dot matrix character.

Tailored for the small-business and personal computer markets, the Model 3110 is attractively priced for OEM's large- or small-lot orders, and is stocked for prompt delivery.



Friction Feed Type

Write for complete information and OEM prices.

EPSON

EPSON AMERICA, INC.
23844 Hawthorne Blvd., Torrance, CA 90505
Telephone (213) 378-2220 · TWX 910 344-7390

CIRCLE 26 ON INQUIRY CARD

Microcomputer Control System Maintains Slide Drive Positioning Accuracy

W. E. Barkman

Union Carbide Corporation
Oak Ridge, Tennessee

Closed-loop control of machine tool slides is routinely provided by manufacturers of numerical control systems. However, these systems—whether hard- or soft-wired—do not always provide the flexibility and initial low cost often required in the early stages of a development effort. Fortunately, single-board computers do meet these requirements and can be used successfully in early prototype development situations.

At the Oak Ridge Y-12 Plant* development of linear motor slide drives is accomplished with a test bed such as shown in Fig 1. A transistor amplifier driven motor and a 1000-lb (454-kg) air-bearing slide are mounted on a steel-topped concrete table that is isolated from building structural vibrations by a pneumatic isolation system. Slide position information is provided to the control system via up/down pulses from a Hewlett-Packard laser interferometer.

Control System Configuration

Input signals required for the servo system consist of position following-error and rate information. Traditionally, the following-error is formulated within the numerical control (NC) as a digital word, while the rate signal is obtained from a tachometer that is attached to the drive lead screw of the machine. Unfortunately, the rate signal is not as easily accessible in this instance because there are no rotating parts in the linear motor slide drive system.

An Intel SBC 80/10 single-board computer was chosen to provide the position following-error data required for closed-loop operation. Rate information was obtained by coupling the up/down pulse output lines from the laser display to individual frequency-to-voltage (F-V) converters and summing the outputs from the F-V converters with an operational amplifier. This rate signal could also have been generated using the microcomputer but with an associated penalty in the execution time of the control loop software. Also, a hardwired circuit could have been used in place of the microcomputer but at the loss of needed flexibility in the early stages of development.

Additional microcomputer hardware used to close the position loop consists of an Intel System 80 chassis, SBC 104 combination memory and input/output (I/O) board, and SBC 310 high speed math unit and an Augat wirewrap interface board. On the interface board are 16-bit up/down counters and buffers for the system command and feedback signals, a 16-bit digital-to-analog converter (DAC) that drives the servo amplifier, and the F-V converters. The 16-bit command and feedback data are coupled to the I/O card via 50-pin flat cables from the wirewrap board, while the up/down command and feedback signals, following-error signal, and rate signal are passed through an auxiliary plug added to the card cage frame. These signals are coupled to the System 80 chassis via BNC connections mounted on the rear panel.

The control loop software begins operation by issuing a strobe signal to the interface board (Fig 2) that causes the current contents of the feedback and command counters to be latched into the buffer registers. (A hardwired logic circuit on the interface board ensures that a data transfer is not attempted while input pulses are present.) The software then reads the contents of the input buffers and converts these counts into a common base using the fixed point multiplication capabilities of the math unit. This step is necessary since the value of the feedback pulses is frequently a fraction of the value of the command pulses.

After the input data are properly scaled, the command and feedback words are subtracted to form a new increment of following-error. This increment is then added to the previous following-error value and the result is output to the DAC. Software operates in a continuous loop, updating the following-error once every cycle.

The computer code was configured to obtain the minimum cycle time for updating the system following-error (thereby avoiding abrupt changes and minimizing interface capacity requirements). Therefore, assembly language programming was required, with attention given to utilizing the fastest instruction sequence, while

*Operated for the Department of Energy by Union Carbide Corp, Nuclear Div under Contract W-7405 eng 26.

FPS Expands the Scientific Universe of PDP-11 Applications

FPS MAKES GREAT COMPUTERS BETTER

The FPS AP-120B Array Processor

A great contribution to technology, the DEC PDP-11*, but it can't give you the computational power required for many scientific applications. That's why FPS developed the AP-120B Array Processor.

The AP-120B Array Processor gives economical minicomputer systems the extraordinary computational power of large scientific computers. For example, an AP-120B has been used in a PDP-11/34 system to reconstruct and analyze complex digital images. Without the AP-120B, the task would take more than two hours. With the AP-120B, it takes less than thirty seconds — that's a 240X improvement!

A PDP-11/70 and AP-120B would offer even greater data handling capabilities.

The FPS architecture is no secret. Internally synchronous operation and seven parallel data paths provide unequalled cost/performance, reliability, and programmability. Programmable I/O units also enable exceptional features, such as direct control of disc storage and real time data flow.

Controlled by simple subroutine calls from a FORTRAN program in the PDP-11, or other host computer, FPS Array Processors can be programmed by selecting routines from the extensive FPS Math Library, by writing new routines in the relatively simple AP Assembly Language, or through use of the AP FORTRAN Compiler.

Hundreds of FPS Array Processors are in use today by people who want to retain the hands-on control and affordability of a minicomputer system, but require the exceptional throughput of a large mainframe for their application.

Find out how this new power in computing (typically under $50K complete) can benefit your application. For more information and an FPS Array Processor brochure, use the reader response number or coupon below. For immediate consultation, contact Floating Point Systems directly.

*DEC and PDP-11 are registered trademarks of Digital Equipment Corporation.

The Age of Array Processing Is Here... and FPS Is The Array Processor Company.

CALL TOLL FREE 800-547-9677
P.O. Box 23489, Portland, OR 97223
TLX: 360470 FLOATPOINT PTL
In Europe & UK: Floating Point Systems, SA Ltd.
7 Rue du Marche, 1204 Geneve, Switzerland
022-280453, TLX: 28870 FPSE CH

Floating Point Systems, Inc.

FPS Sales and Service Worldwide: Boston, Chicago, Dallas, Denver, Detroit, Houston, Hunstville, Los Angeles, New York, Orlando, Ottowa, Philadelphia, Portland, San Francisco, Washington, D.C. International offices: Geneva, London, Munich, Paris, Tel Aviv (Eastronix, Ltd.), Tokyo (Hakuto Co. Ltd.)

Please send me an FPS Array Processor brochure.

Name _____ Title _____

Company _____ Phone _____

Address _____

City _____ State _____ Zip _____

My Computer System is _____ My Application is _____

CIRCLE 37 ON INQUIRY CARD

IMAGINE

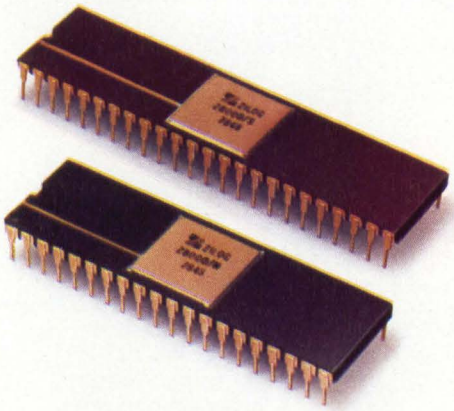
Zilog rockets out in front again to launch a new generation.

For the first time, the architectural sophistication and data processing capabilities of large, main-frame computers has been captured in the cost-effective, easy to use format of the microprocessor. Now you can have the freedom to create entirely new, innovative systems, unhindered by the primitive architectures of previous microprocessors.

A revolution in sophistication.

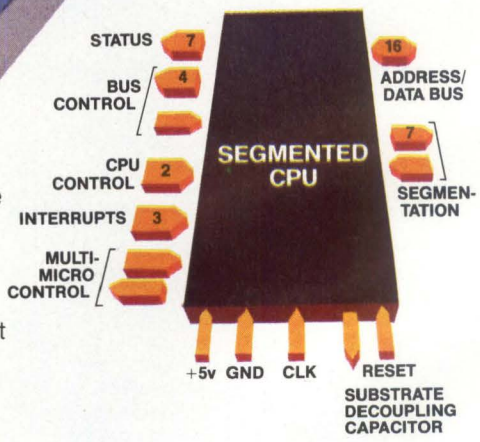
The Z8000 has been designed from the ground up with options to fit your application needs exactly. For the full 8 MB addressing capability, choose the 48 Pin DIP version. Its companion device, the Memory Management Unit, opens the way to dynamic relocation, memory protection and multi-tasking applications.

Flexibility soars to new heights.



The Z8000 allows you to directly address up to 8 MB of memory. All 16 registers are a full 16 bits wide and are completely general purpose. The powerful, problem-solving instruction set supports 7 different data types from bits to 32 bit words, has 8 addressing modes and 418 usable opcode combinations.

The general register architecture helps avoid the well-known bottlenecks inherent in dedicated register designs. When this architecture is combined with the powerful instruction set, the Z8000 system throughput is an explosive 50% greater than any other 16 bit microprocessor available today.



IMAGINE

A REVOLUTIONARY NEW WAY TO THINK ABOUT MICROPROCESSOR SYSTEMS. INTRODUCING ZILOG'S Z8000.

For smaller, less memory-intensive applications, select the 40 Pin version of the Z8000. It's software compatible with the 48 Pin Z8000 but addressing is limited to 64KB in each of its six address spaces. It comes in a standard 40 Pin package.

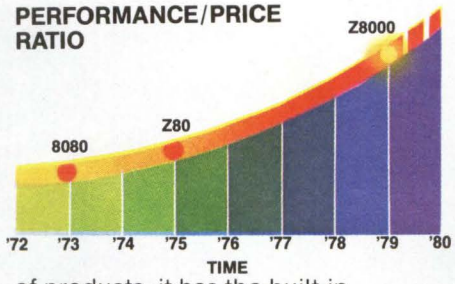
Wait 'till you meet the family.

We're starting off this new microprocessor era with a bang, but it's just the beginning. Soon to come are the Memory Management Unit, peripheral interfaces, FIFO buffer elements, universal peripheral controller and memories for any application you might have.

And, all the new I/O chips, memories and, of course, the companion Z8, take advantage of the flexible Z-BUS architecture to maximize performance, ease of interconnection and minimize PC board area.

Zilog delivers on the next generation of microprocessors. Again!

With the introduction of the Z8000, microprocessor technology explodes to new heights. Bursting with a rich and sophisticated architecture, the Z8000 not only opens the way to revolutionizing your next generation



of products, it has the built-in growth potential to carry your product development efforts out to totally new and unexplored horizons.

Imagine the possibilities, then light your own fuse!

Sound exciting? It is. Get your own fireworks blazing by placing your order today with your nearest Zilog distributor.

In the meanwhile, give your engineering staff a headstart on the fireworks by ordering the Z8000 literature package; in the U.S. order directly from Zilog, elsewhere from your Zilog distributor.

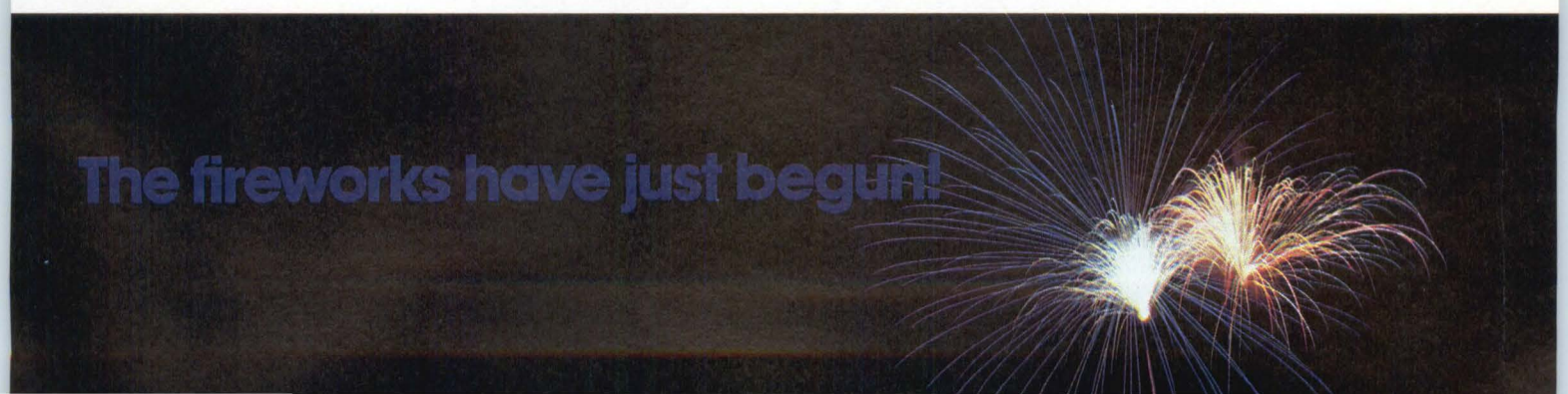
10460 Bubb Road, Cupertino, CA 95014
(408) 446-4666 TWX 910-338-7621
EASTERN REGION: (617) 667-2179
MIDWESTERN REGION: (312) 885-8080
SO. WESTERN REGION: (714) 549-2891
NO. WESTERN REGION: (408) 446-4666
EUROPE (ENGLAND): (0628) 36131/2/3
WEST GERMANY: (08106) 4035
JAPAN: 03-476-3010

An affiliate of
EXXON ENTERPRISES INC.

Zilog

SEE US AT ELECTRO
BOOTHS 1106, 1108.

CIRCLE 28 ON INQUIRY CARD

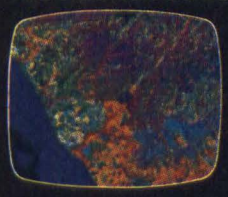


When you need color graphics, Ramtek has it all.

Color. A surprisingly powerful way to add information, manage it, increase the efficiency of its use. However you plan to use it, there is only one company with the breadth of line, the technological mastery, to give you the choices you need without compromise—or needless costs.

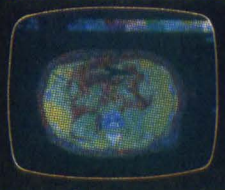
It's Ramtek. For color graphics. For imaging. Ramtek has what you need:

The Ramtek 3000. Eight models let you explore the possibilities of color graphics the moment you plug in your application software. Stand alone image processing and graphics. Fully integrated and ready to go. Desk configuration.

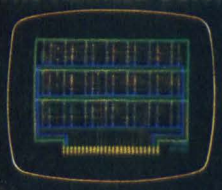


The Ramtek 9000 Series Display Controller. Four models. Total modularity. Buy just what you need; add to it at any time. The high-performance family. The industry standard in imaging and graphics raster scan color.

The Ramtek 9050 Series Display Controller. Four models. The most popular elements of the 9000 Series are here packaged for economy. All are software compatible with the 9000, have expandable memory and interactive capabilities.



The Ramtek Colorgraphics Computer Terminals. Three models let you choose between economy, optimum price-performance, or maximum resolution-performance. Easy to program. Easy to use. Easy to interface. Interfaces to the Xerox 6500 Color Graphic Printer for color hard copy output. These are the price, industry and performance leaders in raster scan color graphics terminals.



The Ramtek Monitor Family. Nine models. Up to 1024 line addressability on the screen in color or black and white. CRT sizes 13" or 19". Cabinet or rack mounted versions.

Ramtek Large Screen Projection. Interface Ramtek's or your own large screen projection unit easily, quickly.

And there's more to come. From Ramtek, the world's largest independent manufacturer of raster scan color graphics and imaging equipment. Direct sales in the U.S. and Canada. Distributors worldwide plus a worldwide network of customer service and depot repair stations.

For more information, write:
Ramtek, 585 N. Mary Ave.,
Sunnyvale, CA 94086.

ramtek

Our Experience Shows

REGIONAL OFFICES: Sunnyvale, CA (408) 735-8400 • Newport Beach, CA (714) 979-5351 • Dallas, TX (214) 422-2200 • Huntsville, AL (205) 837-7000
Cleveland, OH (216) 464-4053 • Washington, D.C. (301) 656-0350 • Metropolitan N.Y. (201) 238-2090 • Boston, MA (617) 862-7720 • West Germany (0611) 771070

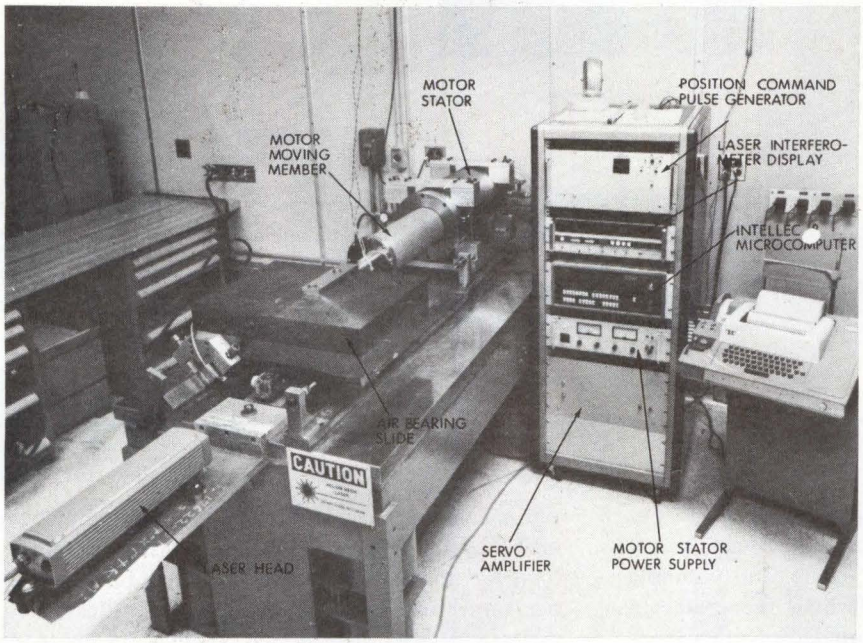


Fig 1 Early test bed configuration. Intellec 8 microcomputer was subsequently replaced by SBC 80/10 single-board microcomputer system

attempting to maintain some degree of modularity. For instance, the hardware math unit was chosen not only for its speed in performing fixed-point multiplication (typically 15 μs) but also for the parallel processing capability. This enabled the software to initialize the arithmetic operation and then continue with other tasks such as I/O servicing and sign adjustment until the math operation was completed. (A math unit status-checking sequence was also added in anticipation of the eventual use of a faster processor.)

Following completion of data scaling, the following-error was formed by subtracting the position command word from the feedback word. However, this was not done with the math unit because of the time required to convert back and forth from fixed-point to floating-point (fixed-point subtraction is not available with the

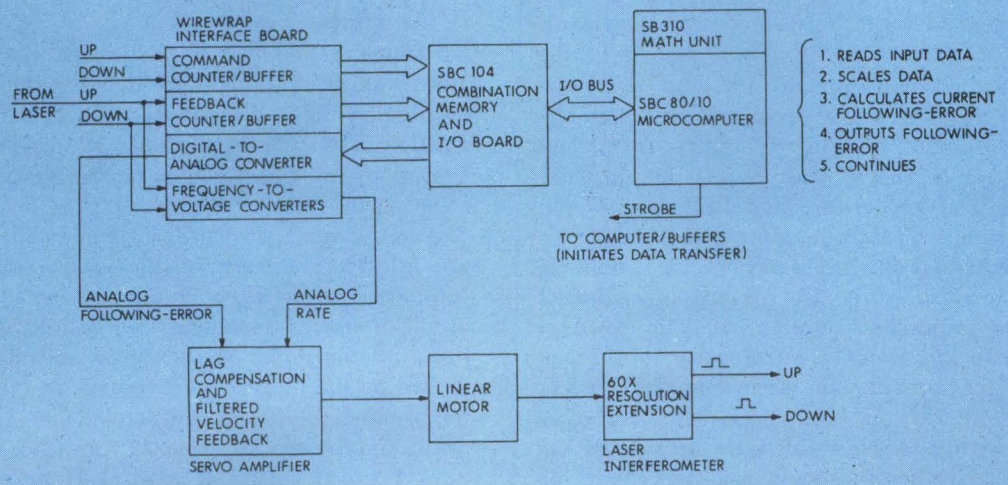
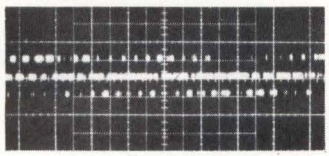
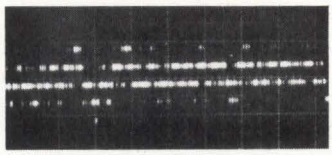


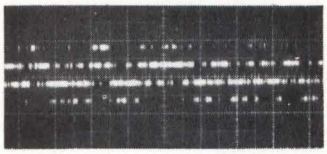
Figure 2 Control system block diagram. Microcomputer reads feedback and command information and outputs following-error to servo system



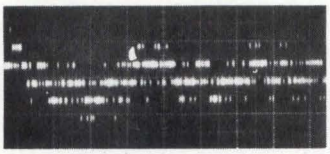
STANDSTILL



0.1 IN (0.25 CM)/MIN



0.2 IN (0.5 CM)/MIN



0.5 IN (1.27 CM)/MIN

Fig 3 Positioning test results demonstrating following-error ripple at 0.1-, 0.2-, and 0.5-in/min (0.25-, 0.5-, and 1.27-cm/min) feed rates. Processor continually executes control loop software and updates following-error every 500 μs. [Vertical scale 0.2 μin (5.1 nm)/div, horizontal scale 50 ms/div, and feedback resolution 0.1 μin (2.54 nm)]

SBC 310) and because parallel processing was not reasonable at this point in the software. Instead, 24-bit subtraction was accomplished by using the "double add stack pointer" instruction (which generates a carry) and an "add register to accumulator with carry" instruction, for a nominal subtraction time of 14 μs.

Nominal execution time of the software is 500 μs. This means that the number of counts being processed each cycle with a 0.1-μin (2.54-nm) feedback resolution and a maximum feed rate of 0.5 in (1.27 cm)/min is relatively small. However, the input counter/buffers must be sized to accept sudden excursions due to external disturbances, or sudden changes in feed rates. For this reason, a 16-bit up/down counter was used to accumulate the position feedback pulses. An 8-bit counter would have been sufficient for the command pulses but the 16-bit counter provides extra capability for future use. A 12-bit command counter would also have been adequate but would have required extra software data manipulation.

A 16-bit DAC was chosen initially in hopes of being able to accommodate large values of following-error. Unfortunately, as the size of the DAC increased, the amplitude of the least significant bit also decreased so that the full range of the DAC was not really usable. An amplifier was added to the DAC output to attempt to extend the usable range (this results in amplifier saturation at a fraction of the DAC full scale output but it does provide a cushion against data loss).

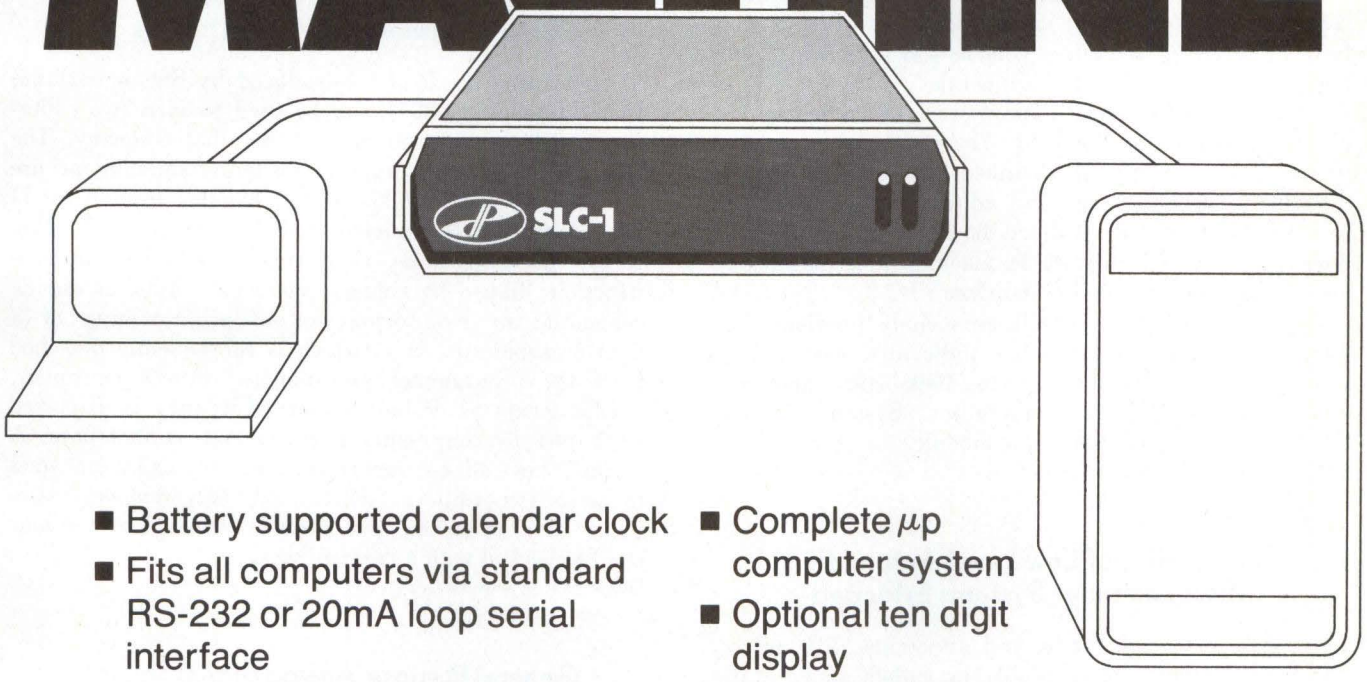
While this provided the necessary signal amplitude to ensure good sensitivity, it also resulted in a distinct nonlinearity. A preferable solution was to program the microcomputer to provide a software gain break so that an 8X increase in gain occurred at following-error values below 1.6 μin (40.6 nm). This extremely low gain-break setting was possible only because of the very high gain servo loop [system following-error for normal operating conditions is less than 1 μin (25.4 nm)]. This technique permitted a "tighter" position loop for normal operating conditions but avoided amplifier saturation for large amplitude disturbances. Nevertheless, it was determined that a 12-bit DAC would be adequate since a minimum drive signal of approximately 0.04 V was required to accurately control the motor. Higher resolution DACs could be used with an accompanying change in the gain-break factor but also with a "sharper" nonlinearity at the gain-break point.

Other limiting factors influencing system performance are the bandwidths of the F-V converters and the laser interferometer. As system resolutions are extended, the feed rates at which the F-V converters saturate and the laser loses data are lowered. This can be alleviated to a certain extent by increasing the bandwidths of the F-V converters (at the expense of degraded low speed performance), but the laser bandwidth is not readily increased.

Test Results

In its present configuration the drive system utilizes lag compensation and filtered velocity feedback to provide stability and high position-loop gain. The system positioning accuracy is demonstrated by monitoring the position following-error ripple as displayed in Fig 3. Variations in this position following-error signal for a constant velocity command (as determined by a constant "rate" of position command input pulses) are a direct measure of the system "positioning uncertainty." Of course a dc signal component is required at all times to maintain the desired position versus time relationship, ie, constant velocity. As demonstrated by the figure, the variations in the DAC generated following-error signal (which define the positioning uncertainty) are less than 1 μin (25.4 nm) at feed rates between 0 and 0.5 in (1.27 cm)/min.

THE TIME MACHINE



- Battery supported calendar clock
- Fits all computers via standard RS-232 or 20mA loop serial interface
- No user modification to operating system required
- Dual independently selectable Baud rates
- Automatically provides time when requested by computer
- Automatic time restoration after power failure
- Complete μp computer system
- Optional ten digit display
- Price $575 (single qty.)

For more information on this timely product, contact:

Digital Pathways Inc.
4151 Middlefield Road
Palo Alto, CA. 94306
Phone: (415) 493-5544

DIGITAL PATHWAYS

CIRCLE 30 ON INQUIRY CARD

DC&AS BRIEFS

Modular CNC Enables OEM to Customize System Configurations

Low cost and microprocessor based, the series 7100 computer numerical control is available for 2- and 3-axis lathe and mill applications, with or without spindle or table control. Programmable interface capability and adjustable parameters enable customizing by the OEM to machine applications. Major components—operator control panel, controller, and power supply—are supplied by Allen-Bradley, 747 Alpha Dr, Highland Heights, OH 44143 in a freestanding cabinet or can be configured by the OEM. One RS-408 and two RS-232 ports permit interface with peripherals.

Predesigned firmware options can be added either at the factory or in the field. The executive or control program is on a self-contained, nonvolatile P/ROM module, program storage and editing requirements are handled by RAM with battery backup, and nonvolatile EAROM is used for adjustable machine tool parameters and optional programmable interface.

Built-in diagnostic capabilities include provision for operator messages, I/O status indicators, test points, power turn-on sequence, system diagnostics, and programmable interface search-monitor. System diagnostics are on a separate, pluggable module.

Circle 150 on Inquiry Card

Capabilities of Low Level Automation Microcomputer Systems Extended

Now with extended range and functions, 210 microcomputer systems are available on either single- (100 x 160 mm, version E) or double-height (233 x 160 mm, version D) Europa format PC boards with the same range of functions. A full set of boards includes single-card computers, memory expansion modules, I/O for device connection or computer linking, and digital and analog process interface modules. Both versions have a 9k-byte memory on the board. Version E now also has a memory module for up to 16k bytes and a combined digital I/O module.

Based on the SAB 8085 microprocessor, the E version CPU can be supplied with up to 9k bytes of RAM and ROM. The combined digital I/O module for signals up to 24 V has eight isolating channels. It is possible to make up miniaturized controllers with only two Europa cards and a power supply of only 5 V. Main memory can be extended to 64 bytes.

Memory of version D has been doubled to 9k bytes. A pocket-calculator sized test panel is now available for simple hardware and software tests and is particularly suitable for putting a system into operation onsite.

Floppy disc drives are connected to the I/O modules if they are to be used in a data collection system. Either standard diskettes or minidiskettes may be used. Programs can now be generated on the 210 system itself with STEM program package either on a 3914 typewriter or, for greater convenience, on a 3974 alphanumeric display unit.

Both microcomputer systems, intended for lower levels of automation, are produced by Siemens AG, Postfach 103, D-8000 Munich 1, Federal Republic of Germany. They are not marketed in the U.S.

Circle 151 on Inquiry Card

Program Loader Can Be Used With Either of Two Controllers

A single program loader introduced by Struthers-Dunn, Inc, Pitman, NJ 08071 can be used to load two different models of controllers made by that company. The Director 1001/3001 program loader is suitable for use with the 1001 controller, which handles from 8 to 32 I/Os, or the 3001, which has a capacity of up to 128. It can be used alone, as during initial program construction; linked by cable to controller units, as during debugging or monitoring; or in programming of a light erasable ROM chip, which is subsequently detached from the programmer and plugged into a controller.

RAM serves as design memory. Circuitry is displayed on a CRT by depressing numeral and symbol keys. A "clear" key allows incorrect contacts, coils, or lines to be erased, while a "delete page" key removes entire pages of a program, and specific elements or sections can be checked with a "search" key.

Circle 152 on Inquiry Card

General Purpose Analog Signal Scanner Meets IEEE-488 and RS-232 Requirements

Intended to complement a controller either by itself or in conjunction with an 8502A digital multimeter in precision data acquisition systems that are compatible with either IEEE 488-1975 or EIA RS-232-B/C standards, the 2204A scanner may be connected directly to as many as 100 channels through 10 scanner circuit cards. The microprocessor based instrument, made by John Fluke Mfg Co, Inc, PO Box 43210, Mountlake Terrace, WA 98043, uses two types of plug-in circuit cards: one, for general purpose applications, has 2-pole dry reed switches; the other, for very low level signals, has 3-pole switches. Input connector cards are available for either ordinary input or thermocouple signals. Optional extender chassis increase capacity up to 1000 input channels. Maximum sequential scanning rates are 125 channels/s when used in a system or up to 5 channels/s in automatic mode. Thirty-two selectable scanning rates are available in automatic mode.

Circle 153 on Inquiry Card

The largest selling color-graphics terminal in the world.

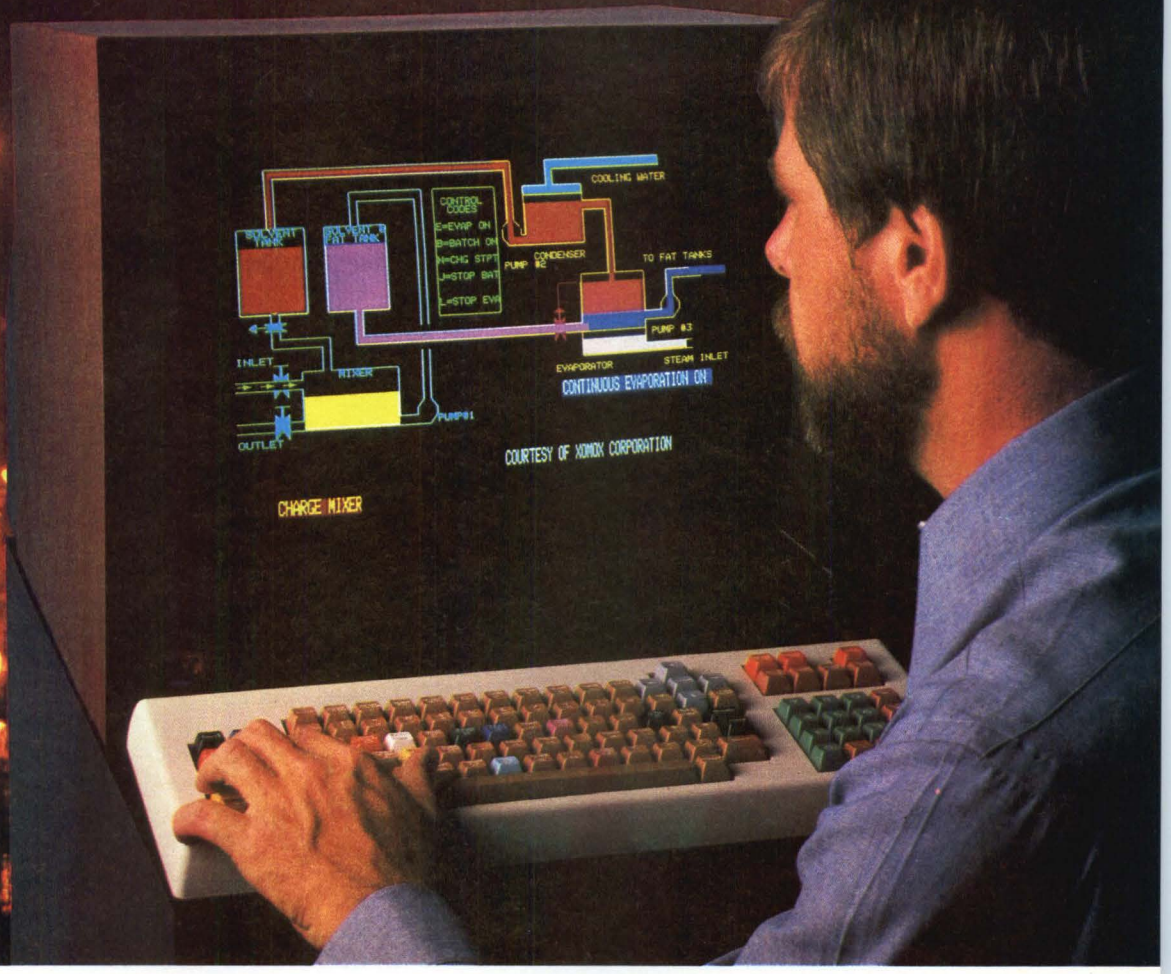
The Intecolor 8001G is helping Bailey Controls, EMC Controls, Dow Chemical, ACCO Bristol, and PPG Industries improve process control systems through color. *Because color communicates better.* Throughout major industries the world over, ISC units operate 24 hours a day, seven days a week, improving and refining control systems.

Check the advanced features of the Intecolor 8001G: expanded hardware and software graphics; 48 lines by 80 characters with two different character heights; 8 foreground colors plus 8 background colors for greater definition; character and line insert and delete; page roll-up; 64 standard ISA character; plotting capability on a 160 by 192 matrix; expanded keyboard with cursor and color controls; and 19" display (high resolution and 25" tubes available at slightly extra cost).

It's just *$1,500 (cash-with-order), and is backed by a 6-month warranty. Guaranteed delivery of your Intecolor 8001G evaluation unit within 30 days or your money back. The same price goes for orders of 100 units or more. The Intecolor 8001G. It'll improve your system and put you ahead of your competition without outspending them. Call your ISC representative for a demonstration.

Color Communicates Better.

$1,500



Unretouched photograph of screen.

*U.S. Domestic price.

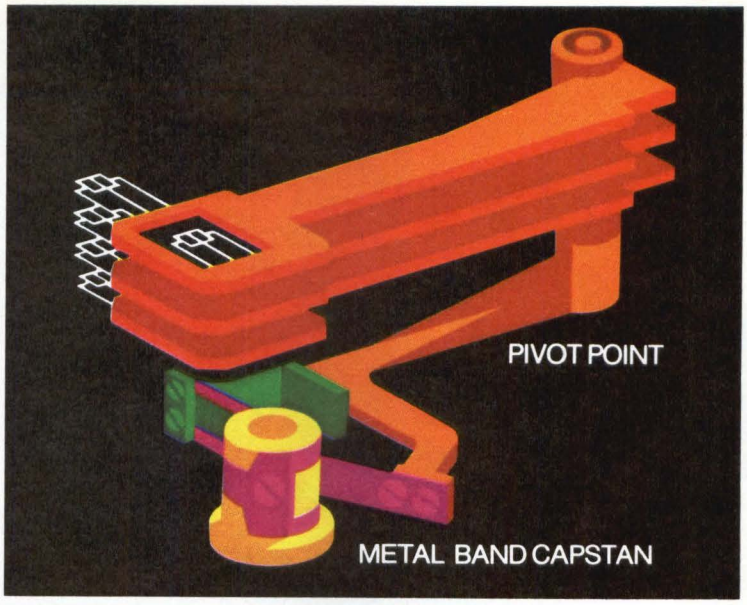
ISC SALES REPRESENTATIVES: AL: 205/883-8660, **AK:** (GA) 404/449-5961, **AZ:** 602/956-5300, **AR:** (GA) 404/449-5961, **CA:** Los Angeles 213/937-5450 or 213/476-1241, Goleta 805/964-8751, Irvine 714/557-4460, Mountain View 415/964-9300, San Diego 714/292-8525, **CO:** 303/759-0809, **CT:** (White Plains, NY) 914/949-6476 or (Holcomb, NY) 716/657-6309, **DE:** (PA) 215/688-7325, **DC:** (MD) 301/656-3061, **FL:** Ft. Lauderdale 305/776-4800, Melbourne 305/723-0766, Orlando 305/425-5505, Valparaiso 904/678-7932, **GA:** 404/455-1035, **HI:** 808/941-9319, **ID:** (UT) 801/973-7969, **IL:** (No.) 312/564-5440, (So.) (MO) 314/821-3742, **IN:** (IL) 312/564-5440, **IA:** (MO) 314/821-3742, **KS:** 913/362-2366, **KY:** (OH) 216/267-0445 or 513/434-7500, **LA:** 504/626-9701, **ME:** (MA) 617/879-7530, **MD:** 301/656-3061, **MA:** 617/879-7530, **MI:** 313/588-2300, **MN:** 612/822-2119, **MS:** (AL) 205/883-8660, **MO:** (East) 314/821-3742 (West) (KS) 913/362-2366, **MT:** (CO) 303/759-0809, **NB:** (KS) 913/362-2366, **NV:** (AZ) 602/956-5300, **NH:** (MA) 617/879-7530, **NJ:** (White Plains, NY) 914/949-6476 or (Holcomb, NY) 716/657-6309, **NM:** 505/265-5655, **NY:** White Plains 914/949-6476, Holcomb 716/657-6309, **NC:** 919/682-2383, **ND:** (MN) 612/822-2119, **OH:** Cleveland 216/267-0445, Dayton 513/434-7500, **OK:** (TX) 214/840-2169, **OR:** 503/620-5800, **PA:** (East) 215/688-7325 (West) 412/892-2953, **RI:** (MA) 617/879-7530, **SC:** 803/798-8070, **SD:** (MN) 612/822-2119, **TN:** 615/482-5761, **TX:** 214/840-2169, Houston only 713/780-2511, **UT:** 801/973-7969, **VT:** (MA) 617/879-7530, **VA:** (MD) 301/656-3061, **WA:** 206/455-9180, **WV:** (PA) 412/892-2953, **WI:** (IL) 312/564-5440, **WY:** (CO) 303/759-0809, **EUROPEAN EXPORT SALES:** (MA) 617/661-9424, **BELGIUM:** Brussels 02-242 36 04, **ENGLAND:** Bournemouth 0202-293-115, **FRANCE:** Rueil 749-40-37, **GREECE:** Athens 642-1368, **ITALY:** Roma 805/647 or 872-457, **THE NETHERLANDS:** Poeldijk 01749-7640, **SPAIN:** Barcelona 204-2099, **SWEDEN:** Vallingby 08-380-370, **SWITZERLAND:** Bern 031-224481, **WEST GERMANY:** Munich 89 3188 1, **AUSTRALIA & NEW ZEALAND:** Melbourne 543-2077, Meadowbank 808-1444, Chermside 59-6436, Wellington, NZ 64-4585, Auckland, NZ 814-9384, **CANADA:** Datamex, Ltd. (Distributor) Dorval 514/636-9774, Ottawa 613/224-1391, Toronto 416/787-1208, Vancouver 604/684-8625, **CENTRAL & SOUTH AMERICA, MEXICO, CARIBBEAN:** (GA) 404/394-9603, **FAR EAST:** (CA) 213/382-1107, **JAPAN:** Tokyo 402-8596, **IRAN:** Tehran 891148, **SAUDI ARABIA:** Jeddah 27790

Intelligent Systems Corp. ☐ 5965 Peachtree Corners East ☐ Norcross, GA 30071 ☐ Telephone 404-449-5961 ☐ TWX 810-766-1581

The SA4000 Fixed Disk Drive.
The SA4000 Series of rigid disk drives are the newest line of low cost mass storage products from Shugart. Our floppy disk drives have been the industry standard for years, and now our fixed disk drives are setting new standards of their own. Like the lowest cost per megabyte in their capacity range so you can have up-to-date Winchester storage at a price that won't bite into your system profits. That means real dollars and cents savings to help keep your system competitive. SA4000 drives are available in capacity ranges that are just right for most systems too—14.5 and 29 megabytes (unformatted). And when you design our drives into your system, you can be sure you've got a system architecture that's compatible with IBM S/32, S/34 and System 1 fixed/floppy architecture.

The head in cost per

Winchester Technology and Two Configurations.
Shugart fixed disk drives use industry-proven Winchester head and media technology to preserve your data in its own safe, sealed environment. The model SA4004, with 14.5 megabyte capacity, utilizes one disk and four heads. The SA4008, 29 mbyte version, has two disks and eight heads. Eight optional fixed heads are available to give you an additional 144 kbytes (unformatted) of head-per-track storage for applications such as indexed files or table look-up. The SA4000 Series offers an easy upgrade too. Keep your floppys for I/O and system back-up. Add our rigid disk drives for the additional capacity and throughput you need to upgrade your operating systems and mass storage.



When You Think Actuators, Think Fasflex II.™ Shugart's new, proprietary Fasflex II™ is another result of Shugart's headstrong commitment to R&D. This open loop band actuator is virtually wear-proof, and it doesn't require any adjustments in the field. Heat dissipation? With Fasflex II it's extremely low—only 200 watts is typical. But the Fasflex II acutator is only one of the benefits you get with the SA4000 series. The drives weigh a mere 35 pounds—that's about half the weight of comparable units. They're compact. They use only 5.25 inches of panel space, they can be easily mounted in a 19-inch RETMA rack. The drives are rugged, yet easy to maintain. The PCB and spindle drive motor are open and accessible on the underside of the drive. No preventive maintenance is required.

# of its class megabyte.

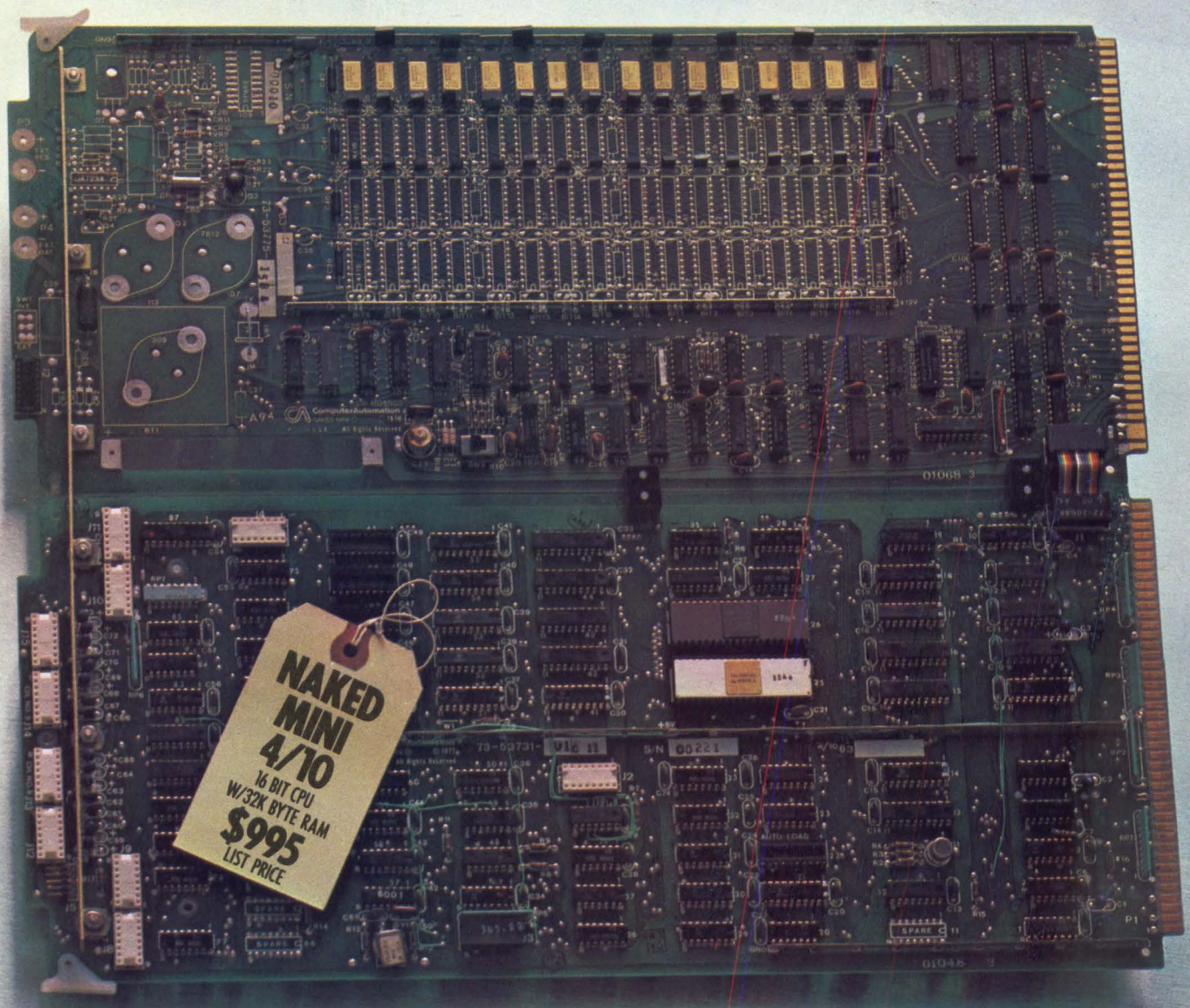
And If You're Looking at the Bottom Line. SA4000 drives are easy to integrate into your system. The drives utilize a simplified interface which can be easily designed into your system. In addition, you can use the same power supply for both the SA4000 drives and floppy drives, since they have the same voltage requirements. Want to get on-line quick? Our new SA4600 controller handles up to four SA4000 drives with an option to control up to four single or double density floppy disk drives. Bottom line? Lower overall system cost. So now's the time to design a classy system with the head of its class—the compact, reliable, low cost SA4000. Shugart Associates, Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 252-6860; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 17-60-06.

Shugart®

The Headstrong Company

CIRCLE 32 ON INQUIRY CARD

THE ONLY 32K BYTE COMPUTER FOR UNDER $1000. (QTY=1)



Our NAKED MINI 4/10 is a genuine price/performance breakthrough. For OEM quantity discounts that'll improve your bottom line even more, call one of the following sales offices: Santa Ana, CA, (714) 546-9550; Santa Clara, CA, (408) 985-6800; Denver, CO, (303) 399-1383; Orlando, FL, (305) 896-1440; Atlanta, GA, (404) 455-1649; Elk Grove Village, IL, (312) 860-1810; Waltham, MA, (617) 890-7190; Livonia, MI, (313) 261-5170; Bloomington, MN, (612) 854-2305; Bloomfield, NJ, (201) 338-8300; Greensboro, NC, (919) 294-5367; Cincinnati, OH, (513) 771-7530; N. Olmsted, OH, (216) 777-8700; King of Prussia, PA, (215) 265-5770; Nashville, TN, (615) 383-3315; Dallas, TX (214) 350-5681; Houston, TX, (713) 981-8859; Bethesda, MD, (301) 656-1217; Bellevue, WA, (206) 455-9650; or write us at 18651 Von Karman, Irvine, CA 92713.

ComputerAutomation
Naked Mini® Division

WHERE OEM'S COME FIRST.

CIRCLE 33 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

I/O System Interfaces Computer To Measurement and Control Signals

The series 500 measurement and control I/O system, announced by Neff Instrument Corp, 1088 E Hamilton Rd, Duarte, CA 91010, interfaces various types of I/O signals to a controlling computer using a single I/O assembly and only one of the computer's I/O ports. It accepts contact closures, voltage levels, and frequency inputs, as well as low level transducer signals via one of the analog systems. Outputs include contact closures, voltage levels, analog voltages or currents, and pulses for driving stepper motors.

Plug-in function cards configure the system for specific types of I/O signals. A serial controller permits operation of up to eight remote systems located up to 20,000 ft (6 km) from the computer to provide full distributed I/O capability. Expansion is possible at both local and remote sites.

Computer I/O circuits include a 4k RAM in which the computer stores scan lists and instructions required to control the peripheral devices. Data are transferred to computer memory on one DMA channel.

Circle 154 on Inquiry Card

Adaptable CNC Eliminates Inflexibility Problems of Some More Costly Systems

By eliminating problems of size, complexity, and inflexibility found in some other computer numerical controls, the 8138 Taskmaster becomes a cost-effective system. It is readily adaptable to fast, precise position control applications and can be used to direct a range of machine operations from linear interpolation in two or three axes to circular interpolation in two axes.

Summit/Dana, PO Box 1906, Bozeman, MT 59715 claims that modular design of this CNC makes it immune to obsolescence. Expansion can be accomplished by a simple substitution of circuit boards.

A standard system offers a 250-command memory and operator selectable resolution from 0.0001 to 0.001" (0.0025 to 0.025 mm), and 4-A/phase motor drivers. It operates in ambient temperatures as high as 50 °C.

Options provide 999-command memory, axis information display, backlash compensation, programmable canned cycles, absolute programming, step and repeat functions, automatic tool offsets, autocycles, linear and circular digitizing in the jog mode, 6-axis control, 8-A/phase motor drivers, and I/O interfacing for remote programming and external program storage in EIA or ASCII code. □

Circle 155 on Inquiry Card

Society for Information Display International Symposium

May 8-10
Chicago Marriott Hotel

Global progress in information display will be accented at SID 79. The symposium, to be held at the Chicago Marriott Hotel from May 8-10, will consist of 13 technical program sessions. Speakers from the U.S., Japan, Hungary, Germany, The Netherlands, and England will reveal recent developments in such topical areas as projection, graphic, fluorescent, and thermal displays and recording; garnet display components; diode laser optical disc recording; and liquid crystal, oscilloscope, and matrix displays.

Opening ceremonies, with welcoming remarks to be given by general chairman J. B. Flannery, Xerox Corp, and program chairman P. M. Heyman, RCA Laboratories, and SID Honors and Awards presentation will be preceded by the annual SID business meeting, conducted by B. J. Lechner, SID President. Highlighting this opening Ruth Davis, Deputy Under Secretary of Defense for Research and Advanced Technology, in her keynote address, will discuss the government's increasing need for display developments as witnessed by the unsatisfied needs of military users. In two invited addresses H. W. Tanka, of Tanka, Walder and Ritger, will speak on research and development policy and economic growth in Japan and J. A. Rajchman of Jan Rajchman, Inc, will discuss displays in the next decade, examining the expanded potential attributable to LSI developments and exploring possible routes open for future developments.

Two parallel discussion panel sessions are scheduled for Tuesday evening. The panelists will demonstrate and assess hardware and software technology trends in home displays and appraise design options in display electronics. Cameras and recorders will not be permitted in the session halls.

Held on Monday, May 7 and Friday, May 11, the annual tutorial seminars will be co-hosted by the University of Illinois Electrical Engineering Department. Eight lectures, two each morning and two each afternoon, will focus on technology developments including phosphors for high contrast CRTs, advances in electron optics that are leading to improvements in spot quality and color, and liquid crystal display optics. Each group of two seminars will be followed by a short, audience/speaker interactive discussion. Advance registration for the seminars is required. Fees are $110 for both days or $70 for one day.

In the evenings, following the formal talks, attendees will have an opportunity to meet face-to-face with speakers. Tuesday evening, the exhibitors will host a social hour in the exhibit area. Wednesday evening, the Lake Forest College campus will be the scene for a cocktail hour, buffet dinner, and lecture on holography. There is an additional $18 fee for the Lake Forest College evening.

A copy of the SID *Digest of Technical Papers,* which features 800- to 1000-word illustrated condensations of all contributed papers, is included in the Symposium fee of $45 for members and $60 for nonmembers. For more information, contact Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134.

Details of the advance program that follow reflect information available at press time.

TECHNICAL PROGRAM EXCERPTS

Tuesday Afternoon

Session 6 **3:40-5 pm** **Ballroom I**

Display Systems

Chairman: T. P. Sosnowski, Bell Laboratories

"Relationship between Display Parameters and CRT System Cost," W. R. Elliott, Boeing Aerospace

An explicit expression identifies the cost of the usually specified display system performance requirements. One factor to be assessed is the contribution of deflection power to the cost of vector CRTs.

"Distributed Intelligence in a Graphics Display System," J. Hatvany and P. Verebely, Computer and Automation Institute of the Hungarian Academy of Sciences, Hungary

An interactive vector-type graphic display family is based on a modular architecture. Graphic functions are distributed between microprocessors by an internal communication system with intensive use of multiprocessing methods.

Session 7 **2-5 pm** **Ballroom II**

Nonimpact Printing

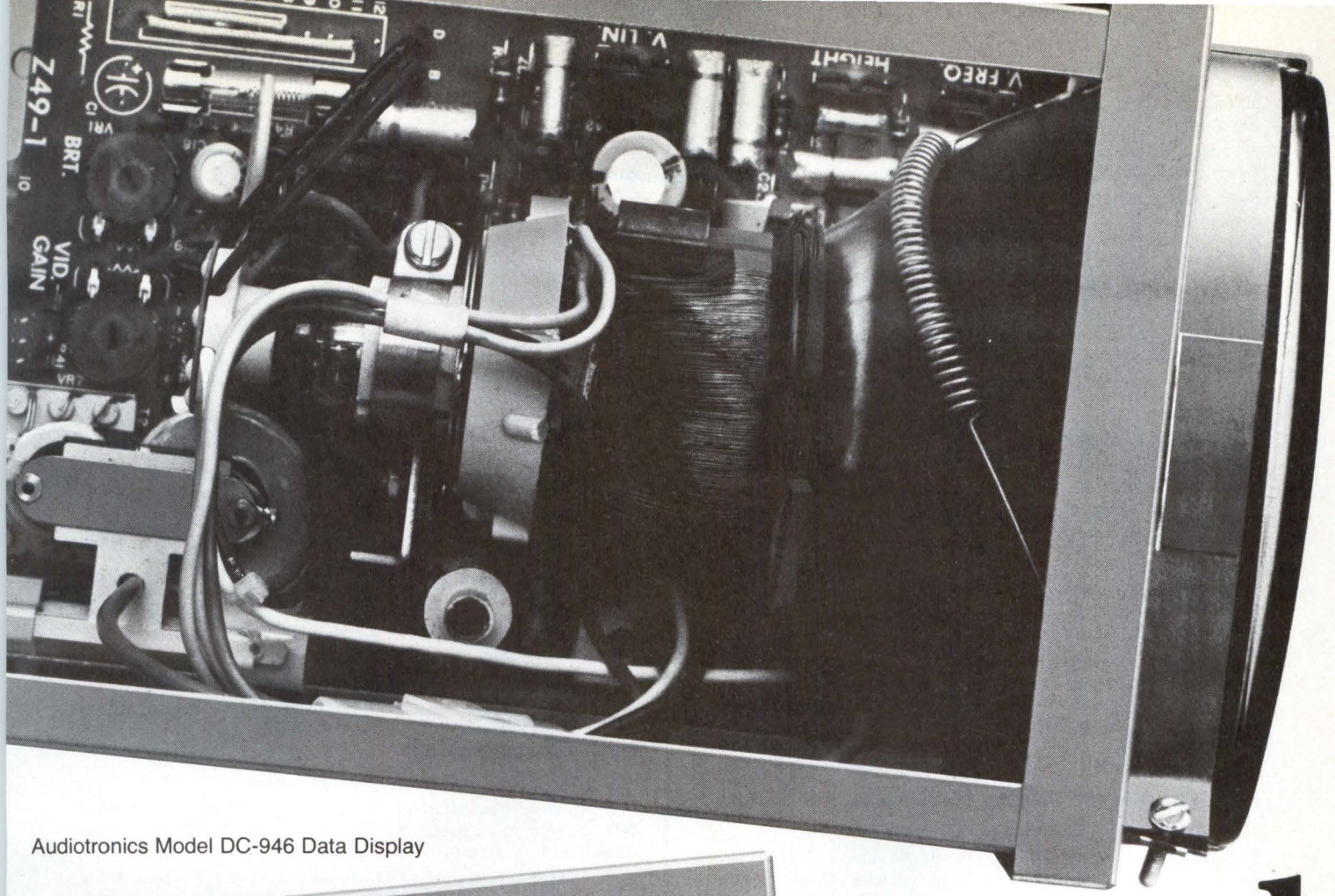
Chairman: L. G. Biggs, Tektronix, Inc

"High Speed Thermal Recording," K. Saito, *et al,* Oki Electric Industry Co, Ltd, Japan

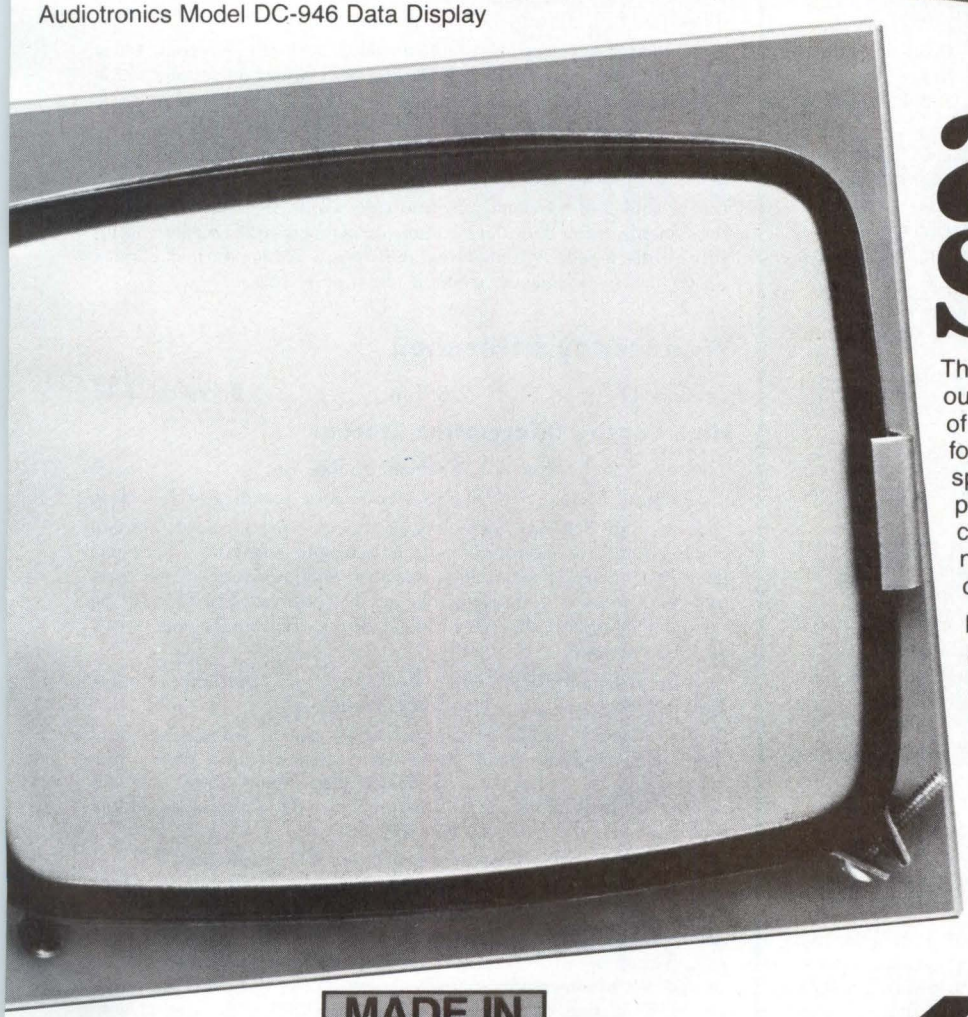
A high speed thermal recorder with the ability to record lines in less than 10 ms uses parallel drivers to heat the head elements instead of multiplexing them.

"Analytical Design Method of Ink Jet Printing," R. Takano, NTT Yokosuka Elec Comm Labs, Japan

Conditions for realizing high speed reliable ink jet printing, analyzed in terms of the ink droplet forming mechanisms,



Audiotronics Model DC-946 Data Display



actual size

This popular Audiotronics data display is one of our 48 standard models. We have sold thousands of them to giants in the industry. Maybe it's perfect for your requirements. If not, talk to us about your specifications. We're dedicated to innovative product design, quality production standards and complete customer satisfaction. Whatever you need, we have the experience and talent to design it, or improve it. Contact us today.

Model DC-946 features:

- modular construction
- 5″ cathode ray tube (12.7 cm)
- solid state
- DC operation—12V dc inputs
- choice of signal inputs:
  TTL (standard)
  Composite video (plug-in module)
- standard 15,750 KHz horizontal scan frequency
- 650 lines resolution

MADE IN ☆☆☆☆☆ AMERICA

AUDIOTRONICS
VIDEO DISPLAY DIVISION
530 FIFTH AVENUE N.W. NEW BRIGHTON, MN. 55112 · (612) 633-3131

CIRCLE 35 ON INQUIRY CARD

mosaic dot size, and beam deflection characteristics, will be discussed.

"Printing Speed of an Electrophotographic Laser Beam Printer Using Overcoated Photoreceptors," A. C. Wu, Sycor Inc

From experimental results for various settings of ac and dc corona devices in a laser beam nonimpact printer using an overcoated photoreceptor the optimum printing speed of printer can be determined.

"Stylus Writable Electrophoretic Display Device," A. Chiang, *et al*, Xerox Research Center

An electrical stylus writable electrophoretic (SWEP) device produces multipixel, large information content images without requiring a threshold medium or integrated switching elements.

Tuesday Evening

Evening Panel 1 **8 pm** **Ballroom I**

Home Displays—Not for TV Only

Moderator: C. N. Judice, Bell Laboratories

Panelists: P. Hughes, National Semiconductor Corp; L. Schwartz, Bell Laboratories; R. Clark, Communications Studies and Planning Co, England; T. Shipchandler, Texas Instruments, Inc; D. Pinsky, Interstate Electronics Corp

Application of hardware and software technology towards introducing new computer based services into the home will be assessed. To emphasize reality rather than speculation, displays of the future will be demonstrated.

Evening Panel 2 **8 pm** **Ballroom II**

Requirements for Display Electronics

Moderator: E. R. Strandt, Delco Electronics

Panelists: D. Bell, Signetics Corp; P. A. Curran, Texas Instruments; B. Dellande, Motorola Semiconductor Products Corp; T. Leeder, Fairchild Optoelectronics Div; D. Nerge, National Semiconductor Corp; G. R. Seaton, Dionics, Inc; and P. Emerald, Sprague Electric Corp

The design engineer generally has several options in selecting a given display technology for a specific application; each requires different driver and data processing facilities. The complexity of the associated electronics limits the designer's options. The panel will discuss aspects of these and how to meet design and cost objectives.

Wednesday Morning

Session 8 **9-11:45 am** **Ballroom I**

Flat Panel Technology

Chairman: L. E. Tannas, Jr, Hycom, Inc

"A Vertical Self-Shift Plasma Display Panel," S. Sato, *et al*, Fujitsu Laboratories, Ltd, Japan

Operating principle and panel characteristics of ac plasma display facilitates editing and tabulation, while retaining driving circuitry simplicity inherent to the self-shift technique.

"A 240-Character Vacuum Fluorescent Display and its Driving Ability," K. Kasano, *et al*, Ise Electronics Corp, Japan

Microprocessor driven 240-character display with ⩾200-fL brightness includes multilayer substrate of Al-thin-film conductors and a glass thick-film insulator.

"Thin Film Transistor Switching of Thin-Film Electroluminescent Display Elements," S. K. Kun, *et al*, Westinghouse Electric Corp

Low voltage TFEL compatible with TFTs will be discussed, citing operating characteristics, and applicability to high contrast, high brightness displays.

"Multi-Mode LED Display Program," K. T. Burnette and W. Melnick, Bunker-Ramo Corp

Progress will be reported on the development of a modular flat panel LED flight display. A 4 x 3″ (10 x 8-cm) concept demonstrator display, assembled from 1 x 3″ (2.54 x 8-cm) modules of green GaP, 64 element/in (25/cm), 0.25″ (6.35 mm) square monolithic LED arrays will also be covered.

"Metal-Elastomer Display Connectors," L. S. Buchoff, Hulltronics

A connector technology makes it possible to economically design a large number of closely spaced contacts (2 mils w x 4 mil centers). Metal paths bonded to an elastomer base are the contact pads and interconnections.

Session 9 **9-10:40 am** **Ballroom II**

CRT Technology

Chairman: C. Infante, Tektronix, Inc

"CRT for Displaying Nanosecond Transients," B. Janko, Tektronix

An 8 x 10-cm microchannel plate electron multiplier is an integral part of CRT for oscillographic display of fast transient signals. Viewing and photographic recording of transient signals with writing speed in excess of 3×10^{10} cm/s has been demonstrated.

"Log Taper Magnetic Deflection," C. Sawyer, Display Components, Inc

In high speed computer driven CRT displays, deflection power, and therefore efficiency, are at a premium. Yoke-glass bulb interface and development of an optimal geometry will be analyzed.

"Non-Glare Concave Surface CRT," E. Miyazaki, Matsushita Research Institute, Japan

By using a concave faceplate with an appropriate radius of curvature, reflections can be made inconspicuous.

Session 10 **10:55-11:45 am** **Ballroom II**

Transmission Displays

Chairman: I. F. Chang, IBM Research Center

"Transmissive Electrochromic Display with a Porous Crystalline WO_3 Counter Electrode," K. Matsuhiro and Y. Masuda, Asahi Glass Co, Ltd, Japan

A transmissive electrochromic display, uses an electron beam deposited and heat treated WO_3 film as counter electrode which is porous, crystalline, and has little optical absorption and excellent reversibility in charge injection and liberation.

"Thin-Film Iron Garnet Display Components," B. Hill and K. P. Schmidt, Philips Research Laboratories Germany

Linear and 2-dimensional electronically controlled passive display components using Faraday-rotation in magneto-optic memory films will be discussed. A film, integrated into a 35-mm format display wafer, has been imaged using a slide projector.

Wednesday Afternoon

Session 11 **2-5 pm** **Ballroom I-II**

High Density Information Storage

Chairman: J. L. Simonds, Eastman Kodak Co

"Solid-State Storage for Display," H. Chang, IBM Research Center

Bubbles and CCD are high density, low power, low cost storage devices that are suitable for terminals and displays. Characteristics of presently available modules and projections for cost and performance improvements in the coming decade will be reviewed. Magnetic disc and optical disc storage technologies will also be assessed.

"Diode Laser Optical Disc Recorder," K. Bulthuis, Philips Research Laboratories, The Netherlands

A high density recording and retrieval system using a gallium aluminum arsenide diode laser writes information on a pregrooved double sided 12″ (30.5-cm) disc which allows readout of any address in a mean-time of 250 ms, thereby providing virtually instant access to 5×10^9 bits.

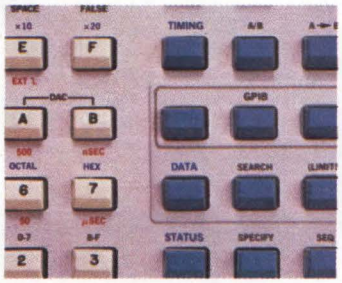
"High Performance Optical Disc Recording Structures," R. A. Bartolini and A. E. Bell, RCA Laboratories

Many high density optical recording systems require storage media capable of high recording sensitivity and high playback SNR. Thin-film antireflection recording structures provide the required performance for an optical video disc system. The design and optimization of these structures are suitable for use in conjunction with a wide variety of optical recording media.

Biomation's K100-D-- no other logic analyzer even comes close.

No wonder the K100-D is our fastest selling new logic analyzer ever. It gives you 16 channels, 1024 word memory, clock rates up to 100 MHz, signal timing resolution to 10ns-plus a built-in display and keyboard control.

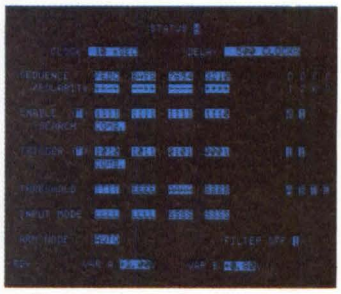
Biomation's K100-D puts it all right at your fingertips — more performance and features than any logic analyzer ever.



It starts with the microprocessor-controlled keyboard and interactive video display. To give you fast, precise control, the display serves as a comprehensive control status menu, with all selectable parameters in reverse video. There's a single, labelled key for each function, corresponding directly to status display choices. So guesswork is eliminated.

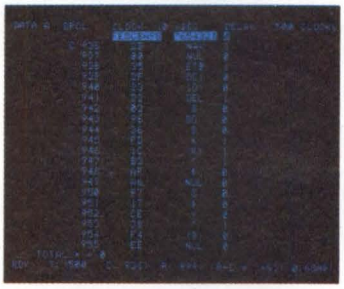
For example, in the data domain, you can direct the display to read in hexadecimal, octal, binary or ASCII, or any combination, by selecting one of four control buttons. There's also a unique "sequence" key that enables you to rearrange the order in which channels are displayed, to aid in data decoding, to simplify side-by-side comparison of timing signals and to enable you to cancel any channels you're not interested in seeing. A separate key controls horizontal expansion.

That gives you an idea of the K100-D's display versatility. Here's a picture of its astounding capture capability.



By providing timing analysis of signals as fast as 100 MHz, you can capture logic signals with resolution to 10ns. And the 100 MHz clock rate protects against obsolescence as the speed of your systems gets faster and faster. The K100-D also has a latch mode that can capture glitches as narrow as 5ns.

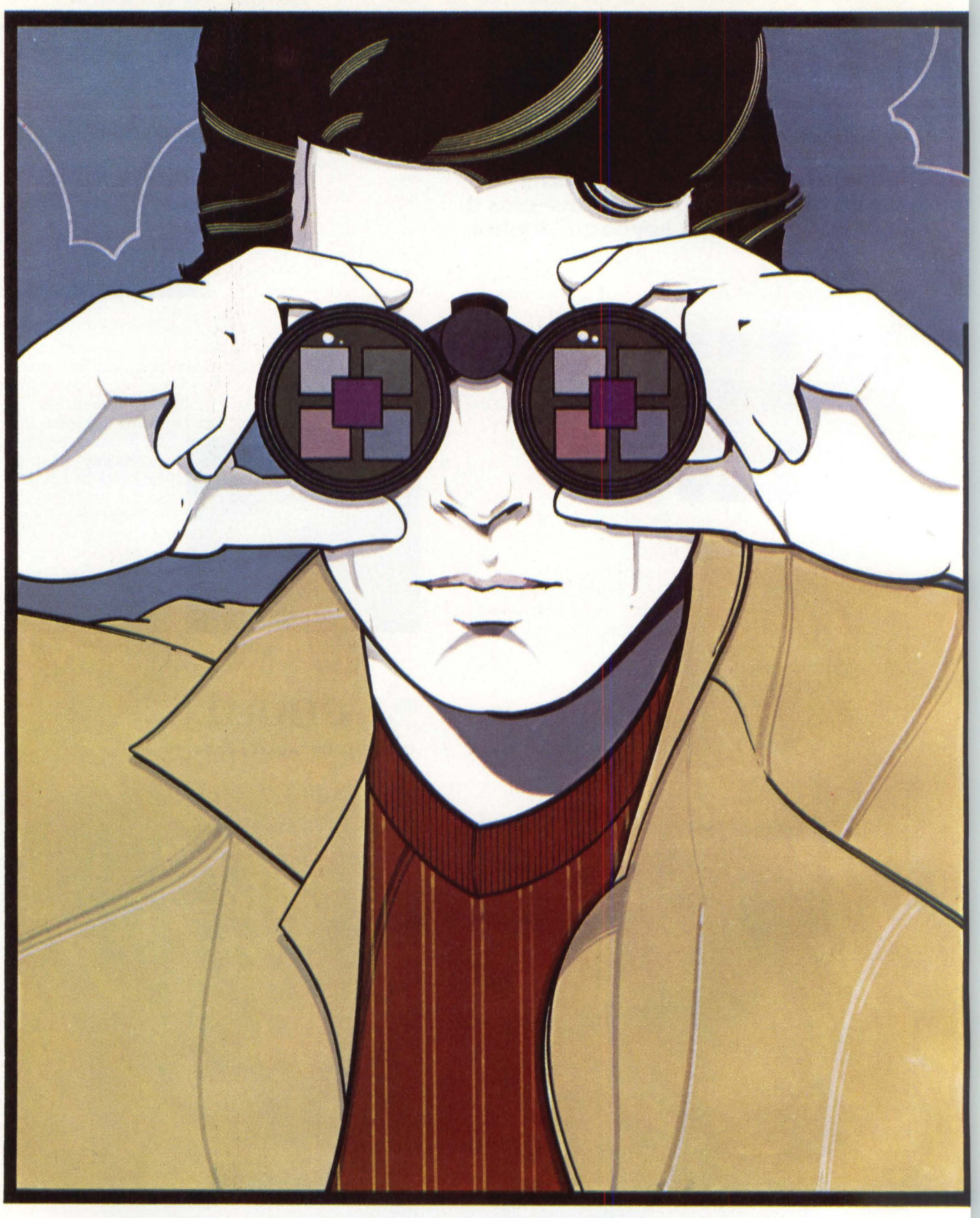
With the 32-channel input adapter, the K100-D is ideal for exploring the new world of 16-bit microprocessors. To give you unprecedented analysis capability, there's a built-in Auto Stop capability you can use to detect, record and display any match (or mismatch) between incoming data and previously recorded data held in a reference memory. Or using Search Mode you can key in a specific word and the K100-D will find it in memory.



To get the full impact of the K100-D, you really do need to have it at your fingertips. That's why we would like to arrange a demonstration. Call us at (408) 988-6800. Or, for more information, write: Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050.

GOULD

CIRCLE 36 ON INQUIRY CARD



The Future Has Arrived.

Intel delivers the 8086. Powerful. Practical. And the Architecture of the Future. Here today.

We have seen the Future and it is called 8086. Even better, it's here today. Our new 16-bit microcomputer is an architectural triumph, introducing designers to a new world of system expansion capability, high-level language programming and dramatically increased system thruput.

Why we call it "The Future"

To deliver the Future, we designed the 8086 with a totally new architecture, super-efficient for implementing high-level, block-structured languages such as Pascal and PL/M-86.

The 8086 addresses up to a full megabyte of system memory with new addressing modes and efficient register utilization that totally support such minicomputer-like capabilities as relocatable and re-entrant code and instruction look ahead.

And the 8086's powerful new instruction set includes both 8-bit and 16-bit multiply and divide in hardware, with efficient byte string operations and improved bit manipulation.

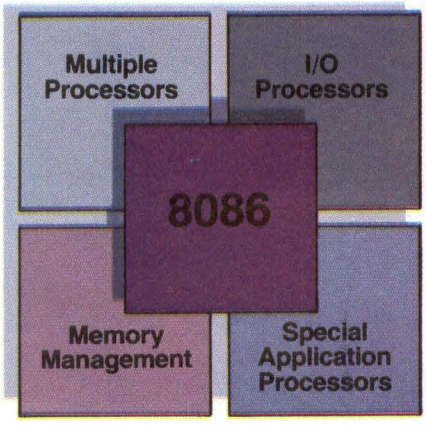
We're committed to delivering the industry's highest performance, today and into the future. The 8086's architecture maximizes system thruput today by delivering ten times the processing power of its 8-bit predecessors. Planned expansion promises another order of magnitude increase in performance through the addition of I/O processors, special instruction set extension processors, memory management and distributed intelligence configurations.

System components for expanded multiprocessor applications are available right now, supporting the Multibus™ architecture in timing, control and drive levels. They include 8288 Bus Controller, 8282/8283 Octal Latches and 8286/8287 Octal Transceivers.

Get a jump on the future.

8086 is the most successful new microcomputer ever. The list of major market leaders who have evaluated 16-bit machines and chosen the 8086 is staggering.

One reason for the 8086's success is our commitment to *your* success. We've made the 8086 the industry's best-supported microcomputer. The cpu, interrupt controller and six additional support circuits are on distributors shelves, with more on the way. You can take advantage of the 28 existing Intel® peripheral interfaces. Our 2716 (16K) and 2732 (32K) EPROMS provide programming flexibility and unique features for 8086 users, including protection against bus contention.



And we complete your system with a variety of off-the-shelf +5 volt MOS RAMs.

You can begin hardware/software development today, using the Intellec® Microcomputer Development system with ICE-86™ in-circuit emulation, PL/M-86 and ASM-86 for assembly language programming and 8080/8085 software conversion.

SDK-86, a complete system design kit including all essential components, makes it easy to begin prototyping without delay.

For an additional head start, iSBC 86/12™ single board computer brings the power of the 8086 to the Multibus with a fully assembled and tested 16-bit system.

The Future belongs to you.

Get to market first and capture a piece of the future for your product. You can order the complete 8086 family from your distributor. Or, for more information, contact your local Intel sales office or write: Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

See us at ELECTRO '79, New York City, April 24-26.

The Cook-able Computer

Introducing a ruggedized version of Intel's iSBC* 80/10A Single Board Computer

From Cryogenics to Hades

Our ruggedized SECS 80/10A likes it hot — or cold. It shrugs off shock, vibration, moisture. And thrives on dust, dirt and grime.

Meets MIL-E-5400, 16400, 4158 — and more. This makes our SECS 80/10A perfect for military systems and tough industrial applications — petroleum, steel, oceanography, communications.

In fact, anywhere a rugged microcomputer is needed.

Functional counterpart of Intel iSBC 80/10A

Exclusively licensed by Intel, our SECS (Severe Environment Computer System) is a functional counterpart of the standard iSBC 80/10A board. Even uses the same development system software.

*Trademark of Intel Corporation

The difference is in the packaging

Our SECS 80/10A, which uses rugged Intel 883B chips, is mounted on a 9″ by 6″ shock and vibration resistant, full ATR compatible board. Conduction cooled, it operates from −55°C to +85°C. Add our numerous support modules and you end up with a versatile severe environment microcomputer system at a fraction of the development cost.

Other SESCO products

We also have a complete line of MIL SPEC core and semiconductor memories. New products include D-DAS, a digital data acquisition system for the 1553 bus, and SETS, a compact digital tape recorder with 23 megabit capacity.

When you're faced with a tough environment, "buy SESCO... it works!"

SECS 80/10A

SESCO
Severe Environment Systems Company
A Subsidiary of Electronic Memories & Magnetics Corporation

20630 Plummer Street • P.O. Box 668 • Chatsworth California 91311
Telephone: (213) 998-9090 • Telex: 69-1404

"Replication of Optical Discs," D. G. Howe, *et al*, Eastman Kodak Co

Full bandwidth NTSC video signals, laser recorded in thin metal films evaporated on glass or plastic substrates, have been photographically replicated. The replicas of submicron spots in 2-μ layers using positive density images are tolerant to poor optical contact during replication and essentially immune to handling or cleaning damage.

Thursday Morning

Session 13 9 am to 12 noon Chicago Ballroom D

Liquid Crystal Displays

Chairman: A. R. Kmetz, Bell Laboratories

"General Theory of Matrix Addressing Liquid Crystal Displays," M. G. Clark, Royal Signals and Radar Establishment, England

Analysis of matrix addressing of an rms responding display covers both binary and multilevel addressing waveforms. The method in the multilevel case can be extended to grey scale displays.

"Addressing Methods for Non-Multiplexed Liquid Crystal Oscilloscope Displays," I. A. Shanks and P. A. Holland, Royal Signals and Radar Establishment, England

Addressing method directly drives X-Y matrix LCDs to display single-valued functions such as oscilloscope waveforms.

"Storage-Type Liquid Crystal Matrix Display," C. Tani *et al*, Nippon Electric Co, Ltd, Japan; and O. Kogure, NTT Ibaraki Elec Comm Lab, Japan

Switching of the relaxation transient of the nematic-cholesteric phase change between a wide angle scattering and a clear quiescent state will be reported. The approach has made it possible to produce low power storage type matrix LCDs up to 306 x 574.

"512-Character Display of Reflective Twisted Nematic Liquid Crystal by Two-Frequency Addressing," M. Hosokawa, *et al*, Suwa Seikosha Co, Ltd, Japan

Two-frequency addressing of a 56-line twisted nematic display using an improved material which affords a reflective high contrast and wide viewable angle characters will be reported.

"Properties of a Display Device using Depolarization in Twisted Nematic Liquid Crystal Layer," T. Uchida, *et al*, Tohoku University, Japan.

Twisted nematic layer device with depolarization provides a wide angle for viewing and has high contrast, sharp threshold, and fast response and recovery.

"An 80-Character Alphanumeric Liquid Crystal Display System for Computer Terminals," K. Odawara, *et al*, Hitachi Ltd

A 1-row, 80-character 5 x 7 dot matrix alphanumeric liquid crystal display system with twisted nematic mode uses a CMOS controller and CMOS 40-stage drivers.

"Reflective and Positive Mode Color LCD using Cholesteric-Nematic Phase Change Type Guest-Host Effect," T. Ueno, *et al*, Nippon Electric Co, Ltd, Japan.

A cholesteric dye display with dark characters on an electrically driven light background will be described.

SEMINAR DISCUSSION EXCERPTS

Monday Morning

Moderator: H. Gene Slottow, University of Illinois

Session 1 8:30-10 am Chicago Ballrooms F/G

Nonscattering Liquid Crystal Display Optics

Dwight W. Berreman, Bell Laboratories

Liquid crystal thickness, optical anisotropy, elastic constants and surface anchoring affect the speed and viewing angle, contrast, gray scale, and multiplexibility of nonscattering liquid crystal displays. These effects and adjustability of parameters will be discussed.

Session 2 10:30 am-12 noon Chicago Ballroom F/G

Advances in Printing

Keith S. Pennington, IBM Research Center

The data processing and office products markets have an increasing need for printing products with improved reliability, cost/performance, and overall functional capabilities. This lecture will review the major trends and functional requirements in these areas of printing, citing the current state-of-the-art and nonimpact printing technologies.

Monday Afternoon

Moderator: I. Chang, IBM Research Center

Session 3 1:30-3 pm Chicago Ballrooms F/G

Electron Optics in CRTs

Robert G. E. Hutter, Polytechnic Institute of New York

Recent developments in the design of electron guns and deflection yokes leading to better spot quality and improved color displays will be described. Examples will illustrate the utilization of the computer in solving design problems

Session 4 3:15-4:45 pm Chicago Ballrooms F/G

New Phosphor Developments for High Contrast CRT Displays

Robert A. Buchanan, and T. Brant Maple, Lockheed Research Laboratory

New thin film materials are making it possible to produce CRT displays with ever-increasing contrast. In this address, the properties of presently available luminescent films will be presented, along with background and analytic material.

Friday Morning

Moderator: Walter Goede, Northrop Electronics Div

Session 5 8:30-10 am Chicago Ballrooms F/G

Plato IV System Architecture: A Case Study of the Organization of Software and Hardware in Interactive Computer Systems

Robert K. Rader, Software Group, University of Illinois

The Plato IV system was designed to run thousands of interactive graphics terminals for use in an educational setting. Design and implementation of this system will be discussed and concepts demonstrated, stressing the integration of software and hardware elements into the system, and the software structures that determine the interactive characteristics of the system.

Session 6 10:30 am-12 noon Chicago Ballrooms F/G

The Use of Synthetic Speech in Interactive Computer Systems

Bruce A. Sherwood, University of Illinois

This lecture will demonstrate the ease with which synthetic speech output can be added to interactive programs, citing its application to computer based education. Techniques of compressed digitized speech and recorded audio will also be demonstrated.

Friday Afternoon

Moderator: Aris Silzars, Tektronix, Inc

Session 7 1:30-3 pm Chicago Ballrooms F/G

Intelligent Terminals

F. H. Dill, IBM Research Center

Inclusion of microprocessors in CRT terminals is an attribute commonly called intelligence. The talk will attempt to classify present terminals by function and capability, look at future possibilities based on developments in microprocessors, memory and storage, and discuss some of the problems associated with terminals intelligence. □

We heard you and...

HERE IT IS! A SMART APL *TELERAY* with...

...High-Resolution APL overstrikes

Five years of listening to thousands of APL users told us to give you the new Teleray Model 11. Its true overstrike, programmable wide-character display and "instant character replay" give you the most versatile APL/ASCII terminal yet available . . . and

And... 32 Programmable Functions

Call up forms and function sequences, answerbacks, in any combination, plus more programmable features than ever before . . . and

And...Mail-in Super Service

Direct-mail servicing, from your operating station to our Service Dept. with no middleman. No-tools, snap-in modules replace in 60 seconds, and reusable mailers get your modules back and forth to you without expensive service calls. Call us toll-free for any service help you need . . . and, so . . .

SEE MODEL 11 AT INTERFACE '79

Call for immediate info!

TELERAY Sales Offices:

(201) 652-7055	(301) 589-2802	(412) 243-8421	(613) 225-0411
(201) 944-1600	(303) 279-7796	(416) 622-6752	(617) 459-2578
(203) 623-5352	(305) 421-4989	(503) 292-3505	(713) 780-2511
(205) 881-9298	(305) 645-3444	(512) 451-5174	(714) 273-4771
(206) 641-6444	(312) 655-0040	(512) 828-0937	(714) 552-7850
(212) 947-0379	(313) 354-6421	(513) 223-8421	(716) 381-4120
(213) 328-9770	(404) 955-0293	(518) 587-2313	(801) 969-4034
(214) 661-0300	(405) 528-6071	(602) 968-5962	(808) 523-1326
(216) 585-8421	(408) 744-1930	(612) 535-5330	(919) 883-9125

TELERAY
DIVISION OF
RESEARCH INC
BOX 24064 MINNEAPOLIS, MINNESOTA USA 55424
PHONE (612) 941-3300

PROCESSOR ARCHITECTURE ANTICIPATES FUTURE PERFORMANCE REQUIREMENTS

Design of Series/1 processors and their relationship to instruction set, interrupt structures, and I/O interfacing are primary determinants of system performance and have a major influence on the machines' life cycle

Richard E. Birney IBM Corporation, General Systems Division, Boca Raton, Florida

Aimed toward realtime, sensor based, and distributed data processing applications, design of IBM Series/1 computer logic evolved from a planned iterative development process. A base architecture—established from design goals and performance specifications—was benchmarked against similar competitive and existing corporation computers. Benchmarking included both kernel analysis and engineering investigations of such design criteria as execution times, code and storage efficiencies, coding productivities, and system costs. Many iterations were implemented during the design evolution, and final decisions were based upon detailed information produced by hardware and software benchmarks. Simultaneously affecting the iterative process was an important set of distinctive factors that emphasized near- and long-term trend characteristics in the prevailing and expected growth of small computer systems with regard to technology, architecture, software, and integrity.

Basically, modular Series/1 computers provide 16-bit general purpose architectures with direct storage addressing to 64k bytes, and expansion to 16M bytes. These architectures offer a choice of central processor designs, proven bipolar large-scale integrated (LSI) logic, and metal-oxide semiconductor field-effect transistor (MOS FET) n-channel memory. A versatile instruction set handles basic bit, byte, word, double word, and four word (floating point) operands. Instruction length is variable from one to three 16-bit words, depending upon any one of 11 addressing modes. Also incorporated are indirect addressing, with either pre- or post-indexing, and several additional complex addressing formats. Input/output (I/O) interfacing allows direct program control, preemptive priority interrupt, and cycle stealing. Comprehensive error checking and reporting are accomplished cooperatively between I/O devices and the processor channel.

Central Processors

In implementing the two central processors—the 4953 and the more powerful 4955—a 16-bit architecture was chosen to provide high performance systems at low cost (Table 1). Comparisons made between similar program development library functions in 32-bit and 16-bit architectures generally revealed a greater than 20%, and occasionally as high as 40%, savings in the amount of storage required to code equivalent functions with a 16-bit architecture. In addition the 16-bit width reduces product cost by using fewer pins and smaller cards for equivalent functions. Main storage savings plus reduced package constraints are directly reflected in the cost to perform a function.

TABLE 1

Comparison of Major Processor Performance Characteristics

Characteristic	4953	4955
Performance	135k instructions/s	367k instructions/s
Maximum Storage	64k bytes	256k bytes
Interrupt Levels	4	4
Floating Point Processor	No	Optional
Address Translator	No	Optional
Program Console	Yes	Yes
Logic Cards	1	3
Maximum Channel Rate	1.3M bytes/s	1.6M bytes/s
Storage Cycle Time	800 ns	660 ns

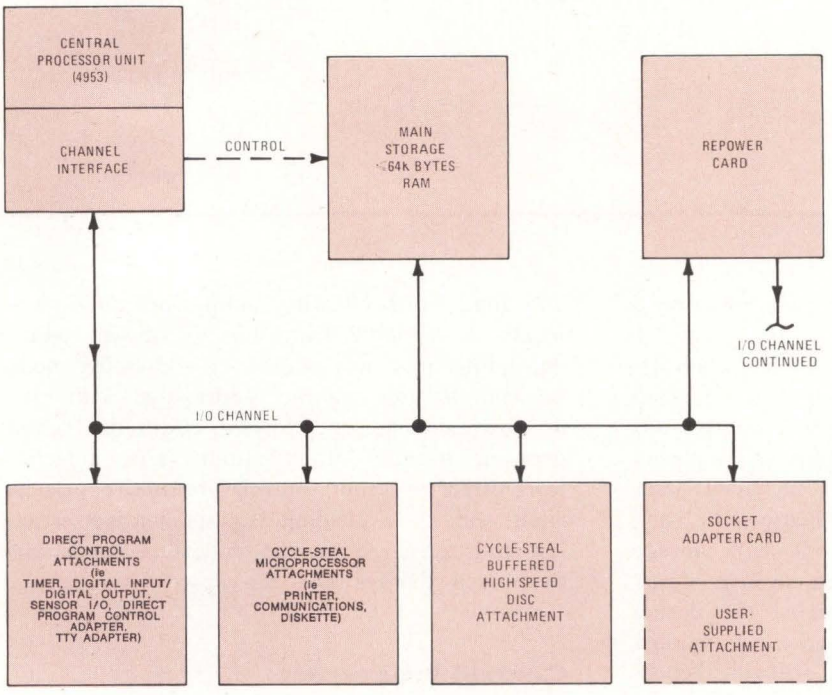


Fig 1 Single bus processor design. Storage for up to 64k bytes resides on I/O interface. Selection of I/O devices is available along with repower capability to extend channel to additional I/O devices

Direct main storage addressability of 64k bytes is sufficient for a large segment of small computer applications; however, for larger tasks, this storage address limitation becomes a severe system restriction. To overcome the addressing constraint and yet retain the storage efficiency of the 16-bit architecture, an address translator is used to extend the main storage addressability of the 4955 to 16M bytes. The address translator supports eight simultaneously mapped address spaces and is designed to simplify communication between address spaces, in contrast to more common address extension mechanisms. During execution of a particular instruction, three address spaces may be accessed. For example, the translator allows execution of a storage-to-storage move with the instruction fetched from one address space, the source operand from another, and the destination operand stored in a third location.

The 4953 processor design trades off cost and performance features. Single bus architecture (Fig 1) allows low complexity in processor design by eliminating special interfaces to main storage. Since either storage or I/O fits easily onto the single bus, the system can be configured for any storage size without the cost penalty of unused card slots in the processor module. The disadvantage of this bus concept is that I/O activity impacts the central processor unit's (CPU's) ability to access storage, resulting in contention between I/O and CPU; subsequently, lower performance occurs within the processor when the channel is cycle stealing at full bandwidth.

Operating with approximately three times the internal performance of the 4953 CPU, the 4955 processor uses a separate storage bus to minimize contention between CPU and cycle-stealing I/O for main storage cycles (Fig 2). The CPU is designed so that the maximum I/O data rate of 1.6M bytes/s consumes approximately one-half of the 3.0M-byte/s storage bus bandwidth; the remaining storage bandwidth is reserved for CPU cycles. This design implies that channel loads have little effect on CPU performance and that no "lockout" of the processor from main memory occurs because of I/O activity. Although storage may not reside on the I/O bus of the 4955, the same I/O adapters may exist on either CPU.

System and Level Registers

Within the processor architecture, two categories of registers exist: system registers and level registers. System registers contain system wide information used by the operating systems and appear singularly within the processor. Level registers are used by a task in process at a particular priority level and are replicated for each interrupt level. This structure provides general purpose registers for ease of programming while replicating these registers on priority levels for fast interrupt response.

System registers can be accessed by a program only when the CPU is operating in privileged state (in other

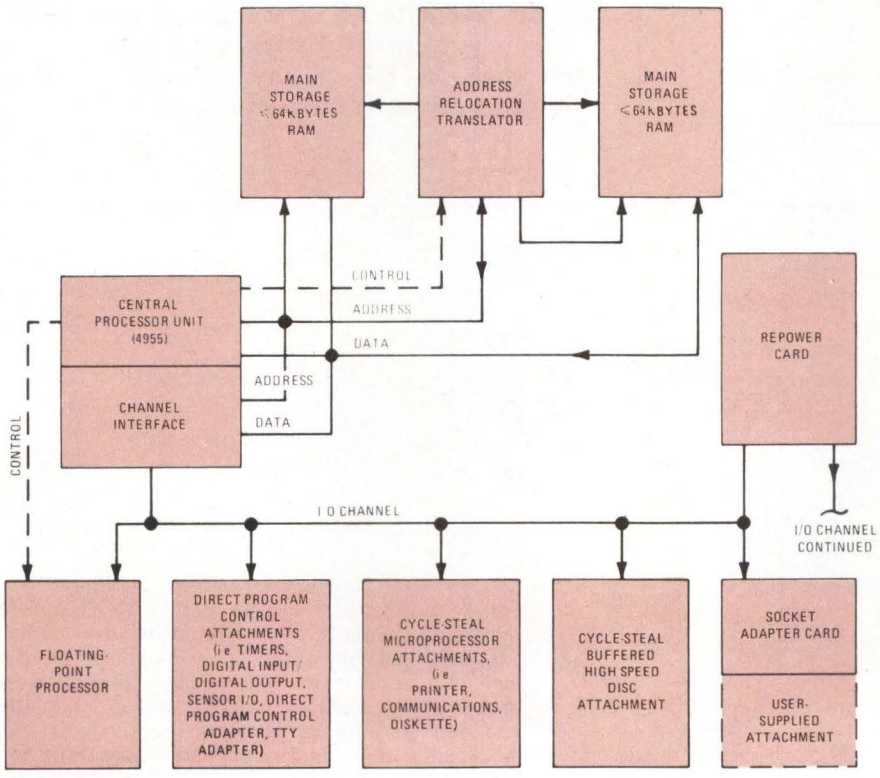


Fig 2 Separate storage bus processor design. Using address translator, storage for up to 256k bytes is available. Fourteen I/O attachments may be fitted prior to repowering channel interface

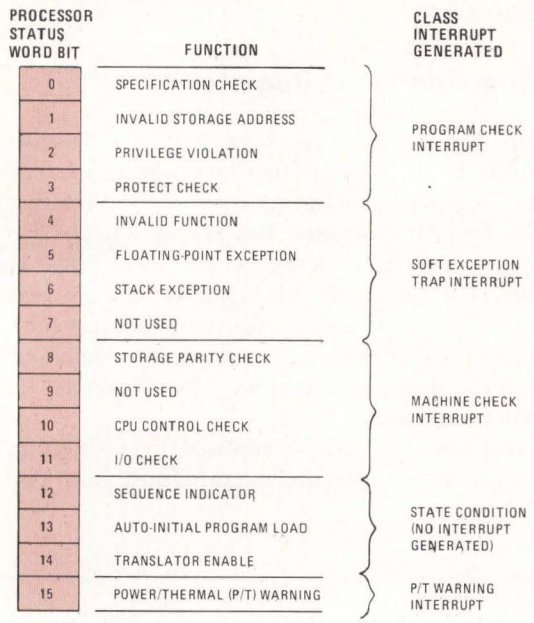


Fig 3 Processor status word register. Register records errors and exception status. Type of error generates corresponding interrupt, allowing system software to handle fault condition

words, by the operating systems). The most important system register is the Processor Status Word (PSW). This 16-bit register (see Fig 3) records errors and exception conditions in the processor that must be handled by the operating system.

Extensive error checking is evidenced within the processors by noting the bit conditions reported in the PSW. The program check interrupt lists errors detected in software. The soft exception trap interrupt lists exceptions where no error has occurred but where software intervention is required; for example, a stack overflow requires that more storage be allocated to the stack. Machine checks are hardware errors detected by internal circuits. Remaining bits indicate state conditions and power/thermal interrupt within the processor.

Level registers are replicated on each priority level and are also called Level Status Blocks (LSB). The LSB (Fig 4) contains the execution time essence of a task and is available to the program in execution. Registers within the LSB and their functions are

Instruction Address Register—Contains address of next instruction to be executed.

Address Key Register—Contains key used for address translation and storage protection.

Level Status Register—(LSR) Contains data relative to status of a task. Results of arithmetic or logical operations are set within bits 0 to 5 in this register and are used when branching based upon certain conditions. Bits 8 to 11 of the LSR indicate whether the task is in supervisory state, being traced, presently in execution, or has all interrupts masked. Remaining bits are reserved for future expansion.

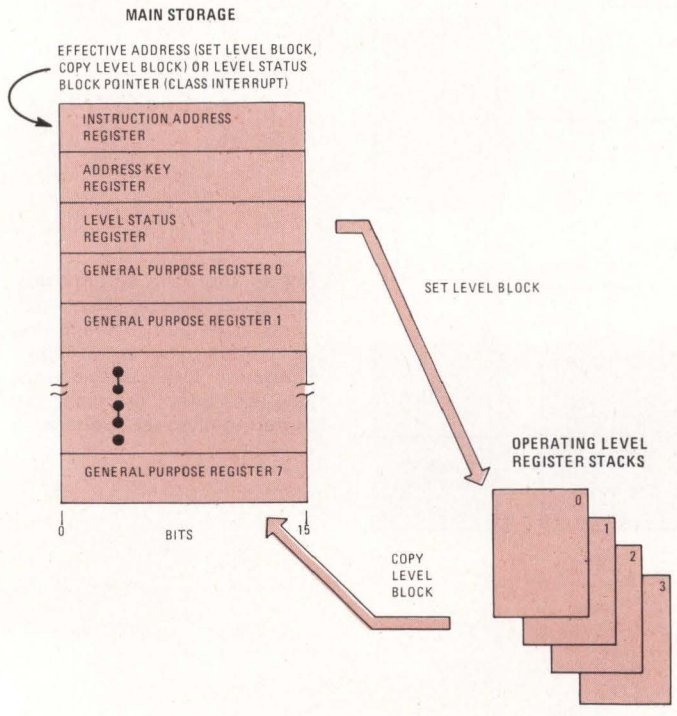


Fig 4 Level status blocks. Set of 16-bit registers replicated on each priority interrupt level contains execution time environment of particular program, including address of instruction in execution, addressing keys used by program, status information, and general purpose registers. Level status block is capable of being loaded and stored from main storage with set level block (SELB) and copy level block (CPLB) instructions

TABLE 2

Major Functions of Instruction Set

Operation	Data Type	Designation	Address Mode
Move	Bit	Register-Register	REG
Add	Byte	Register-Immediate	(REG)
Subtract	Byte/Field	Register-Storage	(REG)+
Multiply	Word	Storage-Register	(REG)*
Divide	Double/Word	Storage-Immediate	ADDR
Compare	Floating Point	Storage-Storage	ADDR*
Branch	Single Precision		(REG+ADDR)
I/O	Double Precision		(REG-ADDR)*
AND			DISP+(REG)*
OR			(DISP+REG)*
XOR			DISP2+(DISP1+REG)*
Reset			
Stop			

* Indirect addressing
\+ Increment by number of bytes addressed

General Purpose Registers—(GPR0 to GPR7) used for data, addresses, or indexes.

Instructions are provided to allow the entire LSB to be loaded or saved in main storage, thereby providing for ease of task dispatching and preempt/resume operations.

Instruction Set

The instruction set is powerful in function, as indicated by 211 instructions and 11 different addressing modes. Table 2 summarizes the major functions provided within the instruction set, dividing the functions into four categories. This level of function has not been typically available in low cost computers. High function, frequency of instruction usage, structured programming aids, and program reentrancy were driving forces in the design of the instruction set by system architects.

An example of the high function available exists in MOVE and COMPARE instructions. One version of these instructions moves a contiguous field of bytes from one location to another in main storage; these fields may extend from 1 to 64k bytes. Other instructions working with fields of bytes are: (a) COMPARE—contrasts one byte field to another, (b) FILL—replicates a general purpose register into a byte field, and (c) SCAN—searches a byte field for a particular value.

An example of a structured software design consideration is found in the provision of an addressing mode to accommodate the structuring of data (Fig 5). One technique used in structuring data is to create a directory that contains the addresses pointing to various data buffers. If the address of the directory is placed into a register, this particular address mode provides direct access to the data item in the particular data buffer. This technique is used in operating systems to

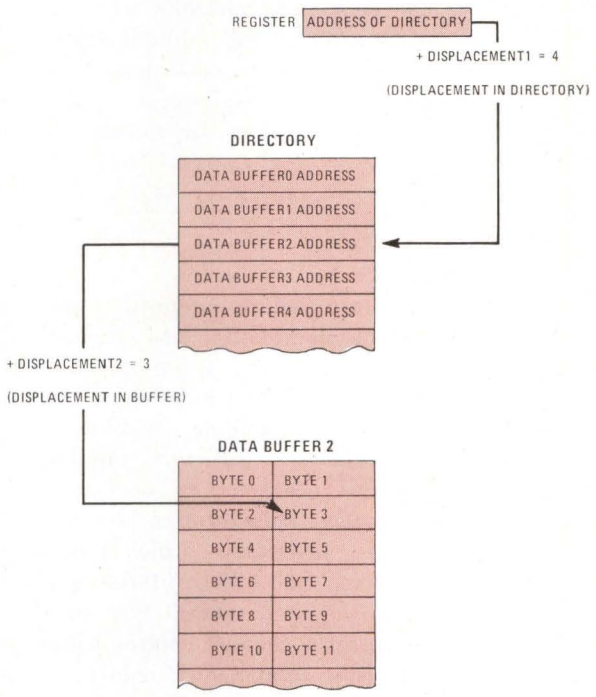


Fig 5 Data directory addressing mode. (DISP2+(DISP1+REG)*) instruction is used to access data organized within directories. Register (REG) parameter specifies register containing address of data directory in main storage. Displacement 1 (DISP1) specifies which data set within directory is accessed. Asterisk (*) indicates that data buffer address is obtained from directory, and Displacement 2 (DISP2) is added to it to obtain particular data element within data buffer defined by directory

access data in subsidiary control blocks connected to a master control block or directory. A base register is set pointing to the master control block, while the master control block contains an address pointing to a task control block. Having built the proper structure, desired data within the selected task control block can be accessed and operated upon using a single instruction.

To support reentrancy within programs and program conventions, such as reverse Polish notation, last-in first-out (LIFO) stacking mechanisms are required. Stacks may be used either for data items (bytes, words, or double words) or for subroutine linkages. As stacks are accessed by a program, checking is performed to ascertain that the size of the stack does not grow to exceed the allocated storage. In Series/1, instructions provide for ease of use in implementing subroutine calls and in placing data on stacks. For subroutine calls, the Store Multiple (STM) instruction saves registers onto a stack while its reciprocal, Load Multiple and Branch (LMB) instruction, restores the registers and provides a return branch to the calling routine (Fig 6). After execution of an STM instruction the stack appears as shown in Fig 7; the stack control block is in storage, and the registers are saved in the main storage location defined by the stack control block. A work area also allocated within the stack provides a storage area for temporary variables when the subroutine may be shared among multiple tasks. The stack control block defines the stack boundaries and is used to check limits on each access to the stack. Since this control block resides in storage, multiple stacks can be defined.

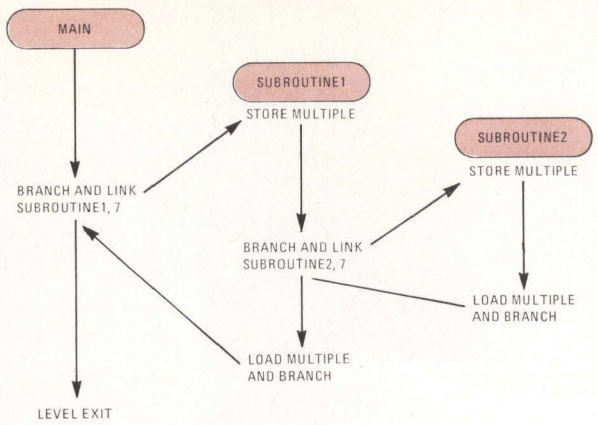


Fig 6 LIFO stacking. Subroutine calls and returns are natural last-in first-out (LIFO) stacking function. Instructions are defined to simplify this function by providing stack operations. Branch and link (BAL) instruction causes branch to subroutine (SUB) while saving return address in register 7. Upon entry to subroutine, store multiple (STM) instruction saves all registers, including return address, in stack. Load multiple and branch (LMB) instruction restores registers that were saved in stack upon entry to subroutine and uses return address to branch back to calling program. Level exit (LEX) instruction returns control to processor when task has finished execution

I/O Devices

Distributed processing, realtime control, communications network control, data entry, and business data processing are examples of the spectrum of applications addressable by Series/1, mandating a large and diverse menu of I/O device handling capabilities. These needs require that the I/O structure minimize the number of CPU cycles necessary to operate an I/O device; otherwise, system configuration would involve complex formulas to determine which I/O devices would preclude others. To achieve these goals, an asynchronous interface was developed that provides a microprocessor to perform channel control within each I/O attachment, thereby significantly reducing central processor involvement with a particular device. The type of microprocessor used is chosen by the designer of the device attachment to optimize cost/performance of that particular device. Up to 256 I/O devices may be attached, including hard files, display stations, diskette files, communication adapters, printers, tapes, sensor controls, S/370-channel attachments, and other devices designed for specific applications.

Two types of I/O are defined for this interface:

Direct Program Control (DPC)—I/O operation is performed inline to the instruction stream, allowing intimate control of the device by software.

Cycle Steal I/O—I/O operation is performed by the device parallel to the processor. Burst mode data transfers are also provided, allowing the channel to be dedicated to a particular device for the duration of a particular I/O operation. This capability is provided for critical devices that must be guaranteed a certain instantaneous data rate. Cycle I/O without burst mode is the predominant method of I/O control.

Those I/O commands where the I/O instruction and control blocks reside in main storage are represented in Fig 8. This diagram shows a DPC operation with data (whether read or write) in the storage location defined by the generated address plus two. Note the reentrancy consideration in the I/O instruction. No device specific information is located within the instruction; it is all contained in a control block pointed to by the OPERATE IO command. This technique allows common code sequences to be easily shared among multiple devices.

Also illustrated in Fig 8 is the format for a cycle stealing I/O operation. After transferring the immediate device control block to the device, the processor proceeds with execution of the next instruction. Meanwhile, the I/O device cycle-steals a Device Control Block (DCB) from main storage. The DCB contains all information needed by a device to perform an I/O operation. Upon completion of this channel command, the device determines whether another command exists; if true, the device will cycle-steal the new DCB and continue data transfer. If the command sequence is complete, a device end-interrupt will signal the processor, and the device will quiesce, awaiting a new com-

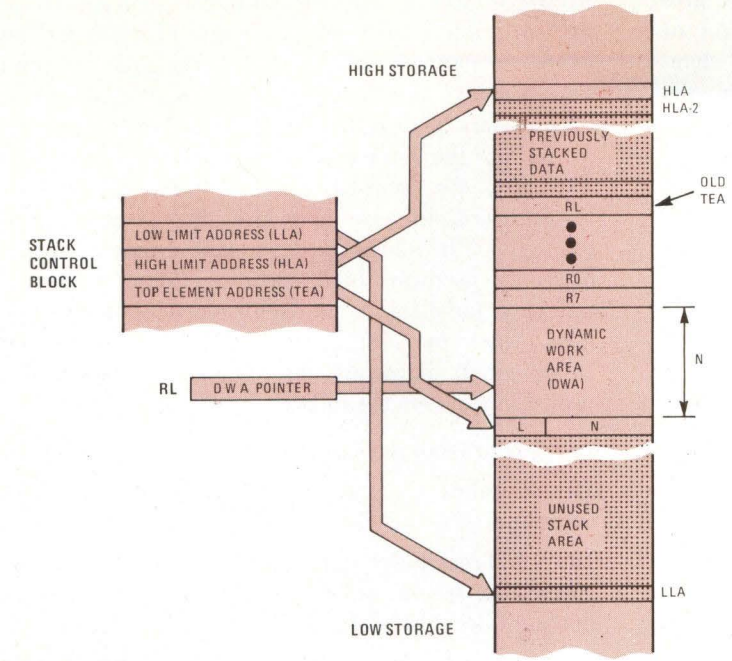


Fig 7 LIFO stack in main storage following STM instruction. Stack control block defines boundaries of stack, specifying upper and lower storage boundaries and address defining current top of data within stack. Within stack, registers (including return address in R7) are saved, work area is defined for use of temporary variables by subroutine, N field defines size of work area, and L field specifies number of last register saved in stack operation. RL is register defined by L field and contains DWA pointer to work area within stack

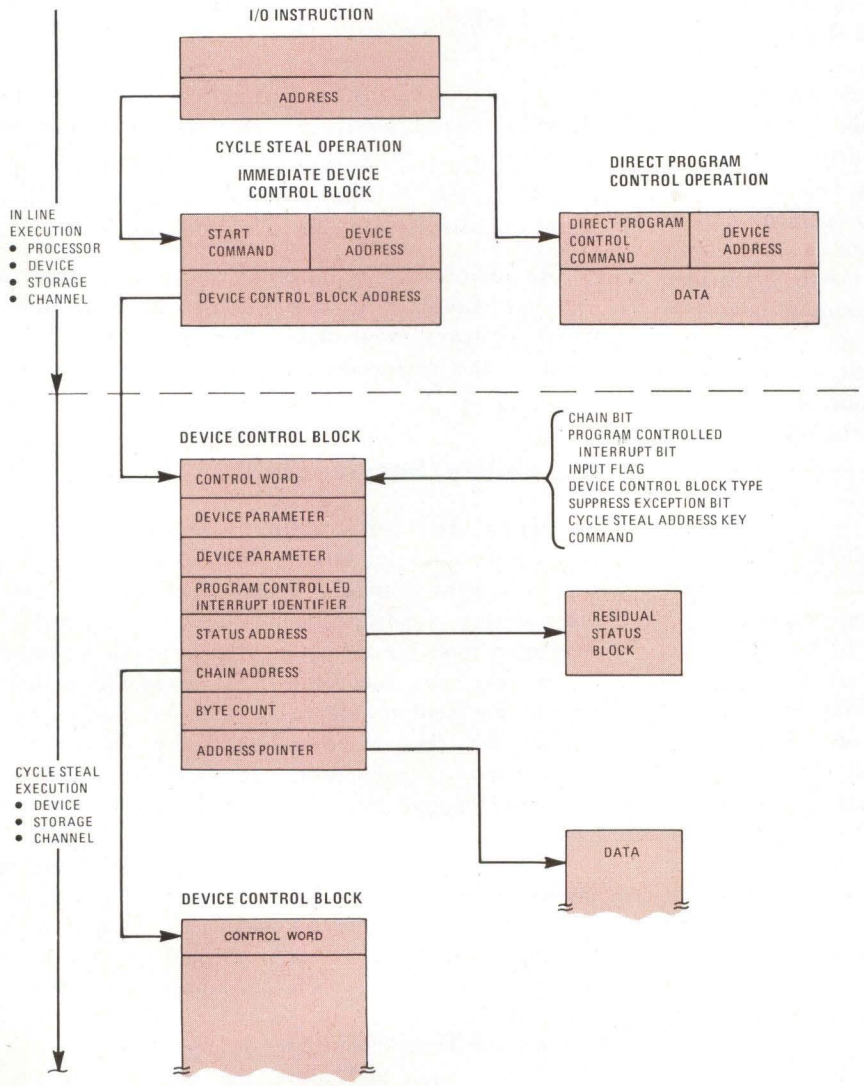


Fig 8 I/O control. I/O operations are controlled by single I/O instruction, which points to storage location that contains 2-word control block called immediate device control block (IDCB). For direct program control of device, second word of IDCB contains data transferred to or from device. For cycle stealing operation, second word of IDCB contains address of device control block (DCB). DCB is fetched from main storage by device and is used to control I/O operations executing in parallel to execution of instructions by CPU. DCB specifies type of operation, where data are located in main storage, where status should be reported, and whether additional commands are to be executed prior to interrupting CPU

mand. Microprocessors within the I/O device attachments fetch and interpret DCBs, freeing the main processor for program execution. Autonomous control of the interface by each I/O device minimizes the channel time for each operation and allows, within the device, parallel preparation of data and address for subsequent cycle steal operations.

Interrupt Mechanism

To provide the fast reaction required in realtime applications, three types of interrupt processing are offered.

Class Interrupts—Occur upon special conditions detected by the CPU itself.

Programmed Interrupts—Caused by an overt action of a program to change its execution priority.

I/O *Interrupts*—Caused at request of I/O devices or other external stimuli.

Class interrupts are used primarily to report on internal checking by the CPU. Machine check interrupts occur when the hardware malfunctions, eg, a parity or I/O sequence problem. Program check interrupts occur when an improper instruction is attempting to execute; for example, when an invalid storage address, protection exception, or an invalid instruction is detected. Other class interrupts are power/thermal warning, supervisor call soft exception trap, and trace and console interrupt. When a class interrupt occurs, a complete snapshot of the status of the registers of the active priority level is automatically copied into a preallocated storage location. A second vector points to the location of the service routine for the particular class of interrupt, and instruction execution begins at that location. Since the class interrupt captures the state of the registers at the exception condition, the problem often can be resolved online by software without impacting unaffected tasks. Online problem resolution is highly desirable in process control or other realtime applications.

Program initiated interrupts are performed by a pair of instructions called Set Level Block (SELB) and Copy Level Block (CPLB). These instructions allow all level registers to be set on any interrupt priority level. If the registers are set on a higher level, an interrupt is performed to that level. If they are set on a lower level, the level is held pending until current operation is complete. Since registers on a level define the essence of a task, ability to load these registers with a single instruction is very similar to dispatching a task. If registers of a selected priority level are first saved in main storage and a new task is loaded to that level, the basis of a preempt/resume operation is accomplished with two instructions. Simple task dispatching and preempt/resume capabilities are helpful in implementing efficient systems where multiple tasks having varying priorities are attempting simultaneous execution. These instructions minimize task switching overhead which, in turn, increases the performance and responsiveness of the system.

Capability for handling the I/O interrupts is demonstrated in Fig 9. With independent copies of registers for each interrupt level, the context switch to handle a new interrupt is performed by hardware in minimal time. Context switch time is that time required to save all registers and status of the task in execution and to set up the environment for the interrupting task. Typically, the majority of this function is handled by software, thereby impacting the responsiveness of the system. In addition to automatic context switching, hardware performs functions often found in first level interrupt handlers in previous machine operating systems. When the first instruction of the service routine is executed, hardware has already determined and placed in registers the following information:

(1) Address of device causing interrupt

(2) Type of I/O interrupt; eg, device end, attention, exception

(3) A breakdown status byte containing information concerning specific cause of interruption; eg, DCB Specification Check, Invalid Address

(4) A base register pointing to a data area that contains parameters relating to particular interrupting devices; this is called Device Data Block (DDB)

(5) Establishment of execution environment within level status register

(6) Loading of instruction address register with address of specific service routine for interrupting device

(7) Service routine may be unique or shared among several devices depending upon method by which software initialized each device's interrupt vector.

The multilevel I/O interrupt allows fast reaction to external stimuli. This fast reaction time requirement exists for many event driven environments and is beneficial to the performance of an I/O intensive system.

Reliability/Serviceability

Reliability And Serviceability (RAS) is a high design priority because modularity makes it difficult to predict a specific standard system configuration, thereby complicating identification of failing components. To overcome this, the design approach requires that each replaceable part incorporate RAS capabilities that allow failing components to be detected during failure. Within the central processor, parity checks, microdiagnostics, and diagnostic instructions—which allow program manipulation of internal registers—are provided.

To monitor I/O integrity of the interface, the main processor channel provides timeouts on tag sequences and watches for incorrect sequences. Device adapters contribute to system integrity through parity checking, cyclic redundancy checks where appropriate, diagnostic instructions, and the use of aids such as wrap-back connectors. These connectors isolate a device from its attachment logic and allow the CPU to exercise the attachment without device involvement. This approach

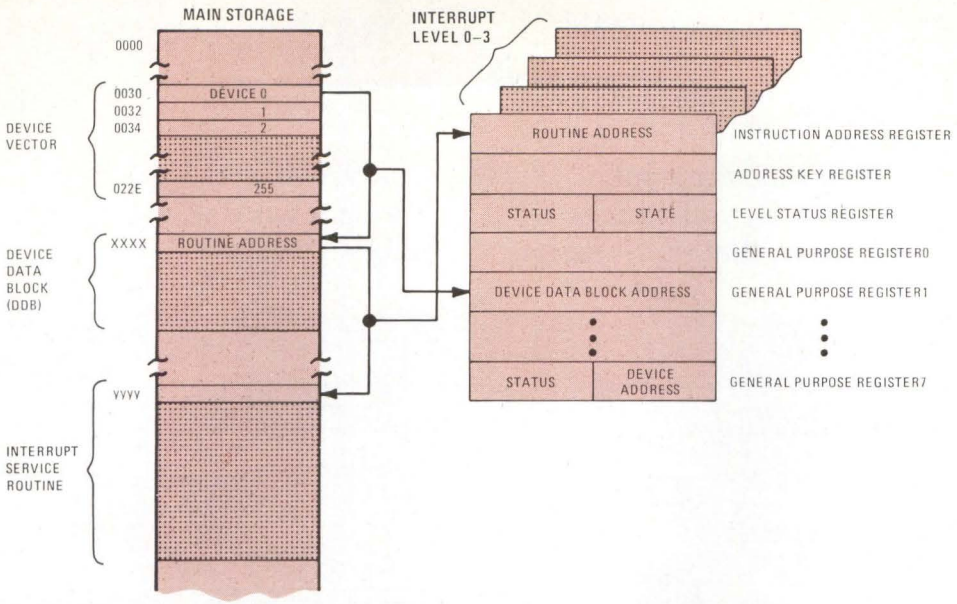


Fig 9 Priority interrupt scheme. Priority interrupts occur to hardware priority level specified by device during interrupt sequence. After interrupt sequence begins on selected level, CPU places interrupting device's address and status in register 7, then fetches storage location of device interrupt vector and places it in register 1. Next CPU fetches storage location specified by vector to obtain address of service routine. Execution of interrupt service routine then begins

permits determination of whether the device or its attachment has failed.

An example of RAS utilization is the system's Initial Program Load (IPL). When the operator presses the IPL pushbutton, a complex sequence of internal system integrity verifications is started. First, the processor thoroughly checks its data path and controls, and then tests its ability to properly read or write the first 16k bytes of storage. At this point, the processor channel tests the tag lines of the I/O interface to determine that they are in the proper states. If all actions are satisfactory, the processor issues a LOAD command (Initiate Initial Program Load tag on interface) to the selected device. The device, upon receipt of the command, proceeds to check out its own data path to verify its ability to operate properly. Only after successful completion of each of these steps does the actual data transfer from the device to main storage begin. If any of the preceding steps fail, indicators are set, either within the device or in the first location of main storage, to signify how far this operation has progressed. The indicators are updated as the IPL sequence continues, and are used to identify a failing unit.

Summary

Architectural design of Series/1 provides processing strength through (a) advanced instruction set—as evidenced in rich function, structured code, and reentrancy considerations; (b) distributed subchannel I/O architecture—to minimize processor involvement in device control; (c) responsive interrupt structure—to allow high response for realtime applications; (d) reliability and serviceability—to optimize cost/performance; and (e) modularity—customizes system to application. A long product life is assured by designing the architecture to exploit structured techniques in software, to meet the challenges of new circuit technologies, and to incorporate microprocessor design concepts.

Bibliography

R. E. Birney and D. G. Bourke, "Series/1—An Architecture for the Future," *Digest of Papers*, COMPCON 77, Sept 1978, pp 218-224

IBM Corp, "Series/1 4955 Processor Description," GA34-0021, IBM Corp, General Systems Div, Atlanta, GA, 1977

IBM Corp, "Series/1 4953 Processor Description," GA34-0022, IBM Corp, General Systems Div, Atlanta, GA, 1977

IBM Corp, "Series/1 System Summary," GA34-0035, IBM Corp, General Systems Div, Atlanta, GA, 1977

IBM Corp, "Series/1 User's Attachment Manual," GA34-0033, IBM Corp, General Systems Div, Atlanta, GA, 1977

Richard E. Birney, project engineer at IBM General Systems Division Laboratory, has been involved in both the definition and the development of Series/1. He holds eight patents, has published twelve technical disclosure bulletins, has received three invention achievement awards, and has merited an outstanding innovation award for work relative to Series/1. He holds BS and MS degrees in electrical engineering from the University of Texas.

Advanced Micro Devices continues its advanced course in microprogrammable microprocessing.

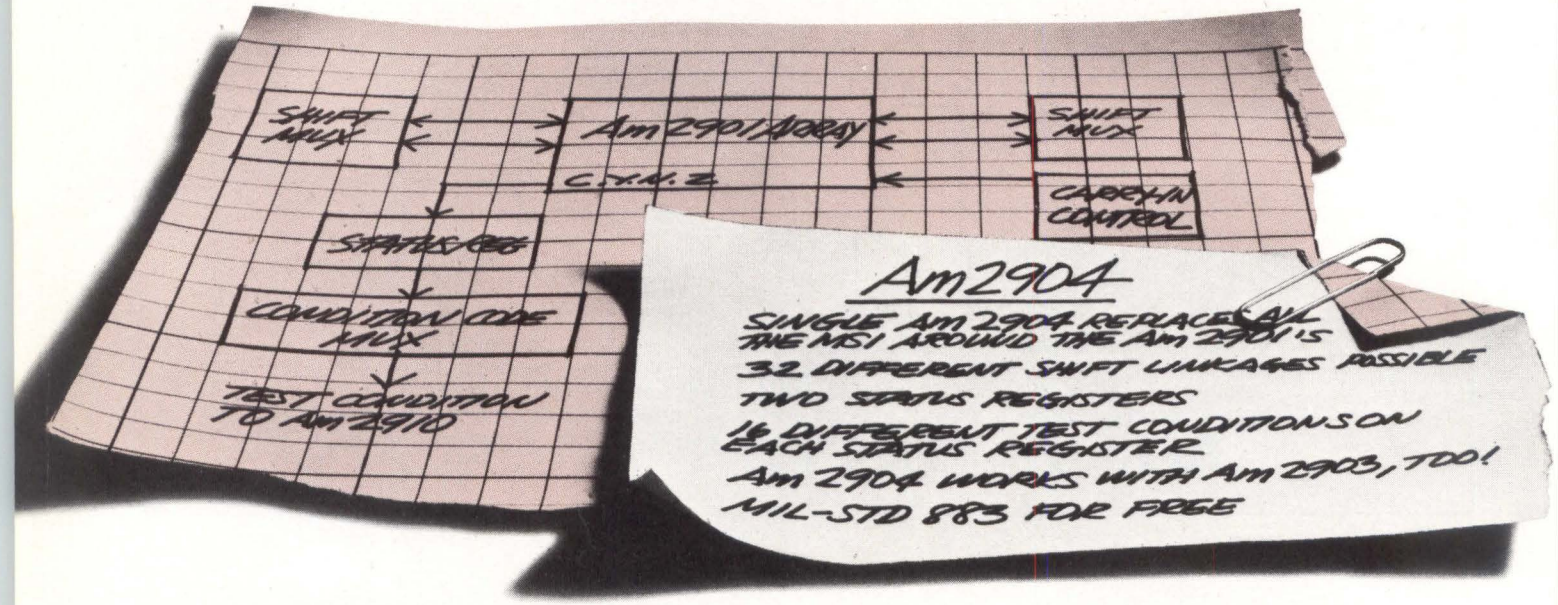
Step by step, function by function, we've been showing you how to build a fast, powerful microprogrammed machine.

When the course is over, you'll know what we know. As it turns out, that's quite a lot.

CHAPTER FOUR: THE DATA PATH, PART TWO.

The heart of the CPU is the Arithmetic Logic Unit.

By putting ALU's together, you can build as long a word as you need. 8 bits, 16 bits, 32 bits, or more.



BUILDING A MICROCOMPUTER, CONTINUED.

But at the ends of an array of ALU's there have always been 15 or 20 packages of glue. Multiplexers. Registers. SSI.

Not any more.

Now there's a single LSI chip that replaces most of the MSI lying around the ALU.

HELLO AM2904. GOODBYE MSI.

Advanced Micro Devices announces the Am2904 Status and Shift Control Unit. It's a single 40-pin microprogrammable part that replaces 15 packs of gates and MSI. It's chock full of mux.

The Am2904 contains multiplexers to form the linkages. Multiplexers to control the carry-in. Multiplexers to test the status after an ALU operation. It even has two registers to save the status bits. All on one chip!

Get the Am2904 from Advanced Micro Devices. Then kiss all that MSI goodbye.

BUILD YOUR LIBRARY. FREE.

Each of these messages is backed by a ton of theory and applications information.

Send in this coupon and we'll send you Chapter Four and tell you how to get the whole book.

Advanced Micro Devices
901 Thompson Place
Sunnyvale, California 94086
I want to build a microcomputer. Sign me up.

Name _____

Title _____

Mail Stop _____

Company _____

Address _____

City _____ State _____ Zip _____

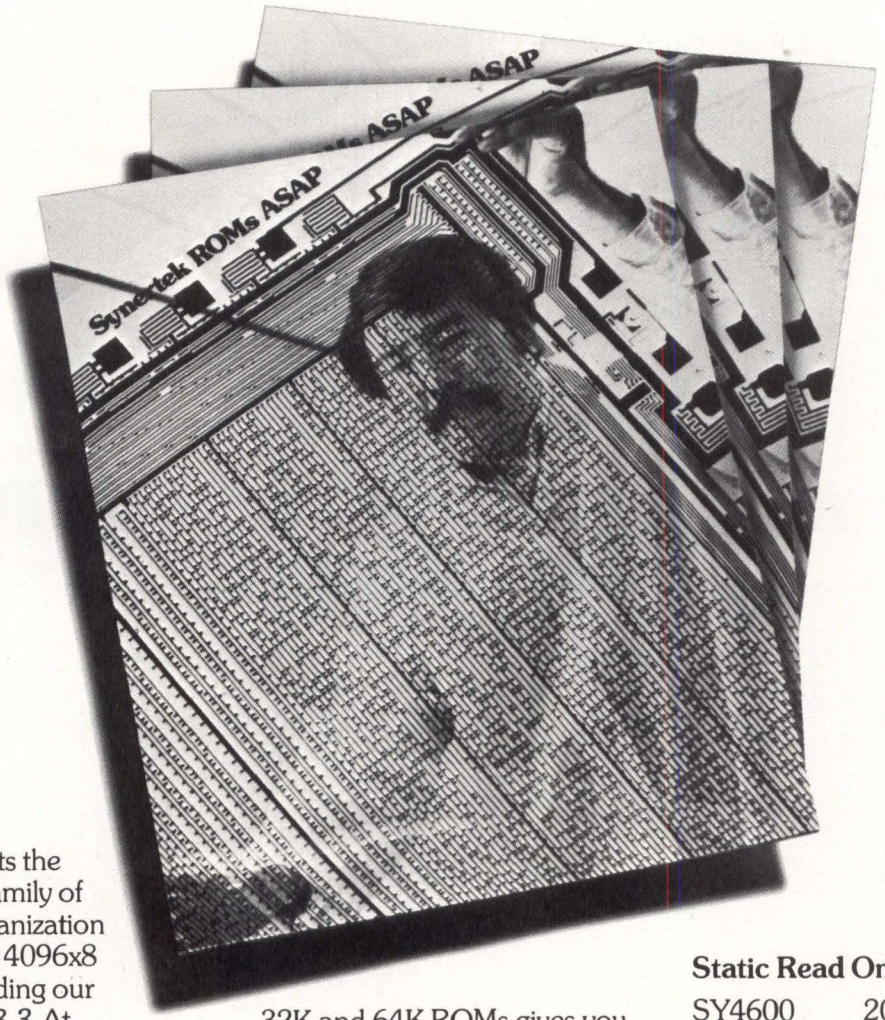
4/79/CD

ADVANCED MICRO DEVICES

Multiple technologies. One product: excellence.
901 Thompson Place, Sunnyvale, California 94086 • Telephone: (408) 732-2400

Next Chapter, A Complete 16-Bit Microcomputer.

The ROMs you need. When you need them.



On-time delivery puts the punch in our total family of ROMs. With the organization you need—8192x8, 4096x8 and 2048x8—including our new *300nsec 2316B-3*. At Synertek, we know there is no product area where service and responsiveness to your needs is more important than in mask programmable ROMs.

That's why two years ago we pioneered a unique dual capability—first mask programming for lowest cost and smallest real estate, last mask for fastest delivery to meet critical production schedules and get you results now. We can even combine first mask and last mask to get you into production today—and still save you money tomorrow.

Pin compatibility on our 16K, 32K and 64K ROMs gives you built-in future memory expansion capability. All it takes to upgrade your system's ROM capacity for new applications is to replace our 16K ROMs with our 32K ROMs or replace our 32K ROMs with 64K ROMs. And you can usually do it with no hardware changes.

When you buy ROMs from Synertek, you know you're buying total service. Contact us now for samples, data sheets and our comprehensive folder, "Synertek ROMs ASAP." Synertek, Inc., 3001 Stender Way, Santa Clara, California 95051. (408) 988-5611. TWX: 910-338-0135.

Static Read Only Memories.

SY4600	2048x8 or 4096x4, 550nsec
SY2316A	2048x8, 550nsec
SY2316B	2048x8, 450nsec (2716 compatible)
SY2316B-3	2048x8, 300nsec (2716 compatible)
SY2332	4096x8, 450nsec (2716 compatible)
SY2364	8192x8, 450nsec, 24 pin

Synertek, Inc.

DESIGNING A MICROPROCESSOR DRIVEN MULTIPURPOSE PERIPHERAL CONTROLLER

Requisites of adaptability to mix/match combinations of I/O devices, operation with existing software, and intelligence formulated the design of a microprocessor based multifunction controller architecture

Richard F. Binder Modular Computer Systems, Incorporated, Fort Lauderdale, Florida

Requirements for a revised generation of peripheral controllers became apparent while the ModComp CLASSIC computer series was still in the conceptual stage of design. System packaging was based on card-edge pluggable wirewrapped boards for modularity and ease of maintenance. To devote a full board space (approximately 550 integrated circuits) to a single card reader or line printer controller seemed unreasonable; this configuration would waste space and entail extra cost. The decision therefore was made to package several such low performance controllers on one board. Specifying that the design approach would be toward a multiported controller adaptable to many different devices in mix/match configuration avoided the problem of choosing which controllers to conjoin. Also, the new controller had to operate with existing software and would therefore require some intelligence. For example, the existing card reader controller is fully buffered and can transfer data in a direct 12-bit card image; in a transitional 8-bit code called "half-ASCII," packed either one or two bytes per word; or in any 8-bit code downloaded by the host minicomputer, again packed one or two bytes per word. It performs multipunch detection while translating to 8-bit codes. Other controllers to be reimplemented are similarly sophisticated.

Clearly, a microprocessor is the way to package the requisite intelligence on a single board. This approach relieves the designer of complex hardware and/or custom microcode design; a microprocessor's firmware is generally more maintainable than microcode fitted to custom logic. Also, interfacing to future devices should be easier.

General Architecture

Since a microprocessor based controller is extremely slow in relation to a controller implemented with discrete logic, the designer must take into consideration the microprocessor's response time. This response deficiency can be concealed for the most part under the overhead of the host's interrupt-driven input/output (I/O) bus without slowing down the overall system. Several nearly instant system responses are still required, however, such as the setting of controller busy status for the addressed port in response to a transfer-initiate command. These responses are generated by hardware in the form of a programmed logic array (PLA) to set status latches. A Z80A microprocessor computes all other status which are stored as 16-

bit words in four 4-word by 4-bit register files for access by the host's software. Fig 1 is a simplified block diagram of the multifunction controller's final design.

Actual execution of commanded operations is of course carried out by the microprocessor; all commands and data are loaded by the host into the command/data (C/D) first in, first out (FIFO) buffer. This buffer allows the host to issue several commands in rapid sequence. The microprocessor fetches the commands from the buffer one at a time and processes each as required. Even though four independent devices can be controlled by this design, the C/D FIFO buffer need not be very deep in storage capacity; the interrupt-driven I/O bus makes it possible for the microprocessor to control to some extent the rate at which it receives commands by controlling the rate at which it generates interrupts. The C/D FIFO buffer in the controller is 16 words deep by 21 bits wide (16 bits for the data and 5 bits to identify the command's function and destination within the controller).

Similarly, since four independent devices can be controlled, the handling of one device cannot wait for the I/O's response to an interrupt for another device. Therefore, three request FIFO buffers are loaded by the microprocessor for the host: service interrupt (SI), data interrupt (DI), and direct memory processor (DMP). The first two requests are vectored in the host for software processing, while the third activates concurrent hardware in the host's I/O processor itself. As each request is needed, the microprocessor loads the request's source identification word into the appropriate request FIFO buffer. The request FIFO buffers are unloaded by the host at its own rate, and the microprocessor is thereby freed to attend to other functions. Another use of the request FIFO buffers is made by device firmware sets (tasks) which must be able to "stack" more than one request of the same type; a single register for each request type prohibits such stacking.

The microprocessor selected had to be fast enough to support the required system throughput. Tentative short benchmark routines were coded for the 8080A, Z80, 9900, and 6800. One of the coded benchmarks was a routine to fetch the 21-bit contents of the C/D FIFO buffer and transfer control to the appropriate task. The following table gives an approximate comparison of various microprocessors' performance derived from a sample routine based on the controller's firmware.

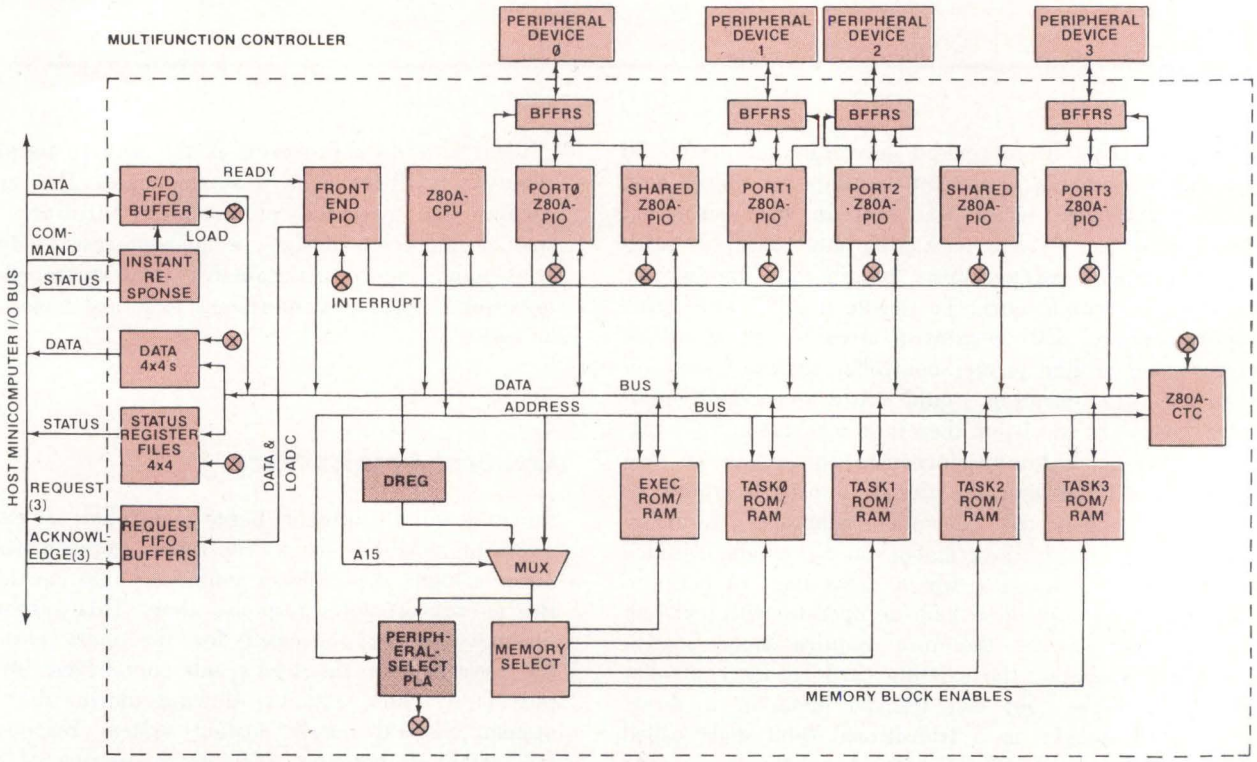


Fig 1 Controller block diagram. Layout exhibits straightforward bus architecture. Distinguishing feature is addressing scheme consisting of displacement register (DREG) and peripheral-select PLA. This hardware makes possible firmware-transparent bank switching

Microprocessor	Clock Periods	Time
8080A-2	167 at 320 ns	53.4 μs
Z80A	92 at 250 ns	23.0 μs
9900	114 at 300 ns	34.2 μs
68B00	58 at 500 ns	29.0 μs

Calculations based upon these short routines indicated that of the machines coded for, only the Z80A would be adequate. All further design was tailored explicitly for the Z80A; no detailed hardware or firmware design was produced for the other machines. (These values were attained by a designer most familiar with the Z80. Greater familiarity with other microprocessors might lessen the disparity in performance, but the Z80's powerful instruction set, vectored interrupt scheme, and twin register sets made it the undisputed choice for this application.)

The four device ports (numbered 0 to 3) must be adaptable to both serial and parallel devices. Originally, the multifunction controller specification called for support of a card reader, three types of line printers (two parallel and one serial), a paper tape punch, a paper tape reader, a serial console terminal, and a full-duplex RS-232-C asynchronous channel with full modem control and fully programmable parameters. A typical configuration might include a card reader in port 0, a line printer in port 1, and an asynchronous channel in ports 2 and 3. Packaging requirements specified a total of 80 signal pins for all four ports. This constraint, together with an analysis of all the parallel devices, led to a 20-bit port configured as eight bidirectional bits for data transfer, four bidirectional bits for status or control (handshaking, etc), seven input bits for status or control, and one output bit for control (Fig 2).

Of the seven input bits, two can be programmed online for signal inversion, and one of these two can be connected to either a pullup or pulldown resistor for device power sensing. The two groups of bidirectional bits, including control of their buffers, can be reprogrammed online. (For a card reader, all bits are input; for a line printer, all bits are output.) This interface configuration can be made to handle most common 8-bit devices. For serial devices, the 20-pin limitation requires that the parallel buffers be removed and replaced with a universal synchronous/asynchronous receiver/transmitter (USART), as well as appropriate line drivers and receivers.

The Z80A-PIO parallel I/O controller chip provides the required bit-programmable port capability (Fig 2), but it has only two 8-bit ports. Six PIO chips are

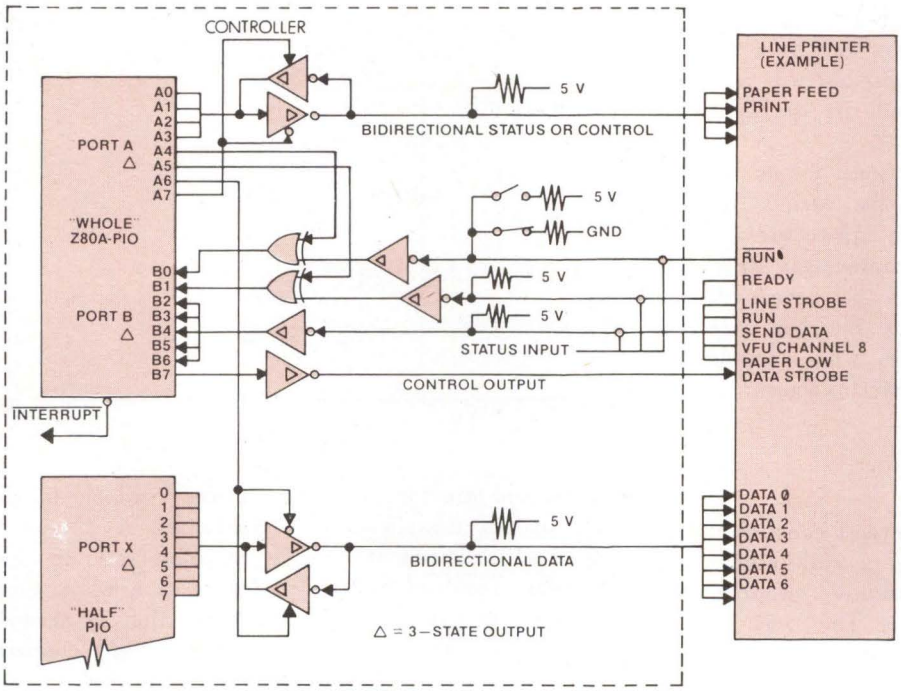


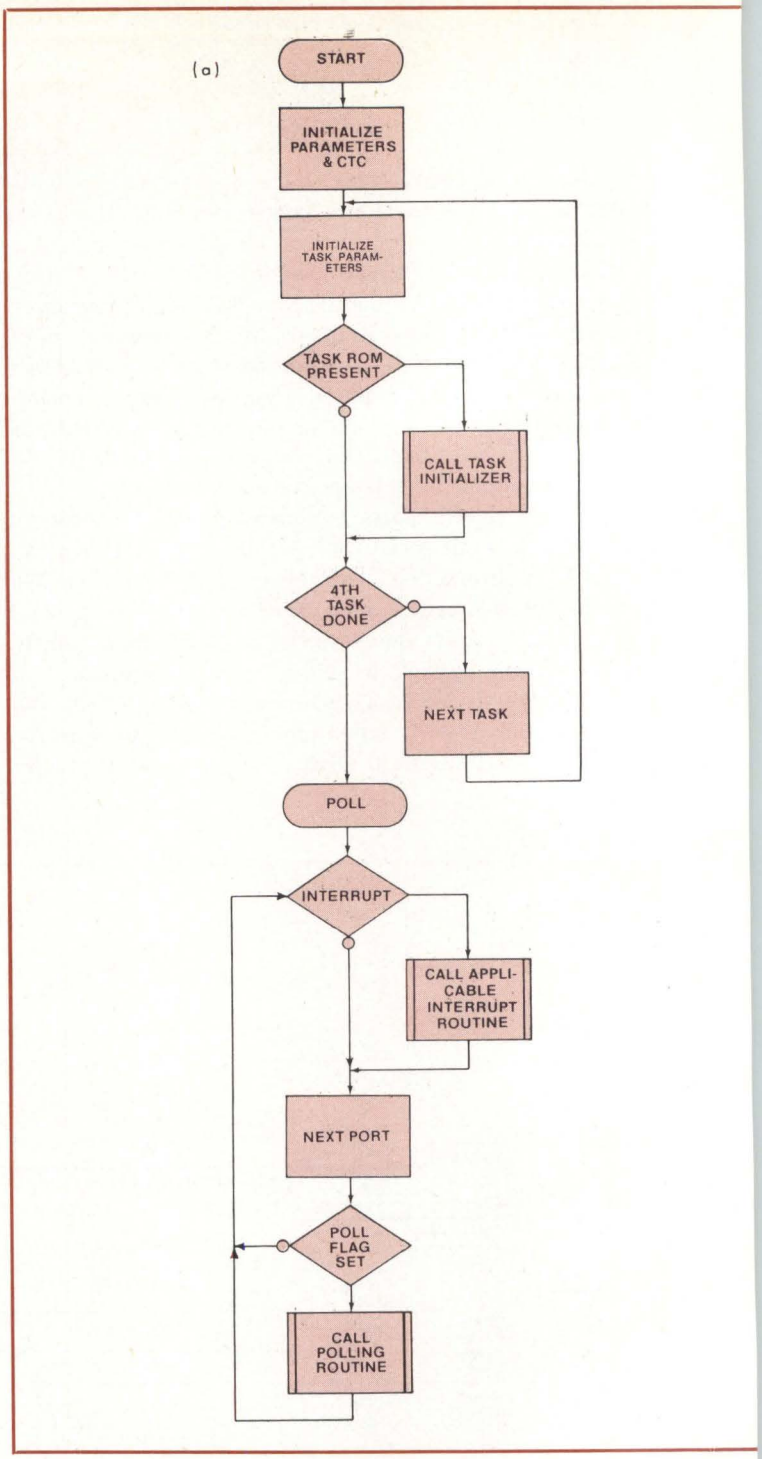
Fig 2 Parallel interface port. Each parallel port interface consists of 3-state buffers connected to port's PIOs to provide each task with ability to program interface to suit its own requirements. For uniformity, all buffers are Intel 8226 even if used only in one direction

needed to drive four 20-bit controller ports. Since one and one-half PIO chips provide 24 bits, the extra four bits control the buffers connected to the programmable bits. The two shared PIO controllers handle only data paths, and therefore are not connected to the microprocessor's interrupt system. All six chips are configured to operate in bit control mode; hence, their handshake lines are not used. Handshaking is accomplished by addressing various port bits. Each controller port has one complete PIO chip that can generate any needed interrupt.

For serial applications, all 24 bits are available to be programmed as required to best support the specialized serial hardware. To minimize serial hardware, the decision was made to restrict console tasks to port 0 or 1, and the channel task to ports 2 and 3 together. A serial line printer uses the console hardware. A USART is connected so that it is handled as though it were an external device. Serial handling may seem somewhat clumsy, but the hardware involved in the microprocessor's bus structure is simplified since there is no need to interface directly to a specific chip. This approach also helps to standardize the tasks in their port handling. The Z80-SIO serial I/O chip was not yet available when this controller was designed. Examination of the preliminary SIO specification, however, indicated that use of the SIO would seriously complicate the controller's internal structure; even if the IC had been available, it probably would not have been used. (The area in question is the displacement register, which will be discussed later.)

Some of the devices to be controlled require either timeouts or cyclic testing of status. These timing functions are triggered by a Z80A-CTC (counter-timer circuit); its four channels are allocated one to each controller port, and are used as timers for intervals up to 16.4 ms (the longest timeout possible with the 4-MHz clock). Longer timeouts are made by firmware counting of CTC interrupts.

A seventh, or frontend, PIO is used between the microprocessor and the host's I/O to load the various requests into the appropriate FIFO buffers and to provide a vectored interrupt signal to the microprocessor when the C/D FIFO contains information to be processed. Sixteen-bit status and data words for the host are stored in separate 4 x 4 register files whose inputs are I/O mapped for loading by the microprocessor.



Firmware Considerations

In order to be able to switch among several concurrent activities, the firmware is designed as a multitasking operating system consisting of an executive program and the various device handlers, or tasks. The executive is always present, while tasks are added as needed by plugging in read-only memory (ROM) sets.

Executive Program

The executive occupies 768 bytes of ROM and 256 bytes of random-access memory (RAM), and has three primary functions: to initialize the system, control time-sharing, and provide executive services available to all tasks. System initialization is performed at power-up [Fig 3(a)]. The first routine executed sets up the parameters required for the controller as a whole and initializes the CTC since the latter function is needed only once for all four ports. A loop is then entered which executes four times, once for each port. Task-not-present status is loaded into the status register file, interrupt entry vectors are loaded into the PIO assigned to the port represented by the pass count of the loop (port 0 on the first pass, port 1 on the second, etc), and a test is made to determine whether the port's task ROM is present. If not, its command entry dedi-

```
                    152  ;       ***********
                    153  ;       *  POLL   *
                    154  ;       ***********
                    155  ;
                    156  ;       POLLING ROUTINE - TEST EACH TASK SEQUENTIALLY FOR POLLING
                    157  ;       SERVICE REQUESTS, CALL TASK IF POLL FLAG IS NON-ZERO.
                    158  ;       OPEN INTERRUPT WINDOW ONCE EACH PASS.
                    159  ;
9071 110603         160             LD    DE,POLF         ;FETCH POLL FLAG ADDRESS
9074 210098         161             LD    HL,DADR         ;FETCH DISPL REG ADDRESS
9077 FB             162  POLL      EI                    ;ENABLE INTERRUPTS
9078 04             163             INC   B
9079 04             164             INC   B
907A F3             165             DI                    ;DISABLE INTERRUPTS FOR POLL SERVICE
907B 70             166             LD    (HL),B          ;WRITE DISPLACEMENT
907C 1A             167             LD    A,(DE)          ;THIS PORT NEED POLLING SERVICE?
907D B7             168             OR    A
907E CA7790         169             JP    Z,POLL          ;NO,TRY NEXT PORT
9081 D9             170             EXX                   ;YES, SAVE CURRENT PARAMETERS
9082 2A0403         171             LD    HL,(POLE)       ;FETCH TASK POLL SERVICE ENTRY
9085 CD8C90         172             CALL  ICALL           ;CALL POLL ROUTINE INDIRECT
9088 D9             173             EXX                   ;GET OWN REG SET
9089 C37790         174             JP    POLL            ;NOW GO POLL NEXT PORT
                    175  ;       THE Z80 DOES NOT HAVE A CALL-INDIRECT INSTRUCTION -
                    176  ;       THE FOLLOWING JUMP SERVES THE PURPOSE.
908C E9             177  ICALL     JP    (HL)
```

(b)

Fig 3 Simplified main controller flow. Controller and four tasks are initialized under control of executive program (a). Program then enters polling loop (b), which provides for priority interrupt service and for one task's round-robin polling service on each pass. In idle condition, loop executes in 11 μs/pass, ensuring reasonably rapid interrupt response

cated location in RAM is loaded with a common ignore-this-command return. If it is present, the first 10 ROM locations—containing PIO interrupt, CTC interrupt, command interrupt, data transfer interrupt, and polling service entry addresses—are transferred to dedicated locations in either executive or task RAM. Control is then transferred to an initializer within the task itself; this routine sets up the port PIOs and CTC as required for the particular task, and generates and loads valid status to replace the initial status loaded by the executive. Control is then returned to the executive initializer, which processes all four ports in this manner before enabling the hardware to respond to the I/O.

Once initialized, the system enters an idle loop whose function is to control timesharing among the tasks present. This idle loop, called the polling loop [Fig 3(b)], enables a task in two ways: interrupt service (priority enabling) and polling service (round-robin enabling). Any activity must begin with an interrupt, either from a task's CTC port or from the outside world (the host or the device connected to the particular port). A CTC or device PIO interrupt is vectored to the relevant task routine, which takes appropriate action. An interrupt from the host's I/O, through the frontend PIO, is vectored to an executive routine which extracts the contents of the current C/D

FIFO buffer location, decides whether it is a command or data, and transfers control to the task routine whose address is in the pertinent dedicated location. Whichever task routine is activated completes its action and returns control to the polling loop. The task activity in question may need service of a type which cannot be triggered by further interrupts (such as emptying a buffer asynchronously with its filling, to a device that does not handshake). Such service is activated by the setting of a dedicated location, called the polling flag, to any nonzero value.

Each task has its own polling flag and an associated polling entry dedicated location. During each pass of the polling loop, an interrupt window is opened for 2 μs. If no interrupt is pending, or upon return from the servicing of an interrupt, the loop tests one port's polling flag. If the flag is zero, the port number is incremented and the polling loop restarts, opening the interrupt window. Each port is tested once every four passes through the loop. If the polling flag is nonzero, the loop fetches the address of the task polling routine from the dedicated location and calls that routine. The task routine takes the action for which it has been set up and resets the polling flag if no further polling service is required, and then returns to the polling loop, which continues as before. Note that interrupt service always receives priority over polling service; this arrangement provides the fastest possible response to the outside world, and is guaranteed by specifying that all interrupt routines must enable the interrupt before returning to the polling loop. If another interrupt is pending, it is serviced immediately.

To minimize both interrupt and polling service times, the system takes advantage of the Z80's two sets of working registers. One set contains registers A, B, C, D, E, H, and L; the second set is a duplicate of the first. A single instruction (EXX) will exchange all but A with their duplicates, and another instruction (EX, AF, AF′) will exchange A and the machine's flag register. The latter instruction is not used in the multifunction controller—A is considered volatile by each routine. The polling loop does the context swap for polling routines, but interrupt routines must do the swap themselves. One set is dedicated to the polling loop; register B contains the number of the next port whose polling flag will be tested, register pair DE contains the address of the polling flag in memory, and register pair HL contains the address of the polling routine being called. The second register set is available for use by any task or executive service routine. The Z80 also has two index registers, IX and IY, but these registers are not used in the controller because indexed instructions suffer a 1-μs/instruction time penalty.

The executive provides several services to any task in the form of callable subroutines. These services perform the functions of

(1) Decoding commands that a task has determined to be of a control nature, such as controller interrupt connection, data transfer termination, etc. Appropriate action is taken and control is returned to the calling routine if required.

(2) Generating one request for a data transfer either to or from the I/O. This request may be either a DI or a DMP request; the executive service routine tests current controller parameters to decide which type is proper.

(3) Initializing or terminating the host's DMP hardware by generating specialized DMP requests for these functions.

(4) Requesting startup or shutdown service of the host's software by generating an SI, and optionally resetting controller busy when setting the SI.

(5) Reinitializing the calling task exactly as is done at power-up. Primarily a diagnostic tool, this function is essentially free—the same routines are used in both cases.

Primary value of the executive services is to reduce the size of the tasks, since each task is limited to 768 bytes of ROM and 256 bytes of RAM. An added advantage lies in the fact that a task designer need not reinvent the wheel by designing all the common functions again for each new task; the effort required to implement new tasks is thereby minimized.

As mentioned above, tasks are limited in size. A more serious problem, however, is the necessity that any task (with certain specific exceptions) be installed into any port position. It is clear that the various port memory areas will have different starting addresses. A conventional software program designed to be loaded into various areas of memory (relocatable software) is accompanied by a list of locations within the program which must be modified upon loading to reflect the program's starting address. Once programmed, however, a ROM set cannot be changed; so it would seem that each task must come in four versions, one for each port. This constraint was considered unacceptable; stocking of all the different ROM sets would create problems for both manufacturer and user. The solution to this problem lies in relocatable firmware, which can be implemented by memory mapping, of which bank switching is a simplified form. Two address bits (A10 and A11) are used to select one of the four tasks, and the most significant address bit (A15) is used to control whether the bank switch is invoked [Fig 4(a)]. All tasks, then, can originate at memory address zero. It is possible to address any memory location in absolute mode (A15 = 1), but only the selected task is accessible in relative mode (A15 = 0). The executive is always addressed absolutely to make its services available to any task. The addresses of those services are assembled with each task as "external" equates.

Located in executive RAM, the push-pop stack is addressed absolutely. PIO and CTC interrupt dedicated locations are also in executive RAM, but these locations are addressed relatively so that accesses to the same relative address in each task will be routed to the proper absolute address by the bank switching control hardware. The interrupts themselves are routed through the same absolute addresses by the vectors loaded into the hardware.

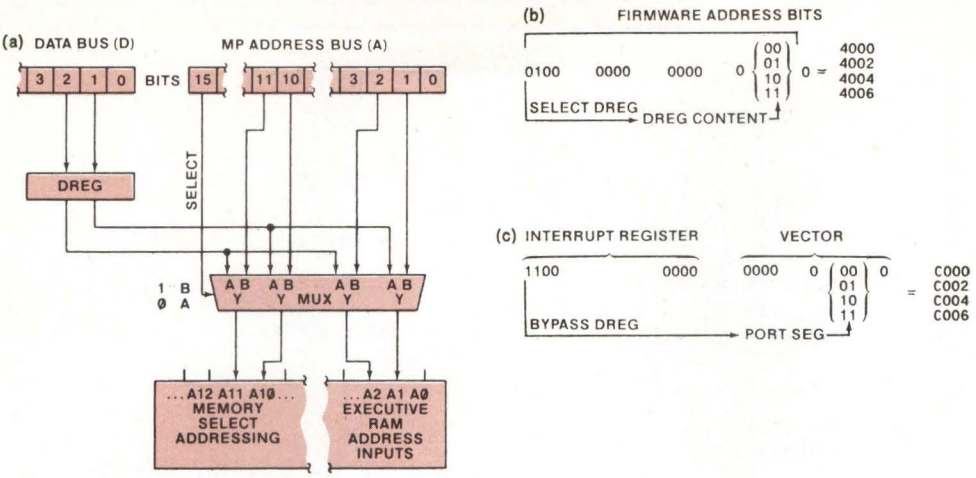


Fig 4 Memory displacement (bank switching). Task/executive selection is accomplished by multiplexing A10 and A11 with contents of DREG. In absolute mode (A15 = 1), any area of memory is accessible; in relative mode (A15 = 0), only selected task is accessible. Interrupt dedicated locations in executive RAM are addressed by multiplexing A1 and A2 with DREG. Addresses generated by task firmware access same actual locations as does hardware interrupt entry. Displacement scheme makes it unnecessary for task to know its port address. In (b), firmware-generated address of 4000 may be actual address of 4000, 4002, 4004, or 4006, as controlled by DREG. Hardware interrupt response (c) concatenates interrupt register and actual vector supplied by interrupting peripheral to produce addresses in executive RAM that correspond to those produced by DREG-modified firmware addressing

Task Routines

Tasks consist of a series of short routines whose functions fall into the following categories: initialization, command and data transfer handling, request generation, and device handling. During initialization, the executive passes control to an initializing routine in the task. This initializer is responsible for setting each of its PIOs with the required I/O bit patterns and interrupt enables, and its CTC port with a timeout and an enable if the CTC is to be used. It initializes task oriented, dedicated locations as required, and it generates and loads the proper controller status to the status register file for access by the host. Control is then returned to the executive. This initialization scheme provides the only reasonable means of controller setup—by the tasks themselves.

Commands to a task are received from the C/D FIFO buffer. A FIFO interrupt, recognized by the frontend PIO, triggers the executive routine which fetches the FIFO contents and transfers control to the task's command handler. The command handler then decides what type of action is requested by examining the 16-bit data pattern of the command, making use of executive service if required, and takes that action. Control is then returned to the executive. Note that online task routines must execute as fast as possible in order to make way for other tasks which may be time dependent. In one design case, compliance with this general rule required that an interrupt routine be divided into two portions; the second half of this routine is triggered by programming a PIO to generate an interrupt when an unused output bit is written to the true state. This splitting of a low priority interrupt routine permits higher priority activity to intervene while guaranteeing that the second half will execute much sooner than if it were a polling routine.

At the transfer rates for which the multifunction controller is designed, direct memory access (DMA) adds unnecessary hardware and complicates such capabilities as character recognition and/or processing. Therefore, data transfers are handled in much the same manner as are commands. One of the extra C/D FIFO bits specifies the direction of the transfer; output data from the host are either output directly to the device or loaded into a buffer for output later, when the device is ready. Buffered data output generally is triggered by polling service, whereas direct output always is a result of a transfer requested by a device interrupt routine signifying that the device is ready. Input data may also be buffered or not, as applicable to a particular device; for example, the card reader task buffers its data to protect the I/O against overflow. Input data are loaded into the data register file. When the host accepts the data in response to the controller's data request, that transfer is loaded into the C/D FIFO buffer

```
                    468  ;       ***********
                    469  ;       *  INTH   *
                    470  ;       ***********
                    471  ;
                    472  ;       ENTER ON INTERRUPT FROM NOT HOLD
                    473  ;
022E D9             474  INTH      EXX                   ;NOT-HOLD INTRPT IF GET HERE
022F 210D03         475  INTH1     LD    HL,CSTAT
0232 7E             476            LD    A,(HL)          ;FETCH CSTAT
0233 0F             477            RRCA                  ;D0, D1 = D1
0234 0F             478            RRCA
0235 07             479            RLCA
0236 17             480            RLA
0237 77             481            LD    (HL),A          ;SAVE NEW CSTAT
0238 CD0A02         482            CALL  LPSTA           ;LOAD MOST-RECENT STATUS TO 4X4'S
023B 3E97           483            LD    A,097H
023D D383           484            OUT   (PIOBC),A       ;SET UP FOR INTRPT ON LINE STROBE
023F 3EFB           485            LD    A,0FBH
0241 D383           486            OUT   (PIOBC),A
                    487  ;       STRIP PAGE PORTION OF BOF INTRPT HANDLER ADDRESS
0243 3E4F           488            LD    A,INTB-INTB/256*256
                    489  ;       THE ABOVE MATHEMATICAL TECHNIQUE TAKES ADVANTAGE OF THE
                    490  ;       FACT THAT ALL INTRPT ROUTINES ARE LOCATED IN THE SAME
                    491  ;       MEMORY PAGE - ONLY THE LOWER ORDER ADDRESS BYTE NEEDS
                    492  ;       TO BE LOADED.  THIS TECHNIQUE IS USED THROUGHOUT THE
                    493  ;       TASK IN ORDER TO CONSERVE EXECUTION TIME AND MEMORY
                    494  ;       SPACE.
0245 320040         495            LD    (PIOBV),A       ;CHANGE PENTV BACK TO "BOF"-ROUTINE
0248 320603         496            LD    (POLF),A        ;SET POLLING FLAG
024B D9             497            EXX                   ;EXIT
024C FB             498            EI
024D ED4D           499            RETI
```

Fig 5 Typical interrupt routine. Routine monitors controller status change from HOLD to READY when operator depresses RUN switch. It reports new status to host, sets PIO to interrupt when next line feed occurs, and loads interrupt dedicated location in executive RAM with address of routine which tests for bottom-of-form status. It sets polling flag—if controller is busy, data transfer commences (polling vector will have been set to address data-to-printer routine); if not, service interrupt is generated to notify host that printer is available (polling vector will address SI-generation routine). Manipulation of D0 in internal controller status word (CSTAT) copies enable bit stored in D1 into status that will be read by host if SI is made

as though it were an output. Upon recognizing this input transfer, the firmware ignores the FIFO data and proceeds to ready the next transfer.

Data requests may be generated by several mechanisms. An interrupt routine servicing a device whose data rate is controlled by the device (eg, a terminal, through a USART) generates a request when it has data for input or when the device requires output. A polling routine emptying an input buffer generates requests as long as there are data in the buffer. Finally, an output data transfer interrupt routine filling a buffer generates a request every time it is triggered by the receipt of a transfer, after loading the just-received data into its buffer.

Data are transferred to an output device by writing the data to the half PIO and then writing a one followed by a zero to another output bit assigned as the strobe line. If a handshake is required, the strobe is set true and allowed to remain set until an acceptance is signalled by the device. Data from an input device are read from the half PIO and then accepted, if the device requires a response, by strobing in the same manner as for output. The CTC is used for two functions: cyclic activity and single-shot timeouts. Most cyclic activity tests and updates status for devices whose status can change during periods of controller inactivity. Such changes are often due to operator intervention. Single-shot timeouts are required for devices which take long periods to execute some function or functions and do not signal the completion of such functions. A currently supported paper tape punch, for example, takes a full second to run up to speed when started; it is left running for 10 s after the completion of a transfer to avoid repeated up and down cycles

and the consequent startup delays. Several concurrent timeouts may be controlled by a common clock handler routine, and this activity by no means precludes cyclic functions as well.

Hardware Architecture

The memory bank switching function is the central capability of the hardware, and is implemented with a single 2-bit register called the displacement register (DREG). Input to DREG is data bus bits D1 and D2 [Fig 4(a)]. This register is loaded either by an executive routine or hardware interrupt routine. The executive routine which fetches the C/D FIFO contents loads two of the extra FIFO bits into DREG by a mapped memory write. The register is addressed as though it were a memory location; hence, any firmware has the ability to load it, but tasks normally do not do so. The two loaded bits are a binary encode of the port selected by the host's controller address bus, and when used as A10 and A11, they select the specified task's memory area. Hardware interrupt response loads D1 and D2 into DREG using the interrupting device's vector to select the task whose device made the interrupt. Dedicated interrupt entry locations are allocated to provide the proper vectors. It is this function which precluded use of the SIO. The SIO generates a series of vectors for a given port, so that bits 1 and 2 cannot be used for port selection.

DREG outputs are multiplexed with A10 and A11 from the microprocessor, and the multiplexer is steered by A15. When A15 is a zero (relative mode), the multiplexer gates DREG's outputs to the controller's internal address bus, and any one of the four task areas can be accessed. When A15 is a one (absolute mode), the microprocessor's actual address is used, and any area of memory can be addressed. The executive is always addressed absolutely; certain tasks, which occupy more than one port and are always installed in the same port location, are also addressed absolutely to avoid the necessity of constantly reloading DREG when executing different subroutines.

DREG addresses not only memory but also most other port oriented hardware in the controller. This scheme is necessary to speed execution times; if a task were required to recognize its port address, and compute and load the addresses of all its devices, most routines would become unreasonably long. To avoid this problem, all PIOs and the CTC are selected by a peripheral-select PLA, which is steered by a combination of address bits 0 to 7 and the DREG outputs. DREG steers both data and status register files and most of the port oriented hardware in the front end. This hardware includes a multiplexer whose inputs are the controller's option-selection switches, and several registers used to control interrupt generation to the host.

In addition, DREG supplies a port selection function in addressing the executive RAM, but in this case DREG's outputs are multiplexed with address bits A1 and A2. Vectors are loaded into the various ports' interrupting peripherals, two locations apart, and these two address bits select which port's dedicated location is addressed when the firmware uses relative mode. For example, the firmware addresses location 4000 (hexadecimal), and any one of the four locations—4000 (equivalent to C000), 4002, 4004, or 4006—is accessed as controlled by DREG [Fig 4(b)]. The firmware cannot address these locations directly in relative mode since DREG overlays the programmed address. During a hardware interrupt response, location C0xx is addressed with the XX being supplied by the interrupting peripheral [Fig 4(c)]. Port 0's PIO supplies 00 to address C000, port 1's PIO addresses C002, etc, with A15 forcing absolute addressing to one of four locations which all appear as 4000 to the firmware. This method (Fig 5) is used for all interrupt vectoring. Extended use of DREG makes it unnecessary for a task ever to know in which port it is installed, thereby significantly increasing the overall throughput of the controller.

Summary

Although the multifunction controller is limited to an aggregate throughput of from 4000 to 8000 bytes/s, depending upon configuration, this performance exceeds the requirements of the peripheral devices it is designed to handle. The microprocessor based design offers satisfactory solutions to most problems and objectives of a multipurpose intelligent peripheral controller: it allows reasonably fast response to the host, enables the system designer to mix or match peripherals, and provides an adaptable interface for additional peripherals. It can easily be configured for installation into a system, and is relatively inexpensive to manufacture and simple to service.

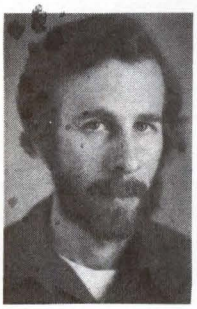
Bibliography

T. Dollhoff, "μP Software: How to Optimize Timing & Memory Usage," *Digital Design*, Feb 1977, pp 44-51

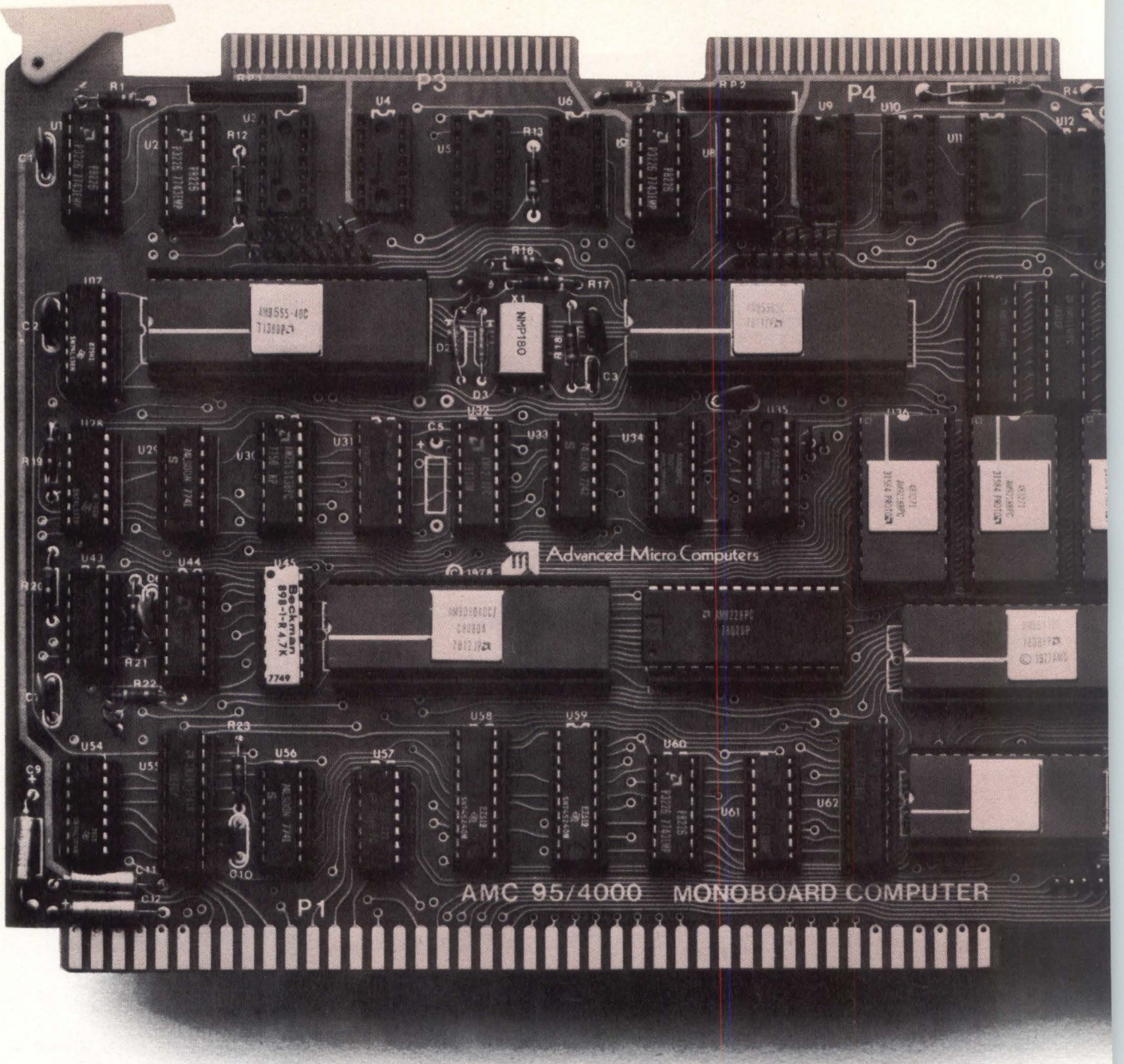
L. Teschler, "Interface Software for Microcomputers," *Machine Design*, Aug 10, 1978, pp 105-109

J. G. Wester and W. D. Simpson, *Software Design for Microprocessors*, Texas Instruments, Inc, Dallas, Tex, 1976

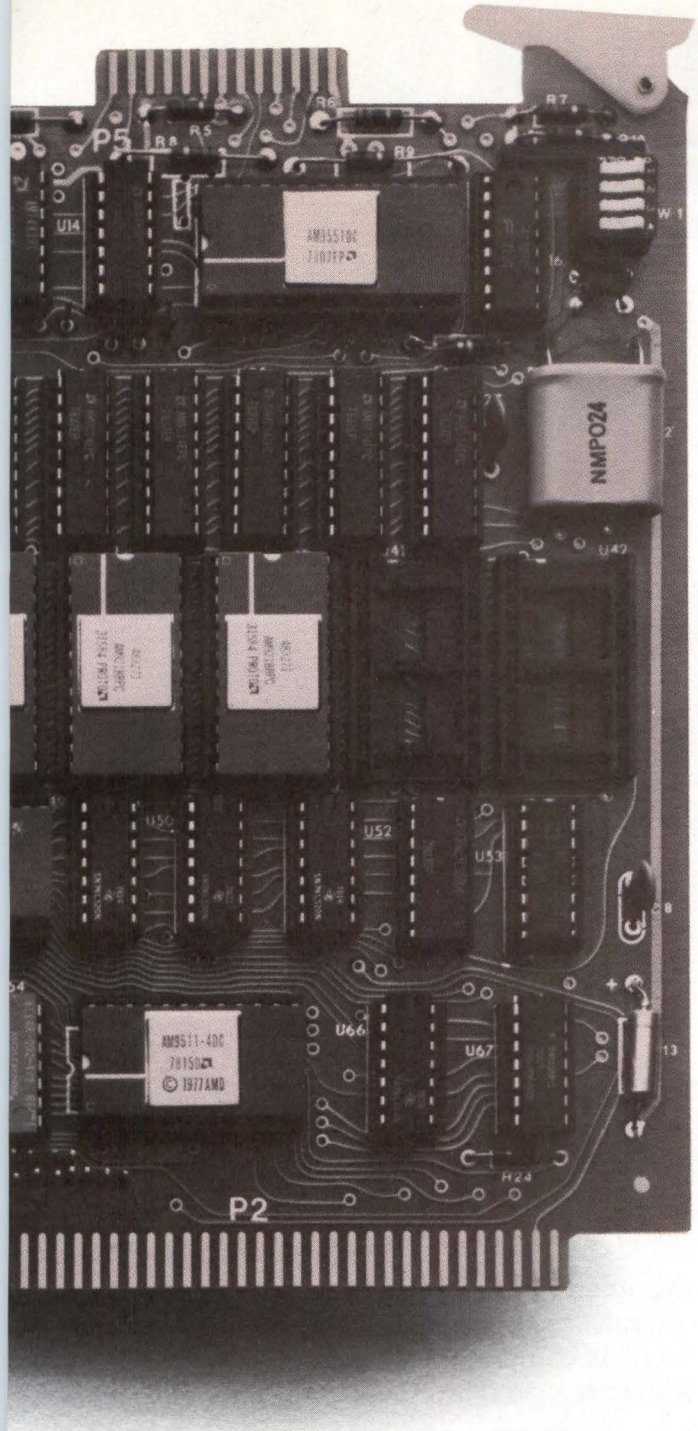
Zilog, Inc, *Z80-CPU Technical Manual, Z80-PIO Technical Manual, Z80-CTC Technical Manual*, Cupertino, Calif, 1976



Currently a design engineer and member of the technical staff with MODCOMP, Richard Binder has held various positions in the I/O development group, designing interfaces for an electrostatic printer/plotter, magnetic tape formatter, card reader, moving head discs, and bulk core memory modules. He attended Rose Polytechnic Institute, and has worked as a mechanical designer and technical illustrator.



THE CHAIRMAN OF THE BOARD.



MEET THE MONOBOARD™ THE WORLD'S MOST POWERFUL SINGLE BOARD COMPUTER.

AMC's Monoboard, the AMC95/4000, is the new boss of microcomputer boards. It performs complex math at twice the speed of any other board. And it can process data at clock rates of 2MHz or more.

The Monoboard really has what it takes to be a leader. It performs both floating-point and fixed-point math operations in the blink of an LED. It can do 16- and 32-bit two's complement arithmetic (add, subtract, multiply and divide), 32-bit floating-point operations, plus transcendental and data-manipulation functions.

But those aren't the only reasons the Monoboard is taking over. It also has four independent DMA channels, 4K bytes of RAM, space for up to 12K bytes of ROM/E-PROM, a serial I/O port, and 48 programmable I/O lines.

And the Monoboard has the same physical configuration as the SBC-80 card family. So anyone now using SBC-80's can pack more power in their systems by simply plugging in the Monoboard.

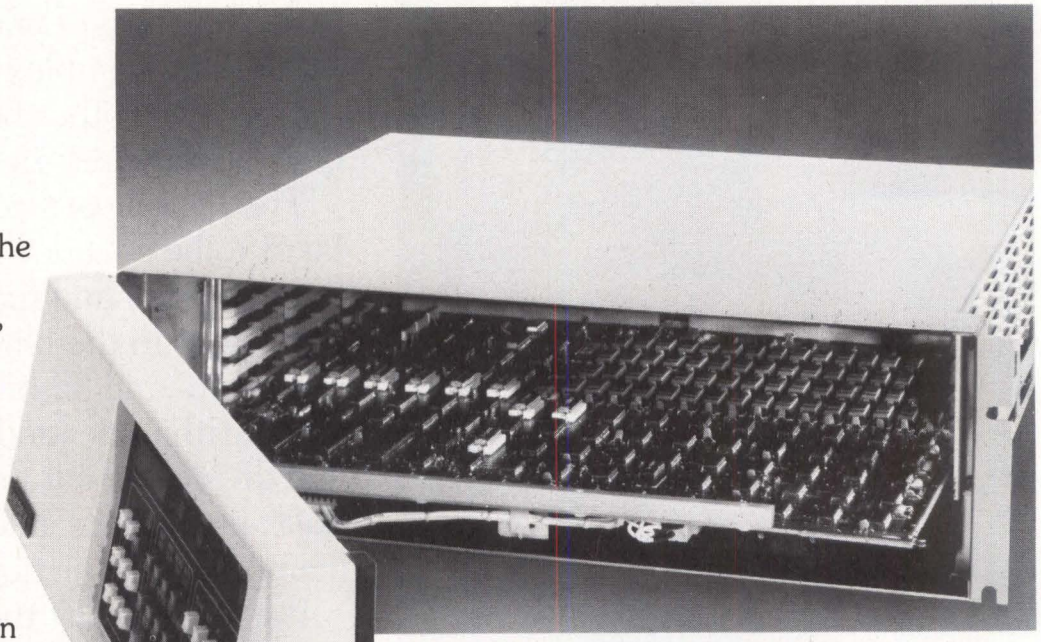
If you want power, and lots of it, get the Chairman of the Board on your side. Get the Monoboard from AMC.

Advanced Micro Computers

3340 Scott Blvd., Santa Clara, CA 95051. (408) 988-7777
Distributed by Advanced Micro Devices.

CIRCLE 137 ON INQUIRY CARD

THE OTHER FOUR SLOTS ARE FOR YOU.

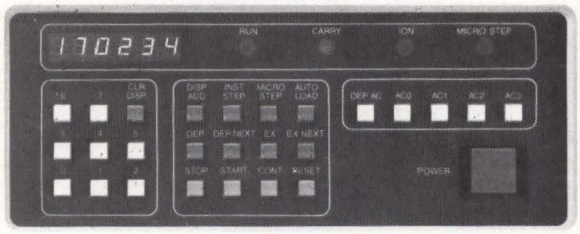


AMPEX MINICOMPUTERS COMBINE CPU AND 64K MEMORY ON ONE BOARD.

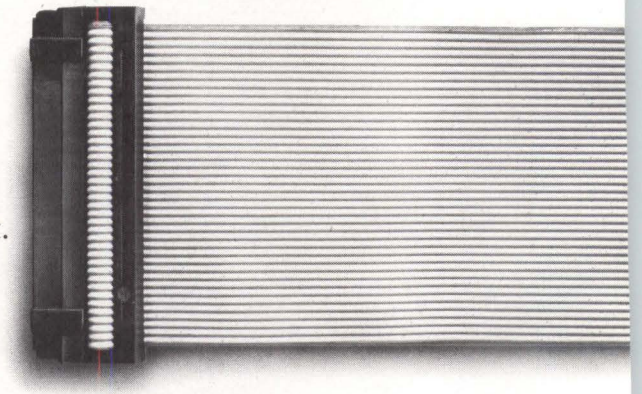
Behind the panel of the 5¼-inch high Ampex 8MS5 Minicomputer, there's an 800 nanosecond CPU and as much as 64K words (128K bytes) of memory. All on a single board.

Leaving four big slots for your own cards. 15 x 15 inch boards, with whatever you need to realize the goals of your system. Insert controllers for disk, tape, printers or terminals. As long as the controller is compatible with NOVA*, it'll be compatible with the Ampex 8MS.

That's because Ampex designed this minicomputer to take full advantage of the environment that has grown up around NOVA computers. But *this* mini has some extras you never expected to see in a mini.



Like front access to all components. And a programmer's console with octal pad input, octal readout and LED indicators. Plus a single bus structure.



Charley Penrose has some suggestions about achieving big system capability in the little 8MS cabinet. Call him at 213/640-0150. Or write to him at Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245.

*NOVA is a trademark of Data General Corporation.

AMPEX MAKES IT EASY.

CIRCLE 41 ON INQUIRY CARD

LOGICAL ENVIRONMENT COMPARISON TESTING HANDLES COMPLEX LSI DEVICES

Evolving from basic comparison methods, conditioned natural environment testing combines the broad capabilities of a large, complex system with the cost advantages of a small LSI tester

Abraham Bluestone Adar Associates, Inc, Burlington, Massachusetts

The proliferation of large-scale integration microprocessor, peripheral interface, and memory chips has brought with it an urgent need for complex and exacting testing capabilities. While available computer-controlled automatic test systems offer technically competent checkout and diagnostics, the high cost of acquisition and software support hinders widespread implementation. An economical, general purpose, programmable test approach for these complicated devices involves the generation of functional logic sequences and permits electrical testing under worst-case conditions. This type of testing has traditionally been handled in three ways: by inhouse systems costing more than $200,000; by in-system testing, less expensive initially, but also less effective and more costly in rework and system failures; or by outside testing services. The choice of these methods is easier for those who can afford the cost of a large sophisticated test system; others are generally limited to the second or third alternative. Recently, however, significantly less expensive test systems for these devices have evolved. They use an updated version of the established technique called comparison testing, which compares the operation of the device under test against the responses of a known-good device.

Test System Evaluation Criteria

Evaluation of a low cost large-scale integration (LSI) test system should encompass the following factors:

Cost—In addition to the hardware expense of a large, general purpose test system, programming and operating costs are significant extra burdens. To be widely affordable, a test system should have a base price under $50,000, with programming and operating costs correspondingly low.

General purpose capability—Test systems dedicated to one LSI device, or to a family of devices, are severely limited in flexibility. To be cost-effective, the test system must be capable of testing a wide variety of microprocessors, memory devices, and microprocessor support chips such as CRT terminal and disc controllers, as well as customized LSI digital devices.

Programming ease—The system should be readily accessible to all design, quality control, and component evaluation engineers, as well as to test equipment programmers. This accessibility can be facilitated if the "natural programming language" of the device under test (DUT) can be incorporated into the test system software, and if functions to be tested can be

described directly rather than through a highly conventionalized test system language.

Test validity—Most importantly, the system must assure completely valid testing procedures and results. In particular, the system should be able to program logic sequences to simulate any desired in-system operating modes, generate worst-case instruction sequences, and provide all asynchronous and/or control inputs, or any similar functions. It should also be able to vary all electrical parameters, ie, timing relationships, logic levels, bias voltages, and output loading, to permit full worst-case testing.

Testing Techniques

Most LSI test systems fall into one or more of the following categories.

Substitution Testing

This technique is performed by placing the DUT in a known working system, its "natural environment," and observing its behavior (Fig 1). There are obvious advantages to substitution testing: zero system purchase price, minimum investment in software development, and fast system startup, since test software, if required,

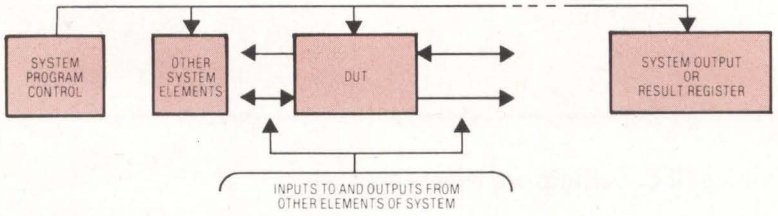


Fig 1 Substitution testing. If system operates properly with DUT inserted, ie, program is run and correct output or result is obtained, DUT is presumed good

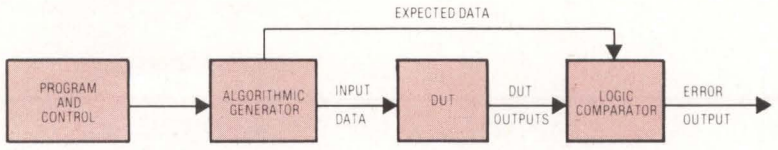


Fig 2 Algorithmic generation testing. Logic sequence calculated by algorithmic generator provides inputs to DUT. DUT outputs resulting from these stimuli are compared with calculated (expected) outputs, also provided by algorithmic generator

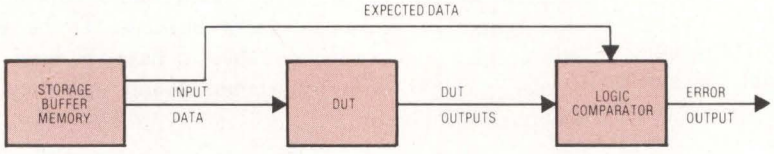


Fig 3 Stored truth table testing. Logic sequence (truth table) for DUT is stored in buffer memory. As input data are clocked out to DUT, expected output data are routed to comparator

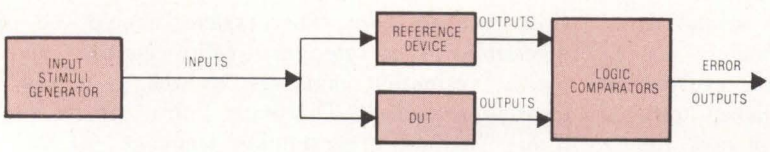


Fig 4 Basic comparison testing. Both reference device and DUT receive same input stimuli. Responses of reference devices are used as expected data, against which responses from DUT are compared at each and every clock time

is written in a language already familiar to the system designer.

There are equally obvious disadvantages. Substitution testing neither provides the capability to classify devices nor easily obtains failure diagnostics. Also, it ties up the final product as a test bed. The most serious objection, however, is that it does not assure completely valid electrical testing, since it has little or no ability to margin or stress the DUT.

Algorithmic Generation Testing

A test system using this technique (Fig 2) requires the construction of a high speed specialized computer that can generate complex logic sequences used as input (drive) and output (expected) data for testing the DUT. The technique has been highly successful in memory testing. It offers the ability to generate complex logic sequences at very high speeds, and can be readily coupled with true electrical testing—varying the test parameters.

On the other hand, the system is difficult to program, requires detailed knowledge of both the algorithmic generator and the DUT, and could require enough auxiliary hardware to bring the final price to well above that of a "low cost" system. Moreover, it is probably impossible to develop, except at great expense, an algorithmic generator that will permit testing the logic state of every pin, for a variety of devices, at every clock time throughout the test. In effect, algorithmic testing is limited to the occasional sampling of outputs on a fairly narrow class of devices, which is not the ideal solution for a general purpose LSI tester.

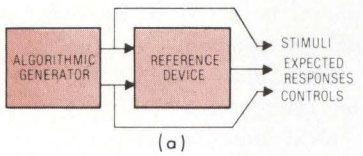


Fig 5(a) Algorithmic comparison testing. Algorithmic generator computes only input data to reference and DUT. Reference computes expected data routed to logic comparators

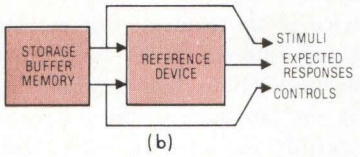


Fig 5(b) Stored truth table comparison testing. Use of reference device to compute expected data simplifies design of either algorithmic generator or buffer storage memory. Since reference computes expected data, task storage buffer memory system is considerably simplified

Stored Truth Table Testing

Stored truth table testing is performed by placing patterns of 1s and 0s in a high speed storage buffer memory and sequencing through the pattern, presenting device inputs to the DUT, and expected data to the tester (Fig 3). Conceptually, implementation of this test technique is simple. Because the bit pattern can be fully defined, completely random, or arbitrary, and because data can be specified in each and every clock time, stored truth table testing is suitable for many logic devices. It is particularly successful when applied to read-only memory (ROM) and small- and medium-scale integration (SSI and MSI) device testing.

Keeping storage buffer costs to a reasonable level, however, requires either sophisticated software or hardware involving looping, semi-algorithmic subroutines, pattern partitioning, and other techniques. Implementation of such complex systems and processing usually involves considerable expense in terms of computer, disc, and programming. In fact, all large LSI test systems in the $200,000 to $400,000 price range employ some variation of these sophisticated stored truth table processing techniques for logic sequence generation.

Comparison Testing

Here a reference device is used to predict the behavior of the DUT (Fig 4). Comparison testing is a practical, low cost, but minimal solution to device testing. The key reason for this technique's low cost is that data are generated by the reference device itself, eliminating the large amounts of memory needed by other types of testers to store both test stimuli and expected responses. Granted that the basic role of the reference device is to "compute" expected data, virtually any type of input stimuli hardware can be used. Fig 5(a) shows an algorithmic generator and Fig 5(b) a stored truth table buffer memory, each employed in reference testing. In both cases, the logic stimuli generator provides inputs to both DUT and reference device, as in the examples of Figs 2 and 3. However, in Fig 5, the reference devices provide expected data, considerably simplifying test system design and programming.

In spite of these attractive attributes, comparison testing has fallen into disfavor for two principal reasons. First, in its basic form it is incapable of performing electrical testing, ie, providing electrical stresses to evaluate DUT performance under worst-case conditions. Second, where the previous objection has been overcome, it has been at the price of also stressing the DUT, raising the question, "What failed—the DUT or the reference?"

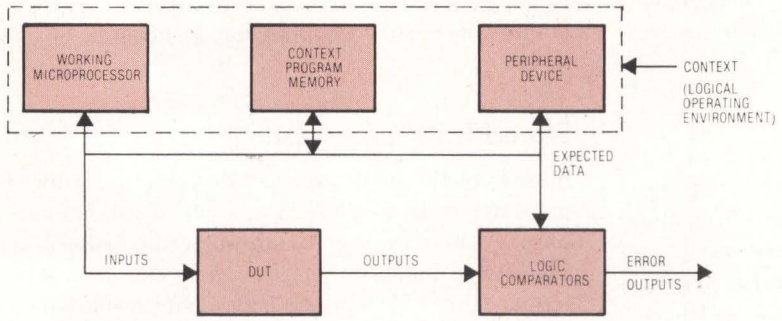


Fig 6 Basic CNE testing. Operational environment—or context—contains both stimuli generator and source of expected data

A carefully designed comparison test technique, conditioned natural environment (CNE), eliminates these problems and meets all other criteria for a low cost LSI test system. The specific issues addressed are (a) logic sequence generation capability—adequate for the most complex LSI devices at extremely low cost; (b) general purpose capability—ability to test any device, without restriction to particular families or device types; and (c) full program control over all electrical variables, allowing complete stressing of the DUT while completely isolating the reference device from these stresses.

Conditioned Natural Environment Testing

Any of the described testing techniques may be used in comparison testing to provide either inputs or expected outputs. However, since microprocessors and their peripheral or support devices are designed to work together as elements of electronic assemblies, these assemblies form the logical "environments" for such devices. Because the device is expected to perform logically in such an environment it should, ideally, be tested in it. CNE testing provides a means of simulating such environments—or contexts—for purposes of logic sequence generation, while at the same time permitting full electrical testing of the DUT.

Generating Logic Sequences

At the core of CNE testing is a working microprocessor assembly (Fig 6) which replaces the simple input stimuli generator of Fig 4. Truth tables (logic sequences) are generated online, in real time, by having the working microprocessor, and peripheral device if present, execute a program previously stored in the memory.

For microprocessor testing, the context microprocessor is the reference device, the DUT is another microprocessor of the same type, and there is no peripheral device. As the context microprocessor executes its program, its inputs from memory are routed to the DUT as drive data and its outputs are routed to the logic comparators as expected data.

If a peripheral device is to be tested, the context—or operational environment—is expanded to include a like device, which now becomes the reference. Again, inputs to the reference, which may now come from either the context microprocessor or the context program memory, are also routed to the DUT as inputs, while reference outputs serve as expected data.

Any logic sequence that the DUT may see in actual operation can thus be generated. Furthermore, changes in desired logic sequences can be quickly generated by simply changing the program stored in memory. In every case, as the context operates on its stored program, each DUT pin sees the same sequence of input logic states at every clock time as does the corresponding reference device in the context. Context logic sequences are also used as reference data for output comparison purposes. The instructions that generate logic sequences are written in the language of the microprocessor itself, and can be readily modified to reflect differing operating requirements.

Providing General Purpose Capability

The concept of the context can be modified to permit testing virtually any type of LSI digital device. The CNE test system is configured to test any given peripheral DUT by inserting a known-good device into the context. Similarly, to reconfigure the CNE system to test any given microprocessor DUT such as an 8080A, 6800, or Z80, it is only necessary to change the context microprocessor.

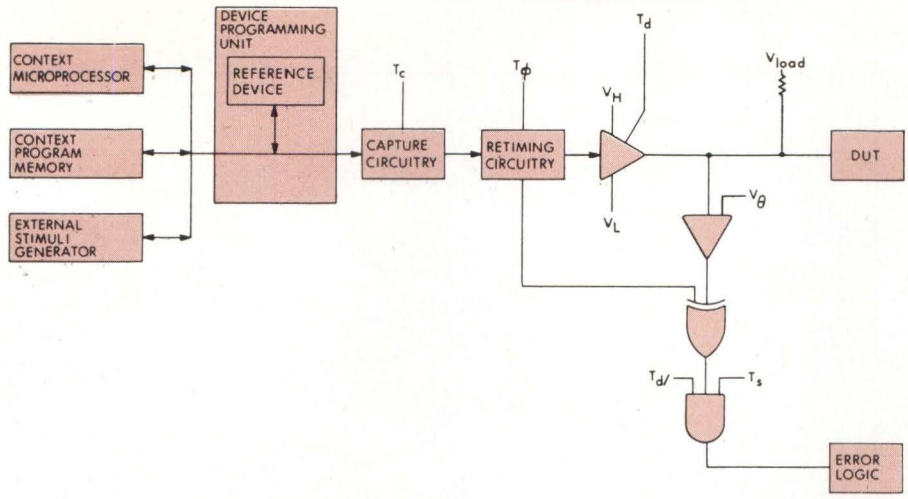


Fig 7 CNE testing. Reference device is isolated from DUT. Signals generated in context are captured, buffered, and shifted in time and voltage levels before being presented to DUT

As actually implemented, reference devices, whether they are microprocessors, programmable interface adapters, or terminal controllers, are physically located in an assembly called a device programming unit (DPU) (Fig 7). There is a DPU for each device type to be tested, and the act of changing DPUs automatically changes the required reference device and reconfigures the system appropriately to test that device.

Changing Timing Relationships

In its simplest form, comparison testing consists of driving the reference device and the DUT with fixed timing from a common source into fixed comparators. Drivers and comparators, for example, might be simple transistor-transistor logic (TTL) gates.

At a somewhat higher level, programmable drivers and sensors can be added. While this offers some improvement in testing, it is still less than ideal, since the reference device and the DUT share the same timing. Consequently, any margining applied to the DUT is automatically applied to the reference device. Therefore, the question of how good is the reference device remains unanswered. Best solution to this problem is a test system in which the timing to the reference, except for clock period, is completely separate from that to the DUT. This approach is basic to CNE testing, and is accomplished by the timing and voltage conditioning circuits shown in simplified form for one DUT pin in Fig 7.

As the context program runs, signals on the context bus lines, which are inputs to the reference device, are also routed to capture flip-flops. These signals are then captured by clocking the flip-flops with programmable timing edge T_c. This operation captures and preserves the logic state (1 or 0) of the signal. Having captured the logic signal, it is now possible to present it to the DUT at any desired time by clocking it out using another programming timing signal T_ϕ.

The manner in which this test system permits changing timing relationships, and hence the stresses seen by the DUT without stressing the context, is shown in simplified form in Fig 8. Two signals, A and B, have durations, polarities, and edge relationships as generated by the context. Both signals are captured, at different times chosen by the test system programmer, by edges T_{c1} and T_{c2}. Having thus preserved the logic states, the programmer determines when to present signals A′ and B′ to the DUT by assigning appropriate values to $T_{\phi 1}$ and $T_{\phi 2}$. Finally, he determines the duration of the two signals as seen by the DUT by gating them off with edges $T_{\phi 3}$ and $T_{\phi 4}$. As a result, the DUT is stressed in three different ways, all under program control: (1) the relationship between the leading edges of signals A and B, designated L, can be varied; (2) the duration of signals can be changed; and (3) the interval between the trailing edges of signals A and B, designated T, can be varied. Thus, while the DUT sees the same logic sequences as the context, the signals have been shifted in terms of their time relationships and their durations have been altered. If necessary, their formats could also have been changed.

Fig 7 also shows that if the signal is to be treated as an output (data) signal and compared with the output of the DUT, it is routed to one side of an exclusive-OR (XOR) gate and control signal T_d turns off the driver. Then DUT output is appropriately loaded by programmable supply V_{load} and sent to a threshold detector/comparator, where it is compared to a programmable threshold voltage V_θ. The comparator output then joins the captured signal at the XOR gate and is strobed at a time T_s selected by the test program. Note that the strobe circuit is turned off by

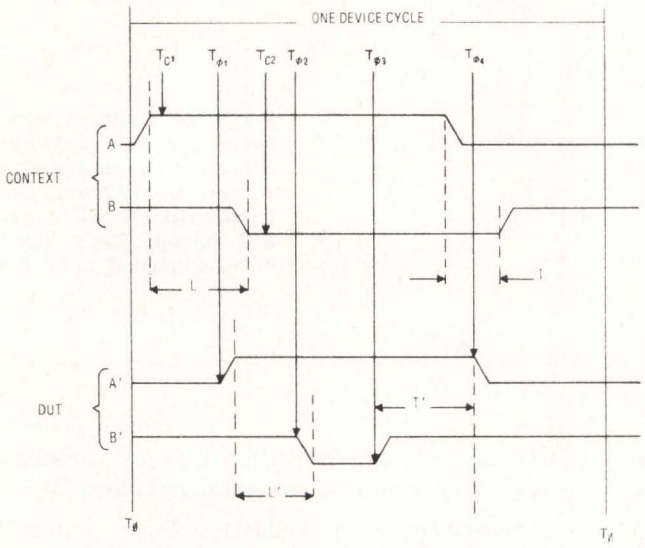


Fig 8 Changing timing relationships (stressing DUT). Capture and reclocking circuits allow timing relationships generated in context to be radically changed, as seen by DUT

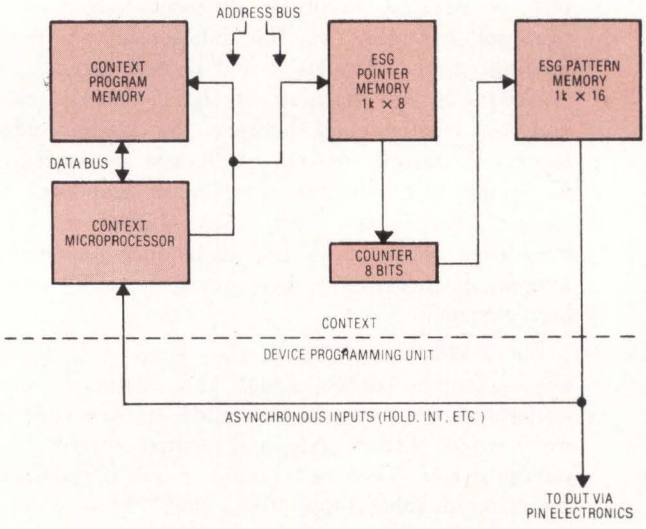


Fig 9 External stimuli generator. Data stored in ESG pattern memory are clocked out under program (pointer) control, to provide asynchronous inputs to reference device and DUT

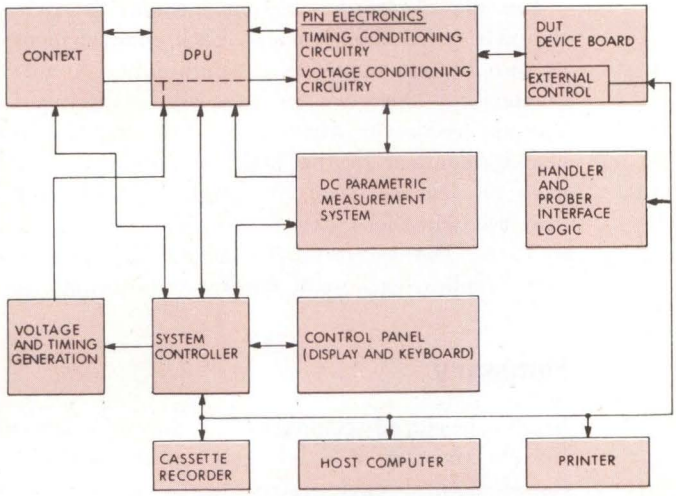


Fig 10 Simplified block diagram of MX-17 LSI test system. Design is based on "conditioned natural environment" (CNE) testing concept. Key to successful practical implementation is DPU, which reconfigures system as required for any LSI logic device

$T_{d/}$ when the DUT pin is treated as an input, and that the driver is turned off by T_d when the DUT pin is an output.

Providing Voltage and Loading Stresses

In Fig 7, if the signal is to be treated as an input, it is routed through the retiming circuitry to a 3-state driver whose high (V_H) and low (V_L) levels are fully programmable. In this manner the voltage levels seen by the DUT can be completely different from those seen by the reference device, providing the ability to voltage-stress the DUT without affecting the context and the reference.

In a similar manner, when the signal being captured is to be treated as an output or expected data, provision is made for loading the DUT output without affecting the reference device. Separate loads, fully programmable, are provided for source and sink. Switching from source to sink loads occurs at full test speeds.

Providing External Stimuli

The ability to simulate the various interrupts that the DUT might encounter in actual operation is crucial to thorough testing. CNE testing satisfies this criterion with a subsystem called the external stimuli generator (ESG) (Fig 9). ESG, essentially a stored truth table sequence generator, consists of a control or pointer memory and a pattern memory whose contents form part of the test program.

The control memory, addressed by the context microprocessor, initiates, controls, and terminates pattern memory output cycles. Data contained in the pattern memory represent patterns of desired combinations of control functions, such as ready, reset, hold, and interrupt. Data out of the pattern memory are routed to the context microprocessor, the DUT, and other system components, where they are translated as the desired external stimuli. Consistent with overall CNE system design, ESG outputs can be specified on a clock-period-by-clock-period basis.

Comparison Test Issues

One of the important problems related to comparison testing is that of the integrity of the reference device, that is, its ability to operate properly under favorable conditions. Since CNE testing provides stored programs to the reference device, these programs include self-tests which verify the performance of the reference device by reporting results to another processor. While such self-tests are often relatively short, the CNE technique permits virtually exhaustive self-testing, if required.

Another problem is that there is a possibility that the comparison tester will show "pass" results because both reference device and DUT are equally unable to meet the test conditions. CNE resolves this problem by operating the reference device in a totally separate and benign environment in which all timing relationships (except clock period), all drive and sense levels, and all biases are at their most favorable values. Worst-case or stress conditions are apparent only to the DUT.

Two disadvantages associated with comparison testing remain as valid criticisms of the CNE technique. One is the inability to test the DUT at cycle times faster than the reference device will run. As a practical matter, the use of premium reference parts will allow the tester to operate at speeds considerably above nominal specification values. This limitation on comparison testing thus becomes of little real significance in production testing.

Second disadvantage is, that since it is clearly impossible to comparison-test the first part of a new design, the engineering designer concerned with advancing device technology does encounter a meaningful restriction. He cannot use the CNE tester unless he provides a reference device emulated by some other technology.

CNE Implementation

The CNE test concept is implemented in actual application as the MX-17 LSI test system. This system comprises the major functional elements shown in Fig 10. The system controller contains a Z80 microprocessor and 16k bytes of memory. The controller processes and routes all program information, data for the context program memory and ESG system, system control instructions, and system outputs. System controller bus, (16 addresses, 8 data bits), handles all input/output and external control, including communication with the printer, host computer, DUT device board, handler/probers, cassette recorder, and control panel.

Program-stored test values are sent from the controller through a digital-to-analog subsystem to the DPU, then routed either to the context or to the DUT. The signals to the context simply provide clock(s) to specify the test cycle time, and impose no stress. Signals to the DUT are first routed through the timing and voltage conditioning circuitry in the pin electronics section to impose the specified stress conditions on the DUT.

The context provides the logic sequences for the DUT. Major elements of the context are a microprocessor, a context program memory, the ESG, and a reference or companion device to the DUT (actually housed in the DPU). DPU configures the test system for the specific device being tested. It houses the reference device which works with the context in generating logic sequences for the specific DUT. It assigns 14 voltage and 46 timing signals to the appropriate pin electronics lines, and it also processes the timing edges received from the timing generation subsystem to form clocks or to assign them to control functions and route them to the pin electronics.

The pin electronics section includes 40 drive/sense channels (expandable to 56). Each channel incorporates its own timing and voltage conditioning circuitry, programmable 3-state driver/sensor, variable output loading, and error logic. There are also four low-level clocks, identical to the logic drivers except that they have no sensing capability, and two high-level clocks provided for those devices requiring drive signals up to 15 V. The section also contains four bipolar device bias supplies, each with current monitoring capability.

Summary

Newly developed comparison techniques are proving the effectiveness of a low cost LSI test system. Conditioned natural environment (CNE) testing, a concept developed for the MX-17 LSI test system, satisfies the following major criteria: (1) it is a low cost system; (2) it provides general purpose testing, not only of microprocessor family devices, but also of a broad range of other devices such as memories, custom LSI devices, and microprocessor support chips; and (3) it provides completely valid electrical testing. All electrical variables to which the DUT is exposed are under program control, and the logic sequences applied to the DUT are those derived from a "natural use" environment. CNE testing, therefore, provides the inherent capability to perform test and margin testing under realistic operating conditions.

Bibliography

Adar Associates, MX-17 Microprocessor Family Test System," Preliminary Data, Adar Associates, Inc, Burlington, Mass, 1977

R. L. Alonso, D. W. Madsen, and H. Thaler, "Conditioned Natural Environment Testing (CNE)—A Low Cost Approach to Full Electrical Testing of Microprocessor and Related Components," *Digest of Papers*, Semiconductor Test Symposium, 1977, pp 42-46

Abraham Bluestone, currently MX-17 product manager, has been with Adar Associates since 1974. Before that he was associated with Teradyne in sales, marketing, and product planning activities. Mr. Bluestone is an active participant in the IEEE Semiconductor Test Symposiums at Cherry Hill, NJ, having appeared in the last three years as a contributor, panel member, and session chairman.

ChainTrain® 1290 — geared down to 900 LPM's to meet 900 LPM budgets.

Now, in the new ChainTrain Model 1290, you can get those same dreamed-about features offered in the ChainTrain 1200 LPM model, only you can get them at 900 LPM's and at conventional 900 LPM prices. The 1290 can handle more 900 LPM tasks at an improved cost/efficiency rate than any other printer on the market! It offers motorized upper and lower tractor positioning, heavy-duty ChainTrain reliability, and it's completely microprocessor (8080A) controlled. There isn't a lot more you could ask from a 900 LPM printer, but we've got a helluva lot more to tell you about it. Communicate with us. We have the ability to respond very, very quickly!

DATA PRINTER CORP
99 Middlesex Street, Malden, MA 02148
Tel: (617) 321-2400 TWX: 710-348-0794
Regional Sales Offices: Clifton, NJ, Santa Ana, CA

Visit Data Printer Corp. at Booth 1230, Interface '79, Chicago, April 9-12, and at Booth 2017, NCC '79, NYC, June 4-7.

CIRCLE 42 ON INQUIRY CARD

APPLICATION NOTE

Number Sorting Algorithm Saves Processing Time

Algorithm for data manipulation accomplishes fast number sorting with microprocessor. Minimal program eliminates clock cycles since number comparisons and associated decision instructions are unnecessary

Martin Newman Tadiran Electronics Industries, Petach Tikvah, Israel

A fast operating number sorting algorithm—a version of the Radix Sorting Method[1]—used within the framework of a traffic analysis procedure with an 8080 microprocessor serves to monitor usage of telephone extensions. Input data to the algorithm consist of a list of telephone extensions together with the number of external calls made at each extension. The algorithm processes this data and arranges the list of extensions corresponding to the number of external calls made at each extension. For application purposes, it is assumed that there are 100 extensions and that the maximum number of external calls made at any extension during the period of analysis does not exceed 127.

Algorithm Details

Input data are listed in two tables —a link-address table and a number table. The former consists of pointers to locations containing the names of the telephone subscribers, while the latter contains the number of calls made by each subscriber in an order corresponding to the link addresses (Table 1).

The algorithm implements two additional tables: an auxiliary table, consisting of 128 locations, that stores the range of call values (0 to 127), and a results table which, upon conclusion of the algorithm, contains the link addresses arranged in a sequence determined by the corresponding values in the reconstructed number table.

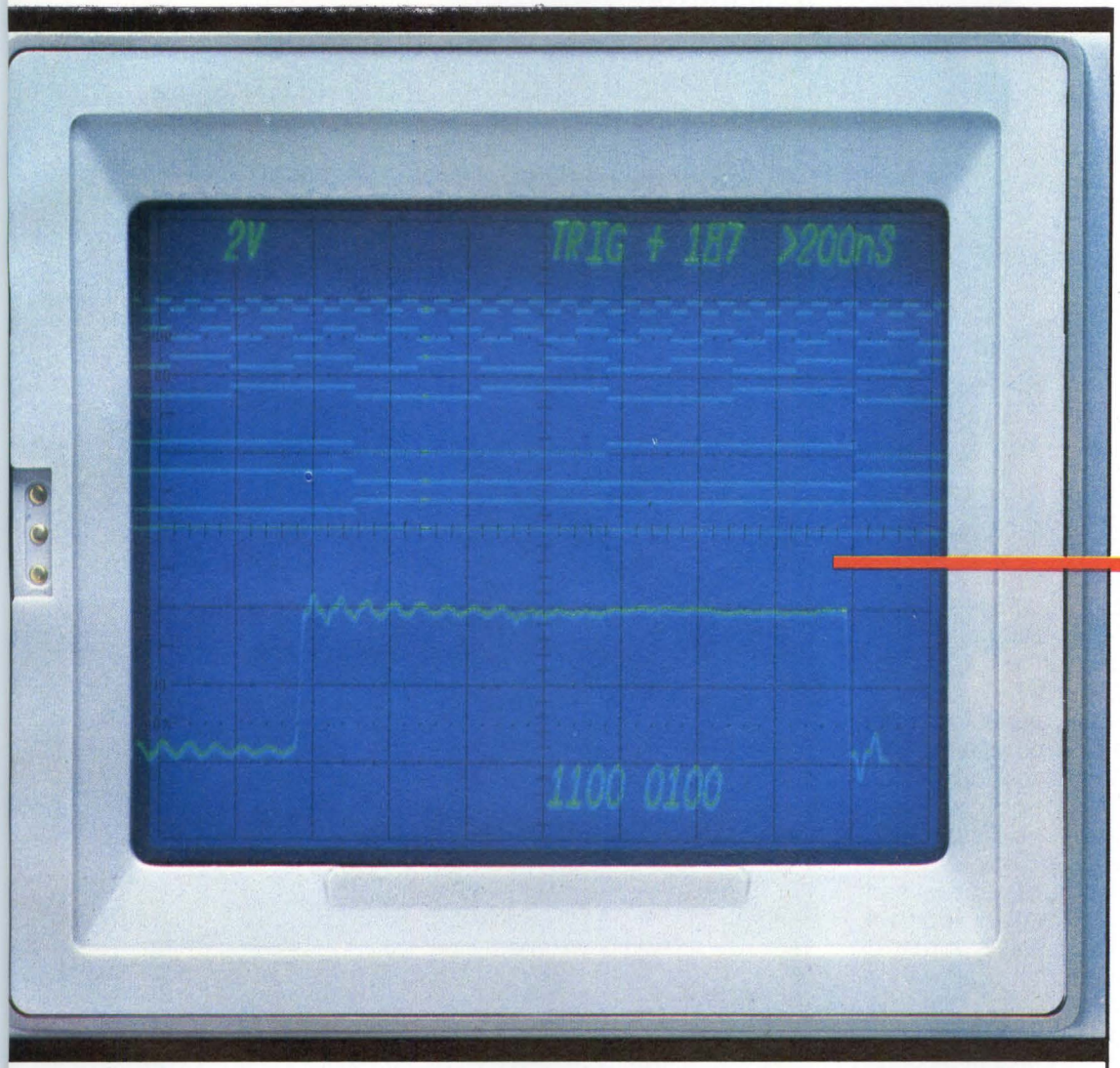
TABLE 1

Data Organization in Telephone Traffic Analysis

Entry No	Number Table	Link Address Table	Subscriber
0	28	279	Jones
1	16	280	Wills
2	5	281	Smith
3	32	282	Thompson
4	95	283	Johnson
5	1	284	Weaver
6	80	285	Fowler
•	•	•	•
•	•	•	•
•	•	•	•
99	72	378	Jackson

TEKTRONIX thinks your logic analyzer should be as versatile as you are

So ours let you see analog and digital displays *at the same time.*



Verify logic and analog relationships at a glance

Digital troubleshooting usually involves two steps: First, logic analysis to find where the problem is located. Then analog measurement to pinpoint the source.

Tektronix 7000-Series Plug-Ins give you both steps. Presented together on the same display: a complete picture of the analog/digital relationship.

Many Tektronix 7000-Series Mainframes allow the 7D01 Logic Analyzer plus vertical amplifier and time base plug-ins to all be housed in a single mainframe. The same configuration gives you full analog *and* digital capability.

First, locate a logic problem with the 7D01's timing display and retain it on the screen through memory. Next, make the analog measurement and put it up on the same display. Both sides of the problem are now revealed in a single image.

Simultaneous analog/digital display: it helps make our Logic Analyzer versatile. So you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

Tektronix®
COMMITTED TO EXCELLENCE

For technical data, circle 43 on Inquiry Card. For a demonstration, circle 44 on Inquiry Card.

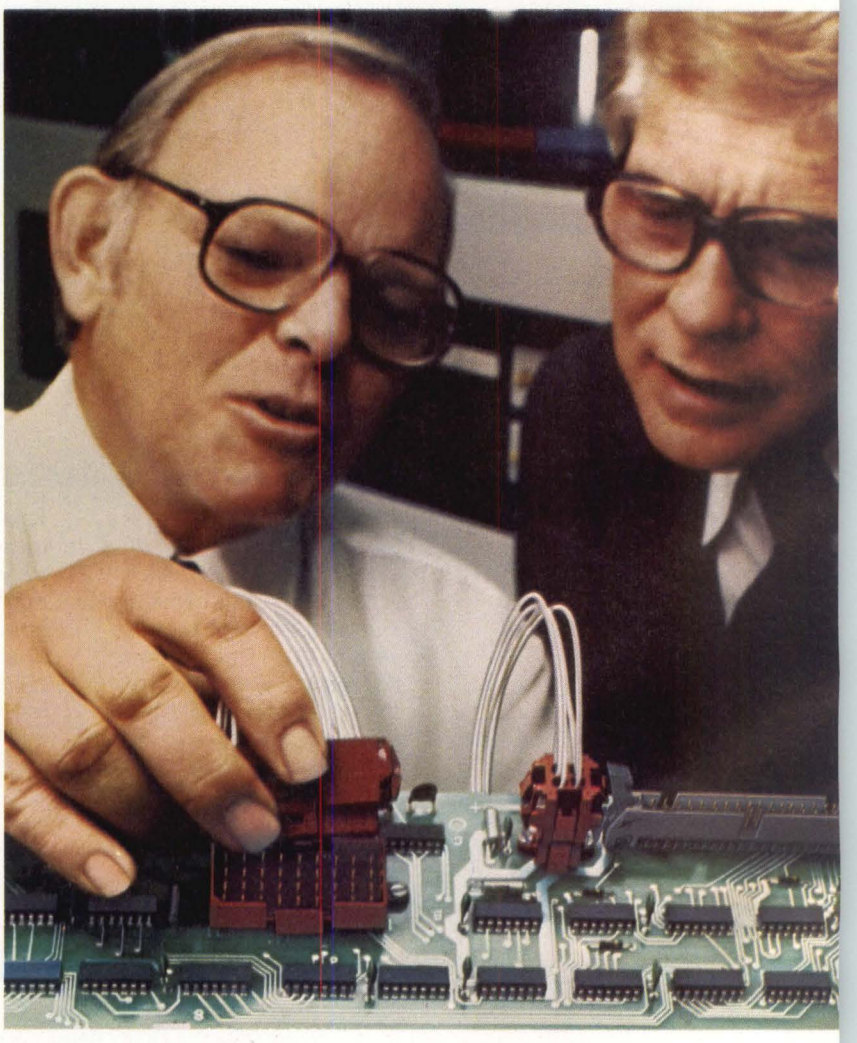
TEKTRONIX LOGIC ANALYZERS THE VERSATILE ONES

For immediate action, dial our toll free automatic answering service: 1-800-547-1512

"Pin hoods...bolts...jackscrews—just show me a way to reduce connector hardware costs without cutting down the reliability as well."

O.K. Here it is.

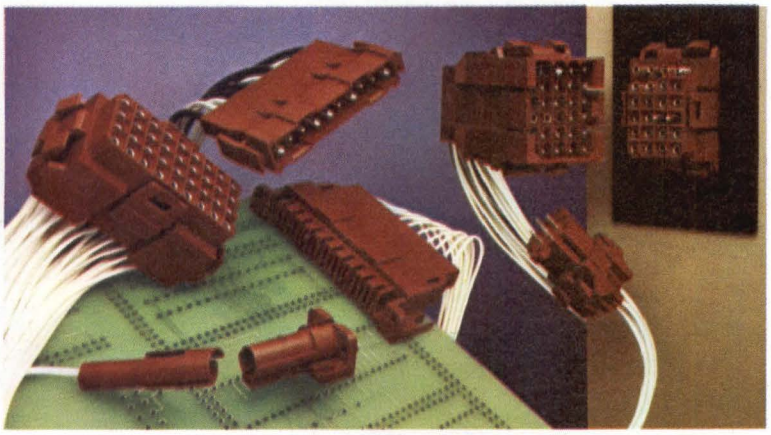
When you switch to the AMP Metrimate Connector line be ready to save as much as $3.50 per connector. In your product and assembly costs. And in your inventory costs. Because Metrimate gets rid of separate pin hoods, mounting hardware and connecting parts. It molds all of them into a housing designed to true metric dimensions.
Are they reliable? They meet all general requirements of national and international testing and approval groups ranging from UL and CSA to IEC and VDE. And AMP technical service helps make sure things stay that way.
They are flexible, too. In fact, you can mix both pins and sockets in the same housing. And choose from a variety of contact types for standard wire, coax cable, or even fiber optics.
Look into the savings. Call the AMP Metrimate Information Desk at (717) 564-0100, Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

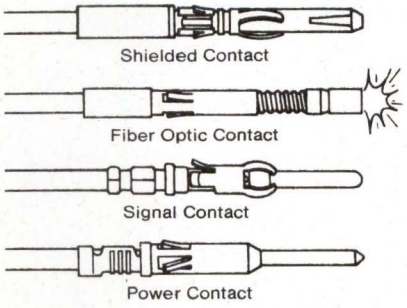


AMP is a trademark of AMP Incorporated

AMP has a better way.

AMP Metrimate.



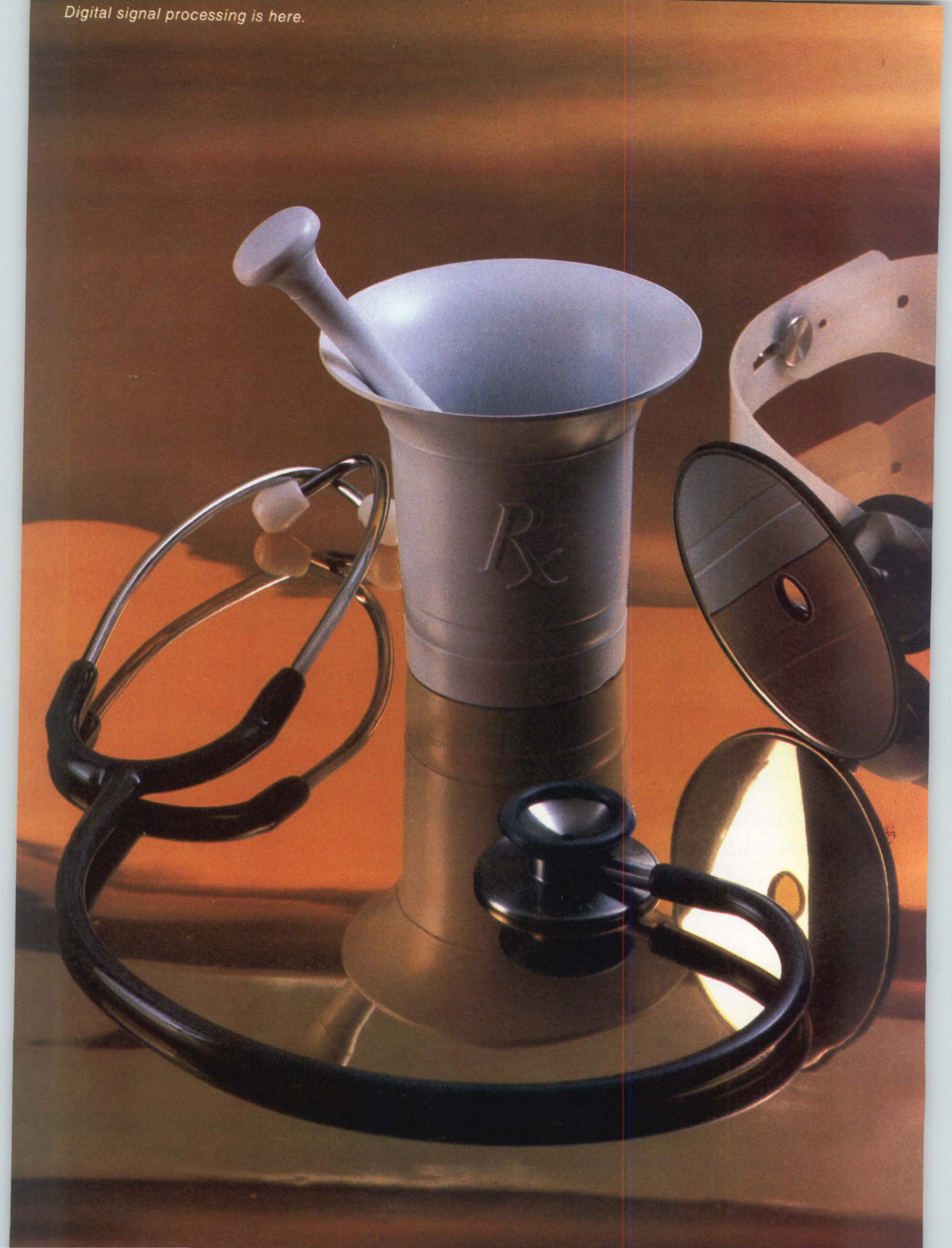


Some facts worth knowing about AMP Metrimate Connectors

Description: Part of AMP's exclusive Multimate Family that accommodates common contacts in a variety of connector housing styles and saves on both tooling and inventory costs.
Voltage rating: 380 VAC, 450 VDC (VDE); 600 VAC (UL); 250 VAC (CSA); 440V (IEC)
Dielectric strength: 1500 volts rms at sea level
Temperature: −55°C to +105°C
Current rating: Signal and Power Contacts; 13A max. per contact (limited only by connector block working temperature).
Insulation resistance: 5000 megohms, min.
Contact resistance: 5.5 milliohms, max.
Durability: 250 cycles, tin-plated contacts
550 cycles, gold-plated contacts
Where to telephone: Call the Metrimate Information Desk (717) 564-0100, Ext. 8400.
Where to write: AMP Incorporated, Harrisburg, PA 17105

AMP

CIRCLE 45 ON INQUIRY CARD


Digital signal processing is here.
Rx

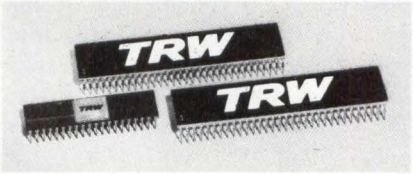
TRW takes another step in digital signal processing

INTRODUCING A NEW FAMILY OF MULTIPLIER CHIPS

We've just taken a giant leap forward and developed a new family of increased performance multiplier chips, called the "HJ" series.

You can select from among 16, 12 and 8-bit devices to provide sophisticated number-crunching options for your minicomputer.

Use our MPY-16HJ, -12HJ or -8HJ to boost your mini's arithmetic performance and you'll open up a wealth of new applications in areas that require general scientific algorithms, like FFTs.



In medical electronics for instance, FFT-supported imaging systems are becoming important supplements to X-ray diagnosis. New techniques—including ultrasound—are being used for viewing internal organs, soft tissue, tendons and blood vessels.

No matter how you decide to apply them, our new multipliers offer higher speed and lower power than any devices you've seen before—the MPY-16HJ, for instance, produces a 32-bit product in just 100nsec and its power consumption is a mere 3W.

Both the MPY-16HJ and -12HJ multipliers offer important new operating features, like zero-nanosecond input register hold time, transparent output registers, and operation on numbers in either unsigned magnitude form, two's complement or mixed. They are easily expandable—you can array them to multiply 32, 48, or 64-bit numbers and greater.

Our MPY-8HJ has a super-fast version available that produces a 16-bit product in just 45nsec. It is designated MPY-8HJ-1 and is specially suited to television applications.

These faster "HJ" series multipliers are plug-compatible with our popular "AJ" series multipliers. Just plug them into a socket wired for the corresponding "AJ" device, and the new features are automatically masked out. You can ignore the additional features and benefit from additional speed and reduced power.

Our new multipliers are very stingy with power—the MPY-16HJ uses just 3W; the MPY-12HJ, 2W; the MPY-8HJ, one lonely Watt.

Prices have been lowered for the new multiplier family, too—in 100's, the MPY-8HJ is priced at $59; MPY-8HJ-1, $71; MPY-12HJ, $103, and the MPY-16HJ, $157.

Like all TRW LSI Products, each of these new MPY/HJ multipliers is available from stock through Hamilton/Avnet. For more information, send in the coupon or talk to one of our digital signal processing experts at 213/535-1831.

TRW LSI Products
An Electronic Components Division of TRW Inc.
P.O. Box 1125
Redondo Beach, CA 90278

Please send data sheets on the new **MPY/HJ** family of multipliers.

Name _____

Company _____

Div/Dept _____ Mail Code _____

Address _____

City _____

State _____ Zip _____

CD-4

TRW *LSI PRODUCTS*
...for Digital Signal Processing

CIRCLE 46 ON INQUIRY CARD

TABLE 2

Pass 1

Number Table	Auxiliary Table: Location Address	Auxiliary Table: Location Contents
9	0	0
6	1	1
3	2	0
5	3	2
4	4	3
3	5	1
12	6	1
8	7	0
9	8	1
4	9	2
4	10	0
1	11	0
•	12	1
•	•	•
•	•	•
•	•	•
•	99	•

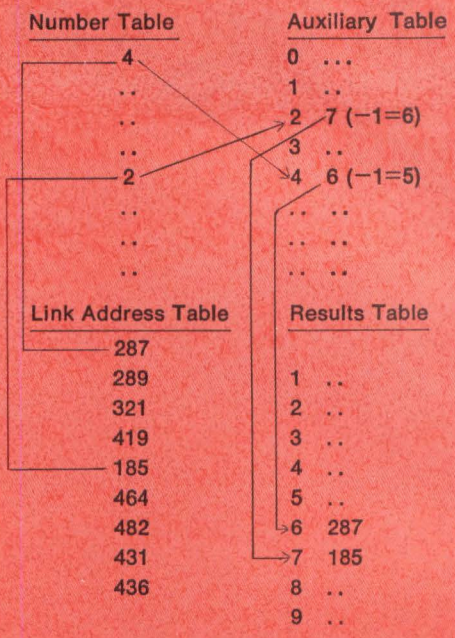
TABLE 3

Pass 2

Number Table: Location Contents	Auxiliary Table: Location Contents Before Pass 2 (Distribution of values)	Auxiliary Table: Location Contents After Pass 2
6	1	0
8	0	1
4	1	1
4	1	2
12	2	3
9	0	0
3	2	5
2	1	7
6	1	8
0	1	9
7	0	10
	0	10
	1	10

TABLE 4

Pass 3



Execution requires three passes, as follows:

Pass 1—Initially, the number table is scanned, and the numbers are used successively as pointers to locations in the auxiliary table (Table 2). Each time that a number is encountered, it is used to point to an auxiliary table location, whose contents are incremented by one. Upon conclusion of Pass 1, the contents of the auxiliary table represent the frequency of occurrence of the corresponding numbers in the number table. Some locations will contain zero, indicating that the corresponding number does not occur in the number table. The remaining locations will contain values of one or higher, depending on whether the corresponding number occurs once or more frequently.

Pass 2—The location of each number in the final or results table is derived by scanning the auxiliary table. The number of entries in the number table—in this application, 100—is inserted into the 8080 accumulator (A) register. The contents of each auxiliary location are subtracted from the contents of the accumulator register, and the results of the subtraction are stored back into the original auxiliary location. This procedure continues until the contents of the accumulator are equal to zero. Upon completion of Pass 2, the auxiliary table will contain pointers to locations in the results table (Table 3). For purposes of illustration, there are only 11 entries with 13 possible values (0-12) in the Number Table of Table 3. In this application, the auxiliary table is scanned in descending order from the highest address to the lowest address. If the application had required arrangement of the numbers in ascending order, the direction of scan would have been from the lowest address to the highest address.

Pass 3—The values in the auxiliary table are used to construct the results table. Upon completion of this pass, the results table contains the link addresses arranged in a sequence determined by the number of calls (Table 4). The number table and the link address table are scanned in parallel. Values extracted from the number table are used to point to locations in the auxiliary table. Then, the contents of each auxiliary location are used to point to a location in the results table. Next, the contents of the location currently addressed in the link address table are inserted into the addressed location in the results table. Each time that a location in the auxiliary table is addressed, its contents are decremented by one. Upon completion of Pass 3, the link addresses are arranged in the results table according to the values of their corresponding numbers.

Number Sorting Program

The number sorting program[2] comprises four steps (see Program for Number Sorting Algorithm).

Step 1—Auxiliary table is cleared

Who are you calling Dumb?

Excuse us.

But, there's a dumb little matter we'd like to clear up.

The computer industry en masse has taken to using our name when referring to any less-than-smart terminal.

It's not that we mind being accepted as a standard in the industry. But, we're concerned over the resulting confusion.

Though other terminals may claim to be dumb-enough or just-as-dumb, there's only one Dumb Terminal®

DUMB TERMINAL. SMART BUY.

terminal. We make it. It's our trademark. Period.

Our name is important to us because it's such a good one. Through unrelenting quality control we build a dependable, easily adaptable terminal that sells like crazy in the fiercely competitive computer marketplace.

In 4 years, we've shipped over 50,000 units.

So next time you hear our name dropped, remember, many terminals are called dumb, but there's only one Dumb Terminal.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Lear Siegler, Inc./Data Products Division, 714 Brookhurst Street, Anaheim, CA 92803
(800) 854-3805. In California (714) 774-1010. TWX 910-591-1157; Telex 65-5444.

CIRCLE 47 ON INQUIRY CARD

Program For Number Sorting Algorithm

```
INITIALIZATION:
    MVI B, 40H      ;Preset Register B with number of operations (40₁₆).
    LXI D,0000      ;Load Register DE with 0000.
    LXI H,0000      ;Load Register HL with 0000; HL is cleared to allow addition of SP.
    DI              ;Disable all interrupts; since SP is used to clear auxiliary table, servicing of an interrupt would disrupt program.
    DAD SP          ;Add value of SP to previously cleared HL to save SP.
    LXI SP,ENAUX    ;Preset SP with: (final address of auxiliary table + 1); SP commences at a high address and counts down.[a]
RESET:
    PUSH D          ;Reset two locations addressed simultaneously by SP; advance SP by two addresses.
    DCR B           ;Decrement register B by 1.
    JNZ RESET       ;If B equals zero, operation is complete; otherwise, return to RESET.
    SPHL            ;Restore value of SP, saved in HL, to SP.
    EI              ;Re-enable all interrupts.
                    ;End of STEP 1.
    MVI B,64H       ;Preset B with number of table entries (64₁₆).
    LXI H, AUX      ;Load register HL with first address of auxiliary table.
    LXI D, TABLE    ;Load register DE with first address of number table.
SCAN 1:
    LDAX D          ;Load accumulator with contents of memory location addressed by register DE.
    MOV L,A         ;Move accumulator to register L; L now contains number from number table that acts as pointer to auxiliary table.
    INR M           ;Increment contents of location in auxiliary table addressed by HL; L equals number from number table.
    INX D           ;Increment register D; advance scan of number table.
    DCR B           ;Decrement register B by 1.
    JNZ SCAN        ;If B does not equal zero, Scan 1 is not finished; return to Scan 1.
                    ;End of STEP 2.
    LXI H, AUX      ;Load address of auxiliary table into register HL.
    MVI A, 64H      ;Preset A to 100₁₀ (number of locations in number table).
SCAN 2:
    SUB M           ;Subtract contents of auxiliary table location addressed by HL from accumulator.
    MOV M,A         ;Substitute contents of accumulator in location addressed by HL.
    INX H           ;Increment HL by 1.
    JNZ SCAN 2      ;If accumulator is not equal to zero, continue with SCAN 2.
                    ;End of STEP 3.
    LXI H, TABLE    ;Load HL with first address of number table.
    LXI B, LINK     ;Load BC with first address of link address table.
    LXI D, FINAL    ;Load DE with first address of results table.
SCAN 3:
    MOV A, L        ;Save value of L in accumulator.
    CPI FIN         ;Compare contents of accumulator with value of least significant byte of final address of number table to check if scan of number table is complete.
    JZ FINISH       ;If comparison indicates that scan of number table is complete, go to end of program.
    MOV L, M        ;Make HL equal to address in auxiliary table.
    MOV E, M        ;Load E with pointer to results table.
    MOV L,A         ;Restore value of L from accumulator.
    LDAX B          ;Load accumulator link address contained in locations addressed by BC.
    STAX D          ;Insert contents of accumulator (link address) in location in results table addressed by DE.
    INX H           ;Increment HL by 1; continue scan of number table.
    INX B           ;Increment BC by 1; continue scan of link address table.
    JMP SCAN 3      ;Resume SCAN 3.
FINISH:
    HLT             ;Halt program.
    END             ;End program.
```

Note: Number sorting program is organized in four steps. In Scan 2, accumulator is preset with number of entries in number table. Values in auxiliary table are successively subtracted from this number until contents of accumulator are equal to zero.

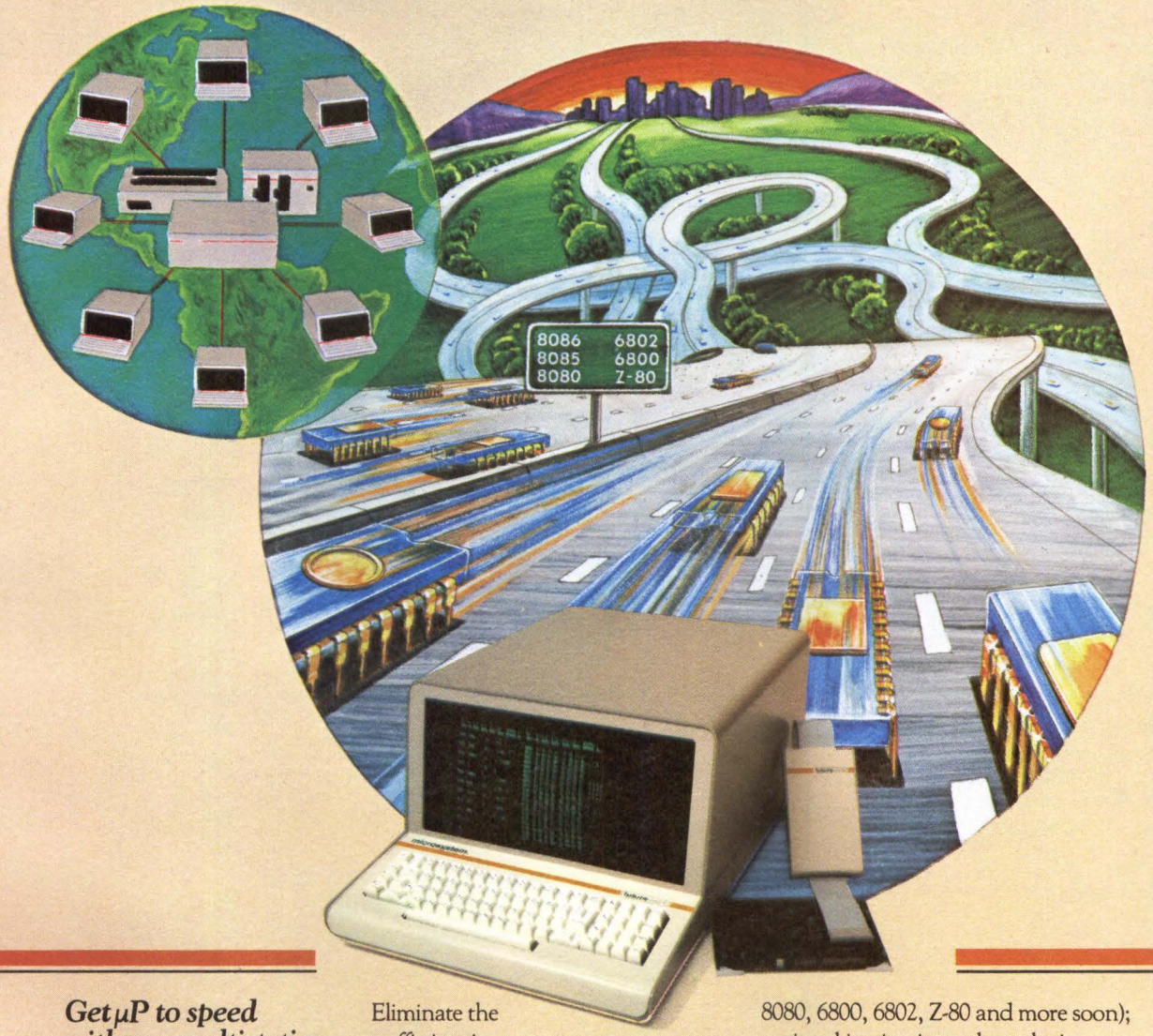
by stack pointer. As described above, this technique has the advantage of addressing two locations and automatically advancing the addressing by two, all within the framework of a single instruction. Prior to use, the current value of the stack pointer must be saved and all interrupts must be inhibited.

Step 2—Number table is scanned and auxiliary table is set up, as described in Pass 1.

Step 3—Auxiliary table is scanned, and pointers to results table are generated.

Step 4—Number table and link address table are both scanned simultaneously, and contents of

Going μP? Our 8-lane universal expressway to μP development is wide open.



Get μP to speed with our multistation development network.

Eliminate the traffic jam in your microprocessor development lab. Get off that one-way road to μP-based product design (with just one chipmaker's microprocessor support) and reduce your per-station cost at the same time. How? With our Universal Multistation Development Network — a distributed processing system that shares disk and printer with up to eight users simultaneously. Give each user his own AMDS station with integral CPU, CRT and keyboard; any one of six supported processors (8086, 8085, 8080, 6800, 6802, Z-80 and more soon); optional in-circuit emulator, logic analyzer and every software aid, including BASIC compilers, relocating macro-assemblers and disassembling symbolic debuggers. It's the first sensible alternative to the high cost of multi-user development support and confining single-chip systems. Futuredata, 11205 S. La Cienega Blvd., Los Angeles, CA 90045. (213) 641-7700 TWX: 910-328-7202.

futuredata

Futuredata Booth at Electro 1319-1321

CIRCLE 48 ON INQUIRY CARD

INTRODUCING THE PERKIN-ELMER 3220

The Highest Performance Mini.

Full 32-bit architecture. DMA bandwidth of 8MBytes. MOS memory in 256KB modules with error correction as standard. Memory error logging down to the chip level, if you want. Memory expansion to 4MBytes. Cache memory, 128 32-bit registers, number-crunching features no 16-bit mini can match. And, all for less than a PDP-11/60.

The Lowest Cost Supermini.

Outstanding run-time speed and accuracy. Fast, responsive program development. Easy, cost-effective program conversion. Check the comparison chart.

Either Way, We've Got Them Beat.

	DEC 11/34	DEC 11/60	P-E 3220	SEL 32/57	PRIME 550
Architecture	16-bit	16-bit	32-bit	32-bit	32-bit
DMA Bandwidth	2MB	6MB	8MB	26MB	2.5MB
Maximum Memory	256KB	256KB	4MB	1.87MB	2MB
Number of Registers	8	16	128	8	128
Direct Addressing	56KB	56KB	4MB	.5MB	32MB (virtual)
Writable Control Store	No	Yes (opt.)	Yes (opt.)	Yes (opt.)	No
Shared Memory Support	No	No	Yes (opt.)	Yes (opt.)	No
Pricing – Processor 256KB, PF/AR, Systems Console, Chassis and Cabinet	$29,700	$41,900	$33,500	$41,600	$70,000
256KB Expansion Memory	N/A	N/A	$10,000	$12,500	$15,000

	Optimizer Technology	Average Compile Time	Whetstone Benchmark	Matrix Inversion Program	Binary Search	Price *
3220 FORTRAN VII	Global	2000 LPM	2.25 Sec.†	3300 Sec.†	39 Sec.†	$ 88,600
VAX FORTRAN IV Plus	Block	1300 LPM	.85 Sec.	3700 Sec.	109 Sec.	$167,200

*Both 3220 and VAX configured with: 512KB, Floating Point, 10MB Disk, Dual Density Tape, OS, FORTRAN.
†Without cache memory option.

Dynamic 32-Bit Software, Perkin-Elmer Quality.

The software available for the Model 3220 is exactly what you'd expect from Perkin-Elmer, a company whose reputation was built on quality products. It's true 32-bit software, tuned and proven where it counts: in the field. And not just for months. For years.

Powerful software like our FORTRAN VII, it's targeted to ANSI FORTRAN-77 and IBM FORTRAN H compatibility to reduce conversion costs.

A flexible operating system for event-driven, real-time applications. Program development with up to 32 on-line, interactive terminals. The industry's most advanced transaction processing monitor, supporting commercial applications with up to 64 terminals, using COBOL and SORT/MERGE II.

Shareable software that allows our OS/32 MTM to make multi-terminal, multi-task program development a snap. And, increases memory efficiency as well.

From the Inventors of the 32-bit Supermini.

Five years ago we introduced the first 32-bit supermini, when we were known as Interdata. Now we are the Computer Systems Division of Perkin-Elmer, a Fortune 500 company respected for 40 years for the reliability and performance of its high-technology products. Today we have more than 2000 successful 32-bit installations worldwide.

The Model 3220 is our first product to be introduced and marketed entirely under the name Perkin-Elmer. The 3220 leads off our new Series 3200, with more to come. A compatible family, based on advanced systems and software, the Perkin-Elmer Series 3200 is the next generation of 32-bit superminis. Perkin-Elmer remains the undisputed leader in 32-bit performance and price.

Find out how we've got them beat any way you look at it.

Call or write for a demonstration today.

Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757. (800) 631-2154. Or, in New Jersey (201) 229-6800.

PERKIN-ELMER

auxiliary table point to locations in results table.

Memory Allocation

The auxiliary table requires 128 bytes of random-access memory (RAM), equal to the range of possible values (0-127). The number table requires 100 bytes of RAM, equal to the number of telephone extensions. The results table and the link address table also require 100 bytes of RAM each. Hence, the minimum RAM requirements of this program are 428 bytes. In the 8080, a data memory is addressed by 2-byte registers (HL, DE, BC). It is convenient, for purposes of speeding up the program, to allocate the addresses of the number table and the auxiliary table such that their most significant bytes are identical. Also, the least significant byte of the address of the auxiliary table is made equal to 0 to 127, while the least significant byte of the number table ranges from 128 to 227. No further constraints are necessary. The program requires 70 bytes of read-only memory (ROM). Time of program operation, assuming a clock cycle duration of 500 ns, is slightly less than 8.8 ms (worst case).

Summary

A number sorting algorithm using the 8080 microprocessor is applicable in cases where the number of entries to be sorted is on the same order of magnitude as the range of values. In the described application, the number of entries in the auxiliary table equals the possible range of number values. If the range of values significantly exceeds the number of entries, the auxiliary table will be disproportionately large and use of another algorithm is preferable.[3]

References

1. D. E. Knuth, *The Art of Computer Programming*, Vol 3, Addison-Wesley, 1973
2. Intel Corp, *8080 Assembly Language Programming Manual*, Publication No 98-004, 1976
3. D. E. Knuth, "Algorithms," *Scientific American*, April 1977

Think Ontel

It's Intelligent

Toren/Gaynor

Buying intelligent terminals?
Then you should be thinking about Ontel! It's the intelligent thing to do.

First of all, we know that extensive software is vital to our OEM users and new Ontel software is continually being introduced. Because of this our users are able to reduce their development costs in a multitude of application areas.

High level languages, forms generation, word processing, text editing and complete utilities and diagnostics, all running under Ontel's disk or diskette operating systems, complete the comprehensive set of sophisticated software packages now available for the OEM market.

Our hardware is truly outstanding. The OP-1 user programmable intelligent terminal series has been carefully planned and engineered as a complete systems family able to fulfill and complement your design specifications. All OP-1 terminals have been designed to make possible on-site feature enhancements. A full range of peripheral controllers is available providing communications, mass storage and printer interfaces. Master processors, coupled with secondary processors, provide unique distributed computing capabilities.

Contact us today for the intelligent answer.

Edward J. Heinze
Vice President Domestic Sales

Ontel Corporation
250 Crossways Park Drive
Woodbury, NY 11797
(516) 364-2121

CIRCLE 51 ON INQUIRY CARD

NOW

Savings.

We've priced these memories to be the best values ever, consistent with full spec. memory elements and our rigid quality assurance programs. Listed prices are single quantity, U.S. only. Substantial OEM discounts available.

48 hour delivery

We'll ship all single quantity orders within 24 hours of receiving your written purchase order. And we'll ship airfreight. With many models, OEM quantity orders (25 or more) can be filled just as fast. Check with us for details.

FOB you.

We'll pay the airfreight on any of these memories, anywhere in the U.S.

But hurry!

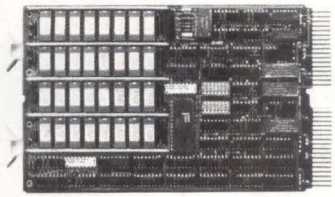
These offers apply only to the specific models shown and may be withdrawn without notice.

Satisfaction.

Field proven reliability and our **full year** warranty on parts and labor will keep you satisfied.

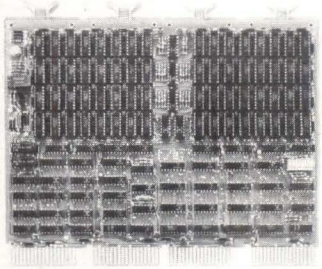
LSI-11

For high density LSI-11 memory expansion the dual height MSC 4601 gives you 32K to 64K bytes, with on-board distributed refresh, in a single option slot. Provision for battery backup. Addressable in 2K byte increments. Only $935 for the 64K byte version.



MSC 4601

The MSC 4501 gives you up to 32K bytes in 8K increments in a single quad slot. Distributed or burst refresh modes are on-board switch selectable. $450 for 32K bytes is our best price ever.

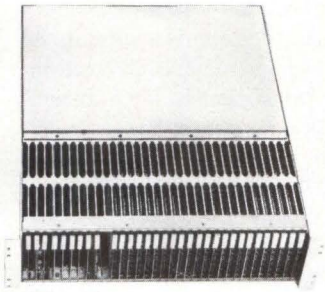


MSC 4501

IS THE BEST TIME TO BUY OUR LSI-11, PDP®-11 & PDP-8 MEMORIES. HERE'S WHY:

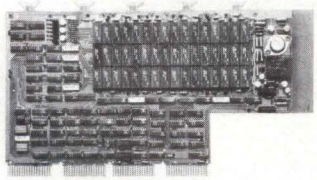
PDP-11

For expanding PDP-11/04 to 55 memory, the MSC 3302, with built in power supply, provides 32K to 248K bytes, with or without parity. Can operate with two CPU's, either singly or simultaneously. $7,370 for 248K bytes with parity.



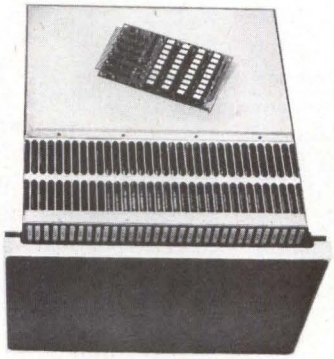
MSC 3302

The MSC 3303 fits 24K bytes into any, single DD-11 small peripheral slot. Works with PDP-11/04 to 55. A special version provides clearance for use with PDP-11/15's and 20's. Lower power and low price of $995.



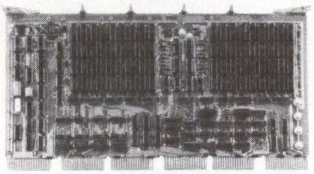
MSC 3303

Our "intelligent memory" for PDP-11/70's has up to 4MB in 64KB increments, with ECC. Nonvolatile with battery backup. Built in microcomputer monitors and locates single bit and parity errors. At $35,210 for 2MB it's cost per byte is less than $0.018.



MSC 3602

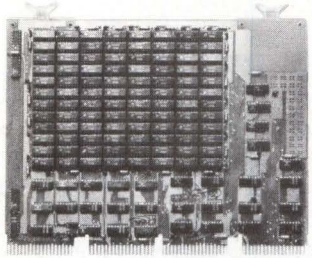
PDP-11/04/34 users can have 32K to 128K bytes, with or without parity, in a single, modified SPC slot. Provision for battery backup. On-board DIP switch assigns address start position on bus. $1,945 for 128K bytes with parity.



MSC 3603

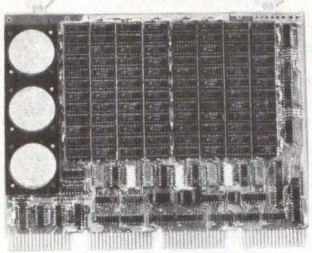
PDP-8/A, E, F, or M

Get 8K words in a single OMNIBUS® slot for only $553. And our special price of $2,146 for four MSC 3102's gives many PDP-8 users full memory capacity.



MSC 3102

If you need a nonvolatile, low power memory, the MSC 3201 gives you 8K words with on-board batteries for $761. Our four board price is just $2,972. Has 30 day data retention and requires only 3.3 watts per board.



MSC 3201

Call us now. 800-525-7498

is our toll free sales hot line. In Colorado call 303-770-7400 collect.

DEC compatible memories... from the first.

Monolithic Systems corp

14 Inverness Drive East
Englewood, CO 80112
303/770-7400

CIRCLE 52 ON INQUIRY CARD

TECH BRIEF

Individual Control of Relays in a Matrix

IC control logic approach for individual relays in a crossbar matrix

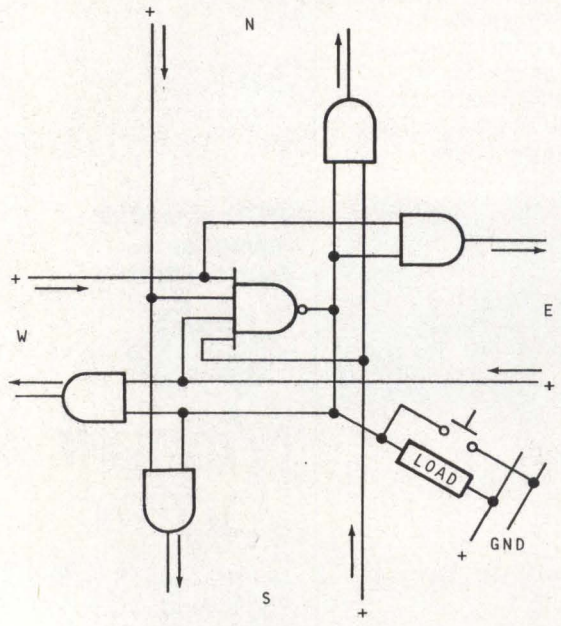
A suggested control logic approach for a crossbar matrix of relays controls individual relays and displays their status. Identical modular control units are used for each intersection of the matrix; their design is independent of the size or form of the relays. The system is expandable, employs general purpose multiple pole relays, and could be equipped with program control. Readily available ICs are used, along with spst pushbutton switches for programming. Status indicators are LEDs, and reed relays are employed for isolation.

Programming and display with a light-indicating pushbutton at each X-Y matrix intersection are provided by the same panel. As the system is designed, only one button in a given column and one in a given row can be on at a particular time. A separate reset button for each row and each column clears the entire row or column. In addition, a common reset button clears the entire board; a single key switch could be used to disable all pushbuttons once the board is programmed.

Because logical control of the coil current through relay contacts can result in an oscillating system, the control system is segregated from the relay contacts. It is also isolated from the coils through an intermediate relay, to allow the coils to operate at a different voltage and from a less filtered and regulated supply. The status indicators are controlled by a relay contact (in a dual-purpose configuration).

The control logic (see Figure) is inspired by functionally similar relay coil and contact designs in which positive and negative coil voltages are fed to the intersection from opposite directions over the contacts of neighboring relays. If a latch circuit at a matrix intersection is set, all identical latches to the N, S, E, and W shall be released (N, S, E, and W representing four arbitrary directions on the control board). This arrangement requires four each of outbound and inbound control lines on each circuit. These lines originate at each matrix-edge circuit.

The illustrated control circuit is shown as one matrix-intersection unit; when a particular latch is set, it will provide release lines to all others with the same X or same Y coordinate. The feed-through control lines will enable the latch just set to remain set. This allows the latch to be implemented simply by a single 4-input gate at the intersection. If more than one of the latches are set momentarily, they will all be released sequentially and will provide hold signals to the last latch set.

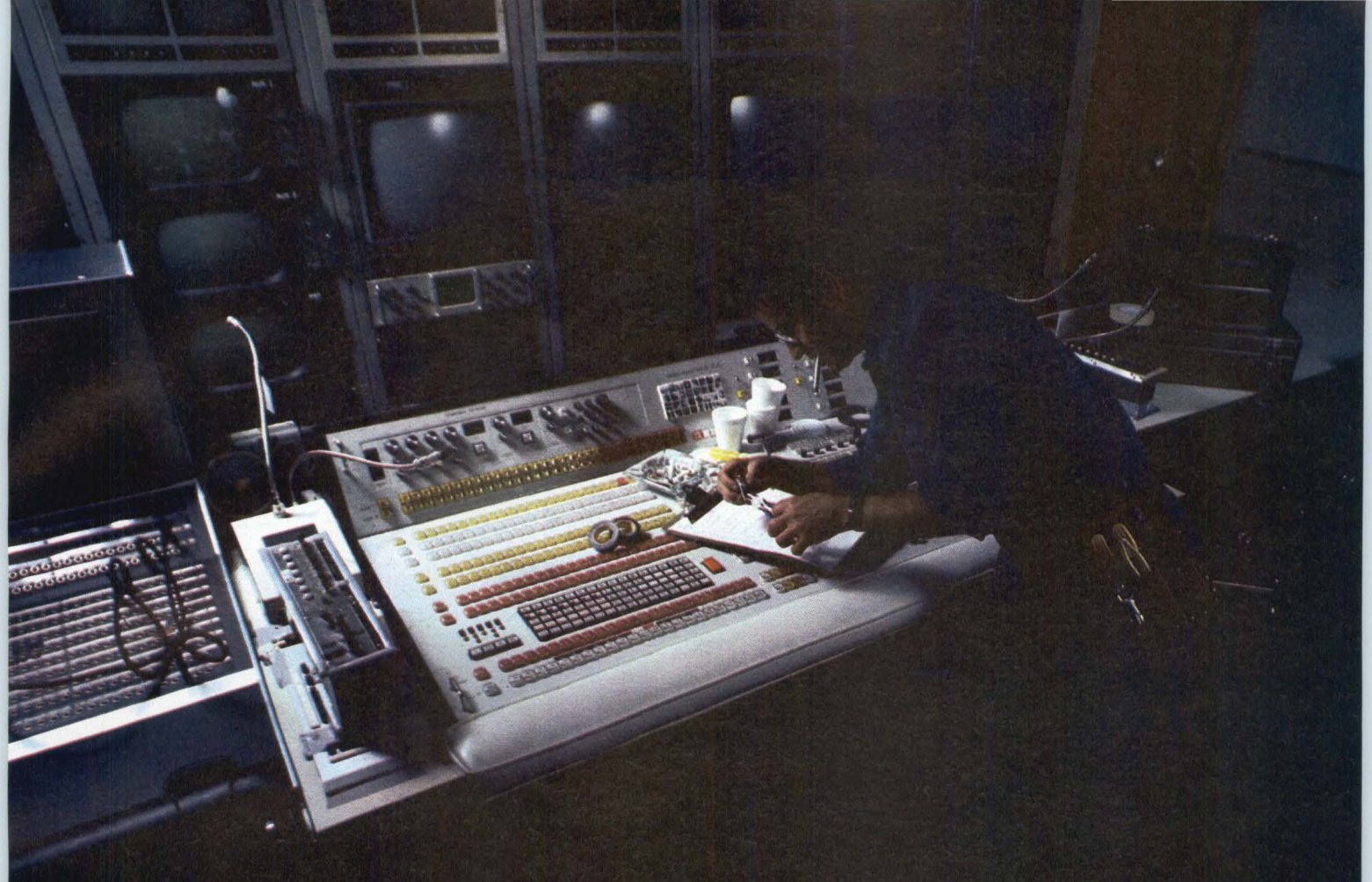


In control circuit of matrix-intersection configuration, output of latching 4-input open-collector NAND gate is connected to isolating reed relay and intersection pushbutton. In matrix assembly, edge and corner circuits will require fewer gates, since they originate control lines. Collective row or column reset buttons operate on respective control line originating points, and control board disable switch operates on line connecting ground side of all intersection pushbuttons

Note

This work was done by Tage O. Anderson of Caltech/JPL. For further information, write to: John C. Drane, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. (NPO-14095).

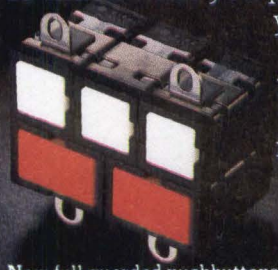
This document was prepared under the sponsorship of the National Aeronautics and Space Administration. Neither the United States Government nor any person acting on behalf of the United States Government assumes any liability resulting from the use of the information contained in this document, or warrants that such use will be free from privately owned rights.



You may not know how expensive a pushbutton really is until months after it's paid for.

The true measure of a pushbutton's cost isn't so much what you pay. It's how many times you pay it.

If you spend less in the first place, you could end up with a higher price tag from what you spend over and over in repair costs and downtime.



New full-guarded pushbuttons.

That's why it's worth it to specify the MICRO SWITCH Advanced Manual Line (AML) of pushbuttons, rockers, paddles and indicators. It's the most complete line of manual controls ever offered, designed to save you money from start to finish.

AML is easy to wire, thanks to single-level termination, simple snap-in PC board mounting and sub-panel mounting that uses individual, strip or matrix hardware (see inset). The result is low installed cost.

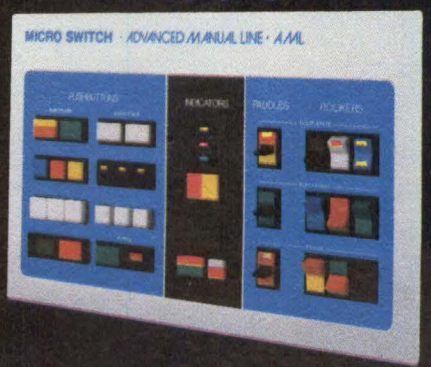
And of course, you get traditional MICRO SWITCH reliability and long life. Which means money savings over the long haul.

No matter how many words you use to describe the broad AML lineup, it all comes down to just two: cost effectiveness. For a panel that's pleasing to the eye as well as the budget.

If you'd like a personal demonstration just call 815/235-6600.

MICRO SWITCH is also ready to provide you with field engineers for application assistance and a network of authorized distributors for local availability.

AML. It's the closest a line of pushbuttons can come to paying for itself.



MICRO SWITCH

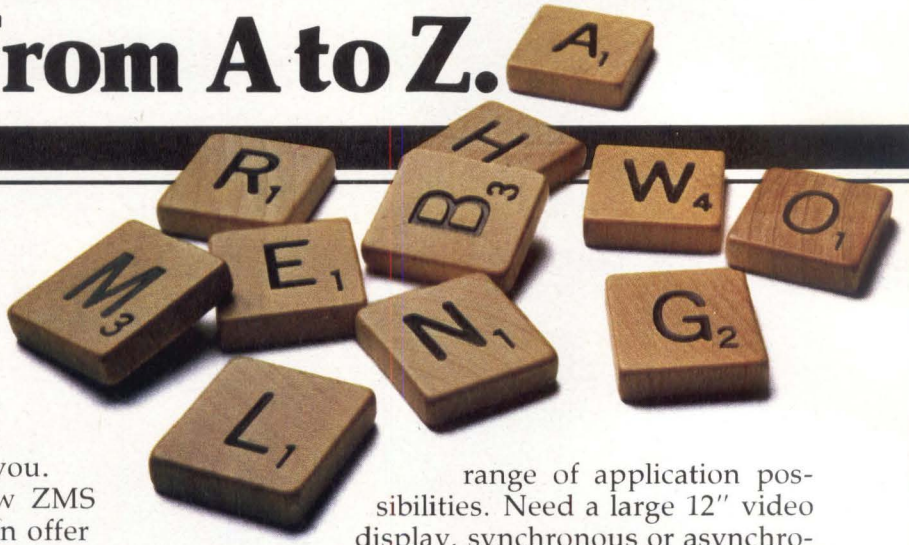
FREEPORT ILLINOIS 61032

A DIVISION OF HONEYWELL

See us at the ELECTRO Show, Booth 2808-2812.

CIRCLE 53 FOR DATA

If you're in the market for intelligent terminals, you could waste a lot of time wandering from A to Z.



Specifying the optimum terminal for your data or word processing system used to be a real problem. Should it be dumb? Smart? Or intelligent? Clustered or stand alone? And which of the 88 plus terminal manufacturers can best fulfill your system requirements?

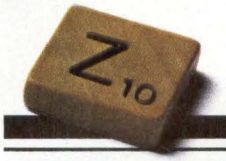
We've just solved the problem for you.

With the introduction of our new ZMS family of intelligent terminals, we can offer you three intelligent solutions: the ZMS-50, ZMS-70 and ZMS-90. They're all 8080A microprocessor-based. All user programmable. And their fundamental microcomputer bus architecture and modular design offer you considerable system flexibility.

The I.Q. test: how much native intelligence do you need?

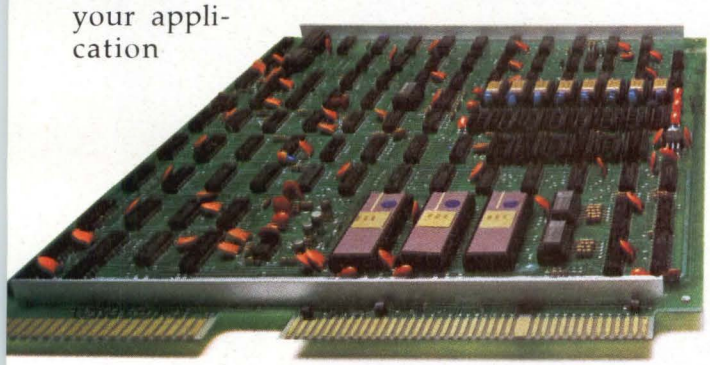
Zentec ZMS intelligent terminals are designed as building blocks, each one offering you a wide range of application possibilities. Need a large 12" video display, synchronous or asynchronous interface and up to 12KB of downloading capability... all at a "smart" price? The ZMS-50's your answer. Want powerful text editing capability, 143,000 bytes of on-line mass storage and a sophisticated set of preprogrammed software routines? Specify the ZMS-70. Or if you need a large video display, detachable keyboard, synchronous interface and 16K bytes of RAM that's expandable to 64K bytes, consider the ZMS-90. Whichever one you start with, its fundamental microcomputer bus architecture, list driven structure and choice of software and firmware modules offer you an almost endless array of system possibilities.

Or you could start with Zentec ...the last word in intelligent terminals.



Flexible & functional, by design

All Zentec ZMS terminals are user programmable and include easily modified software, making them simple to use, simple to re-program. Sophisticated, pre-programmed software routines can also be built-in, easily. And list driven architecture provides superior video flexibility, enabling you to change video fonts, select video enhancements and format data to suit your application



requirements. So you can blink. Blank. Reverse video. Underscore. Double character width. Even re-structure characters called up from the standard 128 character set. And Zentec's unique video circuitry enables you to display non-contiguous data, contiguously. There's even a 25th line added to the standard 24 × 80 character line format, reserved for the operator messages and status information, enabling the operator to bypass the video display to communicate with a host computer.

Have it your way

Equally important ... at Zentec, our philosophy is to be as flexible as our products. So we don't just stop with our standard configurations. Our

application engineers will help you analyze your data or word processing system. Help you select the right combination of hardware, firmware and software. And, where practical, even suggest custom configurations like special keyboards, enclosure modifications, customized firmware and specialized interfaces and protocols. The only thing we won't change is our commitment to quality. From materials to manufacture to MTBF tests, each Zentec intelligent terminal is designed and produced to meet a prescribed set of rigid performance standards.

Addressing the problem

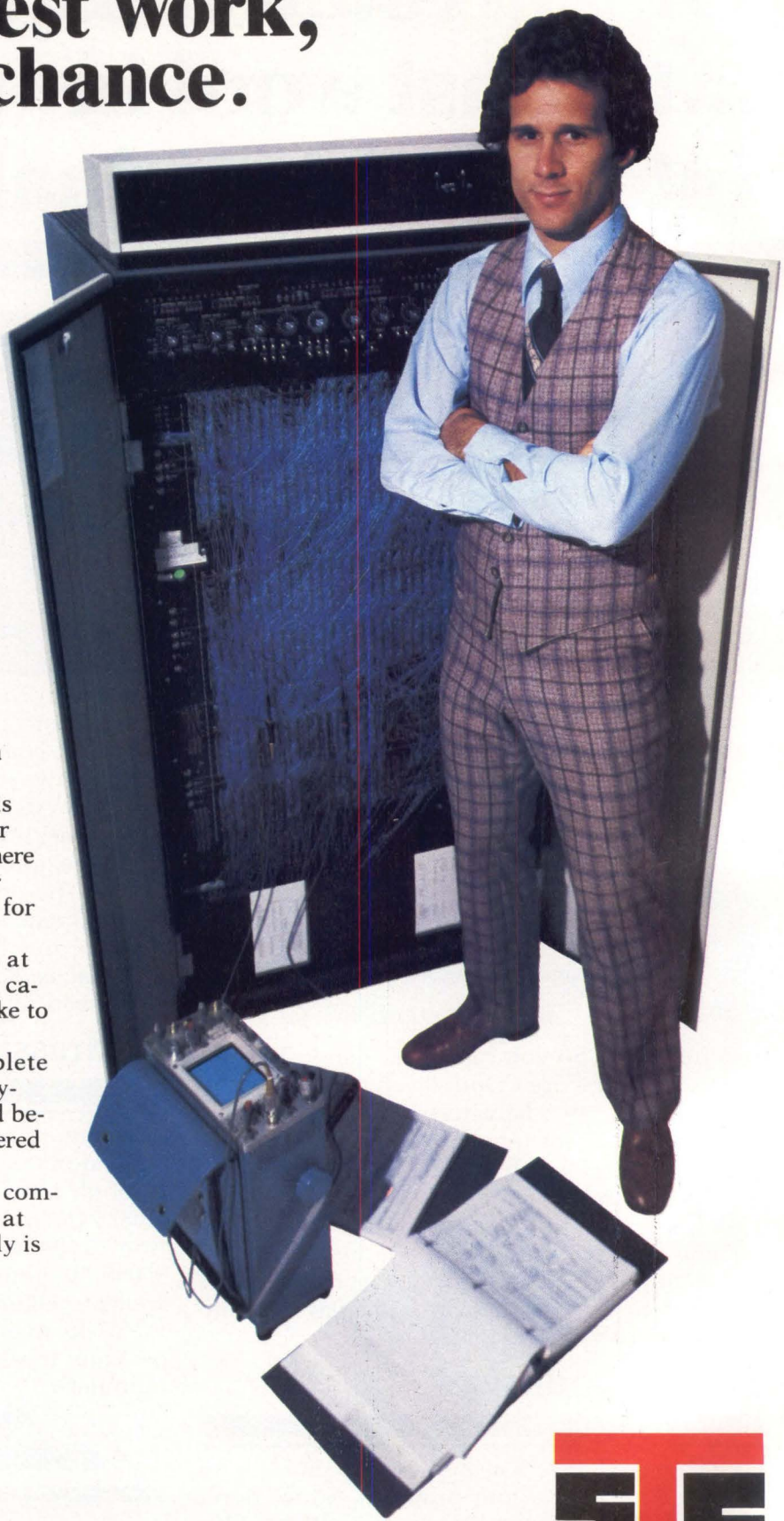
So if you're in the market for intelligent terminals, don't spend your valuable time sorting through a myriad of manufacturers. Call us at (408) 246-7662. Or write to us: Zentec Corporation, 2400 Walsh Avenue, Santa Clara, CA 95050. If you need even more immediate response, call one of our sales offices listed below. We'd like to tell you more about how Zentec can be your most intelligent choice for intelligent terminals.

ZENTEC

... the last word in intelligent terminals.

Sales Offices—Santa Clara, California: Santa Clara, CA (408) 246-7662; Los Angeles, CA, (714) 661-2583; Palatine, IL, (312) 991-0105; White Plains, NY, (914) 428-2801, Boston, MA, (617) 935-4511; Washington, DC, (703) 941-9270; Austria: Tonko, 425-451; England: Zygal Dynamics, 02405-75681; Finland: Videodata, 90-578-877; France: Tekelec, (1) 027-7535; Switzerland: Atek. 041-831043: Australia: Pacific Communications Pty. Ltd., (02) 638-6400.

If you've never had a chance to do your best work, here's your chance.



At Storage Technology Corporation, we continually strive to make our already advanced technology even better. We've built a solid reputation for quality with reliable, well-engineered products.

STC is only ten years old and we are already the world's largest manufacturer of high density tape data storage products and the leading independent supplier of fixed media disks for the IBM compatible market. And we can be very proud of that accomplishment.

Our people have made us what we are today and they are working hard to make us even better tomorrow. We recognize them and appreciate the creative, aggressive contributions made by each of our employees. That's the STC philosophy. And that's one reason we've been able to establish such a rapid, stable growth pattern.

Living in the Denver-Boulder area is just the beginning of an exciting career at STC. We offer challenging projects where you can be in control, where doing your best work means greater opportunity for advancement.

We offer exceptional opportunities at every level and we have some exciting career alternatives that we think you'd like to know about.

Write or send your resume in complete confidence to the Professional Employment Department at the address listed below. Your correspondence will be answered promptly and courteously, and we'll tell you what it's like to be part of our company, and why we can say with pride at STC, people count and technology truly is our middle name.

An equal opportunity employer.

STC

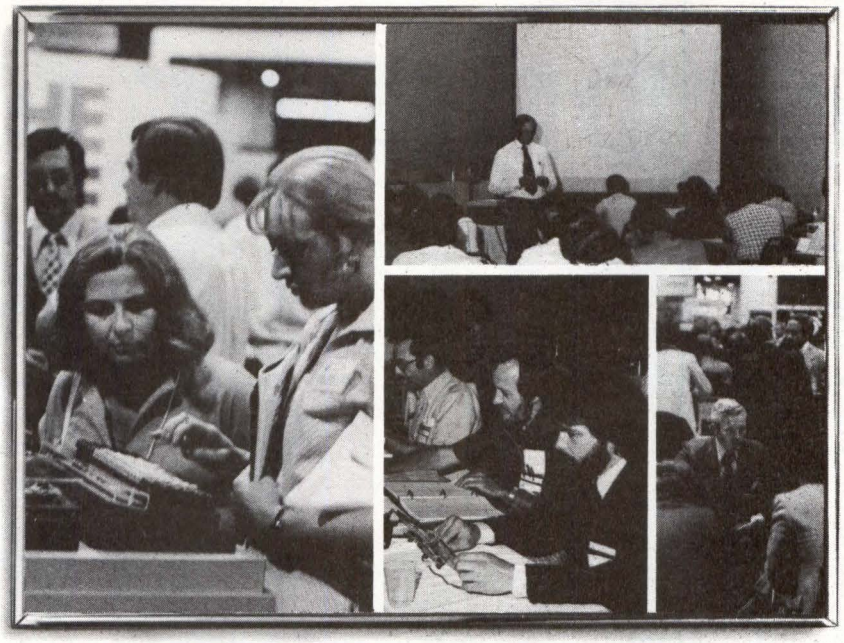
STORAGE TECHNOLOGY CORPORATION

R379

2270 South 88th Street, CD/4-79, Louisville, Colorado 80027

CIRCLE 135 ON INQUIRY CARD

JOIN THE CLASS OF '79
National Computer Conference June 4-7



A unique and extraordinary learning experience will be available to you at the 1979 National Computer Conference, June 4-7 in New York City. The combination of more than 150 technical and professional sessions, a record-breaking exhibit of 1,700 booths, 16 Professional Development Seminars, a comprehensive Personal Computing Festival, plus a wide range of special events will make NCC '79 an exceptional educational offering.

For $60 you can register in advance for the technical and professional program, conference exhibits, and the Personal Computing Festival — a $15 savings on full-conference registration on-site. And you can add to this value by taking advantage of the one-day Professional Development Seminars, each available at $50 including complete course material.

The conference program will meet the needs of commercial and industrial users through sessions on management, marketing, applications, and the impact of computers on society. Special "mini-conferences" will cover such areas as use of computers for financial transactions, in law and public policy, in health care, as well as privacy and security.

Emphasis at the Professional Development Seminars will be on data-base/data communications, mini/micro technology, the automated office, and structured methodologies. Specific topics range from database machines, implementing a word processing system, and structured systems design to computer systems performance, human engineering in teleprocessing systems, and an introduction to microprocessors.

And there's more. At the NCC '79 Personal Computing Festival you'll learn about the latest developments in microcomputer systems and services for personal or business use. The Festival will feature more than 25 sessions, noncommercial applications demonstrations, and commercial exhibits by more than 100 participating organizations.

Join the NCC class of '79. To pre-register for the full-conference program and exhibits...or to obtain additional information on NCC '79, including complete details on other registration categories and housing...use the coupon below. Whichever registration category you select, or whether you attend as a guest of a participating exhibitor, your badge will be mailed to you well in advance of the conference. Deadline for advance registration is May 15.

CD

REGISTER NOW: To be part of the picture at NCC '79, return this coupon today.
Send to: NCC '79, c/o American Federation of Information Processing Societies, Inc., 210 Summit Ave., Montvale, N.J. 07645.
Or telephone: 201/391-9810.

NCC '79
THE COMPLETE COMPUTING EXPERIENCE

- ☐ I wish to preregister for the full conference and have enclosed $60.
- ☐ Please send me additional information on NCC '79, including housing and registration.
- ☐ Please send me information on the Professional Development Seminars.
- ☐ Please send me information on the NCC '79 Travel Service.

Name _____

Title _____

Company _____

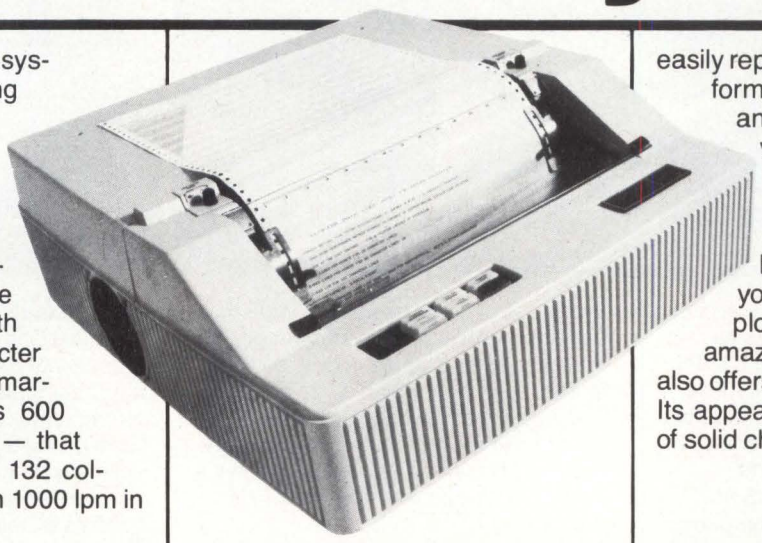
Street _____

City _____ State _____ Zip _____

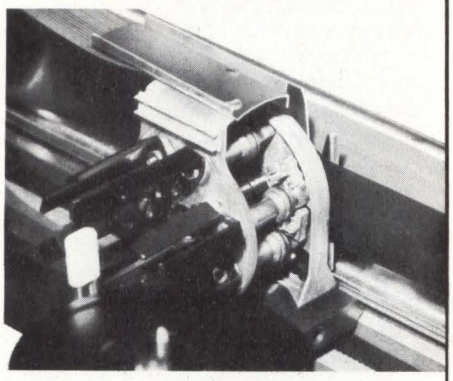
Florida Data has the printer for the next 5 years

Are you worried about system throughput growing faster than your printer capability? Then talk to Florida Data Corporation about the printer for the next five years!

FDC's Model PB-600A can keep the pace with total system growth — it is the fastest character matrix printer on the market. Its print speed is 600 characters per second — that means 230 lpm at full 132 column width or more than 1000 lpm in shorter lines.



Model PB-600A is the fastest character matrix printer on the market.



Print-heads for FDC printers are manufactured in-house with proprietary technology.

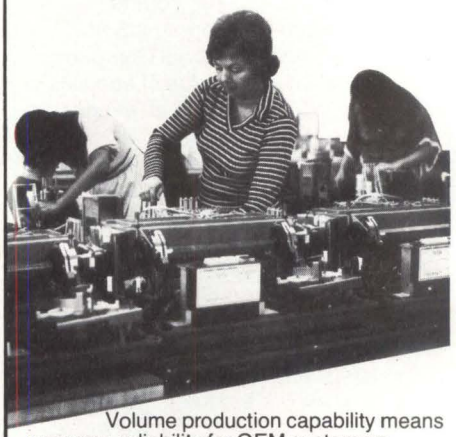
The secret of the PB-600A's outstanding performance is the proprietary print-head technology developed by FDC. We manufacture our own print heads. Print head life exceeds *any* other character matrix printer; FDC heads are warranted for one full year.

Our head technology was a long time coming — the engineers who developed it brought a total of more than 200 years' combined experience to the task. But it was worth waiting for. Now you can enjoy line printer output at serial printer prices, with the added benefits of exceptional reliability and outstanding customer support.

The PB-600A has all the other features you'd expect in a high-quality printer designed especially for OEM customers.

There are *no* duty cycle or page density restrictions on the print head; this means continuous printing, hour after hour. Standard PB-600A features include microprocessor controller, forward/reverse printing, an 894-character buffer, internal test capability and switch selection of four different type fonts. A two-channel paper tape reader provides vertical forms control. Paper tractors may be easily repositioned to accommodate forms from 3" to 14⅞" in width, and a long-life ribbon provides 20 million characters before replacement.

Florida Data also offers the Model BNY, a new binary printer that brings you computer graphics and plotting capability at an amazingly low price. This printer also offers a two-pass character font. Its appearance is very close to that of solid character printing.



Volume production capability means economy, reliability for OEM customers.

Enjoy the economy and reliability that come from high-volume output. Enjoy the OEM customer support that comes from a dedicated, experienced technical staff.

Get the details from:
Florida Data Corporation,
3308 New Haven Avenue,
West Melbourne, FL.
Telephone 305/724-6088.

Distributor inquiries invited.

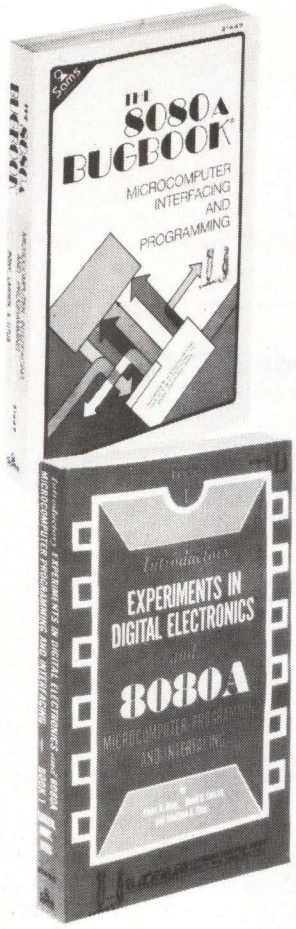
FDC

When it comes to computers, SAMS PUBLISHES THE BOOKS

Introducing... THE BLACKSBURG CONTINUING EDUCATION SERIES™

It has long been the objective of the "Blacksburg Group" to develop timely and effective educational materials and aids that will permit students, engineers, scientists and others to quickly learn how to apply new technologies to their particular needs. The members of the group have long been involved in digital electronics, minicomputers, and microcomputers.

The Blacksburg Continuing Education Series™ is an easy to read format consisting of 16 titles. Subjects range from basic electronics through microcomputers, operational amplifiers and active filters. Each title in the series includes detailed experiments, "hands-on" learning experiences, and examples to reinforce basic concepts. Book Size 5½" x 8½", softbound.



The 8080A Bugbook®: Microcomputer Interfacing and Programming
by Peter R. Rony, David G. Larsen, and Jonathan A. Titus.

Provides a thorough description of 8080A-based microcomputer systems, including the hardware required for a typical 8080A microcomputer, the operation of the status latch, and the interface circuitry required for external input, output, and interrupting digital devices. Over 150 pages are devoted to a detailed description of the 8080A instruction set. More than 30 programming examples, which cover topics such as timing loops, stack operations, clearing memory, input and output, and interrupt servicing, are provided. 416 pages. BUGBOOK® is a registered trademark of E & L Instruments, Inc., Derby, Connecticut 06418.
No. 21447 $10.50

Introductory Experiments in Digital Electronics and 8080A Microcomputer Programming and Interfacing. Book 1.
by Peter R. Rony, David G. Larsen, and Jonathan A. Titus.

A novel introductory approach to the field of digital electronics that starts with the programming of an 8080A-based microcomputer and then proceeds to a treatment of the key concepts required to interface a microcomputer to external digital devices. Gates, flip-flops, latches, decoders, counters, monostable multivibrators, and gating are all described in detail as a prelude to the microcomputer interfacing experiments provided in Book 2. Seventeen programming experiments and forty-four digital electronics experiments are provided. 496 pages.
No. 21550 $12.95

Introductory Experiments in Digital Electronics and 8080A Microcomputer Programming and Interfacing. Book 2.
by David G. Larsen, Peter R. Rony, and Jonathan A. Titus

Book 1 provides the background necessary for this laboratory-based approach to the important principles of microcomputer interfacing: device select and address select pulse generation, accumulator I/O, memory-mapped I/O, and interrupting device servicing. The principles are discussed in the context of a small laboratory 8080A-based microcomputer, which is described in the Appendix. The entire 8080A instruction set is described in detail. Three programming experiments and forty-one interfacing experiments are provided. 416 pages.
No. 21551 $10.95

PLUS . . . there's 13 more timely computer titles. Order Today! See the complete selection on the order form below.

Howard W. Sams & Co., Inc.
4300 West 62nd Street
P.O. Box 558
Indianapolis, Indiana 46206

ORDER FORM

Quantity Ordered

_____ DBUG: An 8080 Interpretive Debugger No. 21536 $4.95
_____ Design of Active Filters, with Experiments No. 21539 $7.95
_____ Design of Op-Amp Circuits, with Experiments No. 21537 $7.95
_____ Design of Phase-Locked Loop Circuits, with Experiments No. 21545 $8.95
_____ Interfacing and Scientific Data Communications Experiments No. 21546 (March 1979 Publication Date) $5.95 (Tentative)
Introductory Experiments in Digital Electronics and 8080A Microcomputer Programming and Interfacing
_____ Book 1 No. 21550 $12.95
_____ Book 2 No. 21551 $10.95
_____ Two Volumes No. 21552 $20.95
Logic and Memory Experiments Using TTL Integrated Circuits
_____ Book 1 No. 21542 $9.95
_____ Book 2 No. 21543 (January 1979 Publication Date) $9.95
_____ Two Volumes No. 21544 $17.95
_____ Microcomputer—Analog Converter Software and Hardware Interfacing No. 21540 $9.50
_____ 8080/8085 Software Design No. 21541 $9.50
_____ NCR Basic Electronics Course, with Experiments No. 21549 $9.50
_____ NCR Data Communications Concepts No. 21548 $6.95
_____ NCR Data Processing Concepts Course No. 21547 $7.95

Quantity Ordered

_____ 555 Timer Applications Sourcebook, with Experiments No. 21538 $5.95
_____ The 8080A Bugbook® Microcomputer Interfacing and Programming Bugbook® is a registered trademark of E & L Instruments, Inc., Derby, Connecticut 06418. No. 21447 $10.50

_____ Sub Total
_____ Add local sales tax where applicable.
_____ Total Amount

Name_____

Address_____

City_____ State_____ Zip_____
(please print)

Save handling charges by enclosing payment with order.
☐ Payment Enclosed (No Shipping and Handling Charge)
☐ Bill Me (Shipping and Handling Charge will be added)
☐ Send me Free Sams Book Catalog

Prices subject to change without notice. 419

Return To:
Attention: Sales Department
Howard W. Sams & Co., Inc.
4300 West 62nd Street • P.O. Box 558 • Indianapolis, IN 46206

CIRCLE 55 ON INQUIRY CARD

INTERFACING FUNDAMENTALS: MULTIPLEXED LED DISPLAYS—PART 1

Christopher A. Titus and Jonathan A. Titus
Tychon, Inc

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

Regardless of their application most microcomputers require peripheral input/output devices. More common output devices include 7-segment displays, 5 x 7 dot matrix displays, teletypewriters, and cathode-ray tube displays. Various methods can be used to interface 7-segment displays to microcomputers, and several different programs typically drive such displays.

One of the simplest interface methods consists of latching the appropriate data values from the data bus under software control (Fig 1). The latch's inputs (7475) are wired to the microcomputer's bidirectional data bus and the latch's outputs are wired to a 7-segment decoder/driver (7447). The decoder's outputs (current sinking) are wired to the 7-segment display with 220-Ω current-limiting resistors. When an OUT 125 instruction is executed, the content of the 8080 microprocessor's A register is latched by the display interface; the two binary coded decimal (BCD) numbers represented by D7 to D4 and D3 to D0 are illuminated on the two displays. The instructions listed in Fig 1 cause a 39 to be displayed.

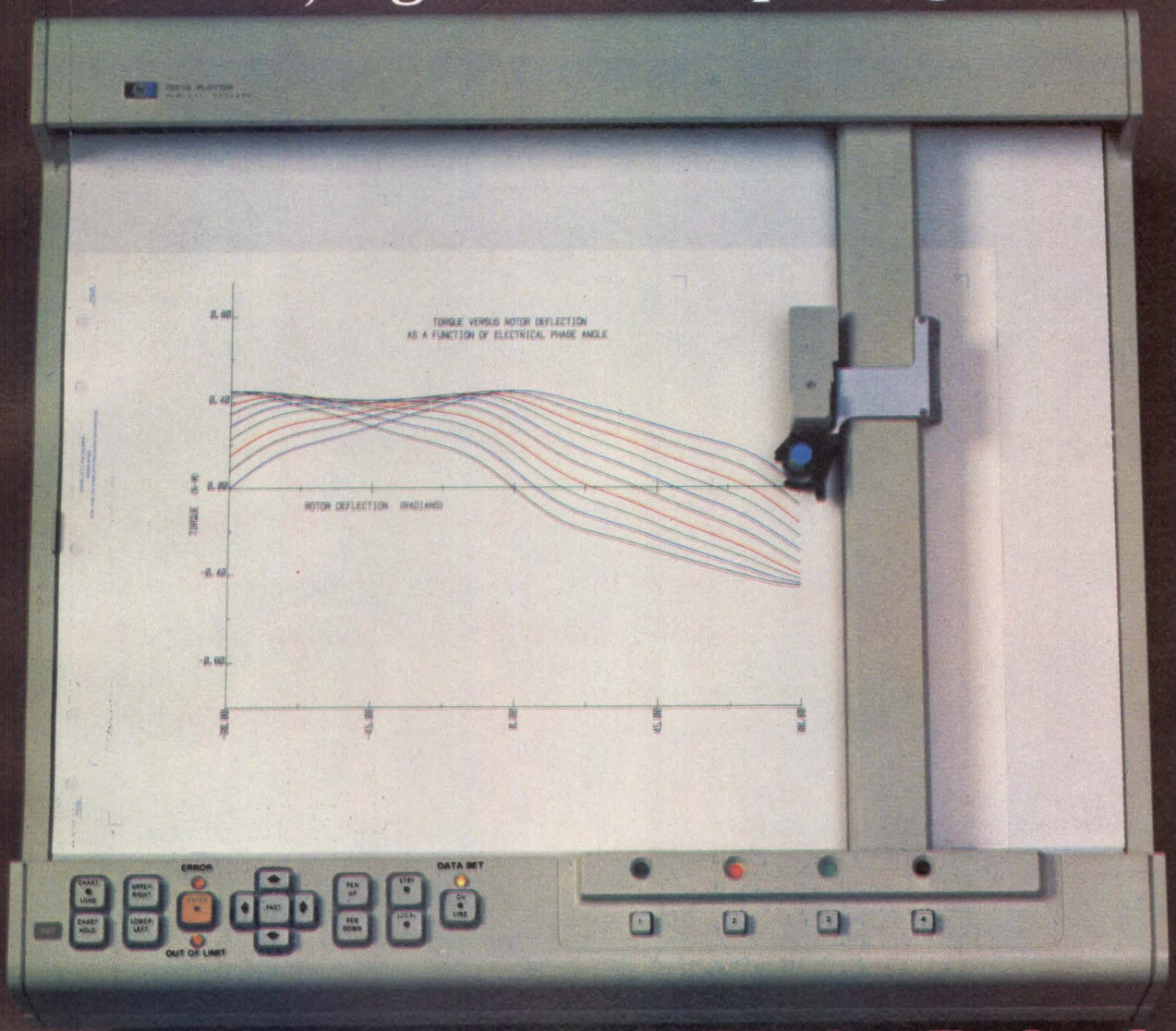
To display a 10-digit number using this method, 10 latches, 10 decoder/drivers, 70 resistors, and 10 7-segment displays are required. One method of reducing the parts count for this interface would be to use a device such as the 8255 programmable peripheral interface (PPI) integrated circuit (IC).* This device can be used as three independent 8-bit output ports, so that it is equivalent to six 7475 latches. Therefore, two 8255 PPI chips would replace the 10 latches in the above interface. One obvious disadvantage of this method is the large number of ICs required. However, one advantage is that relatively simple software drives this interface. Also, due to the latches or 8255 chips, the microcomputer only has to output numeric information once to the interface for it to be continuously displayed, and then can go on to perform any other required operations.

Another interfacing method is digit multiplexing, which reduces the display interface electronics (number of parts) to a minimum, but at the expense of longer and more complex display driver software. Multiplexing a display consists of enabling or turning on one particular digit with a digit enable code and providing the BCD numeric information for that digit to a multidigit display interface. In this way, each digit is turned on, one at a time, as the actual BCD data for each digit is provided.

Multiplexing is usually used only with multidigit displays. As an example, to display the number 237 on a 3-digit multiplexed display, the BCD value for the digit seven would be output to the interface, along with the digit enable code for the righthand display. After a short period (1 to 10 ms), the BCD value for the three would be output, along with the digit enable

*J. A. Titus, *et al* "Microcomputer Interfacing: Accumulator I/O Versus Memory I/O," *Computer Design*, June 1976, pp 114, 116

Fast, high resolution plotting.



Brought to you in color by Hewlett-Packard.

Hewlett-Packard's remarkable four color graphics plotter, Model 7221A, quickly generates professional, hard copy graphics from your design and computational data. A sophisticated microprocessor utilizes 41 easy-to-use commands for programmable selection of pen color, pen speed, character style, arc and circle generation, and an almost unlimited variety of user-defined line styles.

Programmable color comes from four long-life pens that remain stowed away until needed. Under program command, the plotter picks the color you select, draws, and puts the pen back—with the cap on!

With the standard RS232C/CCITT V.24 interface*, the plotter easily connects to most minicomputers, ASCII terminals and timeshare systems, directly or remotely through data communication modems. An internal data buffer stores plotter commands and data until needed, saving both computer and communication time. And your most frequently used shapes and symbols can be stored in the buffer as macro-instructions for execution with one simple command.

Call your Hewlett-Packard sales office today for complete details on our remarkable four color graphics plotter. Priced at only $4600 (U.S. domestic price only), it gives you everything you'd expect from a Hewlett-Packard Plotter. In color.

**Model 9872 has an HP-IB (IEEE 488-1975) interface.* 11804

HEWLETT hp PACKARD

1507 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE 56 ON INQUIRY CARD

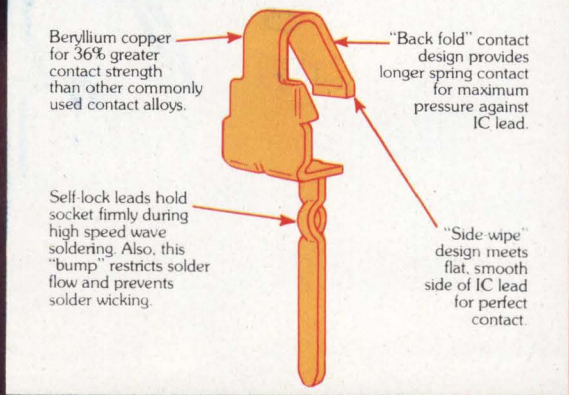
TEST DATA

UNIQUE R-N SINGLE CONTACT DESIGN PROVES SUPERIOR

They deliver 4 times greater holding force on your IC leads.

In a tough, 50-G shock test of 25 ICL sockets—not a single IC package came loose from the socket! More convincing proof that vibration problems are ended with R-N's new low profile ICL sockets. Socket density in multi-layer board can now be increased **without** sacrificing reliability.

...and this FULL LINE of low-profile R-N ICL sockets is priced very, very competitively.

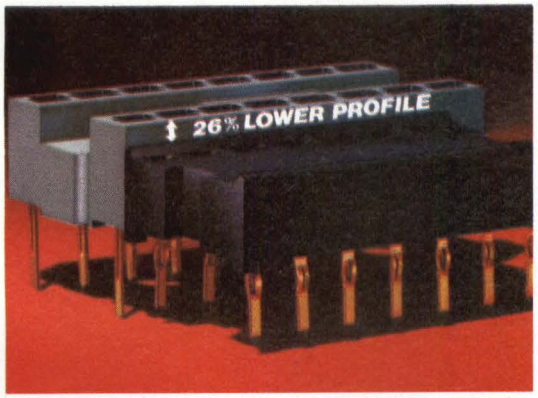


DEBUNKS

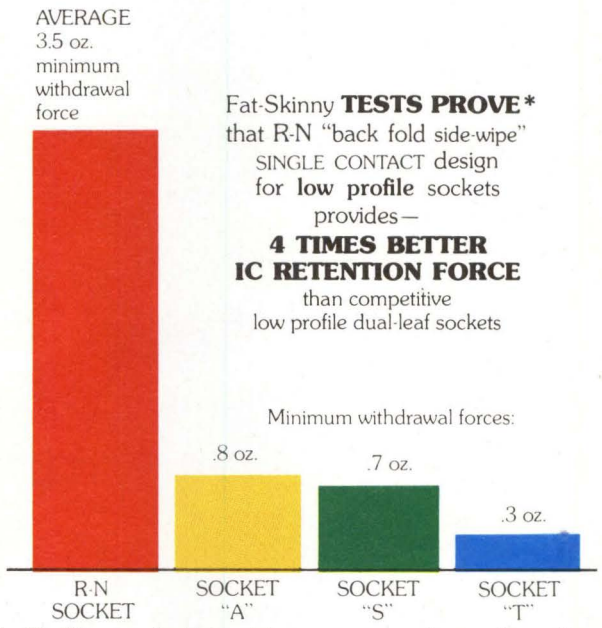
low profile DIP socket MYTH

"...TWO contacts are not more reliable than ONE!"

Surprisingly, a **low profile** (.150" high) DIP socket is a different breed of cat when it comes to engineering in contact reliability. Most standard DIP sockets have dual contacts. (R-N's dual "side-wipe" contacts are among the most reliable in the industry.) But, when you **shorten the contact length** to achieve the "low profile" you lose a great deal of contact force and IC retention strength. So, to achieve effective low profile socket reliability you must **redesign the contacts** and make them out of the **strongest contact material available.**



Low .150" profile of ICL socket reduces board density by 26%.



Fat-Skinny **TESTS PROVE*** that R-N "back fold side-wipe" SINGLE CONTACT design for **low profile** sockets provides—

4 TIMES BETTER IC RETENTION FORCE
than competitive low profile dual-leaf sockets

* In "Fat-Skinny test," withdrawal forces are measured using the smallest size (.008") lead **after** insertion of **largest** size (.012") lead.

Representative NORMAL FORCE Test Scores for 10 R-N ICL low profile sockets

TEST SOCKET	NORMAL FORCE *
1	410 grams
2	465 grams
3	480 grams
4	465 grams
5	395 grams
6	425 grams
7	465 grams
8	395 grams
9	410 grams
10	425 grams

AVERAGE—430 grams

This force is 4 to 5 times greater than average dual contact socket NORMAL FORCE

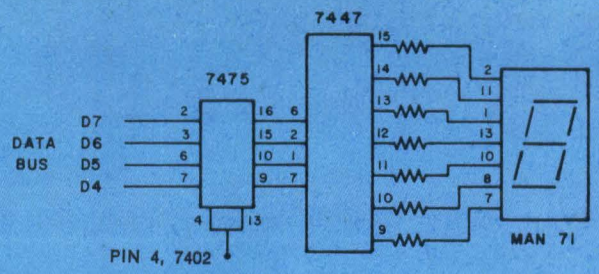
* NORMAL FORCE means force perpendicular or at right angles to IC lead. The single ICL contact exerts this kind of force against the IC lead when inserted into the socket.

WRITE TODAY for latest R-N "Short Form" Catalog of R-N production DIP sockets. Contains full specs, dimensions and material data. Get yours now.

ROBINSON NUGENT, INC.

800 East Eighth Street, New Albany, Indiana 47150 • Phone: (812) 945-0211—TWX: 810-540-4082

CIRCLE 57 ON INQUIRY CARD




```
/THIS SECTION OF PROGRAM OUTPUTS BIT PATTERN
/00111001 (OCTAL 071, HEX 39) TO OUTPUT PORT
/EQUIPPED WITH TWO 7-SEGMENT DISPLAYS.
      •
      •
      •
MVIA    /LOAD A WITH FOLLOWING IMMEDIATE
071     /DATA BYTE (HEX 39, BINARY 00111001)
OUT     /OUTPUT IT TO THE TWO 7-SEGMENT
125     /DISPLAYS EQUIPPED WITH LATCHES
  •     /CONTINUE WITH THE REMAINDER OF
  •     /PROGRAM
  •
```

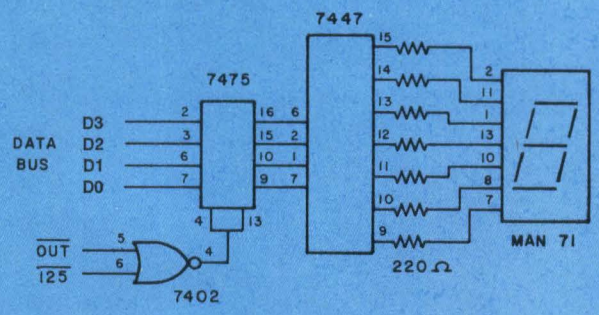


Fig 1 Simple 2-digit LED display interface. 7475 latch inputs are wired to data bus, latch outputs to 7447 decoder/driver, and decoder outputs to 7-segment display with 220-Ω resistors. Execution of OUT 125 causes display interface to latch content of register A; two BCD numbers then show on two displays. Program listing displays 39 on 2-digit display

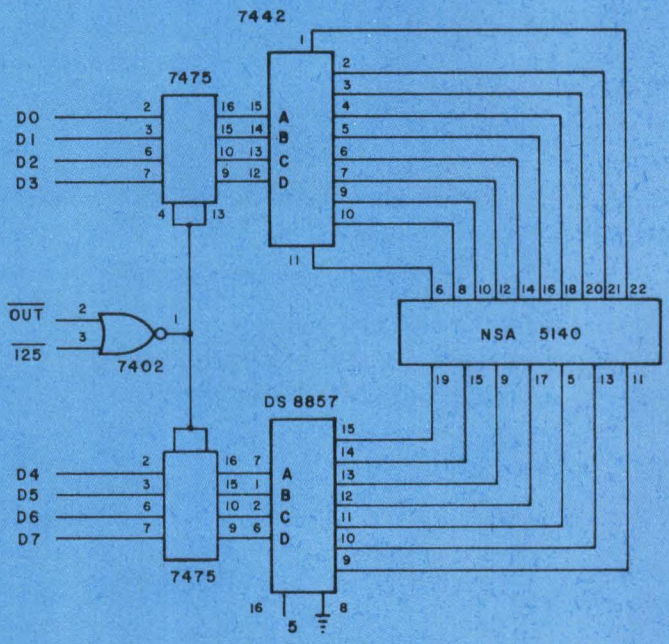


Fig 2 10-Digit multiplexed LED display interface. Digit multiplexing turns on one digit with digit enable code and provides BCD numeric data to multidigit display interface; thus, each digit is turned on, one at a time. Performance of sequence 50 times/s makes display appear to be on continuously

code for the middle digit. Again, after a short delay, the BCD value for the two and the digit enable code for the lefthand display would be output to the interface. By performing this sequence 50 or more times every second, each digit in the display appears to be on, all of the time, because the digits are turned on and off too fast for the eye to see. This method is used in handheld calculators. The interface for a 10-digit multiplexed display is shown in Fig 2.

When an OUT 125 instruction is executed, bits D3 through D0 of the A register will determine which one of the 10 digits in the display will be enabled (turned on). Therefore, these four bits constitute the digit enable code. Bits D3 through D0 are latched (7475) and are decoded with a 1 of 10 decoder (7442). The decoded outputs of the 7442 are wired to the common cathodes of the individual digits in the display. Bits D7 through D4 will provide the BCD code of the value to be displayed (0 through 9). These bits are also latched (7475) and are decoded by a 7-segment decoder/driver (DS8857 from National Semiconductor Corp). The DS8857 supplies the current required to turn on the various segments (A to G) within the enabled digit, selected by the 7442 decoder chip.

A simple program can be written in which five packed BCD words (two BCD digits per word) are output to the display so that a 10-digit number is displayed

LEADER OF THE PACK!

With a Data I/O System 19, you'll always be "top dog."

It's impossible to stay on top of every new development in IC technology—frightening too—especially when it's time to buy a PROM programmer.

Today, there's a lot more in the world to program than PROMs. The programmable logic devices you're specifying today could be dumped next year in favor of a brand new device that can do four times as much and cut the "real estate" in half.

Smart engineers, who want to stay in front of the pack, buy the programmer that won't leave them behind—the Data I/O System 19.

With a System 19 you can program a bipolar PROM, MOS EPROM, FPLA, FPLS, FPGA, PAL, PMUX, programmable port, diode matrix or μP/EPROM. And that's just the beginning of what this remarkable system can do to keep you on top.

Best of all, Data I/O's System 19 is priced within just about everyone's budget.

You haven't shopped around until you've looked at Data I/O. Let us show you the difference. Circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. ***For answers fast, call toll free: 800-426-9016.***

Good idea! DATA I/O

Programming systems for tomorrow...today

"Sure, the big companies They can afford it."

True. For many of the Fortune 500, custom LSI is a way of life. We've been making circuits for Whirlpool since 1968. And putting companies like IBM, Singer and Hewlett-Packard in the chips almost that long.

More recently, Ford, Burroughs, Northern Telecom and ITT have swelled our blue-chip customer list.

But suppose you don't have their resources for developing new products. How can you afford to compete with their dazzling new sewing machines, computers, hand-held calculators, communication systems, appliances and instrumentation?

You do it the way hundreds of smaller companies have done it: with an imaginative product and custom circuits from AMI.

A little LSI goes a long way.

We have scores of case histories showing how emerging, innovative companies have forged to the front with the help of our custom microcircuits. Without going into hock to do it.

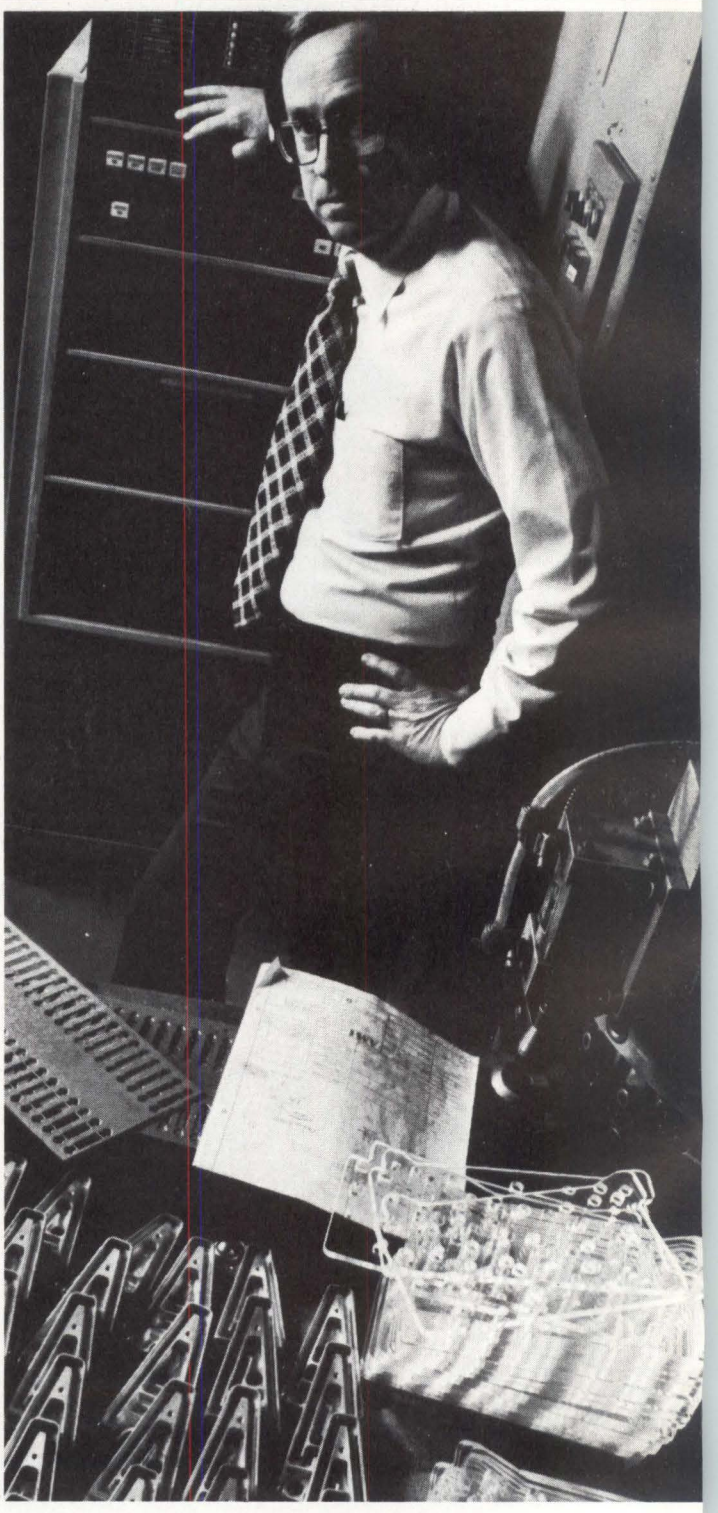
A case in point. A manufacturer of low-speed modems wanted to enter the 9600 bps modem market. So the firm came to AMI for a custom solution. The result: a modem with an order of magnitude fewer components, superior performance and at less than half the going price. It catapulted the company to the forefront of this market.

Two custom AMI chips have made another customer's DTMF (dual-tone-multiple-frequency) receiver the most popular circuit of its kind in modern telephone systems. Another firm has stolen a march on everyone with its high-security cryptographic communication system. (Our chips, again.) And our circuits are helping another company open more garage doors than anyone else.

As different as these companies are, they have one thing in common. None of them sat back and relaxed after getting their first custom circuit. Because they all know this:

You're only as good as your next product.

A custom LSI circuit could put you a year ahead of your competition. That can be the difference between success and failure. And, while your competitors are figuring out how you did it, you move on



use a lot of custom LSI.

to the next generation product.

We've helped our customers stay ahead this way in a number of fields—EDP terminals, TV games, PABXs, facsimile transceivers, burglar alarms and avionics navigation equipment, to name a few.

The beauty of upgrading your product is that it's usually much easier once you have the first custom circuit. And a rapport is built between us. We understand your application and requirements, and you understand what we need to know to make the design changes. Often you work with the same engineers on every project, exploring ways to pack more performance onto the chip. And that again reduces development time and cost.

Which brings us back to that concern.

Doesn't it cost an arm and a leg?

It really doesn't. Although there are initial design and engineering costs, a custom circuit often turns out to be more economical than using standard parts. That's because a custom circuit is a completely integrated system, usually on a single chip. And it comes ready to drop right into your product.

If you build with standard parts, you may be dealing with more expensive components or a larger number of circuits, perhaps providing more capability than your application requires. And remember, components aren't the only costs involved. Assembly and board overhead can run you as much as 50% of your parts price, not to mention the time and money spent on testing and, for microprocessor systems, software development.

We also fabricate a great number of custom circuits along with our catalog products. This increase in volume leads to even more competitive prices, making custom a very attractive way to go. But it's by no means the only way.

Some other alternatives to consider.

As we also build the S2000 (4-bit), S6800 (8-bit) and S9900 (16-bit) microprocessor circuits, we obviously have no axe to grind with the standard approach. We'll steer you that way if it really makes more sense. Or maybe we'll work out a system based on a standard microprocessor with custom peripherals. A lot of our customers have found this the best solution, because many functions, such as A/D conversion, special display drives and high-speed calculations, can't be handled by standard circuits.

While we're talking about alternatives, remember that AMI gives you more custom choices than anyone else. We offer 25 variations of four MOS processes to get you the right speed and power dissipation you need. And we're happy to work with you in any of three basic roles. First, as a complete design and manufacturing service. Second, as a manufacturer only, with you supplying designs created by your company or an independent design house. Third, we could get involved in a joint development program where our circuit designers and your systems engineers work together on a family of circuits for you.

Our new books show you what steps to take.

We've just published two new brochures titled "MOS Systems Solutions: A Dozen Case Histories" and "Six Steps to Success with Custom LSI." They cover the most important factors to consider in choosing a custom LSI supplier. When you see what AMI offers compared with other custom houses, you'll see why we're the leader in this complex field.

So write or call AMI Custom II Marketing, 3800 Homestead Road, Santa Clara, CA 95051. Phone (408) 246-0330. Or one of these regional sales offices: California, (213) 595-4768; Florida, (305) 830-8889; Illinois (312) 437-6496; Indiana, (317) 773-6330; Massachusetts, (617) 762-0726; Michigan, (313) 478-9339; New York, (914) 352-5333; Pennsylvania, (215) 643-0217; Texas, (214) 231-5721; Washington, (206) 687-3101.

We'll send you our brochures. Or, if you prefer, give you a 30-minute presentation right in your office. With the help of custom LSI, you could be right up there with the big companies.

AMI®
AMERICAN MICROSYSTEMS, INC.

Program For 10-Digit Number Displayed on Multiplexed LED

```
/This program drives a 10-digit, multiplexed, LED, 7-segment
/display. In addition, instructions have been added so that
/the intensity of each display is equal.
DISPLA,  LXIH    /Load register pair H with memory
         120     /address where BCD digits are stored
         004     /004 120 = hex 0450
         MVID    /Load D with first digit
         000     /that will be enabled
DISPL1,  CALL    /Display first two packed
         DIGIT   /BCD digits
         0
         INXH    /Increment memory address
         MOVAD   /Get digit enable word into A
         CPI     /Compare it to
         012     /eleventh digit enable count
         JNZ     /Haven't displayed all 10
         DISPL1  /digits yet, so do two more
         0
         JMP     /Have displayed all 10 digits,
         DISPLA  /so display them all again
         0
DIGIT,   MOVAM   /Get packed BCD word into A
         RLC     /Rotate four LSBs into
         RLC     /four MSBs
         RLC
         RLC
         CALL    /Then display this digit
         OUTIT
         0
         MOVAM   /Get the same word again
OUTIT,   ANI     /Save only four MSBs
         360     /(360 = hex F0)
         ADDD    /Add digit enable
         OUT     /Output 8-bit value
         125
         INRD    /Increment digit enable
INTENS,  MVIE    /Load E with a number
         100     /100 = hex 40
INTEN1,  DCRE    /Decrement the number
         JNZ     /If it is nonzero, execute
         INTEN1  /JNZ instruction back to INTEN1
         0
         RET     /When E = 0, return
```

(see Program Listing). This program has to unpack the BCD words stored in memory, combine the BCD digits with a unique digit enable code and then output these eight bits of information to the interface. For instance, the value 01010011 will cause a five to be displayed in the fourth digit from the right on the display. The digit enable code in this example is 0011, and the digit enable code for the righthand display is 0000.

To display the number 3,163,908,332, register pair H is first loaded with the memory address where the two least significant digits (32) are stored. In the Program, this address is 004 120. Only five memory locations are required to store the 10-digit number, because the number is stored in a packed BCD format. The D register, which stores the digit enable code, is then set to 0. The content of register D, which will eventually be latched by the interface hardware, is used to turn on only one digit at a time. At DISPL1, the DIGIT subroutine is called, so that the content of memory addressed by register pair H is moved to the A register. Since the data values are stored in memory as packed BCD digits, this subroutine unpacks them. The digit in the four least significant bits (LSBS) of register A is rotated to the left four times, bit by bit. The first digit to be displayed is now in bits D7 through D4 of register A when the OUTIT subroutine is called.

At OUTIT, the four LSBS of the A register are set to zero by the ANI instruction (the digit to be displayed is in bits D7 through D4). The digit enable code contained in the D register is then added to the BCD number in the A register and the result is output to the interface (OUT 125). When this word is output, the four LSBS determine which digit is enabled and the four most significant bits (MSBS) represent the value to be displayed. The first time the OUTIT subroutine is executed, the A register will contain 00100000, because a two must be displayed on the right-hand digit.

At the end of the OUTIT subroutine, the content of the D register (the digit enable code) is incremented from zero to one preparing it for the next digit enable code. To "intensify" the digit that has just been turned on, the computer executes a time delay at INTENS. Thus, the digit is kept on for a period that allows it to be clearly seen. When the 8080 finishes the OUTIT subroutine, it returns to the MOVAM instruction just before the OUTIT subroutine. The A register is loaded with the content of the same memory location addressed by register pair H, only this time the BCD digit contained in bits D7 through D4 must be displayed. This is the second digit from the right in the number 3,163,908,332. The ANI instruction at OUTIT sets bits D4 through D0 to zero, the digit enable code (one) is added to the number, and the result is output. After incrementing the digit enable code to two, the microprocessor again executes the INTENS delay loop, so that the three on the second digit from the right is displayed for a reasonab'e amount of time. When the RET instruction is executed, the microprocessor returns to the INXH instruction just after DISPL1.

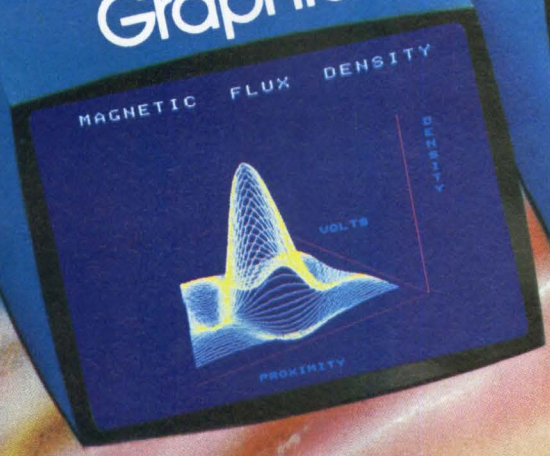
The microprocessor increments the memory address in register pair H and then examines the digit enable code contained in the D register. If this code is less than 012 (decimal 10), the microprocessor jumps back to DISPL1 so that the two BCD digits now addressed by register pair H are displayed. If the digit enable code is equal to 012, then all 10 digits in the number have been displayed. If this is the case, the microprocessor jumps back to DISPLA, so that the memory address in register pair H and the digit enable code in the D register are reinitialized.

From this program, it is evident that the microprocessor constantly updates the display (writes new information out to the interface). New digit enable codes and data values are output to the display every millisecond. Software techniques—converting the program to a subroutine or using an interrupt—can prevent the program from tying up the microcomputer. These methods, together with additional means of hardware interfacing of multiplexed displays, will be concluded next month in Part 2.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Add Aydin IMAGE-ination

with the complete Graphic/Image System



Computer-aided design, Management information systems, Medical/tomography, Command and control, Earth resource/land mapping, Reconnaissance photography, Training/simulation systems, Process control, Micrographics.

Aydin Controls, since 1967 the pioneer in computer graphics and imaging, can help you more efficiently, effectively, and creatively structure your man/machine interface with the 5216 Color Graphic/Image System.

Versatile, modular hardware — You can configure the 5216 for requirements from simple alphanumeric or graphic displays to sophisticated image-processing and analysis applications.

Flexible, easy-to-use software — The 5216 is available with the most comprehensive software package in the industry, including a highly efficient operating system, two- and three-dimensional packages, image analysis program, and interactive list processing software.

Extensive peripherals and accessories — Keyboards joysticks, track balls, graphic tablets, graphic printers, cartridge and floppy disk drives, and much more to come.

AYDIN CONTROLS

We make it easy to add Aydin IMAGE-ination

Our application engineers can help you add Aydin IMAGE-ination. Call or write for a demonstration or for more information.

414 Commerce Drive Ft. Washington, PA 19034 (215) 542-7800 TWX: 510-661-0518

CIRCLE 59 ON INQUIRY CARD

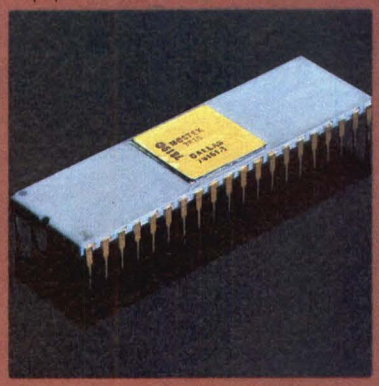
AY-101

Now supports F8, 3870, 3872.

A chip builder's business is building chips. Yours is designing with them. So is ours.

That's why we build a microprocessor lab like you'd design for yourself.

Both the Tektronix 8001 and 8002 microprocessor development labs now fully emulate the 3870, 3872 and F8. You can select the chip that best fits the job without repurchasing or relearning equipment.



INSTRUMENTATION BUILT OUR REPUTATION

The chip builders have their own specialties. But ours is similar to your own: as one of the world's foremost instrumentation designers, Tektronix deals with your kinds of design problems and your kinds of deadlines. We've learned through experience how to maximize equipment versatility and reliability.

That's why our lab supports chips from a variety of builders. Including the 3870, 3872 and F8. The 8085A and 8080A. The Z80A. The 6800. The TMS 9900.

Based on years of experience with microprocessor designs, our labs include many other capabilities like you'd engineer for yourself.

REAL TIME ANALYSIS OPTION

Dynamic monitoring with dual 49-bit breakpoint registers enables quick isolation of timing and logic problems.

ENHANCED BASIC

This enhanced compiler version of BASIC supports the instruction set of the 8080A and can run on the 8080A, 8085A and Z-80A. The compiler produces optimized code. Extensions include facilities for modular programming, interrupt handling, memory I/O, bit operations, and access to I/O ports.

COMPREHENSIVE WORKSHOPS

Microprocessor design workshops are held for our customers monthly, in several locations throughout the country. Programs include a 5-day design workshop and a 3-day course concentrated on the labs themselves.

From engineering to education, you get the painstaking quality you expect from Tektronix. Including expert service and consultation from nearby Tektronix field offices. Ask your Tektronix Sales Engineer for the full story, or contact Tektronix, Inc., P.O. Box 500, Beaverton, OR. 97077. In Europe, Tektronix Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

For immediate action, dial our toll-free automatic answering service, 1-800-547-1512. In Oregon, call collect 644-9051.

Tektronix®
COMMITTED TO EXCELLENCE

For 3870 information circle 60,
For literature circle 61,
For a demonstration circle 62.

FOR FAST REPLY, CALL TOLL FREE (800) 547-1512.
In Oregon, collect 694-9051.

Tektronix microprocessor development labs.

Designed by people on your side of the bench.

QUALITY: The first reason to choose Mostek's LSI-11/2* add-in memory.

2 Optional on-board parity generation and checking.

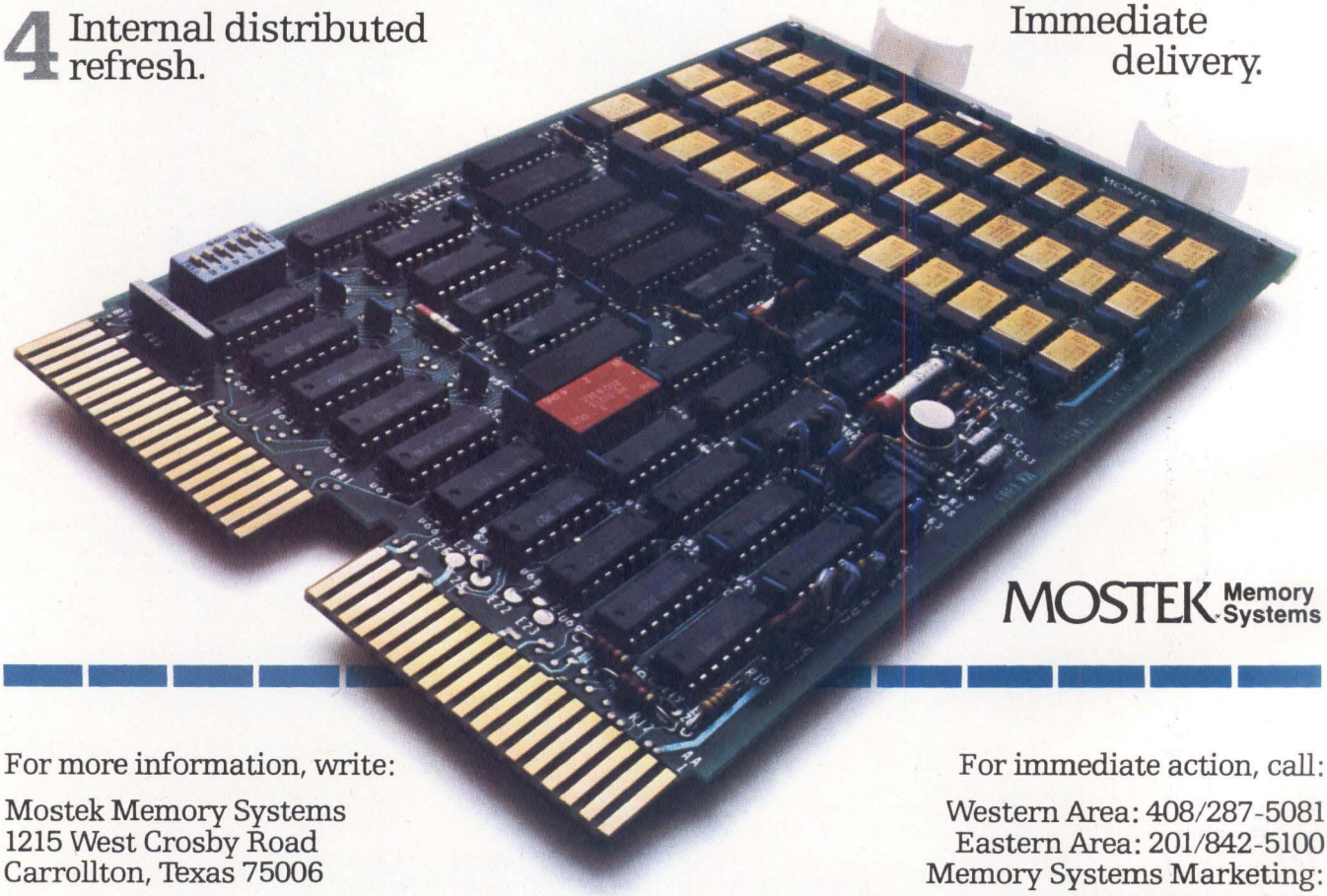
3 Mostek's industry-standard MK 4116 dynamic RAMs.

4 Internal distributed refresh.

5 Totally hardware and software compatible with LSI-11/2 and LSI-11.

6 $1160: 32K x 16. (Single quantity price. OEM discounts available.)

Immediate delivery.



MOSTEK Memory Systems

For more information, write:

Mostek Memory Systems
1215 West Crosby Road
Carrollton, Texas 75006

For immediate action, call:

Western Area: 408/287-5081
Eastern Area: 201/842-5100
Memory Systems Marketing:
214/242-0444 ext. 2552

My need is: ☐ now ☐ 3-6 months ☐ 6+ months

I'm interested in: ☐ LSI-11/2 ☐ PDP11* ☐ PDP-11/70* ☐ Nova 3** ☐ Eclipse**

Name/Title _____

Company _____ Phone ( ) _____

Address _____

*TM of Digital Equipment Corp. **TM of Data General Corp.

Monoboard Microcomputer Adds Programmable Timer For Process Control Adaptations

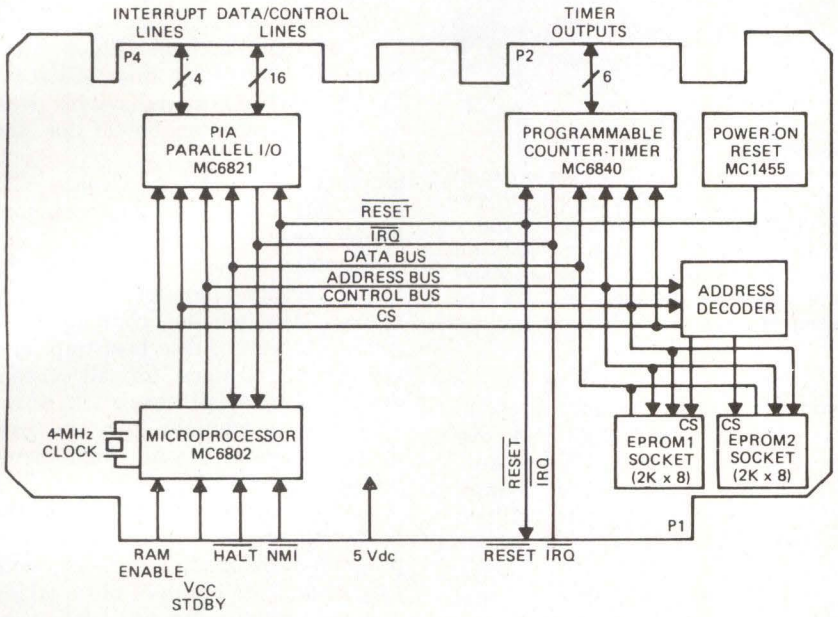


Fig 1 Basic microcomputer. Monoboard micromodule M68MM01B from Motorola Semiconductor Products features programmable timer module for counting, measuring, and generation tasks. Incorporated are necessary crystal clock circuits, reset timer for power-on initialization, and address bus decoding to establish address of each part

Two monoboard microcomputers for the Micromodule line introduced by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036 feature a programmable timer function for process controls. The basic standalone microcomputer is the M68MM01B that has the processing and control power of an MC6802 MPU with its self-contained clock circuit and 128 bytes of static RAM. As shown in Fig 1, the module contains sockets for up to 4k of EPROM or ROM for programming, a peripheral interface adapter (PIA) with 20 programmable I/O lines for parallel data transfers, and a programmable timer module (PTM).

The MC6840 triple 16-bit timer/clock provides for such tasks as frequency measurements, event counting, interval measuring, square wave generation, gated delay signals, single pulses of controlled duration, pulse width modulation, and timed system interrupts. A buffered 4-MHz crystal oscillator circuit provides clock input to the MPU. The MPU's divide-by-4 circuit generates the required 2-phase MPU clock and 1-MHz

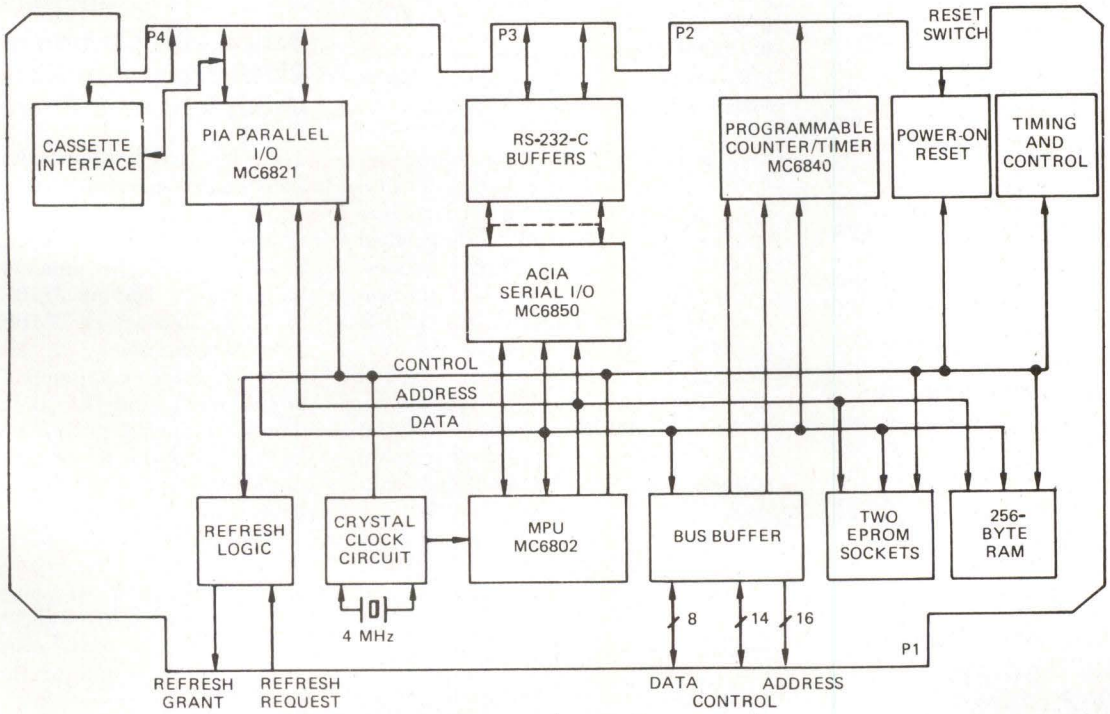


Fig 2 Expanded version. Additions of 256 bytes of static RAM, offboard dynamic memory refresh, ACIA with RS-232-C interface circuits, audio tape cassette interface circuit, and bus drivers increase microcomputer's capability. M68MM01B1A is compatible with M6800 EXORcisor, and is expandable with more memory and I/O

phase 2 external clock for the rest of the system.

The data bus transfers data between the MPU and onboard devices. The address bus selects memory locations within the board. A partially decoded addressing scheme uniquely addresses each onboard EPROM/ROM, PIA, and PTM; these devices are selected by an address decoder circuit which consists of prepatterned P/ROM and PC board interconnections. Both addressing of and data transfers to the onchip MPU RAM are handled within the chip.

Measuring 9.75 x 6.00 x 0.062" (24.77 x 15.24 x 0.157 cm), the module also has a reset timer for power-on initialization. Timer input frequency is 1-MHz internal or asynchronous external gate/trigger inputs. Timer operating modes are continuous (square wave), single shot, frequency comparison, and pulse/width comparison. Power requirements are 5 Vdc at 350 mA; with EPROMS, 5 Vdc at 450 mA. Full compatibility with MC6800 software is supplied.

The second module, M68MM01B1A, is a more fully populated version of the first (see Fig 2) with an additional 256 bytes of static RAM, provisions for offboard dynamic memory refresh, an asynchronous communications interface adapter with RS-232-C interface circuits, audio tape cassette interface circuit, and bus drivers for the address, data, and control bus signals. For greater memory and I/O capacity, other external devices can be added, unlike the M68MM01B which does not have address, data, or control signals available for interfacing with other modules.

Bus compatibility with the M6800 EXORciser™ allows hardware and software development and debugging, and production hardware troubleshooting. Power requirements are 5 Vdc at 550 mA, 12 Vdc at 20 mA, and −12 Vdc at 25 mA; and with EPROMS, they are 5 Vdc at 650 mA, 12 Vdc at 260 mA, −12 Vdc at 180 mA.

Circle 410 on Inquiry Card

System Accepts TV Input Signal And Displays Digital TV Picture

A general purpose microcomputer system with digital image processing, Beck-1/System serves as a standalone system or interfaces to host mainframes as a digital TV display and TV acquisition subsystem. The terminal type enclosure houses a Z80 CPU, up to 64k bytes of CPU RAM and 32k bytes of CPU ROM, serial and parallel I/O ports, floppy disc storage with mini and standard floppy drives, a keyboard, and CRT display. A DMA controller, realtime clock, and floating point arithmetic unit also are available.

Z80 based Beck-1/System microcomputer with TV input and digital TV display digitizes and displays up to 256 x 240 4-bit pixels, has 512 x 480 1-bit pixel interlaced graphics, and programmable character densities to 40 x 120 characters

Capable of digitizing a TV input signal and displaying a digital TV picture, the programmable display processor contains up to 32k bytes of image RAM, displayed as characters, graphics, or a digital TV (gray scale) picture. Programmable parameters include character and pixel size and count, character blink, reverse, underline, and half intensity. Also featured are nondestructive zoom, and horizontal and vertical panning in all three display modes.

Pixel density of the TV input A-D and gray scale display is up to 256 x 240 4-bit pixels (16 levels). Graphic densities are up to 512 x 480 1-bit pixels. Unit can supply an RS-170 compatible signal, interlaced or noninterlaced, or run off camera supplied sync—RS-170, RS-330, or random interlace.

Configurations prepackaged by Beck Corp, 303 Slocum Ave, Neptune, NJ 07753 span a range of OEM and small business needs. Applications using TV input and display capabilities include industrial noncontact measurement, surveillance, broadcast effects, QC inspection, and robotics, as well as others combining TV and computer technologies. Models without the video facilities suit more traditional small business application areas. Software security features for OEM and systems houses prevent interchange of firmware or software between systems; with a diagnostic capability, one system can test another without disassembly. Range of systems are from $2900 for the Beck-1/30A basic system with no disc storage to $6800 for the -1/50C which includes TV input, graphics and digital TV display, 32k-byte CPU RAM, and dual standard floppy discs.

Firmware consists of the BECKMON-1 system monitor and BECKPLOT-1. The monitor contains basic console functions, disc bootstrap, and I/O driver routines for all system devices. Display processor I/O driver and plotting routines give the user display control from high level macro calls.

System software consists of the CP/M operating system, BASIC, and program development package, with PASCAL and 3D graphics to be added soon. Users may also use other companies' software that is compatible with the Z80 CPU and CP/M operating system.

Circle 411 on Inquiry Card

Board Fills Computer's ROM Expansion Needs Using Reduced Power

The iSBC 464™ EPROM/ROM expansion board accommodates both the 16-bit iSBC 86™ or 8-bit iSBC 80™ single-board computers. Containing 2732 EPROMS, the memory can use 8k-bit 2758, 16k-bit 2716, and 32k-bit 2732 EPROMS or 2316E ROMS to meet system needs. It takes advantage of these components' standby power mode and 5-V only features, thereby reducing power consumption by up to 40%; it operates from a single 5-V power supply. Price is $495 in single quantity.

To achieve compatibility with the 86/12 computer, the expansion memory must be able to place a 16-bit word (or one byte) on the Multibus™ data lines, and must respond to a 20-bit address code so that it may be located anywhere within a 1M-byte address space. Multibus compatibility allows the memory to be designed into a multiprocessor en-

"Efficiency is in. Extravagance is out."

—Vector Graphic

That's why when you look for top-quality, low-cost, add-on-memory you should always look for Vector Graphic on your memory boards. It means they stand behind every product through over 200 Vector Graphic dealers.

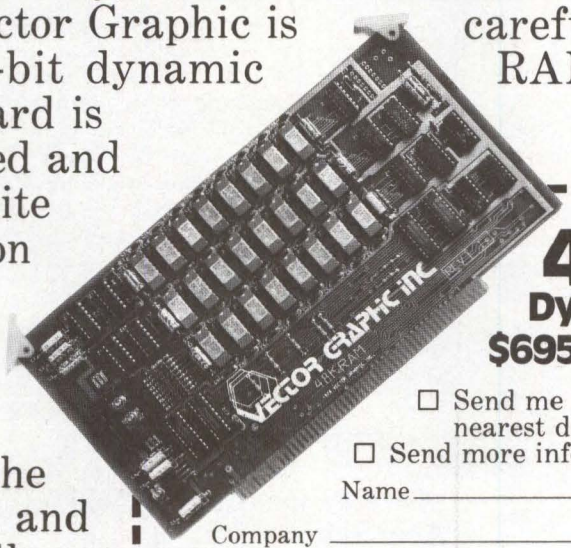
Vector Graphic is the only one who designs in so much quality for so little cost.

The 48K Dynamic RAM memory board is used in the Vector MZ microcomputer, although any Z-80/S-100 computer system can take advantage of the problem-free transparent refresh offered in this high-quality, low-cost add-on-memory.

It's no secret, Vector Graphic is carefully assembling state-of-the-art 16K-bit dynamic RAMs into boards. And each board is thermally cycled, aged and continuously read-write tested over 400 million error-free cycles.

The new 48K board consumes less than 4 watts total power and provides the same superior design and reliability found in all products from Vector Graphic. Remember, it's memory that works.

— Dealer inquiries invited —



48K RAM
Dynamic Memory
$695 (suggested U.S. retail price)

☐ Send me the name of the nearest dealer
☐ Send more information

Name_____

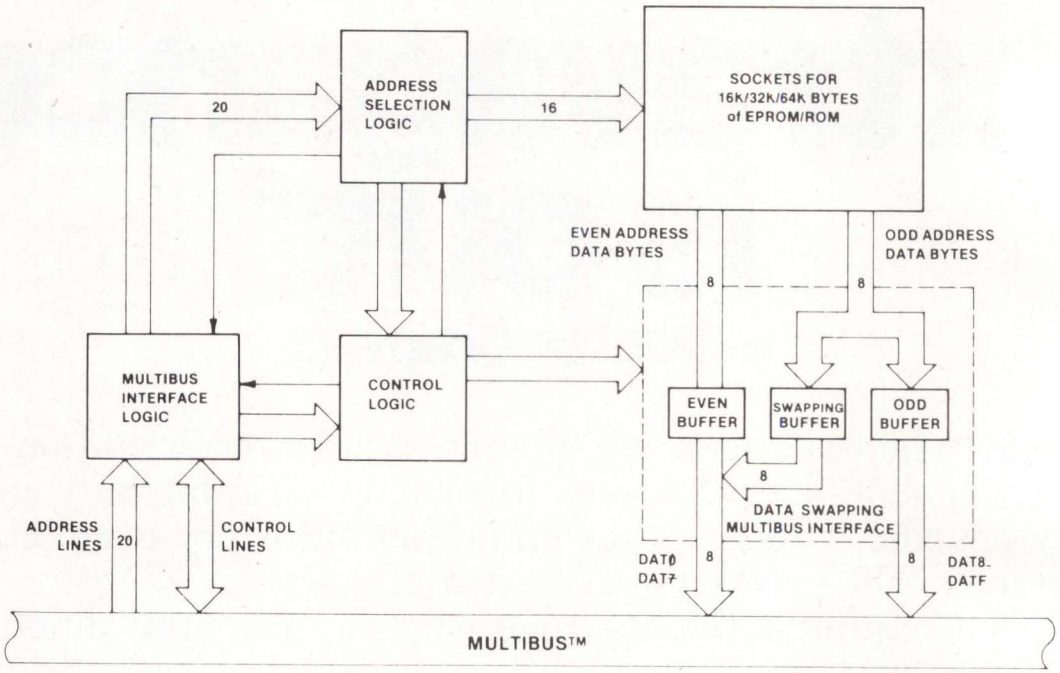
Company _____

Address_____

City/State/Zip_____

VECTOR GRAPHIC INC.
31364 Via Colinas, Westlake Village, CA 91361, (213) 991-2302

CIRCLE 64 ON INQUIRY CARD



Memory expansion board for Intel's iSBC 86/12, as well as iSBC 80, family of single-board computers interfaces with Multibus system bus. iSBC 464 is characterized by 20-bit address and 16-bit data buses

vironment including both 80 and 86 CPU boards.

Developed by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, the board contains 16 sockets for a maximum of 64k bytes of nonvolatile memory. Actual capacity is determined by the type and quantity of EPROM/ROM components installed. Although only one device size may be used, EPROMs and ROMs may be mixed on one board.

The board operates with 1 of 15 switch selectable memory access times ranging from 35 to 1550 ns. Mode of operation is selected by placing two option jumper blocks in the appropriate sockets. The 8-bit only mode provides an efficient memory configuration for systems limited to 8-bit data. The 16/8-bit mode allows 16-bit processors to access 16-bit words; in addition, 8- or 16-bit microprocessors can access either the high or low order byte of a 16-bit word.

Memory space is organized into four banks. Consisting of one-fourth the total board capacity, each bank can contain a maximum of 4k, 8k, or 16k bytes of ROM. Unused memory sockets can be deselected to free memory addresses for use elsewhere in the system. Thus, configurations with fewer than 16 memory components do not fill memory address space with unaddressable blocks.

Circle 412 on Inquiry Card

Word Processing System Also Supports Data Processing Applications

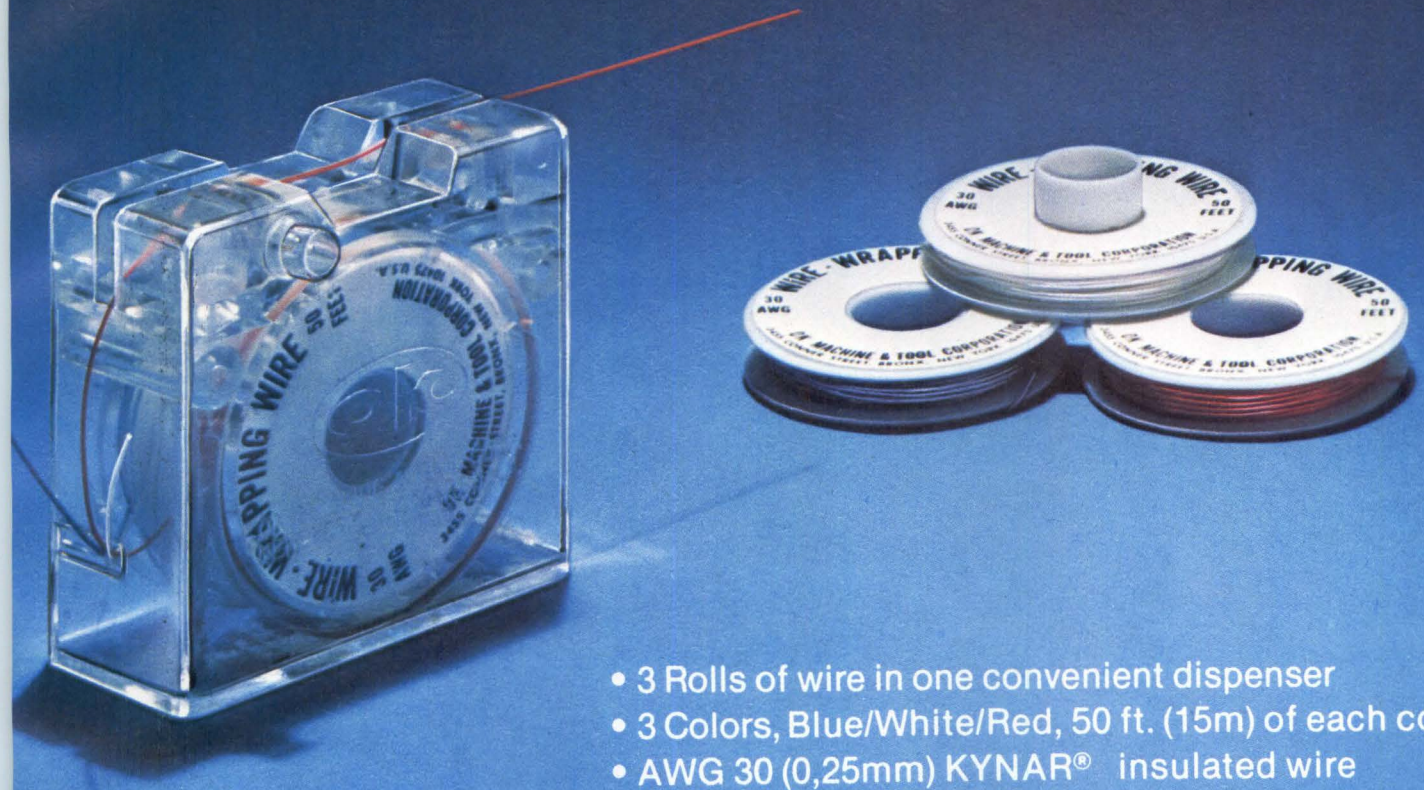
A video based system with data processing capability, Memorite 2 contains the MZ microcomputer with disc storage, the Mindless Terminal, and Qume Sprint 5, a 55-char/s printer. The S-100 bus compatible mainframe has 18 slots and requires a power supply of 8 V at 22 A and ±16 V at 4 A. Two Micropolis MODII disc drives store 630k bytes. The processor is the Mostek Z80A with a 158-instruction set.

For word processing uses, the system handles advanced text preparation, edit, and delete capabilities. It offers automatic letter printing from memory with full formatting techniques. P/ROM resident memory has a capacity of 12k bytes and a 1k-byte static RAM. Speed of the static RAM is 450 ns; the P/ROM's is user selected (450 ns typ).

One serial and two parallel I/O ports have been included by Vector Graphic Inc, 31364 Via Colinas, Westlake Village, CA 91361. Features of the serial port are EIA RS-232, 20-mA current loop, and TTL signal levels; an asynchronous data rate from 110 to 9600 bits/s; and an 8251 programmable USART. With the parallel port, there are TTL sig-

TRI-COLOR

WIRE CUTTING AND STRIPPING DISPENSER



- 3 Rolls of wire in one convenient dispenser
- 3 Colors, Blue/White/Red, 50 ft. (15m) of each color
- AWG 30 (0,25mm) KYNAR® insulated wire
- Built-in cutting plunger cuts wire to desired length
- Built-in stripper strips 1″ of insulation
- Easily refillable
- For wire-wrapping and other applications.

Model No. WD-30-TRI
Patent Pending

WD-30-TRI	DISPENSER WITH WIRE	$5.95
R-30-TRI	TRI-COLOR REPLACEMENT SPOOLS	$3.95

Kynar® Pennwalt

MINIMUM BILLING $25.00 / ADD SHIPPING CHARGE $1.00 / NEW YORK STATE RESIDENT ADD APPLICABLE TAX

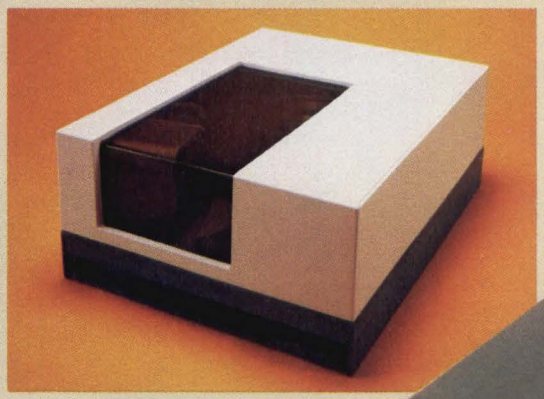
OK® MACHINE & TOOL CORPORATION 3455 CONNER ST. BRONX, N.Y. 10475 (212) 994-6600/Telex 125091

CIRCLE 65 ON INQUIRY CARD

The intelligent disk architecture is available in STC

STC's new 2700 winchester disk family combines the intelligence of a microprocessor, 64k bytes of RAM, and a high-speed bus interface to offer you a versatile new disk architecture. An architecture that can help you achieve new dimensions in system speed and performance. Relieve CPU overhead burdens. Slash interfacing costs, and more.

Yet even without its advanced architecture, you'd still choose the 2700 disk family for its attractive price/performance and reliability values.



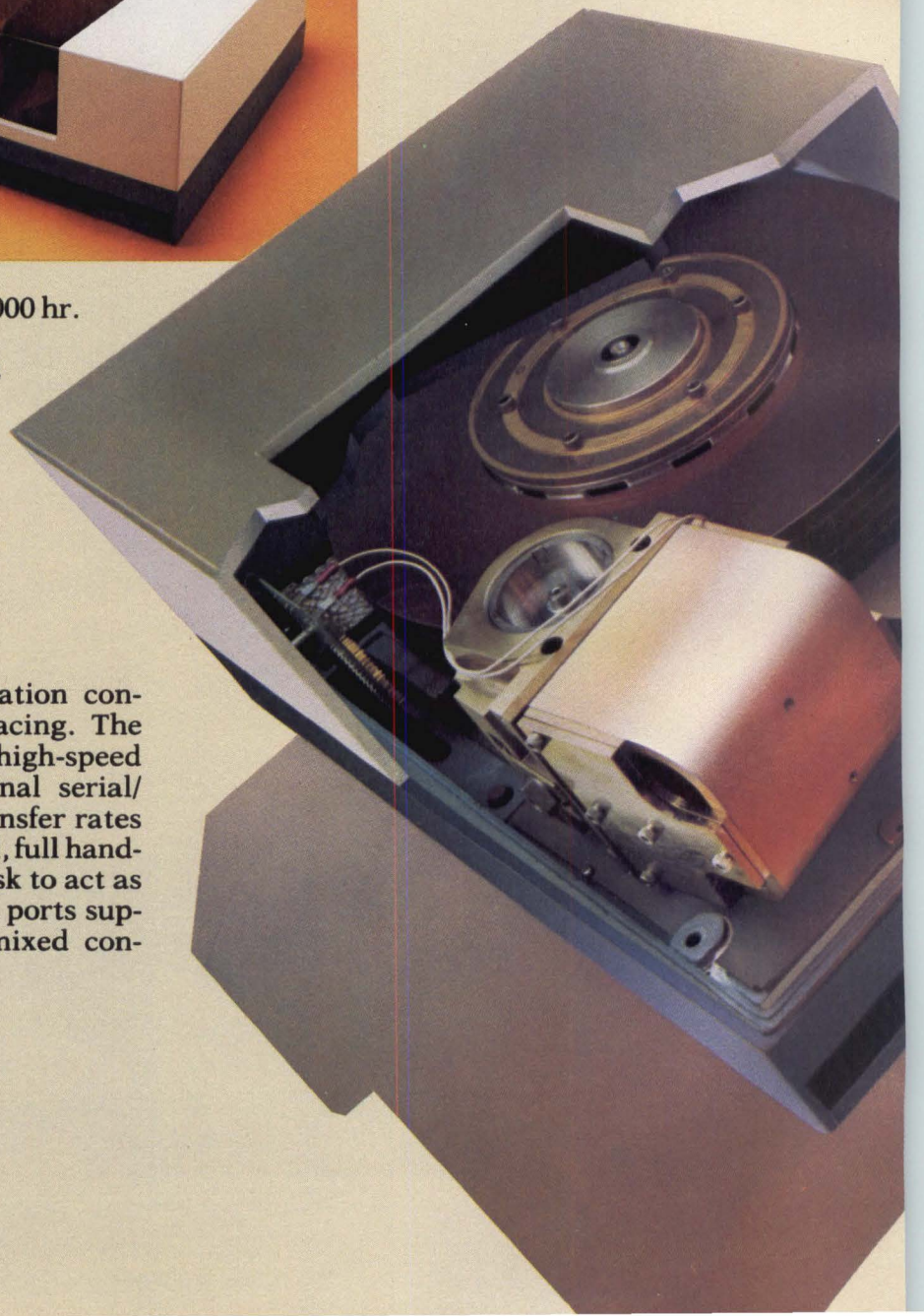
The 2700 family features formatted capacities of 39, 93, and 200 Mbytes, 25 msec average seek time, and OEM prices ranging from less than $3,600* (39 Mbyte) to less than $5,000* (200 Mbyte). With an 8000 hr. continuous operation MTBF, the 2700 will not just keep your customers happy, it'll keep your warranty expenses low.

*Domestic USA OEM prices in quantitities of 100.

Powerful bus architecture for faster data rates and greater flexibility.

Gone are the speed and configuration constraints of serial, data-line interfacing. The 2700 disk family incorporates a high-speed byte-parallel interface, with internal serial/parallel conversion, to give you transfer rates up to 2 Mbytes/sec. The bidirectional, full handshake protocol permits any 2700 disk to act as master or slave, while built-in dual ports support radial, daisy chain or intermixed configurations.

Most important to you, the 2700 architecture offers maximum flexibility for applying these features. For instance, the architecture, coupled with the RAM buffer, permits continuous data transfer on both ports simultaneously. Thus your CPU can communicate with a 2700 on one port while disk-to-disk communication occurs on the other.



you'll need tomorrow Disks today.

The μP can unlock your system's hidden resources.

One way to boost your CPU's performance is to get it out from under system overhead and back to productive computing. The on-board intelligence of the 2700 gives you that capability. Routines such as drivers, data management and utilities can be offloaded to the microprocessor, freeing the CPU and bus for other tasks. But that's just the beginning.

For example, you can use the microprocessor to optimize throughput by means of zero millisecond writes and cacheing algorithms to speed read access.

High-level software, including on-board editor and compiler, simplifies algorithm development for the above and other custom applications. And you can use the built-in RS-232 port to program right on the disk.

An intelligent controller in each drive. For free.

To help you get to the system level faster and easier, we placed 80% of the traditional controller functions within the 2700. Including all device dependent functions. Since you now only have to build a low-cost interface adapter—not a complete controller—your attachment costs are significantly reduced.

Low cost of ownership.

Fewer parts mean fewer failures. So the 2700 contains a minimum number of mechanical parts, only two of which move: spindle and actuator. The microprocessor contributes to this simplicity by replacing all sequencing and servo logic with firmware.

To eliminate scheduled maintenance, the 2700 dispenses with potentiometers. Dynamic adjustments are made internally under microprocessor control. And the 2700's closed loop air system means no filter changes.

If there's ever a failure, internal diagnostics isolate the problem to one of three subassemblies: logic board, head/disk assembly or power system. And these components uncouple quickly for fast repair.

All of this translates into high MTBF, low MTTR, to reduce your warranty and field service costs.

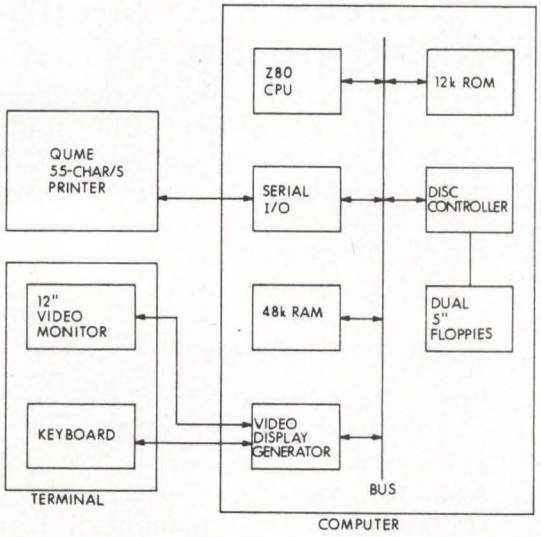
To learn more...

about tomorrow's disk architecture, today, contact OEM Marketing, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone (800) 525-2940; in Colorado 497-5151. In Canada: Ron Reardon, STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W 5R8. Phone (416) 675-3350.

CIRCLE 66 ON INQUIRY CARD

STC

STORAGE TECHNOLOGY CORPORATION



Interaction between Vector Graphic's high speed Z80 based MZ microcomputer and peripherals—Qume printer and video monitor terminal with keyboard—is illustrated. Basic system components are also diagrammed

nal levels; 16 input, 16 output, and 2 control lines; and data transfer rate of greater than 100k bytes/s.

The 12″ (30-cm) diagonal CRT Mindless Terminal has a resolution of 900 lines at center. The keyboard has 56 keys, capacitance type with numerical keypad and cursor control. A 48k-byte dynamic RAM is compatible with the Z80 at 4 MHz.

The system also acts as a data processor, performing standard accounting tasks and custom applications in Business BASIC. Scientific calculations also are available.

Circle 413 on Inquiry Card

Modularity of μComputer Board Series Suits OEM Requirements

Micro Design Series (MD Series™) of OEM microcomputer boards offers the designer two types of Z80 based modules that may be configured in any combination to aid initial production as well as future system upgrading or modification. Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 has designated the standalone microcomputer line as MD™ and the general purpose 8-bit STD-Z80 BUS compatible, expandable board line as MDX™. The latter cards are modularized by function. They include a CPU card; 8k, 16k, and 32k dynamic RAM cards; serial I/O (SIO); parallel I/O (PIO); combination EPROM and UART (EPROM/UART); and software development/debug (DEBUG). All measure 4.5 x 6.5″ (11.4 x 16.5 cm) and are available in 2.5- or 4-MHz versions. The STD BUS, jointly defined by Mostek and ProLog Corp, allows any combination of cards to be used in any card slot.

MDX-CPU1 serves as the CPU of a multimodule Z80 based microcomputer system. Features are the Z80 CPU, 4k x 8 P/ROM, 256 x 8 RAM, flexible memory decoding, and four counter/timer channels; it operates on 5 V only. Three versions of the add-on RAM module—MDX-DRAM8, -16, and -32—are address selectable on 4k boundaries. The -16 and -32 come in 4-MHz versions. Containing a fully buffered asynchronous I/O port with teletypewriter reader step control, the add-on P/ROM module (MDX-EPROM/UART) has 10k x 8 EPROM/ROM. Its serial I/O channel includes RS-232 and 20-mA interfaces, and baud rate generator for 110 to 19.2k baud.

The general purpose MDX-PIO interface, using MK 3881 Z80-PIOs, has up to four fully programmable I/O ports—any combination of two bidirectional plus two input or output ports. Operating from 5-V only, the board features strap selectable port addresses. Full interrupt capability supports Z80 mode 2 interrupts and has two handshake signals for each port. Basis of the MDX-SIO, designed as a multiprotocol asynchronous or synchronous I/O module, is the MK 3884 Z80-SIO. Two full-duplex multiprotocol channels feature asynchronous, bisynchronous, HDLC or IBM SDLC, receiver data registers quadruple buffered, and transmitter data registers double buffered. Also included are a dual baud rate generator, data and clock buffered for RS-232 and 20-mA current loop, and eight modem control lines buffered for RS-232.

Replacing external development equipment, MDX-DEBUG allows the designer to generate and debug Z80 programs in conjunction with the -CPU1 and -DRAM modules. The 10k bytes of firmware include a line or character oriented editor; debugger with memory and register exams, and breakpoints; and assembler featuring relocatable object code with linking loader. RS-232 and 20-mA interfaces, reader step control for teletypewriters, and 110- to 19.2k-baud rate generator characterize the serial I/O port.

The MD cards, while Z80 based and the same size as MDX modules, are not compatible with the bus. MD-SBC1 features 8k x 8 EPROM, 2k x 8 RAM, two 8-bit input ports, three 8-bit output ports, two interrupt inputs, 2.5-MHz crystal clock, and operates from a single 5-V power supply. I/O ports are brought to the 56-pin edge connector.

For evaluation of the MD series, a prototyping kit is available. MDX-PROTO consists of an 8-slot card cage, MDX-CPU1, MDX-DRAM8, wirewrap, extender, and MDX-DEBUG cards. A-D and D-A conversion modules, floppy disc controllers, high speed math, DMA controllers, and other system and I/O intensive modules are planned for future announcement.

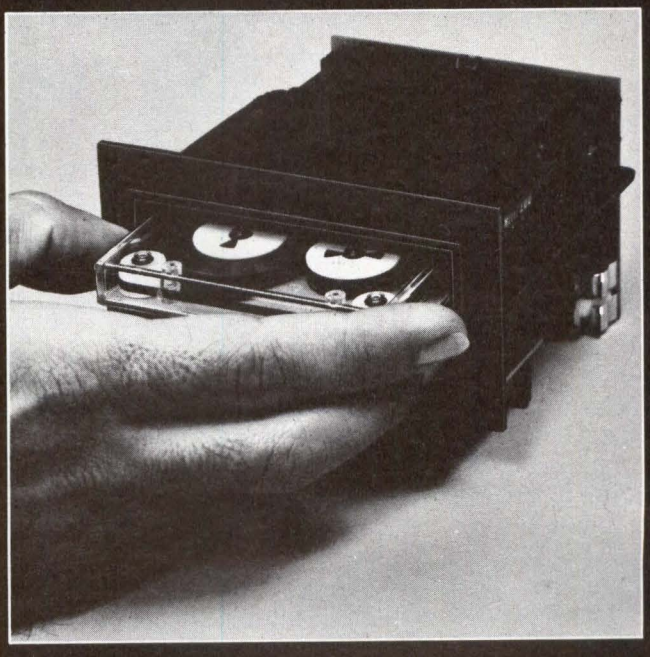
Circle 414 on Inquiry Card

Qantex

672,000 BYTE TAPE DRIVE FOR 3M DC100A DATA CARTRIDGE

MODEL 200 MINIDRIVE™...
The most compact tape drive ever...
Large, up to 672,000 bytes capacity...
Recording on one or two tracks...
Read-after-write capability...
3M DC100A or ITC TC-150 Data Cartridge...
High transfer rate, up to 48,000 bits-per-second...
Low power requirements, +5 and +12 Volts DC only...
High electrical and mechanical reliability...
Flexible configurations range from basic OEM building blocks to complete tape memory systems...
Optional electronics and mounting hardware...
From $250 in single unit quantities...
Contact us today for complete details...

Qantex Division of
North Atlantic Industries
60 Plant Avenue, Hauppauge, NY 11787
(516) 582-6060 TWX 510-227-9660



CIRCLE 67 ON INQUIRY CARD

ANNOUNCING THE LOW-COST 16-BIT MICROCOMPUTER, MP/100.

THIS IS HOW FAR YOUR MONEY CAN GO.

Function and economy. Those are the two reasons we packed more features in our new 16-bit microNOVA® MP/100 than anyone would have thought possible. And at a price lower than anyone would have thought possible.

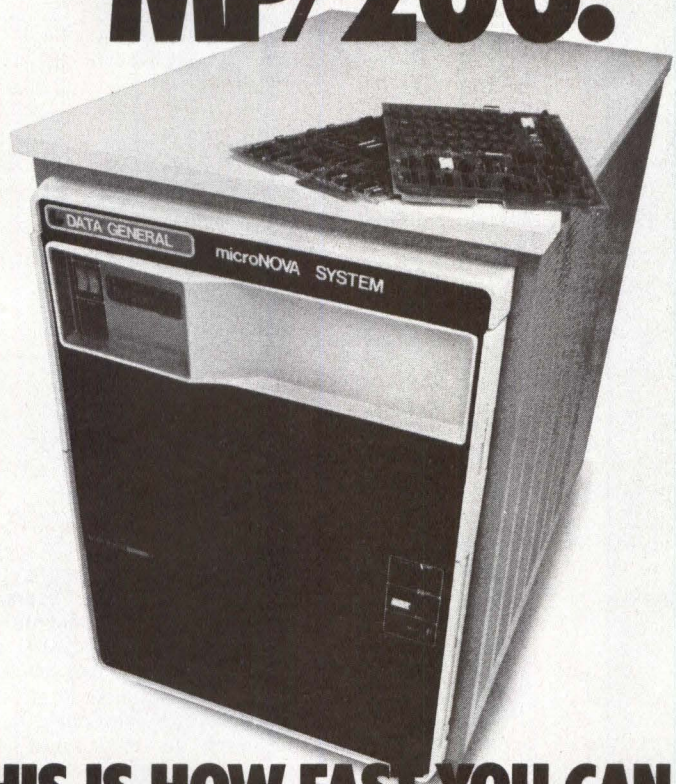
Available at chip, board or box level, the MP/100 is based on the new Data General designed and manufactured 16-bit mN602 NMOS microprocessor. This is where the true functionality begins. Our single, 40-pin package includes the full NOVA® 16-bit architecture and multifunction instruction set, hardware stack and frame pointer, 16-bit multiply and divide, realtime clock, multiple addressing modes, standard and high-speed data channels (2M byte/sec), 16-level priority interrupt and dynamic RAM refresh. It's capable of supporting up to 64KB of RAM/PROM/EPROM memory in standard application and up to 128KB in special application requiring additional memory.

The MP/100 gives you the mN602 microprocessor, an asynchronous interface with full modem control, automatic program load, power/monitor/auto restart and soft control panel all on a single 7½" x 9½" board.

All microNOVA computers are available in a compact, modular 5¼" eight-slot chassis featuring a single board power supply for increased reliability and maintainability. Plus a low cost four-slot card cage for product OEMs.

Our new 16-bit microNOVA MP/100. It can take you a long way on a small amount of money. Most important, the MP/100 is not only compatible with other members of the microNOVA family but also within the entire Data General family of NOVA and ECLIPSE computers. It's a smart way to grow.

ANNOUNCING THE HIGH PERFORMANCE 16-BIT MICROCOMPUTER, MP/200.



THIS IS HOW FAST YOU CAN GO.

Speed and performance. These are the two features that give you the power of a mini in a 16-bit microcomputer. Our new microNOVA® MP/200 is the highest performance microcomputer in the marketplace.

Offering the flexibility of product line integration at multiple levels – board, box or fully packaged system – the MP/200 features fast instruction execution times with an 0.84 microsecond ADD and a full 16-bit hardware multiply in 4.9 microseconds. Standard and high-speed data channel (DMA) provides input/output data rates of up to 3.7M bytes/second. An enhanced NOVA® instruction set featuring byte operations as well signed and unsigned integer Multiply/Divide add to the MP/200's power.

The MP/200 is completely compatible with the MP/100 which means that all peripherals and interfaces are interchangeable. And the MP/100 and MP/200 feature the industry's broadest range of compatible field-proven software for program development and execution. Including disc and real-time operating systems and high level languages such as Business BASIC, Extended BASIC and FORTRAN IV.

Function and economy. Or, high performance. Whichever your need, you'll find the best, cost-effective answer in the MP/100 or MP/200 16-bit microNOVAs from Data General. The right fit for today with the growth for tomorrow. Send the coupon for complete information. And fast. Or call 800-225-7282 or contact your nearest Schweber or Hall-Mark distributor.

MAIL TO: microNOVA PRODUCT INFORMATION
DATA GENERAL CORPORATION
WESTBORO, MA 01581

Name_____

Title_____

Company_____ Tel No._____

Address_____

City_____ State_____ Zip_____

Data General Corporation, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario, Canada. Data General Europe, 61 rue de Courcelles, Paris, France, 766.51.78. Data General Australia, (03) 89-0633. Data General Ltda., Costa Rica, Latin America, 22-79-42. Data General Middle East, Athens, Greece, 952-0557.

CD 479

Data General

We make computers that make sense.

Microprocessor I/O Module Systems Interface With 5-V Logic Units

Four optically coupled, color coded modules and four PC module boards (4, 8, 16, or 24 positions) comprise an I/O module system with industry standard pin configuration. Gordos Arkansas, Inc, 1000 N Second St, Rogers, AR 72756 has designed the systems to interface with 5-V CMOS, TTL, NMOS, or PMOS units. Two output modules (ac or dc) drive a 3-A load, while two input modules (ac or dc) translate their respective load inputs into standard logic levels.

The 8-, 16-, and 24-position module boards have plug compatible logic contacts, while the 4-position board has screw terminal logic connections. All boards feature a barrier strip with screw terminals for load connections, circuitry for pull-up resistors, 5-A field replaceable fuses, LED status indicators, and color coded position indicators. Since the function is self-contained in each module, the user can determine system board layout.

Circle 415 on Inquiry Card

System Teaches µComputer Programming, Interfacing, and Fundamentals

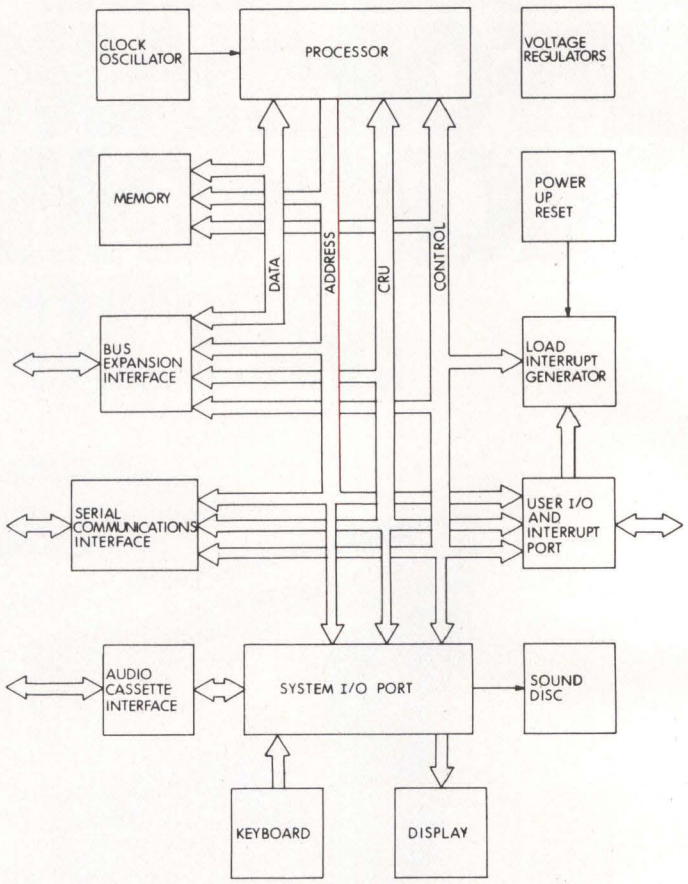
Demonstrating TMS 9900 family applications and advantages, the TM990/189M single-board microcomputer system is a learning aid for instruction of microcomputer fundamentals, interfacing, and assembly and machine language programming. The self-contained board has a TMS 9980A microprocessor, 1k bytes of RAM (expandable onboard to 2k), and 4k bytes of ROM (expandable onboard to 6k). The ROM contains the system monitor (UNIBUG) which sets the baud rates to 110, 150, or 300, and a symbolic assembler. Other features are a 2-MHz crystal controlled clock, 16-bit programmable I/O port and interrupt monitor, and single-step instruction execution.

Mass memory storage is achieved via the audio cassette interface. Texas Instruments, Inc, Semiconductor Group, PO Box 1443, Houston, TX 77001 has built in a 45-key alphanumeric keyboard and 10-digit, 7-segment display with 32-character buffer. It displays data, instructions, and error messages, and may be shifted right or left to view any 10 digits of the buffer. A standard EIA terminal or TTY interface may be added externally.

Other system expansion options are available. A TMS 9902 asynchronous communications controller and accompanying interface circuits for RS-232-C or 20-mA current loop terminals can be added. Also the bus can be expanded using the bus interface. A suitable power supply is available as an option.

A series of visual addressable LEDs is coupled with a piezoelectric speaker for audio signals. When the microcomputer is powered up, four LEDs flash, the speaker beeps, and the display signals "CPU ready." This not only clears the sysetm, but also serves for self-diagnosis. Other LEDs signal the status of the audio cassette when the CPU is in idle and when the keyboard is in shifted mode. The microcomputer board, punched for insertion in a 3-ring binder, costs $299, with user's guide and applications textbook.

Circle 416 on Inquiry Card



System architecture along with user options for Texas Instrument TM 990/189M. Learning aid gives users hands-on experience of microcomputer basics. Components are TMS 9980A microprocessor, 1k of RAM, 4k of ROM, 2-MHz crystal controlled clock, 16-bit I/O port, 45-key keyboard, 10-digit alphanumeric display, and visual and acoustic indicators. Bus, serial communications, and audio cassette interfaces handle system expansion options offered in addition to onboard memory expansion

The Panasonic Dream Machine.

Selecting the right microcomputer for your product is tricky business. There are so many variables. Like the technology. What's available to fit your design requirements? With how many on-chip functions? How many instructions? How fast? How much memory?

Now there's one family of microcomputers with all the right answers. The Panasonic 4-bit MN1400 series.

Three technologies

Panasonic MN1400's are available as C-MOS, P-MOS and N-MOS to fit your specific design requirements. You can fit the right chip to your design.

	Model	Package	On Chip Memory	
			Instruction ROM	Data RAM
N-MOS	MN1400	40 Pin DIP/Plastic	1024 x 8 bits	64 x 4 bits
	MN1402	28 Pin DIP/Plastic	768 x 8 bits	32 x 4 bits
	MN1403	18 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
	MN1404	16 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
	MN1405	40 Pin DIP/Plastic	2048 x 8 bits	128 x 4 bits
	MN1498	40 Pin DIP/Plastic	External	64 x 4 bits
P-MOS	MN1430	40 Pin DIP/Plastic	1024 x 8 bits	64 x 4 bits
	MN1432	28 Pin DIP/Plastic	768 x 8 bits	32 x 4 bits
	MN1435	40 Pin DIP/Plastic	2048 x 8 bits	128 x 4 bits
C-MOS	MN1450	40 Pin DIP/Plastic	1024 x 8 bits	64 x 4 bits
	MN1453	18 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
	MN1454	16 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
	MN1455	40 Pin DIP/Plastic	2048 x 8 bits	128 x 4 bits

Varying computing power

The 12-strong MN1400 microcomputer family offers devices with varying amounts of computing power, so you can choose the chip that meets your specific requirements. And even if your memory needs change, you can substitute another model within the family and save your basic design. You pay only for the computing power you need.

They're all on the chip

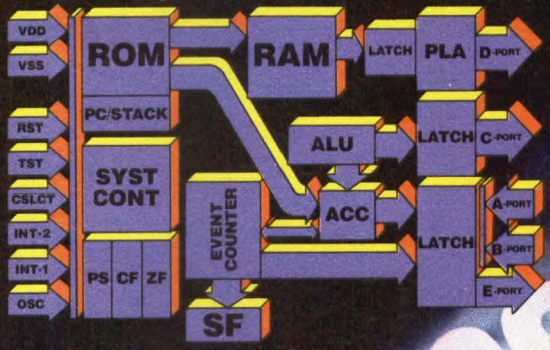
We put all these microcomputer functions on a single chip:

- ALU
- Up to 16,384 (2048 x 8) bit ROM
- Up to 512 bits (128 x 4) RAM
- Two 4-bit parallel input ports
- 4-bit parallel output port
- 8-bit output port with PLA
- With 12 discrete output lines
- 8-bit counter/timer
- Clock generator

Add to that the fast 10μs instruction speed and a powerful instruction set with up to 75 versatile instructions that let you computerize a variety of end products with ease.

And you needn't stop with design. Panasonic takes you from concept through production with software and hardware development tools: cross-assemblers, edit software and debugging and prototyping hardware, and, of course, fast turnaround in mask preparation.

So if on-chip capability has been giving you sleepless nights, take the Panasonic cure. For complete information and prices write to Panasonic Electronic Components, One Panasonic Way, Secaucus, NJ 07094; or call (201) 348-7269.

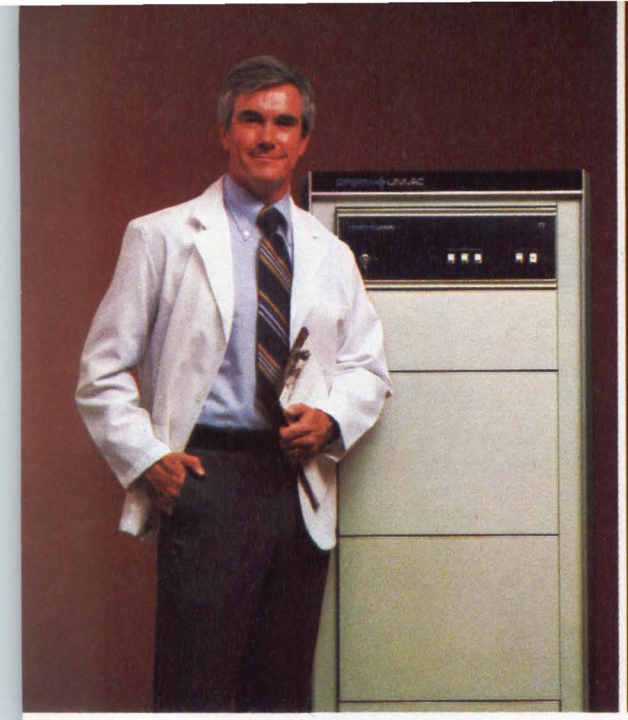


PMOS CMOS NMOS

The 4-bit microcomputer with three technologies and varying computing power

Panasonic®
just slightly ahead of our time

CIRCLE 69 ON INQUIRY CARD



Introducing the Sperry
Designed exclusively for three

The Sperry Univac V77-800 Miniframe is the newest and most powerful mini we've ever built—a high performance, multi-use, general-purpose minicomputer system designed for both commercial and scientific data processing. It has a memory range from 128K bytes to 2 megabytes (with error correcting memory) and a 150 nanosecond CPU with integrated cache of 1024 bytes. Plus 12K bytes of user programmable writable control store.

There's an optional new high speed 64-bit floating point processor that works in conjunction with a new globally optimized ANS '77 FORTRAN.

No wonder our three most important customers think so highly of it.

OUR OEM CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

The Miniframe is customer microprogrammable. So an OEM can implement his own firmware packages. And with the many software packages we offer, the OEM can add all the bells and whistles he wants.

The Miniframe comes with our largest instruction set ever. So OEM's with their own software have much more flexibility in design.

The Miniframe speaks PASCAL, the powerful new language for scientific, commercial, and system programming that most competitive systems still can't speak. And of course, it also speaks COBOL, FORTRAN and RPGII.

More good news is that the Miniframe is compatible with the rest of the V77 product line.

OUR SYSTEM HOUSE CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Naturally, system houses want all the features OEM's do. And more.

So we gave them more.

More operating systems, for example. Choose from VORTEX or our new SUMMIT—an interactive, multi-terminal system with transaction processing and data base management. It gives you easy editing, screen formatting, and documentation aids. Plus speedy, comprehensive program development.

System houses also think PASCAL is important. Because it's more efficient, easier to maintain, expand, and modify.

The Miniframe brings systems builders a new query language called QL-77. It features inquire and report facilities. And interfaces

Univac V77-800 Miniframe. of our very best customers.

directly to TOTAL,* the data base management system. So preprocessing and intermediate handling are a thing of the past. Finally, TOTAL also gives you complete data base access and file access security.

OUR END USER CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Take all the features we designed in for OEM's and system houses and say ditto for the end user.

But we didn't stop there. We also pressed a few special hot buttons just for end users.

Consider QL-77, for example. End users will love our new query language because it reduces the amount of application programming. By storing query language procedures right in the data base file. Where they can be easily and quickly recalled and executed at any time.

Once again, SUMMIT, our new operating system, helps the end user handle transaction processing. Without any additional, expensive software. It's also the right answer for a multi-tasking, "fully-implemented" distributed processing system.

Finally, the Miniframe supports DCA and conventional protocols. So you can talk to both SPERRY UNIVAC and IBM hosts.

YOU'LL KNOW WE DESIGNED THE MINIFRAME JUST FOR YOU.

No matter what your application, no matter what your need, the Miniframe may just be the answer.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, ext. 536.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

We're Sperry Univac.

And our new Miniframe is going to solve some very big problems.

SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORPORATION

*TOTAL is a registered trademark of Cincom, Inc.

CIRCLE 70 ON INQUIRY CARD

Floppy Disc System With 4-Drive Controller Speeds Data Storage

The MD-X floppy minidisc subsystem is available from Imsai Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577. Featuring a DIO-D disc controller, two or four single/double-density 5.25″ (13.3-cm) floppy minidisc drives, power supplies, fans, and cables, MD-2 stores 800k bytes and MD-4 stores 1560k bytes. System configurations are based on 40-track MPI or 77-track Micropolis minidisc drives. Each controller supports up to four drives of the same type on the company's 8080 and 8085 based computers. Models MD-2E and -4E are dual drive expansion units for MD-2 and -4, as well as for the company's minidisc based computers.

These two systems contain the IMDOS multidisc operating system, which simultaneously supports minidisc drives and standard 8″ (20.3-cm) drives. On systems with the company's hard disc unit, a version of the operating system supports mini and standard floppy disc drives as well as hard disc. Utilities are an 8080/8085 assembler, video/context editor, dynamic software debugging program, and diagnostic program.

Model MD-2 and -2E dual drives provide 180k bytes of online storage in single density. In double density, the user may specify 17 sectors/track at 256 bytes/sector for 344k bytes or 5 sectors/track at 1024 bytes/sector for 400k bytes. Dual-drive models MD-4 and -4E provide 354k bytes in single density. In double density, either 17 sectors/track at 256 bytes/sector for 660k bytes or 5 sectors/track at 1024 bytes/sector for 780k bytes of online storage may be specified.

Transfer rates for all models are 125k bits/s single density and 250k bits/s double density. Recording techniques for these respective densities are FM and MFM. Each unit includes two power supplies, 5 Vdc rated at 3 A and 12 Vdc rated at 3.4 A.

All models utilize two minidisc drives in a desktop cabinet. Prices are $1395 for model MD-2, $1995 for MD-4, $995 for MD-2E, and $1495 for MD-4E.

Circle 417 on Inquiry Card

Converter Functions As Interface for Bus/Controller Interaction

The RTP family of 16-bit analog and digital I/O measurement and control subsystems connect to Motorola 6800 Micromodules and EXORciser development systems via the plug-in RTP 7410/73 I/O bus converter that performs the necessary interface function. Up to eight controllers, attached to one converter in chain fashion using RTP I/O cables, are operated in either programmed I/O or interrupt-driven modes by the 6800 CPU.

The bus converter and attached controller registers are addressed as memory locations. Each converter uses a block of 64 memory addresses which provides a minimum of 4 memory addresses for each attached RTP device and 4 addresses for the bus converter itself. The converter is transparent to CPU instructions addressing the subsystems.

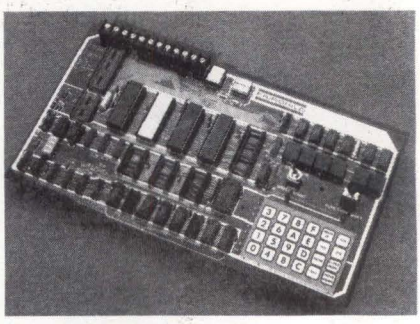
Computer Products, Inc, 1400 NW 70th St, Fort Lauderdale, FL 33307 developed the bus converter with logic to perform byte to word and word to byte conversions, and to inhibit RTP interrupts between the transfers of the two bytes. Price of the converter and termination card is $350.

Circle 418 on Inquiry Card

Course Gives Hands-On Training With Take-Home Microcomputer Board

Systems designers attending a 4-day F3870 and F8 training course are offered the single-board 387X PEP microcomputer system, which serves as a prototyping, emulating, and programming design aid for systems based on standard F3870, F3872, F3874, or F3876 devices. A built-in option allows programming of operating codes either into the F38E70 or into 2716 EPROMS.

Course objective is to familiarize users with the 3870 architecture and instruction set. Attendees practice program development on a disc based F8 system, editing, assembling, and debugging programs. The F3870 is emulated with the Formulator design aid through an umbilical cord; the



PEP system for prototyping, emulating, and programming F387X single-chip microcomputer family is featured in hands-on training course with laboratory sessions, sponsored by Fairchild

PEP system performs emulation by downloading a program that is developed with a cross assembler or development system.

Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042 has priced the course, offered in Mountain View, Calif, at $500 ($400 without the PEP board). Other courses cover the F6800, 9400 Macrologic and 2900 bit-slice families, and 9440 Microflame 16-bit microprocessor family.

Circle 419 on Inquiry Card

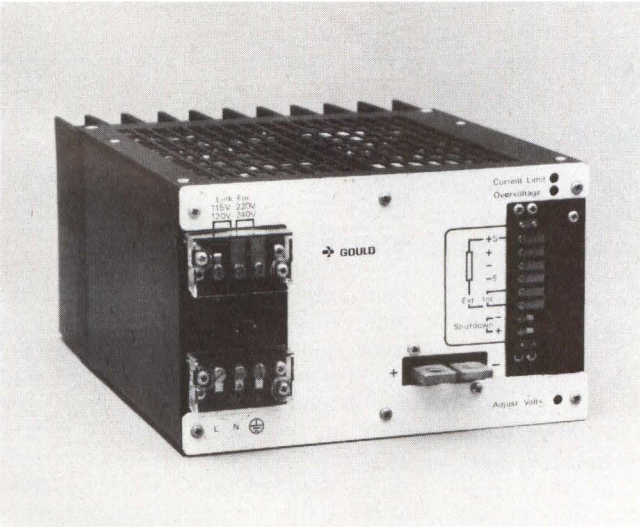
Computer Couples With Controller Interface For Industrial Uses

Operating on the S-100 bus, the Z80 based SBC-100 board contains 1k bytes of onboard RAM, 8k bytes of P/ROM (using 2716), serial I/O with asynchronous and synchronous operation, 8-bit parallel I/O plus handshaking, 4-channel counter/timer, and software programmable baud rate generator. This saves on complicated system modifications and adds flexibility. Coupling with a controller interface creates a control unit for industrial applications. Vectored interrupts are optional, using the Z80-CTC if needed to prioritize interrupts. The counter/timer circuit contains four independent 16-bit counters for use as "divide by" blocks for time delays or as event counters. External interrupts may be prioritized with CTC interrupts, creating an interrupt daisy chain between boards in the system.

(Continued on p 158)

The big switch

...is to full cycle holdup.



The 500 watt MG5-100: 28 millisecond holdup.

Switching power supplies offer substantial holdup. Linears don't.

A Gould switcher will give you full regulated output at −20% line. Or during complete loss of power you'll get full output power for more than a missing line cycle.

Switchers offer other benefits too. They're 1/3 the size and 1/4 the weight of linears.

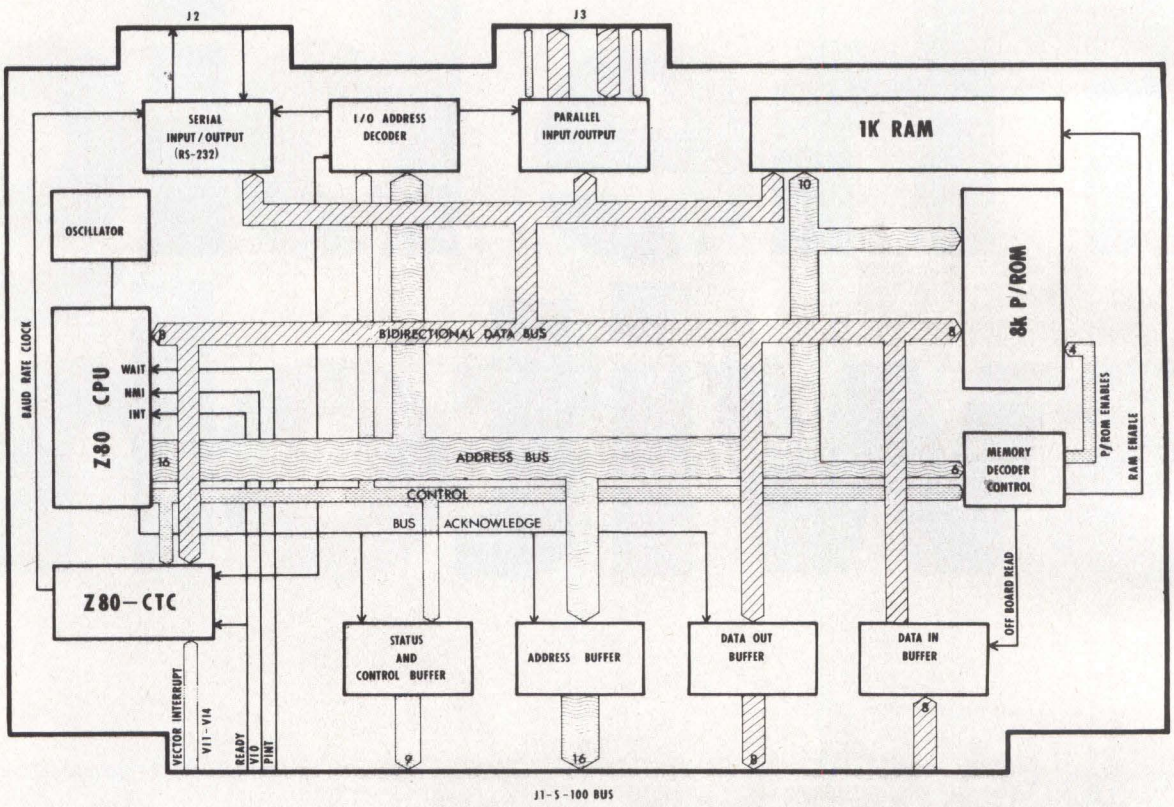
And they save energy with efficiencies of up to 85%.

Gould offers single and multiple output switchers with power levels from 8 to 2,250 watts. Custom designs can be provided to meet your exact specifications. You'll be backed by a high volume production capability and worldwide service network that only a $1.6 billion company like Gould could offer.

For more information or to arrange for an evaluation unit, contact Gould Inc., Electronic Power Supply Division, P.O. Box 6050, El Monte, CA 91731. Phone (213) 575-4777.

Gould.
The power in switching power supplies.

GOULD



Operating on S-100 bus, SBC-100 single-board microcomputer is designed around Z80 microprocessor. Features illustrated in diagram enable board's use in industrial, machine, and process control applications

SD Systems, a div of SD Sales Co, PO Box 28810, Dallas, TX 75228 has designed the single-board microcomputer to operate without a front panel. It costs $229 in kit form and $369 assembled. Other functional components are the crystal controlled oscillator, status and control buffer to drive S-100 bus signals, a 16-bit latch/address buffer, and data out and in buffers. The I/O address decode block decodes the low order eight bits of address to determine ports accessed during I/O instructions. Memory decode and control decodes the high order address bits and selects the addressed RAM or ROM-P/ROM: this block also generates the offboard signal used in controlling the data in buffer. Sockets hold up to four ROMs or P/ROMs each containing 1k, 2k, 4k, or 8k bytes, and can be strapped for any area of memory, as can the 1k-byte RAM.

Combinations with the Versafloppy disc drive controller, VDB-8024 video display board, and ExpandoRAM (up to 64k) are possible to build a data processing system. An RS-232 serial interface connects serial peripherals for online operation.

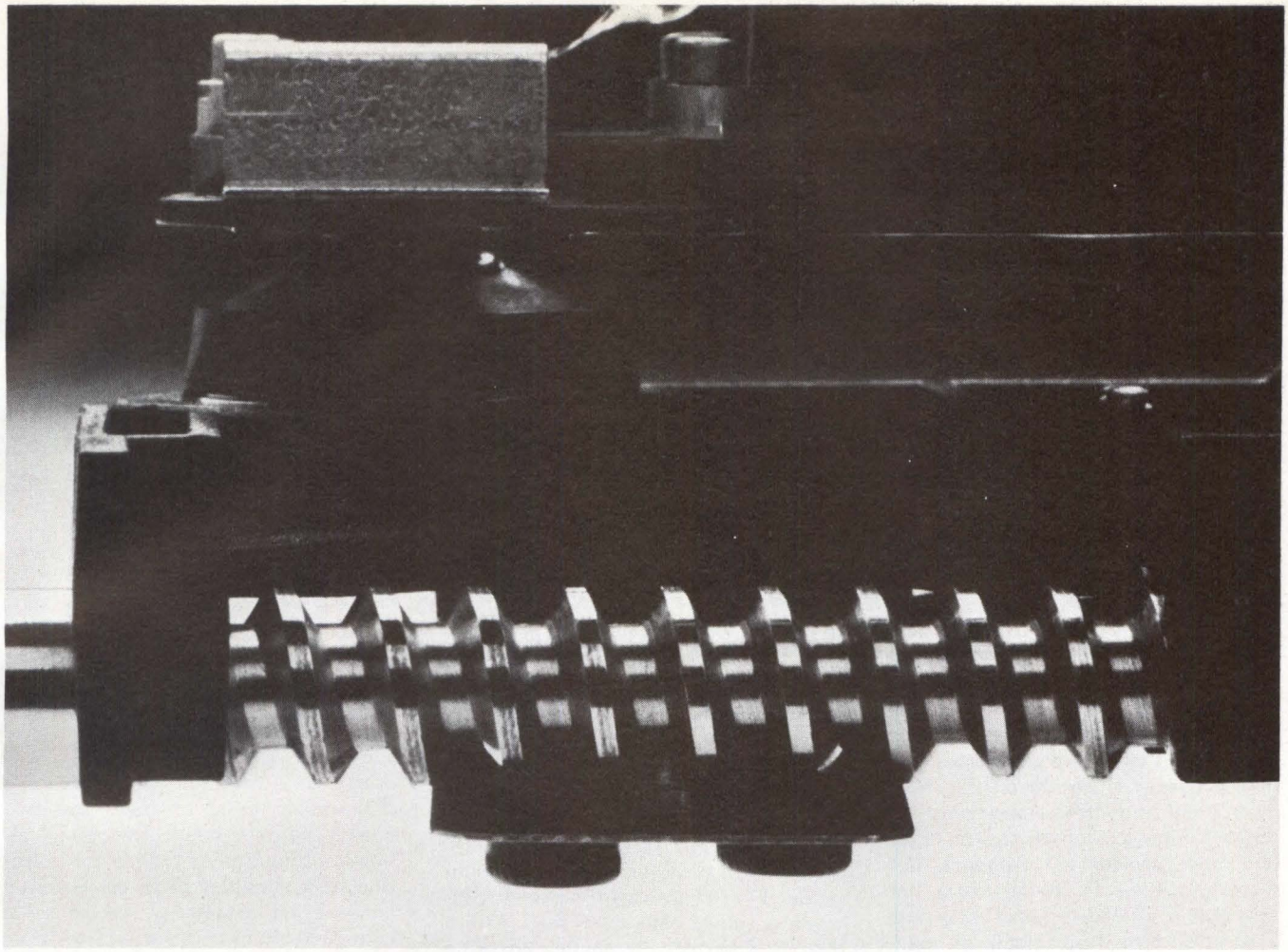
The Versafloppy, featuring S-100 bus compatibility, is designed for Z80, 8080, and 8085 CPUs. Highlights are IBM 3740 single-density soft-sectored format providing 256k bytes of storage on a single side of an 8″ (20-cm) diskette and over 80k bytes/side of a 5″ (13-cm) mini-diskette, double-sided operation, control of up to four drives, optional interrupt operation, and control and diagnostic software in P/ROM. It operates with modified CP/M™ disc operating systems.

Circle 420 on Inquiry Card

Multilevel Microcomputer Systems Provide Range of Color Graphics

Four microcomputer systems provide different levels of capability ranging from small business systems to deluxe systems with color graphics and lightpen. Two Series I business systems are equipped with an 8080A microprocessor, 19″ (48-cm) CRT with eight colors foreground and background, 48 lines x 80 characters, a 60-character/s impact matrix printer, and capabilities of upper/lower case, insert/delete—character/line, and page roll. A separate keyboard with standard ASCII characters contains cursor, color, and numeric cluster pads.

The two differ in their mass storage devices. Intecolor 8070 has a



EVERYONE WHO STILL USES A PLASTIC POSITIONER DESERVES A METAL.

At Micropolis, we've always done things the best way we know how. Even though it may be harder, and cost a little more.

For instance, we offer as much storage capacity in our 5¼-inch MegaFloppy™ disk drives as others offer in larger 8-inch models.

We do it by increasing the track density of our MegaFloppy drives to 100 tracks per inch. That lets us record 77 tracks – as many as on 8-inch 48 TPI drives. This configuration gives us a capacity of up to 946K bytes per drive.

Here's how our double track density works.

While most floppy drives use a cheap, less accurate plastic cam or cam follower to position the read/write head, we use a stainless steel, precision-ground lead screw. Because it helps us achieve high-track storage capacity with lower cost per thousand bytes. And significantly increases reliability.

The lead screw is coupled to the head carriage using a zero backlash, leaf-spring loaded ball. Whose diameter is large enough to contact both lead screw side walls. So ball and screw wear don't lead to loss of positioning accuracy.

A 7.5° 4 phase permanent magnet stepper motor activates the lead screw so that each step command causes the motor to increment 4 "mini steps" equal to one track movement. This reduces stepper motor inaccuracies and friction effects by the ratio 4:1.

Then there's our disk hub design and single point referencing of lead screw to disk hub. Which ensures that, over the full temperature and humidity range, reliable interchange of diskettes between drives is a routine affair. (Patents applied for).

MICROPOLIS™

Where the 5¼-inch drive grew up.

Maybe all this is why people are beginning to realize just how good our drives really are. Because they've made us Number 2 in the marketplace, with over 20,000 units shipped.

So remember our MegaFloppy disk drives the next time you're thinking about floppies. And forget about the ones you're using now.

After all, why settle for plastic when you can have Micropolis?

For a descriptive brochure, in the U.S. call or write Micropolis Corporation, 7959 Deering Avenue, Canoga Park, California 91304. Phone (213) 703-1121. Or, better yet, see your local representative.

CIRCLE 72 ON INQUIRY CARD

590k-byte dual 8″ (20-cm) floppy disc drive, while the 8071 has an 1180k-byte dual double-headed 8″ (20-cm) floppy disc drive. Both use the company's Sof-Disk media and include 5k ROM operating system software (FCS) and disc I/O controller.

Memory consists of 16k of RAM and 17k of ROM. The screen uses 8k of RAM for refresh and 8k for user workspace. Memory expands to 24k of RAM workspace and 15k bytes of EPROM software. Business BASIC, a more powerful ROM BASIC Interpreter, is standard. Options are lightpen, text editor, assembler, graphics plot hardware, and extended graphics software. Prices begin at $7000 for the 8070 and $7800 for the 8071 in quantities of 1 to 24.

Intelligent Systems Corp, 5965 Peachtree Corners E, Norcross, GA 30071 has also introduced the Intecolor 8080 and 8090 standalone systems. Common to both are an Intel 8080 CPU, 8-color 19″ (48-cm) data display, 48-line x 80-character/line format, an RS-232-C serial I/O port, and editing features such as page roll and insert/delete—character/line. Also standard are a 110-character/s bidirectional impact matrix printer and a 2708/2716 EPROM programmer. The separate ASCII keyboards contain eight color keys and 16-key numeric cluster, along with function/control keys.

Both come with a ROM assembler and SCROLLing Editor. The editor facilitates generation and correction of user source programs and documents. Featuring a backwards search command, SCROLL allows the user to move from one end of a text file to another. Positioning of the window display of 20 lines is handled by both direct cursor commands and "command mode" commands.

The 8080 development system has external dual minidisc drive with 160k bytes of data storage, and memory consisting of 16k bytes of RAM (8k screen refresh and scratchpad; 8k user workspace) and 17k bytes of ROM; 16k bytes of RAM workspace and 15k bytes of special EPROM software can be added. Options include a lightpen, graphics plot hardware, expanded graphics software, and Microsoft FORTRAN IV compiler. Price is $6500 in 1 to 9 quantities.

Variations of the 8090 deluxe system include 32k bytes of RAM (8k for refresh and scratchpad, 24k for workspace) and 17k bytes of ROM; a dual 8″ (20-cm) double-headed disc drive supplies media storage up to 1182k bytes; and graphics plot hardware and expanded graphics software. A lightpen detects cursor coordinates, transmits X-Y coordinates, and positions the cursor to that point. The system costs $12,000 in quantities of 1 to 9.

Circle 421 on Inquiry Card

Bus Controller Allows Addition of Mag Tape for Storage and Transfer

The 3000 series provides users of Intel SBC 80 or MDS 800 Multibus™ systems with a means of adding an IBM, ANSI compatible 0.5″ (1.3-cm) magnetic tape system. Electrically, physically, and logically matched to the Intel family of single-board computers, the system's asynchronous parallel I/O processor (GPIB controller) plugs into any Intel Multibus. Systems can be configured using up to two formatters and up to four tape transports, providing 7 or 9 tracks with densities up to 1600 bytes/in (630/cm).

High level interface commands and data from the intelligent controller are transferred via the GPIB. From this bus, a dedicated microprocessor performs all programming, formatting, and error detection functions. The inclusion of a GPIB controller to a Multibus system permits other peripherals and instruments to be added. Included in the rackmount or standalone system by Dylon Corp, 3670 Ruffin Rd, San Diego, CA 92123 are dual 2048-byte buffers, read-after-write error checking with automatic correction, and over 30M bytes of data storage with a single drive.

Circle 422 on Inquiry Card

Single Board Combines Analog Input and Output Functions

RTI-1250 series covers 12-bit input, input/output, and output boards that plug into the LSI-11/2 card cage. All feature a dc-dc converter and selection of input ranges and operating modes by wirewrap methods.

Manufactured by Analog Devices, Inc, PO Box 280, Norwood, MA 02062, RTI-1250 is the input-only board with 32 single-ended (16 differential) protected input channels. The software programmable gain amplifier (RTI-1250-S) can provide gains of 1, 2, 4, or 8 under program control, or the resistor programmable gain model (1250-R) can give full-scale input ranges from 10 mV to 10 V. Also included are a sample/hold amplifier for acquisition of fast slewing signals in real time, and autoincrement of the multiplexer to the next channel following a convert command. Other software commands allow mixing of sequential scanning and random channel addressing. External trigger, interrupt, and polled status modes are available.

RTI-1251 has 16 single-ended (8 differential) input channels and two analog outputs which are 12-bit 4-quadrant multiplying DACs for selection of a variable reference. External load-sensing capability prevents IR voltage losses in long output lines from degrading overall accuracy and calibration.

With two to four D-A output channels plus four high current digital logic drivers and an onboard dc-dc converter, RTI-1252 output-only board is user expandable. A 2-channel board can be purchased to expand to three or four channels by plugging in standard DAC-80 D-A converters. Also offered are optional 4- to 20-mA current loop outputs.

Circle 423 on Inquiry Card

Serial Communications Board Features Eight Independent Channels

Designed for EIA RS-232-C voltage levels as well as current loop interfacing, the 8-channel serial I/O communications board is compatible with Series/80 Multibus™ boards with up to eight asynchronous/synchronous serial data ports. Software defined standard baud rates range from 50 to 9600 with individually programmable USARTS for user defined formats and protocols.

Eight independent channels conform to EIA RS-232-C standards, with

Thinking Systems?

Think of the Possibilities – A Complete Computer for $1275!*

All You Do Is Add The Terminal, Printer, And Applications Software — And You've Got A Complete System!

The Horizon is a complete computer — Z80, 16K RAM, Disk and I/O — priced so that the only limit to application in your system is your imagination! And, the Horizon is packaged in a natural wood cover, adding sales appeal to your system! Think of the possibilities if you're designing a system for education, small business, process control, word processing, engineering, or whatever is on your mind.

Over 10,000 North Star Systems In Use!

We offer you the maturity and reliability to meet the needs of demanding, high-volume applications. Horizon performance and reliability are assured through the use of the proven Z80A microprocessor and industry standard 5¼" 180K byte disk drives. Our professional approach to design (for example, a memory parity option) has been proven in thousands of installations.

North Star Horizon Specifications:

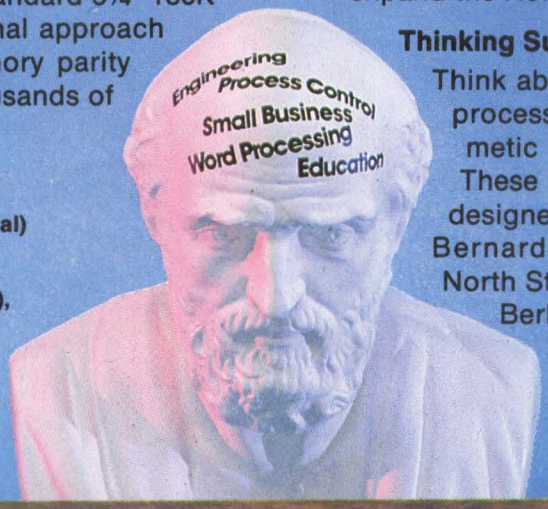
CPU:	4 mhz Z80A
RAM:	200ns (parity check optional)
Bus:	12 slot, S-100
Disk:	180K bytes per diskette
Controller:	Up to 4 drives (720K bytes), 250 KB transfer rate
Cover:	Natural Wood or Blue Metal, no charge

Complete Software Support: DOS, BASIC, and MONITOR!

We provide you with the tools (system software) for writing the application programs that will make your system work! Our BASIC is a *full* extended disk BASIC! Hundreds of commercial software application packages have been developed using North Star BASIC. Additionally, a wide selection of application software for the Horizon is available from independent vendors.

Expand Your Horizon!

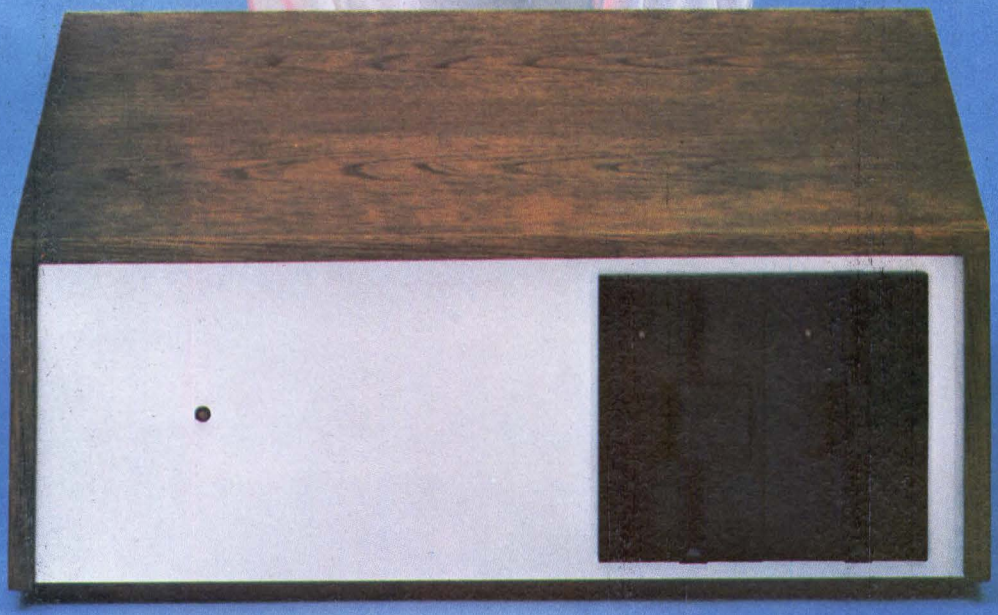
The Horizon can be expanded to 56K bytes or more of RAM, four disk drives (720K bytes), and three built-in I/O interfaces. Performance can be enhanced by the addition of the North Star hardware floating point board. Also, S-100 bus products from other manufacturers may be used to expand the Horizon.



Thinking Sub–Systems Only?

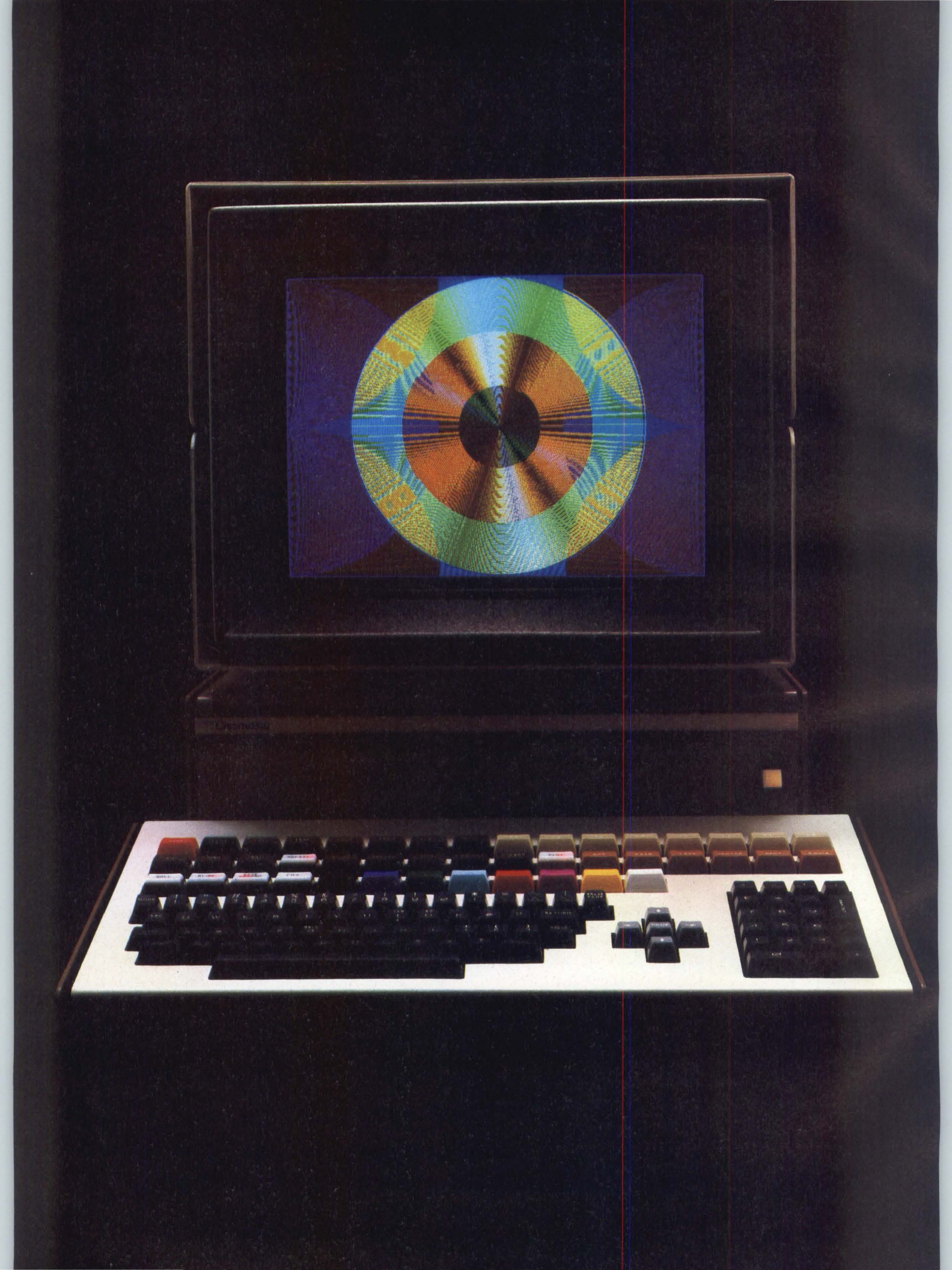
Think about North Star's memories, Z80A processor boards, floating point arithmetic boards, and disk drive systems. These are available for the OEM system designer. For complete information call Bernard Silverman at (415) 549-0858. North Star Computers, 2547 Ninth Street, Berkeley, California 94710.

NorthStar



CIRCLE 73 ON INQUIRY CARD

*In OEM quantities of 100 or more.



HERE'S AN INCREDIBLY BRIGHT IDEA FOR YOUR NEXT SYSTEM.

At Chromatics, one of our most important corporate goals is to stay ahead of our competition—with more innovations, more reliable products and more personalized service.

The result of our efforts is the CG SERIES of color graphic computers that start at $5995 for a complete usable system with color monitor.

Enter your artwork and graphics quickly with our X-Y digitizer tablet and store them on our floppy disk peripherals. Analyze and operate on your results with our Microsoft® Z-80 BASIC software and our graphics packages.

Viewability is enhanced with our multi-hue pattern fill routines, and the operator can Zoom in on the fine detail of a 512 by 512 high resolution color screen. And, for a permanent full-color record, you can even output the final results to a Xerox® 6500 color copier with our color hard copy interface.

In addition, our unified approach creates a powerful Z-80 development system with Assembler, Text Editor and Disk Operating System with operation in full color.

We're so confident of our color graphic computers that we back them with a full year's warranty instead of the usual ninety days or six months. If you should have a problem, we have a strict policy of giving customers the fastest possible turn-around time on repair service.

Watch out for us. We're determined to meet our corporate goal of staying out in front of everybody else. Way out in front.

Chromatics, Inc., 3923 Oakcliff Industrial Court, Atlanta, Georgia 30340; tel: 404/447-8797; TWX: 810/766-4516.

Chromatics™
The World's Most Colorful Computer Company.

Sales Representatives
USA
Alabama: Huntsville
Col-Ins-Co. 800/327-6600
Arizona: Phoenix
Thorson Co. 602/956-5300
California
Graphics Marketing Corp. 213/880-4062
Colorado: Denver
Thorson Co. 303/759-0809
Connecticut
Bartlett Associates 914/949-6476
Delaware
Bartlett Associates 301/656-3061
District of Columbia
Bartlett Associates 301/656-3061
Florida: Ft. Lauderdale
Col-Ins-Co. 800/432-4480
Florida: Orlando
Col-Ins-Co. Inside Fla. 800/432-4480
Local 305/423-7615
Georgia: Atlanta
Col-Ins-Co. 800/327-6600
Hawaii: Honolulu
Thorson Co. 808/524-8634
Illinois
Resource Data Systems 312/564-5440
Indiana
Resource Data Systems 312/564-5440
Iowa (Eastern)
Resource Data Systems 312/564-5440
Iowa (Western)
Professional Marketing Services 612/474-5939
Louisiana: Baton Rouge
Col-Ins-Co. 800/327-6600
Maine
Bartlett Associates 617/879-7530
Maryland: Bethesda
Bartlett Associates 301/656-3061
Massachusetts: Framingham
Bartlett Associates 617/879-7530
Michigan: Detroit
WKM Associates 313/588-2300
Minnesota
Professional Marketing Services 612/474-5939
New Hampshire
Bartlett Associates 617/879-7530
New Jersey:
Bartlett Associates 914/949-6476
New Mexico: Albuquerque
Thorson Co. 505/265-5655
New York: Holcomb
Bartlett Associates 716/657-6309
New York: White Plains
Bartlett Associates 914/949-6476
North Carolina: Winston-Salem
Col-Ins-Co. 800/327-6600
Ohio: Cleveland
WKM Associates 216/267-0445
Ohio: Dayton
WKM Associates 513/434-7500
Oregon: Portland
Graphics Marketing Corp. 213/880-4062
Pennsylvania: Pittsburgh
WKM Associates 412/892-2953
Pennsylvania: Wayne
Bartlett Associates 215/688-7325
Rhode Island
Bartlett Associates 617/879-7530
South Carolina: Greenville
Col-Ins-Co. 800/327-6600
Texas: Austin
Thorson Co. 512/451-7527
Texas: Dallas
Thorson Co. 214/233-5744
Texas: Houston
Thorson Co. 713/771-3504
Utah: Salt Lake City
Thorson Co. 801/973-7969
Vermont
Bartlett Associates 617/879-7530
Virginia (Northern)
Bartlett Associates 301/656-3061
Virginia (Southern)
Col-Ins-Co. 800/327-6600
Washington: Seattle
Graphics Marketing Corp. 213/880-4062
Wisconsin
Resource Data Systems 312/564-5440
Any other states
404/447-8797
Europe & Near East
Techexport, Inc. 617/661-9424
Far East
Computers International 213/382-1107

FOREIGN COUNTRIES

Australia: Crows Nest, NSW
TCG 439-6477
France
Techdata 749-40-37
Japan: Tokyo
Computers International Japan 03/402-8596
Scandinavia: Sweden
Teleinstrument AB 08-380-370
South Africa: Pretoria
Infodata Pty. Ltd. 01278-8141
Switzerland
W. Stolz AG 057-54655
United Kingdom: Bournemouth
Techex Ltd. 0202-293-115
Belgium: Brussels
Spesi (02) 37491-12

CIRCLE 74 ON INQUIRY CARD

A Beautiful Way To Interface

IQ 140

SOROC's first and foremost concern, to design outstanding remote video displays, has resulted in the development of the IQ 140. This unit reflects exquisite appearance and performance capabilities unequaled by others on the market.

With the IQ 140, the operator is given full command over data being processed by means of a wide variety of edit, video, and mode control keys, etc.

The detachable keyboard, with its complement of 117 keys, is logically arranged into 6 sections plus main keyboard to aid in the overall convenience of operation. For example, a group of 8 keys for cursor control / 14 keys accommodate numeric entry / 16 special function keys allow access to 32 pre-programmed commands / 8 keys make up the extensive edit and clear section / 8 keys for video set up and mode control / and 8 keys control message and print.

Two Polling options available: 1) Polling compatible with Lear Siegler's ADM-2. 2) Polling discipline compatible with Burroughs.

IQ 120

The SOROC IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price. The IQ 120 terminal is a simple self-contained, operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.

CIRCLE 75 ON INQUIRY CARD

SOROC TECHNOLOGY, INC.

165 FREEDOM AVE., ANAHEIM, CALIF. 92801

(714) 992-2860 / (800) 854-0147

optional onboard optically isolated current loop interfacing available. The 6.75 x 12 x 0.6″ (17.15 x 30 x 1.5-cm) board from Syscom, Inc, 2996 Scott Blvd, Santa Clara, CA 95050 is address selectable and has a hardware timer with interrupt capability.

Standard Series/80 instructions effect channel control. Two channels are general purpose with data set controls to and from modems. Timer interrupt and modem control signals are jumper selected for connection to any of the eight Multibus interrupt levels. Other features are 5-, 6-, 7-, or 8-bit character formats; 1, 1½, or 2 stop-bit selection; and false start-bit detection. Single-quantity price is $695; optional current loop interface modules are $49/output channel and $29/input channel.

Circle 424 on Inquiry Card

Interface Board Provides Opto-Isolated I/O and Dual Stepper Control

The CTLR-216 process controller card from NANCO Diversified Design, 8380 Vickers St, Suite E, San Diego, CA 92111 installs on Commodore PET computers to handle medium duty applications for stepper motor operated devices. Two 4-phase stepper logic outputs have eight opto-isolated sense input lines and eight opto-isolated output control lines. Occupying 400 bytes, a software driver module runs on any 8k or larger computer. It contains eight commands for control of two steppers, eight heavy duty relays or triacs, and eight input sense lines. All commands—including rate select, stepper move, limit switch inputs, relay control, position index, and execution command—are passed by the user function in PET BASIC.

A computer transformer supplies power to the onboard 5-V regulator. The 4 x 8″ (10 x 20-cm) board, retail priced at $199, contains mounting hardware, parallel user port, control cables, and three IC positions for custom additions. Options include power control unit containing stepper power supplies, heavy duty relays, and I/O termination panel.

Circle 425 on Inquiry Card

FCC Approved Modem Serves As Multifunction Data Equipment

MM-103 data modem and interface adapter (RS-232 not required) gives S-100 bus computers complete communications using direct connection —without a DAA—to the public switched telephone network as the transmission system. It automatically originates and answers calls under software control, automatically dials the telephone, and serves as a clock, using software. Potomac Micro-Magic, Inc, PO Box 11149, Alexandria, VA 22312 has priced the unit at $319.95.

Both the modem and telephone system interface are FCC approved. In place of a DAA, the modem uses a miniaturized proprietary protective coupler to keep high voltages from the computer, and onboard circuitry to accomplish billing delay and level control. In addition, the interface handles control and sensing of auxiliary equipment, and provisions are made for the telephone ringing signal to power-up the computer system.

Characteristics are −50-dBm sensitivity, auto answer, auto originate, auto dialer with computer controlled dial rate, precision dial tone detector, and crystal controlled modem and dialer. Also featured are single-chip transmit and receive filters, software controlled maskable interrupt system, and PC boards with plated through holes, gold-over-nickel edge connector, and solder mask on both sides. Rate selection under computer control ranges from 61 to 300 baud; 600 baud is possible over local telephone systems.

Circle 426 on Inquiry Card

SOFTWARE

Seven Users Can Run BASIC Programs Independently

Memory bank select feature of the memory boards and high performance floppy disc drives are the basis of the multiuser software system's efficiency and speed capabilities. Up to seven users can run separate BASIC programs. The system is composed of BASIC, and a timesharing operating system, which finds an empty bank of memory and puts the user into active queue.

Console I/Os are serviced by interrupts. Another function of the operating system is to coordinate requests for I/O from the discs (requests in the disc queue are ordered by disc and track). Bank select organizes memory space into eight banks of 64k bytes each. In a multiuser system, each user is confined to one memory bank; the active bank is selected with only one I/O instruction.

The BASIC portion is similar to the 16k Extended BASIC, also produced by Cromemco, Inc, 280 Bernardo Ave, Mountain View, CA 94043, with the addition of such features as deadlock prevention and mutual exclusion; an inline BASIC text editor; long variable, label, and subroutine names up to 31 characters; and a protect statement. It is supplied as software only or a combination hardware/software package to upgrade the System Two or Three to a 2-user system.

Circle 427 on Inquiry Card

Disc Operating System and BASIC Software Increase Execution Speed

Users of 6800 microcomputers now have available an advanced disc operating and file management system, and Super BASIC. Both have been announced by PerCom Data Co, Inc, 4021 Windsor, Garland, TX 75042.

Speed of Index™ (interrupt driven executive) is increased because the console and other I/O devices are serviced by interrupt requests instead of by polling. Supporting unlimited DOS commands, the system treats I/O devices and peripherals as disc files. System is expanded by adding utility commands and driver routines that reside on diskette and are loaded into memory only when needed.

ASCII and binary files are handled; disc files are automatically created, allocated, and deallocated. Files, referenced by names of up to eight characters, can be copied onto a diskette by a backup routine.

The console interface segment supports any standard serial ASCII terminal. File management software provides more than 60 system entry points for program linkage, and accommodates up to 16 simultaneous active data control blocks. Versions operate with the company's LFD-400, SWTP MF-68, Smoke Signal Broadcasting BFD-68 disc systems, and Motorola EXORciser development system.

Circle 428 on Inquiry Card

BASIC Software

The extended disc BASIC supports 42 commands and 31 functions. The program requires 12k bytes of memory. It is designed for 6800 computers using the LFD-400 or LFD-1000 disc systems. Upgrade kits allow its use with SWTP or Smoke Signal Broadcasting disc systems.

Compatible with programs written in SWTP 8k BASIC (versions 2.0, 2.2, and 2.3), the system includes other enhancements such as direct random access to disc file data, 9-digit BCD arithmetic, and named disc file and batch processing capability when used with the company's miniDOS™. Also included is line and character position error reporting with mnemonics used in place of numeric error codes.

Circle 429 on Inquiry Card

Information Management Software Handles Small System Functions

BPS is a BASIC information management system featuring relational data base, report writer, and query, edit, update, display, and format functions for small business applications. The system runs on an Ohio Scientific Challenger II or III microcomputer with dual-sided floppy disc drives, Hazeltine CRT with numeric pad, and Okidata 125-line/min, upper/lower case printer. It can be adapted to COBOL and FORTRAN. Mass storage can be increased to 300M bytes.

Interactive programs facilitate rapid inquiry and retrieval; information can be displayed on the screen before being printed. Format and print establish screen displays and special printouts. Up to eight files can be used concurrently to create a report or screen map. All file, record, and field selection, plus hardcopy or screen layouts can be saved as formats for later recall.

Update adds or alters records in a file. If no formats have been defined, a standard field listing appears. Data are searched for and displayed with the display function. The software, priced at $500, is available through Better Programming Systems Inc, 275 Fort Washington Ave, New York, NY 10032.

Circle 430 on Inquiry Card

Software Package Provides Alternative to Current Language

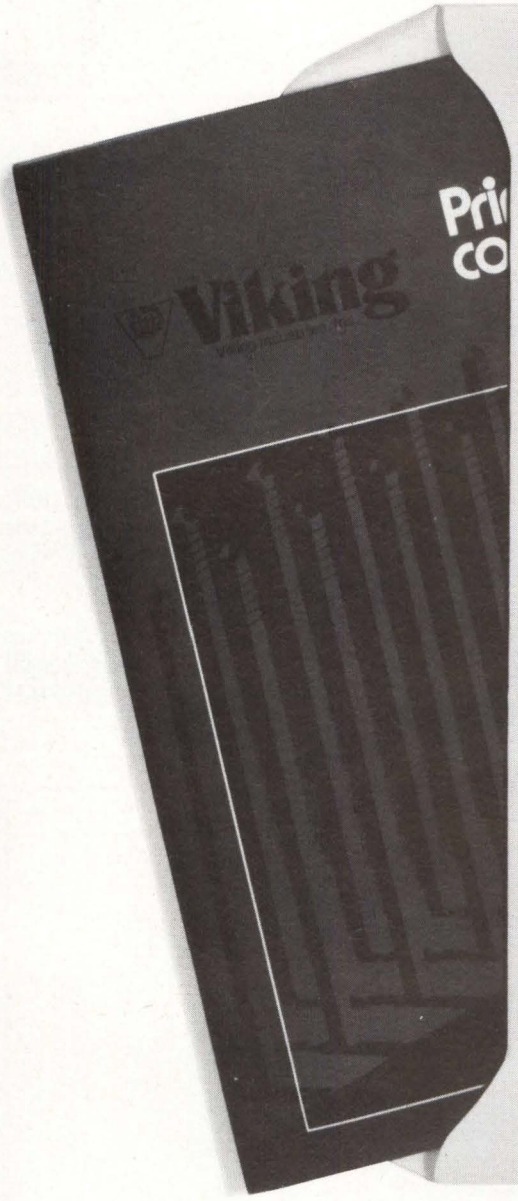
A FORTRAN and assembly language software package for Radio Shack's TRS-80 microcomputer includes FORTRAN-80 compiler, macro assembler, text editor, and linking loader. The package, representing an alternative to BASIC programming for TRS-80 disc users, is available from Microsoft, 10800 NE Eighth, Suite 819, Bellevue, WA 98004. The editor, which allows creation of assembler source, data, and FORTRAN files, expands the utilization of the computer disc hardware.

The Z80 macro assembler has a complete macro facility, full set of conditionals, and relocation pseudo-operations. A text editor gives fast random-access editing capabilities.

FORTRAN-80 includes all ANSI 1966 FORTRAN (except the COMPLEX data type), and such enhancements as mixed mode arithmetic, logical operations on integer data, ENCODE/DECODE for format operations to memory, and end-of-file and error-condition trapping for read and write operations. Compatible with TRSDOS, it is supplied on two minidiskettes and requires a minimum 32k system. Package price is $350. □

Circle 431 on Inquiry Card

Here is absolutely the best PC connector catalog you can get your hands on.



There's no point in being modest about the thing. This is the clearest, most straight forward, easy-to-use PC connector catalog in the business.

It helps that it is also your guide to one of the broadest lines of PC connectors offered by a single manufacturer. We have more basic designs in more depth, with more options than anyone.

But our line is only as good as your ability to get to it. And so we've spent time and effort to make sure our catalog lets you do just that.

It's logically organized – first by contact centers and then by type of terminations.

Everything on each connector series is shown on a single spread. No flipping back and forth.

You spend your time solving your design problem – instead of trying to solve our catalog.

Use the coupon and get your free copy.

Quick delivery of connectors Our distributors keep a large inventory of standard Viking connectors. If you need connectors in a hurry, chances are they're only a phone call away.

O.K. Send me

☐ your latest PC connector catalog.
☐ the name of your nearest rep./distributor.

NAME: _____ TITLE: _____

COMPANY: _____ PHONE: _____ EXT: _____

ADDRESS: _____

CITY: _____ STATE: _____ ZIP: _____

Viking CONNECTORS

21001 Nordhoff Street, Chatsworth, CA 91311, U.S.A./(213) 341-4330/TWX 910-494-2094

CIRCLE 77 ON INQUIRY CARD

OPERATION OF A BLOCK REPLICATE BUBBLE MEMORY SYSTEM

Gerald Cox
Texas Instruments Incorporated
Dallas, Texas

Feasibility of magnetic bubble devices for use as mass storage systems has been proven. Research done at Bell Telephone Laboratories in 1967 indicated that bits of data could be stored in a thin magnetic film formed on a crystalline substrate. Companies such as Rockwell (see *Computer Design*, Nov 1978, pp 27, 30), IBM Corp, Hewlett-Packard, and several Japanese firms are developing or producing magnetic bubble memory devices. Storage capabilities have been increasing, and in early 1977, Texas Instruments began marketing a 92k-bit device (see *Computer Design*, May 1977, p 150 and E. R. Garen, "Magnetic Bubble Memory Devices and Applications," Feb 1978, pp 164-168).

In today's devices, small cylindrical magnetic domains called "magnetic bubbles" are formed in single crystal thin films of synthetic ferrites or garnets when an external

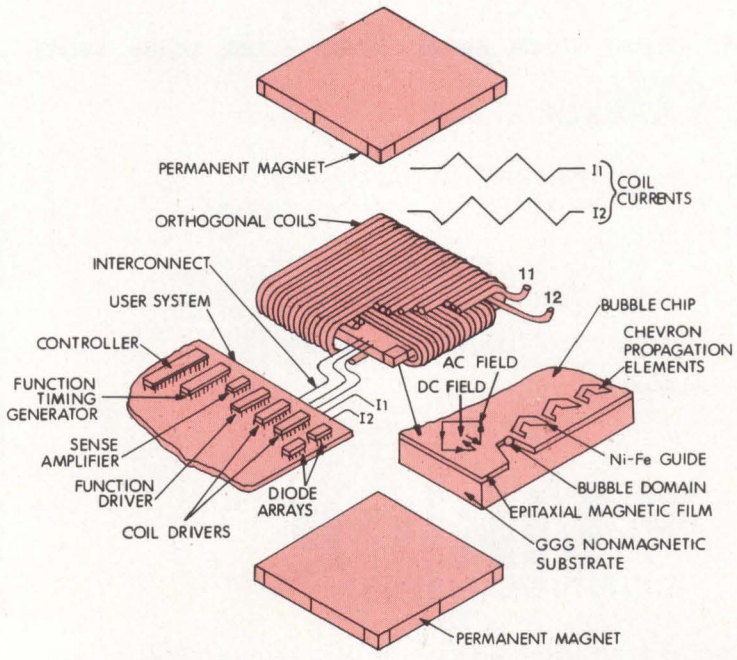


Fig 1 Elements of bubble memory system. Bubble device is located within system of orthogonal coils, which create rotating magnetic field to advance bubbles. Permanent magnets maintain bubbles as local domains in epitaxial magnetic film

SEE US AT
NCC
BOOTH 1506

ADD-ON.

NEW:
256KB semi ADD-INs for
Nova 3, Eclipse, & DEC 2020.

ADD-IN.

MINI-MEMORY. FROM DATARAM.

Either way, you get more memory, more throughput, more performance. Everything but more cost.

If you're looking for a way to get more from your minicomputer without putting too much more into it, our family of ADD-ON/ADD-IN mini-memories adds up to the right answer for you.

Including our new, expanded family of ADD-ON/ADD-IN systems that's ready to go to work for your minicomputer:

Data General
- Nova® 830
- Nova 1200
- Nova 1210
- Nova 1220
- Nova 1230
- Nova 2/4
- Nova 2/10
- Nova 3/4
- Nova 3/12
- Eclipse®

DEC®
- LSI-11®
- PDP®-8/A
- PDP-8/E
- PDP-8/F
- PDP-8/M
- PDP-11/04
- PDP-11/05
- PDP-11/10
- PDP-11/15
- PDP-11/20
- PDP-11/34
- PDP-11/35
- PDP-11/40
- PDP-11/45
- PDP-11/50
- PDP-11/55
- PDP-11/70
- DECSYSTEM-2020

Varian
- 620/f
- 620/i
- 620/L
- 620/L-100
- 622/i
- V-71
- V-72
- V-73
- V-74
- V-75
- V-77

Interdata
- Model 50
- Model 55
- Model 70
- Model 74
- 6/16
- 7/16
- 8/16
- 8/16E
- 7/32
- 8/32

Data 100
- CDP 135

DCC
- 116
- 116E

Whether you're adding it on or in, Dataram will meet your mini-memory requirements with new, reliable 16K single-board design that delivers the performance you want, and saves you money while doing it. Find out more — return this coupon at once, or call 609-799-0071.

I'd like more answers about mini-memories for my _____ minicomputer.

☐ Please send information.

☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

DATARAM CORPORATION
PRINCETON-HIGHTSTOWN ROAD CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

CIRCLE 78 ON INQUIRY CARD

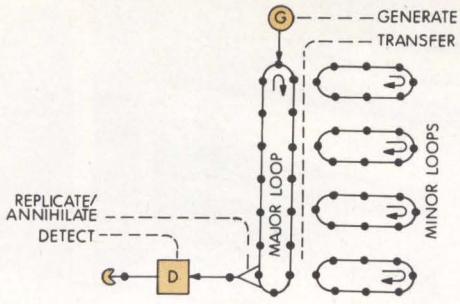


Fig 2 Major/minor loops. Bubbles are stored in minor loops and transferred in parallel to major loop, from which they are read out. Storing information follows reverse procedure

magnetic field is applied perpendicularly to the surface of the film (Fig 1). A rotating magnetic field is used to move the bubbles through the film in a shift register fashion with the presence of a magnetic bubble representing a digital "1," and the absence a digital "0."

Magnetic bubble memories are similar to magnetic tape storage in that they are nonvolatile. Furthermore, they have the high reliability of solid-state products and do not require preventive maintenance. This technology is filling the gap between RAM and hard disc or tape storage and is competitive with floppy disc memories in many applications, especially in systems where initial cost outlay is the primary criterion. Bubble memories are expected to become an integral part of disc systems in the near future, in an enhancement role, by providing access times of less than 8 ms. Their small size and light weight adapts them to use in compact designs or portable applications.

Many different bubble memory organizations have been employed (see J. E. Juliussen, "Magnetic Bubble Memory Systems Approach Practical Use," *Computer Design*, Oct 1976, pp 81-91). The simplest and most straightforward is "single-loop" architecture, in which data circulate in a closed path in shift register fashion.

Single-loop devices correspond to magnetic tape drives and are subject to the same limitation involving serial access to data. A major/minor loop architecture, on the other hand, is analogous to disc storage, in which each minor loop is like one track on the disc (Fig 2). During a write operation in this architecture, data generation occurs one bit at a time in the major loop. Data in the form of magnetic bubbles are then transferred in parallel to the minor loops where they circulate until the next readout.

Block Replication Memory

A 250k-bit bubble memory, the TIB0303, introduced by Texas Instruments in mid-1978, represents a major advance in nonvolatile memory technology (see *Computer Design*, Oct 1978, p 208). This device, which replicates data in parallel blocks instead of serially, is housed in a 20-pin dual-inline package and will be supported by a set of microprocessor based interface ICs. An important feature of the memory is that information regarding redundancy of loops and address synchronization is stored in the bubble chip. The device also has separate input and output data tracks with data storage divided into two blocks for each page of data (Figs 3 and 4).

Data are stored in two banks of minor loops. If there were only one bank of loops, data would be generated only in every other bit position due to physical space limitations of minor loop construction. The result would be a data rate half that of the field frequency.

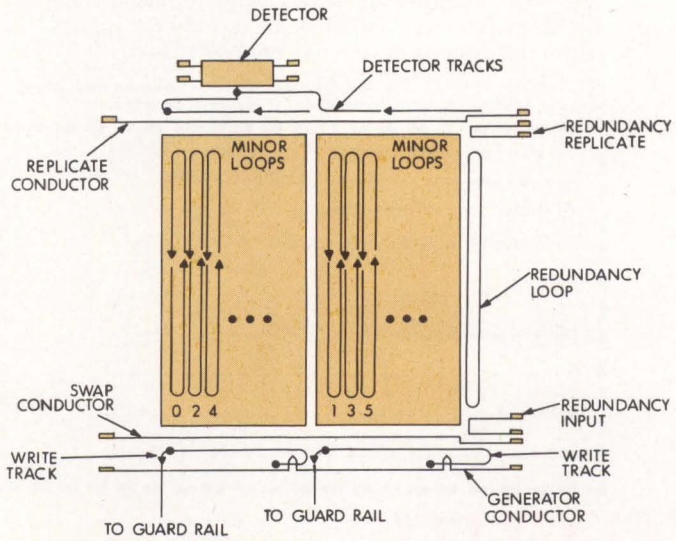
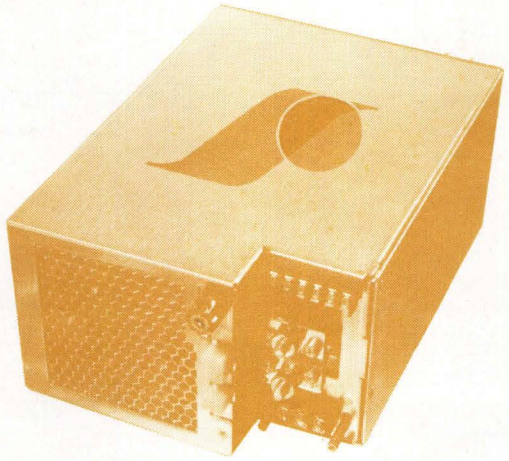


Fig 3 Separate I/O tracks and minor loop architecture. Bubbles are generated and moved serially along write tracks. Electronic pulsing of swap conductor trades bubbles on write track with adjacent bubble of minor loop. At end of write track, bubbles received in trades from loops are annihilated. Swaps are made in parallel blocks, all minor loops entering trade essentially simultaneously. Minor loop bits are replicated (via replicate conductor) onto detector tracks, again in parallel fashion. Even bits in block are stored in one set of minor loops, odd bits in another. Merging of even and odd bits in sequence provides detector with compressed data, bits spaced at twice density allowed by geometric width of minor loops

For 21 years we've quietly built Switchers.



Now it's time to let the World in on it.

Back in 1958, Pioneer Magnetics built its first switching power supply. We've been quietly pioneering the design of switching supplies ever since.

Today we offer the system designer a complete family of standard models providing output voltages ranging from 2 to 48 VDC with output power to 2000 Watts. Single and multiple output configurations with a wide range of options are available.

FEATURES:

A.C. Input: 92 to 138 or 184 to 250V single phase 47 to 63 Hz.
D.C. Input: 24, 48, 120 or 240 VDC standard.
Brownoutproof: Supplies ignore most line variations and continue to supply specified regulated outputs at full load if input voltage drops as low as 80 or 140 VAC.
Total Error Band: Output deviations will not exceed ±2% due to line changes, static and dynamic load changes, ripple and noise spikes, temperature variations and drift.
Power Loss Holdup: Output will remain within regulation 30 msec after loss of AC input at full load and nominal line.
Safety Standards: Standard models are recognized to UL478.

SINGLE OUTPUT SUPPLIES

AC INPUT MODEL / DC INPUT MODEL	TYPE NUMBERS (Add Amps in Blanks) AC MODELS	DC MODELS	PM2496A PM2721 OUTPUT CURRENT	PM2497A PM2722 OUTPUT CURRENT	PM2498B – – – OUTPUT CURRENT	PM2499 – – – OUTPUT CURRENT
OUTPUT VOLTAGE						
2	2D ____	2F ____	100	200	400	300
3	3D ____	3F ____	60	100	200	200
5	5D ____	5F ____	50	100	200	200
5	5D ____	5F ____	60	120	–	–
5	5D ____	5F ____	–	150	300	300
12	12D ____	12F ____	25	60	120	120
15	15D ____	15F ____	25	50	100	100
18	18D ____	18F ____	22	45	90	90
21	21D ____	21F ____	18	38	76	76
24	24D ____	24F ____	16	33	66	66
28	28D ____	28F ____	13	27	54	54
48	48D ____	48F ____	8	16	32	32
SIZE (INCHES) (CENTIMETERS)			5x8x11 12.7x20.3x27.9	5x8x11 12.7x20.3x27.9	5x16x11 12.7x40.6x27.9	5x8x15 12.7x20.3x38.1
WEIGHT (POUNDS) (KILOGRAMS)			16 7.3	18 8.2	35 15.9	25 11.4

MULTIPLE OUTPUT SUPPLIES

AC INPUT MODEL / DC INPUT MODEL		PM2675A PM2775	PM2676A PM2776	PM2677A	PM2678A
MAX. TOTAL OUTPUT POWER IN WATTS		375W	600W	750W	850W
MAIN CHANNEL	OUTPUT VOLTAGES AVAILABLE	2, 3, 5, 12, 15, 18, 21, 24, 28, 48			
	MAX. POWER IN WATTS	250W	500W	600W	750W
SECOND CHANNEL	OUTPUT VOLTAGE	5 12 15 18 21 24 28			
	OUTPUT CURRENT MAX. (see note 1)	7 7 7 CHECK FACTORY			
THIRD CHANNEL	OUTPUT VOLTAGE	5 12 15 18 21 24 28			
	OUTPUT CURRENT MAX. (see note 1)	10 10 10 CHECK FACTORY			
FOURTH CHANNEL	OUTPUT VOLTAGE	5 12 15 18 21 24 28			
	OUTPUT CURRENT MAX.	4 4 4 4 4 3 3			
SIZE (INCHES) (CENTIMETERS)		5 x 8 x 11¾ 12.7 x 20.3 x 29.8 (see note 2)			
WEIGHT (POUNDS) (KILOGRAMS)		20 9			

Note 1: Higher currents available to 30 Amperes. Note 2: Add 1 9/16" (4 cm.) for external fan on Models PM2677A, PM2678A.

The Pioneers in Switching Supplies

Pioneer Magnetics

Pioneer Magnetics, Inc. • 1745 Berkeley Street, Santa Monica, California 90404 • Telephone: 213/829-6751 • TWX 910-343-6249

CIRCLE 79 ON INQUIRY CARD

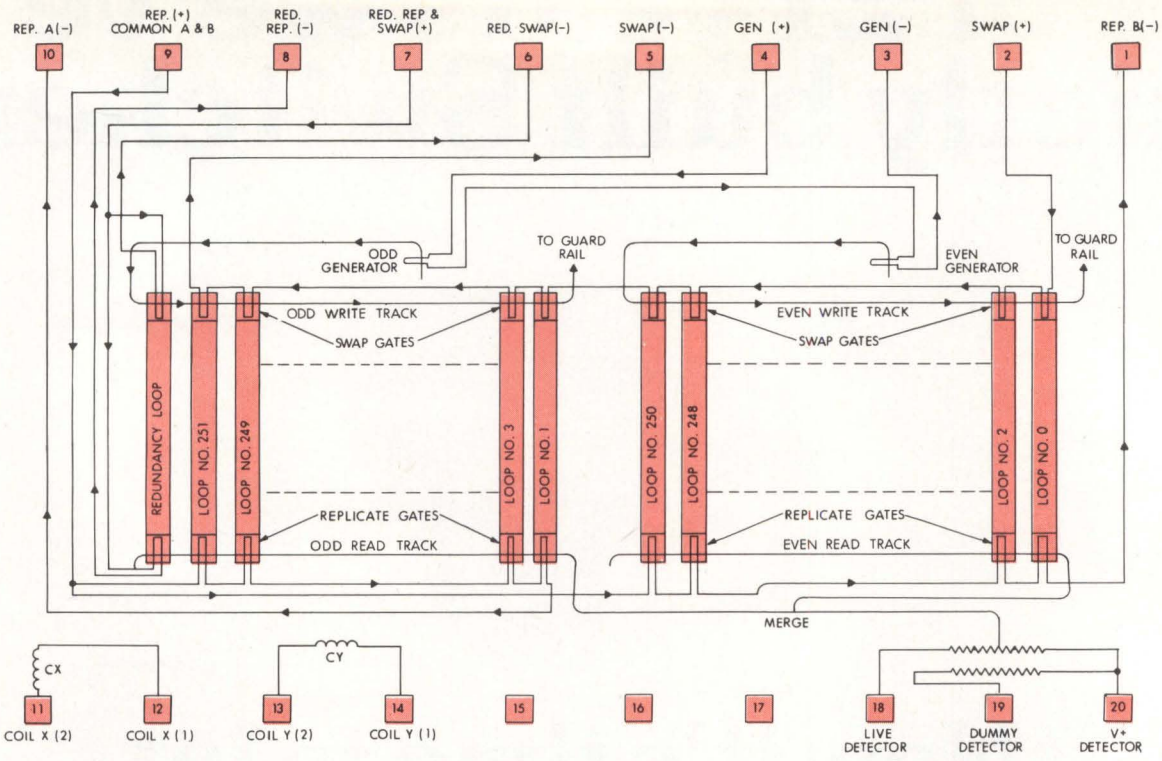


Fig 4 Block replicate architecture. Serial string of up to 224 bits, organized according to user's requirements, is input to bubble memory. String is stored in corresponding bit positions in minor loops. Total of 1137 bits per loop allows storage of 1137 such strings. Memory controller locates corresponding bits upon readout

This memory, however, is divided into two halves so that the even bits of a page of data are stored in the right bank of minor loops and the odd bits in the left bank. Two serially connected generators are used to create identical data in both write tracks. The distance from the odd generator to the first minor loop is one less bubble position than the even generator is from its closest minor loop. Thus data in the odd write track are skewed one bit position from data in the even write track. When data in the two write tracks are in position to be placed in minor loops, a current pulse to the swap gate removes old data from the minor loops and replaces them with new data. Since data stored in minor loops are separated into even and odd bits, data in the write tracks are generated in every bit position, making the data rate equal to the field frequency or twice that of a bubble memory with a single set of minor loops.

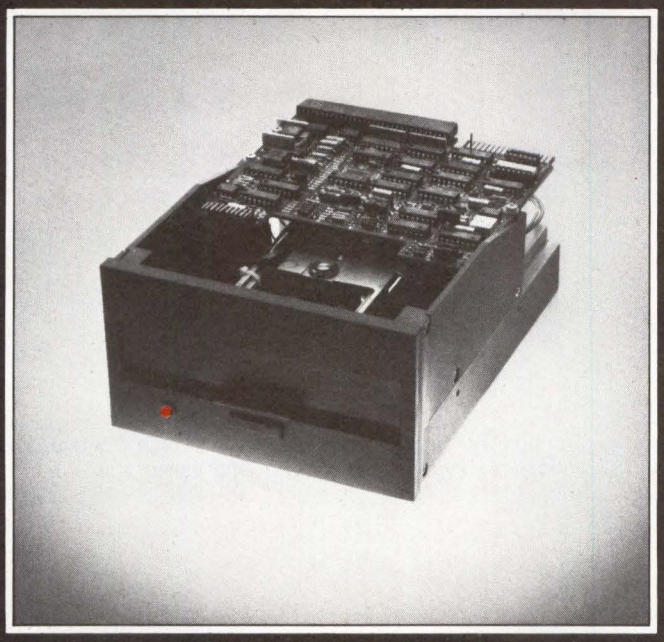
The read track is at the opposite end of the minor loops from the write track. Aluminum-copper replicate-gate elements are located at each junction of a minor loop with respect to the read track. When replicate gates receive a current pulse, bubbles that are in position under the gate are duplicated (replicated) in the output track. Thus, a block of data is duplicated in the read track while data resident in minor loops are left intact.

Data replicated in the read tracks remain two bit positions apart until the two tracks reach a common point called the merge gate. Data in the odd read track are skewed one bit position from data in the even read track, allowing even and odd bits from the two halves of memory to interleave and form the original page of data. Bubbles are propagated along this merged track to the detector, where they are elongated. These stretched magnetic domains then pass under a permalloy pattern detector. Two identical detector elements are deposited on each chip and these are placed in two legs of a precision bridge. The bubble passing under the first detector causes a change in resistance, which is seen as a 5- to 10-mV variation in the signal on the output of the bridge. Bubbles then propagate to a guard rail located between the detectors, preventing passage of bubbles under the second (dummy) detector, which acts as a balance resistance in the bridge.

Loop Redundancy

One of the most important features of the bubble memory is the manner in which redundancy of minor loops is handled. The chip has 252 minor loops of which 28 are allowed to be defective, leaving 224 minor loops for actual use. There are 1137 bits/loop, giving a net storage of 254,688 bits of information. This redundancy provision eliminates the need for perfect chips and reduces costs significantly by increasing yields. A map of unused loops is stored in a dedicated minor loop on the bubble chip. Separate I/O control lines are provided so that reading the redundancy loop does not disturb the other minor loops.

Upon initialization of the system, this redundancy map is read to an internal RAM in the bubble memory controller. During a write or read operation, each bit position in a page of data is then compared with the map stored in the controller. This permits parts to be



Simply Better.

Our MPI 52 two-headed micro floppy drive has speed, accuracy, capacity, and simplicity. It's better than any other drive.

Better because it's faster. Five times faster than the next best. Our exclusive band-positioning design ensures track to track access time of 5 milliseconds.

Better because it's bigger. 437.5K bytes per double density disk, unformatted.

And simply better because it's reliable. The MPI 52 has 1½% speed control, no mechanical switches, and comes fully burned in. There are only 10 moving parts, including our front door diskette ejector mechanism.

Order your industry-compatible MPI floppy disc drive. It's the drive for success.

MPI

MICRO PERIPHERALS INC.
21201 Oxnard Street
Woodland Hills, California 91367
(213) 999-1353

CIRCLE 80 ON INQUIRY CARD

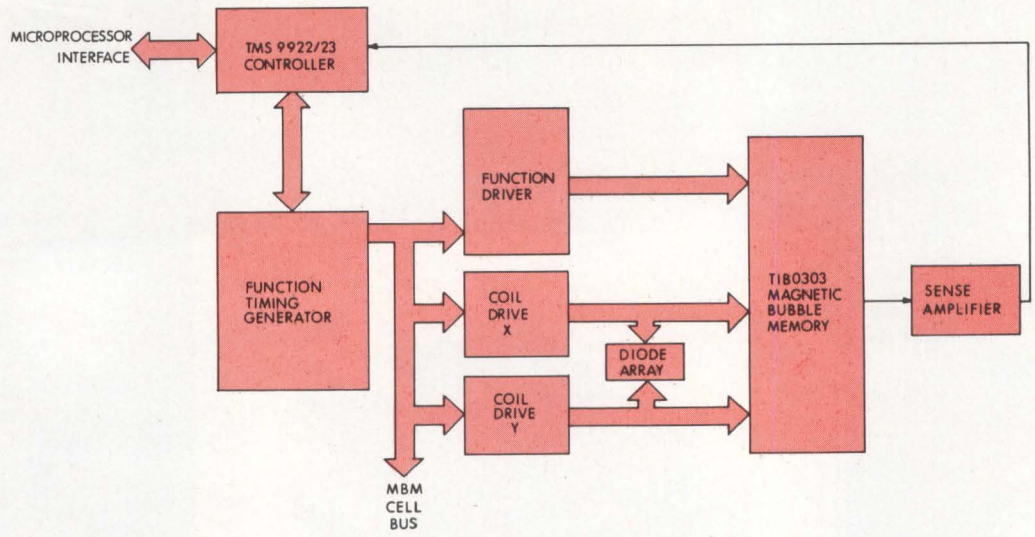


Fig 5 Family of interface and control circuits for 0.25M-bit bubble memory will include controllers, function timing generator, function driver, two coil drivers, and sense amplifier

directly interchanged even though different units contain different sets of defective minor loops.

The loop used to store the redundancy map is also used to store an address synchronization pattern. Since there is no direct means of addressing the minor loops, a method must be established to locate a data reference position when power is first turned on. The address synchronization pattern is a unique leading-code located in the redundancy loop which is used to determine the page zero location in the memory. Using this code, the controller is able to initialize its page counter, allowing data in minor loops to be halted in any bit position within a maximum of 22.5 μs. This is perhaps the most important function of the dedicated minor loop in that it eliminates any special power supply requirements that would otherwise be needed for power-down sequencing to preserve data.

Memory Interface Circuits

A variety of circuits are required to complete the bubble memory system. These include a controller to serve as interface to a CPU and generate enable pulses to a function timing generator, coil and function drivers, and a sense amplifier to amplify the bubble detector's signal (see Fig 5).

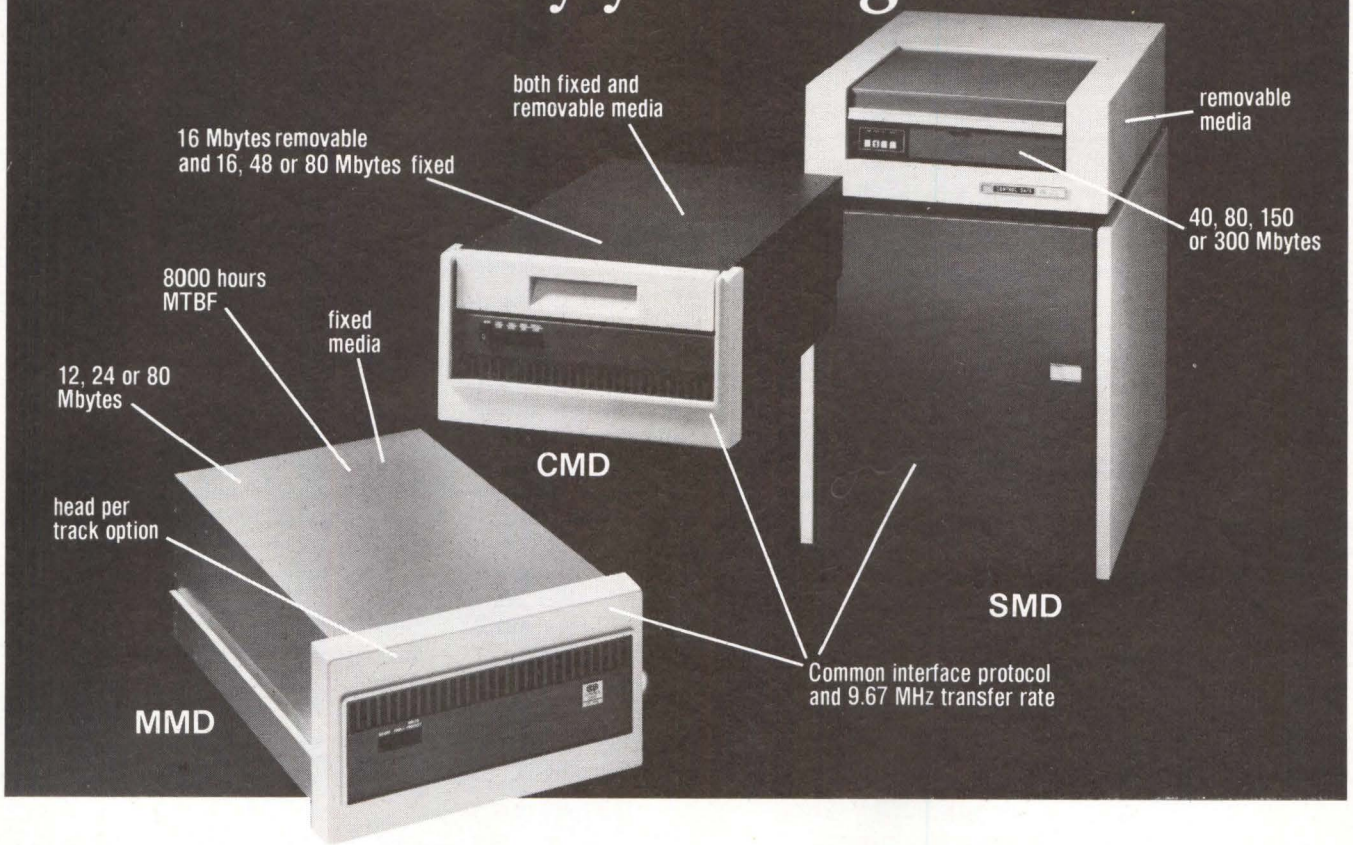
High level interface between the microprocessor and the bubble memory is provided by the controller, which performs parallel to serial conversion from the microprocessor to the bubble memory and serial to parallel conversion from the memory to the microprocessor. It also contains a 28-byte buffer for temporary data storage, a microsequencer ROM for control, internal status registers, I/O buffer latches, and a RAM for temporary redundancy loop storage. It has the capability of operating in either a single-page mode or a multipage mode which ranges from 1 to 1137 pages. In addition, the MOS controller operates in full DMA capacity when used with the TMS 9911. Its main functions are to start and stop bubble movement, maintain page position, and raise or lower flags for bubble memory functions such as generate, swap, block replicate, and redundancy replicate.

Control signals from the memory controller are sent to the function timing generator. This monolithic IC provides the precise timing signals necessary to operate the function driver, coil drivers, and sense amplifier during each field cycle. Function driver circuit converts TTL level signals from the function timing circuit into current pulses required by the bubble memory control elements. Temperature compensation for the bubble module is performed on this chip in conjunction with a thermistor in contact with the case.

The coil driver circuit and diode array are used to generate currents with triangular waveforms in the bubble module coils. TTL inputs from the function timing generator are received by the coil driver, which produces a higher level driving voltage. The coils integrate the voltage into a current which ramps up and then down, producing the desired triangular waveforms.

Voltages from the detector that are too small to be directly useful in the system are received by the sense amplifier. The bubble signal is amplified, level detected, and latched by signals provided by the function timing circuit. Then data output is coupled to the MOS controller.

OEM Module Drives from CDC. It's the family you can grow with.



Control Data offers you a *family of module drives* because OEM storage requirements vary. One application may demand the high capacity and removable media offered by our Storage Module Drive (SMD). Another application may demand the exceptional reliability and fixed media of our Mini Module Drive (MMD). Or maybe our Cartridge Module Drive (CMD) with both fixed and removable media best fits your application.

But there's one thing that our SMD, MMD and CMD all have in common. All feature the widely accepted 9.67 MHz transfer rate. All use compatible interface software and firmware. That means you don't have to change your basic design every time your storage requirements change. That means easier system integration and simple field upgrades. And one source for all your storage requirements.

One Source and One Standard of Excellence

These module drives share something else that's important to an OEM. Quality. We design and manufacture all critical components in-house. We can build reliability into our drives because we built it into our heads, servos and media. Control Data has earned a reputation for building equipment that lasts.

Value to Match Performance

We feel that our cost of ownership is the best in the industry. And we'd like to help you compare our lower cost-per-bit and lower entry costs with others.

Put quality behind your nameplate. Call us at 612/853-5020. Or if in Europe, contact one of our European representatives. Or return coupon to:

R. G. Crowder, Manager CD-49
OEM Product Sales, Storage Peripherals
CONTROL DATA CORPORATION
P.O. Box 0, Minneapolis, MN 55440

Please send information on your ☐ SMD ☐ MMD ☐ CMD

Name_____ Title_____

Company_____ Phone_____

Address_____

City_____ State_____ Zip_____

CONTROL DATA CORPORATION

More than a computer company

4½-Digit Microprocessor Counter/ Decoder Drives LEDs or LCDs

A high speed counter utilizing CMOS technology provides a typical counting rate from 0 to 25 MHz, for a wide variety of applications. The manufacturer, Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014, states that this 4½-digit microprocessor device is the first monolithic counter/decoder on the market to offer direct LED or LCD drive.

Having a 7-segment display driving capability, the chips come in two models—the ICM7224 for LCDs and the ICM7225 for LED displays. For each of these, typical power requirements range from 1 μA at 10 kHz to 2 mA at 20 MHz. Less than 100 μW is dissipated in the quiescent state. The devices will operate as decade counters to 19999 or as timers to 15959.

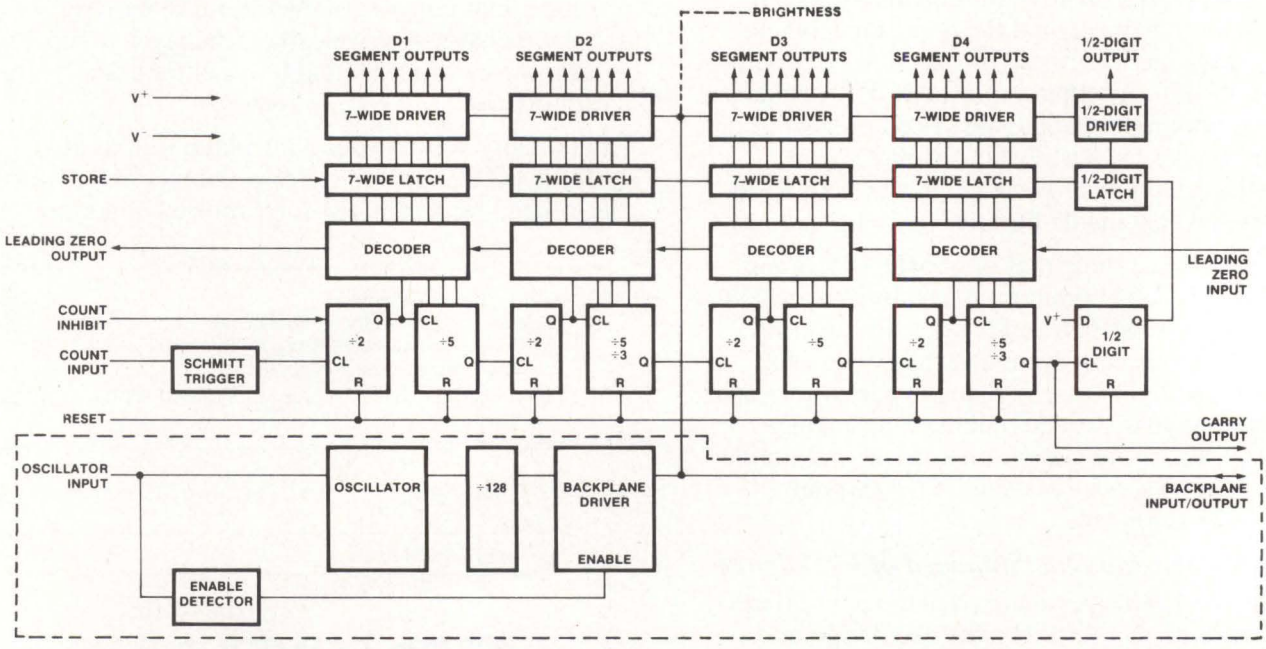
In the LCD driver version, there are 29 segment outputs and a backplane driver output, generating the zero dc component signals necessary to drive a conventional 4½-digit LCD. These devices also include a complete RC oscillator and divider chain to generate the backplane frequency, and a backplane driver disable control, which allows the segments to be slaved to a master backplane signal. No external driver components are needed. Devices may be ganged or cascaded for 8-, 12-, or 16-digit displays.

A direct nonmultiplexed common-anode drive is featured in the LED driver version, eliminating the generation of RF interference. This version provides 28 segment and 1 half-digit open-drain n-channel transistor outputs, suitable for directly driving common-anode LED displays at greater than 5 mA/segment. A brightness input is provided, which may be used digitally as a display enable, or with a potentiometer as a continuous display brightness control.

The counter section of both versions provides direct static counting from dc to 15 MHz, guaranteed, with a 5-V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry that allows a direct interface with ICM7207/A ADCs to implement a low power frequency counter with a minimum component count.

Also included are several features intended to simplify cascading 4-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between 4-decade blocks.

Minimum operating voltages are 3 V (LCD) and 4 V (LED) for use in portable battery operated counting systems. Low operating current of 1 mA at 2.8 V and a 10-MHz count rate allow a single 1500-mAH lithium battery to drive the system for as long as two months.



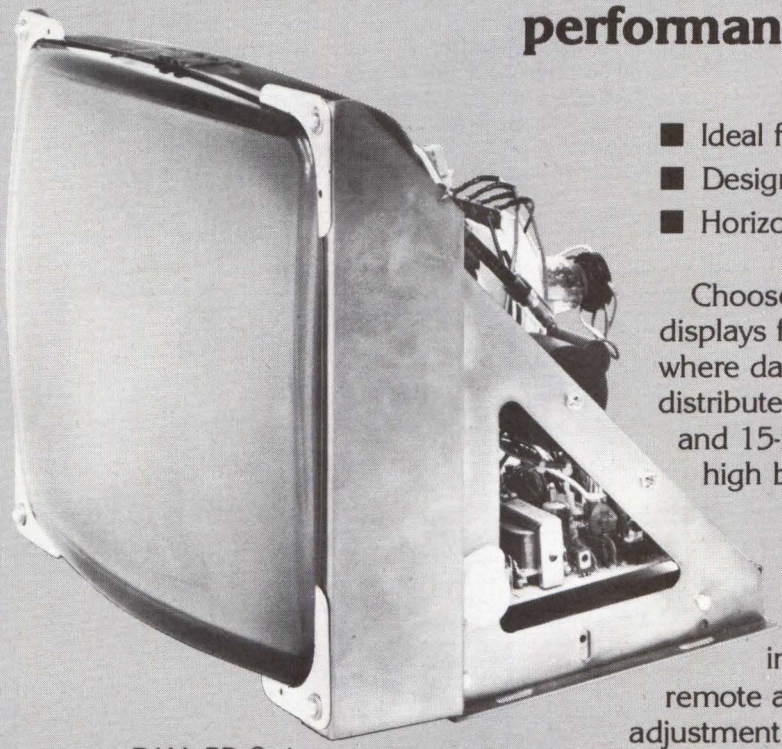
Microprocessor counter/decoder/display driver from Intersil. Elements within dashed line relate only to LCD driver version, ICM7224. Dotted line indicating brightness control line relates only to LED driver version, ICM7225

(*Continued on p* 178)

In Data Display...

RD means high-performance remote operation

BALL RD Series composite input displays set remote performance standards



BALL RD Series
High Performance
Data Display

- Ideal for remote data display
- Designed for standard EIA composite signals
- Horizontal line rates up to 24 KHz

Choose BALL RD Series composite input displays for high-performance applications where data display signals must be distributed over long distances. RD Series 12 and 15-inch models offer wide bandwidth, high brightness, and horizontal resolution of 1000 TV lines. Specifications or mechanical designs can be modified to meet your needs exactly.

Select BALL RD Series composite input displays for your high-performance remote applications, and be sure of precise adjustment and alignment. BALL displays will meet or exceed your performance specifications dependably over the long haul. It's a matter of design.

If you haven't looked at life cycle costs, you haven't found the real bargain in high performance remote data display. Specify the RD Series for a decision you can live with.

In data display, BALL means experience, quality and service.

Ball Electronic Display Division

P.O. Box 43376 St. Paul, MN 55164 (612) 786-8900. TWX: 910-563-3552

Sales Offices:

Downers Grove, IL (312) 960-4434
Ocean, NJ (201) 922-2800
Lewisville, TX (214) 436-2383
Santa Clara, CA (408) 244-1474
Upland, CA (714) 985-7110
Burlington, MA (617) 273-0608

CIRCLE 82 ON INQUIRY CARD

Applications include portable battery powered tachometers, a variety of mobile and marine instrumentation, and a wide range of unit counting and display functions. The devices are available in 40-pin epoxy DIPs.

Absolute maximum ratings include a 0.5-W power dissipation (at 70 °C), a maximum supply voltage (V+ to V−) of 6.5 V, while input voltage at any terminal must lie between V− −0.3 V and V+ +0.3 V. Allowable temperature range is −20 to 70 °C in operation and −55 to 125 °C during storage.

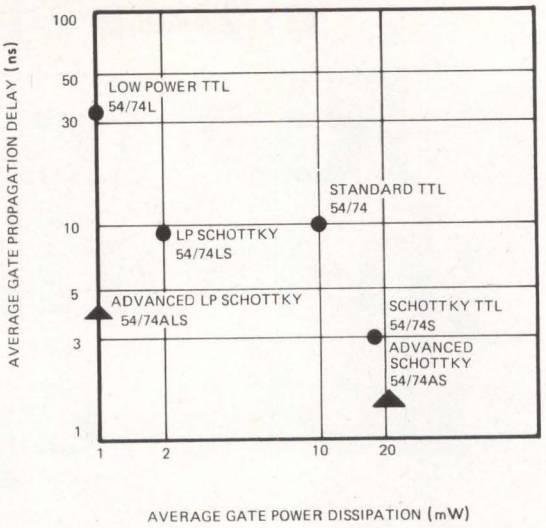
Circle 350 on Inquiry Card

Advanced Schottky TTL Series Provides Fast and Low Power Versions

Improved speed-power products are realized in third generation TTL developments from Texas Instruments, Inc, PO Box 225012, Dallas, TX 75265. The circuits include the high speed advanced Schottky TTL series SN74AS (twice as fast as the earlier SN74S series at approximately the same power consumption) and the general purpose advanced low power Schottky TTL series SN74ALS (more than twice as fast as the SN74LS series, at half the power consumption). Devices will be available in both military and commercial temperature ranges. These new TTL series are fully compatible with Series 54/74, 54LS/74LS, and 54S/74S TTL families.

The advanced high speed series features a typical 1.5-ns gate delay and 22-mW gate power dissipation. Internal gate delay for MSI functions is 1 ns (typ) and power consumption per gate function is 12 mW. Other characteristics include a Vcc of 5 V, a fanout of 10, and a density increase beyond earlier family levels, with gates implemented in 20-pin DIPs and MSI functions in a 300-mil 24-pin DIP.

A 4-pJ speed-power product characterizes the advanced lower power series, typically providing a 4-ns gate delay and 1-mW gate power dissipation. This is achieved through the use of oxide sidewall isolation processing, shallower active junctions using ion-implantation, and smaller chip geometries achieved through use of composed masking. The fanout is



Delay time is plotted against power dissipation for three generations of TTL circuits from Texas Instruments for both low power and high speed versions. Data points marked with triangles indicate most recent series. Continuing trend toward lower speed-power product is most pronounced for advanced low power Schottky with 4-pJ value

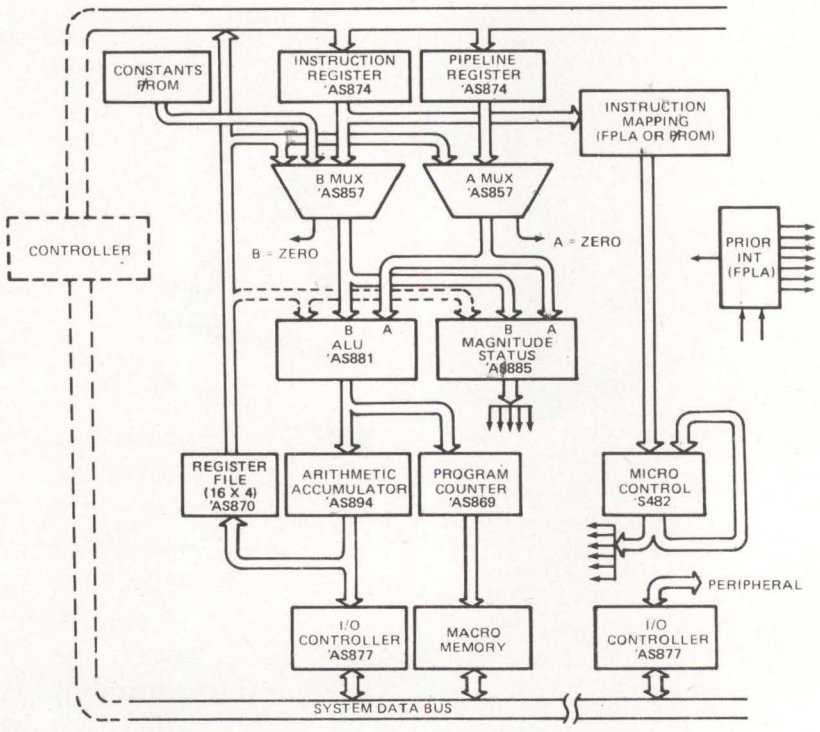


Diagram indicates architecture of typical high speed arithmetic processor utilizing advanced Schottky TTL elements. Mix of faster (AS) and lower power (ALS) elements in design depends on property to be optimized. Optimum selection would be 100% AS for max throughput rate, approximately 50% AS/ALS for cost-effectiveness, and 100% ALS for min power and mobile applications

Genisco High Resolution Displays.

Let us make your computer graphics 'crystal-clear'- fast!

Your future in graphics and image processing can't help being bright with all the Genisco Raster Display "good-omen" benefits going for you. Like ultra-high resolution, nanosecond processing, reliable performance, synergistic software, and modular architecture — that lets you quickly go "on-line" at minimal cost and expand as your needs dictate. Yet, with all this sophistication they're thin-pocket-book priced.

16K MOS/RAM Refresh Memories that go up to 1280 pixels/line X 1024 lines, in 16 gray scales, and 1024^2 full color versions. And, they're all directly addressable.

16-Bit User Programmable Graphics Processor lets you realize optimum operation with 150 ns cycle time manipulation, a set of 55 mnemonic instructions, automatic DMA access, selective erase, user selection from 4096 colors or 256 gray shades, and over 32 refresh memory planes control — using a unique "group select" method. We even offer a scroll and zoom, and a character/vector generator.

Versatile Output. Up to 12 monitors can be operated from a single system. TV/video mixing. Remote monitoring. RS232 ports. Automatic "Circumfill". These are but a smattering of the many advanced monitor control benefits offered by Genisco.

Full Complement of Interfaces for most popular minicomputers are available as standards, and we can economically fabricate a specific configuration where a stock unit won't do.

Flexible FORTRAN Software puts you "on-line" quickly, economically. Present offerings include a comprehensive set of Basic Graphics instructions, an efficient Cross Assembler, and our special GRASP package of FORTRAN callable subroutines — to simplify programming of your particular display configurations. With all this to back your display developments, a bright and 'crystal-clear' future is assured.

Contact Genisco, a name that has been synonymous with technological advances for more than 30 years, for all the particulars — and get a fast start on the path to good fortune.

GENISCO COMPUTERS

A DIVISION OF GENISCO TECHNOLOGY CORP.

17805 Sky Park Circle Dr., Irvine, CA 92714 • (714) 556-4916

CIRCLE 83 FOR SALES INFORMATION
CIRCLE 84 FOR LITERATURE

10 for the military (54) and 20 for the commercial (74) version. For this series, too, Vcc is 5 V. Packaging is provided in 14-, 16-, 20-, and 24-pin DIPs.

Circle 351 on Inquiry Card

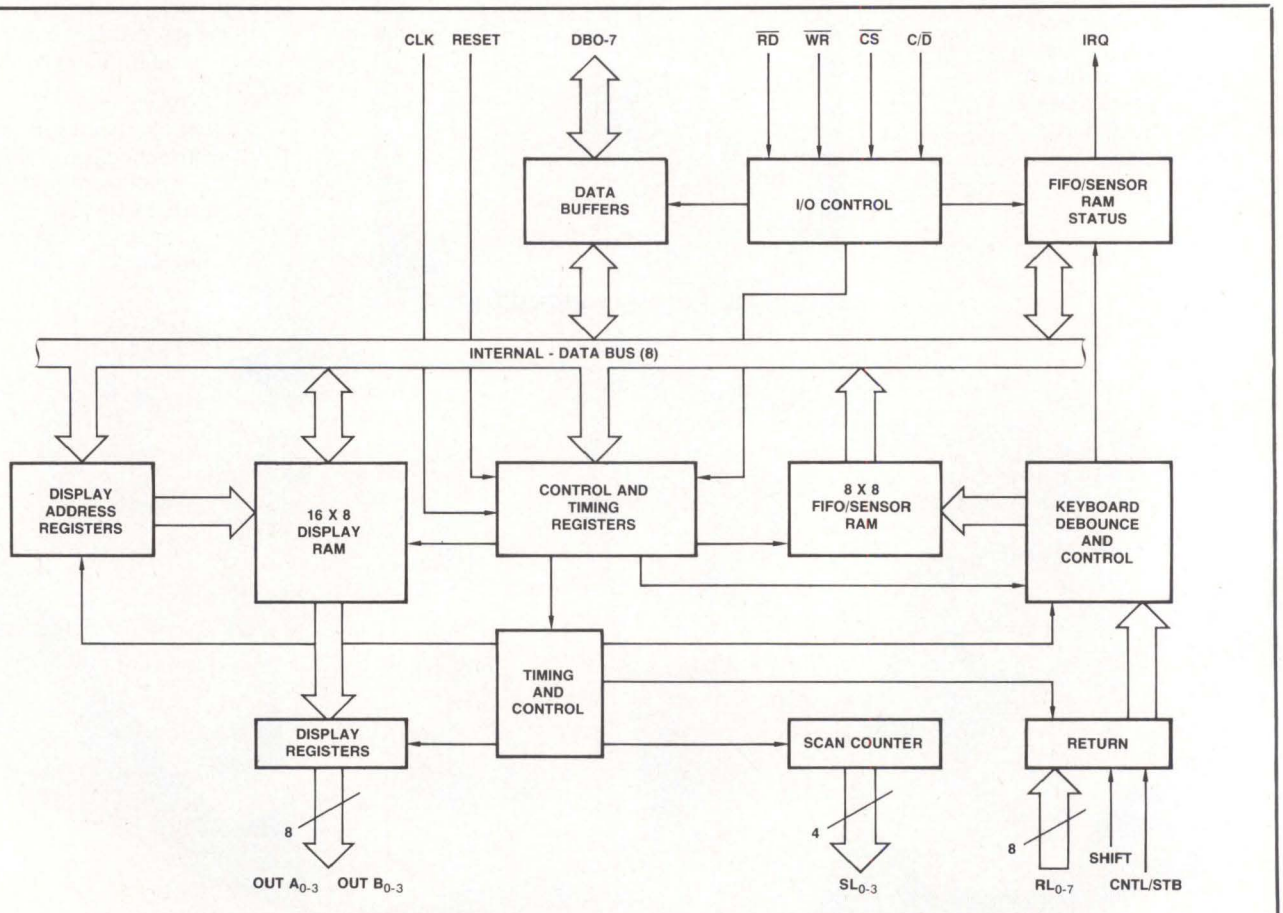
Mode Programmable Interface Controls Keyboard and Display

A keyboard controller produced by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086 allows simultaneous keyboard and display operations. Am8279, designed to work in 8080 and 8085 8-bit microprocessor systems, is mode programmable from the CPU, allowing selection of 2-key lockout, n-key rollover, or scanned sensor mode. It also has a programmable clock so that keyboard scan timing can be adjusted to CPU cycle time.

There is provision for a scanned interface to a 64-contact key matrix, which can be expanded to 128. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard. Keyboard entries are debounced and stored in an 8-character FIFO. If more than eight characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other display technologies. Both numeric and alphanumeric segment displays may be used, as well as simple indicators. Included in the device is a 16 x 8 display RAM, which can be organized into a dual 16 x 4. The RAM can be loaded or interrogated by the CPU. Users can select the option of displaying either one set of 16 alphanumeric characters or two sets of 16 numeric characters. Both right entry (calculator) and left entry (typewriter) display formats are possible. Read and write of the display RAM can be done with auto-increment of the display RAM address.

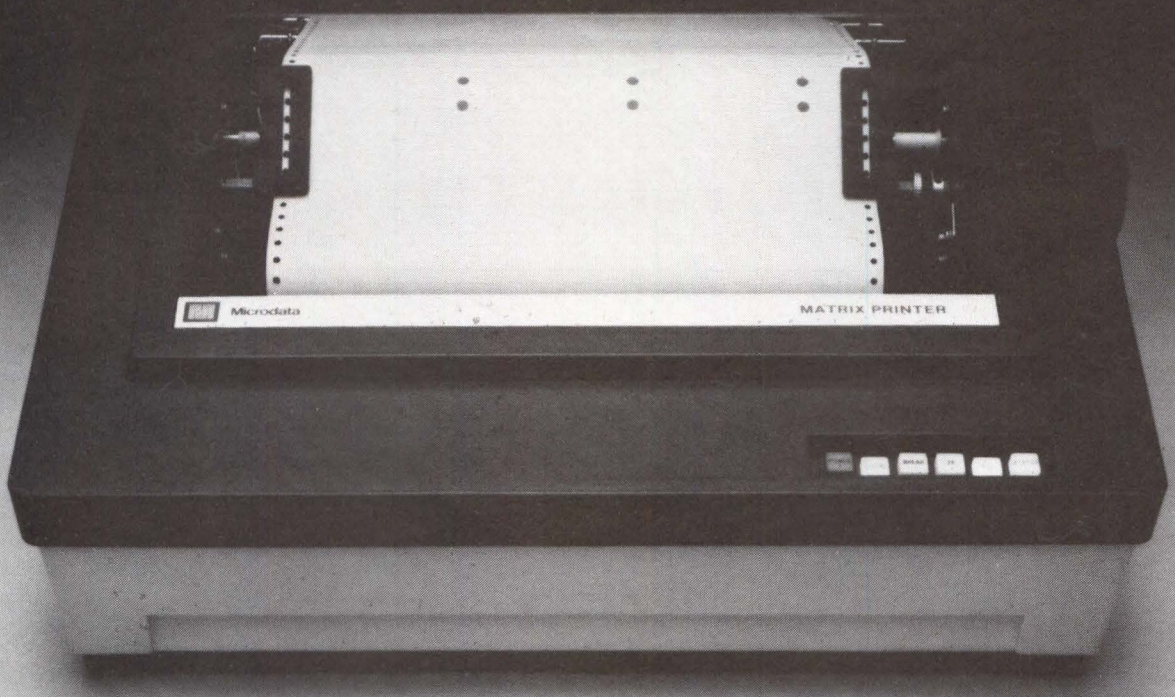
Maximum ratings require that the temperature remain between −65 and 150 °C during storage and between −55 and 125 °C under bias. With respect to Vss, all signal voltages and Vcc are restricted to the −0.5 to 7.0-V range. Power dissipation must not exceed 1.0 W. The device is a plug-in compatible replacement for the like-numbered circuit from Intel Corp, is provided in a 40-pin plastic or ceramic package, and undergoes 100% processing to the requirements of MIL-STD 883.



Programmable I/O interface, AM8279, from Advanced Micro Devices. Capabilities include simultaneous keyboard and display operation

Circle 352 on Inquiry Card

THIS IS THE ONLY DECENT LOW COST 165 CPS MATRIX PRINTER YOU CAN GET IN VOLUME RIGHT NOW.



Other people make them, of course. But you can't get them in volume. Unless you're willing to wait a very long time. And in this business a printer you can't get is about as useful as all those wonderful products that haven't been invented yet.

Even if you did have a wide variety to choose from, you'd probably choose our Matrix printer anyway. Microprocessor control makes it efficient, fast and reliable. And it's programmable from your computer or optional keyboard.

Bidirectional printing and paper feed gives you true graphics capabilities. Special character sets, including foreign language alphabets, provide incredible flexibility. And when you add the optional keyboard, it becomes a remote communications terminal.

Matrix is compatible with all industry standard RS-232-C or parallel interfaces, so you can plug it in just about anywhere.

If you need a good matrix printer in volume and you can't wait forever, contact one of our local sales offices or the Director of OEM Sales, Microdata Corporation, 17481 Red Hill Avenue, P.O. Box 19501, Irvine, CA 92713. Telephone: 714/540-6730. TWX: 910-595-1764.

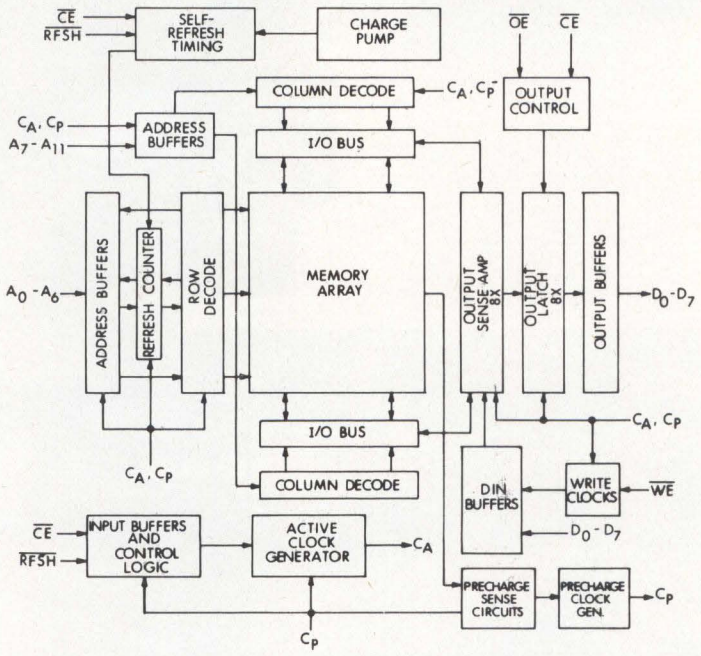
SALES OFFICES

Boston 617/890-2020
Chicago 312/364-5820
Cocoa Beach 305/783-4933
Los Angeles 714/533-8035
Minneapolis 612/881-0810
San Jose 408/245-5013
Washington, D.C. 703/620-3995

Microdata OEM Products
A significant difference.

CIRCLE 85 ON INQUIRY CARD

16k Dynamic MOS RAM Operates With 5-V Supply



Monolithic 2k x 8 dynamic RAM from Mostek is based on n-channel silicon gate process. Latched address and $\overline{CS}$ and independent $\overline{OE}$ allow easy interface in microprocessor systems

Organized as 2k x 8 for wide word applications and having an access time of 150 ns and a cycle time of 270 ns, a dynamic random access memory replaces four 2114 type static RAMs. The device, produced by Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, is claimed to be one of the first available 5-V only dynamic MOS RAMs and the first wide-word dynamic RAM designed specifically for use in present and future generation microprocessor systems.

This low power device requires 150 mW while active and only 25 mW on standby. A single refresh pin allows flexible control of single cycle refresh, burst mode refresh, or automatic refresh in battery backup mode, maintaining data indefinitely without additional command, and resulting in the RAM appearing totally static to the system. Common data I/O and independent chip select and output enable controls permit easy interface to either separate or multiplexed address and data bus systems. The device is fully TTL compatible on all inputs and outputs.

Additional characteristics include 128 refresh cycles over a 2-ms refresh period, automatic precharge for minimum cycle time, and a substrate bias generator included onchip. There are three models: the MK4816-1 with a 120-ns access time and a 215-ns cycle time; the -2 with a 150-ns access time and a 270-ns cycle time; and the -3 with a 200-ns access time and a 360-ns cycle time. These memories, available in 28-pin packages, are compatible with industry standard ROM, P/ROM, and EPROM pin configurations.

Circle 353 on Inquiry Card

CMOS ADCs Guarantee Accuracy to 12 Bits

Believed to be the first analog-to-digital converters to offer guaranteed 12-bit accuracy, 8-bit microprocessor compatibility, and TTL or CMOS logic output, two CMOS hybrid successive approximation devices are available in both commercial and military models. These ADCs, produced by Beckman Instruments, Inc, 2500 Harbor Blvd, Fullerton, CA 92634, provide 3-state outputs, facilitating a variety of busing schemes for the data bit outputs, as well as a serial register output and end-of-conversion output.

Series 7555 provides an A-D building block that includes a successive approximation register, switch and clock chip, thin-film ladder network, and input scaling resistor. It allows the external addition of a comparator and any reference between ±10 V. Series 7556 is a complete ADC, including the 7555 circuitry, a high speed comparator, and a precision −10-V reference. It provides a full 12-bit conversion in 50 μs while typically consuming only 200 mW.

An output of 12 data bits from one of these ADCs is separated into a 4-bit MSB and 8-bit LSB byte. Each bit grouping has a separate inhibit line—low byte inhibit for LSBs and high byte inhibit for MSBs—to control when each group drives an 8-bit microprocessor data bus.

One-half LSB linearity (±0.012% FSR) is guaranteed for temperatures ranging from 0 to 70 °C (commercial version) and −55 to 125 °C (military version). Worst case limits are specified for initial gain setting error and gain error temperature coefficient. Zero offset and zero offset temperature coefficient are also guaranteed.

Both serial and parallel outputs are available with the serial register output outputting data after each bit decision. The parallel output word is available after the rise of the end-of-conversion output. All digital outputs can drive TTL or CMOS gates depending on the supply voltage levels chosen.

Circle 354 on Inquiry Card

Fully Static 32k CMOS ROM Features Industry Standard Pinouts

Featuring TTL compatible I/O, a single 5-V power supply, and CMOS technology, this 4k x 8 read-only memory requires no clock input.

Cut yourself in on the best buy in the industry.

It's no surprise that Western Union and other new distributors and customers chose Infoton data display terminals to help maintain their edge in the marketplace. Because, any way you cut it, the Infoton line delivers reliability, versatility and economy unmatched in the industry.

To learn more about Infoton data display terminals and what they'll do for you, cut out this coupon today. Mail it to Barbara Worth c/o Infoton, Second Avenue, Burlington, MA 01803. And see us at Interface '79, Booth 1040.

Name_____ Title_____

Company_____

Address_____

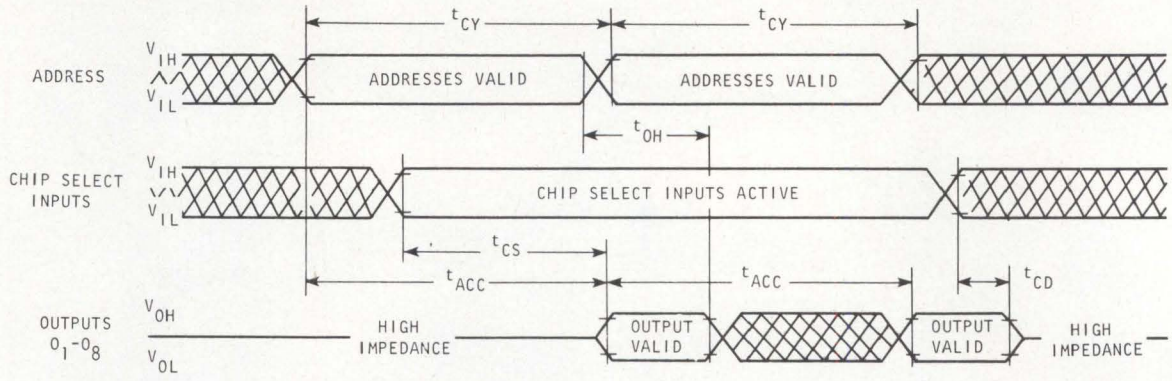
City_____ State_____ Zip_____

Telephone_____

CD-4

Created by Chickering/Howell Advertising, Los Angeles

CIRCLE 86 ON INQUIRY CARD



Read cycle timing for CM3200 ROM from Supertex. Maximum intervals are: address access time, t_{ACC}, 450 ns; chip select time, t_{CS}, 200 ns; chip deselect time, t_{CD}, 200 ns. Minimum intervals are: previous output valid after address change, t_{OH}, 50 ns; cycle time, t_{CY}, 450 ns

Maximum access time and minimum cycle time both equal 450 ns.

Additional characteristics include two mask programmable chip selects, a typical supply current of 10 mA during operation or 10 μA on standby, and a 3-state capability (allowing multiple devices on a common bus). The CM3200 from Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94086 is suited to microprocessor based or battery operated systems. It interfaces easily with TTL circuits, with each output able to drive one standard TTL load.

The 12 address inputs are decoded onchip to select 1 of 4096 words of 8-bit data. Chip select inputs are programmable to be either active high or active low level, and when both are active the eight outputs are enabled. However, when either of the inputs is not active, the outputs are in a high impedance state. All of the eight outputs must be enabled by both chip select controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled.

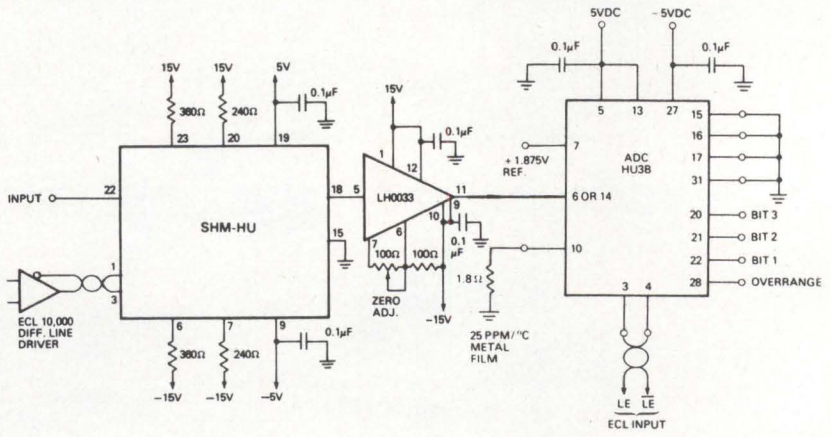
This device is designed for high density asynchronous fixed memory applications such as lookup logic tables and microprogramming. It is pin compatible with the Intel 2708, TMS 2708, and TMS 4732.

Circle 355 on Inquiry Card

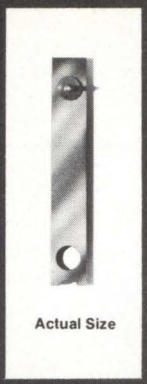
Sample/Hold Provides Signal Processing At Video Speeds

Having a 25-ns acquisition time for a full-scale 5-V input change to 0.2%, a sample/hold is specifically designed for ultrafast sampling applications such as in video data conversion. This thin-film hybrid device has a 50-MHz bandwidth in sample or track mode, functions with up to 8-bit accuracy, and has an output slew rate of 200 V/μs. The SHM-HU from Datel Systems, Inc, 11 Cabot Blvd, Mansfield, MA 02048 was designed for use with the ADC-HU3B analog-to-digital converter by the same manufacturer, but is compatible with other ultrafast ADCs of similar resolution capability.

Input and output voltage range is ±2.5 V with a gain of 0.955; accuracy is 0.1%. The circuit is designed to mate with an LH0033 out-



Sample/hold SHM-HU from Datel Systems is shown in connection with ADC-HU3B analog-to-digital converter. Although specifically designed for use with this ADC, sample/hold can operate with other ultrafast ADCs of up to 8-bit resolution



Actual Size

From an elegantly simple print mechanism based on this unique leaf spring hammer and advanced matrix line printing technology . . . print quality and reliability no other impact printer can match . . . plus full plotting capability at no extra cost that band, drum or chain printers can't provide at any price.

PRINTRONIX..today's 'First Family' in medium speed impact printers.

In 1975, Printronix introduced the first printer designed to fill the need for medium speed impact printing at practical prices. The unique concept and design of this matrix impact line printer brought unequalled print quality to impact printing. Its elegant simplicity, with up to 50% fewer parts than band, drum or chain printers, also established proportionately higher levels of reliability. Today, they are available in 150, 300 and 600 line-per-minute models priced about the same or less than medium speed band, drum or chain printers. They're warranted for one full year while 90 days is typical for others. And they all offer you one feature band, drum or chain printers can't: full graphics plotting capability. Get acquainted with our family. You might be captivated by their cost/performance and cost of ownership attributes. They're all up for adoption. Printronix, Inc., 17421 Derian Ave., P.O. Box 19559, Irvine, CA 92713. (714) 549-8272. TWX: (910) 595-2535.

PRINTRONIX

CIRCLE 87 ON INQUIRY CARD

150 lpm **P150**

300 lpm **P300**

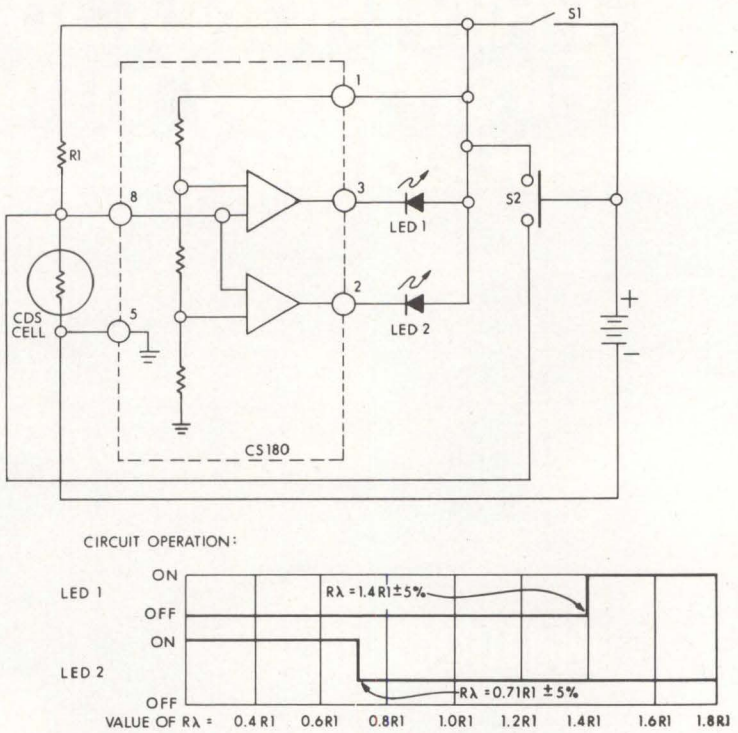
600 lpm **P600**

put buffer amplifier, which must be provided externally, and the circuit is zeroed by adjusting the offset of this external device.

Other important specifications include a differential ECL input for sample control, 1-MΩ input impedance with 5-μA input bias current, and ±10-mA output current. Aperture delay time is 6 ns and aperture uncertainty time is 10 ps. Hold mode droop is 50 μV/μs, and hold mode feedthrough is 0.02%. The device contains its own internal hold capacitor.

Four versions, designated as SHM-HUGC/MC/MR/MM, are available for different operating temperature ranges. The GC model with an epoxy package seal and the MC with a hermetic seal operate over 0 to 70 °C. A −25 to 85 °C range characterizes the MR, while the MM operates over −55 to 125 °C; both of these models have hermetic seals. All of the devices are packaged in 24-pin ceramic cases. Absolute maximum ratings limit power supply inputs to ±6 V, analog input vo.tage to ±5 V, sample inputs to ±5 V (differential), and current input to 50 mA.

Circle 356 on Inquiry Card



Use of CS-180 window comparator from Cherry Semiconductor is indicated in operating circuit for camera iris control. Graph shows on/off conditions as function of photocell resistance, Rλ, normalized to value of exposure reference resistor, R1

Window Comparator Is Implemented Onchip For Manual Aperture Control

Two outputs are provided by a monolithic integrated voltage comparator; one output is energized when the input voltage exceeds an upper window limit, the other when it falls below a lower window limit. Both outputs are abruptly disabled, regardless of input condition, when Vcc falls below a predetermined level. This feature can be used as a battery tester in battery operated applications.

Available from Cherry Semiconductor Corp, 99 Bald Hill Rd, Cranston, RI 02920, the CS-180 was designed specifically for manual aperture control in cameras, but can be utilized in many other applications when a bi-level voltage comparator is required. Its outputs are current regulated to operate LED indicators directly without limiting resistors, even at Vcc values that exceed the LED forward voltage by only 150 mV. The IC will withstand reversal of the power supply to the maximum rated voltage.

Absolute maximum ratings require that Vcc not exceed 6.5 V and that input and output voltages not exceed Vcc. Operating temperature must stay between −20 and 70 °C. The device is provided in a standard 8-pin plastic DIP.

Circle 357 on Inquiry Card

Digital Thermometer and Temperature Controller Are Combined On One Chip

Able to accept inputs directly from a thermistor temperature sensor and to drive LED or LCD devices without interface circuitry, a universal digital thermometer/controller microcircuit is usable in a wide variety of applications, with different thermistor types. The AY-3-1270, produced by General Instrument Corp Microelectronics, 600 W John St, Hicksville, NY 11802, will measure the temperatures found in domestic and commercial equipment and present them on display panels. This circuit can be used as the key element in a digital voltmeter with ±399 range and digital autozero.

The chip uses a single ramp conversion technique to measure the imbalance of a thermistor bridge temperature sensor. A digital autozero system, which operates on every other measurement cycle, is employed to compensate for offsets in the comparators.

Capabilities include leading zero blanking, an accuracy of ±1.0 °C

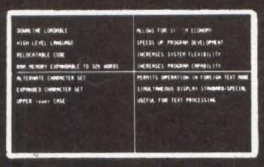
DELTA DATA introduces a new era in video display terminals

A *programmable terminal* for OEM's and large system users...

A *multifunctional terminal* for applications in distributed data processing and office environments of the future...

A *powerful, high performance terminal* that offers an intelligent choice for your special terminal requirements.

Introducing the new DELTA 7000 Series. A family of intelligent terminals which combines the latest 16-bit microprocessor technology with our own proven video display technology. We designed the DELTA 7000 with your interests in mind—from data communications (TTY/IBM 3270 emulation) to specific applications (Text Processing). Then we built in many special features, and loaded the DELTA 7000 with memory to handle your unique applications programs—at a most attractive price.

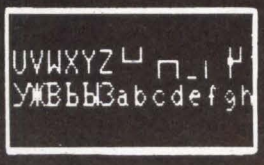


MULTIPLE SPLIT SCREEN
allows you to divide the screen into independent display areas

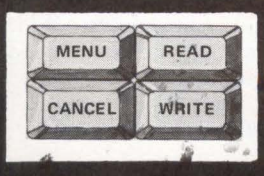
PARITY	PRINT SPEED
BAUD RATE	ASCII/EBCDIC
BLOCK/TTY	SCREEN SPLITS

+ MANY OTHERS

ELECTRONICALLY ALTERABLE ROM
allows status to be set from keyboard or remotely, and retained during power off



EXTENDED CHARACTER SET
generates special fonts and displays up to 672 different characters



MULTI-CHARACTER FUNCTION KEYS
permit one key to display or send a string of multiple characters or codes

Enter your new era in video displays with the new DELTA 7000. Write or call for more information today.

Delta Data Systems Corporation

Woodhaven Industrial Park
Cornwells Heights, PA 19020
(215) 639-9400

U.K. Subsidiary:
DELTA DATA SYSTEMS LTD.
Welwyn Garden 33833

Service in over 150 locations in the U.S. and 14 European countries and Canada.

CIRCLE 88 ON INQUIRY CARD

from 0 to 30 °C (using a thermistor temperature sensor), and a measurement and control range of ±39.9 °C. Power requirements are not critical —a single 9-V, 40-mA voltage supply suffices. The package is a 40-lead dual-inline type, suitable for use in ambient temperatures from −25 to 70 °C.

This n-channel MOS IC provides two control outputs, one of which operates when the reading is higher than the set point, the other when the reading is lower. The switching hysteresis is presettable as required. In addition, 0.05° display hysteresis has been introduced to prevent control output and LSD jitter. An optional power failure detection circuit is provided. At power-up the chip will read normally for about 10 s actual time determined by an external capacitor—then it will store the last reading and flash the display. In this condition the chip will continue to make measurements and operate the control outputs normally. Operating the reset button will restore the normal display. If there is a short duration power failure the circuit will ignore it, but if it lasts longer than 10 s the alarm condition will occur.

Circle 358 on Inquiry Card

Instrumentation Amps Offer 11 Binary Gains

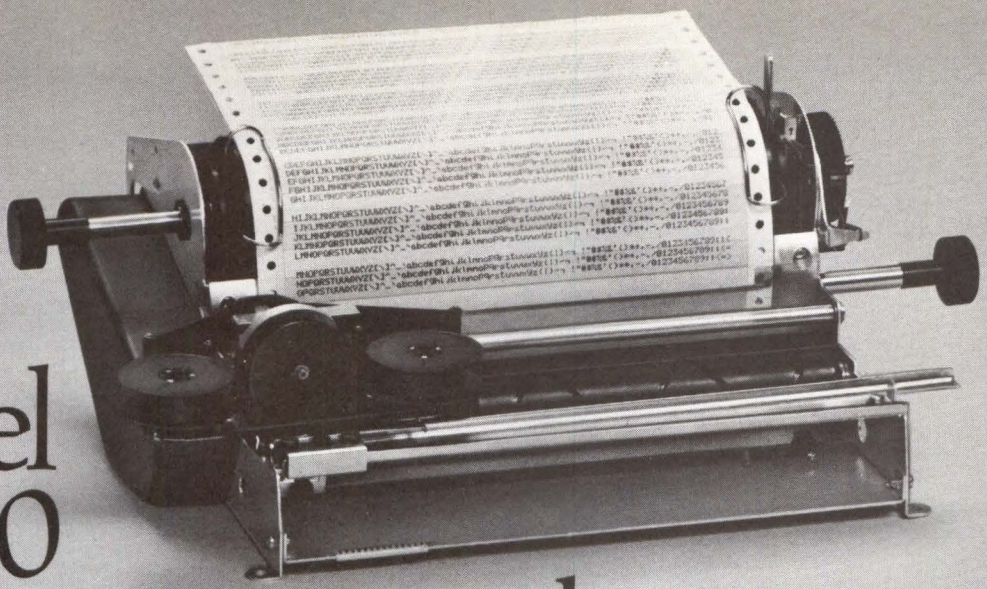
A self-contained, pin-programmable gain instrumentation amplifier provides a full range of gains, from 1 to 1024 V/V in binary weighted steps. Internal laser-trimmed thin-film gain setting resistor networks provide longterm temperature stability for the 3607, produced by Burr-Brown, PO Box 11400, Tucson, AZ 85734.

Inputs from 10 mV to 10 V can be accommodated while good resolution and accuracy are maintained. For example, the 2^{10} gain range of the device combined with the 2^{10} range of a 10-bit ADC produces a total system resolution of 2^{20} or one million to one.

Among the characteristics of the device are a 10-GΩ input impedance, gain errors of 0.02% max, and gain tempco of 10 ppm/°C max. At a gain of 1024 V/V, gain nonlinearity is 0.01% max, common-mode rejection is 110 dB min, max offset voltage drift is 1 μV/°C, RTI, and max offset voltage is 22 μV, RTI (2 mV at a gain of unity).

Change in offset voltage is only ±25 mV max when gain is shifted. This performance is accomplished without external adjustments. With a single offset adjustment, the change is limited to less than 2 mV (1 mV, typ) over the total gain range.

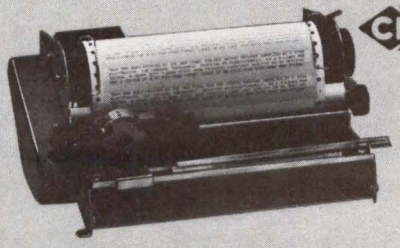
Circle 359 on Inquiry Card



The new Model 830 impact print mechanism has something extra going for it.

The new Model 830 bi-directional impact print mechanism may be just what you've been waiting for. It's a low-cost, 80-column dot-matrix mechanism with a printing speed of 125 CPS and a continuous-duty 7-wire head with a life expectancy of 100 million characters. Its straightforward, simple design makes it both highly reliable and cost efficient. In fact, it's just about the perfect OEM unit for general purpose computers, communication terminals, data loggers and micro computers. Its sprocket paper-feed mechanism accepts multi-ply pin feed paper in any width from 4.5" to 9.5"; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 830 is also available as a self-contained printer. Furthermore, it's from C. Itoh Electronics, Inc. — a name synonymous with excellence in printers. Write for detailed specifications today.

It's from C. Itoh.



Model 820, 150 cps and 9.5" paper width, also available.

C. Itoh Electronics, Inc.

5301 Beethoven Street, Los Angeles, CA 90066
Call: (213) 390-7778 • Telex: WU 65-2451

East Coast
280 Park Avenue, New York, NY 10017
Call: (212) 682-0420 • Telex: WU 12-5059

C. Itoh Electronics is part of the 119-year-old C. Itoh & Co. Ltd., world-wide trading organization.

Ac Linear Coupler Gives Electrical Isolation During Conversion

A gallium arsenide infrared emitting diode (IRED), optically coupled to a bipolar monolithic amplifier, converts an input current variation to an output voltage variation, while providing a high degree of electrical isolation between input and output. Said by its manufacturer, Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, to be the industry's first optically isolated ac linear optocoupler, MOC5010 offers 7500-V peak ac isolation and is UL recognized.

This device replaces a normal coupler, an operational amplifier, and a discrete transistor. It can be biased to maintain a linear output of up to 4 V peak-to-peak with a 12-V supply when current is applied. Other capabilities include 250-kHz (typ) bandwidth, 200 mV/mA gain, and low impedance, emitter-follower output of less than 200 Ω. Applications include telephone line coupling, peripheral equipment isolation, medical electronics, and audio uses.

Maximum ratings for the IRED (at 25 °C) include a 3-V reverse voltage, a 50-mA peak forward current, and a 100-mW power dissipation. The upper allowable limits for the ac amplifier (also at 25 °C) are a 15-V supply voltage, 13-mA supply current at Vcc = 12 V, and a 200-mW power dissipation, which is also the absolute maximum dissipation for the device as a whole. Maximum operating temperature is 85 °C and storage temperature must remain between −55 and 100 °C. The unit is provided in a 6-pin plastic DIP.

Circle 360 on Inquiry Card

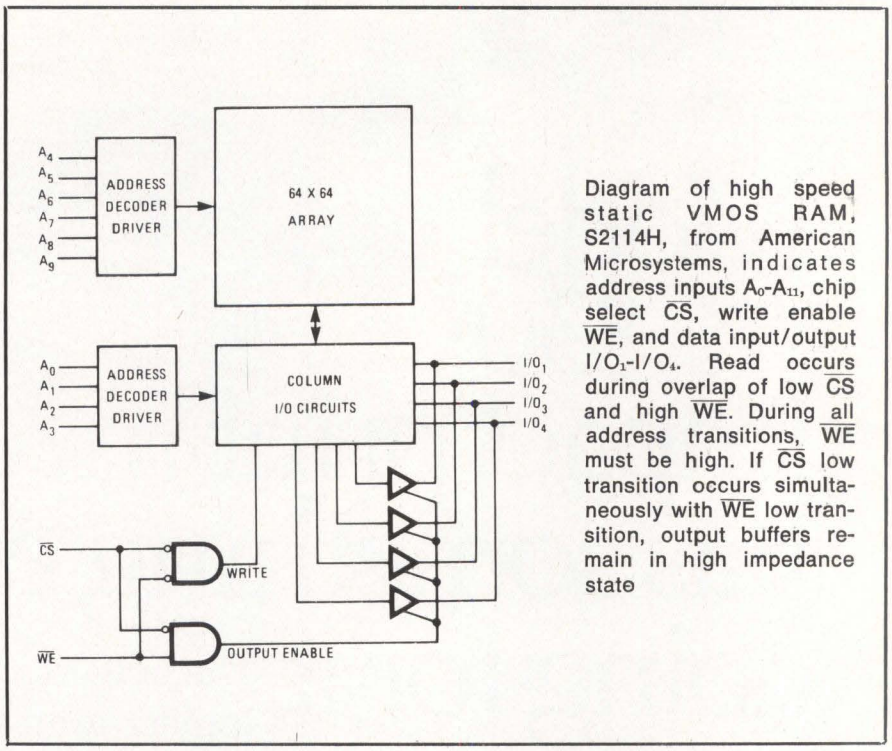


Diagram of high speed static VMOS RAM, S2114H, from American Microsystems, indicates address inputs A_0-A_{11}, chip select $\overline{CS}$, write enable $\overline{WE}$, and data input/output I/O_1-I/O_4. Read occurs during overlap of low $\overline{CS}$ and high $\overline{WE}$. During all address transitions, $\overline{WE}$ must be high. If $\overline{CS}$ low transition occurs simultaneously with $\overline{WE}$ low transition, output buffers remain in high impedance state

High Speed Static RAM Uses VMOS Technology

A static random-access memory with a max access time of 70 ns, the S2114H is a high speed version of the earlier S2114. The faster device is intended for high speed cache and buffer memory applications.

Its characteristics include a 1k x 4 organization, TTL compatibility on all inputs and outputs, single 5-V power supply, and common data I/O with 3-state outputs. The VMOS device from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 requires no clocks or refresh cycles. This simplifies device operation, since no address setup times are required. The chip select function facilitates memory system expansion by allowing the I/O pins to be OR-tied to other devices.

Absolute maximum ratings limit ambient temperature under bias to the −10 to 80 °C range and storage temperature to the −65 to 150 °C range. Voltage on any pin with respect to ground must stay between −0.5 and 7 V, and power dissipation must not exceed 1.0 W. The device is provided in 18-pin plastic or ceramic packages.

Circle 361 on Inquiry Card

Op Amps Offer High Slew Rates

A typical slew rate as high as 60 V/μs and a 3-MHz gain-bandwidth product characterize a family of operational amplifiers, produced by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086. The devices, available in dual as well as single monolithic circuit configurations, and having industry standard pinouts, are internally compensated to allow direct replacement of general purpose amplifiers in system performance upgrading.

These op amps are available in several versions, with 4-digit designations indicating dual configurations, while 3-digit designations indicate single monolithic circuit configurations; versions specified over the commercial range have NE prefixes, and versions specified over the military range have SE prefixes.

A 2-mV maximum offset voltage applied to each of the device types yields guaranteed slew rates of 25 V/μs (35 V/μs typical) for the NE/SE530 or NE/SE5530, 10 V/μs (15 V/μs typical) for the NE/SE535 or NE/SE5535, and 40 V/μs (60 V/μs typical) for the NE/SE538 or NE/SE5538. The input bias current for all device types is 60 nA max. Other features are large common mode and differential voltage ranges, offset null capability, and short-circuit protection. □

Circle 362 on Inquiry Card

A Three-Day Advanced Workshop

managing technical projects & programs

May 15-17, 1979 Colonial Hilton Inn, Wakefield, Massachusetts

Co-Sponsored by
Polytechnic Institute of New York & Institute for Advanced Professional Studies

This workshop for experienced project or department managers will enhance your program management skills. Valuable techniques that enable the technical manager to better control cost, schedule and performance are discussed in lectures, case studies and business games. The workshop provides a highly interactive learning experience and will help you to:

- Plan and control projects more effectively
- Design a project organization
- Interface efficiently with support departments
- Motivate team members to increase project performance
- Communicate ideas and negotiate resources
- Deal with customers effectively

MAJOR TOPICS

- Program Management Concepts & Principles
- Organizing the Project Team
- Effective Program Planning & Control
- New Business Development
- Program Management Leadership
- Effective Conflict Mangement
- Team Building in Project Management
- Time Management

FACULTY

The workshop is led by two highly successful engineering managers with extensive industrial and teaching experience:

- Dr. Hans J. Thamhain, Manager of Program Management for GTE-Sylvania's telecommunication businesses.
- Mr. Philip F. Paul, Management Consultant and former Director of Systems Management for Honeywell's small and medium-scale product lines.

INSTITUTE FOR ADVANCED PROFESSIONAL STUDIES
One Gateway Center
Newton, MA 02158
(617)-964-1412

For complete details or assistance about courses, registration or discussion of in-house presentations, call Donald French at (617) 964-1412.

INSTITUTE FOR ADVANCED PROFESSIONAL STUDIES
One Gateway Center
Newton, MA 02158

( ) Please send me detailed course description

Name _____ Title _____

Company _____ Phone _____

Address _____

City _____ State _____ Zip _____

Is the real cost of your next disk controller being buried?

If you're about to buy a new micro-controller for your Mass Storage System, watch out for buried costs. Eighty-six percent of the real cost of a *nontransparent* disk controller could be spent in future upkeep of mainframe software. This means you could end up paying seven times the purchase price of that 'economical' controller you are now considering! As a money-saving alternative, consider the AED 8000 micro-controller. It *emulates* OEM disk controllers such as RP-03, RP-04 and RP-06, even if that hardware is changed through several generations. Think of the money saved by not having to write a software driver when you first get the controller; plus the additional savings you'll gain by not having to rewrite the driver each time your mainframe manufacturer releases a new OS. The AED 8000 controller not only runs all software for the emulated disk, without patches or software revisions, but also runs mainframe manufacturer's disk diagnostics. And the 8000 now interfaces with Storage Module Drives *including* Winchester Technology—all for a one time purchase price that is surprisingly low. Write or call our Marketing Manager today for the facts. He'll make your new controller's future look a lot brighter!

ADVANCED ELECTRONICS DESIGN 440 Potrero Ave., Sunnyvale CA 94086. Tel. 408-733-3555

Branch Offices: Boston (617) 275-6400, Los Angeles (714) 738-6688

CIRCLE 138 ON INQUIRY CARD

A Five-Day Seminar

testing microprocessor-based systems

June 11-15, 1979 Colonial Hilton Inn, Wakefield, Massachusetts

Co-Sponsored by
Polytechnic Institute of New York & Institute for Advanced Professional Studies

The increasing use of microprocessors and other complex LSI devices is creating significant problems for engineers responsible for testing products incorporating these components. Digital system designers can either contribute to the myriad of testing problems or help eliminate them.

This seminar/workshop, for design and test engineers, enables participants to coordinate microprocessor-based product design with production testing. Emphasis is placed on product design practices influencing testability, test equipment capabilities and limitations, as well as test programming and diagnostic software development.

A prominent faculty will conduct guest lectures, demonstrations and provide you with assistance on your work-related problems.

TOPICS

- Microcomputer system configuration and support chips
- Design practices influencing testability
- Nature of common faults in microcomputer-based systems
- Troubleshooting during development
  - Equipment, applications, capabilities, limitations
- Coordinating design with production test strategies
- Test programming and diagnostic software development
- Production testing equipment
  - Capabilities
  - Applications
  - Limitations
- Recurring and non-recurring costs
- Reducing testing costs
- Reducing delays in product introduction and manufacturing
- Field testing implications

INSTITUTE FOR ADVANCED PROFESSIONAL STUDIES
One Gateway Center
Newton, MA 02158
(617)-964-1412

For complete details or assistance about courses, registration or discussion of in-house presentations, call Donald French at (617) 964-1412.

INSTITUTE FOR ADVANCED PROFESSIONAL STUDIES
One Gateway Center
Newton, MA 02158

( ) Please send me detailed course description

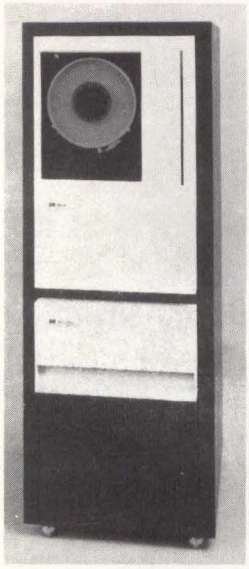
Name Title

Company Phone

Address

City State Zip

PRODUCT FEATURE



See at NCC Booth 3614

Tri-Density Recording Applied to Minicomputer Tape Subsystems

Writing and reading ANSI compatible 9-track magnetic tapes at three different densities can now be accomplished on a 3-speed tape subsystem designed for use with minicomputers. According to Storage Technology Corp, the 1935/1950 series formatter-controller/magnetic tape subsystem not only is the first minicomputer tape subsystem to provide tri-density operation in a single-drive configuration, it also incorporates a number of unique features not found on other minicomputer tape subsystems.

Subsystems can be configured for either tri-density (NRZI/PE/GCR), which requires an optional logic card, or dual density (PE/GCR). Densities for reading and writing in the three respective formats (NRZI/PE/GCR) are 800, 1600, and 6250 char/in (315, 630, and 2460 char/cm). Tape motion, controlled by the magnetic tape unit, is 50, 75, or 125 in (127, 190, or 318 cm)/s.

Features and Capabilities

Each magnetic tape subsystem consists of from one to four magnetic tape units (MTUs) in a radial bus organization, and a single formatter-controller unit (FCU). Separate MTUs can operate at different speeds and densities under control of a microprogrammed sequencer chip in the FCU.

Standard features of the MTU include single capstan tape drive, dual vacuum columns, automatic tape loading, dual gap read/write head and full width erase head, head azimuth adjustment, quick release positive action file reel hub, vacuum assisted tape cleaner plate, BOT and EOT marker sense, pneumatic noncontact file protect sensor, microprogram controlled sequencing and diagnostics, and self-contained modular power supplies. Optional features include power window and automatic file hub. All controls are easily accessible on the front panel and status indicators are readily visible.

There are no user adjustments on the FCU. The unit contains 19 logic cards and has 3 spare card slots for the user's channel interface electronics. (An external interface can optionally be used.) For service, the unit slides forward at a 90-deg tilt.

Rewind of a 2400′ (730-m) reel requires less than 1 min. During high speed rewind a separator removes the tape from the head to protect the tape and reduce wear on the head.

All key circuits are protected against overvoltage and overcurrent conditions. A microprogram sequence control chip has expanded sense and status capability. Up to 42 sense bytes are available from the tape drive.

MTU checkout and adjustment are controlled by an internal microcontroller. Switches and controls needed for maintenance are self-contained and available to service personnel but not accessible under normal operating conditions.

The extensive software diagnostic program is supplied because of the fail-soft tendency of GCR caused by extensive error correcting capabilities. Subsystem repair is aided by a 1.5M-byte software program. The diagnostic program runs over 700 tests covering function, reliability, artificial stressing, and fault isolation.

A hinged deck, which provides front and rear access to the MTU, allows all components to be serviced from the front without removal. Initial setup and functional offline testing and calibration can be accomplished through use of a resident field engineering panel on one of the logic cards.

General Specifications

The FCU is 10.5″ (26.7 cm) high and the MTU is 29.5″ (75 cm); both fit a standard 19″ (48.3-cm) RETMA rack. Input power can be selected as 100/117.5 Vac, 60 Hz or 220 or 240 Vac, 50 Hz. Operating altitude ranges are 0 to 2500′ (0 to 760 m) or 2500 to 6000′ (760 to 1830 m).

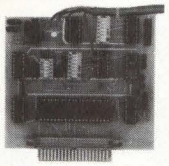
Price and Delivery

OEM quantity prices are $6600 for the model 1935 formatter-controller unit and $7950 for the model 1950 magnetic tape unit. Product quantities will be available in the fourth quarter of 1979. Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027. Tel: 303/497-5151.

For additional information circle 199 on inquiry card

TRS-80 E.S. SERIAL I/O

• Can input into basic • Can use LLIST and LPRINT to output, or output continuously • RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line • Requires +5, -12 VDC • Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010 C. No connectors provided, see below.



EIA/RS-232 connector Part No. DB25P $6.00, with 9', 8 conductor cable $10.95 Part No. DB25P9.

3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No. 3CAB40.

MODEM✲

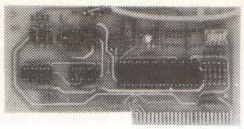
• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output-serial • Connect 8 Ω speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A

VERBATIM MINIDISK

Box of 10

$29.95

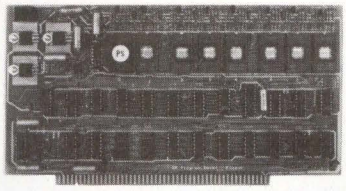
APPLE II✲ SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

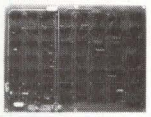
8K EPROM PIICEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. • S-100 bus compatible • Room for 8K bytes of EPROM non-volatile memory (2708's). • On-board PROM programming • Address relocation of each 4K of memory to any 4K boundary within 64K • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software available • Solder mask both sides • Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.



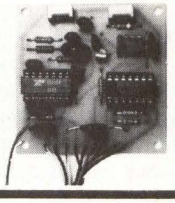
T.V. TYPEWRITER

• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A



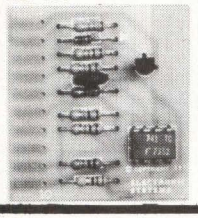
TAPE ✲ INTERFACE

• Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board only $7.60 Part No. 111, with parts $27.50 Part No. 111A



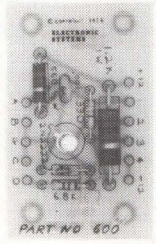
RS-232/ TTL✲ INTERFACE

• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin gold plated edge connector • Board only $4.50 Part No. 232, with parts $7.00 Part No. 232A 10 Pin edge connector $3.00 Part No. 10P



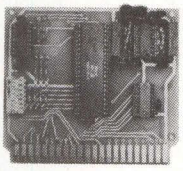
RS-232/ TTY✲ INTERFACE

• Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50 Part No. 600, with parts $7.00 Part No. 600A



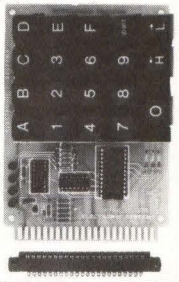
UART & BAUD RATE GENERATOR✲

• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P



HEX ENCODED KEYBOARD E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.

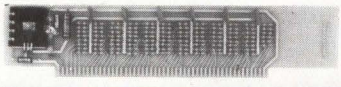


WAMECO INC. wmc inc.

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remic 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCBD $42.95
FPB-1 Front Panel. (Finally) AMSAI size hex displays. Byte or instruction single step. PCBD $42.95
MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCBD ..... $24.95, $168 Kit
QMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only ..... $34.95 $89.95 Kit
CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD .. $25.95 $89.95 Kit
RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD ..... $25.95, $60.95 Kit
EPM-1 1702A 4K EPROM card PCBD ..... $25.95 $49.95 with parts less EPROMS
EPM-2 2708/2716 16K/32K EPROM card PCBD ..... $24.95 $49.95 with parts less EPROMS
QMB-9 MOTHER BOARD. Short Version of QMB-12. 9 Slots PCBD ..... $30.95 $67.95 Kit
MEM-2 16Kx8 Fully Buffered 2114 Board PCBD ..... $25.95, $269.95 Kit

S-100 BUS ✲ ACTIVE TERMINATOR

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A



DC POWER SUPPLY✲

• Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp. • Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps. • Board only $12.50 Part No. 6085, with parts excluding transformers $42.50 Part No. 6085A

To Order: Mention part number, description, and price. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited. 24 Hour Order Line: (408) 226-4064

✲ Circuits designed by John Bell

For free catalog including parts lists and schematics, send a self-addressed stamped envelope.

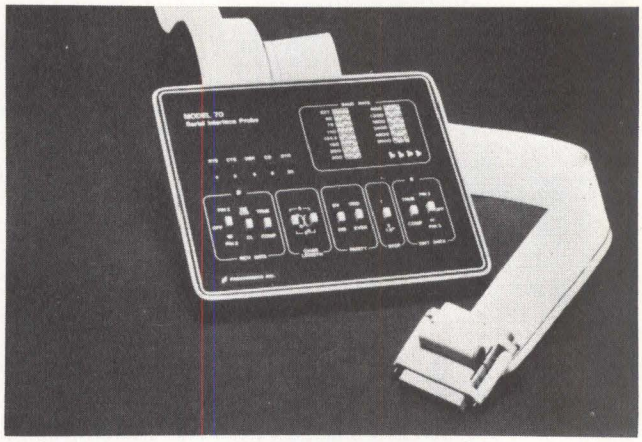
ELECTRONIC SYSTEMS Dept. CD, P. O. Box 21638, San Jose, CA USA 95151

PRODUCTS

Serial Interface Probe Converts Logic State Analyzer Into Testing Tool

Plugging into the model 532 intelligent logic state analyzer's A channel input port, the model 70 probe converts the analyzer into a tester for asynchronous RS-232 and 20-mA current loop interfaces. Connection to the B port permits monitoring of 16 channels of related parallel information. The probe simultaneously receives and transmits data. These modes operate in full duplex. In receive mode, the user can trigger on any char and store a 250-char sequence along with associated handshaking signals. Data are displayed on the analyzer's readouts in hexadecimal, or on an optional oscilloscope or terminal in hex or binary. For transmit mode, a software (P/ROM) option is required for the probe to send tests to a terminal or other serial device. Software also allows hexadecimal entry of custom messages of up to 256 char directly from the keyboard. **Paratronics, Inc,** 122 Charcot Ave, San Jose, CA 95131.

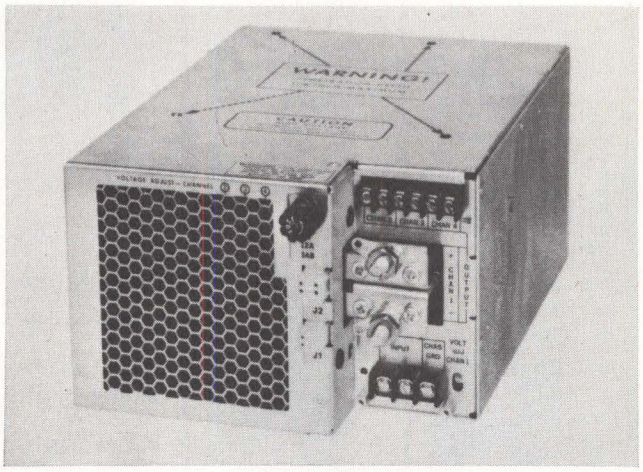
Circle 200 on Inquiry Card



Power Sources Suit ECL Systems Requiring Low Voltages at High Currents

Two UL recognized switching regulator supplies for mainframe computer, processor, and data communication applications provide up to 3 dc output channels, including a main power channel and ECL channel of 2 Vdc with ratings to 30 A. Model PM2575A has max power level of 375 W and PM2676A is rated at 600 W. Regulated outputs are supplied at full load over input voltage ranges of 92 to 138 or 184 to 250 V rms. Units operate efficiently for extended periods at inputs as low as 80 or 140 Vac depending on input voltage. During a power outage, output voltage holds for 30 ms for system shutdown. Overload, short-circuit, and reverse voltage protection; automatic overtemp shutdown; and paralleling capability are std. **Pioneer Magnetics,** 1745 Berkeley St, Santa Monica, CA 90404.

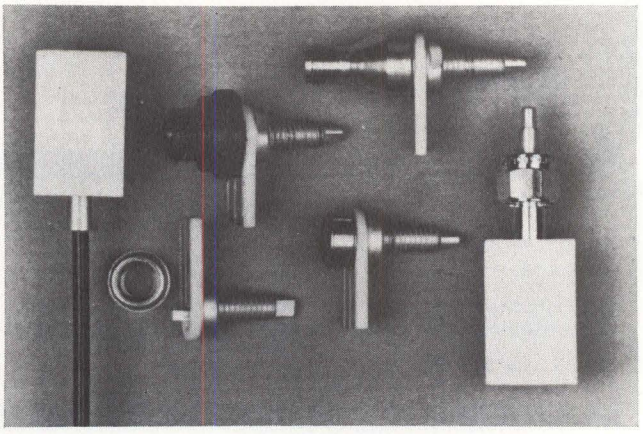
Circle 201 on Inquiry Card



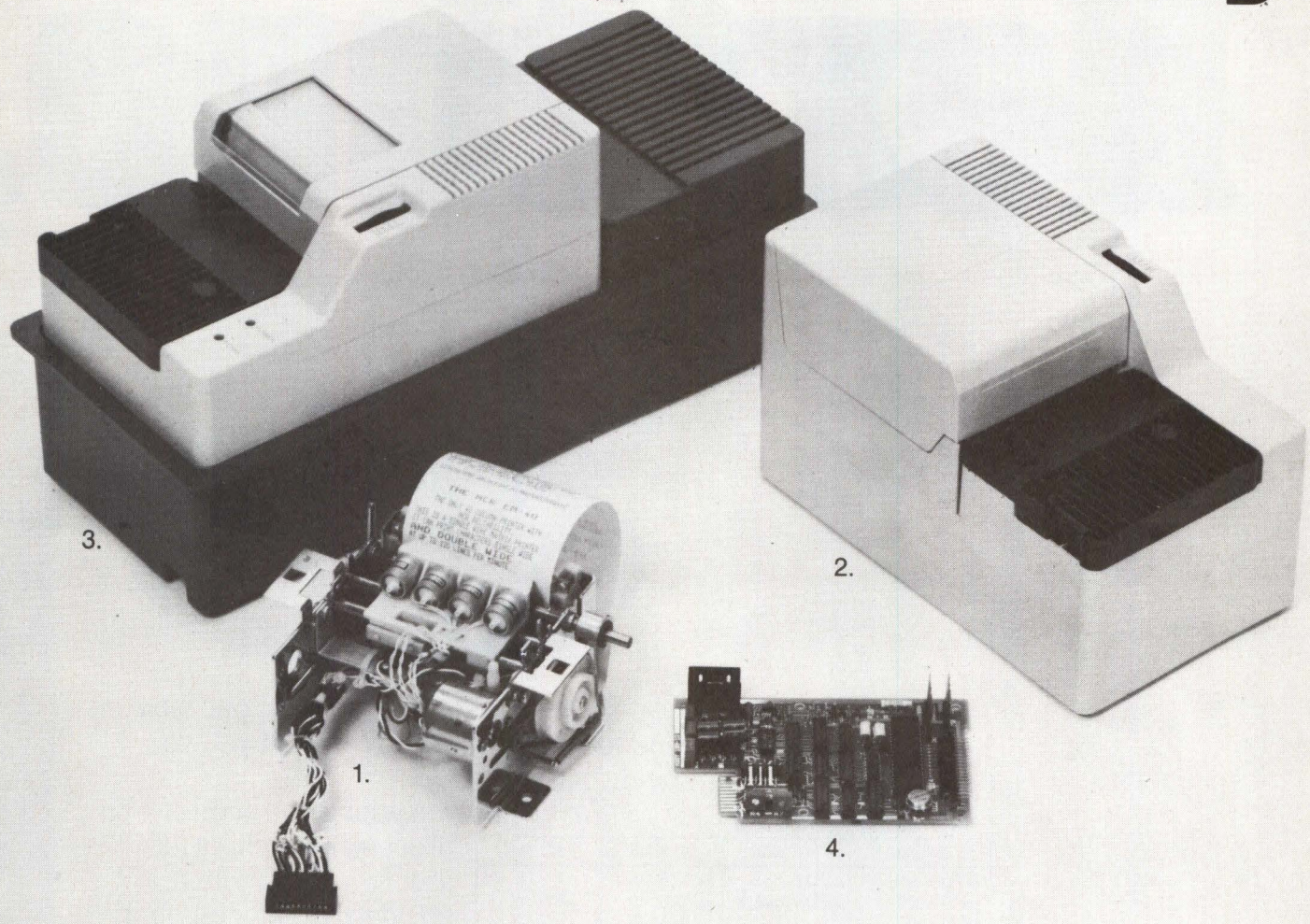
Laser Devices Increase Data Volumes in Communications and Information Processing

TAB-PAC and DI-PAC aluminum-gallium-arsenide laser devices enhance the amount of information used, stored, and communicated. Containing an integrated electronic feedback system for controlling and optimizing the laser's output, the units plug into PC boards in data processing systems or into optical fiber cables for use in communications. Each measures <1" (2.54 cm) and weighs about 0.2 oz (5.7 g). The lasers are powered by a flashlight battery or directly by microelectronic circuitry requiring only 0.2 W of electrical power. They are modulated at speeds >1G bits/s. Laser wavelengths can be selected to match specific application requirements. **Optical Information Systems, a div of Exxon Enterprises Inc,** Elmsford, NY 10523.

Circle 202 on Inquiry Card



Have it your way

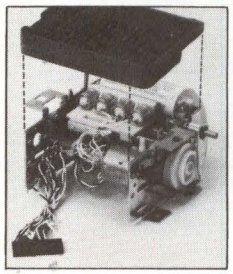


The only 40 column printer with NCR reliability now available almost any way you want it.

1. DIET SPECIAL — Mechanism only (low cost, field proven, available in quantity) add your own electronics.
2. TO GO — Cabinetized Version — comes in a handsome, well finished, gray case, for only a little extra lettuce.
3. BIG MECH — Mechanism (in a finished case) with its own power supply, with or without NCR electronics, packaged as a complete unit.
4. ON THE SIDE — NCR driven electronics, available with any selection.

For delivery information, prices, or literature, please contact:
NCR Engineering and Manufacturing
OEM Marketing
P.O. Box 627, Ithaca, New York 14850
(607) 273-6066.

Compare our ingredients and note the extra value of every unit served.



- Works as printer and/or plotter because of unique single wire design
- Multiple copy capability
- Prints up to 120 lines per minute
- Disposable ribbon cassette is operator changeable
- No messy spools or tricky threading

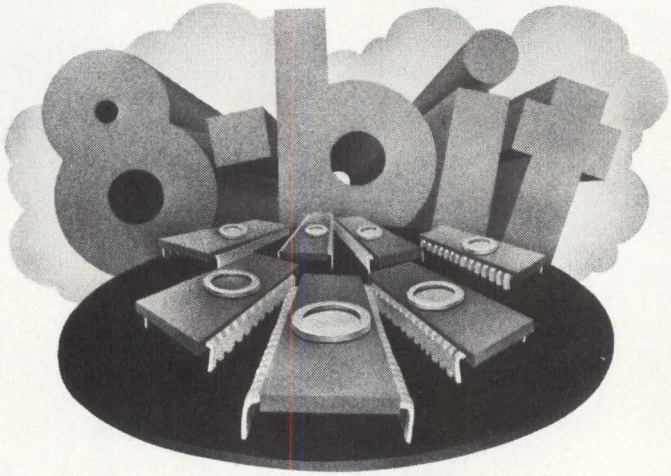
NCR

Engineering and Manufacturing — Ithaca

"Have it your way" is a reg. T.M. of Burger King Corporation, Miami, Florida, and is used with permission.

Who do you think of for a complete line of 8-bit microprocessors?

Next time,



If you haven't checked into our 8-bit line recently, take a look at what you've been missing.

We've got everything you need in 8-bit processors—plus a full assortment of industry standard peripherals and memories. And we've got them all in volume, ready to ship.

Not only do we support the entire 8080A family; we also offer the lower-cost single-chip 8048 family and the higher-performance 8085A series.

And for those with applications that require the capability of a Z80,™ we have the fully compatible μPD780—supported by the full family of 8080 peripherals.

Our 8-bit Families

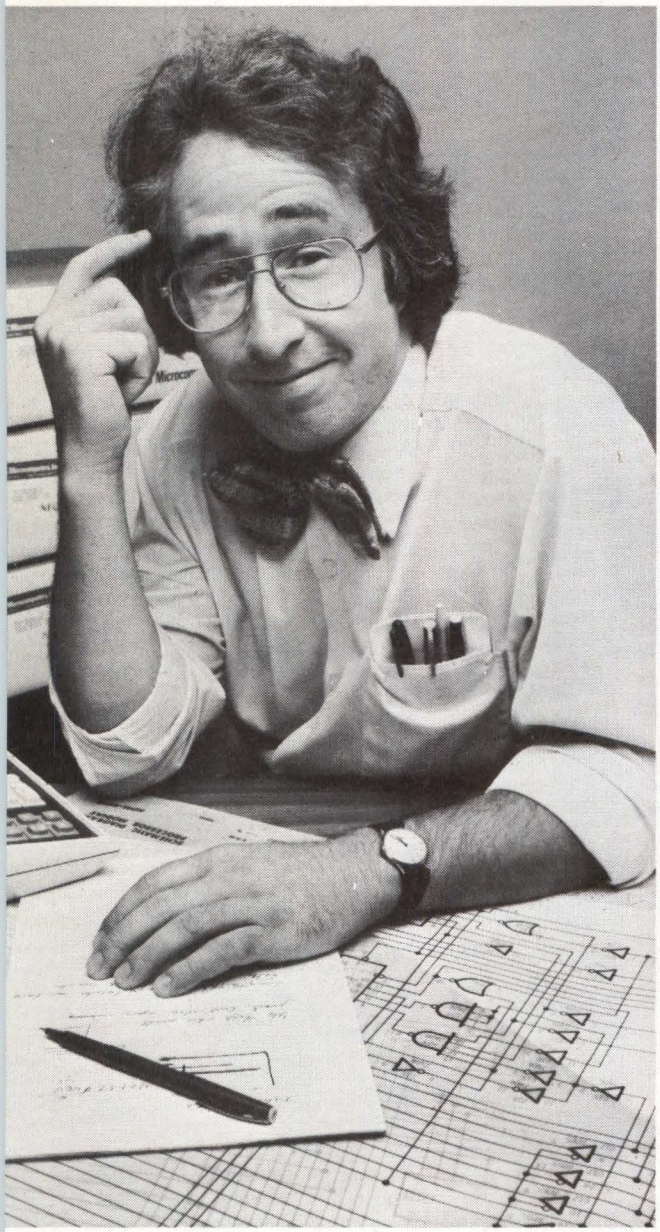
μPD 8080AF	μPD 8085A	μPD 8048	μPD 780
μPD 8080AF μPD 8080AF-2 μPD 8080AF-1	μPD 8085A μPD8085A-2	μPD 8048 μPD 8049 μPD 8039 μPD 8035	μPD 780 μPD 780-1
μPD 8041 →			→
	μPD 8155 →	→	
	μPD 8156 →	→	
μPB 8212 →			→
μPB 8214 →	→		→
μPB 8216/26 →	→		→
μPB 8224 μPB 8228/38			
		μPD 8243	
μPD 8251/A →	→	→	→
μPD 8253 →	→	→	→
μPD 8255/A-5 →	→	→	→
μPD 8257 →	→	→	→
μPD 8259 →	→	→	→
μPD 8279-5 →	→	→	→
	μPD 8355 →	→	
μPD 765 →	→	→	→

TM Zilog

REPS: Action Unlimited, Arlington, TX; Spring, TX. Burton-Medley Associates, Grandview, MO. Cerco, San Diego, CA. Contact Sales, Inc. Burlington, MA. D/Z Associates, Inc., Denver, CO. Electronic Innovators, Inc., Minneapolis, MN. Eltron, Phoenix, AZ. HLM Assoc., Northport, NY; Parsippany, NJ. Imtech, Inc., Cleveland, OH; Dayton, OH. Kaytronics Limited, Ville St. Pierre, Quebec; Downsview, Ontario; Surrey, British Columbia.L & M Associates, Pikesville, MD; Montpelier, VA. Harry Nash Associates, Willow Grove, PA. R.C. Nordstrom & Company, Lathrup Village, MI. Perrott Associates, Inc., Fort Lauderdale, FL; Clearwater, FL; Orlando, FL. Santana Sales, Costa Mesa, CA. Stone Component Sales, Waltham, MA. Technology Sales, Inc., Palatine, IL. Trident Associates, Inc., Sunnyvale, CA. Tri-Tronix, Albuquerque, NM. Tri-Tronix, NW., Mercer Island, WA. 20th Century Marketing, Inc., Huntsville, AL; Greenville, TN. Wolff's Sales Service Company, Raleigh, NC.

DISTRIBUTORS: Almo Electronics Corp., Philadelphia, PA, Baltimore, MD. Bell Industries, Bellevue, WA. Century Electronics, Albuquerque, NM; Wheatridge, CO; Salt Lake City, UT. Norman Davis Electronics, South Euclid, OH. Diplomat/Westland, Inc., Sunnyvale, CA. Diplomat/Southland, Inc., Clearwater, FL. Diplomat/Lakeland, Inc., Elk Grove Village, IL. Diplomat/IPC of Mass., Chicopee Falls, MA. Diplomat, Holliston, MA. Diplomat/Northland, Inc., Farmington, MI. Diplomat/Electro-Com

think NEC.

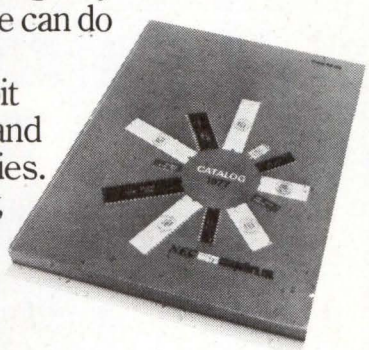


We can also fill your needs for a wide range of high-performance peripherals, including our IBM-compatible, double-density, double-sided floppy disc controller, the μPD765.

NEC not only means advanced technology and volume delivery; we also offer remarkable product reliability—thanks to experienced designers and meticulous manufacturing techniques, backed up by 100% burn-in and testing with MIL-STD-883 methods.

What's more, we give you thorough support—including documentation, design assistance, and product development services. And our engineers are always available to help with specific application problems.

Our new catalog will give you a better idea of just how much we can do for you, not just in 8-bit products, but also in 4-bit single-chip processors and 1K, 4K and 16K memories.



For your free copy, clip your business card or letterhead stationery to this page and send to:
NEC Microcomputers, Inc.,
173 Worcester Street, Wellesley, MA 02181.

If you haven't thought of NEC before, you will.

Next time.

NEC

NEC Microcomputers, Inc.

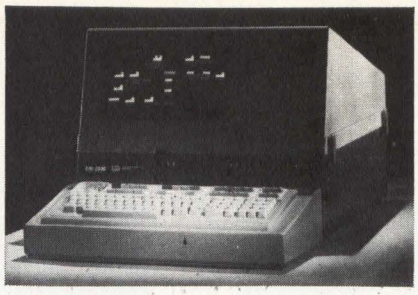
Corp., Minneapolis, MN. Diplomat/St. Louis, Inc., St. Louis, MO. Diplomat/IPC Corp., Totowa, NJ; Mt. Laurel, NJ. Diplomat Electronics Corp., Woodbury, NY. Diplomat/Alta-Land, Inc., Salt Lake City, UT. Future Electronics Corp., Montreal, Quebec; Rexdale, Ontario; Ottawa, Ontario. Hughes-Peters, Inc., Cincinnati, OH; Columbus, OH. Intermark Electronics, Sunnyvale, CA; Santa Ana, CA; San Diego, CA. Kent Electronics, Houston, TX. G.S. Marshall, Sunnyvale, CA; Irvine, CA; El Monte, CA; San Diego, CA; Phoenix, AZ. Milgray Electronics, Inc., Freeport, NY; Orange, CT. Reptron Electronics, Inc., Livonia, MI. Resco/Raleigh, Raleigh, NC. Semiconductor Specialists, Inc., Chicago, IL; Burlington, MA; Farmington, MI; Minneapolis, MN; Hazelwood, MO; Pittsburgh, PA; Dallas, TX; Milwaukee, WI. Sterling Electronics, Phoenix, AZ; Sun Valley, CA; San Diego, CA; Baton Rouge, LA; Waltham, MA; Albuquerque, NM; Dallas, TX; Houston TX; Seattle, WA. Summit Distributors, Inc., Buffalo, NY. Summit Elec. of Roch., Inc., Rochester, NY. Technico, Inc., Columbia, MD; Roanoke, VA. Western Microtechnology Sales, Sunnyvale, CA.

REGIONAL SALES OFFICES: Western Region, NEC Microcomputers, Orange, CA (714) 633-2980. Eastern Region, NEC Microcomputers. Melville, NY (516) 293-5660.

CD-1-3

PRODUCTS

TEMPEST CERTIFIED INTERACTIVE CRT TERMINALS



Certified to NACSEM 5100 Tempest limits and MIL-STD-461 ECM requirements, version of Hewlett-Packard 2640 series has achieved required shielding level by modifying only the external packaging, while retaining the same viewing clarity, electrical assemblies, performance characteristics, and specs of the original unit. Existing terminals can be retrofitted. **Bendix Communications Div,** E Joppa Rd, Baltimore, MD 21204.

Circle 203 on Inquiry Card

SINGLE-BOARD STORAGE MODULE DISC CONTROLLER

An intelligent single-board controller, SMC12 interfaces Data General compatible minicomputers with up to 4 storage module drives in any mix of capacities to 1200M bytes. Two computers with the controllers can share dual ported drives. Transfer rate is up to 1.2M bytes/s. Dual full sector RAM buffers allow single-command contiguous sector transfers to 64k words. Hardware error correction detects and corrects data error bursts up to 11 bits in one operation. **MiniComputer Technology,** 2470 Embarcadero Way, Palo Alto, CA 94303.

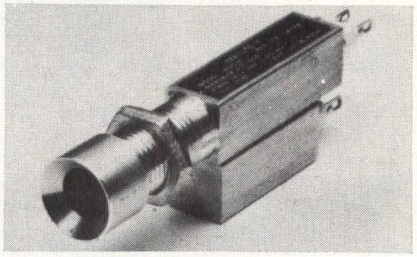
Circle 204 on Inquiry Card

BENCHTOP HIGH VOLTAGE POWER SUPPLIES

Two supplies are designed for precision laboratory high voltage applications. Bipolar model 214 outputs 0 to 1000 V at 15 mA and model 215 features polarity switch with LED indicators and outputs of 0 to ±3000 V at 5 mA. Proprietary linear circuit techniques result in 200-mV resolution, 0.001% regulation and ripple, and 50 ppm/°C tempco. The 5 x 7.625 x 7.25 (127 x 194 x 184-mm) units are arc protected, short-circuit proof, and self-restoring. **Bertan Associates, Inc,** 3 Aerial Way, Syosset, NY 11791.

Circle 205 on Inquiry Card

INDICATOR LIGHTS FOR ANALOG, DIGITAL DISPLAYS



The Varilite system uses a single indicator light that changes color, between the red and green portions of the spectrum, in response to variations in electrical input. No moving parts or color wheels are used. Either analog or digital information can be displayed, and the unit can be used in many applications where a meter or gauge is normally required to indicate a range of information. **Varilite Corp,** 222 Middle Country Rd, Smithtown, NY 11787.

Circle 206 on Inquiry Card

LARGE CAPACITY EPROM ERASING CABINETS

Spectroline PC-1000 erases up to 72, and PC-2000 up to 144 EPROM chips at one time in as little as 7 min. Both feature high intensity ozone-free 254-nm UV grid tubes with specular reflectors for uniform UV distribution. Other features include complete shielding, safety interlocks, conductive foam pads for holding chips and preventing electrostatic buildup, and 60-min timer for automatic shutoff. **Spectronics Corp,** 956 Brush Hollow Rd, Westbury, NY 11590.

Circle 207 on Inquiry Card

MICROPROCESSOR BASED KEYBOARDS

Microprocessor software controls 2-key and N-key rollover, tease protection, and repeat/auto repeat features with a min of hardware in the 6000 series, along with polling, scanning, and message transmission. Microprocessor power eliminates the basic failure mode problems associated with mechanical switching. A contact debouncing scheme provides clean output without limiting operator input speed. Electronic hysteresis eliminates switch tease and multiple char output problems. **Maxi-Switch Co,** 9697 E River Rd, Minneapolis, MN 55433.

Circle 208 on Inquiry Card

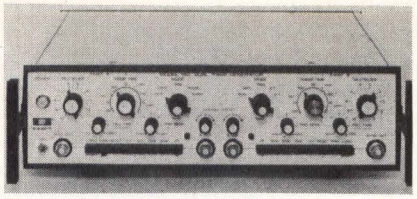
10-BIT SYNCHRO-TO-DIGITAL CONVERTER

Series of converter modules tracks input rates up to 36,000°/s with no added error. The 2.6 x 3.1 x 0.42" (66 x 78.7 x 10.7-mm) modules, designed to mount on PCBs, convert synchro or resolver inputs of 11.8 or 90 V at 400 Hz, or 90 V at 50 or 60 Hz into 10-bit parallel binary outputs representing angle with an accuracy of ±30 min of arc. Consuming 500 mW of power, converters provide TTL/CMOS compatible digital outputs and accept bidirectional input data. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.

Circle 209 on Inquiry Card

PRODUCTS

DUAL RAMP/RASTER GENERATOR

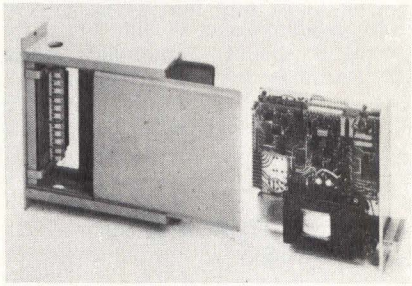


Two generators with ramp times of 1 μs to 1000 s within the model 180 can be operated independently or can be synchronized for 1:1, 2:1, or 4:1 interlace. Position and size controls, reverse sweeps, singleshot frames and fields, composite blanking pulses, and 2:1 and 4:1 vertical sweeps for interlace simplify raster generation. Two independent power amps offer ±10 V of variable dc offset, 80-dB step attenuation in 10-dB steps, and 20 dB continuously variable between steps. **Exact Electronics, Inc,** 6400 Signal St, Tillamook, OR 97141.
Circle 210 on Inquiry Card

HERMETICALLY SEALED DIGITAL DELAY LINE

Sealed in a metal 14-pin DIP, the -5001 withstands such severe manufacturing processes as wave soldering and freon degreasing. Available with a max delay from 25 to 250 ns (selected at time of order), unit offers 5 taps at 20% increments. Schottky buffered input/outputs provide a delay accuracy of ±2 ns/5%, true waveform reproduction, and standard digital fanouts. **Hytek Microsystems, Inc,** 16780 Lark Ave, Los Gatos, CA 95030.
Circle 211 on Inquiry Card

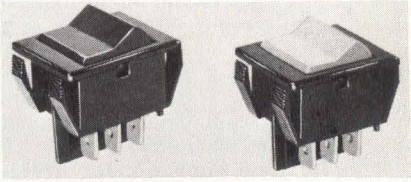
PROCESS CONTROL INSTRUMENTATION



Conditioning cards plugged into a basic motherboard build up units that accept many inputs; the optically coupled output signal may be any std current or voltage process signal. Up to 2 alarm points can be provided. Designed to withstand severe environments, the CATxT series features a transmitting analog alarm in the 0.1% accuracy class. A 0- to 10-V monitor outlet accepts a DVM or the company's Autocal handheld monitor. The auxiliary power supply may be 24 Vdc or 110 V/220 V 60 or 50 Hz. **Struthers-Dunn, Inc,** PO Box 1237, Bettendorf, IA 52722.
Circle 212 on Inquiry Card

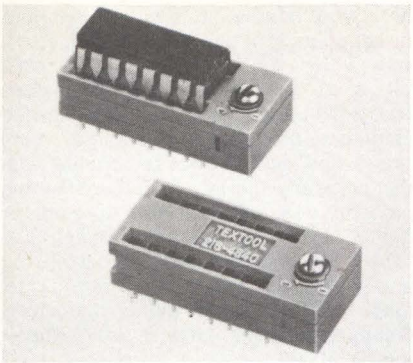
DOUBLE-POLE ROCKER SWITCHES

Snap-in panel mounting switches are UL listed and CSA certified for 10 A at 125 Vac, 28 Vdc inductive; 8 A at 250 Vac inductive, 0.5 hp; and 8 A at 14 V tungsten. The 0.25" (0.635-cm) slip-on terminals may also be soldered. Variations of double- and single-pole circuits, color combinations, metal bezels, illuminated versions, and hot stamping adapt switches to specific needs. Matching panel lights are also offered. **Chicago Switch, Inc,** 1714 N Damen Ave, Chicago, IL 60647.



Circle 213 on Inquiry Card

ZERO INSERTION PRESSURE IC SOCKETS



Econo Zip sockets are available in 16-, 24-, and 40-pin models, and are designed for mounting on std 0.100" (2.54-mm) centers on either axis. Additional device protection features include wide entry holes to accept bent or distorted leads, a screwdriver operated plastic cam for easy operation and prevention of accidental unloading, and long life. A device can literally be dropped into the socket; rotation of the cam to a built-in stop firmly retains the device with good electrical contact. **Textool Products, Inc,** 1410 W Pioneer Dr, Irving, TX 75061.
Circle 214 on Inquiry Card

SCIENTIFIC SUBROUTINE PACKAGE

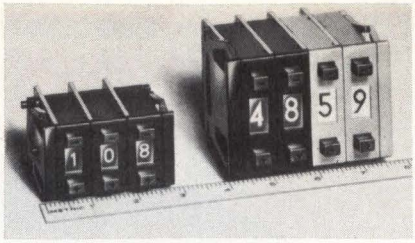
Written for microsoft extended and disc BASIC interpreters, including TRS80 level II BASIC, DPFUN is a 16-digit precision subroutine for engineering and scientific applications, with 13 double-precision exponential, logarithmic, trigonometric, and inverse trigonometric functions. Truncated continued fraction algorithms result in easily entered code, fast execution, and exploit precision available in 64-bit binary floating point notation. Complete subroutine set occupies approximately 2.5k bytes. **Miken Optical Co,** 53 Abbett Ave, Morristown, NJ 07906.
Circle 215 on Inquiry Card

MODEM/TERMINAL INTERFACE DEVICE

Elastic asynchronous-to-synchronous interface (EASI) unit is an option available with the company's 7201C, 7208, and 7296 modems which operate at 2400, 4800, and 9600 bits/s respectively. Device permits asynchronous data terminals to operate with medium and high speed synchronous modems without any speed-loss penalty. Usually supplied as standalone unit with standard EIA connectors, device is also available for the 7208 as a PCB to fit an existing card slot. **Tele-Dynamics Div, Ambac Industries, Inc,** 525 Virginia Dr, Fort Washington, PA 19034.
Circle 216 on Inquiry Card

PRODUCTS

THUMBWHEEL SWITCH WITH BIDIRECTIONAL PUSHBUTTON



Two fingertip plungers, 1 above and 1 below the legend (readout) area of the T55 series switch, control wheel indexing. Required max operating force is 300 g. A clear window covers the legend opening. Measuring 15 x 7.62 mm, the unit is recommended for logic level circuits not exceeding 50 V, 0.1 A. Black matte finish body has white legend on a black wheel (also available in gray). Output codes are BCD, BCD complement only, and single pole, repeating. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.

Circle 217 on Inquiry Card

RACKMOUNTED LIMITED DISTANCE MODEM

RM 3404 handles full-duplex synchronous operation over unconditioned 4-wire voice grade 3002 lines at 4800 bits/s. A dual-channel option enables two 2400-bit/s channels to be carried simultaneously over the same voice grade line and is line compatible with the company's LDM 404B freestanding modem. Features are point-to-point or digital multidrop operation using the LDS 3000 rack assembly; local analog and digital loopback plus remote digital loopback; and signal status indicators. **Gandalf Data, Inc,** 1019 S Noel, Wheeling, IL 60090.

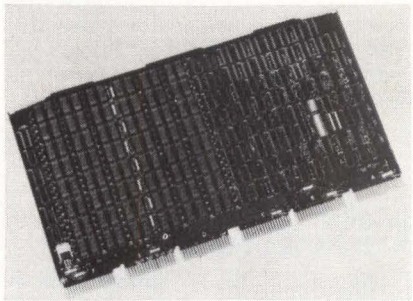
Circle 218 on Inquiry Card

10-MHz OSCILLOSCOPES

Single-trace LBO-513 and dual-trace LBO-514 oscilloscopes feature up to 1-mV sensitivity. Units have 8 x 10-cm displays, Z-axis modulation, 5X magnifier, and complete trigger controls. LBO-508 dual-trace scope also has front panel X-Y operation, ch-1/ch-2 trigger selection, and alternate or chopped display modes. **Leader Instruments Corp,** 151 Dupont St, Plainview, NY 11803.

Circle 219 on Inquiry Card

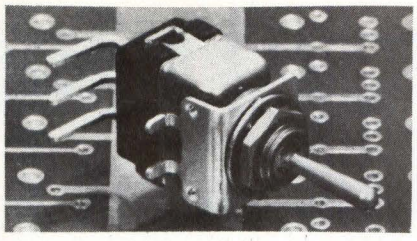
HIGH DENSITY MOS MEMORY FOR PDP-8/A



A hex card that plugs directly into a single CPU slot, the 128k-word x 12-bit PM-S8A is also available in 8 depopulated versions ranging from 112k to 16k words. Features include battery backup power provision and switch selectable addressing. The memory replaces DEC's MS8-C while providing increased capacity. It is hardware and software compatible with the computer and all DEC peripherals. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714.

Circle 220 on Inquiry Card

MIL-STD RIGHT ANGLE TOGGLE SWITCH



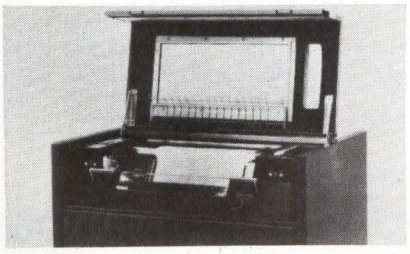
With right angle mounting for tight PCB packaging, units feature nonteasable, dry circuit capabilities, weld-breaking action, gold contacts and sealed bushing, and gold-plated silver contacts. Switches meet MIL-S-8834 requirements for high reliability applications in communications equipment, computer mainframe and peripherals, and navigation and guidance equipment test instrumentation. They are rated 5 A at 28 Vdc. **Aerospace Controls/Systems Div, Cutler-Hammer, Inc,** 4201 N 27 St, Milwaukee, WI 53216.
Circle 221 on Inquiry Card

SHAFTLESS OPTICAL ENCODER

Installing fully assembled and adjusted on an existing shaft, the V-Coder eliminates need for shaft, bearings, and coupling, enabling a 8 x 10^{-6} oz-in (5.6 x 10^{-8} N•m)/s^2 moment of inertia. Installation consists of pushing the encoder on the existing shaft, inserting and tightening mounting screws, and then pushing a thrust pin through an aperture in the case for several seconds while the shaft rotates. The thrust pin automatically aligns the encoder. Outputs include square wave in quadrature, English-metric, and index pulse. **Perrine, Inc,** Paraiso Hot Springs, Soledad, CA 93960.
Circle 222 on Inquiry Card

HIGH SPEED PRINTERS

600-, 900-, 1000-, and 1200-line/min 8080A microprocessor controlled Chain-Train printers serve data and word processing applications. CT-1200 series' horizontal moving font provides precisely aligned vertical print. Features include 132 print positions; 64-char ASCII set; built-in, offline test capability; adjustable paper path, and 6-part forms capability. **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.



Circle 223 on Inquiry Card

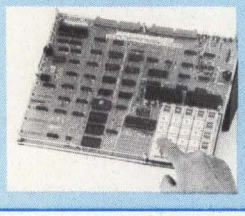
ADVANCED TECHNICAL EDUCATION

INTEGRATED COMPUTER SYSTEMS, INC.

1979 SPRING/SUMMER SCHEDULE

Course 160 — Four Days

Microprocessor Hands-On Workshop



ST. LOUIS May 1-4
NEW YORK May 8-11
SEATTLE May 15-18
TORONTO May 29-June 1
WASHINGTON D.C. June 4-7
BOSTON June 11-14
SAN FRANCISCO June 19-22
SAN DIEGO July 16-19

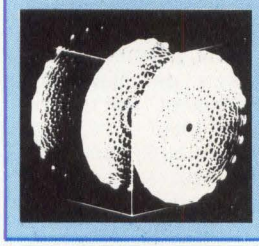
Course 203 — One Day

Military & Aerospace Microprocessor Systems

WASHINGTON D.C. June 8
BOSTON June 15
SAN DIEGO July 20
OTTAWA August 3

Course 365 — Four Days

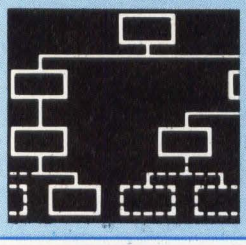
Computer Graphics



PHILADELPHIA May 1-4
SAN FRANCISCO May 8-11
SEATTLE May 15-18
ST. LOUIS June 5-8
TORONTO June 12-15
SAN DIEGO July 10-13
WASHINGTON D.C. July 17-20
OTTAWA July 24-27

Course 320 — Four Days

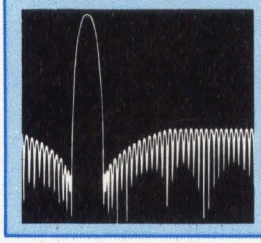
Structured Programming



DETROIT May 1-4
WASHINGTON D.C. May 15-18
CHICAGO June 5-8
TORONTO June 12-15
HARTFORD June 19-22
SAN FRANCISCO July 10-13
MINNEAPOLIS July 17-20
OTTAWA July 24-27

Course 412 — Five Days

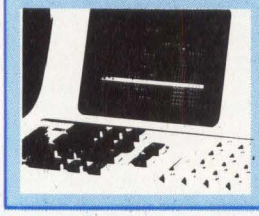
Digital Signal Processing



SAN DIEGO May 7-11
SAN FRANCISCO June 11-15
TORONTO June 18-22
MINNEAPOLIS July 9-13
OTTAWA July 16-20

Course 142 — Five Days

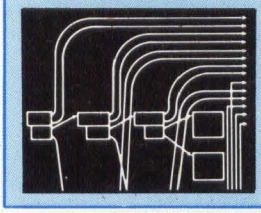
Troubleshooting Microprocessor-Based Systems



NEW YORK May 14-18
TORONTO June 25-29
SAN FRANCISCO July 9-13
SAN DIEGO July 23-27
MINNEAPOLIS July 30-August 3

Course 380 — Four Days

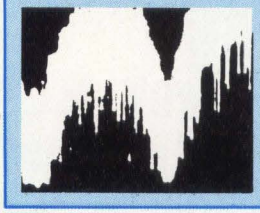
Data Base Management Systems



WASHINGTON D.C. May 8-11
LOS ANGELES May 15-18
TORONTO July 10-13
SAN FRANCISCO July 31-August 3
MINNEAPOLIS August 7-10

Course 444 — Four Days

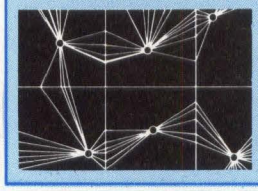
Spread Spectrum Communication Systems



WASHINGTON D.C. May 8-11
LOS ANGELES June 26-29
OTTAWA July 17-20
WASHINGTON D.C. July 24-27

Course 350 — Four Days

Distributed Processing and Computer Networks



ST. LOUIS May 1-4
SAN FRANCISCO May 8-11
CHICAGO May 15-18
TORONTO June 5-8
HARTFORD June 12-15
WASHINGTON D.C. June 19-22
SAN DIEGO July 10-13
OTTAWA July 17-20

Self-Study Microcomputer Training

Course 525A Microcomputer Hardware/ Software

Course 536A Microcomputer Interfacing Techniques

Course 565 Developing Microcomputer Software

Course 240 — Three Days

Small Computing Systems

LOS ANGELES May 2-4
WASHINGTON, D.C. May 9-11
BOSTON May 16-18
TORONTO June 6-8
SAN DIEGO July 25-27
OTTAWA August 1-3

EUROPEAN COURSE LOCATIONS

These courses, and other advanced technology courses, are also offered throughout the year in Paris, London, Copenhagen, Munich, and other European cities. For details, contact:

Course Enrollment Secretary
ICSP Inc. — BELGIUM
Avenue Jules César 2, Bte 2
1150 Brussels, Belgium
Telephone: (02) 762-6000
Telex: 846 62473

For **FREE BROCHURES** and detailed information, please contact: **Course Manager:**

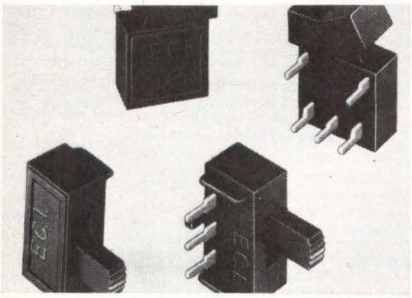
Integrated Computer Systems, Inc.
3304 Pico Blvd./P.O. Box 5339
Santa Monica, CA 90405
(213) 450-2060
(LOS ANGELES)

OR

Integrated Computer Systems, Inc.
300 N. Washington St./Suite 103
Alexandria, VA 22314
(703) 548-1333
(WASHINGTON, D.C.)

PRODUCTS

SIDE-ACTUATED SLIDE AND ROCKER SWITCH



Featuring a firm, positive detent in an enclosed molded housing, the low profile design is suited to video games and calculators. Its contact-terminal allows the slide switch to carry up to 6 A at 125 Vac; the rocker switch carries up to 10 A 125 Vac, for power switching applications. Single-pole 1 and 2 positions are available for PC mounting. PC standoffs molded on the switch housing and 2 dummy terminals on the rocker version supply stability when wave soldering. **Eldorado Components, Inc,** Clayton, NC 27520.
Circle 224 on Inquiry Card

SQUARE INCANDESCENT INDICATOR LIGHT

Designed to eliminate shadows, the SQI series uses Fresnel rings and striated lines for uniform light transmission, elimination of filament hot spots, and 180° viewing angle. The unit provides 20% greater viewing area than round lens devices. Cubelight installs in 6 s with light finger pressure. It snaps into a 0.25″ (0.63-cm) sq hole or gang mounts as a multiunit in a 0.25″ (0.63-cm) wide slot. Lamps insert into rear of lens, locking assembly into position. **Visual Communications Co,** PO Box 986, El Segundo, CA 90245.
Circle 225 on Inquiry Card

FLOPPY DISC CONTROLLER

Single-board model 400 is a DMA controller which operates on S-100 bus and uses IBM 3740 compatible soft sectored formatting. It will handle single-sided, double-sided, single-density, and double-density floppy drives and can manage up to 4 drives with overlapped seek to all. An onboard 1k-byte EPROM stores boot programs or other user defined applications. A proprietary phase locked loop design insures accurate reliable data recovery. **Industrial Micro Systems,** 628 N Ecihoff St, Orange, CA 92668.
Circle 226 on Inquiry Card

TERMINAL-HARDCOPY CONVERTER/INTERFACE

A vector to raster converter and electrostatic printer/plotter interface, Rasterizer™ produces hardcopy for the Megraphic 7000 vector refresh terminal in 10 to 15 s. The unit performs hardware conversion of vector information requiring no software preparation to order vectors. Both 100- and 200-dot/in (39.4 and 78.7/cm) resolution may be jumper selected for 11 or 20″ (27.9 or 50.8 cm) printer/plotters with 100-dot/in resolution on plotters up to 40″ (101.6 cm). **Megatek Corp,** 3931 Sorrento Valley Blvd, San Diego, CA 92121.
Circle 227 on Inquiry Card

PRECISION 10-V REFERENCES

R675 series 10-, −10-, and ±10-V models are available in 14-pin hermetic DIPs that are pin-for-pin equivalent to AD2700 units. The 10-V reference also is supplied in hermetic TO-99 packages. MIL-STD-883 models (-B) offers ±3 ppm/°C tempco for −55 to 125 °C operating range. Commercial/industrial models (-C) have ±5 and ±8 ppm/°C tempco for −25 to 70 °C and −55 to 125 °C operating ranges, respectively. Nominal supplies are within ±5 mV. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.
Circle 228 on Inquiry Card

60-CHAR/s MATRIX PRINTER

A low cost printer with high quality matrix character formation, the 3155 offers reliability in use with 8000 series interactive terminal systems where actual print time and number of displays accessing the printer are relatively low. Print mechanism prints 60 char/s unidirectionally at 10 char/in (3.9/cm), in line lengths up to 132 chars. Housed in desktop unit or on stand, device can be located up to 2000′ (609 m) from controller. **Harris Corp, Data Communications Div,** 16001 Dallas Pkwy, Dallas, TX 75240.
Circle 229 on Inquiry Card

SMALL COMPUTER SYSTEM

Key-Edit series 2 intelligent terminal systems offer floppy disc storage, large capacity CRT, and peripherals for off-line printing and communications. Basic model 22 features CPU with 64k-byte user memory, 1920-char CRT with keyboard, and dual floppy disc drives with 486k-byte capacity. Dual workstation model 24 drives four floppy disc drives with 972k-byte storage capacity; two printers and communications controller are available as options. Software features a high level user programming language. **Consolidated Computer International Inc,** 1604 S Edwards Dr, Tempe, AZ 85281.
Circle 230 on Inquiry Card

PRODUCTS

PORTABLE DATALOGGERS WITH RS-232 CAPABILITY

Interfacing with any RS-232 device, RS-10 converts data from internal digital clock, 10 analog inputs, and 32 bits of digital data to ASCII code at selectable baud rates. The RL-10, used in remote, unattended sites, transmits tape recorded data to a central location automatically, at predetermined time intervals. Front panel reads digital and analog data while scanning; when not scanning, it reads time. Scan control is switch selectable, manual, or by RS-232 control char. **A. D. Data Systems, Inc,** 200 Commerce Dr, Rochester, NY 14623.
Circle 231 on Inquiry Card

PRINTER INTERFACE CARD

Designed with two interfaces (one using Centronics parallel convention and interfacing with the company's 3779 and 3703 dot matrix printers, the other using daisy wheel parallel convention and interfacing with 3355 daisy wheel printer), PRI card has an individual cable connection to each. The daisy wheel interface has built-in ribbon lift and lowering circuitry to free software overhead normally required for this function. **Cromemco, Inc,** 280 Bernardo Ave, Mountain View, CA 94043.
Circle 232 on Inquiry Card

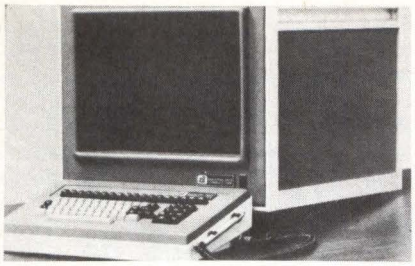
UNIVERSAL P/ROM PROGRAMMING SYSTEM

Use of permanently connected slaves eliminates need for changing personality modules and pinout adapters. Max of 15 slaves connects to program and/or test up to 240 components simultaneously. Smarty SM-100 master unit incorporates 2708/04 programmer; 8-, 16-, 32-, or 64k-bit P/ROM simulator; editor; and EPROM slave programs. Unit has RS-232-C and 20-mA current loop capabilities, 14 switch selectable baud rates from 50 to 9600, and checksum data RAM to insure data integrity. **Sunrise Electronics,** 307-H S Vermont Ave, Glendora, CA 91740.
Circle 233 on Inquiry Card

LOCAL DATA SETS WITH CONTENTION FEATURE

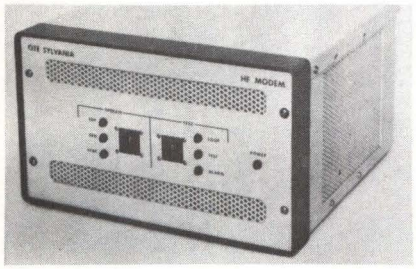
DS-10A local data sets incorporate contention feature Multishare, which monitors transmission line. If line is available, terminal transmits data allowing user to multipoint several terminals within a complex on the same line or port without use of protocol control. Operation is asynchronous, serial, full or half duplex over twisted pair at data rates to 19.2k bits/s for distances greater than 20 mi. Options include optical isolator module, synchronizer module, and MUX port extender. **Telecomm Automation Corp,** Box 283, Newtown, CT 06470.
Circle 234 on Inquiry Card

RUGGED GRAPHICS TERMINAL



ASCII sequences enable onboard capabilities of individual dot addressability for color and blink; automatic vector generation and color fill; realtime (downline loadable) special symbol graphics generation; and independent vector and alphanumeric scrolling with the IDT-100 terminal. Desktop and rackmount configurations are available. Monitor (either the company's ruggedized, permanently converged color monitor or other high resolution monitors) and video generator are mounted on a common chassis. **Industrial Data Terminals Corp,** 1550 W Henderson Rd, Columbus, OH 43220.
Circle 235 on Inquiry Card

HIGH FREQUENCY MICROPROCESSOR MODEM



Employing fast Fourier transform and digital filtering techniques to form multitone audio signals, modem performs arithmetic and digital operations with LSI TTL 4-bit slice arithmetic and logic units that are timeshared under program control. Internal computational accuracy is 16 bits, with double precision and block floating point techniques used for certain functions. Each processor function is program controlled, providing for efficient fault isolation, maintenance, and fail-safe operation. **GTE Sylvania, Inc,** 100 First Ave, Waltham, MA 02154.
Circle 236 on Inquiry Card

LEDS WITH BUILT-IN DRIVERS

Fan-in series panel lamps work directly with TTL or CMOS levels. Available in either logic 1 or logic 0 configurations, LEDs are packaged in cylindrical cartridge configurations, and come in red, amber, or green. Most lenses are Fresnel type in either normal or low profile front panel projection. At 20-mA lamp current, average lifetime is 10 yr. **Data Display Products,** 303 N Oak St, Inglewood, CA 90301.
Circle 237 on Inquiry Card

IEEE-488 INTERFACE FOR LOGIC ANALYZERS

Available as field installation kits or as a factory installed option, HP-IB capability makes automatic functional testing of digital systems possible with 1610A and 1615A logic analyzers. When combined with a controller such as a 9825A, data captured by the programmable analyzers can be transferred to the controller for automatic analysis. Ability to program tests offers fast, easy data accumulation, summarization, and documentation in hardcopy across the bus. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.
Circle 238 on Inquiry Card

2-SPEED SINGLE-MODULE S-D CONVERTER

Consuming less than 2 W of power, SDC-361 converter is accurate to 20 angular seconds. Type II servo loop for output data is always fresh up to the specified tracking rates of 1000°/s for 400 Hz and 250°/s for 60 Hz. Fully trimmed unit features control transformer algorithm for inherently higher accuracy and jitter-free output. Measuring 2.625 x 3.125 x 0.82″ (6.668 x 7.938 x 2.082 cm), unit meets MIL-STD-202E with temp ranges of 0 to 70 or −55 to 105 °C. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
Circle 239 on Inquiry Card

SINGLE-MODE CW INJECTION LASER

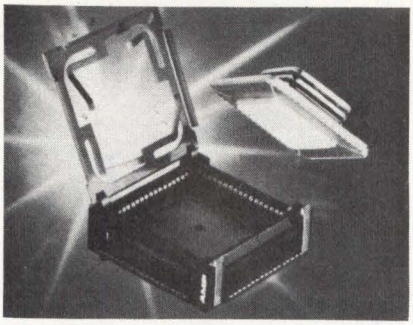
GaAlAs diode incorporates both a double carrier confined, striped laser structure and facet passivation. Typ operating characteristics include stable single transverse mode operation with 7-mW optical power output at <100-mA drive current at 27 °C, second harmonic distortion of <−52 dB, and operation to 60 °C. Peak emission wavelength at 27 °C is 830 nm with a spectral bandwidth of 1 nm. **Laser Diode Laboratories, Inc,** 205 Forrest St, Metuchen, NJ 08840.
Circle 240 on Inquiry Card

MOVABLE POWER DISTRIBUTION SYSTEM

The MN1C series Powermobile, a self-contained system resembling a computer peripheral, utilizes flexible shielded cables to conduct power to various computer components. These cables eliminate expensive custom electrical work required for installation, expansion, or relocation. Unit incorporates an electrostatically shielded isolation transformer designed to eliminate high frequency voltage spikes and transients that cause computer malfunction. A single point grounding system eliminates ground loop current. **Data Processing Power Corp,** 12638 Beatrice St, Los Angeles, CA 90066.
Circle 241 on Inquiry Card

PRODUCTS

CONNECTOR FOR TYPE A LEADLESS SUBSTRATES



A 68-position receptacle accepts leadless ceramic LSI chip carriers and surface mounts to PCBs with pads on 0.050″ (1.27-mm) centers. Measuring 1.165 x 1.165 x 0.366″ (29.591 x 29.591 x 9.296 mm), the connector fastens to the board with a single hold-down screw that provides >200-g normal force/contact for compatibility with tin-lead plated PC pads. Spring-loaded hold-down frame secures LSI package and latches to exert >60-g normal force/contact on metallized pads of ceramic package. **AMP Inc,** Harrisburg, PA 17105.
Circle 242 on Inquiry Card

UNIVERSAL P/ROM PROGRAMMER

This PC board plugs into a spare controller slot of the Ontel OP-1 terminal, extending out of the card cage to allow access to the P/ROM sockets without terminal power-down or card removal. The programmer uses the internal power supply of the terminal. The UPP device functions under software control. All P/ROM types used on the terminal can be programmed. Up to 8 Intel or TI 2716 EPROMs can be programmed at once. Three programmable power supplies are contained onboard. **Nelma Electronics Ltd,** 1707 Sismet Rd, Unit #9, Mississauga, Ontario L4W 2K8, Canada.
Circle 243 on Inquiry Card

TRIMMER POTENTIOMETERS

The 752 series of high performance industrial trimmers measure 0.375″ (0.95 cm) sq for miniaturized circuit board requirements. Cermet resistance elements assure longer life. Case materials are designed to withstand operating temperatures to 125 °C; power rating is 0.5 W at 70 °C. A selection of terminal patterns and adjustment configurations meet various multiturn applications. **VRN St Petersburg,** PO Box 44000, St Petersburg, FL 33743.
Circle 244 on Inquiry Card

IC PRODUCTION SOCKETS

Welcon Lo-Rise™ DIP sockets accept 8- to 40-lead devices on 0.300, 0.400, and 0.600″ (0.762, 1.016, and 1.524-cm) centers. The 802 series is stackable end-to-end [maintaining a 0.100″ (0.254-cm) contact center] and side-to-side. Features are dual-wiping contacts, tapered lead-in ramps, and visual polarization. Anti-overstress internal barrier protects against contact breakage, while a closed bottom prevents solder wicking. **Wells Electronics, Inc,** 1701 S Main St, South Bend, IN 46623.
Circle 245 on Inquiry Card

PLUG-IN 10-A TIME DELAY RELAY

Model 166TD is available with fixed knob adjustable or remote (external resistor) adjustable time delay. Repeatability is ±2% with 45-ms min and 60-ms max release time, and 60/100-ms recycling times. Protection against reverse polarity and false tripping on timing cycle interruption is provided. Contact ratings are ¼ hp or 10 A at 120 Vac; ½ hp at 240 Vac. Electronic circuit provides instant reset if power is removed during the timing cycle without a momentary contact transfer. **Deltrol Controls/Div of Deltrol Corp,** 2745 S 19th St, Milwaukee, WI 53215.
Circle 246 on Inquiry Card

CIRCLE 104 ON INQUIRY CARD

PRODUCTS

PROGRAMMABLE DC POWER SUPPLIES

Constant voltage/constant current supplies offered in 50- and 150-W models are configured as quarter and half rack modules, respectively. 8 P-series units provide voltage/current output levels of 10 V/3 A, 10 V/10 A, 20 V/2 A, 20 V/6 A, 50 V/1 A, 50 V/3 A, 100 V/0.5 A, and 100 V/1.5 A. Output voltage, current, and voltage limit can be controlled by IEEE-488 interface bus, by external analog signals, or by manual controls. The user selects the means of control for each output parameter. **Systron-Donner Corp, Instrument Div,** 10 Systron Dr, Concord, CA 94518.
Circle 247 on Inquiry Card

GENERAL PURPOSE I/O UNIBUS INTERFACE BOARD

Dual I/O™ provides the logic for program controlled parallel transfer of 16-bit data between 2 external user devices and a Unibus system. A single quad-height unit that installs in any available SPC slot, the board is hardware and software equivalent to 2 DR11-C interfaces at one unit load to the bus. 4 Berg connectors serve all user I/O signals. Each set of connectors is pin compatible with DR11-C connectors and accepts std flat ribbon 40-conductor cables with 3M-type socket connectors. **Able Computer Technology, Inc,** 1751 Langley Ave, Irvine, CA 92714.
Circle 248 on Inquiry Card

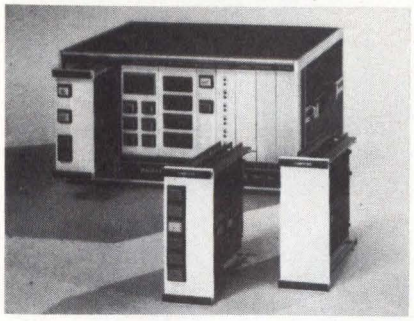
COMPILER/INTERPRETER FOR CP/M OPERATING SYSTEM

A commercially oriented compiler/interpreter BASIC language facility for CP/M™ operating systems, CBASIC-2 improves on the original by adding integer variables, chaining with common variables, multiple line functions, and a cross reference lister for program variables. Intermediate files are smaller and execution is faster. Modular design, maintainability, expanded control structures, and source code security are emphasized. **Software Systems,** PO Box 145, Sierra Madre, CA 91024.
Circle 249 on Inquiry Card

CIRCLE 105 ON INQUIRY CARD

PRODUCTS

DATA ACQUISITION SYSTEM PROCESSOR MODULE



User programming of data acquisition and control functions is possible with the 8085 microprocessor contained in the RIGEL II. In addition, the module offers 16-bit digital I/O port (optional), serial data port (RS-232 and current loop), 32-bit clock with 10-ms resolution, and direct 4-level priority interrupt. Locations hold up to 3k words of ROM for program storage and 750 words of RAM for data storage. The module directly addresses 65k of internal ROM or RAM. **Androtek/dmi,** PO Box 29098, Columbus, OH 43229.
Circle 250 on Inquiry Card

ERROR CORRECTING MEMORY FOR MINICOMPUTER

With storage capacity of 256k bytes on a single board, the 660-ns semiconductor memory for the V77-600 minicomputer detects multiple bit errors and corrects single bit errors. Featuring dual port memory access, the board permits two different processors, operating independently to request access to the memory at the same time. One request will acknowledge when access priority has been resolved by the memory's priority logic. Up to 8 boards may be installed for a max of 2M bytes. **Sperry Univac Mini-Computer Operations,** PO Box 500, Blue Bell, PA 19424.
Circle 251 on Inquiry Card

SMALL DC MOTORS

Series 1616 and 1624 Micromotors, measuring 16 mm in dia and 16 mm and 24 mm in length, have speeds up to 12k r/min. For the -24, torque is up to 0.21 oz-in (0.0015 N•m), and output power is up to 0.9 W. With the -16, torque is up to 0.11 oz-in (0.0008 N•m) and output is up to 0.45 W. Motor voltages are 3, 6, 12, and 24 V. A line of gearheads and optical rate encoders are available for the motors. **Micro-Mo Electronics, Inc,** 3691 Lee Rd, Cleveland, OH 44120.
Circle 252 on Inquiry Card

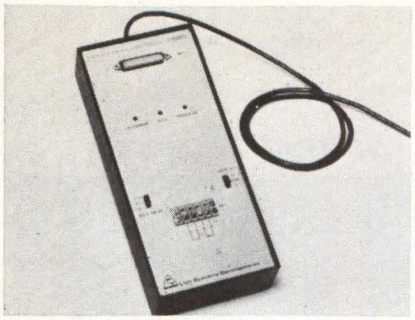
70-CONTACT PAIR PC EDGEBOARD CONNECTORS

Connector series JND, JNK, and JNL are dual readout connectors with contact pairs on 0.100″ (2.54-mm) centers. Extended connectors are offered with 55, 60, 65, and 70 contact pairs and between contact polarizing. JND devices have wirewrap tails, and both JNK and JNL devices have 0.026″ (0.660-mm) round tails for wave soldering. All come with either diallyl phthalate or phenolic insulators. **Viking Industries, Inc,** 9324 Topanga Canyon Blvd, Chatsworth, CA 91311.
Circle 253 on Inquiry Card

FIBER OPTIC TRANSMISSION INTERFACE CIRCUITS

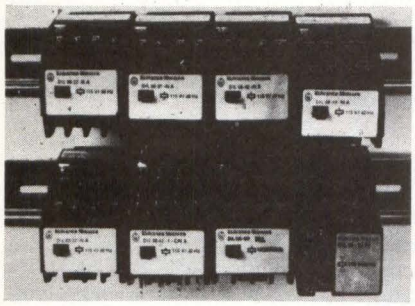
A high speed current driver, SPX 3619 can be used with either LED or laser diode to constitute a complete functional transmitter. Companion 3620 circuit transforms low level photocurrent signals from PIN or avalanche photodiode into logic level output. Both networks feature 20M-bit/s biphase data rate capability, TTL compatible interfaces, and single 5-V power supply operation. The transmitter imposes no restrictions on source other than rise and fall times short enough to realize the data rate. **Spectronics,** 830 E Arapaho Rd, Richardson, TX 75081.
Circle 254 on Inquiry Card

SHORT HAUL MODEM SIMULATOR



Designed as a replacement for inhouse, or for up to 4-km modems, model 2680 operates at speeds to 9600 bits/s, asynchronous, full duplex, over twisted pair cable. Features include optical isolation, adjustable RTS delay, V24/RS-232-C interface, and multidrop application. Operating power is 6 VA at 220/240 Vac, 50 to 60 Hz. **Lion Systems Developments Ltd,** Halifax Rd, High Wycombe, Bucks, HP12 3SE, England.
Circle 255 on Inquiry Card

UNIVERSAL RELAY



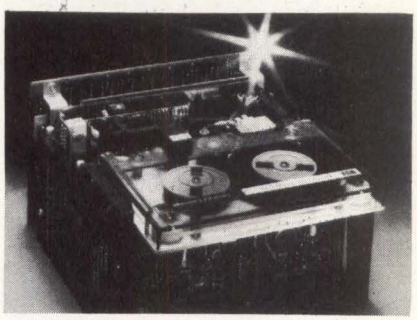
Power output contacts for DIL 08 are rated 10 A continuous at 120 Vac, with an inductive load-making capacity of 150 A max. If a NO contact happens to weld, the armature bridge holding the contacts prevents the NC contacts from reclosing when the relay is de-energized, providing a reliable, fail-safe operation. Coil voltages range from 12 to 120 Vac. The 40 x 50-mm relay has up to 8 NO, 8 NC isolated contacts. **Klockner-Moeller Corp,** 4 Strathmore Rd, Natick, MA 01760.
Circle 256 on Inquiry Card

CHROMATOGRAPHIC FLOW CONTROLLER

Dual channel unit measures gas flows from 4 to 100 std cm^3/min in chromatographic systems. The DFC 100 can be factory-calibrated to measure any 3 of these gases: hydrogen, helium, nitrogen, and 5% methane in argon. Flow rate is controlled electronically. Operating temp is 50 to 140 °F (10 to 60 °C) and tempco of calibration is $<\pm 0.1\%/°C$. Unit measures 2 x 4 x 4" (5 x 10 x 10 cm) and has accuracy and linearity of ±2% full scale and repeatability of ±0.2%. **Tylan Corp,** 19220 S Normandie Ave, Torrance, CA 90502.
Circle 257 on Inquiry Card

PRODUCTS

34M-BYTE CARTRIDGE DRIVE



Microtape™ drive offers 34M-byte reel to reel capacity on a 0.25″ (0.635-cm) cartridge by using 7-track technology on 0.25″ (0.635-cm) ANSI/ECMA digital cartridge. Group code recording results in 7200-bit/in (2834/cm) density. Recording is serpentine, with adjacent tracks recorded in opposite directions, eliminating the previously required rewind time needed to move from one track to the next. **Data Electronics, Inc,** 370 N Halstead St, Pasadena, CA 91107.
Circle 258 on Inquiry Card

TAPE SUBSYSTEM FOR MINICOMPUTER SYSTEMS

IBM/ANSI compatible tape subsystem for the Interdata 16- and 32-bit series minicomputers uses NRZI, PE, and GCR data formats, with rates of 800, 1600, and 6250 bits/in (315, 630 and 2461/cm), between 72k and 781k bytes/s. System components are model 1600 tape controller, Telex models 6840 and/or 6850 mag tape formatters, and models 6240 and/or 6250 tape transports. Unit operates with std Interdata selector channel and Dynamic OS/32 MT software drivers for 9-channel mag tape peripherals. **Information Products Systems, Inc,** 6567 Rookin, Houston, TX 77074.
Circle 259 on Inquiry Card

IEEE-488 BUS FAULT ANALYZER

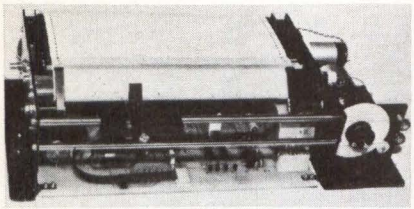
Allowing the user to view or control actual bus data, handshake, and control lines, the 4810 can act as a manual driver, using front panel switches or switch programmed memory. Internal memory allows review of up to 100 char of bus transmissions to assist user in fault analysis. A memory loop feature repeats only the programmed memory segment, bypassing the unused portion of memory. Internal operating rates are 300k bytes/s max, 2 bytes/s, and single-step or external clock rate. **ICS Electronics Corp,** 1450 Koll Circle, Suite 105, San Jose, CA 95112.
Circle 260 on Inquiry Card

PRINTERS AND PLOTTERS WITH INCREASED SPEEDS

200-dot/in (79/cm) electrostatic printer turns out 1000 lines/min. Units print a 64-line, 8.5 x 11″ (21.6 x 28-cm) page in 3.9 s, and deliver up to 15 cut pages/min. Model 3200A printer/plotter and model 3250 printer form 16 x 16 dot matrix char and print 1000 132-col lines/min with 12.5 char/in (4.9/cm). All models use 500′ (150 m) of 11″ (28-cm) wide paper. Options are a scientific/engineering 124-char set and 128-char typesetting set. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.
Circle 261 on Inquiry Card

THERMAL CHART RECORDER

Graphic recording as continuous trace from either digital or analog source plus alphanumerics on external command are provided by Omnigraphic 6100 plotter/printer. In addition to alphanumeric thermal elements, the device provides a special separate element with fast response and long life for writing trace information. Internal memory retains trace data during annotation process. Trace head writes at 75 cm/s; annotation rate is 20 char/s max. **Houston Instrument, Div of Bausch & Lomb,** One Houston Sq, Austin, TX 78753.
Circle 262 on Inquiry Card

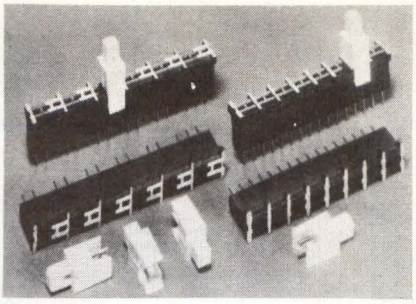


PROCESSOR ENHANCEMENTS

With online diskette storage totaling 1M char, the 1500 dispersed processor gives users choice of either 32k or 60k bytes of user memory. In addition, communication using the IBM 2780 line protocol may occur at the same time that data entry or processing operations take place. New releases of the DOS, Databus, and Dataform software take advantage of the expanded user memory. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.
Circle 263 on Inquiry Card

DIP REPLACEMENT SOCKET/PLUG

Programming or on/off switching is performed by the socket/plug series that replaces DIP switches. Programming switch consists of a white SWP switch plug inserted in an SWS switch socket where a signal is desired through the circuit. It is changed to another circuit by snapping it out of 1 socket position and placing it in another. For the on/off switch, the plug is placed wherever the desired on or off function is required. **Robinson-Nugent,** 800 E Eighth St, New Albany, IN 47150.
Circle 264 on Inquiry Card



PRECISION RESISTOR FOR MILITARY SYSTEMS

S-444 precision fixed resistor is said to have resistance, tolerance, and performance capabilities that surpass all requirements of MIL-R-55182/9. The unit is qualified to the P reliability level of 0.1%/1000 h at 60% confidence level. The resistor has a range from 1 to 100 k Ω with tolerances from ±0.005% to ±1.0%. **Vishay Resistive Systems Group,** 63 Lincoln Hwy, Malvern, PA 19355.
Circle 265 on Inquiry Card

PRODUCTS

ACOUSTIC EMISSION DETECTION UNIT

SC-30 monitors acoustic emissions generated by rotating machinery, pressure, or vacuum leaks, as well as internal leakage, in a contact or noncontact capacity. Adapted for remote online sensing, the ultrasonic unit interfaces with alarm mechanisms, relay devices, or computer type recording instruments. When leakage occurs or mechanical failure is imminent, the problem is sensed ultrasonically and the appropriate interfaced unit is signaled. Capacity to test items on a continuous basis is provided. Reject mechanisms, alarms, recording charts, or microprocessors can be interfaced to recognize and/or eliminate unacceptable products or components. In operation limited range of airborne ultrasonic frequencies are converted into electrical impulses. Using various sensitivity selectors, these impulses can be programmed to act as warning signals that activate the appropriate interfaced device. **UE Systems Inc,** 1995 Broadway, New York, NY 10023.

Circle 266 on Inquiry Card

1.5″ MODULAR OPTICAL ENCODER

Designed for mounting on a motor or other shaft assembly, this 1.5 dia by 0.75 high (3.8 x 1.9 cm) encoder consists of hub-disc assembly, photohead assembly, and cover. It features 5-V TTL compatible outputs and uses gallium arsenide LEDs. Std units can provide 2 channels of up to 100 cycles per revolution; 400 counts are possible with external 4X multiplication. A zero index third channel as well as 12- or 24-V operation are available as options. Modularity allows the selection of the exact measuring configuration required by the application. **Litton Systems, Inc, Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311.

Circle 267 on Inquiry Card

DC-DC CONVERTERS

30C series modular encapsulated converters have max output noise specs of 5 mV pk-pk for dual output models, 8 mV pk-pk for single output units, and 1 mV rms typ for all units. They are available with overcurrent protected single and dual floating outputs of either 5 Vdc at 600 mA with line/load regulation of 0.2/0.1%, and ±12 Vdc at ±125 mA or ±15 Vdc at 100 mA regulated to within ±0.02%. For all models, input to output isolation is 300 Vdc and 100 MΩ shunted by 50 pF. Each output rating is available for operation from an input of either 4.5 to 5.5 Vdc, 10.8 to 15.0 Vdc, 21.6 to 30.0 Vdc, or 42.0 to 56.0 Vdc. **Semiconductor Circuits, Inc,** 218 River St, Haverhill, MA 01830.

Circle 268 on Inquiry Card

DIGITAL PATTERN GENERATOR

Generating patterns from 8 to 64 bits wide and 1024 bits deep at the 10-MHz data rate, the 710 has hex keypad and display to reduce input errors and cut data entry time. Large 16 x 1024 memory allows most microprocessor buses to be simulated. Paralleling up to 4 instruments allows large memories and circuit boards to be tested. In this mode, slave units are controlled by one master unit, eliminating entering of redundant frequency, start, and stop data. A variable skew option allows skew between data on channels 0 to 7 to be varied relative to channels 8 to 16, allowing measurement of effects of propagation delays and simulation of other circuit conditions. Read-only nonvolatile memory option consists of a 2716 type UV P/ROM mounted on the read panel, and allows frequently used data patterns to be retrieved and stored by simply pressing a key. **Moxon, Inc,** 2222 Michelson Dr, Irvine, CA 92715.

Circle 269 on Inquiry Card

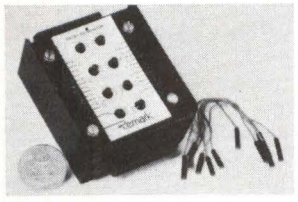
PDP-11 SOFTWARE COMPATIBLE DISC STORAGE SUBSYSTEMS

Designed to offer identical performance characteristics to DEC subsystems and execute all DEC operating systems and diagnostic software without modification, ERP02 and ERM02 add features not found on the DEC systems. The controller incorporates an automatic self-test capability plus extensive subsystem diagnostics in onboard firmware, and added operating functions enhance system performance. Disc controllers use only 2 PC boards that plug into any pair of SPC slots in the CPU, minimizing mounting space requirements. ERP02 emulates the DEC RP11/RP02 subsystem and ERM02 emulates the RH11/RM02. Both models incorporate a CDC 9762 80M-byte storage module drive. **Equipment Resources, Inc,** 120 Interstate N Pkwy E, Suite 120, Atlanta, GA 30339.

Circle 270 on Inquiry Card

DATA LINE MONITOR

Visual indication of prime data communications signals of an RS-232 interface provided by the model 40 allow isolation of modem or terminal problems. When the monitor is inserted between terminal and transmission equipment, it continuously monitors and displays 8 lines of the RS-232 data path. Seven LEDs are permanently assigned to display transmitted data, received data, request to send, clear to send, data set ready, data terminal ready, and data carrier detect. The other indicator is programmable, thus allowing visual indication of any of the other 17 signals in the interface. 25 test points are supplied in the form of 0.025" (0.635-mm) sq pins. Test points and LEDs are clearly marked to simplify use. **Remark International,** 4 Sycamore Dr, Woodbury, NY 11797.



Circle 271 on Inquiry Card

PRODUCTS

MICROCOMPUTER CONTROLLED INTERMEDIATE STORAGE DEVICES

Auxiliary storage/retrieval peripherals that can be used to give terminals intelligence, or to increase the number of functions performed by intelligent terminals, series 232 data stations comprise a 16-bit microcomputer with up to 16k bytes of ROM, 2k to 64k bytes of RAM, 1 or 2 3M DCD-1 transports that accommodate a 100A tape cartridge, and user controls for interfacing with all terminals supporting RS-232 communications interface.

Terminal users can perform numerous data manipulation operations without tying up CPU and communications resources. A proprietary technique enables files to be edited an unlimited number of times. Each of 3 communications ports has its own switch-selectable communications rate, ranging from 110 to 9600 baud. **Digital Datacom, Inc,** 17951 Skypark Cir, Suite K, Irvine, CA 92714.

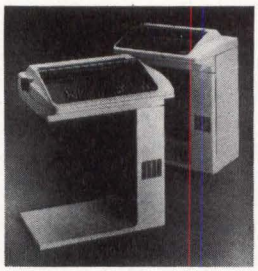
Circle 272 on Inquiry Card

P/ROM PROGRAMMER-DEVELOPMENT SYSTEM

An internal 2k x 8 RAM buffer in the model 4 can be used for in-circuit emulation, along with software move routines to give the operator a development system for both hardware and software design. RAM can be programmed from a master P/ROM, RS-232/TTY input, or directly from the hex keypad. A double-ended 24-pin cable connects the master socket of the programmer to the system socket. Once connected, the system reads internal RAM as an actual in-circuit P/ROM. This allows the designer to discover program and hardware problems before committing to firmware. When a working instruction format has been developed, the system can program EPROM masters from RAM for prototype or production runs. **E-H International, Inc,** 515 Eleventh St, Oakland, CA 94607.

Circle 273 on Inquiry Card

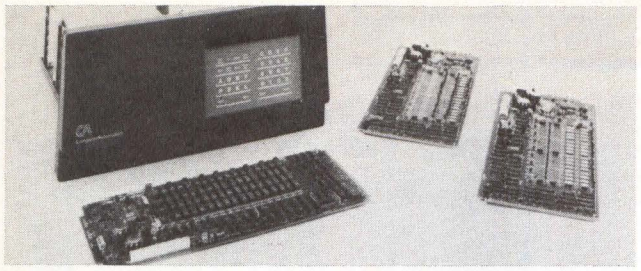
180-CHAR/s PRINTING TERMINALS



Logic seeking, bidirectional Dasher™ TP2 terminal printers use an internal 16-bit microNova™ microprocessor to control printer functions, such as bidirectional printing, variable character formats, and tabbing. All models can print at 180 char/s. This combined with a 1000-word RAM buffer allows efficient operation at 1200 baud without data loss. The units perform plotting and downline loading; downline load permits users to design character sets or special symbols. RO model 6075 and KSR 6077 print in normal and elongated character widths; RO 6076 and KSR 6078 also print condensed characters at 16.5/in (6.4/cm). Models 6077 and 6078 have std typewriter style keyboard for interactive applications and separate numeric keyboard. All models print full 132-col lines. **Data General Corp,** Rt 9, Westboro, MA 01581.

Circle 274 on Inquiry Card

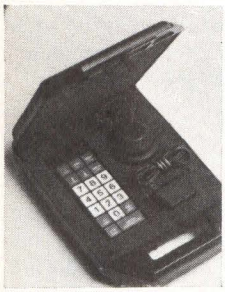
CPU/MEMORY COMBINATIONS IMPROVE MINICOMPUTER PRICE/PERFORMANCE



Featuring high density 580-ns RAM, LSI 4/10, 4/30, and 4/90 are available with 32k-, 64k-, and 128k-byte capacities on a half (7.5 x 1.69", 19 x 42.9-cm) card. 4/10 is a half-card minicomputer, while the 4/30 and 4/90 are full-card (15 x 16.9", 38 x 42.9-cm) CPUs. Larger memories on half cards permit the use of smaller power supplies and chassis. An LSI 4/10 processor with 128k bytes shows a net price reduction of 61%. By combining a 4/30 with the memories, savings over previously available combinations of comparable capacity range from 9% with 32k bytes to 48% with 128k bytes. 4/90 savings range from 17% with 32k bytes to 47% with 128k bytes. **Computer Automation, Inc,** 2181 Dupont Dr, Irvine, CA 92713.

Circle 275 on Inquiry Card

HANDHELD REMOTE ORDER ENTRY TERMINAL



Pocket sized, 8-bit microprocessor based Sprint 100 has a 4k memory in an injection molded case measuring 2.625 W x 6.875 L x 1.156" D (6.67 x 17.46 x 2.937 cm). A color-coded, large keypad assures accurate access to keys. Each entry is confirmed by an audible signal emitted when a key is depressed. The unit's 12-char, alphanumeric LED key-display is designed for accurate reading, reducing eye strain, and misread information. Multiple terminal protocols allow telecommunication with many CPUs and receivers. 4 customer-replaceable, rechargeable, NiCad batteries power the terminal and provide up to 16 h of use between charges. Additional memory protect batteries guard against loss of data. Options include another 4k memory and a case to store terminal and accessories. **Norand Corp,** 550 Second St SE, Cedar Rapids, IA 52401.

Circle 276 on Inquiry Card

PORTABLE SEND/RECEIVE TERMINAL

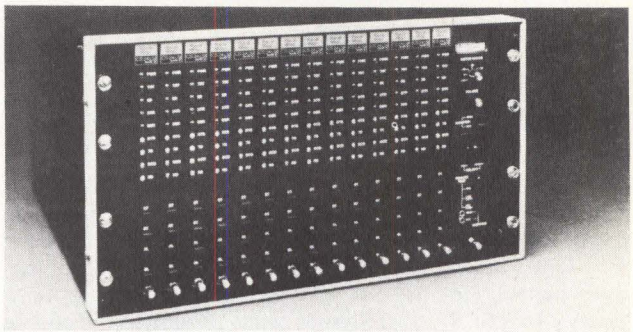
Execuport 4080 provides 80-col thermal printout of the complete ASCII or APL char sets at switch selectable speeds of 10 or 30 char/s in a 15-lb (6.75-kg) package. LED printhead

position display eliminates need to use scale or count spaces in formatting input. Self-test routine produces a full sequential printout of the complete u/lc keyboard character set. Horizontal set and clear tab capability can be controlled at the keyboard or by the computer. New line switch enables operator to choose either carriage return or carriage return/line feed as response to carriage return code. The unit operates in half- or full-duplex and with odd, even, or mark parity switch selectable. **Computer Transceiver Systems, Inc,** East 66 Midland Ave, Paramus, NJ 07652.

Circle 277 on Inquiry Card

PRODUCTS

2400-BIT/s CENTRAL SITE MODEM



Compact construction reduces space requirements for modems, permitting plug-in installation of up to 96 in a std 6′ (1.8-m) equipment cabinet. CS 24 LSI Mark II is compatible with Western Electric 201B and 201C data sets, plus the company's 24LSI, 24 LSI Mark II, and 2200/24. It operates over 4-wire point to point or multipoint lines and is certified for direct connection to the switched telephone network for 2-wire dial-up operation. Each modem in the system provides analog loop, digital loop, and self-test capabilities with individual dc power regulators for added reliability. 9 multicolored LED indicators provide continuous display of each unit's status, plus EIA interface signals. **Racal-Milgo Information Systems, Inc,** 8600 NW 41st St, Miami, FL 33166.
Circle 278 on Inquiry Card

MODULAR FACTORY TERMINALS

Multifunction 200 series terminal configurations range from simple numeric entry and limited display devices to full alphanumeric, interactive data collection stations with badge and card reading capabilities. Based on an internal bus structure, the units and their selectable features are designed for 24-h, 7-day operation in hostile locations. Badge and card reading are performed photo-optically to insure reliability. Completely sealed, micromotion keypads protect the internal electronics of the system. Terminals may be wall or pedestal mounted. A 2-wire data line enables communication between terminals and the processor. An interactive display on models 204, 205, and 206 allows verification of keyboard input and error feedback. **NCR Corp, Data Pathing Div,** Dayton, OH 45479.
Circle 279 on Inquiry Card

150-W OPEN FRAME SWITCHING POWER SUPPLIES

Open frame single PC board design offers high end switching performance in 1-, 3-, or 4-output versions. All outputs are regulated to 0.1% for 92 to 138 V and 184 to 276 Vac line condition, and 0.5% for 0 to 100% load changes. Efficiencies exceed 70% of full load; ripple and noise are <50 mV pk-pk from 50 Hz to 10 MHz. LMG units feature foldback current limiting, provide 28 ms of holdup protection for line dropout, 115/230 Vac line and full load with a 110- or 220-V user-selectable input. LMGT 150/12 and /15 supply 5 V at 20 A on main output, and ±12 at 3 and ±15 at 2.5 A, respectively, on each auxiliary output. 150/12-5 and/15-5 quad output units are 5 V at 20 A on main output, and ±12 at 3 and ±15 at 2.5, respectively, at each first and second auxiliary output, and 5 at 1 A each at the third auxiliary output. **Gould, Inc, Electronic Components Div,** 4323 Arden Dr, El Monte, CA 91731.
Circle 280 on Inquiry Card

LITERATURE

COS/MOS Digital ICs

Intended to aid in device selection, product guide features functional diagrams, max ratings, recommended operating conditions, and static electrical characteristics. **RCA Solid State,** Somerville, NJ.
Circle 300 on Inquiry Card

Crimp-Type Terminals

Booklet explains terminology, describes geometric and metallurgical characteristics of terminals and illustrates manual and automated application tooling. **AMP, Inc,** Harrisburg, Pa.
Circle 301 on Inquiry Card

Miniature/Subminiature Lampholders

Line drawings depicting typ lamps and base configurations, photos, and dimensional drawings for each model comprise catalog. **Chicago Miniature Lamp Works, General Instrument Corp,** Chicago, Ill.
Circle 302 on Inquiry Card

Programmable Signal Processing Filter

Channel response graphs, photos, and specs in 4-p data sheet present model 752, a seventh order elliptic dual low pass anti-aliasing filter with 115 dB/octave roll-off rate in each channel. **Rockland Systems Corp,** Rockleigh, NJ.
Circle 303 on Inquiry Card

Multiplier/Accumulators

Data sheet provides specs, operating characteristics and descriptions, logic and timing diagrams for 8-, 12-, and 16-bit units, and data formats for 2's complement fractional notation. **TRW LSI Products,** Redondo Beach, Calif.
Circle 304 on Inquiry Card

Encapsulated Power Sources

Ac-dc and dc-dc regulated, unregulated, and nonisolated power sources are described with specs, photos, and pinouts. **Wall Industries, Inc,** Bedford, Mass.
Circle 305 on Inquiry Card

Power Supplies

Performance charts, dimensional drawings, photos, specs, and selection charts for switching and linear power supplies and accessories are contained in 148-p catalog. **Lambda Electronics, Div of Veeco Instruments Inc,** Melville, NY.
Circle 306 on Inquiry Card

Liquid Crystal Displays

Data sheets supply performance characteristics and environmental specs for displays along with individual dimension drawings and terminal identification. **Ladcor,** Sunnyvale, Calif.
Circle 307 on Inquiry Card

Electronic Test Accessories

Mini- and maxigrabbers, miniature test probes, and triple banana jacks are among the accessories in 100-p catalog that is illustrated with photos and drawings. **ITT Pomona Electronics,** Pomona, Calif.
Circle 308 on Inquiry Card

Data Communications Devices

Catalog lists photos, specs, and descriptions for devices including couplers, cables, test sets, switches, and interfaces. **Expandor, Inc,** Upper St Clair, Pa.
Circle 309 on Inquiry Card

LITERATURE

Modular Laboratory Computer System

Features of portable MINC system are outlined in brochure that depicts graphics oriented CRT with pictorial and alphanumeric output, floppy disc storage drive, and interfacing modules. **Digital Equipment Corp,** Maynard, Mass.
Circle 310 on Inquiry Card

Industrial Microcomputers and Interface Modules

Interface modules, microcomputer boards and packaging, development systems, plus CINCH™ intelligent data acquisition and control systems are covered in summary. **Control Logic, Inc,** Natick, Mass.
Circle 311 on Inquiry Card

Synchro Converters, Displays, and Encoders

Catalog provides specs, descriptions, and block and dimensional drawings for synchro/resolver and shaft interfacing solid-state TTL products. **Computer Conversions Corp,** East Northport, NY.
Circle 312 on Inquiry Card

Peripherals

Series of 16 data sheets covers data acquisition systems, analog interfaces, digital panel meters, printers, data loggers, 16-bit DAC, and digital voltage calibrator. **Datel Systems Inc,** Mansfield, Mass.
Circle 313 on Inquiry Card

Graphics Workstations

Brochure discusses impact of data plotted with workstation, necessary peripherals, and advantages of plotting data vs scanning computer tabulations. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 314 on Inquiry Card

Liquid Crystal Displays

Mechanical specs, electrical pin-outs, dimensions, and operating characteristics are furnished in separate data sheets for alphanumeric, instrument, and clock applications. **Optel Div, Refac Electronics Corp,** Winsted, Conn.
Circle 315 on Inquiry Card

Information Processing

Catalog describes reports on EDP, word processing, office, and data communications products; reports contain comparison charts, prices, specs, and may include user ratings. **Datapro,** Delran, NJ.
Circle 316 on Inquiry Card

DIP Switches

Catalog contains dimensional drawings, circuitry, electrical characteristics, and material and finishes for line of switches that includes a bottom seal spst device. **Grayhill, Inc,** La Grange, Ill.
Circle 317 on Inquiry Card

Add-On Memory Systems

Application note details interface, communications, and limitations of add-on memory systems and add-in cards. **Digital Data Systems Inc,** Plantation, Fla.
Circle 318 on Inquiry Card

Microcomputer Business/ Development Software

Catalog lists commands for and details business BASIC compiler, SDOS cartridge drive disc operating systems, plus assemblers, editors, and debuggers for 6800 computer systems. **Software Dynamics,** Anaheim, Calif.
Circle 319 on Inquiry Card

Precision Rotating Components

Dealing comprehensively with synchros, servo motors, and other rotative components; listing specs and applications; and presenting test methods, handbook is available for $9.95 from **Muirhead Vactric,** 1101 Bristol Rd, Mountainside, NJ 07092.

Key Switches, Keyboards, and Touchboards

Product line overviews as well as individual data sheets for keyswitches; touchboards; and word processing, communications, key encoded, nonencoded, and data seal keyboards are offered in catalog. **Datanetics,** Fountain Valley, Calif.
Circle 320 on Inquiry Card

A-D Techniques

Application note examines A-D techniques that are pertinent to high performance data acquisition systems. **Dynamic Measurements Corp,** Winchester, Mass.
Circle 321 on Inquiry Card

Magnetic Peripherals

Large capacity, cartridge, and fixed head discs; diskettes; and magnetic tape subsystems plus company support are summarized in brochure. **Data General,** Westboro, Mass.
Circle 322 on Inquiry Card

Frequency Control Devices

Growing family of std oscillators and capability for producing custom crystal filters are outlined in brochure. **Dale Electronics, Inc,** Columbus, Neb.
Circle 323 on Inquiry Card

Numerical Control Accessories

Products and services including NC tape preparation equipment and machine tool control systems are covered in catalog. **Numeridex Inc,** Wheeling, Ill.
Circle 324 on Inquiry Card

Fiber Optic IR LED

Electrical, environmental, and optical ratings plus application oriented performance curves for etched-well LED are cited in data sheet. **IAV, Inc,** Van Nuys, Calif.
Circle 325 on Inquiry Card

Backpanel Interconnect System

DEC compatible press fit/backpanel interconnect system plus optional mating logic and accessories are listed in brochure. **Stanford Applied Engineering,** Santa Clara, Calif.
Circle 326 on Inquiry Card

Minicomputer Software

100 bill of materials, order entry, computer-aided education, accounting, engineering, and marketing packages have been added to the original 230 mainly BASIC packages described in 400-p, tab-indexed catalog. To order, send $49.95 plus $5.00 postage and handling to **Resource Software International, Inc,** 140 Sylvan Ave, Englewood Cliffs, NJ 07632.

In-Circuit Test System

Illustrated with photos and diagrams, brochure provides basic operating information, features, functions of LSI/MSI, SSI, and analog component test system. **Plantronics Zehntel,** Walnut Creek, Calif.
Circle 327 on Inquiry Card

Display Computer

Hardware and software modularity of model 5216 display computer presented in brochure allows custom-like configuration for graphic image application. **Aydin Controls,** Fort Washington, Pa.
Circle 328 on Inquiry Card

Distributed Processing System

Separate brochures detail hardware, software, and peripheral subsystems for Level 66 and Level 68 Series 60 distributed processing systems. **Honeywell Inc,** Phoenix, Ariz.
Circle 329 on Inquiry Card

Dictionary of Microcomputing

More than 900 definitions plus examples, sketches, diagrams, and tables in 190-p dictionary aid in comprehension of microcomputer literature. Available for $14.50 from **Garland Publishing, Inc,** 545 Madison Ave, New York, NY 10022.

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

ADVERTISERS' INDEX

*Appearing in selected subscribers' copies

New opportunities for hardware/software professionals

TAKE A HAND IN THE CHALLENGE OF EXPANDING OUR FACILITIES . . . AND HEIGHTENING YOUR OWN FUTURE

Forward-looking expansion now under way on the part of this major electric utility can offer you a significant opportunity for the responsibilities you want.

ENGINEER/COMPUTER SPECIALIST

The candidate we seek will have both hardware and software capability. In this newly created position, you'll be responsible for design, installation, and start up of systems for all sizes of in-plant computers and peripheral equipment. Project duties will involve working with analog/digital sub-systems and will include support of systems modification and maintenance functions.

Technical degree a must, coupled with minimum 5 years experience in hardware and/or software design, plus exposure to real-time, computer-based data acquisition and control systems. Knowledge of systems as applied to monitoring and control of nuclear power plant processes desirable.

PROGRAMMER ANALYST/ Process Control

Will be responsible for various software-related duties from design through testing and maintenance, to programming for various plant computer software systems. Must also be able to correct existing program logic and modify programs to reflect new methodologies, and improve program efficiencies using real-time computer methods.

Technical degree required, preferably Math or Computer Science major, and 2-5 years experience in programming including proficiency in FORTRAN, Assembly and machine languages.

We offer competitive salaries, commensurate with experience and potential for growth, plus top benefits which include relocation assistance to our desirable North Jersey headquarters. For immediate consideration, in assured confidence, send resume with salary history and current requirement, to:

DEPT. CD409, ATTENTION: R. McCABE

JCP&L / GPU

JERSEY CENTRAL POWER & LIGHT COMPANY
Madison Avenue at Punch Bowl Road
Morristown, New Jersey 07960

MEMBER COMPANY OF THE GENERAL PUBLIC UTILITIES SYSTEM

In principle and practice—an equal opportunity employer M/F

SALES OFFICES

NEW ENGLAND AND UPSTATE NEW YORK

CALDWELL ENTERPRISES, INC.
Lindsay H. Caldwell
129 Cedar Hill Rd.
East Dennis, MA 02641
(617) 385-2533

LONG ISLAND AND MIDDLE ATLANTIC STATES

CALDWELL ENTERPRISES, INC.
Richard V. Busch
Princeton, N.J. area
(609) 924-6300

SOUTHEASTERN STATES

COLLINSON & CO., INC.
Newton B. Collinson, III
Anthony C. Marmon
4419 Cowan Rd., Suite 302
Tucker, GA 30084
(404) 939-8391

MIDWESTERN STATES

Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

WESTERN STATES

BUCKLEY/BORIS ASSOC., INC.
Terry Buckley
Tom Boris
John Sabo
912 South Barrington Ave.
Suite 202
Los Angeles, CA 90049
(213) 826-4621

Plotting System CPS-11

Digital plotter and microprocessor based controller

combine to provide high performance plotting

The CØMPLØT® CPS-11 is a plotter and plotter controller designed to meet your plotting applications... whether on line or remote.

The field proven plotter incorporated in the CPS-11 gives you the highest resolution of any 11" digital plotter on the market today— 4 switch selectable step sizes (in English or Metric) ranging from 200 to 1000 increments/inch. The pen moves at a remarkable rate of 4000 steps per second (240,000 steps per minute). The flat plotting surface and Z fold paper let you see what you're plotting while it's being plotted.

The plotter controller utilizes a microprocessor to provide automatic detection and correction of transmission errors, local generation of alphanumeric characters, circular buffer memory, and greatly simplified host computer software. The controller can either operate the plotter remotely from a host computer or serve as a sophisticated computer interface - whichever fits your specific application.

For complete information on how the CPS-11 can upgrade your plotting capabilities for only $5,390,* call or write Houston Instrument, One Houston Square, Austin, Texas 78753. (512) 873-2620. For rush literature requests or sales office information, persons outside Texas call toll free 1-800-531-5205. In Europe contact Houston Instrument, Rochesterlaan 6 8240 Gistel Belgium, phone (059) 27 74 45.

Visit us at Electro '79, booth 1926

houston instrument | DIVISION OF **BAUSCH & LOMB**

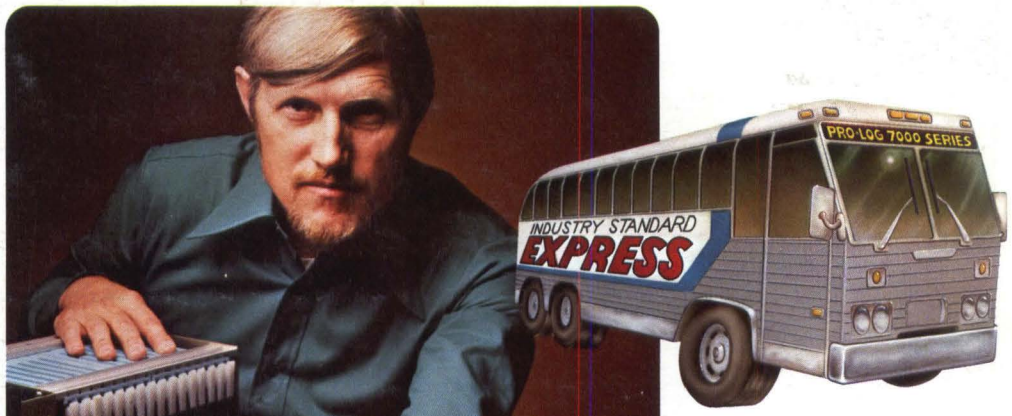
"the graphics - recorder company"

CIRCLE 133 ON INQUIRY CARD

* U.S. Domestic Price Only

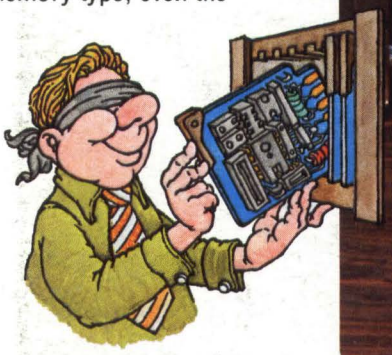
® Registered Trademark of Houston Instrument

PRO-LOG makes it easy to board the STD BUS.



Introducing the STD BUS, the simplest bused microprocessor system ever made. STD means Simple To Debug, Simple To Develop, Swift To Deliver.

The new STD BUS—8-bit microprocessor systems built around a standard bused motherboard which allows any card to work in any slot. Thus you can change the function of your system, the memory type, even the microprocessor type by simply exchanging one card for any other. The STD BUS is 56 lines wide and is compatible with Pro-Log's standard 4½-inch by 6½-inch edge-connected cards.



It's supported by both Pro-Log and MOSTEK and freely available to the industry.

CARDS AVAILABLE NOW
Z-80 PROCESSOR ● 8085 PROCESSOR
16K BYTE 2716 EPROM MEMORY ● 16K BYTE STATIC RAM MEMORY
TTL INPUT PORT CARD ● TTL OUTPUT PORT CARD
TTL INPUT/OUTPUT PORT CARD
TRIAC OUTPUT CARD
MOTHERBOARD ½ RACK ● MOTHERBOARD ¼ RACK
● CARD EXTENDER ● GENERAL UTILITY CARD ● UTILITY DIP CARD
WE ARE DEVELOPING ADDITIONAL CARDS IN THESE CATEGORIES
PROCESSOR ● MEMORY ● DIGITAL I/O ● SERIAL I/O
ANALOG I/O ● PERIPHERAL I/O ● INDUSTRIAL I/O

Watch for announcements as new cards become available.

A whole new card series available for use with the STD BUS.

Our new 7000 Series 8-bit systems were specifically designed for use with the STD BUS. We have cards in limited quantities now, in production quantities in January.

Buy 250 of any one card, and we give you free the plans for that card and non-exclusive manufacturing rights so you can build it yourself.

In addition to cards, we also make a ½ or ¼ rack card cage. It includes motherboard, card edge connectors and mounting brackets.

Every part in our systems is or soon will be a second-sourced industry standard which means that if you produce them yourself, you'll never have to worry about the availability of sole-sourced parts. Through cross licensing arrangements, MOSTEK and Pro-Log both will be supporting and expanding the STD BUS.

Learn about the STD BUS and our 7000 Series Systems.

Send for our Microprocessor User's Information Packet. Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940. Phone (408) 372-4593.

PRO-LOG CORPORATION

Microprocessors at your fingertips.

CIRCLE 134 ON INQUIRY CARD