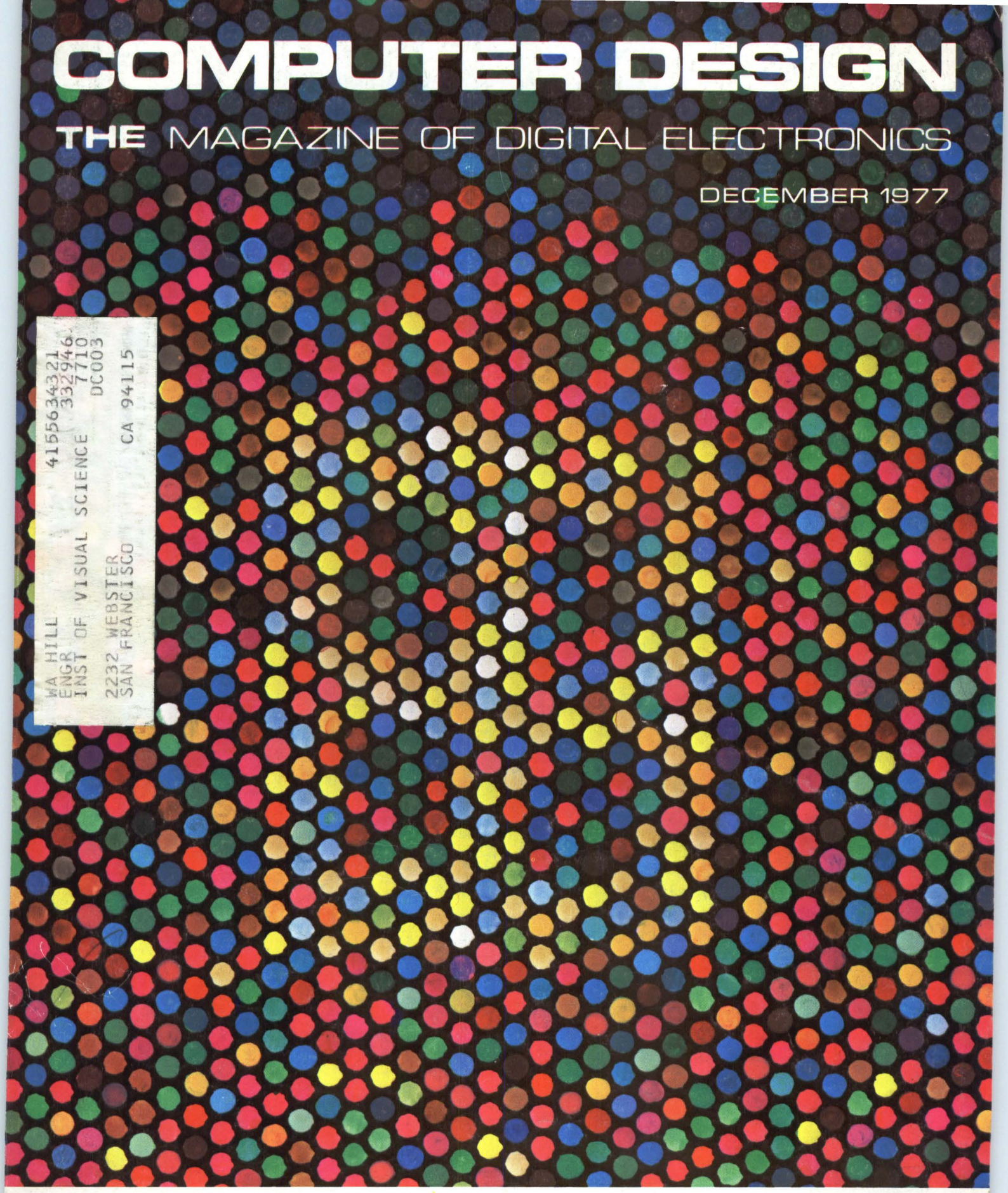
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

DECEMBER 1977



PATTERN RECOGNITION: BASIC CONCEPTS AND IMPLEMENTATIONS

MULTIPLE-WORD BUFFERING FOR DISC CONTROLLERS WITH BIPOLAR FIFO MEMORY

MICROPROCESSOR-BASED INTERFACE CONVERTS VIDEO SIGNALS FOR OBJECT TRACKING

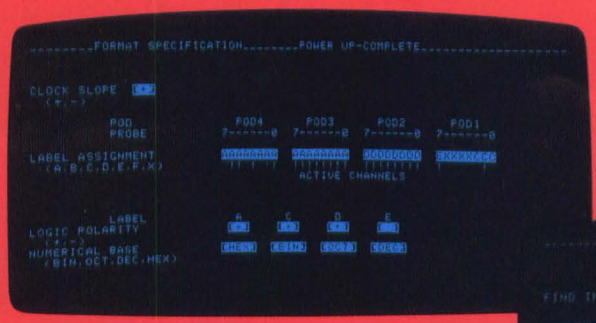
At last...a Logic State Analyzer that practically asks you what to analyze and how to display.

A few simple pushbuttons, an interactive display, sophisticated microprocessor-based intelligence . . . now they're all combined in HP's powerful new 1610A Logic State Analyzer. The result is a simplified "menu" approach to instrument setup, ability to choose highly complex trace specifications with a few simple keyboard entries, program-flow displays that are easier than ever to interpret, and an instrument that virtually self tests.

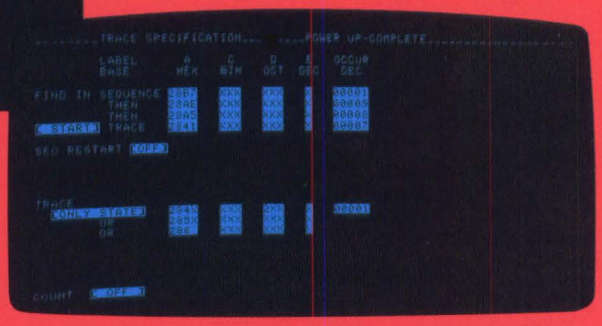
In addition, now you can trace complex branches and nested loops; count the number of states or the time interval between all words to debug or optimize programming; and drive HP Model 9866A or 9866B printers for hard-copy output of test results and set-up specifications.

The new 1610A, priced at $9500*, provides fast setup and easy trouble-shooting in nearly any logic system having data rates to 10 MHz. Your local HP field engineer has the complete story. Give him a call today.

* Domestic U.S.A. price only.

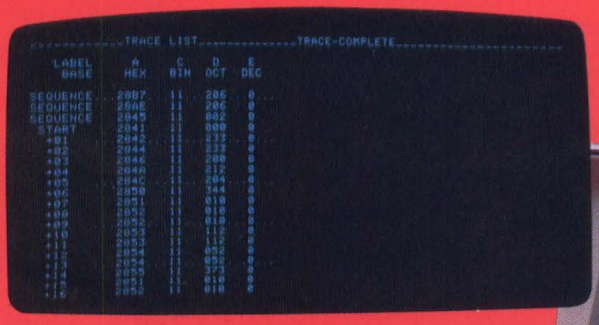


Setup ease. Inverse-video fields and moveable cursor in Format Specification mode direct you in defining clock slope, positive or negative logic and display formats (Hex, Binary, Octal or Decimal). You can also assign alphabetic labels to groups of data bits acting as a unit, greatly simplifying setups and display formatting. In addition, the display verifies probe-lead continuity and signals node activity.

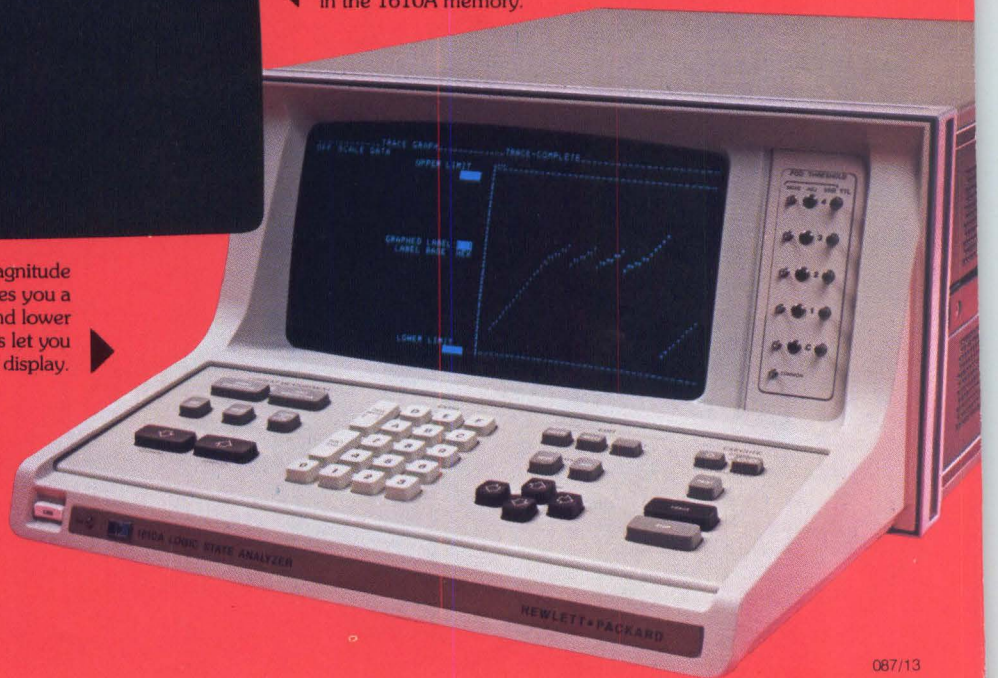


Complex measurement capability. Fields and moveable cursor in Trace Specification mode simplify selection of trigger conditions and trace qualifiers. The ability to define up to seven sequential 32-bit words makes it possible to trace a specific path in complex branched programs. For further conditioning you can define the number of times each sequential state is to occur to allow the analyzing of looped or nested loop programs. And you can define up to seven states or groups of states for selective trace, simplifying data analysis and reducing the need for deep memory.

Simplified interpretation. List Display shows you trigger words plus the program flow you specified in the set-up specifications. Now you can easily compare operating software to original source listings or, in the trace-compare mode, to program flow stored in the 1610A memory.



System overview. Graph Display, showing data magnitude (y axis) vs. time for all 64 words in memory, gives you a system overview. Keyboard entries establish upper and lower y-axis scale values, and moveable intensified dots let you select specific areas for list display.



HEWLETT hp PACKARD

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For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE 1 ON INQUIRY CARD

087/13

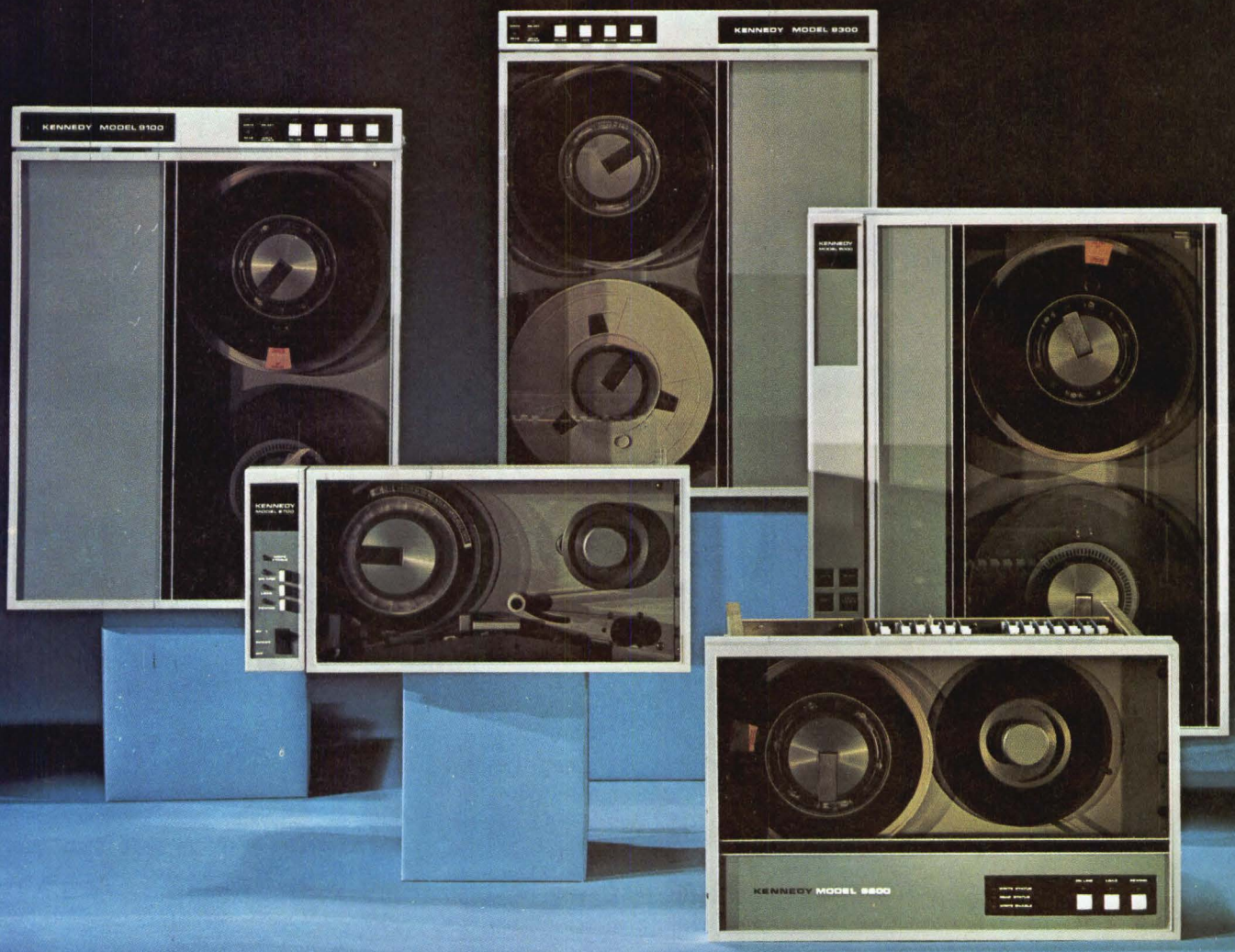
The Class of '77

It's the Kennedy 9000 Series Digital Tape Transports—
the culmination of years of experience in defining,
designing and refining a product line. All Kennedy
Tape Transports possess features found in no other
line — features such as front accessible off-line
test panel, linear non-contact (Mag Pot) position
sensor, interchangeable electronics and capacitive
linear-loop sensing on our vacuum column machines.
Performance is equally impressive, with data
transfer rates to 200KHz and tape speeds to 125 ips.
But features and performance are only part of the story.
Kennedy products have always been designed and
built to be the finest in the field.
We call it class. So will you.

KENNEDY CO.

540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953

CIRCLE 2 ON INQUIRY CARD



KENNEDY- QUALITY- COUNT ON IT

Tally reliability. As good as gold.

Tally reliability is unmatched in the printer industry. The value to you is a 100% duty cycle, 200 line per minute printer that costs far less to own. Less than any other printer around.

You can run the T-2000 as long and as hard as you want without the frustration of downtime and costly repairs. Plus, preventive maintenance is unnecessary. Sliding bearings, pivots and lubrication points are eliminated. There are no electronic timing or hammer flight time adjustments. In short, there's nothing to adjust.

The reason behind this unparalleled reliability is the patented Tally print comb mechanism. It uses a unique flexure technology that's impervious to wear and designed for unlimited life. While other printers like to talk about calculated MTBF, Tally points to field proven MTBF. Most of the Tally printers that have been in the field, including those in operation for over four years, have never required adjustment or repair to the print mechanism. In fact, many have experienced no malfunction at all! No one else can safely make that statement. And Tally backs every T-2000 with a full year print mechanism warranty.

The gold printer above is Tally's commemorative unit marking 10,000 machines delivered. The noteworthy statistic is that 99 per cent plus have never had a mechanism failure.

Find out all the facts on this proven performer and call your nearest Tally sales office, or write or call Tally Corporation, 8301 S. 180th Street, Kent, WA 98031. Phone (206) 251-5524.

TALLY **OEM Sales Offices:** Los Angeles (213) 378-0805 • San Antonio (512) 733-8153 • New York (516) 694-8444
Boston (617) 272-8070 • Chicago (312) 325-9788 • Miami (305) 665-5751
Washington, D.C. (703) 471-1145 • Seattle (206) 251-6730 • Business Systems (415) 254-8350

THE
MAGAZINE
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FEATURES

DEPARTMENTS

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How FORTH™ *software tools have rescued mini and micro project developers reads like a fairy tale.*

FORTH *software*

Software development time: up to 90% *less.*
Memory requirements: up to 90% *less.*
Run times: up to 60% *faster.*

A short time ago, a gloomy Monday found a New York manufacturer desperate. Microprocessor software problems had deep-sixed the delivery date of an artificial-kidney tester.

Four man-months of assembly language programming...and still the device wouldn't work.

Came Tuesday, design specs were rushed to a group of software problem-solvers, FORTH, Inc. Three nights a crack FORTH programmer concentrated on saving the day...flying cross-country to project headquarters on Friday.

By Sunday night, the machine was totally operational!

Five FORTH days, with one man applying microFORTH language and programming techniques, and the tough software task was fully written, debugged and cross-compiled.

For a complicated μP device with: one master panel with thumbwheels, 3-way switch, pushbuttons. Plus dual control panels with more thumbwheels, switches...and lights. Plus two printers; A/D converter; and hydraulic valves. All up in less than a week.

Believing in FORTH has solved many a minicomputer project too.

As when the Navy was caught between the devil and the deep blue sea. mini-hardware already configured to develop a missile guidance system required an image processing capability.

The hang-up? High level languages demanded too much memory; but assembler code, too much development time.

Fortunately, project management was wise to FORTH's track record in image processing. *And* the availability of off-the-shelf miniFORTH software that could accommodate just about any-make mini...on order, on hand, or on line.

National secrets can't be spilled, but what can be told is the performance of miniFORTH tools in the hands of *typical* users: software development time, 3-10 times less. Memory requirements reduced up to 50% over assembly code, with full machine speed capability. All simultaneously!

Easy to see why the Navy selected FORTH as the sole source for this software contract.

FORTH is fact...not fable. There *is* a popular myth: it says you can optimize today's advanced mini/micro hardware—with software tools as old as some programmers. But wishing won't make it so; you need rich new programming techniques.

That's FORTH. Combining the operating system with a multilevel language structure, you instruct machines on your own terms.

Whether you're talking new product development or on-going applications. All the way from process control to interactive graphics to data base management systems, FORTH helps you repeat these success stories. Either through our custom programming services. Or take FORTH tools off-the-shelf for in-house use.

For minicomputer projects, miniFORTH is ready to go for all popular minis.

microFORTH runs on disk-based microprocessor development systems, package-priced at $2500, plus options.

So flexible, so powerful are FORTH capabilities, our case histories strain credulity. We admit it. And we admit, to learn this new shortcut, you'll leave the old-shoe comfort of Basic and Fortran behind.

It's worth it. In cost-effectiveness. In dramatic cuts in development time. In much lower computing-equipment investments. Just what it takes to make heroes in real life.

Moral. You don't have to believe in fairy tales, to know that the limitations of Basic, PL/M, and Fortran are often pretty grim. Calling FORTH in late can save your neck. But calling FORTH *first* can make any software project easier to swallow.

Phone (213) 372-8493, for microFORTH, miniFORTH or programming assistance. Or write: FORTH Inc., 815 Manhattan Avenue, Manhattan Beach, CA 90266. We can help.

FORTH, Inc.

CALENDAR

CONFERENCES

JAN 19-21—U.S./Southeast Asia Telecommunications Conf, Singapore. INFORMATION: John Sodolski, Electronic Industries Assoc, Communications Div, Washington, DC 20006. Tel: (202) 457-4934

JAN 19 and FEB 2—Invitational Computer Conf, South Coast Plaza Hotel, Orange County, Calif; and Pier 66 Hotel & Marina, Ft Lauderdale, Fla. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

JAN 24-26—Reliability and Maintainability, Biltmore, Los Angeles, Calif. INFORMATION: D. F. Barber, PO Box 1401, Branch PO, Griffiss AFB, NY 13441

JAN and FEB—Trade Ctr Exhibitions: Mini/Micro Computers; and Computers and Related Equipment, London, England and Tokyo, Japan. INFORMATION: Roy Mitchell or Peter Ryan, U.S. Dept of Commerce, Domestic and Internat'l Business Administration, Washington, DC 20230. Tel: (202) 377-2838 or (202) 377-2849

FEB 7-10—World Fair for Tech Exchange, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Dr Dvorkovitz & Associates, PO Box 1748, Ormond Beach, FL 32074. Tel: (904) 677-7033

FEB 13-15—WINCON '78 (Winter Conv on Aerospace Electronic Systems), Sheraton Universal Hotel, North Hollywood, Calif. INFORMATION: WINCON '78, 1 Space Pk, Bldg E2/9080, Redondo Beach, CA 90278. Tel: (213) 536-3680

FEB 15-17—IEEE Internat'l Solid-State Circuits Conf (ISSCC), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42d St, New York, NY 10036. Tel: (212) 279-3125

FEB 21-23—ACM Computer Science Conf, Detroit Plaza Hotel, Renaissance Ctr, Detroit, Mich. INFORMATION: Seymour J. Wolfson, Wayne State U, Detroit, MI 48202

FEB 21-23—Datacom '78, Sheraton Park Hotel, Washington, DC. INFORMATION: Ed Bride, The Conference Co, 60 Austin St, Newtonville, MA 02160. Tel: (617) 964-4550

FEB 28-MAR 2—COMPCON Spring '78, San Francisco, Calif. INFORMATION: COMPCON Spring '78, PO BOX 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 1-3—Control of Power Systems Conf and Exposition, Lincoln Plaza Hotel, Oklahoma City, Okla. INFORMATION: Dr M. E. Council, OG & E Prof, School of Electrical Engineering and Computing Science, U of Oklahoma, Norman, OK 73019. Tel: (405) 325-4721

MAR 5-8—TAPPI Internat'l Pulp and Paper Industry Exhibit, Conrad Hilton Hotel, Chicago, Ill. INFORMATION: Wayne Gross, c/o TAPPI, 1 Dunwoody Pk, Atlanta, GA 30341. Tel: (404) 394-6130

MAR 14-17—Printemps Informatique, U.S. Trade Ctr, Paris, France. INFORMATION: Helen Burroughs, U.S. Dept of Commerce, Office of Internat'l Mktg, France/Benelux, Rm 6318, Washington, DC 20230. Tel: (202) 377-4941

MAR 20-22—Industrial Electronics Control Instrumentation (IECI) Conf, Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr S. J. Vahaviolos, Engineering Research Ctr, Western Electric, PO Box 900, Princeton, NJ 08540

MAR 21-23—IECI '78 (Industrial Applications of Microprocessors), Sheraton, Philadelphia, Pa. INFORMATION: W. W. Koepsel, Dept of EE, Seaton Hall, Kansas State U, Manhattan, KS 66506

MAR 22-24—Internat'l Topical Conf on the Physics of SiO_2 and Its Interfaces, IBM Thomas J. Watson Research Ctr, Yorktown Heights, NY. INFORMATION: Dr Sokrates T. Pantelides, Conf Chm, IBM Thomas J. Watson Research Ctr, PO Box 218, Yorktown Heights, NY 10598. Tel: (914) 945-1207 or 945-3000

MAR 27-31—Automated Business and Banking Equipment Exhibition, U.S. Internat'l Mktg Ctr, Singapore. INFORMATION: George I. Middleton, U.S. Dept of Commerce, DIBA/BIC/OIM, Rm 4126, Washington, DC 20230. Tel: (202) 377-2471

APR 17-20—Design Engineering Show, McCormick Pl, Chicago, Ill. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

APR 18-20—The Society for Information Display Internat'l Sym, Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42d St, New York, NY 10036. Tel: (212) 279-3125

APR 24-26—28th Electronic Components Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: J. A. Bruorton, Mktg Administration Dept, Union Carbide Corp, PO Box 5928, Greenville, SC 29606. Tel: (803) 963-6348

APR 25-26—26th Annual National Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: School of Electrical Engineering, Engineering Ext 301 EN, Oklahoma State U, Stillwater, OK 74074. Tel: (405) 624-5146

APR 28-30—PERCOMP '78, Long Beach Conv Ctr, Long Beach, Calif. INFORMATION: Royal Exposition Mgmt Corp, 1833 E 17th St, Suite 108, Santa Ana, CA 92701. Tel: (714) 973-0880

MAY 9-12—Internat'l Magnetics (INTERMAG) Conf, Palazzo Dei Congressi, Florence, Italy. INFORMATION: E. Della Torre, Dept of Electrical Engineering, McMaster U, Hamilton, Ontario L8S 4L7, Canada

JUNE 12-15 MIMI '78 (4th Internat'l Sym and Exhibition of Mini and Microcomputers and their Applications), Zurich, Switzerland. INFORMATION: Secretariat MIMI '78, Interconvention, c/o Swissair Postfach, 8058 Zurich, Switzerland

JUNE 12-16—7th Triennial IFAC World Congress, Helsinki, Finland. INFORMATION: IFAC 78 Secretariat, POB 192, 00101 Helsinki 10, Finland

SHORT COURSES

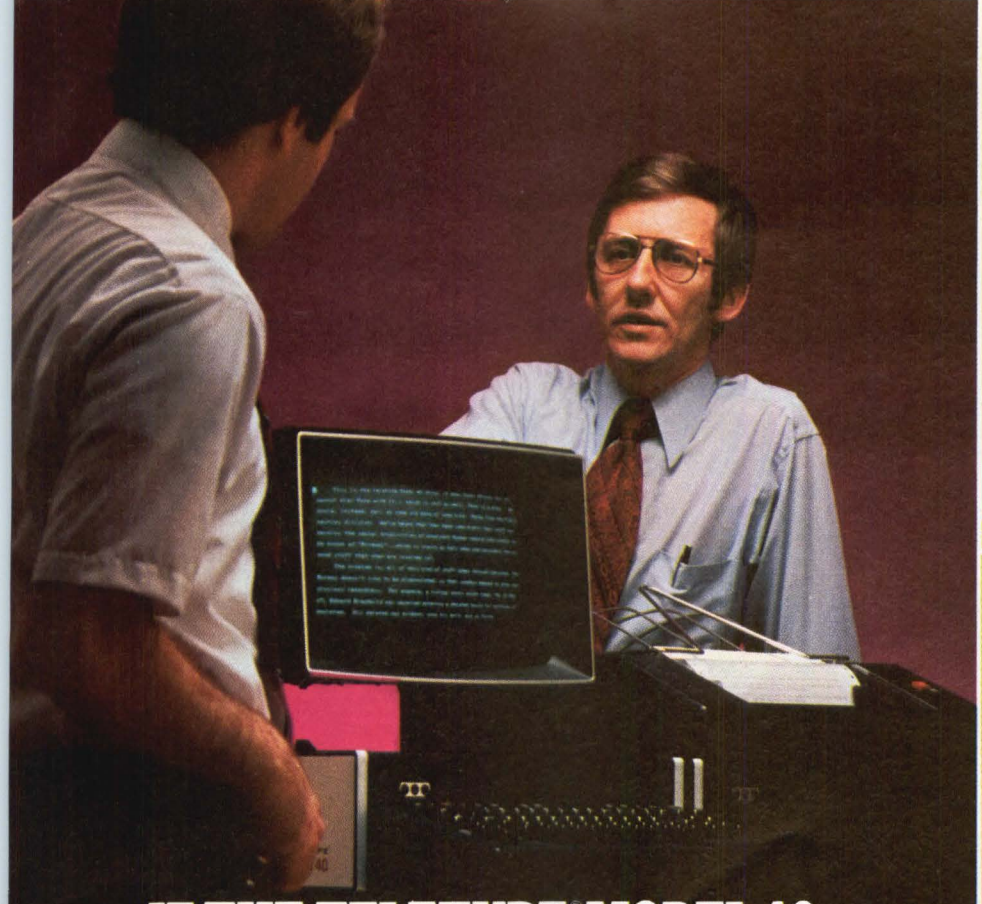
JAN 9-13—Microprocessors; JAN 16-20—Structured Programming and Software Engineering; JAN 18-20—Programming Techniques for Computer Graphics; JAN 23-25—Configuration Management of Software Programs; and JAN 23-27—Digital Filters for Control Systems, and Microprocessors and Microcomputers: Theory and Applications, George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

JAN 11-13 and JAN 23-25—Patent Law for Engineers and Scientists, The Rodeway Inn, San Diego, Calif; and The Biscayne College Ctr for Continuing Education, Miami, Fla. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

JAN 16-20 and JAN 23-27—Microprocessor and Microcomputer Short Courses, Los Angeles, Calif; and Houston, Tex. INFORMATION: Integrated Computer Systems, Inc, 3304 Pico Blvd, 2nd Floor, Santa Monica, CA 90405. Tel: (213) 559-9265

JAN 19-20—Program Testing Tutorials, San Francisco, Calif. INFORMATION: Dr E. F. Miller, Jr, Software Research Associates, PO Box 2432, San Francisco, CA 94126. Tel: (415) 921-1155

FEB 6-10—Data Base Systems: Design, Implementation, Application, and Trends, UCLA, Los Angeles, Calif. INFORMATION: Continuing Education in Engineering and Mathematics, Short Courses, 6266 Boelter Hall, UCLA Extension, Los Angeles, CA 90024. Tel: (213) 825-3344 or 825-1295



IF THE TELETYPE® MODEL 40 SYSTEM EVER MALFUNCTIONS, IT'S DESIGNED TO TELL YOU WHAT'S WRONG.

Even though we probably go to more trouble to insure uninterrupted reliability than anyone else, we're still realistic enough to admit that sometime something's going to go wrong.

So instead of burying our heads in the sand and pretending it won't, we've concentrated our efforts on what can be done to make downtime as short and painless as possible.

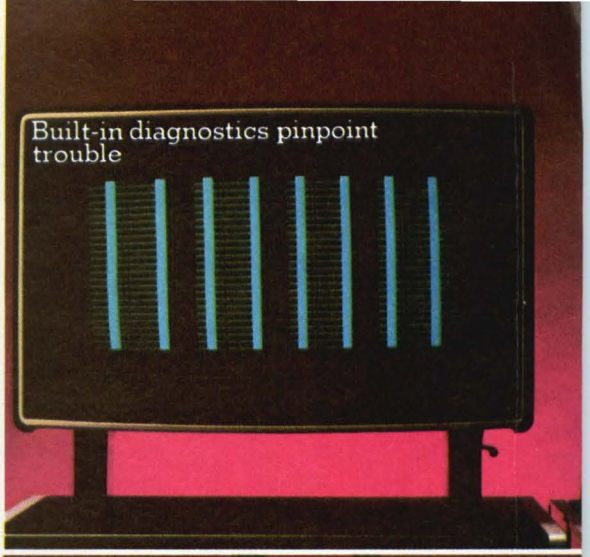
For starters, we gave the model 40 product line its own diagnostic capability. To tell you quickly what's wrong. Then, to make it easy to fix, we used a modular design concept. The result is an average mean-time-to-repair of only 3/4 hour.

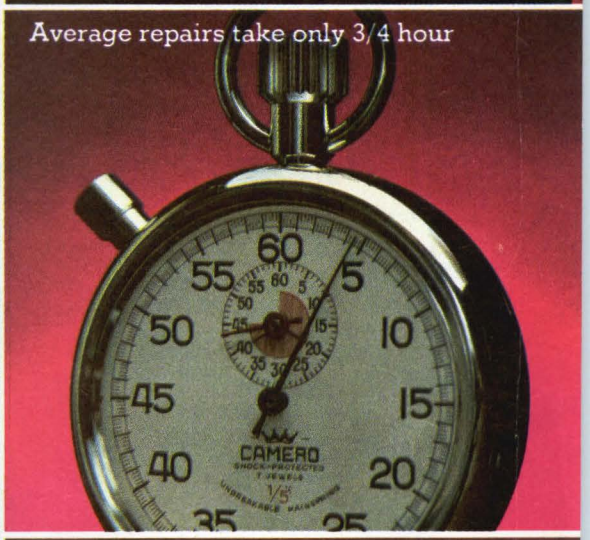
We also made sure that when something does go wrong, you'll never be alone. We've got a nationwide service network standing behind every product with the Teletype name on it. We offer on-call repair service, maintenance contracts, and even an exchange repair service on components and parts.

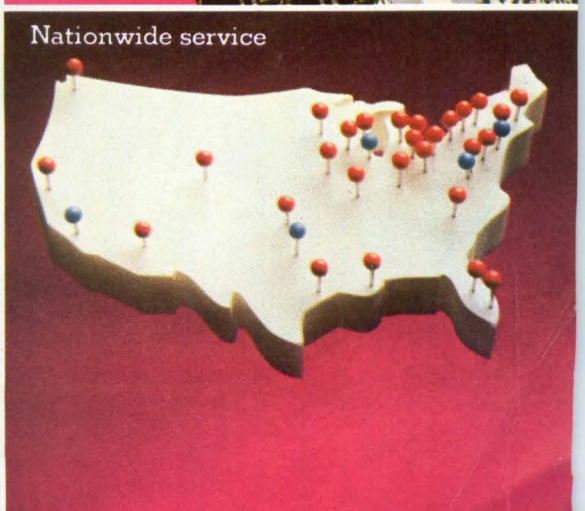
The way we look at it, building something the best way humanly possible is only half our job. The other half is being ready for the unexpected.

For more information about the Teletype model 40 product line, write: Teletype, 5555 Touhy Ave., Skokie, IL 60076. Or call: 312/982-2000.

TELETYPE








Your next high-speed programmable memory just doubled its density.
Again.
The 16K PROM.

BIPOLAR PROM PROGRESS:
Last year, we invented 8K. This year, we invented 16K. Next year, they'll both be industry standards.

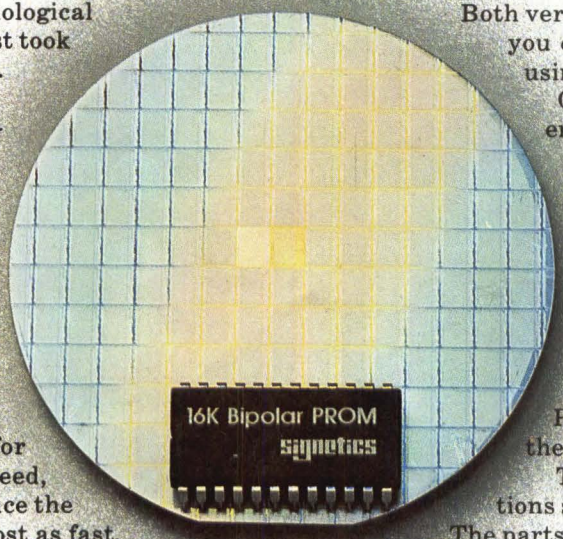
Signetics' acknowledged technological leadership in Bipolar PROMs just took another lengthy stride forward.

Just over a year ago, we announced the world's first field-programmable Bipolar PROM with 8K memory capacity. It was news then, and it's an industry standard now.

Here's even more important news for users of high-density memories—the 16K PROM is a reality. It's the 82S190/191—from Signetics.

More than a Larger Memory. The 16K PROM has a lot more going for it than just raw storage. Like speed, for example—although it has twice the density of its 8K cousin, it's almost as fast, with a maximum address access time of only 80 nsec. Current drain, though, is unchanged—at 175 mA. That's a big advantage for you—half the power per bit, twice the storage capacity.

Like most of its smaller cousins, the 16K PROM is available with two output options: The 82S190 is Open Collector, the 82S191 is Tri-State. That means you can choose the output you need for optimizing word expansion in bused organizations.



Both versions are field-programmable, so you can produce custom patterns by using prescribed fusing procedures. On-chip decoding and three chip-enable inputs are also provided, permitting easy memory expansion.

Signetics—Your Supermarket for PROMs. The partial listing of PROM products in the table below will give you a fair idea of why Signetics stands at the forefront of high-speed PROM technology. Each of the types listed is available in economical Power Plastic DIPs or packaged for use in the military temperature range.

Take a closer look at the specifications shown. There's a lot there to find. The parts themselves can be found on your distributor's shelves. Call him today or use the coupon below to order additional evaluation data.

The 82S190/191 is available now in limited sample quantity. Full production due in January 1978.

signetics
a subsidiary of U.S. Philips Corporation

Signetics Corporation
811 East Arques Avenue
Sunnyvale, California 94086
Telephone 408/739-7700

SIGNETICS PROM SELECTION GUIDE (4K & ABOVE)

Size	Organization	Type	Output*	Pins	Max. T_{AA} (ns)	Max. I_{CC} (mA)	Key Benefits
4K PROMs	1024 x 4 (4096)	82S136	OC	18	60	140	High speed.
		82S137	TS	18	60	140	
	512 x 8 (4096)	82S115	TS	24	60	185	High speed. Has built-in latch.
		82S140	OC	24	60	175	Four chip-enable inputs for easy memory expansion.
		82S141	TS	24	60	175	
		82S146	OC	20	45	155	Fastest available 4K PROMs. .3" wide pkg. saves space.
		82S147	TS	20	45	155	
8K PROMs	2048 x 4 (8192)	82S184	OC	18	100	120	Low current drain.
		82S185	TS	18	100	120	
	1024 x 8 (8192)	82S180	OC	24	70	175	High speed.
		82S181	TS	24	70	175	
		82S2708	–	24	70	175	High speed with 2708 pinout.
16K PROMs	2048 x 8 (16,384)	82S190	OC	24	80	175	16K capacity with drain of only 175mA. 80nsec speed.
		82S191	TS	24	80	175	

* OC - Open Collector; TS - Tri-State

To: Signetics Information Services, 811 E. Arques Ave.
P.O. Box 9052, MS 27, Sunnyvale, CA 94086

- ☐ Please send me technical data on the 82S190/82S191 16K PROM.
- ☐ I'd like additional data on the _____ (type).
- ☐ Send me general product reference material on all PROMs, including those with smaller capacities.
- ☐ I have an urgent requirement. Please have a PROM specialist phone me at once: ( ) _____

Name _____ Title _____

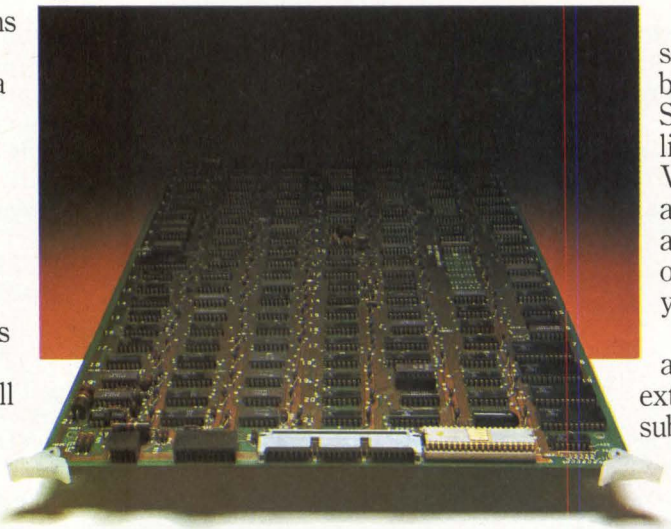
Company _____ Division _____

Address _____ MS _____

City _____ State _____ Zip _____

CD-12

Sperry Univac's new mainframe-on-a-board: What you do with it is your business.



Whether your systems business is scientific, instrument control, or data communications, know this:

Our new V77-200 delivers more computing power than any other computer-on-a-board you can buy. Handling up to 32K/16-bit words of 660ns MOS memory.

Reason enough to call it the world's first mainframe-on-a-board. But there's more.

Because our new V77-200 comes loaded with "big machine" features. Like 8 programmable registers with byte, word and double word manipulation. Up to 32-bits of arithmetic precision. A powerful set of 187 instructions. Hardware multiply/divide. Direct memory access. Programed I/O. Multi-device automatic program loaders. A real-time clock. And a teletype/CRT controller. All standard. And all on a single 10.8" x 17" board.

There's even Virtual Console Logic that eliminates the need for a programmer's console by allowing you to control the V77-200 from a teletype or CRT keyboard.

You get "big machine" performance, too. Example: a microinstruction cycle time of 165ns that allows multiplication functions to be handled in just 4.9 microseconds—divide in just 8.

Plus your choice of OEM-tailored options. Like a variety of connector planes and general purpose interface boards for custom I/O designs. Three different 660ns memory boards (in 8K, 16K, and 32K-word modules). An operator's console. Power-fail detect and data save. Memory parity. Hardware for up to 64 priority vectored interrupts. An integral or modular power supply. And a system chassis. All the "unbundled" pieces you need for quick and easy system integrations.

The new V77-200 also saves you time and money by allowing you to use Sperry Univac's well-established floppy or disk-based VORTEX real-time operating system. In effect, allowing you to concentrate on the development of your application software.

And giving you access to Sperry Univac's extensive library of software subsystems, language processors, and system utilities.

Best of all, the world's first mainframe-on-a-board has a base price of just $1200. Plus a discount plan designed to give even modest-volume OEM buyers a big break. And you can take delivery in a matter of days—not months.

No matter how you configure it, the new V77-200 is the most economical Sperry Univac yet. Delivering the kind of price/performance value that just makes good sense. No matter what business your systems are in.

For more information on the world's first mainframe-on-a-board, please contact: Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, P.O. Box C-19504, Irvine, California 92713, Telephone (714) 833-2400.

SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORPORATION

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Certification 1977

Mandatory use of interface connecting arrangements for customer-owned communications equipment connected to the switched telephone network of the communications common carriers has been one of the more prolonged issues in the field of telecommunications. In many intrastate communications network applications, these "protective" devices were also required for access to leased lines provided by telephone companies.

These connecting arrangements burst upon the telecommunications world following the 1968 Carterfone Decision by the Federal Communications Commission (FCC). In that decision the FCC allowed the connection of nontelephone company equipment to telephone facilities. Referred to as "foreign attachments," such connections had been universally prohibited in all existing federal and state tariffs in effect at that time. Naturally, mandatory use of these devices was strongly opposed by private manufacturers of telecommunications equipment as unnecessary and restrictive, while traditional communications common carriers defended their existence on the grounds of protecting the telephone network from the hazards of the customer-owned equipment.

Since then, unending varieties of telecommunications applications and devices which require connecting devices have been developed and applied to the telephone network. Conflicts between the telephone companies and their opponents on this issue have been debated and tested in technical, regulatory, judicial, and legislative arenas. However, conclusions have always been indecisive, and at best have provided small shifts in their relative positions. Fundamental differences have remained unresolved: the telecommunications industry wanted the connecting arrangements to be eliminated while the majority of the telephone companies insisted that they remain.

After nine years, the issue finally is about to be resolved. On October 5, 1977, the U.S. Supreme Court announced that it will let stand a Fourth Circuit Court of Appeals ruling which validates FCC Part 68 Rules and decided not to hear a pending case filed on this issue. Those FCC Rules permit direct connection of telecommunications systems and equipment to switched and leased line facilities of the telephone network *if* the telecommunications systems and equipment have been certified by the FCC. All judicial avenues have been utilized and concluded; even the U.S. Congress has been involved in this issue by the attempt to pass the Consumer Communications Act of 1976 (see "Communication Channel," *Computer Design,* Sept 1976, pp 14, 19). These past events appear to be finished; FCC certification and registration of telecommunications systems and equipment are now law.

The U.S. Supreme Court's decision, rather than ending this issue, has merely set in motion the events necessary to conclude it. Many of the finer points pertaining to this Supreme Court decision have yet to be resolved by the FCC; the definition and time of those subsequent resolutions are still uncertain. The Supreme Court decision was scheduled to be final on October 24, 1977, but could actually be delayed if telephone companies or states file further petitions for reconsideration of the Court's action in refusing to hear the case.* By mid-October, U.S. Congressman Lionel Van Deerlin (D-Calif), Chairman of the U.S. House Subcommittee on Communications, requested in writing that FCC Chairman Richard Wiley rule on the primary line concept petitioned to the FCC. The concept, related to small key telephone systems and residential telephones, proposed that in the event of certification, the telephone company could insist that at least one telephone set provided by the telephone company be required, at tariff rates, at each location that was equipped with customer-owned telephone instruments or a key telephone system. The FCC must respond to this notification, which could add as much as six months to the effective date of the Supreme Court decision. Delays in the finalization of this decision are, therefore, expected.

A more significant aspect that must be resolved is the matter of "grandfathering telephone systems." Telephone companies pleaded that an unreasonable burden was being imposed to require all telecommunications equipment to meet FCC certification standards in order to connect directly to the telephone network. Since most existing equipment provided by the telephone companies was not expected to meet these standards, it was proposed by the FCC that telecommunications systems and equipment that the telephone companies installed prior to June 1976 would be considered "grandfathered" and initially exempt from certification. They could remain uncertified and in direct connection with the telephone network until some future date. Since the Supreme Court decision to confirm the validity of this FCC Ruling has taken so long, a new cutoff date will be negotiated by the telephone companies and ruled by the FCC.

All similar regulatory aspects must be reconsidered and redefined by the FCC before a definitive conclusion can

*Due to necessary deadlines, it is possible to provide only information and related developments concerning this ruling which were available up until press time.

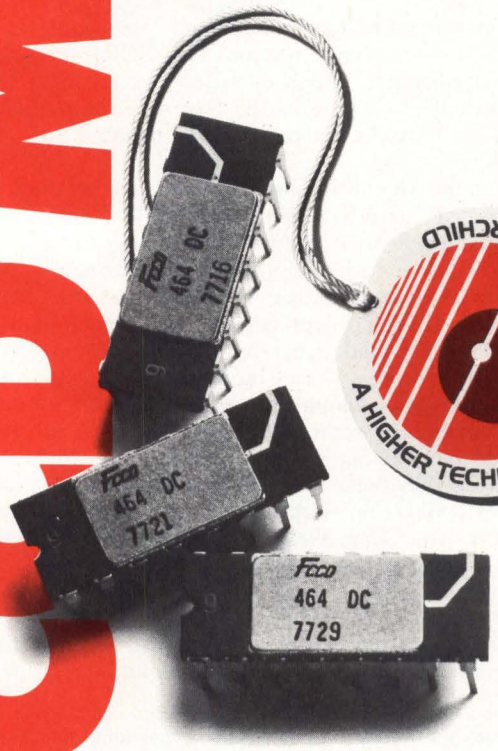
CCD MEMORY

EVER SINCE OUR GREAT MEMORY BREAKTHROUGH THE OLD INDUSTRY STANDARD AIN'T WHAT IT USED TO BE.

When we introduced the Fairchild 64K F464, we said it had the stuff to be the industry standard someday. We even started out with a second source. Apparently, a lot of memory people took us seriously. Response has been so positive, we've already increased our production capacity.

Plugging the gap between MOS and magnetic memories, the F464 is the first semiconductor Bulk Storage Devise (BSD).

The F464 is the densest semiconductor memory ever made. A compact die size of less than 40,000 mil² — not much larger than today's 16K RAMs. All packaged neatly in a standard 0.3-inch 16-pin DIP.



FROM FAIRCHILD
A HIGHER TECHNOLOGY PRODUCT

HIGH PERFORMANCE, LOW OVERHEAD.

There has never been a device like the F464. It's a 65,536 x 1-bit dynamic serial memory organized as 16 randomly accessible shift registers of 4096 bits each. The four address bits are decoded on-chip to select which one of these 16 shift registers is to be accessed. Control inputs include Write Enable and Chip Select. It requires standard power supplies of + 12 V and ± 5 V.

All inputs (except the clocks) are directly TTL compatible. The two high-frequency and two low-frequency clock inputs are low capacitance 12 V signals which can be easily generated with simple logic.

The logic required to generate this 4-phase clock costs less than one memory chip and is generated only once per system.

Part Number	Maximum Frequency (MHz)	Maximum Active Power Dissipation (mW)
F464-4	2	238
F464-3	4	298
F464-2	5	336

Speed and power dissipation for F464 family.

So you don't pay for memory overhead every time you expand. This lower overhead cost means lower system costs to you.

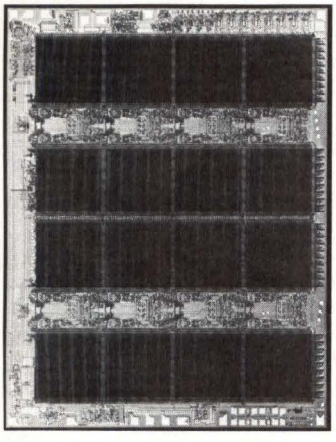
Maximum data rates range from 2 MHz (F464-4) to 5 MHz (F464-2). The minimum frequency for the SPS structure is 1 MHz. Since all 16 registers shift simultaneously, the average random access time (called latency) is only 410 μs at 5 MHz—a truly significant performance improvement over other bulk memory technologies! And, at the same time, the power dissipation remains low: typically 3.5 μW/bit at 5 MHz, and 0.6 μW/bit during standby at 1 MHz. Three part types are available to cover a wide range of maximum speed requirements.

These performance benefits make the F464 a natural for hybrid head-per-tracks or fixed-head discs, extended cache, and many other high-density memory applications.

Other outstanding F464 characteristics include solid state ruggedness, speedy data rates and the most semiconductor memory per square centimeter in the industry. Not bad for a small chip!

LOW COST, HIGH VERSATILITY.

The new F464 is three to four times less expensive per bit than RAMs. It is also cost-competitive with all fixed-head discs. So there are no trade-offs between price and performance. The F464 gives you the best of both.



F464 applications range from typical computers to atypical portable memories and digital delays.

And once you order, you can rest assured that you'll get prompt delivery. Fairchild has a 250,000-square-foot plant in San Jose, California that's totally dedicated to VLSI technology and production.

FOLLOW THE LEADER.

Fairchild pioneered CCD technology. We introduced the world's first commercially available charge-coupled device in 1973. Today, we offer the world's broadest line of CCD products. It stands to reason we'd be the ones to make CCD memories a reality.

For more information on the F464 (or our other CCD products), contact your Fairchild sales office or representative today. Or write directly to our MOS/CCD Division at Fairchild Camera and Instrument Corporation, P.O. Box 880, Mountain View, California 94042. TWX: 910-373-1227.

FAIRCHILD

CALL US ON IT.

be attained. Technical realities must also be considered before present users disconnect existing connecting arrangements. While preliminary certification specifications and procedures have been issued by the FCC, finalization and approval of this certification standard must still be accomplished. Registered telecommunications devices do not actually exist; even traditional connecting arrangements are not presently considered as certified and registered by the FCC. Although many manufacturers are tentatively claiming that their equipment or systems meet certification, in actuality it means only that their product is considered certifiable under the present preliminary, nonapproved specifications. Admittedly, such products have a higher probability of certification than other products that have never attempted adherence to the preliminary standards.

A second technical factor is that most customer-owned systems and equipment were designed to interface to a connecting arrangement, not directly to telephone lines. These interfaces are dramatically different. It is false to assume that removing a connecting arrangement is the sole event necessary to accomplish direct connection. It appears that present telephone line characteristics will be considerably modified with the advent of certification. Present certification standards impose an interface characteristic modification on both the telephone line appearance and the terminal equipment. Devices installed by the telephone companies directly to the telephone line once it is modified will also require modification to be registered.

The transition from connecting arrangements to fully certified telecommunications systems and equipment is a complex procedure which the FCC must coordinate and control in phased sequences. Unfortunately, it appears inevitable that each subsequent phase would tend to impact equipment or devices purchased to meet the requirements of some previous phase. Idealistically, the telecommunications industry and user communities would like to stop all new installations and, without economic concern, be able to immediately convert all existing installations and make certified equipment available from all manufacturing sources.

Three areas of concern are shared by telecommunications users. The first is the availability of present connecting arrangements to permit the continued installation of customer-owned telecommunications systems and equipment. These manufacturers are motivated to curtail and discontinue further manufacturing because the arrangements do not meet preliminary certification standards, facing them with inevitable obsolesence. Telephone companies want to stop the purchase of these obsolete devices and wish to deplete their present inventories as soon as possible. Without a clearly defined alternative, a shortage of such devices can be expected for new installations as well as for maintenance replacement.

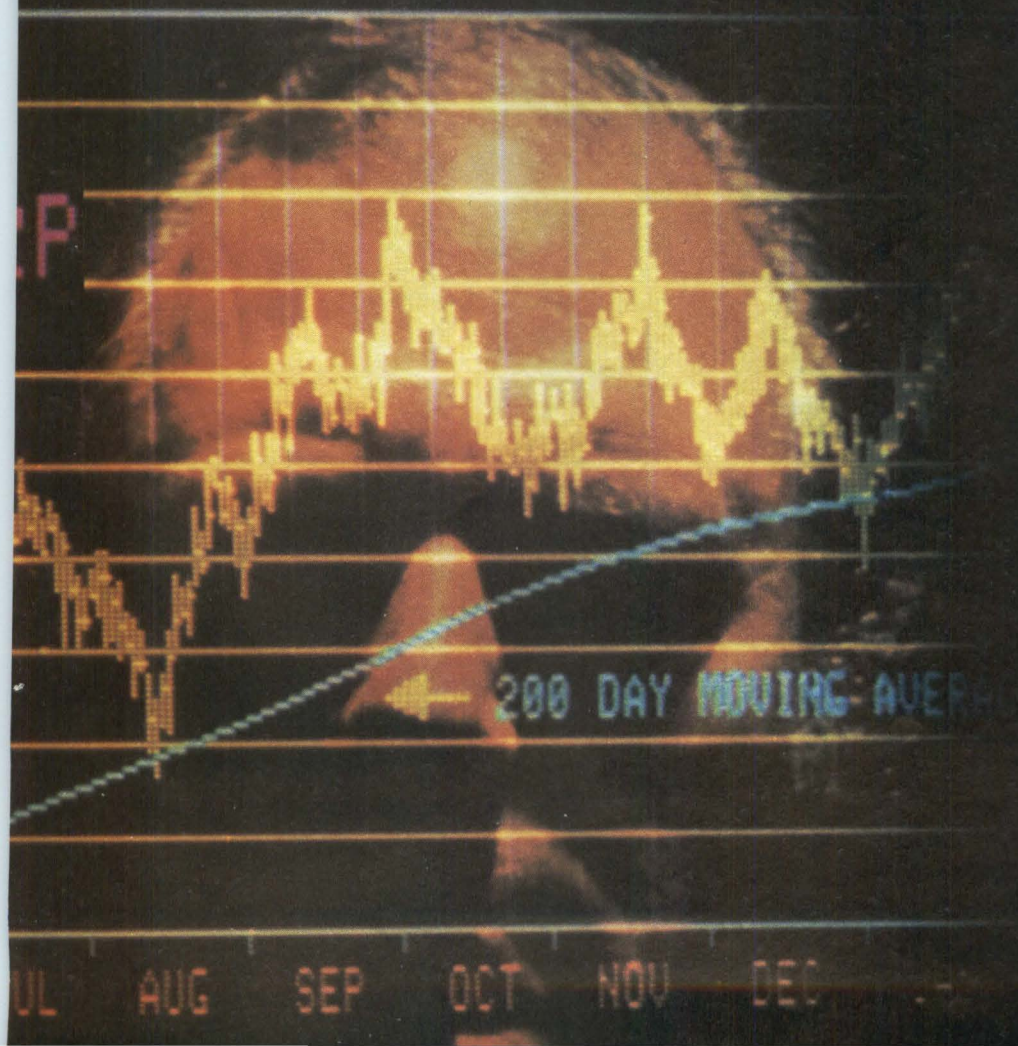
Secondly, certified trunks and equipment terminations are not yet finalized and hence are unavailable. Nonavailability of a connecting arrangement may be temporarily overcome by permitting direct connection of customer-owned equipment to existing trunks. Present circuits in customer-owned equipment must then be extensively modified, if possible, or replaced. The latter incurs the same short-term obsolesence as present connecting arrangements. Manufacturers are not willing to invest in the development and manufacture of direct connection interfaces to present trunk characteristics when certified trunks will replace them shortly. In the same context, users would not purchase interim equipment interface circuits even if they were available.

The third concern is that telephone companies will automatically disconnect existing connecting arrangements once the court's decision is finalized. The validity of this depends on how each state regulatory agency addresses this decision, since state tariffs have jurisdiction over the installation, service, and rental aspects of connecting arrangements. The probability that all telephone companies will immediately remove all present connecting arrangements is very low. Over 500,000 connecting arrangements are installed by telephone companies in the U.S. At an average monthly rental of $6 each, this represents approximately $3M dollars in revenue that will continue as long as the connecting arrangements remain installed. External influences, however, could force a change. For example, a matter pending with the Massachusetts Public Utility Commission could require Massachusetts telephone companies to terminate all charges for existing connecting arrangements. In California, the pending request would refund all past revenue realized from connecting arrangements. Without the revenue, the telephone companies might be prompted to disconnect these arrangements on the grounds that they are maintenance and cost liabilities.

A euphoria has been provided by the Supreme Court's resolving this issue. However, the transitional problems may be discouraging. Discontinued connecting arrangements coupled with the lack of finalized certification standards would result in the nonavailability of registered devices and trunks, and might serve to accomplish the telephone companies' previous objective of curtailing competition in spite of the court decision. The next few months are critical for implementing this decision. The FCC, given the opportunity it has been seeking, is responsible for an orderly transition. Hopefully they will bring that opportunity to reality in an equitable manner without unnecessary delays.

Ramtek's new MICROGRAPHIC™ terminal gives you color, intelligence, graphics, and alphanumerics at a price you can afford.

Color and smarts don't cost a lot anymore.



Here's great resolution and a bright, flicker-free display on a matrix of 512 elements by 256 lines in a terminal that's easy to program to your requirements.

No longer do you have to put up with poor resolution in economy-priced terminals. Ramtek gives you a combination of true graphics—such as vectors, conics, plots and bar charts—and high-speed alphanumerics with a high-resolution industrial-quality monitor. You can choose two sets of 8 colors for both graphics and alphanumerics. Dual and split screen capability too, with all the price/performance benefits of raster scan technology. And the independent alphanumeric refresh offers you single-character addressability within a visible matrix of 25 rows of 80 characters that are bright, crisp, sharp, and well defined. The refresh memory also allows selective erase, modification, and update.

The MICROGRAPHIC terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM. Ramtek's control software gives you TTY compatibility and high-level graphic functions commanded by ASCII text strings. Choose from an extensive list of options such as additional serial I/O ports, alphanumeric overlays, programmable fonts, and packaged software.

Best of all, you'll find Ramtek gives you an affordable price, depending upon your individual requirements. Find out more by contacting us. We're Ramtek, 585 N. Mary Avenue, Sunnyvale CA 94086. In a hurry? Pick up the phone and call us. We'll tell you why you can afford color and smarts.

ramtek

Our Experience Shows

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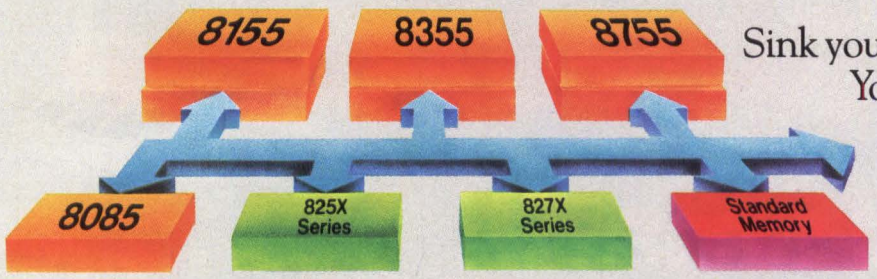
CIRCLE 11 ON INQUIRY CARD

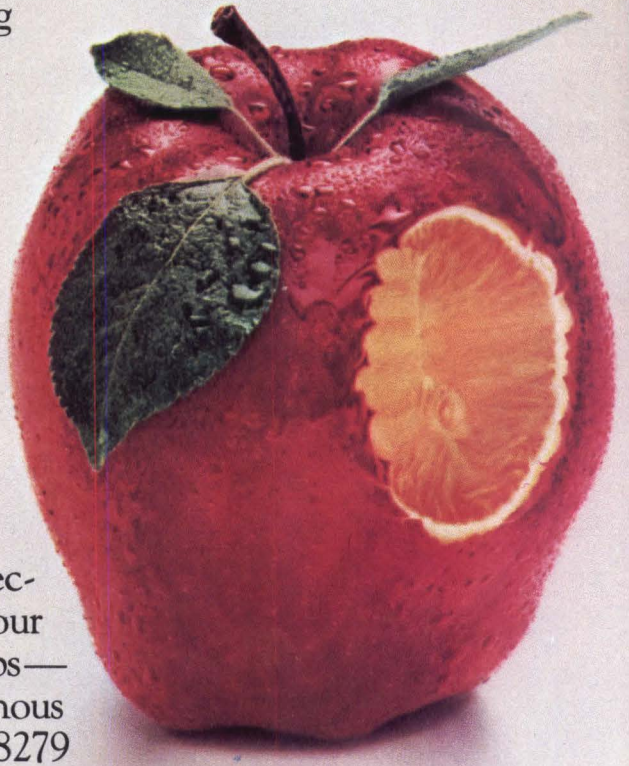
Intel delivers the 8085, designers just



Sink your teeth into Intel's new 8085. You'll find it's the only microcomputer that combines the performance, economic advantages and total support it takes to be recognized as the new industry standard. So it's no surprise that there are already four announced sources for the 8085. In fact, the deeper you go, the better the 8085 gets.

The 8085, even more than the 8080 it succeeds, is a total design solution, not just a component. It delivers higher performance, for capabilities far beyond the 8080's. It has a higher level of integration, so you can design your products with fewer components, making them more competitive and more profitable. And to help you get those products to market quicker we've given the 8085 the industry's broadest base of system and development support.

Yet the 8085 is fully compatible with the 8080. So your investment in existing designs is protected, and implementing new designs is simplified by the wealth of 8080 software and peripherals at your disposal.



It all adds up to a design solution you won't be able to resist. That's true for a broad range of applications. The 8085 can be designed in as an economical stand-alone three-chip system using the 8085 CPU, the 8155 256-byte RAM with I/O and timer, and the 8755 2K-byte EPROM with I/O or its interchangeable 8355 ROM with I/O.

You can expand this basic system for larger applications using additional RAM, ROM, EPROM and Intel's complete family of first and second generation peripheral controllers, including our four new programmable peripheral controller chips—the 8271* Floppy Disc Controller, 8273* Synchronous Data Link Controller, 8275 CRT Controller and 8279 Keyboard/Display Interface. All these components including 8755 EPROM operate from a single +5V supply.

*Available 4th Quarter 1977

the new microcomputer can't resist.

A multiplexed data/address bus permits integration of many auxiliary system functions—such as clock generation, system control and multiple interrupts—onto the 8085 chip while maintaining 8080 compatibility and the same 40-pin package. And forward-thinking engineers will realize that it is also a link to Intel's future generation microcomputer products.

No microcomputer can match the 8085 as a total design solution because no microcomputer can come close to the 8085's support base. Support for the 8085 includes the Intellec® microcomputer development system with resident PL/M, the high level programming language that can cut months off your software development time. Intellec is the only development system with ICE-85,™ providing in-*system* emulation for faster system development and debugging. Then there's application assistance, training classes and seminars worldwide. And a comprehensive development software library at your disposal.

The quickest way to get a taste of the 8085's power and versatility is with the SDK-85 System Design Kit. It's available now for only $250. You can order SDK-85 and all MCS-85™ components directly from your nearest Intel distributor: Almac/Stroum, Components Specialties, Cramer, Hamilton/Avnet, Harvey Electronics, Industrial Components, Pioneer, Sheridan, L.A. Varah, Wyle Liberty/Elmar or Zentronics.

Or, for more information on the 8085 and SDK-85, use the reader service card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. Telephone: (408) 987-8080.

intel® delivers.

CIRCLE 12 ON INQUIRY CARD

A new low for on-board programing.

AMP introduced the DIP switch to solid-state electronics. Now we've gone still further. AMP's new *low-profile* DIP switches are as low as you can get. You can use them to program ICs right-on-the-board without remote wiring. And sandwich boards in less space, to cut packaging costs.

With our new, low-profile DIP switches, cleaning boards is easier than ever. Simply place our protective covers or pieces of tape on the switches and you can clean complete boards without damage.

We're the people who developed and perfected DIP switches —a whole family of them—including our innovative, pluggable Hexadecimal Rotary Switch. Our experience is broader and deeper than anyone's. At AMP we'll have the right answers for your applications.

Bright new lights.

Unique LED DIP switches are available in SPST "on" or "off" as well as momentary-contact types. They permit rapid, visual circuit test, fault indication and programing verification. Plus, for the first time, they permit DIP packaging of LEDS.

Rockers are detented to avoid accidental actuation. Switch leads and LED leads are terminated independently for circuit connection versatility.

There's nothing quite like new AMP LED DIP switches. For more details on them, or the new AMP low-profile DIP switches, call (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

AMP
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AMP has a better way.

Management Capabilities Aid In Monitoring Communications Costs

Selection of communications management hardware has been enhanced with three additions to the family of expandable communications management systems. Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284 has aimed the compatible devices at particular problems of distribution of incoming calls, long distance cost control, and outgoing calls control.

Call processing is performed by reliable, stored program microcomputer-controlled switching or metering subsystems. One of the company's host computer systems performs functions of data base management, optimization of routing decisions, and management and facilities utilization reports.

Infoswitch™ Automatic Call Distributor (ACD) is a telephone switching and management system for uniform distribution of incoming calls among agents and agent groups, affording control and measuring of incoming call traffic and generation of detailed management statistics and reports. The turnkey system, requiring no user programming, includes a host computer, agent telephone instruments with group supervisors, and intelligent switching subsystem for automatic distribution of calls.

Also incorporated are one or more video display supervisor consoles, multiple port asynchronous communications interface, and large disc storage facility. High speed local printers may also be configured with the system. System sizes range from four to 110 telephone trunks, with from four to 72 agent positions.

The multiple Infoswitch Telephone Communications Management System (SHARE) allows multilocation corporations to economically distribute intelligent long distance telephone switching (LDCS), and local and tie-line metering facilities in the field, while maintaining centralized control over the corporate telecommunication network and data base. Main component of the various configurations is a computer with keyboard, video display screen, and large internal user memory capacity. Host computer is equipped with one or two high density cartridge disc drives.

The switching subsystem handles all processing of long distance calls; an intelligent metering subsystem can also be used to monitor long distance, local, directory assistance, and tie-line calls originating within a company. Standard and extended configurations are available.

To account for all outbound telephone calls, the Infoswitch Station Message Detail Recorder (SMDR) extends the long distance telephone control system to a full telephone management system. The intelligent switching system for long distance call control; metering subsystem for local, directory assistance, and tie-line calls; and host computer constitute the system. Printers and mag tape drives may be used with the system.

It can be configured from 16 to 2048 station lines in increments of 16 lines. Rotary dial is standard; tone dial is optional. A variety of interfaces and modems are available for external communications.

Circle 400 on Inquiry Card

2-Way Service To Access Information Via Telephone and TV

Immediate access to a store of information will be possible via an adapted domestic TV set and a telephone line with the Viewdata system. A numeric handheld keypad is used to select information displayed on the screen. As a means of stimulating telephone traffic, especially residential, the United Kingdom Post Office has been developing the teleprocessing service since 1970 to provide immediate and convenient information retrieval and interactive facilities for the general public and business community at a small fee.

Viewdata is transmitted via the telecommunications network, while Teletext is a broadcast signal. However, both services feature a common memory, character generator, and display unit of a combined decoder.

Basic elements of the Viewdata system are the terminal (TV set), transmission system, computer, and data base with progressive indexing system (treeing structure). Currently consisting of 6000 pages, the data base is expected to be expanded to 60,000 for market trials, to be held on a central computer configuration. It was decided to incorporate the line interface unit, comprised of the A-D

converter, terminal identifier, and auto-dialer (for automatic dialing of the Viewdata center from the terminal) in the TV set at the time of manufacture.

Key parties involved in the project are the UK Post Office, the TV set industry (as well as its semiconductor suppliers), and the information industry, which currently involves 80 information providers offering 300 topics with more to follow. The combined Teletext/Viewdata receiver should be through trial production by mid-1978, to coincide with the beginning of a market trial of 700 households and 300 business representatives. Following this, geographically restricted public service is expected by late 1979, with further expansion commensurate with demand.

Refinements to the system are being developed. These include closed user groups requiring a confidential pass number known to an authorized user, conversational mode designed for the deaf community, and hard copy especially useful for businesses. Further details of the system are contained in the paper entitled "'Telecommuting' by Viewdata," by Roy Bright, *Intelcom 77 Exposition Proceedings*, Vol 2, 1977, pp 595-599.

Circle 401 on Inquiry Card

Advanced Satellite Joins Expanding Global Communications Systems

The first of the Intelsat IV-A communications satellites designed to orbit over the Indian Ocean has been launched as part of the expanding global satellite communications system, to replace older models over heavy traffic areas of the 98-member countries of the International Telecommunications Satellite Organization. Over the Indian Ocean, the satellite will have beam diversity and the ability to switch two narrow beam channels to wide beam channels to cover the countries it serves.

The principle of beam diversity has allowed Hughes Aircraft Co, PO Box 90515, Los Angeles, CA 90009 to increase the satellite's capacity to relay more than 6000 simultaneous telephone calls plus two TV programs, compared with 4000 circuits and two TV channels for the earlier Intelsat IV series. To transmit the same band of frequencies twice with beam diversity, the satellite directs a communications beam with a certain frequency to one area of the world and the same frequency to another area. There is no interference because the beams are directed thousands of miles apart.

After launch, the satellite undergoes a period of testing; ground stations communicating with the satellite make equipment changes to conform with allotted frequencies. By June of 1978 these tasks will be complete and the unit will be in position off the east coast of Africa and southwest of India, delivering service to more than 40 nations.

Forms of Electronic Communications Should Depend Upon Users

Users of such emerging, interrelated forms of electronic communications as electronic funds transfer, electronic mail, and computer communications "should have the final choice" in how they are provided, according to Edward Goldstein, director of product management, American Telephone and Telegraph, 195 Broadway, New York, NY 10007. Addressing the House Communications Subcommittee discussing national telecommunications policy, he cautioned against taking any steps that would slow or stop this dynamic field. Believing that common carriers would best meet user communications needs, Goldstein added that any revisions to the Communications Act must retain flexibility to accommodate these emerging applications, which are characterized by lower cost and more convenient methods of communications.

Telecom Service Promises Substantial Savings For Smaller Businesses

Telemax II Telephone Management and Control System will save up to 30% of annual phone charges for smaller business offices with monthly long distance telephone charges above $3000. TDX Systems, Inc, 7670 Old Springhouse Rd, McLean, VA 22101 guarantees a minimum savings of 10%, above the cost of its service.

The network links the user by data circuit to a microcomputer located at an office of Southern Pacific Communications Corp, which in turn is linked by data circuit to one of the company's host computers in Virginia.

Miproc 16-AS, micropower to give you high-speed faster.

Internationally acclaimed Miproc-16 with a compute-rate of up to 4 million instructions per second is the fastest 16-bit microcomputer card family available.

Now supplied with an OEM chassis package, Miproc-16 is even more quickly brought into action.

This cost-effective application system, named Miproc-16 AS, has room for one, two or even three Miproc-16 CPU's. Smartly styled and equipped with add-in 13-slot card bay modules, fans and power supply, this new OEM chassis package eases the way into high speed microcomputing.

Instruction Power

Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

16-bit Power

16-bit program words make programming easy. 16-bit data words maintain high precision in arithmetic operations.

Addressing Power

16-bit dual memory architecture gives 65k words of directly addressable program memory *and* 65k words of data memory with 8 powerful address modes.

Interrupt Power

Multilevel, priority vectored interrupt system handles context changes in less than 2 microseconds.

I/O Power

256 directly addressable I/O channels with data I/O rates of up to 1.7 megabytes/sec. under program control, and up to 20 megabytes/sec. for DMA.

High Speed Processing Power

The unique dual memory architecture combines with high speed Schottky TTL technology to execute most instructions in a single machine cycle.

Software Power

Easy to use cross-assemblers for mainframe or minicomputer make programming faster, *and* **PL-MIPROC**, a super-efficient high level assembly language.

Hardware Power

Comprehensive range of processor, memory and interface cards backed up by sophisticated hardware development aids.

Ruggedized Power

Miproc can be configured to meet any known military specification.

PLESSEY MICROSYSTEMS

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Tel: (714) 540 9931

David Garrison,
Plessey Microsystems,
Suite 408, 11141 Georgia Avenue,
Wheaton, Maryland 20902, USA.

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654 PP044

CIRCLE 16 ON INQUIRY CARD

Long distance telephone calls for the user's office are routed through his own WATS lines, as well as over Southern Pacific's network.

Automatic callback or camp-on queuing, and least cost routing of calls are provided. Additional savings are obtained with a detailed call report that enables individual cost allocation, departmental billing, and reduced call abuse.

Circle 402 on Inquiry Card

Agreement Assures Continued Support of Data Terminals

An agreement-in-principle has been announced under which TRW Communications and Services, Customer Service Div, Fairfield, NJ 07006 will service customers of Wiltek's data communication terminal systems in existing locations and will expand the service to over 20 additional locations presently covered by TRW personnel. TRW will also acquire the spare parts inventory and specialized equipment for the installed base of the over 2000 model I and II terminals. Wiltek, Inc, Norwalk, CT will continue to provide computerized message service and actively market data communications terminal systems and data storage units.

Optical Fibers in Telephone Cable Work Successfully

Optical fibers made by Corning Glass Works, Corning, NY 14830 have been used in an existing telephone network in Italy, carrying messages experimentally more than 5.5 miles (about 9 km) without amplifying the signal. Less than 0.5" (1.3 cm) wide, the cable is manufactured by Industrie Pirelli, Italy, and was laid in Turin between two telephone exchanges of SIP (Italian state telephone organization). The experiment has been carried out by CSELT, Italian telecommunications laboratory and research study center, since September.

The high speed digital transmission system that provides the equivalent of 2000 telephone lines moved data over a single Corguide optical fiber less than 0.004" (0.0102 cm) thick at a rate of 140M bits (140M signal pulses)/s. Signals went the full 9 km without needing amplification or regeneration. Full capacity of the cable with eight fibers will be 8000 2-directional, simultaneous telephone conversations.

The lacquer-coated fibers used are identical to the 1053, except with greater bandwidth and less attenuation; they average more than 400 MHz at 1 km and less than 4 dB/km, respectively. No change in attenuation occurs over a −60 to 80°C operating temperature.

Switching System Unites Separate Telex and Data Services

Formerly separate telecommunication services such as Telex, Gentex, Datex, store-and-forward message service, and high speed data switching are integrated with the digital data switch (DDS) from Collins Commercial Telecommunications Group of Rockwell International, Dallas, TX 75207. Implemented during initial system installation or added later as an optional service, the switch can be configured for application as an international gateway, national transit, or local subscriber exchange, or any combination of these.

Major exchange building blocks of the CCITT-compatible device consist of a single network control group providing programmed control and reporting functions, and one or more call service groups performing call processing and circuit switching operations. The time division multiplex switch matrix is fully nonblocking in operation and is transparent to data. Basic implementation of the matrix provides capacity for 480 low speed or 24 high speed terminations.

A built-in administrative data system provides visibility of the operating status of the network, exchange, and dynamic traffic patterns that occur. Both network and exchange configurations adapt to dynamically changing traffic conditions.

Expanded subscriber features of the switch include automatic international routing of calls, abbreviated selection codes for national address, automatic retry and camp-on to minimize lost operator time, and call duration recording in minutes and tens of seconds. Also included are conference calling with individual recording of call durations, multiline hunting groups to form private branch exchanges of up to 30 stations, and available direct call and dedicated point-to-point circuits. □

Circle 403 on Inquiry Card

Intecolor 8031
Unretouched photo of screen.

Two very sophisticated desk top computers with two very unsophisticated price tags.

We're Intelligent Systems Corporation and we've developed two brand-new stand-alone desk top systems. Both are capable of handling an incredibly diverse range of business, control, research and financial applications—in color. Both have a better price/performance ratio than any other compact computer system on the market.

Take a look at the Intecolor 8031. A compact 13-inch 8-color CRT, it comes complete with graphics hardware and software, a built-in mini disk drive for extra storage, plus "File Handling BASIC" which lets you create, delete, and retrieve program segments from storage, by name.

Now take a look at the Intecolor 8051. Perfect if your needs call for a large-screen format. It comes with the same standard features as the 8031, but it has a big 19-inch diagonal screen and external mini disk drive.

We also have a variety of options available for both units, including a convenient bi-directional desk top printer and a new 2708/2716 PROM programmer.

Contact the ISC representative nearest you for a working demonstration of these two highly sophisticated, versatile and dependable desk top systems. Prices are based on a one unit, cash-with-order basis. Guaranteed 30-day delivery or your money back.

Intelligent Systems Corp.®
5965 Peachtree Corners East
Norcross, Georgia 30071
Telephone 404-449-5961 TWX: 810-766-1581

Intecolor 8051
Unretouched photo of screen.

Motorola's introducing

1977 MPU family introductions

- MC3870P — One-Chip Microcomputer
- MC3870CP — One-Chip Microcomputer
- MC3870L — One-Chip Microcomputer
- MC3870CL — One-Chip Microcomputer
- MC6800P — Microprocessor
- MC6800CP — Microprocessor
- MC6800BQCS — Microprocessor
- MC6800CQCS — Microprocessor
- MC68A00P — Microprocessor
- MC68A00L — Microprocessor
- MC68B00P — Microprocessor
- MC68B00L — Microprocessor
- MC6802P — Microprocessor + RAM & Clock
- MC6802CP — Microprocessor + RAM & Clock
- MC6802L — Microprocessor + RAM & Clock
- MC6802CL — Microprocessor + RAM & Clock
- MC6802BQCS — Microprocessor + RAM & Clock
- MC6802CQCS — Microprocessor + RAM & Clock
- MCM6810P — Byte-Organized RAM
- MCM6810CP — Byte-Organized RAM
- MCM6810BJCS — Byte-Organized RAM
- MCM6810CJCS — Byte-Organized RAM
- MCM68A10P — Byte-Organized RAM
- MCM68A10L — Byte-Organized RAM
- MCM68B10P — Byte-Organized RAM
- MCM68B10L — Byte-Organized RAM
- MC6821P — Peripheral Interface Adapter
- MC6821CP — Peripheral Interface Adapter
- MC6821L — Peripheral Interface Adapter
- MC6821CL — Peripheral Interface Adapter
- MC6821BQCS — Peripheral Interface Adapter
- MC6821CQCS — Peripheral Interface Adapter
- MC68A21P — Peripheral Interface Adapter
- MC68A21L — Peripheral Interface Adapter
- MC68B21P — Peripheral Interface Adapter
- MC68B21L — Peripheral Interface Adapter
- MC6840P — Programmable Timer
- MC6840CP — Programmable Timer
- MC6840L — Programmable Timer
- MC6840CL — Programmable Timer
- MC6840BTCS — Programmable Timer
- MC6840CTCS — Programmable Timer
- MC68A40P — Programmable Timer
- MC68A40L — Programmable Timer
- MC68B40P — Programmable Timer
- MC68B40L — Programmable Timer
- MC6843P — Floppy Disk Controller
- MC6843L — Floppy Disk Controller
- MC6844P — DMA Controller
- MC6844L — DMA Controller
- MC6845P — CRT Controller
- MC6845L — CRT Controller
- MC6846P — MC6802 Combo
- MC6846CP — MC6802 Combo
- MC6846L — MC6802 Combo
- MC6846CL — MC6802 Combo
- MC6846BQCS — MC6802 Combo
- MC6846CQCS — MC6802 Combo
- MC6850P — Asynch. Comm. Interface Adapter
- MC6850CP — Asynch. Comm. Interface Adapter
- MC6850BJCS — Asynch. Comm. Interface Adapter
- MC6850CJCS — Asynch. Comm. Interface Adapter
- MC68A50P — Asynch. Comm. Interface Adapter
- MC68A50L — Asynch. Comm. Interface Adapter
- MC68B50P — Asynch. Comm. Interface Adapter
- MC68B50L — Asynch. Comm. Interface Adapter
- MC6852P — Synchronous Serial Data Adapter
- MC6852CP — Synchronous Serial Data Adapter
- MC6852BJCS — Synchronous Serial Data Adapter
- MC6852CJCS — Synchronous Serial Data Adapter
- MC68A52P — Synchronous Serial Data Adapter
- MC68A52L — Synchronous Serial Data Adapter
- MC6854P — Advanced Data Link Controller
- MC6854CP — Advanced Data Link Controller
- MC6854L — Advanced Data Link Controller
- MC6854CL — Advanced Data Link Controller
- MC6854BTCS — Advanced Data Link Controller
- MC6854CTCS — Advanced Data Link Controller
- MC68A54P — Advanced Data Link Controller
- MC68A54L — Advanced Data Link Controller
- MC68B54P — Advanced Data Link Controller
- MC68B54L — Advanced Data Link Controller
- MC6860P — 0—600 bps Modem
- MC6860BJCS — 0—600 bps Modem
- MC6860CJCS — 0—600 bps Modem
- MC6862P — 2400 bps Modem
- MC6862BJCS — 2400 bps Modem
- MC6862CJCS — 2400 bps Modem
- MC6875P — Clock Oscillator/Driver
- MC6875L — Clock Oscillator/Driver
- MC68488P — General-Purpose Interface Adapter
- MC68488CP — General-Purpose Interface Adapter
- MC68488L — General-Purpose Interface Adapter
- MC68488CL — General-Purpose Interface Adapter
- MC68A488P — General-Purpose Interface Adapter
- MC68A488L — General-Purpose Interface Adapter
- MC68B488P — General-Purpose Interface Adapter
- MC68B488L — General-Purpose Interface Adapter
- MCM6830AP — 1K ROM
- MCM6830ACL — 1K ROM
- MCM68A30AP — 1K ROM
- MCM68A30AL — 1K ROM
- MCM68B30AP — 1K ROM
- MCM68B30AL — 1K ROM
- MCM68308P — 8K ROM
- MCM68308L — 8K ROM
- MCM68308CL — 8K ROM
- MCM68A308P — 8K ROM
- MCM68A308L — 8K ROM
- MCM68316AP — 16K ROM
- MCM68316AL — 16K ROM
- MCM68316EP — 16K ROM
- MCM68316EL — 16K ROM
- MCM68316EBJCS — 2048 x 8 ROM
- MCM68316ECJCS — 2048 x 8 ROM
- MCM68A316EL — 16K ROM
- MCM68708L — 8K EPROM
- MCM68708BJCS — 8K EPROM
- MCM68708CJCS — 1024 x 8 EPROM
- MCM68A708L — 8K EPROM
- MCM68332P — 32K ROM
- MCM68322L — 32K ROM
- MCM68A332P — 32K ROM
- MCM68A322L — 32K ROM

2nd Quarter, 1978

- MC6801 — Microprocessor

3rd Quarter, 1978

- MC6809 — Microprocessor

Introduced
Introducing Now
To Be Introduced

Frequency Range
MC68XX = 1.0 MHz
MC68AXX = 1.5 MHz
MC68BXX = 2.0 MHz

Temperature
MC68XX = 0°C to +70°C
MC68XXC = -40°C to +85°C

Package
MC68XXP = Plastic
MC68XXL = Ceramic

Pin-Out Variations
Suffix A, Suffix E

MC68XXBXCS and MC68XXCXCS = Screened to MIL-STD-883 Class B and C

a Hi-Rel M6800 Family

We're committed to introduce over 100 compatible microcomputer system components in 1977. This makes 94.

Yes, in addition to the recently introduced MC3870 single-chip microcomputer, we're adding well over 100 fully-compatible M6800 microcomputer system components this year.

Counted among them are the 26 types that constitute the bulk of the new Hi-Rel M6800 Family processed to MIL-Standard-883. As the simplified flow chart indicates, there is only one significant difference between Class B and Class C screening methods. For some of you that's a very big difference, so Motorola provides both. If you don't want burn-in there's no need to pay for it, but if you need it, you can get it.

Hi-Rel M6800 introductions through November and early December encompass the MC6802 two-chip system, the MC6800 microprocessor, and most of the M6800 Family functions. That includes RAM, EPROM, ROM, Asynchronous Communications Interface Adapter, Peripheral Interface Adapter, Synchronous Serial Data Adapter, Programmable Timer, and Advanced Data Link Controller. Introduction of the Hi-Rel MC68488 General-Purpose Interface Adapter is just around the corner in the first quarter of 1978. See the table at left for a complete guide to this year's Hi-Rel M6800 Family activity.

Motorola MIL-STD-883 Screening Methods

Screen	Class B	Class C	Comments
Internal Visual	100% 2010 B	100% 2010 B	
Stabilization Bake	100% 1008 C	100% 1008 C	24 Hours
Temperature Cycling	100% 1010 C	100% 1010 C	10 Cycles
Constant Acceleration	100% 2001 E	100% 2001 E	Y_1 Only
Seal	100% 1014	100% 1014	Fine and Gross
Burn-In	100% 1015		160 Hours at 125°C
Final Electrical Test	100% 3 Temps.	100% 3 Temps.	Per Motorola Device Specification*
External Visual	100% 2009	100% 2009	
Quality Conformance Inspection†	Sample	Sample	Per Motorola Device Specification*

*Can be Slash Spec.
†Quality Conformance Inspection Consists of Lot Sample Electrical Tests with Generic Groups B, C, and D. Data Available Upon Request.

Here's a quick guide to decoding the device number suffixes.

Suffix Identification

MC6800 B Q C S
- **S** — Electrical, **M** = Slash Sheet, **S** = Motorola
- **C** — Lead Finish, **A** = Hot Solder, **B** = Acid Tin Plate, **C** = Gold Plate
- **C** — Case Outline
- **Q** — Screening Level Class (See Class **B** and **C** Above.)
- **B** — Motorola Device Type

Case Outline

Case Designation	Leads	Size (in.)
C	14	0.25 x 0.75
E	16	0.3 x 0.75
V	18	0.4 x 1.1
W	22	0.4 x 1.1
J	24	0.5 x 1.25
T	28	0.6 x 1.4
Q	40	0.6 x 2.0

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CD94

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Motorola Microproducts, 3501 Ed Bluestein Blvd., Austin, Texas 78721

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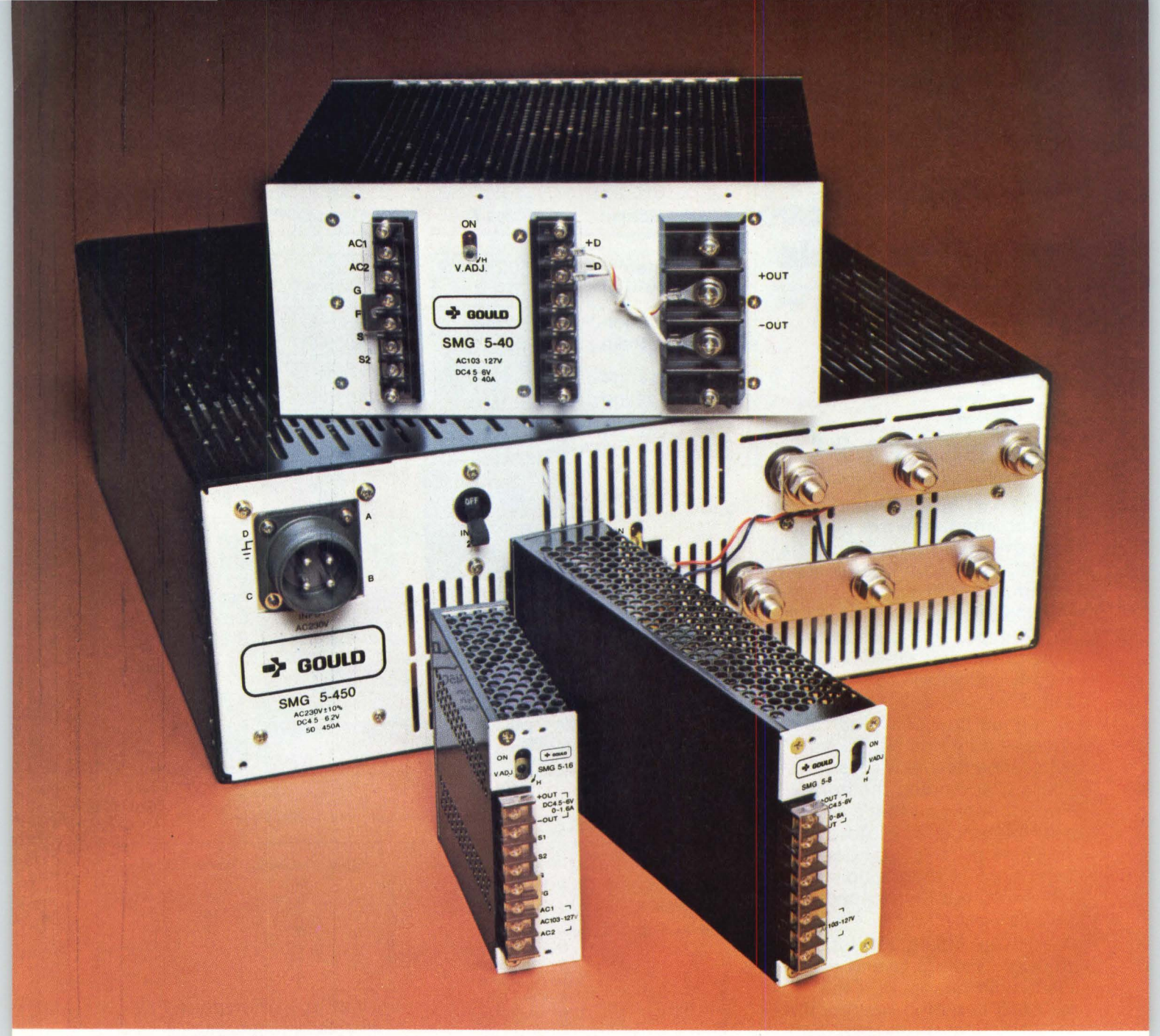


Gould introduces a new range of switching power

Gould's new SMG series lets designers switch to smaller, lighter, more efficient switching power supplies without buying more specs than are needed.

Eighteen new SMG models give the Gould line both wider wattage and a lower price range while maintaining the reliability demonstrated by more than 40,000 Gould units now in use.

The SMG series offers outputs from 8 to 2,250 watts in a wide selection of voltage/current combinations. Units rated above 500 watts are fan cooled and are front panel selectable for 110 or 220 VAC.

All SMG units have short circuit and over-voltage protection. Temperature stability and voltage regulation are outstanding. Holdup protection is as high as 63 milliseconds. There's even an LED "on" indicator on the front panel of every unit.

For complete information contact Gould Inc., Electronic Components Division, 4601 N. Arden Drive, El Monte, CA 91731 or phone (213) 442-7755. TWX 910 587 4934.

Gould.
The power in switching power supplies.

GOULD

32-Bit Computer System Contains 2M Bytes of Main Memory, 4G Bytes of Virtual Memory Address Space

Based on a 32-bit wordlength—for the first time in this computer manufacturer's history—the VAX-11/780 system announced by Digital Equipment Corp, Maynard, MA 01754 combines mainframe capacity and performance with minicomputer price and flexibility. It is claimed to be the industry's fastest computer system priced below $200,000.

The VAX (for virtual address extension) system includes up to 4.3G bytes of virtual address space and up to 2M bytes of main memory, yet is compatible with the company's 16-bit PDP-11 computer family. It has an effective memory access time of 290 ns and is capable of an aggregate throughput rate of 13.3M bytes/s. A single virtual memory operating system (VAX/VMS) allows programs much larger than the physical memory to be run in a manner that is transparent to the programmer. The system is particularly relevant to scientific, data processing, and interactive time-critical applications. It can support as many as 64 users simultaneously.

Main memory consists of 4k metal-oxide semiconductor (MOS), error checking and correction (ECC), random-access memory (RAM) chips, with a minimum system configuration of 128k bytes and a maximum of 2M. A request buffer in the memory controller increases system throughput and eliminates most needs for interleaving.

The instruction set consists of 243 instructions, nine addressing modes, and five data types. It includes integral floating point, packed decimal arithmetic, character string manipulation, and context switching instructions. Up to 15 operations combine in a single instruction. This instruction set has the same mnemonics as the PDP-11. In addition, a system compatibility mode provides the PDP-11 instruction set except for privileged and floating point instructions. An optional accelerator performs a double-precision floating point 64-bit addition in 1.4 μs.

Four hierarchical protection modes, each with read-write access control, support paging memory management. The system contains sixteen 32-bit general registers and 32 interrupt priority levels—16 each for hardware and software. It has two standard clocks—programmable real-time and time-of-year with battery backup for automatic system restart.

A synchronous backplane interface (SBI) serves as main control and data transfer path. Connection of high speed PDP-11 peripherals including high performance mass storage devices with parity checking is enabled by use of up to four MASSBUS buffered interfacing adapters; a single UNIBUS interfacing adapter allows connection of conventional PDP-11 peripherals. This compatibility permits the VAX-11/780 to be used also as host development system for RSX-11M and -11S operating systems running on PDP-11s. Throughput rate for MASSBUS to the SBI is 2M bytes/s; via UNIBUS it is 1.5M.

A diagnostic console subsystem includes an LSI-11 microcomputer with 16k bytes of read-write memory and 8k bytes of read-only memory (ROM), as well as a single floppy disc and an LA36 teleprinter. Use of this console is claimed to permit simplified bootstrapping; improved distribution of software updates; and fast, online, local or remote diagnosis. It provides automatic consistency and error checking to detect abnormal instruction uses or illegal machine conditions. Integral fault detection and maintenance features detect errors on memory or discs, record recent bus activity, detect hung machine conditions, and allow restart recovery.

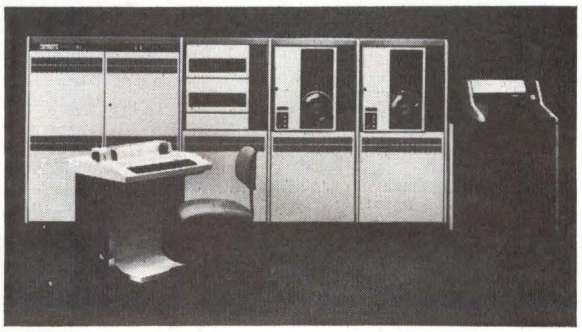
Among the automatic monitoring activities are parity checking for data integrity on the synchronous backplane interface, bus adapters, memory cache, address translation buffer, and error checking and correction on memory. In addition, operating system consistency checks, redundant recording of critical information, uniform exception handling, online error logging, online diagnostics, and unattended automatic restart are performed.

Programs as large as 32M bytes are enabled by a full demand paging operation. Multiple functions are maintained through the VAX/VMS operating system. Program development capabilities include two editors, language processors, symbolic debugger, librarian, and utilities.

Memory management facilities are user-controllable. Pages of a program or an entire program can be locked in memory for time-critical applications. There are 32 levels of software process priority for fast scheduling.

Both Digital control language (DCL) and master control routine (MCR) language are used. As with other PDP-11s, these languages implement VAX-11 FORTRAN IV PLUS, VAX-11 MACRO, PDP-11 COBOL, and PDP-11 BASIC-PLUS-2. FORTRAN and MACRO generate 32-bit native code. FORTRAN can concurrently execute a subset of the PDP-11 instruction set in its "compatibility" mode. A file and record management facility provided by the operating system permits users to create, access, and maintain data files and records with full protection. Such facilities include sequential and relative file organization, sequential and random access. Networking capabilities are supported for task-to-task, access and file transfer, and downline loading.

Batch capabilities include job control, multistream, spooled input and



Multiprogram capability of Digital Equipment Corp's VAX-11/780 32-bit computer system enables access by up to 64 interactive users simultaneously. Intended for data processing, large laboratory, and research center applications, the system contains virtual memory addressing capability of more than 4G bytes

output, operator control, conditional command branching, and accounting. Nonprivileged tasks can be run with little or no modification as a result of an applications migration executive.

Three standard configurations, available to both end-users and OEMs, are offered. Deliveries are scheduled to begin in early 1978, with volume production in mid-year.

A minimum system configuration consists of the VAX-11/780 CPU with 128k bytes of main memory, LA36 DECwriter II teleprinter, two RK06 14M-byte disc drives, and a multiplexer with eight EIA terminal connections and VAX/VMS operating system—priced at $128,000. The next configuration contains 256k bytes of main memory, an RM03 67M-byte disc drive, a TE16 800/1600-bit/in (315/630-bit/cm) magnetic tape drive, plus 8-line multiplexer and operating system—at $153,000. Top configuration has 512k bytes of main memory, an RP06 176M-byte disc drive, a TE16 tape drive, plus multiplexer and operating system—at $185,000.

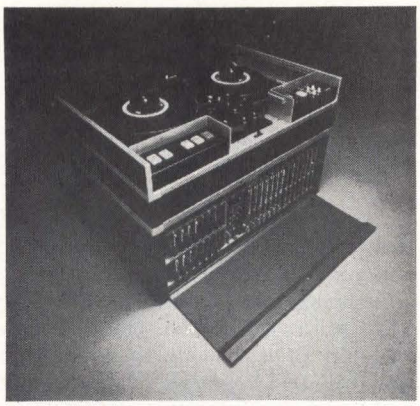
All systems have provisions for additional memory and peripherals. It is expected that the majority of systems, including chosen additional memory and peripherals, will sell in the $200,000 to $300,000 area.

Circle 140 on Inquiry Card

Portable Magnetic Tape Recording System has Bandwidths to 2 MHz

SE7000M tape recording systems are claimed by EMI Technology, Inc, 55 Kenosia Ave, Danbury, CT 06810 to bring the performance of fixed installation systems to field applications in a convenient portable form. The units have direct record/reproduce bandwidths to 2 MHz, FM recording bandwidths to 500 kHz, 7-track (0.5"tape) or 14-track (1.0" tape) channel capacities, and record at 30k bits/in with a 2.5M-bit/s serial transfer rate. Costs are claimed to be from 20 to 60% less than those for units with approximately comparable performance.

FM bandwidths include IRIG intermediate (dc to 40 kHz) and wideband groups I (dc to 8 kHz) and II (dc to 500 kHz). Eight carrier frequencies range from 1.68 to 216 kHz (INT), 3.38 to 432 kHz (GP I), and



SE7000M recording systems from EMI Technology provide fixed installation performance in portable unit. Equalizers and filters enable tape speed switch to be used like oscilloscope; calibration controls are minimized for simple operation

14.0625 to 900 kHz (GP II). A ± zero offset doubles effective dynamic range when recording unipolar data, and a squelch circuit holds the reproduce output at zero until the transport reaches synchronized speed.

FM mode input sensitivity is 0.5 to 10 V peak for 40% carrier deviation, linearity is ±0.5%, and harmonic distortion is less than 1.3% for all tape speeds. Input impedance is 20 kΩ (INT/GP I) and 75 Ω or 1 kΩ (GP I/GP II), output impedance is less than 10 or 75 Ω, and the output signal is ± 1.5 V into not less than 1 kΩ or 75 Ω.

Tape transport is a balanced tension system combining easy threading with operational performance. It provides eight switch-selectable speeds—0.93, 1.0875, 3.75, 7.5, 30, 60, and 120 in/s (2.37 to 304 cm/s)—and the capstan can be phase-locked to an external oscillator for nonstandard speeds.

Signal conditioning electronics include, in addition to input channel conditioners that operate at all tape speeds without adjustment, built-in equalizers and filters for all tape speeds in the reproduce circuits; this permits the operator to use tape speed switch like an oscilloscope time-base control, without the need for substituting plug-in conditioning modules.

Controls have been reduced to the minimum and are mostly of the set and forget type. Included are push-button fast forward and reverse, run forward and reverse, record, stop, power, ready, tape/tack, INT/WBI, WBI/WBII, flutter comp, local/remote, and a rotary tape speed select switch. A built-in FM calibrator with digital meter permits calibration of the complete FM channel without jumpers.

For high density digital recording (HDDR), a compact rack of electronics is available for recording serial or parallel data from TTL or balanced line sources, in either NRZ-L or delay modulation (DM-M) codes. A phase-locked oscillator, adjustable over a 2.5:1 range, permits use of any external clock frequency. With this arrangement an optional 14-channel stuffer can be used for continuous recording of parallel data at an increased record data rate to allow insertion of a block marker for subsequent deskewing.

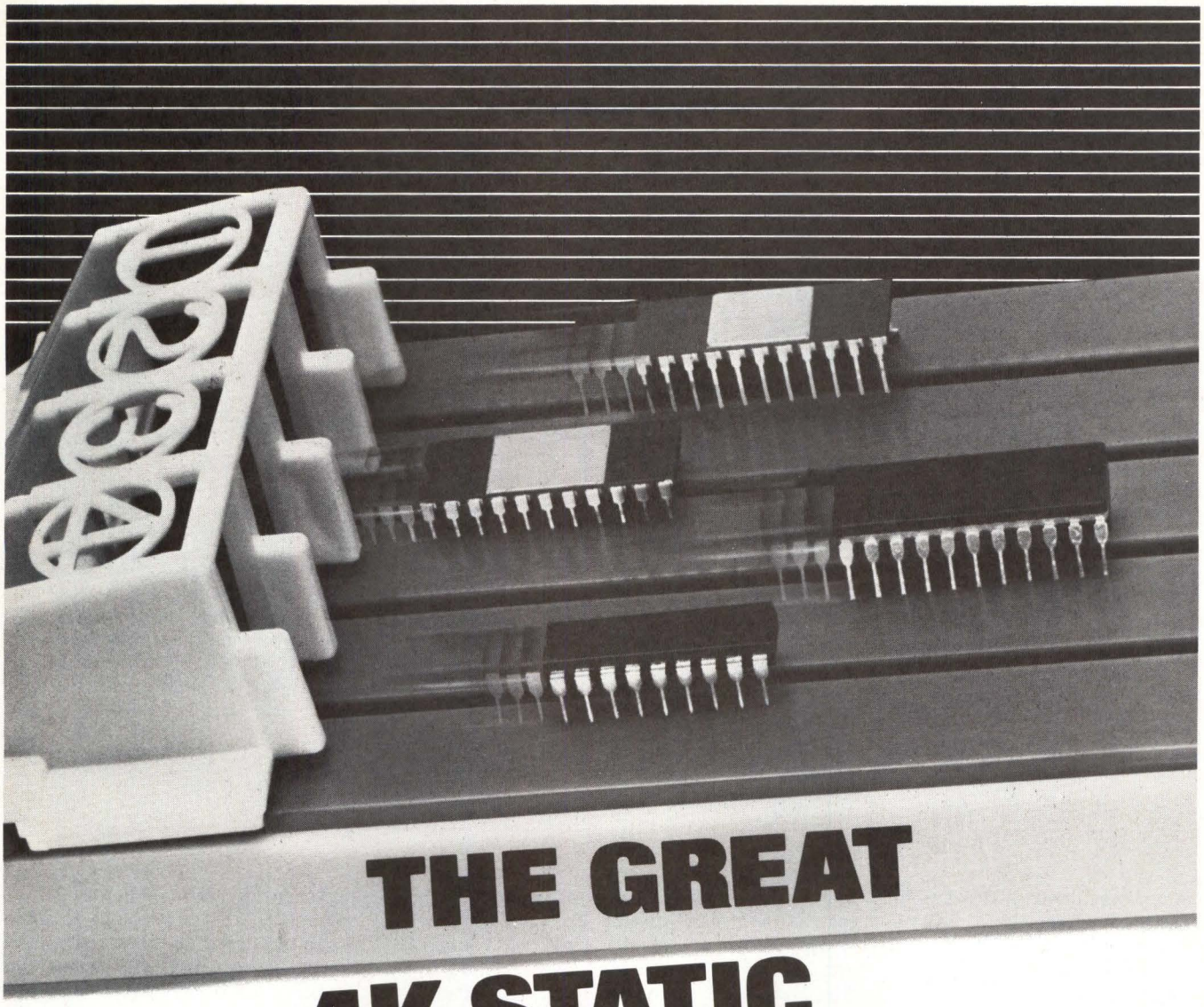
Circle 141 on Inquiry Card

Graphics Controller Uses Compatible RAMs For Variable Resolution

The MTX-512 graphics controller, designed by Matrox Electronic Systems, PO Box 56, Ahuntsic Sta, Montreal, Quebec H3L 3NS, Canada, exploits the compatibility of 16-pin 4k, 8k, and 16k dynamic RAMs to provide selectable resolutions of 256 x 256, 256 x 512, 512 x 512, and 256 x 1024 on a single controller card. Cards are designed to interface mini- or microcomputer to a TV-type monitor and produce a graphics raster that extends close to the physical limit of the scan monitor.

Variable resolution is achieved through the use of circuit design techniques which permit higher density RAMs to replace lower density RAMs. Thus, the 256 x 256 version uses 16 4k dynamic RAMs, the 256 x 512 display uses 8k devices, and the 512 x 512 and 256 x 1024 units utilize 16k versions. Standard TV interlacing, produced when lines of one field or scan fill in spaces between lines of the previous field, can effectively double vertical resolution. Vertical interlace is used to produce the 512 x 512 display; the 256 x 1024 display uses a proprietary horizontal interface technique, which permits horizontal resolution to be doubled while using standard speed memories and logic.

The unit's X-Y addressing scheme uses two directly addressable registers to select a given dot, allowing two computer memory locations to address up to 262k bits of refresh memory. The X register occupies the 10 LSBs of a 16-bit data word for a max-



THE GREAT 4K STATIC RAM RACE

In a world of claims and counter-claims, one thing is clear. EMM SEMI is still in the lead. Of course, we not only had a healthy head start, but we field a whole family of 4K static RAMs.

We *delivered* the industry's first 4K static RAM in 1975, a full year and a half before anyone else. We are now delivering 7 basic static RAM types with many versions of each, and producing them at a greater monthly rate than our nearest competitors combined.

By now we have more 4K static RAMs operating in a wider range of customer equipment than anyone else in the semiconductor memory business — from 10 Megabyte IBM add-on memory systems to hobbyist microprocessor kits.

Whatever your application, from mass storage to telecommunications, from medical electronics to toys and games, chances are there's an EMM SEMI static RAM just right for you. Please call or write today for full details — and ask about our byte oriented RAMs, too.

Memory at work EMM SEMI, Inc.

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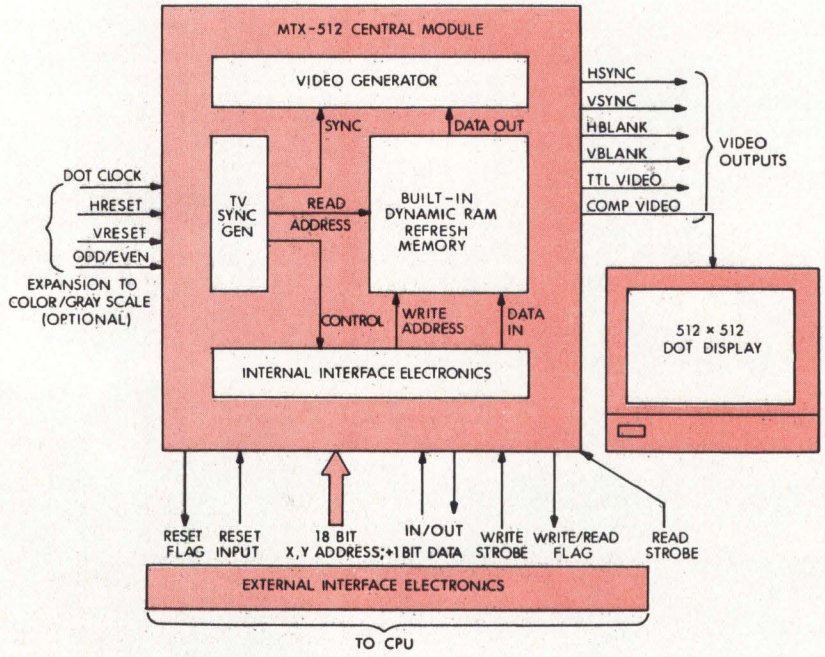
CIRCLE 20 ON INQUIRY CARD



Key to commonality of central module in Matrox's MTX-512 graphics controller is internal interface electronics. Module contains TV sync generator, video generator, dynamic RAM refresh, and internal interface electronics. Variable resolution is achieved by interchanging 4k, 8k, and 16k RAMs

imum resolution of 1024 points. The LSB of X is ignored for 512-point resolution and two LSBs of X are ignored for 256-point resolution. This allows software written for 1024-bit resolution to work for lower resolution units. This principle also applies to the Y register.

By stacking identical multiple boards, color/gray scale systems can be obtained. Each card's sync generator acts as master or slave; a master card can control up to 24 slaves. When a system consists of a master and a number of slaves, video outputs of each card are synchronous, allowing users to combine outputs to form a customized color/gray scale system with up to 24 bits/picture element.

Cards are available for the PDP-11 Unibus and the LSI-11 bus which operate using the 16-bit PDP-11 instruction set. It is possible to interface either card to other computers through a standard 16-bit parallel I/O port. Any card can be user-programmed to produce 256 x 256, 256 x 512, 512 x 512, or 256 x 1024 point matrix. American or European TV standard operation is also field programmable.

Circle 142 on Inquiry Card

Fortran Processor Subsystem Performs 1.5M Operations/s

An Attached Fortran Processor (AFP) that can execute FORTRAN programs at rates of up to 1.5M operations/s—as much as ten times faster than the B 6807—has been developed by Burroughs Corp, Detroit, MI 48232 to provide the high speed processing necessary for engineering and scientific problems. With the AFP attached to any B 6800, 6700, 7800, or 7700 computer, users gain the performance necessary for mathematical operation while retaining the system's business-oriented capability.

The AFP serves as a mathematical program-oriented subsystem to a computer which acts as the system manager. Operating under the master control program, the system manager provides an automatic control environment for the AFP and, at the same time, performs business-related data processing tasks. The AFP is programmed exclusively in FORTRAN.

Advantages of using a dedicated subsystem for high performance engineering and scientific processing lie in the structures of the problems to be solved. Architecture of the AFP is designed for processing large individual programs in which sets of data are operated on repetitively. Such programs execute most efficiently when they have complete access to processor logic, main memory, and secondary storage devices.

Three major elements make up the total system: system manager, Fortran processor, and file memory. A large standard data processing system, the system manager provides an automatic control environment for the AFP, and is responsible for compiling application programs, scheduling jobs, providing data I/O, controlling peripherals, monitoring errors, and performing online system diagnostics.

The system manager exchanges supervisory information with the AFP via two I/O channels linking the AFP

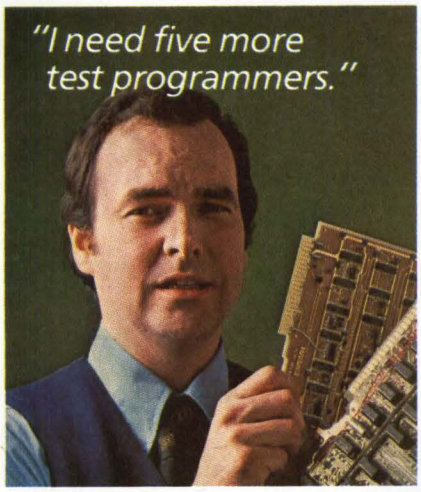
The P400 makes excuses obsolete.

A new product comes on line and the circuit boards start piling up. This is when the excuses begin:

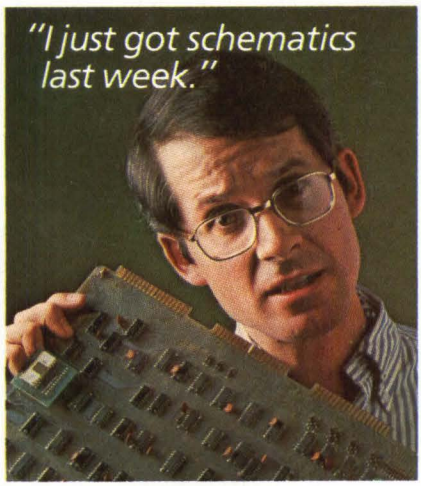
"I can't get near the computer."

"I need more programmers."

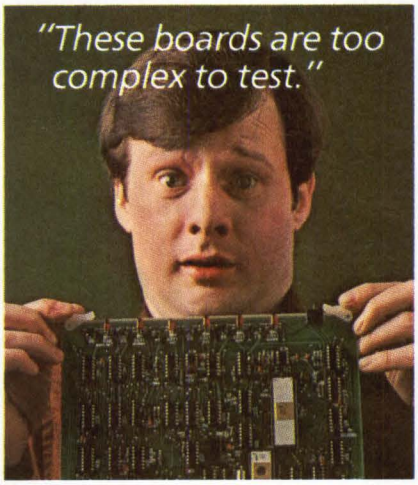
"I just got schematics last week."



It's a difficult time for a test engineer because the success of an important product can hang in the balance.



But Teradyne's P400 Automatic Programming System has changed all that. Used with L100 series test systems, the P400 creates the entire test program



automatically. It gives you all input patterns, provides all diagnostic data, and resolves all races. It cuts programming time from weeks to days. And it does it all without tying up the computer on your production tester or increasing your programming staff.

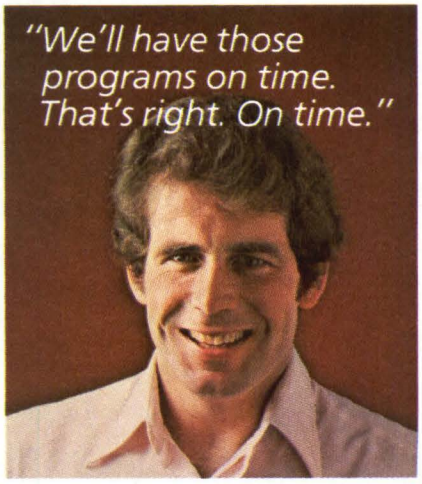
Suddenly, new programs can be ready on time, even in the face of the tightest schedules. And even for the most complex boards.

Just as important, the P400 spares you all the boring work it usually takes to deliver new programs. You get typically better than 95% fault coverage simply by using the telephone to access a large computer containing the P400 software.

The P400 Automatic Programming System.

Now there's no reason for being late.

And we think that's the way you want it.



TERADYNE

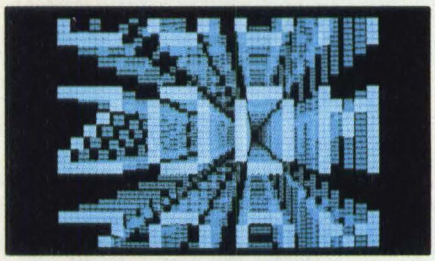
183 Essex Street, Boston, Mass. 02111

Most graphics terminals are too dumb for words.

Even expensive models get tongue-tied when it comes to alpha-numerics. But now there's a bright new graphics terminal that has a lot to say for itself.

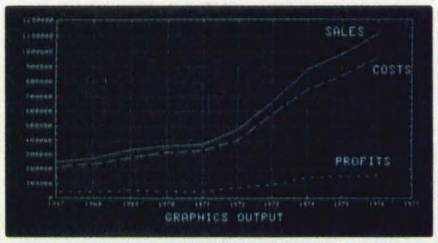
Alpha-graphics: the perfect combination.

It's the Hewlett-Packard 2648A alpha-graphics terminal. For just $5500* it will dazzle you with a



virtuoso display. You'll see zoom and pan, area shading, pattern definition, rubber band line, scientific plotting and graphics text composition. Having independent memories for graphics and alphanumerics, you can do auto-plots with or without words and figures on the screen.

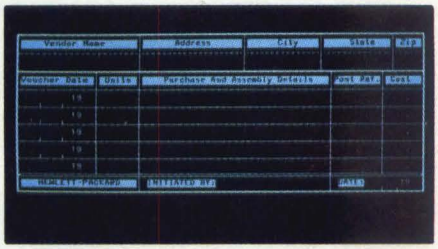
And when you need a smart alphanumeric terminal for on or off-line work, stay right where you are.



How smart is smart?

Ever seen a graphics terminal scroll 200 lines of interactive dialogue? And store up to 220K bytes of data (words and pictures) on twin cartridges? And cut out repetitive routines by storing up to 80 characters on each of eight "soft keys"?

The HP 2648A can also edit with the best of them. Communicate with a computer at rates up to 9600 baud. And accept a plug-in forms drawing mode to generate just about any form your company uses.



Strong as well as intelligent.

Like all our terminals, the HP 2648A has a clean, tough, modular design. Open it up like a suitcase, and you'll see the neat row of plug-in PC boards.

That makes it easy to add options or take care of maintenance. Not that downtime is a problem. Our terminals have such a good track record that we've lowered our maintenance price three times in the past two years. When you do need service, more than 1000 Systems and Customer Engineers worldwide are ready to take care of you.

So why settle for any dumb graphics terminal when ours can figure in your picture? See for yourself by calling the Hewlett-Packard office listed in the White Pages. Or send us the coupon and give our 2648A alpha-graphics terminal a screen test.

Yes, give me the good words (and pictures) on the HP 2648A terminal.

☐ I'd like a demonstration. ☐ Send me information.

Name Title

Company

Address

City/State/Zip

Phone

Mail to: Ed Hayes, Marketing Manager, Hewlett-Packard Data Terminals Division, 19400 Homestead Road, Dept. 1214, Cupertino CA 95014.

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**U.S. domestic price*

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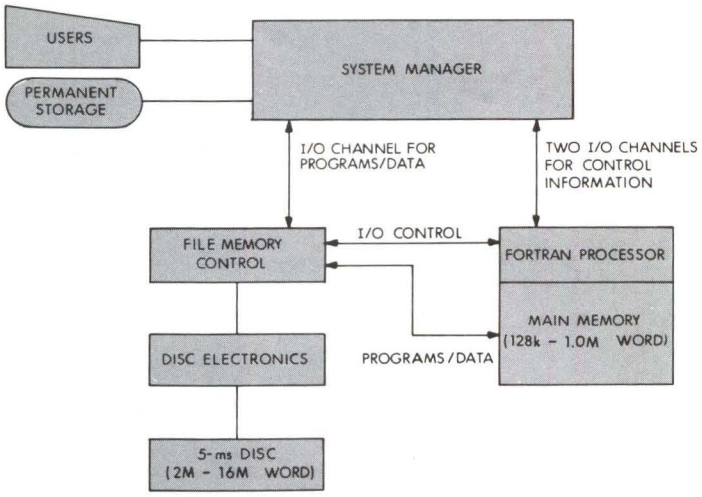


Serving as mathematical program-oriented subsystem to general-purpose computer, Burroughs' AFP has complete access to processor logic, main memory, and secondary storage devices of main system. Processor can execute FORTRAN programs at up to 1.5M operations/s

with the manager's I/O processor. Programs and data flow through an additional channel linking the I/O processor and the AFP's file memory. All peripherals and data communication lines operate through the manager's I/O control and communications processor, eliminating unnecessary I/O interference with the AFP's processing.

Fortran processor, the central processing element in the subsystem, operates at 12.5 MHz. Main memory uses 4k MOS ICs with cycle speed of 160 ns. Expandable from 128k to 1M words capacity, memory is augmented by high speed data and instruction buffers. This processor includes a control maintenance unit which interfaces with the system manager for initialization and for communicating supervisory and maintenance commands. The control maintenance unit has access to critical data paths and registers in the AFP subsystem for fault detection and isolation. It monitors the error detection circuits and reports problems to the system manager.

Internal hardware registers are used for fast arithmetic processing; a memory stack and special register allocation allow efficient subroutine entry, exit, and recursion. High speed buffers are provided for transferring data and instructions between processor and main memory, and for storing temporary results. Four instruction words are transferred in parallel to and from main memory in 160 ns.

The file memory control unit handles the Fortran processor's I/O requests, space allocation directions, and file security keys. The Fortran processor can unlock files or space in file memory for the system memory, which can then independently transfer programs and files to file memory.

The AFP FORTRAN compiler generates code that optimizes use of subsystem resources. AFP FORTRAN is a subset of the language developed for the Burroughs Scientific Processor (BSP) and is also compatible with the system manager's FORTRAN, allowing programs to be moved between systems simply by recompiling.

Circle 143 on Inquiry Card

Copy Processing Systems Use Totally Redundant Large Data Bases

A family of five 2530 series copy processing systems, introduced by Harris Corp, Composition Systems Div, 505 Rodes Blvd, Melbourne, FL 32935, offer large data bases, data base and controller backup facilities, high speed wire line handling, and advanced editorial terminal capabilities. Combination of capabilities with standard product packages for each model results in substantially lower costs than were previously feasible. Four systems—models 2531, 2532, 2533, and 2534—are designed for copy processing; the fifth—2539—performs general-purpose business data processing tasks and serves as a backup for other systems used in copy processing and production work.

Dual data base storage devices of 66M bytes each provide 132M bytes capacity for each system. Data bases on copy processing models are fully redundant for protection and security; in the business system, all 132M bytes can be used for conventional processing applications. Fail-safe protection techniques include a spare processor and cabling on each of the copy processing systems. Options include a "hot spare" controller which can be brought up within several minutes, direct access to an additional single backup data base, or access to the dual data base and controller of the data processing system for conversion to copy processing mode.

Smallest copy processing system is the 2531, which consists of system controller with 128k bytes main memory; HNS/2 operating system software; four 1720 editorial terminals; and interface to support OCR, high and low speed wire lines, online typesetting, and online MicroStor and 2200 systems, plus two 66M-byte duplicate recording disc drives. Expandable from four to 28 terminals,

ANY WAY YOU LOOK AT IT.

THE PDP-11/03 FAMILY OF MICROCOMPUTER PRODUCTS.

If you're an OEM thinking about putting a microcomputer in your product, you ought to know which company has the most complete range of products in the industry. The answer is:

Digital.

And you know all these products will work together because they were designed to. From the start.

High Performance Hardware. We begin with the 16-bit PDP-11/03. It gives you over 400 basic instructions, optional floating point, and incredible throughput—thanks to its highly integrated PDP-11 multi-function instructions. And it comes complete in a box with power supply and fans.

If you need more room, there's our new PDP-11/03-L—a bigger box with more slots, 32Kb of MOS, universal power supply, bootstrap with diagnostics and monitor lights, and space for up to 32Kb of UV-PROM or ROM.

For communications, we have both asynchronous and IBM-compatible synchronous controllers, a multiplexer with four lines on one board, and modem control for remote uses.

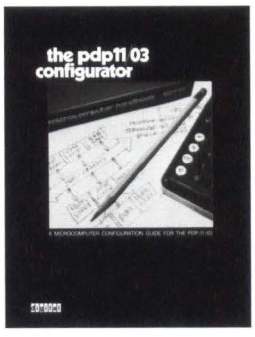
All this plus an IEEE #488 instrument bus, four processor options, eight memory options, and ten I/O options.

Proven Software. Choose from two high-performance real-time operating systems that have proven themselves in thousands of installations: the high-speed RT11, or the RSX11—our event-driven multi-tasking version. Languages include MACRO, BASIC, MU-BASIC, FORTRAN and APL.

Worldwide Service. We don't sell you and forget you.

As a Digital customer, you are supported by 6600 professionals operating out of 350 locations worldwide.

We can be on the spot within hours and our well-stocked regional depots help cut repair time even further.



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While other microcomputer companies are still trying to build systems from the bottom up, we've already got two field-proven OEM packages designed from the top down—using all the systems expertise we gained with our larger computers.

The Floppy Disk PDP-11V03 comes complete with 32Kb of MOS memory and your choice of a hard-copy or video terminal.

And the memory can be expanded to 56Kb—more than enough for foreground/background operation.

The 11V03 comes with dual floppy disk drive, hardware bootstrap, and the RT11 operating system—standard. It's simple to use, simple to install, and totally compatible with the rest of the PDP-11 family, so you can sell new systems without designing new programs.

The Hard Disk PDP-11T03 is the only microcomputer-based hard disk system on the market.

It comes with CPU, 32Kb of memory, hard copy or video terminal, a 7.5 million byte disk sub-system, and RT11 operating system—standard.

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Anyway you look at it.

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PDP 11/03-L

THE WORLD'S MOST COMPLETE MICROCOMPUTER SYSTEM.


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the system has a console control unit for precise systems monitoring. Interfaces permit attachment of paper tape reader and punch, 180-char/s printer, and multiplexer ports for up to 16 devices.

The 2532 is similar except that its basic capacity supports eight 1700 editorial terminals and up to 24 multiplexer ports for extended I/O device attachments. Using four MicroStor controllers, terminal capacity is expandable to 32 terminals, consisting of eight 1700 devices and 24 MicroStor reporter terminals. Additional terminals can be added using wire lines and other I/O interface ports. In a standard configuration the system consists of eight terminals, 128k main memory, 132M bytes of disc storage, and other features.

A basic 2533 includes 12 series 1700 editorial terminals; 24 additional reporter terminals can be attached using up to four MicroStor controllers. Video layout and phototypesetters can be added to achieve total copy processing system capability.

Top end of the family is the 2534, which includes 16 editing terminals, and as many as 16 other I/O devices within its 32 multiplexer port configuration. By adding up to four MicroStor controllers and their associated six terminals/controller, the system can be expanded to 40 reporter input and editorial terminals.

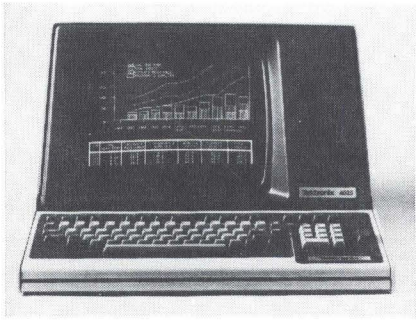
The 2539 is a dual purpose processor that represents a business data processing system as well as a totally redundant backup processor for any of the copy processing systems. The system's 132M-byte data base operates as two independent 66M-byte storage units. When converting to copy processing backup mode, the business data processing software, HNS/ADMIN, is simply replaced with HNS/2 copy processing system software, terminals are recabled, and copy processing disc packs are loaded into the systems' disc drives.

Circle 144 on Inquiry Card

Display Terminals Allow Scrolling of Both Alphanumerics/Graphics

Computer display terminal model 4025 is claimed to be the first to allow scrolling of both alphanumerics and graphics as well as the only raster scan terminal that can copy 53 lines with the company's 4631 copier. Tektronix, Inc, Information Display Group, PO Box 500, Beaverton, OR 97077 has directed the series at the predominantly alphanumeric user with limited need for graphics.

Display on the 4025 is divided into 640 x 480 addressable points for graphing purposes. Graphic information is stored using a virtual bit map method, which allows graphic memory to be integrated into the alphanumeric memory list, and permits alphanumeric and graphic information to be scrolled together.



Tektronix' 4025 raster scan display terminal integrates graphics and alphanumerics using virtual bit map to store graphic data, and separate memory for alphanumerics. When alphanumeric data are scrolled, graphics display scrolls along with them

In the terminal, a virtual bit map references cells of graphics memory to the display list rather than to specific addressable points on the display screen. When the display controller scans the list and comes to a part designated as graphics, it goes to graphic RAM rather than to alphanumerics ROM. The pointer in the alphanumerics list, instead of pointing to a specific bit in the virtual bit map, points to a group of bytes that designate the dot pattern for the part of the graph that is included in one character area (8 x 14 dots).

This technique also allows hard copy to be produced in an 8.5 x 11" (21.6 x 28 cm) typed report format. This is accomplished by connecting the 4631 copier to the terminal's display controller.

Terminal model 4024 provides alphanumerics for users who need only forms capability. Both units are microprocessor-based terminals with local function capability.

Circle 145 on Inquiry Card

Minicomputer Configured With Virtual Memory For Distributed Processing

The 2200VS offers ease of program development and implementation, and a smooth growth path from small- to medium-scale computers, contributing to the benefits of distributed data processing. The interactive system, introduced by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851, is a multijob, multiuser system with a common data base which integrates all user functions into one overall system. In a small configuration, the WSC/60 includes 64k bytes of memory, one workstation, one 10M-byte disc drive, one diskette drive, and a 240-line/min printer. The largest configuration of the WSC/80 has 512k bytes of RAM and can include up to 23 workstations, up to eight 288M-byte disc drives, 9-track magnetic tape drive, diskette drive, and various printers.

Based on the 2200VS processor, WSC/60 and WSC/80 systems feature virtual memory. The memory management technique utilizes disc storage as an extension of physical CPU memory to give each workstation a virtual memory area of 1M bytes. This means that programmers do not have to modularize or overlay programs, or partition or swap; programming costs are substantially reduced.

Each workstation provides the user with direct conversational communication with the computer through the CRT/keyboard console. The 1920-char screen display features dual intensity, blinking and audible alarm. System functions are called through a command processor; the procedural language handles both batch and interactive modes.

System modularity results from the use of independent, intelligent I/O processors (IOPS). Each IOP controls several devices, handling all data transfers between the device and memory on a direct path. I/O and CPU

processing take place concurrently, maximizing throughput and requiring a minimum of overhead.

To support use in distributed processing systems and provide general capability to communicate with remote systems and support remote I/O, the processor provides a communications option. Implemented with a special I/O processor, which occupies one IOP slot in the CPU, the option supports one or two bisynchronous lines at speeds of 1200, 2400, 4800, or 9600 baud. Protocols include 2780/3780 emulation, 3270 emulation, remote 2246P workstations, and HASP.

ANSI-74 COBOL, RPG-II, and BASIC languages, plus an assembly language, containing most instructions of the IBM 360/370, are supported by the system. Programs can be written incorporating all four languages, and programs based on each can be run simultaneously on the system at different workstations.

An interactive text editor, symbolic debug facility, three utilities for data entry/file maintenance, and utilities for sort/merge/copy are provided. Other features include automatic program sharing, automatic data compaction, print spooling, memory error correction, and an ID/Password security system.

Circle 146 on Inquiry Card

Dispersed Processor Offers Concurrent Data Entry/Communication

The diskette-based 1500 dispersed processor offers intelligent data entry and local data processing capability, as well as concurrent communication with remote location. The system may operate standalone or in conjunction with a host computer.

In the system, Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, incorporated an advanced processor, typewriter-style keyboard, two diskette drives, high speed video display, and integral communications capability. The display presents 24 lines x 80-char on a nonglare green-on-black screen; an inverse video feature can be programmed to highlight fields such as error messages or program status indicators.

The processor contains 32k bytes of RAM and an additional 4k of system ROM. Processor and support circuitry as well as system memory are all on a single board. System memory provides complete support for communications I/O, display and keyboard logic, an optional serial printer, and diskette I/O.

Software for intelligent data entry, local data processing and storage, and communications is provided. DATAFORM® or DATABUS® programming languages and the diskette operating system allow the system to verify data entered before they leave the system. The operating system dynamically manages the internal flow of data, maintains system reliability and security, and provides for maximum usage of system and associated devices.

With the addition of an appropriate communications modem, the integral communications interface facility supports communications with other systems. Using either an IBM 3780 emulator or DATAPOLL communications software, the processor can transmit data at speeds to 4800 baud in synchronous mode. Under the DATAPOLL package the system acts as a slave processor, automatically transferring text files to and from a central processor.

Under the multitasking operating system, the system can run two programs at once. A primary application (data entry or processing) can proceed at the same time as a secondary program (communications or print spooling).

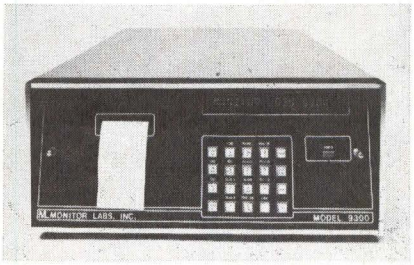
Circle 147 on Inquiry Card

Smart Data Logger Uses Microprocessor To Add Features

System 9300, a smart data logger, handles thermocouples and voltage side-by-side, autoranges, produces engineering units, averages, and provides up to four different alarm levels per channel. The unit, announced by Monitor Labs, Inc, 4202 Sorrento Valley Blvd, San Diego, CA 92121, is built around the F8 microprocessor, which enables it to implement in software many functions previously handled by hardware.

The unit features simple setup and daily operation through a ROM-stored application program. Operator entered data are stored in RAM, and an EAROM program save option provides backup during power outages. The operator programs the unit via a 20-key pad, responding to English language questions displayed on a 20-digit alphanumeric display.

Thermocouple linearization and compensation are handled by the application program, which accepts operator-entered slope and intercept corrections for each channel. Alarm and limit levels are also implemented in software. Each channel has four individually programmable limits. The



Handling temperature and voltage side by side, 9300 series data logger from Monitor Labs uses ROM-stored program to provide easy setup and daily operation

operator specifies which devices will output under alarm conditions, including reporting by exception.

The unit precisely measures analog inputs from 1 μV to 12 V, either with autoranging or by selecting the 30-mV, 300-mV, 3-V, or 12-V range for each channel. Resistor networks are available for measuring current or higher voltages.

A universal reference for thermocouples is located on each isothermal connector. Each channel is digitally compensated, allowing adjacent channels to mix thermocouple types and voltages, while maintaining 0.1-degree resolution and high accuracy.

Data on any or all 40 channels can be averaged through digital accumulation and division. Sample period is selectable from the keyboard, allowing up to 999 samples/average. Invalid data are automatically excluded from the average, which is computed for the remainder of the current period following a power outage.

(*Continued on p* 42)

There may be a µP board out there we can't test.

But we haven't found it yet.

Chances are we won't. Dozens of different μP boards have run through our new 3040A Logictester™ in the first six months, with 100% success.

You never know what our rapidly changing technology will produce tomorrow though, and you need assurance your tester can handle it. The 3040A delivers that confidence, and more.

Like testing at full data and clock rates. Four bi-directional buses handled at one time. And four processors test your board's μP instructions, RAMs, ROMs, PIAs . . .all at multi-MHz rates!

All this and programs finished in *days,* not months.

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Circle 22 for literature.
Circle 23 for a demonstration.

Standard equipment includes a 4½-digit digitizer, battery-protected clock, 16-column alphanumeric printer, 20-digit alphanumeric display, dual scan modes, and monitor mode. The system expands to 1040 inputs with good channel-to-channel isolation through low thermal switches. High normal mode rejection ratio is supplemented with an optional multipole active filter.

An optional monitoring feature called Mag-Check immediately verifies that each data record is properly written on magnetic tape. This feature uses a built-in buffer controller which reads what is written and compares the record to data initially placed in the write buffer. If an error is detected, data are erased and the record is rewritten.

Circle 148 on Inquiry Card

Enhanced Process Control System Allows Central Control with Color CRTs

Contending that CRT consoles will supplant conventional analog displays in industrial-instrumentation installations, Honeywell Inc, Process Control Div, 1100 Virginia Dr, Fort Washington, PA 19034 announced enhancements to its TDC 2000 process control system. These additions to the system allow centralized control with color video displays, and can be applied to simple process units or to complex plant installations.

System enhancements include historical and real-time trend recording, alarm annunciation and display, logging, CRT and keyboard interface to intelligent multiplexers, and digital start/stop operations. System security is guaranteed with Uninterrupted Automatic Control which automatically detects malfunction of from one to eight controllers, alerts the operator, switches in a reserve controller, and resumes control of the process.

The distributed control concept provides centralized operations with three levels of capability: basic, supervisory, and total. All three provide automatic transfer of control to reserve controller devices and redundant process-interface units, and permit remote placement of control and interface equipment.

A basic configuration supplements fundamental control interfaces with a logger/printer. Three video stations replace single-function panel mounted devices for alarming, recording, indicating, and timekeeping. On the supervisory level, the center consists of one supervisory station and two or three basic stations. Used when enhanced display and computational functions are required, it performs alarm-scan functions as well as data handling and control. The total approach is used when complex programmable computing capability is needed.

Circle 149 on Inquiry Card

Vision System May Allow Computers to Handle Inspection Tasks

If computers can be given "eyes," they will be able to process visual data, and can then be used to handle inspection tasks as well as jobs involving the transfer and assembly of parts. Scientists at the General Motors Research Laboratories, General Motors Technical Center, Warren, MI 48090, after several years of investigation, have formulated two approaches which were reported at the Fifth International Joint Conference on Artificial Intelligence in Cambridge, Mass recently.

Described by Drs Michael L. Baird and Walton A. Perkins, each of the two approaches uses a television camera. Images picked up by the camera are digitized and relayed to a computer. From this point, however, the methods differ.

Dr Baird's system uses a program to sharpen the image so that the computer can rapidly and reliably find non-overlapping parts even on visually confusing surfaces which tend to camouflage the parts' outlines. Using digitized data (a mosiac of minute squares in shades of gray), the computer works through a sequence of image enhancement operations to silhouette the part and emphasize its outline. From this well-defined outline, position and orientation of the part can be calculated.

The computer vision system presented by Dr Perkins can recognize and determine the position of several objects, even if they overlap and are partially obscured. To achieve this, the computer is shown the parts it is to recognize. It analyzes each part, computes geometric properties of its boundaries and internal holes, forms a model, and stores these data. Characteristics of objects which the camera views are then matched to the stored data, allowing the system to recognize those parts that are similar even when partially obscured. When a part is found, its position and orientation is determined.

Claimed to be the first industrial computer vision system of its kind, SIGHT-I, installed at GM's Delco Electronics Div in Kokomo, Ind, locates and calculates the position of transistor chips during their processing. The computer-camera system also verifies a chip's structural integrity and rejects those that are defective.

According to the scientists, the next step is to couple the computer vision system with a manipulator, so that it can "do something" with the recognized part. This manipulation problem is currently under study at the Research Laboratories.

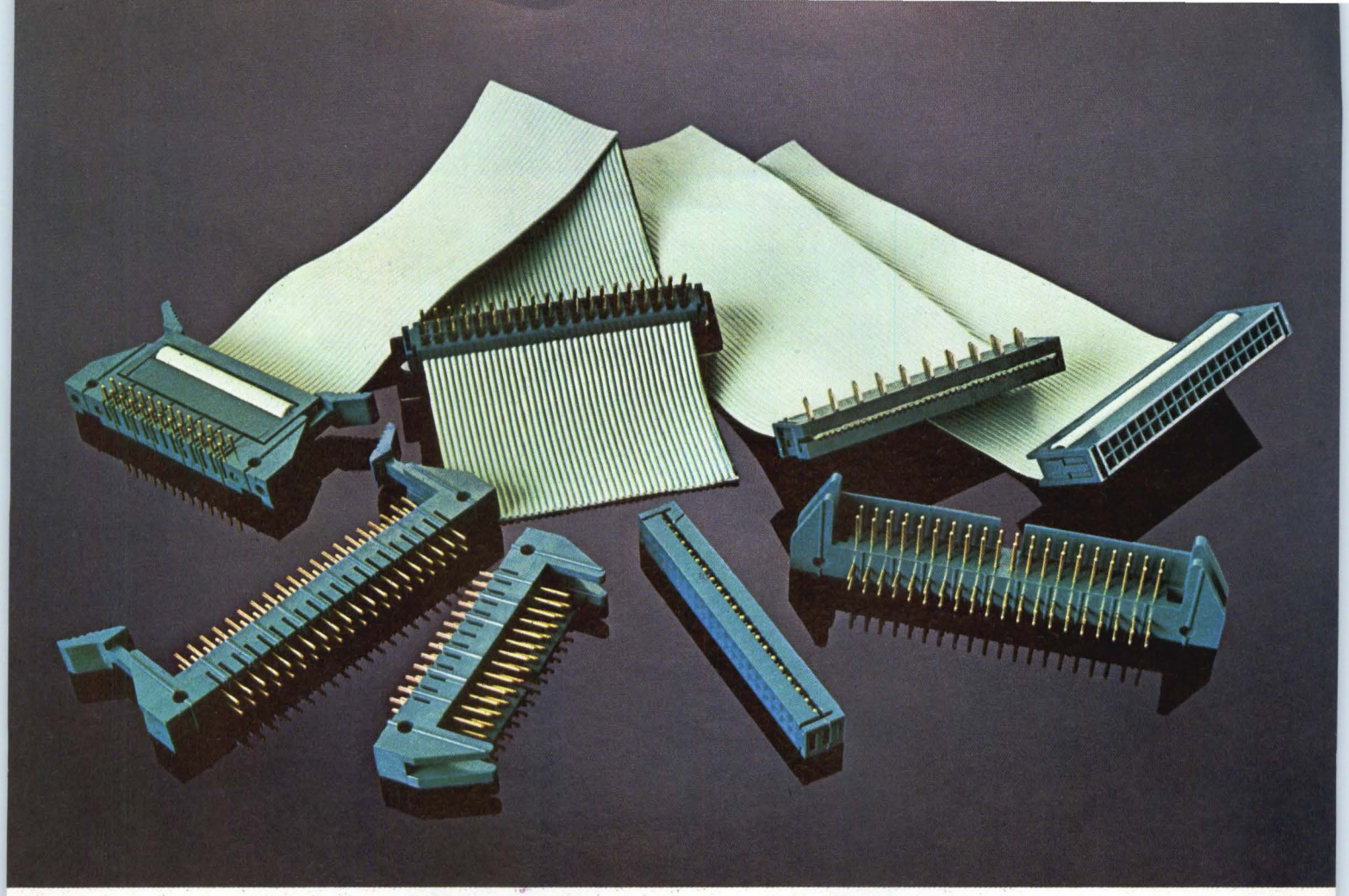
Circle 150 on Inquiry Card

Document System Adds Word Processing To DECsystem 10

An automated document management system (ADMS) has been developed by Adapt, Inc, 450 Sansome St, San Francisco, CA 94111 specifically for the DECsystem 10 and 20. With ADMS, users of these systems will be able to manage an unlimited number of large and small documents interactively, thereby adding the dimension of word processing to their data processing capabilities.

The package, a user-oriented text processing language that allows flexibility in processing of documents, features justification/hyphenation, automatic page makeup, page size flexibility, footnoting, universal commands, and automatic numbering as well as photocomposition, typewriter terminal, or microfilm output. Information can be accessed directly from a data base and converted into camera ready pages. The system is suited for interfacing with most data processing systems presently in use, and will not greatly reduce the total processing power of the system.

Circle 151 on Inquiry Card



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CIRCLE 24 ON INQUIRY CARD

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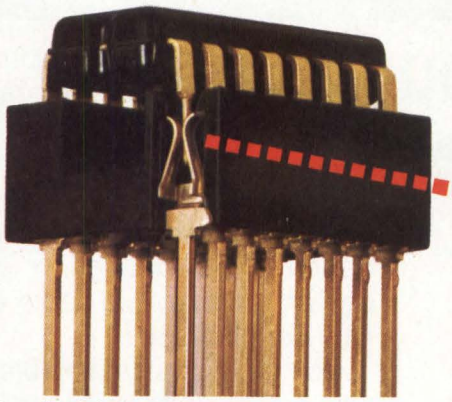
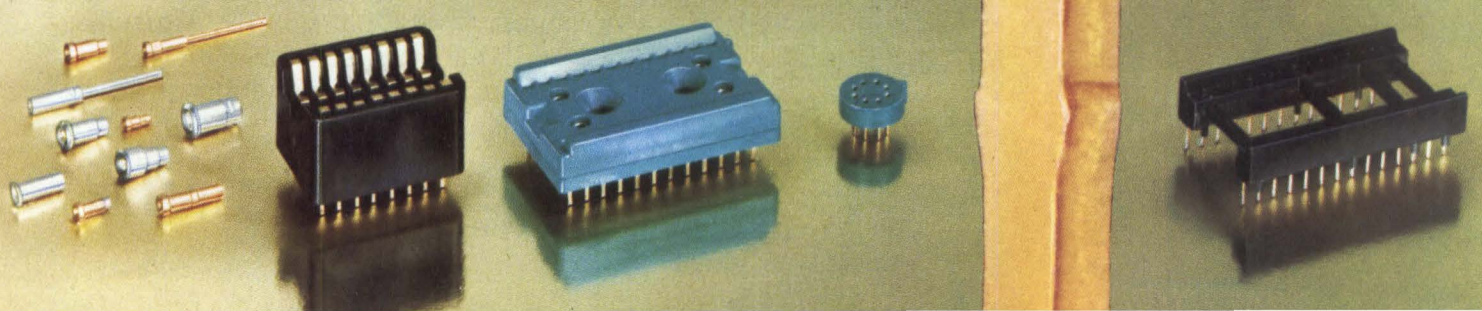


Get the **high reliability** that eliminates trouble. RN DIP sockets make contact with the wide, flat sides of your IC leads. This provides **100% greater surface contact** for positive electrical connection.

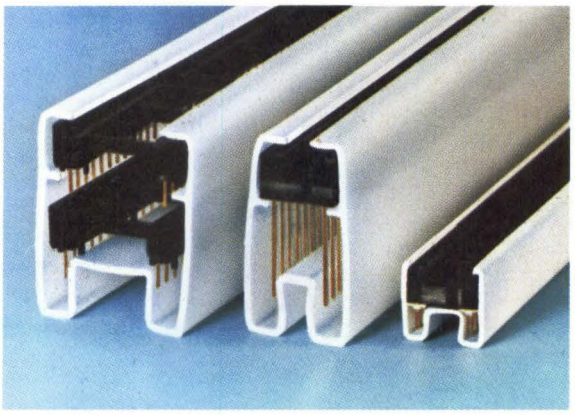


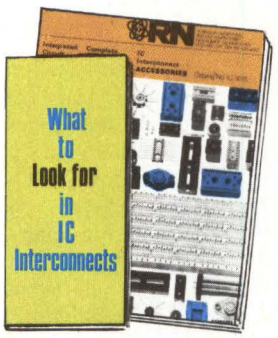
DIP SOCKETS for the price you're paying for junk!

Robinson Nugent "side-wipe" DIP sockets make 100% greater contact than any edge-bearing socket on the market.

This 100% greater contact with the wide, flat surface of your IC leads is your guarantee of unmatched reliability. This RN "side-wipe" contact provides constant low contact resistance. No edge-bearing contact can possibly deliver this long term dependability. This designed-in reliability of RN DIP sockets is your assurance of trouble-free IC interconnects—yet they cost no more than ordinary sockets.

Put an end to troublesome junk sockets! Write today for catalog and informative book *"What to Look for in IC Interconnects."* It's free from RN—the people who make more kinds of high reliability IC sockets than anyone.





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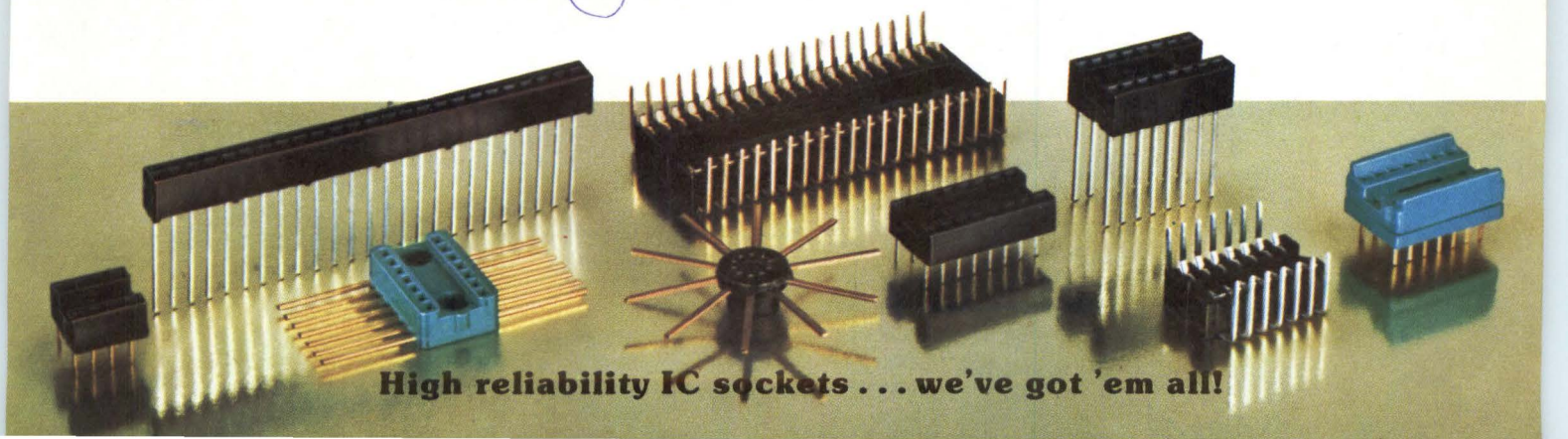
CIRCLE 25 ON INQUIRY CARD



Computer System Uses Editing Terminals to Speed Braille Production

A computer configuration containing two 4070 central processors will be used in the production of braille literature. Supplied by GEC Computers Ltd, Elstree Way, Borehamwood, Hertfordshire WD6 1RX, England, the equipment will be used in the Royal Institute for the Blind's printing center to produce a range of braille books for educational, vocational, and recreational purposes.

The configuration will include two CPUs, each with 192k bytes of core memory; four 4.8M/4.8M-byte fixed/removable cartridge disc units; two 300-line/min printers; two 9-track 800-bit/in magnetic tape units; four digital I/O devices; two control thermal printers; paper tape unit; four magnetic tape cassette decks for braille coded tapes; and two cassette decks for maintenance and diagnostic programs. Input and text editing terminals are Lynwood displays. Braille editing terminals and manual cassette encoders were specially developed by Sigma Electronic Systems.

Operators at 16 text entry visual display terminals key in text from English originals. The computer system directly accepts these inputs and translates data into braille output coded onto magnetic tape cassettes. These cassettes control embossing machines that automatically punch the braille characters onto zinc plates for use on a printing press.

Visual display terminals allow operators to edit text on entry. Separate refresh graphics display terminals are used to edit the braille characters prior to committing the output to embossed paper or zinc.

Circle 152 on Inquiry Card

Report Writing System Eases Access to Public Data Bases

A simplified means of obtaining information from demographic, economic, or corporate data bases, the Qwick Query report writing system is available on General Electric's MARK III® remote computing service. The system has access to several public and proprietory data bases maintained by CACI, Inc, Washington, DC, which were previously accessible only after programming report requirements, and is suitable for use in accessing corporate records.

To retrieve information and format reports from office terminals, users define categories of information in a data dictionary according to their own specifications. Complex calculations or comparisons can be reported by answering queries made by the system.

Dictionaries are available for Site II, a demographic data base of population and housing information categorized by ZIP code, county, state, and metropolitan statistical area, and for County Business Patterns, which lists vital statistics of commercial organizations by county. Both are derived from Bureau of Census data.

Circle 153 on Inquiry Card

Transaction Controller Allows Interactive Screen Formatting

A transaction-oriented software monitor developed by Interdata, Inc, a unit of Perkin-Elmer Data Systems, 2 Crescent Pl, Oceanport, NJ 07757 enables online transaction processing systems to be developed, implemented, and maintained. The Interdata Transaction Controller (ITRAC) runs on the company's 32-bit systems, and features compatibility with COBOL language, interactive screen formatting, and online screen-form testing capability.

Compatibility with COBOL enables application programmers to focus on the application, providing high productivity and avoiding training costs. Interactive screen formatting allows rapid implementation by new users.

Screen form designers format their screen on the CRT face as desired. Data entry fields and user prompts or cues are marked with a special keyboard character. The entire screen face is sent to the transaction controller which responds with a series of interactive fill-in-the-blanks forms, which solicit information for input data validation when the system is put into service.

Online testing allows forms to be completely tested before they are used. An online utility transaction called modify allows specific changes to be made without affecting the rest of the screen, and without changing the COBOL program. These features shorten development cycles and speed system maintenance.

ITRAC runs as a series of related tasks under the operating system; users can also run other online or batch tasks, including the multiterminal monitor. Communications services transparent to the user are provided through ITAM with the system's line control module. System requirements are a model 7/32 or 8/32 processor with at least 192k memory, 10M-byte disc, communications, and a model 1200 terminal.

Circle 154 on Inquiry Card

Business Software Adds Capability to Color Control Systems

Software packages for use with computerized color control systems provide additional production control capabilities and operating cost reductions. With the Cogit system, the computer system from Applied Color Systems, Inc, PO Box 5800, Princeton, NJ 08540 will generate production batch tickets, formula explosions, and a current product cost analysis as well as give detailed information on quantities and costs of raw materials onhand and onorder, work-in-process, and finished goods.

Interactive operation between operator and video terminal provides detailed descriptions of various possible responses to program questions. The software monitors all phases of color matching operations including modification of production formulas complete with manufacturing instructions, explosion of formulas to production quantities, and generation of complete batch tickets. □

Circle 155 on Inquiry Card

Announcing a small breakthrough.

TI's compact Model 763 send/receive terminal with built-in bubble memory.

The new *Silent 700** Model 763 Memory Send/Receive Terminal is a data entry breakthrough in a small package. It's the table-top terminal with powerful ASR capabilities...all built-in.

Magnetic bubble memory.
Built-in bubble memory means you can enter and edit data off-line, then transmit it when you want to.

The bubble memory is expandable, in the terminal, to 80K bytes. And it's non-volatile, so it retains data even when the power is off.

With the 763 you have the standard ASR functions such as playback on/off, record on/off, rewind playback and record, and playback forward and reverse. And the built-in, easy-to-use text editor brings new power to data handling.

***Silent 700* Performance.**
Virtually silent 30 characters-per-second printing, a hard copy you can keep, and excellent value is what the 763 offers with its *Silent 700* heritage.

It's microprocessor based, which means fewer components for more reliability, less weight and size.

There's a keyboard that's as familiar to use as a standard typewriter, and there's TTY current loop or EIA interface standard.

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TEXAS INSTRUMENTS.

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Cargo Vessel Load Stresses Simulated by Multipoint Computer Systems

When Spanish cargomasters loaded gold and silver ingots aboard their tiny vessels for the long trip from the Americas to Europe, they distributed the weight as best they could by instinct and by rules based on experience. Yet many of those cargo ships are still being sought by treasure hunters hoping to salvage their bullion. Instinct and experience did not always suffice against hurricanes and unexpected shifts of unbalanced cargoes.

Even in more modern days, on much bigger vessels, manual calculations—and experience—were the chief tools when deciding where to store certain cargo and what cargo to place in specific ship locations. On the whole, those methods were successful. Ships managed to move from port to port safely—if not always comfortably.

Today, however, the situation is drastically different. Merchant ships are designed and built for specific types of cargo. Each class of vessel—containership, RO-RO (roll on-roll off or trailer carrying) ship, drilling vessel, oil tanker, bulk carrier, O/B/O (oil/bulk/ore) carrier, LASH (lighter aboard ship) vessel, ore carrier, and "ordinary" cargo ship—has unique lading requirements.

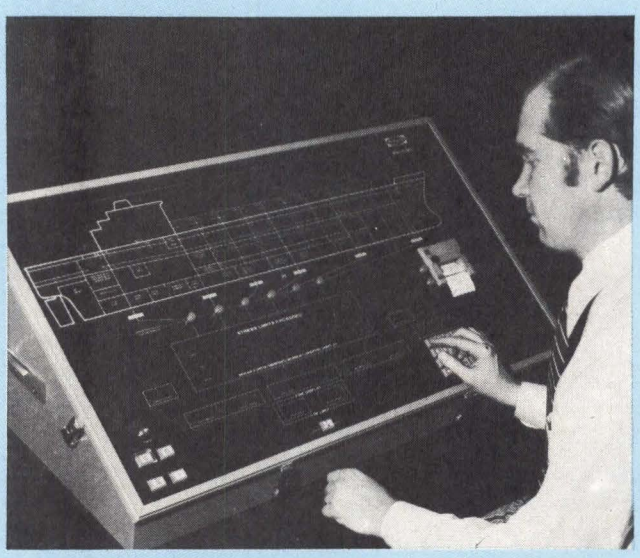

Fig 1 Typical LOADMAX-200™ system. "Live" mimic diagram configuration at top of front panel is for a trailership (designated RO/RO for roll on/roll off). More than 100 cargo locations are specified and considered in calculating shear force and bending moment limits. Tonnage information for cargo to be stored at each specified location is entered through keyboard. Microprocessor constantly updates overall data

Such special problems that must be considered in lading involve hull stresses, stability, and trim. Stability is particularly important with the relatively new LNG (liquified natural gas) carriers because of the cargo's low specific gravity.

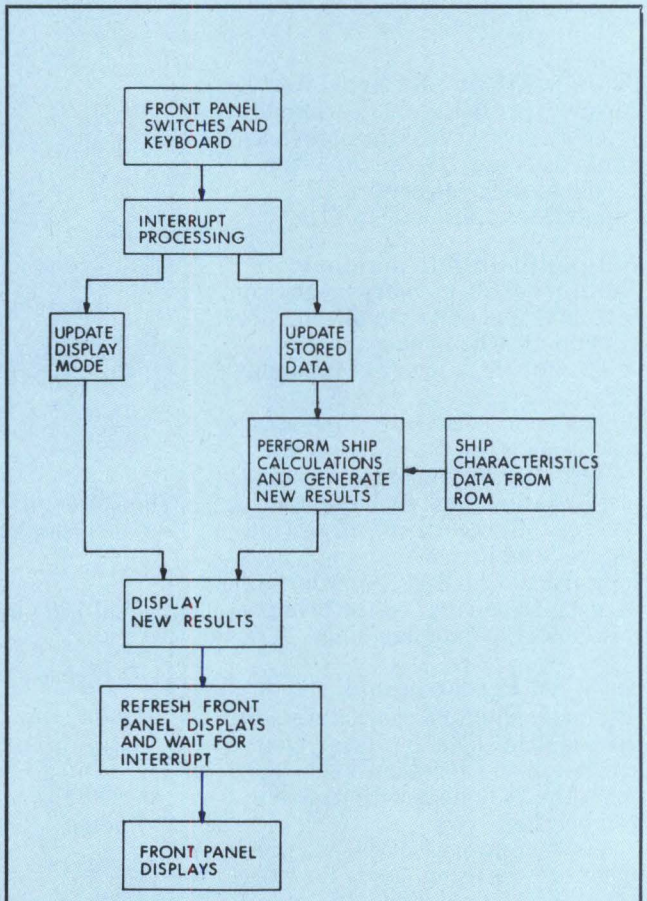

Fig 2 System data flow diagram. Ship locations and data on cargo to be stored at those locations are entered by cargo officer through keyboard on front panel. These data interact with data on characteristics of the ship (stored in ROM) to determine effects proposed loadings would have on ship's balance. Shear force and bending moment effects as well as summary of total weight at each location are displayed on front panel

(*Continued on p* 50)

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CIRCLE 27 ON INQUIRY CARD

Still another factor involved with all these ships, although not concerning safety, is the time required to unload, reload, and return to sea. This consideration can have a strong effect on economics and profit structures.

Digital Loading Computer System

One method of accurately determining proper loading and stability for a vessel is LOADMAX™ (a commercial designation for load monitoring and control system). Basically a digital computer system with unique display panels (mimic diagrams) for each vessel (or class of vessel when applicable), LOADMAX-100 computes shear force, bending moment, draft, and displacement (or deadweight). A more sophisticated model, the -200, performs stability calculations in addition. The system operator or ship's cargo officer instantly knows the effect of any suggested amount of cargo on a ship *before* that cargo is loaded aboard.

Each system, designed and built by Raytheon Co, Maritime Systems Dept, W Main Rd, Portsmouth, RI 02871, is about as simple to use as a desk calculator yet retains the value of the cargo mate's experience and knowledge (Fig 1). The "live" mimic diagram for the vessel being loaded depicts each storage and ballast area on that vessel. Knowing the weight and dimensions of each cargo unit to be loaded, the cargo officer can address any one of the many individual locations and "load" the cargo through a small keyboard.

Data on longitudinal and vertical centers of gravity, hydrostatic characteristics, and stress limits for the vessel and for each addressable location are maintained in nonvolatile memory. This memory cannot be affected by operator error, line voltage fluctuations, electromagnetic or radio frequency interference, or other factors. Shear force and bending moment effects are calculated and compared to stress limits, then displayed on the front panel.

As the operator introduces tonnage data through the keyboard, that information appears on the display directly above the keyboard. When a tonnage entry is made for any storage location, the data are again displayed on the mimic diagram at the specified location. Cumulative effects of all loadings are shown on several displays at the lower center of the front panel. Excessive shear force or bending moment values and any load that causes stress limits to be exceeded are shown both numerically and graphically. Fig 2 indicates the data flow throughout the system.

In effect, a cargo officer has a continuous presentation of loading distribution, drafts, and resultant stresses throughout the vessel. This presentation is always current since the system also computes and displays distribution

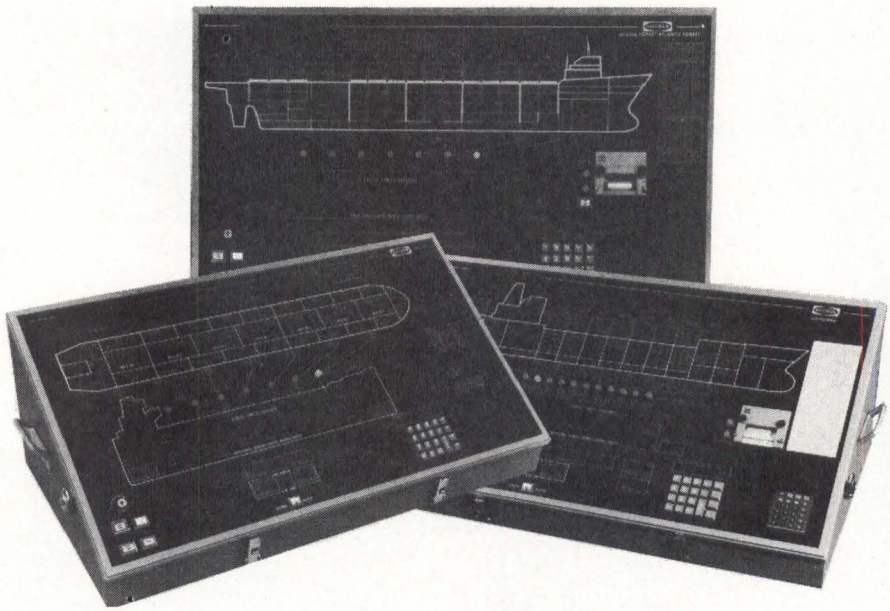

Fig 3 Front panel variations. Lower left configuration is for ore carrier; upper center panel is for LASH (lighter aboard ship) and contains impact printer for hard copy record of data; lower right configuration for containership includes small calculator in bottom right corner and blank white space alongside printer for grease pencil notations. Other formats might include clipboard for notes on cargo to be loaded. Still other mimic diagram configurations are used for drilling vessels, oil tankers, oil/bulk/ore carriers, and liquified natural gas carriers

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All our standard goodies.

A big 12-inch screen, 128-character ASCII set, upper and lower case, Typamatic repeat on all keys, and a 24-line display are standard. The same goes for our exclusive No Hassle toll-free 800 number. One call gets you service. Where you need it. When you need it. Worldwide.

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CIRCLE 28 ON INQUIRY CARD

and weight of fuel and other consumables on the ship. A recall function on the keyboard permits the operator to obtain a display on the keyboard window of the total tonnage entered for any tank or cargo area.

The graphic display provides a "curve" of computed values on a scale of 0 to ±199.9%, in either shear force (SF) or bending moment (BM) as chosen by a pushbutton at the bottom of the panel. An "excess" alarm light for each point alerts the operator to stress values of ±100% or greater. The numeric display shows the values of shear force and bending moment simultaneously for any readout point selected by the operator by pressing one of the pushbuttons above the display.

Two sets of shear force and bending moment maximum values are stored in the permanent memory. One is for normal "still water" conditions, while the other allows temporary higher hull stress limits to be maintained during loading and discharge through use of a "port condition" mode. In addition, a "light ship" switch allows all tonnage entries to be cleared instantaneously, setting up the system for all new input.

The keyboard address code enables distinction among cargo, ballast, and consumable tonnages so that the system can provide separate totals for each. Data also can be input from punched cards, magnetic tape, discs, or other devices. The system will reject illegal entries such as an attempt to make tonnage in a location a negative value by removing more than exists at that point.

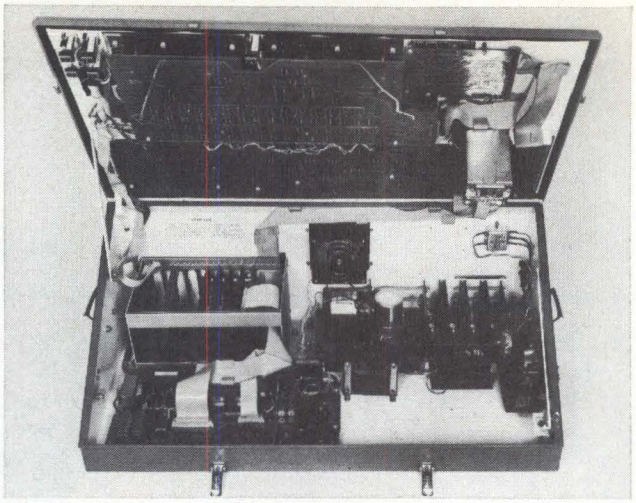

Fig 4 Interior view of system cabinet with cover raised. Printed circuit boards in subchassis at left rear of cabinet contain 8080A microprocessor for system, up to 16k of p/ROM in 8k units, 2k RAM, and separate 8080A microprocessor for printer control. Remainder of cabinet contains front panel/printer interface electronics and emergency power source capable of supplying memory power for up to four hours after main power fails or is disconnected

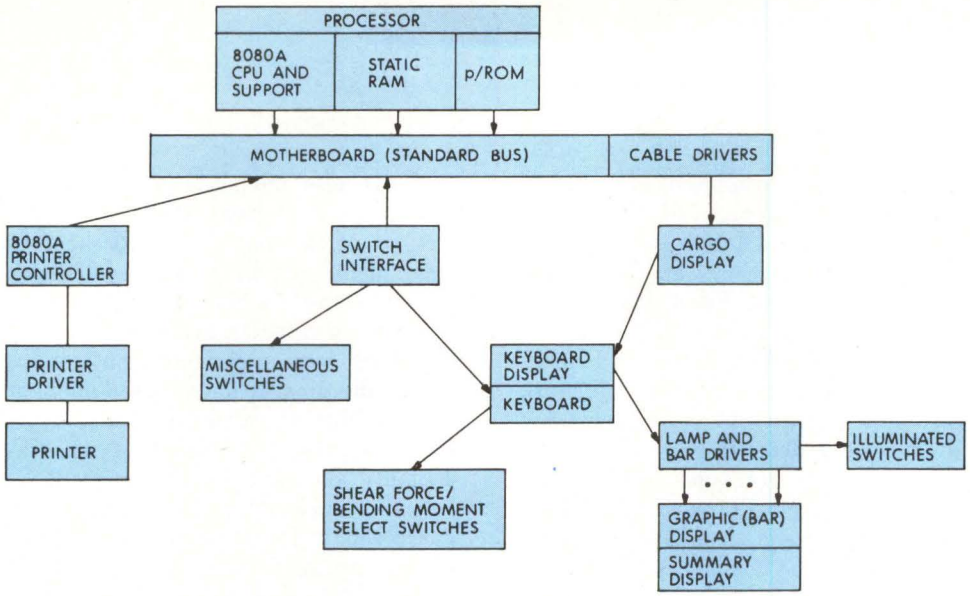

Fig 5 Block diagram of overall system. Processor interfaces to all switches, displays, and printer assembly via motherboard bus. Up to 16k bytes of p/ROM can be supplied (in 1k increments, 8k per board) as data base for permanent ship statistics and program. RAM maintains displays based on both p/ROM-stored data and information input through the keyboard. Processor CPU is 8080A microprocessor; separate similar microprocessor maintains line buffering, matrix character conversion, timing, and control of dot matrix printer

(*Continued on p* 54)

Various mimic diagram panel configurations are attainable (Fig 3) to match the storage areas of practically any vessel. A maximum of 64 4-digit light-emitting diode (LED) individual tonnage displays and 16 digital summary displays can be included. Panel legends can be provided in any of several languages, and engineering measurement units can be either metric or British.

If desired, a Practical Automation, Inc miniature alphanumeric impact data printer can be included for a hardcopy record of desired data. It provides 20 columns in ASCII format on 2.25″ (5.7-cm) paper. This printer routinely prints out a record of each entry made through the keyboard. On demand, it will print out a full tabulation of final entries by tonnage categories as well as a summary of final calculations and values of the percent of shear force/bending moment at each readout point. It will also print out a complete "sailing report."

System control is maintained by an 8080A microprocessor located on one of several printed circuit boards housed on a subchassis in the left rear of the system case (Fig 4). This microprocessor performs calculations and updates displays within 2 s for a complicated ship. It works out the balance of the ship, the relation of ship and load, the moment for the ship to get its trim in the water, and the total load weight to obtain mean draft. It also computes shear force/bending moments at each readout point along the ship between adjacent sections of the hull. Up to 16 shear force/bending moment points can be accommodated depending upon requirements of the application.

To perform these calculations, the microprocessor (Fig 5) selects data on each location from up to 16k bytes of electrically-programmable read-only memory (p/ROM) and combines them with information received from a 2k-byte random access memory (RAM). The p/ROM data base contains both program and permanent conditions of the ship that must be considered in all calculations. The PC board subchassis houses p/ROM boards (up to 8k/board in 1k increments) as well as the RAM board and a separate 8080A microprocessor board for the printer.

System accuracy is within 0.4% for draft and stability between light ballast and full load. Power requirements are 90 to 135/185 to 255 V, 47 to 63 Hz 1ϕ, 750 W max. Operating temperature range is 0 to 55°C if no printer is included (0 to 50°C with printer); nonoperating range is −40 to 70°C. Both ranges are at up to 95% relative humidity, non-condensing. Claims for the system include that the cost can usually be returned in a single voyage because of the increased earning capability. Circle 160 on Inquiry Card

DC&AS BRIEF

Multiterminal Systems Offer Variations of Supervisory Control

Redac 800, a microprocessor-based, supervisory industrial control system especially designed for transit, pipeline, and conveyor applications, is made up of combinations of Redac 800 master and Redac 80 remote communications terminals. Basic system and components are manufactured by Westinghouse Electric Corp, Industry Systems Div, 200 Beta Dr, Pittsburgh, PA 15238. Possible configurations include one master and several remote terminals; one master tied to several other masters, each of which is tied to several remotes; a 16- or 32-bit central computer tied to several masters, each in turn tied to several remotes; or a central computer tied directly to several remotes. Other components can be added to enable direct digital control.

A master terminal, using an internal microprocessor as controller, can handle up to 96 remote terminals on one to four party lines as well as a port to the central computer. A data logger can be included if desired. Either 25- or 32-bit word lengths can be handled for remote addressing, data transfer, control, and checking. A single printed circuit board contains all logic, decoding memory, 16 status inputs, 16 analog inputs, and a 300-baud FSK modem.

Remote terminals are based on large-scale integrated circuit technology and are capable of withstanding harsh environments. A standard unit can operate at an ambient temperature of 50°C; a −20 to 70°C optional range is also available.

Before a remote terminal performs a control function, it checks with the master in BCH coding to be certain a received message is correct. Functions can be controlled with either latched or pulsed capability. Because a single-word interrogation system is used, the remote's 300-baud modem becomes equivalent to a 1500-baud system; however, for expanded operation, the terminal can be supplied with a 1200-baud FSK modem (capable of 9600 baud) or an RS-422 channel providing 76.8k-baud direct line switching. □

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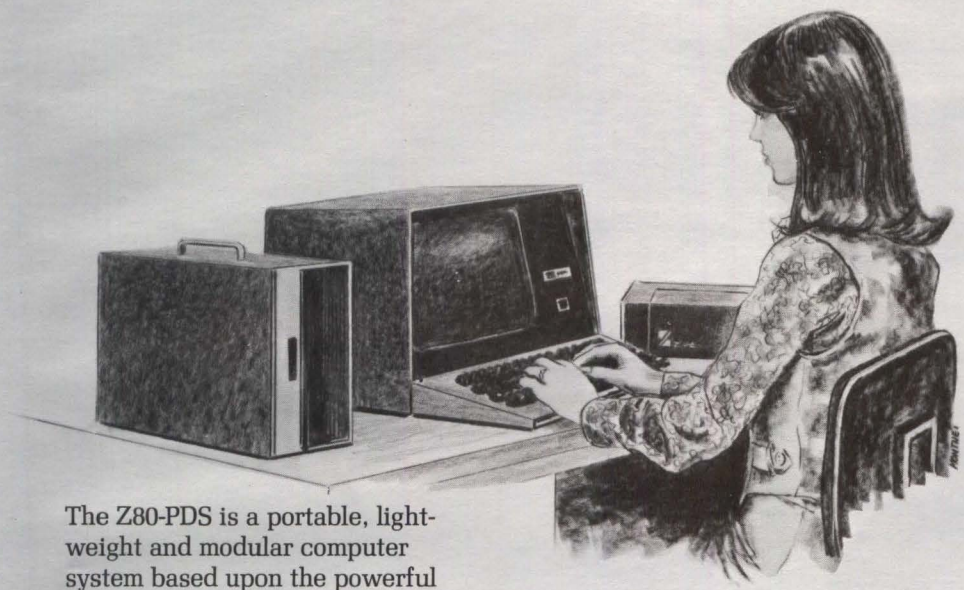
A low-cost high performance programmer's work station.



The Z80-PDS is a portable, lightweight and modular computer system based upon the powerful Z80-CPU. It offers an ideal solution for developing and debugging Z80 programs. The PDS is available with options that allow easy expansion for additional I/O or memory. And the price for the basic Z80-PDS is only $2850* That includes:

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☐ Optional items available: • Printer I/O Port • Zilog Video Monitor and Keyboard • PROM Programmer • Up to 64K bytes of Memory • Additional Serial or Parallel I/O Ports.

Full disc compatibility with Zilog's larger Development Systems makes the Z80-PDS an excellent low-cost work station for adding program development power to microcomputer design teams.

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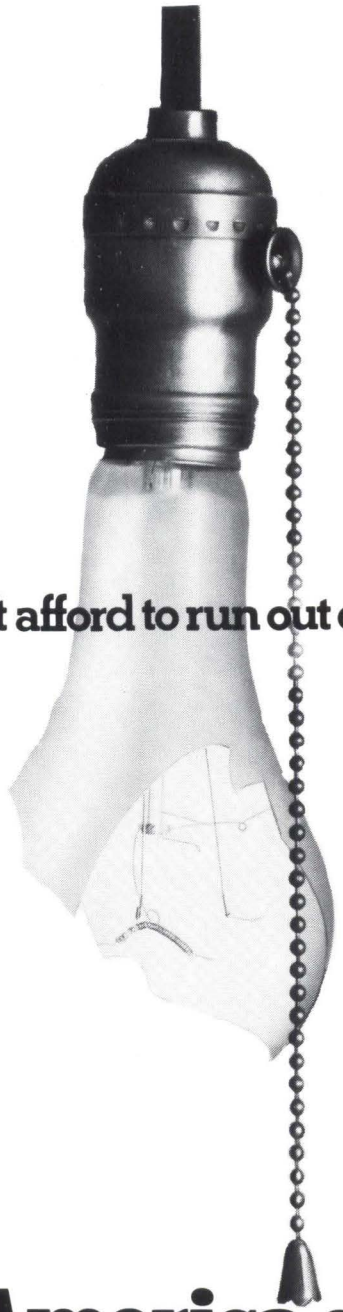

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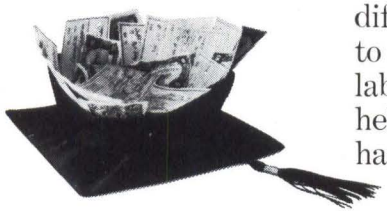

Basic digital principles for classifying and distinguishing complex analog signals using computational algorithms are presented for system designers. These algorithms are particularly conducive to modification and optimization by computer software

Pattern Recognition: Basic Concepts and Implementations

Dennis Feucht

Tektronix, Incorporated
Beaverton, Oregon

Clearly distinct but interrelated phases—data acquisition, pattern analysis, and pattern classification—evolve in a typical pattern recognition task. During acquisition, analog data (such as speech, environmental variables, or process changes) are gathered from physical sources (such as transducers, sensors, or detectors) and converted into a digitized format for computer processing. Then, the data are examined for recognizable structures or features that can be formulated for further systematic investigation. Typically, data analysis includes feature extraction, feature selection, and cluster determination. Finally, the analyzed information is best-fitted by computer algorithms to a known class of patterns for identification.

This discussion first defines the problems in pattern recognition, and then surveys the current approaches to decision-making and classification. Two techniques in particular—clustering and learning—are examined in detail.

Pattern Recognition Tasks

Three phases exist in the pattern recognition task: (1) acquisition of analog data and conversion to digitized data, (2) extraction of features (characteristics) from collected data, and (3) classification of data by these features. For example, physical variables, such as sound or light intensity, are converted by means of transducers (such as microphones, or photocells) into electronic signals. Further processing converts these physical data into a digital form capable of being further processed by a computer (first phase).

For a complex waveform (such as sound waves), it is necessary to determine what features are most useful for classifying the waveform (second phase). If the pattern recognition (PR) system designer knows the classes, a set of features is selected (often empirically), and transducer signals are processed to extract the desired features. Consider the classification of speech signals. One approach is to select frequency ranges over the audio spectrum (100 to 3500 Hz for speech recognition), and then to measure how much of a given sample of a speech signal falls within each frequency band. These measurements are the features extracted from the speech signals. The system could extract these features with electronic hardware, or it could extract them by converting the speech signals first to digital signals and then to the appropriate features. For small computer systems, the latter approach is less attractive since it usually requires large amounts of memory to store digitized speech.

After the features are determined, a PR system must have some method to identify them as belonging to a particular class of patterns (third phase). The designer must develop a classifier, usually in the form of a set of decision functions. Decision functions may be determined by trying them on a set of patterns for which the classifications are already known, and then modifying them until a satisfactory classification results. This set of known patterns is called the training set. Another

set of known patterns which includes a typical selection of expected patterns may be used to verify performance; this is the test set. For a general pattern recognition problem, therefore, basic elements are a set of features, a set of classes, a training set of patterns, and a test set of patterns.

Pattern Vectors and Feature Space

Each feature can be considered a variable in n-dimensional space, where each feature is assigned to a dimension. If there are fewer than three features, this space, known as feature-space or pattern-space, can be illustrated graphically.

Each pattern appears as a point in pattern-space. When a pattern is described by more than one feature, the pattern is a multidimensional or vector quantity. If the features of n-dimensional pattern-space are designated as x_i, $i = 1, \ldots, n$, a pattern $\mathbf{x}$ is

$$\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \\ \cdot \\ \cdot \\ \cdot \\ x_n \\ 1 \end{bmatrix}$$

Here, the augmented "1" is included for compatibility with further developments involving decision functions. Pattern-space may be described by a vector of m pattern vectors (or matrix), $\mathbf{X}$, where

$$\mathbf{X} = \begin{bmatrix} \mathbf{x}_1' \\ \mathbf{x}_2' \\ \cdot \\ \cdot \\ \cdot \\ \mathbf{x}_m' \end{bmatrix} = \begin{bmatrix} x_{11} & x_{12} & \cdots & x_{1n} \\ x_{21} & x_{22} & \cdots & x_{2n} \\ & & & \\ & & & \\ x_{m1} & x_{m2} & \cdots & x_{mn} \end{bmatrix}$$

and the prime (′) after a vector indicates that it is transposed.

Pattern Recognition of Speech

The speech signal, which is a function of time, must be transformed so that it is a function of both time and frequency. At any interval in time, an analysis of the frequency components of the speech signal may be carried out using the Fourier transform for the analysis. The transform actually used is a modified version that can work on discrete data, such as a digitized speech signal. This modified form may be either the discrete Fourier transform (DFT) or the computationally more efficient fast Fourier transform (FFT). These transform a time-related signal, f(t), into a frequency-related function, g(f). To do this, however, the transform must use f(t) over all time. Since this is not possible, a time interval long enough to achieve a good approximation is adequate. Therefore, f(t) may be divided into regular intervals of time, and an FFT analysis done on f(t) within each interval. For speech, this interval is typically 10 ms long. Once the transforms are carried out, a 3-dimensional plot of the signal amplitudes as a function of frequency and time can be made (called a spectrogram).

If a frequency-amplitude cross-section for any time interval is plotted, amplitude peaks usually occur at several frequencies, known as formant frequencies. With their corresponding amplitudes, formant frequencies can be used as features of speech patterns. The first three formants are adequate for speech recognition.

Elemental speech sounds are known as phonemes. A phoneme is characterized by its formant frequencies and peak amplitudes, and also (more subtly) by the changes in these features as phonemes are produced in succession. A cross-section of pattern-space in the f_1-f_2 plane (where f_1 and f_2 are the first two formant frequencies) may reveal two successive phonemes, p_1 and p_2, which will appear as two different points in pattern-space. The transitional sound from one phoneme to another may take one of many trajectories in pattern-space to get from p_1 to p_2. On a spectrogram (with only the peak amplitudes shown), the transitions appear as shown in Fig 1.

Decision and Classification Techniques

Once features have been extracted from the physical pattern, the pattern vectors can be placed in pattern-space as points. For different classes of patterns, clusters of points would be expected, where each cluster represents a distinct class. The classifier serves to determine to which class a particular pattern belongs.

Decision Functions

One approach to designing a classifier is to find a function which separates two classes, or several functions which separate three or more classes. These functions are called decision functions. In this discussion, only linear decision functions are considered; however, extrapolation of these concepts to nonlinear functions is fairly straightforward. In two dimensions, these functions are lines, and may be written in the form

$$x_1 - mx_2 - b = 0 \text{ or } w_1x_1 + w_2x_2 + w_3 = 0$$

where m = slope of line, b = x_1 intercept, $w_1 = 1$, $w_2 = -m$, and $w_3 = -b$.

In the n-dimensional case, the decision functions are hyperplanes of the form

$$w_1 x_1 + w_2 x_2 + \ldots + w_n x_n + w_{n+1} = 0$$

Thus, this equation may be written in vector form as: $\mathbf{w} \cdot \mathbf{x} = 0$ where

$$\mathbf{w} = \begin{bmatrix} w_1 \\ w_2 \\ \cdot \\ \cdot \\ \cdot \\ w_{n+1} \end{bmatrix} \text{ and } \mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \\ \cdot \\ \cdot \\ \cdot \\ x_n \\ 1 \end{bmatrix}$$

To illustrate the operation of a decision function in two dimensions, consider the case of two patterns.

$$\mathbf{x}_1 = \begin{bmatrix} 1 \\ 4 \end{bmatrix} \text{ and } \mathbf{x}_2 = \begin{bmatrix} 4 \\ 2 \end{bmatrix}$$

with the decision function $d(\mathbf{x}) = 0$ separating them (Fig 2), where

$$d(\mathbf{x}) = x_1 - \tfrac{1}{2}x_2 - 2 = 0$$

or, in vector form

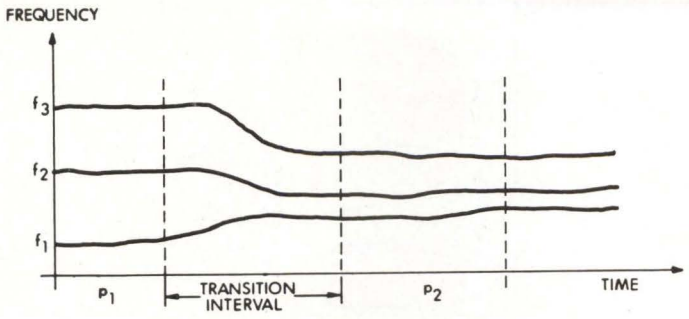

Fig 1 Trajectories of transitional sound. Transition intervals between elemental speech sounds, such as p_1 and p_2 characterized by the lowest resonant frequencies (formants) f_1 to f_3, contain significant information for classifying an utterance

$$d(\mathbf{x}) = \mathbf{w} \cdot \mathbf{x} = [1, -\tfrac{1}{2}, -2] \begin{bmatrix} x_1 \\ x_2 \\ 1 \end{bmatrix} = 0$$

If $\mathbf{x}_1$ is substituted into $d(\mathbf{x}) = \mathbf{w} \cdot \mathbf{x}$, then

$$d(\mathbf{x}_1) = [1, -\tfrac{1}{2}, -2] \begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} = 1 - 2 - 2 = -3$$

and for $d(\mathbf{x}_2)$

$$d(\mathbf{x}_2) = [1, -\tfrac{1}{2}, -2] \begin{bmatrix} 4 \\ 2 \\ 1 \end{bmatrix} = 4 - 1 - 2 = +1$$

Note that $d(\mathbf{x}_1) < 0$ and $d(\mathbf{x}_2) > 0$. For any point above $d(\mathbf{x}) = 0$, $d(\mathbf{x})$ is positive, and negative for points below. Thus for the 2-class case, the polarity of the evaluated $d(\mathbf{x})$ determines to which class a given pattern belongs.

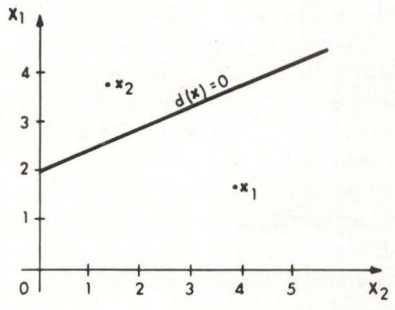

Fig 2 Decision function in 2-dimensions. Decision function $d(\mathbf{x}) = 0$ separates two patterns in 2-dimensional feature-space. For $\mathbf{x}_1$, $d(\mathbf{x}_1)$ will be positive; for $\mathbf{x}_2$, $d(\mathbf{x}_2)$ will be negative, thereby providing a means of discriminating between two classes of patterns linearly separable in feature-space

Multicategory Classifiers

With the 2-class problem the classifier needs only one decision-function. For multicategory classification, more than one decision function is required. Therefore, multicategory classifiers are needed to make a class identification of a pattern from the results of two or more decision functions.

A type I multicategory classifier considers a given class, say ω_i, as one class and all other classes, collectively, as a second class. Then a decision function is found which will separate these two classes. For n classes, n decision functions will result. For a given pattern belonging to class ω_i, only $d_i(\mathbf{x}) > 0$ and $d_j(\mathbf{x}) < 0$, for all $j \neq i$ [Fig 3(a)].

A type II classifier [Fig 3(b)] consists of pairwise separation which requires decision functions that separate two classes at a time. Separation of classes ω_i and ω_j requires a decision function $d_{ij}(\mathbf{x}) = 0$. Classification results if, for all classes, $d_{ij} > 0$; then, the pattern belongs to class ω_i.

The third type of multicategory classifier is a special case of the second type, modified so that any point in pattern-space is assigned to a given class. In the previous classifiers, any point within the triangle formed by the three lines would not be classified as belonging to any of the three classes shown. To eliminate this indeterminate region, the general decision function $d_{ij}(\mathbf{x}) = 0$ is made to be $d_i(\mathbf{x}) - d_j(\mathbf{x}) = 0$ where d_i and d_j are the decision functions of a type I classifier. For this scheme, the criterion for pattern assignment to class ω_i is that $d_i > d_j$ for all $j \neq i$. Notice that no indeterminate region exists for the type III classifier [Fig 3(c)].

A type I classifier has the largest amount of indeterminate space, being the center triangle and the three wedges radiating out from it. If classes can be separated with a type I classifier, the region of identification is more constrained, and therefore better identified, than with types II and III. In addition, if one class is of special interest it can be discriminated more easily. The type II classifier indeterminate space consists only of the center triangle. When classes of patterns are easiest to separate by class-to-class comparison, the type II classifier will probably be the easiest to design.

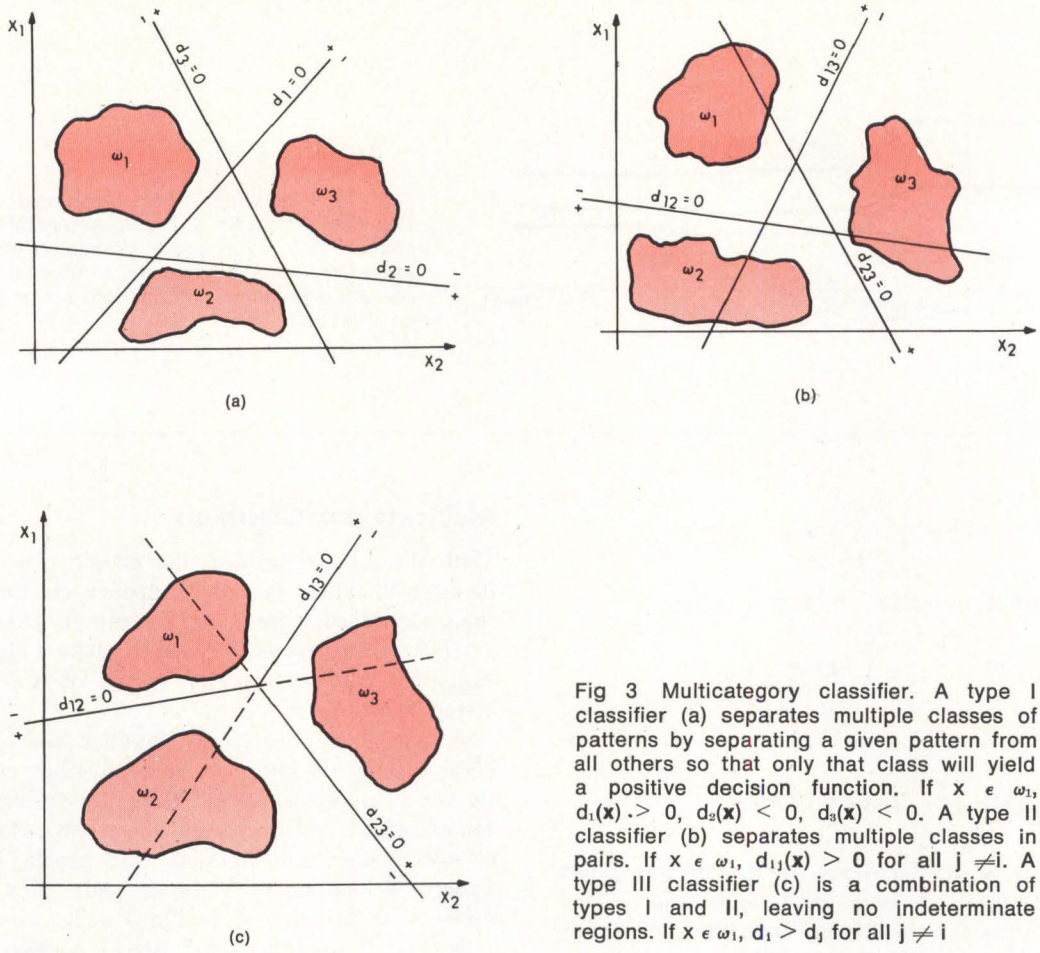

Fig 3 Multicategory classifier. A type I classifier (a) separates multiple classes of patterns by separating a given pattern from all others so that only that class will yield a positive decision function. If $x \in \omega_1$, $d_1(\mathbf{x}) > 0$, $d_2(\mathbf{x}) < 0$, $d_3(\mathbf{x}) < 0$. A type II classifier (b) separates multiple classes in pairs. If $x \in \omega_1$, $d_{1j}(\mathbf{x}) > 0$ for all $j \neq i$. A type III classifier (c) is a combination of types I and II, leaving no indeterminate regions. If $x \in \omega_1$, $d_i > d_j$ for all $j \neq i$

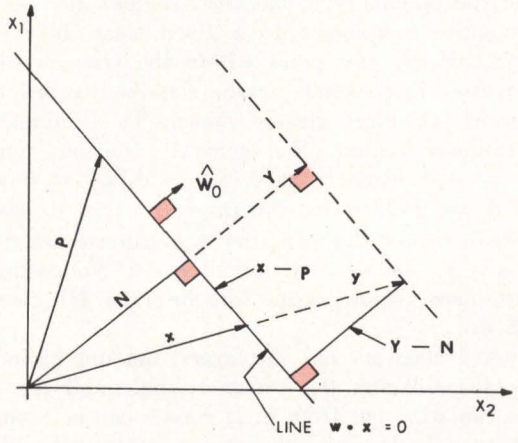

Fig 4 Hyperplane properties. A hyperplane in pattern-space is illustrated in plane x_1-x_2 with line $\mathbf{w} \cdot \mathbf{x} = 0$. Unit vector $\hat{\mathbf{w}}_0$ direction specifies orientation of the line, and is useful for determining distance between given point in space and line

Weight Vectors and Hyperplane Properties

In describing basic types of classifiers, it is assumed that the decision function coefficients $w_1, w_2, \ldots, w_{n+1}$ are already known. The primary goal in designing a pattern classifier is to find some method to determine these cofficients. Since the general form of a decision function is $\mathbf{w} \cdot \mathbf{x} = 0$, the goal is to find $\mathbf{w}$, the weight vector. The expression $\mathbf{w} \cdot \mathbf{x} = 0$ then describes a hyperplane in pattern-space. Before investigating methods for deriving $\mathbf{w}$, some properties of hyperplanes should be discussed.

Given the equation of a hyperplane, $\mathbf{w} \cdot \mathbf{x} = 0$, which can be expressed as

$$\mathbf{w}_0 \cdot \mathbf{x} + w_{n+1} = 0$$

where

$$\mathbf{w}_0 = \begin{bmatrix} w_1 \\ w_2 \\ \cdot \\ \cdot \\ \cdot \\ w_n \end{bmatrix}$$

If the dot product of two vectors is zero, they are perpendicular in direction, or $\mathbf{w} \cdot \mathbf{x} = 0 \Leftrightarrow \mathbf{w} \perp \mathbf{x}$. If $\mathbf{x}$

and $\mathbf{p}$ are points contained on $\mathbf{w}\cdot\mathbf{x} = 0$, $\mathbf{x} - \mathbf{p}$ is contained by the hyperplane. Consequently, if $\mathbf{w}$ is perpendicular (or normal) to the hyperplane, $\mathbf{w}\cdot(\mathbf{x} - \mathbf{p}) = 0$ or $\mathbf{w}\cdot\mathbf{x} = \mathbf{w}\cdot\mathbf{p}$. Writing out the dot products, and canceling w_{n+1} from both sides results in $\mathbf{w_0}\cdot\mathbf{x} = \mathbf{w_0}\cdot\mathbf{p}$ or $\mathbf{w_0}\cdot(\mathbf{x} - \mathbf{p}) = 0$. This result indicates that the vector $\mathbf{w_0}$ is normal to the hyperplane $\mathbf{w}\cdot\mathbf{x} = 0$ since $\mathbf{x} - \mathbf{p}$ lies on the hyperplane.

A vector with a magnitude of unity in the direction of $\mathbf{w_0}$ is

$$\hat{\mathbf{w}}_0 = \frac{\mathbf{w_0}}{||\mathbf{w_0}||}$$

where the $\wedge$ symbol indicates a unit vector and $||\mathbf{w_0}||$ is the magnitude (norm or length) of $\mathbf{w_0}$.

$$||\mathbf{w_0}|| = \sqrt{w_1^2 + w_2^2 = \ldots + w_n^2}$$

In two dimensions, these equations can be graphically presented as shown in Fig. 4. Note that the distance from the origin to the line is the length of $\mathbf{N}$, or $\mathbf{w_0}\cdot\mathbf{p}$. This is true for any point on the line since, for arbitrary point $\mathbf{x}$, $\mathbf{w_0}\cdot\mathbf{x} = \mathbf{w_0}\cdot\mathbf{p}$.

The distance to the line described by $\mathbf{w}\cdot\mathbf{x} = 0$ is

$$D(\text{line}) = |\mathbf{w_0}\cdot\mathbf{x}| = \left|\frac{-w_{n+1}}{||\mathbf{w_0}||}\right| = \left|\frac{w_{n+1}}{||\mathbf{w_0}||}\right|$$

For any point in general in hyperspace, $\mathbf{y}$, the distance from $\mathbf{w}\cdot\mathbf{x} = 0$ to $\mathbf{y}$ is the length of $\mathbf{Y} - \mathbf{N}$. Also, $||\mathbf{Y}|| = |\hat{\mathbf{w}}_0\cdot\mathbf{y}|$ (see Fig 4). Then,

$$||\mathbf{Y} - \mathbf{N}|| = |\mathbf{w_0}\cdot\mathbf{y} - \mathbf{w_0}\cdot\mathbf{x}|$$

This equation for the distance of a point to a line can be presented in a more useful form by rewriting $\hat{\mathbf{w}}_0\cdot\mathbf{x}$ as

$$\hat{\mathbf{w}}_0\cdot\mathbf{x} = \frac{\mathbf{w_0}\cdot\mathbf{x}}{||\mathbf{w_0}||} = \frac{\mathbf{w}\cdot\mathbf{x}}{||\mathbf{w_0}||} - \frac{w_{n+1}}{||\mathbf{w_0}||}$$

Since $\mathbf{w}\cdot\mathbf{x} = 0$,

$$\mathbf{w_0}\cdot\mathbf{x} = -\frac{w_{n+1}}{||\mathbf{w_0}||}$$

and

$$D(\text{point to line}) = \left|\frac{\mathbf{w_0}\cdot\mathbf{y} + w_{n+1}}{||\mathbf{w_0}||}\right| = \left|\frac{\mathbf{w_0}\cdot\mathbf{y} + w_{n+1}}{||\mathbf{w_0}||}\right|$$

Summarizing, vector $\hat{\mathbf{w}}_0$ is normal to the hyperplane $\mathbf{w}\cdot\mathbf{x} = 0$ and describes its orientation. The constant term in the equation for line, w_{n+1}, is related to the distance of the line from the origin. When $w_{n+1} = 0$, the line passes through the origin.

Minimum-Distance Classifiers

If two clusters of points in pattern-space are well separated, a decision function in the form of a hyperplane can be used to separate pattern-space into two regions that correspond to two classes. A technique can be developed for determining a decision function which will linearly separate the two clusters of points. First, points representing the typical values of each cluster must be determined. These points are known as prototypes or cluster-centers, since they are usually located at an average (or mean) distance from the points of the cluster they represent. The value of the prototype point may be found by averaging the points in a cluster of N points.

$$\mathbf{z} = \frac{1}{N}\sum_{i=1}^{N}\mathbf{x}_i$$

Next, some measure is needed of the similarity of a given pattern with the prototype. One similarity measure is the Euclidean distance of the point from each prototype point. Whichever prototype point is closest is considered to be the most similar and is assigned to the same class. This approach is known as minimum-distance classification. The distance of a given pattern, $\mathbf{x}$, from a cluster-center, $\mathbf{z}$, is the length of $\mathbf{x} - \mathbf{z}$ or $D = ||\mathbf{x} - \mathbf{z}||$. For two dimensions, this is

$$D^2 = (x_1 - z_1)^2 + (x_2 - z_2)^2$$
$$= x_1^2 - 2x_1z_1 + z_1^2 + x_2^2 - 2x_2z_2 + z_2^2$$

For multiple classes, the general form of the decision functions can be derived by considering that, for the ith class

$$D_i^2 = ||(\mathbf{x} - \mathbf{z}_i)||^2 = (\mathbf{x} - \mathbf{z}_i)\cdot(\mathbf{x} - \mathbf{z}_i)$$
$$= \mathbf{x}\cdot\mathbf{x} - 2\mathbf{x}\cdot\mathbf{z}_i + \mathbf{z}_i\cdot\mathbf{z}_i$$

Since $\mathbf{x}\cdot\mathbf{x}$ is the same for all classes, it can be eliminated. Multiplying by $(-\frac{1}{2})$, the general decision function is

$$d_i(\mathbf{x}) = \mathbf{x}\cdot\mathbf{z}_i - (\tfrac{1}{2})\mathbf{z}_i\cdot\mathbf{z}_i$$

Because D_i^2 was multiplied by a negative number to obtain $d_i(\mathbf{x})$, the largest decision function identifies the minimum distance and hence the class of $\mathbf{x}$. Since the general form of a decision function is $d(\mathbf{x}) = \mathbf{w}\cdot\mathbf{x} = 0$, the components of $\mathbf{w}$ can now be determined. They are

$$w_i = z_i \text{ for } i = 1, \ldots, n$$
$$w_{n+1} = -(\tfrac{1}{2})\mathbf{z}_i\cdot\mathbf{z}_i$$

The third type of classifier uses decision functions for each class derived from the prototype for that class. In this case, the decision boundary in two dimensions for two classes is a line which is the perpendicular bisector of the line joining the two cluster-centers. It fits the intuitive notion of the minimum-distance classifier concept by running midway between cluster-centers.

As an example, consider a 2-dimensional pattern-space containing the training set for the three classes shown below. Prototypes are found by taking the average of the individual vector components (with $\mathbf{x}$ and $\mathbf{z}$ not shown as augmented).

$$\omega_1 = \left\{\begin{bmatrix}1\\4\end{bmatrix}, \begin{bmatrix}2\\6\end{bmatrix}, \begin{bmatrix}3\\4\end{bmatrix}, \begin{bmatrix}2\\6\end{bmatrix}, \begin{bmatrix}2\\5\end{bmatrix}\right\} \mathbf{z}_1 = \begin{bmatrix}2\\5\end{bmatrix}$$

$$\omega_2 = \left\{\begin{bmatrix}2\\2\end{bmatrix}, \begin{bmatrix}1\\0\end{bmatrix}, \begin{bmatrix}0\\1\end{bmatrix}, \begin{bmatrix}1\\0\end{bmatrix}, \begin{bmatrix}1\\1\end{bmatrix}\right\} \mathbf{z}_2 = \begin{bmatrix}1\\1\end{bmatrix}$$

$$\omega_3 = \left\{\begin{bmatrix}4\\4\end{bmatrix}, \begin{bmatrix}4\\3\end{bmatrix}, \begin{bmatrix}5\\2\end{bmatrix}, \begin{bmatrix}3\\4\end{bmatrix}, \begin{bmatrix}4\\3\end{bmatrix}\right\} \mathbf{z}_3 = \begin{bmatrix}4\\3\end{bmatrix}$$

Then, for a type III classifier,

$d_1(\mathbf{x}) = \mathbf{w}_1\cdot\mathbf{x} = [2, 5, -14.5]\cdot\mathbf{x}$,

where $w_{13} = -(\tfrac{1}{2})(z_{11}^2 + z_{12}^2) = -(\tfrac{1}{2})(4 + 25) = -14.5$

$d_2(\mathbf{x}) = \mathbf{w}_2\cdot\mathbf{x} = [1, 1, -1.0]\cdot\mathbf{x}$,

where $w_{23} = -(\tfrac{1}{2})(1 + 1) = -1.0$

$d_3(\mathbf{x}) = \mathbf{w}_3\cdot\mathbf{x} = [4, 3, -12.5]\cdot\mathbf{x}$,

where $w_{33} = -(\tfrac{1}{2})(16 + 9) = -12.5$

To test this classifier, a point chosen near $\mathbf{z}$, such as

$$\begin{bmatrix} 1 \\ 4 \end{bmatrix}$$

should result in $d_1 > d_2, d_3$. Substituting,

$$d_1 \left(\begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} \right) = [2, 5, -14.5] \begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} = 2 + 20 - 14.5 = 7.5$$

$$d_2 \left(\begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} \right) = [1, 1, -1.0] \begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} = 1 + 4 - 1 = 4.0$$

$$d_3 \left(\begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} \right) = [4, 3, -12.5] \begin{bmatrix} 1 \\ 4 \\ 1 \end{bmatrix} = 4 + 12 - 12.5 = 3.5$$

Thus,

$$\mathbf{x} = \begin{bmatrix} 1 \\ 4 \end{bmatrix}$$

is closest to $\mathbf{z}_1$ and farthest from $\mathbf{z}_3$; therefore,

$$\begin{bmatrix} 1 \\ 4 \end{bmatrix} \epsilon\, \omega_1.$$

A geometric interpretation of the minimum-distance classifier is obtained by examining the terms of $d(\mathbf{x}) = \mathbf{x}\cdot\mathbf{z} - (1/2)\mathbf{z}\cdot\mathbf{z}$. The distance $|\mathbf{x}\cdot\mathbf{z}|$ is found graphically by projecting $\mathbf{x}$ onto $\mathbf{z}$. The length-squared of the segment along $\mathbf{z}$ to point 1 is $|\mathbf{x}\cdot\mathbf{z}|$. The second term has a length-squared of the segment along $\mathbf{z}$ to point 2, which is midway between $\mathbf{z}$ and the origin. The decision function is positive if point 1 is closer to $\mathbf{z}$ than to the origin. When decision functions are compared, the result is relative to the other cluster-center rather than to the origin.

Clustering Techniques

Techniques known as clustering algorithms can be used to classify patterns in an unsupervised manner. Among these are several algorithms that can be programmed and run on a small computer.

Threshold Algorithm

The threshold algorithm is conceptually simple. First, a cluster-center, $\mathbf{z}_1$ is established. An easy method of doing this is to use the first pattern vector, $\mathbf{x}_1$. Then, the next pattern is taken (arbitrarily) and its distance to $\mathbf{z}_1$ (and any other cluster-centers, as they appear) is computed. If this distance is less than a specified threshold value, T, it is assigned to that cluster. If not, the algorithm creates a new cluster-center using that pattern as the cluster-center. Fig 5 is a flowchart of this algorithm.

Several characteristics of the threshold algorithm deserve special attention. First, since the choices of $\mathbf{x}_1$ for the initial cluster-center greatly affect the classification, the algorithm is improved if approximate values for the cluster-centers are chosen as initial values. Second, the value of the distance threshold, T, affects the resolution of the clustering. If T is too large, several distinct clusters may be lumped together as a single cluster. Conversely, if T is too small, a cluster may be broken into several artificial clusters. To determine a value for T, consider what effect its value has on the number of clusters. A typical function is plotted in Fig 6(a).

Notice that between T_1 and T_2, N_c is relatively independent of T. This may be explained by considering the clusters in pattern-space [Fig 6(b)]. If clusters a and b are separated as shown, good classification will occur for $T_1 < T < T_2$, and T is usable in this range. If clusters a and b overlap, no interval of $N_c(T)$ will be flat, and a and b will not be linearly separable. In this case, statistical techniques for optimal classification are needed. Of course, if T is too large, the curve will be flat for $N_c = 1$, but this is a trivial condition.

Maximin-Distance Algorithm

To improve on the simple threshold algorithm, the maximum-minimum-distance or maximin-distance algorithm uses Euclidean distance measures in a similar fashion. It is shown as a flowchart in Fig 7.

An initial $\mathbf{z}_1$ is an arbitrarily chosen pattern, $\mathbf{x}$, and the point farthest from $\mathbf{x}$ is set equal to $\mathbf{z}_2$. A minimum-distance classifier, such as the one already discussed, is used to classify the remainder of the pattern points. Then, from each class, the pattern farthest from its assigned cluster-center is chosen, and the distance to its cluster-center is compared with the average distance between cluster-centers. If it is greater than this average distance, it is made a cluster-center. This is done for all classes, and if any new cluster-centers appear, the procedure is repeated until no changes in the number of cluster-centers occur.

Although the maximin-distance algorithm is an improvement over the threshold algorithm, its final classification of patterns is still dependent upon initial conditions. For a chosen $\mathbf{z}_1$, the farthest point from it may be a bad data point, as noise in the data will often lead to lone points far from any others. However, the algorithm chooses a threshold value automatically by using the average distance between cluster-centers.

To find the farthest point from $\mathbf{z}_1$, the distance to every other point must be computed. This may be time-consuming for a large data base. Also, choosing the farthest point may cause a distinct cluster to be combined with the nearest cluster since the average distance between cluster-centers will be large at first. Finally, this algorithm will not converge to a final solution for some distributions of patterns. If a point is located midway between two cluster-centers whose clusters contain an equal number of points distributed similarly around their respective cluster centers, the algorithm will not converge.

K-Means Algorithm

Examination of the pattern distribution may allow approximate choices of cluster-centers. The K-Means algorithm begins with such choices (even if they are arbitrarily chosen data points in pattern-space). Using a minimum-distance classifier as a similarity measure, the algorithm assigns the remaining points to one of the K cluster-centers, then computes a new cluster-center for each class by averaging the points for each cluster.

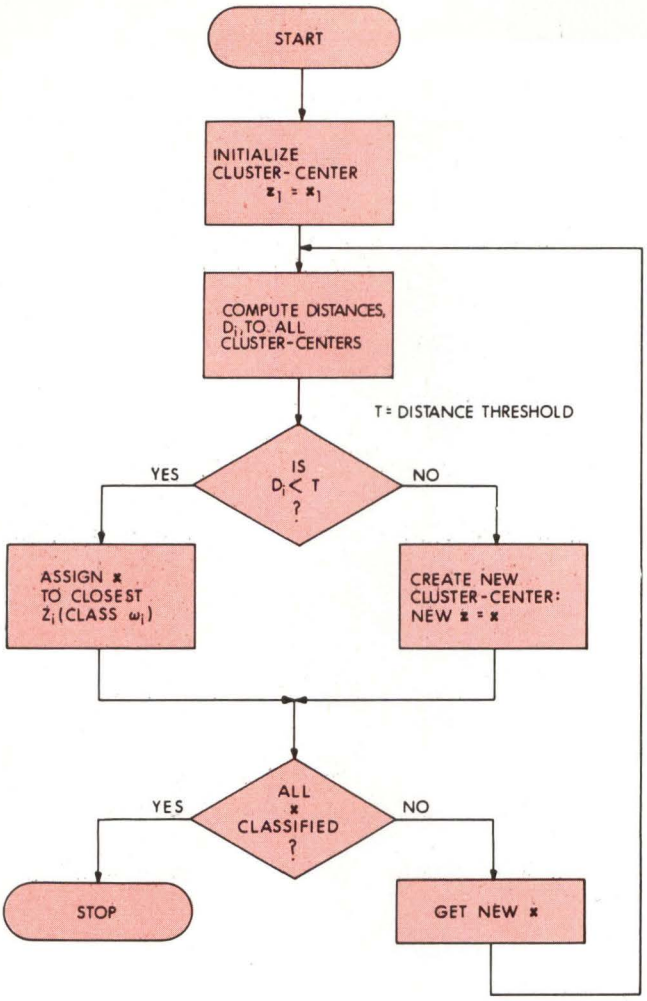

Fig 5 Threshold algorithm. This simple algorithm uses given distance threshold, T, as basis for determining class membership of pattern

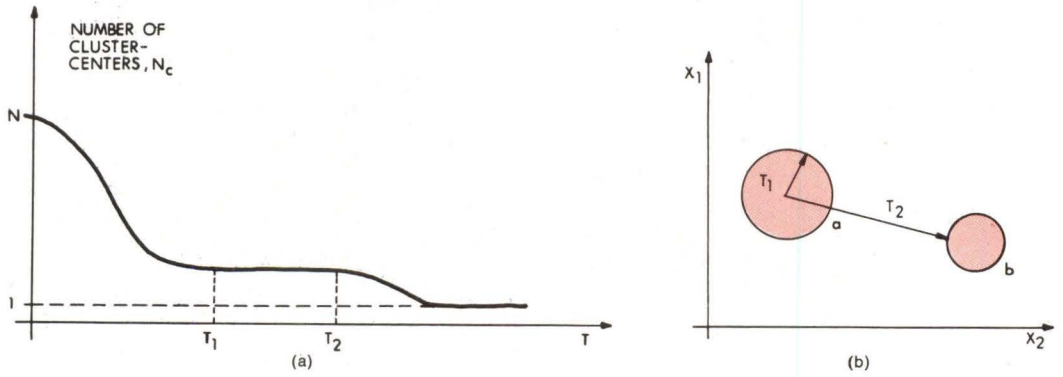

Fig 6 Number of clusters as function of threshold value. (a) When value of T is between T_1 and T_2, number of clusters, N_c, is independent of T. In this interval, T corresponds to length which sets threshold boundary in feature-space between clusters (b)

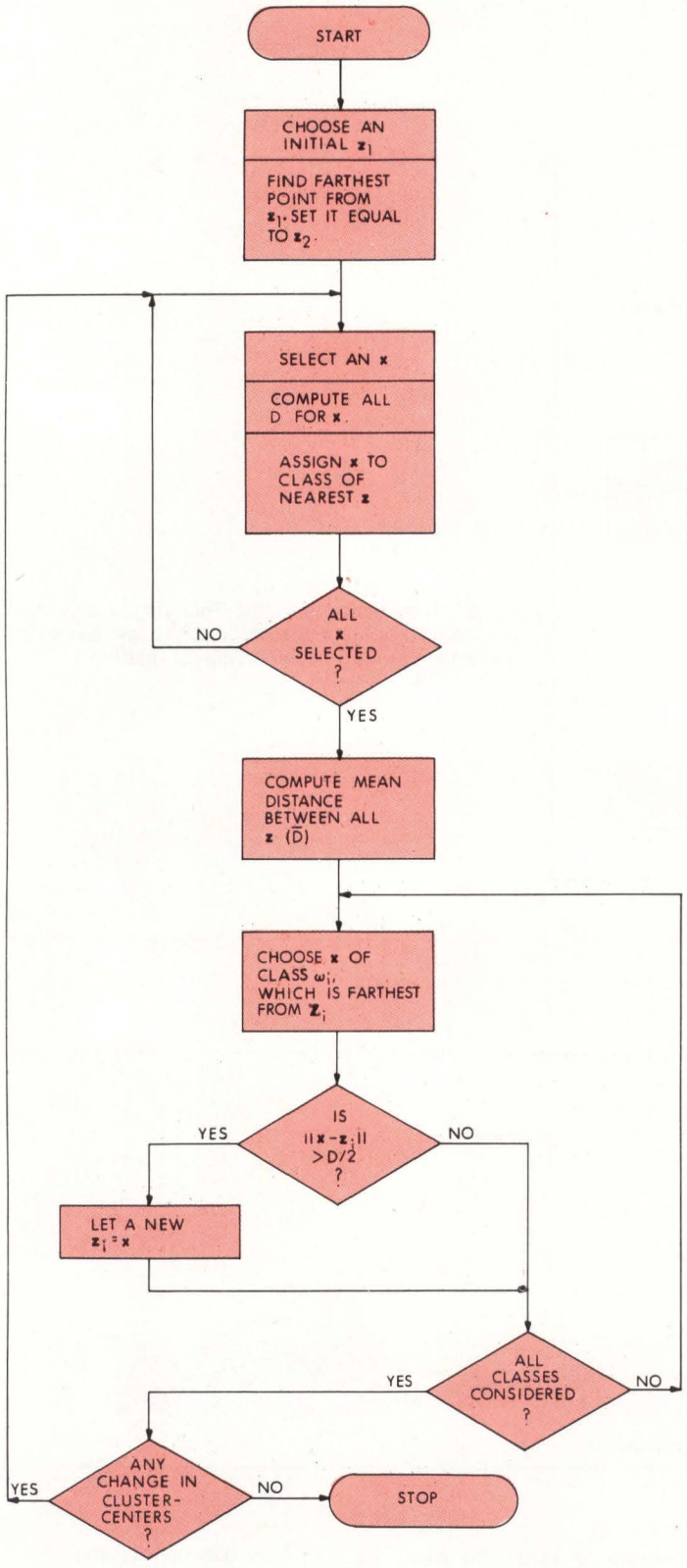

Fig 7 Maximin-distance algorithm. Similar to the threshold algorithm in approach, threshold value is not fixed but is calculated from mean value of cluster-centers

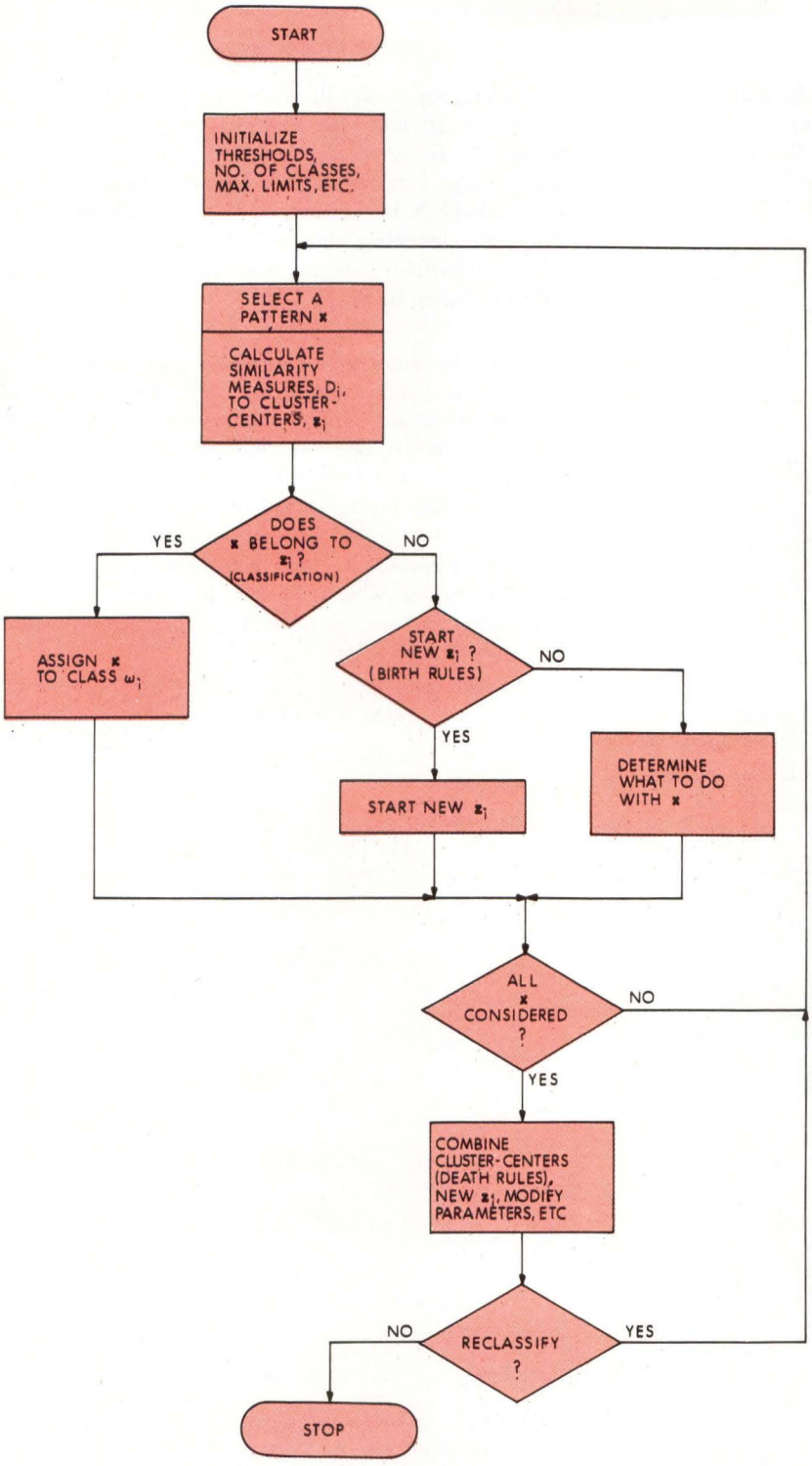

Fig 8 General clustering algorithm. In general, some criteria of similarity of patterns are needed for class assignment. Also needed are procedures for creating (birth rules) and eliminating (death rules) cluster-centers. Finally, means of determining termination conditions is used to end algorithm

Classification is repeated, assigning all points to the new clusters. When the assignments do not change from the previous iteration, the algorithm has converged. This algorithm is affected by K, the number of cluster-centers to start with, as well as their values.

General Cluster-Seeking Algorithm

The problem of designing a completely general clustering algorithm has not been solved. However, there is a general technique for the development of specific algorithms (see Fig 8). At times it may be desirable to

lump two or more clusters into a single cluster. This requires some set of rules (death rules) to determine when this should be done. Similarly, the creation of new cluster-centers requires a set of rules, as in the threshold and maximin algorithms (birth rules).

Learning Techniques

Cluster-seeking algorithms that have been developed are unsupervised algorithms, since the classes of a given set of patterns are determined by the algorithm. It is possible, however, for an algorithm to be trained to recognize the proper class for a given pattern using a reward-punishment concept. Once the algorithm has been trained to properly classify patterns of a known class membership (the training set of patterns), it can be used on unknown ones.

Perceptron Algorithm

For a training set of N patterns which belongs to one of two known classes, ω_1 and ω_2, the weight vector $\mathbf{w}$ for N decision functions must be determined. For patterns $\mathbf{x}_{1i}$ belonging to ω_1, decision functions are of the form $\mathbf{x}_{1i} \cdot \mathbf{w} > 0$ and for patterns $\mathbf{x}_{2i}$ belonging to ω_2, $\mathbf{x}_{2i} \cdot \mathbf{w} < 0$ or $-\mathbf{x}_{2i} \cdot \mathbf{w} > 0$. The set of patterns $\{\mathbf{x}_{1i}, -\mathbf{x}_{2i}, i = 1, \ldots, N\}$ can be written in matrix form where $\mathbf{X}$ is the matrix of training sample patterns. Then, the learning algorithm's goal is to find a weight vector, $\mathbf{w}$, which satisfies $\mathbf{Xw} > 0$. This perceptron algorithm is shown in Fig 9.

When the algorithm chooses a pattern and calculates its decision function, if $d(\mathbf{x}) > 0$, the weight vector is satisfactory at least for that pattern and is not changed—the next pattern is tried. When $d(\mathbf{x}) < 0$, the weight vector must be adjusted so that the decision function will come out positive. The pattern vectors of class ω_2 have been multiplied by -1 so that all decision functions must come out positive to be correct. This is done by replacing $\mathbf{w}$ with $\mathbf{w} + c \cdot \mathbf{x}$, where c is a positive correction increment. Therefore, on the kth iteration, the new value of $\mathbf{w}$ is

$$\mathbf{w}(k+1) = \begin{cases} \mathbf{w}(k) \text{ if } \mathbf{w}(k) \cdot \mathbf{x} > 0 \\ \mathbf{w}(k) + c\mathbf{x} \text{ if } \mathbf{w}(k) \cdot \mathbf{x} \leq 0 \end{cases}$$

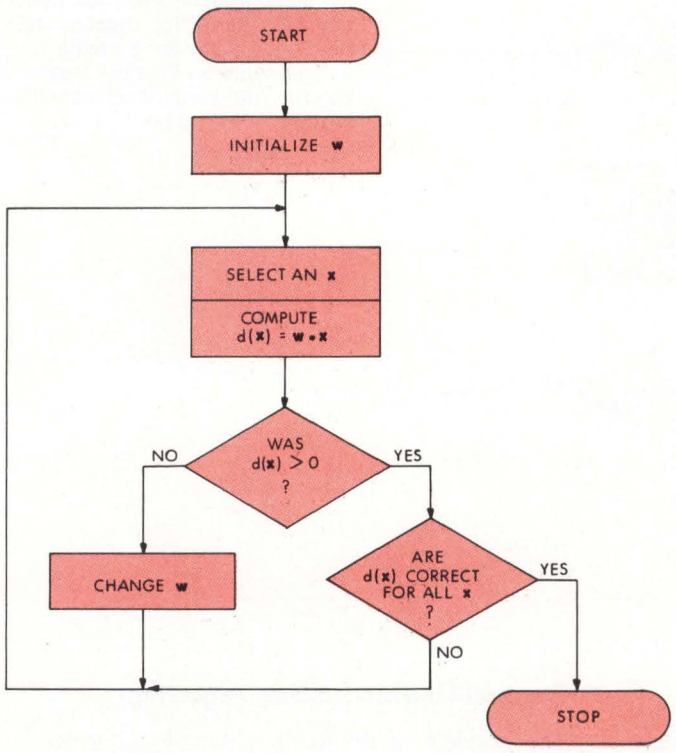

Fig 9 Perceptron algorithm. This 2-class learning algorithm modifies weight vector of decision function d(**x**) in search of a **w** which allows for correct classification of all known patterns. Only linearly separable clusters can be classified

On the next iteration, $\mathbf{w}$ will be closer to the correct value, even if $d(\mathbf{x}) \leq 0$, since $d(\mathbf{x})$ is now

$$d(\mathbf{x}) = \mathbf{w}(k+1)\cdot\mathbf{x} = (\mathbf{w}(k) + c\mathbf{x})\cdot\mathbf{x} = \mathbf{w}(k)\cdot\mathbf{x} + c\mathbf{x}\cdot\mathbf{x}$$

This new $d(\mathbf{x})$ is greater than the previous $d(\mathbf{x})$, which is equal to the first term, $\mathbf{w}(k)\cdot\mathbf{x}$. Now $d(\mathbf{x})$ is greater than the previous $d(\mathbf{x})$ by the amount $c\mathbf{x}\cdot\mathbf{x}$. This second term must be positive since $c > 0$ and $\mathbf{x}\cdot\mathbf{x}$ must be positive. Therefore, it appears that the algorithm will converge.

To better understand how this algorithm works, consider the training set in 2-dimensional feature-space.

$$\omega_1 = \{\mathbf{x}_1, \mathbf{x}_2\} \text{ where } \mathbf{x}_1 = \begin{bmatrix} 3 \\ 1 \end{bmatrix} \quad \mathbf{x}_2 = \begin{bmatrix} 1 \\ 2 \end{bmatrix}$$

$$\omega_2 = \{-\mathbf{x}_3, -\mathbf{x}_4\} \text{ where } \mathbf{x}_3 = \begin{bmatrix} -2 \\ -4 \end{bmatrix} \quad \mathbf{x}_4 = \begin{bmatrix} -4 \\ -3 \end{bmatrix}$$

Letting $c = 1$ and $\mathbf{w}(0) = 0$, the algorithm proceeds as follows:

$$d(\mathbf{x}_1) = \mathbf{w}\cdot\mathbf{x}_1 = [0, 0, 0] \cdot \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix} = 0$$

Since $d(\mathbf{x}_1)$ is not greater than 0, $\mathbf{w}$ must be modified.

$$\mathbf{w}(1) = \mathbf{w}(0) + 1 \cdot \mathbf{x}_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix}$$

Next

$$d(\mathbf{x}_2) = \mathbf{w}\cdot\mathbf{x}_2 = [3, 1, 1] \begin{bmatrix} 1 \\ 2 \\ 1 \end{bmatrix} = 6$$

Since

$$d(\mathbf{x}_2) > 0, \mathbf{w}(2) = \mathbf{w}(1) = \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix}$$

The procedure continues as shown in Fig 10. All $d(\mathbf{x})$ are correct when the procedure terminates with

$$\mathbf{w} = \begin{bmatrix} 2 \\ -1 \\ 6 \end{bmatrix}$$

Why does the perceptron algorithm work? Instead of developing a proof of its convergence (for linearly separable classes), an intuitive approach is used. First, it is already known from the hyperplane properties previously developed that $\mathbf{w}$ is perpendicular to the de-

ITERATION	CLASS	w	x	d(x)	MODIFY w
1	1	(0,0,0)	(3,1,1)	0	YES
2	1	(3,1,1)	(1,2,1)	6	NO
3	2	(3,1,1)	(-2,-4,1)	-9	YES
4	2	(1,-3,2)	(-4,-3,1)	7	NO
5	1	(1,-3,2)	(3,1,1)	2	NO
6	1	(1,-3,2)	(1,2,1)	-3	YES
7	2	(2,-1,3)	(-2,-4,1)	3	NO
8	2	(2,-1,3)	(-4,-3,1)	-2	YES
9	1	(-2,-4,4)	(3,1,1)	-6	YES
10	1	(1,-3,5)	(1,2,1)	0	YES
11	2	(2,-1,6)	(-2,-4,1)	6	NO
12	2	(2,-1,6)	(-4,-3,1)	1	NO
13	1	(2,-1,6)	(3,1,1)	11	NO
14	1	(2,-1,6)	(1,2,1)	6	NO

Fig 10 Example of perceptron algorithm in tabular form. Each of two patterns of classes one and two are used to determine $d(\mathbf{x})$ with $\mathbf{w}$. If $d(\mathbf{x}) < 0$, $\mathbf{w}$ is modified by adding $\mathbf{x}$ to it

cision surface described by the decision function $d(\mathbf{x}) = \mathbf{w}\cdot\mathbf{x} = 0$. For a particular pattern $\mathbf{x}_1$, $\mathbf{w}\cdot\mathbf{x}_1 > 0$ if $\mathbf{w}$ and $\mathbf{x}_1$ lie in the same general direction so that the angle between them, θ, is less than 90 degrees. Another expression of the dot product of two vectors, $\mathbf{a}$ and $\mathbf{b}$ is

$$\mathbf{a}\cdot\mathbf{b} = ||\mathbf{a}|| \cdot ||\mathbf{b}|| \cdot \cos\theta$$

Since magnitudes of vectors are always non-negative, the dot product is such that the following cases can occur.

Sign of Dot Product	Angle Between Vectors
Positive	<90 degrees
Zero	=90 degrees
Negative	>90 degrees

For the perceptron algorithm, a $\mathbf{w}$ must be found which points in the same general direction as the pattern vectors. Then, adding a vector $\mathbf{x}$ to $\mathbf{w}$ causes $\mathbf{w}$ to point more in the direction of $\mathbf{x}$. This is why $\mathbf{w}\cdot\mathbf{x}$ always improves after $\mathbf{w}$ is modified. In adding the patterns $\mathbf{x}_i$ to $\mathbf{w}$, the effect on $\mathbf{w}$ is to cause it to tend toward the mean of $\mathbf{x}_i$ since the mean is

$$\mathbf{m} = \frac{1}{N}\sum_{i=1}^{N}\mathbf{x}_i$$

As the algorithm proceeds, the value of $\mathbf{w}$ approaches $\mathbf{m}$. This is similar to the minimum-distance classifiers already discussed. However, the method of arriving at the result illustrates a primitive form of learning since $\mathbf{w}$ iterates toward the correct value, and is corrected when wrong.

Absolute Increment Correction

In the perceptron example, c is arbitrarily chosen to be 1, a fixed increment. However, the algorithm would converge faster if c were made just large enough to have the correct classification occur after weight adjustment (using the same pattern, of course). This value can be found by choosing c so that $\mathbf{w}(k+1)\cdot\mathbf{x} > 0$ or $[\mathbf{w}(k) + c\mathbf{x}] \cdot \mathbf{x} > 0$. Then $\mathbf{w}(k)\cdot\mathbf{x} + c\cdot\mathbf{x}\cdot\mathbf{x} > 0$, and $c > -\mathbf{w}(k)\cdot\mathbf{x}/\mathbf{x}\cdot\mathbf{x}$. Since $\mathbf{x}\cdot\mathbf{x} > 0$ and $\mathbf{w}(k)\cdot\mathbf{x} \leq 0$ (having been wrongly classified), then $-\mathbf{w}(k)\cdot\mathbf{x} \geq 0$ and $c > 0$. Therefore, the equation for c could also be written

$$c = \frac{\mathbf{w}(k)\cdot\mathbf{x}}{\mathbf{x}\cdot\mathbf{x}} = \frac{\mathbf{w}(k)\cdot\mathbf{x}}{||\mathbf{x}||^2}$$

This value of c is used in the absolute-correction perceptron algorithm.

Multicategory Perceptron Algorithm

For three or more classes, three types of classifiers have been discussed. The perceptron algorithm could employ the first type of classifier (one-of-N) by using N decision functions for N classes, where each decision function discriminates between the given class ω_i and all other classes considered together as ω_j. The N weight vectors could converge toward a solution of each decision function as it was exposed to the class it identified versus the patterns of the other classes. Similarly, for a type II classifier (pairwise) the number of decision functions needed is N taken two at a time or

$$\frac{N(N-1)}{2}$$

In this case, the perceptron algorithm trains individual decision functions by presenting patterns of two classes and adjusting the weight vector accordingly. For the third type of classification, the largest decision function determines the class; or, if $\mathbf{x} \in \omega_i$, $d_i(\mathbf{x}) > d_j(\mathbf{x})$ for all $j \neq i$.

Using the type III classifier, a more general form of the perceptron algorithm can be developed. On the kth iteration, if pattern $\mathbf{x} \in \omega_i$, the N decision functions are tested with $\mathbf{x}$. If $d_i(\mathbf{x}) > d_j(\mathbf{x})$ for all $j \neq i$, the weight vectors are not adjusted, or $\mathbf{w}(k+1) = \mathbf{w}(k)$. However, if for some m, $d_i(\mathbf{x}) \leq d_m(\mathbf{x})$, the weight vector of $d_i(\mathbf{x})$ is increased. The weight vector of $d_m(\mathbf{x})$ is decreased, and the other weight vectors are unaffected.

Summary

Classification of complex information by computer algorithms requires the selection of decision functions which will allow separation of patterns of signals into classes. These classes may be predetermined and represented by linear classifiers based on chosen decision functions or specified by the recognizer itself, as with clustering techniques. In addition to clustering, a different approach to unsupervised classification is to use learning algorithms such as the perceptron. All of the approaches to pattern recognition presented here require well-separated clusters of classes in feature-space since the decision functions are linear and no statistical properties of the patterns, which are necessary for overlapping clusters, have been considered. The ease with which these algorithms may be modified and optimized as computer software makes them particularly attractive when compared with fixed hardware designs.

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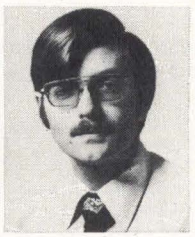

Dennis Feucht received a BSEE degree in computer science from Oregon State University. As an instrument design engineer at Tektronix he is presently involved in oscilloscope design; his previous design experience includes pulse and function generators and microcomputer systems.

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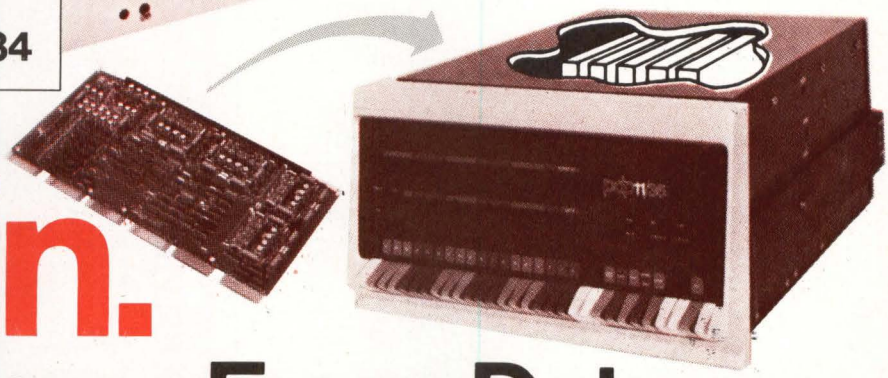

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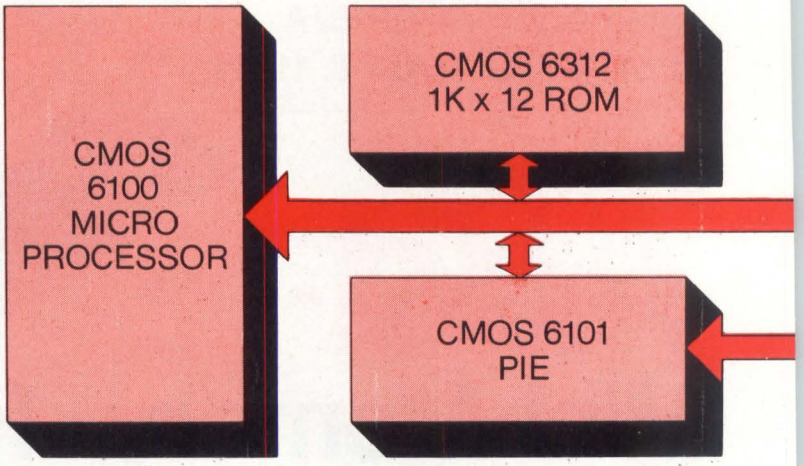

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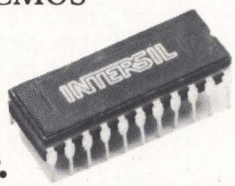

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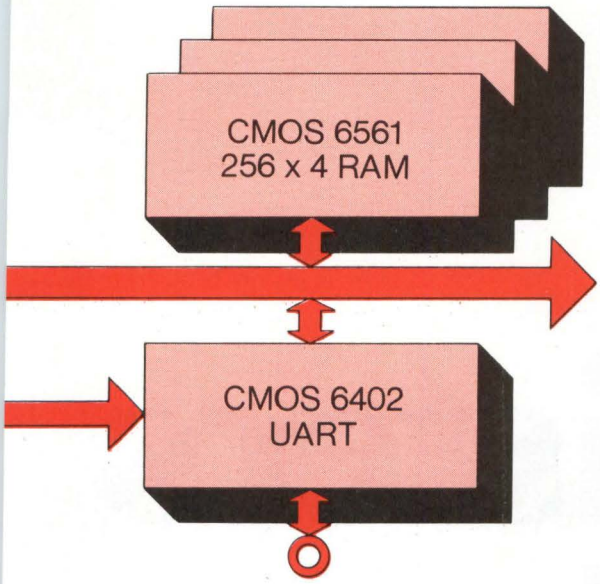

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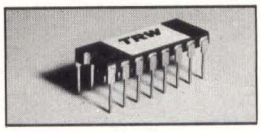
The biggest, fastest little  shift registers you can buy.

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Multiple-Word Buffering for Disc Controllers With Bipolar FIFO Memory

Krishna Rallapalli*

Bipolar Memory/LSI Division
Fairchild Camera and Instrument Corporation
Mountain View, California

When a disc is interfaced with a computer, a multiple-word buffer memory usually is needed in the disc controller since data bits arrive continuously in a serial stream from the disc. Data bits are first assembled into words in a serial-to-parallel converter and then are loaded into the buffer. Next, a request is made to the computer for direct memory access. However, no computer can respond instantaneously to a direct memory access request and simultaneously grant access to the memory. The delay from the time of request to the access grant is known as direct memory access latency and usually lasts a few microseconds.

Since the disc is a synchronous device, data bits continue to arrive while the disc controller is waiting for a grant to memory. If the controller does not have enough local buffering capacity, a data overrun condition will result, necessitating re-reading the whole sector from the disc. A similar situation exists while performing a write operation. Parallel data are obtained from memory using the direct memory access (DMA) facility, and a parallel-to-serial converter generates the serial bit stream to be written on the disc. Without sufficient local buffering, DMA latency will cause an overrun condition because another word will not be available as soon as the previous word is written.

In the past, disc drives had modest bit rates, and computer systems did not contain many DMA devices. Also, two to four words of local buffering were deemed satisfactory by designers. Buffers and associated serial-to-parallel and parallel-to-serial converters were implemented using medium-scale integration (MSI) devices. However, for today's increasing disc speeds and complex computer systems containing many DMA devices, 16 or more words of local buffering are required in the disc controllers. Such large buffers containing MSI devices are no longer attractive economically, especially since bipolar large-scale integration (LSI) is now more cost-effective.

A first-in first-out (FIFO) buffer memory is an LSI device that automatically stores words in the order they are entered at the input and makes them available at the output in exactly the same order. Moreover, data entry and data extraction from the FIFO buffer can be asynchronous. Because these two properties are precisely what a buffer memory in a disc controller needs, FIFO devices are ideal candidates for this application.

Two industry-compatible bipolar FIFO memory devices to be discussed are a 16-word by 4-bit low power Schottky device (9403), and a 64-word by 4-bit isoplanar integrated injection logic (I^3L)™ device (9423). Except for storage capacity, both devices are identical

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in architecture, pin configuration, and packaging. Also, data can be entered in serial or parallel format and can be extracted in either serial or parallel mode for both devices. Of greatest importance, serial-to-parallel and parallel-to-serial conversions and buffer memory functions are combined into a single LSI device.

FIFO Buffer Operation

As shown in Fig 1, the FIFO buffer contains a 4-bit input register with serial and parallel data inputs, and control inputs and outputs for handshaking and input expansion. The fall-through stack is N − 2, 4-bit words deep with self-contained control logic, where N equals 16 for the 9403, and N equals 64 for the 9423. Thus, the stack is 14 or 62 words deep, respectively. The fall-through stack physically consists of rows of flip-flops (four per row). If data are loaded into the first row of flip-flops and the second row contains no data, the stack control logic transfers data from the first row to the second. If the third row is empty, data will fall from the second row into the third, and so on. Also, the device has a 4-bit output register with serial and parallel data outputs, and control inputs and outputs for handshaking and output expansion.

Parallel data are entered into the input register using data inputs D_0 through D_3, and the parallel load (PL) input as the clock pulse. A high level on the PL input operates the direct set and clear inputs of the input register flip-flops. The quiescent state of the PL input is low. Serial data are entered using D_s as data input and the serial input clock ($\overline{\text{CPSI}}$) as clock input. Data entry occurs on the high-to-low transition of $\overline{\text{CPSI}}$; the quiescent state of the clock is low. For $\overline{\text{CPSI}}$ to effect shifting, the serial input enable ($\overline{\text{IES}}$) input must be low. The decision to assign individual pins for the $\overline{\text{CPSI}}$, PL, and D_s inputs was deliberate, since the chances of entering data in both serial and parallel formats at the same time are rare. Hence, the use of one parallel data input pin for serial data entry is possible. However, in disc controllers, parallel data come from the computer data bus and serial data come from the disc read electronics. If the same pin were used for both types of data, an external multiplexer would be required to feed into the FIFO buffer. Assigning individual pins eliminates this requirement.

Whenever the input register receives four data bits (by serial or parallel entry), the status flag, input register full ($\overline{\text{IRF}}$), output goes low. If the transfer-to-stack ($\overline{\text{TTS}}$) input is activated with a low pulse, data

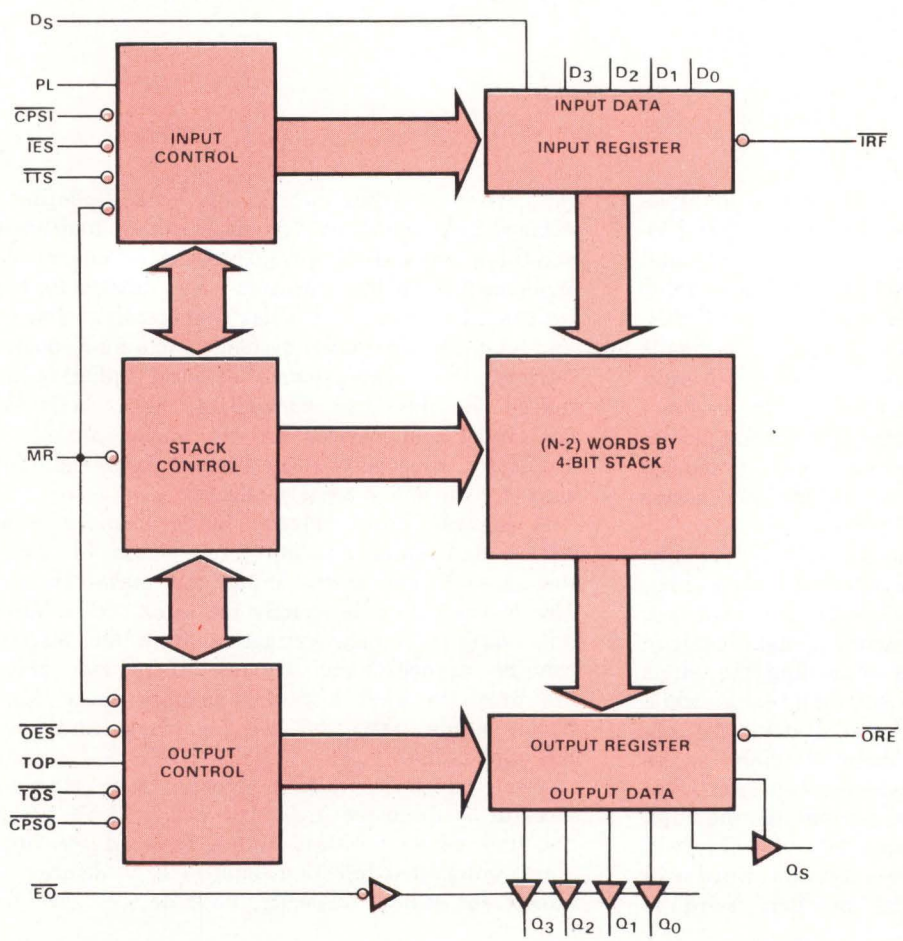

Fig 1 Block diagram of FIFO buffer memory. Data can be loaded in either serial or parallel format into input register, and then transferred into fall-through stack by activating appropriate control inputs. Stack control keeps track of words automatically and delivers them to output register. Data from output register are available in either serial or parallel format

from the input register are transferred into the first stack location, provided this location is empty. As soon as data are transferred, control logic attempts to initialize the input register so that it can accept another word. However, initialization is postponed until the PL input is low. The device is designed so that $\overline{IRF}$ can be connected to the $\overline{TTS}$ input. With such a connection, when a data word is received by the input register, the word automatically enters the stack and falls through toward the output, pausing on the way as needed for an "empty" location. Initialization of the input register causes the $\overline{IRF}$ output to go high. A high on $\overline{IRF}$ shows that data may be loaded into the input register.

Normally, output register empty ($\overline{ORE}$) is low, indicating that the output register does not contain valid data. As soon as a data word arrives in the output register, $\overline{ORE}$ goes high to indicate the presence of valid data. If the output enable ($\overline{EO}$) input is low, the 3-state buffers at the output are enabled, and data are available on the Q_0 through Q_3 outputs. If the $\overline{EO}$ input is high, the 3-state buffers are disabled and, hence, the outputs will be in a high impedance state.

Data can be extracted from the output register either serially or in parallel. The Q_s output is used for serial data output, and $\overline{CPSO}$ for the associated clock input. The Q_s output is also driven by a 3-state buffer; however, its enabling is controlled internally. The output register is shifted on the high-to-low transition of the normally low $\overline{CPSO}$ input. As soon as the last data bit is shifted out, $\overline{ORE}$ goes low, designating an empty output register.

The quiescent state of the $\overline{TOS}$ input is low. A high-to-low transition on this input allows new data to be loaded from the stack into the output register. If data are waiting in the last stack location, they appear in the output register after the high-to-low transition of the $\overline{TOS}$. If the last stack location is empty at the transition, any data that arrive into the last stack location automatically fall into the output register. The $\overline{ORE}$ output can be connected to the $\overline{TOS}$ input so that as soon as the last data bit is shifted out, other data are automatically demanded from the stack.

For the TOP input, the quiescent state is high. A low-to-high transition on this input allows data to be loaded into the output register. Moreover, a low level on the TOP input causes the $\overline{ORE}$ output to go low. TOP and $\overline{EO}$ inputs can be connected together so that data are made available at the Q_0 through Q_3 outputs when $\overline{EO}$ is low. When $\overline{EO}$ goes high to disable the Q_0 through Q_3 outputs, data are automatically demanded from the stack. Note that $\overline{TOS}$ does not affect $\overline{ORE}$.

In summary, $\overline{TOS}$ is used for automatically demanding data in the serial mode of operation and TOP is used for demanding data in the parallel mode. Also note that serial and parallel data outputs are assigned to independent pins. It would have been possible to share one of the parallel data output pins for serial data. However, in a disc controller, parallel data from the FIFO buffer are connected to the computer data bus, and serial data output from the FIFO buffer is connected to the write electronics of the disc. If a common output pin were used, a demultiplexer would be needed to separate the serial data. Assigning separate pins eliminates this requirement. The output enable serial ($\overline{OES}$) signal is used for serial expansion.

The FIFO buffer is cleared by a low on the master reset ($\overline{MR}$) input. This level causes the flag outputs $\overline{IRF}$ and $\overline{ORE}$ to indicate an empty condition; ie, $\overline{IRF}$ is high and $\overline{ORE}$ is low. The $\overline{MR}$ input does not clear data flip-flops in the stack or output register; it only initializes the control section. Thus, the Q_0 through Q_3 outputs are not affected by the $\overline{MR}$ input.

Expansion Capability

FIFO buffer organization has been designed so that LSI devices can be arrayed. Expanding vertically results in increased word storage; horizontally results in longer word lengths (in multiples of four bits). To illustrate the expansion connections, a FIFO buffer array consisting of eight devices is shown in Fig 2. If m 9403 devices are used in a row with n such rows in the array, 15n + 1 words of storage with 4m bits in each word are obtained. If 9423 devices are used instead of 9403, the results are 63n + 1 words with 4m bits in each word.

The D_s inputs of the first four devices are connected together, and serial data from the disc are entered on this line. The $\overline{CPSI}$ inputs are also connected together, and this line is used for shifting data. The $\overline{IES}$ input of device 1 is grounded, while the $\overline{IES}$ inputs of devices 2, 3, and 4 are connected to the $\overline{IRF}$ outputs of devices 1, 2, and 3, respectively. The $\overline{TTS}$ inputs of all four devices in the first row are connected together and to the $\overline{IRF}$ output of device 4.

After initialization by a low on the $\overline{MR}$ input, the $\overline{IRF}$ outputs of all devices in Fig 2 go high. Under these conditions, only device 1 responds to $\overline{CPSI}$ because its $\overline{IES}$ input is low; the next four clock pulses shift four bits of data into the input register of device 1; its $\overline{IRF}$ output then goes low. Control logic in device 1 inhibits $\overline{CPSI}$ from affecting this device any further.

The $\overline{IES}$ input of device 2 is now low, and the clock shifts data into the input register of device 2. On the eighth clock pulse, the $\overline{IRF}$ output of device 2 goes low and prevents further shifting into device 2. This process continues with devices 3 and 4. Therefore, on the sixteenth clock pulse, the $\overline{IRF}$ output of device 4 goes low and activates the $\overline{TTS}$ inputs of all four devices in the first row. The stack control logic in each device responds by transferring data into the stacks from the respective input registers; the input registers then are initialized. Thus, the $\overline{IRF}$ outputs of all four devices become high once again. An automatic priority scheme assures that if the $\overline{IRF}$ output of device 4 is high, the input registers of all four devices have been initialized.

In Fig 3 the timing diagram illustrates the serial entry of 16 data bits. Any attempt to clock data when the $\overline{IRF}$ output of device 4 in Fig 2 is low can be designated as a data overrun condition.

Parallel entry into the array in Fig 2 is made with a high level pulse on the PL inputs. In disc controllers, parallel loading is used during write operations to the disc. The same conditions prevail (ie, $\overline{IRF}$ outputs of all four devices are low) in the input section

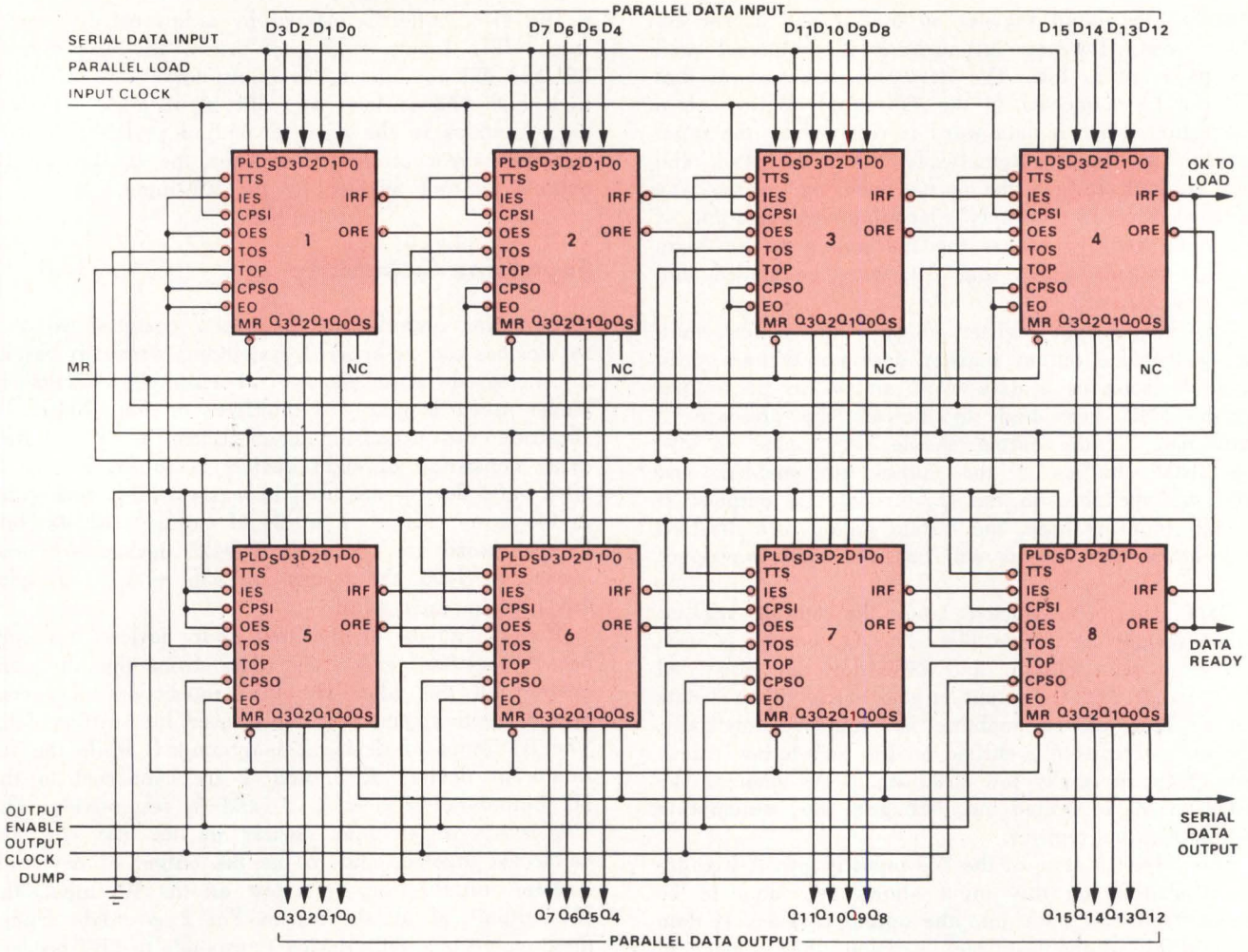

Fig 2 16-bit FIFO memory array consisting of eight devices (two rows of four devices each). FIFO devices can be expanded both horizontally and vertically without external logic. Data are entered into or extracted from array in either serial or parallel format

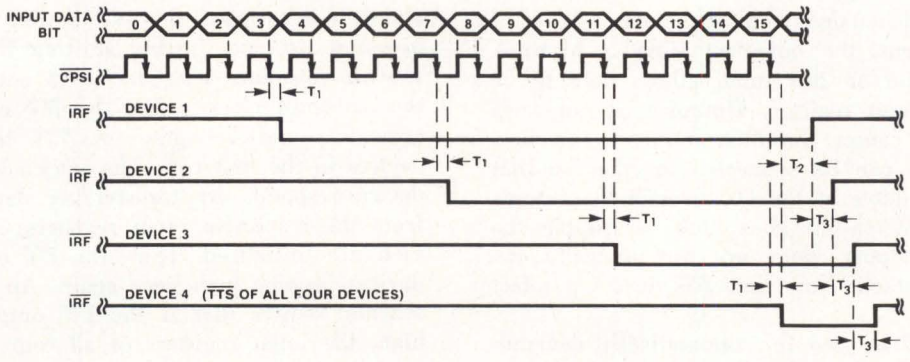

Fig 3 Timing diagram depicting 16-bit serial data entry into FIFO memory array. Clocking occurs on high to low transition of $\overline{CPSI}$ input. $\overline{IRF}$ output of each device goes low to indicate that its input register is full. $\overline{IRF}$ of device 4 activates $\overline{TTS}$ of all four devices to initiate fall-through. Automatic priority scheme is designed into devices so that high level on $\overline{IRF}$ of device 4 guarantees that input registers of all four devices are empty. T_1 is propagation delay from $\overline{CPSI}$ to $\overline{IRF}$ (typ 18 ns), T_2 is propagation delay from $\overline{TTS}$ to $\overline{IRF}$ (typ 48 ns), and T_3 is propagation delay from $\overline{IES}$ to $\overline{IRF}$ (typ 31 ns)

that exist after the sixteenth clock pulse in the serial entry mode. Because all $\overline{TTS}$ inputs of the first row of devices are activated, data are loaded into the stacks. Note that initialization of the input registers does not take place until the PL inputs are low. During a write operation, a DMA request can be generated whenever the $\overline{IRF}$ output of device 4 is high. Data loaded into the stacks arrive into the output registers of the first four devices. When the $\overline{MR}$ input was activated to initialize the array, the $\overline{ORE}$ outputs of the first row of devices are low, and the $\overline{IRF}$ outputs of the second row are high. As soon as data arrive into the output registers of the first row, the $\overline{ORE}$ outputs go high. An automatic priority scheme exists in the output section also. Thus, a high on the $\overline{ORE}$ output of device 4 guarantees that valid data are present in all four output registers of the first row.

The $\overline{ORE}$ output of device 4 is connected to the PL inputs of devices 5 through 8, as well as to the $\overline{TOS}$ inputs of the first row. Note that if serial extraction is not needed, the $\overline{TOS}$ inputs can be grounded. The $\overline{EO}$ inputs of the first row are also grounded; hence, data appear on the first row outputs. The high level on the $\overline{ORE}$ output of device 4 activates the PL inputs of the second row. Thus, input registers of the second row are loaded from output registers of the first row. The $\overline{IRF}$ outputs of the second row go low; the $\overline{IRF}$ output of device 8 is connected to the TOP inputs of the first row and to the $\overline{TTS}$ inputs of the second row. A low level on the TOP inputs of the first row causes their $\overline{ORE}$ outputs to go low. This makes the PL inputs of the second row low. Moreover, the low on the $\overline{IRF}$ output of device 8 activates the $\overline{TTS}$ inputs of the second row. Thus, data from the input registers of the second row go into their stacks. The stack controls in the second row initialize their input registers, and the $\overline{IRF}$ outputs go high. The automatic priority scheme mentioned earlier also is present at the inputs of devices 5 through 8. The high level from the $\overline{IRF}$ output of device 8 restores the TOP inputs of the first row to the quiescent high state.

If the stacks in the second row are full, activating the $\overline{TTS}$ input does not initiate a data transfer from the input registers. The $\overline{IRF}$ output of device 8 remains low until data are transferred into the stacks of the devices in the second row. Thus, as long as devices 5 through 8 are holding 16 words for 9403s (64 words for 9423s), the $\overline{IRF}$ output of device 8 remains low. This level also holds the TOP inputs of the first row low. As long as the TOP inputs are low, data cannot be loaded into the output registers by the stack control. Under these conditions, the first row of devices temporarily loses the ability to use its output registers for new data storage. As a result, the array of 9403s in Fig 2 has a storage capacity of 31 words instead of 32. For 9423 devices, the same array results in 127 words instead of 128.

Data loaded into the stacks eventually arrive at the output registers of devices 5 through 8, and the $\overline{ORE}$ outputs go high. Note that the automatic priority scheme is still in effect at the outputs, and a high level at the $\overline{ORE}$ output of device 8 guarantees availability of data. During a read operation from the disc, the $\overline{ORE}$ output of device 8 can be used to make a DMA request.

Available through 3-state buffers are the Q_S outputs of devices 5 through 8. These outputs are connected together to extract serial data for writing onto the disc. The $\overline{CPSO}$ inputs are connected together and driven by the write clock. When no valid data are present in the output register, the Q_S outputs are in the high impedance state.

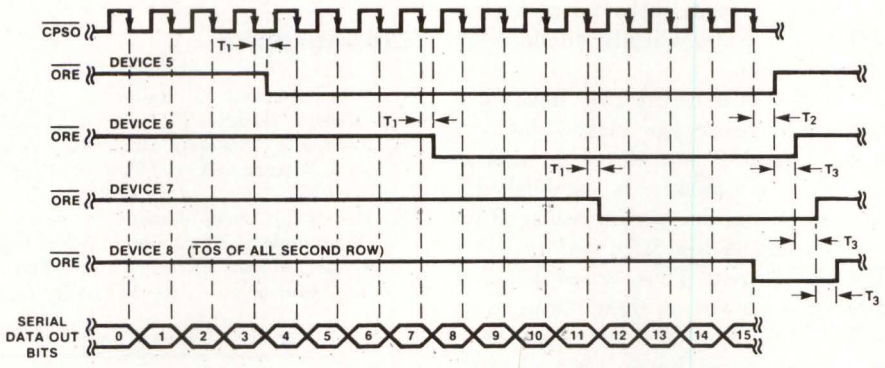

Fig 4 Timing diagram depicting 16-bit serial data extraction from FIFO memory array. After shifting out four bits of data, $\overline{ORE}$ output goes low, indicating that its output register is empty. $\overline{ORE}$ output of device 8 activates $\overline{TOS}$ signal of second row of devices to demand new data word from stack. Automatic priority scheme guarantees that when $\overline{ORE}$ output of device 8 is high, data have arrived into output register of all four devices. T_1 is propagation delay from $\overline{CPSO}$ to $\overline{ORE}$ (typ 32 ns), T_2 is propagation delay from $\overline{TOS}$ to $\overline{ORE}$ (typ 41 ns), and T_3 is propagation delay from $\overline{OES}$ to $\overline{ORE}$ (typ 26 ns)

The $\overline{OES}$ input of device 5 is grounded, while devices 6, 7, and 8 receive their $\overline{OES}$ inputs from the $\overline{ORE}$ output of the preceding device. As soon as data arrive into the output registers, the $\overline{ORE}$ outputs go high. The Q_s output of device 5 is enabled and contains information identical to that on the Q_0 output. The Q_s outputs of devices 6, 7, and 8 are disabled because their $\overline{OES}$ inputs are high. The $\overline{CPSO}$ clock shifts out the data bits in the same order as they are entered at the array input. After the fourth clock pulse, the $\overline{ORE}$ output of device 5 goes low and its Q_s output is disabled into the high impedance state.

The $\overline{ORE}$ output of device 5 inputs a low on the $\overline{OES}$ of device 6 to enable its Q_s output. Device 6 now begins shifting out its data, and the Q_s output is disabled when the device is emptied. Then, the $\overline{ORE}$ output of device 6 goes low and device 7 is enabled. The process continues until the last data bit has been shifted out and the $\overline{ORE}$ output of device 8 goes low. This activates the $\overline{TOS}$ inputs of the second row, and more data may be loaded into the output registers.

Illustrated in Fig 4 is the timing diagram for 16-bit data extraction. During a write operation, any attempt to shift data when the $\overline{ORE}$ output of device 8 is low will result in a data overrun condition. Data can be extracted from the array in parallel by making the TOP inputs of the second row devices low.

Automatic Priority Scheme

Most conventional FIFO buffer designs provide flag outputs analogous to the $\overline{IRF}$ and $\overline{ORE}$ outputs. However, when such devices are operated in arrays, unit-to-unit delay variations require external gating to avoid transient false indications. This technique is commonly referred to as composite status generation. The FIFO array described has been designed to avoid this situation. An automatic priority scheme is built in to assure that a slow device automatically dominates the array regardless of its location.

In Fig 2, devices 1 and 5 are called row masters, and devices 2, 3, and 4 are slaves to row master device 1. Similarly, devices 6, 7, and 8 are slaves to their row master, device 5. Row mastership is established by sensing the $\overline{IES}$ input during the period when $\overline{MR}$ is low. As described previously, a low $\overline{MR}$ input results in a high level at the $\overline{IRF}$ output. Thus, when $\overline{MR}$ is low, only the row masters have a low on their IES inputs (they are grounded). The $\overline{IES}$ inputs of slaves are high. This condition is sensed and stored by device logic to establish and retain row mastership.

All devices in any given row transfer data from their input registers into the stacks simultaneously. However, no slave can initialize its input register until its $\overline{IES}$ input goes high. Thus, initialization starts with the row master and eventually ends with the last slave in that row.

A similar situation occurs at the output registers of a row; data are loaded simultaneously from the stacks into the output registers of all devices in a row. Only the $\overline{ORE}$ output of the row master is allowed to go high. The $\overline{ORE}$ output of a slave cannot go high unless its $\overline{OES}$ input is high. Therefore, the row master is the first to indicate data arrival on its $\overline{ORE}$ output, and the last slave of that row is the last device to indicate data arrival. Although the automatic priority scheme allows arrays to be built with no external logic, this scheme is essentially based on a ripple effect, and maximum speed of the array operation is affected by the rippling. Design of the FIFO array is such that master-slave hierarchy can be easily replaced by traditional composite status logic to improve the array's operating speed; however, this would require some external logic.

Conclusions

FIFO buffers can be implemented using MSI elements such as counters and register files. However, such realizations require several integrated circuits even for modest word capacities of four or eight words. To use such a FIFO implementation as a local data buffer in a disc controller, serial-to-parallel and parallel-to-serial converter logic must be added. FIFO buffers first appeared as MOS/LSI devices several years ago, but were not accepted immediately for disc controller designs because of their speed limitations and serial-to-parallel and parallel-to-serial conversion logic overhead.

A low power Schottky FIFO device (9403) is now available which surmounts many of the above disadvantages and offers 16 words of storage. Development of I^3L technology made 64 words of FIFO storage economically feasible in the 9423. As this technology matures, larger FIFO buffers will become economical, and buffering a whole sector rather than a few words in a disc controller will be viable.

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Krishna Rallapalli is currently employed by the Computer Products group at National Semiconductor, participating in future systems development. Prior to this, he was involved in processor and peripheral controller designs, and performed managerial functions in application engineering pertaining to bipolar LSI products. He holds an MSEE from the University of Saskatchewan, Canada.

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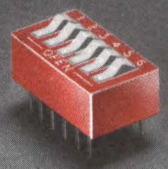

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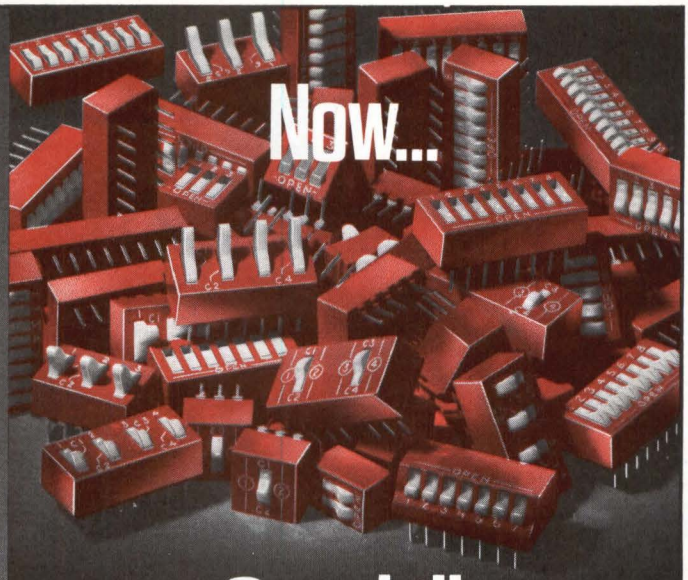

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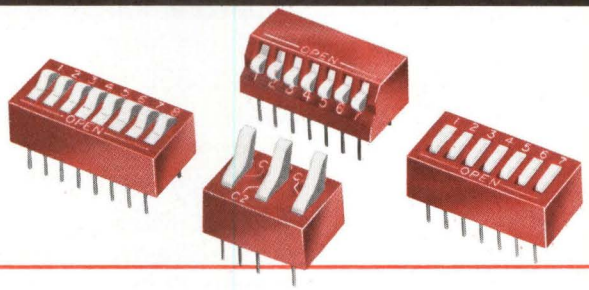

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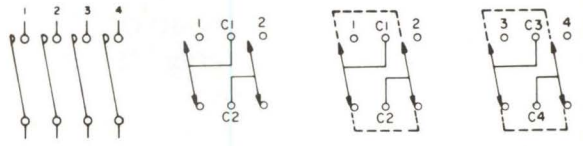

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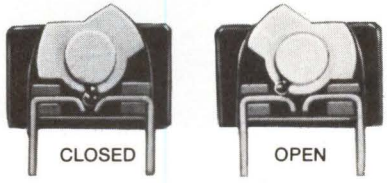

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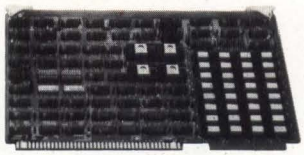

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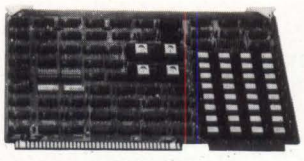

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Integrated into a video monitoring approach that provides data processing and cost benefits for a diverse application, a digital interface accepts TV scanning signals and produces equivalent X and Y tracking coordinates—under microcomputer direction—that accurately define object movements

Microprocessor-Based Interface Converts Video Signals for Object Tracking

Kenneth S. Lubinski, Kenneth L. Dickson, and John Cairns, Jr.

Virginia Polytechnic Institute and State University
Blacksburg, Virginia

Recent advances in electronic technology have benefitted many indirectly related fields of research. In the process of investigating certain effects of environmental contaminants, a video monitoring system was developed to record and analyze the movements of individual objects (fish). A television camera tracks the object in a square observation tank, and the video signals produced by the camera are converted into 8-bit X- and Y-position coordinates by a video-microprocessor interface. A voltage comparator in the interface acts as an image detector, responding to negative voltage peaks in the video signal produced when the vidicon tube in the camera detects a dark image against a lighter background. An 8080-based microcomputer samples these coordinates from the interface, averages all coordinates along the object's length into mean X and Y coordinates, determines whether the object has moved far enough to warrant recording a new position, and, if so, stores the mean coordinates and the running time using a teleprinter and punch. The system is relatively simple and less expensive than more sophisticated video-digitizing equipment, has greater resolution capabilities than photocell-array systems, and does not require "pingers," miniature transmitters that are attached or implanted during ultrasonic studies. In addition, raw data produced by the system, a time-series of X-Y coordinates, can be analyzed immediately or subsequently. This monitoring approach can easily be applied to situations where the analysis of the movements of objects in a 2-dimensional field is required.

System Description

The monitoring system includes the observation area, overhead television camera, video-microprocessor interface, 8080-based microcomputer, Teletype™ terminal (TTY), and a video monitor (Fig 1). The observation area is normally sealed off from external disturbances by a plywood housing, and internal indirect lighting evenly illuminates the area from above. Suspended directly above the center of the observation area, which measures 50 cm on each side, the television camera is oriented such that the video lines produced by it run parallel to the left and right sides of the tank (water flows slowly from the deep to the shallow end). Although each video field, or scan, is made up of 262.5 lines, only 200 of these travel across the observation area. Video signals are delivered to both the video-microprocessor interface and the video monitor; the monitor permits visual observation of the

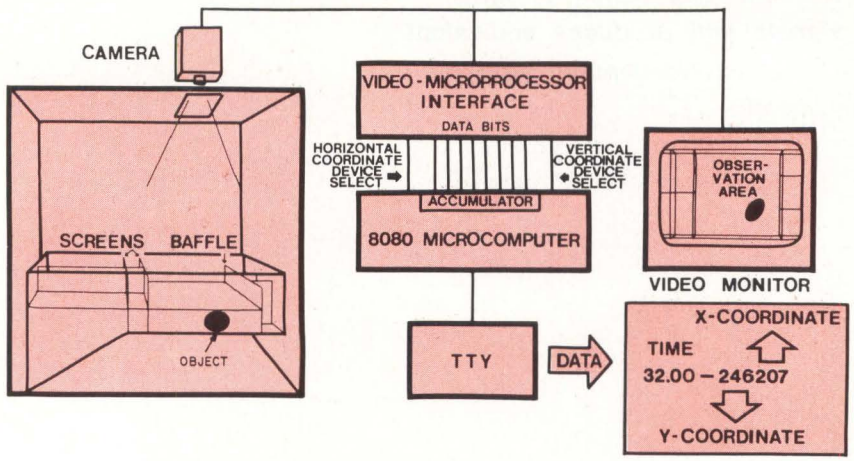


Fig 1 Monitoring system. Video signal from television camera enters both video-microprocessor interface and video monitor. Interface generates digital X and Y coordinates of points along length of object, and microcomputer controls sampling of coordinates, data manipulations, and storage using teleprinter and tape punch. Raw data are a time series of mean X and Y coordinates (time in seconds followed by a 3-digit octal Y coordinate and a 3-digit octal X coordinate

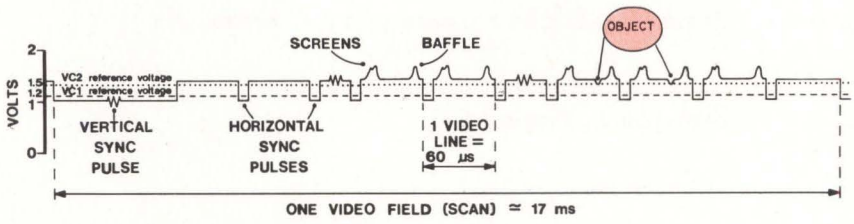


Fig 2 Video signal. Camera produces variable voltage signal (1 V peak-to-peak) containing low amplitude vertical and horizontal sync pulses. High voltage peaks between these pulses represent light reflecting off boundaries (screens and baffle) of observation area, while low voltage peaks represent points along length of object. Video signal is fed into two voltage comparators whose reference voltages are adjusted to detect sync (VC1) and object pulses (VC2)

object's movements while its coordinates are being sampled and stored. Under normal conditions, water depth in the tank averages around 8 cm, reducing problems from parallax during up or down object movements.

Interface Operation

An explanation of video-microprocessor interface operation requires a brief description of the video signal produced by the camera. The video signal is a variable voltage signal (Fig 2) having a 1-V peak-to-peak range. Short (5-μs), low-amplitude horizontal sync pulses occur between each video line, and long (400-μs), low-amplitude vertical sync pulses occur at a 60-Hz rate between each video scan. Between these sync pulses, high voltage peaks correspond to bright images picked up by the vidicon tube in the camera and low peaks to dark images. For instance, high voltage peaks occur in the video signal when the vidicon tube detects bright light reflecting off the screens and baffle that make up the downstream and upstream boundaries, respectively, of the observation area. Each video line that passes over the dark image of the object, on the other hand, contains a low voltage peak that corresponds to a point along its length.

In the interface, the video signal is input to two voltage comparators (Fig 3). A single integrated circuit (IC) (SN72720) houses both comparators, designated VC1 and VC2. These comparators and the other electronic devices in the interface are powered by the power supply for the microcomputer. The reference voltage (+) to VC1 is adjusted to approximately 1.2 V using a potentiometer. This allows VC1 to detect the vertical and horizontal sync pulses described earlier. The reference voltage to VC2 is adjusted to approximately 1.5 V, which allows that comparator to detect negative voltage peaks that correspond to points along the length of the object. Outputs of the voltage comparators are transistor-transistor logic (TTL) compatible and are used to trigger the other digital devices in the interface.

Two digital counters (actually two pairs of 4-bit binary counters, SN7493A) run constantly in the interface and are the sources of the 8-bit numbers that serve as tracking coordinates. The first counter is reset to zero during each video scan when the video lines

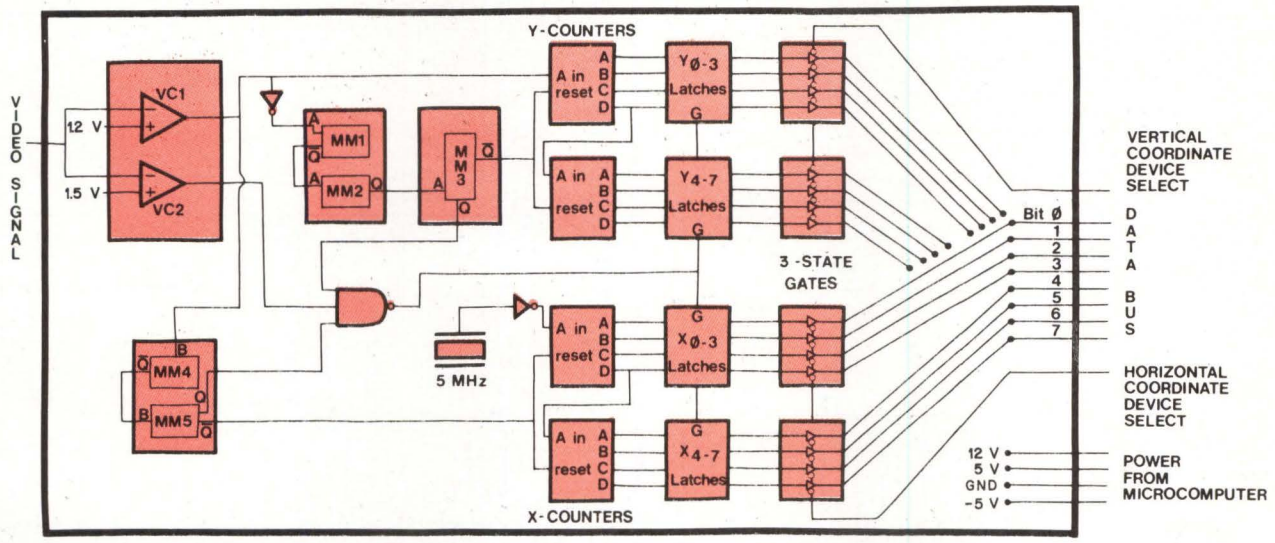


Fig 3 Interface schematic. Generalized schematic shows all digital devices and signals used to convert video signal into X and Y coordinates. Coordinates originate in two pairs of binary counters, one triggered by VC1 and other by a 5-MHz crystal-controlled oscillator that divides each video line into 176 sections. Monostable multivibrators, MM1 to MM5, are used to limit periods during which object can be detected to those when video signal is traveling across interior of observation area, and also to reset counters

finish crossing the inside of the observation area. When the video lines again start crossing the observation area, they are triggered by VC1 and produce Y-coordinates. The second counter is reset to zero each time a single video line leaves the observation area. When the following line reenters the observation area, this counter is triggered by a 5-MHz crystal-controlled oscillator. The oscillator divides the segment of each video line that falls within the observation area into 176 divisions, thus creating X-coordinates.

Each data bit of the counters is connected to a latch (four separate latches are available on each SN7475 chip). Output of VC2, the comparator adjusted for detection, is gated into the enable (G) of all of the latches. Each time a video line crosses a point on the object that is dark enough to trigger VC2, the output from VC2 enables the latches. As a result, the binary numbers present in the counters at that point in time are transferred and held in the latch outputs. Output of VC2, however, must be gated into the latches to prevent them from being enabled by vertical and horizontal sync pulses. For this purpose, monostable multivibrators (MM1 to MM5) produce two separate gating signals; two monostable multivibrators are available on SN74123 chips, and one each on SN74121 chips. Relationships between these signals and the video signal are illustrated in Fig 4.

Each gating signal must be at a high logic level for VC2 to enable the latches. The first gating signal is produced by adjusting MM1 to detect vertical sync pulses. MM1 is retriggerable and produces a positive pulse only if it does not detect a horizontal sync pulse within a 200-μs time interval. Output of MM1 is fed through MM2 to MM3. These multivibrators create, respectively, the rising and falling edges of the vertical gating signal. This signal, therefore, allows detection only during the central portion of each video scan that passes over the observation area. Similarly, MM4 and MM5, triggered by VC1, produce the rising and falling edges, respectively, which make up the horizontal gating signal. This signal, however, allows detection only during the central segment of each video line. By using external capacitors and potentiometers to adjust the monostable multivibrators in the interface, the size of the detection area may be adjusted to almost any rectangular shape within the field of view of the camera lens. Outputs ($\overline{Q}$)

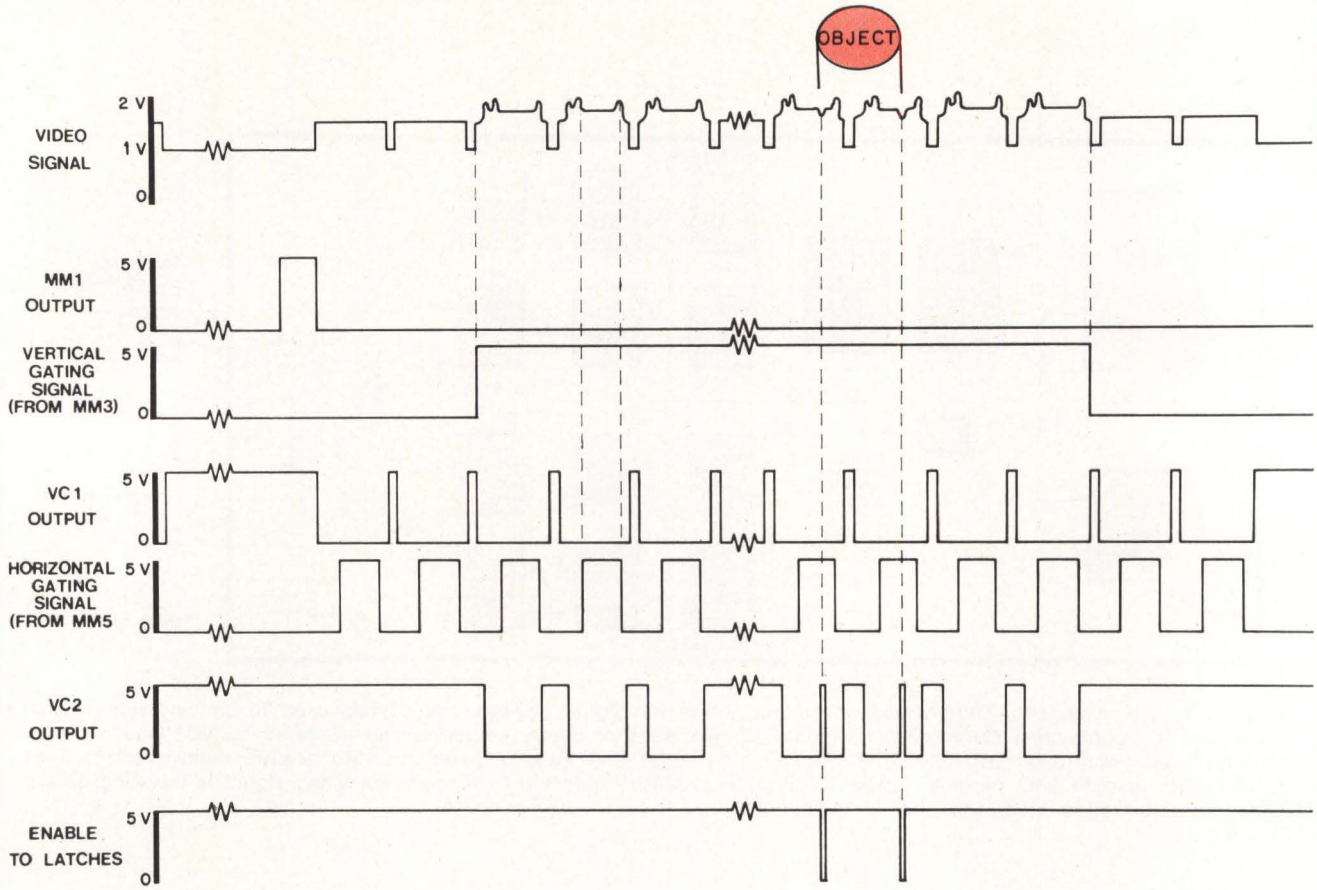


Fig 4 Timing relationships between video and gating signals. Vertical and horizontal gating signals and output from VC2, the detection comparator, are input to a 3-input NAND gate. When all three signals are at a high logic level, data latches are enabled, resulting in transfer of binary numbers present in counters to latch outputs

from MM3 and MM5, which represent the complement of the gating signals, are used to reset the vertical and horizontal counters as explained previously.

Latch outputs are directed into 3-state gates; four gates are available on each SN74125 chip. Two separate device-select pulses for the vertical and horizontal coordinates are produced by a device address decoder in the microcomputer. These pulses are used to enable the 3-state gates to output either the Y- or the X-coordinate in the latches onto the data bus and into the accumulator register of the microcomputer.

Software Control

The microcomputer controls the sampling of coordinates during tracking and thereafter manipulates and stores the collected data. A software flowchart describing the operation of the microcomputer is shown in Fig 5.

After all counters and storage locations are initialized, the microcomputer waits for a 4-s flag that is produced internally by a crystal-controlled oscillator. At each 4-s interval, a running time counter is incremented through the use of a floating-point program resident in programmable read-only memory (p/ROM). Initially experiments were performed with faster sampling rates, but results proved that sampling once every 4 s was more than sufficient to accurately track objects at the speeds they exhibited. Even at this seemingly slow sampling rate, a constantly moving object could produce 9000 data points in a 10-h experiment, and this volume of data would approach the storage capacity of available paper tape equipment. Typically, between 4000 and 7000 data points were produced.

After the running time counter is incremented, the pair of coordinates present in the interface latches are input into the accumulator of the microcomputer via the data bus. These coordinates are then moved into the first two memory locations of a data storage buffer. A second pair of coordinates are then input from the interface, but are not stored in the data buffer unless the Y-coordinate of the pair is different from the Y-coordinate of the previous pair. If this

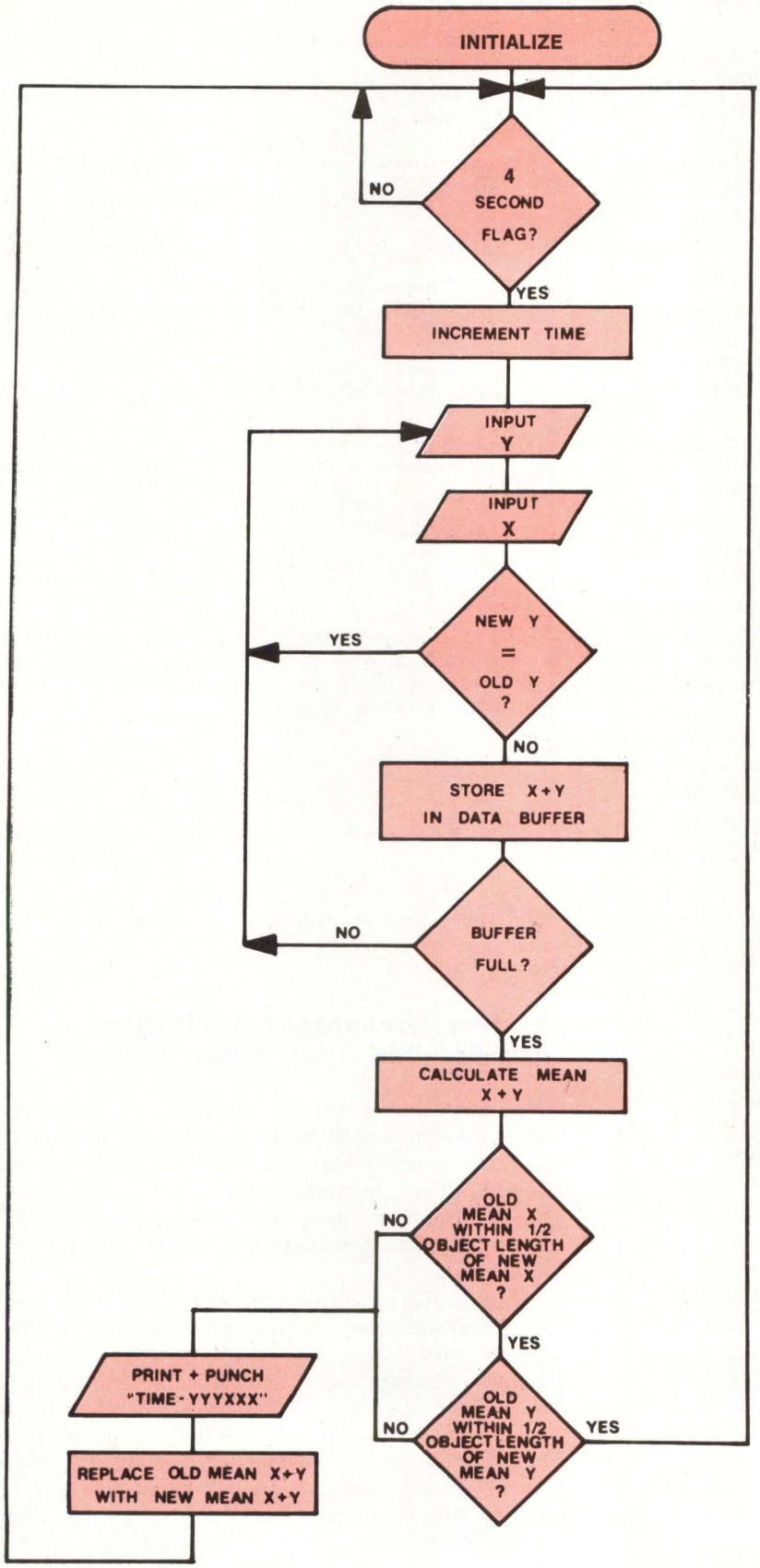


Fig 5 Flowchart of control decisions and sampling steps. At every 4-s flag, different X and Y coordinates are input into a data buffer until it is full. Mean X and Y coordinates are then calculated and printed along with running time of experiment, if object has moved a distance greater than one-half its length along either axis

step were omitted and the sampling happened to begin during a period of video lines that did not cross the object, the data buffer would fill up over and over again with the same pair of coordinates, representing the last point on the fish that was dark enough to trigger VC2. Coordinates are continually fed into the data buffer in this manner until it is full.

Size of the data buffer can easily be changed according to the size of the object being monitored. Other factors that must be taken into account in determining the size of the data buffer are how many coordinates are necessary to estimate accurately the object's mean location and how much time can be spent sampling coordinates from the interface. Objects that measure approximately 5 cm in total length have been monitored but usually only 60 to 70% of the length is dark enough to be detected by VC2. If an object this size orients directly perpendicular to the video lines, 10 to 12 lines may cross points that are dark enough to trigger VC2. An object oriented parallel to the video lines, however, may only be crossed by two to three lines. Typically, the data buffer size is set to hold 10 to 12 pairs of coordinates. This size buffer requires a maximum of only three to four video scans, or 51 to 68 ms, to become full even if the object's orientation is parallel to the video lines, while at the same time providing enough data points from which to derive accurate mean coordinates.

When the data buffer is full of coordinates that represent points along the length of the object, a subroutine is called to average both X- and Y-coordinates. Mean coordinates are stored, and a comparison is made between the current mean coordinates and the previous mean coordinates. If the object travels a distance greater than 50% of its total length along either the X- or Y-axis, the new mean coordinates are output to the teleprinter along with the running time of the experiment. Although this technique somewhat reduces the system's working resolution, it prevents unnecessary data from being accumulated during long periods of time when objects remain stationary. The new coordinates are then substituted for the old coordinates in memory. Fig 6 illustrates a sample of typical data output.

The present monitoring program occupies about 1k of random-access memory (RAM). The floating-point program resident on p/ROM occupies 1.25k and requires an additional 0.25k of RAM as a scratchpad. Currently, a more sophisticated software program is being developed for the video monitor system which will allow 15-min intervals of coordinate data to be analyzed for several parameters in real time. This program may require an additional 3k of RAM, and will require faster data storage capabilities than are now available with punched paper tapes. The parameters currently being analyzed by running the stored coordinate data through a larger computer include percent of time spent in motion, total distance traveled, percent of time spent turning, mean straight path length, and total time spent in each of four quadrants of observation area.

Position	Time — VVV(8)*	HHH(8)**	DATA DESCRIPTION
a	4.000 — 262	233	/EXPERIMENTAL RUNNING TIMES ARE RECORDED IN DECIMAL, COORDINATES IN OCTAL
b	8.000 — 211	237	
c	12.00 — 124	244	/MOVEMENT CONTINUOUS FROM POSITION a THROUGH e
d	16.00 — 037	242	
e	20.00 — 030	233	/OBJECT REMAINED STATIONARY AT POSITION e FOR 140 S
f	160.0 — 071	217	
g	164.0 — 150	156	/CONTINUOUS MOVEMENT RESUMED
h	168.0 — 217	071	
i	172.0 — 300	051	

* Vertical or Y (↑) coordinate: 310₈ to 0₈
** Horizontal or X (→) coordinate: 0₈ to 260₈

Fig 6 Typical output. Object movements result in listed output. Note that only mean coordinates are recorded if object has moved a prescribed distance from its previous position

System Advantages, Limitations, and Possible Applications

The video-microprocessor interface provides several advantages over both methods previously used to monitor object movements and other general monitoring systems. The practicality and convenience offered by these advantages may well stimulate other applications of computer-controlled processes via video-monitoring.

This system's most obvious and important advantages over previously used methods are that movements can be recorded faster, for longer periods of time, with greater accuracy, and automatically without a full-time observer. These advantages are particularly beneficial because, traditionally, studies of animal behavior have been laborious, time-limited, and highly subjective. An additional advantage from a monitoring standpoint is that raw data produced by the system are immediately stored and can be analyzed later for any parameter that may attract sudden interest.

The major advantage of the video-monitoring system over other similar monitoring systems lies in its power of resolution. Photocell-array systems are limited in resolu-

tion by the number of photocells used; some other video-monitoring systems (see Ref) are similarly limited. At the same time, increasing the number of photocells in an array also increases the chances of device failure, which may be critical during long-term monitoring. In addition, photocell equipment is restricted to one use, while the video camera is portable and could easily be reassigned to other monitoring uses.

A final advantage of the video-monitoring system is that it represents an initial developmental stage and, with some minor modifications, could perform additional tasks. For instance, by positioning a mirror next to the observation area at a proper angle to provide the camera with a side view of the object, a 3-dimensional position could be monitored. Alternatively, by storing additional coordinates (eg, maximum and minimum Y-coordinates sampled at each time interval and their corresponding X-coordinates), rotational orientation of the object to the water flow could be analyzed. These modifications would require some programming changes, however, and it should be noted that certain tradeoffs are necessary between how many points can be stored and how many analyses can be made on those points in real time.

The video-monitoring system is not without limitations. Its primary limitation is that the object being monitored must necessarily be darker than any other point in the observation area (although the system can likewise monitor bright points by reversing the inputs to the voltage comparators and by readjusting the reference voltages). Technically, voltage comparators are minimally sensitive to a difference of approximately 4 to 5 mV between their inputs; this represents the magnitude of how much darker (or lighter) the monitored object must be than background levels. Turbidity and variable background levels of light, therefore, create detection problems. For this reason, the system does not compare well with ultrasonic tracking systems, even though it does not require transmitters. Light limitations of the system for all practical purposes restrict its use to controlled-lighting environments. Time limitations of the system are caused by data storage and recording devices rather than by scanning time of the camera or response time of the interface. It should be noted, however, that in other applications where sampling time is critical, the 60-Hz video-scan rate may be limiting.

A list of possible video-monitoring applications to industrial control, measurement, and inspection processes was prepared by Sparks (see Ref). These include several processes that deal with the monitoring of moving objects such as particle counting, automatic speedometer calibration, pattern recognition, and operation of safety devices (kill-switches). Other possible applications might include liquid-level sensing and monitoring of flow rates or assembly line velocities. In any case, the video-microprocessor interface described should be adaptable to applications in many areas of research and industrial monitoring in addition to that of animal behavior, and the practical conveniences of video-monitoring in general should hasten the actual development of these applications.

Summary

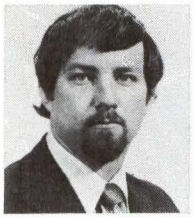
The electronic structure and operation of a video-microprocessor enable an interface to convert standard video signals into 8-bit X and Y coordinates of sufficiently dark (or light) objects within the field of view of the camera. Advantages and limitations of the complete video-monitoring system in which the interface operates must be considered by designers when deciding on the applicability of the system to their needs. The main advantages of the system over other monitoring systems are in its speed and resolution capabilities, whereas its major limitation lies in its dependence on controlled lighting conditions.

Acknowledgements

The authors wish to thank Gary F. Westlake for his original ideas concerning the development and design of the interface and the Manufacturing Chemists Association for providing the funds for its development.

Reference

J. E. Sparks, "Television that nobody watches," *Machine Design*, Feb 10, 1972, pp 3-7



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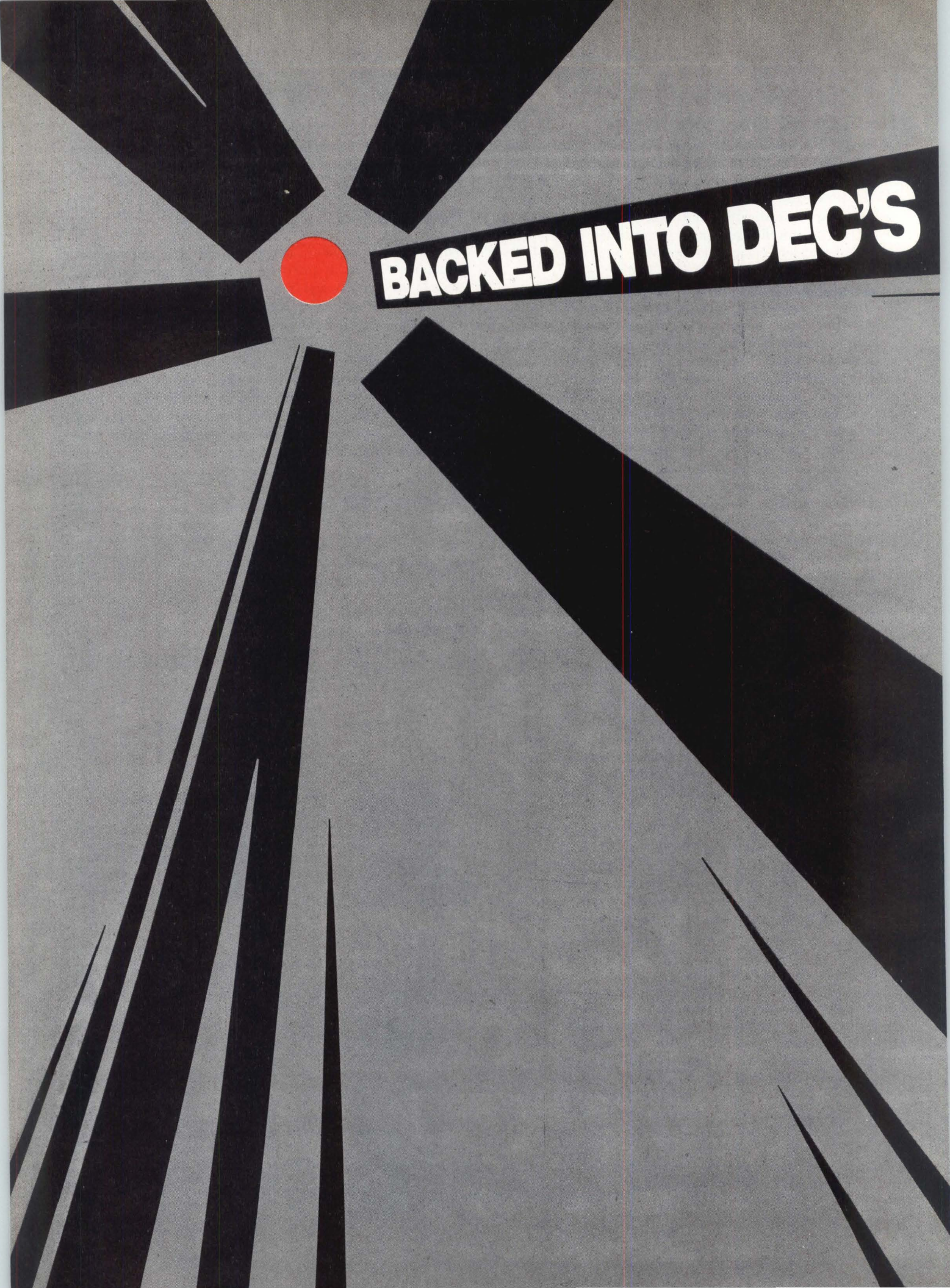
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APPLICATION NOTE

VMOS Peripheral Drivers Solve High Power Load Interface Problems

Lee Shaeffer

Siliconix incorporated
Santa Clara, California

Design of VMOS-type peripheral drivers results in high output current, easy paralleling, transient immunity, negligible input drive, and no supply voltage to overcome disadvantages of traditional devices for logic interfacing to high power loads

Traditional peripheral drivers suffer from several problems when called upon to deliver high power to loads —output current is limited, paralleling to increase current capability is difficult, and damage by transients is possible when driving reactive loads where high current and high voltage are present simultaneously. Furthermore, most peripheral drivers require substantial supply and input drive currents, which make their compatibility with metal-oxide semiconductor or complementary metal-oxide semiconductor logic marginal.

A different metal-oxide semiconductor field-effect transistor (MOSFET) technology, the VMOS (Vertical MOS) process produces a peripheral driver that has a high output current capability, is easily paralleled, is relatively immune to transients, and requires negligible input drive power. Power required from the supply may also be neglected—no supply is needed. An additional advantage of

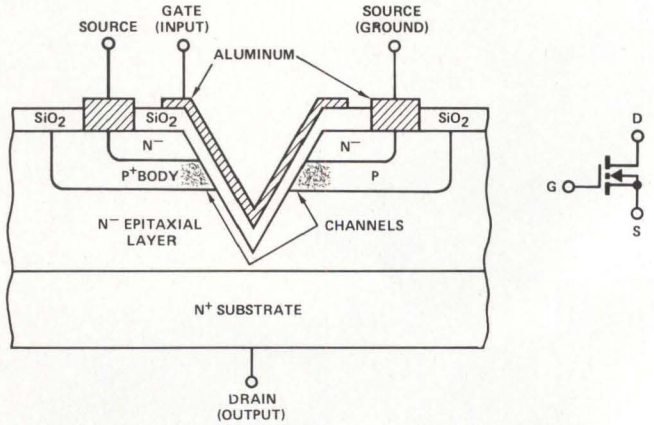

Fig 1 Cross-section of VMOS channel. High current chip is made by laying many channels side-by-side. S55V01/S55V02 series peripheral drivers, which conduct 2 A, have total gate length of 1.1" (2.8 cm) on chip which is 43 x 71 mils. Because current is automatically shared between channels, no special layout is needed

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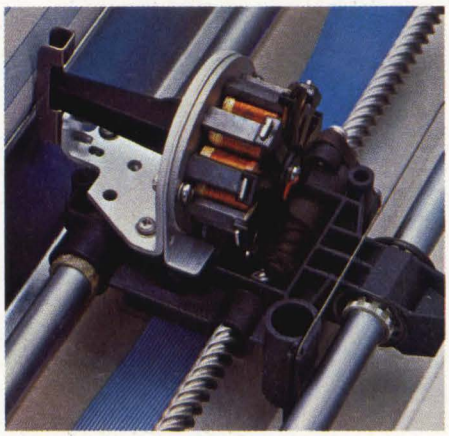

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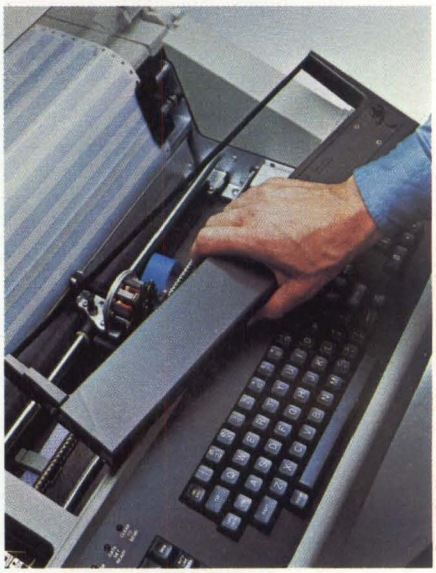

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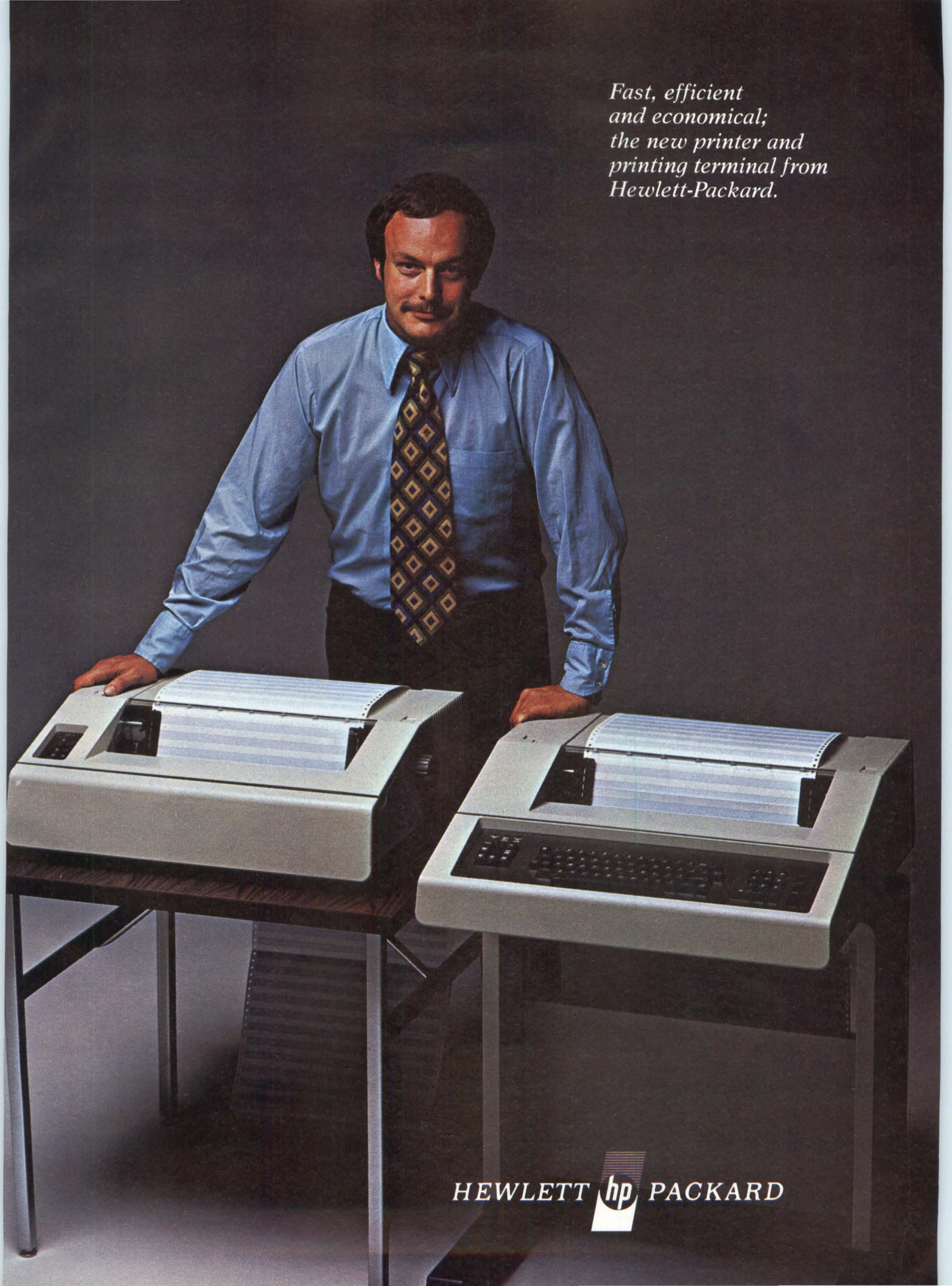
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devices produced in this way is a very fast switching time—4 ns to switch 1 A, when driven properly. When applied to peripheral interface systems, these features increase capability and reliability, and decrease power requirements and parts count.

VMOS Technology

While VMOS performance is similar to that of a standard n-channel MOS (n-MOS) transistor, VMOS processing is similar to that of a double-diffused epitaxial (epi) planar transistor. Key advantage of VMOS over standard n-MOS is that the vertical structure is capable of a much higher current density; appreciable current flows perpendicular to the chip plane rather than parallel, and may be conducted through a chip of moderate size. For example, a 43 x 71-mil VMOS chip can conduct 2 A, while 10 A will pass through an experimental chip which is approximately 160 mils on a side.

A VMOS channel (Fig 1) is started by growing an n-epi layer on an n+ substrate. A p-well, which later becomes the body, is then diffused into the epi, followed by an n+ source diffusion. A V-groove is preferentially (anisotropically) etched through the entire structure, with gate oxide and field oxide grown, and aluminum metal is deposited to form the source connection and gate. The groove effectively produces two channels and doubles the current density. Finally, the entire chip is passivated to prevent contaminants from entering the sensitive gate region.

The n+ substrate, which is also the drain, is the output connection, while the body and source are tied to ground, and the gate becomes the control and input terminal. In operation, the drain (output) to body (ground) diode junction is reverse biased and no current flows. When the gate is positive with respect to ground, however, n-type carriers—induced in the p-type body by the electric field surrounding the gate—create the so-called "channel" through which current passes. Electrons can now flow from the n+ substrate, through the induced n-type channel in the body, and out the n+ source. Since this electron current passes entirely through n-type material, VMOS is strictly a majority carrier device.

Bipolar transistor operation is fundamentally different because electrons flow through the base region as minority carriers. Also, collector current is controlled by a low voltage (<1 V) and relatively high current input, rather than by a low current and relatively high voltage (approximately 10 V) input as it is for VMOS. The difference between the operation of VMOS and bipolar transistors is striking, considering the similarities in processing. Processing for a power transistor is essentially the same until the V-grooves are etched.

Comparing VMOS with a standard n-MOS transistor shows major processing differences, although electrical operation is nearly the same. Vertical structure gives VMOS the following advantages.

(1) Defined by diffusion depths rather than by less controllable mask spacings, VMOS channel length is shorter, one to two microns versus five or more microns for standard processing. Since the current density of a MOSFET is proportional to w/l (channel width divided by channel length), its current density is three to six times greater. Therefore, for a given channel width—which is the primary determinant of chip size—the technology can deliver three to six times the drain current that standard MOS can deliver.

(2) Shorter channel length also reduces chip capacitances by a comparable amount. For example, a 2-A VMOS geometry has an input capacitance of about 45 pF, while a standard device with equal current capabilities, if it could be fabricated, would have an input capacitance of 250 to 300 pF. The lower capacitance produces switching times which are approximately five times faster (4 ns versus 20 to 25 ns, with a 50-Ω pulse generator input).

(3) The VMOS epi-layer increases breakdown voltage, because it absorbs the depletion region from the reverse-biased body-drain diode junction. This layer is thin and is part of the drain, so it does not adversely affect performance other than by adding a slight series resistance. To achieve a high breakdown voltage in a standard MOSFET, the body—and therefore the substrate—must be lightly doped. Unfortunately, this makes the threshold voltage difficult to control, and renders the devices susceptible to parasitic leakage paths created both by contaminants and by electric fields surrounding the drain metalization. Furthermore, gate oxide must be thick enough to withstand the entire gate-drain voltage (versus about one-third V_{DG} in VMOS), so that a high voltage standard MOSFET would conduct less current for a given input voltage.

Peripheral Driver Capabilities

S55V01/S55V02 series drivers conduct 2 A of continuous current, 3 A peak (at 35, 60, or 90 V breakdown)—considerably greater than the 300 mA specified for standard drivers, such as the 55450/75450 series. This extra current is needed when driving heavy duty relays, solenoids, and stepper motors. Extra power dissipation encountered at these higher current levels is not a problem, since the S55V01 series is packaged in a TO-3 header with a maximum power dissipation of 25 W, and the S55V02 series is capable of dissipating 6.25 W in a TO-39 package.

If greater current is needed, drivers may simply be paralleled, since they have resistive output characteristics—two devices in parallel will automatically share current. Furthermore, the temperature coefficient of their saturation (ON) voltage (V_{OL}) is positive; thus, if one device draws more current initially, it dissipates more power and heats up. This, in turn, causes V_{OL} to increase, forcing the other paralleled drivers to conduct a greater share of the current. Power-wasting buffers or ballast resistors are not needed for eliminating the current hogging prevalent in bipolar output stages. The only compensation needed for paralleling VMOS devices is the inclusion of a noncritical resistor (300 Ω to 1 kΩ, 0.25 W) or ferrite bead in each input lead to prevent high frequency oscillations. The current mismatch between paralleled devices is usually less than 20%.

The same phenomenon responsible for automatic current sharing also increases the reliability of a single device, because hot spots cannot develop during switching transitions. If current tries to flow more heavily through a particular portion, the chip heats up only slightly before the excess current is forced to other areas on the chip. Bipolars behave

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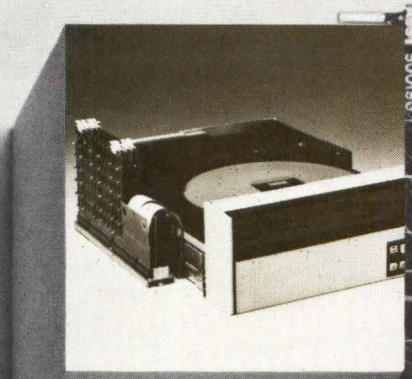

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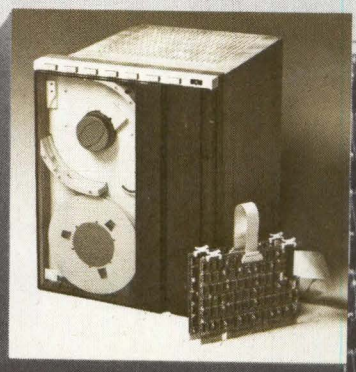
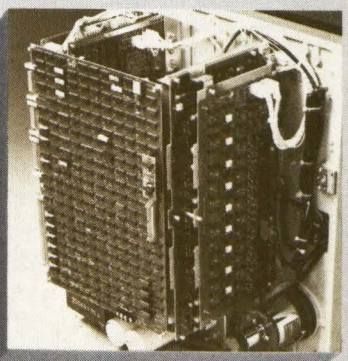
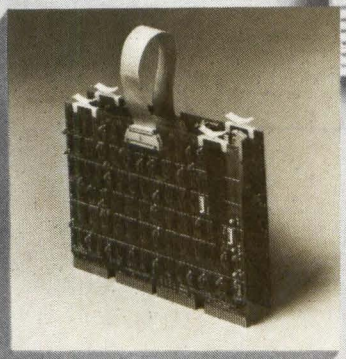


Magnetic Tape Subsystems, vacuum column and tension-arm designs, with speeds from 12.5 to 75 ips are offered in one to four drive configurations, formatted in PE, NRZI or dual density. Autoload cartridges or open reel tape from 7 to 10½ inches are available.



Magnetic Tape Formatters, embedded or stand-alone models, provide all necessary logic for reading and writing PE or NRZI formats on both 7-track and 9-track tapes. The space and cost saving microprogrammed embedded formatter is contained on a single multi-layer PWB within the transport.



Wangco single-source systems feature high-performance PDP-11 and NOVA compatible controllers designed to work at maximum efficiency and lowest cost with Wangco disk and tape transports. Compact controller design requires minimum space in the host computer.

Flexible Disk Drive Systems for interface to PDP-11 and NOVA computers are available in one to four drive configurations for low cost data storage in IBM compatible format.

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CIRCLE 40 ON INQUIRY CARD

in just the opposite way; a hot spot conducts even more current, which further aggravates the problem and decreases reliability due to resulting high temperatures, metal migration, and secondary breakdown. This should be considered when switching inductive loads, such as relays, solenoids, or magnetically actuated printer hammers, since peak voltages are often present simultaneously with peak currents.

Another major advantage of the technology is its low power requirements: drive current is 10 nA typical, 500 nA maximum. For an input drive of 10 V, this represents a maximum power dissipation of 5 μW. If a CMOS gate has an output current capability of 1 mA, and switching time is not important, the gate can simultaneously drive two thousand VMOS peripheral drivers (a fanout of 2 x 10^3. Conversely, bipolar peripheral drivers designed to mate with CMOS logic, such as the 1631, require 50 to 200 μA typical, a current factor of at least five thousand more. VMOS, therefore, is suitable when many peripheral drivers are to be driven from a single logic element, or when the logic itself is low power.

A second power consideration concerns the current that the peripheral driver draws from the logic supply. In a typical bipolar driver, logic consumes roughly 5 mA, which is 25 mW at 5 V or 75 mW at 15 V. Direct power supply requirements of a VMOS driver are zero, because it requires no logic supply; it obtains its required power from the logic element driving it. This saves more than 0.25 W when ten loads are driven.

Complete lack of a power supply connection represents an additional advantage when the load is located away from the logic. By physically incorporating the VMOS driver into the load as a buffer, the load presents a high impedence to whatever logic element it may be connected. Only two high impedance connections—the control input and ground —need to be made between the logic and buffered load.

VMOS peripheral drivers can switch very quickly—1 A in 4 ns when driven by a 50-Ω pulse generator. This high speed is a definite advantage when driving PIN diodes or laser diodes. Of course, this speed is not possible unless the device is driven fairly hard. Still, when driven by standard CMOS logic, it can switch within 25 to 30 ns, including the delay introduced by the gate itself.

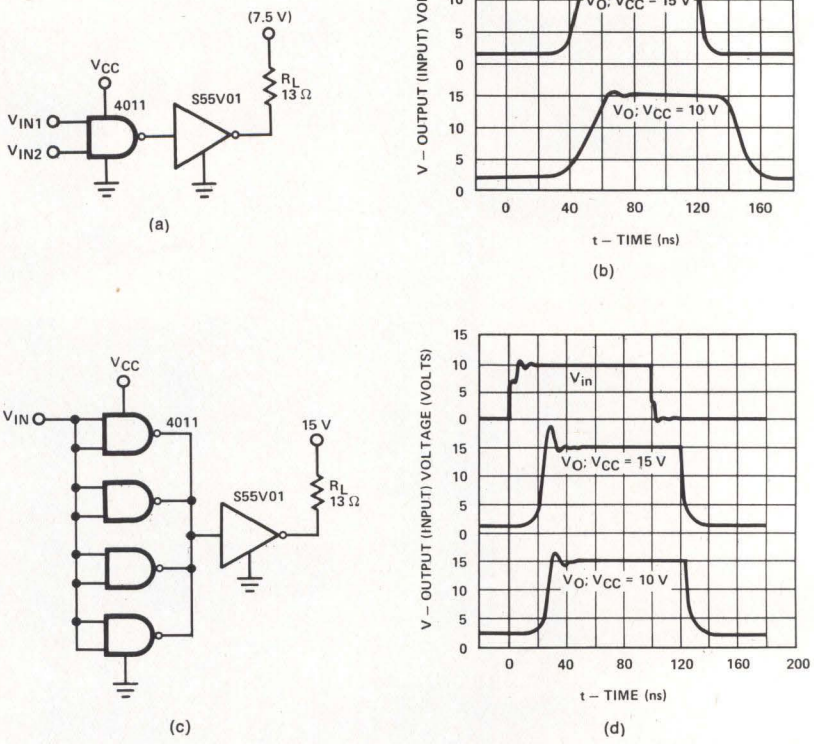


Fig 2 CMOS logic interface. All that is required to interface S55V01 to digital CMOS is simple connection (a). Switching times are on order of 50 ns and depend somewhat on logic supply voltage (b). Switching speed is doubled by connecting four CMOS gates in parallel to quadruple available peak input drive current (c) and (d)

Several inherent factors must be evaluated when designing with VMOS. First, VMOS peripheral drivers do not have sharply defined switching transitions; that is, there is no definite voltage for which a peripheral driver is fully on or fully off, since it actually has a linear transfer characteristic. Output current capability of the drivers is about 700 mA with a 5-V input (V_{IH}); the guaranteed minimum is 300 mA. Increasing V_{IH} to 10 V raises the output current (I_{OL}) to 2 A typical, 1 A minimum. In the off state, the output current (I_{OH}) is a maximum of 1 mA with an input drive (V_{IL}) of 0.8 V; taking the input closer to ground reduces this current considerably ($I_{OH} = 0.5$ μA max for $V_{IL} = 0$).

In most applications, the lack of sharp switching transitions is not a problem since on/off levels are fully compatible with outputs of CMOS logic. TTL can also directly drive VMOS, but some pullup or level shifting is helpful, or even necessary, when switching high currents. This may even be an advantage since limiting the drive voltage reduces the maximum surge current into the load.

A second design consideration is that the on voltage drop (V_{OL}) in-

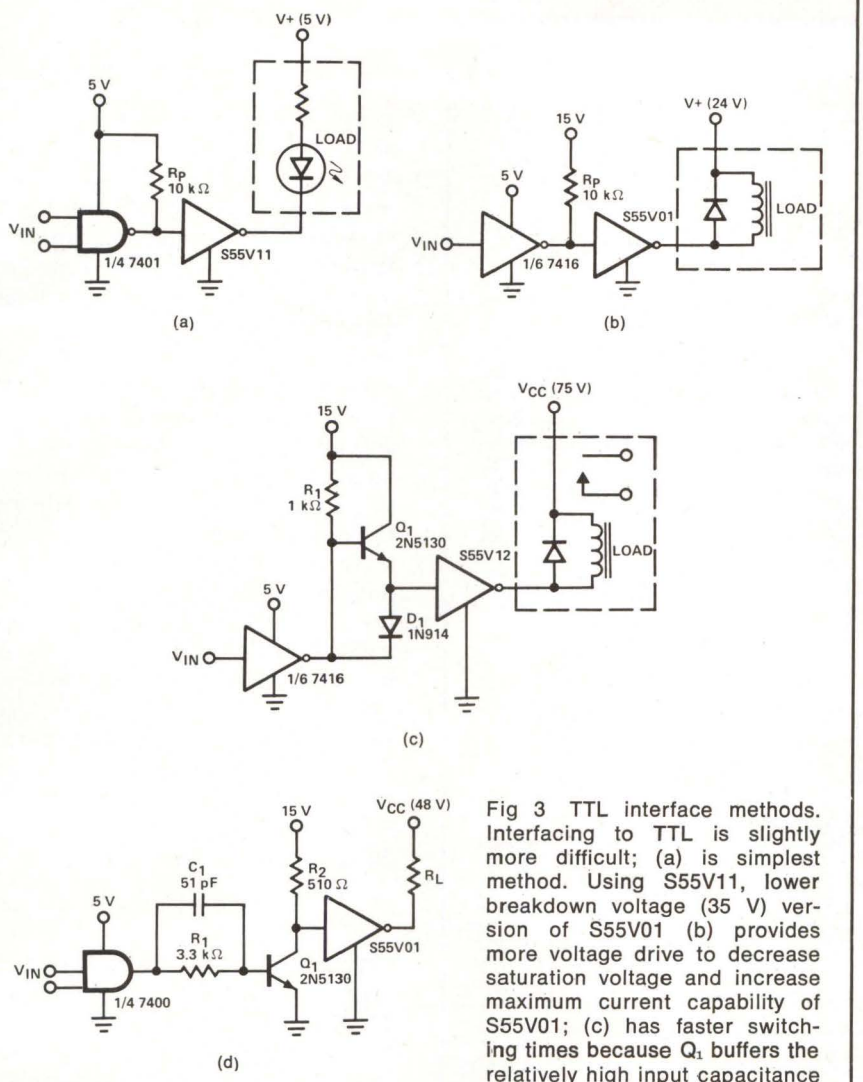


Fig 3 TTL interface methods. Interfacing to TTL is slightly more difficult; (a) is simplest method. Using S55V11, lower breakdown voltage (35 V) version of S55V01 (b) provides more voltage drive to decrease saturation voltage and increase maximum current capability of S55V01; (c) has faster switching times because Q_1 buffers the relatively high input capacitance of the S55V12. Bipolar voltage amplifier (d) translates the 0.4- to 2.4-V TTL output swing to a 15-V drive signal

creases with increasing temperature because of its positive temperature coefficient—it nearly doubles when the temperature increases from 0°C to 150°. This phenomenon increases the power dissipation in the peripheral driver which, in turn, further increases the temperature. While this is not a factor at low power levels, a good rule of thumb at high power levels is to increase the calculated power dissipation by 50% when figuring heat-sink requirements.

Applications

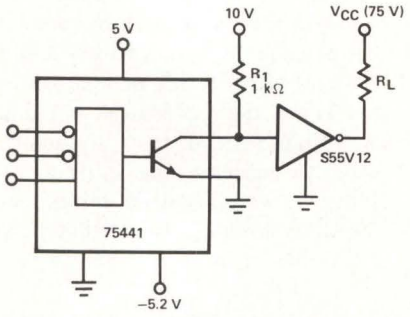
Low input current requirement of the peripheral drivers is desirable when interfacing with standard CMOS logic. Fig 2(a) is the simplest possible configuration—the driver is connected directly to the output of the VMOS, with no extra components needed. Fig 2(b) shows the switching response of the circuit for different values of logic supply voltage. Since the inherent delay of the driver is 2 ns, the CMOS gate is responsible for most of the delay in the circuit. The driver loads the CD 4011 NAND gate with 1000 MΩ in parallel with 65 pF, its input and Miller capacitance, which should be considered when driving multiple peripheral drivers from a single CMOS gate in an application where speed is important. To decrease switching time, the drive current to the driver is increased by paralleling several CMOS gates [Figs 2(c) and 2(d)]. Of course, operation from the highest possible logic supply voltage (for example, 15 V) also ensures fast switching times.

Interfacing to TTL is not as straightforward since the output voltage swing of TTL is less than it is for CMOS. When driven by the minimum guaranteed V_{OH} of 2.4 V, the input drive to the VMOS is inadequate, and the peripheral drivers will switch currents of only 50 mA or less, which is far below their 3-A peak capability. A pullup resistor to V_{CC} should be used to increase the current capability to a guaranteed minimum of 300 mA, which is the output current realizable with a 5-V drive to the input [Fig 3(a)].

A better solution is to use open-collector TTL with its output pulled up to 15 V [Fig 3(b)]. Driven by the increased voltage, the driver will switch 1 or 2 A comfortably. If faster switching times (<30 ns) are needed, the best approach is the totem-pole drive shown in Fig 3(c). To achieve a fast turn-on time without an unduly small pullup resistor, which dissipates considerable power when the switch is in the off state, an emitter follower drives high peak currents into the capacitive VMOS input. A bipolar transistor may also be used to amplify the TTL voltage levels if open collector TTL is not available [Fig 3(d)]. Note that this circuit can be driven by any low level signal, including ECL, if a comparator such as the AM686 is used in place of the SN7400 quad NAND gate. Switching times of this circuit are less than 40 ns in both directions.

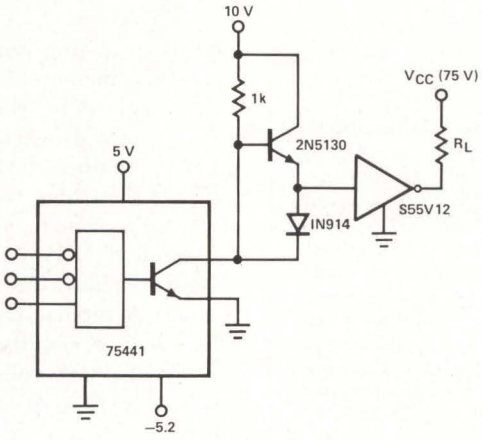
Interfacing to ECL is slightly more complicated due to its negative logic levels. The S55V01/S55V02 series can be used to buffer an ECL-compatible peripheral driver, such as the SN75441, which is good to 30 V and 150 mA. The S55V12, which is identical to the S55V01 except that its breakdown/saturation voltage is higher, increases these capabilities to 90 V and 2 A, respectively. The 75441 has an open collector output, so it interfaces to VMOS with either a pullup resistor or totem-pole driver (Fig 4).

Two VMOS peripheral drivers are needed to make a line driver, since capacitive loads such as cables or long data buses require a bidirec-

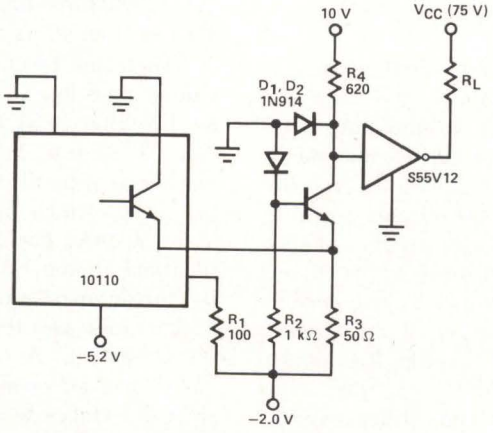


(a)

Fig 4 ECL interface methods. S55V12 can increase voltage and current capabilities of 75441 ECL-compatible peripheral driver; (a) uses only pullup resistor on output of 75441 to interface to S55V12. Increased performance is achieved using totem-pole output in (b). ECL can be interfaced to S55V12 without use of 75441 with MC10110 circuit (dual 3-input, 3-output OR gate) shown in (c)



(b)



(c)

tional current drive. Fortunately, because of the simplicity of these peripheral drivers, it is relatively easy to source as well as to sink current into the load. However, the VMOS that is sourcing current must have its "ground" terminal connected to the output bus, and its input driven by a peak voltage whose value is greater than the positive supply for maximum efficiency. Bootstrapping (using a charged capacitor to generate a voltage higher than the positive supply) is therefore necessary since the output will only rise to within 4 or 5 V of the rail if the input is driven directly from the positive supply. The value of the bootstrap capacitor is small (about 0.05 μF at 500 kHz) because of the low input drive current requirements of VMOS. Using several high speed bipolar transistors in an inverter-totem pole arrangement produces turn-on and turn-off times of 20 and 30 ns, respectively, into a load of 50 Ω in parallel with 1000 pF.

Summary

VMOS has several advantages when used to fabricate peripheral drivers. It requires negligible drive current and no power supply connection; thus, it is suited for CMOS logic and low power systems. In high power applications, it is rugged, reliable, easily paralleled, and extremely fast. Although fully CMOS-compatible, VMOS peripheral drivers will also interface directly to TTL, and to ECL with level shifting. Present VMOS peripheral drivers are capable of up to 3-A currents, 90-V breakdowns, and 25-W dissipation; even greater capabilities should be available in the near future.

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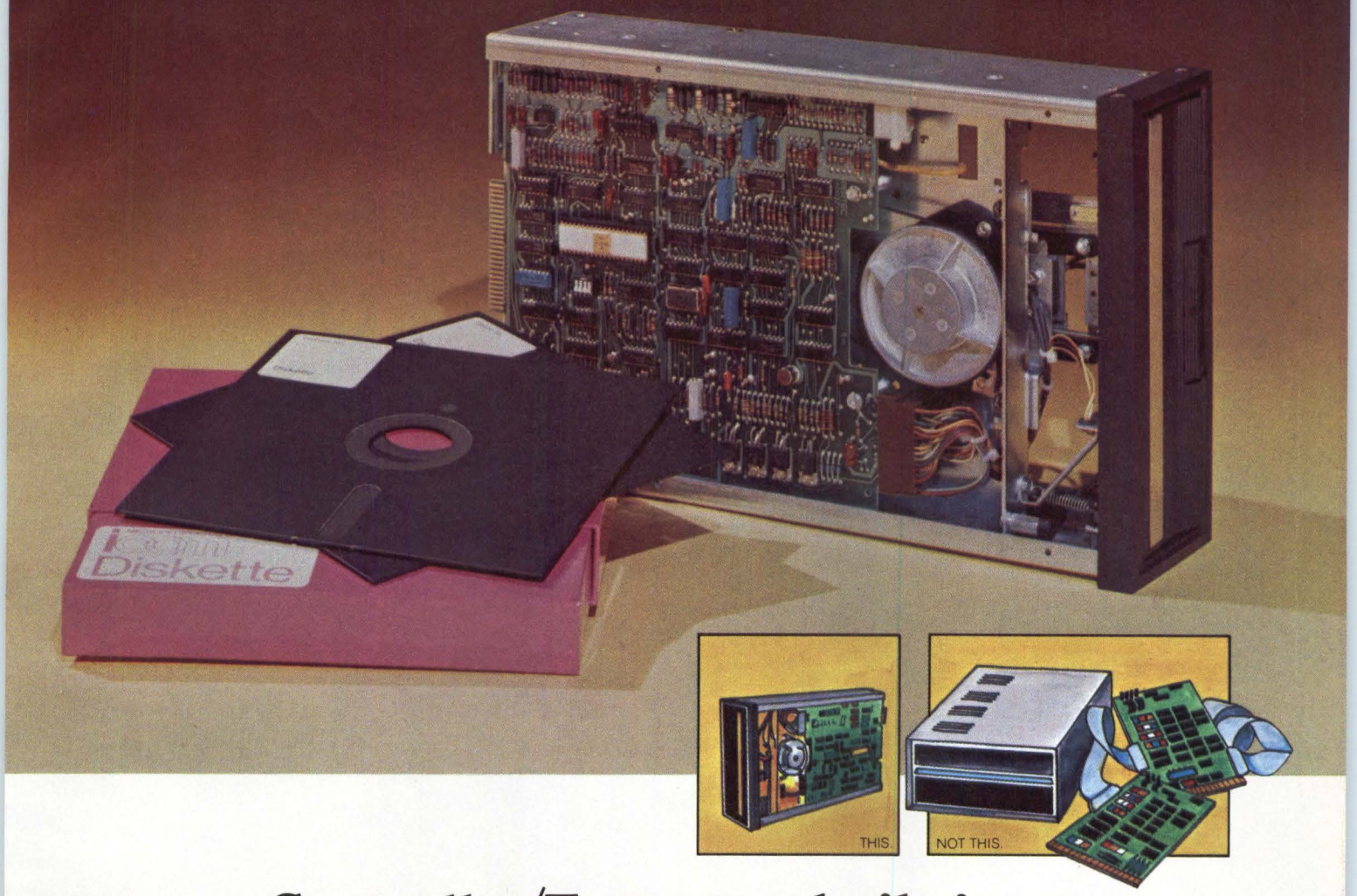

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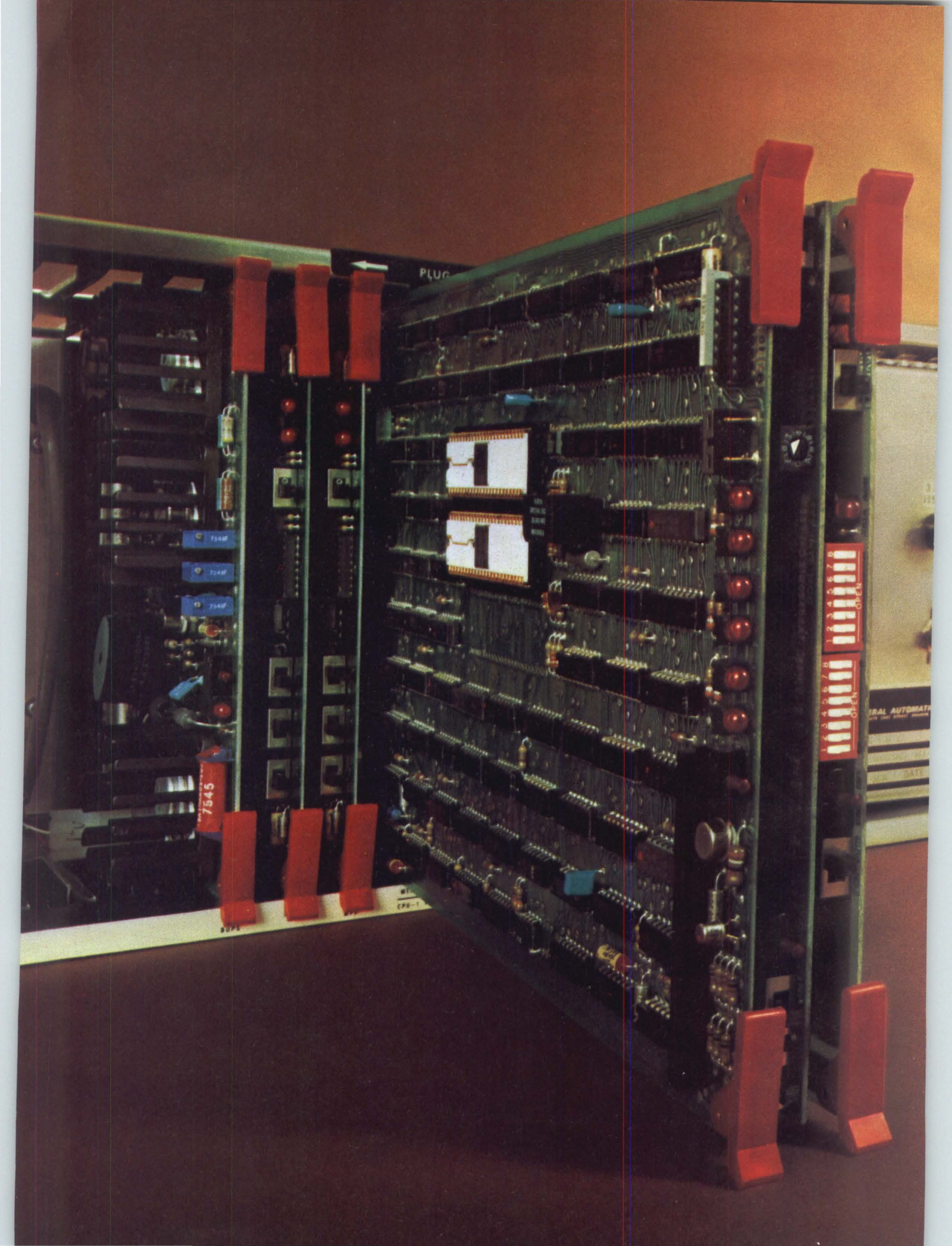
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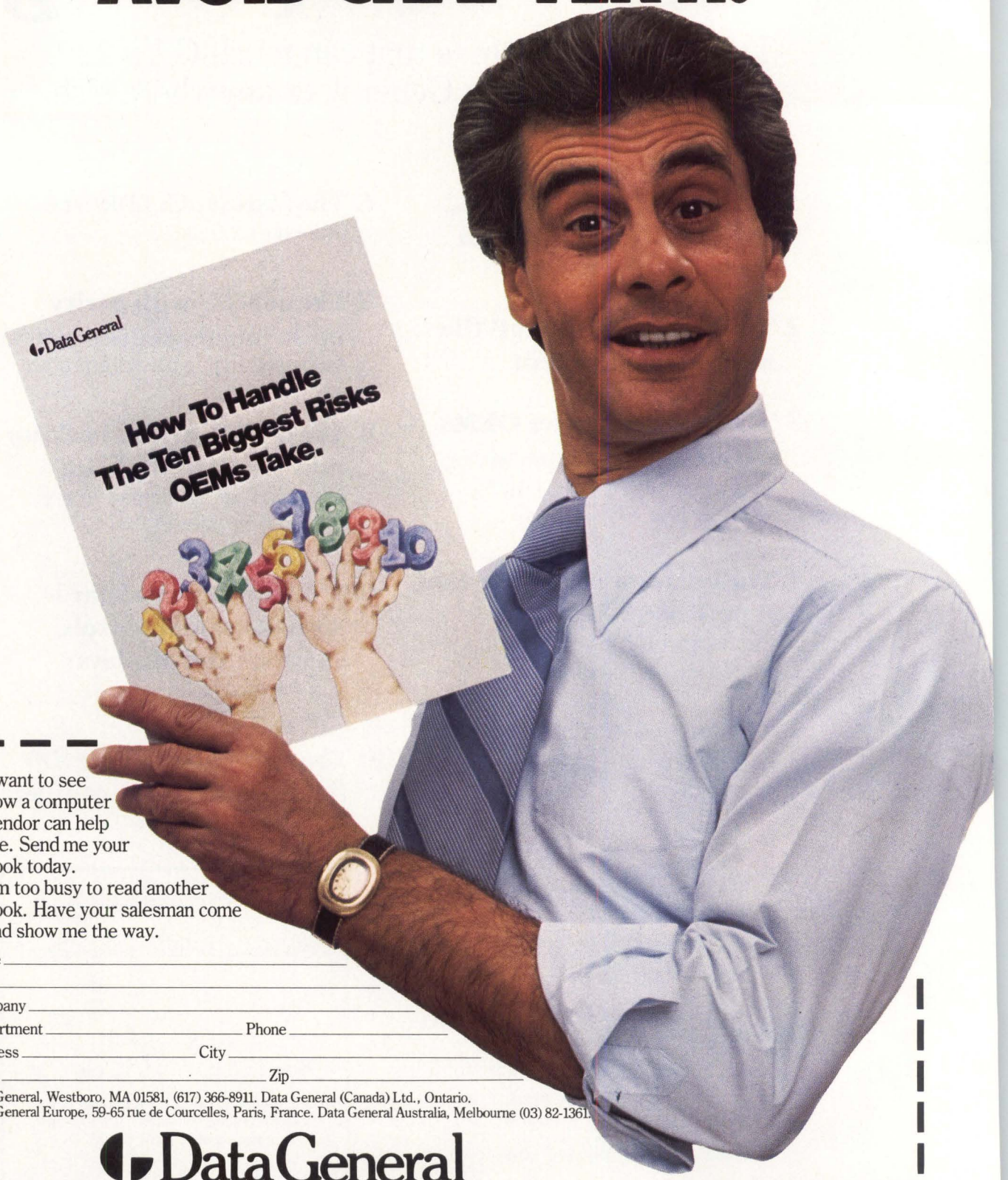

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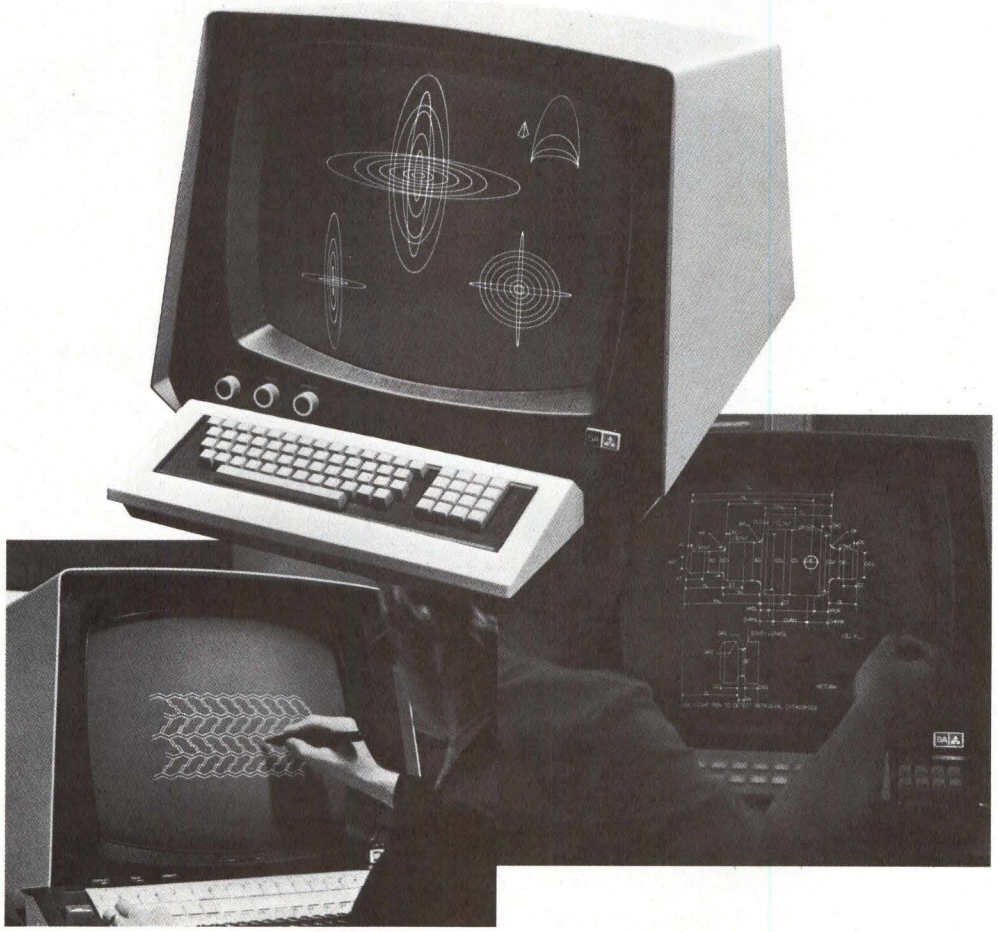

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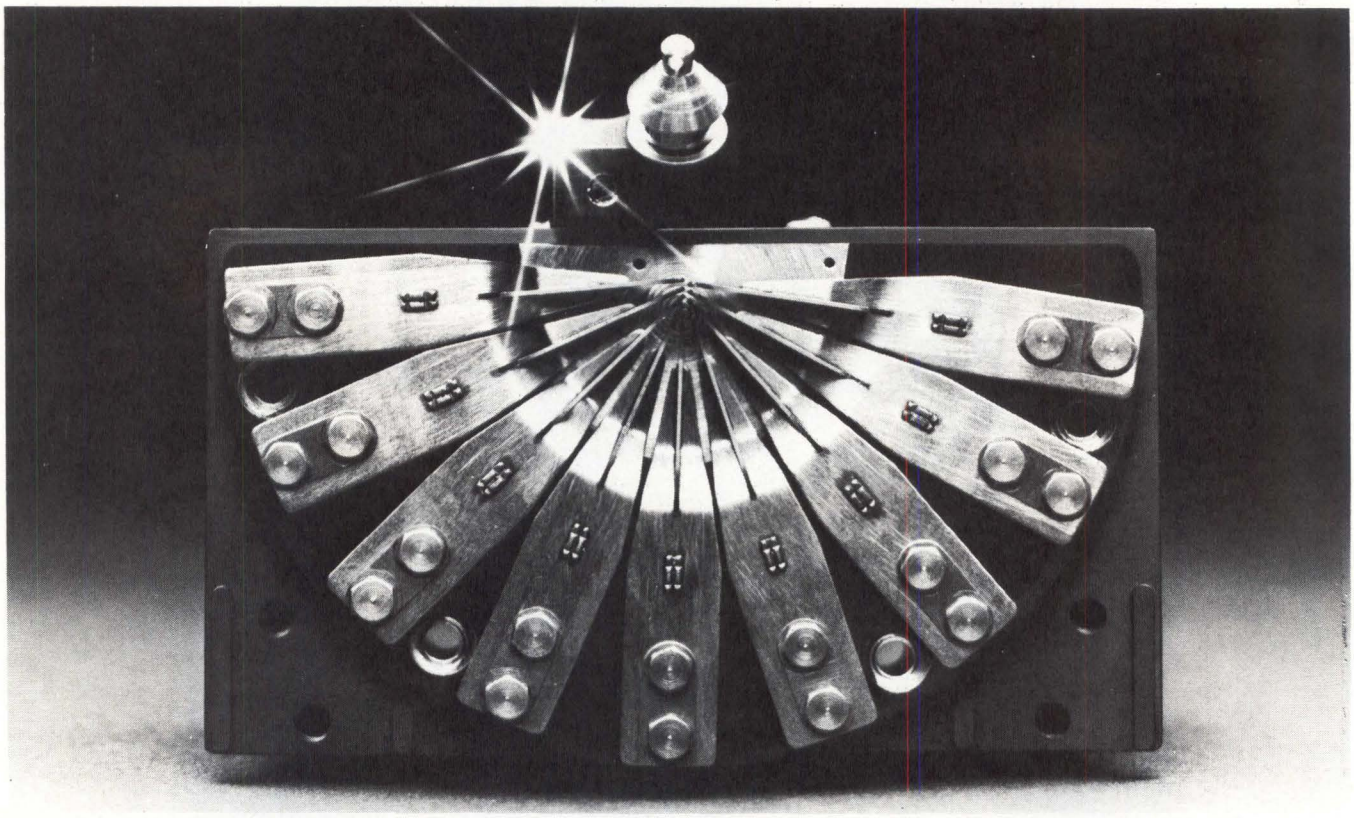

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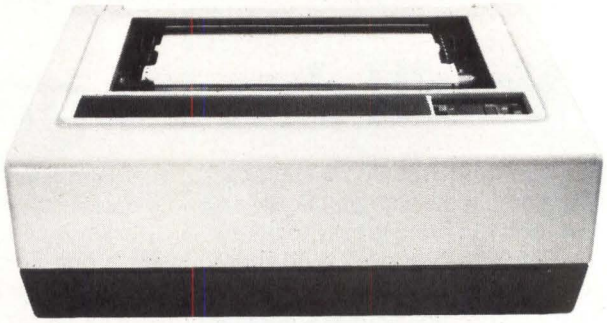

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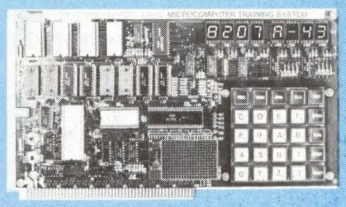

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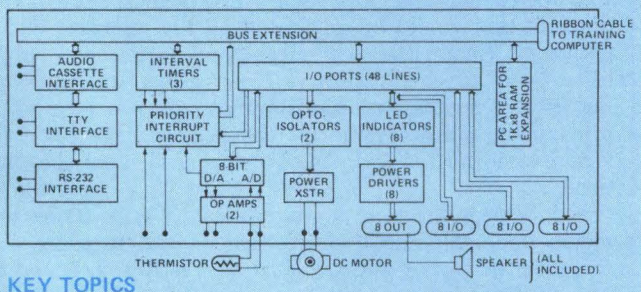

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Microcomputer Interfacing: Sample-and-Hold Devices

David G. Larsen
Peter R. Rony
Virginia Polytechnic Institute & State University

Christopher Titus
Jonathan A. Titus
Tychon, Inc

Sample-and-hold devices or sample-and-hold amplifiers are analog circuit elements equivalent to the digital latch. They are used to sample an analog signal and then hold it steady at a particular point so that a voltage of interest may be measured or used elsewhere in a system. Operation of an ideal sample-and-hold device (Fig 1) shows that the sample-and-hold output follows, or tracks, the input during the sample period and then holds the latest analog voltage when it switches to the hold mode. Input and output voltage lines in the Figure are offset slightly for clarity.

Concepts Relating to S/H Devices

Acquisition Time	Time required (generally a few microseconds) to go from the hold state to tracking state, in which output remains within a 0.01% range of input. This is also called settling time when the S/H device is already in sample mode. (Fig 4)
Offset	Difference between the device's input and output voltages when input is ground. It is generally in millivolts. Offset may be adjusted to zero using external components, but will usually change with time and temperature. (Fig 4)
Slew Rate	Maximum rate of change for output, expressed as V/s. It is a limitation imposed by the charging rate of capacitors and actual slew rates of operational amplifiers present in the S/H circuit. (Fig 4)
Aperture Time	Time period required by the device (usually a few nanoseconds) to go from sample mode into hold mode once the hold command has been received. (Fig 5)
Droop Rate, Decay Rate	Rate of discharge of the S/H capacitor, expressed in mV/s, which is a function of switch leakage current and current required by other circuit elements connected to the capacitor. (Fig 6)
Gain Error, Linearity	Variation of the observed output from the expected output over the S/H device's entire output voltage range. It is usually expressed as a percentage, say 0.01%. (Fig 6)

These sample-and-hold (S/H) devices are extensively used in conjunction with digital-to-analog (D-A) and analog-to digital (A-D) converters. For example, they may be used to:

1. Hold an analog signal steady so that an A-D conversion may be performed
2. Simultaneously sample many analog inputs for later measurement (requiring one S/H device per analog input)
3. Deglitch a D-A converter's (DAC) output to eliminate output voltage spikes or settling transients
4. Distribute one DAC's output to several points, where analog voltages must be constantly maintained

The second and fourth uses are becoming less important than they were two or three years ago. It is probably less expensive now to dedicate an A-D converter (ADC) to each input to be measured and to have one DAC per output, depending upon the specific application.

The most common use of S/H devices is to sample and hold an analog signal at a particular point while an ADC measures it. An S/H device is particularly useful in situations in which a DAC and comparator are used in conjunction with microcomputer software to create an ADC.[1] When an S/H device is used prior to inputing the unknown signal to the comparator (or an ADC module if one is used), the digitization may give an accurate representation of the unknown voltage. For example, Fig 2 represents a block diagram of a typical S/H computer interface that permits the peak voltage from an instrument to be measured. It is assumed that the instrument provides a positive clock pulse, called PEAK, when the peak maximum is reached. The SAMPLE pulse from the computer allows the S/H module to sample the unknown signal from the instrument. When the peak is reached, the PEAK signal clocks a logic 0 into the output of the flip-flop, forcing the S/H device into the hold mode. Fig 3 shows the timing diagram that would be generated by the interface circuit in Fig 2. Again, the S/H output and instrument output have been offset for clarity. Now, either a slow ramp ADC or fast successive approximation ADC can be used to provide the correct value for the peak voltage since the S/H device will maintain the voltage until it can be digitized.

S/H devices are not, however, ideal. Some terms that aid in understanding their restrictions and uses are contained in the Listing and are illustrated in Figs 4, 5, and 6.[2] As can be observed, there are important limitations to their capabilities. Those devices that have short acquisition times use small capacitors and thus will have a large voltage droop rate. Use of larger capacitors means longer acquisition times but less voltage droop. When high acquisition speeds and long hold times are required in an application, two S/H modules may be used. The first quickly acquires the analog signal at the point of interest, and the second acquires and holds the output from the first device. The second S/H device takes longer to acquire the voltage presented by the first device, but since a large capacitor is used, its droop rate will be much lower. Ref 3 provides further details.

A number of S/H devices are commercially available, eliminating the need to construct your own. The following

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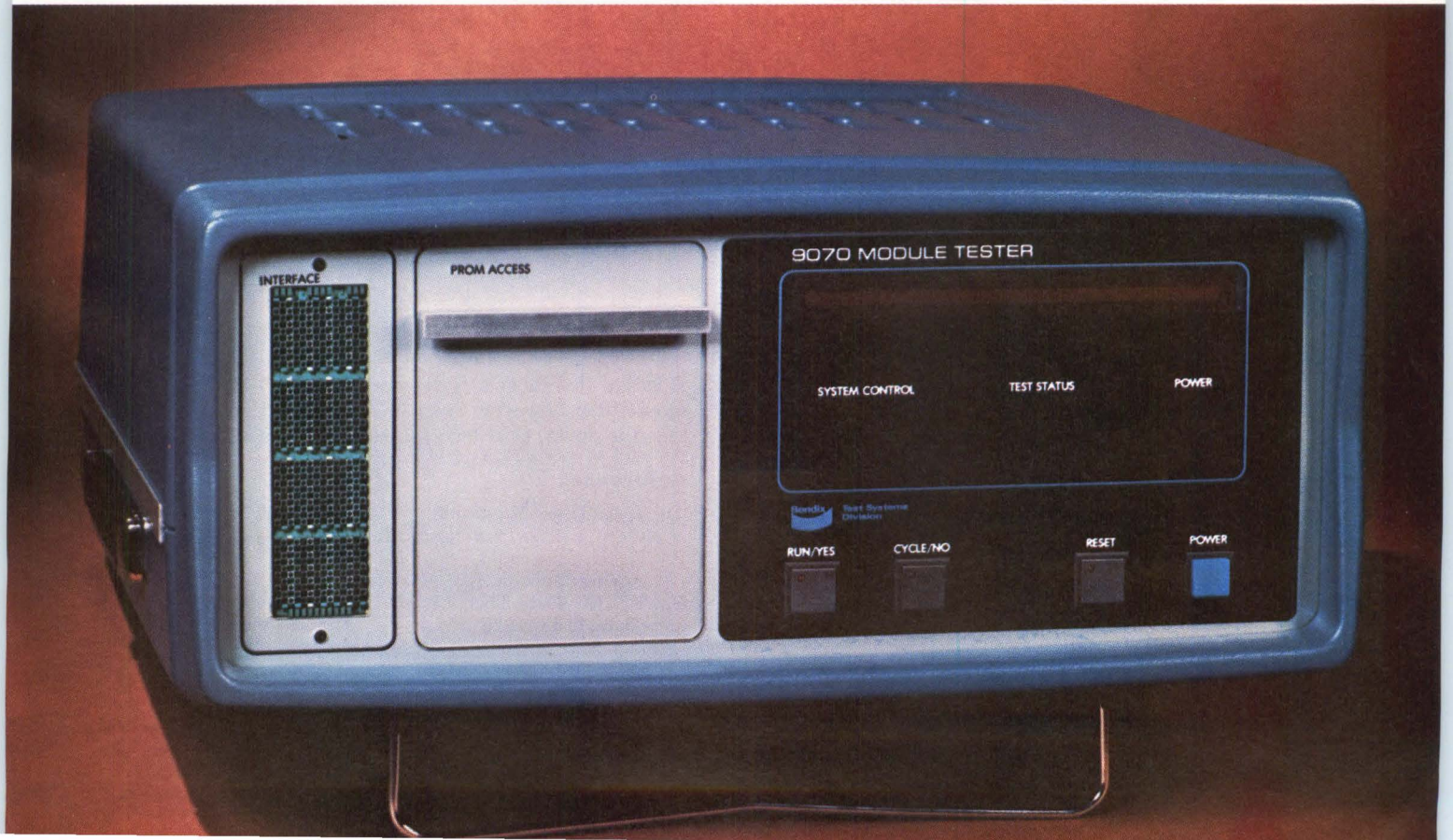

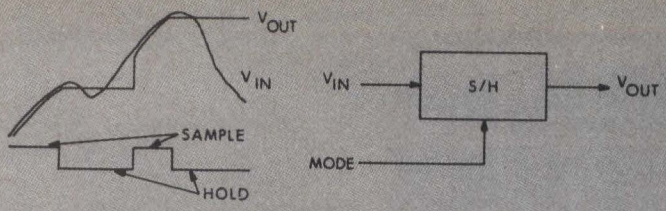

Fig 1 Inputs and output for ideal S/H device. Both sample and hold modes of operation are shown

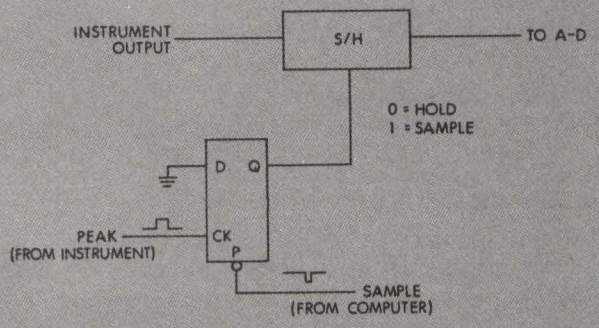

Fig 2 Block diagram of typical S/H microcomputer interface circuit. Instrument supplies PEAK input pulse to flip-flop; SAMPLE pulse from computer presets flip-flop to logic 1

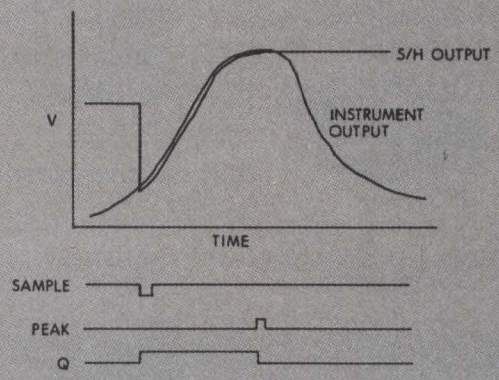

Fig 3 Typical timing diagram for interface circuit in Fig 2

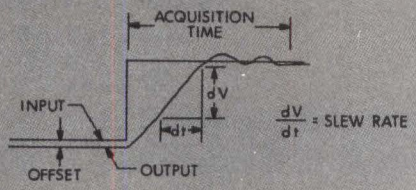

Fig 4 Representation of acquisition time, offset, and slew rate[2] (Courtesy of Analog Devices, Inc. All rights reserved)

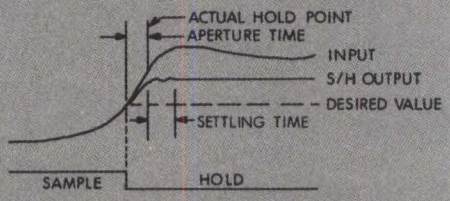

Fig 5 Representation of aperture and settling times[2] (Courtesy of Analog Devices, Inc. All rights reserved)

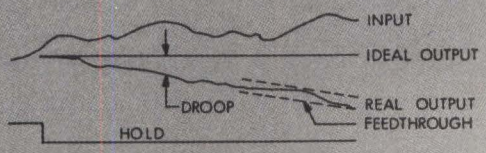

Fig 6 Representation of linearity, droop rate, and feedthrough[2] (Courtesy of Analog Devices, Inc. All rights reserved)

list of modules, although not complete, is representative of those available.

Analog Devices, Inc, Norwood, Mass		
SHA-5	General-purpose	$ 47
SHA-1A	General-purpose	$150
Burr-Brown, Tucson, Ariz		
SHC80KP	Low cost	**$ 34**
SHM60	High speed	$104
Datel, Inc, Canton, Mass		
SHM-LM2	Low cost IC	$ 8
SHM-CM	General-purpose, ±12 V	$ 89
Hybrid Systems Corp, Bedford, Mass		
SH703	Low cost	$ 22
Intersil, Inc, Cupertino, Calif		
IH5110	Low cost IC	$ 9
National Semiconductor Corp, Santa Clara, Calif		
LF398	Low cost IC	$ 5
Teledyne Philbrick, Dedham, Mass		
Model 4853	High speed	$125

Prices of the above S/H devices are subject to change without notice; however, keep in mind that the general price trend is down, as is true for most semiconductor devices.

References

1. J. A. Titus, *Microcomputer Analog-Digital Conversion Devices*, E & L Instruments, Inc, Derby, Conn, 1977
2. D. H. Sheingold, *Analog-Digital Conversion Handbook*, Analog Devices, Inc, Norwood, Mass, 1972
3. LF-398 Data Sheet, National Semiconductor Corp, Santa Clara, Calif, 1976

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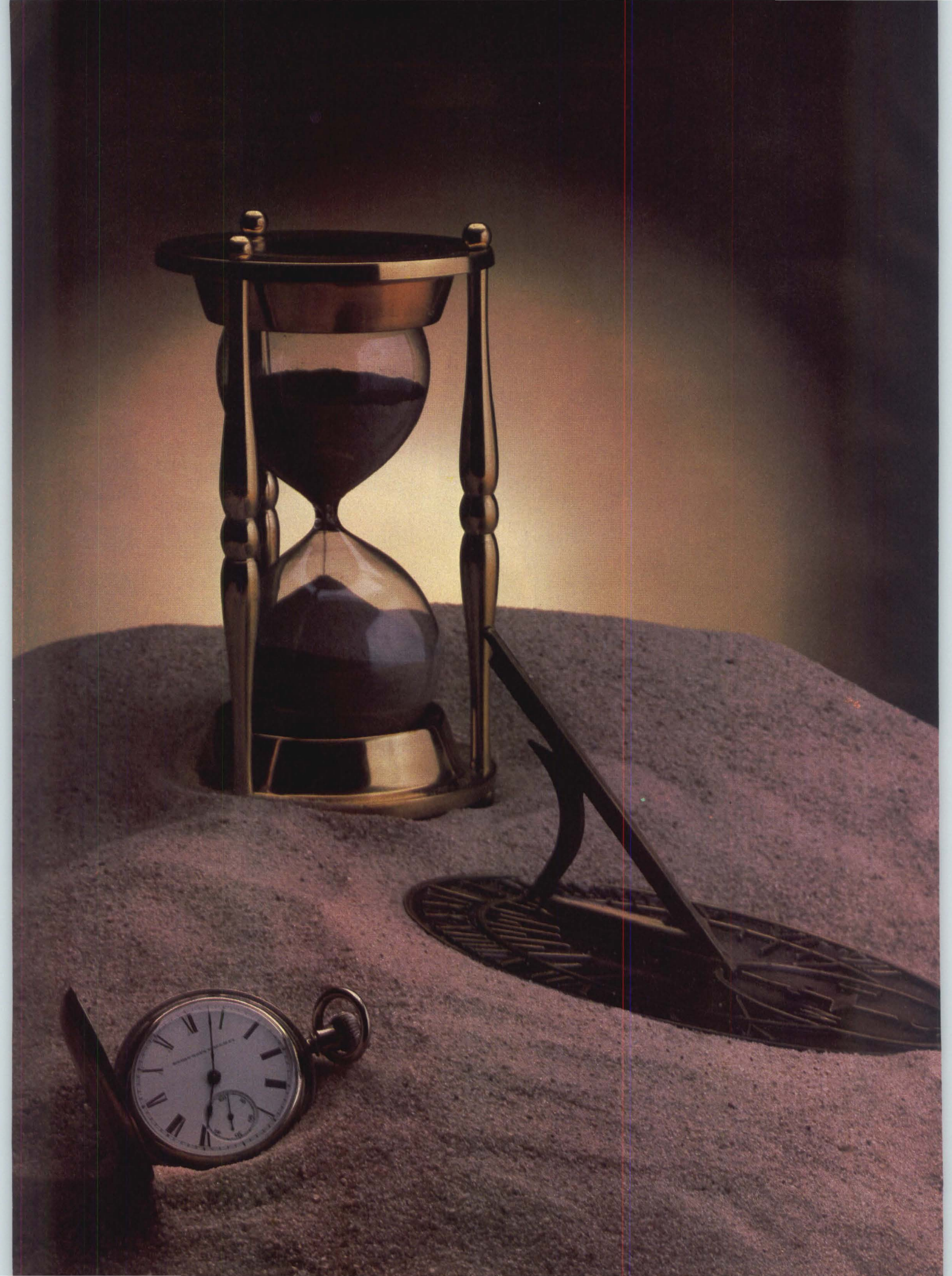

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The SEL 32/35 can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including control processor with floating-point arithmetic, memory, chassis, power supplies and cabinet.

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Added Quad Serial Port Module and Optically Isolated Digital Input Module Enhance Microcomputer Series

Two modules for the SuperPac 180 microcomputer series are the 1821 optically isolated digital input module and 1860 quad serial port module with total communications capability. Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 developed the multiport input module to function in a 180 system under control of the company's 1806 or 1810 microcomputer system; the quad serial port module interfaces modems, computer peripherals, and other computers to the SuperPac series.

Digital Input Module

Interfacing of machines, instruments, sensors, controllers, and other 180 microcomputer series devices is facilitated by the 1821 which provides complete isolation of the microcomputer from the process. A major feature is the module's ability to protect the microcomputer from electrical interference, ground loops, and common mode noise normally found in industrial environments.

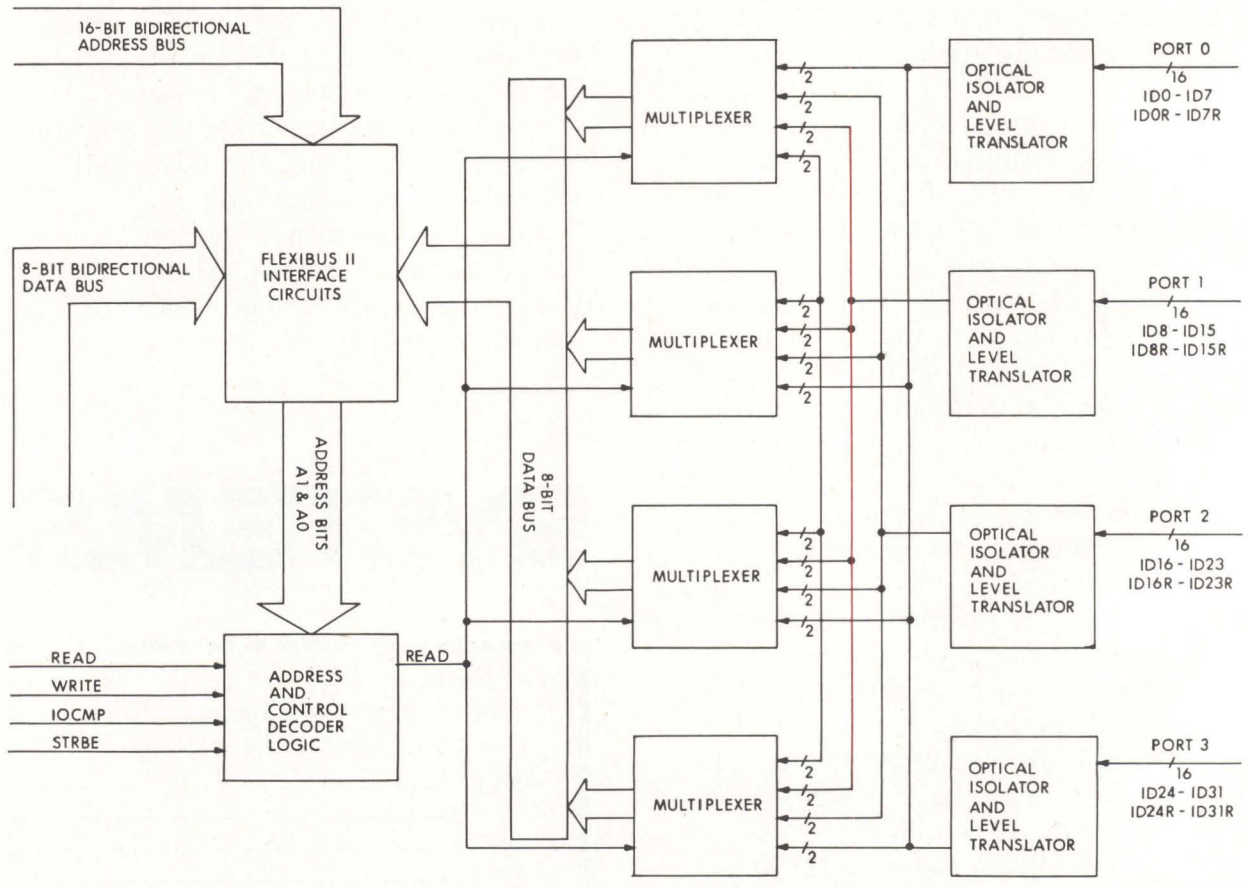
Three configurations are available: the baseline module which accommodates 32, 24-Vdc digital input signals, and options A and B which are configured to accept 32, 115-Vac and 5- to 50-Vdc input signals, respectively. Optical isolation and bounce filters, as well as individual reference return lines, are provided for each of the 32 inputs (organized as four 8-bit parallel ports).

The module is useful in either industrial or laboratory environments which develop ac or dc compatible signals for measurement and control purposes. Multiple devices may be used in the same chassis with other series modules to extend system input capability. All modules are automatically connected, upon insertion, through the Flexibus II backplane circuit board and connectors.

Circle 170 on Inquiry Card

Quad Serial Port Module

On the single PC board of the 1860 module are four independent, asynchronous, full-duplex, tri-function serial ports (RS-232-C, 20-mA current loop, and party line), each with optically isolated UARTS. Baud rates from 110 to 9600 are switch selectable on a per port basis.



Input interface of 1821 optically isolated module consists of 32 digital input bits organized as four 8-bit parallel ports. Inputs are optically isolated and multiplexed, and may be bit or byte organized by user program under appropriate software control. Bounce filters of 5 ms are provided for dc inputs; hold up circuitry is provided for ac inputs

(Continued on p 114)

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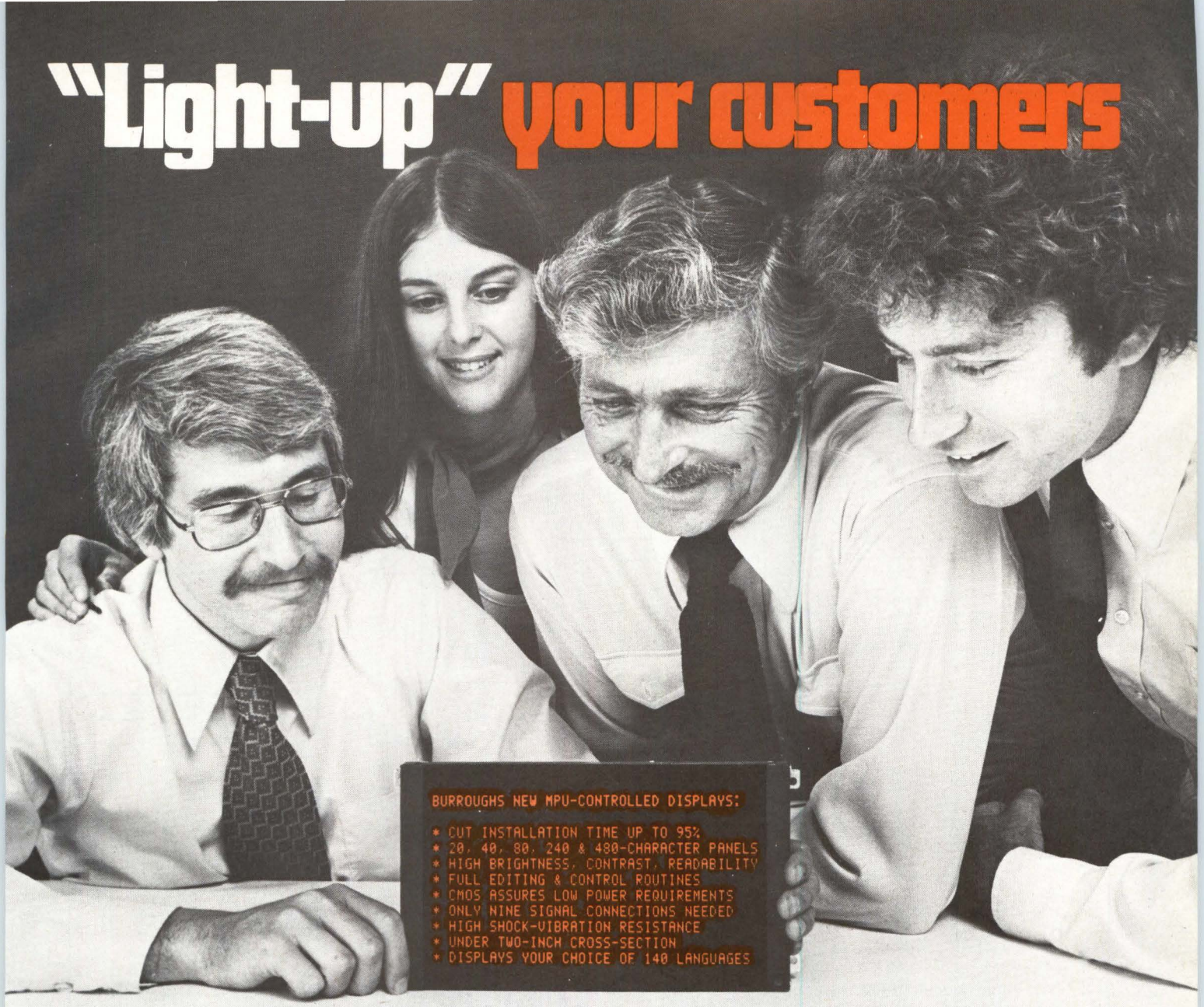

...with Burroughs new microprocessor-controlled thin display systems!

Burroughs announces a major advance in its popular line of SELF-SCAN® gas plasma displays: *microprocessor-control and memory!* This means big savings plus the greatest operating and packaging flexibility *ever* in the flat panel display of alphanumeric information.

Your engineers will "light-up", too, as they discover operating advantages unmatched by any display. The new SELF-SCAN II displays are bright, crisp, easy-to-read. And, with Burroughs' unique new simplified control circuitry, the display panel — complete with electronics — is less than 2" thin for easy installation in compact designs.

The display's built-in microprocessor memory and control eliminate the need for you to design, develop and build circuitry to effect display operation. Just feed in appropriate 8-bit signals for the characters and control commands and you're in operation. Large system manufacturers save 95% of the engineering and development time formerly required and small system producers can now use displays since "design-in" cost is no longer a significant factor.

Adapting the Burroughs displays to your needs is as easy as a change in software. Their operation can be tailored for any product and changed for others with different display requirements.

The display subsystem operates off an 8-bit bi-directional buss or a TTL buss. Data can be entered at rates up to 1 MHz. and, with the addition of a keyboard and communication interface, it becomes a low-cost, compact data terminal!

The system's edit and control routine allows insertion, deletion and blinking of letters or lines, increasing or decreasing brightness, right-to-left data entry, etc.

Light up your customers and your engineers. And lighten your costs with Burroughs SELF-SCAN II microprocessor-controlled displays. For a copy of our SELF-SCAN Subsystems Brochure, write Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Plainfield, New Jersey 07061 or call (201) 757-5000. Overseas, contact Burroughs ECD International, Buckingham House, The Broadway, Stanmore, Middlesex, England.

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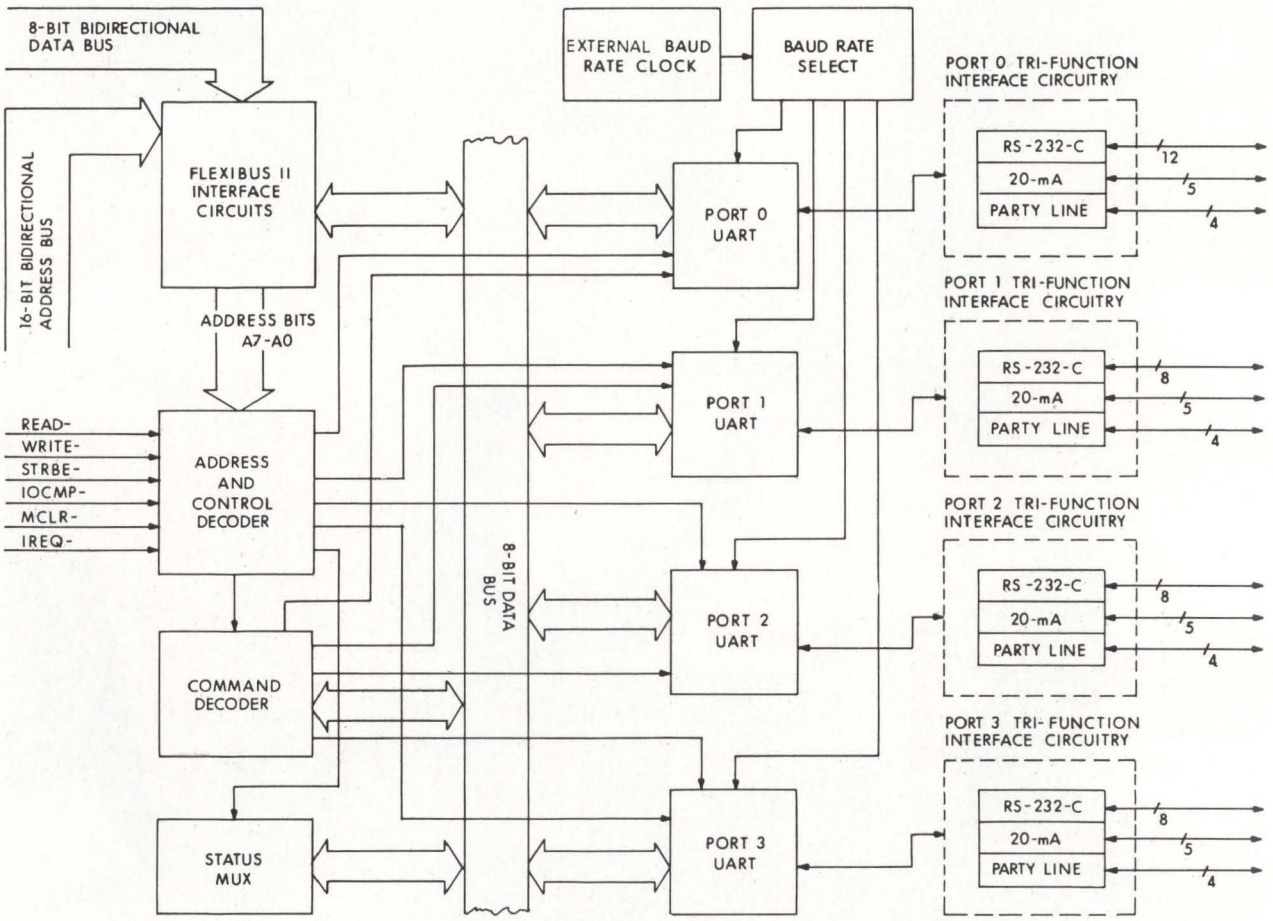

Quad serial module 1860 features RS-232-C, 20-mA current loop, and party line compatible interface circuitry for each serial port, selection of which is accomplished by connecting external device to specific pins provided on each user serial port connector. Port 0 is major modem compatible and ports 1, 2, and 3 are minor modem compatible. Up to 32 satellite microcomputer systems (remoted up to 1000 ft, 305 m from host) may be interfaced to host system via module

Each port allows independent software programmable options including parity bit generation and checking, odd, even, or no parity. Interrupt or polled operation may be selected by user software commands to the interrupt controller. Port interrupts, processed by the interrupt controller, operate in one of four modes: fully nested, rotating priority, maskable, and polled.

Interface circuitry providing RS-232-C serial communications is provided on each of four ports; circuitry for 20-mA current loop compatibility is identical for all ports. A high level digital output per serial port is provided for controlling a TTY paper tape reader. Party line operation may also be selected for each serial port, for distributed systems interfacing.

Circle 171 on Inquiry Card

Programmable μComputer Analog I/O System Cuts Development Time

Electrically and mechanically plug-compatible with Motorola Micromodule and EXORciser microcomputer systems, the MP7400 is a low cost 8-bit analog I/O system containing both input and output on a single board. Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734 has accommodated up to 64 single-ended or 32 differential input channels, and two output channels on each board, functioning as analog data acquisition and analog output systems, respectively.

The input portion includes an analog multiplexer, high gain instrumentation amplifier, 8-bit ADC, plus

Our new mini/micro computer printers... "the easy ones."

Features:

- Three popular ASCII input configurations
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EASY TO USE

A time-proven, dot matrix impact printing element can print 64 alpha-numeric and special symbols in 40 characters/line at 50 CPS on single or multiple-copy paper rolls. Options such as Tally Roll take-up and Fast Paper Feed, make the printers easy to fit point-of-sale and related fields.

Combining form and function, the modern package blends with virtually any surroundings, while its flip-top design allows convenient access for paper replacement and servicing.

EASY ON BUDGETS

Best of all, single-unit prices for the DP-1000 Series start at under $700, with substantial Dealer and OEM quantity discounts.

Want to see a demonstration in your office, or more details? That's easy too. Just contact Ken Mathews at Anadex; 9825 DeSoto Avenue; Chatsworth, CA 91311; Telephone (213) 998-8010; TWX 910-494-2761.

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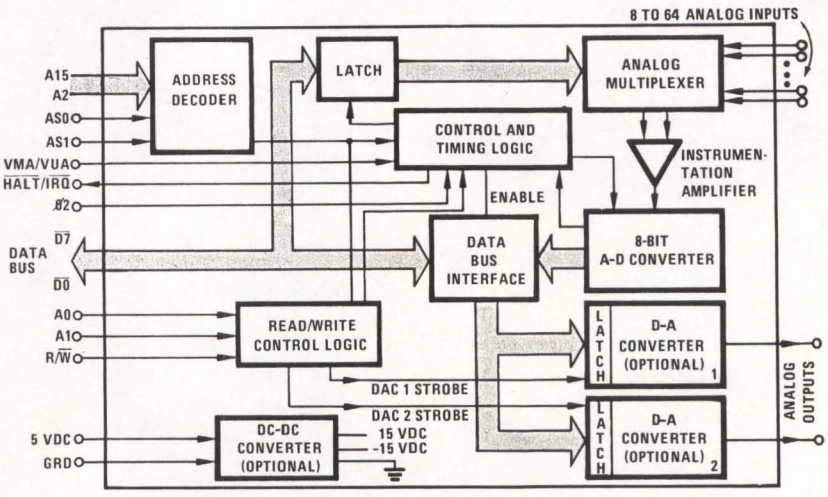

Components in block diagram comprise Burr-Brown's MP7400 analog I/O system for Motorola Micromodule and EXORciser. It serves to digitize low or high level analog signals. Single-board system is treated as memory input or output by CPU

timing, decoding, and control logic. The amplifier handles input levels as low as 10 mV FS allowing direct connection to low level inputs such as thermocouples.

Two 8-bit DACs with input latches and control logic comprise the output portion. A dc-dc converter is available for operation from the computer's 5-Vdc power supply.

Simplifying software implementation, the system interfaces to the microcomputer as memory. Any memory instruction can be used to access or write data. Memory mapped operation allows it to be used with or without halting the CPU, or in interrupt mode.

Input voltage range is ±10 mV to ±5 V, input overvoltage protection is ±15 V, and input throughput accuracy is better than ±0.4% FSR on the ±5-V range. Output voltage range is strap selectable with five ranges to ±10 V at 5 mA. Output throughput accuracy is better than ±0.4%.

Circle 172 on Inquiry Card

Software is Efficient Memory and Real-Time Management System

A fast multitasking, multiuser, real-time operating system for 8080 and Z80 microcomputers, FAMOS™ is an efficient management system which maintains dynamic, noncontiguous disc files; dynamic memory and program allocation; and extensive application of disc buffering in system functions and in the compiler. It supports more than 25 interactive terminals, in-house and remotely.

Multisessioning capability allows one terminal to perform as many tasks concurrently as memory will allow. MVT Microcomputer Systems, Inc, 21822 Sherman Way, Canoga Park, CA 91303 has also extended dynamic resource management to programs, file space, and buffers. System operates with 8k MVT-BASIC™ compiler.

Circle 173 on Inquiry Card

Input/Output Card Programs EPROMs for All Microcomputers

Working with microcomputers having 5-V I/O ports, the EP-2A EPROM programmer needs 1½ I/O ports and 256 bytes of microcomputer memory. Power requirements for the 2.2 x 4.3" (5.6 x 10.9-cm) card from Optimal Technology, Inc, Blue Wood 127, Earlysville, VA 22936 are 5, −5, 12, and 28 V with a maximum current of 150 mA for any voltage.

Software on paper tape is available for the Fairchild F8 kit #1 and Motorola MC6800 D1 evaluation card. A software listing is also available for the D2 evaluation card. A program p/ROM routine and verify routine comprise the software.

Circuit provisions include a 25-V regulator, 20-mA programming current limiter, and address counter. Jumpers added at the board connector permit programming of the Intel 2716 EPROM with no software changes.

Circle 174 on Inquiry Card

Dual Floppy Disc Option Is Available for 12-Bit μComputer System

A dual floppy disc module interfaces the PCM-12 microcomputer system to Data Systems Design's model 210 floppy disc memory system. Fully plug-compatible with that model, the 12440 module from Pacific Cyber/Metrix, Inc, 3120 Crow Canyon Rd, San Ramon, CA 94583 allows users of the company's PCM-12 (see *Computer Design*, May 1976, p 210) to execute all PDP-8 floppy disc diagnostics, and makes it compatible with mass storage operating systems designed for the PDP-8 minicomputers.

Circle 175 on Inquiry Card

Microprocessor Lab Facilitates Development of μProgrammed System

Microprogrammed systems, regardless of their architecture, can be prototyped and programmed with the microprocessor-based System 29, which includes a CRT console and dual-drive floppy disc configured and programmed for this purpose. The development system is a complete prototyping setup that can be used to develop hardware and firmware designs, and then check out the prototype design.

Introduced by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086, the basic system consists of a mainframe with two separate systems in one package. A support processor includes an Am-

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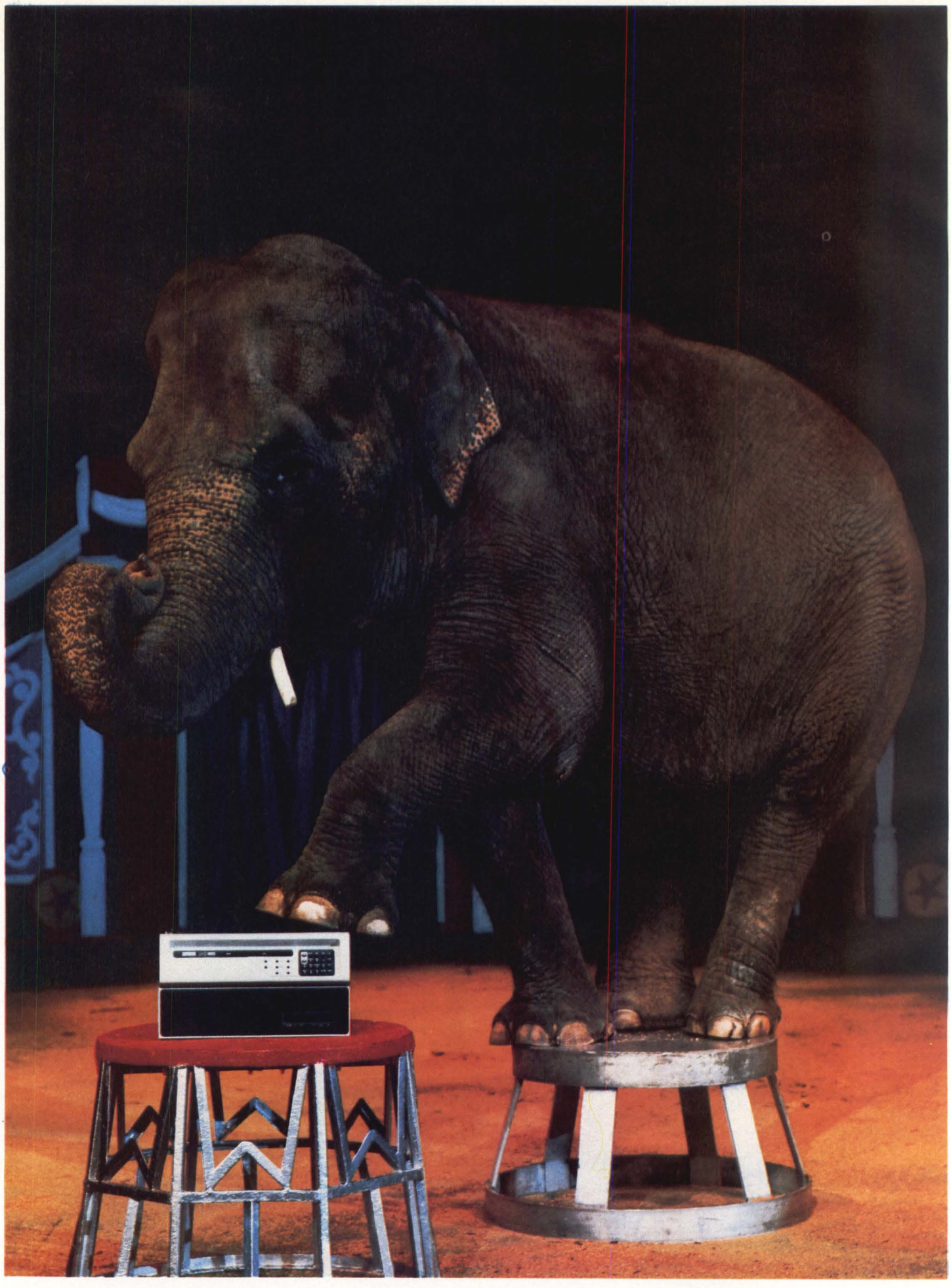

Digital announces a PDP-8 with an enormous memory.

Something big has just happened to the world's most famous small computer. In fact, something enormous.

Digital has just put 128K of memory into the PDP-8.

This act is brought to you by a powerful new memory management option called KT8-A. And by two new MOS memory modules that fit large amounts of memory into small amounts of space. Simply by adding these 16K or 32K modules in whatever combination you choose, you now expand your PDP-8/A into something bigger. What's even better, you can mix MOS and core. And that means you can protect your program in non-volatile core while you expand your data base in MOS.

And thanks to the KT8-A all this memory is under new management. Not only does the KT8-A let you address up to 128K words of memory, but it also offers you memory relocation and memory protection, while asking little in operating system overhead so you get faster system performance.

What's the cost of these enormous advancements? That's the next attraction.

The new PDP-8A MOS memory models are available at prices that are as crowd-pleasing as their performance. For a 16K 8A205 you'll pay as little as $3900 (quan. 1). 8A425 with 64K is as low as $11,000. And the top of the line 8A625 with 128K is yours for as little as $18,050.

They're the new big-memory Eights from Digital. Step right up.

Large memories aren't our only new trick.

New hardware and software improvements are also in the PDP-8 spotlight.

The VK8-A is a new low cost PDP-8A option that provides high quality video output plus keyboard and printer interfaces. Video character generation uses a super-sharp 9x9 dot matrix for high resolution on single or multiple CRT monitors up to one thousand feet away.

Also new for PDP-8 users is MACREL/LINKER—a sophisticated assembler with MACRO facilities that lets you implement, expand and update your system faster while reducing software development time.

And last but not least there's DECNET 8—a series of software protocols that let you form your own PDP-8 network.

The PDP-8. Bigger. Smaller. And better than ever.

A short while ago, we made big news with DECstation 78. A low-end system that set new highs for ease of use and simplicity.

Now we're expanding the PDP-8 family up, as well as down, and that means new opportunities for OEMs and end-users alike. Look into what's happening with PDP-8s. Call your nearest Digital sales office today.

Or send the coupon to PDP-8 Marketing Communications, Digital Equipment Corporation, 129 Parker Street, PK3-1/M34, Maynard, Massachusetts 01754. European headquarters: 12, av. des Morgines, 1213 Petit-Lancy/Geneva. In Canada: Digital Equipment of Canada, Ltd.

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Digital Equipment Corporation, 129 Parker Street, PK3-1/M34,
Maynard, MA 01754
Please send additional information about the PDP-8 family.

Name _____ Title _____

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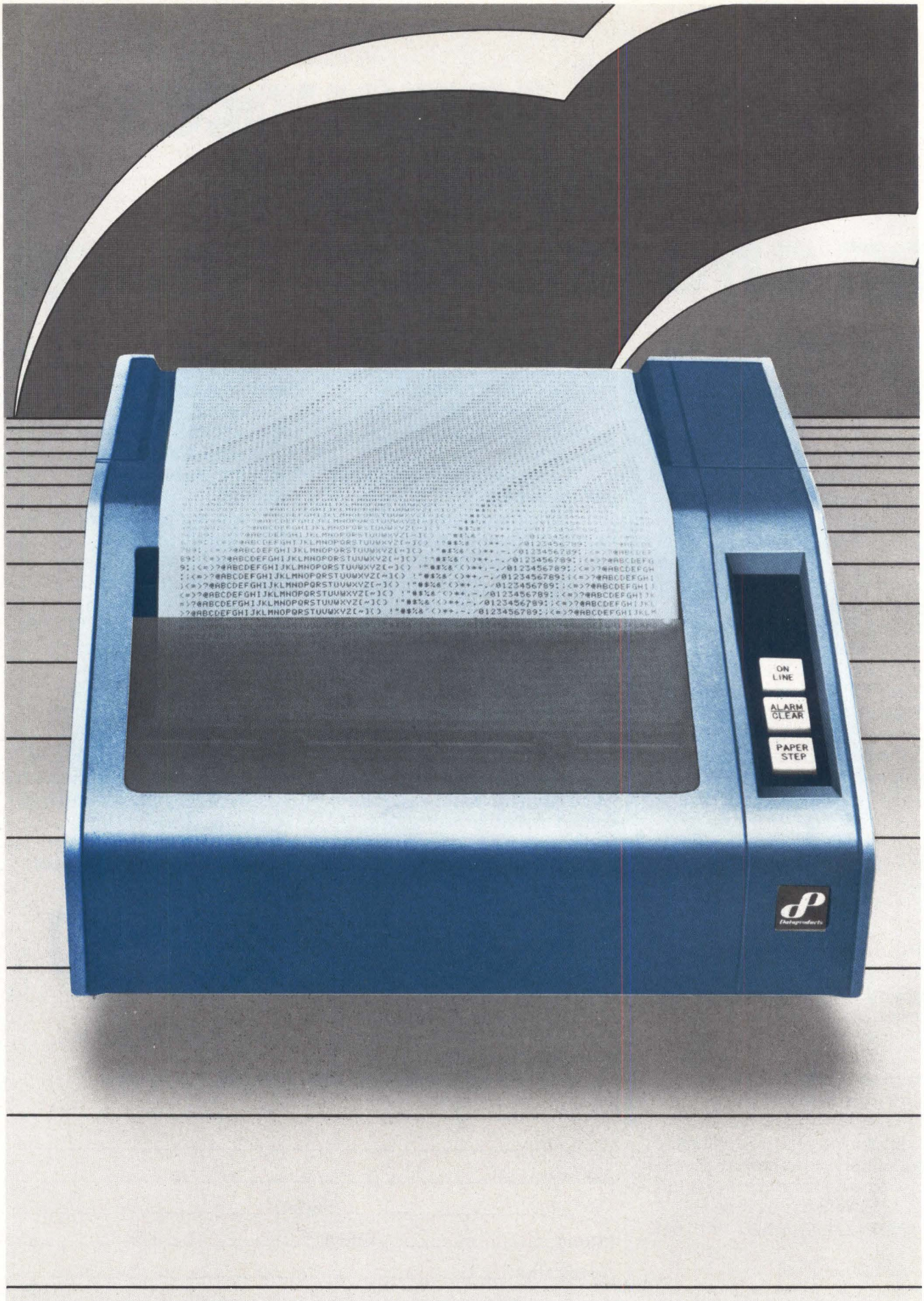
Phone _____ OEM _____ End-User _____

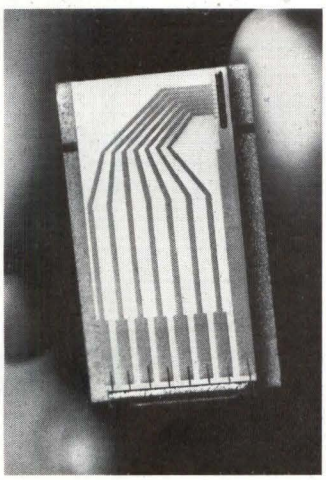
Application _____

CD127


ON LINE
ALARM CLEAR
PAPER STEP
Dataproducts

DATAPRODUCTS' NEW ERA T-80 THERMAL PRINTER:

80 CPS FOR THE PRICE OF 30.



Dataproducts' New Era T-80 thermal printer is nearly three times faster than other thermal printers.

Yet it costs about the same.

What's more, the T-80 offers you Dataproducts dependability, assured by a smartly conservative design, a unique solid-state print head, and a minimum of moving parts.

Noise, too, has been minimized.

The quiet T-80 hums at 80 cps, so it can be seen but barely heard.

And head changing is a snap.

Any operator can put in one of our incredibly small, self-cooling heads in a snappy 10 seconds.

Our New Era T-80 thermal printer, with its parallel or optional RS-232-C interface, is ready to tie into your CRT, your terminal, or your processor.

The T-80: fast, inexpensive, quiet, and reliable.

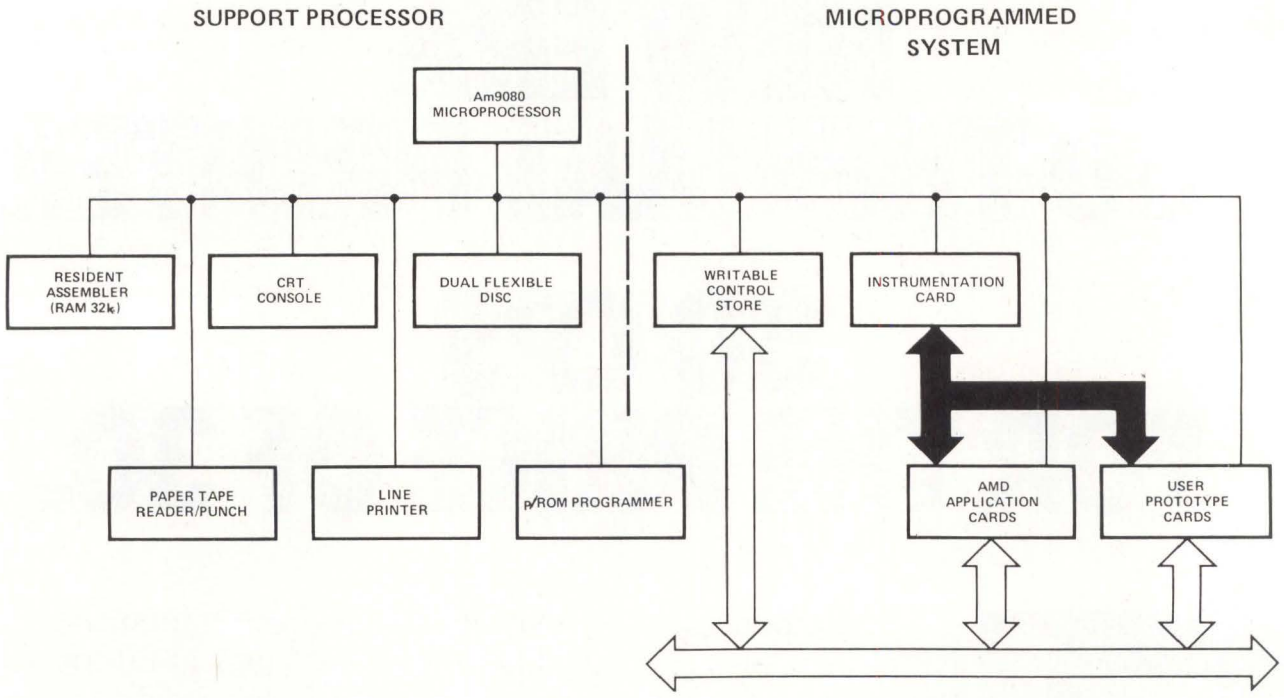
Altogether, an unbeatable combination.

Dataproducts

THE PRINTER COMPANY

NORTH AMERICAN SALES HQ: 6219 De Soto Avenue, Woodland Hills, CA 91365, (213) 887-8451; Telex 69-8492.
EUROPEAN SALES HQ: Darmstaedter Landstrasse 199, Frankfurt, W. Germany, Phone 681034; Telex 841-416344.

CIRCLE 51 ON INQUIRY CARD



Support processor of System 29 is configured and programmed to support a microprogrammed system. Advanced Micro Devices has incorporated facilities of an interactive editing system for building microcode definition and source files, a microprogram assembler for assembling microcodes, and prototype checkout workstation for debugging hardware designs

9080A CPU card; 32k-byte memory card, expandable to 64k; four RS-232 serial ports; a parallel port; and power supply. The microprogrammed system has one writable control store card of 2k x 64 bits; an instrumentation card; computer control unit application card; five slots for user cards; and a power supply of 5 V, 25 A (50 A optional).

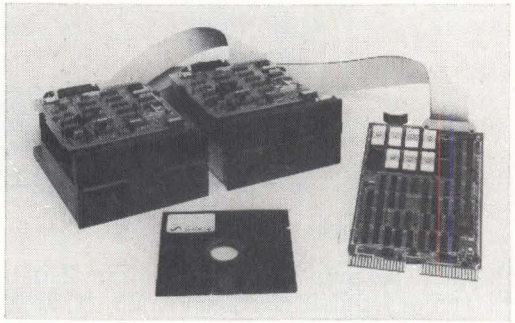
Available facilities are an interactive editing system, resident microprogram assembler, and prototype checkout workstation. Universal prototyping cards allow prototyping within or outside of the system's structure. Software includes various microprogram aids, disc operating systems, and programs.

Circle 176 on Inquiry Card

LSI-11 Controls Minidisc Drives Through Interface Board

The MDC-11 multifunction controller allows up to three Shugart SA-400 minidisc drives [5¼" (13.3-cm) format] to be controlled by an LSI-11 computer system. Being produced by Andromeda Systems, 14701 Arminta St #J, Panorama City, CA 91402, the interface board provides a DMA dynamic memory refresh controller, minidisc controller, and sockets for up to 4096 16-bit words of EPROM. The single dual-width card containing these functions plugs into the LSI-11 Q-bus, using standard voltages (5 and 12 V).

Minidisc controller controls the drives via programmed command and



Physical configuration of dual-drive minidisc controller from Andromeda Systems shows SA-400 drives connected to MDC-11 board via controller cable. Mini-floppy diskette is shown in front. Three useful functions of LSI-11 compatible interface are divided into minidisc controller, DMA dynamic memory refresh controller, and 4k x 16 EPROM area

Now-Remote Printing and Plotting: $8180!*

You could pay more for a printer alone. But now you can have remote print stations with plotting capability . . . for no extra cost. A new opportunity that should interest you . . . more than remotely.

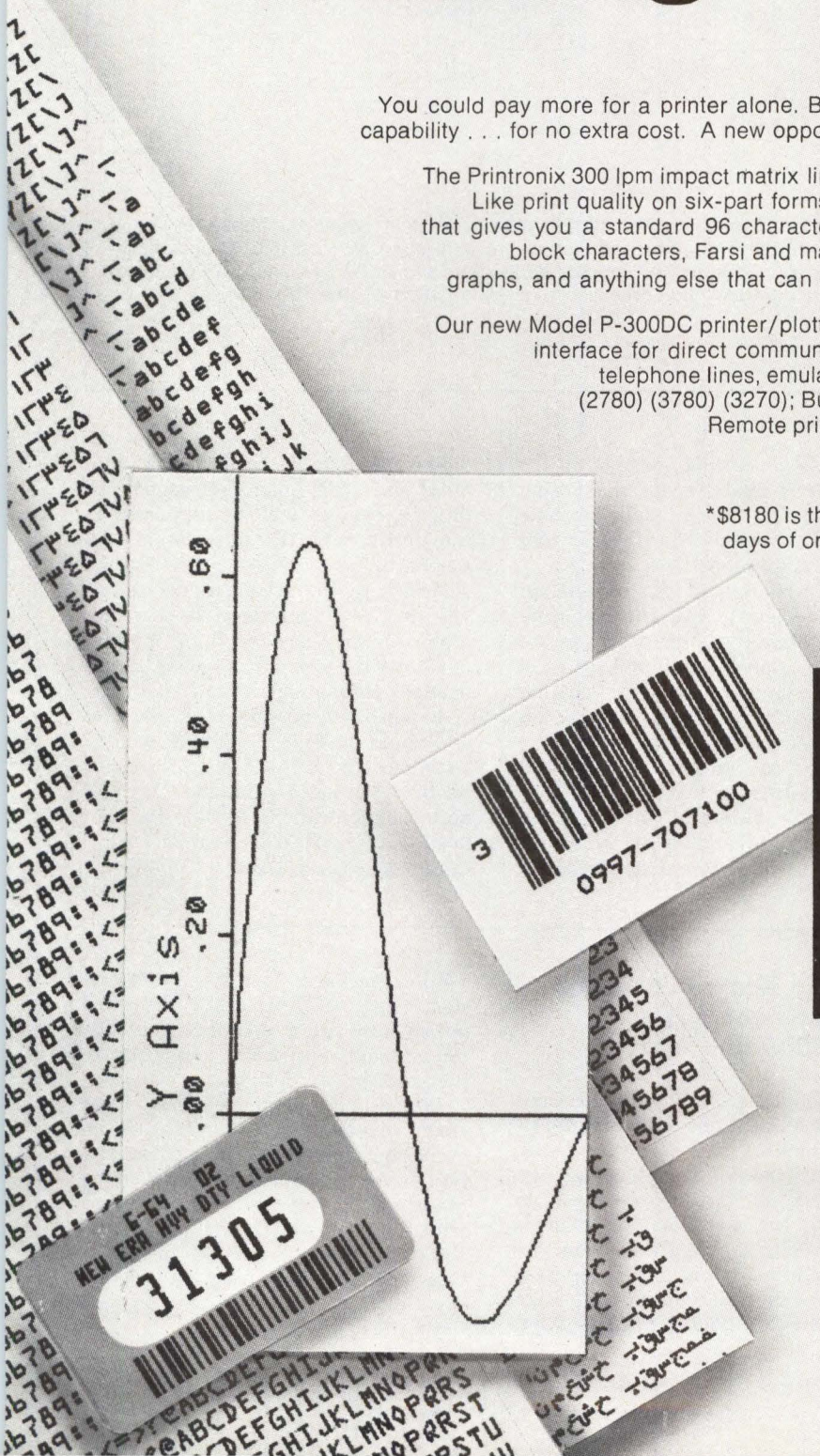
The Printronix 300 lpm impact matrix line printer is the one that offers you several advantages. Like print quality on six-part forms other printers can't match. Or a 160 character capacity that gives you a standard 96 character set plus another 64 characters, such as OCR-A, large block characters, Farsi and many others. And the capability to plot bar codes, charts, graphs, and anything else that can be displayed on a CRT . . . at the price of a printer alone.

Our new Model P-300DC printer/plotter has an integral microprocessor data communication interface for direct communication with your host computer over switched or private telephone lines, emulating any one of the following line protocols: IBM BISYNC (2780) (3780) (3270); Burroughs; Honeywell (VIP-7700); or UNIVAC (DCT-1000). Remote printing. Remote plotting. Anywhere. Anytime. For $8180.

If you order one today, we'll ship it tomorrow.

*$8180 is the domestic U.S. price, which includes installation and 90 days of on-site service. No "extra" costs. Just extra performance.

Printronix, Inc., 17421 Derian, Irvine, California 92714.
Call us at (714) 549-8272.



PRINTRONIX...

More than a remote possibility!

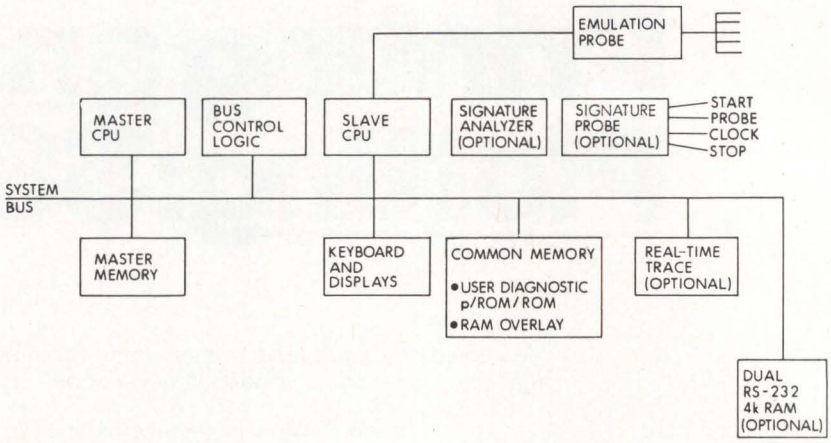
CIRCLE 52 ON INQUIRY CARD

data transfer. It automatically performs track seek and verify, 16-bit CRCC generation and checking, and drive motor timeout shutoff. In addition to data R/W capability, the board also formats the minidiskettes.

The DMA dynamic memory refresh controller, available separately, allows the user to disable the CPU microcode controlled refresh function. The EPROM section, accommodating up to 4k words of 2708-type or 8k words of 2716-type chips, permits critical software and data to reside in nonvolatile memory. It generates its own −5 V in an onboard inverter.

The EPROM may be addressed at any 4k or 8k increment. Also, standard LSI-11 bootstrap addresses may be mapped into the EPROM chips no matter where they are addressed. Several variations of the controller are offered.

Circle 177 on Inquiry Card



Millennium Systems' μSA instrument features dual system architecture. Functions related to operator interaction are controlled by master CPU and those related to unit under test are controlled by slave CPU. This enables system to support different microprocessors by substitution of one CPU card

Advanced Diagnostic Techniques Form Basis of Microprocessor Analyzer

Designed primarily for field maintenance use as well as production and depot use, the MicroSystem Analyzer (μSA) combines two advanced diagnostic techniques—signature analysis and in-circuit emulation—to locate faults in microprocessor-based products. In-circuit emulation, implemented by connecting an umbilical cord from the analyzer to the unit's microprocessor socket, exercises the DUT in a precise, repeatable way. As the signal generating portion of the design, it is effective for diagnosing system faults at the module or function level. Functional testing can also be done on an inoperable unit.

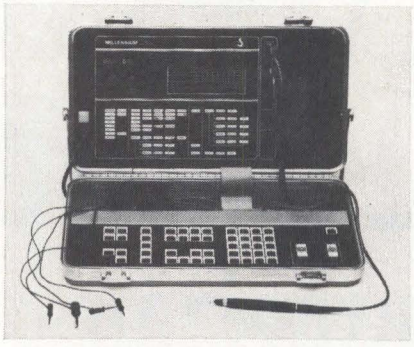
Troubleshooting at the component level is achieved with the signature analysis option that provides signature probe, additional function keys, and signature analysis board. Locating faults by probing test nodes, this method causes a defined stimulus to be applied to the system under test and then observes the signatures.

Universal design of the tool, developed by Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014, permits it to be used with 8080 and 6800 microprocessors. Additional devices will be supported in the future, with the substitution of a CPU card.

Access to the system under test is via the keyboard and 20-character alphanumeric display. Both are under software control, allowing modification through program changes.

Expansion is possible with space for additional modules. Options include real-time trace of 128 transactions of 32 bits relative to a designated event, and communications module for connection to an RS-232 modem.

Circle 178 on Inquiry Card



Portable MicroSystem Analyzer contains all facilities required to monitor and control fault isolation process in a 6800 or 8080 microprocessor-based system under test. Signature analysis and in-circuit emulation combine to provide capabilities that are more powerful than those of either approach used alone

Multiple Microprocessor Development System Adds 8085 Support

With complete 8085 software and hardware emulation, software development support, and hardware debug capability, the 8085 option for the 8000 series microprocessor labs from Tektronix, Inc, PO Box 500, Beaverton, OR 97077 extends coverage of this multiple-approach development aid to another microprocessor. Like the other 8080, 6800, Z80, and 9900 support packages (see *Computer Design*, April 1977, p 120), the 8085 option runs as a component of the total system approach to easing microprocessor-based designs.

Integration sequence has three stages involving emulation of program execution; debugging using the prototype's I/O and clock; and verification of normal operations by the prototype with the prototype control probe substituted for the emulated microprocessor. A real-time trace and debug capability is optional.

Circle 179 on Inquiry Card

Microcomputer Offers Multiple Function Capabilities on One Card

A one-card microcomputer for the F8™ based systems, the OCM/1 operates as a standalone board for low volume production, real-time emulation of pilot production, and field testing, or as a low cost development system using a teletypewriter or keyboard display. The board, introduced by the Instruments and Controls Div of Fairchild Camera and Instrument Corp, 1725 Technology Dr, San Jose, CA 95110, consists of a processor, memory, I/O, and interrupt. Standard configuration incorporates two interrupts and two timers.

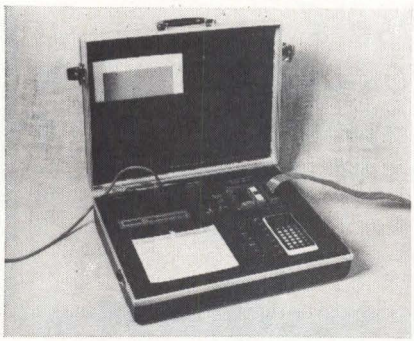
The processor includes 3850 CPU, 3853 static memory interface, clock generation, and reset circuitry. Contained onboard are 1k bytes of RAM for permanent storage; sockets will hold 2k bytes of EROM and 2k bytes of fusible-link p/ROM. The program storage unit (PSU) contains the FAIRBUG resident monitor for debugging.

I/O consists of the 3850 CPU and 3851 PSU, each with two 8-bit I/O ports. Two sockets allow two more PIO devices for four additional I/O ports. A circuit allows additional I/O capability of communicating with a teletypewriter, RS-232 device, or 20-mA current loop. An alternate PSU is available separately for low cost I/O.

Circle 180 on Inquiry Card

Micromonitor Provides In-Circuit Hardware/ Software Debugging

COSMAC Micromonitor CDP 18S030 pemits in-circuit debugging of any CDP1802 microprocessor system hardware and software in real time. Available from RCA Solid State Div, Rte 202, Somerville, NJ 08876, the tool is housed in an attache case containing built-in keyboard, display, and status indicator lights, as well as software debugging routines. A self-test card simulates a user system to verify and assure the monitor's operation.



Controlled by a built-in microprocessor, the unit uses the 1802 CPU, power supply, clock, and memory of the test system to run a user program. Operation is either from the keyboard or from an external terminal if a hardcopy record is desired. Three modes are available for running programs.

Circle 181 on Inquiry Card

Microcomputer for OEMs Features Simple Analysis and Troubleshooting

The M68-MBC microcomputer system for OEMS consists of a hexadecimal keyboard, 6-digit hexadecimal display, monitor program, general-purpose board, and 4-slot motherboard. Mounting frame with brackets for front, back, side, or 19" (48-cm) rack panel mounting accepts three peripheral boards. Main computer board accepts up to 768 words of RAM, 2.5k p/ROM with optional p/ROM adapter, and TTY/CRT/cassette interface. Electronic Product Associates, Inc, 1157 Vega St, San Diego, CA 92110 provides onboard monitor program.

Circle 182 on Inquiry Card

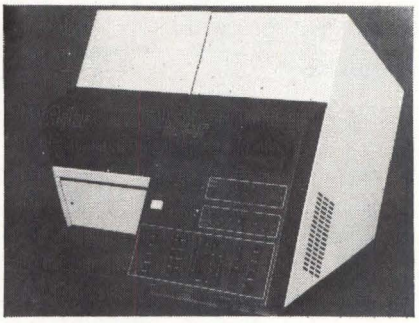
Expandable, Assembled µComputer Features Upward Compatibility

Typical configuration of the Xycon III microcomputer from Computer Systems Unlimited, 25903 Peterman Ave, Hayward, CA 94545 consists of a 1.3-μs 8085 process card with master/slave capabilities, built-in RS-232/TTY port, real-time clock, and eight level interrupts. Other components include a 32k RAM, 63-key u/lc keyboard with numeric keypad, and 24 x 80 CRT. The expandable system is compatible with a variety of peripherals. System software is also available.

Circle 183 on Inquiry Card

System for Peripherals and µProcessors Operates With Test Packages

Testing of microprocessors, microprocessor support chips, ROMS, and RAMS takes a different approach with the MX-17 microprocessor family test system introduced by Adar Associates,



Inc, 11B North Ave, Burlington, MA 01803. A "conditioned natural environment" is used so that the logic sequence, through which the DUT is exercised, is written in the language of the microprocessor itself.

The user retains full programmable control over all test variables, including logic levels, bias voltages, all timing edge placement, and formatting of data, addresses, and clocks. System operating modes include basic go/no-go testing and sorting into bins.

Turnkey test packages for 8080A, 6800, Z80, and 8085 microprocessors as well as peripheral devices enable testing by simply loading the package into the system. Elements include a program cassette with complete logic sequence and test conditions, device programming unit which configures the system to test the device, a device board wired to the pinout of the DUT, and documentation package.

Circle 184 on Inquiry Card

Expansion Card Adds High Speed I/O to Computer Series

Series/80 board level computers based on the 8080 microprocessor have been expanded with the addition of the BLC 508 I/O expansion card, which connects to the system bus through the 86-pin card edge, and has a 100-pin edge connector for parallel I/O. The 8-bit parallel ports—four input

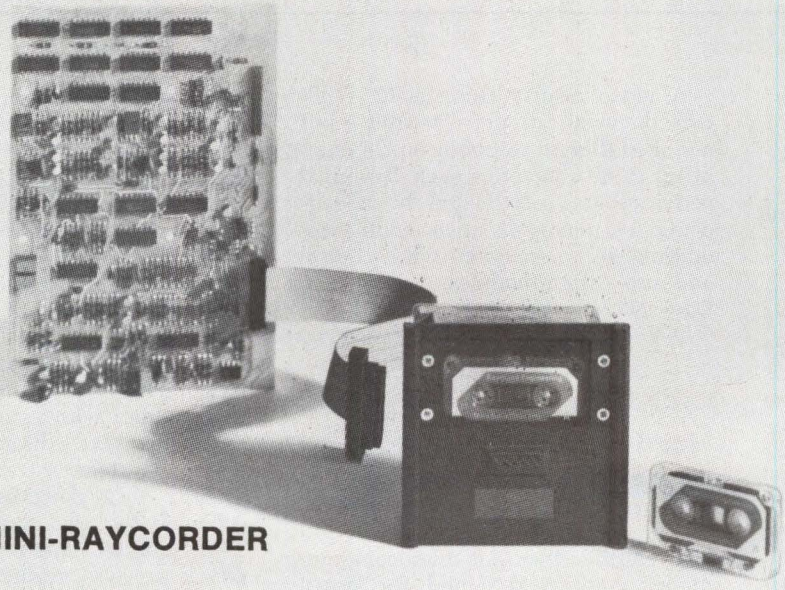
One of the Finest New OEM Products For the Computer Industry . . .

now even better

Though it looks the same on the outside, today's Mini-Raycorder incorporates many improvements which make it even more reliable, easier to use and better performing than the original design. The Model 6409 Mini-Raycorder, which scored such a resounding success as the world's first tape recorder for ANSI proposed standard Mini-Data Cassettes, is now impossible to beat.

Check these new features for yourself:

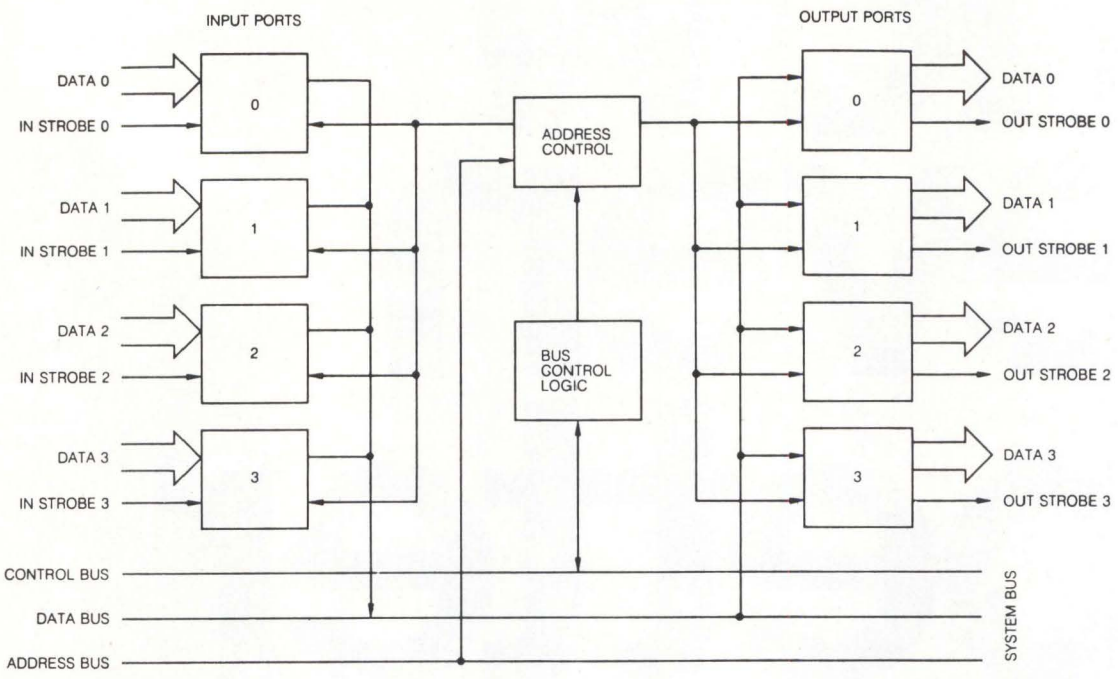
Ball-bearing motor for improved reliability
New servo design for better tape handling
Full bi-directional operation available
Optional connector configurations available for easy interfacing
Improved cassette insertion and removal



THE MINI-RAYCORDER

CIRCLE 56 ON INQUIRY CARD

Raycorder Products Division **RAYMOND ENGINEERING INC.**, 217 Smith Street, Middletown, Connecticut 06457
a subsidiary of Raymond Precision Industries



Block of port addresses of National Semiconductor's I/O expansion card is set by two rotating switches to one of 64 possible base addresses, and can be switch disabled. Output ports have variable width strobe, selectable from 100 to 1600 ns

and four output with variable width strobe for peripherals—have data transfer rates as high as 1.3M bytes/port.

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has designed all data, address, and control signals to be TTL-compatible. Operating on 5 Vdc, board accepts eight external interrupt requests which are buffered and passed onto the system bus.

Display Terminal Communicates With EXORciser System

Hardware and software development power of the M68SDT EXORciser are increased by the EXORterm 100, announced by Motorola Semiconductor Products, Inc, Microsystems Div, PO Box 20912, Phoenix, AZ 85036 as the first of a series of display terminals for the EXORciser development system. Communications between the two devices takes place via a detachable keyboard and RS-232-C serial communications link at manually selectable rates from 110 to 9600 bits/s. Keyboard contains 12 special encoded function keys plus standard teletypewriter terminal keys.

A video display using a 12″ (30-cm) diagonal CRT presents user input and EXORciser response on 24 lines of up to 80 characters each. Terminal activities are coordinated by a self-contained micro-executive module operating in conjunction with control and application modules.

Circle 185 on Inquiry Card

Hardware, Firmware, and Software Features Enhance Microcomputer

The versatile modular microcomputer model 2000 is designed for OEMS, with maximum access to registers, interrupts, and system diagnostics. Astral Computer Co, 991 Commercial St, Palo Alto, CA 94303 has based the computer on the 6800 microprocessor. It is available as a standalone single-board computer or in one of two enclosures complete with power supplies and 12-position motherboard.

Separate 10 x 4.5″ (25.4 x 11.4-cm) cards contain the processor, memory (8k RAM, 8k EPROM, or both), I/O, and floppy disc interface. System is supported with extended 8k BASIC, assembler, text editor, and disc operating system software. Firmware consists of a powerful monitor that occupies the two available p/ROMS. Two separate interchangeable front panels are also available. □

Circle 186 on Inquiry Card

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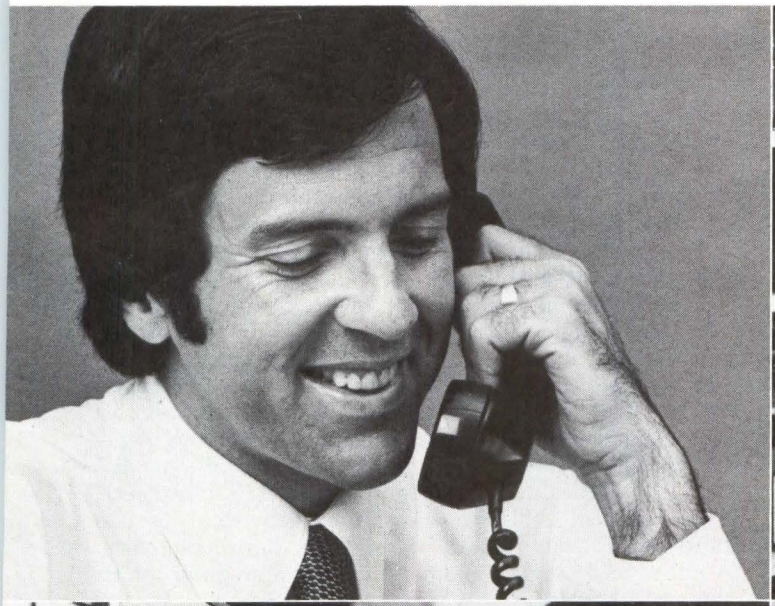

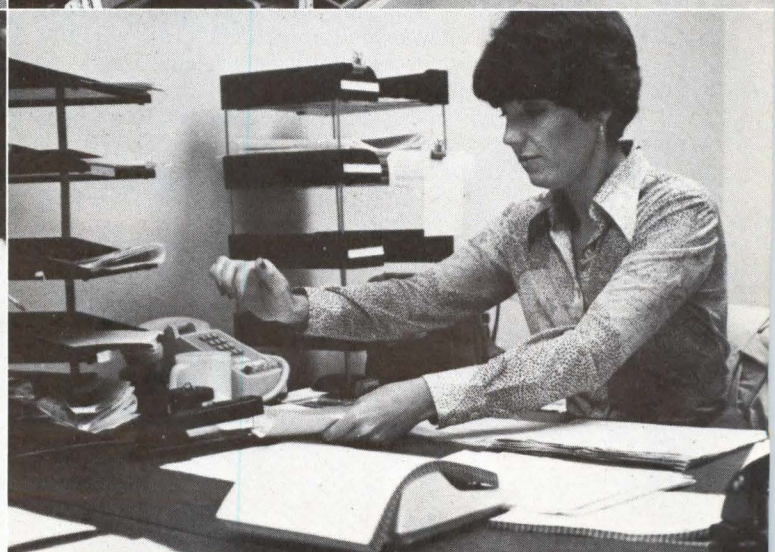

Charge-Transfer Devices
Part 2: CCD Memories

Eric R. Garen

Integrated Computer Systems, Inc
Culver City, California

The first in this series of three columns dealt with the principle of operation of the three basic charge-transfer technologies—charge-coupled, bucket-brigade, and charge-injection devices. This second column describes some early charge-coupled device memories and systems and emphasizes the characteristics of two new chips with 64k-bit capacity from Fairchild Semiconductor and Texas Instruments.

Charge-coupled device (CCD) digital memories of course have been available for several years. Although early introductions included the Fairchild 9k-bit CCD 450 and 16k CCD 460 as well as the Intel 16k 2416,* these chips have seen relatively limited use. Because of their basically serial organization, they are obvious alternatives to disc and drum memory. However, these early CCD devices are generally economical only for requirements of less than 1M byte; in such small sizes, the high fixed cost of the mechanical drive system makes disc more expensive. Above 1M byte, even fixed-head discs are more economical.

The primary advantage of these first CCDs was access time rather than cost. CCD access times of 250 to 1000 μs were far more attractive than the 8 to 10 ms of disc or drum for applications such as "memory swapping" in timeshare systems. In addition, there was improved reliability and error rates. CCD memories equipped with even single-bit error correction encoding and decoding circuitry exhibit rates of 1 error per 10^{13} operations, and recent Fairchild data show the same rate with no error correction.

Within the last year significant advances have been made in CCD technology. Both Fairchild and Texas Instruments have been sampling 64k CCD memories for several months, and both expect to be in full-scale production by the publication date of this column. These 64k chips are so much more economical than the earlier 9k and 16k versions that the earlier chips are now virtually obsoleted for disc and drum replacement applications.

Fairchild's CCD 464 and Texas Instruments' TMS-3064 64k chips have the same structure from the user's point of view. Essentially, they are organized internally as 16 addressable 4k-bit shift registers. Each chip has one data input line and one data output line (Fig 1) which can be selectively multiplexed to any of the 16 internal shift registers. The multiplexer is controlled by four address lines. Each of the 16 registers normally recirculates its data except during a write operation. In a write operation, data from the input line are written into the selected register while the other 15 registers are recirculated.

Both chips are rated at a maximum transfer rate of 5 MHz. Thus the maximum latency time (the time to read out any desired bit) is about 800 μs (4095 shifts at 5 MHz) and the average access time is 400 μs. The 16 x 4k organization was chosen to achieve a latency 16 times less than the latency of a straightforward 1 x 64k organization.

While each of the internal registers appears to the user as a single 1 x 4k shift register, in actuality it is organized in a serial-parallel-serial format (Fig 2). For example, each of the registers in the TMS-3064 inputs data into a "horizontal" 32-bit input register clocked at the 5-MHz rate. After 32 clocks, this register is full and the 32 bits are shifted in parallel into 32 "vertical" shift registers (each 126 bits long). These vertical registers are shifted downward at one thirty-second the rate of the 5-MHz horizontal clock. At the final stage, another horizontal register shifts the bits out in series at 5 MHz.

This serial-parallel-serial structure has several advantages. First and foremost, it requires far less power than a single 1 x 4k register since the vast majority of the bits are shifted through the vertical registers at slow speed. Because power consumption is proportional to frequency, this organization is vastly superior to a 1 x 4k register in which all bits would shift at high speed. The second major advantage of this structure is that each bit is transferred only 160 times (128 vertical and 32 horizontal transfers). Thus the

*H. R. Crouch, J. B. Cornett, Jr, and R. S. Eward, "CCDs in Memory Systems Move Into Sight," *Computer Design*, Sept 1976, pp 75-80

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It can save time; no time-fill characters needed, even at 9600 bits per second.

It offers cursor positioning by—and reporting to—the host computer. And, of course, it can store forms locally and automatically check formats.

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Etc., etc., etc.

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Check what you look for in an off-line switcher	. . . and check what our new OLS Model 10 gives you.	Check what you look for in an off-line switcher	. . . and check what our new OLS Model 10 gives you.
☐ Brown-out protection	50 ms hold-up of output voltages at full load and V_{in} nominal.	☐ Synchronized outputs	All outputs are synchronously clocked to a 20 kHz switching frequency.
☐ High efficiency	70% typical, 65% min. at full load and V_{in} nominal.	☐ Short-circuit protection	Foldback (adjustable).
☐ High reliability	Conservative design with safe areas considered.	☐ Overvoltage protection	V_{out} +10% to 20%.
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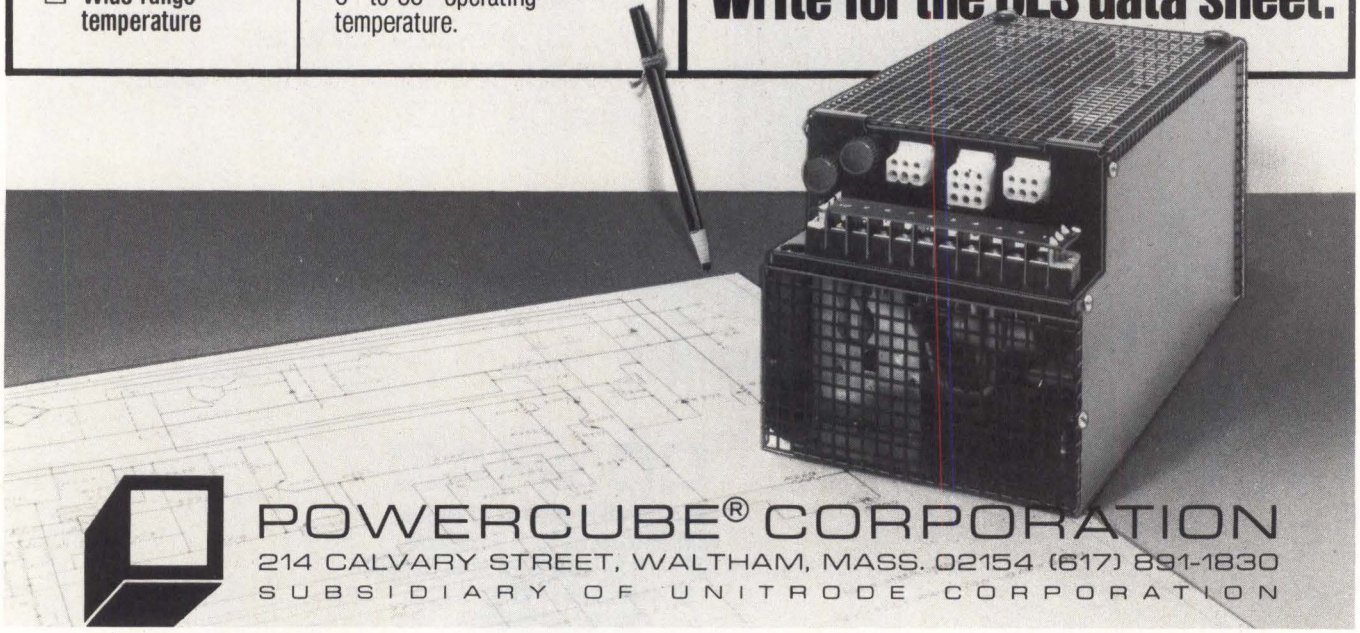
☐ Input line filtering	EMI line filter standard. Meets VDE and other domestic and international requirements.	☐ Adjustable outputs	5 V nominal, 4.8 to 5.3; +/−12 V nominal. 11.5 to 12.5 (+/−15 V also available).
☐ Low noise	5 V output, 75 mV peak-to-peak max. +/−12 V outputs, 125 mV peak-to-peak max.	☐ Easy maintenance	95% modular circuit cards and subassemblies.
☐ Wide range temperature	0° to 60° operating temperature.	**Write for the OLS data sheet.**	



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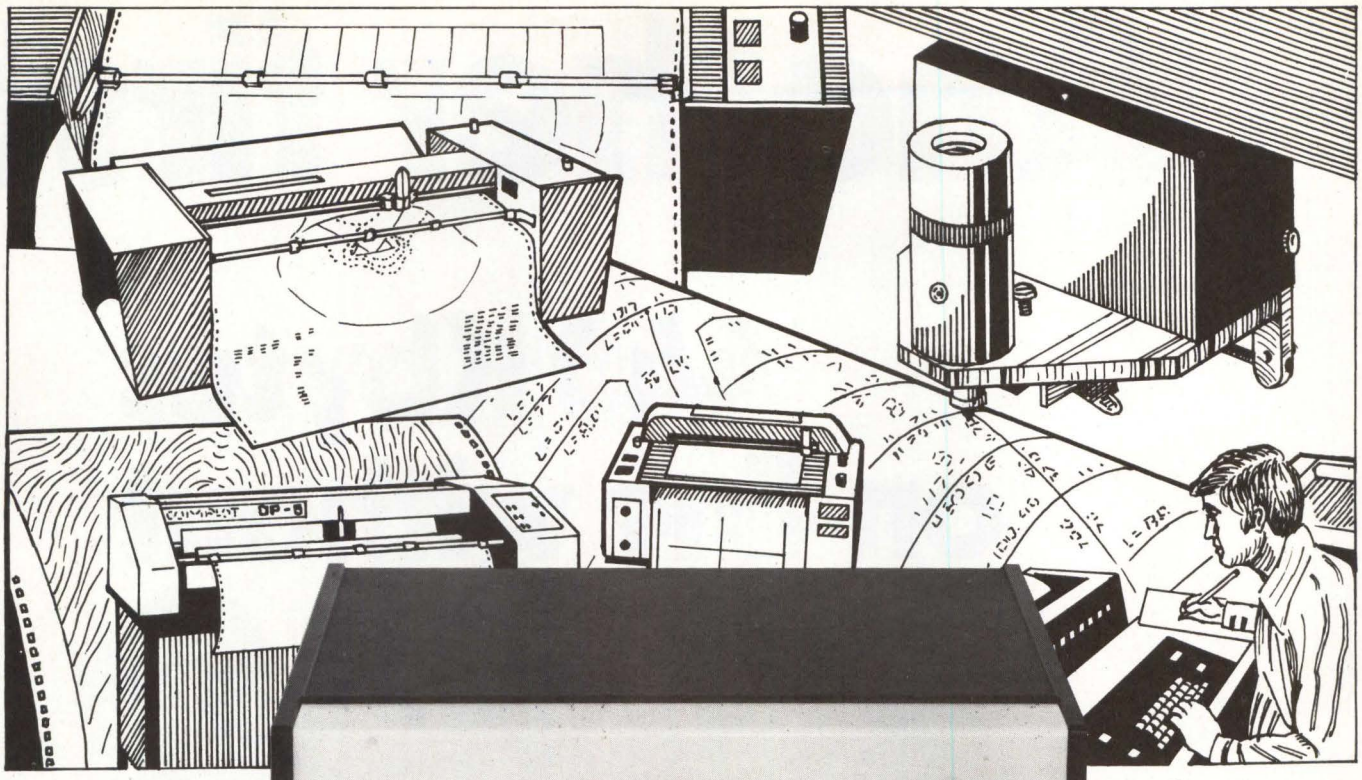

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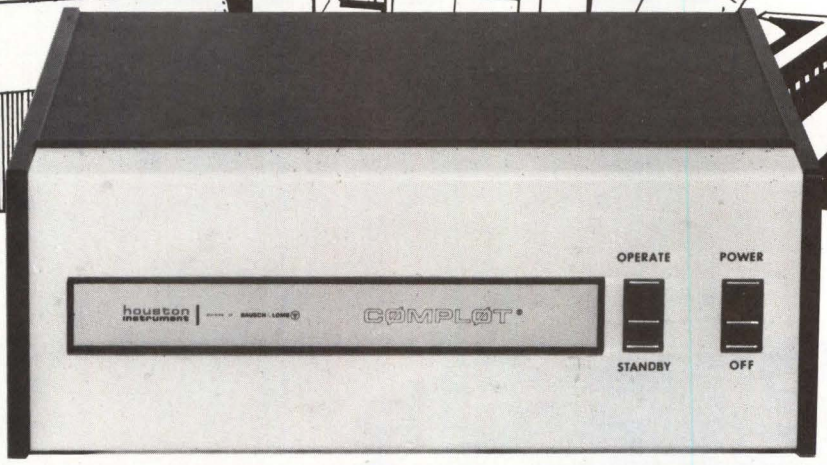

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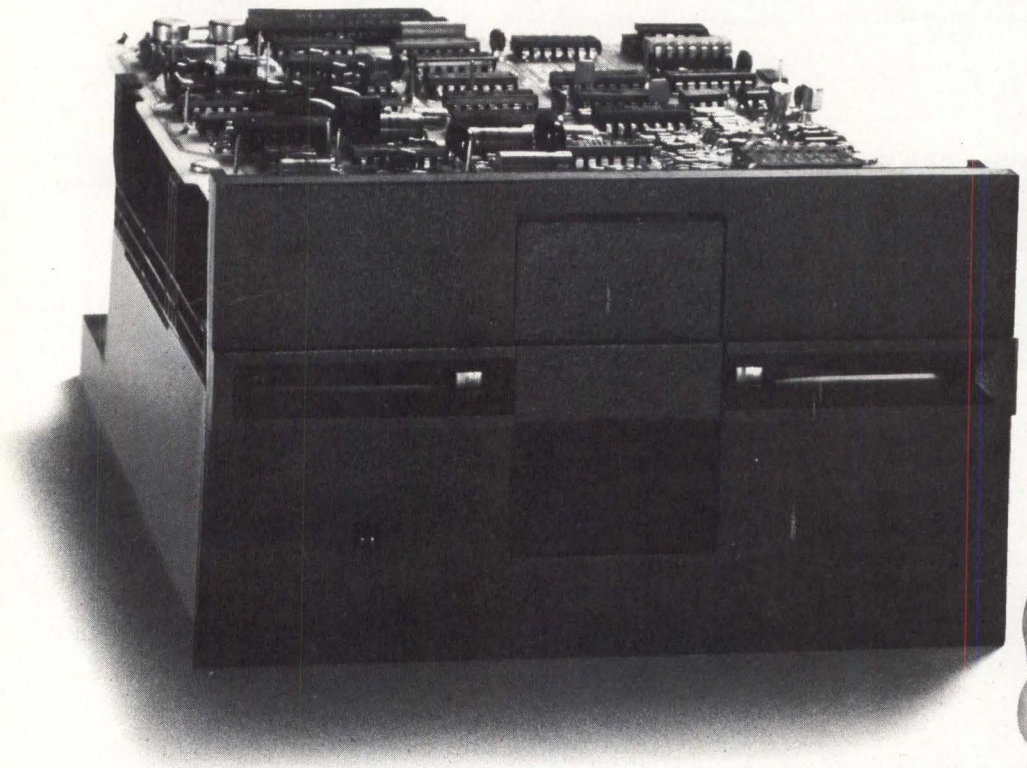

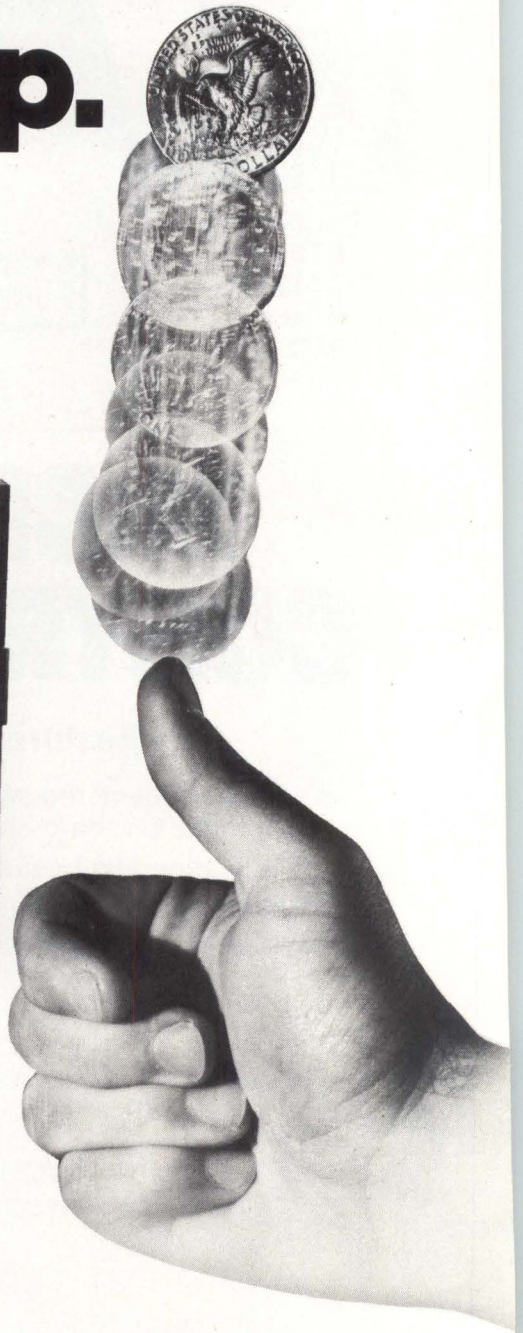

from number 1

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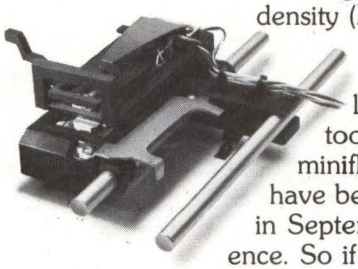

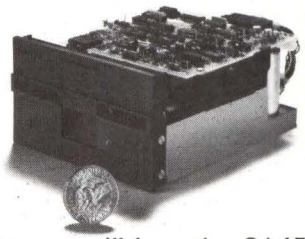

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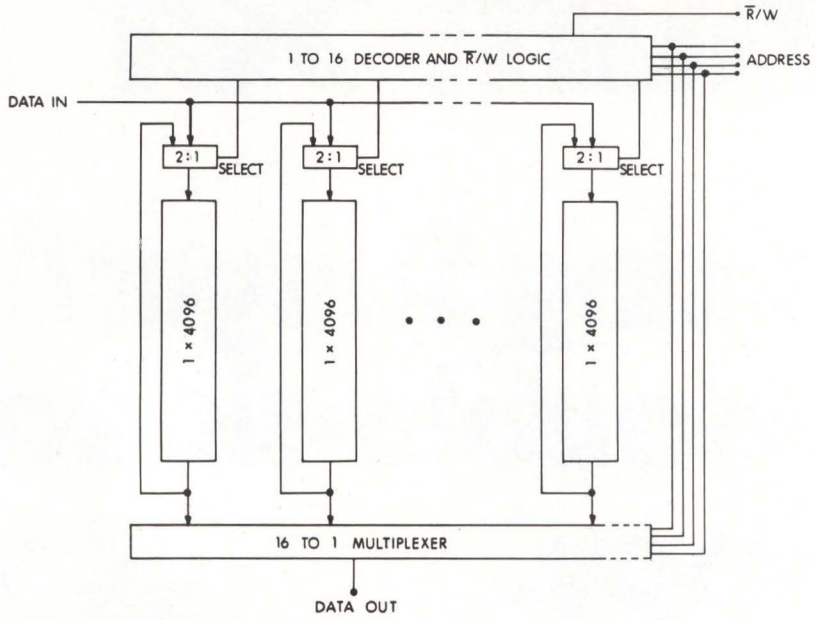

Fig 1 Generalized block diagram of 64k CCD memory. Configuration is 16 x 4096 addressable registers

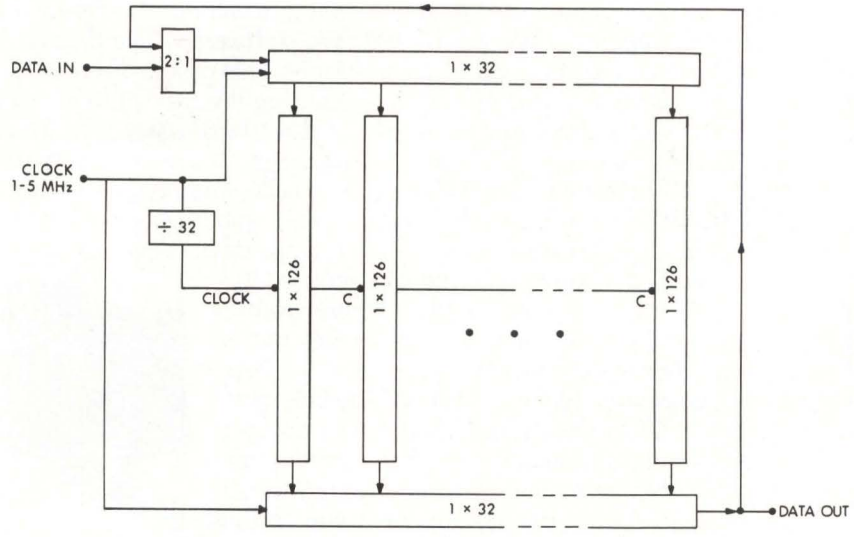

Fig 2 Serial-parallel-serial organization of 4k-bit registers. Note that vast majority of bits are clocked at one thirty-second the actual serial data I/O rate

transfer efficiency (percentage of charge actually transferred from cell to cell) is far less critical than it would be for a 1 x 4k register.

Several key differences exist between the Fairchild and Texas Instruments chips. First, the Texas Instruments chip requires only the two high frequency (5-MHz) clock phases. From these the high capacitance driving, low frequency clocks are generated onboard the CCD chip. Texas Instruments regards this as an advantage over the Fairchild chip which requires four external clocks, including two high and two low frequency clocks. Fairchild contends that inexpensive external clock drivers will suffice, and the cost is marginal.

Although Texas Instruments initially sampled some very large chips (60,000 mil^2), the size of their current version is 192 x 210 mils (40,000 mil^2), which is only slightly larger than the Fairchild 39,000-mil^2 size. The difference in size is partially attributable to Texas Instruments' onchip clocks, but even more to a unique seventeenth loop on the chip. This loop is not

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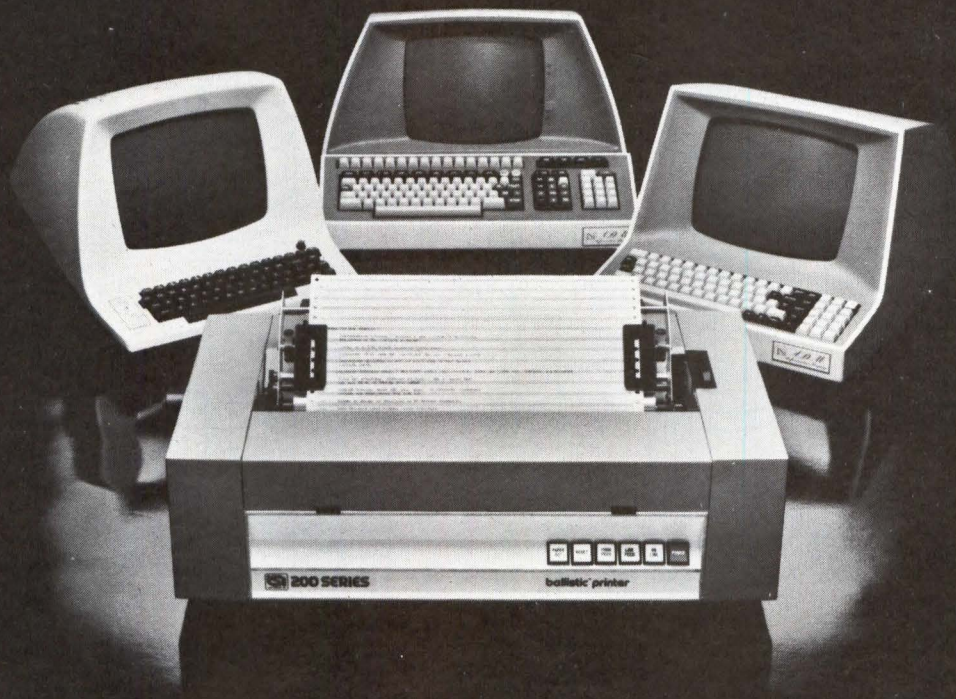

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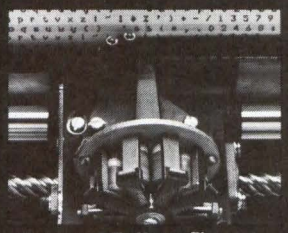

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Add to this such features as fully buffered input. Optional interfaces: serial, RS232, Parallel, and Current Loop. And you can see why we believe our Ballistic Printer is one of the most versatile printers you can buy.

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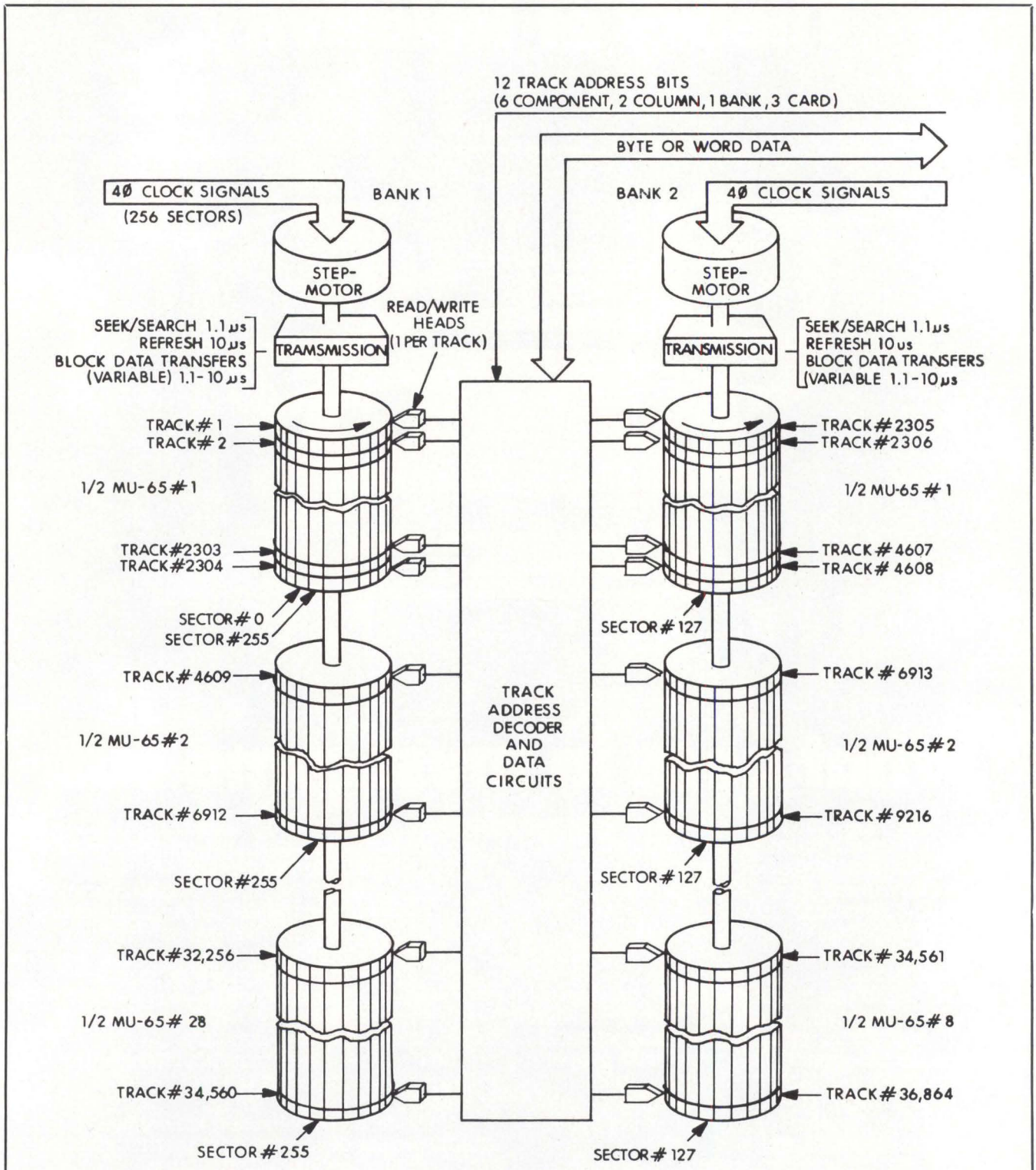

Fig 3 Pictorial representation of IN-65 CCD memory system data organization and operating speed. This system can be thought of as a pair of super fast head-per-track drums with 36,864 tracks, each made up of 128 storage cells for 9-bit bytes (Courtesy Intel Memory Systems)

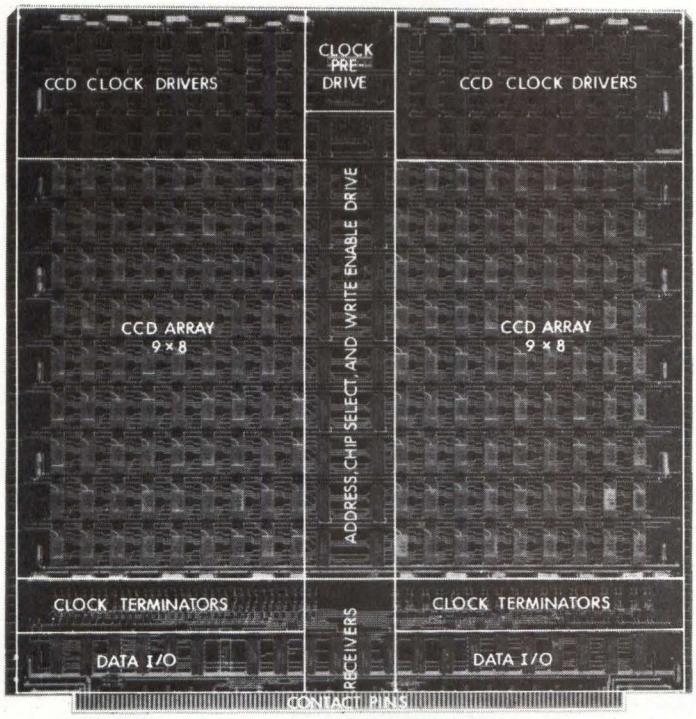

Fig 4 Fairchild 1M-byte CCD memory board. This single board contains 162 CCD memory devices of 64k each for a total capacity of 1 million 9-bit bytes. It uses a 3-layer PC board with a center layer ground plane (Courtesy Fairchild Semiconductor)

used for data; instead it provides temperature compensation for improved performance over the full 0 to 70°C still-air range. Fairchild claims that they did not use the extra loop because their tradeoff analysis showed that the extra silicon does not sufficiently improve margins over temperature to be worthwhile.

This extra loop does solve a problem, however. Ordinarily, empty charge wells in the data loops tend to fill with charge as a result of leakage current, and leakage current increases rapidly with temperature. If a fixed "1/2" voltage were to be used for comparison when sensing the data wells for 0 or 1, a bias would develop toward 1 at high temperature. To compensate for this in their initial device, Texas Instruments shifts 1/2 charges into the seventeenth loop. As these 1/2 charges are shifted through this auxiliary loop, they will be augmented by any leakage current and reduced by any charge transfer inefficiency, at exactly the same rate as the data charges in the other 16 loops. Thus, they will serve as a perfect reference value for the comparison circuit to determine if each of the 16 data bits is a 1 or 0. Temperature effects thereby will be greatly reduced.

Fairchild designed the CCD 464 chip to be longer and narrower so that it fits into a 0.3" (0.76-cm) 16-pin package compared to Texas Instruments' 0.4" (1.0-cm) 16-pin case. The 0.3" (0.76-cm) package facilitates the use of automatic insertion equipment, which may be a marketing advantage when chip volumes become large. Fairchild also points out that Motorola will second source their chip as part of the companies' technology exchange agreement. David Ford, Motorola's strategic marketing manager for CCD memories, says he expects the MCM-0464 to be sampled by the time this column is published.

An example of a memory system which utilizes such devices is the Intel IN-65. This CCD memory is organized as a system of eight PC boards, each containing 128k x 9 bits of storage. A board is logically arranged as 512 sets of nine parallel loops, so that each loop set stores data bytes in parallel with parity. Since a loop set is 256 locations long, it can be thought of as a 256-position, 9-bit wide shift register. There are 512 such 9-bit wide registers on a single board; thus a system of eight boards has a total capacity of 1,048,576 9-bit bytes. In effect, this system is comparable to a super fast head-per-track drum with 36,864 tracks, each consisting of 128 storage cells for 9-bit bytes (Fig 3). Because of its short loop length (256 positions), the maximum access time to any location is less than 300 μs, making this unit extremely attractive for memory swapping applications.

Considerably more density is accomplished on a developmental Fairchild memory system which packs 1

million 9-bit bytes on a single 15 x 16" (38 x 41 cm) board—eight times that of the IN-65. This board contains a total of 162 Fairchild CCD 464 64k chips for a total operating capacity of 9,437,184 bits (1,048,576 9-bit bytes). Data density is 41.9k bits/in^2.

On this board, data receivers, input latches, multiplexers, and output drivers are located adjacent to the contact pins in the section labeled as data I/O on Fig 4. Receivers, at the center of the contact pin edge, are provided for address, chip select, write enable, and clocks. By locating logic very close to the contact pins, in both receiving and driving circuits, lead lengths are kept short enough to eliminate the need for terminating networks.

Array address drivers, chip select, and write enable drivers are located in a center strip between the two halves of the CCD array. CCD predrive logic is located just above that strip with CCD high power clock drivers located on either side such that they are at the farthest points from the contact pins. Clock drive circuits drive the CCD memory array and are terminated near the data I/O logic.

64k CCD memories are aimed not only at the rotating memory market, but even more directly at mainframe RAM. Currently, mainframe and minicomputer memory represent nearly one-third of the total semiconductor market; so CCD practitioners are not thinking small. They believe that a practical approach to reducing large computer memory cost could be to use a combination of a small, high speed MOS or bipolar cache memory, a larger medium speed MOS buffer, and a very large CCD main memory. To attack this market, CCD designers follow a rough rule of thumb—the one-third rule—which says that if the per-bit cost of CCD is roughly one-third that of RAM, CCD will win. So far, they are optimistic. The 64k CCD chips are about the same size as Intel's and Texas Instruments' 16k RAMs (although larger than Mostek's 27,000-mil^2 16k RAM). Since the 64k CCD and 16k RAM rely on similar design rules and processing, the CCD designers expect similar yields and similar prices.

Of course, if the 16k RAM is initially used in higher volume, it could move down the experience curve somewhat more rapidly, thus dropping in price faster than CCD. The technologies are so similar, however, that it would be hard for any large difference to develop. CCD designers, therefore, expect to keep pace and hope to maintain a competitive chip price with the 16k RAM.

Price estimates have the 64k CCD pegged as

Year	64k CCD Chip Price (dollars)	Chip Price/Bit (millicents)
1977	65	100
1978	20	30
1979	10	15
1980	7	10

At these prices, CCD should be very competitive not only with RAM, but also with bubble memories (the subject of an upcoming column). Price projections for bubbles are not unlike those given for CCDs, and the principle differences will be non-volatility of bubbles, denser packing of bubbles in the long run (CCD is better now), and higher speed of CCD (10X). Based on these projections, a system price of $1400 for the Fairchild 1M-byte CCD board (Fig 4) will be feasible in 1980.

Just as exciting as these prospects for CCD memories, charge-transfer devices are now taking the fields of signal processing and image sensing by storm. They will be the subject of next month's column.

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Combination RAM-I/O Chip Consolidates Functions for Smaller Microprocessor Systems

Low end microprocessor-based systems which have relatively small memory requirements but which nevertheless require a number of peripheral interfaces are suggested as ideal for application of a combined RAM and I/O chip. The n-channel LSI device is said to do the job of five or more standard memory and peripheral interface units.

INS8154 was designed by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 to interface with the SC/MP II and other of the company's microprocessors. The memory portion of this dual function device contains 1024 bits of static RAM organized 128 x 8; the I/O portion consists of two peripheral ports of eight bits each. Each I/O pin may be defined as an input or an output to provide maximum flexibility and each port may be read from or written into in a parallel (8-bit byte) mode.

To improve efficiency and simplify programming in control-based applications, a single bit of I/O in either port may be set, cleared, or read with a single microprocessor instruction. This is claimed to be virtually unique among I/O devices.

In addition to basic I/O, one of the ports may be programmed to operate in several types of strobed mode with handshake. Strobed mode together with optional interrupt operation permit both high speed parallel data transfers and interface to a wide variety of peripherals with no external logic.

The data bus buffer (see Figure), a Tri-State(R) bidirectional, 8-bit buffer, interfaces the RAM-I/O chip to a microcomputer data bus. Data, control, and status information are transmitted to and received from the chip via the data bus buffers. Execution of a store instruction by the microprocessor may be used to transmit data and control information from the CPU to the chip. Execution of a load instruction may be used to transmit data and status information from the chip to the CPU.

A low on CS0 plus a high on CS1 chip select input pins enables communication between the chip and the microprocessor. State of the M/IO input pin determines whether communication between the CPU and chip will involve the RAM or the I/O portion. A high on M/$\overline{IO}$ selects the RAM while a low selects the I/O.

NRDS is an active-low read strobe. A low on this pin enables data or status information to be read from the chip. NWDS is an active-low write strobe. A low on this pin enables data or control information to be written into the chip.

The address input bus determines where communication will take place in the chip. When the RAM is selected, the address bus determines which of the 128 bytes of RAM will be read from or written into. When I/O is selected, the address determines which I/O or control register will be enabled for communication with the CPU. These pins are normally connected to the seven low address lines of the microprocessor.

Since the RAM is fully static, no refresh or clocks are required. Data out of the RAM are the same polarity as data in, and readout is nondestructive. The RAM is a standard 6-transistor cell similar in design to the 2102A.

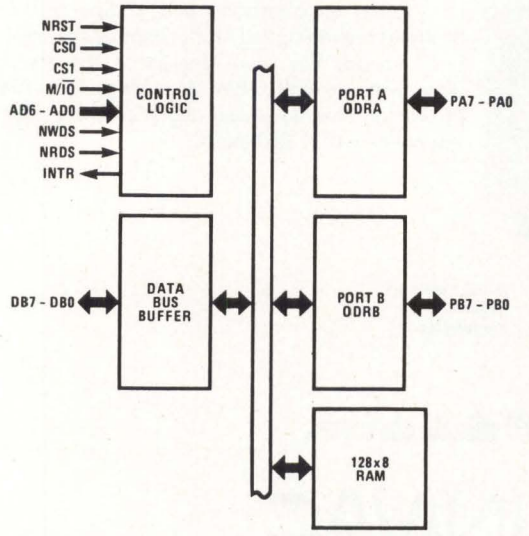
Each of the two ports consists of an 8-bit output data latch with buffer and an 8-bit input data latch. Full flexibility is provided with the ability to define any bit of the two ports either as an input or as an output. Bit set, clear, and read of all I/O pins are also provided. Moreover, port A may be operated in strobed input or strobed output modes.

Associated with each port is an output definition register (ODR), an 8-bit latch that defines which of the I/O pins in the respective port are to be used as outputs. Both ODRs are write only registers. If a read operation is performed with the address set to that of an ODR, the data bus will remain in the high impedance state.

The interrupt request (INTR) output is an active high signal used to interrupt the microprocessor when a strobed mode data transaction has occurred. This signal is active only when port A is in the strobed mode. INTR will be set to a low when a master reset is applied (NRST set low).

NRST is the master reset input for the chip. A low on this pin clears all registers in the I/O portion of the chip (ODRA, ODRB, and the port output data latches) and places the data bus in the high impedance state independent of any other control strobes. After a master reset, both I/O ports will be in the basic I/O mode and configured as inputs. The master reset does not change any data previously stored in the RAM and does not allow data to be written into or read from the RAM while NRST is low.

The RAM-I/O is packaged in a 40-pin DIP. It operates with a single 5-V power supply and is fully TTL compatible.



Basic block diagram of INS8154 RAM-I/O chip. This n-channel 128 x 8-bit device provides both data storage and peripheral interfacing functions on one chip. A single instruction sets, clears, or reads one bit of I/O in either port

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CIRCLE 64 ON INQUIRY CARD

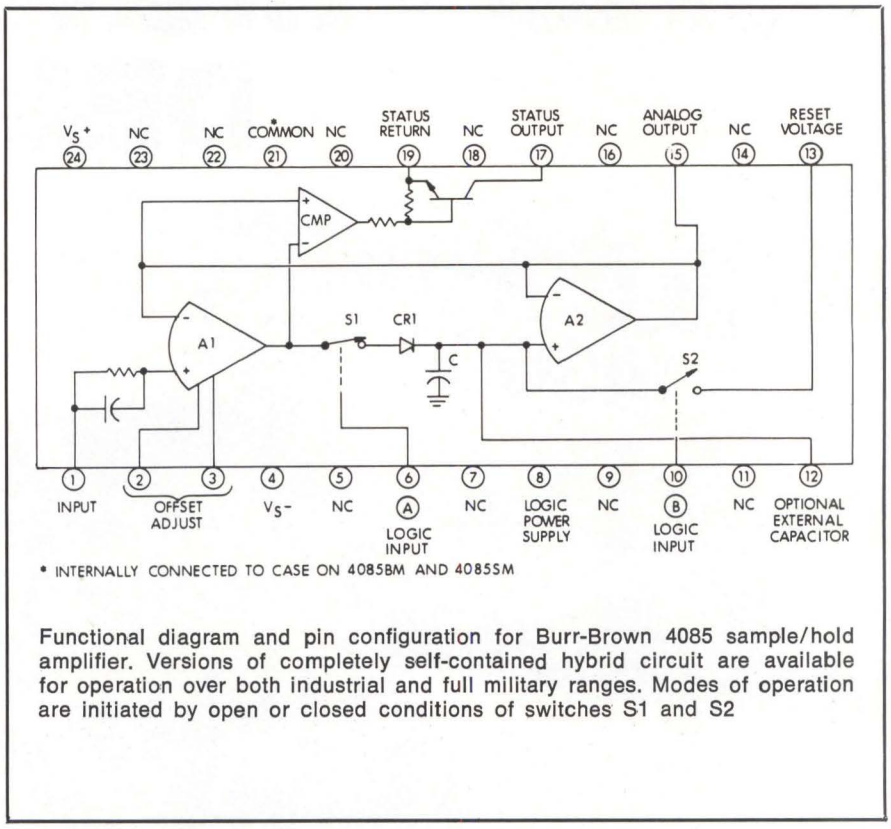
ASTRO Devices Second-Sourced

Pin-for-pin compatible with the UC1671 (from Western Digital) and the INS1671 (from National), the second-source COM1671 asynchronous/synchronous transmitter-receiver (ASTRO) is now in production by Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11786. The n-channel, software responsive device can handle complex communication formats in a variety of system applications.

It performs the functions of interlacing a serial data communication channel to a parallel digital system, is capable of full-duplex communications (receiving and transmitting) with synchronous and asynchronous systems, and operates on a multiplexed bus with other bus oriented devices. Programming is provided by a processor or controller via the bus, with all parallel data transfers accomplished over the bus lines.

Baud rates from dc to 1M/s are handled. Integral handshaking terms insure easy interfacing with modems or other peripheral devices such as display terminals. A programmable diagnostic mode allows the selection of an internal looping feature to connect the device internally for processor testing.

Circle 350 on Inquiry Card



Functional diagram and pin configuration for Burr-Brown 4085 sample/hold amplifier. Versions of completely self-contained hybrid circuit are available for operation over both industrial and full military ranges. Modes of operation are initiated by open or closed conditions of switches S1 and S2

Hybrid Peak Detectors Provide ±0.01% Accuracy

First of its type to be offered in a hybrid circuit package and the only one available for operation over the full military temperature range are only two of the claims being made by Burr-Brown, PO Box 11400, Tucson, AZ 85734 for its 4085 hybrid peak detector. In addition, the IC is said to be the lowest priced unit currently on the market. Its applications include monitoring of power lines and analytical instrument output as well as testing of components.

The device detects positive-going input signal peaks over the −10 to 10 V range with ±15-V supplies and holds each peak value until reset or until a higher peak is detected. Optionally, it can be put in hold mode to ignore higher peaks. Dynamic accuracy is better than 0.01% (12 bit) to 500 Hz and output droop is ±0.06 mV/ms max at 25°C.

In operation, the specialized sample/hold amplifier tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital status output indicates that a peak has been detected. Then the device can be commanded to hold that value, ignoring additional peaks, or to reset to a user-specified reference voltage.

In peak detect mode (S1 closed, S2 open as shown on diagram), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reverse biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output.

In hold mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage.

In reset mode (S1 open, S2 closed), the voltage on the capacitor will charge to whatever voltage is applied to the reset voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reset voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.

Three versions are available: the ceramic 4085KG has a specification range of 0 to 70°C while BM and SM are hermetically sealed metal packages with specification ranges of −25 to 85°C and −55 to 125°C respectively.

Acquisition time is 200 μs max, input offset is 2 mV typ (adjustable to zero), input offset drift is 50 μV/°C typ, and input bias current is 15 pA max.

Typical prices quoted for these hybrid peak detectors in 1 to 24 quantities are $49, $64, and $81, respectively, for the 4085KG, BM, and SM. 100 to 249 prices, respectively, are $36, $42, and $59.

Circle 351 on Inquiry Card

If you're this kind of systems OEM,

You're building complex turnkey projects.

You need more than "iron".

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You'll like our systems engineering help, because we understand system problems. And we don't love you and leave you, but supply full support — field service, documentation, personnel training, even sales support.

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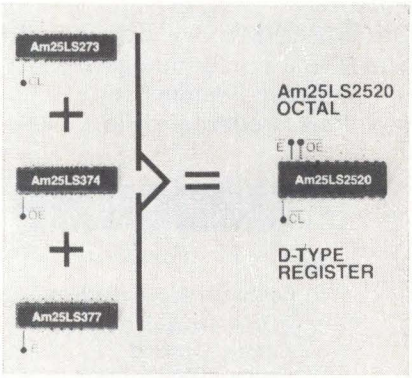
CIRCLE 65 ON INQUIRY CARD

Two Modcomp IV and four Modcomp II processors are the center of a new digital traffic control system for the city of Baltimore, engineered by TRW Inc. The TRW system has the capacity to control signals at 1200 key intersections in the city, and also provide surveillance of a five-mile section of the Jones Falls Expressway.

Single DIP Combines Features of Three ICs

Features previously available only on three separate devices are now combined on a single octal register —the Am25LS2520. This device consists of eight positive edge-triggered D-type flip-flops in a single, 22-pin, 0.4″ (1 cm) center-to-center DIP and offers features of the 20-pin Am25LS273 (common clear), the Am25LS374 (common 3-state enable), and the Am25LS377 (common clock enable) octal registers. Typical clock-to-output delay is 21 ns.



Am25LS2520 octal register. Capabilities of three separate ICs are obtained from a single 22-pin package

When the clear input is low, internal flip-flops are reset to logic 0 (low), independent of all other inputs. When the clear input is high, the register operates normally.

When the 3-state output enable ($\overline{OE}$) control input is low, the Y outputs are enabled and appear as normal TTL outputs. When $\overline{OE}$ is high, the Y outputs are in the high impedance (3-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable ($\overline{E}$) input is used to selectively load data into the register. When the $\overline{E}$ input is high, the register will retain its current data. When the $\overline{E}$ is low, new data are entered into the register on the low-to-high transition of the clock input.

Availability of these three features in one package enables designers to reduce both the device type proliferation and package count in new system designs. In many cases this 22-pin device will replace two 20-pin functions.

The register is produced by Advanced Micro Devices Inc, 901 Thompson Place, Sunnyvale, CA 94086 in molded and ceramic hermetic packages for use over commercial and military operating ranges. It is processed fully to the requirements of MIL-STD-883.

Circle 352 on Inquiry Card

IC Functions as Floppy Formatter/Controller

The dual density FD1781, an MOS/LSI floppy disc controller/formatter that accommodates the interface systems of most drive manufacturers, has been introduced by Western Digital Corp, PO Box 2180, Newport Beach, CA 92663. Special features of the n-channel silicon gate device include automatic track seek with verification; selectable track-to-track stepping, head settling, and engage

times; double buffering of data; 8-bit bidirectional bus for data, control, and status; and flexible formatting, including full compatibility with IBM 3740 data entry systems. The device also provides data, data strobe and address mark input/output for reading and writing data, and can accommodate MFM, M^2FM, group coding, as well as other double-density encoding methods.

Circle 353 on Inquiry Card

Multiplying DACs Meet MIL-STD-883 Class B

MDA 100 and 120 high reliability, 4-quadrant multiplying hybrid digital-to-analog converters, available from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716, feature exclusive pull-up resistors for guaranteed logic compatibility. Each device also incorporates a welded-lid package design and meets MIL-STD-883 Class B requirements, allowing use in rugged military and industrial applications.

MDA 100 is a true 10-bit multiplying DAC with a full 10-bit linearity. The 16-pin device is a pin-for-pin replacement for the Analog Devices AD-7520 and the Hybrid Systems HS-331. MDA 120 is a true 12-bit multiplying DAC with a full 12-bit linearity. The 18-pin device is a pin-for-pin replacement for the Analog Devices AD-7521.

Circle 354 on Inquiry Card

FPLAs Offer Alternative To Random Logic Designs

Two high performance Schottky TTL field programmable logic arrays (FPLAS) are claimed by their manufacturer to be practical LSI alternatives for random logic designs. This is said to result from coupling innovative control options with increased cost effectiveness. SN54S/74S330 and SN54S/74S331 feature a built-in capability for multidimensional expansion of their basic 12-input x 50-product term x 6-output organization. A special circuit is included that can decode true product terms to automatically enable the FPLA outputs.

Expandability is possible to virtually any size array without external logic or control. The control option can be activated by fusing a single titanium-tungsten link or by implementing a dedicated enable input as an alternative for conventional expansion or logic control. Outputs are constantly enabled when system power is applied so that the devices can be programmed to stand alone.

Among the advantages of these FPLAS from Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 is that time consuming reduction of complicated Boolean functions can be eliminated or reduced significantly by "writing" compound/multiple gating functions directly. Virtually any combination of AND, NAND, OR, or NOR logic functions can be programmed to replace random logic gates.

Typical delay time of 35 ns specifically enables use of these devices as one of the major building blocks in the company's S481 Schottky bit-slice chip set, a micro/macroprogrammable 4-bit slice processor element which can perform micro-operations at rates up to 15 MHz. Design flexibilities of the bit-slice permit emulation of virtually any hardware or algorithm to provide full protection of software investment.

Packaging is in high density 20-pin DIPS for either commercial (0 to 70°C) or extended temperature (−55 to 125°C) requirements.

Circle 355 on Inquiry Card

22-Pin 4k RAMs Provide Higher Access Speeds

Improved speed-power performance plus increased noise immunity without changes in system design are promised system manufacturers that use the 2107C family of 22-pin 4k RAMs. Offered in both ceramic and plastic, C-1, C-2, and C versions, respectively, provide maximum access speeds of 150, 200, and 250 ns; read and write cycles of 380, 400, and 430 ns; and read-modify-write of 450, 500, and 550 ns. These speeds are guaranteed over a 0 to 70°C range. Typical power dissipation is 420 mW in active operation.

All power supplies (12, 5, and −5 V) have ±10% tolerances, which Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 says is twice the industry standard. In addition, maximum supply currents are lower; maximum average I_{DD} from the 12-V supply ranges from 35 mA for the C-1 to 30 mA for the C.

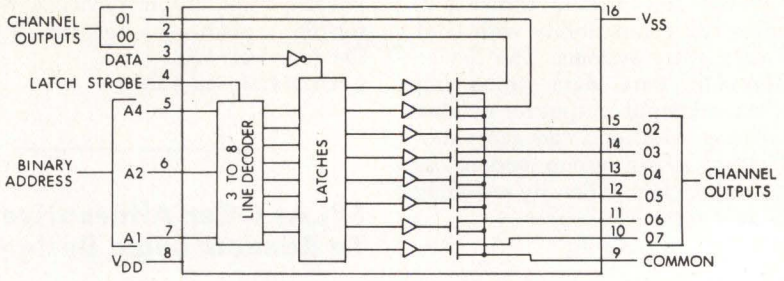
Based on the same fabrication technology and storage cell design as the 2104A family of 16-pin 4k RAMs, the 2107C family is expected to be used in new system designs where higher access speeds are desired. In addition, the family can directly replace 2107B, 2107A, and other standard 22-pin devices. Demonstrations have shown it to be compatible and interchangeable at board socket level.

Circle 356 on Inquiry Card

p-Channel MOS Circuits Drive Large LCDs

According to the manufacturer, the LS7100 and LS7110 are the first MOS devices capable of driving 8" (20 cm) LCDs that are offered off-the-shelf in large quantities. The 16-pin, p-channel circuits from LSI Computer Systems, Inc, 1235 Walt Whitman Rd, Melville, NY 11746 are input-compatible with CMOS and TTL systems to drive liquid crystal displays requiring segment drive voltages of from 5 to 60 V. Both operate over the −40 to 85°C range.

LS7100 is a BCD to 7-segment latch/decoder/driver that operates at 5 to 80 V. It requires a minimal amount of circuitry to interface with a 120-Vac line and drive a liquid crystal or gas discharge display. Its repertoire includes the digits from 0 to 9, as well as −, L, U, P, A, and H.



Block diagram of LS7110 multiplexer/demultiplexer/driver. In addition to driving LCDs of up to 8" (20 cm), this device can serve in many communications applications

LS7110 is a combination binary-addressable, latched 8-channel multiplexer, demultiplexer, and driver operating at 5 to 80 V. In addition to driving LCDs, it can be used for switching analog or digital signals, as a switching matrix, in communications, and for gathering and dispatching information. It can perform at high voltage levels and readily interfaces with 28- or 50-V signals.

Circle 357 on Inquiry Card

DAC Prices Reduced

Price reductions up to 29% for a line of high speed multiplying digital-to-analog converters have been announced by Signetics, PO Box 9052, 811 E Arques Ave, Sunnyvale, CA 94086. The NE5007/5008 converter ICs offer direct interface to TTL, ECL, HTL, CMOS, and p-MOS families, and incorporate advanced circuit design that achieves 85-ns settling time as well as high swing, adjustable threshold logic inputs to provide full noise immunity. Units are pin- and functionally-compatible with mono-DAC-08 converters originally introduced by Precision Monolithics.

Circle 358 on Inquiry Card

Semicustom MOS Chips Offer Up to 550 Gates

A family of MasterMOS chips announced by International Microcircuits, Inc, 3004 Lawrence Expressway, Santa Clara, CA 95051 consists of 10 semicustom chips ranging in size from the equivalent of 50 2-input gates to 550 2-input gates in 50-gate intervals. They operate at 7 MHz at 15 V, twice the speed of the original MasterMOS family. Each chip includes additional buffers for interfacing with LS-TTL or TTL. Computer-designed symmetrical logic cells are said to increase layout efficiency of interconnections of functions; eg, only four weeks are required to produce the first 75 prototypes.

Circle 359 on Inquiry Card

Bipolar Multipliers Feature Reduced Power Dissipation

Power reductions in MPY-8, -12, and -16 bipolar multipliers, resulting from substitution of military temperature range chips for commercial range devices, now eliminates all forced air cooling for operation over the 0 to 70°C commercial range. According to the manufacturer, TRW Electronic Components Div, PO Box 1125, Redondo Beach, CA 90278, this is achieved by a 20 to 30% reduction in supply current. However, the devices are fully compatible with previous MPY series multipliers.

Output delay times have been improved for all of the multipliers. The 8-bit, 130-ns MPY-8 has reduced average power from 1.75 W to an average of 1.2 W. One-half of the 1.2-W total power is consumed by the onchip registers. The multiplier itself consumes only 0.6 W. Efficiencies have been increased for the 12-bit, 150-ns -12. Average power has been cut from 3.5 to 3.0 W. The 16-bit, 160-ns -16 has dropped from a 5-W average power dissipation to an average of 4 W. □

Circle 360 on Inquiry Card

Announcing the quality oem fixed and removable Cartridge Module Drive with SMD interface.

The new Model 9448. The highest-performance, highest-capacity Cartridge Module Drive available today.

Ask Control Data.

Here is the first OEM Cartridge Module Drive with a 9.67 MHz transfer rate and 30 ms access time. This speed makes our CMD compatible with industry standard controllers. And the highest-performance CMD available today.

What's more, it's the first CMD that's interface-compatible with MMD and SMD disk storage. This means you can operate from a single controller three types of storage with capacities ranging from 12 to 300 Megabytes. And get a new, highly flexible growth path.

You also get the options you need. Control Data's new CMD is available in 32, 64, and 96 Megabyte capacities. Each model contains 16 Megabytes of easy front-loading cartridge memory. The remainder is fixed memory. Data can easily be copied from fixed disk to removable cartridge for greater security at lower cost.

All three models offer hard or soft sectoring, same packaging, common spares and many other benefits. Find out more about CDC's CMD breakthrough. Mail the coupon.

Call (405) 946-5421 or return coupon to Terry J. Hardie, Control Data Corporation, 4000 N.W. 39th Street, Oklahoma City, OK 73112.

Tell me more about your OEM Cartridge Module Drive.

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Ask our oem people

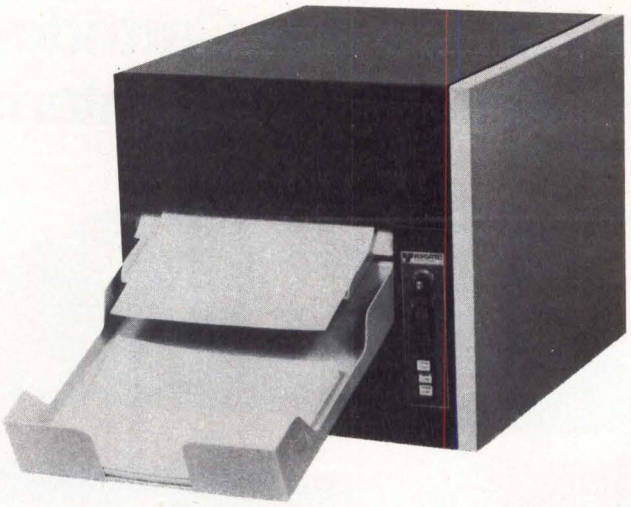
CONTROL DATA CORPORATION

CIRCLE 71 ON INQUIRY CARD

PRODUCT FEATURE

Computer Graphic Family

Multifunction



Versatility of the 3000 series electrostatic printer/plotters enables OEM designers to include them in fixed or mobile facilities for either land or sea operation. Alphanumeric and/or graphic hard copy, in a high quality, permanent presentation, can be produced from a variety of either parallel or serial digital data inputs. Six desktop models from Versatec include printers, plotters, and printer/plotters; all are also available for rackmount installations. Units are operable at a tilt of as much as 15 degrees in any direction for mobile or shipboard applications.

All units employ a proprietary nonimpact writing process called matrix electrostatic writing technique (MEWT™). Dual array writing head configurations, with either 100 or 200 stationary nibs/linear inch (39 or 79/cm), permit overlapping of dots for improved contrast and precise image formation. Image areas can be clear white, completely black, or anything in between.

Design Features

A specially coated paper used with this printing technique temporarily stores electrostatic charges selectively imposed by the writing head nibs. These patterns become visible after the paper is exposed to a liquid toner. Black particles suspended in the toner adhere to the paper only where an electrostatic charge exists. Copies are ready for immediate use when they leave the print unit.

In this raster scan writing method, one horizontal line—a single row of dots—is written, after which the paper is incremented slightly and another row (or scan) is written. By programming each scan, any design can be output, including shaded graphics and any size alphanumerics.

Internal circuitry converts ASCII-coded characters to preprogrammed plot patterns. Each character is formed by either a 7 x 9 or 16 x 16 dot matrix. An option, called simultaneous print/plot or SPP, permits print characters to be overlaid with plot data.

Most system control and write timing functions are carried out by an Intel 8080 microprocessor. Data and internal state information are transferred to other electronic and electromechanical subassemblies via an 8-bit bidirectional, 3-state data bus. Memory and peripheral device addresses are transmitted over a separate 16-bit address bus. Six timing and control outputs are available, and four control inputs, four power inputs, and two clock inputs are accepted by the microprocessor.

Two 256 x 4-bit random-access memories (RAMs) comprise a print buffer which can store one line of print data. Two other similar RAMs store one scan of plot data for a plot buffer. Presettable counters address the buffers to input or output a character or byte.

Either read-only memories (ROMs) or programmable ROMs (p/ROMs) store character dot patterns. ROMs are 2048 x 8 bits in size and each can contain 128 7 x 9 characters or 64 16 x 16 characters. p/ROMs are 1024 x 8 bits and are used for special character sets. Normally one ROM is used for standard 7 x 9 units and two are used for 16 x 16 units.

All printed circuit boards, including one for the power supply, plug into a common backplane, providing electronic modularity. The switching-regulator type power supply provides 5, −5, 12, −12, and 400 Vdc to the electronic and electromechanical subassemblies.

Operational adjustments are minimized by a self-aligning feature. The backplate electrode self-aligns to the writing head, the toner wiper bars self-align to the toner channel, and the 2-part cutting assembly self-aligns. In addition, a differential drive eliminates paper tracking problems to prevent the paper from skewing and tearing.

Print data are sent to the printer/plotter one ASCII-coded byte at a time. When one complete print line is received or a print line is properly terminated, the printer/plotter converts the codes into plot patterns and performs a number of plot scans to generate a character line. For 7 x 9 characters, nine scans are used for normal character generation and three additional scans generate the descenders where relevant; units with 16 x 16 character sets generate a total of 20 scans per print line.

Design of the series is based on operation with 11″ (28-cm) wide roll paper which can be cut in varying lengths either remotely by computer program or manually from a front panel control. However, 11 x 8.5″ (28 x 21.6 cm) fanfold paper can be used in applications where required.

Standard available controllers interface with Data General, Digital Equipment, Hewlett-Packard, IBM, Interdata, and Control Data computers. Optional controllers permit hardcopy production from Tektronix and Hewlett-Packard display terminals and other digital video sources.

Offers

Capability

Specifications

Printers 3150 and 3250, featuring 100- and 200-dot/in (39.4 and 78.7/cm) resolution, respectively, have the following respective specifications: 1056 and 2112 writing nibs; 1000- and 500-line/min print speed, 7 x 9 and 16 x 16 character dot matrix; 12.5-char/in (5/cm), ASCII 96 gothic character set for both; 132 columns/line, 6.6 lines/in (2.6/cm) for both; and 57 and 64 lines/fanfold page. The 3100 and 3200 plotters, respectively, also have 1056 and 2112 writing nibs, plus 2- and 1-in/s (5- and 2.8-cm/s) plot speed; and 10.24- and 10.56-in (26.77- and 26.82-cm) plot widths. Printer/plotters 3100A and 3200A combine all specifications of the printer and plotter of the respective resolutions.

General specifications include 110/115/200/300-Vac ±10%, 48- to 400-Hz, 500-W max power requirements; and 32 to 105°F (0 to 40°C), 10 to 95% relative humidity (noncondensing) operating environment. Paper and toner can be stored for a maximum of one year at 40 to 80°F (4 to 27°C) and 40 to 70°F (4 to 21°C), respectively.

Standard desktop models measure 17.5 x 19 x 22.5″ (44.5 x 48.3 x 57.2 cm), or 46 x 19 x 22.5″ (117 x 48.3 x 57.2 cm) with base; rackmount models measure 17.5 x 19 x 22.5″ (44.5 x 48.3 x 57.2 cm). These three configurations weigh 105, 160, and 105 lb (47.6, 72.6, 47.6 kg), respectively.

Price and Delivery

Single unit prices are $8550 for the 3100 plotter and 3150 plotter, $9250 for the 3100A printer/plotter, $10,500 for the 3200 plotter and 3250 printer, and $11,400 for the 3200A printer/plotter. Mounting base/supplies cabinet costs $495. OEM discounts are available on all. Deliveries are 60 days ARO. Versatec, a Xerox Co, 2805 Bowers Ave, Santa Clara, CA 95051. Tel: (408) 988-2800.

For additional information circle 199 on inquiry card.

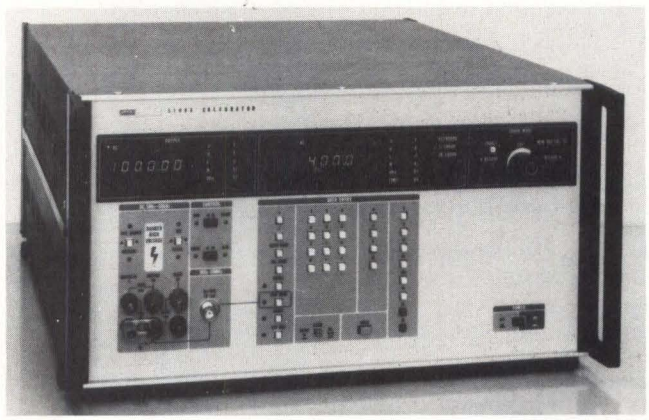
PRODUCTS

CRT and Line Printer Combine Visual Plotting and Rapid Hard Copy

Full graphic requirements from simple charts to complex engineering drawings and 3-dimensional views are met by the 2282 graphics CRT and the 2231W-3 matrix line printer. The CRT adds plotting and fully automatic alphanumeric lettering capability to the System 2200 CPU. A matrix of 800 X- and 512 Y-addressable locations are provided in a 7 x 6" (17.8 x 15.2-cm) area on the 12" (30-cm) diagonal screen. Plotting vectors are generated by turning a series of dots on or off. All CPU plotting output is displayed for possible operator modification. In addition, a 112-char ASCII set is stored in memory and can be plotted in 15 different sizes for different applications. The printer uses a 7 x 8 dot matrix for the same character set, printing at 120 char/s and 40 to 250 lines/min, depending on line length. Hard-copy of the CRT display is generated by printing strips of 800 x 8 dots under program control until the display is reproduced. Normal line feed spacing is reduced during image reproduction to provide vertical image continuity. An expanded character can be provided for highlighting. **Wang Laboratories, Inc,** 1 Industrial Ave, Lowell, MA 01851.

Circle 200 on Inquiry Card

Microprocessor-Controlled Calibrators Provide Multipurpose Capabilities



Models 5100A and 5101A, combining the capabilities of several instruments, accept data through simple front panel keyboards or with optional system interfaces for calibration of VOMs as well as 3½-, 4½-, and most 5½-digit DMMs. Control is maintained by a microprocessor. Outputs include dc voltage to 1100 V with 50-ppm accuracy; ac voltage to 1100 V with a bandwidth of 50 Hz to 50 kHz; ac and dc current outputs from 10 μA to 2 A; and resistance of eight decade values from 1 Ω to 10 MΩ. An option provides wideband ac from 10 Hz to 10 MHz with function ranging from −57.5 to 23 dBm. In addition, a tape cassette built into the 5101A provides a permanent storage of frequently used procedures. After a cassette containing output parameters is read into memory, the operator presses the advance key to select the sequence. Each cassette can store up to 58 procedural steps and can be programmed as easily as operating the basic instrument itself. **John Fluke Mfg Co, Inc,** PO Box 43210, Mountlake Terrace, WA 98043.

Circle 201 on Inquiry Card

Intelligent Keyboard Offers Broad Programming Options for Terminal Designers

Combining 103 Hall-effect logic scan key modules with a single-chip microcomputer results in a full-function keyboard for intelligent and distributed processing terminal applications. The microcomputer integrates 8-bit CPU, ROM, RAM, I/O lines, and a time/event counter on a single chip. A 40-pin EPROM, pin-compatible with the ROM, is available for prototyping. Features of the 19.38 x 16.34 x 1.44" (49.23 x 16.1 x 3.66-cm) model 103SD24-1 keyboard include 4-mode, 8-bit ASCII code assignment; choice of serial or parallel data outputs; 14 relegendable keytops for programming keys; 8-deep FIFO character storage; N-key rollover; and timed/auto repeat for selected keys. Each key module provides one isolated input and one isolated output. The output signal is valid when the input interrogation signal is true and the key is depressed. Enabled output will reflect the normal performance of a level sinking output. When the input is at high level, the output is inhibited by forcing the output transistor into off state. **Micro Switch Div of Honeywell,** 11 W Spring St, Freeport, IL 61032.

Circle 202 on Inquiry Card

Have it your way.

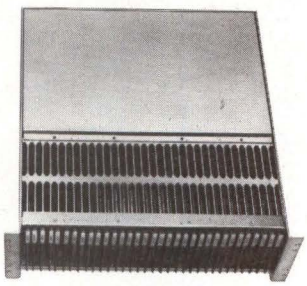
Bit by bit our Standard Modular Memory lets you make every word count.

The Standard.
768K x 16 in one 5¼ x 19 inch chassis.

Need more?
You can address up to *eight* of our MSC 2601 Standard Modular Memory units for up to 6144K x 16.

Want it your way?
Our field-proven MSC 2601 uses dynamic 16K RAM elements. You can organize each card 16K x 1 to 64K x 9. Multiple cards give you almost any word and bit size you want.

Any way you like it.
Up to 14,155,776 bits in one MSC 2601.



MSC – 2601

When you like it.
Access time up to 350 nsec. Cycle time as fast as 450 nsec.

Together in the rack.
RETMA rackmountable or freestanding. Self-contained with power supplies and forced air cooling. Battery backup available, too, for nonvolatile storage.

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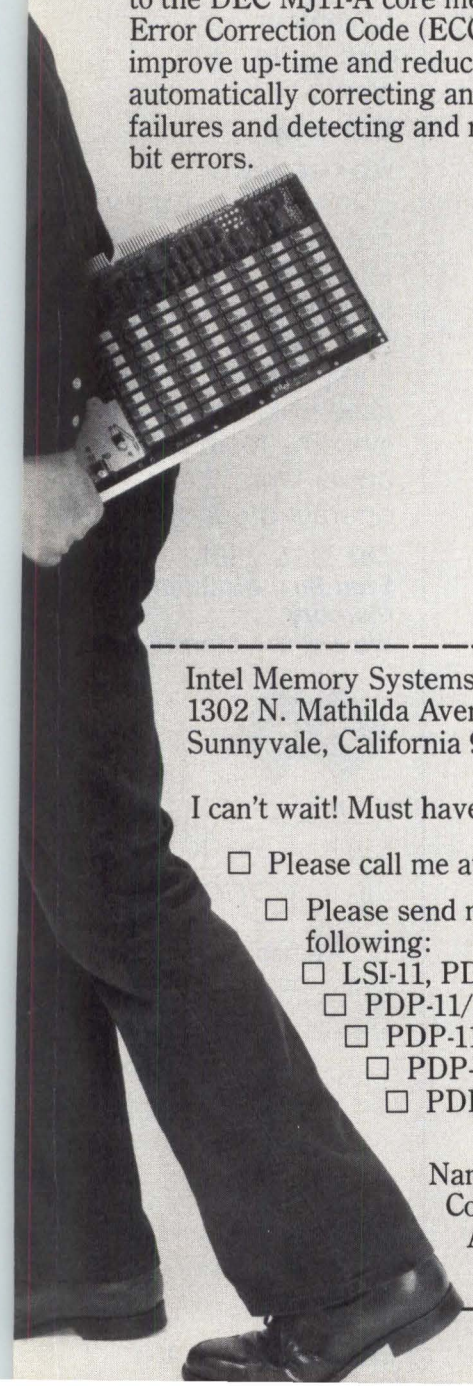

For PDP-11 add-in memory go with our in-4711 plug in boards. You'll get memory that's even faster than DEC's. 16K words per hex-wide board. With or without parity. To further expand PDP-11 memory and reduce UNIBUS™ loading choose our in-4011 add-on. With memory management you can expand to 128K words in 16K increments. And since the in-4011 requires only one UNIBUS load, you get added system flexibility.

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☐ PDP-11/45
☐ PDP-11/55
☐ PDP-11/70

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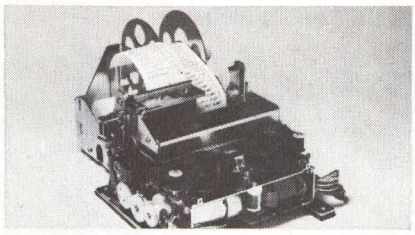
PRODUCTS

DOT MATRIX IMPACT PRINTERS

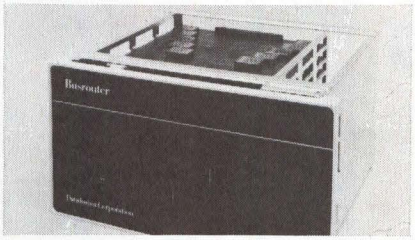


Model 520 2-stage receipt and journal printer, model 540 ticket or slip printer, and model 510 roll printer, comprise the series 500 family of 40-col dot matrix impact printers. Dc motor-driven mechanism prints at 2.5 lines/s; unit weight is 2.5 kg, and size as small as 175 x 146.5 x 112.5 mm. Warranty includes continuous duty headlife of 100M char and MCBF (mean cycles before failure) of 5M lines/mechanism. **C. Itoh Electronics, Inc,** 280 Park Ave, New York, NY 10017.
Circle 203 on Inquiry Card

ULTRA-MINIATURE FAN

Designed for applications where limited space is available, model V60CL features a multi-vane impeller, driven by a high efficiency ac motor. With an output of 10 ft^3/min (4720 cm^3/s) in free air, high performance fan has an impeller diam of 2.3 x 1.26" (5.8 x 3.2 cm) and weighs 1.7 oz (47.6 g). Compactly designed with aerodynamic characteristics, fan provides optimum pressure/flow. **Micronel,** Box 271, 8 Kane Industrial Pk, Hudson, MA 01749.
Circle 204 on Inquiry Card

UNIBUS™ SWITCHES

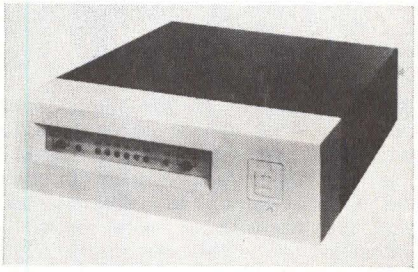


The OSR11-A busrouter allows physical and electrical switching of the Unibus™ for DEC PDP-11 series computers. Each switching plane allows a Unibus cable to be plugged in as the common and then selectively connected to one of two other cables via normally closed or normally open relay contacts. Using up to eight switching planes, various configurations perform multiple bus switching, and insertion and deletion of peripherals in the middle of the Unibus. **Datafusion Corp,** 21031 Ventura Blvd, Woodland Hills, CA 91364.
Circle 205 on Inquiry Card

SUBMINIATURE CONNECTORS

MELO-D series devices are non-environmental, rectangular connectors, with snap-in front removable contacts, which are intermountable and intermateable with existing D-type connectors. Crimp, solder cup, and wrap-post contacts are provided. Five configurations range from 9 to 50 contacts. Positive locking is provided with stainless steel threadlocks or a quick coupling system. **Positronic Industries, Inc,** 208 W Center St, Rogersville, MO 65742.
Circle 206 on Inquiry Card

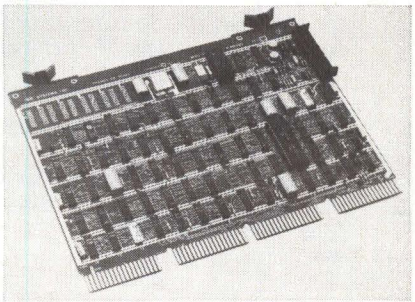
WECO-COMPATIBLE MODEM



GDC 212A transmits and receives binary, serial data over switched telephone network in asynchronous operation at 300 bits/s and synchronous or asynchronous at 1200 bits/s. With special buffer, modem is compatible with WECO 212A and 100 series. Std features of standalone unit include local and remote loopbacks, end-to-end test, and selftest. **General Data-Comm Industries, Inc,** 131 Danbury Rd, Wilton, CT 06897.
Circle 207 on Inquiry Card

ASYNCHRONOUS SERIAL LINE ADAPTER

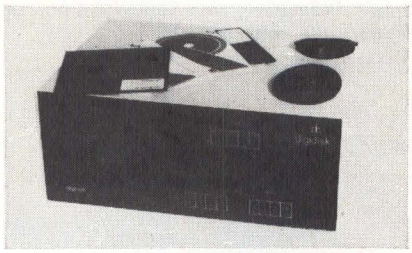
The MDL-11W serial line adapter combines all operational features of the DEC DL-11A, B, C, and D modules on a single board. Functions include switch selectable mode of operation, address, interrupt vector, and transmitter/receiver clock sources. Std features are a 20-mA active current loop interface, EIA RS-232-C interface drivers/receivers for local or remote terminal operation, full- or half-duplex operation, and 16 baud rates from 50 to 19.2k. Module is compatible with DEC operating systems and diagnostic software. **MDB Systems,** 1995 N Batavia, Orange, CA 92665.



Circle 208 on Inquiry Card

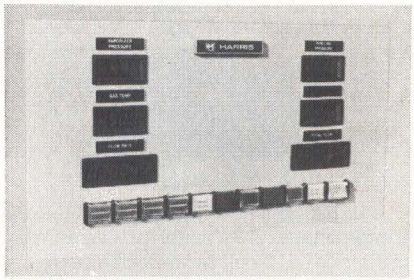
PRODUCTS

µP-BASED MINI-FLOPPY DRIVE



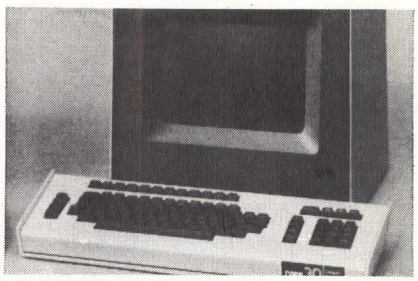
Digidisk™ system for emulating paper and mag tapes allows the operator to prepare and edit messages and data off-line, and then transmit them through the optional built-in acoustic coupler. Unit operates with any data communication printer or CRT terminal through std RS-232 interface. Responding to remote control code from a computer, microprocessor-based drive uses flexible minidisc with a capacity of >100k char. Control program resides on the disc. **Digicom Data Products, Inc,** 1440 Koll Cir, Ste 108, San Jose, CA 95112.
Circle 209 on Inquiry Card

HIGH SPEED PRINTER



Model 1654, a 1200-line/min chain printer, has been added to the 1600 family of remote batch terminals and distributed processing systems. Major applications for unit are in high volume production environments. Features include 132 or 136 print positions/line, a selector for 6 or 8 lines/in, and EBCDIC print chains having 0.095 and 0.079″ (0.24- and 0.20-cm) fonts in various paired combinations of 48-, 64-, and 96-char sets. **Harris Corp, Data Communications Div,** 11262 Indian Trail, PO Box 44076, Dallas, TX 75234.
Circle 210 on Inquiry Card

CRT TERMINALS



COPS 15, 20, and 30 series terminals are available with upward and downward software and functional capability. Std features are 1920-char screen capacity, 7 x 9 dot matrix, 128 ASCII char set, 12″ (30-cm) diag CRT screen, and variety of keyboards to suit particular application. Communication interface has full- or half-duplex/buffered transmission; EIA RS-232-C and 20-mA current loop; switch-selectable baud rates; and odd, even, mark, or space parity. **Computer Peripheral Corp,** 1225 Connecticut Ave, Bridgeport, CT 06607.
Circle 211 on Inquiry Card

Techtran
truly the best

New Compact Portable Model 815

Designed for lower speed terminals

- 145,000 characters per tape
- Full local and remote control
- Selectable speeds—10 and 30 c/s
- Character edit
- Optional battery powered
- Custom made carrying case available
- Only 6 lbs.

All Techtran Recorders have

- RS-232 Terminal and Modem/CPU Interfaces
- ASCII coding (Baudot Optional)
- Character edit
- Low cost magnetic tape cassettes
- 145,000 characters per tape
- Full local and remote control

Only $950.

...much lower in OEM quantities

for PRINTERS

Popular Model 8400

- 1000 c/s Data Search
- Powerful text editor
- Timesharing compatible
- Fast 110-2400 speeds
- File protect

for DATALOGGERS

Fast Model 8410

- Large 145,000 character storage per tape
- Remote, unattended data retrieval
- Operates under logger command
- Fast 110-2400 speeds

for CRT's

Powerful Model 8421

- Dual decks for merging and copying
- Powerful text editor
- 1000 c/s Data Search
- Format Mode
- Program control
- Fast 110-2400 speeds

for TEST STANDS

Versatile Model 8420

- Fast 110-2400 speeds
- Transparency Mode
- Dual decks for merging and copying

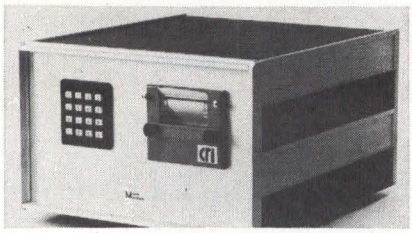
Choose the one that's best for you.

TECHTRAN
INDUSTRIES, INC

200 Commerce Drive, Rochester, New York 14623 Tel: (716) 334-9640 TWX: 510-253-3246 Los Angeles Tel: (213) 349-0775

PRODUCTS

PRINT TERMINAL MONITOR

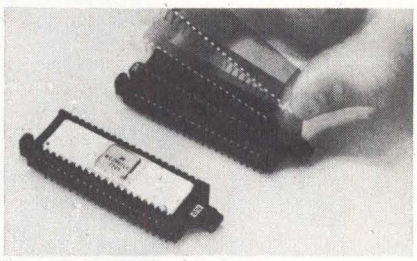


A fully programmable, microprocessor-based hardware monitor, Micromeasure will compute, accumulate, and print response time information for up to four CRT terminals simultaneously, including total number of transactions, time of day, date, high and low responses, average response, and total time of all transactions. Summaries are printed either automatically or on command over preselected time frames of up to 24 h. All instructions and machine functions are controlled through a hexadecimal keypad located on the front panel. **Computer Resources, Inc,** 4650 W 160th St, Cleveland, OH 44135.
Circle 212 on Inquiry Card

DIRECT-DIAL DATA STATION

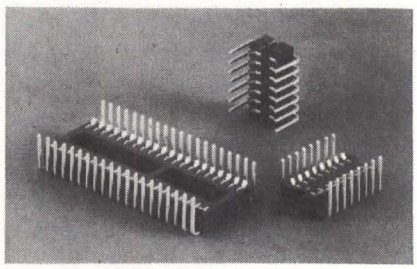
The 40+TK1 stores messages in an MOS solid-state buffer rather than on paper tape or magnetic tapes, and is designed to replace low speed, leased-line, and tape-operated terminals. Data transmission speed can range from 1200 to 2400 bits/s over dial-up lines. All data communications functions are fully automatic. Data station includes an ICC 40+ data display system, keyboard, and control modules, as well as communications control module and buffer, and 110-char/s printer. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.
Circle 213 on Inquiry Card

LOW INSERTION FORCE IC SOCKET



Intended for high pin-count packages, the LIF-Lock socket is a low-insertion force connector designed to minimize package and lead damage. Contacts grip package leads on both flat faces with a force of approximately 200 g each. To accommodate misaligned leads, each contact position has a generous funnel entry. Sockets are available in 24-, 28-, and 40-position sizes, fit std 0.100 x 0.600" (0.254 x 1.524-cm) PC board hole patterns, and are rated at 3 A with <25-mΩ contact resistance. **AMP Inc,** Harrisburg, PA 17105.
Circle 214 on Inquiry Card

WIREWRAP DIP SOCKETS



Permitting wirewrapping on same side of board as the IC, wirewrap pins on AS/U DIP socket are bent around and are on its upper side, where each IC lead can be seen and quickly wirewrapped, saving time in breadboarding of prototype circuits. Available in 14-, 16-, 20-, 24-, 28-, and 40-pin sizes, socket permits board-to-board space savings of from 25% to 30% in depth when multiple boards are used. **Robinson-Nugent, Inc,** 800 E Eighth St, New Albany, IN 47150.
Circle 215 on Inquiry Card

DATA COMMUNICATIONS TERMINAL

MIGET (miniature interface general-purpose economy terminal) provides keyboard entry and simultaneous 32-char display output compatible with all microcomputer and microprocessor systems using RS-232-C interface and ASCII code. The 8 x 10 x 3″ (20 x 25 x 7.6-cm) terminal weighs 4 lb (1.8 kg). Features include eight selectable baud rates from 110 to 9600, complete TTY compatibility, and optional self-contained memory system and acoustic coupler. **Micon Industries,** 252 Oak St, Oakland, CA 94607.
Circle 216 on Inquiry Card

COMMUNICATIONS NETWORK SYSTEM

Smart/Network connects geographically dispersed asynchronous data terminals to host computers while maintaining error-free transmission and compatibility with all common computers and terminal types. Data-driven statistical multiplexing techniques automatically route a terminal at any speed to any user-specified host computer, transmitting data over lines not normally usable. **Digital Communications Associates, Inc,** 135 Technology Pk, Norcross, GA 30092.
Circle 217 on Inquiry Card

FIBER OPTIC READOUT ASSEMBLY

Designed and packaged to resist shock, vibration, moisture, and other environmental hazards, nonencoded model 905-H display fiber optic readout assembly meets MIL-STD-883, Level B. It features an internal decoder, and LEDs that transmit through fiber optic tubes to produce a 0.43″ (1.09-cm) high char display on the 0.500 x 0.62″ (1.27 x 1.57-cm) display screen. Screen is a 7-segment display with 0 to 9 numeric capability as well as plus, minus, decimal point, and limited alphabetical char. **Master Specialties Co,** 1640 Monrovia Ave, Costa Mesa, CA 92627.

Circle 218 on Inquiry Card

IEEE-488 TAPE RECORDING SYSTEM

Data transfer directly from the GPIB (IEEE-488) to 0.5″ (1.27-cm) mag tape without interfacing is possible with the model 1015A-S tape recording system. Once on tape, data may be transferred into any computer for analysis, or read back through the bus to any GPIB-compatible minicomputer or calculator. Features include dual 2048 buffers to insure no loss of data during interrecord gaps, and transfer rates of up to 7.5 kHz. Both 7- and 9-track models are available. **Dylon Corp,** 7854 Ronson Rd, San Diego, CA 92103.
Circle 219 on Inquiry Card

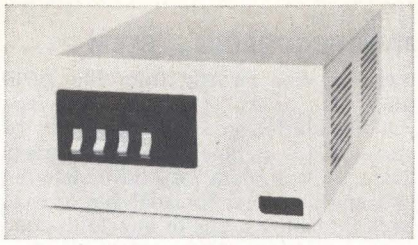
CRIMP CONTACT CONNECTORS

Miniature D-shaped rear-release Amphenol® 17 series rack and panel connectors feature insulation-support crimp contacts that secure both wire conductor and insulation in place, lessening chance of strain in actual application. The pin and socket contacts accept any conductor size from 22 to 26 AWG and are designed with backend tabs to crimp insulation up to a 0.050″ (0.127 cm) max OD. Std contact configurations are 9, 15, 25, 37, and 50. **Amphenol North America Div, Bunker Ramo Corp,** 900 Commerce Dr, Oak Brook, IL 60521.
Circle 220 on Inquiry Card

PRODUCTS

FULL DUPLEX, 1225-BIT/S MODEM

The VA3415 modem series, an improved version of the VA3400, transmits and receives at speeds up to 1225 bits/s, permitting it to operate with multiplexers that overspeed. Crystal controlled unit works with the company's multiline dialer, allowing a single automatic calling unit to handle up to seven lines. Two modems can be connected at

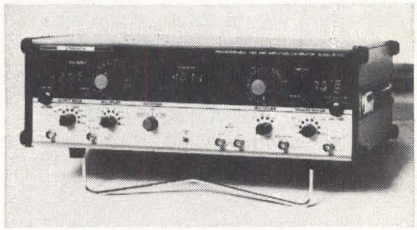


each end of a 4-wire leased line to provide two 1200-bit/s data streams without separate multiplexers. Modem connects to any dial-up telephone line with registered DAA. **Vadic Corp,** 222 Caspian Dr, Sunnyvale, CA 94086.
Circle 221 on Inquiry Card

OSCILLOSCOPE ADAPTER SWITCH

Converting any conventional, single-channel oscilloscope into a multichannel logic analyzer for troubleshooting digital logic circuits, MS-1 adapter allows switch-selectable display of two, four, or eight channels of data and operates in either chop or alternate sweep modes. Up to eight data lines may be sampled simultaneously while displaying digital logic levels and timing relationships on a conventional scope. **Mid-South Instrument Services, Inc,** PO Box 1252, Gretna, LA 70053.
Circle 222 on Inquiry Card

PORTABLE PROGRAMMABLE TEST SET



Model 6125C is a flexible, lightweight package that offers programmability on all front panel functions, and serves as voltage calibrator, sweep/delay-time or frequency calibrator, risetime calibrator, and error indicator. As an oscilloscope calibrator, the user can program ranges, divisions of vertical amplitude, marker frequency and number of markers, deviation, rep rate of the fast square wave, and either of two modes of remote operation. **Ballantine Laboratories, Inc,** PO Box 97, Boonton, NJ 07005.
Circle 223 on Inquiry Card

PHONEME SYNTHESIZER KIT

Votrax® VSK, designed to be used with a microprocessor, combines unlimited vocabulary, operational simplicity, and low data requirements. Programmed to speak based on phonetic coding principles, unit can produce all combinations of words and phrases. Phonetic coding permits production of speech at low data rates, offering continuous speech at 20 char/s and easy interfacing to any microprocessor system with an 8-bit parallel output. Fully assembled, the single circuit board uses std 5- and ±12-V power supplies. **Vocal Interface Div, Federal Screw Works,** 500 Stephenson Hwy, Troy, MI 48084.
Circle 224 on Inquiry Card

CONTROL SYSTEM MODULES

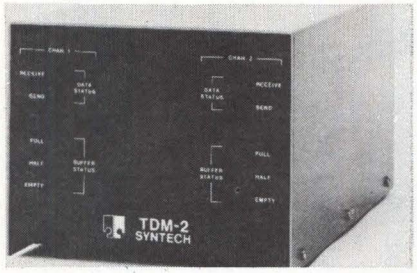
Paricode II modules connect directly to a voice-grade communication circuit and provide for transmission of alarms, analog and digital data, control signals,

and status information via coded audio tone signals. Single and multiple-channel equipment includes scanner modules for transmission of multiple signals on one tone channel, and frequency multiplexing modules which provide for 20 or more tone channels on one circuit. MiniData modules each transmit up to four data quantities and eight status or alarm signals on each channel. **Harris Corp, Controls Div,** PO Box 430, Melbourne, FL 32901.
Circle 225 on Inquiry Card

FLEXIBLE DISC WORD PROCESSOR

A single, flexible disc word processing system uses either the IBM Selectric typewriter or a high speed daisy wheel printer to provide recording, editing, and printing of text. User-oriented keys select char, word, line, or continuous printing as well as a 3-digit indicator for line selection. Std features of DataMaster II include rapid search, or search and list; automatic letterwriting; merging of paragraphs and automatic right margin adjust; and ASCII communications. **Tycom Corp,** 26 Just Rd, Fairfield, NJ 07006.
Circle 226 on Inquiry Card

MULTIPLEXER



TDM-2, a 2-channel time division multiplexer, enables simultaneous transmission of two channels of asynchronous data over a single synchronous data communication line. It can be used in private line terminal-to-terminal or computer-to-terminal applications and in point-to-point or multipoint networks, allowing each channel to operate independently in full-duplex, half-duplex, or simplex mode. The number of channels for split stream synchronous modems is doubled with the device. An EIA cable and two EIA receptacles are included. **Syntech Corp,** 11810 Parklawn Dr, Rockville, MD 20852.
Circle 227 on Inquiry Card

COMMUNICATION INTERFACE MODULES

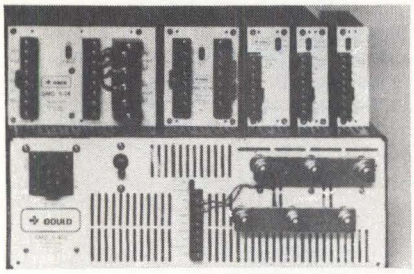
Used to repeat data, convert data from one format to another, indicate line conditions, and display faults, DR-1 is a circuit repeater converter, DR-2 a 12-circuit current loop to RS-232-C converter, and DR-3 a 12-circuit RS-232-C to current loop converter. OSA-4C provides 4-circuit current loop line monitor display and OSA-232-C serves as a 4-circuit RS-232-C line monitor and display. All modules are implemented on 4.5 x 6.5" (11.4 x 16.5-cm) PC cards. **Dataprobe Inc,** 254 Green St, South Hackensack, NJ 07606.
Circle 228 on Inquiry Card

SUBSUBMINIATURE SWITCH

B2 series basic snap-action switch, rated at 7 A, 28 Vdc or 115 Vac, features five different terminal styles, and conforms to and is qualified under M8805/4 (MS24547). Measuring 0.500 x 0.200" (1.275 x 0.508 cm), the unit provides movement differentials up to 0.005" (0.013 cm), operating force of 5 oz (140 g) max, and silver or gold contacts for low level or dry circuit requirements. The unit complements the B3 series, allowing users a choice of mechanisms. **Otto Controls Div, Otto Engineering, Inc,** 36 Main St, Carpentersville, IL 60110.
Circle 229 on Inquiry Card

PRODUCTS

SWITCHING POWER SUPPLIES



For use in enclosed unit applications in data processing and telecommunication areas, the SMG series consists of 12 5-V models at current levels from 1.6 to 450 A, three 12-V models, and three 24-V models. All units operate from a 115-Vac input. Output power ranges from 8 to 2250 W. Models with outputs of 500 W and above incorporate 115/230-Vac switchable inputs and built-in fan cooling. Power density for larger units exceeds 2 W/in^3 (0.12/cm^3). Efficiencies exceed 70%. **Gould, Inc, Electronic Components Div,** 4601 N Arden Dr, El Monte, CA 91731.
Circle 230 on Inquiry Card

DATA CARTRIDGE RECORDER

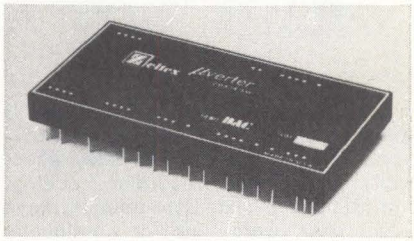
A write-only drive, the 300W utilizes the DC-300A type cartridge and can store over 350,000 characters in a single track configuration. Tapes can be written in 128- or 256-char blocks with a 16-bit CRC character as required by the ANSI tape cartridge standard, and read with ANSI-compatible cartridge readers. Input buffers accept incremental 8-bit parallel or asynchronous serial data via RS-232 or current loop. **Columbia Data Products, Inc,** 6655 Amberton Dr, Baltimore, MD 21227.
Circle 231 on Inquiry Card

IMPACT MATRIX LINE PRINTER/PLOTTERS

Incorporation of a microprocessor data communication interface enables remote printer/plotters to communicate with a computer base station over switched or private telephone lines. Interface functions by emulating Burroughs, Honeywell (VIP-7700), IBM BiSync (2780, 3780, or 3270), or Univac (DCT 1000) line protocols. Printing mechanism can plot graphics, charts, curves, bar codes, labels, and char of any size. Model 300DC operates at 300 lines/min, and 150DC at 150 lines/min. **Printronix, Inc,** 17421 Derian Ave, Irvine, CA 92714.
Circle 232 on Inquiry Card

14-BIT DAC

ZDA14QM, a modular 14-bit D-A converter, offers stability of 0.0003%; it is usable in two current or three voltage modes for either unipolar or bipolar operation. Gain, unipolar, and bipolar offsets are externally adjustable. Preselected and screened analog switches and 1-ppm/°C thin film resistors are used in design to insure accurate performance. Epoxy encapsulated case measures 2 x 4 x 0.4" (5 x 10 x 1 cm). **Zeltex, Inc,** 940 Detroit Ave, Concord, CA 94518.



Circle 233 on Inquiry Card

DC-DC CONVERTERS

Dual and triple outputs totaling up to 12 W at levels suitable for microprocessors, memories, data converters, and op amps are delivered by a family of 55 to 65% efficient dc-dc converters. The MC series of oncard local power sources offers a π input filter to reduce input reflected ripple to <1% of input voltage, I/O isolation of 300 Vdc min, and output ripple and noise of 2 mV rms (30 mV pk-pk typ). MTBF of each model exceeds 100 kh. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.

Circle 234 on Inquiry Card

WIREWRAP PANELS

Model 2-1077MPB Micro-Designer series is a 6.875 x 10.775" (17.5 x 27.4 cm) microprocessor panel featuring min of two ground planes and four power buses for mounting 120 ICs (14- or 16-pin) and discrete components. Panel has documentation package and accessories for use in engineering design and production programs. Component pin eliminates need for carriers. Panel contains plated-through holes on a 0.100 x 0.100" (0.254 x 0.254-cm) grid, available with three I/O formats. **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460.

Circle 235 on Inquiry Card

PROGRAMMABLE DIGITAL SIGNAL PROCESSOR

Range of signal processing software found on the SPS-81 is utilized at a fraction of the hardware costs by the SPS-61 high speed programmable digital signal processor. It permits asynchronous I/O tasks to proceed concurrently with processing to achieve digital processing of continuous data streams with or without host computer involvement. User programming for real-time or batch operations can be at the FORTRAN, Macro-assembler, or Microcode assembler level. **Signal Processing Systems, Inc,** 223 Crescent St, Waltham, MA 02154.

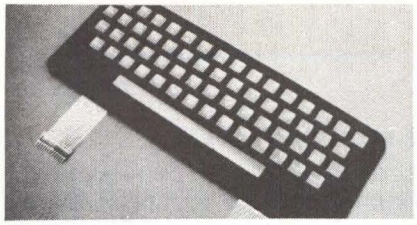
Circle 236 on Inquiry Card

MINIATURE TOGGLE SWITCHES

Toggle actuators, with color-coded plastic caps, are offered in 571 and 573 series switches. Options include five round toggles: short (0.220" or 0.559 cm), std (0.410" or 1.04 cm), and long (0.550, 0.640, and 0.840" or 1.4, 1.63, and 2.13 cm) as well as two lengths of flatted toggles (0.450 and 0.840" or 1.14 and 2.13 cm). With or without epoxy seals, 571 series offers six terminal options, while 573 series are designed for PC board mounting. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.

Circle 237 on Inquiry Card

ALPHANUMERIC KEYBOARDS



Series EA boasts a bounce of <3 ms, resistance of <50 Ω, and key travel of 0.125" (0.318 cm). Keyboards include full alphanumeric assemblies for data entry applications and provide 60 keys and a space bar with as few as 24 output lines on a flexible tail to decode all contact closures. Custom key legends and a range of coding matrices are available. **Chomerics, Inc,** 77 Dragon Ct, Woburn, MA 01801.

Circle 238 on Inquiry Card

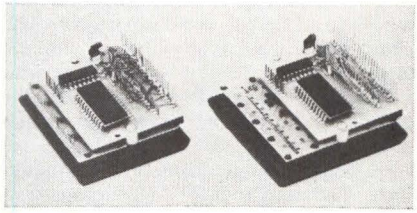
INTERCONNECT TEST SYSTEMS

Series 8210 automatic wire circuit analysis systems check electrical circuit paths of PC boards, wired backplanes, harnesses, wired racks or assemblies, and cables. System 8211 provides single real-time function with local single test station control; 8212 provides single or dual real-time functions with local or remote control of a single test station; and 8213 accommodates up to four test stations (local or remote) with real-time access to central control. A digital comparator performs resistance and voltage comparisons under program control over many decades. **DITMCO International Corp,** 5612 Brighton Terr, Kansas City, MO 64130.

Circle 239 on Inquiry Card

KEYBOARD ENCODERS

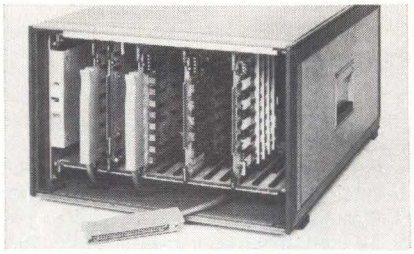
A BCD or hexadecimal encoder can be added to the company's low profile keyboard with an optional "Adder-Board." Std unit is a 16-line to 4-bit parallel data encoder providing either BCD output when used with a 10-, 12-, or 16-station keyboard; or hexadecimal output when used with a 16-station keyboard. Optional key bounce elimination circuitry provides a delayed strobe pulse. Inputs are intended to be supplied V_{CC} (5 Vdc) through keyboard switches. Outputs interface with TTL or DTL. **Stacoswitch, Inc,** 1139 Baker St, Costa Mesa, CA 92626.



Circle 240 on Inquiry Card

PRODUCTS

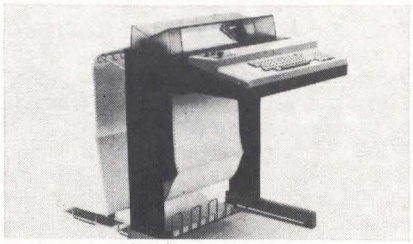
ASCII PARTY LINE SYSTEM



A mainframe which houses up to 10 programmable plug-in Smart PC cards permits automatic data acquisition and control systems to be connected without building hardware interfaces or writing software drivers. Transparent to user programs, the cards communicate with calculators, computers, and microprocessors via pre-formatted ASCII char, using decimal notations and std formats expected by the programs. ASCII party line system appears to the user's system as either a high speed teletypewriter (7000 ASCII char/s) or IEEE-488 bus instrument. **Computer Data Systems, Inc,** 186-58 Homestead, Morrison, CO 80465.
Circle 241 on Inquiry Card

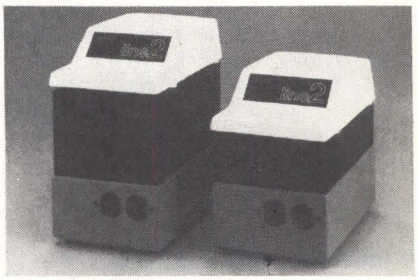
8-BIT TELEPRINTER

TC480, available in receive only (RO), keyboard send/receive (KSR), and automatic send/receive (ASR) versions, can be upgraded with optional I/O units and memory to an interactive terminal for both on- and offline data collection, time sharing, limited batch communications, text editing, and word processing. Minicomputer interface allows TC480 to operate as a console terminal. It can be equipped with RS-232, telegraphic (polar or neutral current), passive telegraphic, and 20 mA current loop options. Communication code is ASCII in 10- or 11-unit char structure, and transmission mode is asynchronous. **Olivetti Corp of America, Telecommunication Products,** 500 Park Ave, New York, NY 10022.



Circle 242 on Inquiry Card

POWER LINE CONDITIONER



Protecting sensitive electronic equipment against electrical interference, the line 2 conditioner filters and regulates electrical power. It eliminates installation of dedicated power lines needed by minicomputers, microcomputers, and other equipment. Line also protects against brownouts by automatically correcting voltages of 90 to 120 Vac to 120 Vac ±7%, or within ANSI limits. Plugged into a 120-V outlet, unit has two std 3-prong receptacles for powering equipment. Models are rated at 1 and 2 kVA. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.
Circle 243 on Inquiry Card

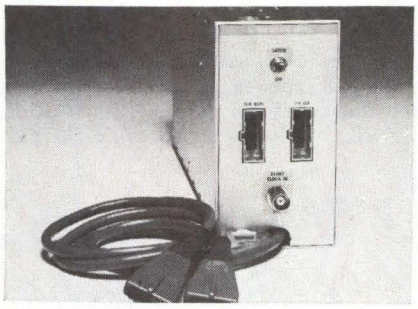
DATA COMMUNICATIONS DIAGNOSTIC UNIT

Interactive Hawk 4000 Datatrap monitors, transmits, and receives data between a modem and terminal on a 9″ (23-cm), 512-char screen. Its internal microprocessor allows quick diagnosis of data communication problems; it permits trapping and storage of 2000 char for later recall and study. System operates with BISYNC, SDLC, HDLC, and ADCCP std protocols and handles full-duplex asynchronous data rates from 75 to 19,200 bits/s and synchronous line rates up to 75,000 bits/s. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.

Circle 244 on Inquiry Card

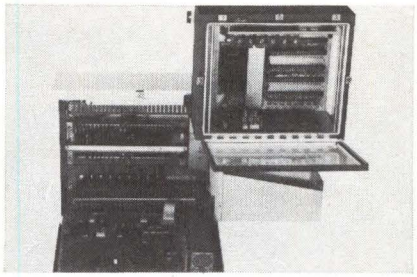
16-CHANNEL DIGITAL LATCH

The 16-channel DL 502 digital latch enhances the user's ability to make asynchronous measurements by latching pulses as narrow as 5 ns and amplitudes as small as 500 mV centered on a threshold set by the user. Device plugs into any TM 500 mainframe/power module and interfaces to the company's LA 501W logic analyzer with both housed in the mainframe. The company's P6451 low capacitance data acquisition probes connect to the latch, which can then interface to either the 7D01 or LA 501W analyzers. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.



Circle 245 on Inquiry Card

µC-CONTROLLED 10-MHz MEMORY TESTER

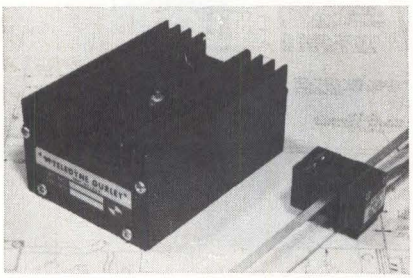


M-5 is a dedicated benchtop tester designed for production testing of memory devices, memory boards, and memory systems, and for functional burn-in testing. An 8080A microcomputer functions as test supervisor, controlling the pattern processor, programmable power supplies, control panel emulation, error mapping software, and user communications. Basic system contains two 8-bit address generators; data pattern generation is expandable from 16- to 40-bit data word widths in 8-bit increments. **Micro Control Co,** 7956 Main St NE, Minneapolis, MN 55432.

Circle 246 on Inquiry Card

PRODUCTS

HIGH RESOLUTION LINEAR ENCODER



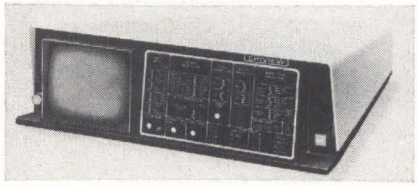
With up to 50,800 pulses/in, (2000 pulses/mm), model 8716 consists of a glass scale with vacuum-deposited chrome lines, an optical reading head that takes up <2 in³ (32 cm³), and a separate electronics package. Salient features include non-contacting, friction-free operation; output data rates up to 500 kHz; quadrature square waves or direction-sensed pulse outputs; complete DTL, TTL, HTL, or CMOS compatability; and optional zero index pulse. **Teledyne Gurley,** 514 Fulton St, Troy, NY 12181.
Circle 247 on Inquiry Card

HIGH POWER HANDLING SOLID-STATE DEVICES

Handling high electrical currents in a compact efficient form, units have a heat pipe bonded directly to the silicon wafer. This cooling technique permits production of devices which are capable of handling hundreds of watts of power, yet are 75% smaller and 85% lighter than existing devices. The transcalent semiconductors have integral heat pipes that are bonded directly to the silicon wafers. Circular fins mounted on the external part of the heat pipe radiate the heat into the surrounding environment. **RCA Corp, Solid-State Div,** Rte 202, Somerville, NJ 08876.
Circle 248 on Inquiry Card

DATA COMMUNICATIONS LINE MONITOR

Epiview accepts full-duplex data in either synchronous or asynchronous modes at speeds up to 100k bits/s, and displays them on a CRT in ASCII, EBCDIC, or hexadecimal code. In std configuration, data are displayed on an integral 5" (12.7-cm) CRT, with selected segments accentuated by character blinking and/or reverse imaging. Data stream can be viewed in real time, or can be recorded to allow later data analysis. **Epicom, Inc,** 592 N Douglas Ave, Altamonte Springs, FL 32701.
Circle 249 on Inquiry Card



MOBILE UPS SYSTEMS

PEP is designed to provide clean uninterruptible electric power to sensitive electronic equipment, and to protect this equipment from circuit fluctuations caused by voltage changes, overloaded lines, frequency shifts, or power failure. Std models output 100, 250, or 500 VA, and are complete with stainless steel cart. The system operates from internal batteries or from any std ac line, or from both. **Marine Electric RPD, Inc,** 178 National Rd, Edison, NJ 08817.
Circle 250 on Inquiry Card

MULTICHANNEL MULTIPLEXERS

In plug-in configurations for use with either single-ended or differential analog input signals, the GMM-4 provides three performance features that complement the high resolution and accuracy of the company's 15-bit GMAD-4 A-D conversion system. Input-to-output linearity is within 0.01%; input impedance of 1 GΩ assures min degradation of accuracy with high impedance signal sources; and input current offset of <20 pA permitting high impedance signal sources to be directly connected to the ADC without reducing their accuracy. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.
Circle 251 on Inquiry Card

MAG TAPE CONTROLLER BOARDS

Mag tape controllers for all Data General Nova/Eclipse and compatible computers are software transparent to the computer's operating systems. Designed with std low power Schottky, single-board controllers are imbedded in mainframe or expansion chassis. TFC 701 offers NRZI recording for all std tape drives over a speed range of 12.5 through 125 in (31.8 to 318 cm)/s; TFC 702 offers both NRZI and/or phase encoded recording techniques over the same range. **Aviv Corp,** 300 Sweetwater Ave, Bedford, MA 01730.
Circle 252 on Inquiry Card

2-SPEED SYNCHRO-TO-DIGITAL CONVERTER

Module set consists of two independent type II tracking S-D converters and a digital combiner to offer single speed and multispeed commonality, and immunity from analog crossover instability. Full 19-bit resolution reduces quantization and hysteresis error to <2.5 s of arc. Model LSI/36 2-speed modular S-D converters are based on an LSI Trig Logic™ processor and have 100-h burn-in. Specs include 10-r/s tracking on fine speed input. **North Atlantic Industries, Inc,** 200 Terminal Dr, Plainview, NY 11803.
Circle 253 on Inquiry Card

SNAP-IN LED INDICATOR

Constructed of a finned black nylon body which can be simply snapped into a 0.156" (0.396-cm) hole in the panel, the 5L4 mounts on 0.25" (0.63 cm) center-to-center. With a T-1 size red diffused LED, unit outputs 0.5 mcd min at 20 mA. Operating voltages up to 28 V are permitted with the addition of a resistor on the anode lead. Electrical specs without resistor are typ forward voltage of 1.8 V at 20 mA and max continuous forward current of 70 mA. **The Sloan Co,** 7704 San Fernando Rd, Sun Valley, CA 91352.
Circle 254 on Inquiry Card

MODULAR BATTERY RECHARGER

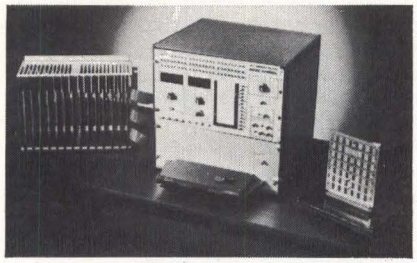
Addition of a modular charger and substitution of NiCd cells for nonrechargeable dry cells, now permits a recharge capability. Recharger measures 1.75 x 1.75 x 1.75" (4.45 x 4.45 x 4.45 cm), plugs directly into wall socket, and has snap terminals that mate with terminals of std battery holders. All that is required for recharging batteries is unsnapping the battery pack from the product and snapping it onto the charger. **Dynamic Instrument Corp,** 933 L I Motor Pkwy, Hauppauge, NY 11787.
Circle 255 on Inquiry Card

MULTICHANNEL DATA ACQUISITION SYSTEM

Model DA, a multichannel system with switching functions, is designed to accommodate from four to ten information channels. Auxiliary output signal drives remote indicators, recorders, controls, or computers for test stand monitoring or process control. Each channel has a single PC board that plugs into solidly mounted connectors, supplying transducer excitation and continuous output of 0 to 1 V. **Tyco Instrument Div,** 4 Hartwell Pl, Lexington, MA 02173.
Circle 256 on Inquiry Card

PRODUCTS

REMOTE CONTROL MUX TERMINAL



The 5000/6000 line of microprocessor-driven remote terminal units (RTUs) for hostile environment and process/industrial applications are easily interfaced with most minicomputers. They are linked to central computers via in-plant wiring, voice-grade phone circuits, microwave, or uhf/vhf radio. UART-compatible word formats and std RS-232-C serial interface permit RTU-CPU communications via std serial asynchronous interface port at rates to 1200 baud. Units can have up to 16k bytes of p/ROM-RAM. **LFE Control System Industries,** 2920 San Ysidro Way, Santa Clara, CA 95051.
Circle 257 on Inquiry Card

STORAGE MODULE CONTROLLER

Model 4091 embedded storage module disc controller provides an interface for up to two CDC storage module series (or equivalent) disc drives, with capability of mixing or matching drives. Max storage capacity is 600M bytes. Unit contains a microprocessor for monitor and control of events, execution of commands, alternate-track selection, and on-the-fly CRC generation. Designed around Data General's 4231 controller, the device runs Data General software or company software drivers that can be system generated under RDOS. **Datum, Inc,** 1363 S State College Blvd, Anaheim, CA 92806.
Circle 258 on Inquiry Card

FLEXIBLE PROBE

Unpluggable piercing flexiprobe, designed to flex on irregular surfaces, automatically realigns itself after contact with a test point, and penetrates any substance or residue on solder joints to give an accurate test reading of circuit boards. It can be inserted into front or rear loading receptacles and is interchangeable with all of the company's matching barrel diam unpluggable probes. **Ostby and Barton,** 487 Jefferson Blvd, Warwick, RI 02886.
Circle 259 on Inquiry Card

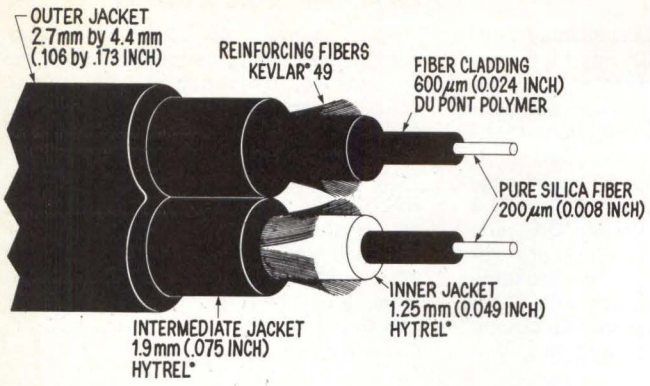
TIME DIVISION MULTIPLEXER

Designed primarily for multiplexing/demultiplexing two simultaneous teleprinter messages with rates of 50 baud each in a full-duplex communication of 75 baud over a single line, unit possesses four switch operational modes: MUX, A ONLY, B ONLY, and LOOP. For single line mode, 50-baud carrying line is connected directly to long distance line, with the remaining subscriber line connected to an additional teleprinter, via AUX socket. **Koor Systems Ltd,** Sgoola Industrial Zone, PO Box 76, Petach Tykva, Israel.
Circle 260 on Inquiry Card

PE/NRZ MAG TAPE CONTROLLER

A plug-in single-board dual density controller, the TC-140 features total software compatibility with existing Interdata operating systems. With all interface and formatting electronics for both PE and NRZ, unit operates via selector channel or multiplexer bus. Up to four drives can be handled in any combination of 7-track NRZ, 9-track NRZ, 9-track PE, or 9-track PE/NRZ, at any two speeds in the range of 12.5 to 125 in (30.5 to 317.5 cm)/s. **Western Peripherals, Inc,** 1100 Claudina Pl, Anaheim, CA 92805.
Circle 261 on Inquiry Card

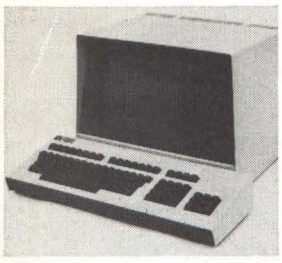
DUAL-CHANNEL SILICA CORE FIBER OPTIC CABLE



Designed for 2-way communication, PFX-S220R cable resists physically hostile environments. Two inner cables, color-coded for identification, are reinforced with Kevlar 49 aramid fiber in a protective jacket of Hytrel polyester elastomer. Typ properties are 40-dB/km at 775 nm attentuation (50-dB/km at 820 nm), 0.4 (calculated) numerical aperture, 0.27 (−10 dB) exit numerical aperture, and core diameter of 200 μm. Silica core is well-centered within a tough hard cladding to which a connector may be directly crimped. Cables are resistant to radiation, vibration, microbends, impact, water immersion, and temp cycling from −80 to 150°C. Run lengths up to 1 km are possible. **E. I. du Pont de Nemours & Co, Plastic Products and Resins Dept,** Wilmington, DE 19898.

Circle 262 on Inquiry Card

CRT DISPLAY TERMINALS



A Teletype™-compatible display terminal with roll or page mode of operation utilizing the ASCII code set, model 200 features 80 x 24-char display, 9 x 9 dot matrix, character mode transmission, RS-232-C and 20/60-mA current loop interface, and 16 switch-selectable data rates up to 19,200 bits/s. The unit's detached solid-state keyboard comes in five different configurations. Model 400 is a multifunctional terminal using the ASCII code set. Advanced functionality results from the internal Z80 microprocessor and firmware design. Capabilities include complete formatting and editing with block mode transmission, as well as character mode for normal log-in procedures or straight character operation. **Infoton,** 2nd Ave, Burlington, MA 01803.

Circle 263 on Inquiry Card

DATA CONVERTER

BAC-2780 receives EBCDIC data via IBM binary synchronous protocol, performs required error-checking functions, translates data to ASCII, and outputs them in serial asynchronous format to a user-attached receiving device. IBM bisync protocol with CRC-16 error checking allows error-free operation, yet the user can attach a peripheral device equipped with asynchronous ASCII RS-232-C interface. In operation, the unit receives data via a modem connection at modem-specified data rates up to 9600 Hz. The converter and its attached peripheral output device emulate an IBM 2780 receive-only terminal. Additional features include data transparency protocol and full BSC handshaking. **KMW Systems Corp,** 11807 Royalton Rd, North Royalton, OH 44133.

Circle 264 on Inquiry Card

PRODUCTS

TAPELESS NUMERICAL CONTROL

CalCuTrol 52, a 5-digit, 2-axis control, combines a pocket calculator's simplistic operation with a microcomputer's programming sophistication and contains keys, displays, logic, and power supplies needed to drive two stepping motors in an open-loop configuration. Unit accepts random mixture of absolute and incremental data. Control features include insert/delete, high and low speed program examine, nine subroutines, ten canned programs, 475 sequences, and condensed step/repeat format. **Automation Unlimited, Inc,** 120 New Boston Pk, Woburn, MA 01801.
Circle 265 on Inquiry Card

DUAL, ALPHANUMERIC LED DISPLAY

Hercules model 1785 LED display consists of two 0.54" (1.37-cm) high, red 14-segment char combined in a single package, which can display alphanumeric char plus some symbols. Composed of GaAsP emitting material, solid-state displays have typ 600 μcd/segment luminous intensity at 20 mA/1.6 V_F. The 18 horizontal double DIP pins on 0.100" (0.254-cm) spacing are set up for multiplex drive. End stackable units have common cathode with right-hand decimal point. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.
Circle 266 on Inquiry Card

CRYSTAL CLOCK OSCILLATORS

HY-4560 low power CMOS oscillator operates from 5- to 15-Vdc power supply, draws only 20 mW, and can be furnished at any frequency from 600 Hz to 5 MHz. Requiring a 5-Vdc power supply, HY-4550 250 kHz to 50 MHz oscillator is TTL compatible. Both units measure 0.815 x 0.515" (2.07 x 1.31 cm) with a seated height of 0.200" (0.508 cm) and possess frequency stability of $\pm$0.01% over specified operating conditions. **Hytek Microsystems Inc,** 16780 Lark Ave, Los Gatos, CA 95030.
Circle 267 on Inquiry Card

QUAD BACKPLANE OPTION TO FLOPPY DISC SYSTEM

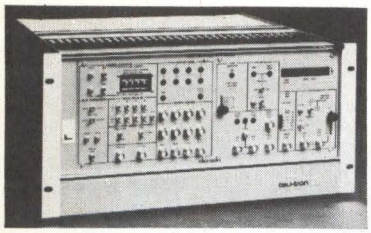
MF-11 floppy disc/LSI-11 system doubles backplane capacity through its optional H9270 quad backplane. Functionally identical to the PDP-11/V03, and using only 10.5" (26.7 cm) of rack space, it houses the Shugart dual floppy system, front panel console, DEC H9270 quad backplane, and power supply. System accommodates additional interface cards for various LSI-11 peripherals. **Charles River Data Systems, Inc,** 235 Bear Hill Rd, Waltham, MA 02154.
Circle 268 on Inquiry Card

INTELLIGENT REMOTE CONTROLLER

An S-100-based computer control system that communicates over std 110-Vac power lines, the Introl™ system is intended to control appliances and equipment, or read status information at remote locations without the need for direct wiring. The AC Controller™ board is S-100-compatible, controlling up to 64 remote units; AC Remote™ unit has two independently controllable ac sockets that can turn two 500-W appliances on or off. Computer can also poll the remote to check on/off status. **Mountain Hardware, Inc,** PO Box 1133, Ben Lomond, CA 95005.
Circle 269 on Inquiry Card

MAGNETIC TAPE TEST SYSTEM

MBG-1 magnetic media BERT permits selective measurements of bit error on magnetic tape systems in the frequency band from 1 bit/s to 50M bits/s. The unit fully stresses systems by providing a broad range of pattern generation and detection capability to cause the magnetic tape media as well as associated electronics to exhibit failure modes. In record mode, the instrument allows for combinations of switch-programmable words up to 2048 bits long to be interleaved with pseudorandom sequences ranging in length from 63 bits to approx 1M bits. In play back mode, error rate measurements can be made on either switch-programmable data field or pseudorandom data field as well as the composite. **Tau-Tron,** 11 Esquire Rd, Billerica, MA 01862.



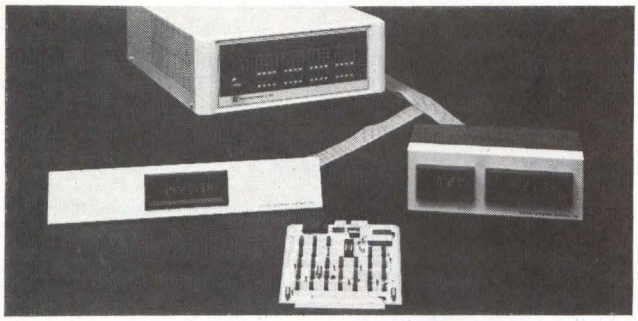
Circle 270 on Inquiry Card

LOGIC ANALYZER DISPLAY FORMATTER

Designed to expand capabilities of 50D and 50D16 logic analyzers, model 50D011 permits display of digital data on any std XY display or XY oscilloscope in timing domain, data domain, or map mode format. Data can also be viewed as either positive or negative true. In timing domain format all 16 lines and 510 bits of digital data, stored in the logic analyzer's memory are shown horizontally across the display. Cursor, trigger marker, and cursor readout operate as in the basic analyzer. In data domain format, sixteen 16-bit words, with their respective addresses and hex/octal conversions, are displayed in binary form according to the position of the cursor. Map mode generates an XY plot of data stored in memory, arranging them in a 4 x 4 (50D) or 8 x 8 (50D16) configuration. **BP Instruments, Inc,** 10601 S De Anza Blvd, Cupertino, CA 95014.

Circle 271 on Inquiry Card

REAL-TIME CLOCK FOR TI 960/990

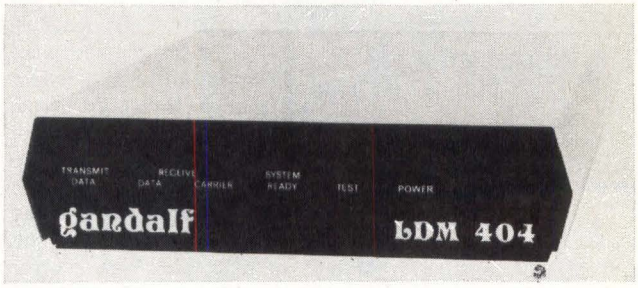


Clock models 960-030 and 990-030 are designed to operate as CRU interface cards, to provide hardware time and data support for 960 and 990 computer systems. Provision for battery backup allows time and date information to be maintained during power loss, eliminating need for operator initialization of time and data software counters. Operating systems on both computers can be modified to read time and data information directly from the clock module, providing long term accuracy not available with software counters. The 60-Hz line frequency supplies an accurate timebase under normal operation, while a crystal-controlled oscillator is used during power failure. **Digital Interface Systems, Inc,** PO Box 1446, Benton Harbor, MI 49022.

Circle 272 on Inquiry Card

PRODUCTS

LIMITED DISTANCE MODEM

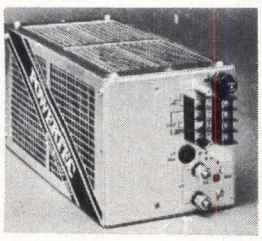


LDM404B, designed for full-duplex synchronous communication at 4800 bits/s, operates over 4-wire voice grade metallic lines (conditioned or unconditioned) and T carrier and most other carrier systems, and is suitable for use in metropolitan areas for mid-range applications where short haul units are not satisfactory but distances do not warrant the cost and complexity of long haul modems. Transmitter uses quaternary amplitude modulation followed by frequency translation to a narrow band centered in the voice channel. Receiver performance is optimized by delay equalizing with digital filtering techniques and using custom designed hybrid active phase processing networks. **Gandalf Data Inc,** 1019 S Noel, Wheeling, IL 60090.
Circle 273 on Inquiry Card

HIGH DENSITY STATUS/ALARM DISPLAYS

From eight to 64 alarm points are monitored in a unit only 1.75″ (4.45 cm) high which can be rack, panel, or desk mounted. This high density packaging is suitable for applications requiring visual alarm annunciation. Control logic monitors status of alarm points. A pair of indicator lamps assigned to each point display status: green represents normal and red alarm. In event of alarm, the appropriate indicator lamp will show a flashing red display; simultaneously, a pulsating audible alarm will sound. Alarm inputs may be either NC or NO contacts or 24 Vdc, 48 Vdc, or ground voltage. Unit can be powered by 115 Vac, 24 Vdc, or 48 Vdc. All std ISA sequences are available. **Puleo Electronics, Inc,** 415 Merchant St, San Francisco, CA 94111.
Circle 274 on Inquiry Card

MULTIPLE-OUTPUT SWITCHING SUPPLY



A natural convection-cooled unit that provides up to three independent dc outputs from 2 to 28 V, the 9F is available with a variety of current ratings (eg, 9F250TC-006 provides 5 V at 40 A, 12 V at 2.1 A, and 5 V at 5 A). Operation at 40 kHz not only eliminates heavy and large low frequency magnetic elements, but also insures silent operation. Efficiency of approx 80% minimizes heat dissipation and provides economical operation. The unit accepts either 115- or 230-Vac line input with a tolerance from −20% to 10%. This tolerance combined with a 30-ms storage time makes the supply virtually brownout proof. Built-in overvoltage and overload protection are provided along with input fusing and soft-start circuitry. **Powertec, Inc,** 9168 De Soto Ave, Chatsworth, CA 91311.
Circle 275 on Inquiry Card

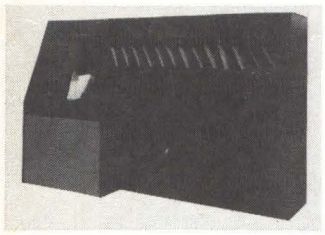
PROCESSORS WITH UP TO 128k WORDS OF MEMORY

PDP-8A/205, 425, and 625 processors incorporate a KT8-A memory management option in all configurations having from 32k to 128k words of core, MOS, or mixed core and MOS memory. The MS8-C MOS memory modules, available in both 16k- and 32k-word configurations, use 4k RAMS for high density. KT8-A and MS8-C modules permit current PDP-8/As to be upgraded to 128k-word capacity. The memory management option is software-compatible with programs written for -8s and permits access to the entire 128k words of memory by program and DMA devices. It also allows extended virtual field addressing, memory protection, and reduced operating system overhead. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 276 on Inquiry Card

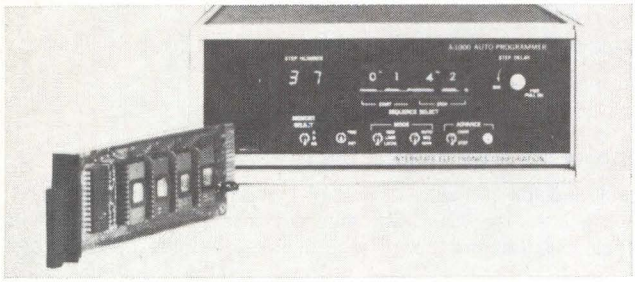
DOCUMENT READER/SORTERS

The 92660 and 92680 can read and sort encoded checks, credit card charges, customer billings, and food coupons at speeds over 35,000 documents/h. The smaller 92660 reader/sorter separates magnetically encoded documents according to predetermined sets of characteristics and groups similar documents into individual pockets. Primarily for use in check processing applications, it features a MICR system that captures data from documents conforming to ABA spec 147R3 or ANSI X3.3, processing documents at rates up to 830 6" (15-cm) documents/min. 92680 contains 14 document pockets and optional OCR and OMR reading capabilities which can capture magnetic as well as optical characters and marks from intermixed documents in a single pass. **Control Data Corp,** Box O, Minneapolis, MN 55440.



Circle 277 on Inquiry Card

INSTRUMENTATION CONTROLLER FOR ATE SYSTEMS



A-1000 Autoprogrammer is specifically designed for the company's SPG-800 programmable generator, but can also interface with other ASCII format equipment. For incoming or production inspection, calibration, or quality-control applications, the controller drives an SPG-800 linked to the UUT. Test unit is then connected to a programmable DVM and a printer, both of which may be controlled by the device. In operation, the autoprogrammer sends the generator specifying commands for parameters such as waveform, frequency, and amplitude; the generator in turn produces the signal needed for the UUT. Data from the tested device are read out on the DVM and hardcopied on the printer. The unit can be programmed to insert time delays from 1 to 10 s in multiples of 25 ms. **Interstate Electronics Corp,** 707 E Vermont Ave, Anaheim, CA 92803.

Circle 278 on Inquiry Card

PRODUCTS

MINIATURIZED 6250-BIT/IN TAPE SUBSYSTEM

Offering minicomputer users four times the tape capacity in one-fourth the space, model 6250, a 6250-bit/in (2460/cm) magnetic tape subsystem, is available in std 19" (48-cm) EIA rackmount configurations. Transport is designed to fit PE and GCR data formats. A lower performance 6240 model, differing in only three plug-in modules and head assembly, operates with NRZI and PE data formats. Available in 45-, 75-, 100-, and 125-in/s (114, 190, 254, and 317 cm/s) configurations, units transfer data at rates up to 781k bytes/s, and have a rewind speed of 500 in/s (12.7 m/s). Subsystem includes a microprogram-controlled formatter/controller which can accommodate up to eight tape transports and can intermix any combination of up to four speeds and three tape densities. **Telex Computer Products, Inc,** 6422 E 41st St, Tulsa, OK 74135.

Circle 279 on Inquiry Card

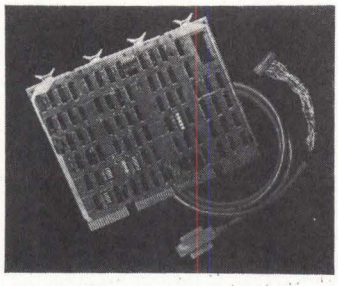
FIXED-HEAD DISC SUBSYSTEMS

High performance head/track disc subsystems using Winchester-type technology provide high speed, extended controller features, and configuration flexibility necessary for applications requiring high speed data access or data acquisition rates. The subsystems transfer data at 910k bytes/s and have an avg access time of 10.12 ms. Drives are available in 2M-byte (model 6064) and 1M-byte (6063) capacities. Both are 8.75" (22.22-cm) high rackmounted units. Max subsystem capacity is four drives per subsystem in any combination of the two sizes. For use with Nova or Eclipse computers, the units are supported by multiprogramming advanced operating system (AOS) and real-time disc operating systems (RDOS). **Data General Corp,** Rte 9, Westboro, MA 01581.

Circle 280 on Inquiry Card

PDP-11 TO IEEE-488 BUS INTERFACE

Designed for use with DEC PDP-11 computers, the GPIB11-1 interface to the IEEE Std 488-1975 bus is configured as a single quad-height board which plugs directly into a small peripheral controller slot, allowing the PDP-11 to talk, listen, or control up to 14 instruments on the bus. Hardware decoding of bus command messages ensures high speed operations. Software is provided as utility and driver programs that are available as macro source files which may be assembled as FORTRAN, BASIC, or macro-callable subroutines. Interface includes a 2-m cable with a std bus connector on one end. **National Instruments,** PO Box 9922, 8330 Burnet Rd, Austin, TX 78758.



Circle 281 on Inquiry Card

LITERATURE

Supervisory Control Equipment

Block diagrams and descriptions are given in brochures describing series 8000, a master station designed for small to moderate size supervisory control and data acquisition systems. **Harris Corp, Controls Div,** Melbourne, Fla.
Circle 300 on Inquiry Card

Acoustic Telephone Coupler

Data sheet describes the model 503A acoustic coupler, designed to interface with any std LA36 terminal for conversational timesharing of a remote computer system. **Omnitec Data,** Phoenix, Ariz.
Circle 301 on Inquiry Card

Digitizing Systems

Folder defines the process of and application for sonic digitizing, and details specific applications for data converters, interfaces, and related devices. **Science Accessories Corp,** Southport, Conn.
Circle 302 on Inquiry Card

Rack Mounted Modems

Data sheet describes and illustrates the 113BR2 FCC-registered LSI modem that transmits and receives binary serial data at rates up to 300 bits/s. **General DataComm Industries Inc,** Wilton, Conn.
Circle 303 on Inquiry Card

Connecting Systems

Connectors, relay sockets, metal plating and anodizing, systems installation hardware, and fluid systems are presented in condensed catalog containing features and photographs. **Viking Industries, Inc,** Chatsworth, Calif.
Circle 304 on Inquiry Card

Programmable Controllers

Foldout bulletin, including diagrams and condensed specs, outlines the Automate® 31M and 31ML microprocessor-based controllers that incorporate functional programming language. **Reliance Electric,** Cleveland, Ohio.
Circle 305 on Inquiry Card

Screened Image Displays

Application note provides an overview of SP-400 screened-on-glass, planar gas discharge displays by encompassing a description of family characteristics, applications, and specs. **Beckman Instruments, Inc, Information Displays Operations,** Fullerton, Calif.
Circle 306 on Inquiry Card

CCITT V.35 Interface

Wallet card and stick-on labels contain a chart that gives pin assignment, common mnemonic name, direction of signal flow, RS-232 or V.35 spec, and function of each signal in terminal-modem interface. **International Data Sciences, Inc,** Providence, RI.
Circle 307 on Inquiry Card

Switches

Catalog, comprised of photos, line drawings, and specs, describes slide, snap action, rotary, pushbutton, toggle, leaf, rocker, and paddle switches. **Chicago Switch, Inc,** Chicago, Ill.
Circle 308 on Inquiry Card

CMOS Microprocessor Components

Features, descriptions, functional diagrams, and instruction summary are given in 20-pg brochure on the 1800 family of LSI components. **Hughes Aircraft Co, MOS Products,** Newport Beach, Calif.
Circle 309 on Inquiry Card

Digital Datalogging

Benefits of digital datalogger are demonstrated in booklet that covers data reliability, noise rejection, low cost alarm annunciation and process control, and operation with online computer systems. **Acurex Autodata Inc,** Mountain View, Calif.
Circle 310 on Inquiry Card

Timeshared Microcomputer System

Brochure lists features, utilities, and systems available for S-100 bus-compatible Alpha Micro multiuser, multitasking software development system. **MicroAge,** Tempe, Ariz.
Circle 311 on Inquiry Card

Card Edge Connectors

Series "AC" gold dot connectors are featured in brochure that includes a cutaway diagram, statistics, and technical information on contact type and tail length, number of positions, dimensions, and options. **GTE Sylvania Inc,** Titusville, Pa.
Circle 312 on Inquiry Card

Data Communications

Handbook, "Telecommunications from the Terminal User's Viewpoint," covers technical aspects and applications of modems, automatic dialers, and associated equipment with diagrams and graphs. **Vadic Corp,** Sunnyvale, Calif.
Circle 313 on Inquiry Card

Alphanumeric Impact Printer

Standalone model AIP-40 printer with a 50-char/s rate is discussed in booklet containing block and timing diagrams, and electrical and mechanical specs. **Datel Systems, Inc,** Canton, Mass.
Circle 314 on Inquiry Card

Microminiature Connectors

Miniature rectangular, circular, center jackscrew, and strip connectors, available in densities up to 1600 contacts/in^2, are depicted through dimensional diagrams, electrical specs, and std wire terminations in 64-pg catalog. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 315 on Inquiry Card

Thyristor Gating

Application report describes use of triacs, SCRs, and thyristors in microprocessor-based control systems, noting factors involved in coupling, isolation, transient noise problems, and circuit malfunction protection. **Texas Instruments Inc,** Dallas, Tex.
Circle 316 on Inquiry Card

Variable Resistors

Series 550 of 2-W, 0.75" (1.9-cm) diam cermet resistors are depicted through dimensional drawings in catalog that also includes electrical and mechanical characteristics. **CTS Corp,** Chicago, Ill.
Circle 317 on Inquiry Card

DIP Headers

Catalog on DIP header series 600, 625, and 8625, and pin line header series 0600 and 0625 gives dimensioning, material details, and available platings. **Aries Electronics, Inc,** Frenchtown, NJ.
Circle 318 on Inquiry Card

Component Burn-In

Graphs, charts, tables, photographs, applications, typ burn-in load circuits, and glossary of terms characterize handbook on component burn-in technology. **Wakefield Engineering, Inc, Systems Div,** Wakefield, Mass.
Circle 319 on Inquiry Card

Power Cords

Catalog presents technical and application details, physical and electrical specs, and illustrations on type SJT shielded and unshielded electronic cords for data handling equipment. **Belden Corp, Electronic Div,** Geneva, Ill.
Circle 320 on Inquiry Card

LITERATURE

Low Profile DIP Relay

Features, applications, and dimensional diagrams comprise brochure illustrating the sensitive dpdt electromechanical relay that fits std 16-pin IC sockets. **Gould, Inc, Control and Systems Div,** Plantsville, Conn.
Circle 321 on Inquiry Card

Teleprinters

Illustrated with photogaphs, brochure lists features and specs for the EDT 1232 line of 120-char/s teleprinters. **Western Union Data Services Co,** Mahwah, NJ.
Circle 322 on Inquiry Card

Indicator Lights and Lampholders

Short-form catalog covers features, dimensional drawings, and electrical and mechanical specs of std lenses, incandescent and neon indicators, cartridge hardware, and lampholders. **Chicago Miniature Lamp Works, General Instrument Corp,** Chicago, Ill.
Circle 323 on Inquiry Card

Monopanel Keyboards

Brochure lists detailed product specs, dimensional drawings, schematic diagrams, and output code charts for 12- and 16-key keyboards with alphanumeric or telephone format nomenclature. **Centralab Electronics Div, Globe-Union Inc,** Milwaukee, Wis.
Circle 324 on Inquiry Card

Magnetic Media Measurements

Brochure contains techniques utilized in making digital measurements and includes a description of typical stress patterns as well as the making of measurements on selected portions of these patterns. **Tau-Tron, Inc,** North Billerica, Mass.
Circle 325 on Inquiry Card

Scanning Systems

Line of computer-assisted, high speed and precision digital flatbed scanning systems is encompassed in brochure that points out descriptions and operating specs for each model. **Optronics International,** Chelmsford, Mass.
Circle 326 on Inquiry Card

10-Col Thermal Printhead

Bulletin on DM-1050, a printhead that allows nonimpact printing at speeds to 8 lines/s, specifies descriptions, features, performance characteristics, application data, thermal paper manufacturer listing, and dimensional drawings. **Gulton Industries, Inc, Hybrid Microcircuit Dept,** Metuchen, NJ.
Circle 327 on Inquiry Card

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An annual listing of articles, columns, product features, and special items

Information Theory

An Asynchronous Arbiter Resolves Resource Allocation Conflicts on a Random Priority Basis, K. Søe Højberg .....Aug, p 120

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Two-Step Procedure Improves CRC Mechanism, P. J. Fortune .....Nov, p 120

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Single Architecture Terminal Combines Graphic and Alphanumeric Capabilities .....Apr, p 150

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Flat Panel Displays Offer Graphics Alternatives, J. W. Aichroth .....Oct, p 101

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Single Architecture Terminal Combines Graphic and Alphanumeric Capabilities .....Apr, p 150

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Peripheral Interfacing With Microprocessors, A. J. Weissberger .....Feb, p 108

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Computer Graphic Family Offers Multifunction Capability .....Dec, p 150

Printer/Plotter is Price-Compatible with Microprocessor Systems .....July, p 146

Voice Response Equipment

Design Guidelines for a Computer Voice Response System, P. Thordarson .....Nov, p 73

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Analog-Digital and Digital-Analog Conversion Equipment

Highly Stable Analog-to-Digital Converter, NASA .....Jan, p 106

Low Cost A-to-D Conversion During Microcomputer Idle Time, H. A. Raphael .....Mar, p 112

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

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Terry Buckley—Tom Boris
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Los Angeles, CA 90049
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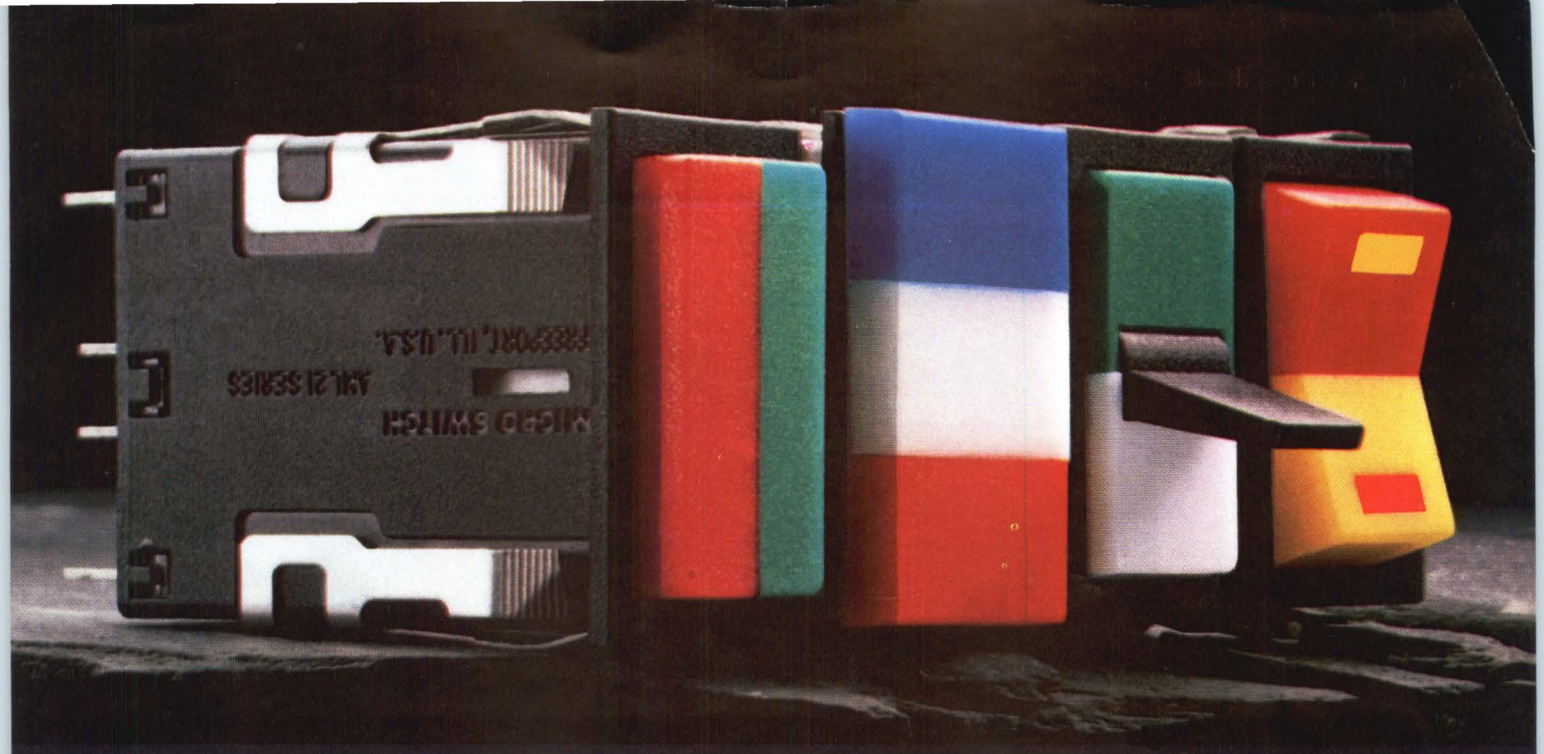
ADVERTISERS' INDEX



To make a complete line of pushbutton controls, you need more than pushbuttons.

Pushbuttons from MICRO SWITCH's AML (Advanced Manual Line) have always been attractive to designers. Because they look so good. And because they're so easy to mount and wire.

But now, the AML series is even more appealing. Because now there's a variety of rocker and paddle switches to choose from, including dual lamp and dual color. Which means now you can perform just about any function with a harmonious display. You don't have to compromise.

AML controls also look appealing to the people who have to do the wiring. All are designed with the same depth for single level termination, regardless of switch or terminal type.

There's easy snap-in mounting from the front, PC board mounting or subpanel mounting using individual, strip or matrix hardware.

Which means mounting is simpler. Wiring is simpler. Engineering time is reduced. And total installed cost is lower.

Plus, they offer solid state, electronic control or power switching in the same size housing. All AML devices are designed to meet international, UL and CSA standards.

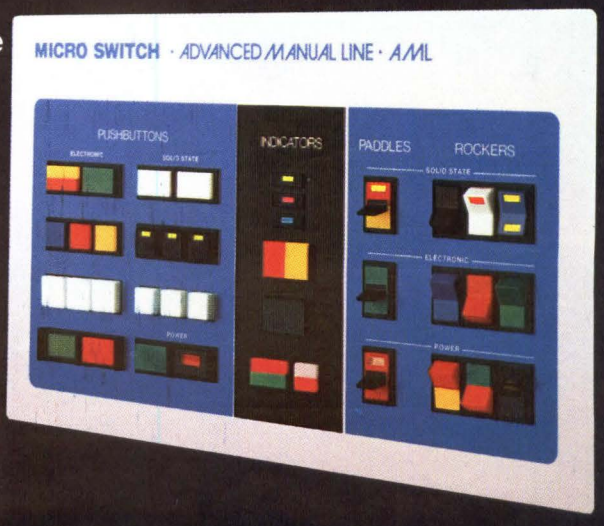
Displays include split screen, hidden color, and a unique three-segment lens cap indicator. The choice of lamps includes T-1¾ wedge base, neon and LED.

AML has it all —pushbuttons, indicators, and now, paddles and rockers. But to see how good-looking AML really is, contact us for a personal demonstration.

MICRO SWITCH will provide you with field engineers for application assistance and a network of authorized distributors for local availability. Write us for details or call 815/235-6600.

MICRO SWITCH products are available worldwide through Honeywell International.

MICRO SWITCH
FREEPORT, ILLINOIS 61032
A DIVISION OF HONEYWELL



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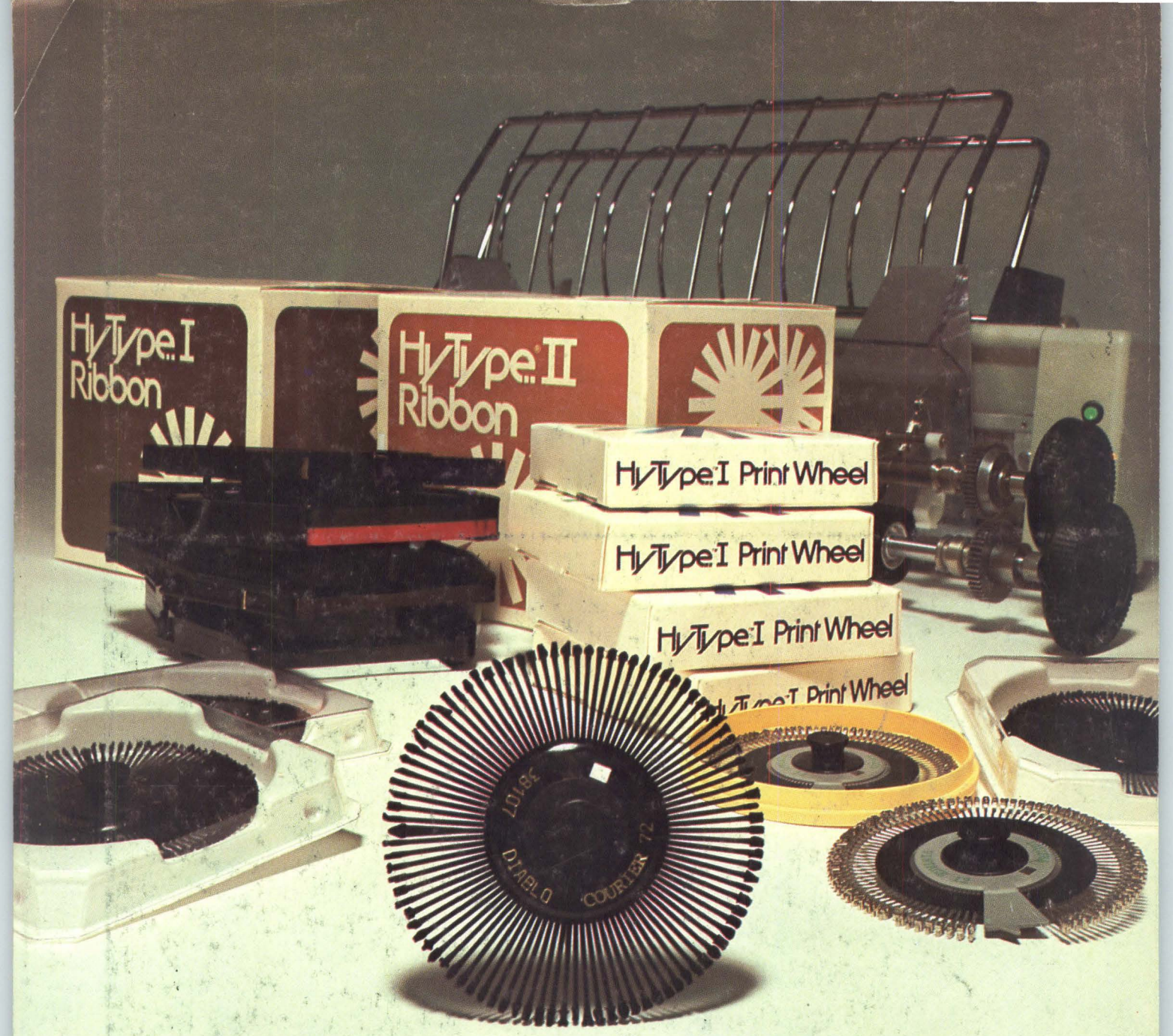

Diablo Daisy Power

Diablo Delivers More Features, Options, And Technology!

Diablo HyType daisy wheel printers give you everything you need to add customer sales appeal to your system! We offer the largest selection of plastic and metal-clad printwheels in a wide choice of fonts and languages. To make our printers easy-to-use, you can choose from a whole range of cloth and carbon ribbon cartridges in colors or black. Add to that our split platen and varied paper and forms handling features and you've got operation easy as a, b, c! Then there's our exclusive internal power supply, a front feed inserter, even proportional spacing on our word processing mechanisms. And behind it all are the combined resources of Diablo and Xerox, dedicated to maintaining our leadership role in daisy technology. After all, we invented it in the first place! Diablo Systems, Inc., 24500 Industrial Blvd., Hayward, CA 94545, Diablo Systems, S.A., Avenue de Fre 263, 1180 Brussels, Belgium and Mitsui & Company, Ltd., 2-1, Otemachi, 1-Chome, Chiyoda-ku, Tokyo.

Diablo

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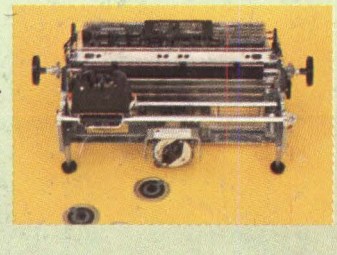

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