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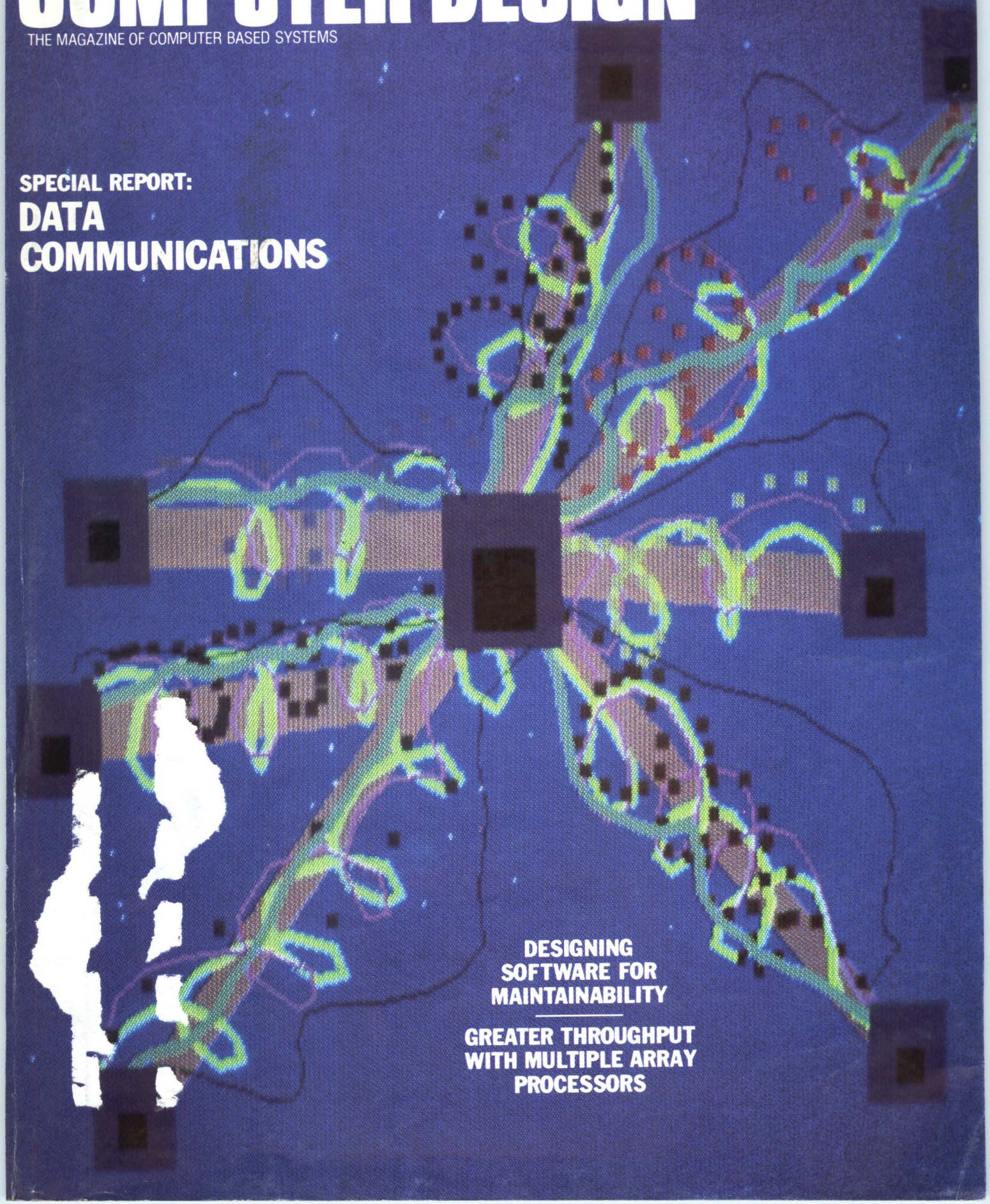
SEPT. 1981

COMPUTER DESIGN

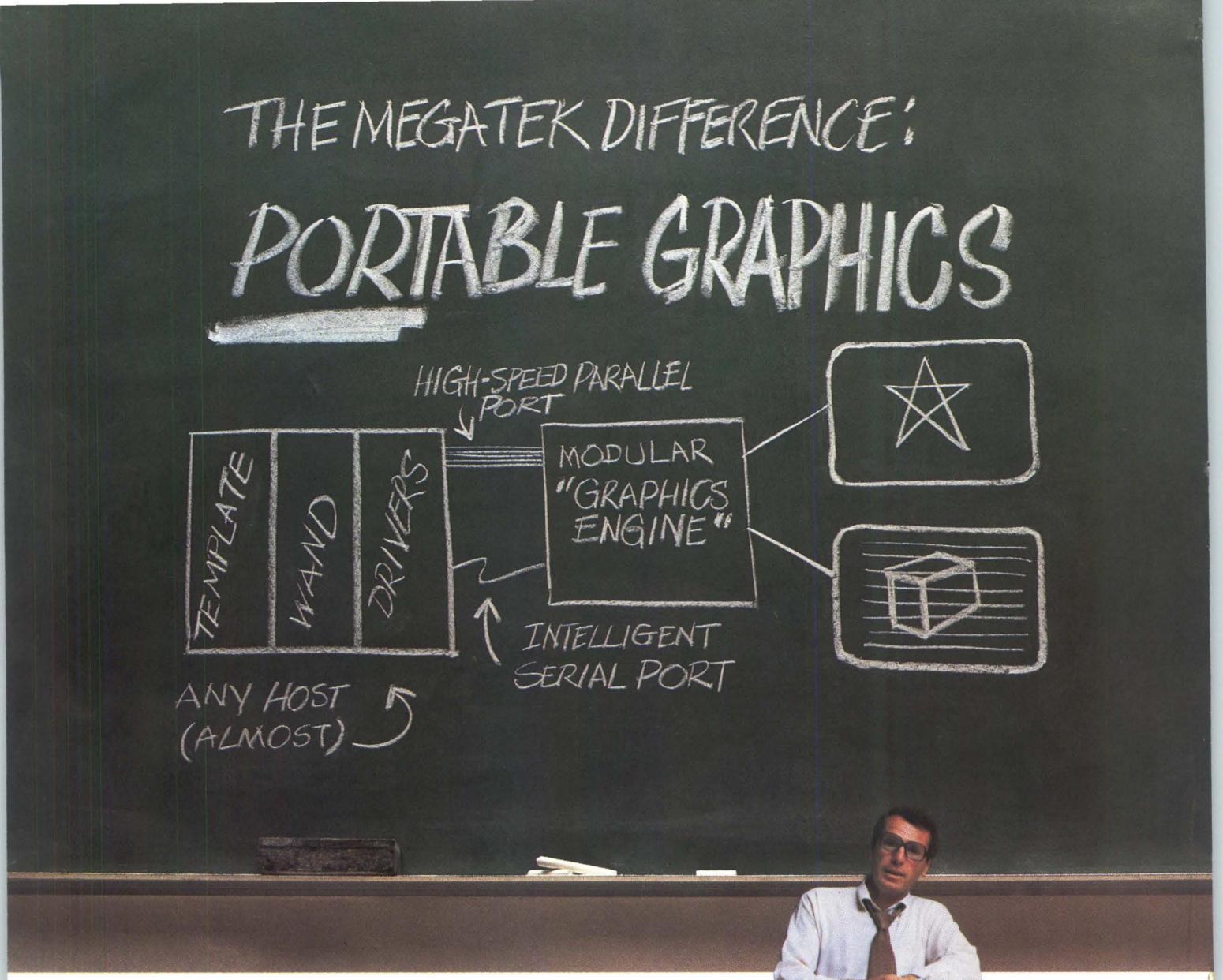
THE MAGAZINE OF COMPUTER BASED SYSTEMS

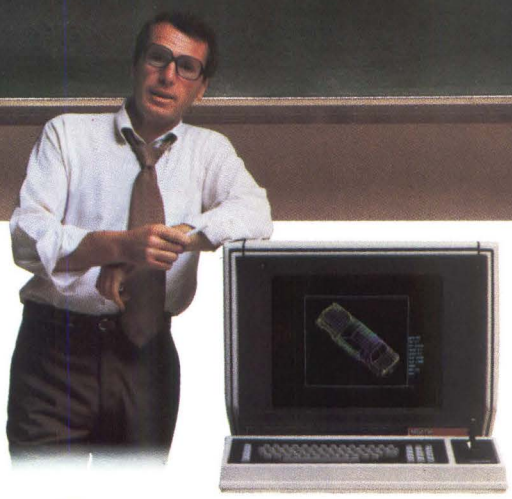


SPECIAL REPORT:
DATA COMMUNICATIONS

DESIGNING SOFTWARE FOR MAINTAINABILITY

GREATER THROUGHPUT WITH MULTIPLE ARRAY PROCESSORS





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The new T-1805 dual purpose serial printer uses a unique 40 x 18 matrix dot pattern for high quality correspondence printing; or, flip a switch, it uses a 7 x 9 matrix for high speed data processing printing. In the high speed mode, it generates reports at time-saving throughput rates reaching 200 lines per minute. In the reduced speed correspondence mode, its pivoting print head lays down overlapping dots to create a letter-perfect character that looks like it came from an office typewriter.

The T-1805 is the latest evolution in the popular and proven T-1000 series of serial printers. As such, the T-1805 offers the same quality construction, high reliability, ease of operation and operator conveniences. Plus, for the benefit of the office crew, the T-1805 is exceptionally quiet. Its 53 dbA noise level ranks it as the quietest impact printer on the market.

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CIRCLE 3 ON INQUIRY CARD

UP FRONT

Reader's road map to the new *Computer Design*

In redesigning our magazine, we're changing everything from Cover to Cover. This month you can't miss our new Cover design, prepared using computer graphics; it has a brand new look. The single Contents page has blossomed into a 2-page spread, giving us more room to point out special items being covered and where to find them in the magazine. And, in this section—UP FRONT—in coming months you'll find special announcements and encapsulated versions of late breaking events.

Other things are different too

Instead of dividing up all the information into special departments, we're going to concentrate it in three main sections: SYSTEM TECHNOLOGY, SYSTEM DESIGN, and SYSTEM COMPONENTS. Within these sections, you'll find reports on what's happening in Data Communications, Test and Measurement, Computer Based Systems, and every other area related to computer technology and computer based systems design.

To find what you're looking for

Take a look at the Contents page. There under System Technology you'll find articles on Data Communications, Control and Automation, Data Conversion, Computers, and several other subjects. Listed under System Design are Software, Computer Based Systems, and Memory Systems; and under System Components, the list begins with Data Communications and goes on to System Elements. All include page numbers to help you locate them in the magazine.

What's covered where

System Technology encompasses in-depth reviews of important technological developments that have a potential impact on the systems you are involved in developing. Staff written articles will point out what's important about particular subsystems, how developments took shape, or why an emerging technology may become important to you.

System Design collects contributed and solicited articles written by you or your contemporaries that cover technical aspects of digital design, development and applications of devices, equipment, and systems, as well as engineering ideas and techniques. Within this section a Special Report made up of four or five articles concentrates on a major subject area. This month, for example, the emphasis is on Data Communications. In November, Control and Automation will be the Special Report.

System Components showcases recently introduced products in every area of interest. This section should help keep you up to date on what's available, what the specs are, who makes it, and how much it costs.

And in the months to come

Next month you'll see a change in format designed to make our pages more exciting and easier to read. Most important, however, is that despite changes, *Computer Design* will continue to evolve as a valuable source of information to OEM system designers and will strive to serve you as well as it has for the past 20 years.

UP FRONT

IBM produces Applesauce?

From an unfamiliar, come-from-behind position, IBM announced its $1565 entry and its intentions to compete in the personal computing market. The contestant, a powerful 16-bit machine, displays the power to handle larger, more demanding tasks than those handled by rivals at a competitive price, and comes with a label signifying compliance with FCC emi interference regulations. CP/M and UCSD p-Code system software packages allow existing applications packages to be transported to the machine with minimal modifications.

First FCC deadline approaches

All Class A computing devices (commercial, industrial, and business) first manufactured after October 1, 1981, must be verified by the manufacturer for compliance with the new FCC emi standards. The compliance standards are detailed in Part 15, Subpart J, of the FCC Rules and Regulations. Copies of Volume 2, *Revised Basic Manual,* containing Part 15, dated July 1981 (with supplemental service), may be ordered as S/N 004-000-81002-3 for $21 from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402.

Report on local network equipment

A special report on the manufacturers of local network equipment is being prepared for the *LOCALNetter Newsletter*. The report will be a summary of local network vendors and information on their equipment produced to date. It is expected to be available in late 1981 or early 1982.

Manufacturers who build local networks and/or components and equipment usable by manufacturers of local networks are invited to submit product descriptions, product manuals, names and addresses of important marketing contacts, and prices of equipment to Kenneth J. Thurber, Editor,*The LOCALNetter Newsletter,* PO Box 24344, Minneapolis, MN 55424, for possible inclusion in the report.

Straight from

Tektronix — Integrating logic analysis and pattern generation functions, the Digital Analysis System, Tektronix claims, gives designers an edge by allowing systems to be evaluated before hardware or firmware is complete.

Data Translation — Doubling Q-bus bandwidth, according to Data Translation, board level data acquisition system transfers data to memory via an external bus at rates to 250 kHz.

Baudex — High speed multiple line printing is more efficient, Baudex states, when multiple cartridge module dot matrix printheads are stacked than when serial carriages are run at faster speeds.

Storage Technology — A virtual storage system for large scale sequential disc data set applications, Storage Technology says, significantly increases disc space utilization, improves total system throughput, and offloads the host of many data management functions.

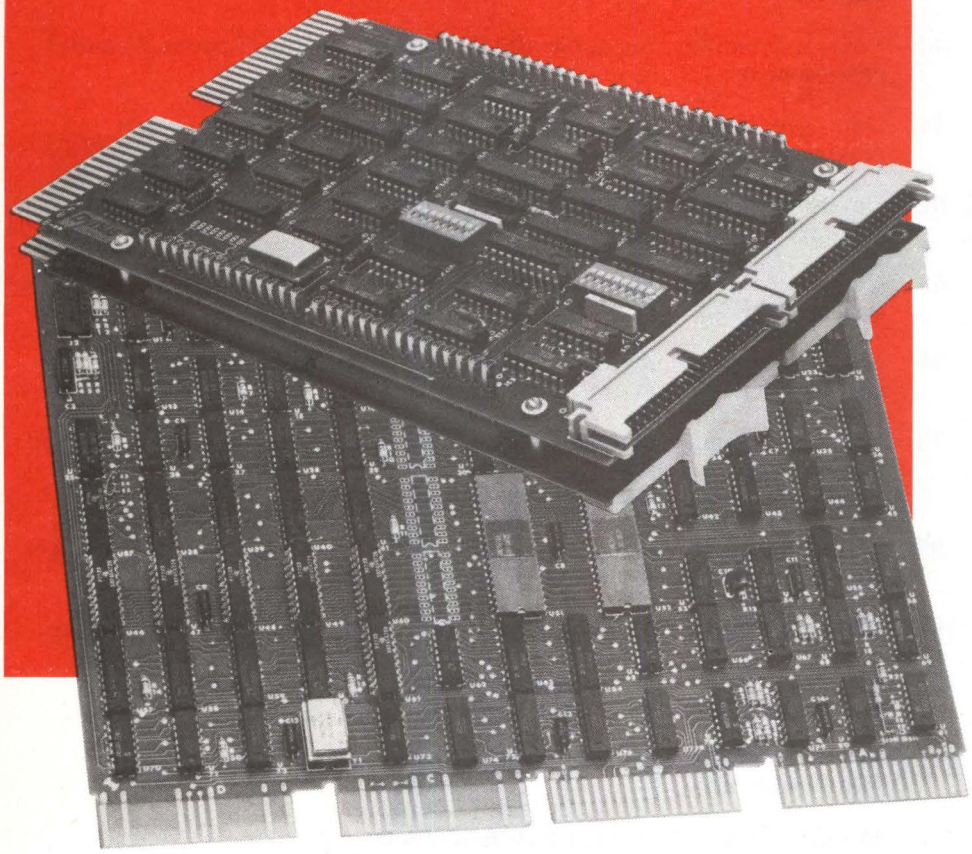
Honeywell — A new set of software packages from Honeywell is reported to allow its DPS 6 and Level 6 computer systems to operate in the SNA environment.

Hewlett-Packard — The 64000 logic development system, Hewlett-Packard maintains, now includes emulation for three 16-bit microprocessors.

IBM — IBM now offers software, hardware, and features that it claims enable the SNA products to communicate via X.21 or X.25 data transmission services.

Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept, PO Box 593, Littleton, MA 01460. (USPS 127-340)

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS



Now, from the company that delivers the industry's widest range of DEC-compatible memory products, a family of peripheral controllers that's second to none. From comparatively simple cartridge disk controllers to complex 300MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11® or PDP®-11 minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and a lot more. Like space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

Look at the chart of our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

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MINI	LSI-11	LSI-11	PDP-11	LSI-11	PDP-11	LSI-11	LSI-11	LSI-11	PDP-11	PDP-11	PDP-11
COMPATIBILITY	TM11/TU10			RK05		RM02	RK07	RP06	RM02	RK07	RP06

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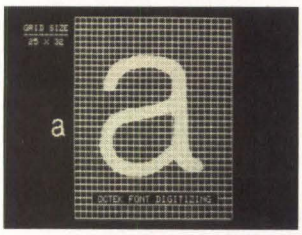
CIRCLE 4 ON INQUIRY CARD

COMPUTER DESIGN®

System technology

78 *CMOS double-metal technology requires three masks: one for each metal layer and a third for the via hole, which connects the two layers*

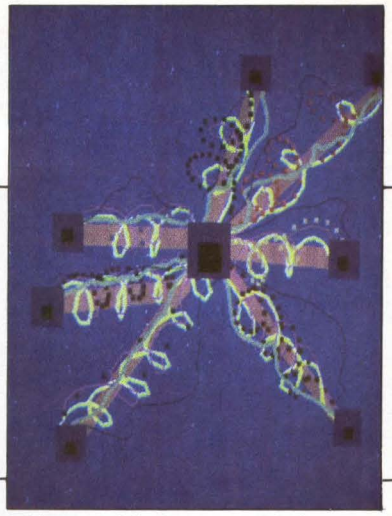
System design



213 *Computer aided design potential. Character profile is digitized and processed to create new font for cathode ray tube display or dot matrix printer*

Vol 20 No 9
Sept 1981

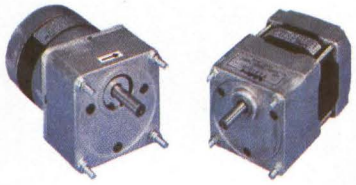
Special report on data communications



This month's cover, entitled "Communications between terminals," was generated on a Digital Effects VP-3 by Larry Gartel

System components

Departments



262 *Induction gear motors have 60-, 70-, or 80-mm core diameters*

Editorial reviewers for this issue

James M. Crafts
Thomas Crawford
Ralph J. Preiss

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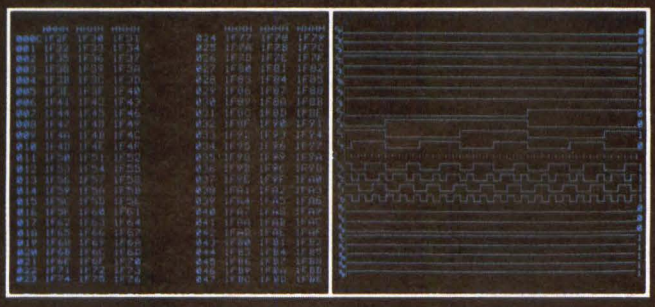
100 MHz high-speed hardware analysis.
The K101-D's advanced high-performance hybrid probes let you capture glitches as narrow as 5 ns. And, with 48-channel recording, 515-word memory and 16-level triggering, you'll trap the data you need. The convenient display formatting and expansion simplify analysis.

Call now for a free demo.
See for yourself why the K101-D is a breakthrough in logic analyzers for the years ahead. For a demonstration or a copy of our detailed product brochure, write Gould Inc., Biomation Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For fastest response, call 408-988-6800.

For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.



For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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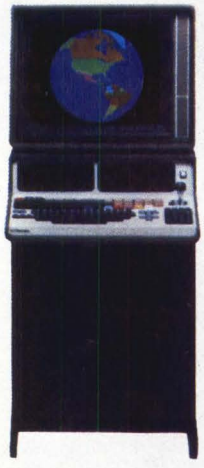

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Chromatics proudly announces the availability of its revolutionary MC68000 driven CGC7900-1 color graphics computer with 1024 x 768 viewable resolution at the unprecedented price of $14,995.

The CGC7900 is the equivalent of a full-blown minicomputer with the latest in color graphics capability. A 10 megabyte hard disk and dual double-density 512K byte flexible disk drive can also be added to create large local data bases or to load programs. The CGC7900 is assembled as an integrated system and utilizes DOS or the IDRIS general purpose operating system designed especially for the MC68000 CPU. PASCAL and C Compilers are supported.

At last, price is no longer an issue when choosing between medium and high resolution graphics. Now Chromatics offers you much more resolution, power, speed and versatility with the CGC7900-1 for only $14,995.

BREAKTHROUGH

Chromatics

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Telephone: 404/493-7000/TWX: 810/766-8099. For additional product information call toll free 1-800-241-9467.

CIRCLE 6 ON INQUIRY CARD

Ignorance of the Law: No Excuse!

Results of our impromptu poll on emi regulations in the June editorial show that 45% of our readers are ignorant of the FCC regulations that were adopted on May 12, 1980, concerning spurious emi from computing devices. Although 55% of our readers are aware of the regulations, only 22% are in the process of complying. Virtually everyone wants more information.

The FCC as a regulating body has been around since 1927. The Communications Act of 1934 put sharper teeth in the FCC's power of enforcement. Two sections of this Act specify the penalties for nonconformance with the new emi regulations. Under Section 502, FCC officers can directly impose administrative sanctions, depending on the seriousness of the violation. Sanctions range from warnings up to a maximum fine of $5000 per day per violation. Section 501 provides for criminal prosecution of violators through the Justice Department at FCC request. This section also calls for a maximum court assessed fine of $10,000 per day per violation and a prison sentence of up to one year. Just who goes to jail is not clear, but it's a pretty good bet that it would be a corporate officer. Remember, the VP of Engineering is a corporate officer. An FCC engineer assured me that Section 501 is used only as a last resort in the case of repeated and flagrant violations. The maximum penalties in Section 502, although solely exercisable by an FCC official, are also used only in instances of excessive violations.

The first implementation date for Class A equipment, October 1, 1981, is nearing. Class A pertains essentially to computing equipment and systems used in commercial, industrial, or business environments and does not include equipment used in the home. All equipment ***first manufactured*** *after that date must be verified by the manufacturer for compliance with the emi standards* ***before*** *being put on the market. Verification, as mentioned in Part 2 of the FCC Rules, means that the manufacturer is responsible for compliance with emi regulations. It could be a lot worse: the FCC also has a "Certification" procedure for Class B equipment which requires the manufacturer to submit actual test data to the FCC. Verified equipment must then display an appropriate label as prescribed by Section 15.816.*

Lest you think this wording implies a grandfather clause to exempt all equipment manufactured before October 1, let me assure you that the FCC, a typical bureaucracy, has provided ample "Catch 22" situations. If a complaint is filed with the FCC concerning your equipment, you can be required to bring the equipment into compliance, even if it was manufactured prior to the October 1 mandatory date.

The most sinister sections of the emi regulations deal with "complaints." Anyone can file a complaint, just as anyone can take you to court. If there is a complaint about a customer's equipment, and the FCC determines that your equipment is indeed responsible for the interference, the FCC will notify you, but it can also shut down your customer's system. It's bad enough when a customer suffers downtime from a malfunction; think what your customer's reaction will be when the FCC sends a "friendly" notice to cease and desist from system operations? Complaints can also come from a customer who has been advised of the FCC requirements and finds your equipment unsuitably labeled.

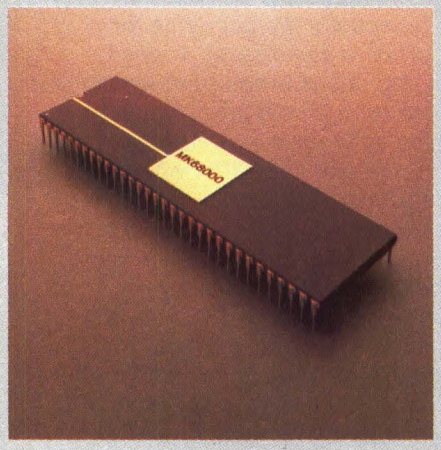
There is one other kind of complaint which I think is the most dangerous: a complaint made by another manufacturer. Here, I plead with our industry to act with restraint and not give way to the temptation of legalized unfair competition. It would be a crime to have such a closely knit industry as ours, which has advanced so far in so short a time, resort to dog-eat-dog tactics. It would be reassuring to know that the same kind of cooperation among competitors that has been the hallmark of this industry will be used to lick the emi problem. I'm convinced that one of the chief reasons this business has grown so quickly is that we are nurtured by each other's ideas and integrity.

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—April
"Optimizing Microprocessor Input/Output Techniques"
Lynn E. Costlow, Sperry Flight Systems

This article will now compete with other monthly winners for the 1981 Windjammer cruise award.

Mostek.
The best reason yet to choose it.



For new 16-bit designs, the 68000 is clearly your best choice. Quite simply, it has the best architecture you can get. Results from 3 separate benchmark studies* and 2 independent product preference polls† confirm it.

That's one reason to pick the 68000 first. The other reason is Mostek. Because with our new MK68000, you now also have a choice of manufacturers. High volume domestic manufacturers with a proven track record in VLSI production.

All of which means a better, more predictable future with the 68000. A future, in fact, that will be supported by a variety of peripheral chips, including a Serial Input/Output (SIO), a Parallel Interface Timer (PIT) and a Memory Management Unit (MMU). Plus a truly inexpensive yet powerful development tool that will make design-

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*"A Tale of Four MPUs: Benchmarks Quantify Performance." Robert D. Grappel and Jack E. Hemenway, April 1, 1981 EDN Magazine, a Cahners Publication

Exerpted from 16-Bit Microprocessors, Copyright 1981 by Howard W. Sams and Co., Inc., Indianapolis, Indiana.

"Digital Filters — Part II: Performance Comparisons of 16-Bit Microcomputers," V.P. Nelson and H.T. Nagel, February, 1981, IEEE Micro, Vol. I, No. 1

† Annual Minicomputer Survey, November ,1980, with permission of DATAMATION MAGAZINE, G.S. Grumman/Cowen & Co.

Electronics 1980 Product Preference Poll, with permission of ELECTRONICS MAGAZINE, McGraw-Hill, Inc.

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CIRCLE 7 ON INQUIRY CARD

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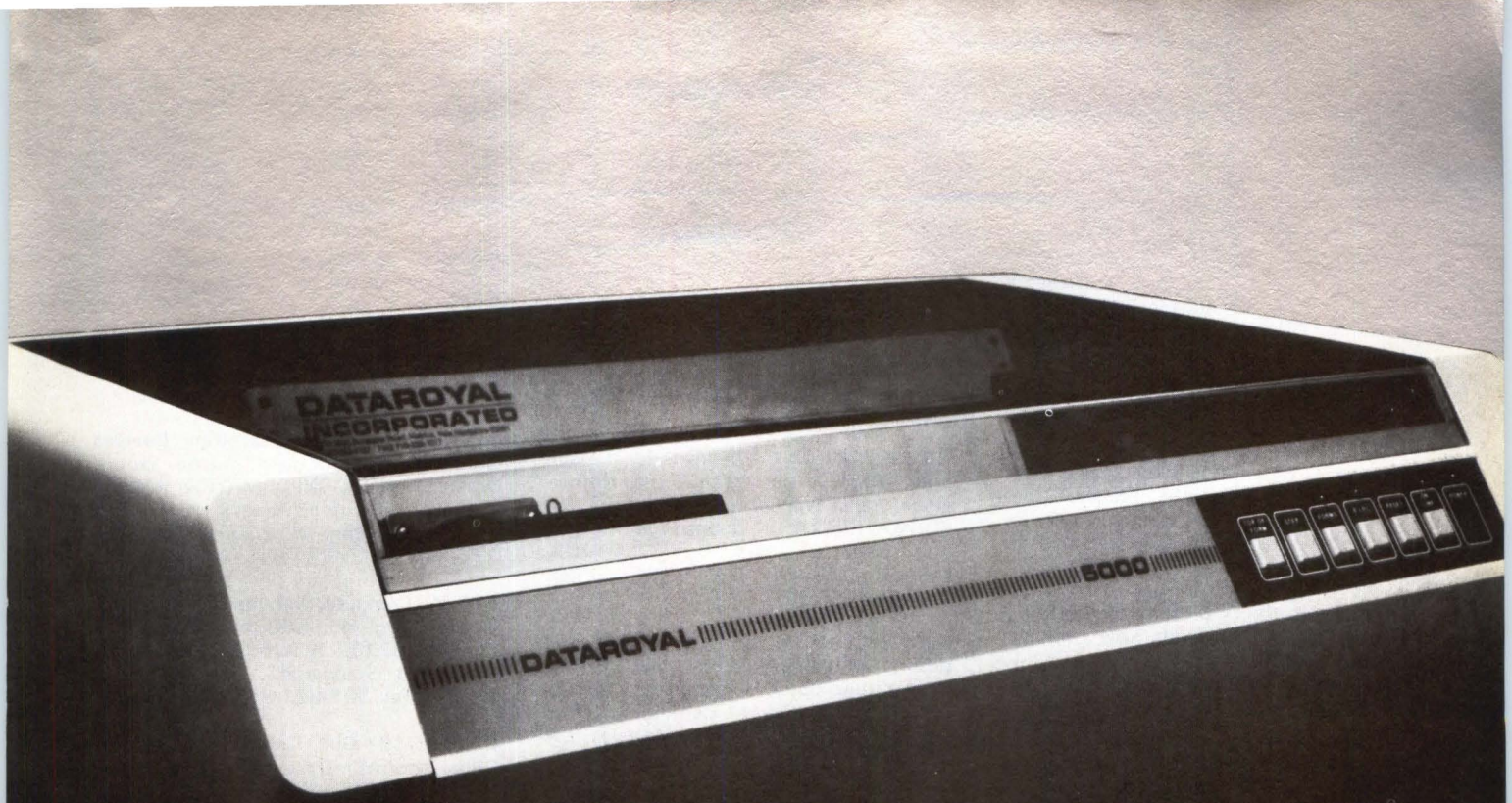

WHILE OUR COMPETITORS TALK ABOUT PRINTER RELIABILITY,

DATAROYAL PROVES IT.

Many printer companies talk about how reliable their products are. But very few can publish hard evidence supporting those claims.

Dataroyal knows that every printer breakdown, service call, or extra maintenance procedure increases the cost of owning and operating your system. So we don't make claims we can't prove.

Dataroyal tests our IPS-5000 printers non-stop at 100% duty cycle and page density. These printers have now surpassed an MTBF (mean time between failure) figure of 2000 hours-*without failure, maintenance, or any special treatment.* Under normal conditions, this performance rating means years of reliable operation between service calls.

And our printhead life now exceeds 500 million characters. All of this reliability spares you the time and expense you might now be spending on your existing printers.

This superior performance has made Dataroyal the intelligent choice for major domestic and international OEM systems manufacturers. Want to see our proof? Contact us, and we will send you our latest test results. And *that's* not just talk.

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CALENDAR

CONFERENCES

OCT 5-8—Electronics Test and Measurement Conf, Hyatt Regency, Chicago, Ill. INFORMATION: Dona Atwood, Registrar, Electronics Test and Measurement Conf, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

OCT 12-14—Conf on Local Computer Networks, Hilton Inn, Minneapolis, Minn. INFORMATION: Dr Abe Franck, Gen'l Chm, UCC, U of Minnesota, 227 Experimental Engineering, 208 Union St SE, Minneapolis, MN 55455

OCT 12-15—INFO '81 (Information Mgmt Expo and Conf), Coliseum, New York, NY. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10167. Tel: 212/661-8410

OCT 12-16—India Industrial Exhibition, Atlanta, Ga. INFORMATION: Alan Isacson, A. B. Isacson Assocs, Inc, 331 Park Ave S, New York, NY 10010. Tel: 212/475-1771

OCT 15-18—Northeast Computer Show, Hynes Auditorium, Boston, Mass. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

OCT 19-20—ACM Sym on the Impact of Small Computer Systems (Sigsmall), Orlando, Fla. INFORMATION: S. Ron Oliver, The MITRE Corp, 433 N Circle Dr, Colorado Springs, CO 80908. Tel: 303/471-0102

OCT 19-21—Autotestcon '81, Orlando Hyatt House, Orlando, Fla. INFORMATION: William Stalls, PO Box 5837, MS 333, Orlando, FL 32855

OCT 21-23—San Francisco Bay Area Computer Showcase Expo, Brooks Hall, San Francisco, Calif. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

OCT 27-29—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Louis J. Sobotka, Program Chm, 1981 Internat'l Test Conf, Bell Laboratories, PO Box 830, Allentown, PA 18105. Tel: 215/439-6198

OCT 28-29—Western Computer Show, Calgary, Alberta. INFORMATION: Laurie Whitsed, Computing Equipment Assoc, 55 Bloor St W, Suite 1201, Toronto, Ontario M4W 3K2, Canada

OCT 28-30—FOCS (IEEE Sym on Foundations of Computer Science), Nashville, Tenn. INFORMATION: Prof R. Book, Dept of Mathematics, U of California, Santa Barbara, CA 93106

OCT 29-NOV 1—Southeast Computer Show, Atlanta Civic Ctr, Atlanta, Ga. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

OCT 30-NOV 1—South Florida Computer Showcase Expo, Miami Expo/Ctr, Miami, Fla. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

NOV 5, 12, AND 17—Invitational Computer Confs, Amsterdam, The Netherlands; Paris, France; and Milan, Italy. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 9-11—ACM '81 (Assoc for Computing Machinery Conf and Expo), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: ACM '81 Conf Info, PO Box 24059, Village Station, Los Angeles, CA 90024

NOV 9-12—Autofact III Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: Autofact III, SME Public Relations, One SME Dr, PO Box 930, Dearborn, MI 48128

NOV 9-12—Isratech '81, Binyanei Ha'ooma Conv Ctr, Jerusalem, Israel. INFORMATION: Joan Leavitt, Ruder & Finn, 1225 19th St NW, Suite 270, Washington, DC 20036. Tel: 202/466-7800

NOV 9-13—IECI '81 (Internat'l Conf and Exhibit on Industrial Control and Instrumentation Applications of Mini- and Microcomputers), Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: LeRoy Bushart, FMC, 328 Brokaw Rd, Santa Clara, CA 95051. Tel: 408/289-3871

NOV 10-12—Interface West '81, Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

NOV 10-12—MIDCON, O'Hare Expo Ctr and Hyatt Regency O'Hare Hotel, Chicago, Ill. INFORMATION: Robert Myers, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 11-12—ECSG (Electronic Connector Study Group) Sym, Franklin Plaza, Philadelphia, Pa. INFORMATION: Jim Pletcher, Amp, Inc, Harrisburg, PA 17105. Tel: 717/780-8857

NOV 13-15—Los Angeles Computer Showcase Expo, Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

NOV 17—Invitational Computer Conf, Hyatt Palo Alto, Palo Alto, Calif. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 19-22—COMDEX '81, Las Vegas Conv Ctr, Las Vegas, Nev. INFORMATION: The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

DEC 7-9—Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Assocs, 1629 K St, NW, Washington, DC 20006. Tel: 202/296-8100

DEC 8—Computer Networking Sym/NBS, Gaithersburg, Md. INFORMATION: Robert Toense, B226, Technology Bldg, Nat'l Bureau of Standards, Washington, DC 20234. Tel: 301/921-3516

DEC 15-19—Gulf Computer Exhibition, Dubai Internat'l Trade Ctr, Dubai, U.A.E. INFORMATION: Seymour House, 17 Waterloo Pl, London SEIY 4AR, England. Tel: 01/930-3881; OR Trade Ctr Mgmt Co, PO Box 9292, Dubai, U.A.E., Tel: 472200

SEMINARS

OCT 6-7, NOV 2-3, AND NOV 5-6—Computing Applications in Engineering, Boston, Mass; Dallas, Tex; and Houston, Tex. INFORMATION: Educational Programs Mgr, Engineering Systems Group, MR1-1/M75, Digital Equipment Corp, 200 Forest St, Marlboro, MA 01752

OCT 13-15 AND NOV 17-19—Understanding and Using Computer Graphics, New York, NY, and Atlanta, Ga. INFORMATION: Bob Sanzo, Dir of Marketing, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

NOV 9-13—Making Silicon Talk ... and Listen, Santa Barbara, Calif. INFORMATION: A. H. (Steen) Gray, Jr, Signal Technology, Inc, 15 W De La Guerra, Santa Barbara, CA 93101. Tel: 805/963-1552; 800/235-5787 (outside Calif)

SHORT COURSES

SEPT 28-OCT 2, SEPT 30-OCT 2, OCT 5-7, OCT 12-16, OCT 20-23—Comparative Database Mgmt Systems; Computer Performance Evaluation; Configuration Mgmt; Microprocessors and Microcomputers: Theory and Applications; AND Computer Graphics Systems: Design and Applications, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

A FULL SPECTRUM OF CHOICES IN DEC-COMPATIBLE DISK STORAGE:

And now a new 32.2-Mb Winchester/Floppy System

DATA SYSTEMS DESIGN

More disk storage choices than you get from DEC.

DEC designs great CPUs. Data Systems Design gives you disk storage to match.

For CPU quality, you can't beat DEC's LSI-11 and PDP®-11. But their disk storage doesn't always measure up. At Data Systems Design, data storage is our *only* concern. That's why our DEC®-compatible disk systems are more reliable, less expensive, more compact and easier to maintain than the disk systems you get from DEC.

And you get more choices of systems, too, so you can pick the exact features your product application requires.

DSD 880 gives you more megabytes per buck for your PDP-11 and LSI-11.

With the addition of a new DSD 880 version, you now have three choices in winchester disk storage: 31.2, 20.8 or 7.8 megabytes. Each with a choice of 0.5 single- or 1-megabyte double-sided floppy backup. More capacity for less cost-per-megabyte than any comparable DEC alternative.

To match the capacity of the DSD 880's 31.2-megabyte winchester disk, for example, you'd need three DEC RL02 disk cartridge drives plus bootstrap card, and you'd pay about twice the cost of one DSD 880. Plus, you'd give up the high reliability of the DSD 880's winchester technology—a state-of-the-art choice DEC doesn't even offer LSI-11 and PDP-11 users. And you'd have three ungainly boxes over 30 inches high—as compared with the DSD 880's compact 5¼-inch panel height, which saves you rack space and cabinetry costs and allows use in space-critical applications.

Whether you choose the 32.2, 21.8 or 8.8 megabyte winchester/floppy system, your disk system is more cost-effective than any comparable DEC disk drive or combination.

The hardware bootstrap is built right into the interface so you don't have to pay extra for a separate board.

The DSD 880 interfaces require 70% less backplane space than equivalent DEC configurations.

And the HyperDiagnostic™ panel simplifies troubleshooting for cost-effective remote diagnosis.

Fully compatible three ways.

The DSD 880 is hardware-compatible. It integrates with any DEC LSI-11 or PDP-11 computer-based system. Combine the DSD 880 with a VT103 containing an LSI-11/23 and you've got a complete, powerful table-top microcomputer with up to 32.2 megabytes of storage.

Software compatibility is no problem either. You can use your RT-11 or RSX-11 operating systems with RL01 or RL02 (winchester) and RX02 (floppy) handlers. With no modifications at all. And the DSD 880 runs all applicable DEC diagnostics and utilities.

It's media-compatible, too. DSD floppies can use either DEC double-density or IBM single-density formats.

With its higher capacities, smaller size, lower cost and more, the DSD 880 gives your DEC computer-based system the disk storage it deserves.

A choice of 4 floppy systems.

Pick the features you need. Data Systems Design gives you more choices in DEC-compatible floppy disk systems, too.

Each of the four floppy systems is packaged in a low-profile 5¼-inch chassis. All offer built-in hardware bootstrap and complete DEC RX02 compatibility, plus a choice of domestic or international configurations, and complete documentation for easy system integration.

DSD 480 provides double-sided floppy storage for your LSI-11 or PDP-11.

For twice the capacity of DEC's RX02, choose the DSD 480. An optional EXCHNG™ software program lets the DSD 480 transfer files between IBM- and DEC-generated diskettes.

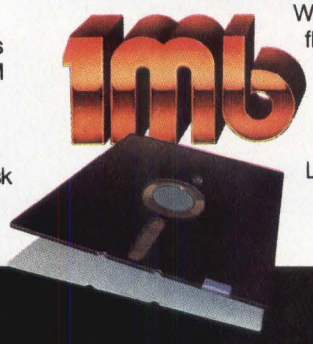
DSD 470 gives you low-cost double-sided floppy storage for your LSI-11.

The DSD 470 is software compatible and can be configured for single- or double-sided diskettes. And its single-board controller/interface* has far fewer parts than separate boards for better space utilization and improved reliability.

Choose DSD 440 for single-sided floppy storage with your LSI-11 or PDP-11.

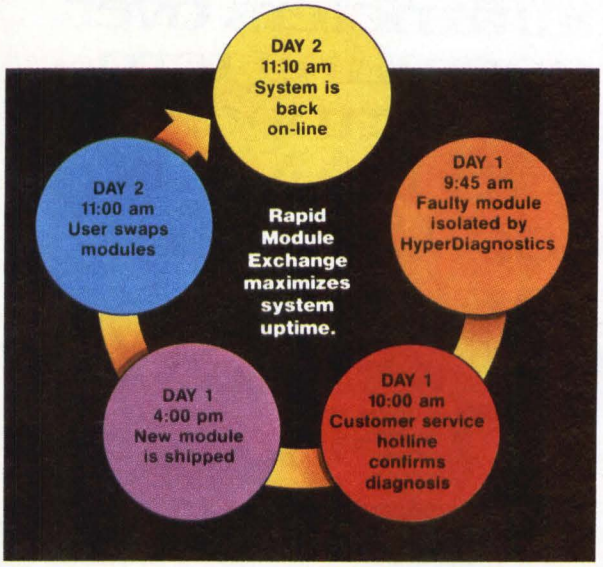
The DSD 440 is RX01 and RX02 software-compatible. It can transfer data 20% faster than DEC's RX02, and features built-in self-diagnostics for easy servicing.

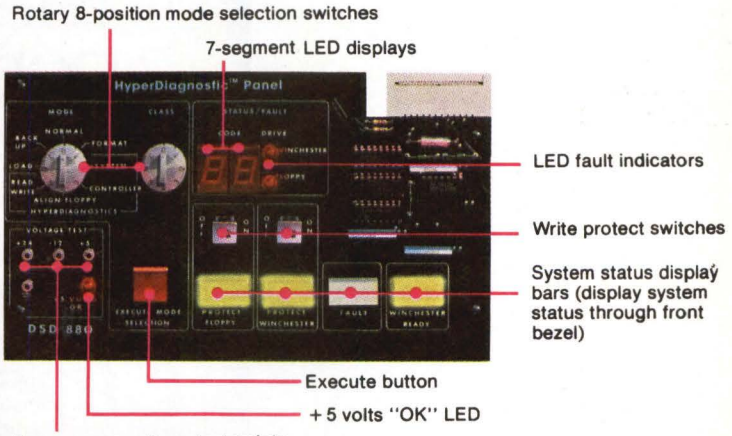
Choose DSD 430 for lowest entry cost with your LSI-11.



With 2 single-sided floppy drives, the DSD 430 gives you full RX02 compatibility and complete LSI-11/23 four-level interrupt support.

More reliable performance and easier maintenance.





DSD 880 HyperDiagnostic™ Panel

A revolutionary concept in uptime: Remote diagnosis ends costly service calls.

The true measure of a system is its ability to perform. Day after day, reading and writing data on demand. Data Systems Design units outlast any other disk system on the market. But even the most rugged system has an occasional problem. And that's when Data Systems Design really shines.

You know the usual service scenario. There's a problem, so you call the service rep. And wait for a return call. Then you wait for someone to show up. And every minute is costing money, in addition to the high cost of the service contract itself.

Data Systems Design ends all that with the service system that will soon be the industry standard: remote diagnosis.

HyperDiagnostics,™ standard on the DSD 440, 480 and 880, allow the user to test, exercise and debug without a CPU or a service call. Easy-to-use controls activate microprogrammed routines, and LED indicators designate fault status. On the 430 and 470, ODT-driven self-diagnostics and software diagnostics assist in troubleshooting.

A call to our service hotline gets instant back-up and confirmation of the diagnosis.† Our service records show that over 20% of the problems are fixed over the phone, with no service needed.

When a faulty module is isolated, **Rapid Module Exchange**™ gets the user back on-line faster than a service call. Thanks to our system's modular design, the user simply swaps modules after consultation with a hotline advisor. We usually ship out a new module the same day a failure is diagnosed in a specially-designed reusable carton for easy return of the original module.

For less than half the cost of a DEC service contract, our **HyperService**™ option extends warranty protection for one year beyond the standard 90 days and covers factory repairs and Rapid Module Exchange Service.

At Data Systems Design, we have carefully considered every step in the process to make service as easy and cost-effective as possible.

Get the disk storage you deserve for your DEC-based system.

For full technical details, write Data Systems Design, Inc., 2241 Lundy Avenue, San Jose, CA 95131, or call the sales office nearest you.

United States: Western Region (408) 727-3163; Eastern Region (617) 769-7620.

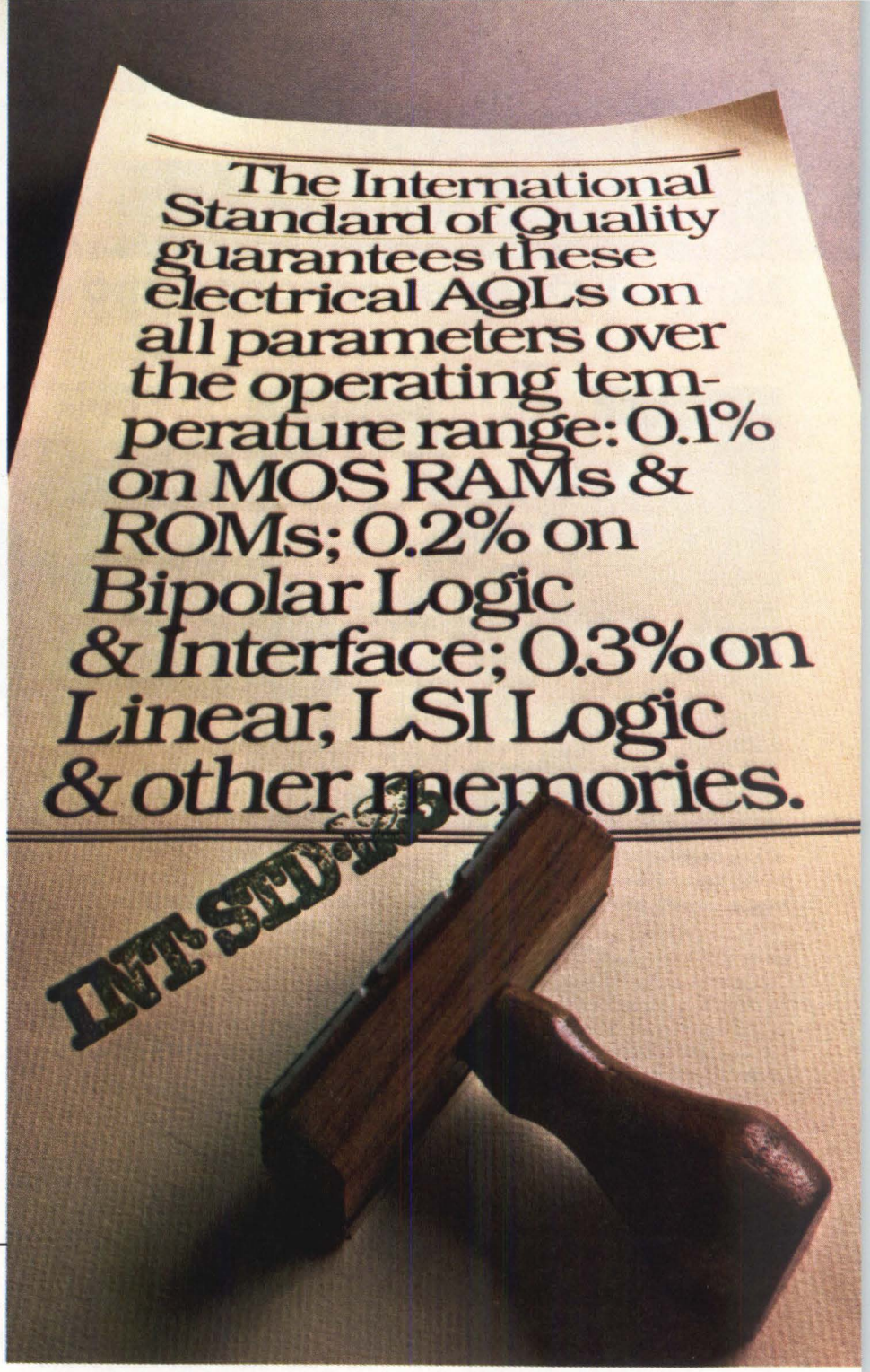
International: Australia: Melbourne 03/543-2077, Sydney 02/848-8533; Canada 416/625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/298783; Italy 02/4047648; Japan 06/323-1707; Netherlands 020/45 87 55; New Zealand 4/693-008; Norway 02/78 94 60; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria 089/1204-0.

*This controller/interface is also available separately as the DSD 4140.

†Although these services are available within the U.S.A. only, comparable service is available through our international distributors.

Circle 101 for DSD 880 information.
Circle 102 for DSD 480 information.
Circle 103 for DSD 470 information.
Circle 104 for DSD 440 information.
Circle 105 for DSD 430 information.

Data Systems



If there's one thing this world doesn't need it's another rotten RAM. Another rejected ROM. One more paralyzed EPROM.

This is your chance to do something about it.

WE'RE ALREADY DOING OUR PARTS.

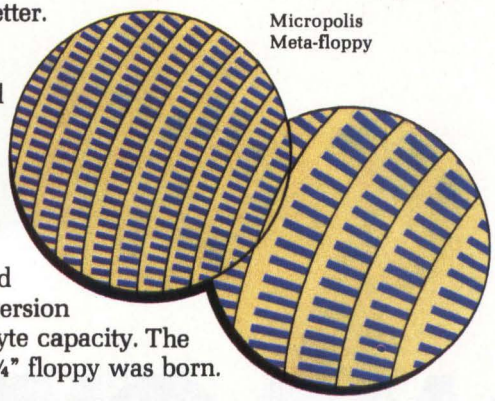
From now on, insist that all your MOS memories meet or exceed INT·STD·123, The International Standard of Quality. We do.

Fact is, nobody's MOS RAMS and ROMS come with a guaranteed AQL better than 0.1%. Not here. Not in Japan.

Some plain 96/100 TPI

FACT: We invented 1 megabyte technology.

When the mini-floppy, with less than 100 kbytes capacity was introduced in 1976, we had a choice. Go along with the rest or do better. We chose to do better. Within a year we doubled both bit density and tracks per inch, resulting in a single sided floppy with 0.5 million bytes and a double sided version with one megabyte capacity. The high capacity 5¼" floppy was born.



Typical
Mini-floppy

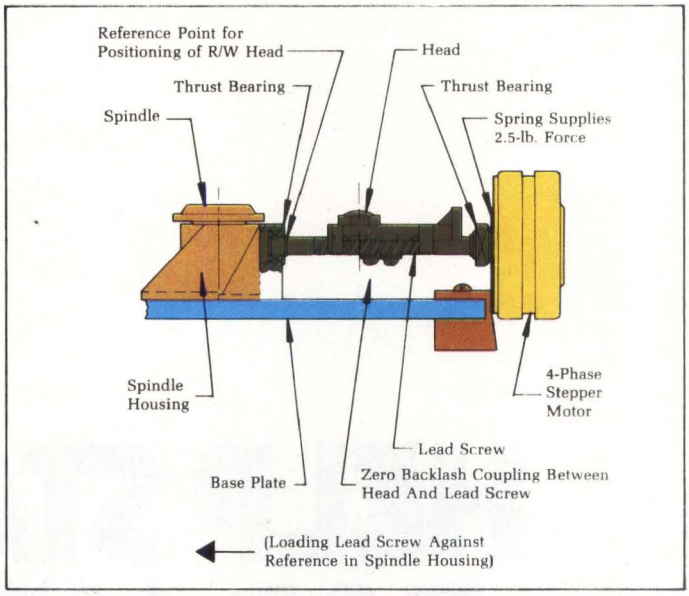
FACT: It took solid engineering to do this.

To quadruple capacity, yet keep interchangeability at the highest level, was no easy task. It took solid, innovative engineering at all levels. The result:

• **Disk Centering Mechanism** - In our drive, the center of the diskette fits over a profiled spindle and is clamped into place while the spindle rotates to assist centering. This technique assures precise centering to within 250 μ-inches and eliminates disk crunching problems.

• **Head Positioning Accuracy** - A precision ground stainless steel leadscrew with metal follower provides more precise positioning than the run-out sensitive pulley and belt approach used by others. Use of a four phase stepper motor and four steps per track averages the effects of all stator and rotor poles, resulting in ± 83 μ-inches positional accuracy.

• **Temperature Compensation** - Our temperature compensation loop includes only the diskette, pre-loaded leadscrew and spindle housing. The baseplate is specifically excluded since its expansion is compensated by a proportional change in the preload of the leadscrew. This approach consistently limits temperature variations to ± 250 μ-inches.



• **Balance Between Speed & Accuracy** – We chose 10ms track-to-track positioning and 380 kbps transfer rate as an optimum balance between speed on one hand, and accuracy and interchangeability on the other.

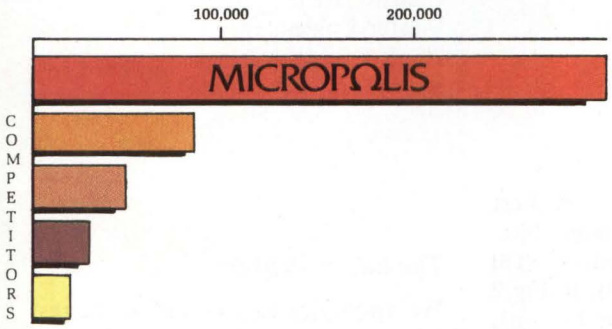
• **Silent Operation** - In band type drives an annoying chatter results from the head's travel from track to track. Our precision stainless mechanism eliminates this noisy irritation.

FACT: Our drives really work.

While others are still learning, our 96/100 TPI drives are operating reliably in systems all over the world. So well, in fact, that we're extending the warranty to 12 months on new OEM agreements. Design and process controls learned years ago, coupled with effective quality control, assures drives ready to work in your system.

facts about 5¼" floppies

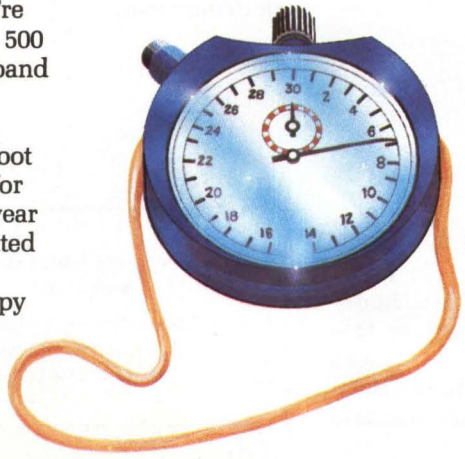
FACT: We've delivered more 96/100 TPI drives to OEM's than all others.



To date we've delivered over 200,000 double track density drives; more than all of our competitors combined. Hundreds of manufacturers of successful small business systems have selected Micropolis drives for their cost effectiveness and proven reliability.

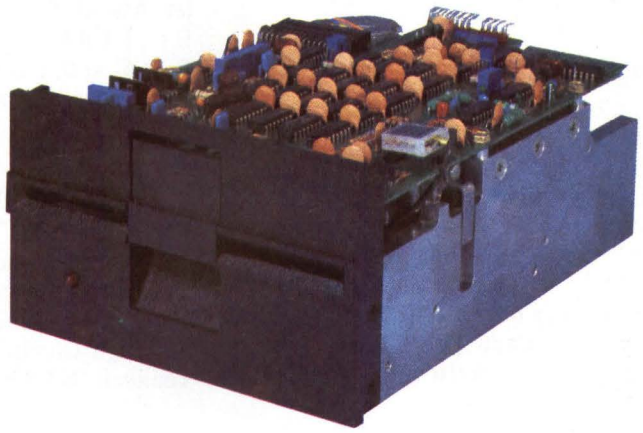
FACT: We're producing more than one each minute.

If you need high performance floppies on time, and in quantity, come to Micropolis. We're producing over 500 a day... and expanding. Expansion includes a new 60,000 square foot plant planned for occupancy by year end and dedicated completely to 96/100 TPI floppy production.



FACT: We've invented again - A 2 megabyte 5¼ inch floppy.

At NCC we introduced a new 2 megabyte floppy, made possible by again doubling density to 12,000 bits per inch. Micropolis' Model 1117 has 6ms track to track positioning, 500 kbps transfer rate and a host of features including a "chassis within a chassis" for unparalleled electrical shielding and resistance to mounting effect. Industry standard mounting and bezel permit easy introduction into existing systems.



So you win both ways with Micropolis. If you need 96/100 TPI floppies now, order our field proven 1015/1016 series. If you're working on a new system, design in our 2 megabyte Model 1117, the high performance "chassis within a chassis" floppy.

For more information phone us or write on your letterhead.

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To the Editor:

In attempting to reduce roundoff errors ("Reducing Roundoff Errors in Microprocessor Based Calculations," Henry A. Davis, Feb 1981, pp 113-117), reordering the sequence of operations during expression evaluation will sometimes gain precision. For instance, there are four values of 123.4, 25.78, 4.479, and 1.244. If we have a virtual machine of 4-decimal point precision, then while summing up these four numbers, we have:

(1)		(2)	
123.4		1.244	
+ 25.78		+ 4.479	
149.1		5.723	
+ 4.479		+ 25.78	
153.5		31.50	
+ 1.244		+ 123.4	
154.7		154.9	

The actual total of the above numbers is 154.903. Evaluation (2) gives a total of 154.9, which is accurate in all four digits. Consequently, this leads to an important programming tip—ie, always manipulate small values first.

Mr Davis gave an example of matrix operation with inherent errors in the data. This kind of error is certainly not pertinent to reducing roundoff errors.

Tsuei-chi Yeh
Taipei Institute of Technology
Taipei, Taiwan 106
ROC

To the Editor:

In my rush to return the proof of my article, "Forth—The Language of Machine Independence" (June 1981, pp 117-121), I didn't notice the deletion of John Cassady's name as the author of the Forth based 8080 assembler. This note is an attempt to rectify that omission.

Gary Feierbach
Inner Access Corp
PO Box 888
Belmont, CA 94002

To the Editor:

There is a minor error in J. Robert Logan's article, "Automated Network Synthesizer Compacts VLSI Design" (Apr 1981, p 173): In Fig 2 let ABCD = 0101. Then by 2(a), $F = D\overline{C}B\overline{A} + \ldots = 1$; and by 2(c), $F = C = 0$, a contradiction. The error occurs in line 2 of the table; it should be for A = 0 B = 1 that $F = \overline{D}C + D\overline{C} = D \oplus C$. This can be seen by examining line 5 of the table on p 176; 3* and not 3 appears.

Gerald D. Chandler, Assoc Prof
Dept of Math and
Computer Science
Fairleigh Dickinson Univ
Teaneck, NJ 07666

To the Editor:

Rate "Bubble Memory Circuits Promote 3-Dimensional Stacking," by Russell MacDonald (June 1981, pp 135-141), very low regarding the TI promotion of its bubble memory products. One very important feature of these devices was omitted—that they have been dropped from TI's product line and will not be available from any source after present prototype quantities are unloaded on unsuspecting engineers.

Your editorial staff should have caught this—and TI should have alerted you to potentially misleading statements in the article, which imply that TI is supporting this product.

Charlie Allen
Master Logic
761 E Evelyn Ave
Sunnyvale, CA 94086

The Editor Replies:

We apologize to you and to the rest of our readers for any inconvenience (or crushed anticipations) you may have suffered by reading our article on TI's bubble memory, and then finding out that TI has withdrawn the product from the market. If you think you were surprised, think of how the TI bubble people must have felt. As late as NCC I had a meeting with them, when we discussed future article possibilities for bubble products. The press release announcing the withdrawal arrived at our offices after the June issue had been printed and shipped. Someday maybe there really will be electronic mail.

—Ed

Letters to the Editor should be addressed:

Editor, Computer Design
11 Goldsmith St
Littleton, MA 01460

A WINCHESTER WINNER...

11 megabytes for only $1395

Score a budget bullseye with this special, limited-time Winchester disc drive offer from PRIAM and HOKUSHIN. Put the 11.5-megabyte, floppy-disc-sized DISKOS 1070 drive into one system or a hundred for only $1395* each. To make it even easier for you to zero in Winchesters on your system, you can get the DISKOS 1070 *and* PRIAM's SMART Interface to control it for just $1895*! Power supply for both, $295.

Average head positioning, 73ms. Track-to-track, 23 ms. Brushless DC spindle motor for operation anywhere in the world. Internal shock mounts, with spindle and head locking. Super reliability: 10,000 hours MTBF. And early next year HOKUSHIN plans to provide a 21-megabyte version in the same package.

When you want even higher capacity, PRIAM's family of faster drives can be plugged right in to give you 34 to 158 megabytes. The SMART Interface daisy-chains any mix of up to four 8 or 14-inch PRIAM drives.

Shoot your order our way before December 15, for delivery before February 1, 1982, and you've scored!

*Terminator included, of course.

CONTROLLERS AND ADAPTERS AVAILABLE FROM THESE SUPPLIERS:

MULTIBUS: ADES, CPC, Intel (215B), Mator Systems
S-100: ADES, Alloy Engineering*, Mator Systems
MC6800: Novex*
LSI-11: Dilog (DQ203), Mator Systems, Peritek*, Xylogics (530)

*Requires adapter, SMART Interface.

PRIAM can supply the SMART-E, a higher-performance version of the SMART interface and ANSI and SMD drive-level interfaces, too.

For complete specifications, call or write *now* to:

PRIAM

3096 Orchard Drive, San Jose, CA 95134 • (408) 946-4600 • TWX: 910-338-0293

HOKUSHIN

Electric Works, Ltd., Tokyo, Japan

CIRCLE 12 ON INQUIRY CARD

THE BEST PLACE TO WORK ON YOUR OWN IDEAS IS NOT AT WORK.

Until now, the most sophisticated computers were found at work. Which meant anyone who needed a computer to develop his own ideas did so before anyone arrived in the morning. Or after everyone left at night.

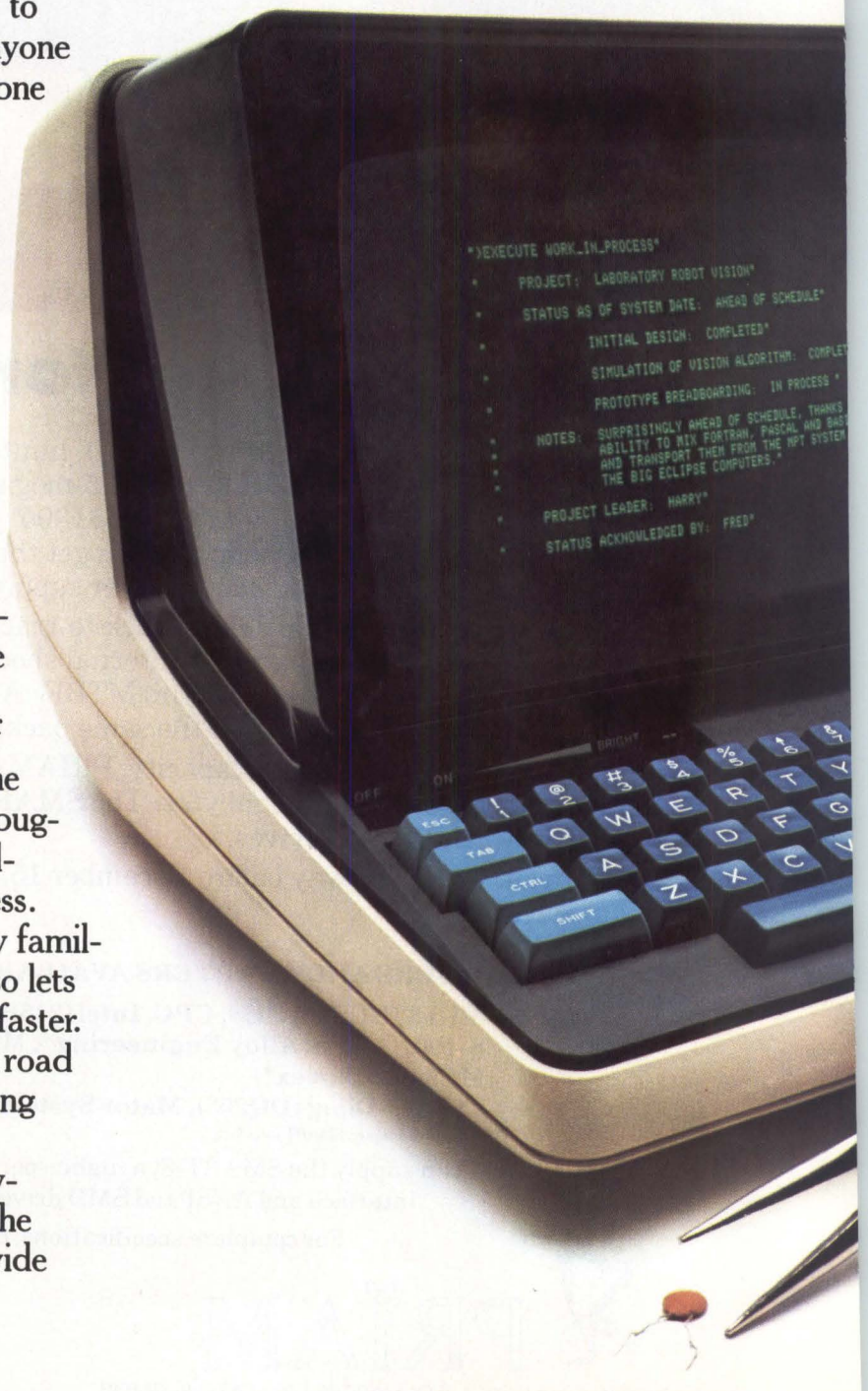
Fortunately, that is no longer necessary. For some of the best parts of a big computer can now be had in a computer small enough (and inexpensive enough) to fit into anyone's budget (personal or corporate).

The MPT/100 computer you see here.

The MPT/100 runs a multitasking FORTRAN and a multitasking PASCAL that executes at assembly language speeds. An ANSI-compatible BASIC that lets you write quickly large programs that take up a small amount of space. A full range of user-friendly aids like a Command Line Interpreter, a Menu Editor, and a Debugger. And MP/OS, one of the most advanced operating systems in the business.

Such systems software is not only familiar and consequently easy to use. It also lets you get your software up and running faster. So you (and your ideas) can be on the road while everyone else is still on the drawing board.

You (and your ideas) can go anywhere in the world. Because we give the MPT/100 computer the same worldwide support we give every Data General computer. And when you've really taken off,



you can grow with all your software, all your peripherals, everything you've learned. Because we've gone to great lengths to make our computers get along with each other.

What, you may ask, is inside the computer? A 16-bit microNOVA® computer. 64K-bytes of memory. 80-column by 24-line screen. Full keyboard with numeric pad. 716-KB of on-line storage on two 358-KB mini-diskettes.

Out back you'll find an I/O bus that accepts the standard microNOVA peripherals, including Data General Winchester-type disks. As well as your own interfaces. And two synchronous/asynchronous communications ports programmable to 19.2K baud.

And a host of operating features you'll have to see in action.

The point here is that with an MPT/100 computer of your own, there is no reason why you can't do what a lot of other companies have done with other Data General computers.

Like Summagraphics Corporation of Fairfield, Connecticut, a company whose Computer Aided Drafting (CAD) systems have made their customer's draftsmen 3-10 times more productive. An achievement that has tripled Summagraphics systems business in 20 months.

If you would like more information about the MPT/100 computer, call your local Data General office, your Data General manufacturer's representative, or one of the distributors listed below. Or write us at MS C-228, 4400 Computer Drive, Westboro, MA 01580.

We would suggest, however, that you ask us to send this information to your home.

Unless, of course, you're planning to use the MPT/100 to work on your hot new project at work.

MPT/100 computers are available for delivery from SCHWEBER, HALLMARK, KIERULFF, ALMAC/STROUM and R.A.E. in Canada.

Data General
We take care of our own.

CIRCLE 13 ON INQUIRY CARD

High cost wrap/pin boards made OBSOLETE

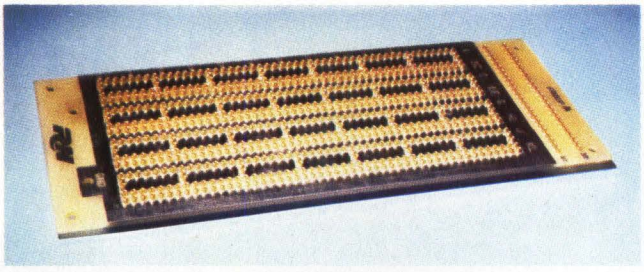
Save money, save time! Wire your boards faster, easier than ever before —with the RN QUICK/CONNECT point-to-point IDC wiring system.

Here is a wiring system that does what wrap/pin does—but does it faster, easier. The wire is simply pushed into the "Quick/Connect" tine which pierces the insulation (IDC) making a gas-tight connection between wire and terminal. "Daisy chain" wiring is accomplished with no break in the wire, no insulation stripping.

You'll never willingly use wrap/pin for boards again. Consider these advantages:

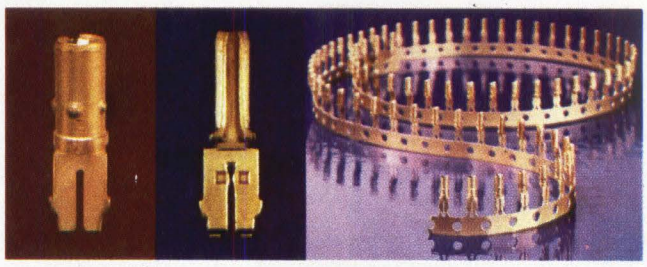
1. **High speed wiring simplicity**—You connect just **one** wire per connection. There is **no time-consuming insulation stripping** as needed with wrap/pin.
2. **Fast, easy wiring changes**—Repair or modify boards by simply removing the individual wires and quickly re-wiring. Field wiring modifications are simple and fast.
3. **Meets highest reliability standards**—Durable four-finger BeCu contacts and fully heat treated IDC tines insure gas-tight performance.
4. **High density low profile boards**—The "Q/C" board profile is only 0.235″ compared to the 0.703″ wrap/pin board. "Quick/Connect" boards go right into production racks.
5. **Wiring machines available**—The semi-automatic wiring machines now in use can be readily modified for the "Q/C" system. Also, semi-automatic "Q/C" machines are available.

This is not just a "dream" system. A major electronics firm is currently using the "Quick/Connect" system on a regular basis.



Many standard "Quick/Connect" prototype socket boards are available now—with a wide selection of 1/0 configurations and board sizes. COMPUTER INTERFACE BOARDS for DEC* PDP-11 and LSI-11. Apple** interface boards also. MICRO-COMPUTER BOARDS in INTEL Multibus*** as well as S-100 configurations now in stock.

*Trademark Digital Equipment Corp. **Trademark Apple Computer Inc. ***Trademark INTEL Corp.



Socket Terminal

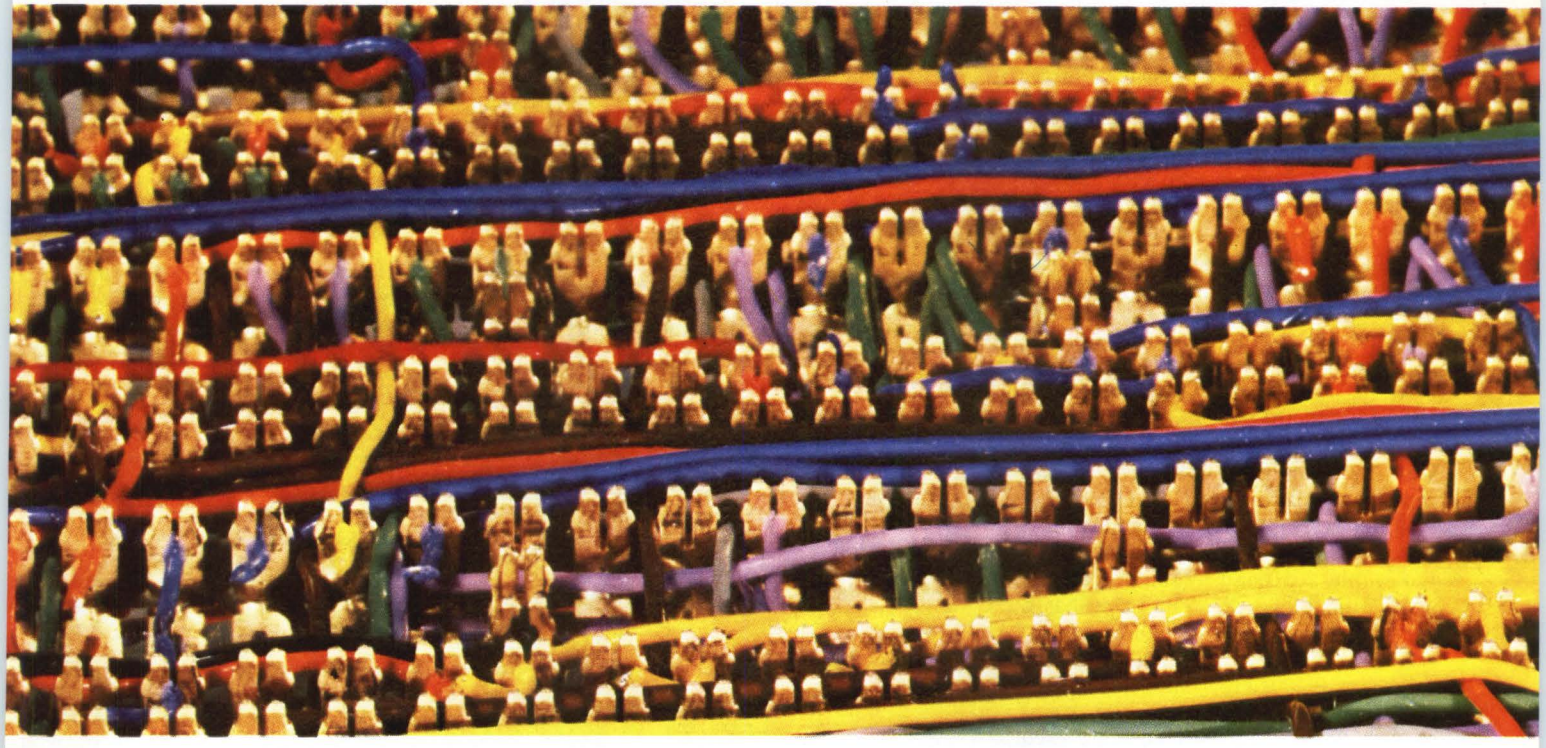
Sockets and terminals supplied on strips for easy board insertion.

Write or call today for full details on this new point-to-point wiring system that will obsolete wrap/pin boards. The time and money savings are truly phenomenal!

RN® ROBINSON NUGENT, INC.

800 East Eighth Street, New Albany, Indiana 47150 • Phone: (812) 945-0211—TWX: 810-540-4082

An "eyeball" comparison tells you instantly that "Quick/Connect" has got to be faster to wire, far less costly than wrap/pin boards!



MAIL THIS COUPON NOW

Send me full details on your new "Quick/Connect" board wiring system.

RN *800 East Eighth Street*
New Albany, Indiana 47150

Name_____ Title_____

Company_____

Address_____

City_____ State_____ Zip_____ Phone_____

My possible application is _____ EE-980

CIRCLE 14 ON INQUIRY CARD

DATA COMMUNICATIONS

Broadband local network system supports multiple communications applications

WangNet broadband local area network is a 340-MHz coaxial cable system that provides separate independent communications channels to support such applications as distributed data and word processing, electronic mail, facsimile, and video. The system, recently introduced by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851, uses frequency division multiplexing to divide the total cable bandwidth into many separate channels. Transmission speeds range from 300 to 64k bits/s for non-Wang devices and up to 12M bits/s for communications between company systems.

Network architecture is a tree-like cable/bus topology (Fig 1). The main trunk cable is looped at its midpoint, divided into transmit and receive halves, and folded back upon itself so that it appears at user outlets as a 2-cable system. Headend controllers or translators are not required. Data on the transmit line propagate toward the network loop where they pass to the receive line and propagate back to all network user outlets. On the receive line, addressed physical or logical destinations capture the information.

Commercial-type CATV hardware is used in the system. Main trunk and branches of the network distribution cable are of 0.412″ (10.5-mm) dia, 75-Ω seamless aluminum sheathed coaxial cable. Attenuation per 100′ (30.5 m) is 1.63 dB max at 300 MHz. Bandwidth is 10 to 350 MHz, with frequency response flat within 2 dB and minimum carrier/noise ratio of 40 dB. The cable has a minimum bending radius of 7″ (17.8 cm). Where runs are 2000′ (610 m) or longer, 0.500″ (12.7-mm) dia cable is recommended to minimize losses. RG-59 or RG-6 flexible coaxial cables are used for drops between the main bus and user outlets. Outlets can be had in 1-, 2-, 3-, or 4-outlet configurations.

Three bands are currently allocated within the 340-MHz cable frequency spectrum. Interconnect band offers dedicated and switched channels, analogous to leased and switched network lines respectively, for transparent, protocol independent, full-duplex multipoint and point to point communications. Wang Band is reserved for communications between Wang VS, OIS and 2200LVP/MVP/SVP systems. Utility band provides seven dedicated channels for standard CATV-type video communications. These three bands together occupy about 35% of total available system bandwidth. The remaining 65% is reserved for addition of future applications. System bandwidth allocations are shown in Fig 2.

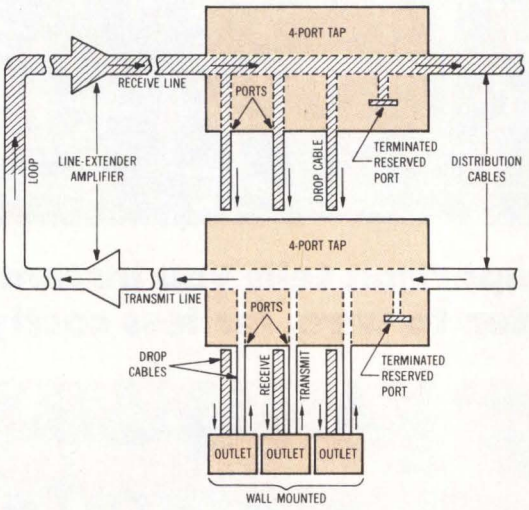


Fig 1 WangNet cable/bus. Four-port tap devices connect main bus to flexible coaxial cable drops that terminate at user outlets. Unidirectional line extender amplifiers, if required, are ac-powered through center conductor and shield of main broadband cable

Three channel groups are provided in the Interconnect band. Thirty-two dedicated channels service point to point or multipoint communications between RS-232-C compatible devices at up to 9600-bit/s data rates. Sixteen dedicated channels provide similar services for RS-499 devices at rates to 64k bits/s. These dedicated channels require one crystal controlled fixed-frequency modem per user device communications port. Channel assignments are fixed, with no master control required. The third, or switched service offered by the Interconnect band, provides 256

(continued on page 32)

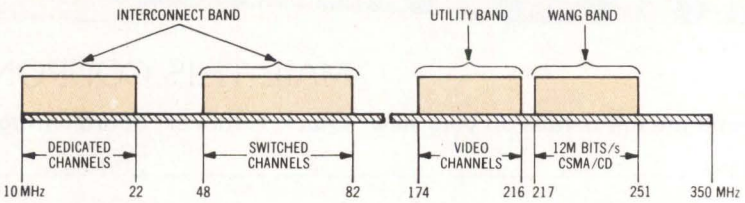


Fig 2 System frequency allocations. Unassigned 22- to 48-MHz, 82- to 174-MHz, and 251- to 350-MHz bands allow for future expansion of system services

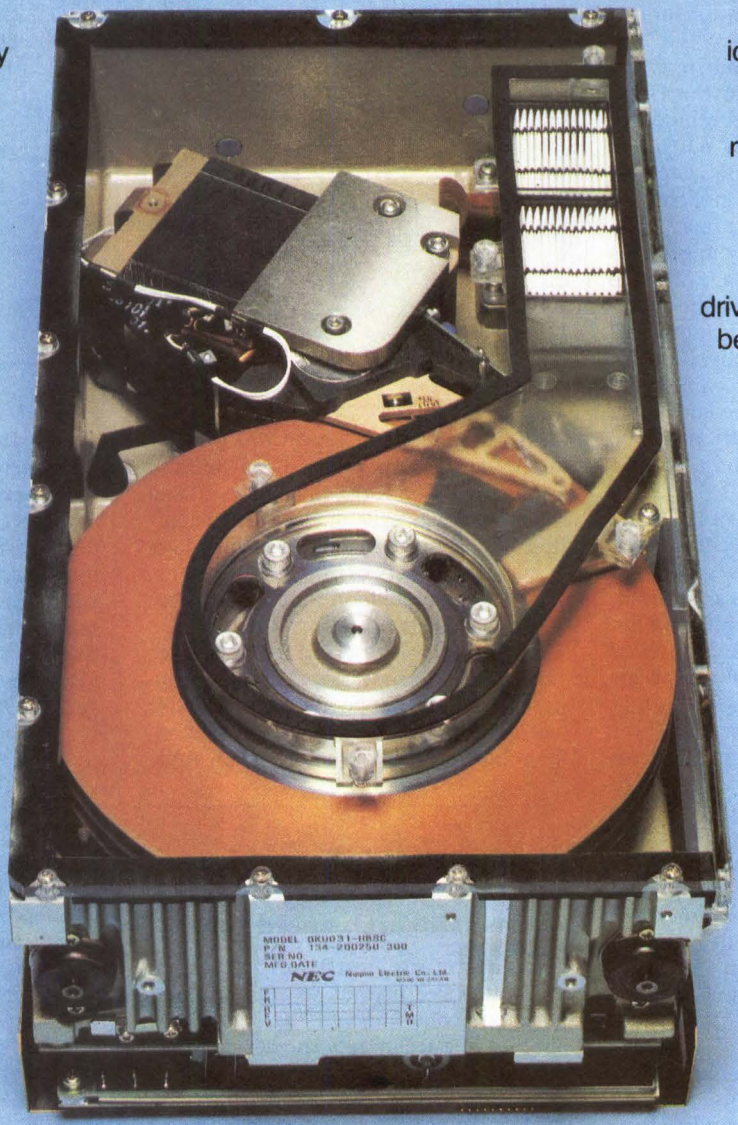
NEC introduces 8-Inch Winchesters.

With more capacity. Faster access. And the reliability you'd expect from NEC.

Once again, NEC leapfrogs conventional technology with its new D2200 family of eight-inch Winchester disk drives.

The first models in the series deliver 30-millisecond access time with capacities of 25.5 and 42.5 megabytes, respectively, and use conventional storage module device (SMD-type) controllers for convenient interfacing and formatting.

Sealed-disk Winchester technology is enhanced with voice-coil actuators, direct-coupled DC spindle motors and closed-loop air circulation which reduces parts count, eliminates periodic maintenance and gives the D2200 Series an MTBF in excess of 10,000 hours. When service is required, it's fast: the D2200s have a 30-minute MTTR.



The D2200 family is ideally suited to medium and heavy volume interactive business applications that require frequent disk access, as in virtual memory, database access and data communications operations.

Eight-inch Winchester drives are increasingly popular because they offer significant savings in installation, packaging, maintenance and cost-of-ownership.

And once again, NEC technology adds an extra dimension. Call your NEC Information Systems representative for more information.

NEC

NEC Information Systems, Inc.

Home Office: 5 Militia Drive, Lexington, MA 02173, (617) 862-3120
Eastern Office: 36 Washington Street, Wellesley, MA 02181, (617) 431-1140
Central Office: 551C Tollgate Road, Elgin, IL 60120, (312) 931-1850
West Coast Office: 8939 S. Sepulveda Blvd., Los Angeles, CA 90045, (213) 670-7346

CIRCLE 15 ON INQUIRY CARD

DATA COMMUNICATIONS

switched frequency channels for point to point communications between 512 RS-232-C devices at rates to 9600 bits/s.

Interconnect band switched service requires one frequency-agile modem per device communications port plus one DataSwitch per WangNet system (Fig 3). The function of the DataSwitch is to manage and allocate the 9600-bit/s channels. The microprocessor based modems include an RS-232-C compatible connector that accommodates a Wang or non-Wang communications interface, RS-366 for autodial function, keypad for calling procedures, and LEDs for indicating call status.

Each frequency agile modem is assigned a unique address and the DataSwitch monitors the line continuously for call/connection requests. When one station calls another, the DataSwitch instructs calling and called modems to shift frequencies to compatible channels. The modems must be connected to user outlets in a manner that the distance along the transmit line from the DataSwitch, through the network loop, and along the receive line to any network outlet should not exceed 2 cable-miles (3.2 km). Installations that require cable runs exceeding this specification will be evaluated by the company on a request for quotation basis.

Wang Band is reserved for Wang systems only. Data are packet-formatted for transmission at 12M bits/s over virtual circuits. The HDLC packet format has a variable (2k-byte max) information field and link access is via an improved version of carrier-sense multiple-access with collision detection (CSMA/CD) that offers complete error recovery and flow control. Wang VS, OIS, and 2200 systems connect to the cable through a cable interface unit (CIU), one CIU being required per connected system. The CIU is a Z80 based intelligent controller with 128k memory. It performs a number of tasks including CSMA/CD functions (listen-before/listen-while talk), packet assembly/disassembly, error detection/correction, buffering, and flow control. Failure of a CIU affects only the system attached to it.

Wang Band allows resource sharing among all connected systems, file and document transfers, remote editing of documents resident on other OIS or word processing-equipped VS systems, and distribution of documents or messages using the company's MAILWAY™ electronic mail system. Wang Band can also communicate with the Interconnect band via a frequency agile modem. The band's 16-bit addressing capability accommodates very large network configurations, theoretically contention for 65,535 VS, OIS, and 2200 systems.

Utility band is reserved for such video applications as security and teleconferencing. It supports seven 6-MHz video channels, each capable of handling one composite color video/audio signal from customer-supplied video equipment.

Prices and delivery dates for WangNet-associated hardware are: 9600-bit/s and 64k-bit/s fixed frequency modems, $850 and $1200 respectively with delivery in first quarter 1982; frequency agile modems $1250 and DataSwitch $12,000, both available June, 1982; and CIU, $3800, available in the fall of 1982.

—James W. Hughes, Senior Editor

Circle 241 on Inquiry Card

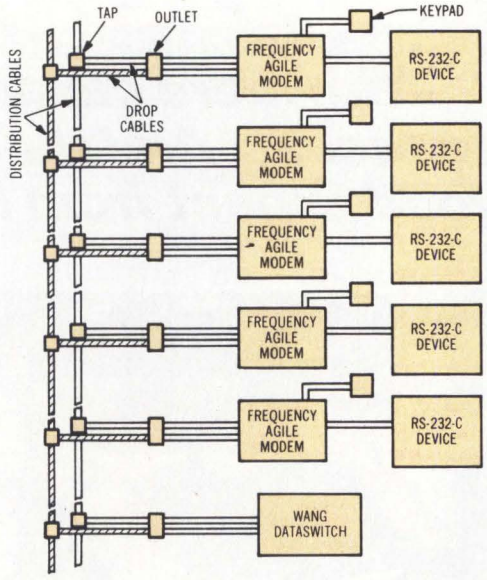


Fig 3 Interconnect band switched channel arrangement. DataSwitch dynamically allocates 256 frequency channels to 512 user systems

Multiport modem combines medium speed channels over single high speed line

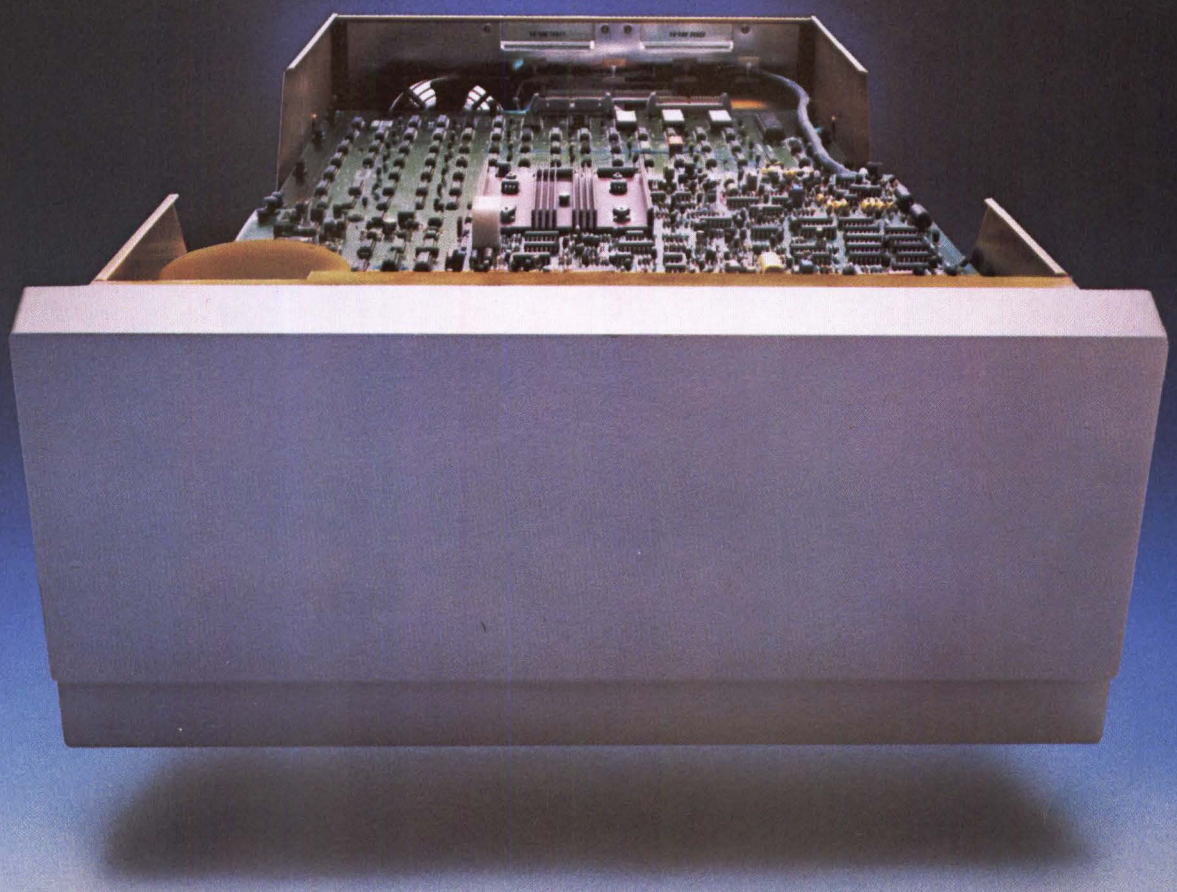
Bandsplitting multiport modem DL 96/V.29 BSM permits several terminals to share one modem. Using a bit-interleaving technique, the device transmits up to four medium speed channels over one high speed line, resulting in savings in line costs and in the cost of separate modems for each channel. The unit, introduced by Infotron Systems Corp, Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003, conforms to CCITT V.29 specifications for 9600-bit/s modems.

Intended for point to point, multipoint, and multiport applications, the synchronous modem operates full-duplex at 9600, 7200, and 4800 bits/s over 4-wire type 3002 unconditioned lines. Multiport inputs may be in any combination of 2400-, 4800-, and 7200-bit/s channels up to a cumulative input of 9600 bits/s. The modem may be reconfigured for changing requirements using front panel switches.

(continued on page 37)

Century Data Systems
A Xerox Company

Drives for the 80's



Century achieves a new milestone in space.

The 160MB Marksman.

Planned evolution: a logical, cost-effective extension of a complete line of Marksman Winchester disk drives.

In just over two years, Century Data has boosted capacity of the Marksman eight-fold while cutting per-megabyte costs by a factor of three.

Like the 80MB model introduced at this year's NCC, the new Marksman 160 incorporates an improved head positioning concept developed in conjunction with the Xerox Advanced Development Laboratory.

A new torque motor and closed-loop servo system increases track density and improves data reliability. This motor boosts performance by 23 percent, yet fits in the same physical space as a stepper motor.

Remarkably easy to interface.

SMD or Marksman interfaces are standard.

It's also available with an embedded intelligent formatter

Continued on next page.

Century Data Systems
A Xerox Company

You finally found a supplier that can deliver 40MB Winchesters now.

Century Data Systems.

And what we'll deliver is disk drives. Not promises.

In fact, Marksman 20 or 40 MB Winchesters can be in your hands—in quantity—in a matter of weeks from your order. It takes that long for some other suppliers to send you a letter saying your order's in backlog.

Where time is of the essence, Century can go further. Not only will we deliver fast, we can ship intelligent Winchesters that can cut system integration time from months to days.

And don't think you have to pay a stiff price for a proven product that's available now. The 20 and 40MB Marksman drives go head-to-head on costs with similar-capacity disks of any size.

In fact, you won't find a better cost per MB. Anywhere. Your

Century representative can tell you more.

Highlights:
Capacity: 20 and 40MB
Transfer rate: 960KBS
Avg. Seek Time: 65MS
Error rates:
Recoverable: <1 in 10^{10} bits
Nonrecoverable: <1 in 10^{13} bits
Positioning: <1 in 10^{6} seeks
MTBF: >8000 hours
MTTR: <30 minutes

Space

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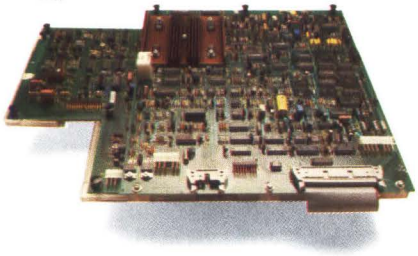


that typically enables systems integrators to interface to mini/micro bus structures in less than a week.

No more suffering through six months (or more) of in-house controller/formatter design time and the resultant hidden costs. Most of the difficult work is already done.

Century also provides the hardware application information and support to make your software job quick and inexpensive.

The result: Your systems can be sent to market that much faster for a competitive leg up.

Upward growth path... the story of the Century.

Start your customers out with 20 or 40MB drives. Solid, proven products available in OEM quantities now. Then integrate Marksman 80s and 160s as their storage needs grow.

With Century, an upper limit will be hard to find.

Cost/performance ideally suited to minis and micros.

Marksman 160 is a fixed Winchester disk with *significant* cost advantages. It will be available in various interfaces, with or without cabinets, embedded controller/formatter, and power supplies.

Call us now to reserve your evaluation unit.

Highlights:
Capacity: 160MB
Transfer rate: 1280KBS
Avg. seek time: 50MS
Error Rates:
Recoverable: <1 in 10^{10} bits
Nonrecoverable: <1 in 10^{13} bits
Positioning <1 in 10^{6} seeks
MTBF: >8000 hours
MTTR: <30 minutes

The million dollar clean room.

At Century Data, one particle of dirt a fraction of the diameter of human hair is considered absolute filth. So we spent a million dollars to make sure that kind of mess never contaminates our Winchesters.

First, we built a clean room with two sections, each wrapped in a bubble of intensively filtered air flowing in a laminar pattern. In one section, we degrease disk, head and enclosure materials with freon.

In the main clean room section, the actual assembly takes place on six clean benches. Each engulfed in its own additional bubble of even cleaner air.

Our next task: making sure the people who assemble the Winchesters are clean enough. A surgical nurse would be too dirty.

The only people that get into our clean room are professionals who have just been scrubbed and scoured. They wear surgical clothing, masks, hoods and special shoes. And they don't eat, chew gum, drink coffee, smoke or even sweat.

The total effect duplicates the zero-error concept of manufacturing used in manned space flight.

Without that kind of clean on top of clean, you just can't be confident of a sealed disk drive. Especially when you think of that flying head, 80 atoms of air away from the whirling high-speed disk. Let just the tiniest fragment of a particle in, and it will not only threaten the data's integrity, it could even damage the components.

Impressive as it is, our million dollar clean room is just one of many quality assurances that goes into a Century drive.

We've put another three million dollars into the most sophisticated automatic test equipment, fixtures and software you'll find anywhere.

It's all part of a continuous commitment to quality like nothing else you'll find in the industry.

Century ready with SMD drives.

Some manufacturers can keep you waiting a year or more for removable-pack disk drives. Especially if you need SMD interface capabilities.

But not Century Data.

Our removable-pack Trident drives are available now. With SMD interfaces, as well as DTL/TTL's. From our 50 and 80 megabyte table-top and rack-mountable models to our 300 megabyte free standing models.

Tridents are dependable, too. Our fully enclosed, specially sealed contamination control system protects your data's integrity, even during preventative maintenance.

We could go on. But the big plus is that you can get our Tridents. Fast. Which means you can start pushing sales out the door. Instead of stalling your customers with some story about how long it takes to get a drive with SMD.

So don't risk your sales by waiting around for a disk drive. Talk to Century about Tridents, today. And get your systems up, running and out to your customer.

Century goes for a quiet drive in the office.

Computer systems were once confined to the computer room, along with all of the other devices that went with them. Tape drives, disk drives, printers and terminals were free to whirr, buzz, click and tap at will.

But this is the age of office automation, when computing equipment is liberated from the computer room for face-to-face contact with secretarial offices and even executive suites. The problem: the clicks and whirrs and buzzes have to be left behind.

Dedicated DP systems. Word processing. CAD/CAM in engineering and design offices. Locally networked data bases. All of these applications give Century Data a mandate to design and manufacture Winchester disk drives that fit this new environment —not interfere with it.

At Century, special equipment and engineering expertise combine to bring quiet drives to the office.

Anechoic is Greek for "no echo." It's also the name for our chamber specifically designed to test noise levels in Winchesters. Pyramid shapes laid over insulating materials capture and absorb sound within the room.

Drive prototypes are placed within the anechoic chamber and put through their paces, while sound measuring devices read noise levels with laboratory accuracy. Drive-quietizing studies are made at the design stage—and verified on production units—enabling advances in engineering toward the quieter drive.

While one anechoic chamber is used for testing

and reducing sound levels from rapidly spinning disks and head-positioning mechanisms, another is used to measure emissions in the radio-frequency spectrum. With this precise way to measure RF noise, we can improve our designs and reduce these emissions.

Century's anechoic chambers are just two devices among many to help us make the better Winchester. It's all part of an ongoing multi-million dollar investment in the future of disk data storage.

For the full Story of the Century...
just check the information you want, and we'll send it to you right away.

- ☐ Marksman: 160MB
- ☐ Marksman: 80MB
- ☐ Marksman: 40MB
- ☐ Marksman: 20MB
- ☐ Trident: 300MB
- ☐ Trident: 200MB
- ☐ Trident: 80MB
- ☐ Trident: 50MB

☐ I would like an evaluation unit for one of the Marksman Winchester or Trident Removable-Pack Disk Drives listed above. Someone will contact me to make arrangements as soon as possible.

Send to: Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806.

Please enclose your business card. CD

Century Data Systems
A Xerox Company

Century Data Systems
1270 N. Kraemer Blvd.
Anaheim, CA 92806

North American Headquarters
(714) 632-7500

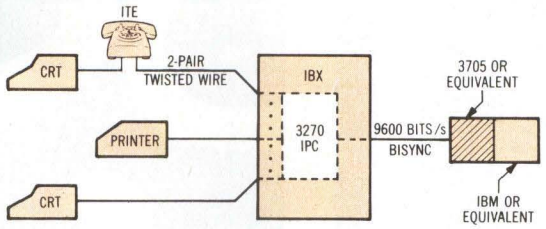
DATA COMMUNICATIONS

Variations in line conditions are compensated for by automatic adaptive equalization, with no manual adjustment required. Typical error rate is 1 in 10^6 with signal to noise ratio of 25 dB on simulated 3002 unconditioned lines. The unit can tolerate up to 5-s line transients without having to retrain. The modems are equipped with pushbutton switchover to dial backup lines.

Modulation technique is 8-phase, 4-amplitude quadrature (QAM). Transmit signal levels are 0 to −16 dBm (domestic) and −5 to −21 dBm (international), adjustable in 2-dB increments. Dynamic range of the receiver section is 0 to −34 dBm, without adjustment.

Dimensions are 19″ x 3.5″ x 12.5″ (48 x 8.9 x 31.8 cm), and weight is 16 lb (7 kg). Price is $5500. The unit is also available without the bandsplitter (DL 96/V.29) at $4500. Delivery is 45 days.

Circle 242 on Inquiry Card



Simultaneous voice transmission plus IBM 3270 emulation. System handles simultaneous voice and data communications on same 2-pair twisted, building-wide wiring plan. CRT terminals can be up to 8500′ (2591 m) from IBX using optical fiber and 2-pair twisted cable. Integrated Terminal Exchange (ITE) is company-provided electronic station instrument into which CRT can be plugged directly

Any combination of standard ASCII CRTs and printers, in increments of up to 16 devices, can be supported by each 3270 IPC. Data switching capabilities of the IBX S/40 allow any user CRTs to be located throughout a building and still remain multifunctional. Formatted screens, protected fields, and program function keys are supported. The IPC also acts as a port contention device for any number of terminals that may be queued for busy ports, to maximize port usage during busy periods.

Plans for future IPCs include support of a number of office automation devices, as well as support of such local area networks as Z-Net™ and Ethernet™.

Circle 243 on Inquiry Card

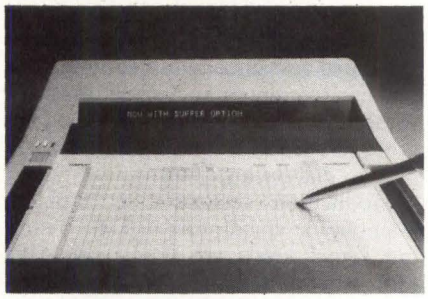
Packet controllers convert formats and protocols via digital switch system

A family of packet controllers called InteNet adds new local area networking functions to the switching capabilities of Integrated Business Exchange Series 40 (IBX S/40) from InteCom Inc, 16509 Addison Rd, PO Box 401467, Dallas, TX 75240. IBX S/40 is a 4000-port nonblocking voice/data switching system that supports simultaneous voice and circuit switched data from 110 to 56k bits/s on a per user basis. The InteNet concept allows the IBX S/40 to be equipped with a family of InteNet Packet Controllers (IPCs) that use internal packet switching techniques to provide format and protocol conversion.

First offering in the product family, 3270 IPC, allows industry standard ASCII terminals to emulate IBM 3277 devices connected to an IBM or equivalent host. The IPC supports Bisync communications with the host processor at 4800- or 9600-bits/s data rates and appears to the host as an IBM 3271 Model 2 control unit. No software changes are required in a basic configuration.

DATA COMMUNICATIONS

Handprint data entry device emulates asynchronous buffered CRT terminal



Handprint data entry device. User can select any line for display by touching area to left of line. Line or page can be transmitted by touching area to right of line. All lines added since last transmission will be sent to host computer. Characters can be changed by writing over them

Buffered Micropad converts data printed by hand on a pressure-sensitive writing surface to standard ASCII code. The buffered device is an enhancement to the unit introduced last year by Micropad, Inc, 35 E Wacker Dr, Suite 1510, Chicago, IL 60601. It allows users to enter a line or a page of up to 512 chars, edit or verify on an integral 40-char LED line display, and transmit the data to a local host or to a remote timeshare computer using a standard 110-, 300-, 600-, or 1200-baud modem.

The information is written in a grid of 16 rows x 32 col or 10 rows x 28 col, switch-selectable, using an ordinary pen or pencil. As the letters or numbers are written they are converted, character by character, into ASCII. Each character may be transmitted for processing together with two additional characters (triplet mode) that identify its position on the document. Alternatively, the data may be stored within the unit (buffered mode) and transmitted as a block of 512 characters. Entered data or application responses from the host system may be output to the line display or to an optional CRT display.

User commands are available via standard positions on the top line of the writing area. They are: mode select (buffered or standard); upper- or lowercase; page clear; break; and up to 3-char termination for each transmitted data block. Unit price for the device is $3100, with OEM discounts available. Delivery is 60 days ARO.

Circle 244 on Inquiry Card

COMBINATION PLATTER FOR DEC SYSTEM USERS.

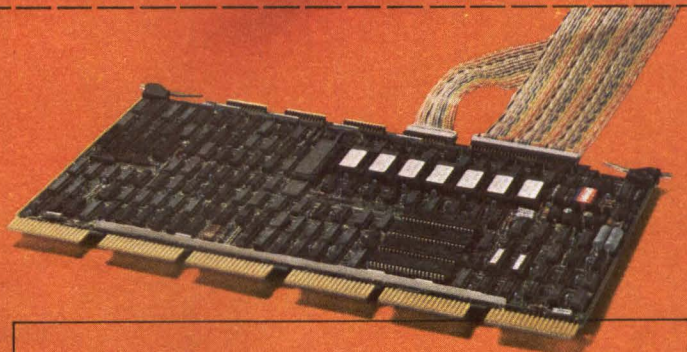
AED's new single-board controller mixes SMDs and Winchesters.

Chinese cuisine is probably the most eclectic in the world. The blending of carefully prepared foods with exotic herbs and spices is a centuries-old art developed to perfection by the Chinese and relished the world over.

DEC users will also relish the added system flexibility obtained with our new STORM 25™ controller board. It allows you to mix 80 and 300 megabyte storage module drives and SMD-compatible Winchesters in any combination you please. Up to four drives can be accommodated by this single-slot, HEX board controller. And there's no compatibility problem, because STORM 25's on-board firmware emulates the RM02 and RM05 disk systems, and is transparent to DEC's operating system and diagnostics. Media may be interchanged, too, because STORM 25's pack format is identical to that of the RM02 and RM03 (80 MB), or RM05 (300 MB).

Another tasty feature is STORM 25's external Writeable Control Store (WCS) capability. This allows the OEM or system user to functionally replace firmware control store memory. The STORM 25 hardware also provides a unique self-test capability that automatically tests all major functions of the controller 'in system'.

Unique configuration flexibility. Cost-effective multi-disk control. Plus easier field maintenance. STORM 25 is definitely a controller for disk connoisseurs. Call or Telex our Marketing Department today for the sales office nearest you. 30-day delivery. Advanced Electronics Design, Inc., 440 Potrero Ave., Sunnyvale, CA 94086. Phone 408-733-3555. Telex 357-498.



If normal bingo response time is too slow for your needs, please attach your business card to this coupon and mail today! Or call **(800) 824-7888.** From California call **(800) 852-7777.** Ask for operator 604.

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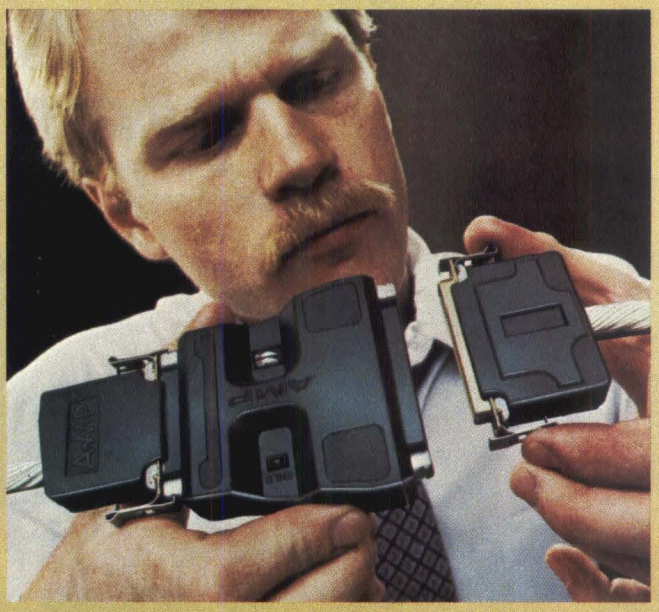
440 Potrero Ave., Sunnyvale, CA 94086. Phone 408-733-3555. Telex 357-498.

cd97

RS 232 and RS 449, bring them together with our subminiature Ds. It's easy.

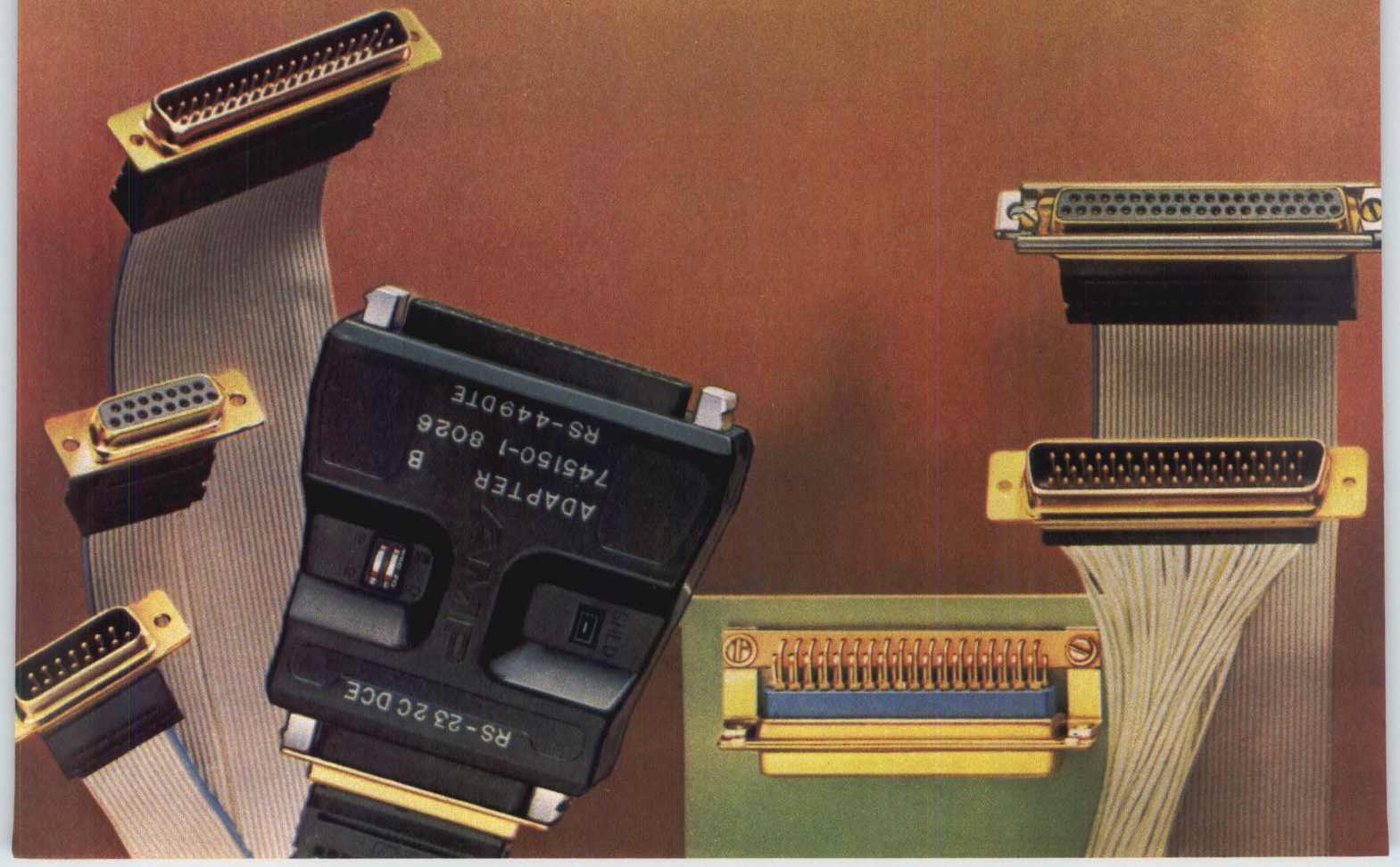


Save your systems from obsolescence. Bring them up to the standard with AMPLIMITE subminiature D adapters.

They interface RS 232 with the new RS 449 cable-to-cable or directly to your equipment. One way or the other, you save the cost of major redesign.

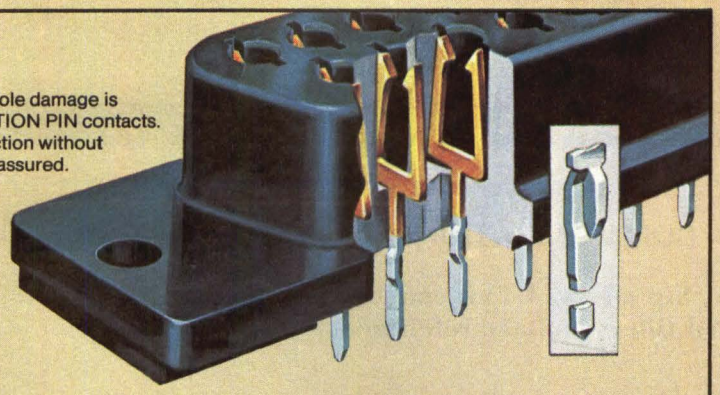
Our subminiature Ds also give you the widest choice. Metal shell and all-plastic connectors. Filtered assemblies. Mass termination styles. Standard, high density and MIL-C-24308 versions. And the most complete selection of accessories made.

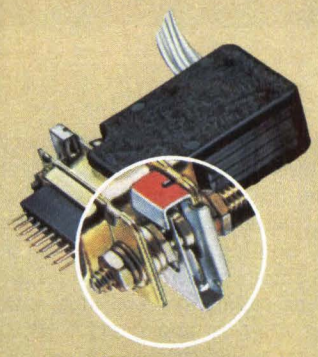
You bring a lot together with our AMPLIMITE connector system.



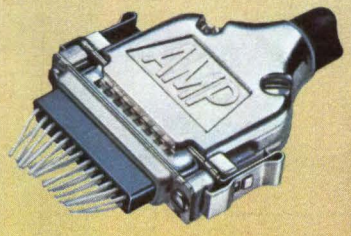
AMP Facts

Plated-through hole damage is avoided with ACTION PIN contacts. Gas-tight connection without soldering is also assured.

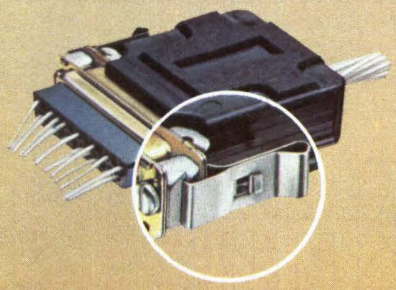




Two styles of slide latch clips simplify plug and receptacle mating.



Metal-shelled shielded connector provides EMI protection.



Spring latch assembly allows easy harness hook-up to RS 449 standards.

For more information, call the AMPLIMITE Connector Desk at (717) 780-8400.

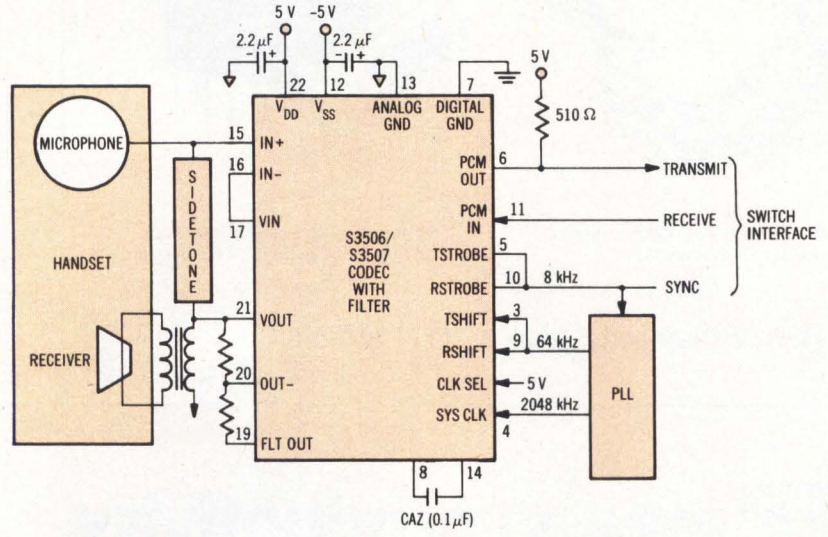
AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.

CIRCLE NUMBER 10

DATA COMMUNICATIONS

Single-chip μ-Law/A-Law codecs incorporate onboard filters, voltage reference



Voice processing in digital telephone application. Transmit and receive timing signals are common since asynchronous operation is not necessary. Phase lock loop (PLL) derives 2048-kHz system clock and 64-kHz shift clock from 8-kHz sync signal received from switch. Sync signal also serves as transmit/receive strobe signal. Microphone output feeds directly into coder input while decoder output drives receiver through impedance matching transformer

Improved A-Law (CCITT) S3506 and μ-Law (North America) S3507 are monolithic 4-μm silicon gate CMOS companding encoder/decoder chips, designed to implement the per-channel voice frequency codecs used in PCM systems. The chips, developed by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, use 60 mW operating and 5 mW idle power, and operate from dual ±5-V power supplies. The chips incorporate the band limiting filters and A-D conversion circuits that conform to the desired transfer characteristic.

The chips have independent transmit and receive segments with greater than 75-dB isolation. The sections use switched capacitor filter techniques and are complemented by an analog filter and programmable I/O op amps onchip for anti-aliasing and gain adjustment. No external anti-aliasing prefilter is required. Voltage references are derived onchip from the 8-kHz strobe present on the line card. Idle channel noise reduction circuits reduce interchannel crosstalk by 75 dB and idle channel noise by 15 dBrnc0.

For an 8-kHz sampling rate the PCM I/O data rate can vary between 64k and 2.1M bits/s. Separate transmit/receive timing allows synchronous or asynchronous operation. The output op amp delivers ±3.1 V into a 1200-Ω load, or can be switched off for reduced power (48 mW). The encoder has a dual-speed autozero (AZ) loop for fast acquisition on power-up. Absolute group delay is 410 μs at 1 kHz.

These circuits provide the interface between subscriber loop analog signals and the digital signals of the PCM highway in digital telephone switching systems. They come in 22-pin packages with 0.400″ (1-cm) centers, and require only an AZ capacitor and an output pullup resistor as external components. The chips can be used in such PCM applications as exchange, PABX, channel bank, digital telephone, fiber optic, or other non-telephone uses. A 28-pin S3507A chip provides standard μ-Law A/B signaling capability. The units meet or exceed AT&T D3 and CCITT G.711, G.712, and G.733 specifications.

A typical digital telephone application is shown in the Figure. Many new PABX designs use PCM techniques for voice switching, and there is a growing trend toward their application at the telephone level.

Circle 245 on Inquiry Card

Communications processor supports simultaneous RJE and transaction processing

Operating as a frontend or network processor, the Distributed Communications Processor/20 (DCP/20) is a medium performance modular hardware system that uses distributed communications architecture. Developed specifically for network applications by Sperry Univac, Div of Sperry Rand Corp, PO Box 500, Blue Bell, PA 19424, the system supports simultaneous remote job entry and transaction processing.

Based on multiple microprocessor and LSI technology, the system consists of a processor, local storage, and communication line modules. System memory is an IC error correcting storage system that expands in 128k-byte increments from a minimum of 256k 8-bit bytes to a maximum of 512k bytes. Mass storage disc and magnetic subsystems, and host interface modules, are also available.

The system provides network control, a wide range of data transmission rates, multiple terminal type support, modularity with system growth capabilities, and the ability to tailor communication networks to fit data processing and transmission needs. It can handle up to 45 communication lines and accommodate asynchronous, synchronous, and wideband transmissions at speeds up to 64k bits/s. It also supports the universal data link control procedure, as well as character oriented communications protocols.

Circle 246 on Inquiry Card

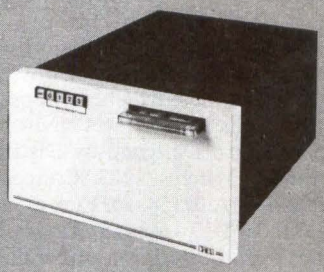
Build your own DEC system with CRDS...

MF-211

10½" Enclosure for LSI 11/23 System with built-in RX02 equivalent floppy disk system. Available with or without processor and memory.

HD-11/T

20.8 Megabyte Winchester disk software equivalent to 4 RL01 units. Optional cartridge tape backup.



FD-311

RX02 equivalent dual floppy system, single or double sided. Includes bootstrap loader, self-tester, formatter and diagnostic diskette.

MB-211

5¼" enclosure with 8 quad slot backplane. Front panel console with switches for Enable/Halt, Boot/Init and Line Time Clock.

Complete software compatibility at a savings!

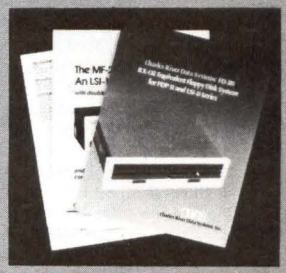
With CRDS, you can configure your own DEC system and be assured of complete software compatibility. Each of the above systems is provided with slides for rack mounting or can be used in desk top applications. All DEC LSI 11 based modules and associated software packages are available through CRDS, if desired.

Attractive Packaging
Careful attention is given the CRDS repertoire of enclosures in assuring you an attractive yet comfortable blending of product in the DEC environment.

Significant Savings
Flexibility of procurement plus attractive OEM schedules allows you to optimize dollar savings in configuring your CRDS system. Use the time tested technique. Compare.

Warranty and Maintenance
A 90 day warranty is offered with your CRDS system. In the event of malfunction, by use of provided diagnostic routines, the defective submodule is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.

Call or write for a comprehensive literature package and prices.



CRDS

Charles River Data Systems, Inc. 4 Tech Circle, Natick, MA 01760 Tel. (617) 655-1800 TWX (710) 386-0523

CIRCLE 20 ON INQUIRY CARD

CONTROL & AUTOMATION

Industrial chassis offered for distributed control environments

A Multibus compatible industrial chassis, ICM/80 is offered for distributed control environments where floppy disc storage media cannot meet environmental conditions. Designed by Distributed Computer Systems, 223 Crescent St, Waltham, MA 02154, for rack mounting in a standard 19″ (48-cm) RETMA housing or, with the addition of brackets, in a NEMA sealed enclosure, the chassis can contain software in P/ROM or can be downline loaded using RS-232 interfaces or multidrop modems over twisted pair.

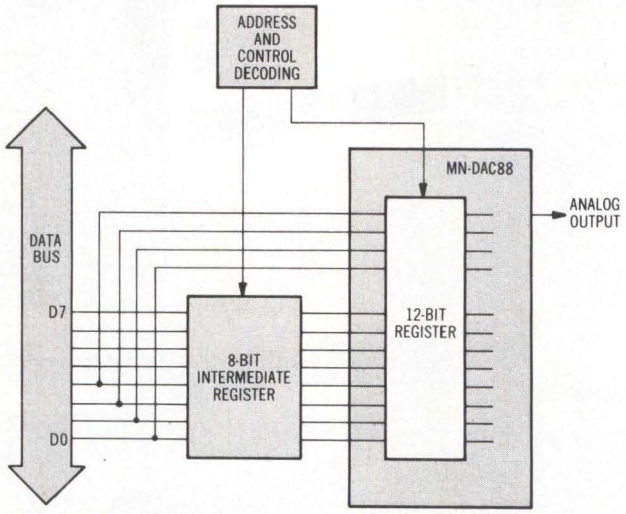
The chassis contains an all-aluminum 9-slot Multibus card cage with integral fan assembly. A second cage can be mounted for a total of 18 card positions, or a UPS or sealed Winchester disc can be mounted in this area. Up to four signal conditioning I/O panels can be mounted on the front of the chassis, making up to 64 opto-isolated channels available for control applications. Panels include plug-in fuses, LED status indicators, and pullup resistors. The front panel controls system reset, 60-Hz (50-Hz) line clock, HALT/ENABLE, and a power off/on/lock keyswitch.

The chassis measures 19″ x 17″ x 12″ (48 x 43 x 30 cm), providing compatibility with the Intel ICS/80. Its power supply provides 5 V at 25 A, 12 V at 2 A, −5 V at 2 A, −12 V at 2 A, and 24 V at 1.5/3.4 A. The chassis is compatible with any of the company's CPU, memory, or I/O modules.

Circle 247 on Inquiry Card

DATA CONVERSION

Military 12-bit DAC has fast TTL input register



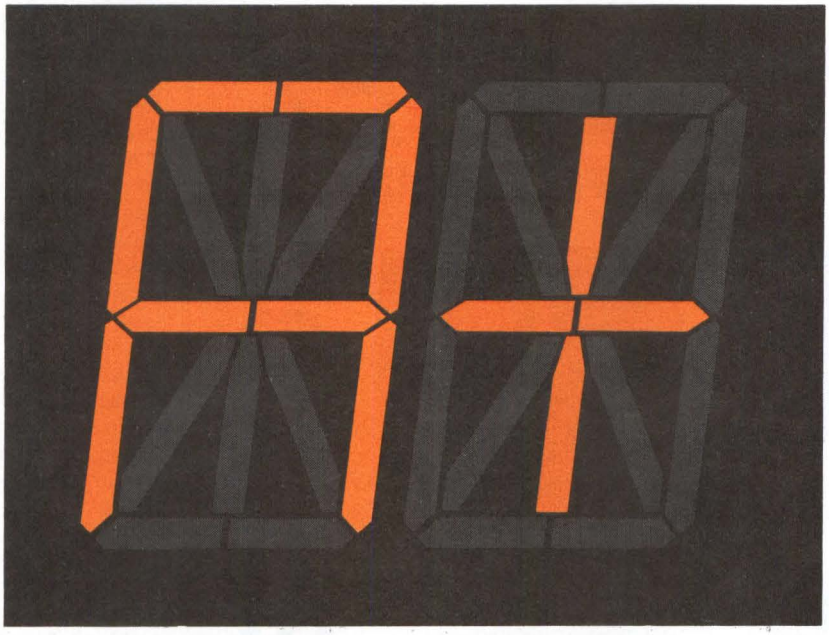
MN-DAC88 12-bit DAC interfaced to 8-bit microprocessor. 8-bit intermediate register is used for double buffering to avoid undesirable analog output slewing

MN-DAC88 is a 12-bit DAC with digital inputs that are TTL compatible and an internal input register that provides easy interfacing to micro- and minicomputer data buses. The device is manufactured by Micro Networks Co, 324 Clark St, Worcester, MA 01606. Three user selectable output ranges are available (0 V to 10 V, ±5 V, and ±10 V). Performance features include fast output settling (6 μs for a 20-V change), ±0.1% FSR maximum absolute accuracy, and ±½ LSB linearity and monotonicity guaranteed over the full operating temperature range. Maximum power consumption is 760 mW.

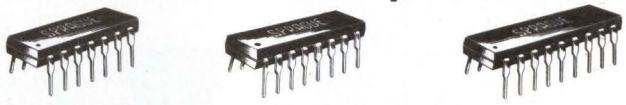
The DAC is functionally laser trimmed for linearity, gain, and offset, eliminating the need for external potentiometers.

(continued on page 46)

BE SMART ABOUT COSTS WHEN YOU WANT TO BE BRIGHT ABOUT DISPLAYS.



Sprague Electric continues to be No. 1 for cost-effective volume production of bipolar gas-discharge display driver ICs.



As the need for larger and brighter gas discharge displays has been increasing, Sprague Electric has been continually expanding its skills in the manufacture of bipolar high-voltage drivers.

For nearly 10 years, Sprague has employed state-of-the-art processes to produce millions of display drivers with voltage ratings well in excess of **100 V**. We have combined these processes with logic and buffers in a single unit, permitting a lowest-cost approach to integrated high-voltage circuitry. As a result, both the reliability and economy of Sprague drivers have been repeatedly proven in point-of-sale terminals, computer peripherals, avionics, instrumentation, electronic games, etc. Sprague is now developing **200 V** monolithic integrated circuitry for release shortly.

For Engineering Bulletins 29301C, 29302, 29303, 29311A, and 2913B, write to: Technical Literature Service, Sprague Electric Company, 555 Marshall St., North Adams, Mass. 01247.

For application engineering assistance, write or call Mark Heisig or Paul Emerald, Semiconductor Division, Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.

For the name of your nearest Sprague Semiconductor Distributor, write or call Sprague Products Company Division, North Adams, Mass. 01247. Telephone 413/664-4481.

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CIRCLE 21 ON INQUIRY CARD

DATA CONVERSION

Units are available for three operating temperature ranges (0 to 70 °C, −25 to 85 °C, and −55 to 125 °C). Linearity and accuracy are tested 100% and guaranteed, both at room and extreme temperatures.

Applications include microprocessor based data distribution systems, programmable power supplies, and servo drivers. Packaged in a hermetically sealed ceramic 24-pin DIP, the device is complete with internal reference and output amplifier. Optional MIL-STD-883 processing and guaranteed linearity and accuracy specifications over the −55 to 125 °C temperature range make the MN-DAC88 a suitable choice for military avionics and fire control systems.

Interfacing the DAC to 8-, 12-, and 16-bit microprocessors is simplified by the internal 12-bit register. External address and control decoding are required, however.

Interfacing to 12- and 16-bit processors is fairly direct and can usually be accomplished by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line and using the output to drive the register enable input. For most processors, valid data remain in the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the DAC immediately after one of the addresses or control signals changes but before valid data go away.

Interfacing to 8-bit processors is slightly more complicated; an 8-bit external register is needed. (See the Figure.) Address decoding must be organized such that the 8-bit intermediate register and the DAC's internal 12-bit register appear at two different addresses. The 12 bits of digital data are sent to the DAC via two data transfers. First, the 8 LSBs of digital data are written to the intermediate latch. Then, the 4 MSBs of digital data are written to the 12-bit latch. The result is that the 4 MSBs on the data bus and the 8 LSBs held in the intermediate latch are all latched into the DAC latch simultaneously. This technique is called double buffering; it avoids the analog output slewing to an undesirable state, which would be determined by the LSBs of the new digital data and the MSBs of the previous digital data.

Circle 248 on Inquiry Card

12-bit wide, 6-word deep FIFO register on CMOS DAC

A CMOS, monolithic, 12-bit DAC contains a 12-bit wide, 6-word deep first in, first out (FIFO) register stack. AD7544, from Analog Devices, Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062, can be interfaced directly to 16-bit microprocessors. Applications are seen in graphics displays, vector scan CRTs and X-Y plotters, complex waveform generation, and ATE.

Twelve-bit words are written to the top of the register stack under the

(continued on page 51)

Image processing systems
Modular graphic display systems
Frame buffers–Television monitors

Grinnell has them all, for almost any application: from simple black and white line drawing to full color image processing. Select a packaged system, or configure one "your way."

GMR 270 Series: 512 × 512 frame buffers and full color pipeline image processing systems.

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All systems are available in both U.S. and European versions, with plug-compatible interfaces to most minicomputers (including DEC, Data General and PRIME). Proven system designs ensure reliability, and an expanded FORTRAN library and driver package makes operation easy.

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CIRCLE 23 ON INQUIRY CARD

AMI Standard Cells. Custom

designs from basic elements.

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Now AMI offers all the benefits of custom circuits in half the development time and cost. With AMI Standard Cells. Custom designs from standard circuit elements.

How AMI standard cell designs are developed. Computer-drawn custom integrated circuits can be developed quickly from a library of standard logic cells. These logic cells include gates, flip-flops, counter and register bits, and I/O elements that have been previously laid out and tested. The computer combines and arranges the cells to produce a custom design that meets your exact performance needs. In less time, at less development cost. And every circuit is tested to a 0.1% AQL.

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In addition to standard cell designs, AMI offers a full spectrum of other custom approaches to best meet the needs of your market place. Approaches like semicustom logic arrays. Computer-aided and hand-drawn custom circuits. We can even teach you to design your own circuits. And we will provide custom fabrication for your designs.

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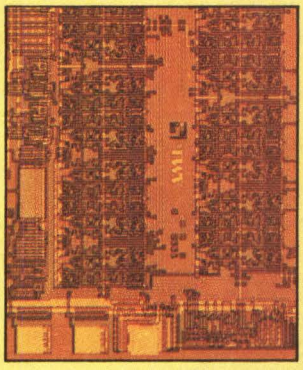
We're designing standard cell circuits in both NMOS and CMOS. And while they won't replace all our custom designs, they can give you a custom circuit for less development money, in less time than ever before.



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The most natural solutions in MOS.

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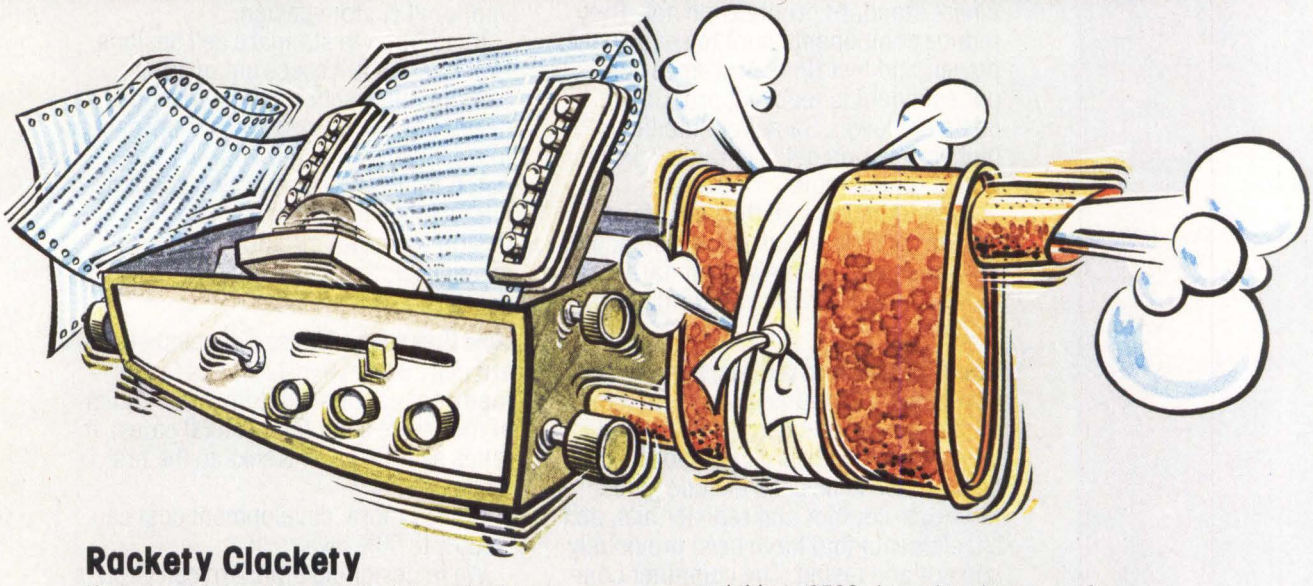
DEPT CD-9

Do You Need to Midasize™ Your Serial Matrix Printer?



Rackety Clackety

If you want the work a matrix printer outputs, you have to live with the noise it puts out. That's the nature of the beast.

Until now.

INFOSCRIBE 1000 is a serial matrix impact printer, but its sound level is **only 53.9 dBA.** By independent sound laboratory test.* No other matrix printer we know of can make this claim.

If you ran **INFOSCRIBE 1000** in the public library, Marian the Librarian wouldn't even look up. It's that quiet.

Our Family Tree

INFOSCRIBE 1000 is not only no nuisance, it's no nonsense. The whole Infoscribe printer family shares technology and parts, cutting down on operator training, maintenance time, parts stocking, and specialized software. And this reflects where it counts: in lower bottom-line cost of ownership.

Cornucopia of Features

We poured features into the **INFOSCRIBE 1000**; it will pour them out for you. Sophisticated features like versatile graphics, under full software control; data processing quality characters at 10, 12, or 16.5 cpi, with correspondence quality characters at 10 cpi; subscripts and superscripts in any selected pitch; double-wide printing, true underlining; three 96-character sets in any alphabets, selectable on a character-by-character basis; rugged tractor feed; and an input buffer expandable to 3532 characters, to name a few.

As for throughput, you'll be delighted. A basic print speed of 180 cpi coupled with vertical and horizontal tabbing, plus bidirectional printing with logic seeking in both directions, pushes work out of the machine at an impressive rate. 100% duty cycle operation, naturally.

Beauty and the Beasts

INFOSCRIBE 1000 sits on a pedestal in your office, but it could as easily sit on a pedestal in the Louvre. It's a wonder of sleek, gracious design that makes competitive instruments, with their protruding ganglia and tumorous knobs, look like props for a horror movie.

And **INFOSCRIBE 1000's** esthetics are pure practicality. They reduce noise, exclude dirt, simplify operation, and put maintenance where it belongs: inside the case. Why not upgrade your computer with a printer that's a work of art: **INFOSCRIBE 1000.**

And Why Not Now

This is the time to place your order for one or a thousand **INFOSCRIBE 1000's.** At $1,825 for single units (considerably less in OEM quantities), Infoscribe's prices are outright philanthropy. Get full details immediately from your local Infoscribe distributor/representative or computer dealer.

Contact Infoscribe for an abstract of the independent testing laboratory report.

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INFOSCRIBE

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CIRCLE 24 ON INQUIRY CARD

DATA CONVERSION

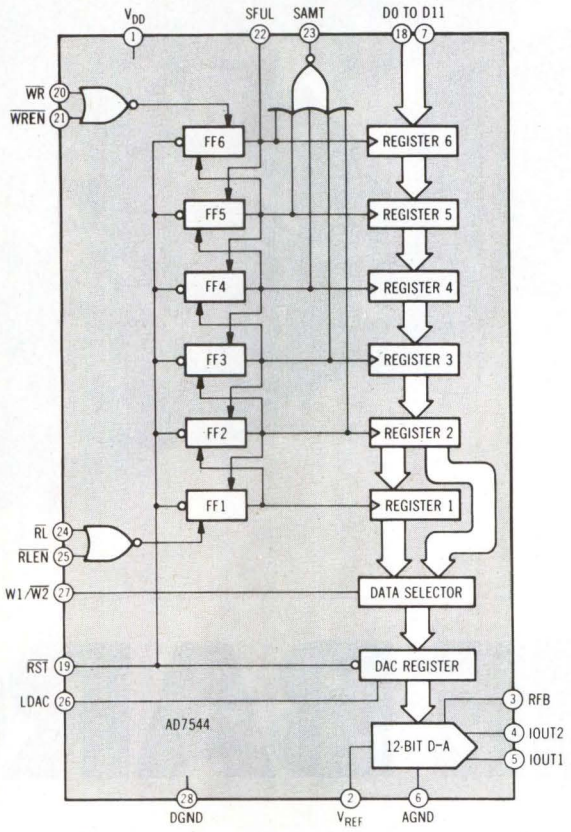
control of $\overline{WR}$ (write) and $\overline{WREN}$ (write enable). (See the Figure.) The 12-bit word then falls through the stack into the empty register nearest the bottom. Hence, the stack is full after 6 write instructions.

Stack contents can be rolled down toward the DAC register under control of $\overline{RL}$ (roll) and $\overline{RLEN}$ (roll enable). The DAC register may be loaded with either word 1 or word 2 of the stack, depending upon the word-selector control input W1/$\overline{W2}$. System reset $\overline{RST}$ loads all 0s into the DAC register and resets the stack register control flipflops to allow a full 6-word load operation.

The multiplying DAC draws 2 mA, maximum, from a single 5-V power supply. Gain drift is 5 ppm/°C, maximum, for all grades. Initial gain accuracy is trimmed to ±1 LSB, maximum, on all G grades, eliminating external gain trimming in many applications. Relative accuracy over temperatures is guaranteed at ±½ LSB, maximum, for K, B, and T grades, and at ±1 LSB, maximum, T min to T max, for J, A, and S grades.

The DAC is available in a plastic (N suffix) or ceramic (D suffix) 28-pin DIP. Operation is specified over the 0 to 70 °C temperature range for JN, KN, and GKN grades, the −25 to 85 °C range for AD, BD, and GBD grades, and the −55 to 125 °C range for SD, TD, and GTD grades.

Circle 249 on Inquiry Card



RFB — DAC FEEDBACK REGISTER
$\overline{RL}$ — ROLL
$\overline{RLEN}$ — ROLL ENABLE
DGND — DIGITAL GROUND
AGND — ANALOG GROUND
FF1 TO FF6 — CONTROL FLIPFLOPS 1 TO 6
IOUT1 AND IOUT2 — OUTPUT FROM R-2R LADDER

AD7544 functional block diagram. Device includes 12-bit wide, 6-word deep FIFO. 12-bit words are loaded into register under control of $\overline{WR}$ (write) and $\overline{WREN}$ (write enable), while 2 status flags, SFUL (stack full) and SAMT (stack almost empty, one word left) control data feed rate from CPU

$17.36

THE BARGAIN IS

It is if you're shipping more than 10,000 logic systems a year.

Because the Plessey Microcell™ approach can replace your multi-chip TTL and CMOS designs with an economical single chip if you're using as few as five standard IC's.

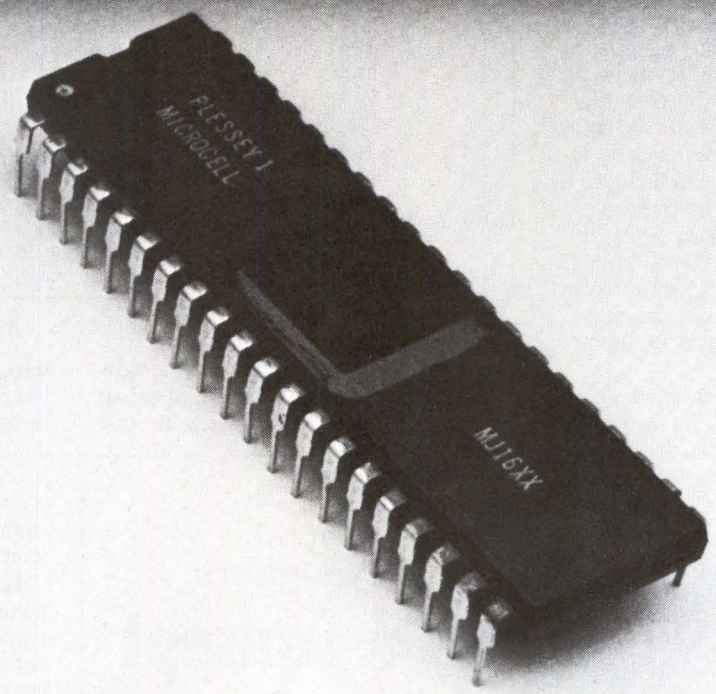
Microcell puts up to 2000 standard 8 MHz N-channel MOS gates on a chip. But the gates are in software, not silicon, so that with our computer-aided design, we can deliver working prototypes just 18 weeks after we get your logic diagrams.

A typical candidate for the Microcell bargain would be a logic system using 12 standard and 3 MSI TTL IC's, the equivalent of 800 gates. At 10,000 systems a year, the TTL devices alone would cost $17.43/system or $174,300/year.

Developing a custom Microcell chip would cost about $30,000 for the first prototype chip.

But Microcell IC's in production would typically be $5.50 in the 10,000 quantity (about $3.50

$30,000



ON THE RIGHT.

at 200,000/year), for a total cost of $85,000. Savings are similar or better for more gates and higher volumes.

And the savings go beyond the lower chip costs, because our one-chip solutions take less real estate, less assembly and much less testing and rework. And eliminate the timing and interface problems of multi-chip designs.

At most, Microcell takes ten per cent more silicon than a custom design, but it gets your systems to market 6 months sooner.

And we all know that time is money, don't we?

For more information, please contact Plessey Semiconductors, 1641 Kaiser Avenue, Irvine, CA 92714. Telephone (714) 540-9979.

Plessey

MORE BUG FOR YOUR BUCK.

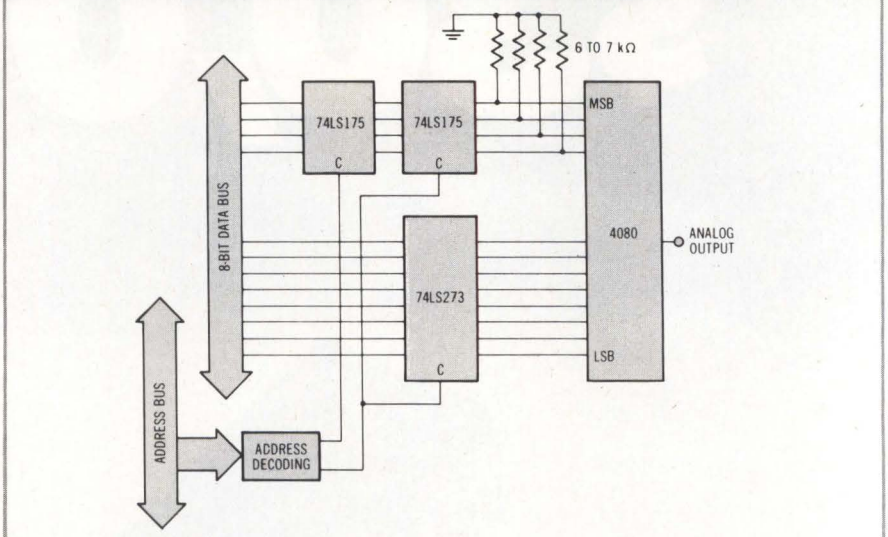
CIRCLE 25 ON INQUIRY CARD

DATA CONVERSION

12-bit voltage output DACs settle in 250 ns

Members of the new 4080 DAC series from Teledyne Philbrick, Allied Dr at Rte 128, Dedham, MA 02026, will settle a 10-V step to ±0.02% FSR (±2 mV) in 250 ns maximum. Typically, they can settle to ±0.01% FSR in that time period. Three devices with different analog output voltage ranges are included in the series. The 4080 includes 0 to −10 V and 0 to −5 V output ranges. 4081 outputs over ±2.5 V and ±5 V, and 4082 outputs over ranges of 0 to 10 V and 0 to 5 V. All three units operate from ±15-V supplies. Power consumption is 900 mW, maximum. Digital inputs are TTL compatible.

The thin film hybrids combine a proprietary, high speed, dielectrically isolated switching network, a low capacitance, thin film, chromium cobalt resistor network; and a discrete fast settling output op amp. Each unit also includes a precision −10-V reference in its hermetically sealed, 24-pin metal dual-inline package. For military/aerospace applications, the 4080 series is available for fully specified operation from −55 to 125 °C with high reliability screening to MIL-STD-883, Method 5008.



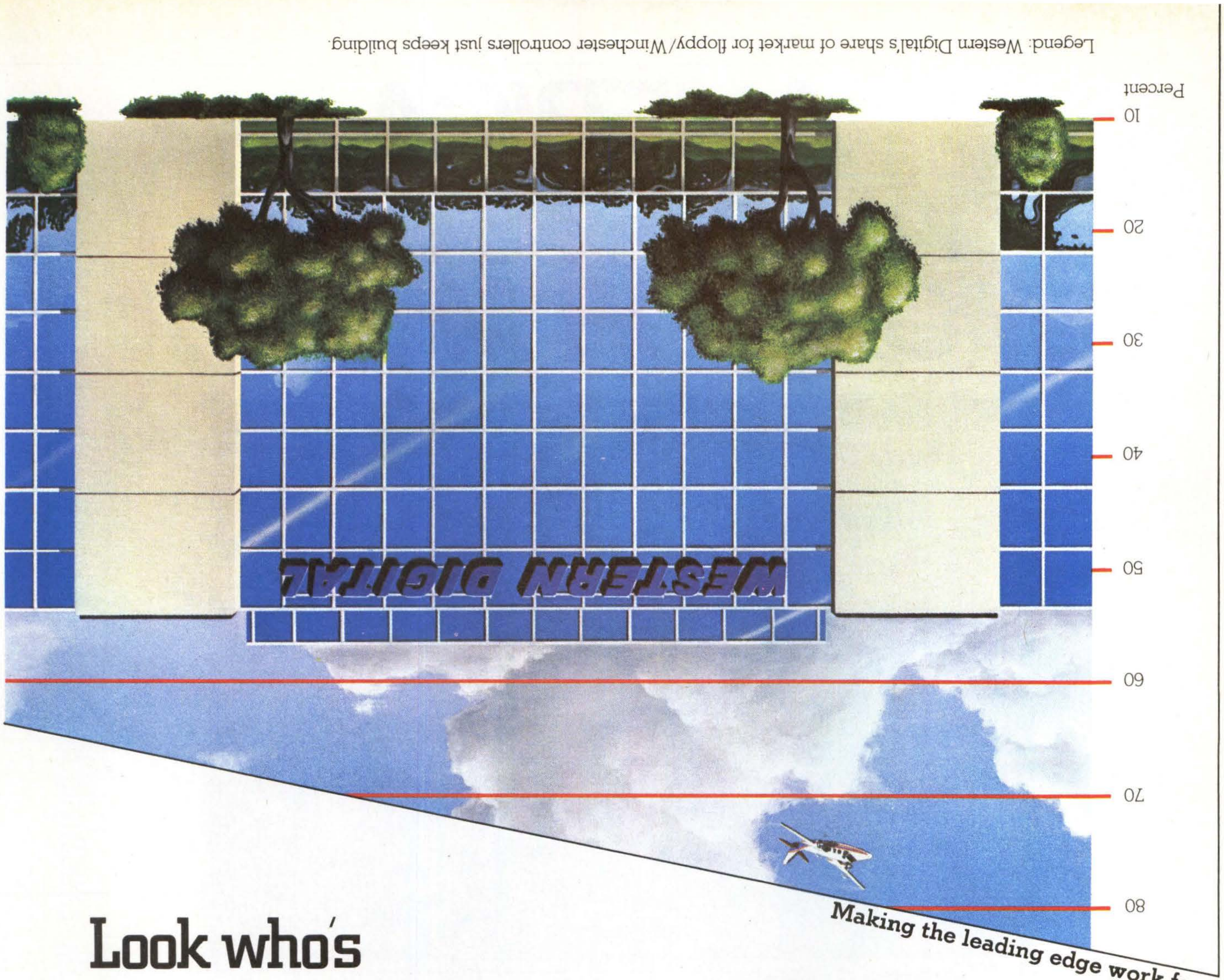
4080 DAC with double-buffered inputs for mating to 8-bit microcomputer

12-bit performance, integral linearity error of less than ±½ LSB, and monotonicity over temperature are guaranteed. Initial offset error (±0.01% FSR) and gain error (±0.1%) are actively laser trimmed at the factory. For most applications, external accuracy adjustments are not needed.

The choice and location of a DAC's input latch is critical. Low power Schottky logic is preferred because these devices usually exhibit data delays between rising and falling signals that are more uniform than those of standard or straight Schottky TTL. Physically, the latches should be as close to the converter as possible, and the lead lengths from latch outputs to DAC inputs should be equal.

The Figure shows a 4080 DAC that has been double buffered for mating to the data bus of an 8-bit microcomputer. The first 4-bit latch holds the 4 MSBs of a given 12-bit digital word. As the 8 LSBs are written to the 8-bit latch, the 4 MSBs are latched into the second 4-bit latch, and the DAC has all 12 of its digital inputs updated at once. By double buffering the MSBs instead of the LSBs, the ability to produce LSB size output changes with a single write cycle is retained and digital feedthrough on the MSBs is reduced.

Circle 250 on Inquiry Card



Look who's turning the disk controller market upside down.

It's no secret. Western Digital has been building a reputation for innovative disk controllers for years.

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What's more, today, Western Digital's 7-member family of floppy disk controllers is *the* industry standard. Giving you nothing short of the broadest selection of controllers in the business.

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Of course, our pioneering Winchester controller effort is equally impressive. Either as a fully-assembled board or money-saving chip set. And our extensive on-line design support services are yet another plus.

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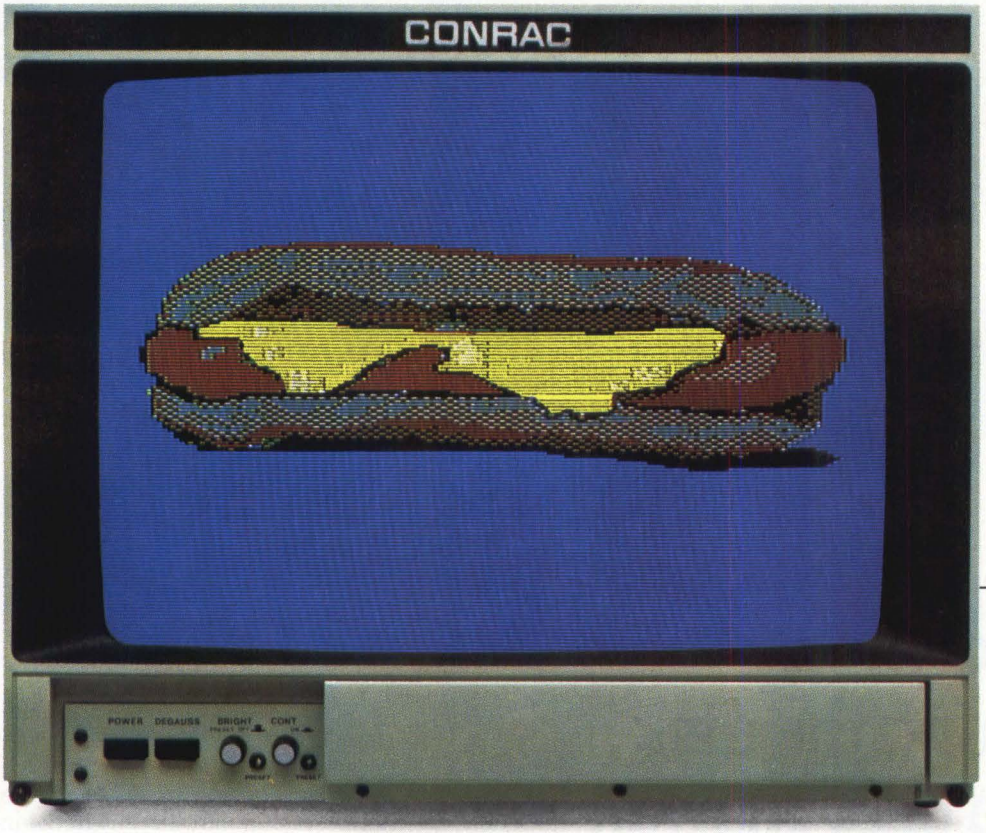

Introducing the Conrac Series 7200, 7100 and 2400.

Just when it seemed like the offshore suppliers might catch up, Conrac stole another technological march.

We've taken the highest resolution CRTs and pushed them to the limit with our proprietary high resolution circuitry.

The combination is unbeatable.

Series 7200 is the monitor for the most demanding engineering graphics system. It pairs a 1280 pixel, .31 mm pitch, shadow mask CRT with circuitry that gives you selectable scan rates from 15 kHz through 36 kHz, twice the normal video amplifier bandwidth (−3 db 40 MHz) and the capability of accepting high resolution EIA RS343 or standard EIA RS170 composite video format. And you have your choice of either 13-inch or 19-inch diagonal screen.

Series 7100 strikes a perfect balance of price and performance for engineering, business and scientific systems. It uses the same high signal resolution circuitry as the 7200 series but utilizes a 500 pixel CRT. You further optimize costs by choosing either a 13-inch (.63 mm pitch) or 19-inch (.79 mm pitch) screen size.

Series 2400 gives you a strong option in high resolution monochrome. With Conrac's proprietary circuitry, this 19-inch tube performs like never before. It accepts either standard resolution EIA RS170 or high resolution EIA RS343 composite video inputs.

Find out more about the new Conrac monitors. And ask us for details on price and delivery. We'll convince you that when America decides to compete, it wins.

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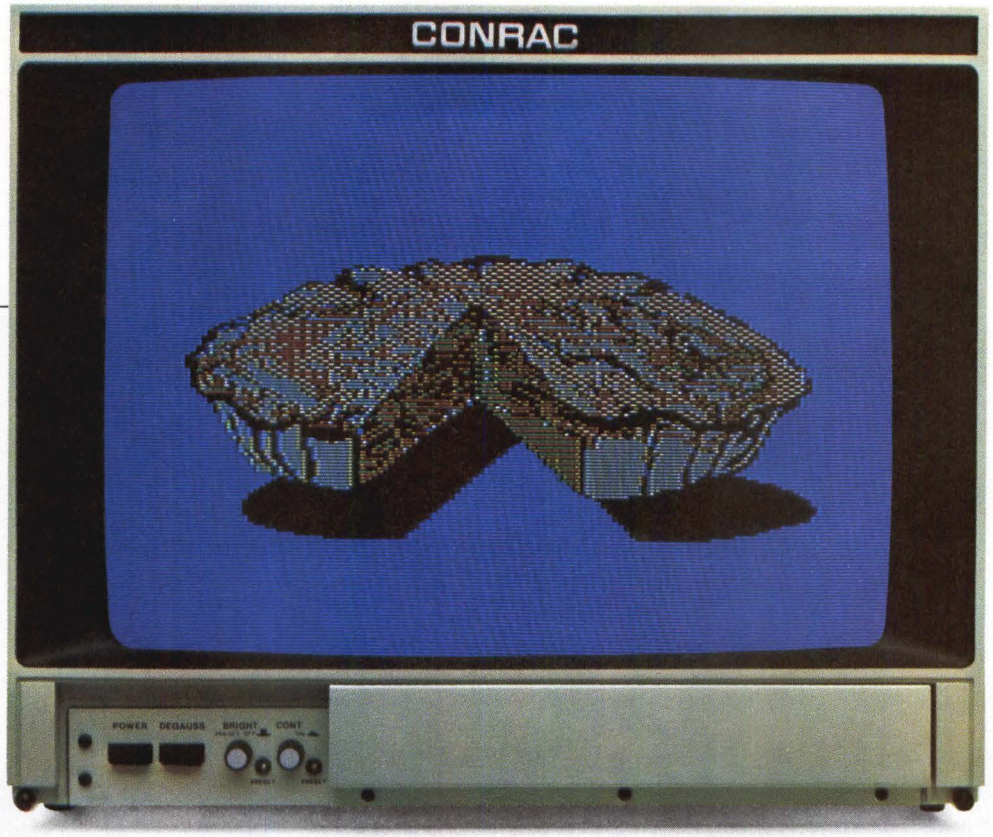

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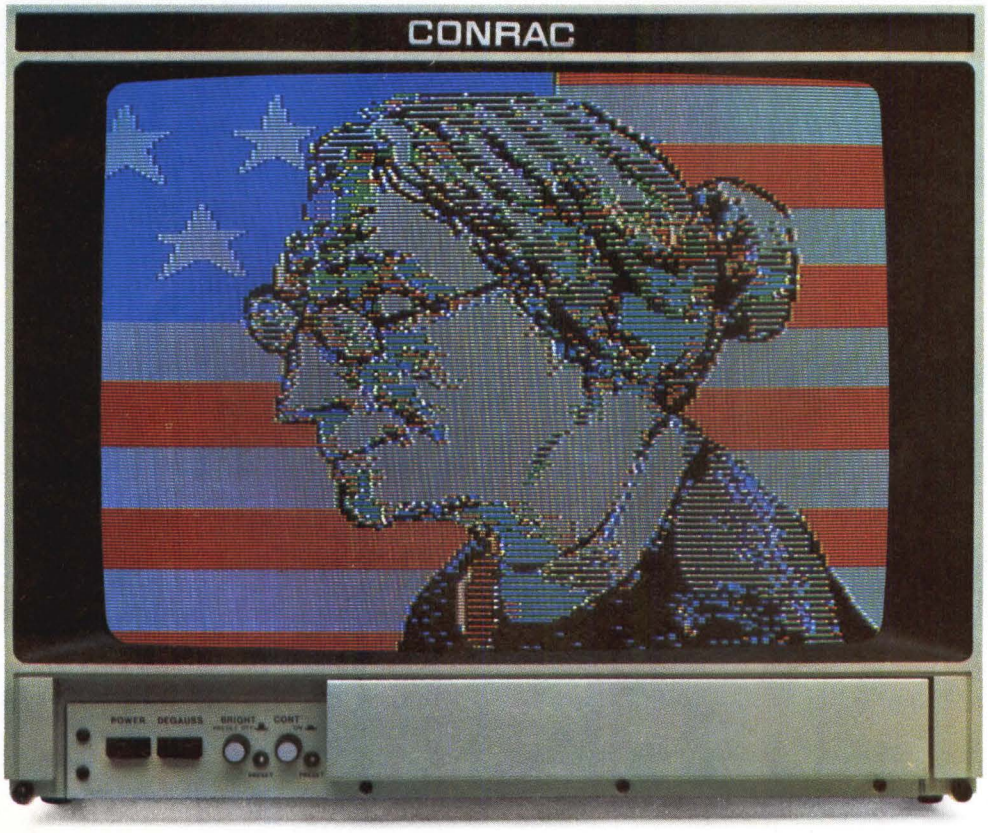
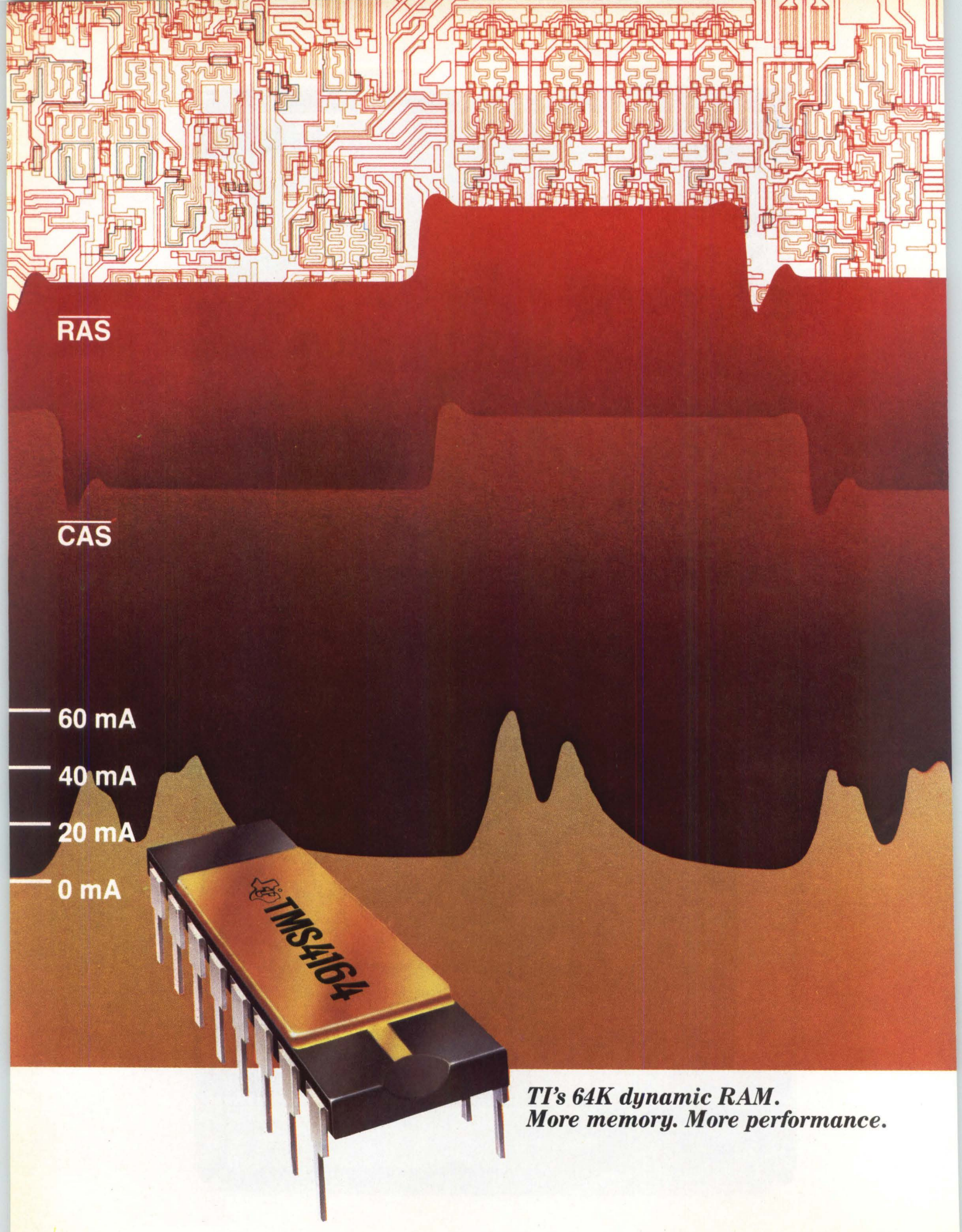


CIRCLE 28 ON INQUIRY CARD



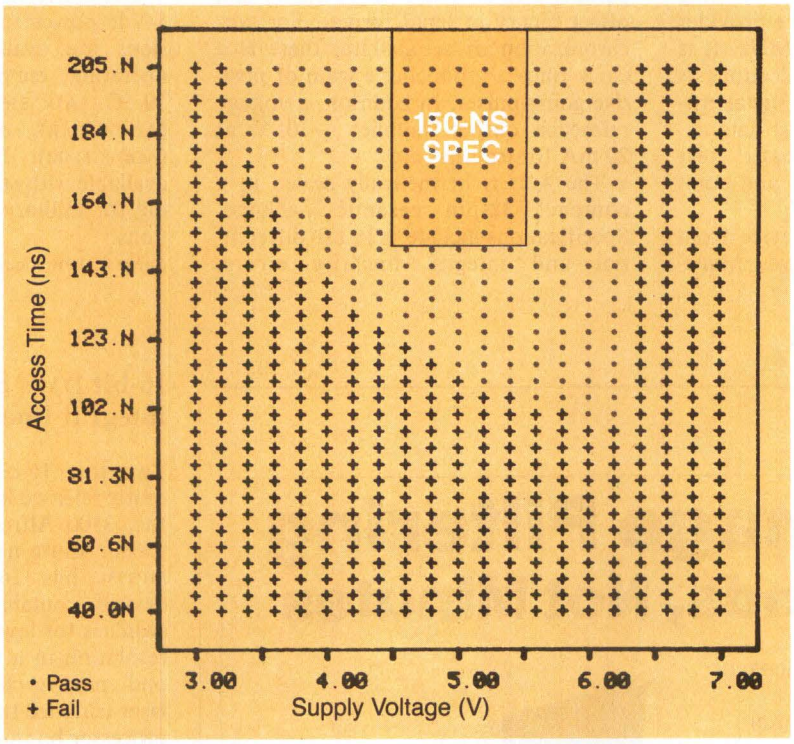
TI's 64K dynamic RAM.
More memory. More performance.

TMS4164

The performance leader. From Texas Instruments.

When we began designing the 64K RAM, we decided to make it better than the 16K. Not just four times bigger.

What's better? In a word, performance. Add up high speed, reliability, low power and improved system operating margins, and you'll see why our superior performance puts the TMS4164 in a class all by itself.



Faster access times
The wide range of TMS4164 functionality and speed potential is demonstrated in the graph to the right. This illustrates the wide operating margins designed into the high-performance 150-ns TMS4164. And, even faster devices are on the way.

Power dissipation
At 125-mW typical, the TMS4164 is unequalled in the industry for low power dissipation. Power design features like interlocked clocks mean you use only as much power as you need. Only when you need it. Our optimum architecture, requiring only 256 sense amplifiers, assures you of minimum power dissipation and enhanced reliability.

Ease of use
Two separate 8-bit internal buffers simplify use — one is for row address, one is for column address. TTL-compatible, one-clock operation greatly expands input timing flexibility and assures fast throughput.

TMS4164 64K Dynamic RAM			
	4164-15	4164-20	4164-25
Access Time Row Address (Max)	150 ns	200 ns	250 ns
Cycle Time Read or Write (Min)	280 ns	350 ns	410 ns
Cycle Time Read/Write (Min)	280 ns	350 ns	410 ns
Power Dissipation Operating (Typ)	140 mW	125 mW	105 mW

Lowest power surge
Our 256 cycle refresh architecture has significantly reduced the current surge problem of designing with other dynamic RAMs. The resultant lower current spikes (≅60mA), less than on *one* 16K dynamic RAM, facilitate system power distribution, increase noise immunity and improve board layout.

And there's more
The TMS4164 is the smallest 64K chip (35K mil²) in production. Perfectly suited for use in main-frame computers and large minicomputers, the TMS4164 also finds ideal application in microprocessor-based systems which demand small size, low cost, and improved performance.

Available now
The high-performance TMS4164 is now stocked for immediate delivery. Order today from your nearest authorized TI distributor. Or, for more information, write Texas Instruments Incorporated, P.O. Box 202129, Dallas, Texas 75220.

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

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CIRCLE 29 ON INQUIRY CARD

DATA CONVERSION

Hybrid 10-bit ADC achieves 800-ns conversion time

A 10-bit ADC has an 800-ns maximum conversion time over its full operating temperature range. The device provides conversion rates up to 1.25 MHz. It is especially useful in such applications as fast servo systems, high speed signal processing, transient analysis, fast data acquisition systems, automatic test systems, pattern recognition, and computerized typesetting systems.

Designated ADC-816, the device from Datel-Intersil, 11 Cabot Blvd, Mansfield, MA 02048, features input voltage ranges of 0 to −5 V, 0 to −10 V, 0 to −20 V, ±2.5 V, ±5 V, and ±10 V. Data outputs are positive logic straight binary; offset binary; 2's complement in parallel format, and straight binary and offset binary in serial format. For synchronization of serial data, there is a clock output producing a train of positive going pulses. In addition, a voltage reference output supplies −10 V at 20 mA for external use.

The ADC is hermetically sealed in a compact 32-pin ceramic package. Specifications include ± ½ LSB differential and integral linearity errors, ±37 ppm/°C maximum gain tempco, and ±12 ppm/°C of full scale maximum zero tempco. ADC-816 has no missing output codes over the rated operating temperature range.

The converter requires ±15-Vdc and 5-Vdc power supply inputs. Three versions are available in the following operating temperature ranges: 0 to 70 °C (ADC-816MC), −25 to 85 °C (ADC-816MR), and −55 to 125 °C (ADC-816MM). In addition, units are available with MIL-STD-883 Class B screening for military and aerospace applications.

Circle 251 on Inquiry Card

16-bit DACs attain ±0.0008% integral linearity

Two true 16-bit linear DACs were recently released by Micro Power Systems, Inc, 3100 Alfred St, Santa Clara, CA 95050. MP370 has 18-bit resolution and MP9331 has 16-bit resolution. Both devices contain storage registers and switches for low linearity error and high resolution in a monolithic chip. A second, passive chip provides multiplying laser-trimmed thin film resistors. Microprocessor bus interfacing is facilitated by an independently latched storage register.

The device achieves an integral linearity of ±0.0008% (16 bits) and differential linearity of ±0.0004%. Converter capabilities include 2- and 4-quadrant multiplication, settling in 2 μs, and a low scale factor drift of ±1 ppm/°C. Both types are TTL/DTL and CMOS compatible, operate from a single 15-V supply, and consume less than 60 mW of power. Input registers provide data storage when latched, or transparent registers when unlatched, so that data conversion can be performed either continuously or from stored data.

Two 18-bit resolution DACs are offered: The MP370B is a 28-pin metal package for military temperature ranges, and the MP370C is a 28-pin metal package for commercial temperature ranges. MP370 is a pin compatible replacement for Hybrid Systems' DAC370-18. MP9331 is supplied in a 24-pin double DIP. MP9331 is a pin compatible replacement for Hybrid Systems' DAC9331-16.

Circle 252 on Inquiry Card

DEANZA MONITORS... WORTH A SECOND LOOK.

Your first look reveals DeAnza's family of sophisticated color monitors, each offering unsurpassed resolution, flexibility and reliability. When you look again, you focus on our very reasonable prices.

Take a look at these advanced features.

DeAnza's family of five color monitors, 13″ and 19″ models, are available in cabinet and rack-mount configurations to match your application and they offer these advanced features:

- 256x256 to 1024x1024 bit resolutions
- Analog displays of from 3,000 to 7,000 alphanumeric characters
- Up to 1,400 line displays
- Shadow mask CRT's with a choice of In-line or Delta-gun
- Variable horizontal and vertical scanning frequencies
- Sophisticated solid state circuitry

Then look at our prices.

If you think our features look good, take a look at our prices. For instance, compare our Model CM19MC monitor to Conrac's 5411C19. For a single unit price of $3,900, the CM19MC offers you features like Delta-gun, virtually permanent convergence settings, shadow mask CRT, analog display to 4,000 characters, 700 display lines and variable vertical and horizontal scanning frequencies.

Call or write for our free monitor brochure.

Whether you're looking at price, performance or both, DeAnza monitors are hard to beat. If you'd like to look a little further, call or write today for our free monitor brochure.

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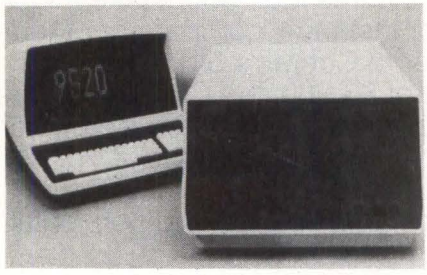
CIRCLE 31 ON INQUIRY CARD

DEVELOPMENT SYSTEMS

Development system and emulator separate software development tasks



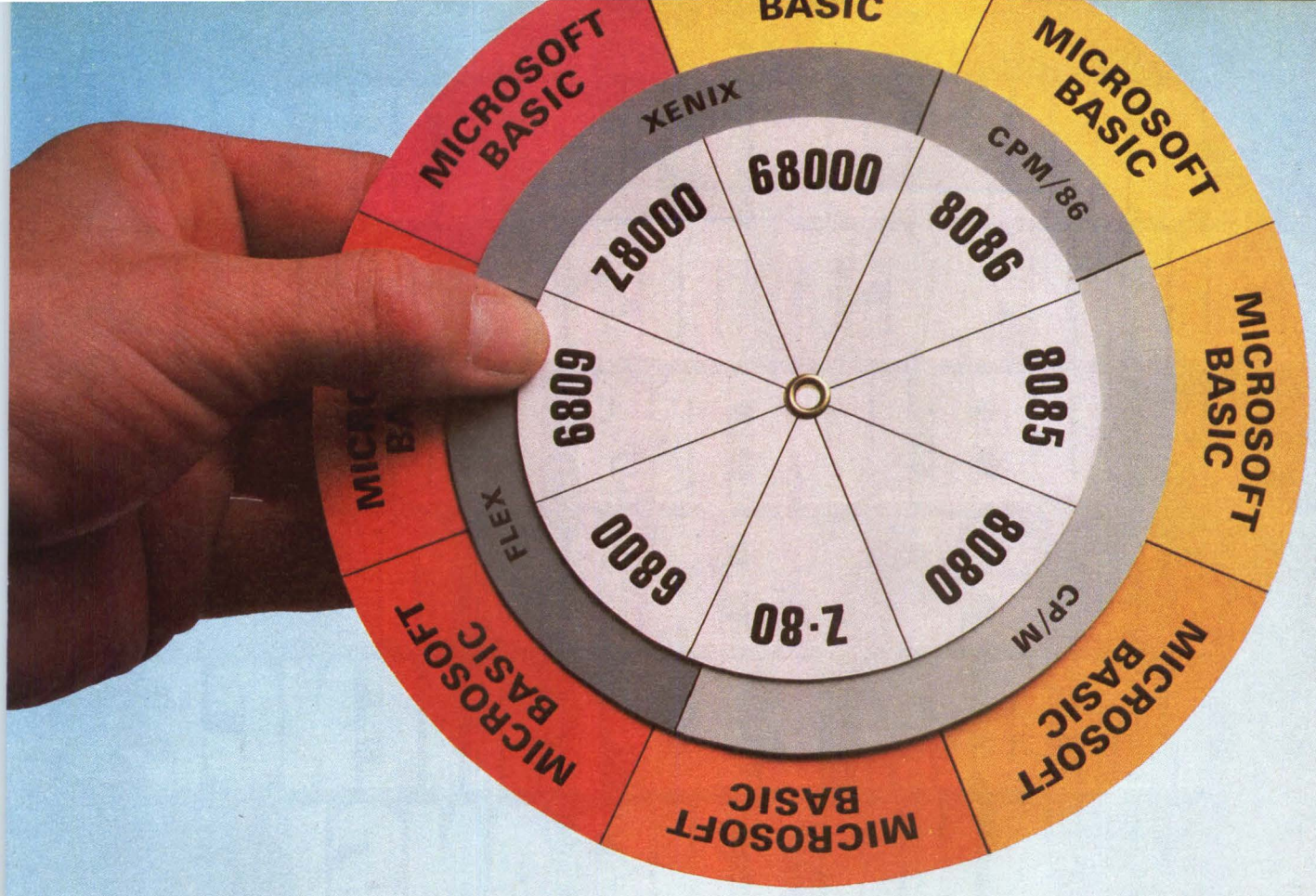
The model 9520 development system, designed to expand to a 2-user system, provides high level languages and a total microprocessor development system in a single enclosure, while the 9508, a stand-alone emulator, supplies an efficient means of developing hardware, debugging software, and integrating hardware and software into a working system. These first members of the 9500 development system family from Millennium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014, distribute the debugging task and offload the software development system by supplying separate software development and debug stations.

Included in the development system are dual double-density floppy disc drives, providing total working storage of 1M byte; 64k bytes of memory, with parity; four serial ports (three RS-232 and one high speed RS-499); an IEEE 488 parallel port; and a self-contained switching power supply. An additional 48k bytes of expansion memory are available on a separate board. DMA access is provided for overlapped processor and disc activity. A built-in system confidence check at power-up verifies operation of major modules and indicates go/no-go in LED displays. Additional user diagnostic programs isolate faults to individual replaceable modules.

Macro assemblers are available with the system to generate programs for the 8080, 8085A, Z80A, 6800, 6801, and 6802 microprocessors, as well as for the 8049 family. Z8000 and 8086 processors will be supported in the future. A linking loader is provided to link relocatable modules and resolve global references. A Pascal compiler offers object code generation for the 8080/Z80/8085 microprocessors, with Z8000, 8086/88 output scheduled for later this year.

Operating under MP/M, the development system uses a screen oriented text editor to speed program preparation and changes and allow operation with multiple CRTs. With the system's multitasking capabilities, two or more functions can be performed simultaneously. All programs developed on the system can be downloaded for execution on the 9508 8-bit emulation system via an RS-232 port. Programs can also be downloaded to the 9516 16-bit emulator via a high speed parallel IEEE 488 port, and access to hard disc and additional computers is available via a high speed RS-422 port to the 9580 multi-user software development system or the RS-232 port to the user's minicomputer. Software drivers provide for serial interface to either Centronics or Tally line printers, and an optional external CRT with ASCII keyboard is available.

(continued on page 66)



If they write it in Microsoft BASIC they'll only write it once.

Transparent BASICs. Microsoft BASIC implementations are user-transparent from system to system. That's what makes them the defacto standard of the industry. Applications programs written in Microsoft BASIC are transportable across systems with little or no modification. That's a powerful selling tool for an OEM. When a customer is ready to move up to a new system, applications software written in Microsoft BASIC is ready to move, too. That's why more OEMs build systems with Microsoft BASIC than with any other implementation of the language.

More BASICs. There are Microsoft BASICs for Z80, 8080, 6800, 6809 and 6502 microprocessors. Off the shelf BASICs for CP/M® and FLEX. There are Microsoft BASICs for the 8086 and Z8000 under such operating systems as CP/M-86® or the XENIX® OS. All of which means that when you're ready to migrate, you or your customers won't have to start developing applications programs from scratch.

Interpreter and compiler. Write and debug programs with the Microsoft BASIC interpreter. Save, execute and distribute programs with our ultra-efficient BASIC compiler. Microsoft BASIC compiled code is highly optimized, fast, and compact.

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Better BASICs. Microsoft BASICs have been in use for over six years and now have more than 700,000 installations. What's more, more applications software has been written in Microsoft BASIC than any other BASIC. Here's why: Microsoft BASIC provides powerful features such as WHILE/WEND, PRINT USING, CHAIN and COMMON, error trapping, protected files, EDIT command, trace facilities, PEEK and POKE, and dynamic string space allocation. Plus, we're adding features all the time—updates are free to most customers.

OEMing hardware? Why not OEM software? Microsoft's aggressive new royalty program makes it easy. Your initial investment is low and you pay us royalties only as you sell systems. Start with the BASICs. But don't forget Microsoft FORTRAN, COBOL, Pascal and the XENIX operating system (UNIX® for 16-bit microcomputers). If you'd like all the details about Microsoft's OEM royalty program, call our OEM Accounts Manager, (206) 455-8080. We'll show you how you can OEM software.

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CIRCLE 33 ON INQUIRY CARD

ONLY ONE OF THESE COMPACT DISK DRIVES DELIVERS BOTH 25 YEARS OF MEDIA EXPERIENCE AND THE ANSI INTERFACE.

THE ONE FROM 3M.

INTRODUCING 3M BRAND COMPACT DISK DRIVES.

A new family of 8" Winchester drives offers you a unique combination of features—features that pay off in high-quality performance, reliability, and product migration. 3M designed and built these drives so that the features would be right for OEM applications—starting with the media itself.

1 WHAT MAKES THESE 3M DRIVES DIFFERENT FROM EVERY OTHER WINCHESTER IN THE WORLD?

Scotch® Brand media. An industry leader for over 25 years. Its proven performance is the cornerstone of our new fixed disk drives. The medium is critical—it's *precisely* where super-reliable data storage should start.

One guarantee of this performance is the thoroughly proven surface lubricant called Lubyte™. Lubyte helps protect against head crashes, loss of data and computer system downtime.

2 COMBINED WITH ANSI INTERFACE: HIGH PERFORMANCE OFF-THE-SHELF.

By using the ANSI interface, these Compact Disk Drives let you take full advantage of state-of-the-art technology for both low-cost design *and* high performance. The standard makes a disk drive's interconnection to its controller easier. 3M has made sure that the new drives deliver the flexibility you need to support specific systems and applications.

The ANSI interface is microprocessor-based, and works efficiently at high data rates. The result: 3M drives are easy on customers' equipment overhead.

3 MIGRATION FROM 10 TO 60 MEGABYTES AND BEYOND.

The third benefit the 3M Compact Disk Drive family gives you is the migration needed to keep up with user demands. Migration that won't dead-end your customers, or cost them an arm and a leg to obtain.

The 3M 8431 drive offers a total unformatted capacity of 10 megabytes on a single disk, with 8649 BPI and an average track density of 219 TPI. The 3M 8432, with two disks, delivers 20 megabytes, with the same bit and track density. The 3M 8533 offers 60 megabytes on three disks, with track density increased to 693 TPI. Modularly expandable, the drives offer you and your customers cost-effective increases in capacity from 10 to 240 megabytes.

4 THE "SUPER-CLEAN" AIR SYSTEM.

Because reliability is so critical to the operation of a sealed-environment disk drive, the drives have a specially-engineered super-clean air system (patent pending). A cast aluminum deck, for example, separates the heads and media from the motors: a feature that helps make 3M's super-clean air system distinct from ordinary systems. Air is cleaned to 10 particles per cubic foot/minute or less.

5 AND OTHER OUTSTANDING FEATURES.

Like microprocessor-controlled rotary actuators (patent pending), drive modularity, data separation and direct track addressing, and low power consumption. Right now, these new drives are the only ones that give you *all* of these features in one 8" Winchester package. It's time to evaluate them against the competition. For complete information write to:

Compact Disk Drives
Marketing, Data
Recording Products
Division/3M,
223-5N, 3M
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3M Hears You...

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CIRCLE 34 ON INQUIRY CARD

DEVELOPMENT SYSTEMS

Model 9508 provides full-speed emulation of 8085A, Z80A, 6801, 6802, 6803, 8048, 8049, 8021, and 8035 microprocessors. When used with the 9520 development system, the CRT used to control the emulator also communicates with the development system in the pass-through mode, allowing the total hardware/software development/integration station to be configured with only one serial port.

The emulator is provided with high speed 16k-byte static RAM (8k standard, 8k optional) emulation memory that is mappable into target system memory spaces on 1k-byte boundaries. Emulation memory can be mapped anywhere in the address space of the microprocessor being developed. During system integration, software can be integrated a module at a time in emulation RAM, then moved to target system memory.

The emulator operates under either an internal or external clock and provides a straightforward command set. An inline assembler enables the user to make program patches using assembly language mnemonics. Disassembly is provided in memory dumps of program segments and realtime trace displays.

Circle 253 on Inquiry Card

Pascal development system features cache memory for CP/M

An S-100 development system for CP/M applications, PDS-80 is designed specifically for systems integrators, applications software developers, and serious end users. The system, a product of Ithaca Intersystems, Inc, 1650 Hanshaw Rd, Ithaca, NY 14850, offers design features that produce the power and speed necessary for rigorous single-user applications.

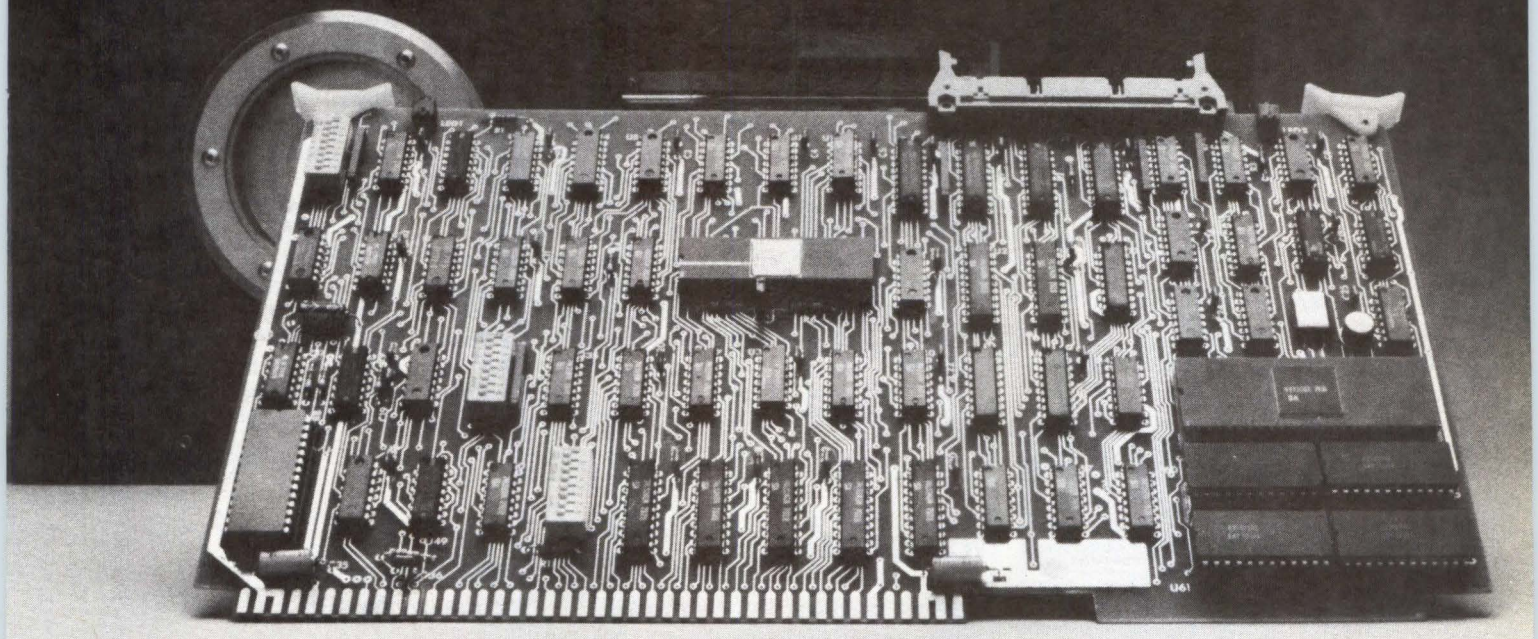
Pascal/Z, a fast Z80 native code compiler, generates ROMable and reentrant object code and relocatable object modules, and permits separate compilation. Since there is no interpreter, Pascal/Z programs execute 5 to 10 times faster than an identical code run under interpretive P-code implementations.

Cache BIOS for CP/M utilizes the DMA and interrupt capabilities of the company's Series II disc controller and memory boards to buffer whole tracks in extended memory, increasing execution speed up to four times. It also includes sophisticated system testing and protection features.

The system's front panel mainframe functions as a diagnostic tool, allowing the user to examine or change any location in memory; set breakpoints in data, address, or status; and single- or slow-step through programs. It also permits the system to be used for both hardware and software development. Two other mainframes are offered: a tabletop version without front panel and a rack-mount version with constant voltage power supply. Both feature a 20-slot

(continued on page 68)

The little guys have done it again.



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CIRCLE 36 ON INQUIRY CARD

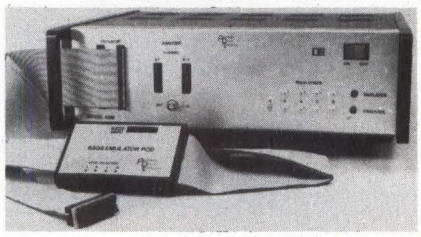
DEVELOPMENT SYSTEMS

S-100 motherboard that provides flexibility in system configuration.

Also included in the system are a 2.4M-byte diskette drive unit and five special utilities written in Pascal. InterEdit is a screen oriented editor for entering documents and programs, while Spell is a spelling editor with a 10M-word user modifiable dictionary. Compare allows the user to view all differences between two files. Quickopy allows the user to copy an entire disc in less time than with the PIP utility from CP/M, and Help allows online access to documentation at both the system and application levels. The complete system is unit priced at $7995.

Circle 254 on Inquiry Card

Emulator/logic analyzer speeds μprocessor development and integration



Model 4009, offered by Advanced Digital Technology, Inc, 13400 Northrup Way, Suite 15, Bellevue, WA 98005, combines features of a realtime, fully transparent 68B09/E emulator and a 12/20-MHz, 18-channel logic analyzer. This packaging method allows the incorporation of previously unavailable features to speed microprocessor integration and development.

A user CRT terminal provides for control and display of emulator and logic analyzer operations. The menu oriented display allows the user to disassemble programs in mnemonic form and control all available system features. Features are controllable by terminal or host computer through three interface ports; two RS-232-C ports and one cassette interface are standard. Baud rates are software selectable from 50 to 19.2k.

Four logic breakevents, in combination with realtime 2k x 56-bit wide trace memory, provide a debugging tool; the trace memory is configured to allow the operator to examine the trace during emulation. Emulator features include a 64k pass counter for individual or multiple breakevents, event to event timing in quarter clock cycles up to 400 s, and fault isolation to card level with LED status indicators. Also featured are memory display of all ROM/RAM locations and modification of all RAM locations, register display and modification of all register locations, user diagnostics, and battery backup.

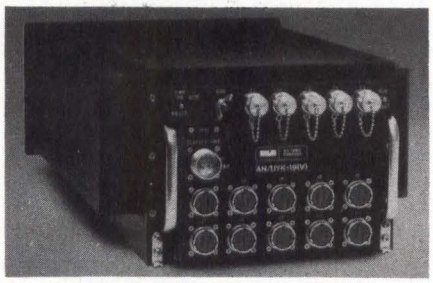
Included in the logic analyzer are two 8-bit logic probes with variable threshold detection and high impedance inputs, and an external clock probe. Features include a 2k x 20 trace with selectable clocks and event interleaving with emulator trace (synchronous and asynchronous operation).

Options for the package include memory overlay of 16k bytes of emulator RAM mappable to the target system in 32 blocks of 0.5k x 8 bits and 32k bytes of emulator RAM mappable to the target system in 64 blocks of 0.5k x 8 bits. An IEEE 488 interface with connector and a Centronix printer interface with connector are available as well. The emulator system is also available without the logic analyzer.

Circle 255 on Inquiry Card

COMPUTERS

16-bit militarized computer uses multitasking operating system



The 16-bit 1666B, an off the shelf military/severe environment computer system, and an enhanced RMX/RDOS multiprogramming, multitasking operating system allow users of the AN/UYK-19 family to advance in technology while maintaining software and interface compatibility. Developed by Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050, the computer is software identical to the 1666 and is designed to meet environmental requirements of MIL-E-5400, MIL-E-16400, and MIL-E-4158. The 1666B is a complete system in a single ATR chassis including processor, power supply, and 8 I/O interface slots. Up to 512k bytes of fast semiconductor or 128k bytes of core memory can be configured in the chassis. Core memory capacity extends to 2048k bytes with expansion memory chassis. Nonvolatile core system performance is rated at more than 275 Whetstone KOPS while 4-way interleaved semiconductor memory exceeds 450 Whetstone KOPS. Floating point capability is available in firmware or high speed hardware.

RMX/RDOS operating system offers multiprogramming with up to 16 concurrent processes. Each process has up to 64k words (128k bytes) of map protected address space; address space can be extended by virtual overlays and window mapping. Installation of a 1- or 2-card conversion kit converts the computer into an MSE/14 Mil-Spec ECLIPSE, and allows use of software from that family as well as that of the Data General ECLIPSE family.

Base price of a 1666B with 128k bytes of core memory is $59,000. System price with a 35.6M-byte military disc, model 4050, is $109,000. License charge for RMX/RDOS with full support is $2400.

Circle 256 on Inquiry Card

MICROPROCESSORS/ COMPUTERS

Bipolar VLSI μprocessor supplies high performance in harsh environments

A bipolar 16-bit microprocessor, the F9445 is claimed to be the fastest single-chip microprocessor available. Offered by Fairchild Camera and Instrument Corp, Microprocessor Div, 4800 Patrick Henry Dr, Santa Clara, CA 95051, in 16-, 20-, and 24-MHz speed ranges, the 24-MHz device has a 250-ns register to register time. The 20-MHz version can perform a 16- x 16-bit multiplication in 3.5 μs.

Designed using the company's I^3L® technology, the high performance VLSI device operates over a temperature range of −55 to 125 °C and in high radiation environments, adapting it to applications requiring full performance in harsh environments. Density and power dissipation achieved with the I^3L technology allow the device to fit into a standard 40-pin package.

The device has a 16-bit multiplexed address and data bus, with eight

(continued on page 70)

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CIRCLE 37 ON INQUIRY CARD

MICROPROCESSORS/ COMPUTERS

program-accessible registers. It supports several address modes, including direct, indirect, indexed, and relative. The CPU has an interrupt system with 16 levels of priority and supports fast channel I/O and DMA. Included in the microprocessor's instruction set are bit, byte, word, and double-word instructions.

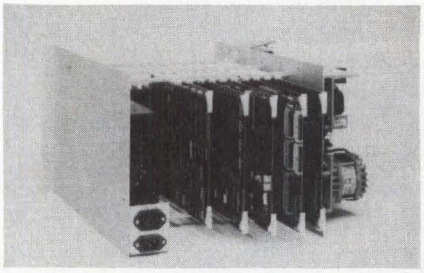
Architectural features of the microprocessor allow the use of high speed, 16-bit multiply and divide instructions. Double-word (32-bit) floating point assist and 8-bit byte instructions, and stack instructions with both stack and frame pointers, allow software floating point arithmetic routines that rival the performance of special purpose hardware and floating point devices.

The microprocessor is complemented by a set of general purpose circuits for I/O, memory interface, and peripheral support. Designed as system building blocks, these circuits match signals and timing to reduce need for additional interconnect logic. Support circuits include an I/O bus controller that generates I/O bus signals and timing, and a multiple data channel controller that supplies handshaking and address signals for data I/O and DMA at up to 50 MHz. A dynamic memory controller, programmable multiport interface, memory management unit, console controller, and in-circuit emulation modules will be available next year.

The FS-I development system supports the microprocessor. Software includes a disc operating system and two high level languages. A prototyping and evaluation board (PEP-45) and application training programs are available as well.

Circle 257 on Inquiry Card

Microcomputers are designed for efficient Pascal execution



The Modular MicroEngine family of microcomputer systems, from Western Digital Corp, 3128 Red Hill Ave, PO Box 2180, Newport Beach, CA 92663, meets the needs of system integrators and OEM designers developing Pascal programs. ME1600 series systems eliminate assembly language, interpreters, and the problems of fitting programs and applications into computer architecture that is not efficient for Pascal.

Five boards in the ME1600 subsystem implement processing, storage, file management, I/O, and user access to the company's Sentinel/24™ bus. Serving as the basis of the series, the subsystem includes a Pascal processor, 128k-byte dynamic RAM module, floppy disc controller, serial/parallel I/O controller, boot terminator module, and 10-slot chassis with 170-W power supply.

The ME1665 system incorporates the subsystem and a double-density, double-sided, floppy disc drive. Included in the ME1670 packaged system are the subsystem, two double-density, double-sided, floppy disc drives, and a desktop enclosure. The ME1675 packaged system is composed of the ME1670 system plus a 150-char/s line printer and an 80-char x 24-line CRT terminal. All four systems execute the company's interactive operating system with text editor, file management, and debugging facilities.

Circle 258 on Inquiry Card

Single-board microcomputer supplies fast video and disc

A single-board, Z80A based turnkey system, the 8-bit Stratos provides software programmable character font and priority masked interrupts for all system parameters. Developed by Symbiotic Systems, Inc, 118 Naglee Ave, Santa Cruz, CA 95060, the system uses a 6-layer single-board construction to minimize connectors, from which many electronic problems arise. The use of all low power circuitry increases reliability by maintaining low operating temperatures.

Included in the system are 80k bytes of RAM, 1.2M bytes (System D8) or 0.65M bytes (System D5) of online storage, and a 12″ (30-cm), high resolution, green phosphor video monitor. Operating at 4 MHz, the system features very fast video and disc routines. The built-in software directed disc controller handles up to four drives in any combination of single- or double-sided, single- or double-density, 5.25″ or 8″ (13.34- or 20-cm) drives with programmable soft-sectored format. A built-in switched power supply provides power for the system, built-in disc drives, and keyboard, and allows quiet, cool, fan-free operation.

The main addressable memory is composed of 64k bytes of dynamic RAM, with an additional 16k-byte bank that is software switchable to the zero position in memory. Within this additional bank, 8k bytes are used for fast floppy data transfers, allowing faster data manipulation within main memory. Another section of this memory is used for system personalization programs. Video mapped RAM is accessed during memory refresh time to avoid CPU delay due to screen refresh. A 2k-byte EPROM is provided in addition to the main memory.

With the FONT^R program, the user can create characters on an 8 x 9 matrix with the system's lightpen. Fonts that have been created (each with a maximum of 256 characters) can be saved on diskette and then recalled for use during word processing. This feature allows the user to alternate between two languages with one keystroke or to perform full editing with mathematical symbols.

The flexible, fully decodable port bus allows the system to function as a member or controller of a distributed intelligence network. Operating under MP/M^R and/or CP/NET^R, each system will perform all of its standard functions, plus multitasking with MP/M, in local mode, and will be able to access a common data base and shared peripherals through the network.

Circle 259 on Inquiry Card

Microcomputer systems offer choice of CPU power and storage capacity

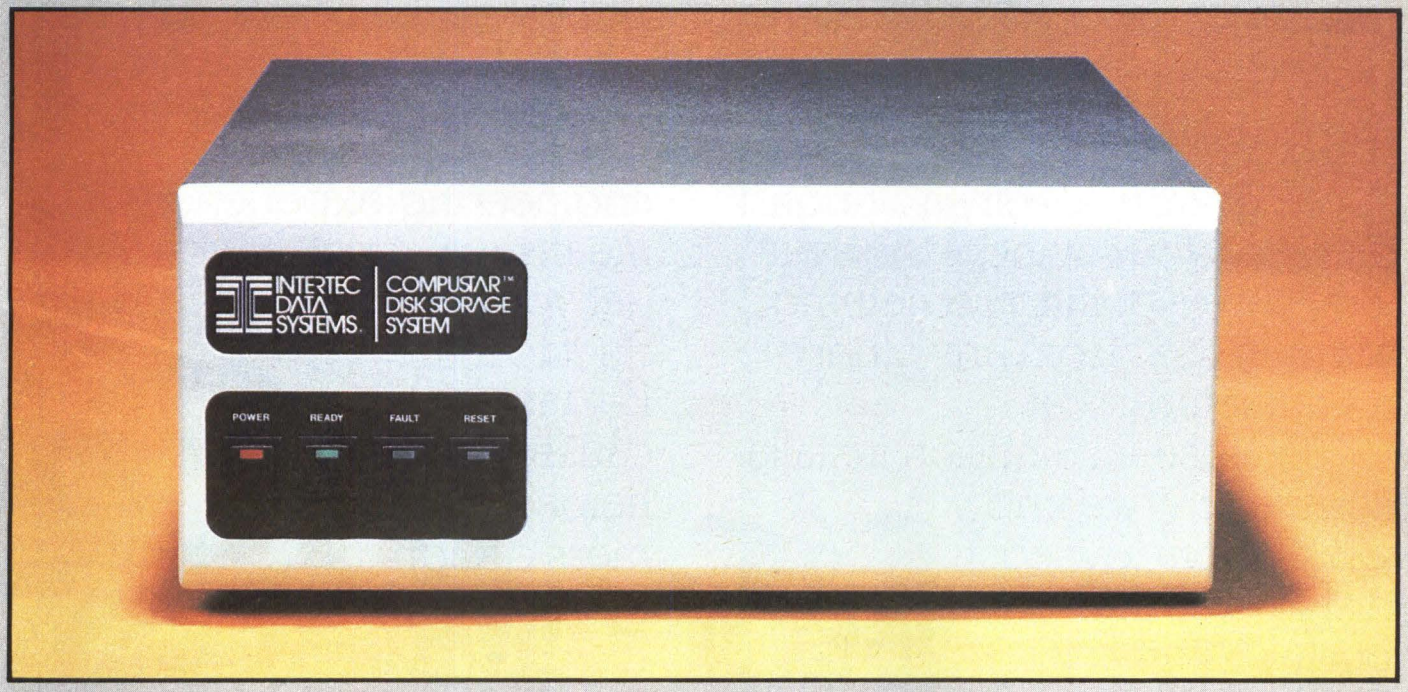
Z80 based System 1010, Stretch 1000, and MP-1000 provide choices in memory, CPU power, and data storage volume. The systems, available from CSSN, Inc, 120 Boylston St, Boston, MA 02116, range from an entry level unit to a 16-user shared storage system. Common to all are 64k RAM, 13M-byte cartridge tape drive, from 10M to 169M bytes of disc storage, and IEEE S-100 bus.

System 1010 provides a 10M-byte hard disc drive for entry level users, and allows Z80 users who run CP/M applications on floppy discs to move up to hard

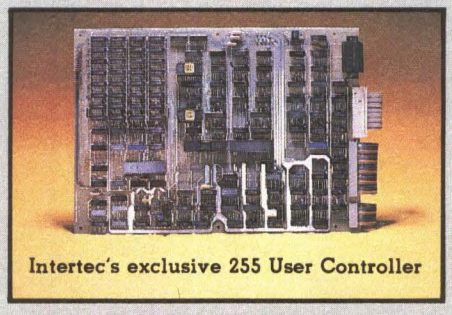
(continued on page 74)

SOLVE THE STORAGE SHORTAGE

with ten multi-user megabytes



CompuStar's 8-inch Winchester



Intertec's exclusive 255 User Controller

CompuStar Cable Assembly

If you could think of just one way to improve our phenomenally popular SuperBrain, what would it be? More disk storage? Well, we already thought about it. And for only a few thousand dollars for a whopping 10 megabytes of lightning-fast storage, it's nothing short of another major breakthrough! From the company that wrote the book on price/performance . . . Intertec.

Our New CompuStar™ 10 Megabyte Disk Storage System (called a DSS) features an 8 inch Winchester drive packaged in an attractive, compact desktop enclosure. Complete with disk, controller and power supply. Just plug it into the Z80 adaptor of your SuperBrain and turn it on.* It's so quiet, you'll hardly know it's there. But, you'll quickly be astounded with its awesome power and amazing speed.

The secret behind our CompuStar DSS is its unique controller/multiplexor. It allows many terminals to "share" the resources of a single disk. So, not only can you use the DSS with your SuperBrain, you can configure multiple user stations using our new series of CompuStar™ terminals, called Video Processing Units or VPU's™.

Four CompuStar VPU's are available. At prices starting at less than $2,500. Some models are designed to operate as stand-alone microcomputers, with internal disk storage. Just like your SuperBrain. Each model features its own 64K of RAM and can be "daisy-chained" into a powerful multi-user network. Just connect one VPU into the next. Using easy-to-install cable assemblies. Connect up to 255 users in a single system. One at a time. As you need them.

Whether you need an extra 10 megabytes for your SuperBrain or an enormous multi-user network, the CompuStar™ DSS solves your storage shortage problems. Sensibly. And economically. Plus, your investment is protected by a nationwide service network with outlets in most major U.S. cities. Providing efficient on-site or depot maintenance.

Get a demonstration of this extraordinary new system today. Call or write now for the name and address of your nearest CompuStar dealer.

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CIRCLE 38 ON INQUIRY CARD

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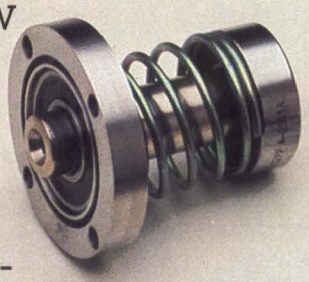
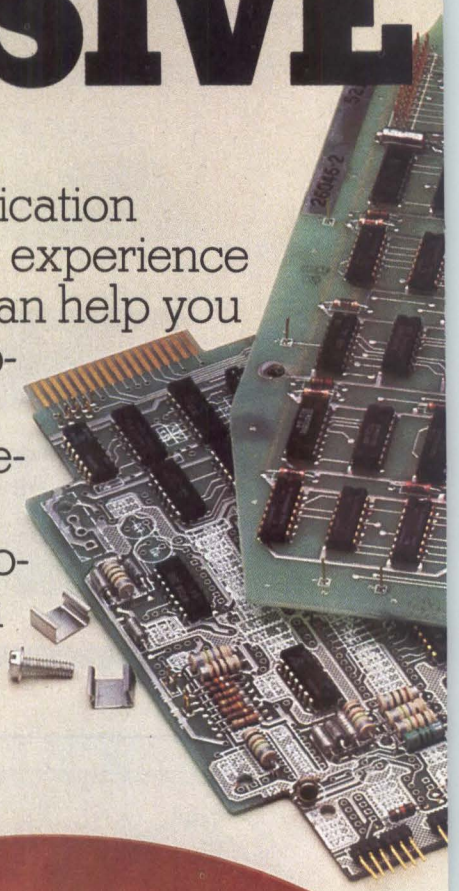
When you specify a Shugart drive for your standalone system, you're getting something you can't get from any other manufacturer.

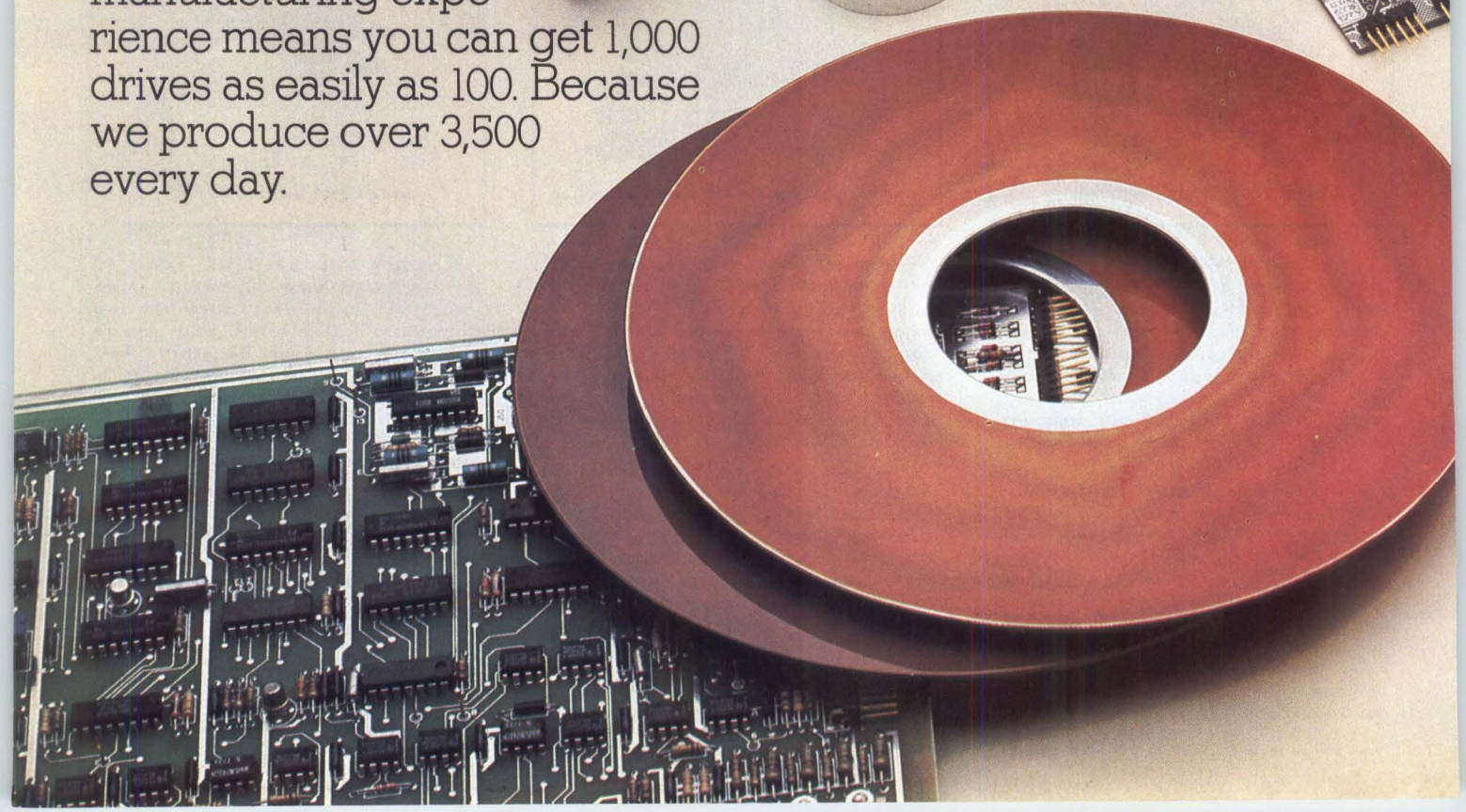
Because—1.8 million installations later—we know more about low-cost disk drives than anybody.

Our high-volume manufacturing experience means you can get 1,000 drives as easily as 100. Because we produce over 3,500 every day.

Our application engineering experience means we can help you get your product to market faster. Because we've helped customers design more







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To the SA850 double-sided floppy with up to 1.6 megabytes of storage. All reliable thanks to its Bi-Compliant™ head design.

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CIRCLE 39 ON INQUIRY CARD

MICROPROCESSORS/ COMPUTERS

disc capacity. For data management applications, Stretch 1000 comes with 128k bytes of RAM, expandable to 1M byte, and true hardware memory mapping. High capacity, multiprocessor MP-1000 provides up to 16 users with independent microprocessors sharing common disc storage. It features user "slave" Z80 computers that access shared devices such as magnetic tape or disc via a "master" CPU.

To ensure data file protection, each system features the company's BackUp integral hardware/software cartridge tape subsystem that allows file by file save and restore functions. Since each file is independently accessible, the subsystem provides greater flexibility than typical bit-stream devices. All three systems use the company's proprietary CP/M compatible hard disc operating system, and are compatible family members with the company's 24M-byte System 1000.

Circle 260 on Inquiry Card

Single-chip μcomputer executes BASIC to ease software development

A single-chip microcomputer, developed by Zilog, 10340 Bubb Rd, Cupertino, CA 95014, the Z8671 contains a BASIC interpreter masked into its 2k bytes of internal ROM. This feature allows programs to be written in a high level language, instead of assembly language, reducing program development time.

The system's BASIC/DEBUG, a subset of Dartmouth BASIC, allows direct access to hardware registers and memory, supplies hexadecimal and decimal I/O, and permits calls to machine language routines. DEBUG, an onchip editor, enables programs to be interactively edited and debugged before they are run. Using BASIC in a realtime environment facilitates the writing of programs without a complete development system.

Ability to access machine language subroutines in external memory from a BASIC program allows the user to circumvent the interpreter for portions of a problem that require faster execution. This procedure provides a method of tailoring program speed to the requirements of a specific problem.

Other features include six levels of vectored interrupts, fast instruction execution, efficient memory use, and I/O and bit manipulation capabilities. A large external memory expansion capability allows for up to 124k bytes of ROM or RAM. The chip also features a full-duplex UART for communication with a program development terminal. Standard baud rates of 110 to 19.2k can be selected at the chip. Packaged in a 40-pin DIP, the device operates from a single 5-V power supply. All pins are TTL compatible.

Circle 261 on Inquiry Card

Array processor transforms LSI-11 into number cruncher

A fully programmable floating point array processor, SKYMNK, processes floating point numbers at rates up to 1 megaflop. The "micro number kruncher," a product of Sky Computers, Inc, PO Box 8008, Lowell, MA 01852, computes vector math, fast Fourier transforms, digital filtering, format conversions, and image processing at speeds 50 to 100 times faster than a standalone microcomputer.

Contained on two quad PCBs that plug into any LSI-11 or -11/23 quad Q-bus backplane, the processor operates under RT-11 or RSX-11M for FORTRAN or Macro programs; it extends the LSI-11 instruction set to include vector, matrix, and compound mathematical instructions computed in real and complex arithmetic. The processor operates internally with standard PDP-11 32-bit single-precision floating point format and 48-bit extended precision operation. It is tightly coupled to the host computer and shares the host's memory (up to 1M byte addressable), keeping memory expansion under user control.

Circle 262 on Inquiry Card

POWER-ONE
D.C. POWER SUPPLIES

Our customers select their favorite models

The choice wasn't easy. Not with 105 open frame linears and a full switcher line to choose from. Still, the top models of the past year — proudly pictured below — have been named.

Actually, this is a statement of Power-One's most popular D.C. power supplies — as determined by our customers. Obviously, applications vary widely, from small floppies and micro-computers to large mainframe systems.

But one thing they all have in common. They're built by Power-One. Which means the most reliable power supplies available, at the lowest cost possible.

So take a look at our entire line. Send for our new 1981 Catalog and Facilities Brochure for details.

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- High Efficiency - 75% min.
- Compact/Light Weight
- 115/230 VAC Input
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- Totally Enclosed Packaging
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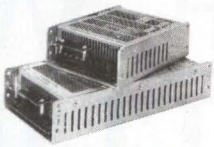
- 24 Hour Burn-in

SINGLE OUTPUT

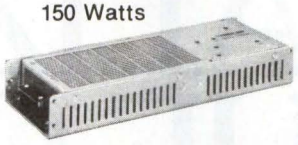


5V to 24V Models

SD, 60W : $115.00
SF, 100W : $170.00
SK, 200W : $250.00

MULTIPLE OUTPUT

150 Watts



5V @ 20A -12V @ 3A
12V @ 5A 5V to 24V @ 3.5A User Selectable

SHQ-150W : $295.00

QUME PRINTER SUPPLY

5V @ 10A
±15V @ 4.5A/16A Peak

SP305 : $345.00

Disk-Drive

- Powers Most Popular Drives
- 7 "Off the Shelf" Models
- Powers Drives & Controller
- UL & CSA Recognized
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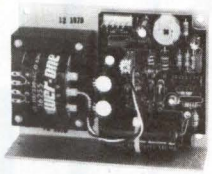
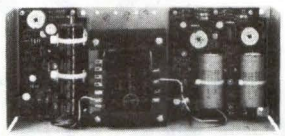
5¼" FLOPPY SUPPLIES



CP340, 1 Drive : $44.95
CP323, Up to 4 Drivers : $74.95

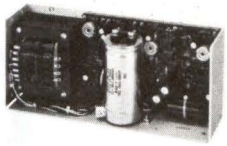
8.0" FLOPPY SUPPLIES



CP205, 1 Drive : $69.95
CP206, 2 Drives : $91.95
CP162, Up to 4 Drives : $120.00

WINCHESTER SUPPLIES

2 Models to Power any Manufacturer's Drive



CP379, CP384 : $120.00

Open-Frame Linear

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- ±.05% Regulation
- Two Year Warrantee
- UL & CSA Recognized
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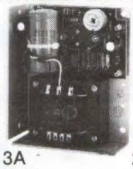
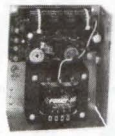
SINGLE OUTPUT



5V @ 3A 24V @ 1.2A
12V @ 1.7A 28V @ 1.0A
15V @ 1.5A 250V @ 0.1A

HB Series : $24.95

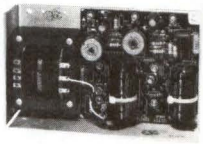
SINGLE OUTPUT



5V @ 6A 24V @ 2.4A
12V @ 3.4A 28V @ 2.0A
15V @ 3.0A 48V @ 1.0A

HC Series : $44.95 to $49.95

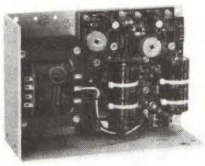
DUAL OUTPUT



±12V @ 1.0A or
±15V @ 0.8A

HAA15-0.8 : $39.95

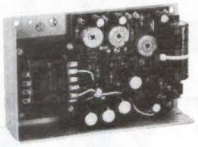
DUAL OUTPUT



±12V @ 1.7A or
±15V @ 1.5A

HBB15-1.5 : $49.95

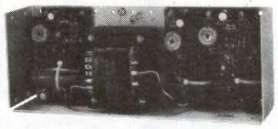
TRIPLE OUTPUT



5V @ 2A
±9V to ±15V @ 0.4A

HTAA-16W : $49.95

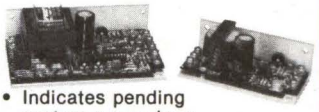
TRIPLE OUTPUT



5V @ 3A
±12V @ 1A or
±15V @ 0.8A

HBAA-40W : $69.95

POWER FAIL MONITORS



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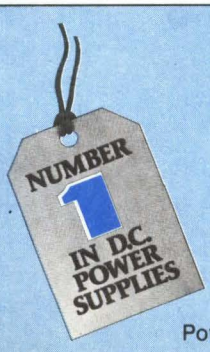
- Monitors AC line and DC outputs.
- Allows for orderly data-save procedures

PFM-1 : $24.95 PFM-2 : $39.95



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We will even include some very impressive four color photography of our 32-bit hardware. Just like you see on all the other pages of this publication.

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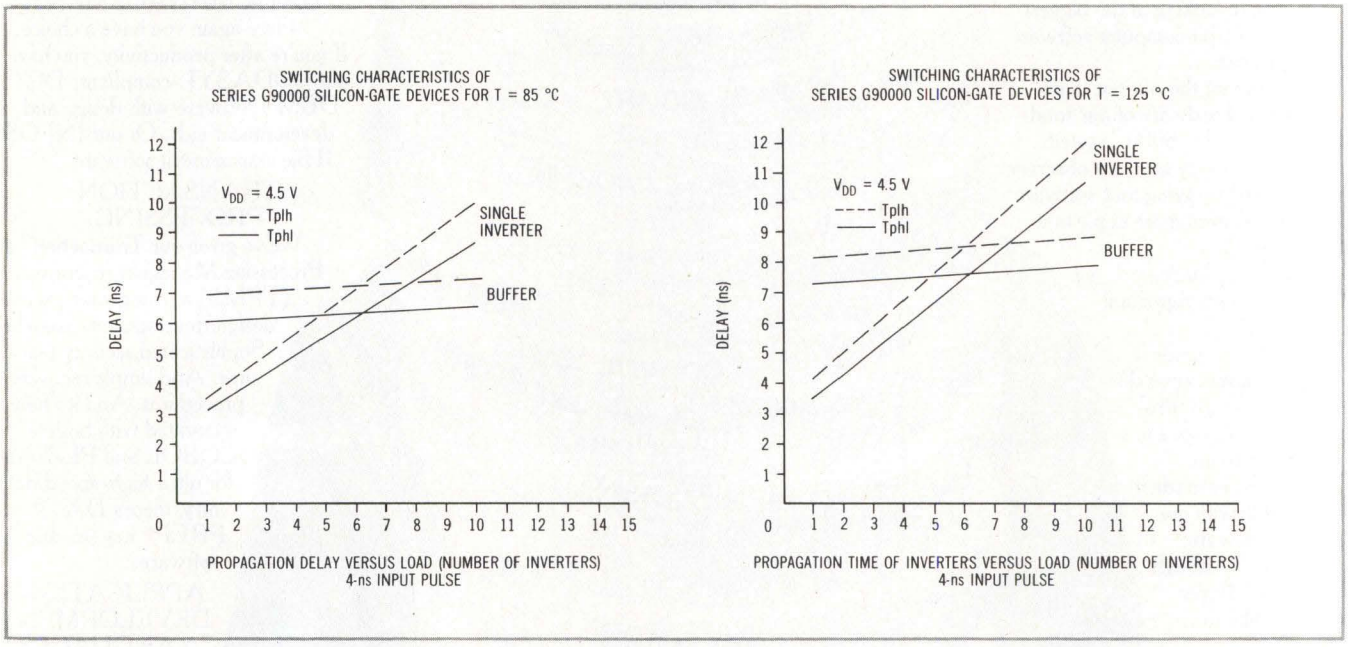
CIRCLE 42 ON INQUIRY CARD

INTEGRATED CIRCUITS

CMOS double-level metal gate arrays provide increased density and connectivity



A new series of double-level metal CMOS gate arrays was recently announced by International Microcircuits, Inc, 3350 Scott Blvd, Santa Clara, CA 95051. Bipolar double-metal arrays have been available for some time. Driven by increased volumes of metal limited logic products, such as microprocessors, CMOS double-metal technology is a relatively recent development. Indeed, IMI claims its G90000 family to be the first double-level metal gate arrays. The new oxide-isolated silicon gate circuits have from 1160 to 5100 cells per chip. Each cell provides the logic power of a 3-input gate.

Double-level metal technology increases both the gate density and the availability of interconnection channels. For example, the die of the 5100-cell chip is smaller than that for the 1960-cell chip introduced by the company two years ago. Most of the density increase is attributable to double-metal technology. Also, because of the increased interconnection options, a higher cell utilization should be obtained with double-level metal. Historically, the company's gate array products have been used to implement an entire system, thus replacing a PC board; to collect the glue chips that support standard logic on a single chip; and, now at the 5000-gate level, to implement LSI and VLSI functions for large system users.

Characteristics and performance

Specifications for the G90000 double-level metal gate array family are shown in the table. Both CMOS and TTL interface logic levels are offered. Inverter delay is rated at less than 3 ns at 5 V, with a fanout of 3 at 70 °C. Delay at 85 and 125 °C, as a function of fanout load, is shown in the graphs. Output drive per buffer is rated at up to 20 LS loads at 5 V and 70 °C. Toggle rates in excess of 40 MHz are available.

Design and fabrication

The company utilizes a CAD system including fully automated routing and placement to translate logic into mask layouts. Surprisingly, the company expects compute time to be reduced by as much as a factor of ten when "wiring" double-level metal chips. The reason is that this new technology provides many more connection options.

Double-level metal implies the design of three masks: one for each metal level and a third via hole mask. The via hole mask defines the holes that connect the

(continued on page 84)

G90000 Double-Level Metal Gate Array Family Characteristics

Part Number	Available Gate Cells	Interface Pads	Output Buffers	Die Size (mils)
G91160	1160	64	60	188 x 189
G91790	1790	64	60	222 x 222
G92240	2240	68	64	253 x 253
G92780	2780	84	80	278 x 273
G93500	3500	106	101	306 x 308
G95100	5100	100	96	294 x 297

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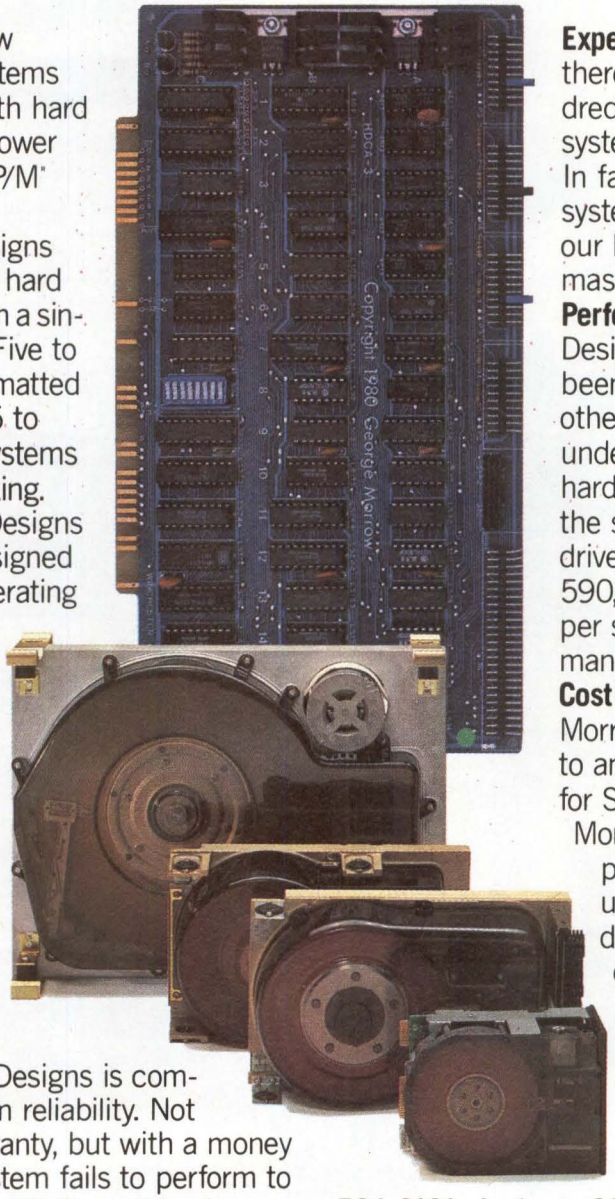

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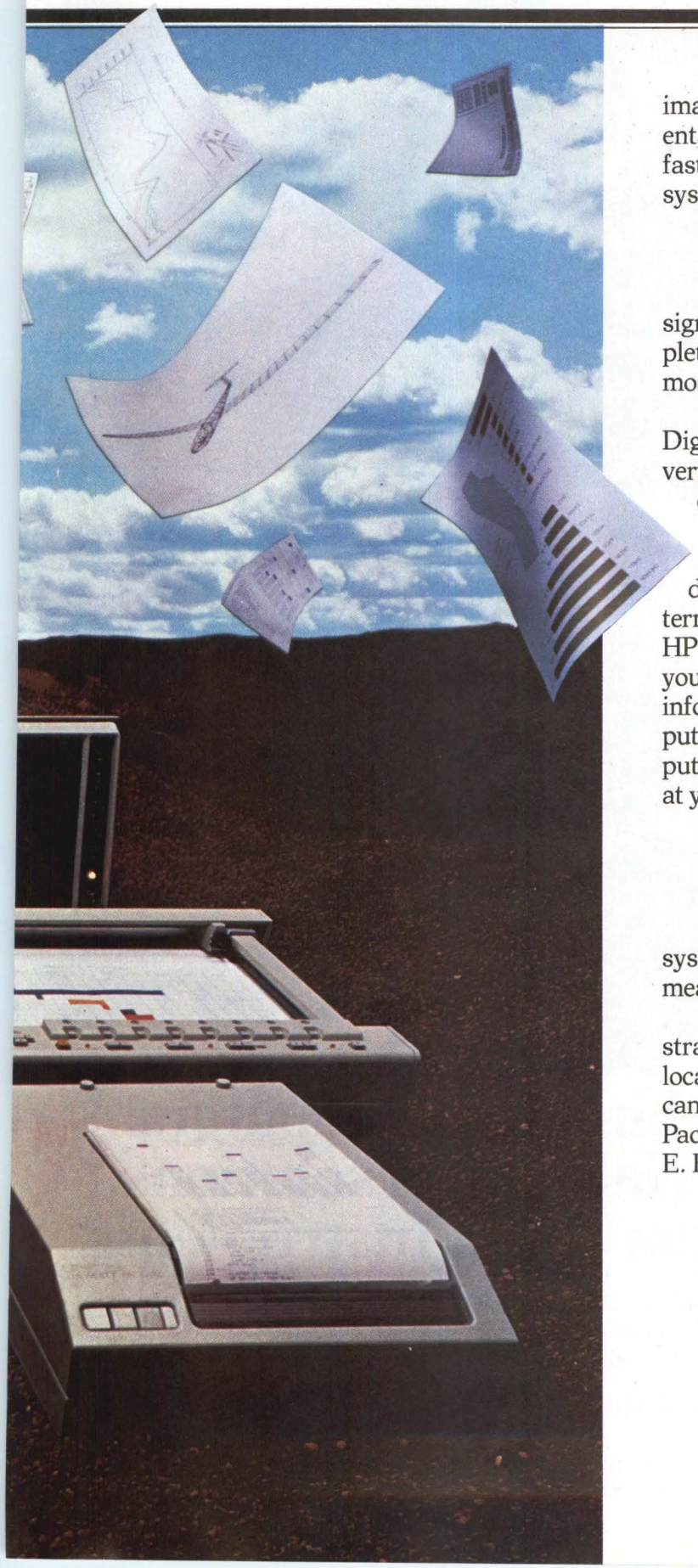

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Solve a majority of your industrial control design problems rapidly. Economically. Efficiently. TI's broad TM990 Series of microcomputer modules can match your needs down the line. And off the shelf. Saving design time and money because they are pre-assembled, pretested. Giving you all the performance of TI's 16-bit 9900 microprocessors.

Super fast CPU

If you need a high-performance general purpose 16-bit CPU, then the new TM990/1481 two-board CPU is your answer. With 95 distinct instructions, it has the processing power of a minicomputer.

While the TM990/1481 is 3½ times faster than other TM990 CPUs when executing non-floating point instructions, it shines at floating point arithmetic. *It is 40 times*

faster. In fact, the TM990/1481 performs double precision floating point in the same time as it takes competitive products to perform single precision.

Memories: Broader range

Your choice in TM990 memories includes a variety of directly addressable semiconductor memory modules.

There's also provision to handle floppy disks drives. The TM990/303A controls up to four standard drives or three mini diskette drives.

Exceptional I/O capability

Interfacing with the outside world is relatively easy. The TM990 Series contains a comprehensive selection of I/O modules: Digital. Analog. Industrial AC and DC. And, *a readily available speech module*, the TM990/306. It can speak 179 words and is ideal for situations where the spoken word is the most effective means of communication.

Recently added to the TM990 line are two new communication modules. The TM990/308 Industrial Communication Module permits communication with as many as 31 other compatible TM990 systems. Over distances up to 10,000 feet, using twisted-pair lines. The optically isolated interfacing built into the 308 simplifies interconnects and lowers installation costs even in electrically noisy environments.

The TM990/307 allows communication with up to four RS232 devices such as terminals or modems.

Functional integration: Slashes your software costs

Functional integration. Hardware and software units developed together. To work together. TI is first with this system concept of the 80's that can substantially cut software development time and costs.

Key element is a set of software interconnect standards that ties the system together.

The Realtime Executive implementation allows you to interface

Broad and growing series: TI's TM990

Microcomputer Modules:
TM990/100MA
TM990/101M
TM990/180M
TM990/1481

Memory Module:
TM990/201 EPROM/RAM
TM990/203 Dynamic RAM
TM990/206 Static RAM

Mass Storage Module:
TM990/303A Floppy Disk Controller

Digital I/O Modules:
TM990/305
TM990/310

Analog I/O Modules:
TM990/1240
TM990/1241
TM990/1243

Communication Modules:
TM990/307
TM990/308

Speech Module:
TM990/306

Card Cages & Enclosures:
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TM990/520
TM990/522
TM990/530

Industrial AC and DC I/O Modules:
TM990/5MT Series

Data Entry and Display Microterminal:
TM990/301

University Module:
TM990/189M

Software Development Module:
TM990/302

TI's Component Software with the system easily and quickly. These Component Software packages provide a library of statements common to many programs. You choose what you need and combine it with the specific software required by your application. Savings can be more than two-thirds the cost of writing a typical program.

Available now: the File Manager. Coming soon: Software Data Communication packages.

The File Manager package performs such functions as library level management of diskette storage. Including install formatted volume, open/close/read/write files, random access to files.

TI's powerful AMPL hardware and software development system includes full speed emulation of 9900 microprocessors, and provides for program development in assembly language, TI Microprocessor Pascal (complete with concurrency), and Power Basic.

Complete accessories

The TM990 Series is supported by a broad selection of accessories — card cages, connectors, cables, and power supplies. Just added: the TM990/522 Enclosure containing a four-slot OEM chassis, power supply, and cooling fan in a neat, attractive, table-top unit.

For faster, simpler solutions to industrial control problems, take the shortcut. The TM990 Series of microcomputers. For more details about these time and money saving modules, see your local TI distributor, or fill out and return the coupon.

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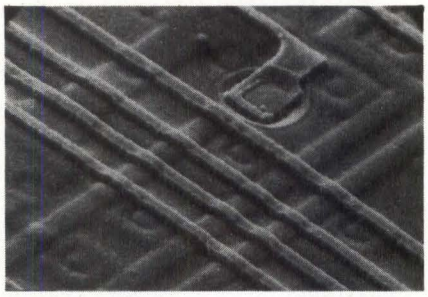
CIRCLE 45 ON INQUIRY CARD

INTEGRATED CIRCUITS



two metal levels. The firm recently began the operation of a 4″ (10-cm) wafer fabrication facility totally dedicated to CMOS gate arrays including double-metal devices. The photograph shows two metal layers with overlapping interconnections and a via hole connecting the two layers. Double-level metal fabrication requires the gentle sloping connection edges and tapered via hole radii shown in the photo. Although simple, the technology is proprietary to the company. Process yields are claimed to be high. Inspection and testing are provided from design through fabrication and packaging.

—Douglas Eidsmore, Senior Editor

Circle 263 on Inquiry Card

ECL gate arrays offer 500-ps gate delays

A family of high performance emitter-coupled logic (ECL) gate arrays, designated SCD 1000, 2000 and 3000, were recently announced by Plessey Research (Caswell) Ltd, Caswell, Towcester, Northants NN12 8EQ, England. The first three members of a new gate array family, the devices were developed utilizing the high performance Plessey process III(V), and offer local gate delays of 500 ps and flipflop clock rates in excess of 300 MHz.

SCD 1000 is based on a single-level ECL gate. Up to 100 gate functions may be realized using this circuit. Inputs and outputs to the array are through 28 pin connections. Each connection includes a buffer transistor capable of driving a 50-Ω line at ECL 10k logic levels. Power dissipation is less than 1 W. The array can be customized on two layers of metallization.

SCD 2000 and 3000 are larger versions. Both offer up to 300 gates and 64 pin connections. SCD 2000 offers the same performance as SCD 1000 with a power dissipation of over 3 W for some variants. The SCD 3000 offers gate delays of about 2 ns and a maximum power dissipation of 750 mW.

Typical applications for the three circuits are seen as replacements of ECL 10k and ECL 100k standard SSI and MSI parts. Packaging is in either DIPs or chip carriers (leaded or unleaded) from 16 to 40 leads. Leaded chip carriers are normally used for 64-pin applications. The company has developed software to assist in mask design.

Circuits containing 600 and 1200 gates are being developed. These will be followed by a complete family of arrays based on a reduced geometry version of the process. Largely by virtue of the reduced interconnection capacitance experienced by the new process, this family will offer improved circuit performance.

Circle 264 on Inquiry Card

Programmable array logic circuits implemented in 24-pin, 300-mil packages

PAL® series 24 is a family of user programmable devices for the replacement of conventional 54/74 series SSI/MSI TTL components with a 6:1 reduction in chip count. Developed by Monolithic Memories, Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, the 24 series complements the PAL series 20 by providing two more inputs and two more outputs, allowing more complex functions to be implemented in compact 24-pin 300-mil (0.076-mm) SKINNYDIP™ packages. The new circuits have the equivalent of 200 gates.

Four types are available in the 24 series. PAL20L10 is a 20-input, general purpose combinatorial building block for random logic replacement. PAL20X10 is a 20-input AND/OR/XOR gate array with 10 registered outputs. It can be used as a 10-bit counting chain for the vertical/horizontal timing control of a CRT and similar bit counting functions. PAL20X8 is also a 20-input AND/OR/XOR gate array, but has eight registered outputs. This device could be used as a programmable octal interface, octal parallel counter, or octal shift register. It could also be used as a program counter to perform jump and increment functions for a microprogrammed sequencer. PAL20X4, a 20-input registered AND/OR/XOR gate array with four registered outputs, could be used as one-half of a 64k dynamic RAM controller to perform refresh and lower/upper byte multiplexing.

Circle 265 on Inquiry Card

DATAGRAPHIX 132-COLUMN DISPLAYS GIVE YOU NOT ONLY BETTER QUALITY, BUT LETTER QUALITY.

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CIRCLE 47 ON INQUIRY CARD

INTEGRATED CIRCUITS

Single chip converts RAM to FIFO buffer memory

A new single-chip, FIFO (first in, first out) RAM controller has been designed to change standard RAMs into FIFO buffer memories. Claimed by the manufacturer, Signetics, 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086, to be the first of its kind, 8X60 is an address and status generator that will implement a high speed/high capacity FIFO stack using standard RAMs. Present FIFOs are size limited. By controlling RAM to handle data as FIFO, large standard RAMs can be used as FIFO data buffers. The number of RAMs controlled by the part is theoretically unlimited. However, power and space limits constrain the maximum number.

Controller capabilities and characteristics

Specifically designed for applications with high speed bipolar RAMs, the FIFO RAM controller (FRC) can be adapted for use with MOS RAMs. The FRC is seen as the interface between independently clocked systems, such as buffer disc or tape memories, data communications concentrators, CPUs to terminals or printers, and DMA applications.

The device is capable of controlling up to 4096 buffer memory words. Word width is defined by the user. FIFO depth can be 64, 256, 1024, or 4096. Depth is selected via two length select signals.

All inputs and outputs are standard TTL. Address outputs have a 16-mA drive capability. Buffer transfer rates exceed 8 MHz. To support high speed operation, the 8X60 has a "fallthrough" time of zero. Standard FIFOs require time for fallthrough in addition to access time, and cannot be re-accessed during fallthrough.

8X60 is manufactured using the company's Integrated Schottky Logic (ISL) process. It operates from a single power supply and requires only one additional, external dropping resistor providing a current supply to internal ISL logic. The FRC is available in a 28-pin plastic DIP and is specified over 0 to 70 °C.

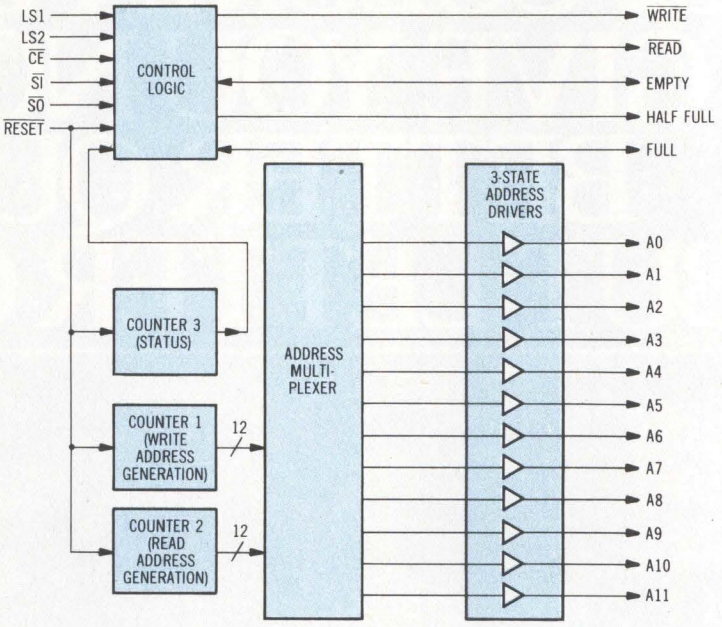
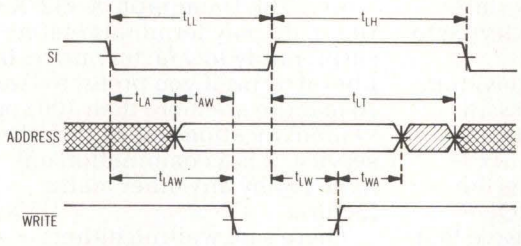


Fig 1 Functional block diagram of FIFO RAM controller. Complete FIFO buffer is shown. Additional interface, eg, standard data latches and timing controls, may be required



t_{LA} — ADDRESS STABLE DELAY
t_{AW} — ADDRESS LEAD TIME
t_{LT} — ADDRESS OUTPUT DISABLE
t_{LW} — WRITE OUTPUT INACTIVE DELAY
t_{WA} — ADDRESS TIME LAG
t_{LAW} — WRITE OUTPUT ACTIVE DELAY

Fig 2 FRC write cycle timing. t_{LL} and t_{LH} are SI (shift in request for write cycle) low and high, respectively. Write and read cycles are symmetrical

Functional operation

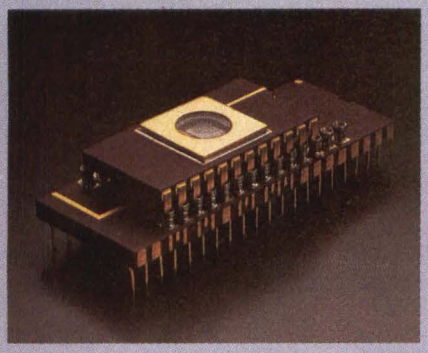
The device is shown in the block diagram in Fig 1. Counters 1 and 2 are 12-bit, write and read (respectively) address generation counters. The outputs are multiplexed to the twelve 3-state address drivers. Three-state address outputs enable the FIFO memory space to be part of the RAM memory. Counter 3 is a 12-bit, up and down status counter. It generates full, empty and half-full status signals.

Read/write operations are dealt with first-come, first-served. Operationally, the device writes into or reads from the FIFO buffer memory. To write, SO (shift out request for read cycle) must be high and SI (shift in request for write cycle) must be low. The write cycle timing is shown in Fig 2. When the foregoing

(continued on page 92)

The first user-programmable, 8-bit micro that runs hot and cold: MK38P70.

UNITED TECHNOLOGIES MOSTEK



What it means is simply this: now you can also use the MK38P70 as your final production device for low volume, extended temperature applications. If you do, you'll be making an excellent choice.

First, the P-PROM MK38P70 is more cost-efficient than a mask-ROM microcomputer in low volume quantities.

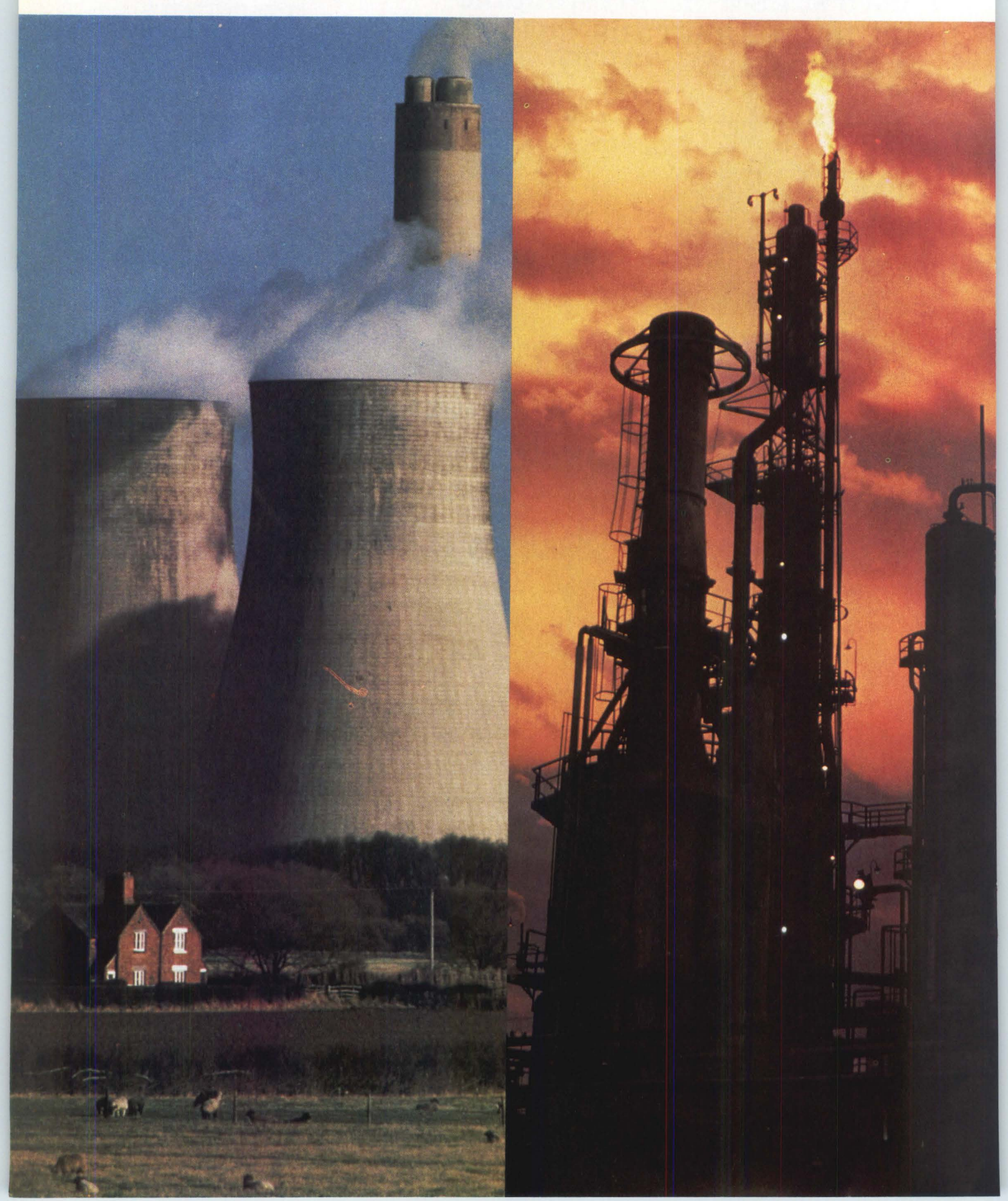
Second, it's also more versatile. With the MK38P70, you can program the piggyback EPROM and change it if necessary (as often as you like) on any standard EPROM programmer. Once completed, you're ready for production because the MK38P70 will meet final system specifications.

And, if the application subsequently becomes higher volume, you can still use the MK38P70 to emulate a total of 8 mask-ROM equivalents.

A −40°C to +85°C operating range. Add that to unparalleled emulation capability and it's easy to understand why the MK38P70 continues to be the hottest, user-programmable microcomputer you can get. Call your nearest Mostek distributor to find out more. Or contact Mostek, 1215 West Crosby Road, Carrollton, Texas 75006 (214) 323-1801. In Europe, contact Mostek International at (32)2.762.18.80. In the Far East, Mostek Japan KK (03)-404-7261.

CIRCLE 48 ON INQUIRY CARD

VRC: Memory Products for



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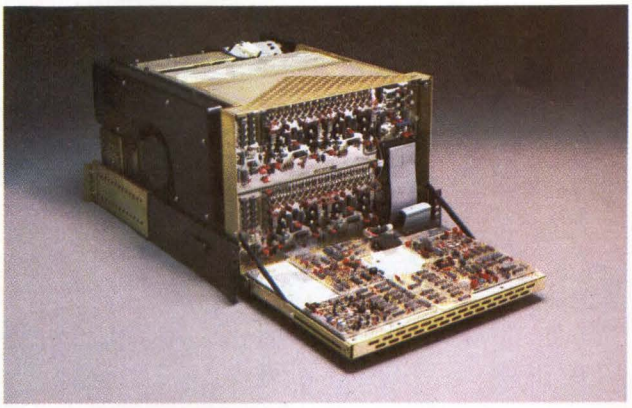
From Alaska to Australia, from an arctic climate to a tropical environment, from petrochemical site to power generating plants, from telecommunication networks to life safety systems, in more than 30 countries worldwide, Vermont Research provides the building blocks of memory systems. The VRC® 4016 Drum Memory is as reliable on the North Slope as it is in the protected environment of a hospital. For telecommunications, data entry, news editing and typesetting, petrochemical and textile processing, VRC memory devices provide a measure of performance our customers build reputations on.

WE FIT IN PRACTICALLY ANYWHERE

With our plug-compatible interfaces, the VRC 4016 can provide rapid access, mass storage capacity and reliability for any host computer at a low per-bit cost. Its compact, rugged design provides up to 37.9 million bits of non-volatile storage capacity with an access time of 8.5 milli-seconds, yet requires only a 12¼" x 17½" x 22" compartment space. Data reliability is enhanced by uniform bit density and constant media thickness over a single recording surface. Demonstrated MTBF is over 28,000 hours.

The design life of the VRC 4016 is ten years. Add the storage economy of .035 cents-per-bit, Mean-Time-To-Repair of less than one hour, and you have a cost-effective, reliable mass storage system. One that offers more than any solid-state or disc device of equal storage capacity.



VRC 4016 *37.9 million bits of storage*

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INTEGRATED CIRCUITS

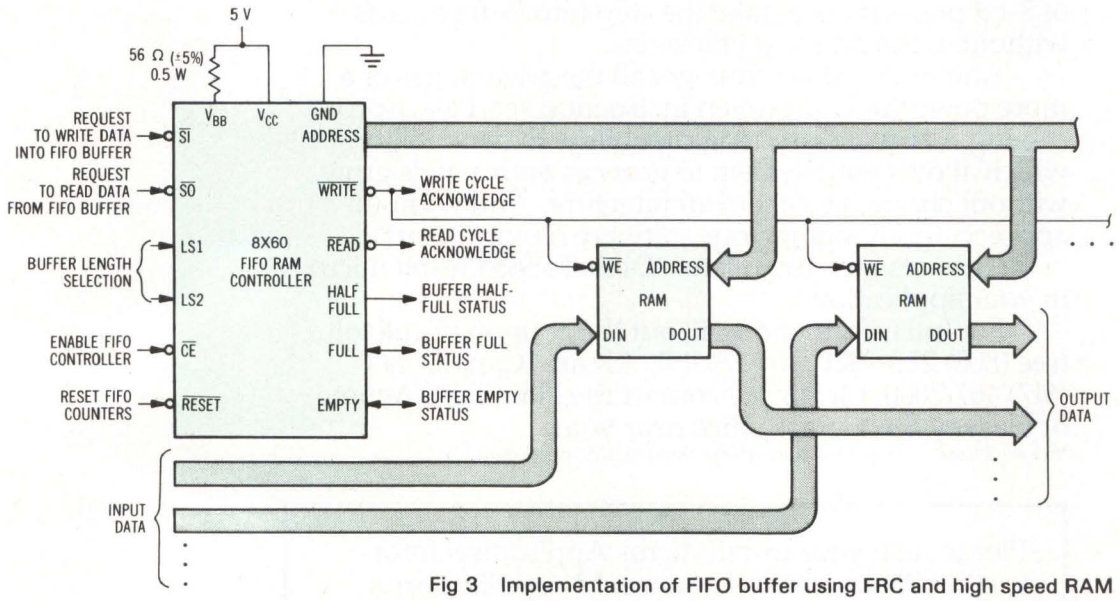


Fig 3 Implementation of FIFO buffer using FRC and high speed RAM

conditions exist, along with other control parameters, the write address in counter 1 is output to the address bus via the multiplexer, and the $\overline{\text{WRITE}}$ output goes low. When the write cycle is over, for example, $\overline{\text{SI}}$ is forced high, the $\overline{\text{WRITE}}$ output goes high, and the address output buffers return to a high impedance state. Counters 1 and 3 are both incremented and Counter 2 is unchanged. Write and read cycles are symmetrical. To read, $\overline{\text{SI}}$ must be high and $\overline{\text{SO}}$ low.

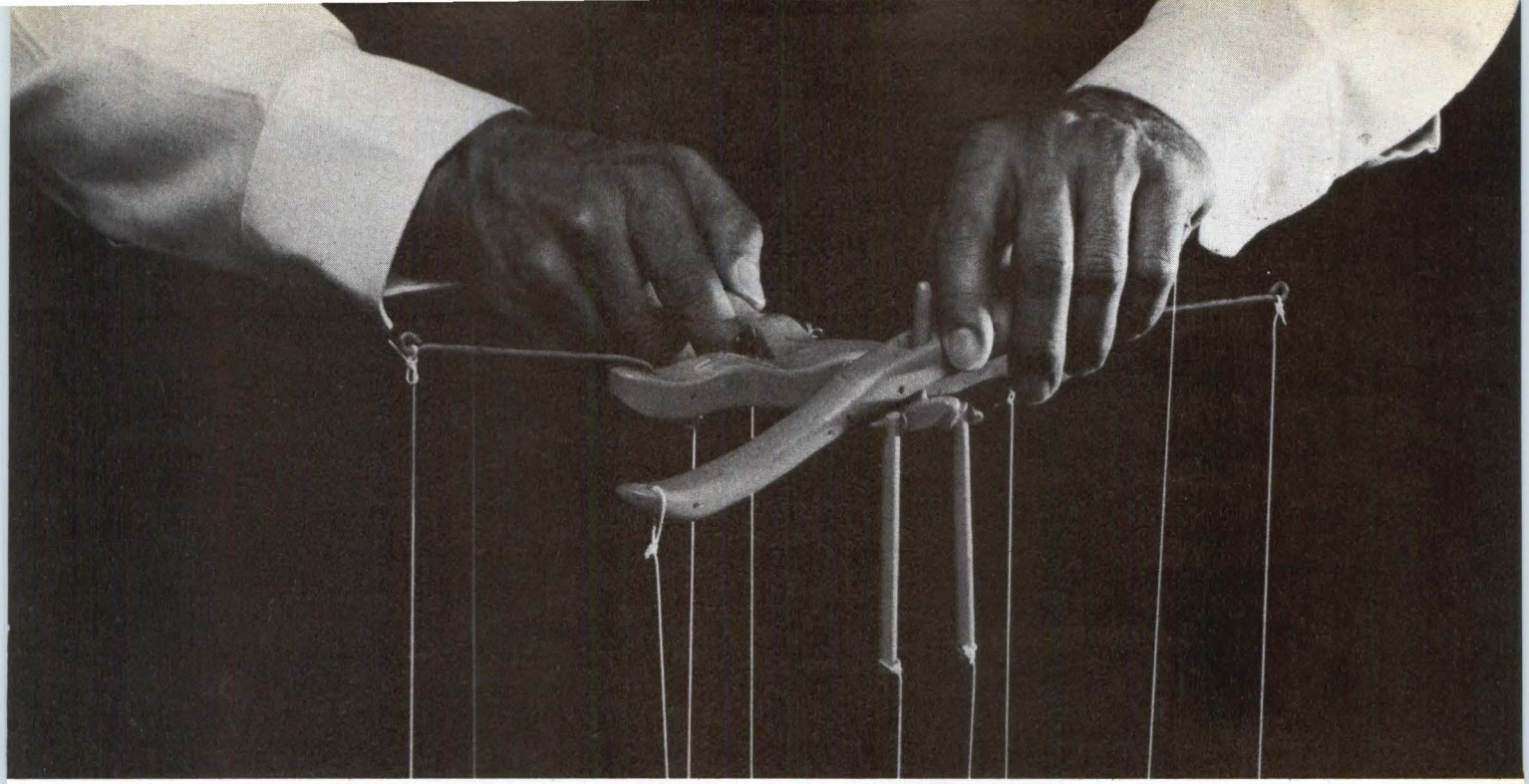
Arbitration logic is onchip. The control logic is designed to prevent read/write contention problems. If one cycle is requested while the other is in progress, the requested cycle will begin as soon as the other is completed. This first come, first served procedure assumes that other control parameters are met.

FIFO memory buffer length is selected by the LS1 and LS2 inputs. When less than the maximum length is selected, the unused high order bits of the address outputs are held in the high impedance state.

A functional diagram of the device, implemented as a FIFO buffer, is shown in Fig 3. RAMs that set up address slower than 5 ns will need delays to extend address hold time after the rising edge of $\overline{\text{WE}}$, and to extend address setup time before the falling edge of $\overline{\text{WE}}$.

—Douglas Eidsmore, Senior Editor

Circle 266 on Inquiry Card



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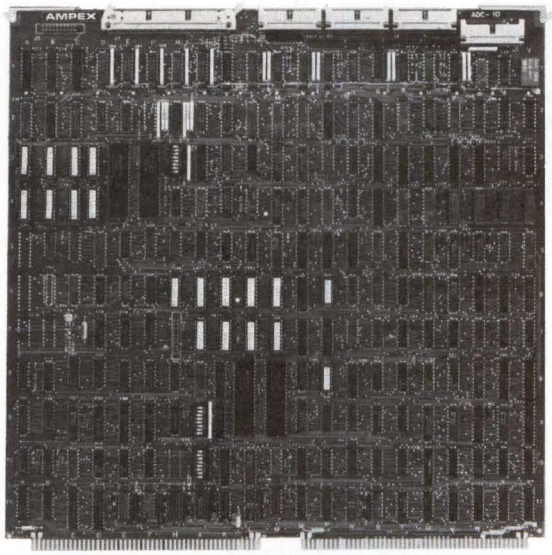

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Result: greater flexibility, lower costs, more control. That's because our new Constellation Series DEC and DG controllers are part of the Ampex "Subsystem" concept. It provides single-source buying for controllers, disk and tape units, so you're assured full compatibility and efficient performance.

DG EMULATION. The ADC-10 and ADC-20 are designed for Data General Nova* and Eclipse* systems. The ADC-10 attaches SMD or CMD disk drives with full emulation. The ADC-20 supports both streaming and start/stop tape drives, as well as attaching SMD disk drives. Dual microprocessor design provides high performance control of all interfaces.

DEC EMULATION. The ADC-11 and ADC-21 are both single-board DEC PDP-11 controllers with the ADC-11 attaching SMD drives with full emulation. The ADC-21 supports both streaming and start/stop tape drives, and also attaches SMD disk drives. Specify our Constellation Series. Control your costs as well as your design.

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CIRCLE 52 ON INQUIRY CARD

INTEGRATED CIRCUITS

CMOS display decoder/drivers handle triplexed LCDs

Designed to drive triplexed LCDs, the ICM7231/7234 IC family includes input buffer and digit address decoding circuitry and contains a mask-programmed ROM for storing input data. Four versions are available from Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014. ICM7231 will drive 8 numeric 7-segment digits and 16 independent addressable annunciators, with address and data input in parallel format. ICM7332 will drive 10 numeric 7-segment digits and 20 independent addressable annunciators, with address and data input in serial format. ICM7233 will drive four 18-segment alphanumeric characters with address and data in parallel format, and ICM7234 will drive five 18-segment alphanumeric characters with address and data in serial.

The CMOS driver family generates the voltage levels and switching waveforms required to drive triplexed LCD, without other components. A complete 6-bit ASCII-to-64-combination character generator is onchip. The new family will interface directly with high performance microprocessors. Input levels are TTL compatible, and the data accepted output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an onchip resistor string, and the output of a totally self-contained onchip oscillator is used to generate all display timing. All devices in this family have been fabricated using MAXCMOS® processing and all inputs are protected against static discharge. Devices are packaged in a 40-pin plastic DIP. Typical power consumption is 40 μA at 5 V (500 μW maximum).

Circle 267 on Inquiry Card

High performance op amps cut power requirements

Claimed to be the first full-performance, low power BI-FET II op amps, LF441-single, LF442-dual, and LF444-quad feature a typical power consumption of 150 μA per amplifier and high impedance JFET inputs of $10^{12}\ \Omega$, typical. Manufactured by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, the series is implemented in the company's BI-FET technology, a process that combines bipolar and field effect transistors onchip. This technology offers the low input bias and offset characteristics of FETs and the high performance of bipolar transistors.

Intended for low power applications that require superior dc and ac characteristics, such as battery-powered installations, the new op amps require one-fourth to one-tenth the supply current of standard parts. Since they are pin compatible with standard op amps, substitutions can provide a reduction in power consumption.

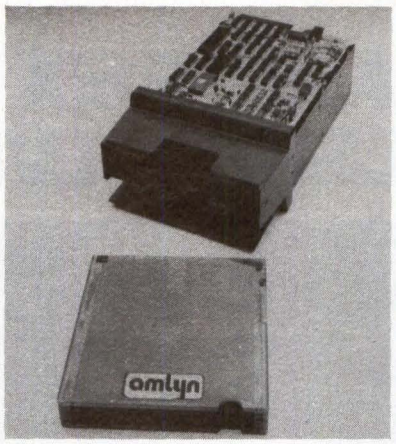
All three devices offer an input noise voltage of 40 nV/$\sqrt{\text{Hz}}$, and a low input noise current of 0.91 pA/$\sqrt{\text{Hz}}$. Matched high voltage JFET input devices reduce the input bias currents to 50 pA maximum, and reduce the offset currents by a factor of 10^4 over standard op amps. LF441 and LF442 feature low input offset voltages of 0.5 mV maximum and 1 mV maximum, respectively, as well as maximum input offset voltage drifts of 10 μV/°C. LF441 and LF442 are available in 8-pin plastic DIPs and TO-5 metal cans. LF444 is available in a 14-pin plastic DIP.

PERIPHERALS

5.25″ floppy drives store 8M bytes using 5-diskette cartridge

MiniPac 5.25″ floppy disc drives use a 5-diskette cartridge to supply up to 8M bytes of storage in online or Winchester backup applications. Diskette recording is single-sided at 9500 bits/in (3740/cm) using 170 tracks/in (67/cm) and is compatible with IBM and Winchester formats. Model 5850 is functionally compatible with controllers interfacing to Shugart SA850, and A506 is physically compatible with controllers interfacing to the Seagate ST506.

To make the device, Amlyn Corp, 1758-H Junction Ave, San Jose, CA 95112, designed a proprietary diskette cartridge holding five spin coated, high resolution diskettes. An articulating selector device removes the addressed diskette and loads it on the drive spindle. Users can change the entire 5.25″ x 5.5″ x 1″ (13.34- x 13.9- x 2.5-cm) cartridge or individual diskettes within it. Mechanical selection and insertion of diskettes is not only faster than a manual operation but supplies more precise registration of media when placed on the spindle, reducing the possibility of damage to the diskette.



Amlyn's MiniPac uses a proprietary cartridge containing up to five high resolution 5.25″ diskettes to store 8M bytes. Selection and insertion of diskettes is performed automatically by an articulating selector mechanism within the drive

Containing an Intel 8051 microprocessor and support chips including 256 bytes of RAM and 4k bytes of P/ROM for microcode control instructions, the drive control card handles realtime control functions. One benefit derived from microprocessor control is that minidiskettes recorded at standard 48-, 96-, or 100-track/in (19, 38, or 39/cm) densities can be read by the drives. This permits existing programs and data recorded on standard diskettes to be used with the drive; software permits the unit to determine which density it is reading, allowing the diskettes to be mixed in the cartridge.

In addition, the processor supplies control to compensate for diskette dimensional changes due to environment

(continued on page 100)

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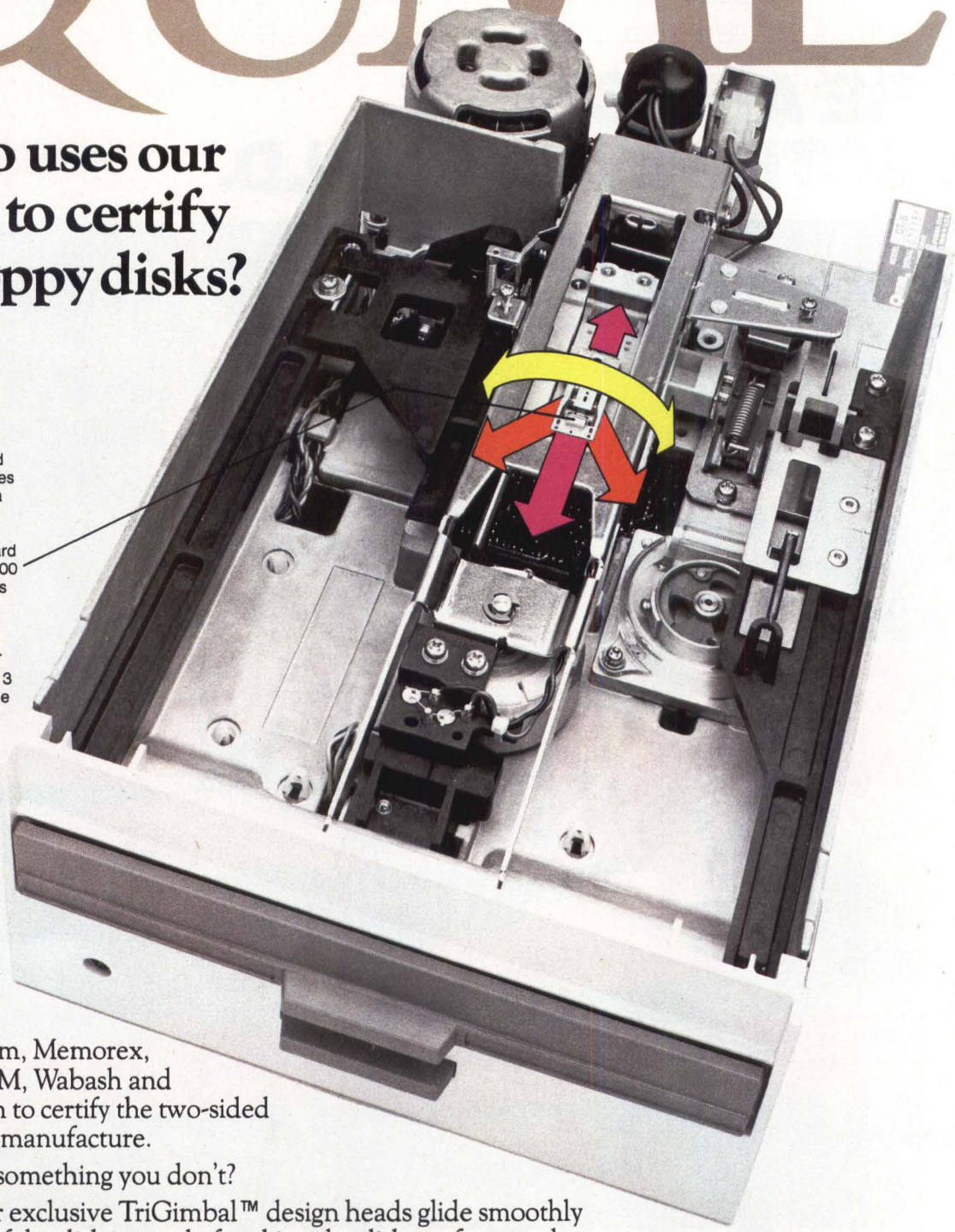
CIRCLE 54 ON INQUIRY CARD

QUME

Who uses our drives to certify their floppy disks?



ROLL, PITCH, and YAW: Exclusive TriGimbal™ head design rotates on three axes for a floating ride on media surface.

TAP TEST: Industry standard is a modest 25,000 to 30,000 impacts. QUME standard is an awesome 100,000 to 150,000 impacts.

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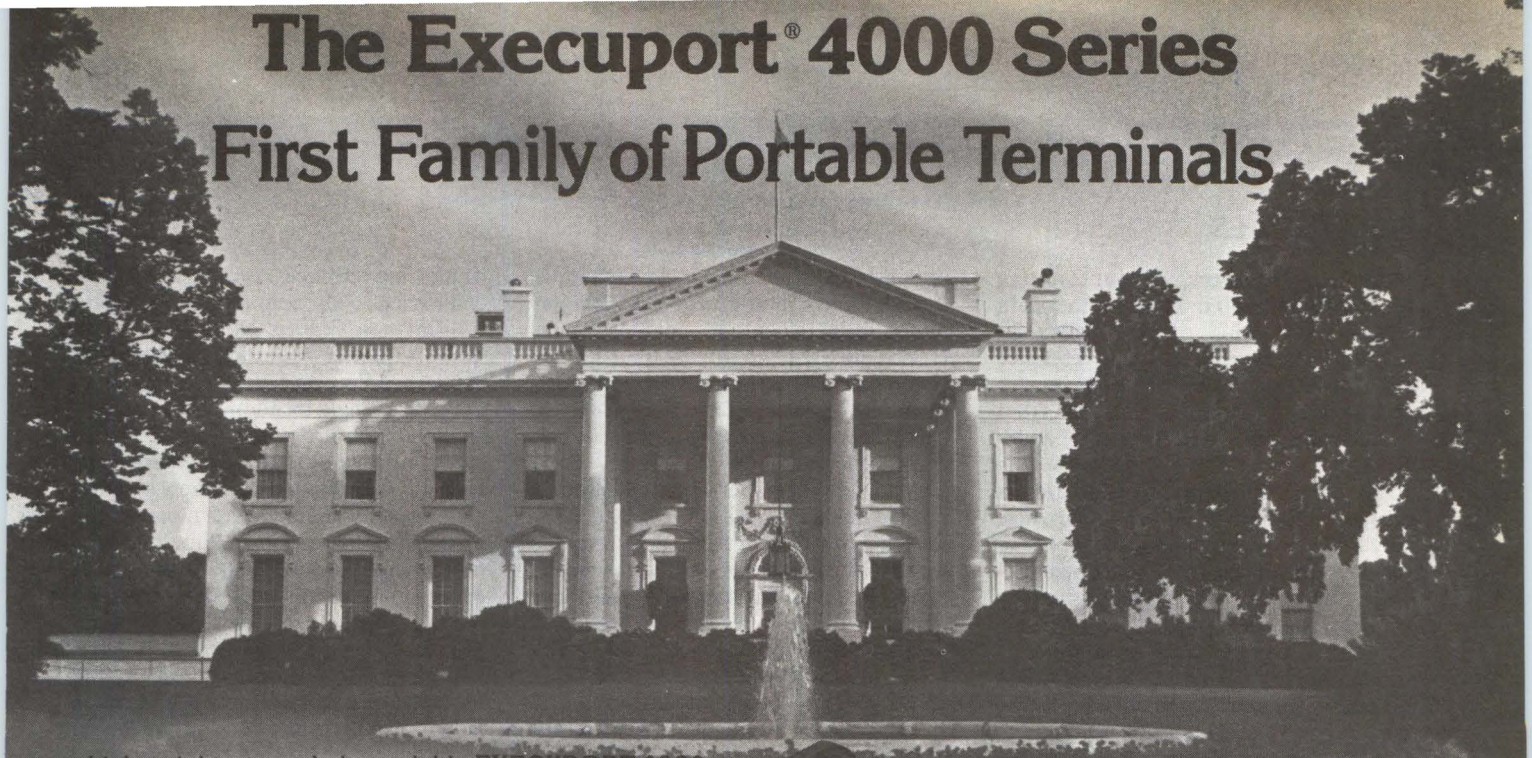
CIRCLE 191 ON INQUIRY CARD

The Execuport® 4000 Series
First Family of Portable Terminals



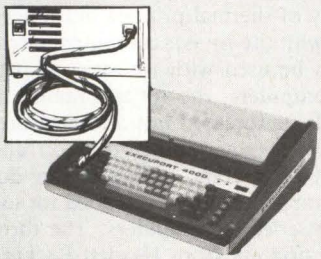
Lightweight, rugged, dependable **EXECUPORT 4000** portables perform like heavyweights.

The EXECUPORT 4000 Series has the special features you want at no extra cost: printhead position indicator, horizontal tabbing, embedded numeric pad, true upper and lower case, built-in self test, data logger with 128 printing characters, bi-directional ¼ line stepping and a choice of keyboards.

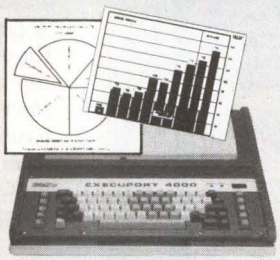
The **EXECUPORT 4000** is a wide carriage portable and desk top terminal, which will accept either 136 or 80 column paper.

The **EXECUPORT 4080** incorporates all of the standard 4000 Series features in a low cost, 80 column terminal.

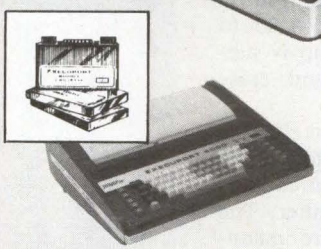
The **EXECUPORT 4741** emulates the IBM 2741 with EBCD code.



EXECUPORT 4000 D/4080 D terminals are equipped with an FCC-approved modular phone jack for direct, hardwire connection into telephone company networks. Telephone numbers can be dialed directly through the terminal keyboard.



EXECUPORT 4000 G generates business graphics when used in combination with ISSCO DISSPLA® and TELL-A-GRAF® or with PICTURE-PAC® by Service Bureau Corporation. The terminal can be ordered with a choice of keyboards.



EXECUPORT 4000 B is a multi microprocessor-based terminal designed for data entry, manipulation and storage. The terminal has 11.5K bytes of integral, non-volatile bubble memory. Removable 11.5K byte bubble memory cassettes increase the mass data storage capability to 23K bytes.

EXECUPORT-SHERLOCK™ automatically transforms data communications into virtually unbreakable code. Equipped with SHERLOCK encryption by Analytics, Inc., the terminal eliminates the need for secret encoding keys, ID codes or passwords. Complete end-to-end SHERLOCK systems are available.

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Manufacturers of Execuport® Terminals

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CIRCLE 55 ON INQUIRY CARD

PERIPHERALS

or misclamping errors, without resorting to embedding servo data in the data tracks. Positioning of the read/write heads is referenced to a single reference track on each diskette. The drive locates this track and references all tracks from it, eliminating the need for track 0 alignment.

The articulator mechanism uses a stepper motor to position the cartridge tray to the proper angle for the picker to remove or replace the addressed diskette. Articulation is accomplished by stepping the drive motor a predetermined number of steps from the cartridge home position. The diskette picker is similarly controlled. Home positions are sensed when a vane on the cartridge or the picker arm passes between the elements of a photointerrupter switch mounted on the base of the drive.

The picker selects the appropriate diskette from the articulated cartridge, moves it and centers it over the spindle, and clamps it to the spindle. Reversing the process returns the diskette to the cartridge. The spindle drive motor rotates the spindle via a belt drive system. Normal operating speed is 360 r/min; provision for 600 r/min, however, allows discs recorded at 48 and 96 tracks/in (19 and 38/cm) to be rotated at speeds that produce read data at F and 2F rates required by the drives.

Read/write heads are another proprietary design. This single-element design uses hot pressed manganese/zinc/ferrite composition to achieve 9500 bits/in (3740/cm) recording density. Each head is 0.004″ (0.10 mm) wide with a 0.001″ (0.025-mm) erase element on either side and 0.002″ (0.050-mm) intertrack spacing for data erasure. A 30- to 35-μin (0.762 to 0.889 μm) gap is supplied for both read/write and erase heads.

In direct contact with the diskette, the head surface is designed to allow maximum signal transfer to and from the surface with minimal wear to either. The Dysan VSR diskettes used are manufactured using a spin coating technique that results in a 50-μm thick magnetic coating that supplies superior recording capabilities.

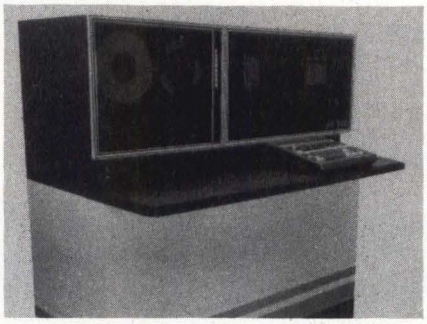
Read/write head carriage assembly is positioned via a heliband metal band that connects the assembly to the drive motor. A 1.8° stepper, the motor drives the heads in 0.0059″ (0.149-mm) increments equivalent to the spacing of data tracks on the diskette. Fine accurate movements of the assembly are made possible by a microstepping technique that permits rotation of the stepper motor in increments as small as 59 μin (1.49 μm)—1/100th of the spacing between data tracks. Modulating the width of the drive pulses of the stepper motor causes a variable current to flow in one drive coil and allows the rotor to be located anywhere between the motor's normal full-step positions. Closed loop feedback is supplied from a scale sensor through the microprocessor to the motor drive circuitry. The resulting positional accuracy between read/write head and data tracks is important in locating the reference track whenever a diskette is picked and clamped to the drive spindle.

Typical unformatted capacities are 4M bytes per cartridge using 800k bytes per diskette surface and 5.2k bytes/track in single-density recording; 8M bytes/cartridge, 1600k bytes/diskette, and 10.4k bytes/track in double-density mode. Transfer rates for these capacities are 250k bits/s in single density, 500k bits/s in double. Average rotational latency is 83 ms with track to track access time of less than 3 ms. Average seek time is 70 ms.

Prices in OEM quantities of 500 are in the $800/unit range. Evaluation units are being shipped; production volumes are expected to begin early in 1982.

Circle 268 on Inquiry Card

Disc based distributed plotting system handles 8-plotter network



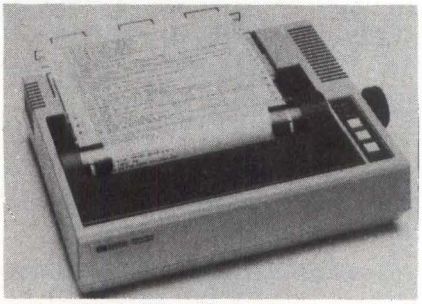
Users of multiple plotters can increase productivity and streamline their operations with Plot Management System PMS 7000 from Gerber Scientific Instrument Co, Inc, PO Box 305, Hartford, CT 06101. This disc based system permits up to 8 of the company's pen plotters or photoplotters to be managed in a distributed plotting network—linked to a host or standalone—reducing plot turnaround time and making better use of plotting resources. Plot queuing, data conversion, job accounting, and data transmission reduce plotter idle time, simplify plotter operations, and reduce media handling and plotter setup time.

From a single location, users can collect and convert data, allocate workload, prioritize plotting requirement, transmit information to remote plotting systems, and control and monitor the operation. Plot queuing allows priorities to be assigned to 32 jobs; the unit automatically transmits plot data specified on the queue to the next appropriate plotter.

Basic system configuration is the model 7100; operated by two interactive video display stations with a shared ASCII keyboard, this unit is driven by a 256k minicomputer, and includes 19.6M-byte disc drive, dual-density magnetic tape unit, and plotter interface. Options include an RJE communications package, distributed systems communications package, and 120M-byte disc drive.

Circle 269 on Inquiry Card

Thermal/impact printers offer low cost hard copy on desktop/personal computers



A family of thermal printers introduced for use with the HP 9826 computer system can also be used with HP series 80 personal computers, the HP 2640 family of terminals, automated test and measurement systems, and other desktop and personal computers; a companion dot matrix impact printer is intended for use with HP series 80 computers. The three thermal printers from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, feature 120-char/s bidirectional printing, HP-IB interface, and national character sets. They use flat fan-fold thermal paper; serial and parallel interfaces are optionally available. Model HP 2671A provides the full 128-character ASCII set, plus a line drawing character set for creating forms and a Roman extension set for national characters.

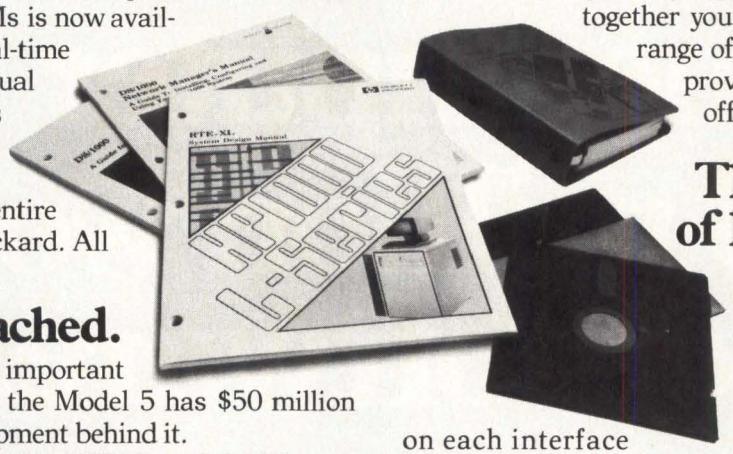
(continued on page 104)

There's more behind Hewlett-Packard's microcomputer than $50 million worth of software.

Full system support.

Announcing the new HP 1000 L-Series Model 5 microsystem.

The same two-board microcomputer that's becoming so popular with OEMs is now available as an integrated, real-time system—complete with dual minifloppies, 128K bytes of memory, your choice of interactive terminals *and* full support for the entire system from Hewlett-Packard. All for under $10,000.



All strings attached.

Software is the most important part of any system, and the Model 5 has $50 million worth of software development behind it.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the real-time computing environment your applications programs demand—programs you can develop in Assembler, FORTRAN 4X and BASIC. And our HP DSN networking software makes it simple to put low-cost computing wherever you need it.

Data base management on a microcomputer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

Configure it out for yourself.

The Model 5 is completely modular, so you can virtually design a system yourself. Hard disks and other peripherals can be plugged in directly. And thanks to a 60% reduction in memory costs, you can go all the way to 1/2 megabyte of memory for an additional $2000.

Whether you buy a packaged system, or put one together yourself, you can get HP's full range of customer support services, provided from more than 170 offices worldwide.

The ins and outs of high-speed I/O.

In designing the Model 5, we used an advanced distributed intelligence architecture that puts a separate LSI I/O processor on each interface board. This means each processor has its own direct channel to the entire 1/2-megabyte memory. (We used state-of-the-art 64K RAMs to put the 512K bytes of memory onto just one board.) With the CPU free to concentrate on computation, you get significantly increased throughput and exceptional performance.

If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or for more information, and our new OEM catalog, write to Joe Schoendorf, Hewlett-Packard, Dept. 12107, 11000 Wolfe Road, Cupertino, CA 95014.

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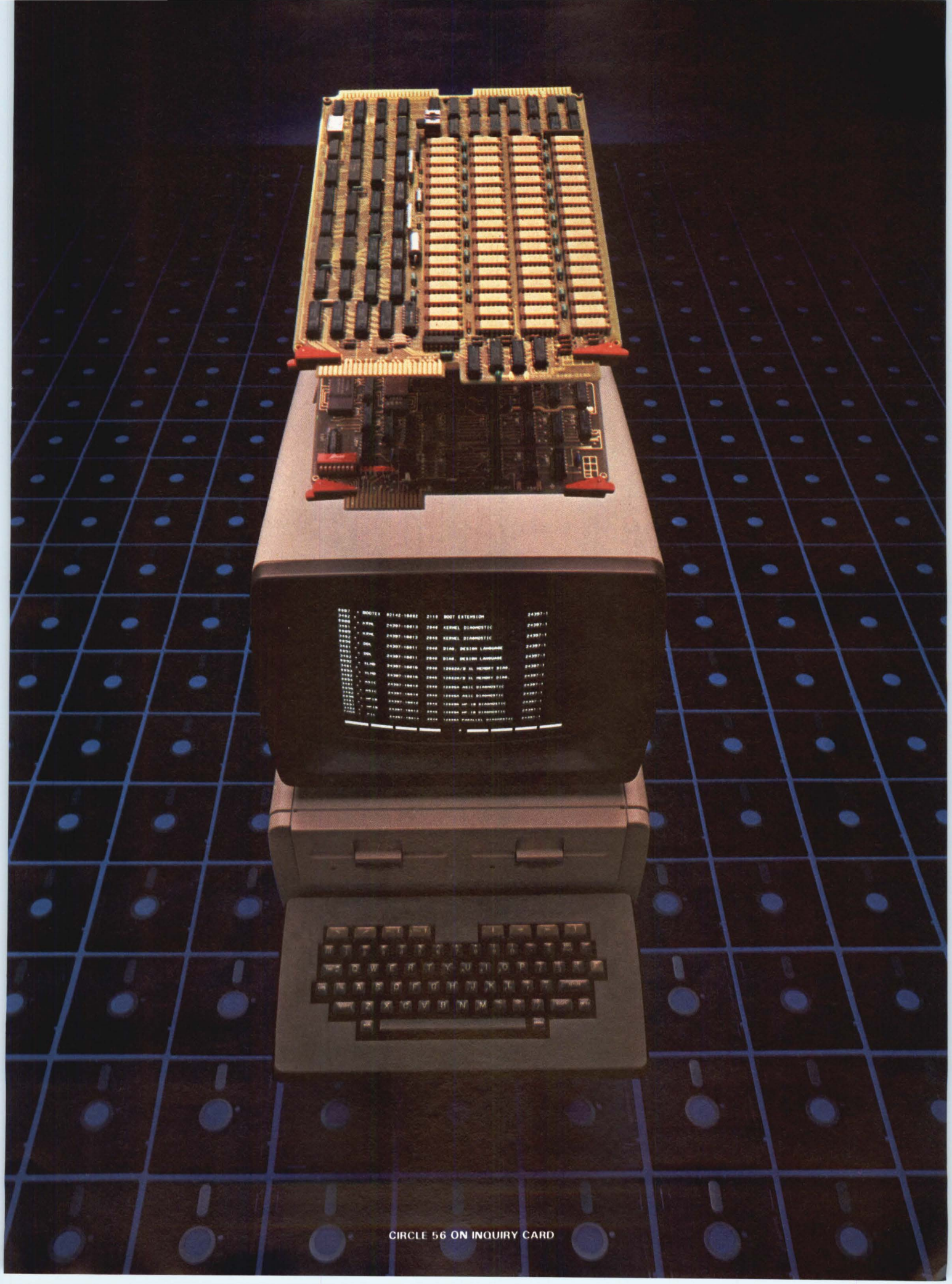
Prices U.S.A. OEM quantities of 100 units. Prices subject to change without notice.



CIRCLE 56 ON INQUIRY CARD

PERIPHERALS

Normal print mode of 80 cols/line and compressed print mode of 132 cols/line are standard. The HP 2617G provides high resolution raster graphics in addition to these features. Its 90-dot/in (35/cm) resolution allows precise copies of graphics from screen to hard copy. All of the HP 2617A and 2617G features, plus raster graphics functions, are provided by the HP 2673A thermal printer. Enhanced character sets, vertical and horizontal formatting, and print enhancements such as bold printing and expanded print mode are standard.

The HP-82905 dot matrix impact printer features a graphics mode that prints a dot-by-dot version of CRT graphics on hard copy. Variable columns and 80-char/s printing are standard. The printer is priced at $945.

Circle 270 on Inquiry Card

Nonimpact printer rivals units using laser xerographic techniques

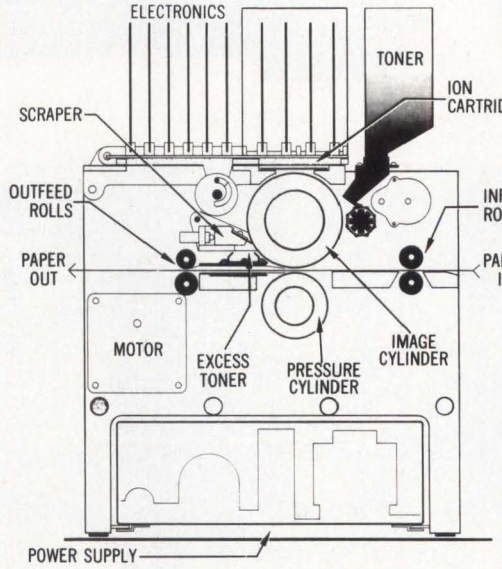
A nonimpact printing mechanism that forms characters comparable in quality to those of impact character printers, model 2460 image output module operates at 60 pages/min, using an ion deposition imaging technique. Marketed by Delphax Systems, 977 Pantera Dr, Mississauga, Ontario L4W 2W6, Canada, as a low speed, low cost alternative to units using laser xerography, the mechanism requires less than half the number of parts. This reduction in parts, and the accompanying reliability, is achieved by depending on electronics rather than complex mechanical assemblies.

The primary advantage of the ion deposition imaging mechanism is simplicity and reliability. Mechanisms reduce parts count by a factor of four and improve reliability four times over laser xerographic mechanisms. The six steps required for laser xerography are reduced to four basic process steps. These are placing a selective binary charge on a dielectric drum, developing the image, transferring and fixing, and cleaning excess from the drum.

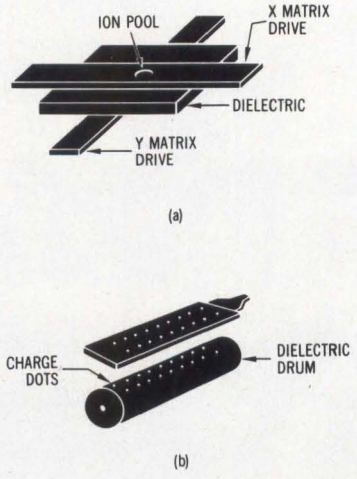
In place of the laser, modulator, and mirror assembly necessary in laser printers, the mechanism uses an easily replaceable ion projection cartridge that lays the image directly on a dielectric drum. The patented ion projection cartridge contains more than 2000 ion generators, each composed of an insulator layer with an electrode on each side. Air surrounding each electrode pair is ionized with an ac voltage pulse. Ions from the resulting pool are directed through a 2-dimensional matrix pattern toward the dielectric drum. The technique allows dots to overlap 50%, resulting in an image density or dot matrix resolution of 240 dots/in (94/cm) in either direction.

Constructed of a hardened aluminum sleeve, the patented dielectric drum

(continued on page 106)



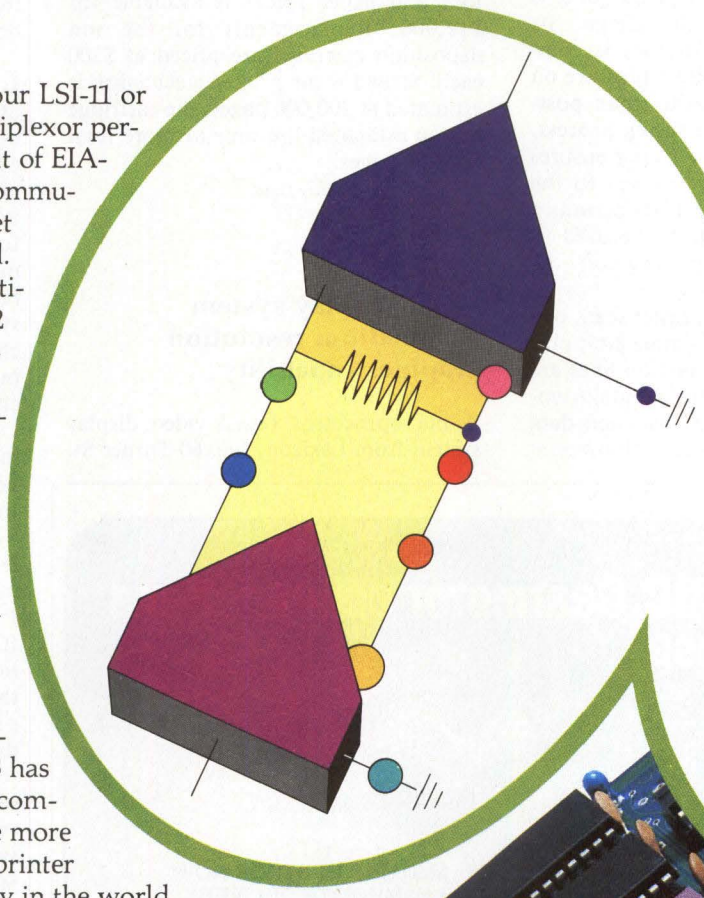
Delphax 2460 image output module provides simple reliable marking for high speed nonimpact printing applications. Key features include patented ion cartridge for image generation, durable dielectric drum, single component toning system, and straight-through paper path



Ion deposition technology used in 2460 image output modules relies on ion projection cartridge that lays image directly on dielectric drum. Cartridge contains 2000 ion generators (a) each composed of insulator layer with electrode on either side. Ions from pool are directed through 2-dimensional matrix pattern (b) toward drum that attracts negatively charged ions to form latent image to be toned

The only DZ11 Compatible Multiplexor for LSI-11. And it has RS-422 plus RS-232 and current loop capability-

MDB makes the difference!



Now you can have it all for your LSI-11 or PDP* 11 system! Full DZ11 multiplexor performance with the added benefit of EIA-RS-422 long line capability—communicates at distances to 3000 feet (914.4m) at rates to 19.2K baud. What's more, MDB's DZ11 multiplexors let you combine RS-422 with EIA-RS-232 in any combination up to a total of eight lines on a single board. Or combine RS-232 with current loop in the same way. Eight and sixteen channel RS-232 DZ11 multiplexors are also available. No more doubling up on boards, distribution boxes, rack space or price. You see the results in your system's performance and cost.

And that's not the only difference we can make to you. MDB has line printer controllers that are completely self-testing and we make more controllers for more computer/printer combinations than any company in the world. MDB offers PROM modules with window mapping, communications interfaces that support X.25 and a unique LSI-11/23 system with 22 bit addressing and up to 4 Mbytes of memory. From purely compatible to purely incredible all MDB products are built with exceptional quality and responsiveness to customer requirements. Our boards are warranteed for a full year, many are available off the shelf and they can be purchased under GSA contract #GS-OOC-02423.

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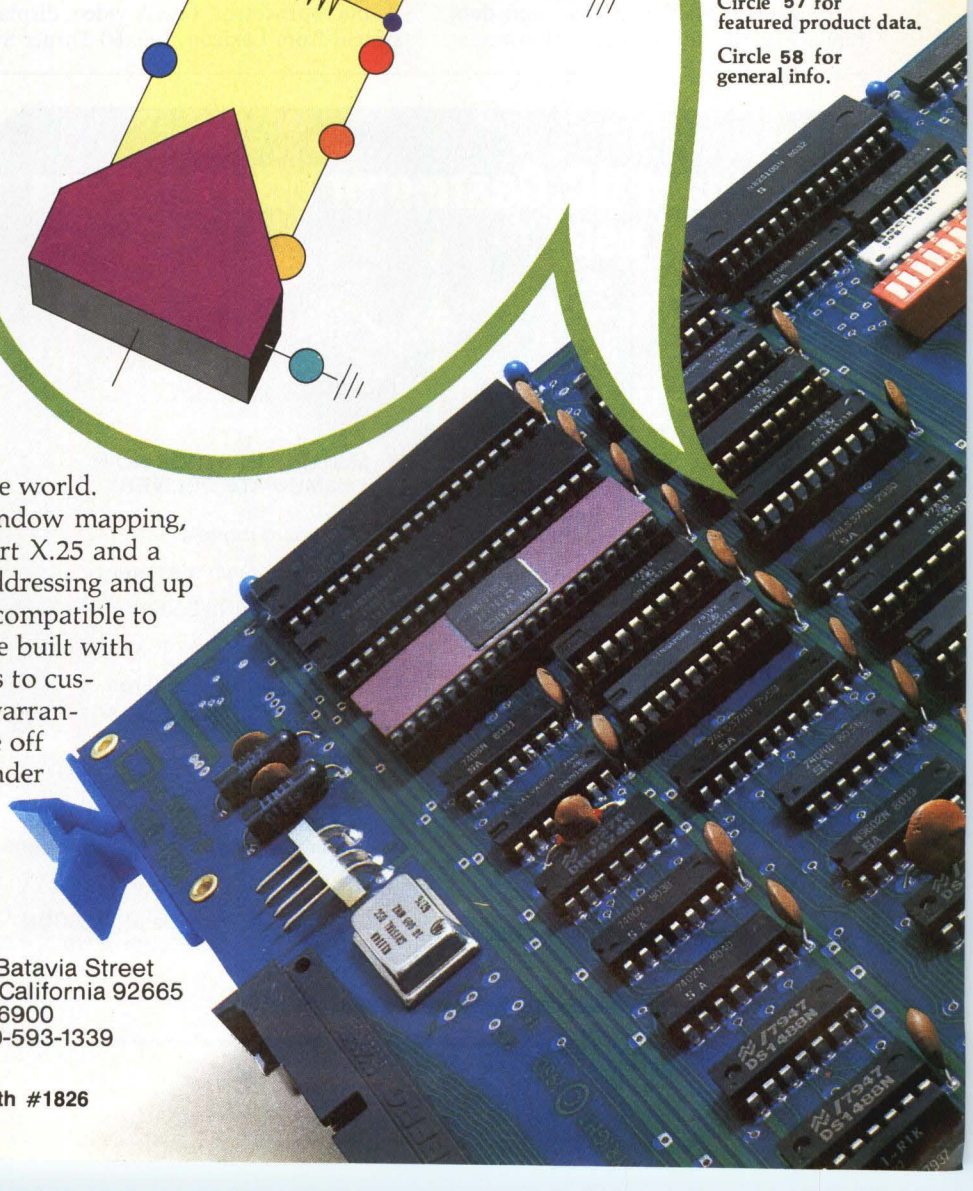
*Trademark Digital Equipment Corp.

Circle **57** for featured product data.

Circle **58** for general info.



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PERIPHERALS

rotates at 0.008″ (0.20-mm) distance from the cartridge. Elimination of the need for a photoconductive surface allows the drum to have a surface that is resistant to scratching, and capable of operating in normal light. The drum attracts negatively charged ions to its surface. The attracted ions form an electrostatic latent image.

A single component magnetic toner is used to tone the latent image. Its relatively low fusing efficiency is compensated for by using direct pressure on the dielectric surface rather than post-transfer heat during the fusing process. Transfer at the point of fusing ensures that most of the toner adheres to the paper. Durability of the drum permits a simple sharp steel blade to be used to remove the toner remaining on the drum.

The electronics accept raster scan, one page at a time, across a simple 8-bit plus parity interface. Four function lines are used to control mode and maintain synchronization. Maximum sustained data rate across the interface is 750k bytes/s; average rate assuming an 8.5″ x 11″ (21.6- x 28-cm) format is 615k bytes/s.

The 2640, consisting of controller module and power supply in addition to printer mechanism, will sell for approximately $8000 in OEM quantities. Formatter electronics, paper feeding and sorting systems, and software will turn the mechanism into a copier, facsimile device, or page printer depending on the type of digital signal provided. An evaluation unit including an RS-232 interface and paper feeder is available for $12,000. Replacements for the ion deposition cartridge are priced at $200 each. MTBF for the printer mechanism is estimated at 200,000 pages; the cartridge has an estimated life time of more than 100,000 pages.

Circle 271 on Inquiry Card

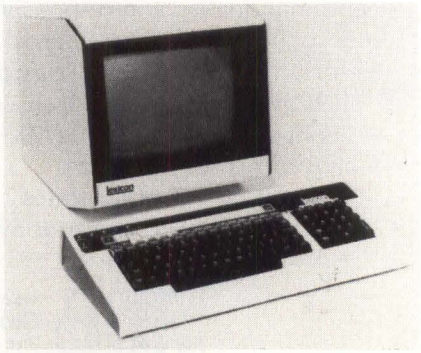
Video display system has medium resolution graphics capability

A microprocessor based video display system from Lexicon, Inc, 60 Turner St, Waltham, MA 02154, Lexiscope 4000 provides medium resolution monochrome graphics display capability using raster scan technology with a 560 x 500 fixed resolution. System firmware provides graphics capabilities, such as vector generation; selectable plotting modes and line styles; elastic line plotting aids; and graphics text with multiple sizes, styles, and orientation. The system also contains a full-featured alphanumeric display capability with separate memory that can be used and enabled independently of the graphics display.

Text in both the alphanumeric and graphics memories uses a 5 x 8-dot matrix in a 7 x 10-dot field. Two independent 25-line x 80-character pages of display memory can be alternated under software control. Optionally, the unit can display a 50-line x 80-character format with each character half of normal height. Descenders improve the readability of lowercase letters. The system allows the user to define custom characters or complete character sets to meet specific requirements. Custom character sets are implemented with EPROMs, eliminating the need for custom masks. The system also supports hard-copy output of graphic and alphanumeric images.

Compatible with Data General models 6503/D200 terminals, the system emulates many of the features of the Hewlett-Packard model 2648A graphics terminal. It plugs into any available slot of the NOVA® or ECLIPSE® backplane and uses the main computer's bus as a high speed parallel interface between host and display.

Available as a complete system or as separate components, the system allows cost-effective integration into OEM and system integrator configurations. The M-4 display monitor, a 12″ (30-cm) P39 green phosphor unit, and two modes of KB4 detached serial keyboards are optional, and a host-independent RS-232-C version of the system will be available later this year. Single-unit price for the system is $3400.



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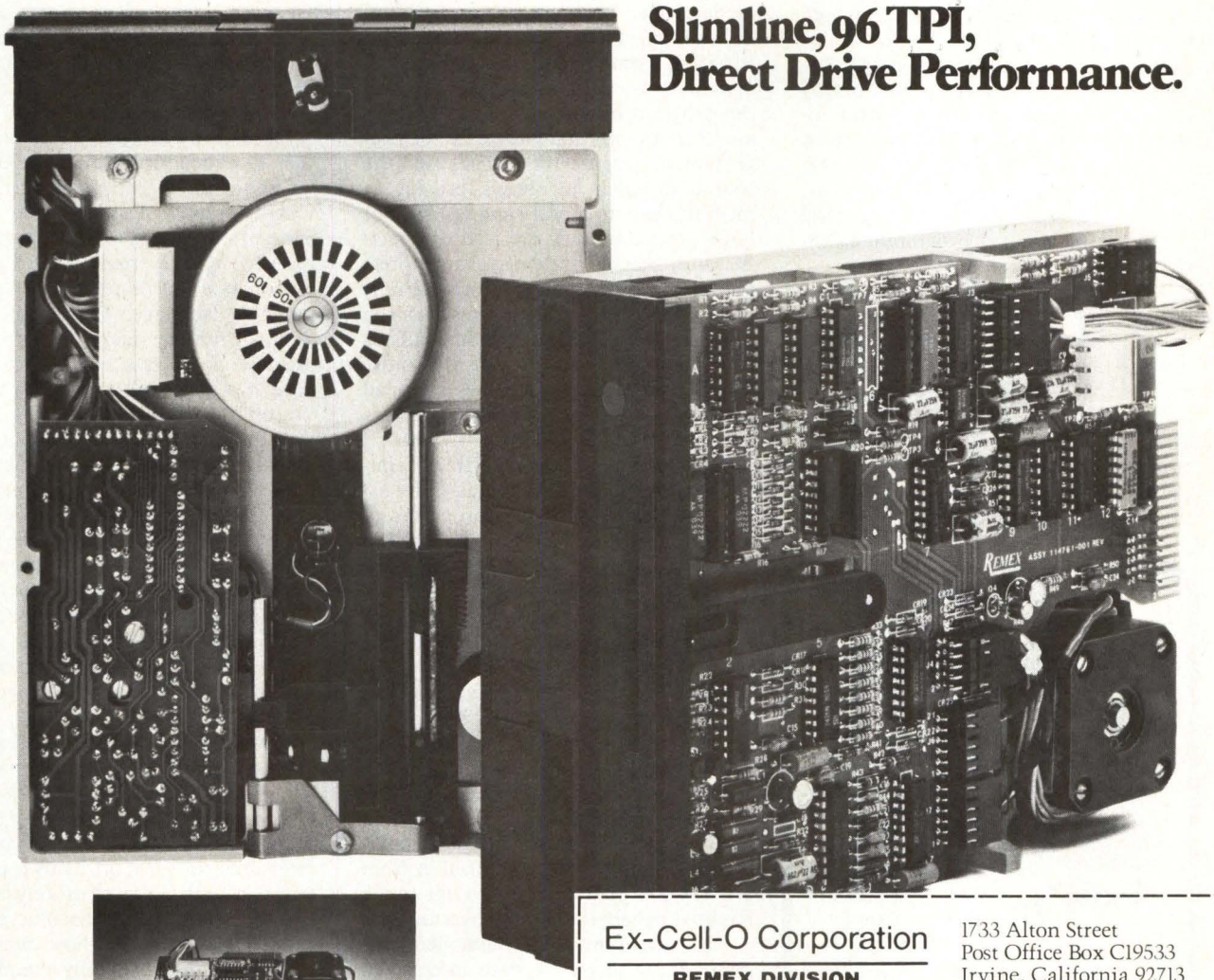

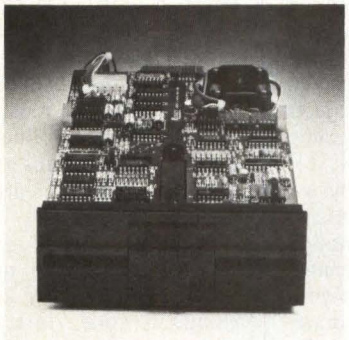

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SOFTWARE

Compilers replace interpreters as microprocessors come of age

Although the benefits of programming microprocessors in a high level language are difficult to ignore, the great variety of complicated program development techniques may have discouraged high level language use. Now, a general purpose, portable, language system implements Pascal on microprocessors by providing a traditional development environment that will be familiar to most minicomputer programmers. It is perhaps the first machine-independent, retargetable, Pascal system for general use in a minicomputer programming environment.

Among the many factors that make Pascal a good choice, its unusual flexibility to serve a wide range of applications certainly stands out. Scientific and engineering programs typically perform extensive calculations on small amounts of data that have relatively little internal structure. In striking contrast, commercial programs usually perform simple calculations on large amounts of highly structured data. Pascal is the premier language designed specifically for both types of programming.

Most microprocessor based languages are implemented as interpreters and, until recently, Pascal was no exception. Program statements are stored in memory. A runtime package executes the program by interpreting each statement. Interpretive languages can be programmed interactively because the source program is always present in memory, easy to modify and restart. For large programs, they are also compact: A 20- or 30-char statement can express the task of a hundred or more machine instructions. Interpreted programs run five to ten times slower than machine code, however, and because the entire runtime package is always present, small programs incur substantial memory overhead.

Minicomputers and mainframes implement most high level languages by using compilers that translate programs into assembly language. Compilers are not interactive. Because source program statements will be long gone from memory by the time a compiled program runs, debugging involves a tedious cycle of edit, compile, assemble, link, load, run, and edit again. Compiled programs typically occupy 20% to 30% more storage than hand-optimized machine code, or up to ten times more space than interpretive code. They are quite fast, however, and although they do need some runtime support, only those components actually used are linked in from a library, so that small programs pay a minimal penalty in storage overhead.

Fast execution makes compiled programs more attractive than interpreted programs, especially for small projects where a compiled program will occupy less memory as well. Unfortunately, it is more difficult to compile a program than to interpret it, and few microprocessors are fast or powerful enough to support a good compiler. So-called interpretive compilers offer a hybrid solution. They translate source statements into an intermediate pseudocode that resembles a powerful assembly language. Then, a relatively small runtime package interprets the compiled pseudocode. Pascal is almost always implemented this way.

The many Pascal language systems available for microprocessors differ only in two important respects. They are more like a pure compiler, if the pseudocode is close to machine language, or more like a pure interpreter, if the pseudocode is quite powerful, with attendant trade-offs in either case. Also, options during compilation or interpreting have great impact on flexibility and convenience in the programming environment.

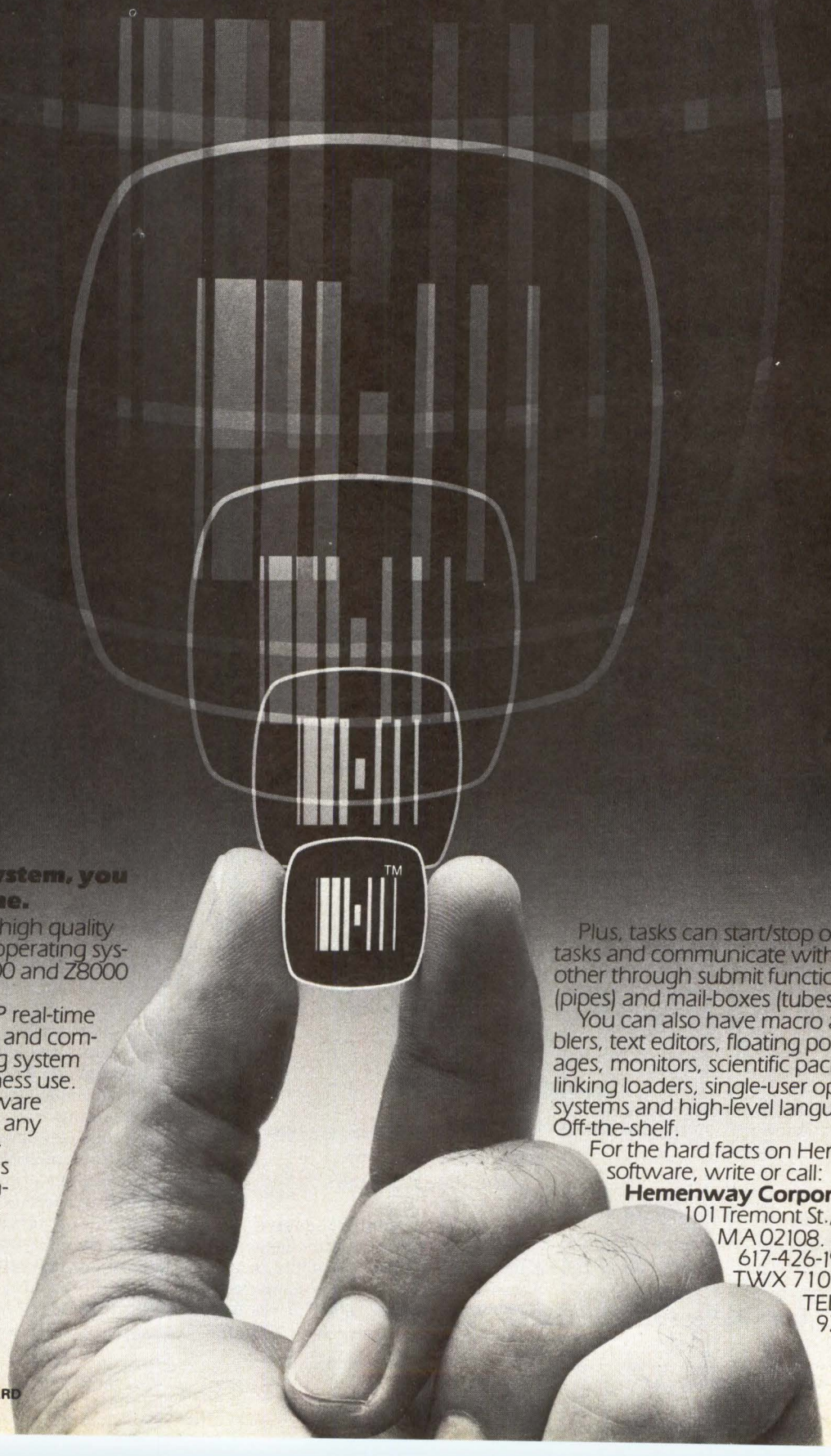
Licensed by Language Resources Inc, 4885 Riverbend Rd, Boulder, CO 80301, for about $5000/copy, PAS-86 runs on a VAX-11 (under VMS), PDP-11 (UNIX), System/370 (CMS) or 8086 (RS86) to compile Pascal language programs and produce pseudocode that is remarkably close to assembly language. Then, although an optional runtime package interprets this pseudocode on 8808, 8085, or Z80 targets, most designers will use the host based "resolver" to further convert pseudocode into native instructions that execute directly on the 8-bit microcomputers or the 8086. PAS-86 thus combines pure compiler performance with an interpreter option that can compress large programs. Most important, programmers use PAS-86 exactly as they would use a conventional cross-compiler for a prototype minicomputer. Although ISIS and others are supported, there is no need for a specialized microprocessor development system.

Portability is an essential feature of any high level language, and PAS-86 ensures machine independence in two interesting ways. As a software vendor, Language Resources Inc is naturally motivated to transport its own product. PAS-86 is written almost entirely in Pascal and is in fact highly machine independent. Extending the host and target machine sets requires only a modest programming effort, mostly directed at the "resolver" that produces native code for the target. PAS-86 users can be assured that their programs are at least as portable as PAS-86 itself.

Often overlooked, a subtle characteristic of interpreters makes interpreted programs inherently less portable than compiled code. Interpreted languages are easy to enhance, whereas compiler extension tends to be difficult. Market pressure and designer temptation have produced many supersets of BASIC, for instance, and interpretive Pascal shows the same tendency toward nonstandard extensions. End users may appreciate

(continued on page 110)

Introducing MSP 16-bit Multi-Tasking Systems Software



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CIRCLE 62 ON INQUIRY CARD

SOFTWARE

the relatively high compatibility among standard compiler dialects (eg, FORTRAN) and expect equally good portability from programs compiled under PAS-86.

Certain capabilities that might be considered features are notably absent from PAS-86. It will not interpret pseudocode on the host machine. Conversely, it will not compile a Pascal source on the target machine. Even the target machine interpreter is optional for 8-bit microprocessors. There is no target interpreter for the 8086, perhaps because it almost executes the pseudocode directly.

All of the missing capabilities would be easy enough to add, but all were omitted on purpose. For example, there is little to gain by interpreting an 8080 program on a VAX-11. Although it might achieve rudimentary debugging, a false sense of confidence is the more likely result. Similarly, although 8080 based compilation could bypass downloading and approach the convenience of interactive development, it would also keep programmers waiting for the 8080 to perform a lengthy task that is far better suited to a supermini.

As microprocessors approach or even surpass minicomputers in performance and memory size, the trend is likely to be away from the interpreted programs that have been common on microprocessors and toward the compiled programs usually found in a minicomputer environment. Now, a Pascal programming system exploits this tendency by generating native microprocessor code on a timesharing system. Dispensing entirely with the proprietary microprocessor development system, it allows high level programming of microprocessors in the familiar development environment typically used to program minicomputers.

—Shawn Spilman, Technical Editor

Circle 273 on Inquiry Card

16-bit operating system handles 32 users, executes 256 tasks

OASIS-16, a comprehensive 16-bit operating system, offers features that increase capability, flexibility, and convenience, while providing complete compatibility with Z80 OASIS. Developed by Phase One Systems, Inc, 7700 Edgewater Dr, Suite 830, Oakland, CA 94621, the system supports dynamic user partitioning for up to 32 users, an enhanced ISAM file structure, interprocess communications, expanded memory capacity, priority scheduling, enhanced EXEC job control language, a new tape drive, device drivers, and a full screen editor. Written in C, the system will be easily transported from initial 8086 designs to targeted Z8000 and 68000 CPUs, as well as others.

Dynamic file allocation avoids the need to pre-allocate space for major files. The initial file open creates a space that expands as necessary. To facilitate this feature, all files are byte addressable at the lowest level. ISAM files feature a Beta + tree structure. The extended binary "tree" can be searched from any "branch" down to any "twig" or "leaf" to find a record. Variable length records replace fixed length versions. This approach speeds the insertion, retrieval, and modification of records.

Performing task to task communications, interprocess communications allows one file to open a channel to another and communicate with it directly. Maximum file size is 273M bytes; up to 32 volumes can be online, for a total of 8736M bytes available at any time. The full screen editor offers full cursor controls and backward/forward scrolling. Built-in macro capability allows up to three complex chained editing functions with a single operation. Special global, line, and character oriented modify commands are also included.

Priority scheduling assigns up to 8 precedence levels as part of the log-on profile. Enhancements to the EXEC JCL allow use of words with more than eight characters and pass an unlimited number of arguments. New command verbs include FOR/NEXT, REPEAT/WHILE, and DO/UNTIL, plus others.

Additional features include dynamic file allocation, multilevel dictionary, sequential and keyed file access types, file locking and automatic record locking, relocating macro assembler/debugger/linkage editor, high level BASIC compiler and interpreter, and diagnostic and conversion utilities. Options include CONTROL relational DBMS, file sort, BiSync 2780/3780 communications package, IBM 3740 formatting utility, C compiler, RM COBOL, Pascal, FORTRAN, and Forth. The system is priced at $1495.

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GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

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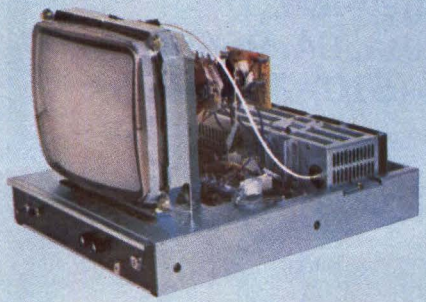
You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



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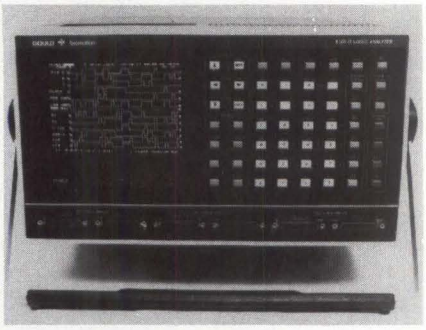
CIRCLE 64 ON INQUIRY CARD

TEST & MEASUREMENT

Logic analyzer handles integration problems in stored program systems



With 48 data input channels, 512 x 48-bit memory, and 100-MHz front end, Biomation's K101-D handles high speed data and timing recordings of complex program flows. Flexible clocking and trace level control suit bus oriented applications

Supplying the high resolution time and data analysis demanded by microprocessors, minicomputers, and mainframes, the K101-D serves as a powerful tool for integrating hardware and software, and is designed to handle the timing and data analysis problems that crop up in complex stored program based systems.

This high performance 48-channel logic analyzer from Gould Inc's Biomation Div, 4600 Old Ironsides Dr, Santa Clara, CA 95050, monitors time and data and adds interpretive features to solve software problems and subtle hardware errors. Demultiplexing capability of the instrument is particularly valuable in microprocessors that use multiplexed signals to reduce pins and save space. Sophisticated input clocking allows data to be traced in virtually any multiphase clock system. The unit features 12 external clock inputs that can be combined to provide synchronous clocking up to 50 MHz, as well as versatile data formatting, an integrated digital voltmeter, frequency counter, four input modes, and six clocking modes.

To isolate and record relevant sections of a data stream, the unit can select a sample of data by bit pattern and clock or event delays, continuously recording according to instructions and then arranging recorded data in a variety of formats. The analyzer can follow a program sequence, isolating and recording specified sections of data flow, and can summarize entry, execution, and exit codes of a complex instruction loop in a

(continued on page 114)

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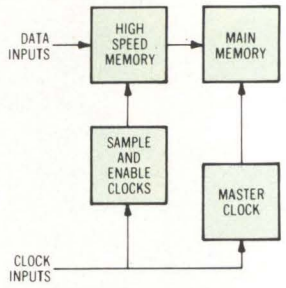
CIRCLE 66 ON INQUIRY CARD

TEST & MEASUREMENT

single pass, even though instructions may be separated by several megabytes of data. There are 16 selective trace control levels, each with user definable stop, jump, advance, and trace events with data patterns up to 48 bits wide.

Twelve separate clock inputs arranged as six sample clocks and six latch enables allow users to match the clocking scheme to testing needs. Clock selections are specified from six Boolean equations. Internal clocking with 10-ns resolution reveals timing problems and data skew. Glitch capture is better than



Each of K101-D's three input sections can be clocked separately, or clocked from the same signal. Clock input from one section can clock in synchronous data from another section. Thus, users can mix internal and external clocks and shift data from high speed to main memory

5 ns. Simultaneous internal and external clocking enable simultaneous time and data domain measurements.

The analyzer has four user selectable threshold references: preset TTL, ECL, and two variable thresholds with a ±10-V range. Sample, glitch, latch, and demux input mode options pinpoint anomalous conditions.

Data are displayed in binary, octal, hex decimal, ASCII, EBCDIC, and sign. A search feature locates combinations of data words, or addresses, and indicates first, last, and next occurrences in memory. Compare, backed by a 515 x 48-bit memory, indicates discrepancies between old and new recordings. Graph display uses a word value on the vertical axis and memory location on the horizontal axis to present an overview of program behavior, making loops, branches, and control/status cycles easy to recognize.

Time domain displays of internally clocked recordings show details down to 10 ns. All 48 channels may be viewed and individual channels compared using a system of up to 10 pages, made up of 6 signals each. Up to 24 channels can be viewed at once.

The unit's programmable RS-232-C and IEEE 488 parallel ports enable users to control instruments, transfer data, convert output into hard copy, or feed data to a computer. An additional RS-449 port provides capability to communicate with future peripherals and probes. The analyzer is designed to interface with disassembly modules that will automatically transform machine code into assembly language.

Circle 275 on Inquiry Card

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Call this expert team into consultation, anywhere in the U.S.A. (or visit us at OIS). The team is equipped with versatile fiber-optic system demonstrators that allow them to "mock up" a state-of-the-art data-link system — **tomorrow's** state of the art, available today. They also have driver/modulators capable of putting any OIS laser source through its paces, under *realistic* conditions duplicating actual usage.

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- Complete line of Digital Transmitters and Receivers that can be combined to meet all laser and LED link requirements.
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CIRCLE 68 ON INQUIRY CARD

INTERFACE

Color graphics controller supplies high resolution on single Multibus board

RGB-GRAPH is a color graphics video display controller on a single Multibus compatible plug-in board. Hardware features incorporated in the board by Matrox Electronic Systems, Ltd, 5800 Andover Ave, TMR, Quebec H4T 1H4, Canada, include zoom, shift, pan, scroll, clear, clip, mask, and overlay. Software programmable video parameters enable users to drive most black and white or color monitors.

Consisting of six main functional units, the controller produces a bit mapped display with user selectable resolutions. Each pixel can be addressed via a pair of X and Y position registers that feature an auto increment/decrement capability for high speed vector drawing and DMA control. A VLSI circuit, the CRT controller provides all video timing signals including horizontal and vertical sync and blanking, display refresh RAM addresses, as well as timing and control for cursor and lightpen. Made up of 128k bytes of dynamic RAM, display refresh memory gives 512 x 512 x 4 resolution; each pixel in memory is identified by a 4-bit address. The controller scans memory every 16.66 ms to generate video signals or load digitized images into memory at speeds of over 100M bits/s. The video generator performs conversion of data from RAM into video signals, conversion of digital video data into RAM writable format, and hardware video processing functions such as zoom, scroll, and overlay.

Normally the board appears to the CPU as 16 consecutive 8-bit wide I/O locations strapped on any 16-address boundary. In DMA applications, an additional video RAM window 1k-locations wide is mapped into the CPU memory space. Starting address for this 1k block can be positioned anywhere in the 20-bit memory map.

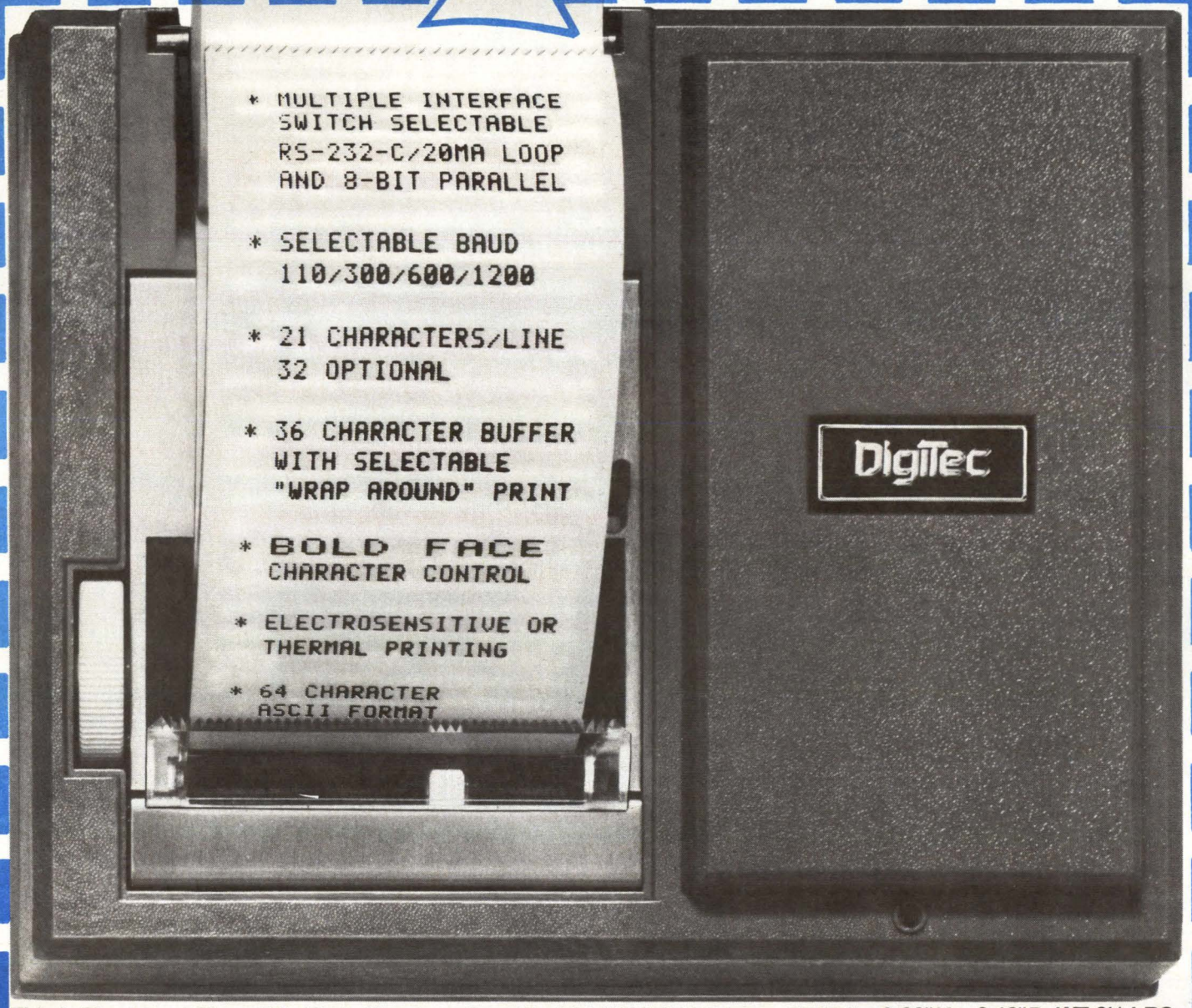
Vertical scroll and horizontal shift capability can be combined to produce a full 2-dimensional pan inside the 512 x 512 address area. Zoom is independently controllable in the X direction (magnification by 1X to 8X) and Y direction (magnification by 1X, 2X, or 4X). Hardware clear allows the display to be cleared to black or a preset color in a single frame. Overlay logically combines the fourth video plane with the other planes; overlays can be programmed AND, NAND, OR, or XOR. A mask register enables display and loading of selected video planes under software control.

A single card can be configured for a 256 x 256, 512 x 256, 512 x 512, 1024 x 256, or 1024 x 512 display format with up to 4 bits/pixel. Multiple cards can be stacked to provide up to 16 bits/pixel with up to 65,536 different colors. A color display alphanumeric board is also available.

Software for generating vectors, polygons, conics, area fills, zoom, scroll, and special video effects is available. Firmware for emulating Tektronix 4010 or 4016 graphics terminal permits an intelligent color terminal to be built by combining an RGB-GRAPH with the company's ZBC-80 CPU board.

Circle 276 on Inquiry Card

If your printer can't fit in this space and you're paying more than $299,* you're using the wrong printer.



This Is The Actual Size of DigiTec's New Low Cost Model 6430/6470 Printers 7.38"W x 3.08"H x 6.12"D, WT 3½ LBS.

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Circle 70 for Info Only. Circle 83 for Demo Only.

INTERFACE

Disc drive controllers support multiple 5.25″ hard disc drives

Microprocessor based DTC-510 provides all the functions necessary for control of up to two 5.25″ (13.34-cm) Seagate Technology ST506 Winchester disc drives; DTC-520 can handle up to four ST506 and IBM compatible single- or double-density, single- or double-sided minifloppy drives in any combination. Both controllers, products of Data Technology Corp, 2344A Walsh Ave, Santa Clara, CA 95051, feature microprocessor intelligence, single-board design, shared power supply with the same power requirements as drives, and efficient host protocol.

Controller functions include overlapped seek, logical to physical unit correlation, automatic seek and verify, automatic head and cylinder switching, odd parity checking, logical sector addressing, sector buffer and interleaving, error detection and correction, extensive fault detection, and integral data separation. Commands and data transfers are transmitted from the host over a bidirectional 8-bit data bus. Typical I/O requests are performed by passing a command description block to the controller. Optional microdiagnostics provide for incoming inspection, system test, and/or field service. For quantities of 500, the DTC-510 controller is priced at $650, and model DTC-520 at $750.

Circle 277 on Inquiry Card

Mini-cassette controller adds mass storage to Z80 STD BUS systems

Digital cassette controller board CCB-1 adds 18k bytes of file oriented offline storage to the basic Z80 STD BUS system. With the board, Tetronics, 322 E Deepdale Dr, Phoenix, AZ 85022, supplies a separate 2716 EPROM to handle board initialization and provide compatibility with the Mostek CPU-1, DDT-80 operating system (Version 1.3), and ASMB-80 assembler, editor, linking loader (Version 1.0). The EPROM allows the tape transport to replace paper tape I/O, without changing the Mostek output commands.

The general purpose board also interfaces to other operating systems or user generated software. Wirewrap jumpers are provided for user selectable functions including I/O port addresses, read after write operation, and common or independent power for the tape drive motor. The controller allows files to be searched and provides true digital cassette drive and extensive error checking. The board generates and decodes Manchester phase encoded signals for the cassette transport.

All inputs and outputs are fully buffered. The output is specifically designed to drive a Braemar CM-600 digital cassette transport; however, the board can be modified to drive other transports. The board measures 4.5″ x 6.5″ x 0.062″ (11.4 x 16.5 x 0.157 cm) and offers single 5-V operation or 5- and 12-V operation when separate motor drive power is desired.

Circle 278 on Inquiry Card

THE LAST THING WE'LL SELL YOU IS A TERMINAL.

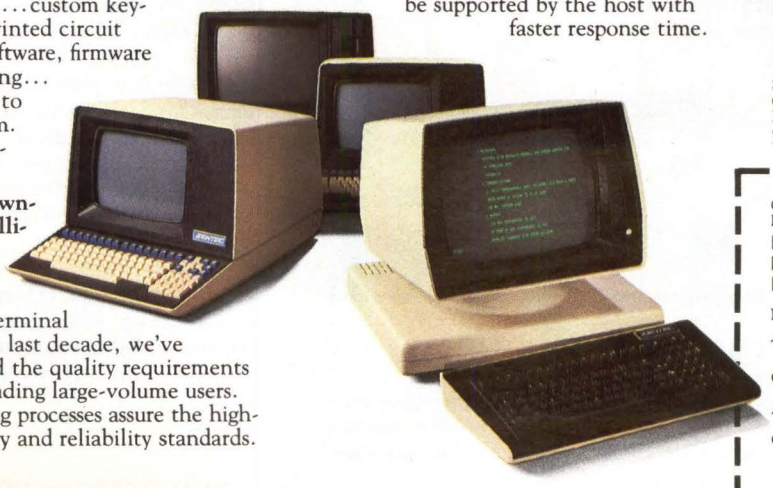
There are hundreds of CRT terminals on the market. Some good. Some not so good. And you can buy most of them, right off the shelf. So why do more large-volume users specify Zentec? It's simple really. We provide intelligent solutions to your information processing needs. It's our business. And our solutions don't begin with a terminal. They end with one.

The Total Solution—a Custom Approach
The solution begins with you, with your system and business objectives. We work with you to help analyze and set your objectives from the viewpoints of marketing, engineering, manufacturing and your customer. Then our hardware and software team applies your solution requirements against our modular systems. We implement a unique terminal workstation around a flexible minicomputer-like bus architecture and threshold LSI technologies. In short, Zentec provides a custom solution... custom keyboards, custom printed circuit boards, custom software, firmware and even packaging... whatever it takes to solve your problem. All at a very competitive price.

Lower Cost of Ownership—the Intelligent Investment
Quality is a fundamental part of every Zentec terminal system. Since the last decade, we've met and surpassed the quality requirements of the nation's leading large-volume users. Our manufacturing processes assure the highest product quality and reliability standards. Each component, subsystem and system is 100% tested. Burned in. Then tested again. As a result, our DOA (Dead-On-Arrival) rate is less than 1%. This means you can eliminate testing our terminals prior to shipment to your customer. And our MTBF (mean time between failure) is over 10,000 hours. That translates to fewer service calls. But even if a call is necessary, our MTTR (mean time to repair) is now under 20 minutes. Work the entire equation: *competitive price + low DOA + long MTBF and short MTTR = low cost of ownership.*

Custom Solutions—Added Value
The fundamental values of a custom terminal can add up to your most intelligent alternative, specifically:

- Code executed at the terminal workstation level reduces host overhead, extending the life of the host system.
- More terminal workstations can be supported by the host with faster response time.
- Faster response time, keyboards customized to meet application requirements and other ergonomic features add up to high operator productivity.
- Value-added terminal workstations assure greater control of the aftermarket for your products.



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CD9

CIRCLE 73 ON INQUIRY CARD

MEMORY SYSTEMS

Standard RAM modules provide memory expansion for Q-bus/Multibus systems

Two standard RAM module series, fabricated using 64k-byte dynamic RAM technology for high density and low power requirements, are offered by Texas Instruments Inc, PO Box 1443, Houston, TX 77031. The TMM10010 series provides cost-effective memory expansion for LSI-11 computer systems; memory expansion for Multibus systems is provided by the TMM40010 series.

Offered in 128k-, 192k-, and 256k-byte RAM modules with an onboard P/ROM to handle logic functions, a second-generation version of the TMM10000 series, the TMM10010, can operate at maximum Q-bus speed. Typical read access speed is 175 ns, typical write access speed is 75 ns, and typical read or write cycle time is 360 ns. Jumper selectable address space permits the user to address from 256k to 4M bytes; the user can also select starting addresses on 4k-byte boundaries. An optional parity controller eliminates the need for a separate parity controller board.

The Multibus compatible TMM40010 series modules are available in 64k-, 128k-, 256k-, and 512k-byte versions. Typical read and write access times are 325 and 110 ns, respectively. Typical read or write cycle time is 710 ns. The modules operate in either the standard 64k-byte address space or 1M-byte extended address space. Starting and ending addresses are independently selectable on 4k-byte boundaries. Word transfer and high-, swap-, and low-byte transfer are supported.

In addition, the series provides single-bit error correction and double-bit error correction with inhibit capability. Onboard LEDs indicate the type of error and the exact location of the failing RAM. Control status and error status registers, accessible via two I/O ports, are also provided. Optional features include a user selectable battery backup and an advanced-acknowledge feature providing read acknowledges of 110 to 320 ns.

TMM10010 modules measure 8.43″ x 5.187″ (21.41 x 13.175 cm) and require an operating voltage of 5 V ±5%. TMM40010 modules measure 12″ x 6.75″ (30 x 17.15 cm) and require an operating voltage of 5 V ±5%.

Circle 279 on Inquiry Card

Single vendor graphics support...

We've put the pieces together.

SYSTEMS Graphics Support Platform provides you with three key elements —graphics support software featuring Template ™, CONCEPT/32 minicomputers and support for a wide range of graphics devices. Our single vendor graphics support is the best approach to meet your computer graphics requirements.

Template is the most powerful and comprehensive 3-D graphics software support package available today. With over a dozen device drivers, SYSTEMS Graphics Support Platform provides you with the graphics device independence and state-of-the-art functionality required for most user applications. To fully support Template, SYSTEMS provides on-site installation, training and customer service.

SYSTEMS CONCEPT/32 minicomputers provide the speed, precision, addressability and software development tools to complement Template and the various graphics devices. To get the complete graphics support picture, call or write the company that put all the pieces together.

Systems Engineering Laboratories, Inc., 6901 W. Sunrise Blvd., Ft. Lauderdale, FL 33313. (305) 587-2900, 1-800-327-9716.

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Proven COMPUTER Performance

SYSTEMS

A Subsidiary of GOULD INC.

CIRCLE 75 ON INQUIRY CARD

MEMORY SYSTEMS

Board provides 1M byte plus program security for desktop computers

WMAZ-4, a 512k-byte memory board developed by Eventide Clockworks, Inc, 265 W 54th St, New York, NY 10019, uses 64k-byte RAMs to expand the memory size of a Hewlett-Packard 9845 desktop computer. A hardware security system gives software suppliers and OEMs positive security against unauthorized software use. ROM modules can be added with BASIC extensions and utilities. Security is provided by an electronically encoded serial number read by the proprietary program. This code prevents programs from being run on any other machine; if the code is missing or incorrect, the user can be informed that he is not adhering to his license, or the program can be erased. It is impossible to run the program without the program security code; although programs can be copied, they are not usable.

A programmer's utility package ROM that is optionally available with the board provides new BASIC keywords that enhance programming productivity. Available commands include XREF, MAP, CHANGE, FIND, DUMP ALPHA, and MSI (mass storage is).

Two versions of the board are offered. The 512k-byte board is priced at $6500, and a half-populated version, at $4250.

Circle 280 on Inquiry Card

RAM card serves as 8- or 16-bit wide memory for S-100 systems

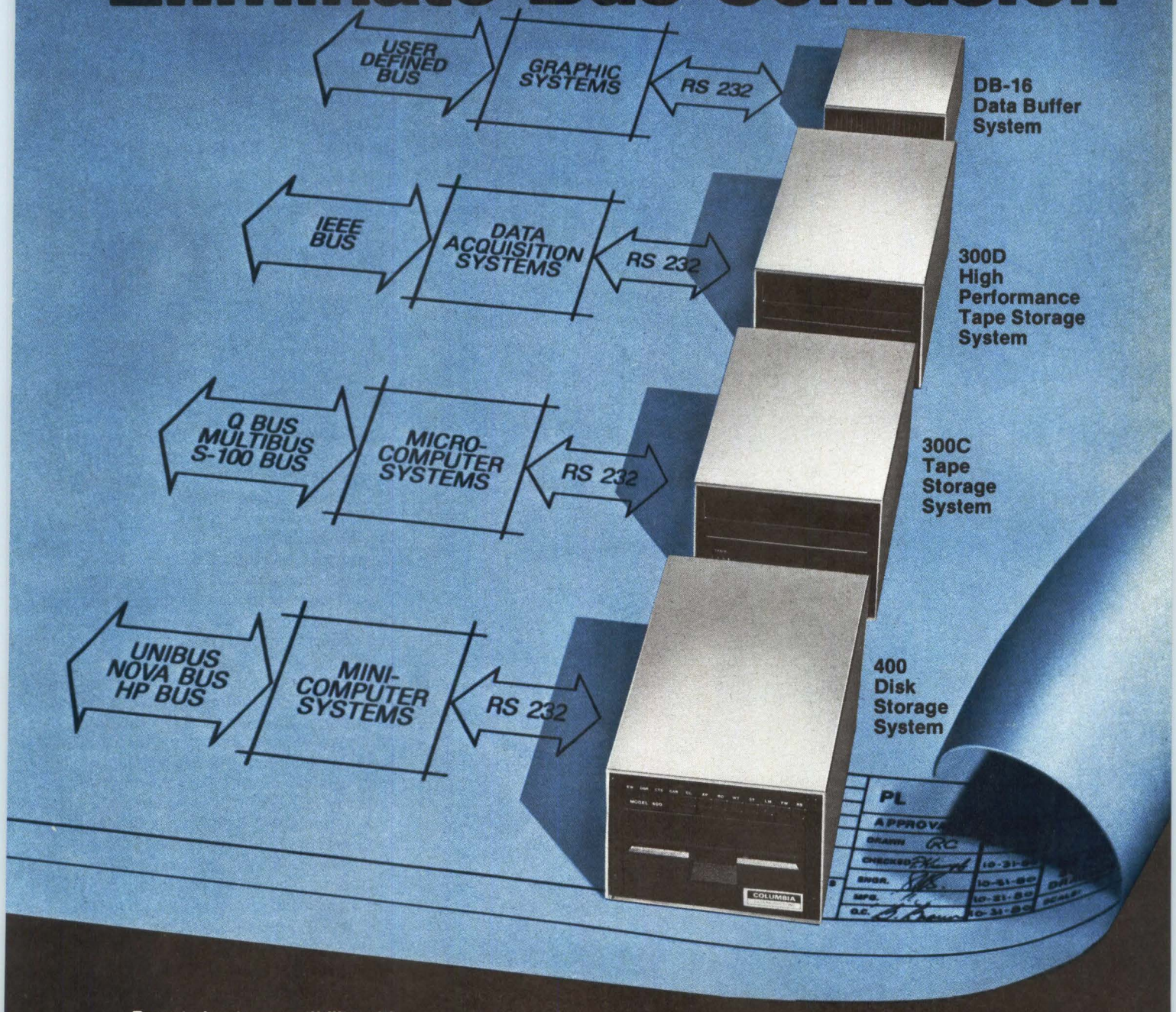
SCP-110 acts as either an 8- or 16-bit wide memory for S-100 bus systems. Using Intel's 100-ns 2167 type power-down memory chips and a fully static design, the 64k-byte card from Seattle Computer Products, Inc, 1114 Industry Dr, Seattle, WA 98188, eliminates system timing problems and allows operation with a variety of CPU cards and DMA devices.

Organized as 64k x 8 or 32k x 16 bits with dynamic data bus switching, memory is addressable on any 64k boundary within a 16M-byte address space. The card uses extended 24-bit addressing, the upper 8 bits of which can be disabled. Block disabling allows disabling of any 4k block, all of the board above a 4k boundary, or all of the board below a 4k boundary. Access time from address is 190 ns, and memory management is provided without wait states.

Chips are used in a power-down mode to minimize current. Power requirements for an active board are 1.6 A at 8 V, while an inactive card requires 0.8 A. All signal inputs to the board pass through Schmitt trigger buffers and have a minimum of 0.4-V hysteresis at 25 °C. Operating temperature is 5 to 65 °C. The card is available in 16k-, 32k-, and 48k-byte versions (for OEMs only); 16k- and 48k-byte versions are 8-bit wide only. An optional version that uses 70-ns 2167 chips is also available.

Circle 281 on Inquiry Card

Our RS-232 Peripherals Eliminate Bus Confusion



Forget about compatibility with the Multibus, Q bus, S-100 bus, Unibus or the host of others. Most systems have an RS-232 data port. So select an RS-232 compatible peripheral from Columbia Data Products and leave the bus confusion to others.

System compatibility isn't all you get with CDP peripherals. You also get microprocessor intelligence in our floppy disk, cartridge tape or RAM based storage systems.

That intelligence gives you remote control and failsafe operation for data acquisition applications ...comprehensive editing for data entry, graphics and data processing applications...file management and telephone data logging for data communications applications.

And Columbia Data peripherals also deliver performance. Dual port data transfer rates can be up to 19.2K baud, with storage capacity of 5.15 Mbytes on tape, 180 Kbytes on disk and 32 Kbytes in RAM. The buffered input and output ports can be set at different baud rates to match system requirements and constraints...or achieve data rate conversions.

With intelligent tape and disk systems priced under $1400 and semi-conductor storage under $700 in OEM quantity, you get that compatibility and performance at the right price.

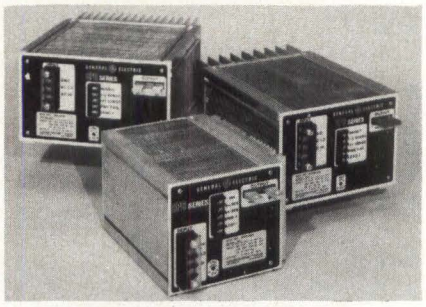
COLUMBIA
DATA PRODUCTS, INC.

Columbia Data Products, Inc.
8990 Route 108
Columbia, Maryland 21045
(301) 992-3400

CIRCLE 77 ON INQUIRY CARD

POWER SOURCES & PROTECTION

Switching power supplies allow side or bottom mounting in existing systems



A line of 300-, 400-, and 500-W switching power supplies, 6PS series switchers have a 50M-h MTBF. Offered by General Electric Co, Power Supply Operation, 705 Corporations Pk, Scotia, NY 12302, the convection cooled units are housed in compact, corrosion resistant enclosures and feature a single transistor forward converter design. Typical input ranges are 85 to 135 and 175 to 260 Vac, and typical output range is 4.5 to 6.3 Vdc.

Side or bottom mounting is allowed by adjustable mounting centers on the length axis. Each corner has a rail with two dovetail slots running the length of the unit. Mounting blocks supplied with each unit can be inserted into any two rails and fastened with set screws.

A minimum 75% efficiency rating is achieved through the use of 175 °C high efficiency Schottky rectifiers, 30-kHz operation, high speed power switching transistors, and a unique base drive circuit. Key components have been derated to increase reliability. Several voltage references provide load protection. Average and fast current limit circuits provide protection from long term and transient overload conditions, respectively.

A load current monitor allows users to determine actual output current without using complicated external shunts or ammeters. The units shut down if internal temperatures exceed a safe operating level. User adjustable overvoltage shuts the supply down if output voltages exceed 120% of rated. Terminals are provided for remote sensing, remote inhibit and remote programming capabilities. Single-unit prices range from $365 to $595. □

Circle 282 on Inquiry Card

SERPENTINE VERSION AVAILABLE

17+ MEGABYTE DISK BACKUP

CARTRIDGE TAPE DRIVE

The Model 400 and 401 MAXIDRIVE™ packs 17.2 megabytes on a 450 ft. data cartridge. The model 400 offers a standard, and the 401 incorporates a serpentine recording head. Read-after-write dual gap and selective erase are standard for both models. Unique, hard mounted motor. Rugged transport mechanism. Excellent power dissipation. High, 6400 bpi density. Fast, 192,000 bps transfer rate. Solid state BOT/EOT detection. Plug-in electronics. Plus more.

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CIRCLE 79 ON INQUIRY CARD

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"As OEMs discover the advantages of Quantum 8-inch Winchester drives, the demand grows daily. In Manufacturing, we're prepared to meet high-volume OEM commitments."

—Harold C. Medley, VP-Manufacturing, Quantum Corporation

A very manufacturable disk drive.

Quantum's 10, 20, 30 and 40-megabyte Q2000 disk drives were designed to be built in high volume at low cost.

Working as a team, Quantum design and manufacturing engineers created a drive that gives you better performance than the industry-standard Shugart SA1000, yet can be manufactured with simple, low-cost parts and fast, efficient production methods.

Low-cost, high-volume production.

To meet your low-cost, high-volume delivery requirements, we designed our manufacturing process as carefully as we designed the drive itself.

Our unique conveyorized "clean-air tunnel" combines the best of proven techniques for Winchester drive assembly. The drive is assembled on a conveyor line, so production is more efficient than with independent assembly stations. And the laminar-flow clean-air tunnel completely eliminates the need for a large, expensive "clean room," cutting production costs and increasing worker efficiency.

Specially-designed automated testing equipment thoroughly exercises each drive through all its functions, to assure highest quality while keeping labor costs down.

Every manufacturing operation is planned for easy, smooth expansion to meet growing OEM requirements.

In short, we're geared for low-cost, high-volume production of quality disk drives that we're proud to deliver to you.

Get to know Quantum now.

From manufacturing and engineering to management and customer service, Quantum has the very best people in the disk drive industry today. People who can help you plan an affordable growth path for your small computer systems.

For details on Quantum low-cost 8-inch Winchester drives, call Bob Teal, Quantum Corporation, 2150 Bering Drive, San Jose, CA 95131, phone (408) 262-1100.

QUANTUM *Driving down the cost of quality.*

CIRCLE 188 ON INQUIRY CARD

STR® technology for high data integrity. Three major tape formats for design flexibility.

We don't forget the OEM's needs.

The STR-810 digital recorder is designed for data logging, data acquisition and as a system loader. Using either the 3M DC-300A or DC-300XL cartridges, packing density is 1600 bpi, for respective data capacities of 2.3M bytes and 3.4M bytes per cartridge, using four tracks. Features include microprocessor-controlled tape movement and read/write electronics. For maximum versatility, interfaces include RS-232 and IEEE-488. Or, using control and status lines available, you can interface to specific microcomputers such as LSI-11 and 8080. EPI's optional ANSI X3.56 formatter, with NRZI or phase-encoded personality cards, turns the 810 into a plug-in component for industrial instrumentation and mini/microcomputer-interfaced peripheral markets. Price: $756 in quantities of 100. **STR-STREAM** is a high-speed, high-capacity version of the 810 designed for Winchester disc backup. Density is 6400 bpi for 17M bytes capacity per cartridge. Features include advanced head design, MFM formatting and compatibility with 8" or 14" discs.

CIRCLE 80 ON INQUIRY CARD

EPI's STR-610 is a compact, low cost digital recorder that's ideal for use with POS terminals, smart CRT terminals and as a general peripheral for mini/microcomputer-based systems. The 610's recording density is 800 bpi for a capacity of 168K bytes/track, using a two-track 3M DC-100 mini-cartridge. Formatting is ANSI Standard and interfacing is parallel, with a variety of options. Price: $280 in quantities of 1,000. **The STR-LINK III** is a high-speed (9600 baud), portable program loader that uses the STR-610's drive system and shares the same specifications. It is used as a field service tool for diagnostic work or as a peripheral in a mini/microcomputer system. STR-LINK III uses a serial RS-232 interface for data communications or data terminal applications, and it can be controlled through RS-232, ASCII control codes, or manually. Price: $1,615 in single quantity.

CIRCLE 81 ON INQUIRY CARD

STR-LINK II is EPI's proven medium-speed (1200 baud) universal portable program loader for programmable controllers and process control systems. Using a standard cassette, it features switch-selectable transmission modes for maximum flexibility. Price: $1,889 in single quantity.

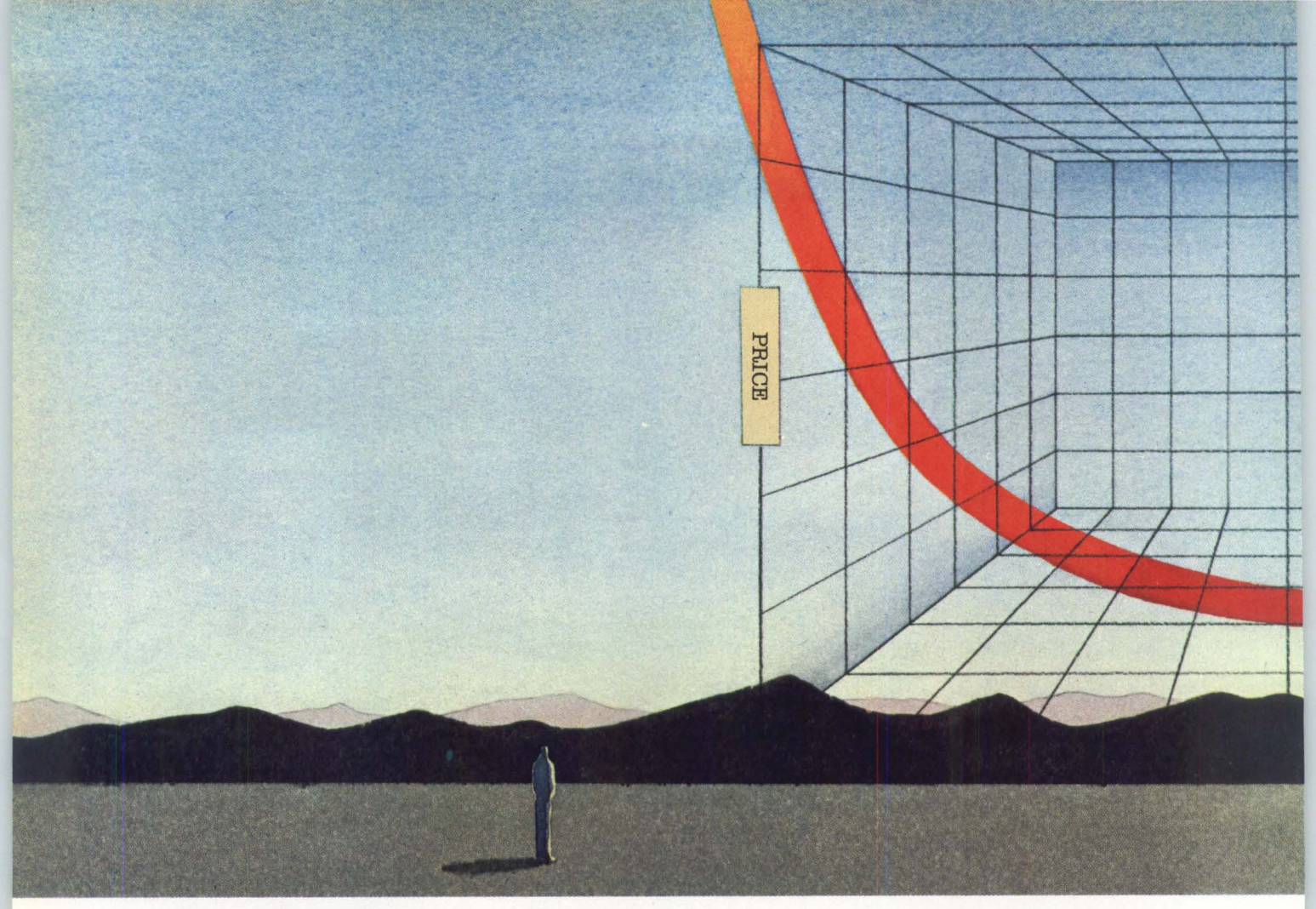
For maximum design freedom, proven reliability and high data integrity through Speed Tolerant Recording technology, remember EPI—the company that doesn't forget the OEM's needs. For more information, contact Electronic Processors Inc., P.O. Box 569, Englewood, Colorado 80110. Phone (303) 761-8540.

CIRCLE 82 ON INQUIRY CARD

EO/4

Let EPI remember for you.

ELECTRONIC PROCESSORS INCORPORATED



How to break the 8- without

It's not as hard as you think. Forget complex designs. And two-year waits.

All you do is get your hands on the Intel 8088.

And then leave the other 8-bit systems standing in your tracks. Without breaking the bank.

Because the 8088 gives you two to five times the performance of other 8-bit processors. For a whole lot less.

In fact, at $14.10 for 100 pieces, 75% less than last year. (Because high volume shipments are already pushing the 8088 down a super fast price curve.)

And about 20% less than you'd pay for a Z80 or MC6809 system.

For some simple reasons.

The 8088 runs at full speed with slower speed memories than you need for other 8-bit microprocessors.

And about 1/3 less memory at that. Thanks to its powerful instruction set that helps you reduce the size of assembly language programs.

Which together with the 8088's library of high level software (Pascal, CP/M, Basic and Fortran) should help you cut the other part of system costs. The part that's larger than hardware.

But even though you're paying less, you'll be getting more.

Like 1-megabyte addressing.

Extra power for 16-bit number crunching.

And faster string processing.

Fact is, our recent benchmarks show the 8088 runs circles around a Z80A, Z80B or MC6809 when it comes to terminal and small business applications.

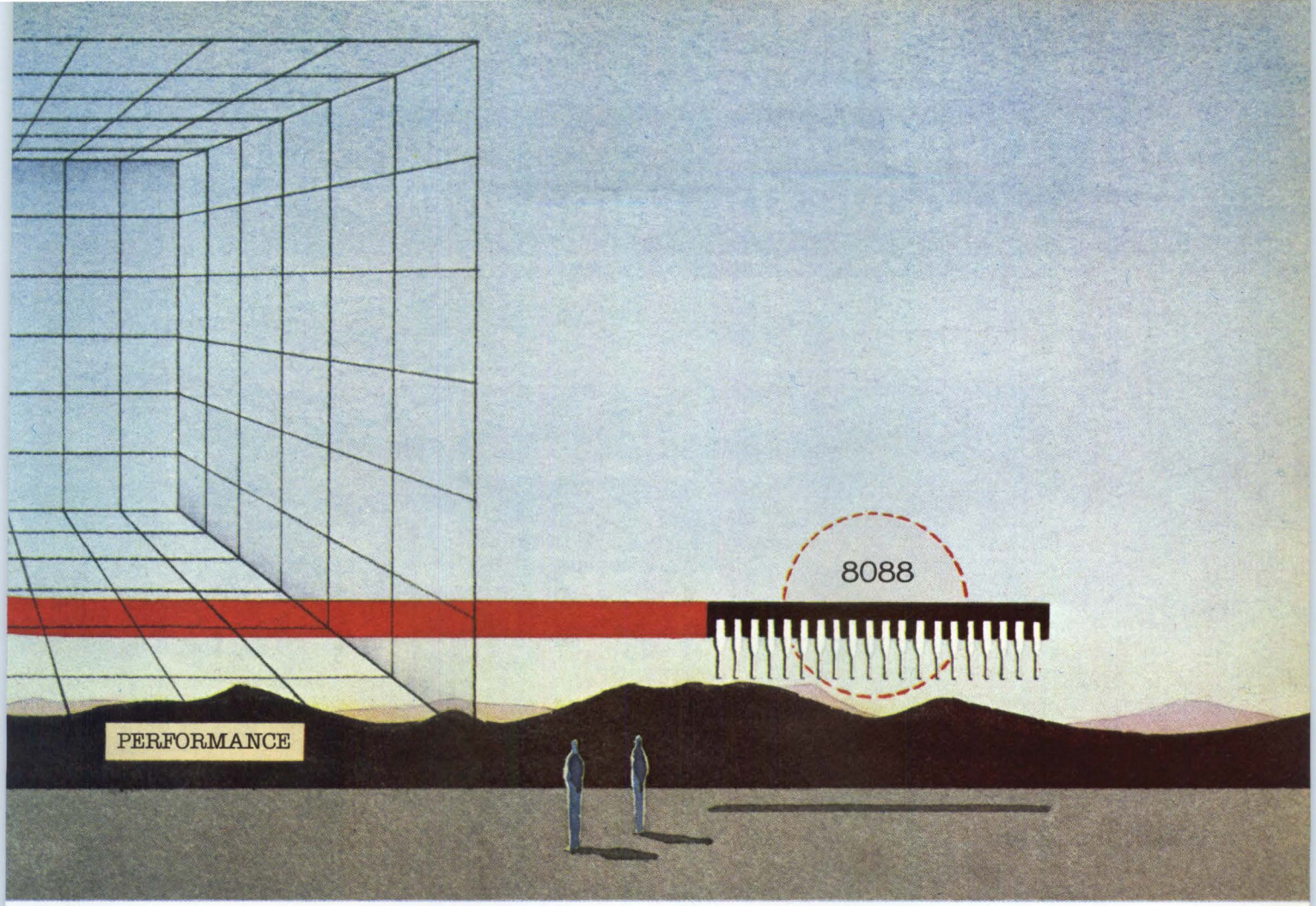
But don't think you have to stop there. With any of our iAPX 88 multiprocessor configurations, you can give performance an added boost—and still keep the cost and simplicity of an 8-bit system.

For 100 times the throughput on number crunching, just choose the iAPX 88/20 system.

Relative Performance

	Intel 8088 (5 MHz)	*Zilog Z80B (6 MHz)*	*Motorola MC6809 (2MHz)*
Computer Graphics	*1.0*	*0.1*	*0.05*
16-bit Multiply	*1.0*	*0.17*	*0.5*
Block Move	*1.0*	*0.75*	*0.49*

Full details of these benchmarks available in the iAPX 88 Book.



bit performance barrier going broke.

It combines the power of the 8088 with our 8087 numeric coprocessor.

Or if you're worried about getting bound up in I/O. Don't. Select our iAPX 88/11 system that speeds I/O processing three to five times by putting an 8088 together with an 8089 I/O processor.

Then there's the fact if you ever decide to make the jump to 16 bits, you won't have to jump. The 8088 is 100% software compatible with our 8086.

Because we don't think you should have to sell out your future to get the best deal on price/performance today.

And to put you in the right frame of mind, we're ready to make you an offer.

Just clip this coupon and send it with $5 to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. (Or call 408-987-8080.)

We'll send you the book on how to design iAPX 88 systems and a coupon good for one free 8088.

Everything you need to start breaking through barriers—without going broke.

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intel® delivers solutions

CD9

CIRCLE 184 ON INQUIRY CARD

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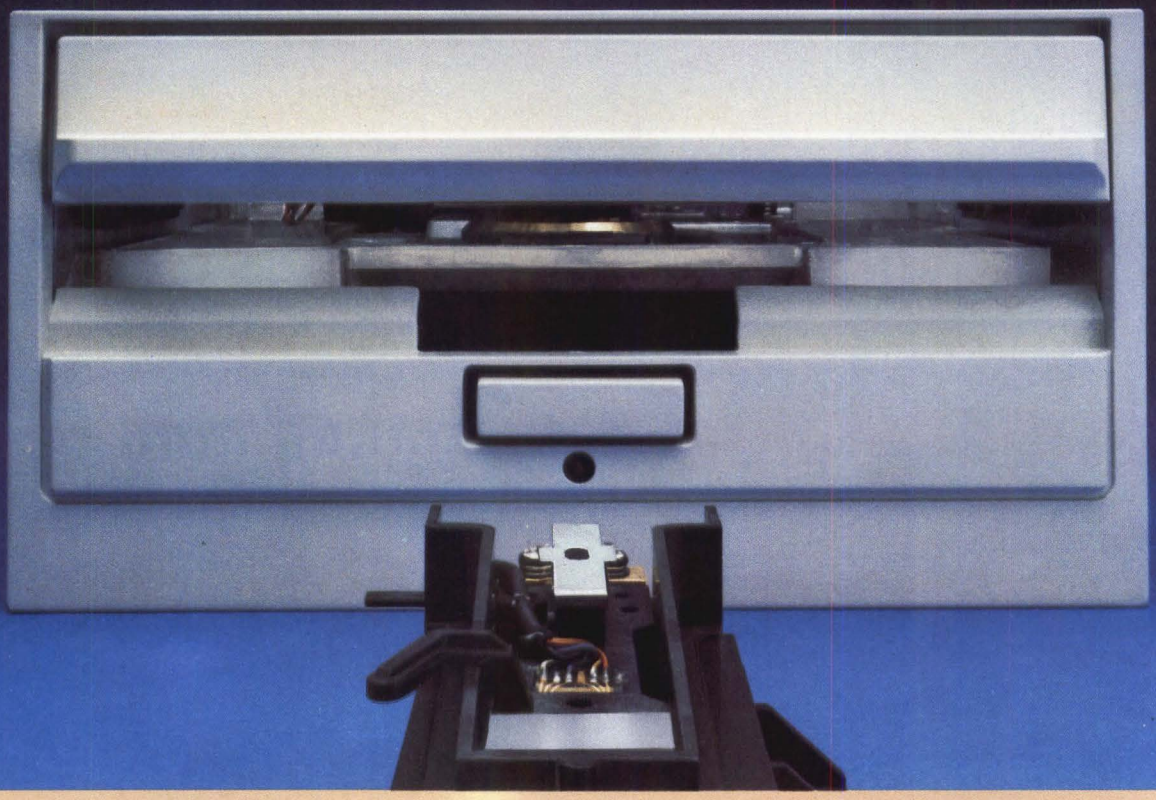

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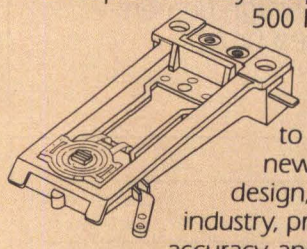

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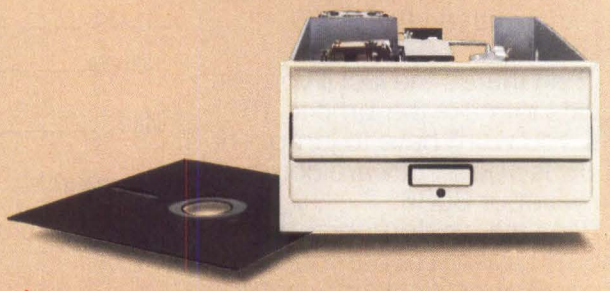

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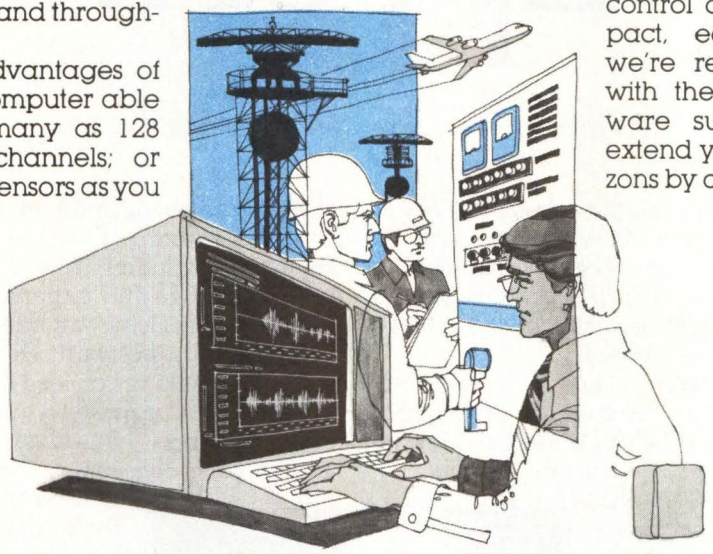

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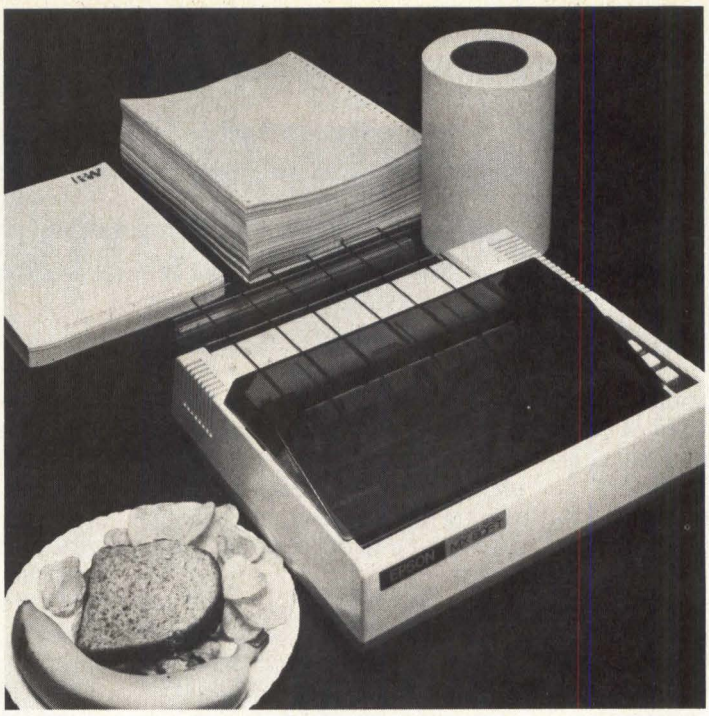
The new MX-80 F/T. You can feed it anything. Almost.



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This is Epson's newest and most versatile printer —the MX-80 F/T. It does everything the famous MX-80 does, and since it accepts both friction and tractor-feed paper, it prints on almost anything. So for many OEM uses, this printer may be the best printer you can buy.

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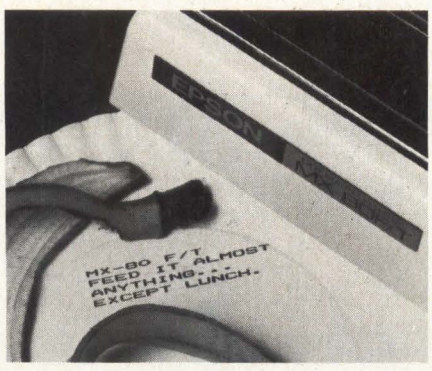
It prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. And since all Epson printers are known for reliability— and the MX-80 F/T is no exception—it prints and prints and prints. You can expect 100,000,000 characters from the print head. And when the head finally wears out, it's so inexpensive you can just throw it away. To put in the new one takes only one hand and a few seconds of time. The MX-80 F/T is compact, weighs only 15 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor.

But here's the best part. The MX-80 F/T prints on just about anything you feed it. It has both a friction and a tractor-type pin-feed mechanism. So it prints on forms, labels, letterheads, roll or continuous fan-fold computer paper. Or even paper plates.



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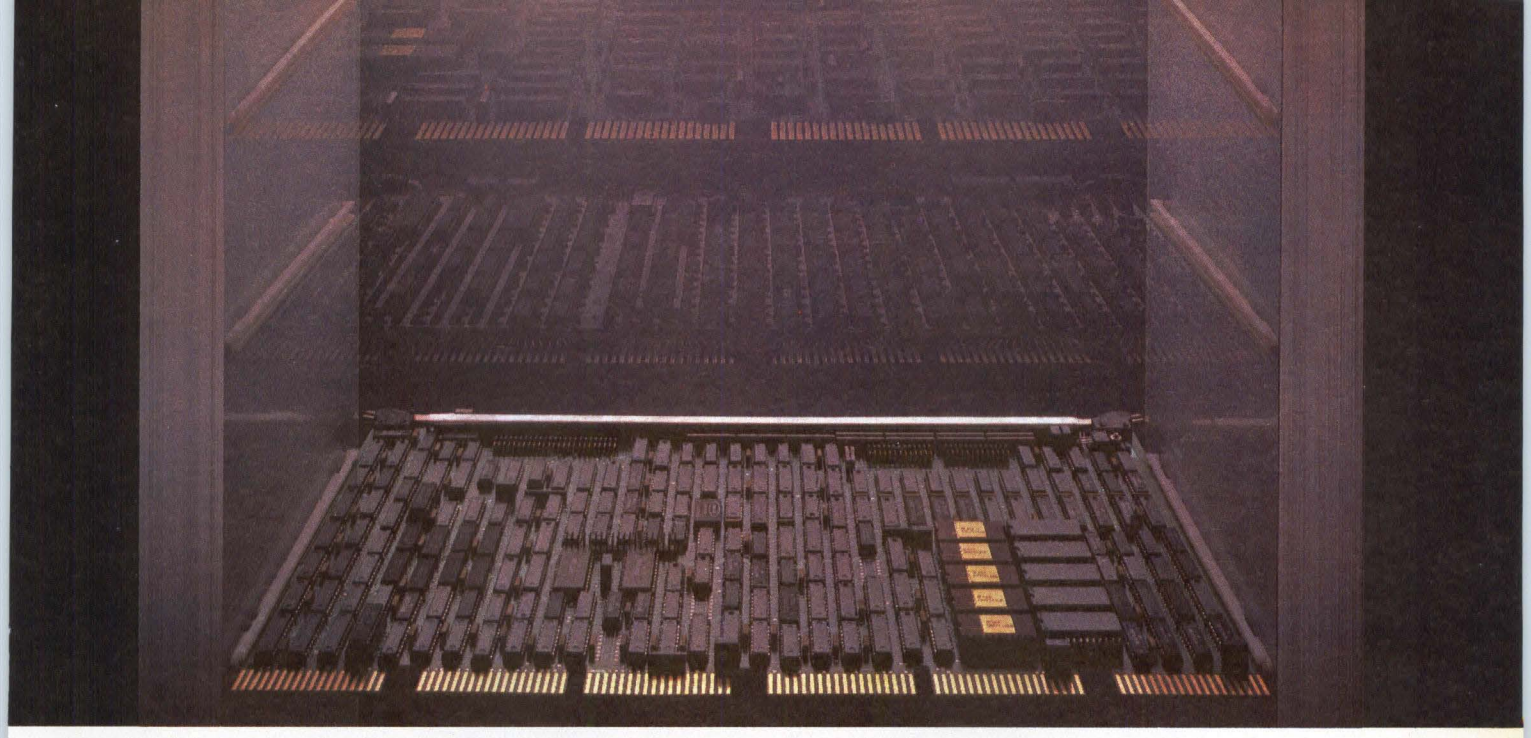

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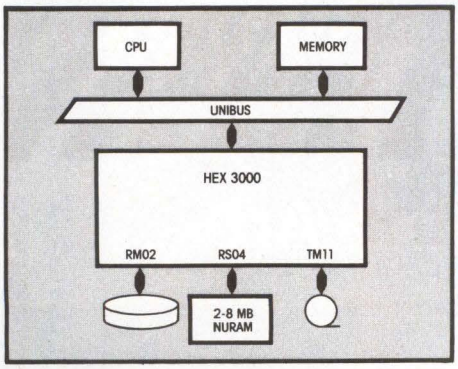

Cuts costs in the factory and in the field. By using one board to do the work of three or more—with no degradation—you save a bundle in a number of ways.

Your most immediate savings is the elimination of two comparably priced controller boards. But farther down the line, the HEX 3000's upgrade flexibility lets you expand a configuration less expensively because you don't necessarily need to buy additional boards or a larger chassis.

This also means your spares inventory costs are cut way back. Not only in the factory, but in the field as well.

And at the same time, the HEX 3000 increases your system's reliability because it uses far fewer ICs to do the whole job (198 in all).

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The XPU's generalized intelligence emulates the transfer processing logic of DEC's RM02 disk, TU10 tape and RS04 fixed head disk controllers. So it's fully hardware and software compatible with any UNIBUS system.

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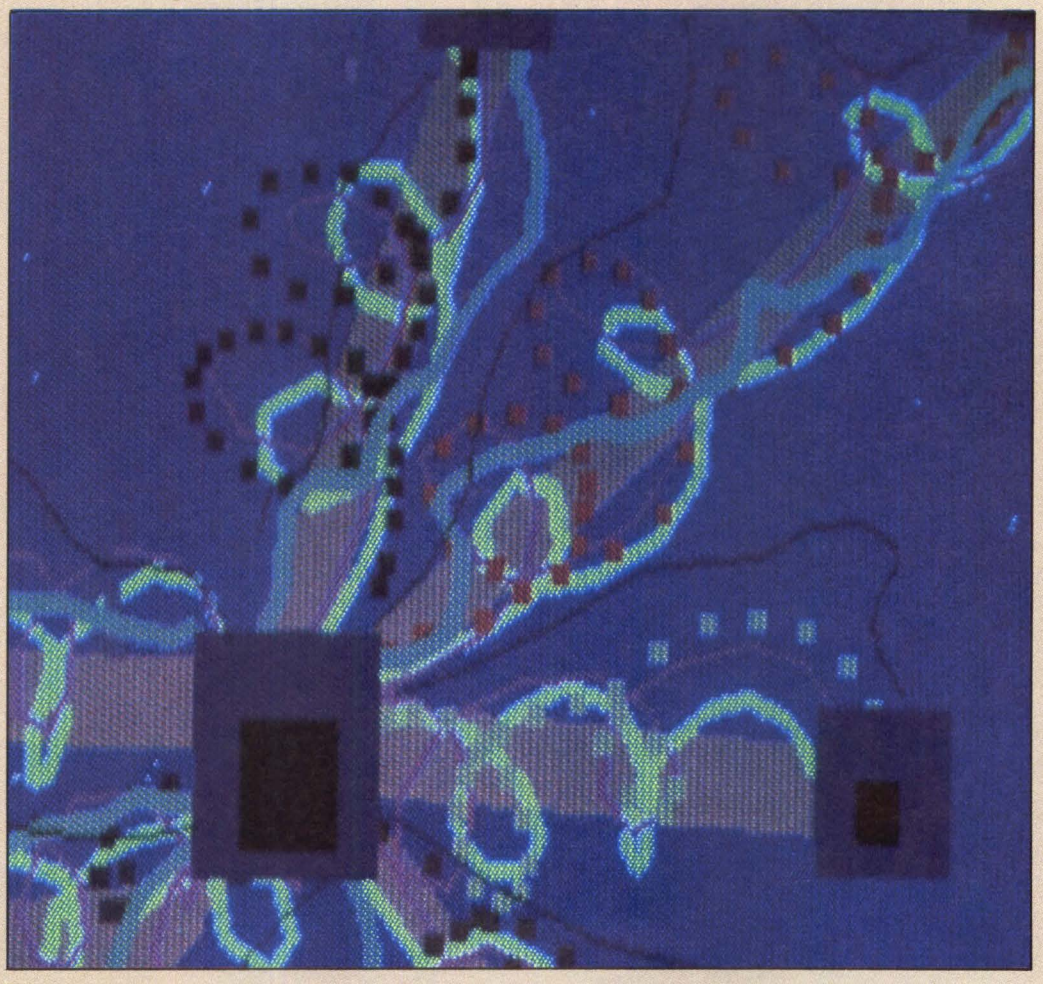

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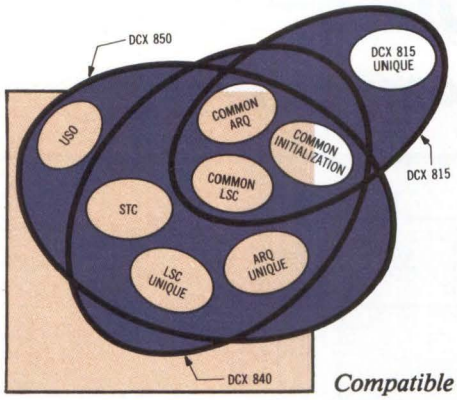

Compatible software modules. **156**

Special report on data communications

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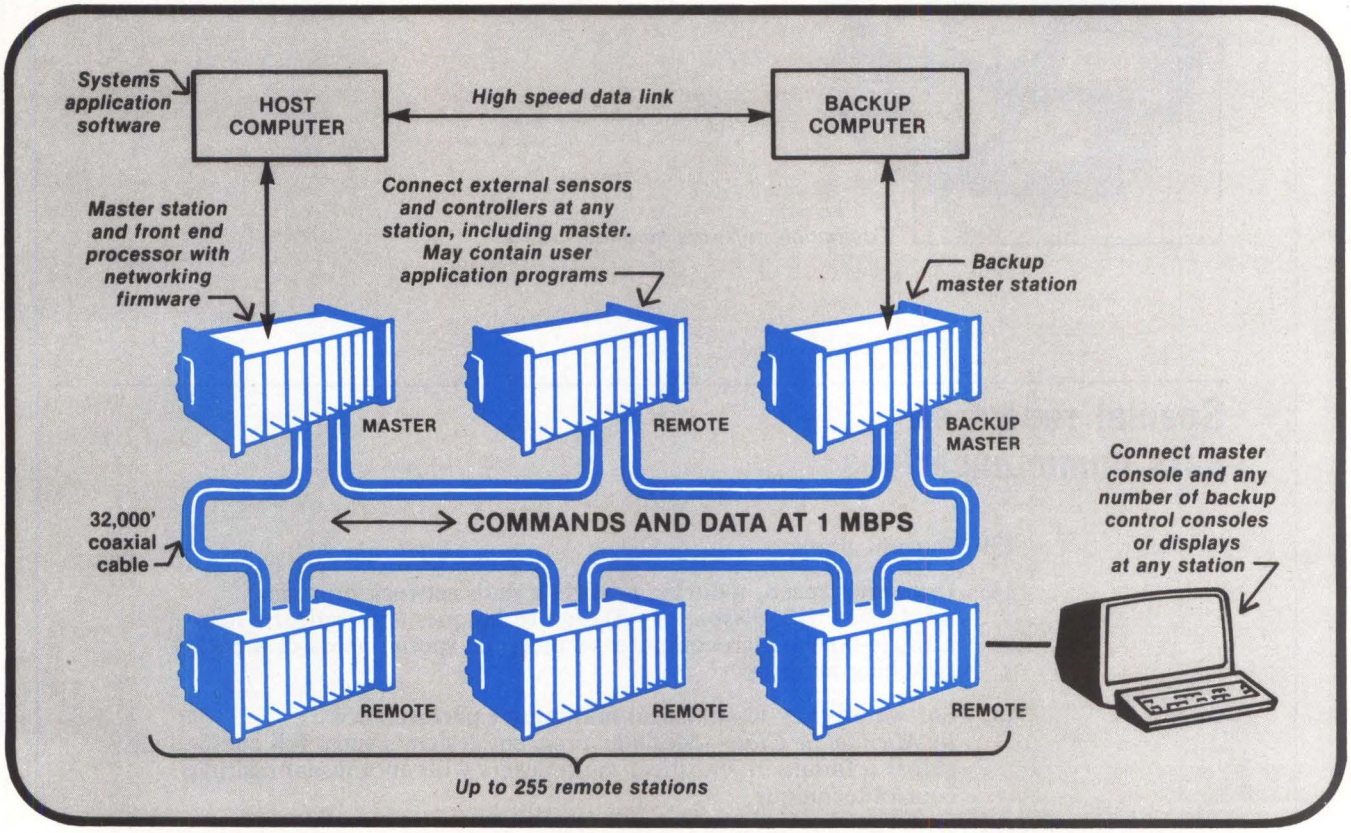

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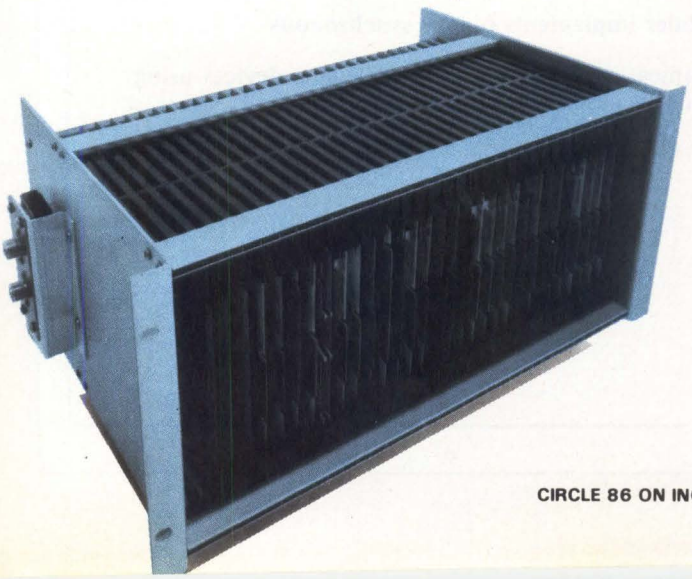

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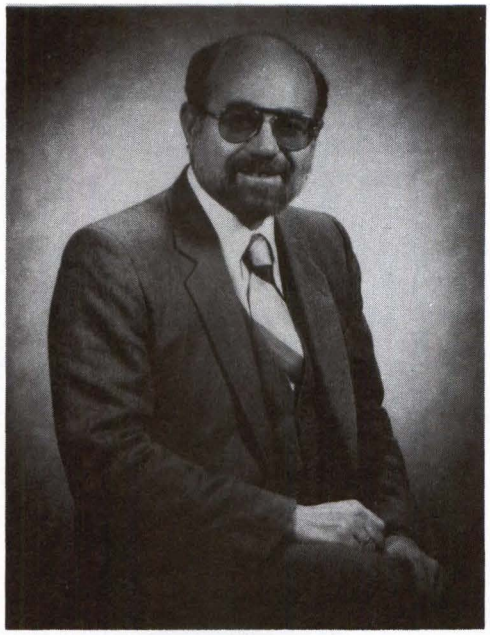
INTRODUCTION



An admirable aspect of our business is the speed with which the computing industry has advanced. The steps have included not only the 25-year march from vacuum tube logic to present-day large scale integrations, but also the astounding number of discrete and complex special disciplines that have so quickly evolved. The day of the computer generalist is fast disappearing; both hardware and software specialists now require concentrated knowledge simply to keep pace with the industry.

Data Communications, September's special theme, is certainly one of those rapidly evolving specialties. Although a specialized field of interest, it is almost as broad in scope as was the entire computing industry during its middle years. Now we are approaching the ability to link discrete computing systems into vast networks of computing power, and the microcosmic view of communications offers possibilities for the internal architecture of tomorrow's discrete systems. With chip complexity and board level sophistication increasing, each subsystem is endowed with greater intelligence to enhance the total system. As protocol and error detection/correction hardware dwindle to the single-chip level, the urge to communicate between subsystem elements using a single pair of wires will become just as great as the urge to communicate between systems on a global scale.

Look to data communications technology to filter its benefits into all of the other digital systems disciplines.

Saul B. Dinman
Editor in Chief

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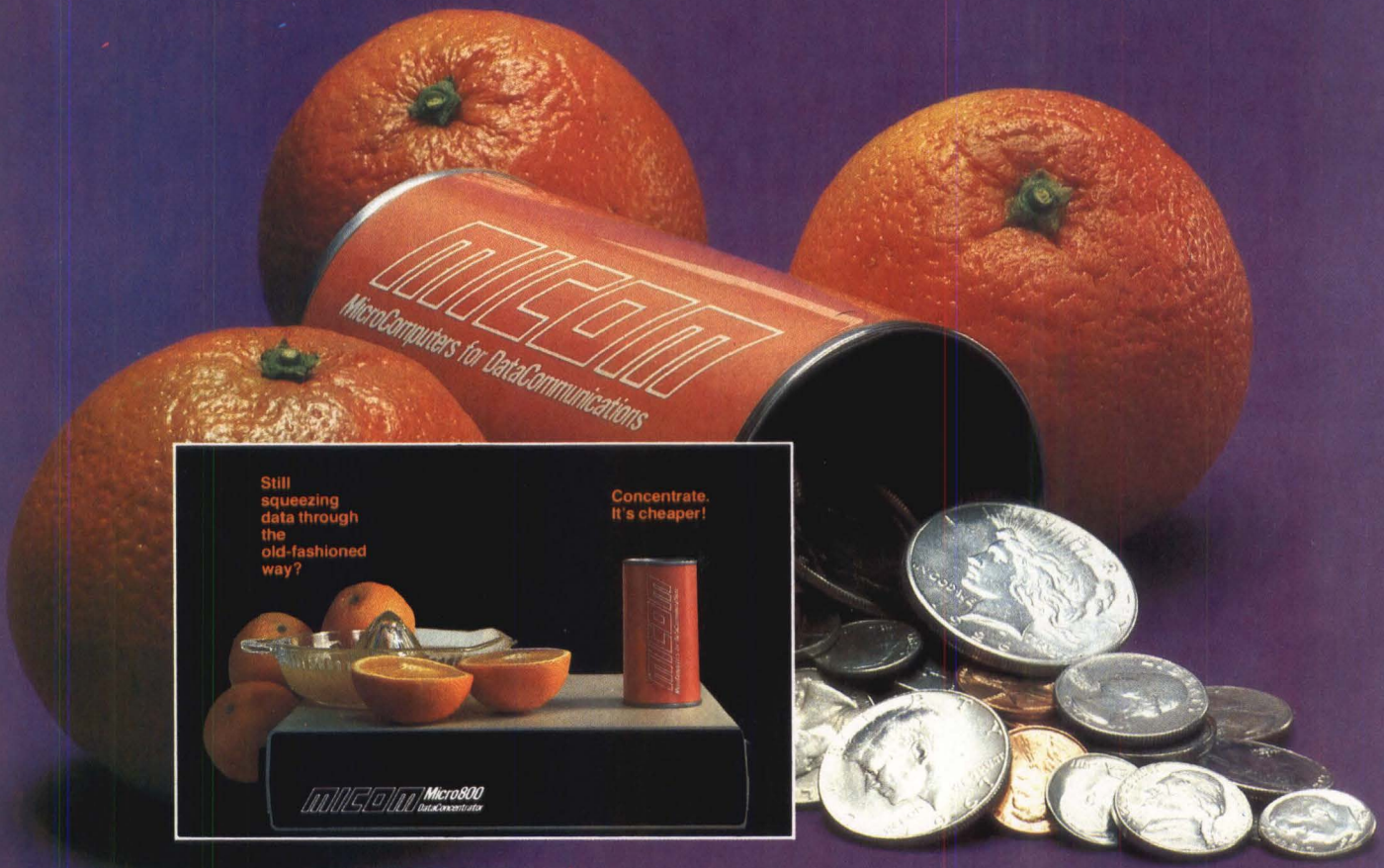

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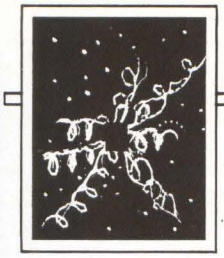

Design techniques and tradeoffs help a single-board microcomputer to meet the special needs of a packet switching network

Increasing speed, reducing costs in a data network processor

Digital communication networks place unique demands on switching processors. Most computers available today do not adequately address these demands. Motivated by the need to upgrade and expand an existing PDP-11 based system, the project reviewed here describes the design of a digital communications processor for a packet switched network. The design process resulted in an MC68000 based multiwire processor board.

Besides achieving increased throughput with reduced cost, the system is compatible with existing system interfaces and software. It fills a significant gap in computer hardware available to communications network designers. A prototype of the computer board discussed here has been completed; it has passed all diagnostic tests and soon will be evaluated in actual service.

Description of the network environment

A digital data network consists of processors (nodes) and communications lines (links) that connect terminals to host computers. Nodes can have from 10 to 100 terminals and 2 to 4 links, with terminals running as fast as 2400 baud and links as fast as 56k baud (Fig 1). A node can also support unit record equipment, such as line printers and card readers. Some nodes also support

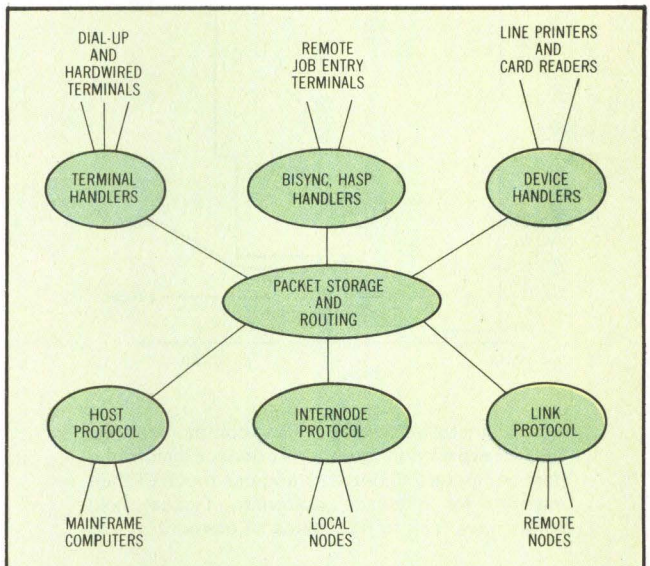

Fig 1 Basic node structure illustrates major functional partitions. In smaller nodes, all circled functions are in software on single CPU, whereas in larger nodes they may be distributed among multiple CPUs or partially implemented in hardware

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Acknowledgment

The author wishes to thank Doug Chinnock at CompuServe for providing the data used in the accompanying figures, as well as for many helpful suggestions.

multiple synchronous protocols, such as DDCMP and CCITT X.25. While most network sites do not have to support all of the preceding functions at once, today's trend is toward more and faster interconnections, which requires either more or larger network nodes to handle the traffic.

In addition to the equipment it must support, the communications processor must also supply considerable intelligence. Terminal connections require special processing to match the characteristics of particular terminals. It is also desirable to provide character echoing and translation facilities in the node. Systems designers envision additional functions in future networks, such as screen editing support.

The principal advantage of a digital data communications system is the error-free transmission achieved through store and forward techniques. Complicated protocols used for error detection and retransmission are handled by the node. Modern networks use packet switching to concentrate and route the data. Packets can be dynamically re-routed around failed portions of the network, increasing overall reliability.

Implementation of these features requires a large program. Program code and data buffer size combined have been growing steadily, and now exceed the 64k-byte memory space provided by most minicomputers (Fig 2). Although processing requirements often

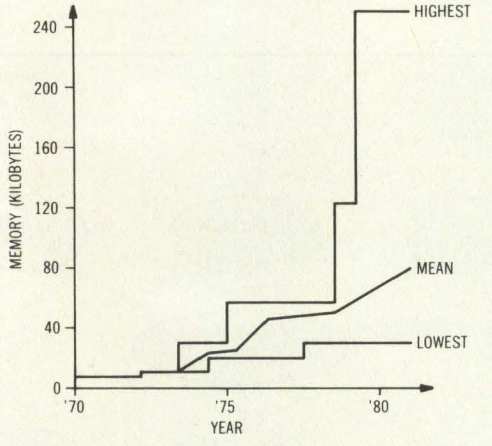

Fig 2 Installed memory on communications CPUs. Largest configurations connect mainframe host computers to network and use much of their memory for message buffering. Typical field nodes have 32k to 64k bytes of memory

stretch the limits of minicomputers, cost and size considerations do not allow the use of mainframes. In fact, many communications nodes are used in offices in which small size and quiet operation are essential.

Network demands on processors

The processor must be fast to serve all the devices and system functions required of a node. Link processing, in

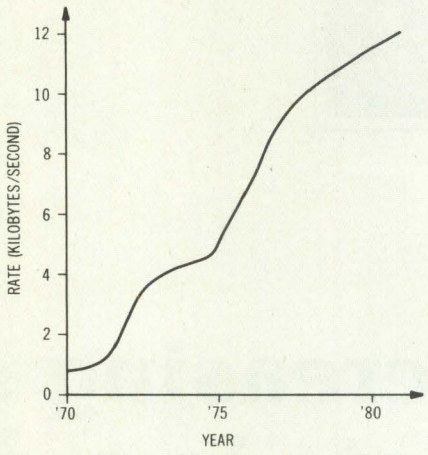

Fig 3 Data throughput of nodes (total peak data rate). Jumps in throughput correspond to major technical advances, such as development of 9600-baud modems. Emergence of 1200-baud dial-up modems and 56k-baud service will produce another leap in throughput

particular, must be fast enough to avoid overruns. A node must service all possible line interrupts within a character time. It is also necessary that it be able to accept all characters received on the asynchronous input lines. In practice, even faster processing is required to perform packet routing and other functions, though these are not as time critical. The capacity of present PDP-11/40 based nodes is limited to about four 9600-baud synchronous links, which the increasing throughput requirements will soon exceed (Fig 3).

Since memory bandwidth is the principal limiting factor in communications processing, it would seem that a memory cache might help. However, caching depends on the principle of program locality; that is, the most recently used piece of program or data is most likely to be the next piece used. Mathematical programs, such as matrix multiplication, demonstrate high degrees of locality. Unfortunately, typical digital communications tasks do not. Since a node is driven by random external interrupts, and the processing required for individual events is small, the most recently accessed instruction is not likely to be accessed in the immediate future. The situation is even worse for data packets, which are usually accessed only once after they are stored. Adding a cache to an existing PDP-11 system results in only about a 40% hit ratio, for a speed improvement of 20%.

Lack of program locality also makes standard memory extension methods inefficient. Individual processes execute for only a short period of time, necessitating frequent context switches. Context switching is fairly time-consuming, and requires a supervisor trap and the modification of mapping registers. The resulting software overhead wastes nearly 15% of available

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processing time, and the PDP-11's memory mapping hardware adds another 10%. By this time, the node is so bogged down that the additional memory cannot be used efficiently.

A memory management unit for the PDP-11/40 was designed in an attempt to increase memory bandwidth. The unit requires less time for mapping and less software overhead than other methods, but is also less flexible and works only on one computer model. While it has allowed some memory extension, acceptable partitions in the program are now difficult to find, and the best solution appears to be a larger intrinsic address space.

Network processing software now available is written for the PDP-11. A processor added to the network should have an instruction set similar to that of the PDP-11 to allow machine translation of the software. Many existing nodes use UNIBUS® and Q-bus backplanes. A processor that can plug into one or the other of their cabinets will allow easy upgrading to the new system. It will also avoid redesign of the custom interfaces on either machine. Using existing interfaces simplifies software conversion by minimizing device driver changes.

A final consideration for the new system is reliability. Communications equipment is often at remote sites where maintenance is difficult and costly. As with any utility, long periods of downtime can be disastrous.

A system to meet network processing requirements

The first step in designing a new system was to evaluate what was commercially available. From a software point of view, a new PDP-11 would have been best, but the emphasis in larger models is on timesharing and mathematical usage. Their costs are not justified by the improvement in basic computational speed. Other processors were considered, especially 32-bit models, but they either were unavailable in small inexpensive sizes or demanded too great an effort for reprogramming.

Multiprocessing is another way of gaining increased speed and memory capacity with existing computers. Node program structure permits ready distribution of tasks among several processors. The Advanced Research Projects Agency (ARPA) network[1] uses such a multiprocessor for nodes in the network, with additional software to reconfigure around failed processors. However, the extra interconnection hardware and cabinet space required tend to price such configurations out of range for a medium size network. Furthermore, the complex software needed to overcome failed modules would require major rewriting of the existing program. Therefore, multiprocessing has been ruled out for the time being, though it may be necessary in the future as communications demands increase.

Benefits of using an MC68000

New 16-bit microprocessors are more powerful than some minicomputers and are relatively inexpensive. Of various processors available, only the MC68000 could directly address an extended memory space.[2] It was also nearly twice as fast as the processors it could replace and had an instruction set with many similarities.

One major feature of the MC68000 is the ease of machine translation of software for it. It has architectural similarities with the PDP-11 that allow many instructions to be translated one for one. Although some instructions require lengthy sequences for emulation, an analysis of present software has shown that these are seldom used. In some cases, human intervention is required to generate reasonable programs, but in nearly 99% of actual instructions it is not.

Advantages of using a Q-bus

A PDP-11 (Q-bus) type input/output (I/O) system is preferable for several reasons. It allows use of existing cabinets, and does not require purchase or design of new peripherals. Only the central processing unit (CPU) needs to be replaced in an upgrade from the PDP-11 to the new CPU. Furthermore, the I/O driver program sections are easier to translate, since only the instructions change and not the devices. An ideal upgrade involves only the exchange of CPUs. Of course, the converted program will have to be loaded into the new processor.

Since the Q-bus is designed to handle a single-board CPU, it facilitates the upgrade more than does the UNIBUS. Its disadvantage, that it is considerably slower,[3] can be overcome by incorporating frequently accessed memory (ie, program memory) onto the CPU board itself. The rapidly growing availability of peripherals for the Q-bus—at a cost considerably below that for UNIBUS peripherals—further biases the decision in the direction of the Q-bus.

Advantages of a single-board solution

The principal difficulty, with either I/O bus, is the long memory access time. Providing all memory on the

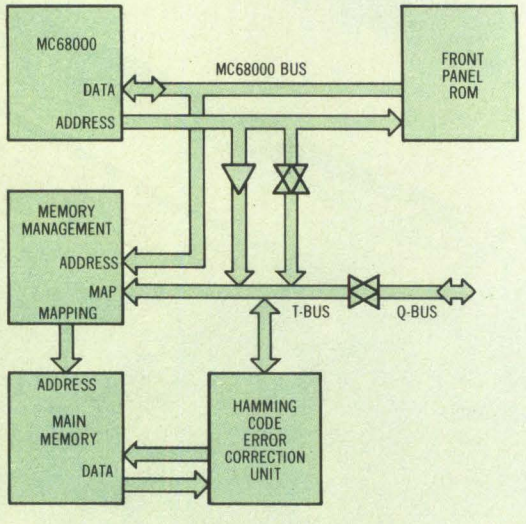

Fig 4 Principal data paths of MC68000. T-bus features multiplexed address and data, simplifying the Q-bus interface. All 6 possible data transfers among MC68000, main memory, and Q-bus are supported

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Q-bus would reduce throughput by nearly two-thirds. As noted earlier, caching is ineffective for communication node applications. Other options, such as a dual Q-bus with separate memory banks for odd and even words, are too clumsy.

The 64k dynamic random access memory (RAM) provides the solution by allowing adequate memory to be placed on the same board as the CPU, resulting in minimal access delays. Thus, the MC68000 is able to run at full speed, yielding a throughput nearly double that of a PDP-11/40. Additionally, a full 256k bytes of high speed memory is provided—four times the amount available with earlier systems. High density multilayer or multiwire technology can fit the large number of chips required for all these features onto a single quad-sized board. Automated layout, extremely high density, and good noise immunity recommend multiwire technology for the present application. For the production of small quantities, it is also the cheaper of the two. Fig 4 shows the multiwired arrangement of microprocessor, memory, and Q-bus on a standard quad-sized board.

Final solution

Onboard memory features 22-bit Hamming error check and correct (ECC) using large scale integration chips. The ECC system can correct and rewrite data within one additional system clock cycle. With 64k RAMs, the board can contain up to 256k bytes of memory.

A simple memory management scheme facilitates future network enhancements. The mapping function is overlapped with initial dynamic RAM addressing so that its delay is completely hidden. While this results in fairly high relocation granularity, it still permits the addition of utility packages, such as screen editor support, to the network. Soon local utility processing will be added to nodes.

The Q-bus interface also permits future growth. The full 256k-byte address space of the bus is available to the processor, allowing additional, though slower, memory to be added. Direct memory access from Q-bus to the onboard RAM permits access from intelligent peripherals or other processors. Thus, an elaborate store and forward communications system can be designed using this board.

Results

More than 5000 instructions of PDP-11 source code were successfully translated into working MC68000 code in approximately four months. A set of macros allowed the MC68000 assembler to process PDP-11 source code directly. In this way, over 95% of the instructions, tables, and storage was translated. The remaining cases, which were attributed mostly to the different byte sequencing, were handled by adding to the source code macros that translate one way for PDP-11s and another way for MC68000s. With this technique, the modified

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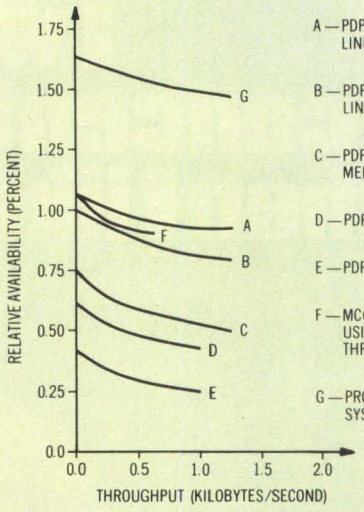

Fig 5 Node processor availability relative to idle PDP-11/40. Throughput measurements for representative CPU configurations were made on systems with one link

PDP-11 source was assembled directly into MC68000 machine code without human intervention, thus requiring maintenance of only one copy of the program.

Although the translated PDP-11 code does not run as efficiently as true MC68000 code and takes up more room, it performs surprisingly well. In tests on an early prototype system, code size expanded approximately 10%, while execution speed was still at least 50% faster than on a PDP-11/40. (See Fig 5.) In the future, this problem could be solved by switching to a high level language such as C or BLISS, which can be compiled easily for either machine.

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Until recently, Andrew Wilson has been a design engineer with CompuServe, working with mainframe computers and digital networks. He is presently attending Carnegie-Mellon University in pursuit of a PhD in computer engineering. He received a BA from Pomona College and an MSEE from the University of Arizona.

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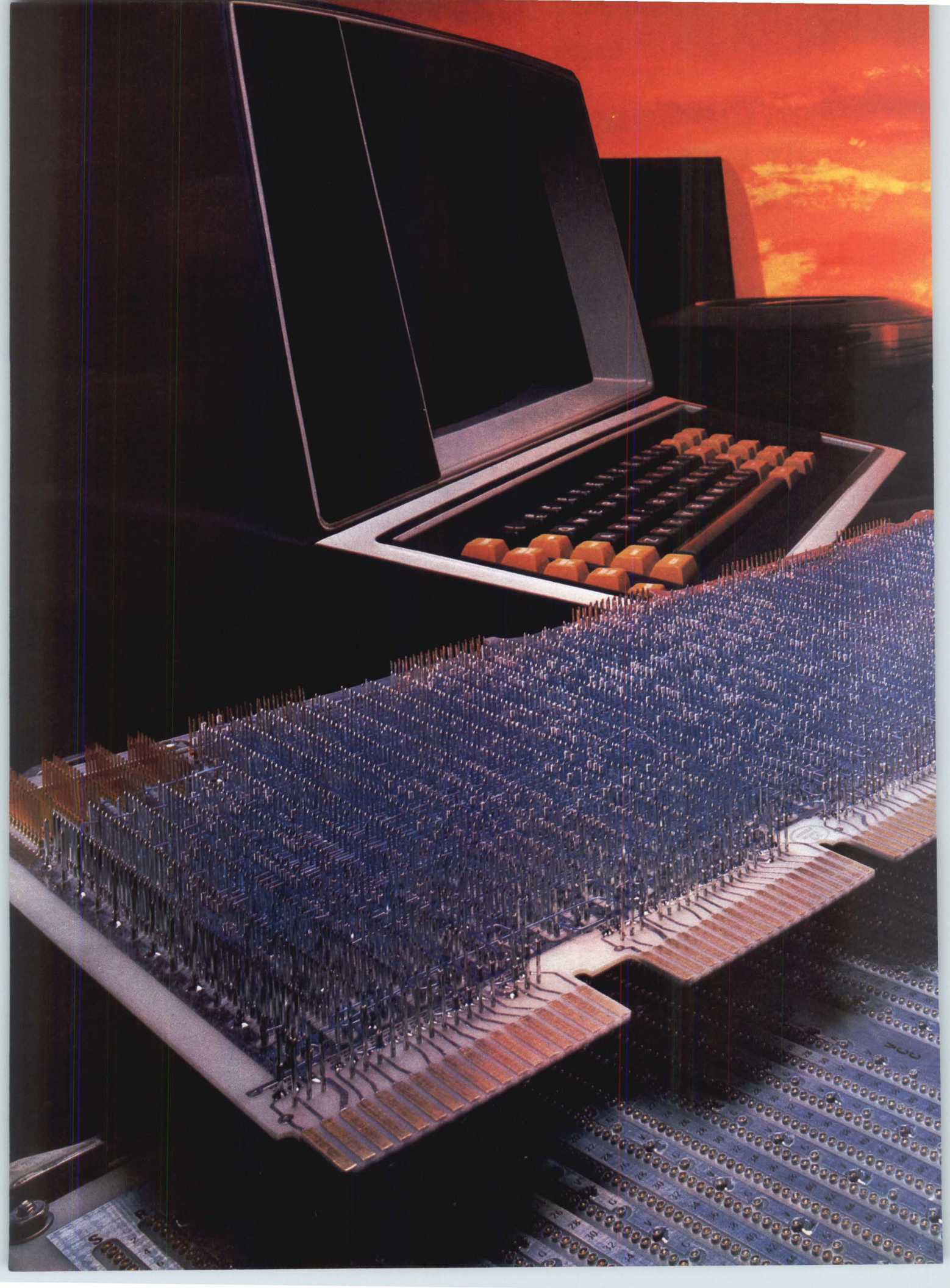

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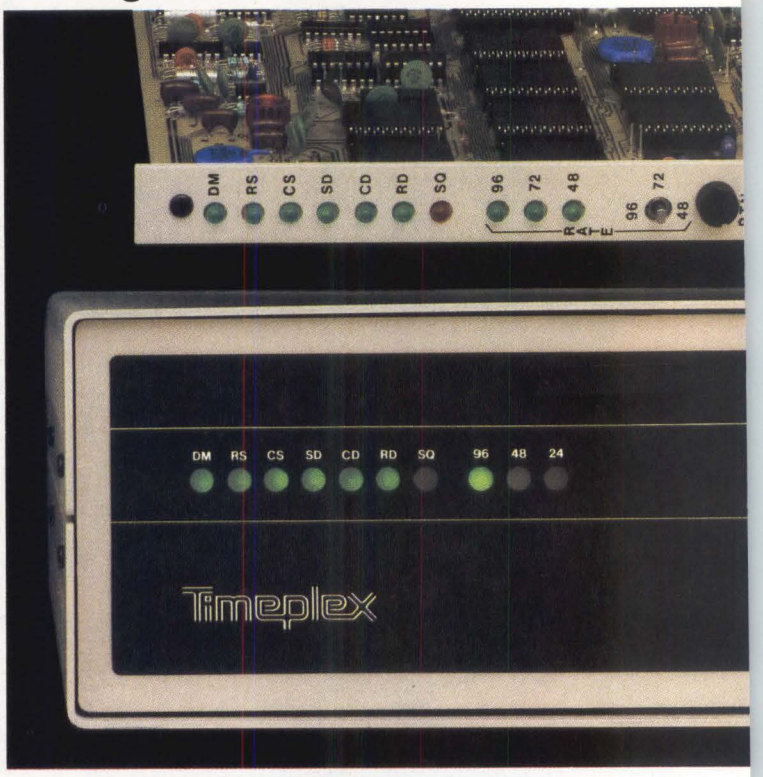

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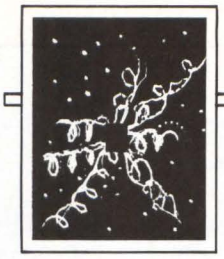

Modular program design ensures full compatibility across a family of statistical multiplexers with an unusual realtime control technique

Software is key to statistical multiplexer performance

Statistical multiplexers are used to combine many asynchronous channels into one composite, synchronous line for transmission by modem over the telephone network. Their use reduces line costs and protects channel data from network-induced errors. Originally, every terminal was linked to its host computer by a modem, with one telephone channel per terminal. The next step up from that primitive network was the time division multiplexer, which could multiplex N asynchronous channels, each operating at M bits/s, into one synchronous channel at NM bits/s. Statistical multiplexers developed because terminals are usually inactive, and, as a result, time division multiplexers usually transmit only idling information for most of the channels. Statistical multiplexers achieve a 2:1 compaction ratio by transmitting only data from active terminals.

Microprocessors manage compacted data flow in a statistical multiplexer, and memory is used to buffer the data. Character buffering is needed because there will be short periods when all terminals are active and the input data rate exceeds line capacity. In addition, throughput will sometimes fall below the optimal, MN/2 rate when line errors cause retransmission of frames. Excess characters are stored until the traffic subsides in either case.

Statistical multiplexers are software-intensive products, whereas modems are hardware-intensive. Software often needs to be changed because bugs are found, new features are needed, or new applications are developed. Therefore, software used at the top of a product line should be compatible with software at the bottom of the product line since, without compatibility, the entire product software will be cumbersome and costly both to develop and to maintain.

An example of a low cost statistical multiplexer that is fully software compatible with top-of-the-line models is the RIXON DCX 815 used in point to point multiplexing. Like most other low cost units, the 815 has a capacity of either four or eight channels and a buffer size of 5k bytes. Other statistical multiplexers that compete in the low cost marketplace may have slightly different features, but all maintain these features through software control.

At the top of a statistical multiplexer product line, multinode network handlers like the DCX 840 have many outgoing composite synchronous links as well as many asynchronous low speed channels. These large devices are equipped with a mapping capability that directs the low speed channels to the correct composite link. While low cost statistical multiplexers automatically map one channel at one site to another channel at another site, the large units interconnect channels from one site to any other site dynamically in response to keyboard commands.

Mapping ability is analogous to a telephone exchange, where operators connect one circuit to another with patch cords. Of course, in the DCX 840, digital electronics does the patching in response to keyboard commands. In contrast to mapping, packet switching handles data like mail, with the node sites behaving like

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mailboxes: data pass from site to site until the destination address coincides with the site address. An advanced version of the DCX 840, the DCX 850 contains a switching option to give the network user the freedom to select his end-port connection rather than have the network map entirely preassigned.

Point to point statistical multiplexers use one microprocessor to implement full duplex protocol for the synchronous link, to buffer characters across low speed channels, and to receive or transmit. Larger units perform the same tasks but use a separate circuit board, each with its own microprocessor, for each task. The multiplexer must also take care of the system test and configuration mapping, which requires yet another microprocessor based card. Various manufacturers subdivide their units differently, but all intend to partition the system among modular software tasks. Thus, a customer can specify all multiplexing parameters to suit his needs. For example, he can designate the number of low speed ports and composite links, thereby purchasing no unnecessary capacity.

Although diverse, the DCX statistical multiplexer line uses common software (Fig 1). Any change to DCX series software is easily incorporated into each member of the product line. For example, if a change to the full duplex protocol becomes necessary, the "common ARQ (automatic repeat request)" module is altered. That change is then easy to integrate into the DCX 815, 840, and 850 because "common ARQ" is part of their core software. Unique software modules contain the unique addresses and instructions needed for interfacing the core software to the multiplexer hardware.

A task control block (TCB) concept makes it possible to use the same programs in large and small systems while changing only the addresses of the peripherals in the unique program segments. TCBs are blocks of data and instructions that manage a program by interfacing it with other programs and TCBs. A TCB consists of a priority level, a link to the next (lower priority) TCB, an event list to keep track of all events that must occur before the TCB program can run, and an execution address in the program. It is not part of a program; instead, it is in control when its program actually runs. The executive uses TCBs to pull programs into operation and to suspend them when required.

In Fig 2, the executive has its top TCB pointer set to address 1000; however, the top priority task's program is not running because its event list has not been satisfied. Instead, the third program is running because its event list was satisfied when the executive sought a task to run. If the third program eventually writes to a disc (a lengthy operation), it enters a wait state and its execution address is stored in its TCB. The program remains passive, in this case, until the write to disc has been accomplished.

Each TCB controls a program that performs a particular task. When a program reaches the point where it has no more work to do and must wait for an event, its TCB releases control to the next lower priority TCB. The lowest priority TCB releases control back to the top of the chain, closing the loop. For example, three programs perform the ARQ function: a receive task, a transmit task, and a base load task (to assemble and disassemble frames). The receive task enters a wait state when no input data are available for processing. This transfers control to the transmit task, which defers to the base load task, in turn, when there are no output data.

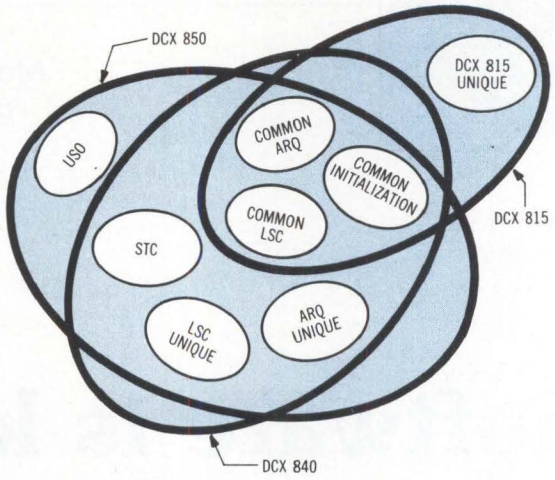

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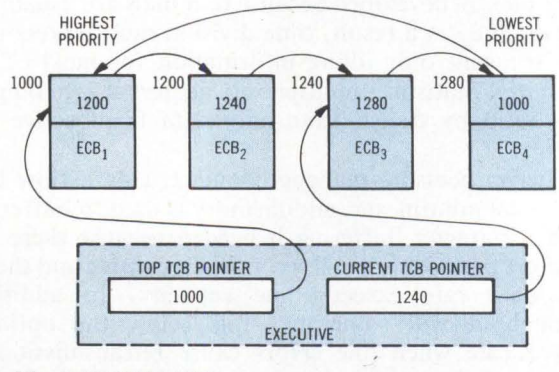
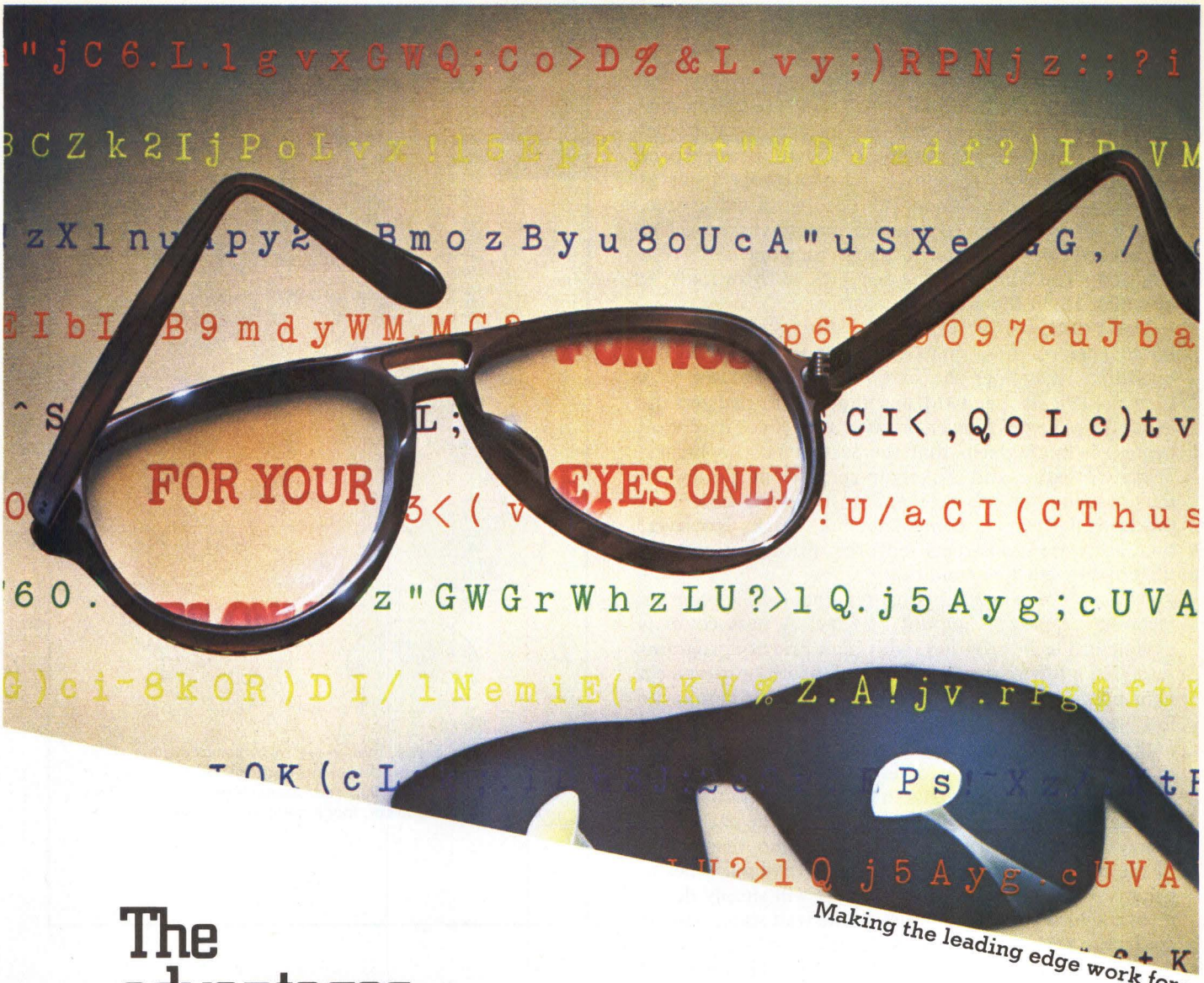
Fig 1 Compatible software modules. Core program consists of common modules. Unique addresses and extra instructions for specialized hardware occupy unique modules



ECB — EVENT CONTROL BLOCK

Fig 2 Task control blocks. Address pointers link TCBs into chain in priority sequence. Pass count apportions time allocated to each task. Remaining TCB space holds accumulators, execution address, event list, etc



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CIRCLE 97 ON INQUIRY CARD

DCX series multiplexers are based on the TMS 9900 microprocessor, which makes TCB implementation particularly easy. The 9900 has no internal scratch pad registers; instead, programmers assign a workspace pointer in memory to address 32 contiguous bytes as scratch pad registers. Each TCB occupies a workspace, in DCX series multiplexers, and as many workspaces as are needed can be defined, although only one is active at any time. The complete TCB occupies 40 bytes, only 32 of which are in the actual workspace.

The DCX executive exists only during initialization. After performing a hardware test to verify proper operation, it creates the nine TCBs required for DCX software (Fig 3). Each TCB has in one of its registers the address of the next lower priority TCB. Once execution begins, it might seem that the system has no highest priority program and is likely to spend as much time on the mundane "thumbwheel and pushbutton" task as on the critical "receive composite link" task. However, two software constructs enforce prioritization and thereby prevent this condition.

A pass count system ensures that each program receives the proper amount of time. A pass count is assigned to each program, with high priority programs receiving a low pass count and low priority programs a high pass count. For example, the "receive composite link" task has a zero pass count, and the "thumbwheel and pushbutton" task has a high pass count. Furthermore, every entry point of every program is prefaced with a loop that decrements the pass count (reloading it if negative) and returns to a wait state if the pass count remains positive. Program execution cannot resume until the program has been "scheduled" enough times to exhaust its pass count. Until then, it will simply decrement the pass count and return to the wait state, passing control to the next task in the chain.

Interrupts also help to prioritize tasks. They occur at random, requiring the microprocessor to break away from the task it is running to service the interrupt. Once an interrupt has been serviced, the microprocessor usually resumes execution of the interrupted program. However, after an interrupt routine has serviced the composite link, execution resumes at the highest priority task instead. Programs with lower priority, which are therefore further down the chain, will rarely be accessed during a period of frequent composite link interrupts. In fact, if composite link interrupts are sufficiently frequent, low priority programs may not run at all, even if their pass count has been decremented to zero. In general, as program execution proceeds down the TCB chain, the probability increases that a composite link interrupt will send control back to the top of the chain.

Although the microprocessor system has no executive, it maintains task control through TCBs that ensure more important programs a higher priority. Once the hardware for the product line has been developed, the time-consuming and costly process of software programming can be prorated by using the same software throughout the product line. In the case of the DCX series, the small unit, DCX 815, uses the same TCBs as the larger units, although the latter allocate their tasks among several different microprocessors. TCBs can be manipulated like this because each is fairly independent and easy to link with other TCBs during system initialization. Portable TCBs reduce development cost and make it easy to maintain new features. Furthermore, small systems are fully compatible with large systems because both are based on the same core software.

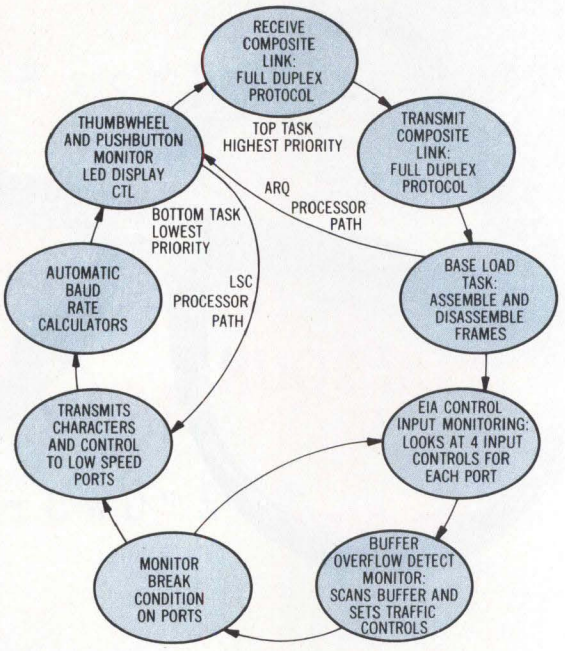

Fig 3 Nine tasks implement multiplexer product line. Low cost, single-processor product follows outside path through task chain. High-end, multiple-processor product can follow three inside loops concurrently

---

Michael Clott, a senior engineer at Rixon Inc, is project manager for the DCX multiplexer line. Before joining RIXON, he worked on microwave system analysis at Bell Laboratories. He has a BSEE from Case Institute of Technology and an MSEE from Georgia Institute of Technology.

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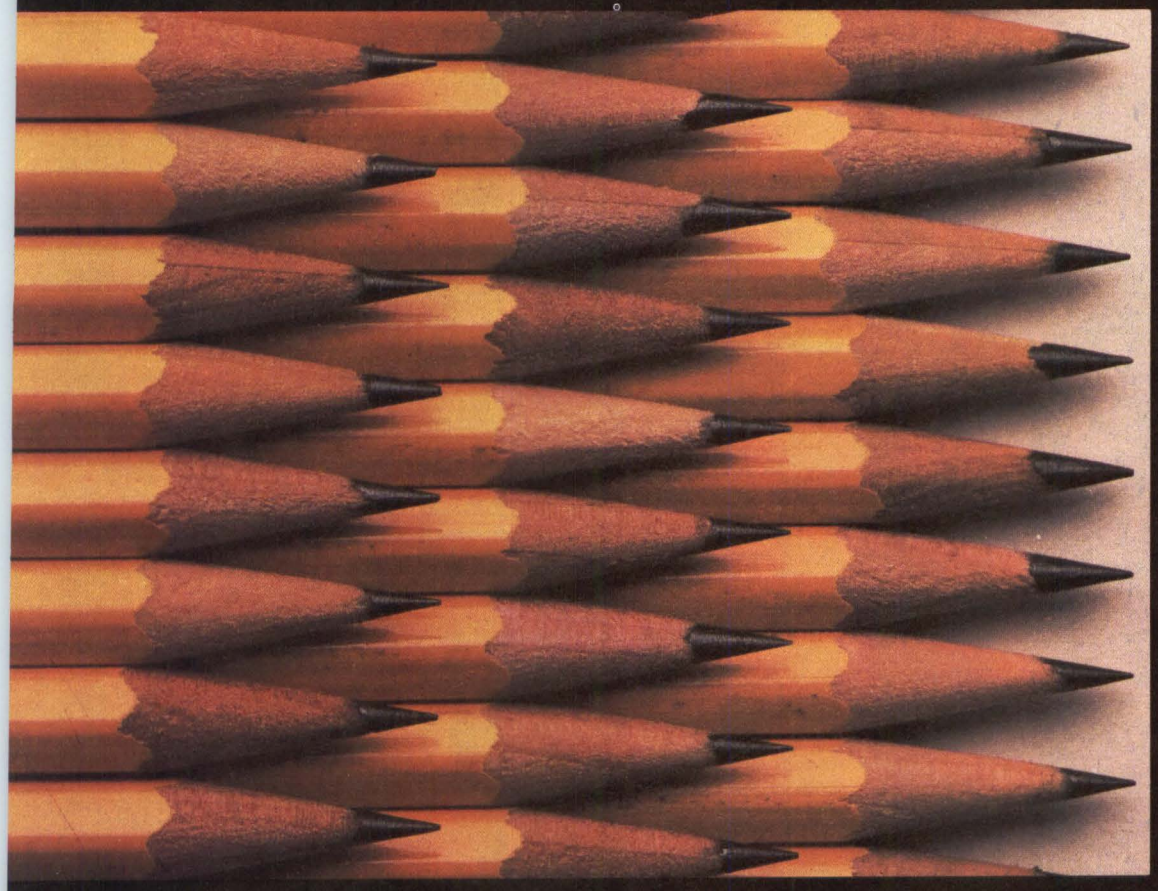

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Ben Segal, Datacomm Applications Engineer

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Asynchronous vs Synchronous. Asynchronous messages are transmitted without clock synchronization. Instead, start and stop bits frame each character and synchronize the transmitter and receiver. This method is less expensive, but relatively slow and inefficient.

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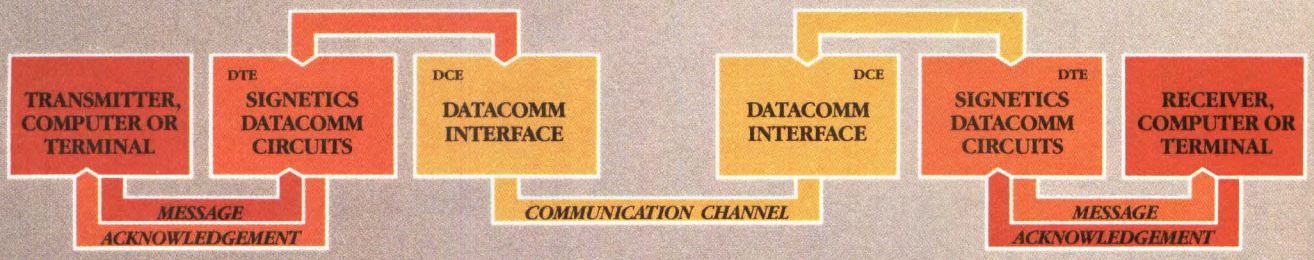
BASIC DATACOMM SYSTEM



For high-speed applications, you need synchronous protocols. These are controlled by special sync characters at the start of each message. Its advantages: no limit to the length of messages and more efficient use of the datacomm line.

Character-Oriented vs Bit-Oriented. Both of these synchronous protocols transmit messages in data blocks. But character-oriented protocols add special characters to identify the fields within the message. These can't be duplicated by message characters. In contrast, bit-oriented protocols use only three control characters and zero insertion/deletion to keep them out of the message. The result is less redundancy and higher throughput.

Error-Checking. All protocols add extra bits to the message which are used for error-detection. These check-bits are monitored by the receiver, and if errors are detected, the message is re-sent. Your protocol will determine the specific error-checking routine.

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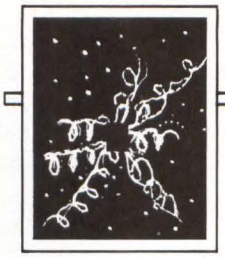

Precise adjustments increase baud rate for any cable type and length to improve performance of an RS-232 interface

Extending the limits of an RS-232 interface

The RS-232-C interface plays an important role today in low frequency, serial data communications. Because the Electronics Industries Association specification governing its drive length and frequency capabilities is somewhat general, designers can exceed the maximum recommended 50′ (15-m) cable drive length and 20k-baud rate. To drive farther, designers can alter cable types and reduce baud rate; to drive faster, they can shorten cable distance. Since all these factors are interrelated, one can be sacrificed for better performance in another area. In fact, further alterations can extend both cable length and baud rate within the scope of the RS-232-C specification.

Alterations are usually accomplished by a trial and error method because the specification does not express the specific performance adjustments possible. This introduces two questions. First, precisely what adjustments will allow, for instance, a 75′ (25-m) cable, a 40k-baud rate, or both, and still keep the RS-232-C interface in specification? Second, what magnitude of adjustments gives the desired performance without exceeding the RS-232-C specification for signal duration in the transition region?

L. T. Pearson
Federal Aviation Administration
ACT 243, Technical Bldg, Pomona, NJ 08405

Remaining in specification is important because it reduces the possibility of data alteration or loss. The specification states that the key limiting requirement for data and timing interchange circuits is the time required for the signal to pass through the transition region, which must not exceed 1 ms or 4% of the nominal duration of a signal element on the interface circuit, whichever is less. (See Fig 1.)

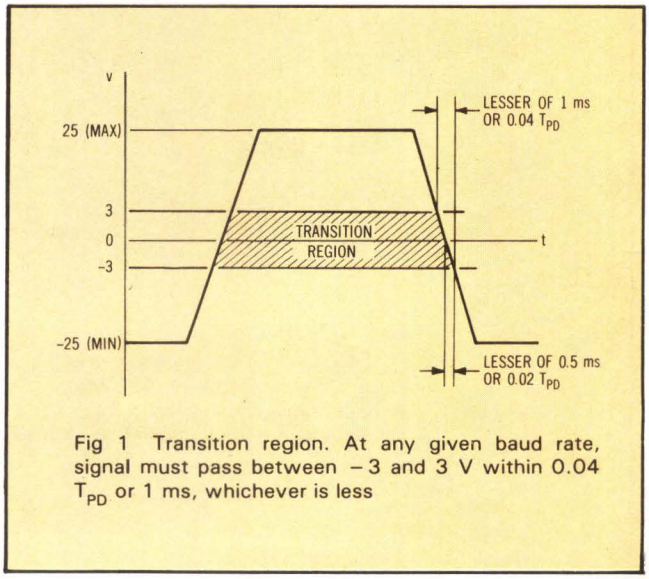

Fig 1 Transition region. At any given baud rate, signal must pass between −3 and 3 V within 0.04 T_{PD} or 1 ms, whichever is less

Examining the RS-232-C circuit configuration of a typical universal asynchronous receiver/transmitter [Fig 2(a)] reveals that the slowest signal response path (V_1) through the transition region occurs while the output transistor switches off. [See Fig 2(b).] At 20k baud, the time allotted for signal excursion through the transition region must be at least 1 ms or 0.04 T_{PD} (time per period of the nominal duration of a signal element), whichever is less.

T_{PD} = 1 / (baud rate) = 1 / 20k = 50 μs

or, (0.04) T_{PD} = 2 μs

Thus, time to cross the signal transition region must not exceed 2 μs, since for 20k baud 2 μs < 1 ms.

Delay of the signal through the transition region is caused by, and translates to, interface capacitance—the major portion of which is cable responsibility. Therefore, specific baud rates in combination with specific drivers determine the length of cable one can drive in an RS-232-C interface, without exceeding the maximum time allowable to traverse the transition region as described in the specification. Consequently, the maximum allowable interface capacitance will vary with the individual situation. However, the specification states that one can exceed 50′ cable lengths if the capacitance is held to 2500 pF. This does not hold true when driving farther than 50′ or at rates higher than 20k baud. In these cases, capacitance well below 2500 pF will prevent compliance with the transition region timing requirements. Moreover, at rates lower than 20k baud, 50′ drive lengths can be extended along with the allowable 2500-pF capacitance, making the 2500-pF stipulation meaningless.

An empirical method determines the specific interfacing alternatives available and their required magnitudes. The transition region circuit of Fig 2(b) can be redrawn to show that the worst case response occurs when the line capacitance is discharging. [See Fig 2(c).] Assuming signal symmetry about the transition region, one-half of the transition region response can be modeled from 0 to −3 Vdc. In this model, the maximum allowable capacitance is that which limits the signal voltage response from 0 to −3 Vdc to no more than one-half of the 0.04 T_{PD}, or

$T = \frac{1}{2}(0.04\ T_{PD}) = 0.02$ (baud rate)

Capacitance beyond this amount makes the signal move too slowly through the transition region for it to meet the RS-232-C specification.

Solving the general equation for capacitance in Fig 2(c) gives:

Loop 1:

$$-E/s = -(R + 1/sC)\,I_1 + (1/sC)\,I_2$$

Loop 2:

$$0 = -(1/sC)\,I_1 + (R_L + sCV)\,I_2$$

Solving for I_2:

$$I_2 = \frac{\begin{vmatrix} -(R + 1/sC) & -E/s \\ -1/sC & 0 \end{vmatrix}}{\begin{vmatrix} -(R + 1/sC & 1/sC \\ -1/sC & R_L + 1/sC \end{vmatrix}}$$

$$= [-E/sC^2] / [-RR_L - R/sC - R_L/sC - 1/(sC)^2 + 1/(sC)^2]$$

$$= [E/RR_LC]\ 1/s\,(s + (R + R_L)/RR_LC)$$

Converting to the time domain:

$$i_2 = [E/R + R_L]\,[1 - (1/e\,(R + R_L)/RR_LC)\,t]$$

Solving for capacitance:

$[R + R_L/RR_LC]\,t = \ln E - \ln [E - i_2\,(R + R_L)]$, where $i_2 = 3\ \text{Vdc} / R_L$

$$C = (R + R_L)\,t / RR_L\,[\ln E - \ln (E - (3/R_L)(R + R_L))]$$

To solve for maximum allowable interface capacitance, baud rates and driver voltages must be inserted into the

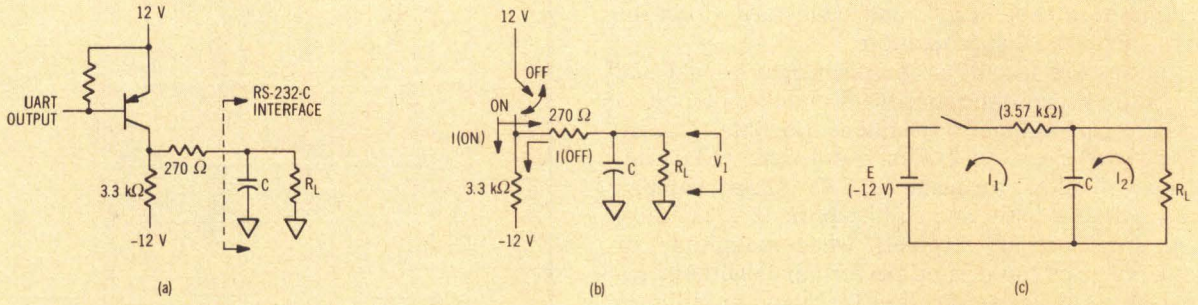

Fig 2 Typical circuit model. When output transistor in (a) switches off, slowest path V_1 through transition region results as shown in (b). Then, in (c), loop equations yield maximum capacitance at any combination of baud rate and driver voltage

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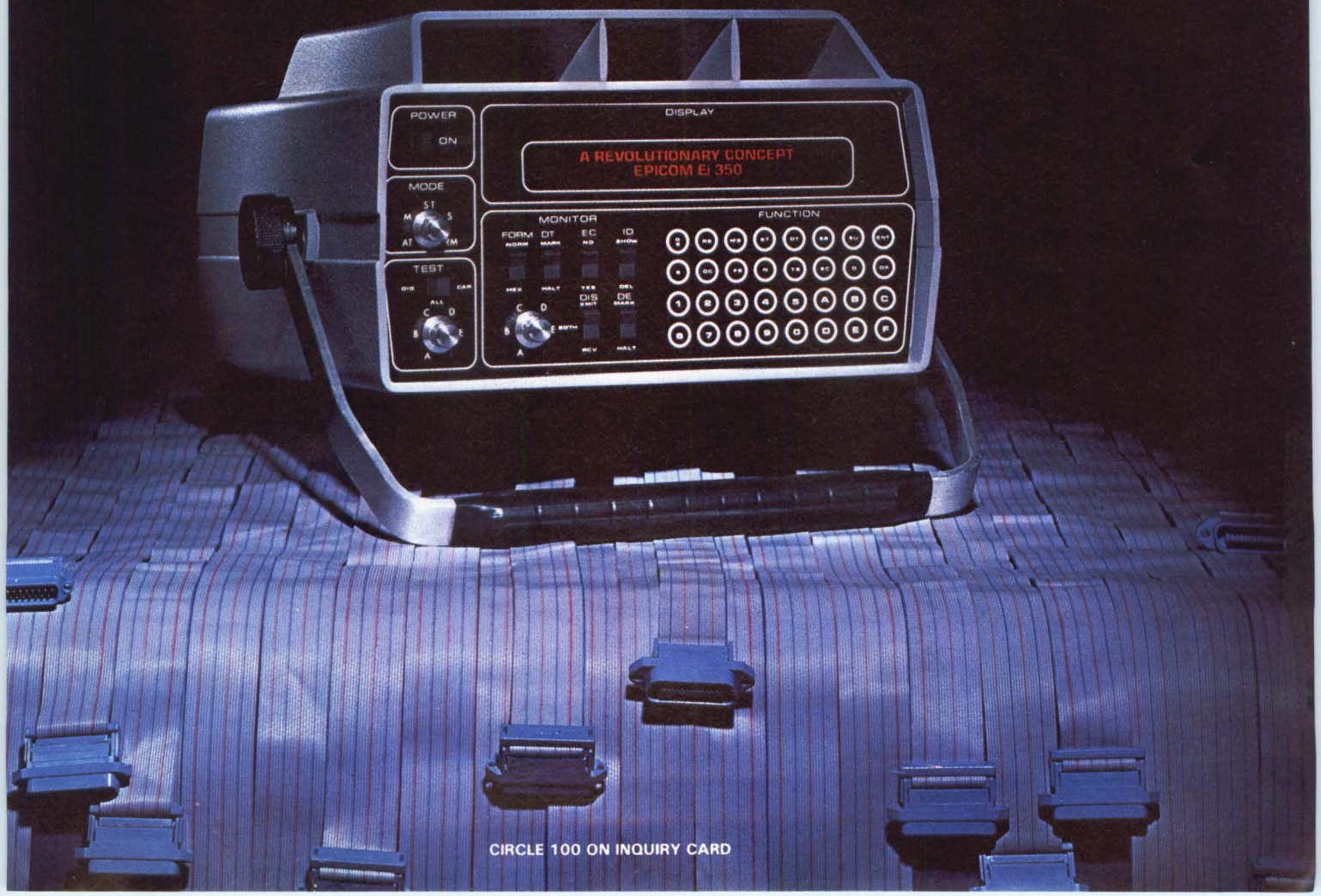
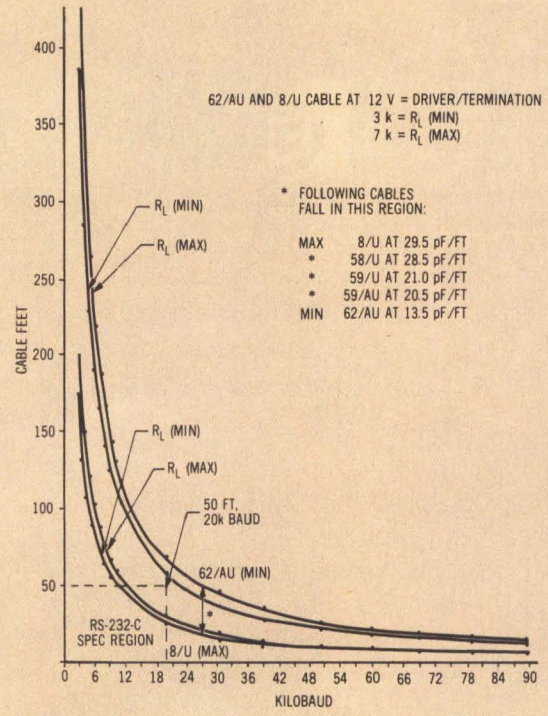


CIRCLE 100 ON INQUIRY CARD



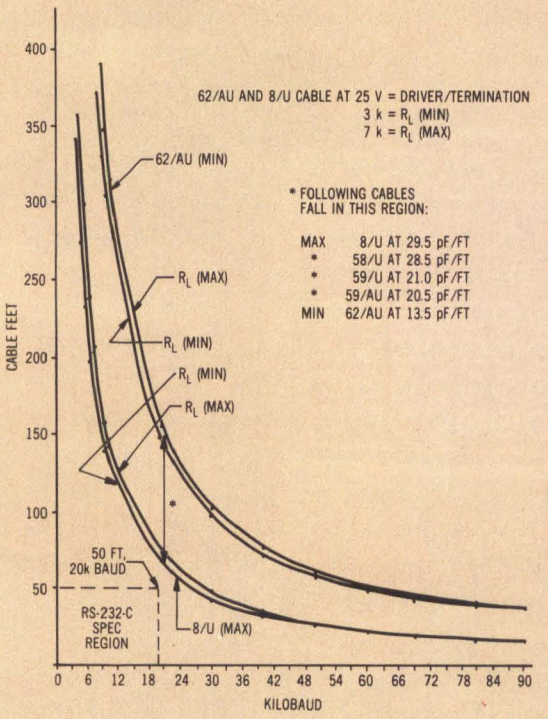


Fig 3 Cable performance tradeoffs. Graphs plot maximum cable length for 62/AU and 8/U cables driven at 12 and 25 V for various loads

general equation. Resistances are known. By solving this equation for capacitance, and dividing (the capacitance) by the μF/ft rating for various cables (ie, 62/AU at 13.5 pF/ft), the baud rate, cable length, driver voltage, and cable type design information can be defined. With these data available, it is easy to see whether the design requirement asks too much of the RS-232-C interface, and what adjustments can be made to accommodate the requirement. Of course, driver and terminator capacitance must be subtracted from the total capacitance before determining the capacitance to be allocated for the cable. A rule of thumb is to reserve approximately 100 pF (maximum) to this source. For simplicity, and since its impact is minimal, it is not included in the Fig 3 data.

As noted, the general RS-232-C requirement of 20k baud and 50′ can be exceeded by some cables with powerful (±25-V) drivers, while under other circumstances (±12-V drivers) greater discretion is required in the choice of cable type. The effect of load variation, which is minor, is also illustrated in Fig 3. To interpret the data, a ±12-V driver with a 62/AU cable can safely drive 100′ (30 m) at a rate of up to 12k baud, without exceeding the RS-232-C requirements. A more powerful (±25-V) driver will go up to 30k baud at that same distance. The interface capacitance that cannot be exceeded in this case is 1350 pF, which is well below the 2500 pF that was specified as a safe RS-232-C upper limit. The same approach can determine cable length and baud rate restrictions for any driver and cable combination.

About the Author:

L. T. Pearson is a senior electronics engineer at the FAA Technical Center in Atlantic City, New Jersey, where he determines computer hardware design requirements for air traffic control simulation. Before this, Mr Pearson set design requirements for computer hardware and software for the U.S. Army at Fort Monmouth, New Jersey. Other experience includes work with computer hardware architecture and peripherals at Sperry Univac. Mr Pearson holds a BSEE from Lafayette College and an ME in engineering science from the Pennsylvania State University.

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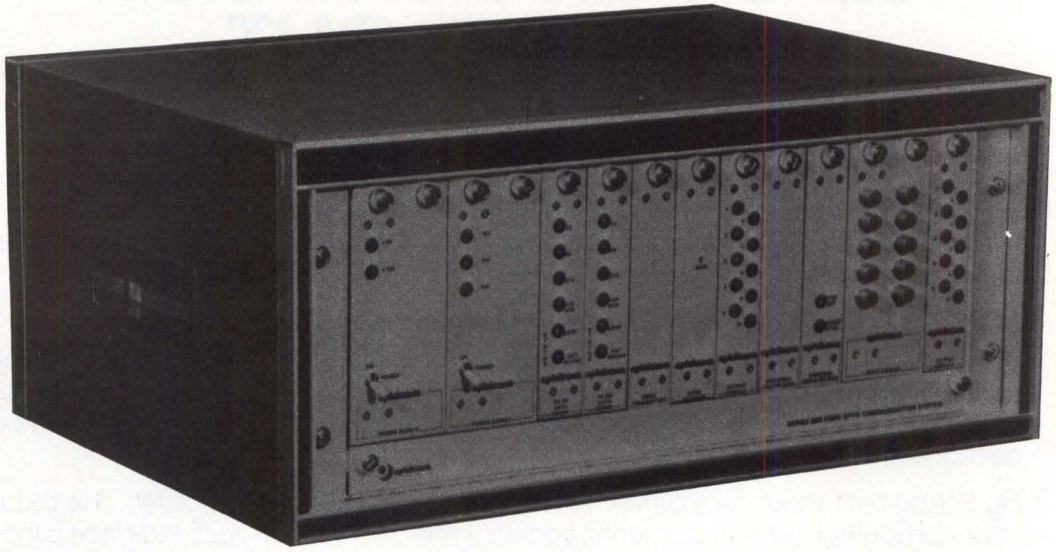

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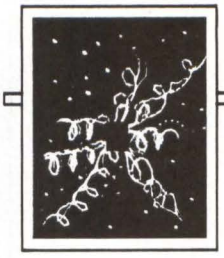

Interfacing a microprocessor with peripheral chips from a different manufacturer improves performance and reduces programming

SDLC interface mates M6800 peripheral to 8086

Microprocessors do not necessarily require the use of peripheral devices from their own families. For example, several manufacturers supply peripheral devices to support serial data link control and other communications protocols. These devices concentrate most of the logic needed to implement the protocol and some of the communication link controls in a single device, which is usually a peripheral for one of the manufacturer's microprocessors. Teaming a microprocessor with a peripheral device from the same family usually requires minimal logic to interface the two devices. Nevertheless, the use of a functionally similar peripheral device from a different microprocessor family could offer significant advantages from the software standpoint. These advantages could justify the extra hardware needed to interface the peripheral device with the alien microprocessor.

An 8086 based microprocessor system that uses the MC6854 advanced data link controller to implement serial data link control (SDLC) protocol logic offers several advantages. There are quad data buffers for both the receiver and the transmitter. Prioritized status registers simplify the software. Also, it is possible to request an interrupt when a full word of data is ready to be transferred, instead of when only one byte is ready, as with most other SDLC controllers. This feature reduces processing time needed to support the SDLC interface, which is especially important at high baud rates.

Sorin Yakobovitch
Tadiran Electronics
Holon, Israel

Adapting M6800 peripherals to the 8086

Interfacing an M6800 compatible peripheral device to the 8086 is perhaps the major problem solved by the circuit in Fig 1. With slight modifications, this circuit could be used for interfacing the 8086 to most synchronous peripherals in the M6800 family, such as the MC6840, MC6843, and MC6850. The ring oscillator (A1a to A1d flipflops) divides the 8086 clock to obtain a freerunning E clock that meets all MC6854 needs. A jumper selects the proper oscillator output for the E waveform according to the clock rate (5 or 8 MHz) of the 8086. Ring oscillator outputs also serve as low order inputs to A2, a fast, bipolar, 256- x 4-bit, programmable read only memory (P/ROM) with open collector outputs.

Other inputs to the A2 P/ROM also appear in Fig 1. $\overline{RD}$ and $\overline{WR}$ lines derive from the 8086. $\overline{CS}$, obtained by

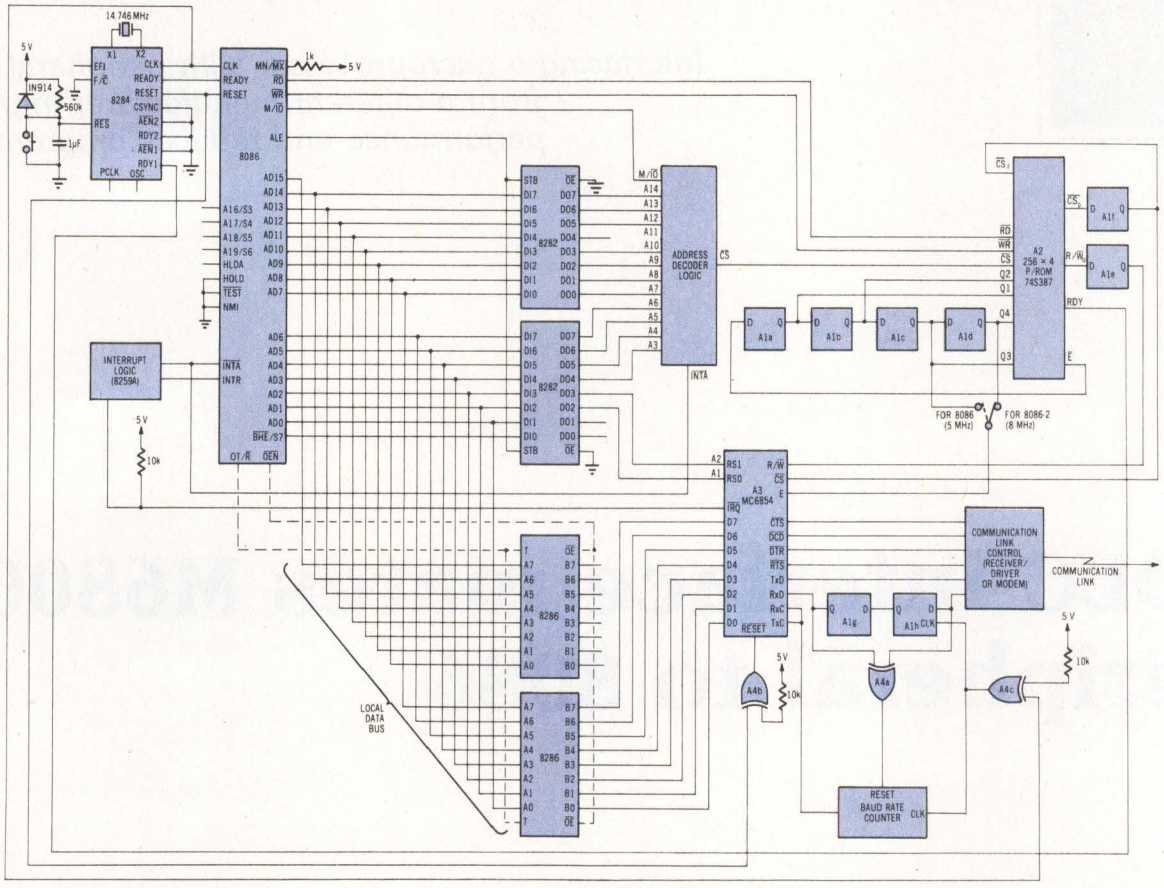

Fig 1 Interface circuit diagram. Three chips interface 8086 microprocessor with MC6854 synchronous peripheral chip. Two of these, A1 and A4, also help recover clock from received data stream. Same technique mates other M6800 family chips to 8086

decoding the 8086 address lines, goes low whenever the 8086 addresses one of the MC6854 registers. $\overline{CS}_i$, the MC6854 chip select line, preserves the state of the $\overline{CS}_o$ P/ROM output from the last 8086 clock cycle.

Outputs of the A2 P/ROM are $\overline{E}$, RDY, R/$\overline{W}_o$, and $\overline{CS}_o$. $\overline{E}$ is supplied as input to the ring oscillator. Using the P/ROM instead of a simple inverter to invert the E waveform avoids forbidden states in the ring counter (eg, 010 and 101 for the divide-by-6 counter). When a forbidden counter state appears during start-up or for some other reason, the $\overline{E}$ output of the P/ROM is forced equal to the E input, canceling the inverter function. This arrangement forces the counter back into a normal state during the next 8086 clock cycle.

Whenever an MC6854 register is accessed, the RDY output from the P/ROM, which drives RDY1 of the 8284 clock generator and counter, requests a proper number of wait cycles from the 8086. These extra clock cycles meet the timing requirements of the MC6854. The P/ROM's RDY output can be wire-ORed with ready outputs from other peripheral or memory boards and connected to the RDY1 or RDY2 inputs of the 8284.

P/ROM output $\overline{CS}_o$ is latched every clock cycle to obtain $\overline{CS}_i$, which serves as the chip select for the MC6854 and also as input to the A2 P/ROM. Finally, the R/$\overline{W}_o$ output is also latched every 8086 clock cycle to obtain an R/$\overline{W}$ signal for the MC6854. Latching both the $\overline{CS}_o$ and R/$\overline{W}_o$ P/ROM outputs prevents undefined output states generated during P/ROM access from reaching the MC6854. The RDY output need not be latched because the 8248 latches RDY internally.

Proper programming of the A2 P/ROM ensures that $\overline{CS}_o$ and R/$\overline{W}_o$ generate $\overline{CS}_i$ and R/$\overline{W}$ signals which meet the MC6854 timing requirements. The number of wait cycles added to any bus cycle that addresses the MC6854 (by keeping RDY low for the proper amount of time)

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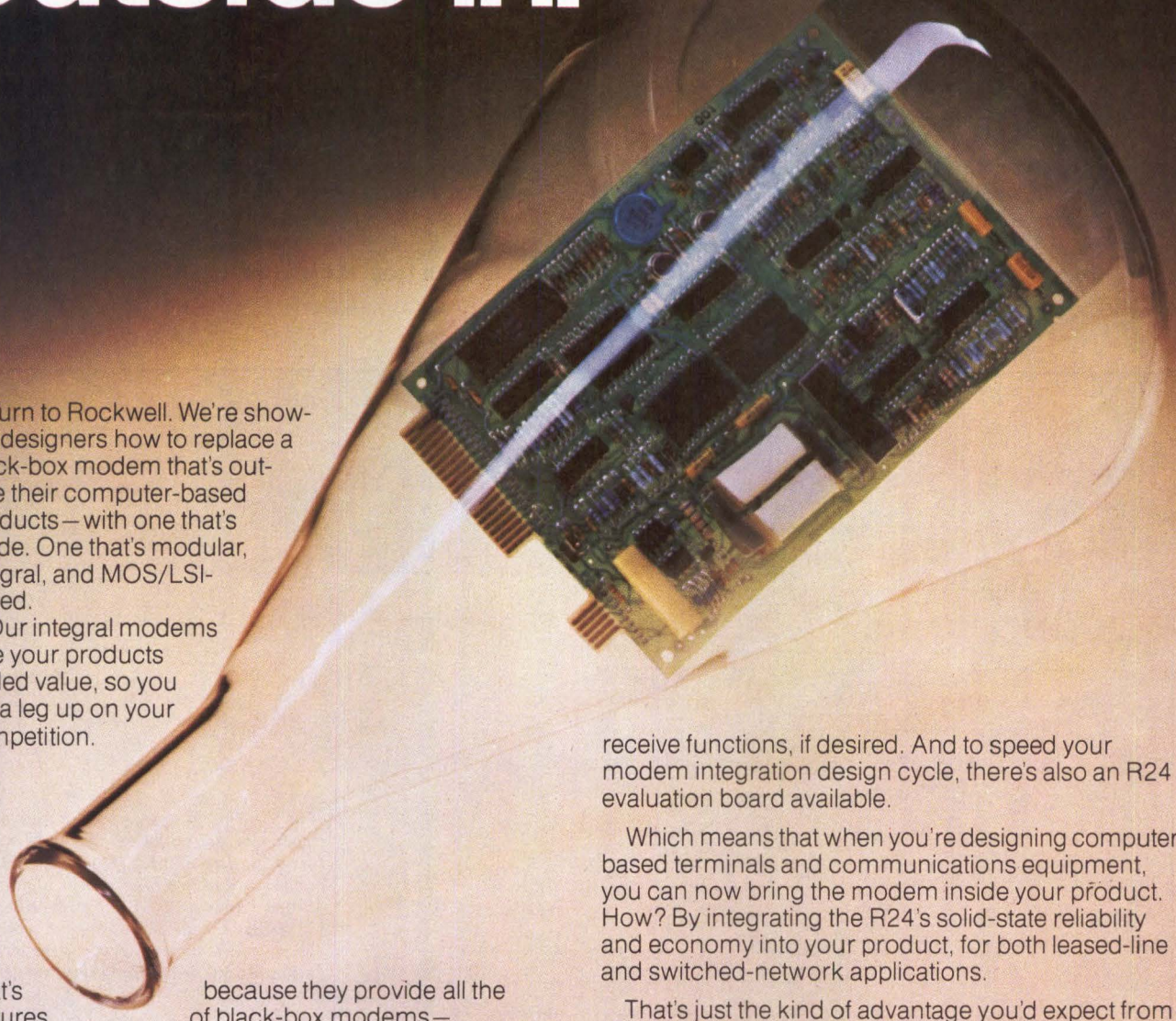

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depends on when the beginning of the bus cycle catches the freerunning E waveform. Fig 2 shows two different situations. The first results in a few wait states, the second in many.

Recovering a clock from the received data stream

Even if the nominal transmitter and receiver clock frequencies are theoretically equal, there is usually a difference between them because of tolerances in their respective oscillator components. Without synchronization between the transmitter clock and the receiver clock, this causes a phase difference between the two clocks that can increase with every bit transmitted. If the phase difference exceeds the maximum allowed value, incorrect data stream sampling by the receiver could produce erroneous data. A synchronous communication link solves this problem by sending not only data but also a clock for use by the receiving device. SDLC frame format allows simple recovery of the clock from the received data stream. A recovery circuit on each SDLC interface board eliminates the need for separate communication lines or more complex modems to handle transmitter and receiver clock signals, making the data link practically asynchronous.

The receiver clock for the SDLC interface in Fig 1 is recovered from the received data stream by means of the simple circuit using devices A1g, A1h, A4a, and the baud rate counter. This clock recovery circuit capitalizes on the fact that the sending device transmitter samples data on the falling edge of the clock, and the receiver at the SDLC interface samples data on the rising clock edge. Upon detecting a transition in the received data stream, the clock recovery circuit sends a short reset pulse to the baud rate counter, synchronizing it with the transmitting device. A fast reset pulse, relative to the receiver clock, improves synchronization by forcing the rising edge of the recovered clock closer to the rising edge of the transmitting device clock.

The greatest tolerance for transmitter and receiver clock frequencies of the two devices occurs when the serial data from the transmitter are coded in non return

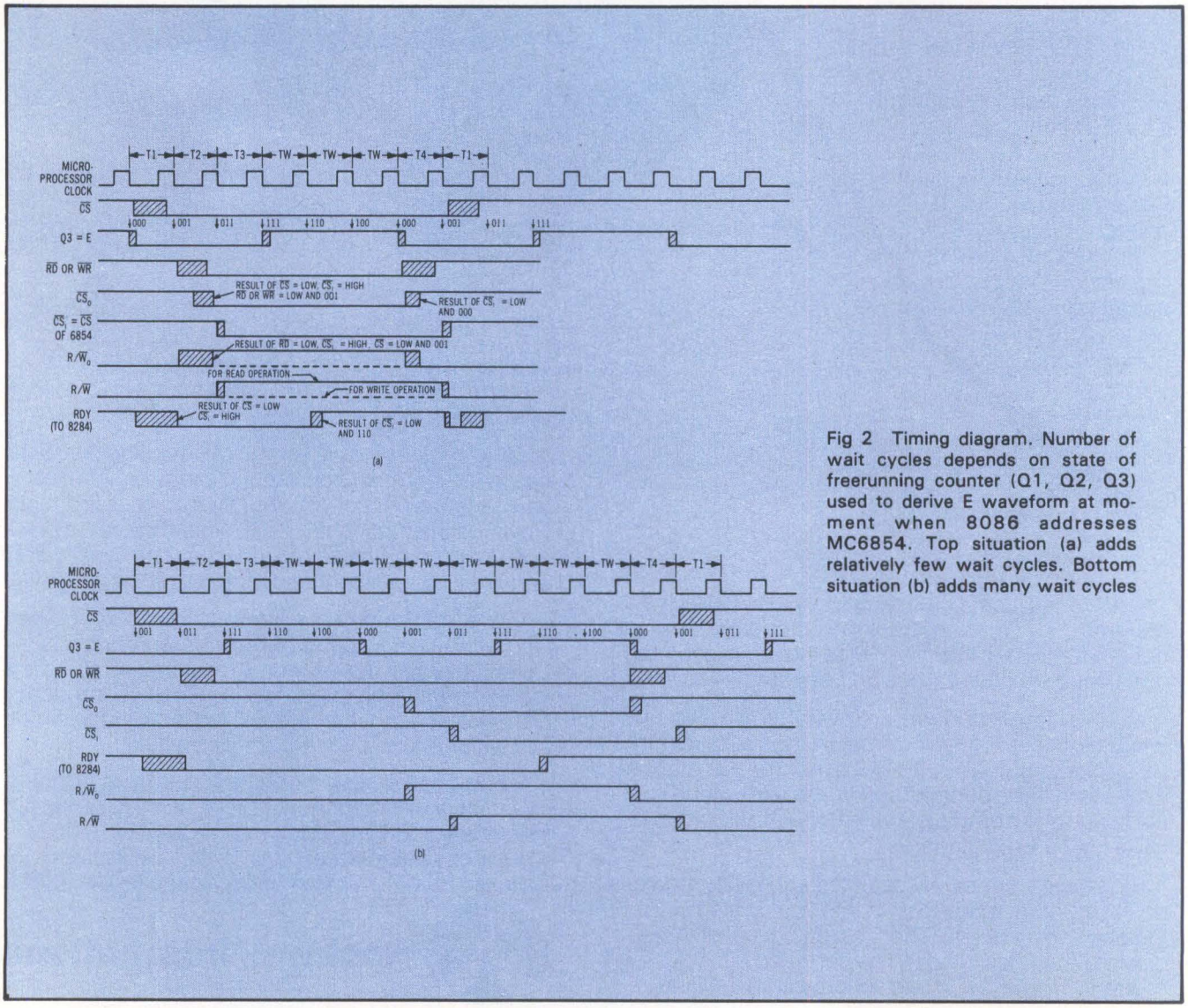

Fig 2 Timing diagram. Number of wait cycles depends on state of freerunning counter (Q1, Q2, Q3) used to derive E waveform at moment when 8086 addresses MC6854. Top situation (a) adds relatively few wait cycles. Bottom situation (b) adds many wait cycles

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to zero inverted (NRZI) data format. (See "SDLC Overview.") If the nominal baud rates of the transmitted data and the received data are equal, the counter used by the receiver clock recovery circuit can be used as the baud rate counter to obtain the transmission clock at the SDLC interface.

Half-duplex serial communication interface

Fig 3 is a complete SDLC interface for point to point or multipoint, half-duplex communication over balanced lines according to the RS-422 standard. The schematic shows the link control circuit for this type of interface and also contains a time-out circuit for use when the interface belongs to the primary unit of the SDLC link. It has a differential line driver and a differential line receiver, both connected to a balanced, twisted pair, communication line. Transmitter and receiver alike are controlled by the ready-to-send ($\overline{RTS}$) line from the MC6854. Software must set $\overline{RTS}$ low for the 8086 to transmit data across the line; $\overline{RTS}$ automatically goes high after the SDLC transmitter in the MC6854 sends the last bit of the frame closing flag.

When $\overline{RTS}$ is low, the line driver output is enabled, and data from the SDLC transmitter in the MC6854 pass across the communication line. When $\overline{RTS}$ is high, however, the receiving device is disabled to prevent transmitted data from reaching the SDLC receiver in the MC6854. The pull-up resistor at the receiver output translates this high impedance output state into a stream of 1s (idle state) at the RxD input of the SDLC receiver. At the end of a transmission, when the $\overline{RTS}$ line of the MC6854 goes high, it disables the line driver and enables the line receiver. The line remains inactive, with both driver outputs in a high impedance state, until the unit on the other side of the communication link enables its

SDLC Overview

SDLC is one of the most popular bit oriented protocols. It can be viewed as an envelope in which data are transferred from one station to another across a data communication link. The link can be either multipoint or point to point and involves at least two participating stations. SDLC data links assign two roles to these stations: primary (commanding) and secondary (responding). The primary station is responsible for the data link and issues commands to which all other participating stations respond. Secondary stations are linked to the primary station.

Either half- or full-duplex exchanges can be used for the flow of information. The basic unit of information on an SDLC link is a "frame." It is the vehicle for every command and response and for all the information that is transmitted using SDLC procedures. The frame format is shown below.

Opening Flag (F)	Address Byte (A)	Control Byte (C)	Information Field (I)	Frame Check Sequence (FCS)	Closing Flag (F)
01111110	8 bits	8 bits	Any length	16 bits	01111110

Each frame is enclosed in "flags," which are used for frame synchronization and have the binary configuration 01111110. The opening flag (F) of the frame serves as a reference for the position of the address (A) and control (C) fields. The closing flag (F) terminates the check for transmission errors. A frame is easy to identify because it begins with a flag and contains only non-flag patterns up to the closing flag. This does not restrict frame content, however, because the transmitter must insert a binary 0 after any succession of five contiguous 1s within the frame. Thus, no flag pattern is ever transmitted by chance. After the opening flag is detected at the receiving end, the receiver removes any 0 that follows five consecutive 1s.

The address byte (A) functions such that the primary station is never identified, whereas secondary stations always are. The control byte (C) embodies the link level control of the SDLC. When an information field (I) is used, it is unrestricted both in content and length. The 16-bit field of the frame check sequence (FCS) is used for error detection through cyclic redundancy checking. If an unusual condition occurs during transmission, the transmitter aborts the frame by sending eight consecutive 1s.

When the transmitter is in an "out-of-frame" condition (ie, not transmitting a frame), it is in an idle state. Either a series of contiguous flags or a mark idle (consecutive 1 bits) may be transmitted in this state. Although SDLC is a synchronous protocol, it provides an optional feature that allows its use on basically asynchronous data links—NRZI (nonreturn to zero inverted) coding. This coding specifies that the signal condition not change for transmitting a binary 1, but that a binary 0 cause a change of state. It guarantees that an active line will have a transition at least every five bit times because of the zero bit insertion. Since asynchronous operation requires the receiver sampling clock to be derived from the received data, NRZI encoding makes the design of clock recovery circuits easier.

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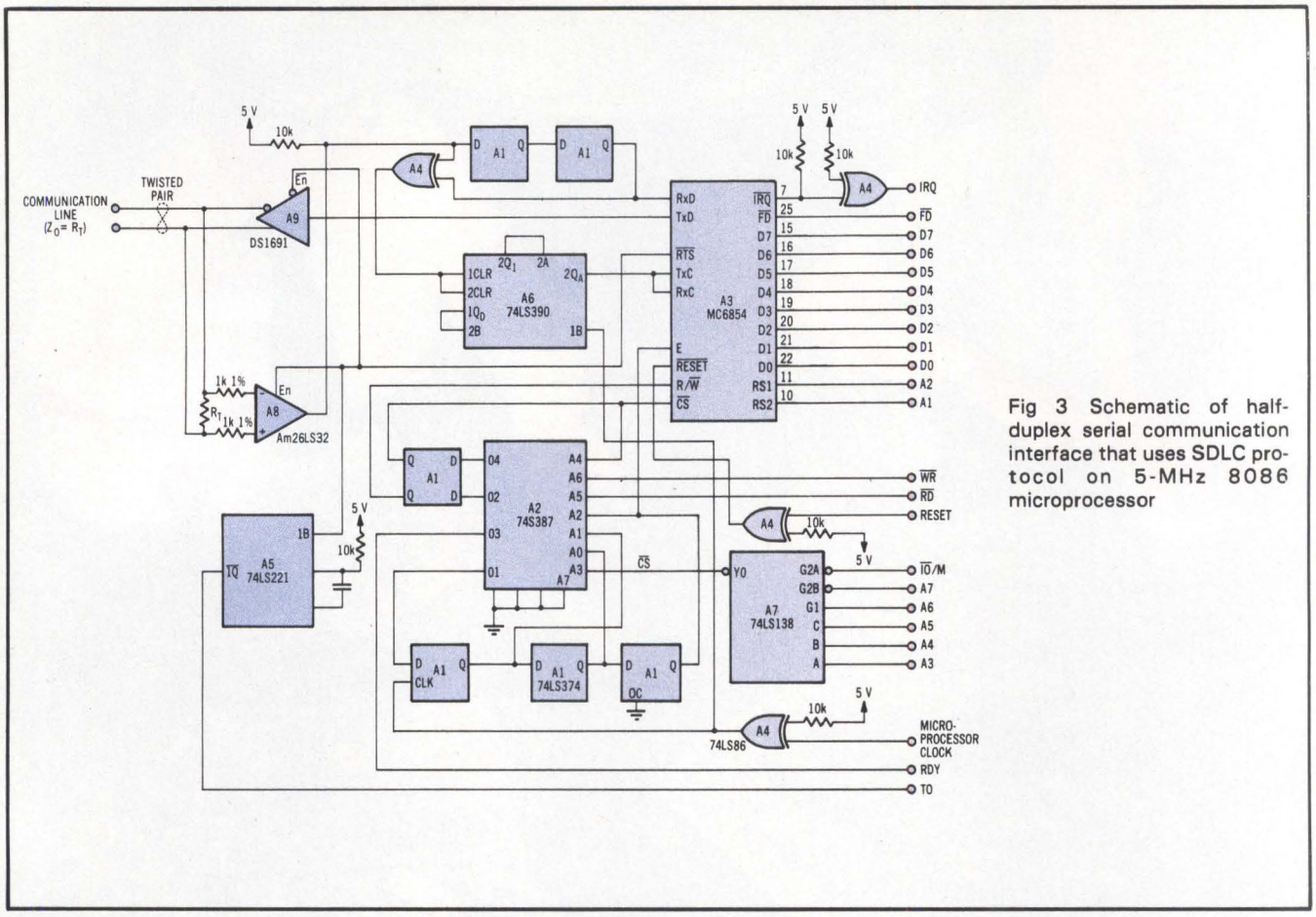

Fig 3 Schematic of half-duplex serial communication interface that uses SDLC protocol on 5-MHz 8086 microprocessor

driver to start transmitting. A fail-safe feature in the receiver at the interface translates this high impedance state into an idle state at the RxD input of the MC6854.

The primary unit polls the secondary unit and expects to get an answer from it within the time-out period following the end of the polling frame transmission. A time-out circuit allows the 8086 in the primary unit to determine whether there was a response within the time-out period. In Fig 3, the time-out 1-shot, A5, is triggered by the rising edge of the $\overline{RTS}$ signal, and a time-out (TO) signal requests an 8086 interrupt. Flag detect ($\overline{FD}$), another interrupt, notifies the 8086 that frame reception has started. The SDLC receiver generates $\overline{FD}$ whenever it detects a flag character. If the SDLC link idle state is a mark idle, as it should be for the circuit in Fig 3, there are two $\overline{FD}$ pulses for the answer frame: one for the frame opening flag and another for the frame closing flag. Only the $\overline{FD}$ pulse produced by the opening flag should interrupt the 8086, since only this pulse marks the beginning of frame reception.

Programming a half-duplex interface

Use of the MC6854 chip to implement the half-duplex SDLC interface greatly simplifies supporting activities performed by the 8086. To begin transmitting a frame, the 8086 invokes a transmission start-up routine and passes it two parameters: a pointer to the beginning of the data buffer and a count of the number of bytes to send (Fig 4). The transmission start-up routine first forces the $\overline{RTS}$ line low by setting the $\overline{RTS}$ bit of control register CR2 in the MC6854. RTS must remain low until the opening flag of the frame has been sent. This arrangement ensures that $\overline{RTS}$ will go high only at the end of the closing flag transmission.

To delay RTS reset, the transmission start-up routine loads the first in, first out, transmit memory (called a FIFO) in the MC6854 with the address and control bytes of the frame to be sent. It then polls the MC6854 status register SR1 for an indication that the transmit FIFO is ready to accept more bytes for transmission (TDRA flag set). The RTS bit in CR2 of the MC6854 can be reset at this time because the opening flag has been sent.

If the number of bytes to be sent, TXCNT, is smaller than the FIFO capacity, the transmission start-up routine loads any data bytes from the transmission buffer into the FIFO until it reaches the last byte. It writes the last byte into a special FIFO address to terminate the frame. Then, it resets the RTS bit in the CR2 register and enables $\overline{FD}$ interrupts (along with TO interrupts for primary units only). IRQ interrupts from both the transmitter and the receiver are left disabled (control bits RIE and TIE cleared in CR1). This is the right side path in Fig 4.

If, instead, the number of bytes to be sent exceeds the transmission FIFO capacity, the transmission start-up routine must fill the FIFO by loading it with the first two

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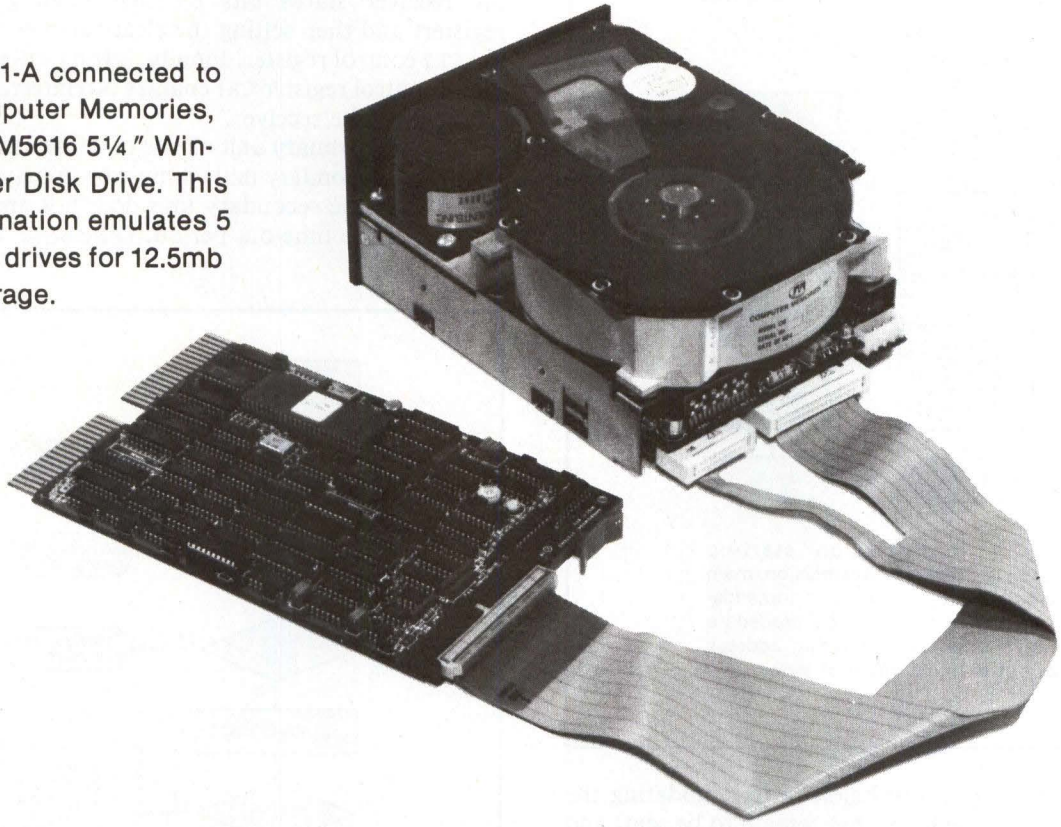

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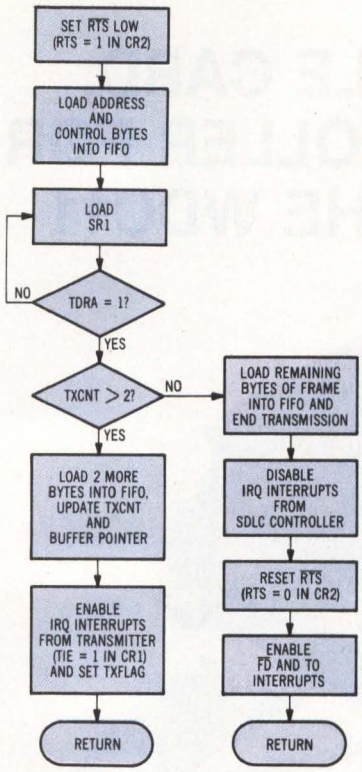

Fig 4 Transmission start-up routine. To begin transmission, main program prepares data in transmission buffer and invokes procedure flowcharted here, passing address of buffer and number of bytes

data bytes from the transmission buffer, updating the TXCNT counter (of the bytes that remain to be sent) and the pointer (to the next data byte), and setting TXFLAG, the flag used to notify the interrupt service routine that only interrupt requests from the transmitter are enabled. Then, concluding the left side path in Fig 4, the transmission start-up routine returns to its caller.

Every time the transmission FIFO is ready to accept two more outgoing bytes of data, the interface initiates an IRQ interrupt (Fig 5). The 8086 interrupt service routine first establishes that the IRQ interrupt originated at the SDLC interface by checking the IRQ status bit in SR1. A zero value in this bit indicates a spurious interrupt that the service routine can safely ignore. If the IRQ flag is set, however, the interrupt service routine checks TXFLAG to learn whether the SDLC interface is sending or receiving data. If sending data, after loading the last byte of the frame into the FIFO, the interrupt service routine terminates by resetting control bits TIE and RIE in CR1 (to disable IRQ interrupts from the SDLC controller), resetting the RTS control bit in CR2 (to force the MC6854's $\overline{\text{RTS}}$ line high after the last bit of the frame closing flag is sent), resetting TXFLAG, and enabling $\overline{\text{FD}}$ interrupts. It also enables TO interrupts if the interface belongs to the primary unit on the SDLC link.

The interface does not require 8086 support between the transmit and receive phases of the SDLC communication process. The IRQ interrupts of the MC6854 are disabled at this time because control bits TIE and RIE are reset in CR1. However, when a frame starts to be received, its opening flag causes an $\overline{\text{FD}}$ pulse that interrupts the 8086. The $\overline{\text{FD}}$ interrupt service routine then disables further $\overline{\text{FD}}$ interrupts to prevent the closing flag from causing an interrupt. It masks TO interrupts, if any, to prevent the time-out signal from causing an interrupt at the end of the time-out period, and it resets the receiver status bits by first reading the status registers and then setting the clear-receiver-status bit in the CR2 control register. Finally, setting RIE and clearing TIE in control register CR1 enables IRQ interrupts that are initiated by the receiver.

When the primary unit of an SDLC link sends a polling frame to a secondary unit, it must be prepared for those times when the secondary unit does not answer before the end of the time-out period. Otherwise, the primary

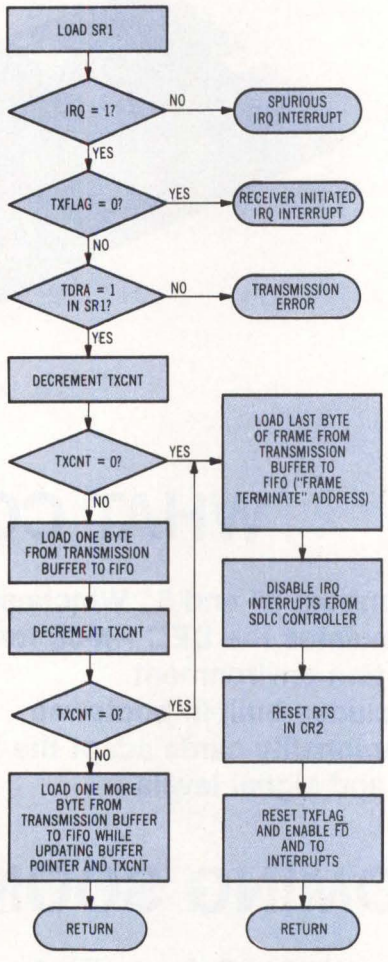

Fig 5 IRQ interrupt service routine. Flowchart details program steps to handle IRQ interrupt initiated by transmitter. Fig 6 shows procedure for IRQ interrupts from receiver

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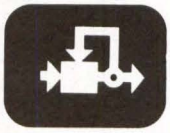

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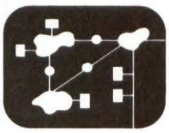

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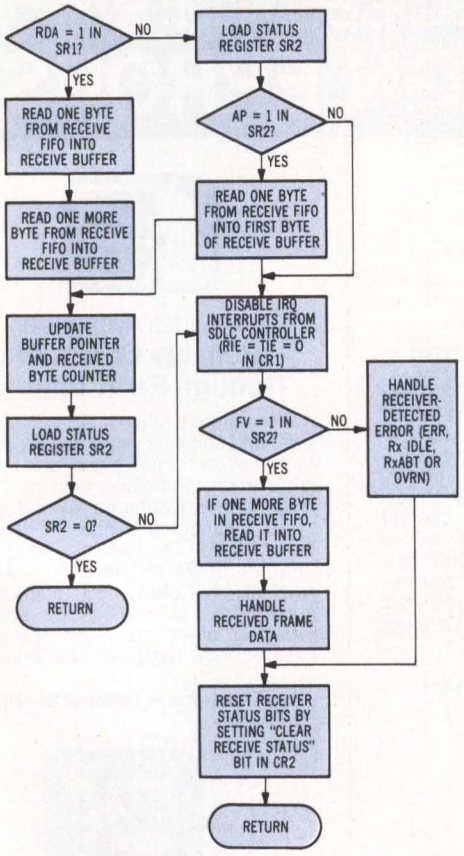

Fig 6 Servicing receiver-generated interrupts. Flowchart in Fig 5 branches to this procedure when IRQ interrupt originated at receiver

unit could wait indefinitely and paralyze all communication. The primary unit interface solves this problem through a TO interrupt. If there is no response from the secondary unit before the end of the time-out period, TO interrupts the 8086, and the TO interrupt service routine masks $\overline{FD}$ interrupts and further TO interrupts. It then disables the IRQ interrupts from the SDLC controller by resetting TIE and RIE in CR1. Finally, it calls a routine that suspends waiting for the secondary unit answer frame and handles all remaining time-out housekeeping operations.

If the beginning of an answer frame is received before the end of the time-out period, the $\overline{FD}$ interrupt produced by the opening flag of this frame causes the $\overline{FD}$ interrupt service routine to disable TO interrupts. It then enables interrupts from the SDLC receiver, which will issue an IRQ to interrupt the 8086 every time received data are ready to be transferred out of the receiver FIFO.

Several abnormal conditions also cause the SDLC interface to initiate an IRQ interrupt during reception. An end-of-frame condition can signal either a good or invalid frame check sequence, or an abort. Status bits FV, ERR, and RxABT in the MC6854 distinguish among these three conditions. Unexpected detection of an idle condition also causes an interrupt. Detection of an idle condition will not normally interrupt the 8086 because only the beginning of frame reception enables receiver initiated IRQ interrupts, and then only after status bits have been reset. Since receiver initiated interrupts are disabled when the receiver detects the end of a frame, any idle condition that causes an IRQ interrupt must be abnormal. Finally, an overrun condition that occurs when incoming data overwrite data that have not been unloaded from the receiver FIFO will also cause an IRQ interrupt with the OVRN status bit set in status register SR2.

The IRQ interrupt service routine first verifies that the IRQ interrupt originated at the SDLC interface by establishing that SR1 status bit IRQ is set (Fig 6). If this bit is not set, the service routine can ignore what must be a spurious interrupt. The IRQ service routine next checks TXFLAG, which is cleared when the SDLC interface is not transmitting. Only IRQ interrupts initiated by the receiver can occur when TXFLAG is zero. The IRQ interrupt service routine concludes by following the procedure outlined in Fig 6.

Conclusion

A general purpose interfacing technique mates the 8086 microprocessor to a whole range of peripheral devices in the M6800 family. When used with an MC6854 advanced data link controller, this technique implements an SDLC communications interface that offers significant design benefits for optimizing the use of the 16-bit microprocessor. Although a small amount of extra hardware is needed to match the microprocessor with an alien peripheral device, greatly simplified programming needs more than compensate for the additional logic.

About the Author:

As a senior design engineer at Tadiran Electronics in Israel, Sorin Yakobovitch is responsible for designing interfaces for a distributed computer system. Before joining Tadiran Electronics, he was project leader for a portable medical monitor and then for an LSI-11 video interface for graphics display at M. G. Electronics in Israel. Mr Yakobovitch has an MS degree in electronics engineering from the Polytechnic Institute of Bucharest, Rumania. His areas of interest are medical electronics, computer hardware, and realtime software.

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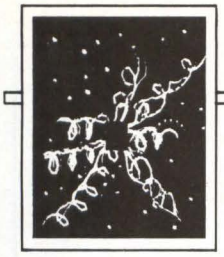

Two circuit boards and a standard software package give iSBC systems a complete Ethernet interface that needs only high level programming

Putting Ethernet onboard the multibus

Ethernet has developed rapidly from a concept to a multivendor local area networking system. The system was demonstrated recently at the 1981 National Computer Conference in Chicago, where a yellow Ethernet cable snaking through the Intel, Xerox, and Digital Equipment Corporation booths provided the transmission medium for messages sent around the three locations.

Even before the NCC demonstration, there was great interest in Ethernet local area networks, with several domestic and European companies quietly working on Ethernet based systems. Since that exhibition, interest has grown. That is one reason why Intel has released a single-board Ethernet controller. Another reason is the many systems that are potential sites for Ethernet communications capability. Making Ethernet compatible with the MULTIBUS® seemed to be the key to broadening the base of local area networking.

Two boards—a processor and a SerDes

The iSBC 550 controller consists of two boards, an 8088 based processor board and a serialization/deserialization board referred to as the "SerDes" board. (See Fig 1.) The processor board contains circuitry for processing, packet buffering, and transferring processed packets to system memory. The SerDes board meets the tricorporate specification for data link control and physical link control. It converts 8-bit parallel data into serial data, frames the messages, computes the cyclic redundancy check polynomial, and determines whether the message received matches the computed value. It also handles the Manchester encoding and decoding of message data, performs destination-address recognition, and takes care of the collision-handling scheme.

Joseph P. Harakal
Intel Corporation
5200 Elam Young Pkwy, Hillsboro, OR 97123

Like other iSBC boards, the iSBC 550 board pair is built to common dimensions: 12″ (30 cm) wide, 6.75″ (17 cm) high, and 0.5″ (1.3 cm) deep. Board edge connectors are arranged in the standard iSBC layout to make the boards compatible with the MULTIBUS interface.

The iSBC 550 processor board contains a 5-MHz version of the 8088 microprocessor, 16k bytes of dynamic random access memory (RAM) dedicated for Ethernet program execution, and 8k bytes of programmable read only memory firmware that supports data link control and the MULTIBUS Interprocessor Protocol (MIP). An additional 8k-byte high speed static RAM is used to buffer transmitted and received data. The processor board provides the necessary commands and control to the SerDes board and receives status and data from it. All data transfers from the Ethernet data link control on the SerDes board are buffered through the 8k bytes of static RAM.

The SerDes board uses small scale integration and medium scale integration logic. It interfaces to the processor board, and through that to the MULTIBUS, but it does not attach directly to the MULTIBUS. The SerDes board accepts transmitted data from the processor board and sends received data to it. In addition, the SerDes board communicates with the processor board using three handshake signals: a "transmit request complete," a "receive request complete," and a "collision detect."

MIP and program interface

The iSBC 550 Ethernet controller contains firmware that supports the MIP interface. The MIP interface defines a pseudo-architecture by which processes executing on different single-board computers can communicate with one another in a reliable, controlled manner. Via MIP, systems consisting of heterogeneous sets of processors running heterogeneous realtime executives and application programs can communicate in a routine fashion.

MIP was created to permit multiple processors residing on the common MULTIBUS to work together

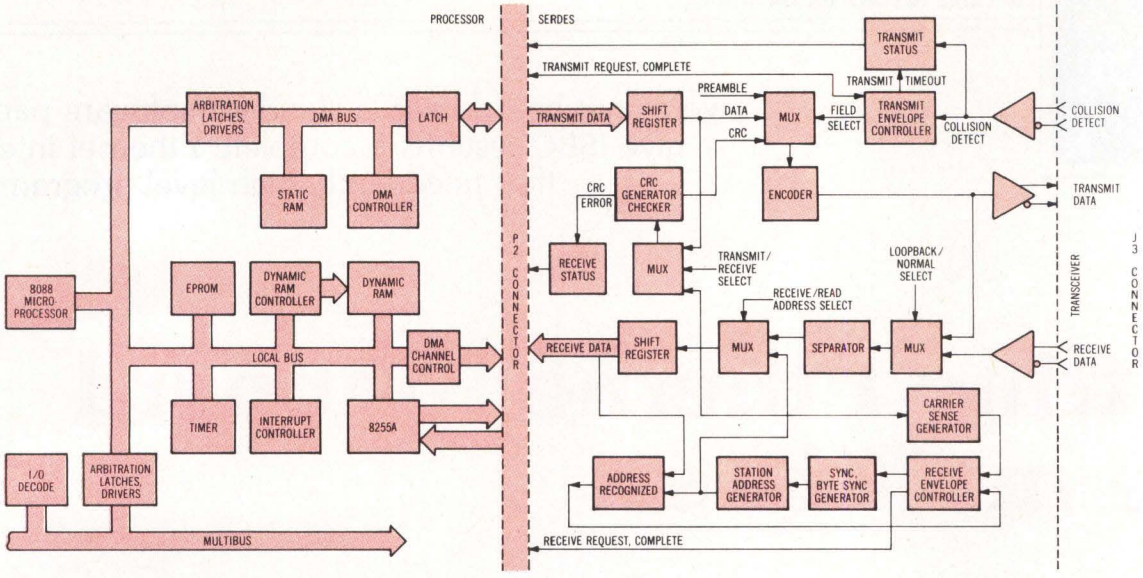

Fig 1 Ethernet controller block diagram. iSBC 550 consists of two boards. 8088 based processor board at left buffers packets and transfers them to system memory. SerDes board converts 8-bit parallel data into serial data, frames messages, and checks for errors

efficiently. A memory based, task-to-task communications protocol, MIP provides loosely-coupled multiprocessing on the MULTIBUS through communications supported by a uniform set of operating system interfaces. MULTIBUS Message Exchange software, iMMX 800, simplifies message transfer across the MULTIBUS. The software supports the addressing, data transfer control, and special memory management services required by such a loosely-coupled multiprocessor arrangement.

System configurations

The iSBC 550 controller and iMMX 800 software package can be used in conjunction with any of the iSBC 80/24, 80/30, 86/05, 86/12A, 88/25, or 88/40 boards to configure systems specialized for 8- or 16-bit processing environments, as well as special numeric processing. (See Fig 2.) Inserting the central processing unit, memory, special options boards, and the iSBC 550 controller into an iSBC cardcage completes the physical interface. Loading an iRMX operating system that includes iMMX 800 software modules satisfies most of the system software requirements. All that remains for the user to develop are four higher levels of communications software, as described in the Ethernet specification.

Ethernet controller firmware consists of commands and data that affect the control of message flow, message type recognition, and multicast addressing. For

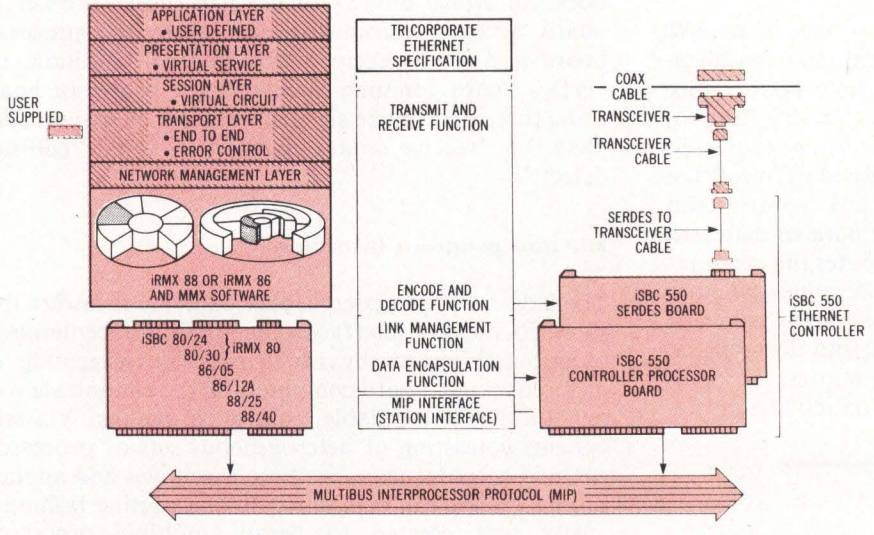

Fig 2 System configuration diagram. Adding iSBC 550 boards to cardcage completes physical interface for a variety of processors. With iMMX 800 to satisfy most software needs, only high level communication must be programmed

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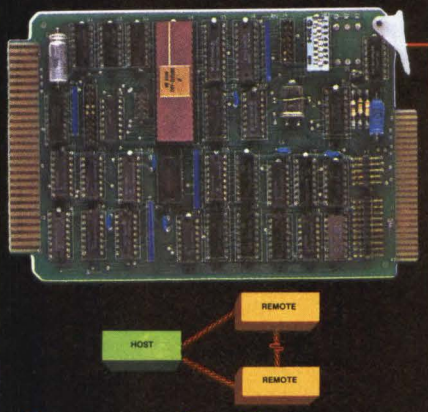

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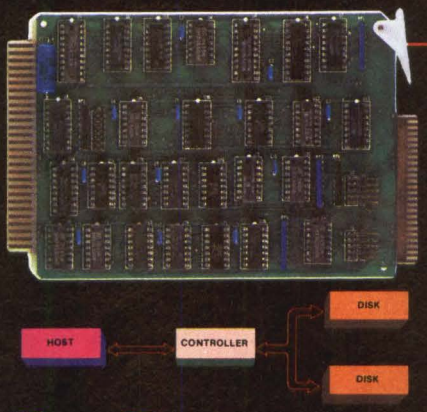

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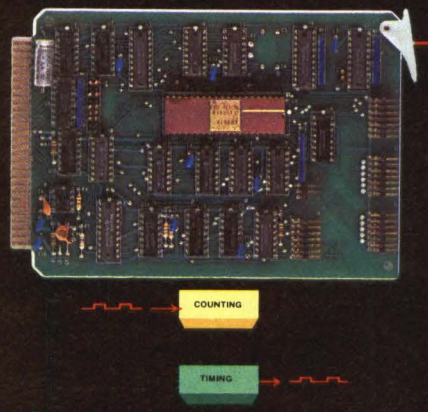

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Ethernet Local Area Networking

The Ethernet approach to local area networking was described first in the late 1970s, as a culmination of work by Robert Metcalfe and David Boggs at Xerox. A few years later, Intel, Digital Equipment, and Xerox Corp formally agreed to support the concept and jointly issued a set of Ethernet specifications. Published and distributed in September 1980, the Ethernet specification describes specific physical and electrical parameters for the hardware interface of compatible systems. It also describes a layered architecture of functional structures. Only the first two layers, the physical layer and the data link control layer, have been specified in detail. Four remaining, higher layers have not been defined beyond a functional description.

Physically, Ethernet transmits messages serially on 50-Ω coaxial cable. A cable segment can be up to 500 m long and connect up to 100 stations. Each station attaches to the coaxial cable via a transceiver system, through a cable that connects the transceiver to the station and cannot exceed 50 m in length. Messages are formatted into standard frames made up of octets, each 8 bits in length. Framing consists of a destination portion (6 octets), a source portion (6 octets), the message type (2 octets), data (46 to 1500 octets), and a frame check sequence (4 octets). Messages can be addressed to a single station, to all stations (broadcast), or to a number of selected stations (multicast). Signals are transmitted using Manchester encoding, a means of combining separate data and clock signals into a single, self-synchronizable data stream suitable for transmission on a serial channel.

Message data are transmitted at 10M bits/s. Only one station can transmit at a time. Therefore, Ethernet defines a collision-handling scheme that protects the bus from multiple-station access. Called carrier sense, multiple access with collision detection (CSMA/CD), the scheme ensures detection of multiple-access situations and aborts multiple-access transmissions. Stations retry at different times to avoid repeated collisions.

Because of the CSMA/CD approach, the bus access method can be strictly first-come, first-served. The advantage of this approach is that each station, through its controller subsystem, shares access to the cable without the need for a separate bus control system. Consequently, the communications network is not vulnerable to catastrophies caused by network control failure. Also, the circuitry is considerably easier to implement.

example, two commands control message flow: RECEIVE A MESSAGE and TRANSMIT A MESSAGE. Other commands pertain to network statistic counts, message types to be accepted, and multicast addressing. Firmware recognizes eight message types and up to eight multicast addresses.

Ethernet interface

The Ethernet specification calls out a maximum length for the coaxial cable and transceiver cables. In addition, the specification forces the transceivers to be extremely close (on the order of centimeters) to the coaxial cable to meet the capacitive loading parameters. Physically, the iSBC 550's SerDes board can connect to a supplied 22″ (56-cm) cable made up of four twisted pairs of wire. This cable is identical to the Ethernet transceiver cable in its connector, which attaches to the transceiver cable. One twisted pair carries message data to the transceiver, one carries data from the transceiver, one supports the collision detection scheme, and the last pair supplies power to the transceiver.

Messages to be transmitted pass from the iSBC 550 processor board to the SerDes board. After framing and cyclic redundancy check computation, the serialized data are sent via twisted pair to the transceiver. By this time, the data have been Manchester encoded and are converted by the transceiver into electrical signals whose characteristics (rise and fall times, amplitude, etc) are consistent with Ethernet specifications.

Data intended for a particular Ethernet station are received by the transceiver and sent back to the SerDes board for deserialization and transfer to the iSBC 550 processor board. The SerDes board then routes the message to the appropriate process based on the destination address and message-type information sent along with the message.

Conclusion

Putting Ethernet onboard the MULTIBUS was the first step in a cost-effective program that offers the standard Ethernet local area network protocol to original equipment manufacturers and volume end users. Like the iSBC, iRMX, and iMMX products, the iSBC 550 Ethernet controller can serve as a building block that provides a total application solution. Whether that application is prototyped on an Ethernet based Intellec development system or later developed for a component based system, the iSBC 550 offers an easy-to-use cornerstone for Ethernet networking.

About the Author:

Joseph P. Harakal is a product manager at Intel Corporation. His recent work experience includes product management for the iSBC 550 Ethernet communications controller, the iMMX 800 MULTIBUS message exchange software package, and the realtime multitasking executives iRMX 80 and iRMX 88. Mr Harakal holds an MS in computer science from Texas A & M University.

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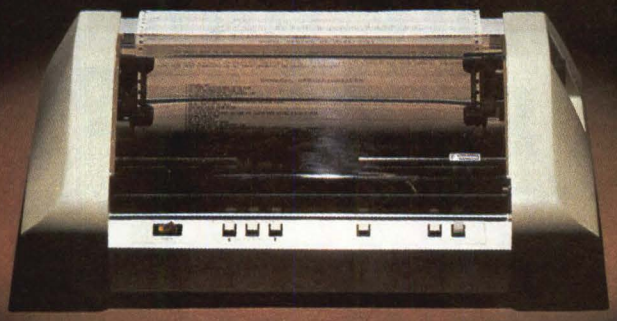

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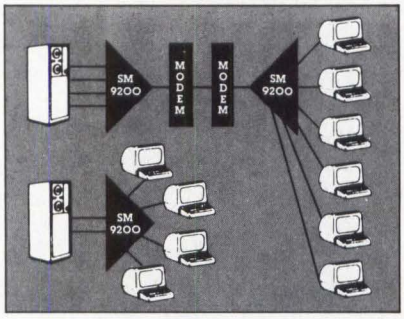

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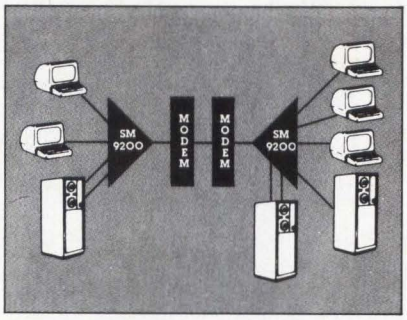

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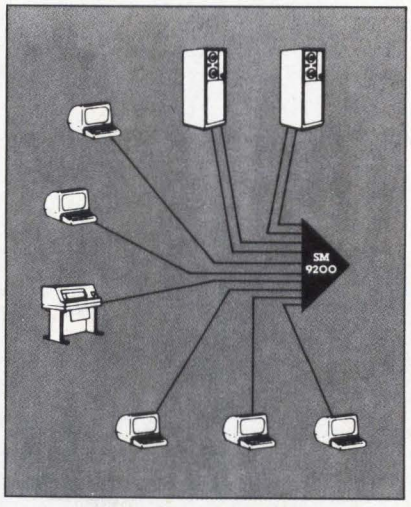

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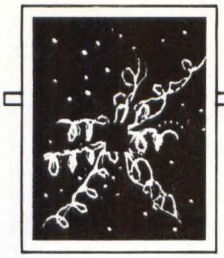

Communications between data processing devices using binary synchronous protocol is eased by use of a single-chip controller

Serial input/output controller implements binary synchronous communication

Developed by International Business Machines Corporation, binary synchronous protocol, or *bisync*, is a popular communication protocol used in the exchange of information between data processing devices. Bisync is a character oriented protocol; information is transmitted in blocks between two (or more) data communication devices. The data link is the medium through which this information is conveyed; a point to point data link that uses the ASCII transmission code is discussed here. Other codes, such as EBCDIC, are not covered, but the format for bisync is basically the same.

A data link consists of a master station (usually a computer) and a slave station (usually a terminal), as well as associated communication gear, ie, modems and phone lines. The master station controls message flow by polling and selecting the slave station. Polling involves sending a general request message to the slave station(s) to determine whether or not any of the slaves have data to send (traffic). If a slave station does have traffic, it responds to the poll, and the master can then select that particular slave for information exchange. Slaves can only respond to a master device and cannot initiate communication on a data link.

The Z80 serial input/output (SIO) controller represents here the flexibility and power available in a data link to implement the bisync protocol. The SIO facilitates bisync communication by performing the essential controller functions.

Controller functions

Functionally the SIO can be described from two different points of view: as a data communications device, it transmits and receives serial data in a wide variety of data communication protocols; as a Z80 family peripheral, it interacts with the Z80 central processing unit (CPU) and other peripheral circuits, sharing the data, address, and control buses, as well as being a component in the Z80 interrupt structure. A dual-channel

Mike Pitcher
Zilog
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data communication interface, its basic functions as a serial to parallel, parallel to serial converter/controller can be programmed by the CPU for a range of serial communication applications including computer to computer, terminal to computer, telecommunications, and process control.

The SIO supports all common asynchronous and synchronous protocols, byte or bit oriented, plus functions traditionally performed by the CPU. These functions are accomplished via the two fully independent channels, with an interrupt structure that allows fast data transfers.

As a peripheral to other microprocessors, the SIO offers features such as non-vectored interrupts, polling, and handshake capability. Fig 1 illustrates the conventional devices replaced by the single-chip SIO. Full interfacing is provided for CPU or direct memory access (DMA) control. In addition to data communication, the circuit can handle SIO with fast (or slow) data communications devices. While designed primarily as a member of the Z80 family, it is well suited to other CPUs. Packaged in a 40-pin plastic or ceramic dual inline package (DIP), the N-channel, silicon gate, depletion load device uses a single 5-V power supply and the standard Z80 family single-phase clock.

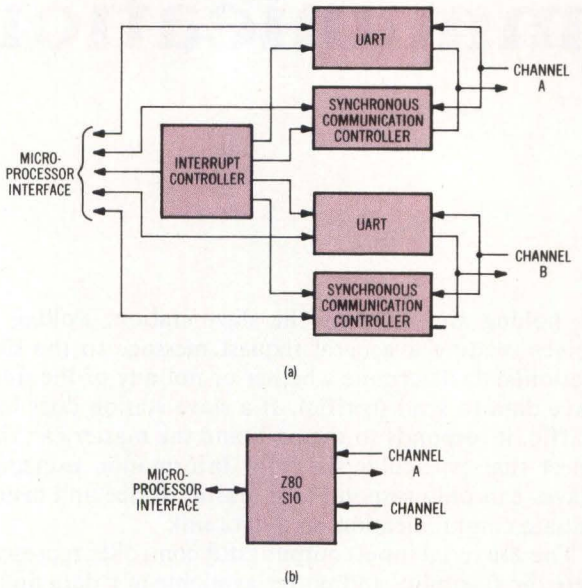

Fig 1 Block diagram of conventional devices replaced by Z80 SIO (a). Single-chip SIO provides two independent full-duplex channels that can be programmed for asynchronous or synchronous protocols including bisync (b)

Internal structure

Internal structure of the device includes a Z80 CPU interface, internal control, and interrupt logic. Each of the two full-duplex channels contains its own set of control and status (write and read) registers, and control and status logic that provide the interface to modems or other external devices.

The register group includes five write-only 8-bit control registers, two write-only sync-character registers, and two read-only status registers; the interrupt vector is written into an additional 8-bit register in Channel B that may be read through another 8-bit register also in Channel B. Bit assignment and functional grouping of each register is configured to streamline the programming process.

Logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. Modem control inputs, Clear to Send and Data Carrier Detect, are monitored by the external control and status logic under program control. All external control-and-status-logic signals are general purpose in nature and can be used for functions other than modem control.

Bisync basics

The SIO provides an efficient means of communication between data processing devices using the bisync protocol. Since bisync is one of the most common protocols used in modern communications, a discussion of the bisync protocol is now appropriate.

A unique feature of the bisync protocol is the message block. Message blocks consist of a header, body, and trailer (Fig 2). The header is made up of two or more sync (SYN) characters (hence the name bisync), a start of header (SOH) character, and addressing and control information for a particular slave station.

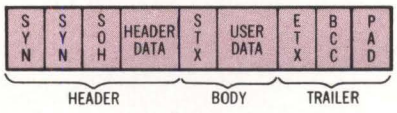

Fig 2 Basic message block format for bisync protocol. Header is composed of two or more SYN characters

Beginning with a start of text (STX) character and encompassing the entire text information, the body generally contains ASCII text data, although 8-bit binary data can be transmitted using transparent text mode. The trailer contains the end of text (ETX) character and the block check character (BCC), which is used for detecting errors through a cyclic redundancy code (CRC) or longitudinal redundancy checking (LRC).[1,2]

Error detection is essential when transferring information between data processing equipment. Since ASCII specifies only seven bits for its code, the eighth bit is used for vertical redundancy checking (VRC), more commonly known as character parity, which in synchronous communications is generally odd, and in asynchronous communications, even. Fig 3 shows typical ASCII characters with parity. The SIO can be programmed for 7-bit characters with odd parity enabled to

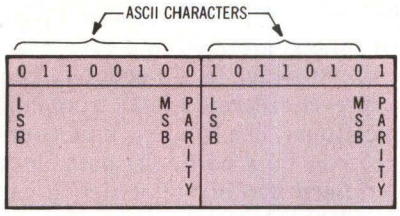

Fig 3 Two ASCII characters with parity; example of odd character parity or vertical redundancy checking. Number of 1s should be odd

minimize software overhead. Because VRC applies only to the individual character, the entire message block has an LRC, a simple bit position checksum where the number of 1s for each position (0 through 6) is even for a block of data, that makes up the BCC. Since the BCC is a character, LRC, which includes all characters, except SYN, starting with the first character after SOH or STX and up to and including ETX in the trailer (Fig 4), is subject to the same character parity rules as the rest of the data block. The SIO cannot calculate the LRC, leaving the task to the user. LRC can be generated on a microprocessor with little effort by taking the message block and XORing the data with an initial value of zero to provide even LRC.

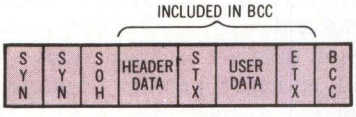

Fig 4 Characters included in BCC

SIO bisync applications

Both byte oriented and bit oriented synchronous communications are supported by the Z80 SIO. Synchronous byte oriented protocols can be handled in modes that allow character synchronization with an 8-bit sync character, any 16-bit sync pattern (bisync), or an external sync signal. Leading sync characters can be removed without interrupting the CPU. The SIO also supports CRC error checking. Receiver CRC accumulation for synchronous byte oriented modes is delayed by one character time so that the CPU may disable CRC accumulation on specific characters. Both CRC-16 and CCITT (International Consultative Committee for Telephone and Telegraph) error checking polynomials are supported.

The internal structure of the SIO includes a CPU interface, internal control and interrupt logic, and two independent, full-duplex channels. Each channel contains its own set of control and status (write and read) registers, and control and status logic that provides the interface to modems or other external devices. A typical application is shown in Fig 5. Registers for each channel are designated as follows: write registers 0 through 7 are WR0-WR7, and read registers 0 through 2 are RR0-RR2. Two special cases of the bisync protocol in which the SIO can be used are the transparent text mode and error recovery procedures.

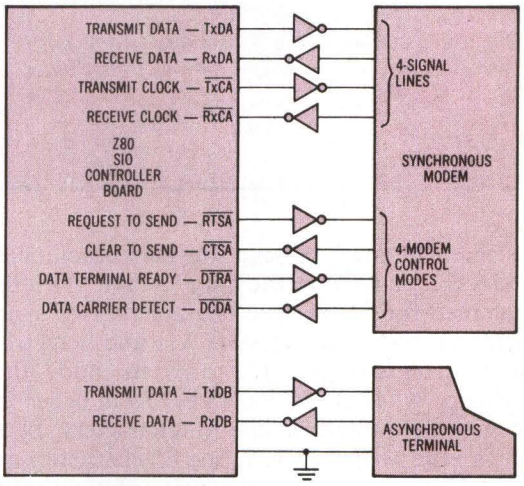

Fig 5 Typical Z80 SIO bisync application. SIO has two full-duplex channels. Each channel has own set of control and read and write registers

Transparent text mode

Transparent text mode is useful in bisync when information exchanged between master and slave is not ASCII data. For example, a binary data file (object program) might be sent from master to slave. ASCII transmission code is only seven bits long, making it difficult to send 8-bit binary data.

Bisync protocol has provisions for sending 8-bit binary data by using transparent text mode transmission. In this mode, character parity is disabled, allowing the full eight bits to be used for data. However, to allow control within the constraints of the protocol, there are certain limitations on the binary data pattern; during transparent mode, some communication control characters are preceded by a data link escape (DLE) character, actually making the control characters a 2-character sequence. To distinguish a data byte from a control DLE, the protocol specifies the insertion of another DLE. The receiver then throws away the first DLE, keeping the second as data. Table 1 shows the communication control characters that are valid during transparent mode.

Another character change occurs when the SYN character is used for line fill. Normally, the SYN character is ignored, but during transparent mode the SYN is preceded by a DLE, and both are consequently ignored by the receiver. In the event that the CPU does not

TABLE 1

Control Codes Used in Transparent Mode

DLE	STX	Start of transparent text
DLE	ETB	End of transparent text block
DLE	ETX	End of transparent text
DLE	SYN	Idle sync
DLE	ENQ	Enquiry
DLE	DLE	DLE data
DLE	SOH	Start of transparent header

have a character ready to send, the SIO automatically inserts SYN characters into the data stream. With the SIO programmed for 16-bit sync characters, two syncs are sent from the SIO (write registers WR6 and WR7) when its transmit buffer is empty. In transparent mode, the user must change WR6 and WR7 to DLE, SYN in order for the SIO to provide the proper line fill characters. In accordance with the ANSI standard, line fill characters are not included in the SIO CRC calculation during transmit. During reception in transparent mode, the software must disable CRC accumulation when the DLE SYN character sequence is detected.

In transparent mode, the user must also be concerned with the error detection codes. If parity is enabled in the SIO normally, it must be disabled during transparent mode. This change in SIO operation affects both transmit and receive and should therefore be considered if using full duplex.

Since the SIO allows CRC enable/disable on the fly, the software can easily control CRC accumulation in both receive and transmit. During transmit, the CRC must be enabled/disabled before the character is transferred into the serial shift register. During receive the CRC accumulation is delayed eight bits. After the character is transferred from the serial shift register into the buffer, the user has to read that character, decide whether or not to continue CRC accumulation, and disable/enable CRC before the next character is transferred to the buffer. This is not generally a problem, since character transfers occur every 833 ms at 9600 baud. Table 2 shows the characters included and omitted in the CRC during transparent mode.

When CRC accumulation is to be resumed, the software should enable CRC before the desired character is transferred to the receive buffer. Suppose, for example, that a DLE pair is received during transparent text mode. The SIO generates an interrupt when the first DLE is transferred to the receive buffer. The driver program reads the DLE and immediately disables CRC. When the next interrupt occurs, the driver reads the second DLE and immediately enables CRC to include the second DLE into the CRC accumulation.

Error recovery

Recovery procedures provide a means of preventing data link instability. The recovery mechanism consists mainly of timers, grouped into four basic areas, and a negative acknowledge (NAK) counter. The NAK counter is used to prevent repeated NAKs from inhibiting further communications. The sending unit counts how many NAKs it receives for a particular data block so that after a predetermined number of retries, it can recover and pursue another course of action. The particular count value and course of action taken when the count expires are left up to the user.

Four software or hardware timers (timer A, or response timer; timer B, or receiver timer; timer C, or gross timer; and timer D, or no activity timer) prevent the data link from getting "hung" or going idle for extended periods of time. Generally, the shortest interval is used with timer A, and the longest interval is used with timer D. For maximum system efficiency, however, the receiver timer (B) should timeout before the response timer (A). The particular implementation of these timers varies from system to system, and some flexibility of exact timer values is left up to the user.

Since it is assumed that interrupts will be used with the SIO, an interrupt driven receiver timer count is kept in memory and is reinitialized each time a character is received (receive interrupt). The same applies to the response timer, except that when a timeout occurs, the transmit driver can respond in one of two ways. If the SIO is set to transmit CRC on transmit underrun, then the driver could simply set its flags and not fill the buffer. This allows a normal exit, since the SIO will then send its CRC bytes. If, on the other hand, the SIO is set to not transmit CRC on transmit underrun, then it sends sync characters (SYN SYN or DLE SYN, whichever was last written to WR6 and WR7) until the transmit buffer is filled or transmit data are set to marking.

In any event, enough time must be allowed after CRC is sent so that the receiver can properly decode CRC. Because of the character delay within the SIO during CRC accumulation, about 20 clock cycles are necessary after

TABLE 2

Characters Included and Omitted During Transparent Mode

Omitted from CRC		Included in CRC
DLE	SYN	DLE of DLE DLE
DLE	SOH	ETX of DLE ETX
DLE	STX[1]	ETB of DLE ETB
		STX of DLE STX[2]

[1]If not preceded by transparent header within same block

[2]If preceded by DLE SOH within same block

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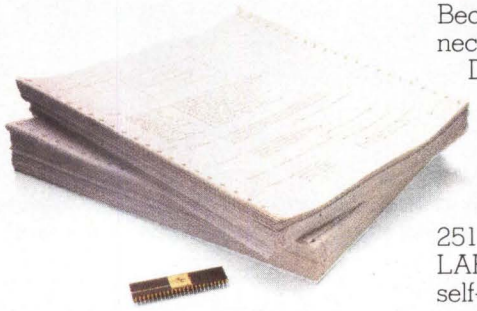

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the last CRC byte is sent to ensure adequate decoding time. The SIO could be programmed to send pad characters either by disabling parity and sending 8-bit FFs (hex) or by filling WR6 and WR7 with FF hex. If enabled, the SIO automatically sends whatever is in its sync registers upon transmit underrun. Multiple message blocks do not have to be separated by pad or sync characters as long as CRC is valid for the previous message block. However, to ensure adequate time for the receiver to process CRC, it is recommended that at least two pad characters follow the last character of a block.

Summary

Using the Z80 SIO for the bisync protocol is fairly straightforward. Although use of the SIO in the transparent text mode requires care, the implementation is greatly simplified by the SIO's flexibility, as compared with other serial communications ICs. The CRC capabilities of the SIO provide a powerful means of maintaining maximum data integrity with minimum software overhead. The user will find the SIO, coupled with the DMA and the interrupt capabilities of the Z80 processor, well suited for meeting most data communications needs.

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1. American National Standards Institute, ANSI X3.28, 1976
2. "General Information—Binary Synchronous Communications," IBM publication number GA27-3004-2, 1970

About the Author:

Mike Pitcher has been working in the computer industry since 1974, with a particular interest in distributed intelligence and data communications. As an applications engineer at Zilog, he is currently designing hardware and software for projects using Zilog components. He received his education at the Georgia Institute of Technology in Atlanta, Georgia.

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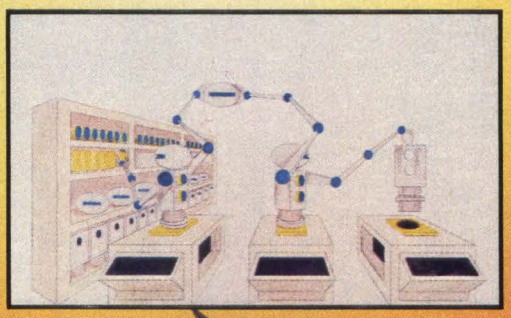

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Software maintenance activities support the evolution of a system and its software to meet the changing requirements of its users and their environment

Designing software for maintainability

For the last ten years, considerable attention has been given to methods for developing software that would reduce its cost while increasing its reliability. The goal for software technology has been to produce the perfect program—fulfilling all of the system's requirements, without error. Even if this can be achieved, it won't be enough! Software will still require maintenance. In fact, it has been claimed that at least 50% of the cost of a system's hardware and software is due to software maintenance, and that percentage is rising.[1]

Many people view the increased cost of software maintenance compared to cost of development as an alarming trend that must be curbed. Cited frequently is the even more ominous comparison of $75 per instruction for software development versus $4000 per instruction for maintenance.[2] To understand the significance of maintenance cost in the life cycle of a system and to control that cost, we must first understand how maintenance money is being spent.

What is software maintenance?

Software maintenance is the phase in the life cycle of a system that follows software development. It is the period of time from the delivery of the system to its first user until the system is no longer used. Software maintenance is also the set of activities performed on the software during the system's maintenance phase. Normally, "maintenance" signifies making repairs to a system to keep it running according to its original specifications. In contrast, "software maintenance" is used to signify both making repairs and improving the *system*, including hardware as well as software. In fact, one of the major reasons for selecting software rather than hardware to implement a system's functions is to allow for the option of changing the system by changing just its software. The high cost of software maintenance may indicate a conscious choice made by system designers to effect a significant reduction in the cost of system maintenance. An example is the modification of the F-111's weapons system. There were two versions of the system to be changed, one implemented in hardware and the other in software. It cost $8,000,000 and 78 months to complete the modification to the ballistics function in hardware as opposed to $20,000 and 15 months for a comparable change in software.[3] The difference was attributed to the time and cost of producing modification kits for hardware and installing them in aircraft.

Software maintenance is performed to repair, to adapt, and to improve a system. Repairs are usually high priority changes that must be made to the software including correction of errors inherited from the development phase and errors introduced during the maintenance process; and correction of other kinds of system deficiencies such as operational procedures, malfunctioning equipment, and internal software structure. Adaptations, while necessary, can usually be planned and scheduled without the urgency of repairs. Some adaptations are necessitated by situations external

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Software Maintenance Planning Factors

Before planning for software maintenance, it is useful to define goals, to determine what resources are needed, and to understand what factors affect software maintenance cost. Goals specify which factors a plan is optimizing; different goals lead to different plans. The following are examples of goals for a system life cycle that affect the cost of software maintenance. The first set minimizes some part of life cycle costs.

Minimize development cost—In this case, no expenditures are made during development which might reduce maintenance costs. This goal is used by a developer who has no responsibility for maintenance and wishes to maximize his profit. It is a valid goal for a system that will only be used for a short time or will not be altered.

Minimize maintenance cost—In this case, additional cost may be incurred prior to maintenance in order to reduce expenditures during the maintenance phase. This goal might be selected when a system will have many installations or users, and changes must be handled economically over a long period of time. One obvious example is the design of an operating system to facilitate its installation and adaptation to different equipment configurations. This goal is also appropriate when software is installed within systems or at locations where it is difficult to make modifications. In programming organizations, minimization of maintenance costs can free more people for new system development.

Minimize operating cost—In this case, software maintenance costs may be high because they offset the even higher cost of replacing equipment or using additional people.

Minimize life cycle costs—This goal requires a balancing of development and maintenance costs to minimize the total. At this time, it is not known precisely how to do this, although some actions are known that ought to help.

This second set of goals maximizes the utility of a system.

Maximize availability and reliability of a system—There are systems in which downtime cannot be easily tolerated. Examples are realtime systems such as a process control system or an air traffic control system. Any "man rated" system where a processing error can cause loss of life requires particularly high reliability. These requirements transcend the cost of maintenance per se.

Adapt to user needs—There are situations in which the cost of changing a system's software is secondary to the goal of providing new capabilities to users. One such case is a vendor who sells or leases hardware along with the software, gaining a profit from the hardware as long as users like the software.

Deliver early and plan for enhancement—This is the evolutionary approach. The initial capability is deliberately minimal, as is the development cost. The system user receives an operational, useful system earlier and can influence the definition of later increments of capability based on operational experience. In this case, higher maintenance costs can be anticipated, especially when compared to development costs. These costs can be justified when the system evolves in closer coordination with the desires and needs of the user. In contrast, a system that is delivered with the wrong set of capabilities for a user, because he did not know what would be most useful at the time of development, is likely to have a high development and maintenance cost, or a very short life.

The last goal is one that is not usually intended, but occurs nonetheless when software is late.

Meet development schedules and sacrifice quality—There are times when delivery of a system is paramount to other considerations such as completion of implementation or thorough testing. Anything can slip but the delivery date. Justifications include interfaces with other systems, other key decisions that must be based on operation, and unavailability of funding or personnel after a specified date. The effect on maintenance of a schedule-driven development depends on whether the system is ever used. If there is a maintenance phase, it is likely to be more costly if the development was chaotically truncated to meet a time commitment.

to a system or its software, such as changes in the interfaces to other systems, changes in equipment including computer hardware, and changes in the form or content of data inputs and outputs. Improvements are optional changes. They can be studied for cost-effectiveness, prioritized, and scheduled by the managers of maintenance. Examples include user requested enhancements and modifications needed to increase system efficiency or to reduce operating cost.

Recent surveys of data processing installations[4,5] measured the distribution of effort in each area of software maintenance and found that 20% to 30% of the total was spent on repairs (12% were emergencies), 20% was used for adaptation, and between 50% and 60% of the total was spent on improvements (40% were user requested enhancements). All three categories involve changing the software. To make changes, it is necessary to identify those parts of the software to be changed, and then *re*design, *re*code, *re*test, and *re*document. This would imply that software maintenance is the same as software development. Software maintenance and software development are similar but not the same.

Recognition of the differences can help in planning for and influencing the cost of software maintenance.

How does software maintenance differ from software development?

Perhaps the major difference between software maintenance and software development is that software development takes place first. Also, maintenance begins with a different baseline, and fewer options are available because the important design decisions have already been made. Resources available for maintenance tend to be fewer than those available for development and are often inadequate for making changes. This is especially true of memory space in minicomputers. The system must be changed while remaining compatible with the existing environment, operational procedures, and resources.

The environment in which maintenance is performed can be different from that of development. The highest maintenance priority is to keep the system running smoothly for its users. While the system is being developed, however, it belongs to the developers who can establish their own priorities. Having system users also means having reports on system faults or errors. It has been observed that with each new release of a system comes a flurry of reports on errors undetected by the testing process. Due to the lack of instrumentation to log system and user operations, it can be difficult to collect data needed to isolate the origin of an error or to reproduce the conditions that caused the error. Hardware systems and equipment often include built-in instrumentation for detecting and diagnosing errors during normal operation; software designers also have such tools and control the use of the system during tests so that error-causing conditions can be reproduced; but software maintenance personnel do not usually have the luxury of built-in instrumentation during normal operations.

In addition to the lack of data about system malfunctions, maintenance personnel often have difficulty obtaining knowledge of the software. This knowledge must be transferred from those who built the software to those who maintain it. While a system is being developed, knowledge accumulates gradually during the design and implementation processes. Because the total system exists when it is being maintained, the problem is to discover the relationship of the parts to the whole system behavior and to each other. Even well-documented systems tend to indicate only what they contain, not the reasons for key design decisions. This makes it difficult to predict the effect that a change in one part of a system will have on the rest of the system.

Another significant difference between development and maintenance is the technical status of the software. Many large systems take considerable time to develop and may be in their maintenance phase for an even longer period of time. As a result, systems under maintenance may become obsolete, and maintenance personnel work with systems that are well behind the state of the art in hardware and software and are, hence, more costly to maintain. With this time lag, it becomes increasingly difficult to find people trained to maintain a system that uses obsolete techniques and tools, and to motivate people to do that work.

Software changes made during development can be different from those made during maintenance. Development builds the system; maintenance can destroy it. One of the few detailed published studies of the effect that software maintenance has on a large system is an analysis of approximately 20 releases of IBM's OS/360 over a 12-year period.[6,7] A few simple measures were taken such as the total number of modules, the time, and the number of modules "handled" per release. Data indicated "a general upward trend in the size, complexity, and cost of the system and the maintenance process."

Three laws of "Program Evolution Dynamics" were used to describe the effect of software maintenance on the system. The Law of Continuing Change needs no explanation. Maintenance is change. While the IBM study did not provide quantitative data, other studies give some idea of the extent of change. Daly cites a system in which 70% of the code was changed in the first two years of maintenance.[8] The average life of a line of code was 18 months. In another study of 1.9 million lines of code, the average life of a line of code was 31 months.[9]

"Development builds the system; maintenance can destroy it."

The Law of Increasing Entropy states that as a software system changes, it deteriorates. In the IBM study, this decay was evidenced by an increase in the time needed to make changes and in the cost of those changes. Another study showed that maintenance was 12% of the system cost after one year, and 46% after four years.[10] The complexity of the system also increased, as indicated by the ratio of modules handled per release to the number of modules in the system before the new release. Growth in number of modules was accompanied by increased interdependence among modules because of the growing number of intermodule (global) references. The maintenance effort or "work input rate," defined as the number of modules changed per unit of time, remained constant.

Under the Law of Statistically Smooth Growth, the maintenance process is observed to be self-limiting. The system continues to grow from one release to the next until its structure becomes too unstable or the effort too great to make the next set of changes. At this point, effort is concentrated on internal changes to the software which provide no directly visible enhancements to users but reduce the size of the system and clean up its structure. Locally, growth between releases might be erratic, but the long term pattern is smoothed by limits of the system itself and by the policies of the organization that manages the system.

The IBM study of the OS/360 indicates the necessity of maintaining and repairing the internal structure of software as it undergoes change even if it was well-structured initially. This activity competes for maintenance resources with activities to provide user enhancements. To underscore the importance of planning for software maintenance as distinct from software development, the differences between software development and software maintenance have been somewhat exaggerated. However, the two activities are not independent; system life cycle planning must consider the interplay between them.

Planning for software maintenance

Activities that can make maintenance of software easier and more efficient span both the development and maintenance phases of the software life cycle. Their common theme is the process of changing software. If software maintenance is making changes, then software development must anticipate changes. This is true for the design of a system as well as its software, since the system design includes the allocation of hardware resources to software. For example, inadequate computer memory capacity, and the inability to add more, has been a frequent difficulty in weapon systems. When space is exhausted, it can be a complex, costly, error-prone process to rewrite software in order to recapture space needed for implementing changes or new system capabilities. Sometimes it is possible to obtain space by offloading functions and/or data from one computer to others that are introduced into the system for just this purpose. Designing for change should keep open the option to expand memory and even computing capacity in some systems.

Design for change

In the design of software, widely advocated software engineering techniques are consonant with the objective of designing for change. Top-down design principles encourage design decisions to be made in steps from the abstract, more flexible stage to the detailed, less flexible stage. The more abstract stages are machine and configuration independent. Implementations can result which provide equivalent capabilities although a different programming language, operating system, or computer may be used. Modularity supports flexibility when those portions of the system that are most likely to change can be encapsulated in modules so that their modification will have minimum impact on the rest of the system. Greater flexibility in systems can also be achieved if optimization is introduced into the design as late as possible and if the design is documented first. Optimization tends to obscure the design and make an implementation resistant to change.

An approach to designing software for ease of extension and contraction is given in a paper by Parnas,[11] who advocates designing a family of programs rather than a single program. Members of the family may be future versions of a system, increments to be delivered over time, or versions tailored for specific users. The first step in Parnas' methodology affects the definition of requirements. Identifying possible subsets of the requirements, beginning with the minimal subset and adding minimal increments, will lead to a more flexible system design, even though the subsets are not separately implemented. As Parnas points out, this principle is especially useful for government acquisitions since specification of requirements is an acceptable role for government buyers. The other steps in the design of flexible software influence how the software is developed and are usually the prerogative of the developer. They involve the rules of selecting modules, the principles used in specifying and refining design, and the nature of relationships or dependencies among modules.

Document for change

It is not sufficient to merely design systems for change. Designs must be communicated from the development personnel to the maintenance personnel. The key to good maintenance documentation is not the amount produced but the kind. Overdocumentation has two dangers: it is costly to generate and costly to use too much documentation. Daly suggests limiting documentation to that which can be maintained after the system is in use.[12] Any documentation that is not maintained becomes a source of misinformation leading to errors.

"The key to good maintenance documentation is not the amount produced, but the kind."

In order to understand how to document changing system software, it is useful to examine the kinds of changes that software can undergo. When a system is viewed as a collection of interacting modules, the design of the system can be documented in terms of the interfaces of its modules and the connections among them. An interface defines what functions a module performs, what are its expected inputs, what outputs it generates, and what resources it uses, including data and other modules. The latter resources are the connections or intermodule dependencies. A module is any separate system component from a small subroutine to a major subsystem, which can be distributed on different computers, and can, itself, consist of modules.

A system is defined by its implementation as well as its design. An implementation is the coded software that is specific to a hardware and software configuration and uses a particular programming language. Consider some of the combinations of software that are possible as families of systems are generated and maintained:

Resources for Software Maintenance

Planning involves providing resources to perform maintenance. The resources can be grouped into five primary categories. Key issues are shown for each category.

Products of Development—The two products of development are the software and its documentation. These are obviously the substance on which maintenance operates. Planning issues include the following: What kinds of documentation will be delivered? How and when will the products be transferred to the maintenance organization? What is acceptable quality? How will it be determined?

Support Facilities—These resources include computer hardware, equipment, and software needed to test a software system. Tools to aid in software maintenance are represented by hardware performance monitors, compilers, simulators, test data generators, and editors for entering data. Planning issues include: What equipment and hardware will be required? Where should they be located? Should facilities for maintenance be the same or different from the development facilities or the operational facilities? Should some facilities be shared among similar systems?

Procedures—Important resources for system maintenance are the procedures used to generate software, to train personnel, and to manage the maintenance effort. The procedures for generating software are design, coding, and documentation standards and conventions. Management procedures include control of modifications; monitoring status; and reporting of errors, change requests, and resource status. Planning should address which procedures should be established before maintenance and how procedures should make the transition from development to maintenance.

People—Maintenance is labor intensive. People can be characterized by the organization to which they belong, their knowledge of the system, and their technical skills. Among the planning issues are: What organization will be responsible for maintenance? Are the same people used for both development and maintenance? Will they maintain only one or several systems? How will they be trained?

Funds—The source of funds and the amount available or required must be established. The way in which funding must be justified, and the time it takes to obtain it must be considered long before maintenance begins.

Cost Factors for Software Maintenance

While precise quantitative cost relationships are not known, the relationship of certain system attributes to maintenance cost is apparent.

Application—The size of the system determines how much must be known in order to make changes to it. The complexity of the system, measured in terms of number of external and internal interfaces, also affects ease of understanding the system and modifying it. The stability of requirements originally implemented will determine both the frequency of change requests and the kinds of changes that may occur during maintenance.

Development—The quality of the software and documentation produced during the development phase will determine how much repair of development errors is needed, how easily the software can be understood, and how difficult it is to change. Many of the resources used for development can be transferred to maintenance, eg, people and support facilities. This transition positively affects both the expenditures for similar capabilities in the maintenance phase and the efficiency of the maintenance process.

Operation—There are variations in the use of a system that affect maintenance costs. The number of users and frequency of use can influence the number of requests for changes; the number of installations can affect the number of versions of a system that must be maintained; and the reliability and availability requirements will determine how much testing must be done to remove errors or assure reliability.

Maintenance—The quality of the staff, the tools available, and the management procedures can affect the cost of maintenance.

Funding—Although listed last, funding is the driving factor in maintenance cost. What gets done and how long it takes to do it are determined by how much money is available; whatever the amount, it will always be spent.

A module can consist of one interface definition and more than one source code implementation, eg, a released and an experimental version for which the interface is unchanged.

A module can consist of one implementation and more than one interface definition, eg, when different systems use subsets of the module's capabilities.

Different systems can be constructed from different subsets of the available modules as long as a subset is complete, with all of its required connections present. For example, an operating system can have different subsets for different configurations of hardware.

Different systems can be constructed from different versions of the implementations of modules, eg, a released system and a development version not ready for release, or a version for one computer and a version for another.

In order to maintain changing software, relationships must be documented. This includes:

the relationship of externally observable behavior to the modules causing that behavior;

the intermodule dependencies, including data as well as function;

the relationship of various levels of design decisions to their ultimate implementation in code, so that maintenance personnel can retreat to a more abstract level and redesign a new member of the family;

the versions of source code associated with any given version of a system;

the differences between one version of a module, or a system, and subsequent versions; and,

the relationships among the components of documentation so one can move among them to understand why things happen, where they happen, and how they can be changed.

Fulfillment of these documentation requirements may mean that detailed documentation local to modules is unnecessary, since it can be derived directly from the code. Nonetheless, there can be a large volume of documentation to generate and to maintain as a system changes.

Manage change

A new class of automated aids is supporting the management of software changes. The aids are made possible by using the computer to create, store, and present all kinds of documentation in addition to the software. Text editors and word processors are becoming commonplace tools for text handling. Database management systems can process and organize items of information. With modest additions, these tools can be used to generate, modify, coordinate, and control source code and other related software documentation.

"A new class of automated aids is supporting the management of software changes."

Text editors are the simplest kinds of automated aids for maintenance of many versions of modules and systems. The next level of automation can provide configuration control by uniquely identifying and dating each version of a text entry, identifying what changes have been made, providing audit trails between updates so that one can roll back to a prior version, and controlling access to the text so that unauthorized changes cannot be made. The Programmer's Workbench of Bell Laboratories is a well-known system of this kind.[13]

Much greater power can be achieved in a programming environment for managing change when the documentation can be automatically analyzed. Formal specification of module interfaces and interconnections, either as part of a programming language or as a separate language, makes this information available to provide the following additional automated services.

Systems can be constructed from a user definition of a basic set, and the set automatically derived from the formal specification of intermodule dependencies.

Systems can be automatically reconstructed by an analysis of the parts of a system that are affected by a set of modifications.

Consistency checks can be made across modules based on interface definitions.

Completeness checks can be made on the composition of a system to see that the resources used by all of the modules have been included.

There are a number of programming environments that can provide services like those listed above. Examples are the Program Development System at Harvard,[14] INTERCOL at Carnegie-Mellon University,[15] Mesa at Xerox PARC,[16] and a system called Gandalf being developed at Carnegie-Mellon for the Ada language. These particular systems are not yet widely used or available commercially. However, they do not appear to be difficult to implement. The choice of a formal language to define module interconnections and the implementation of its translator is probably the major effort. Automated aids such as these are useful for supporting development and maintenance of large, centralized systems containing many components or utilizing many people for their software development and maintenance. The services of these automated aids can be extended to the management of distributed systems, where the nodes may be separately specified and maintained but coordination and maintenance of interfaces is critical to the operation of the collection of nodes.

The future of software maintenance

There are a number of trends in computer technology that may affect the future of software maintenance.

Increased availability of tools

The great expense of producing automated aids for software development and maintenance has prevented all but the largest systems or programming environments from acquiring many tools. The efforts to standardize Ada as a programming language have included plans for the definition, design, and development of an integrated set of tools for all users of Ada.[17] Another technology effort, sponsored by the Air Force's Rome Air Development Center, is the National Software Works, which will provide these tools to remotely located users via the ARPANET.

Quantitative measures of maintainability

If quantitative measures can be devised that predict the difficulty of maintaining software from observations of its design and code, then software might be developed that will be easier to maintain. There are many embryonic attempts to devise such quantitative measures. The attributes being measured include reliability, testability, understandability, and modifiability.

Monitoring the maintenance process

The IBM[18] study showed how a few simple data points for each release of a system could reveal the dynamics of software maintenance. These and other quantitative measures will be used to learn how to improve the

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management of software maintenance. Data similar to those of the IBM study might show when a new release is needed, when the system must be restructured, and when the system is too expensive to change any further. Other data should monitor the quality of the maintenance effort and provide data to help estimate the cost of maintenance.

Higher level software

The ideal way to generate software would be directly from the specifications for its component interfaces and the data transformations to be performed by its processing. Such specifications would not have to be algorithmic (procedural). If one assumes that error-free software is automatically generated from the specifications, the maintenance process is reduced to identifying changes in specifications and modifying them. There have been some practical steps in the direction of "automatic programming," especially in business applications.[19,20]

Conclusions

Software maintenance is much more than correcting problems created by poor software development. It supports the evolution of a system and its software to meet the changing requirements of its users and their environment. High software maintenance costs incurred during this evolution are not inherently bad if they represent the successful extension, adaptation, and utilization of existing sysems and their software. By planning for software maintenance early in the system life cycle, unnecessary costs and delays can be avoided. In fact, the right actions taken during the development phase can benefit both development and maintenance of software.

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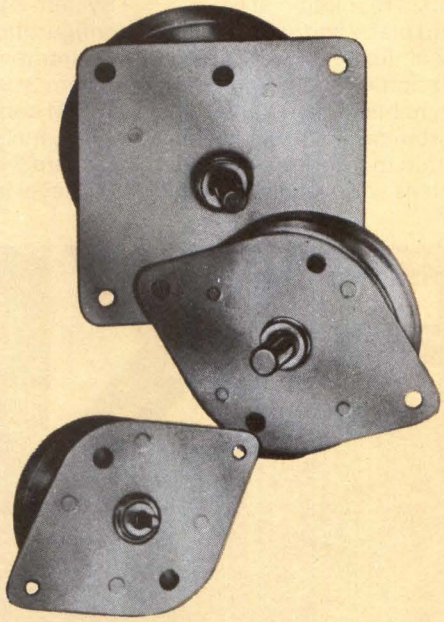

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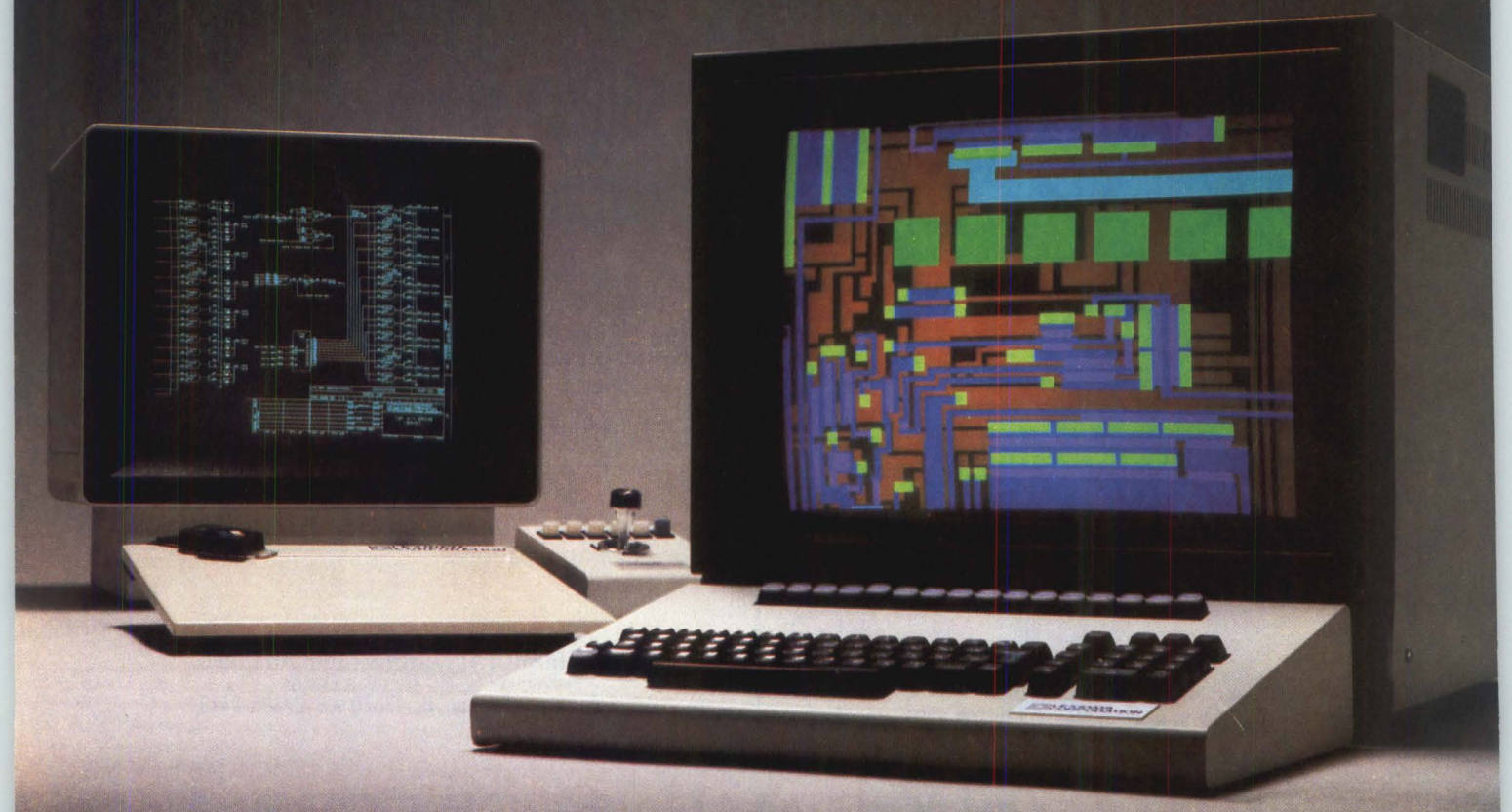

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Array processor interfacing techniques capitalize on architectural features for a tenfold improvement in minicomputer performance

Greater throughput with multiple array processors

Connected to minicomputers as peripheral devices, array processors can speed up iterative arithmetic computations by several orders of magnitude. However, one model can be connected in a multiple-unit configuration to provide a proportional increase in high speed performance at only an incremental increase in cost. Multiple parallel-bus architecture and a modular multiprocessor structure distinguish the array processor discussed in this article from others, and are two features that facilitate the use of two or more such array processors with a single host computer. The multiple array processors can be connected to one another and to the host in several ways, each providing improved throughput over single-array processor configurations. In general, it is possible to achieve an increase in throughput that is nearly proportional to the number of array processors.

Using a multiprocessor architecture, most array processors contain two or more independent processing units that perform highly specialized tasks. These include at least an arithmetic unit and a host interface, in addition to memory. Addressing can be accomplished within the arithmetic unit or by a separate controller. Some array processors contain various input/output (I/O) units to relieve the slower host from the realtime data transfer process. The design discussed here combines all of these units (running asynchronously to optimize individual processing speeds) with a central control processor to further offload the host computer. In this system, a central system processing unit (CSPU) regulates overall array processor operation, an arithmetic processing unit (APU) handles all data addressing and floating point operations, and input/output subsystems (IOSs) perform data transfers directly to memory. A host interface module (HIM) connects the array processor to the host computer.

Most array processors also contain two or more separate memories whose access times are optimized for such specialized operations as control storage (a small, high speed memory), buffering (a large, relatively slow memory), and scratchpad storage (a mid-size, medium speed memory). An efficient design provides three similar memories, each with its own bus; thus, each processing unit can access each memory bus. In addition, each processing unit contains its own local program memory, which is downloaded from one of the bus memories by the CSPU. This multiple bus structure, coupled with the asynchronous processor operation, is critical to the ability to interconnect more than one array processor.

The three buses (which can connect memories of different speeds) afford a convenient way of handling realtime double-buffered I/O with simultaneous APU processing and without memory contention problems. Two or more array processors can be interconnected simply by tying one or two buses together; the interconnected buses act as a single bus in the multiple array processor system.

Organization of data flow through a multiple array processor system tends to classify the configuration as

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either a series or a parallel architecture. In the parallel configuration, input data reside on a common input bus. Alternate (or overlapped) blocks of data are processed simultaneously by the two APUs, and results are sent to a common output bus. Each processor in a parallel configuration performs essentially the same set of arithmetic tasks [Fig 1(a)].

In a series configuration, each APU performs a portion of the overall arithmetic task. As with the parallel structure, the input data reside on a common input memory bus. Each array processor, in sequence, performs its segment of the total procedure, placing its intermediate results on a shared transfer bus that also handles the final output transfer [Fig 1(b)]. Overlapped computations create a software pipeline. Data propagate from one array processor to the next as each performs its portion of the computation. In general, each array processor is handling a different block of data at any given time.

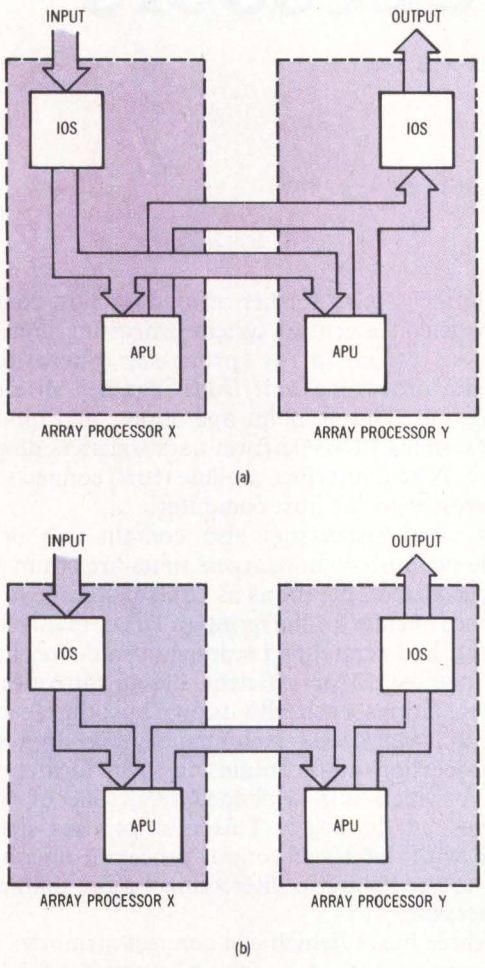

Fig 1 Series and parallel configurations. Using parallel architecture (a), APUs X and Y perform identical operations on alternate blocks of data. With series architecture (b), APUs perform sequential segments of overall processing task

Both series and parallel configurations achieve maximum speed by allocating I/O and arithmetic to separate memory buses. Each arithmetic processing unit uses a high speed memory bus local to its own array processor to access its working memory data. Synchronization can be accomplished in various ways. Although special I/O or APU instructions may be required in some cases, most applications can use flag synchronization with standard software function calls.

Parallel architecture

Two array processors can work in parallel to double the throughput from a single data source to one or more data destinations. (See Fig 2.) Data are supplied as input on bus 3, which is shared by both array processors. The two APUs pick up alternate blocks of data from bus 3 and perform their separate operations in parallel, each using its own bus 2. In this example, APU operations are assumed to be identical. Final APU results are sent either back to bus 3 for output through an IOS, or to bus 1 for output through the HIM.

Fig 3 shows typical data flow timing for a parallel combination of two array processors. Array processor X synchronizes arithmetic processing and I/O through use of normal software executive procedures. Array processor Y achieves synchronization through one of several semaphore flag methods. It can read the X processor flag register through its bus 2; or the input IOS can write, through its bus 2, into the Y processor's flag register. A write to the flag register can either start the Y APU directly, or interrupt the Y CSPU to use normal software executive procedures for processor synchronization.

For procedures that are limited by APU performance, the dual parallel array processor configuration shown in Fig 2 runs about 20% slower than twice the speed of a single array processor. The 20% penalty is caused by the fact that each CSPU shares a bus with an APU. An alternate configuration that eliminates one or both of the cross connections between buses 1 and 2 affords a speed improvement of exactly 2 : 1 over a single array processor system. However, synchronization of the Y APU with the I/O requires software additions that are not part of the standard executive. In this case, semaphore flags are exchanged through bus 3. As an alternative, digital signal ports on the two IOSs may be connected as a communication path. In most cases, the throughput need not be doubled exactly; the cross connection between buses 1 and 2 eliminates the need for special software.

Series architecture

Three array processors working in series can triple the throughput from a single data source to one or more destinations. (See Fig 4.) Each array processor operates independently except for the sharing of a common bus 2 memory. The overall load of arithmetic tasks is divided about equally among the three array processors.

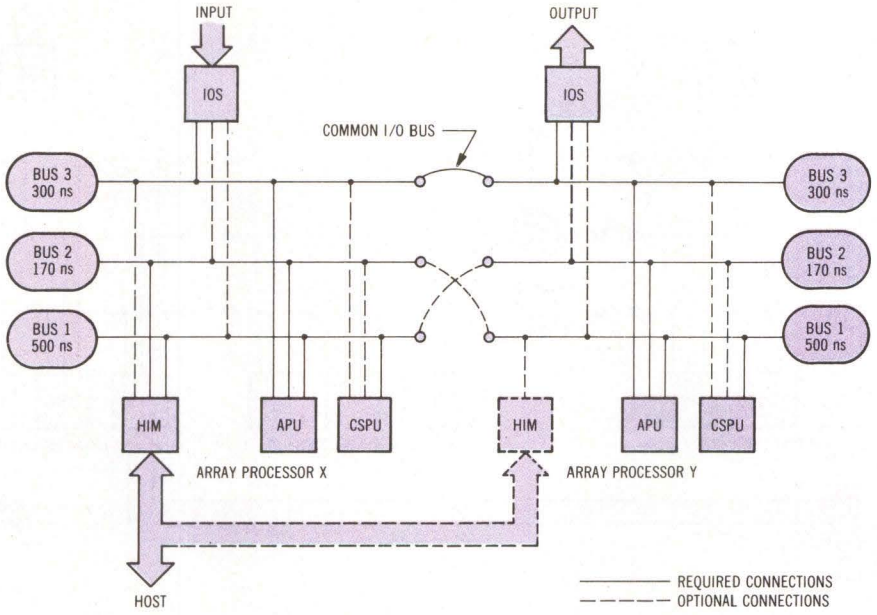

Fig 2 Typical parallel architecture. APUs take turns reading data blocks from medium speed, common input/output bus 3. Each APU performs complete task using its own high speed bus 2 for working storage, and sends results to IOS on shared bus 3 or to HIM on low speed bus 1. Optional cross connection links buses 1 and 2 for synchronization purposes only

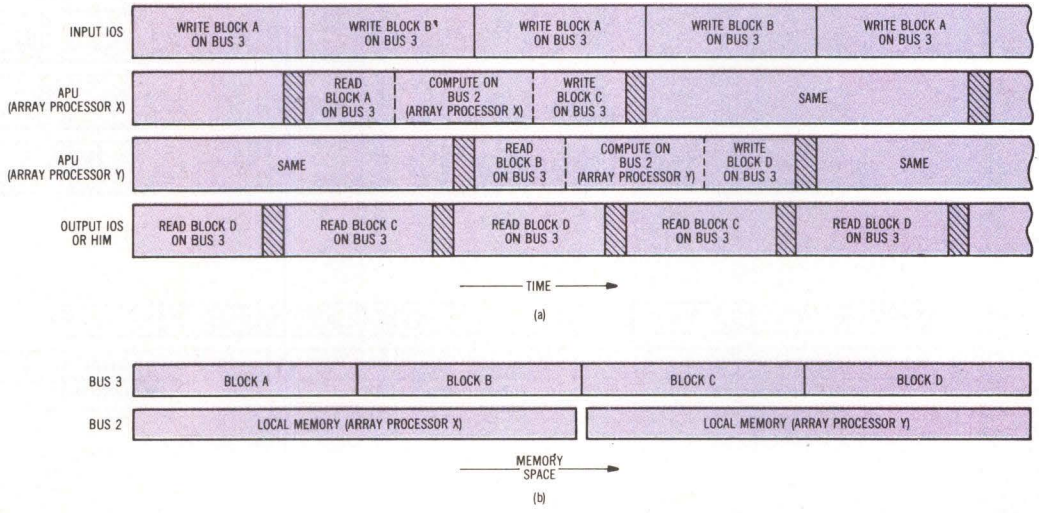

Fig 3 Parallel structure timing and synchronization. In (a), each of four horizontal bars shows internal processor operation as function of time. In (b), each horizontal bar represents one memory bus. Horizontal axis represents memory address space. Note that there are two independent bus 2 memories

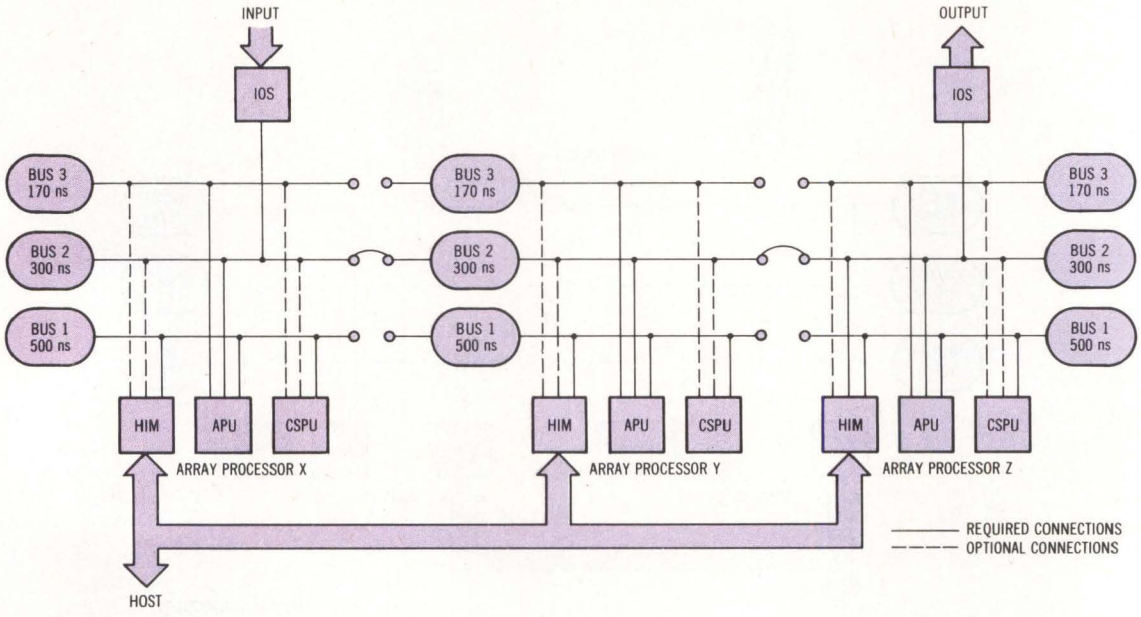

Fig 4 Typical series architecture. Except for shared memory bus 2, each array processor operates independently by accepting input data from medium speed bus 2, performing its portion of total processing task on high speed bus 3, and returning results to bus 2

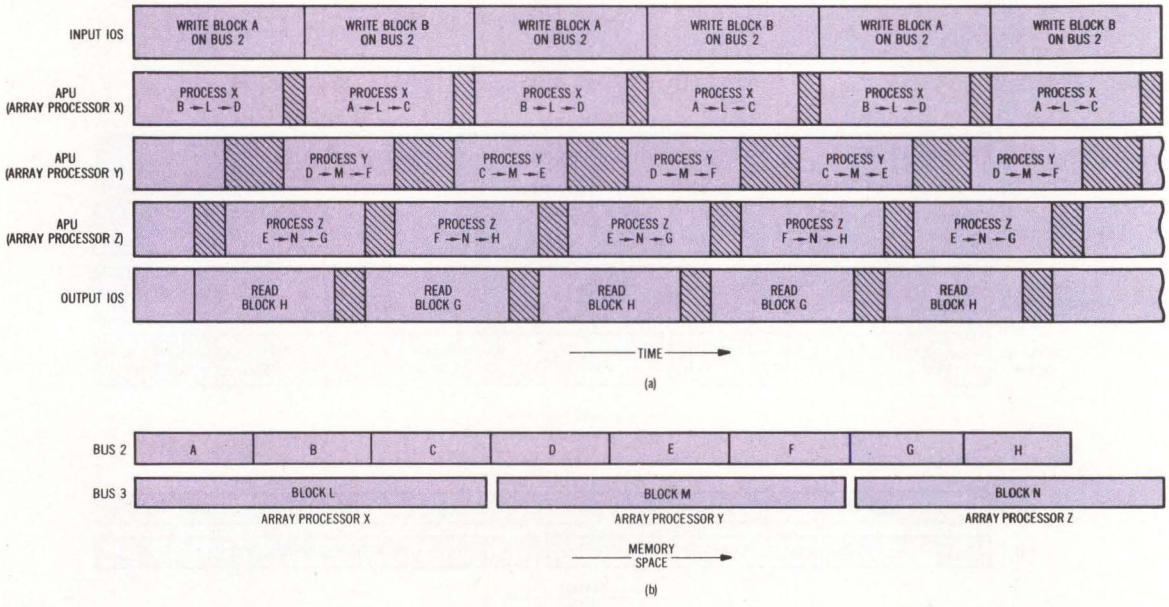

Fig 5 Series architecture timing and synchronization. In (a), each of five horizontal bars shows internal processor operation as function of time. In (b), each horizontal bar represents one memory bus. Horizontal axis represents memory address space. Here, three independent bus 3 memories are shown

Data are input to bus 2 of array processor X. The APU in array processor X performs its share of the tasks on its high speed bus 3, leaving the results on the common bus 2. The APU in array processor Y picks up data on bus 2, performs its third of the tasks using its high speed bus 3, and leaves results on bus 2. The APU in array processor Z then performs the remaining tasks in its own bus 3 memory, placing the final results on the common bus 2 for output via an IOS, and/or on bus 1 for output to the host.

Fig 5 shows data flow timing for the series configuration. Synchronization is accomplished in the same manner and with the same options as for the parallel configuration. In general, the simplest technique, involving no modification of standard software, involves writing to and later sensing the system flag register.

Selecting the configuration

Consider an input data stream at 400 kHz, on which we are to compute real, 1024-point fast Fourier transformations (FFTs). The input and output each require a memory cycle every 2.5 μs; there is no IOS or memory speed limitation here. However, this problem requires an FFT to be computed in less than the block time of 2.5 μs; the processor under consideration is capable of performing this in 4.6 ms. Clearly, we need to double the number of APUs on the job. We simply put two array processors in parallel using the configuration shown in Fig 2. Bus 3 memory must provide four cycles for each input sample (an input write, an APU read and write, an output read); the required memory cycle time is $2.5 \div 4 = 0.63$ μs. The slower 500-ns memory would suffice; the 300-ns memory is a better choice.

Next, consider a 200-kHz input data stream to be processed in blocks of 1024 samples (block time approximately 5 ms), for which we must compute frequency translation and convolution filtering requiring 3.5 ms; FFT requiring 4 ms; and power spectral averaging, peak searching, and scalar operations requiring 3.0 ms. The cumulative 10.5 ms of processing requires three array processors working together. Using the configuration in Fig 4, we can assign the workload serially according to the three divisions just mentioned. The serial configuration has two advantages over the parallel configuration in this example. If task requirements change, only one processor's software needs to be modified. Furthermore, since the speed of the convolution phase will probably be limited by processor speed, and not by memory speed, the speed of the bus 3 memory on the first array processor can be relaxed to 300 ns, affording a significant savings in cost.

In general, the use of the serial configuration is advisable in all but the simplest applications because the memory workloads tend to be more evenly distributed. Portions of the processing that are not limited by memory speed can be isolated to allow the use of lower cost memory.

Conclusions

An array processor design containing multiple parallel memory buses allows two or more processors to be interconnected easily. The combined array processors afford a processing speed improvement in almost direct proportion to the number of processors used. Flexibility of multiple buses facilitates double-buffered I/O and eliminates memory contention between the arithmetic processor and I/O subsystems. A configuration allowing the serial flow of data is generally the easiest to maintain (from the standpoint of software), and is the most cost effective.

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John F. Burns is with CSPI, where he works in customer support for signal processing applications. Mr Burns received his BSEE degree from Cornell University. He is a member of the IEEE and is currently secretary of the Washington, D.C. chapter of the Acoustic Speech and Signal Processing Society.

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Image processors have advanced from the laboratory experiment level to low cost systems that satisfy commercial needs

Image processing architecture expands range of applications

During the early 1970s, research laboratories and medical diagnostic centers were the primary users of image processors. Suddenly, however, commercial applications for digital picture processing seem to be sprouting everywhere, thanks to the lower cost of memory, microprocessors, and other semiconductors that constitute most of the cost of such equipment. A complete image processing subsystem (Fig 1) today occupies only a single printed circuit board. Besides performing video digitizing and picture display, it stores up to four images on its circuit board, performs image processing, and transmits control and image data to a host computer.

Application areas for low cost image processing equipment range from commercial to industrial environments. Fig 2 shows an application in banking. A bank can digitize and store the picture, signature, and account file of each of its customers. Such a picture data base can reduce fraud and provide greater security for financial institutions. Data storage requirements are surprisingly modest. Using picture processing to reduce the storage space required, the signature shown in Fig 2 occupies only about 400 bytes. A bank with 100,000 customers could store all of their signatures on a 40M-byte disc drive.

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Octek Incorporated
7 Corporate Pl, S Bedford St, Burlington, MA 01803

Fig 3 is an example of another application of a picture data base—inventory control for a museum. Cataloging a museum's collection, each item of which is different, is not easy. The task of the researcher seeking information on an object in the collection is no easier. Visual cues aid much of the research. Therefore, even with access to a computer system to reduce the data, there still must be a way to refer to a picture file or the object itself for important visual cues. A picture data base is well suited for just such a project. It enables the researcher to sort not only by historical and archaeological data, but by visual cues as well.

Low cost image processing systems have also found applications in computer aided design. In Fig 4, a character is digitized and processed to create a new font for a dot matrix printer. Company logos and special symbols can be digitized as well to create custom fonts for a programmable printer.

Video digitizing

Video inputs to the Octek 2000 image processing subsystem are RS-170 compatible. That is, standard television cameras of the type used with closed circuit television monitors, video tape recorders, or other equipment employing the RS-170 video standard can be connected directly to one of the video inputs. Incoming video signals are in a raster format. The electron beam that scans the target in a camera sweeps horizontally, then retraces and sweeps again.

Simultaneously, the beam sweeps vertically, at a much slower rate so that a complete picture, or field, is

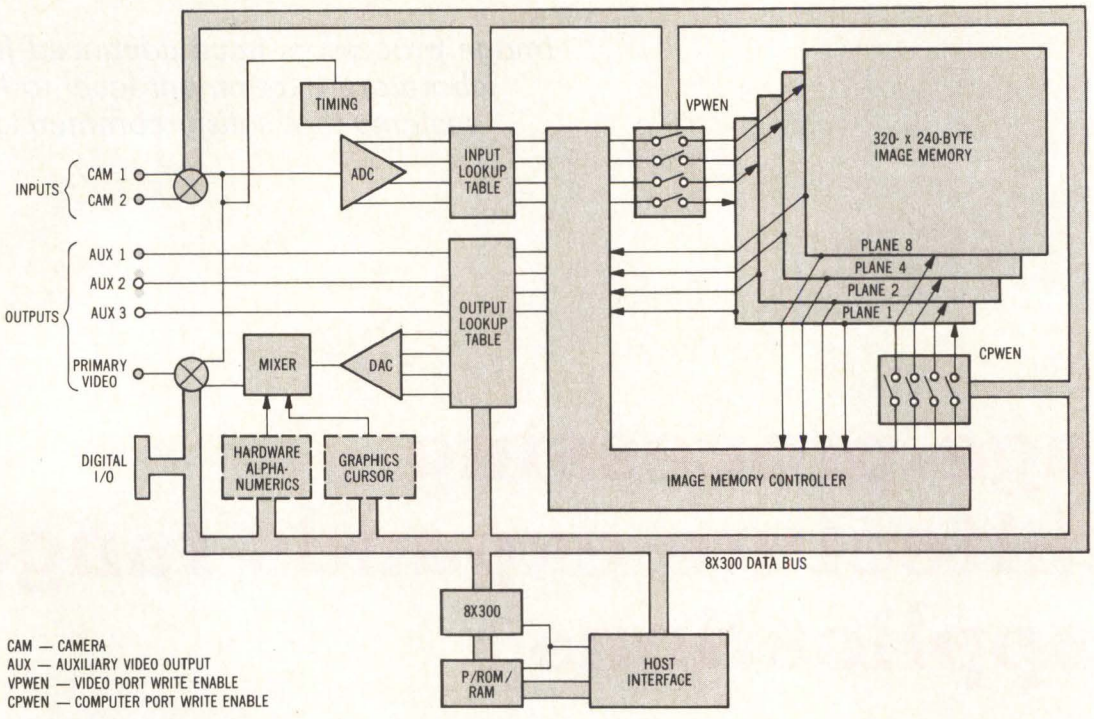

Fig 1 Low cost image processing system block diagram. Octek 2000, shown here, fits on a single 15" x 15" (38- x 38-cm) circuit board. ADC processes inputs compatible with RS-170 into 4-plane image memory. Output lookup table maps up to 16 colors from a 64-color palette, or 16 shades of gray. Output circuits mix alphanumeric and graphic output and handle cursor control. Fast 8X300 microprocessor has excess capacity for image processing functions

formed every sixtieth of a second. The analog video data are converted into digital data by a high speed, 4-bit analog to digital converter (ADC). Each 4-bit nibble represents the "gray level" at one spot in the picture. The converter is synchronized exactly with the video input to create a clear, stable digital image. As a result of this digitizing process, the television camera input is converted into 307,200 bits of digital data up to 60 times a second.

Image storage

Following digitization, the video data are directed to a digital translation table, for data transform functions, and then stored in an image memory. The image memory has the capacity to store a complete video field. Each picture element (pixel) is stored as a 4-bit word representing one of 16 gray levels. The memory is synchronized with the ADC so that a complete image field is stored in one-sixtieth of a second.

For applications that do not require 16 gray levels, the 2000's microprocessor can partition the image memory into 3-bit, 2-bit, or 1-bit memory planes. Up to four sequential images can be stored in this way for animation or motion studies. The host computer can access the dual-port image memory during the same memory cycle as the video input or output. It need not wait until the digitizing process is completed in order to write to or read from the image memory.

Image display

Image memory output is directed to four video outputs. The primary output is equipped with a 16-gray-level digital to analog converter (DAC). The remaining three outputs are binary video (black and white, no gray) only and are intended for color output (when used with a color television monitor) or for operating independent, multiple, black and white displays. Model 2000 can display 16 colors at a time from a software palette of 64 colors. In addition to 16 gray levels, the primary video output is equipped with an optional hardware graphics cursor and hardware character generator. The cursor's coordinates, size, and shape are programmable from the host computer. The hardware character generator displays 32 lines of text with up to 64 chars/line. Video

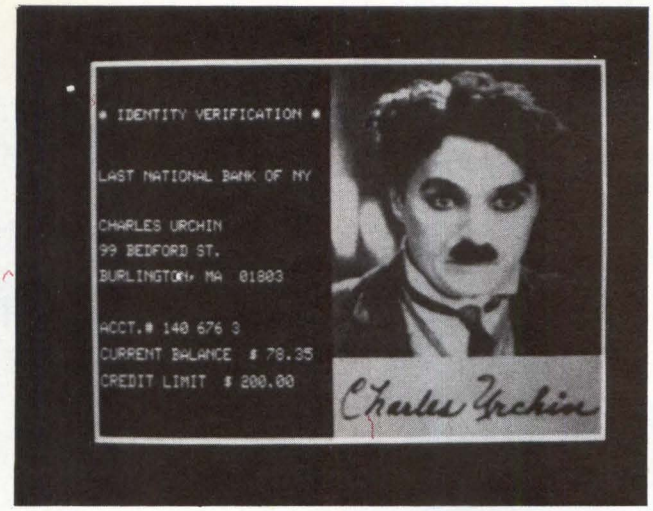

Fig 2 Commercial application verifies identity. Digitized image can be stored with customer account data in regular commercial data base. Picture processing reduces memory overhead. For example, signature portion of image occupies only about 400 bytes

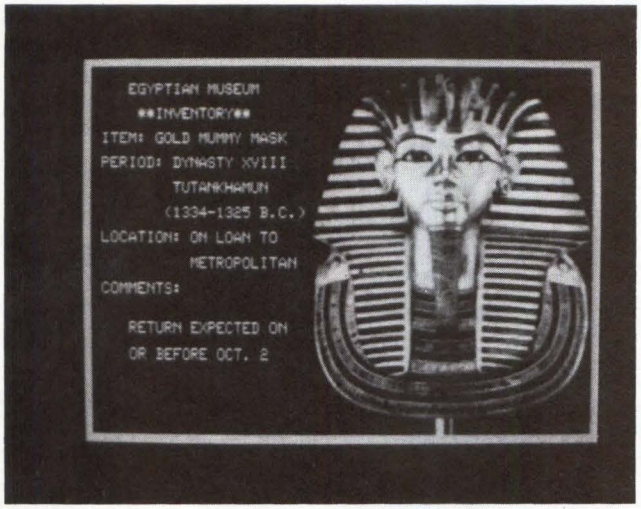

Fig 3 Information retrieval system uses visual cues as key. In museum catalog applications, appearance of object is primary characteristic used to store, cross-reference, and locate data

outputs generate standard RS-330 video, allowing the images to be displayed in raster format on a variety of popular video monitors.

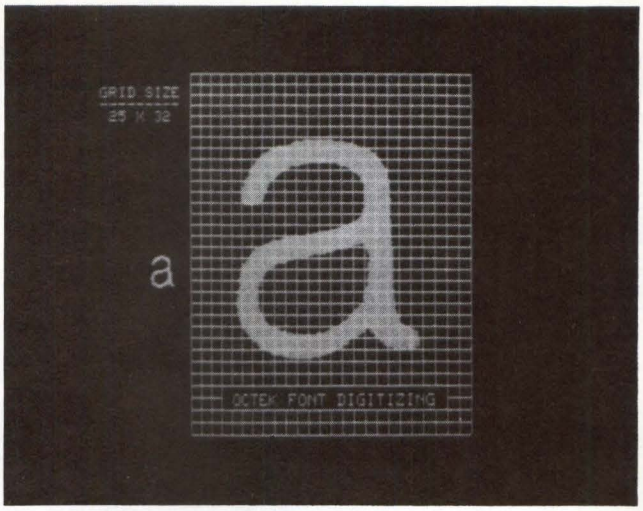

Fig 4 Computer aided design potential. Character profile is digitized and processed to create new font for cathode ray tube display or dot matrix printer. Closely related potential for robot vision lets image processing subsystem distinguish objects and identify abnormalities

Image transmission and processing

Image data can be transmitted to or from the host computer by either programmed input/output or direct memory access. Under programmed input/output, the onboard microprocessor handles all data exchanged. Direct memory access transfers are processed by a separate onboard controller that drives the image memory directly. Full-screen, 16-gray-level pictures can be transferred to the host in less than a quarter of a second. Thus, pictures can be stored on and recalled from a disc quickly for picture database applications.

An onboard, high speed, bipolar microprocessor controls various hardware functions. For example, image data can be read or loaded in blocks, and image areas can be summed by the microprocessor. Beyond these activities, the processor can be programmed to perform specific image processing or analysis tasks. An optional random access memory permits the downloading of developed microprograms.

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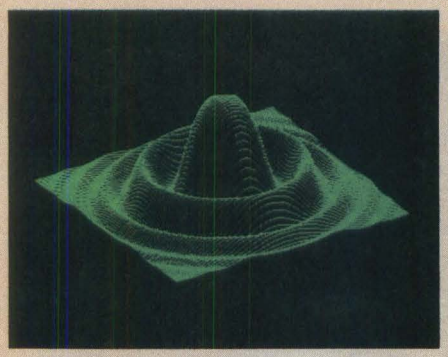
John Trombly is president of Octek Inc of Burlington, Mass, a manufacturer of image processors for computer assisted design, robot vision, and automated visual inspection. Prior to co-founding Octek in 1978, he was with Hewlett-Packard Co and Arthur D. Little Inc. The designer of microprocessor based test systems, modems, carrier telephone systems, and radio pagers, he holds five patents, and has written articles on image processing for electronics and computer journals. He received a BS degree in electrical engineering from Lowell Technological Institute.



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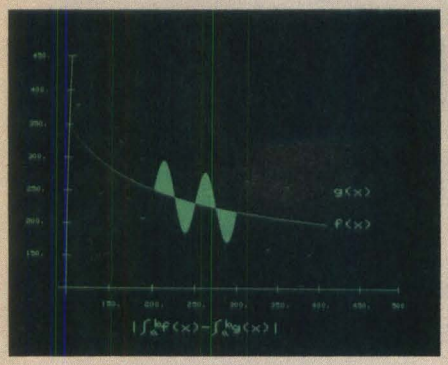

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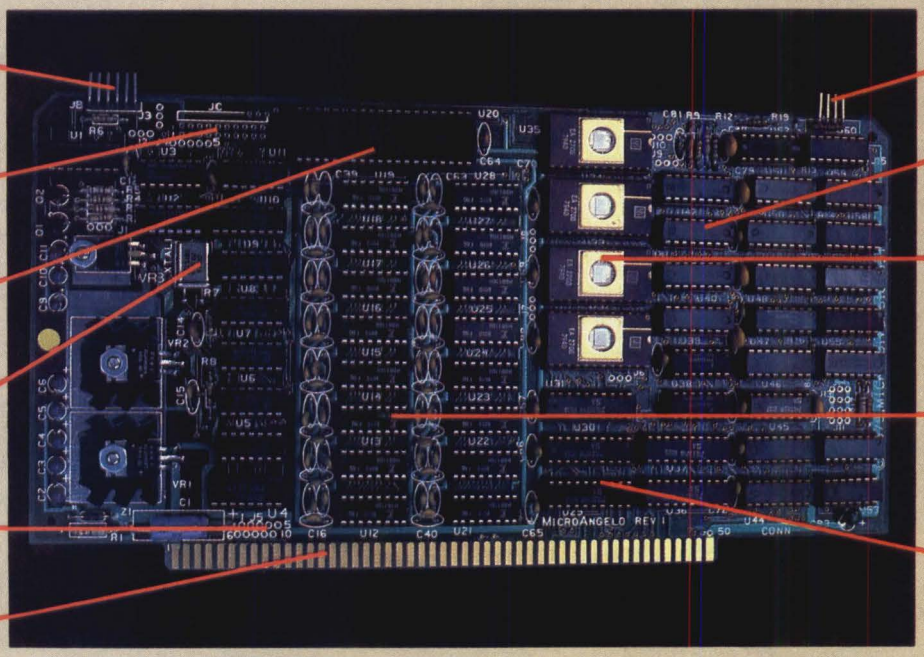

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Semiconductor memory array in data path between sensors and tape transports solves data acquisition system design problems

Design method treats CPU as memory add-on

Memory subsystems are traditionally designed for a particular type of microprocessor, constructed by using a specific memory technology, and then annexed to the host processor as a memory add-on. Now, thanks to the advent of totally modular memory subsystems, an arbitrary host processor instead can serve as a "host add-on" to a particular memory system. A geophysical instrumentation package designed around a modular memory system benefited from this "backward" approach to serve data logging applications that simplify oil well exploration. Besides cutting the initial cost of the data logging system by about one-third, the host add-on design approach achieved an ongoing savings of 25% to 30% in offline data processing costs.

Reducing the cost of capturing digitized measurements of seismic shock waves was a primary design goal. Seismic shock waves are generated by carefully placed explosions or large, truck-mounted vibrators (Fig 1). Most existing systems used in geophysical data logging record the data picked up by the sensors directly onto magnetic tape. The high cost of a typical, direct recording, data acquisition system results from its mechanical limitations and the unnecessary overhead that it imposes on subsequent data processing steps.

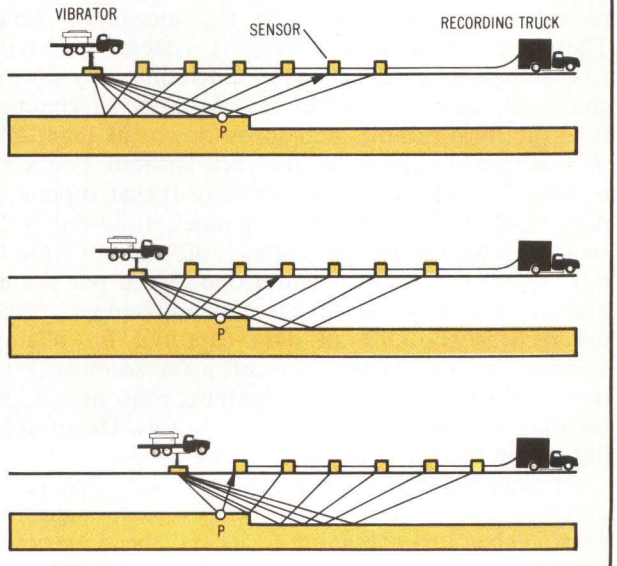

Fig 1 Geophysical data capture. Truck-mounted vibrator generates acoustic waves that reflect off underground strata. Discontinuity near point P is identified when truck moves forward and different sensor receives its distinctive acoustic signature

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In a direct recording instrument, each channel receives a composite waveform from several sensors that are positioned and tuned to reinforce desired signals along their common channel while attenuating unwanted signals. For geophysical exploration, an unwanted signal might be ground roll—a wave that propagates along the surface and contains no useful information about underground formations. Reinforced signals include waves reflected from rock layers deep underground, waves that help to identify strata whose presence may indicate petroleum deposits.

Several limitations contribute to the expense of conventional instrumentation systems for geophysical data logging. One is that they have a fixed number of channels. Typical instruments record about 50 or 60 channels of data. None of the channels can be disconnected when making a limited range of measurements. Therefore, unused channels continue to operate alongside the active channels, recording useless data on great lengths of wasted tape. Since meaningful data are interspersed with data from the unused channels, the entire tape must be searched just as diligently as if it were packed with valid information.

Another limitation of conventional systems is that they enforce a trade-off between tape transport capability and the frequency or duration of data collection sessions. Single-speed tape transports can handle only a limited range of data formats. Therefore, to allow the greatest data format flexibility, a tape transport with two or more speeds is needed. Furthermore, although single-speed transports are less expensive initially, they are likely to cost more to use because they require extra measurements to gather enough data for useful analysis when the tape speed is too low, and they waste tape when the tape speed is too high.

Multiplexed recording is possible because seismic waves never exceed about 200 Hz, and the tape can record frequencies well into the megahertz range. Therefore, standard data logging systems record the first sample from all channels (including any inactive channels), then the second sample from all channels, then the third sample, and so on down the tape. Data thus recorded cannot be analyzed without first being demultiplexed into a stream of records that supplies all data samples from the first channel, followed by all samples from the second channel, all samples from the third channel, and so on until one record per channel has been assembled in sequence. A complete set of channel records contains all data captured for a single seismic wave that lasted, at most, a few seconds. When it reads the tape, the central computer must demultiplex the data before it can begin data analysis. Demultiplexing wastes mainframe computer resources.

Another limitation, the mechanical delay inherent in all tape transports, also contributes to data acquisition costs. Tape must accelerate to its full speed before the first data sample arrives, and tape acceleration consumes a lengthy interval on an electronic time scale. On the other hand, the tape must not start moving any sooner than is necessary because every second of motion involves many inches of tape that must be searched for data during the demultiplexing process.

Capitalizing on a host add-on design approach, the simple expedient of placing a modular semiconductor memory array in the data path between the sensors and the tape overcame all of the difficulties that contribute to increased data logging costs. The use of Intel's Series 90 memory subsystems simplified the task of designing the memory array into the system because Series 90 includes all related hardware such as card cages, backplanes, and power supplies.

Series 90 entered into the design decision because it can operate with a variety of user-built application modules such as those shown in Fig 2. Application modules can be assembled on Intel utility cards or any printed circuit card that fits the Intel card cage and bus connector. Alternatively, they can be assembled on an external chassis and connected directly to the bus with a ribbon cable and a special connector.

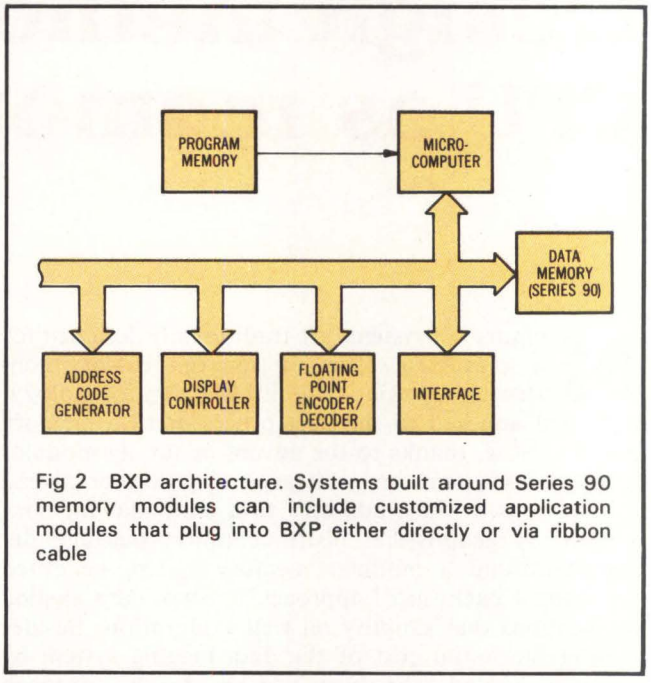

Fig 2 BXP architecture. Systems built around Series 90 memory modules can include customized application modules that plug into BXP either directly or via ribbon cable

digital radio receiver with serial-to-parallel conversion circuitry, the Series 90 data memory module, a tape formatter and controller, and the tape transport, with a

The high speed bus used with the series is called a Byte Exchange Path, or BXP™, and consists of 132 lines divided into five functional groups: 24 address lines (17 of which are now in use, allowing up to 16M words per module), 4 module address lines that address up to 16 modules, 88 data lines to handle word widths from 16 to 88 bits, 12 control lines that allow various modes of operation, and 4 status lines used to optimize the asynchronous mode. As in almost any bus, all of these lines extend in parallel to all modules in the system, thereby supporting a variety of data flow configurations.

Data logging subsystems can use the BXP architecture to communicate among themselves in the simplest possible way. The subsystem shown in Fig 3 includes a cathode ray tube terminal serving as the operator inter-

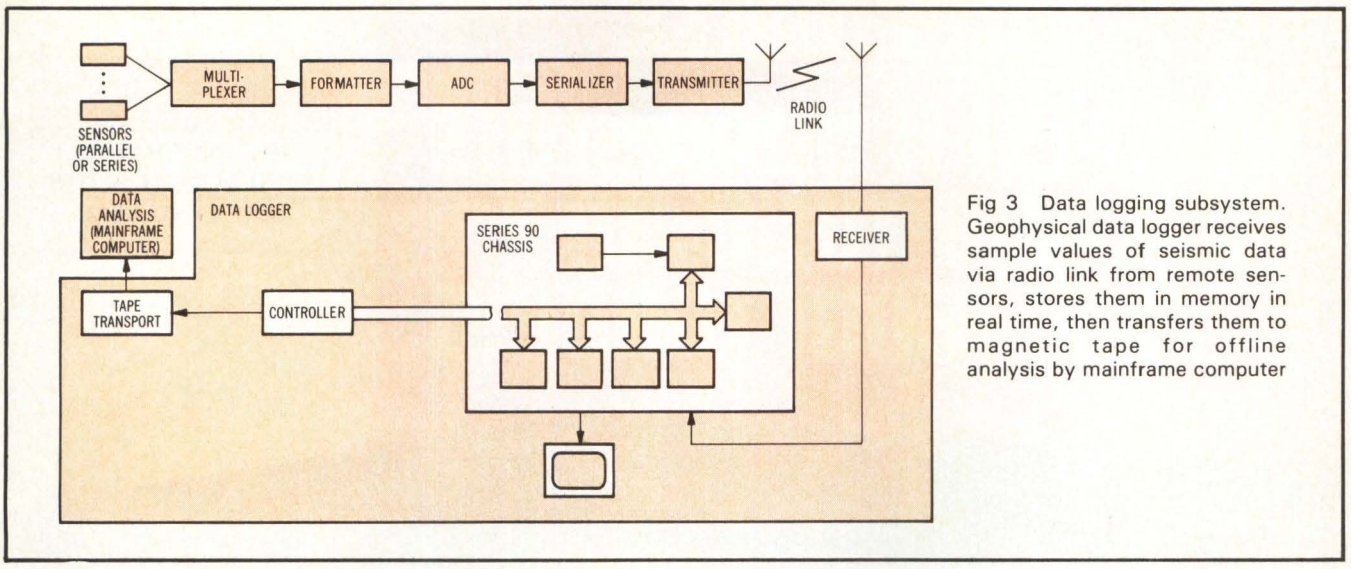

Fig 3 Data logging subsystem. Geophysical data logger receives sample values of seismic data via radio link from remote sensors, stores them in memory in real time, then transfers them to magnetic tape for offline analysis by mainframe computer

face. The data acquisition subsystem, tape formatter, and terminal connect directly to the BXP through appropriate interface circuitry. The data logging subsystem includes a microcomputer, a remote data interface, an encoder/decoder for storing the data in mainframe floating point format, an address code generator (which selects the channel to be stored at any given moment), and a data memory of 128k bytes or more.

The data logger stores measurements in the memory, then transfers the memory data onto tape, thereby freeing the memory for use with another set of measurements within a few seconds, when the next shock wave appears. The number of channels can vary, and, because the system includes a microprocessor, channel width can be set in advance from only a few channels to the full system capacity. Only those channels that are actually in use need to be recorded on tape. Once the memory captures data, the transfer to tape, although immediate, requires a relatively inexpensive, single-speed transport mechanism. Because only valid data are recorded, the use of a slower transport mechanism can reduce costs even further.

Channels must be multiplexed as they are recorded in memory for the same reason that they must be multiplexed for direct recording on tape. However, when the microprocessor is used, demultiplexing can occur as the data are transferred to tape from memory, eliminating the offline demultiplexing step at the home office computer center. Also, because the memory does not impose a mechanical delay, data recording begins the instant the first sample arrives on the first channel. Once data are captured, the data logger waits as long as is necessary for the tape transport to accelerate before starting to write memory data onto tape.

The market for geophysical instrumentation is expanding as the search for domestic oil intensifies. Intended to provide a less costly, scaled-down system that would nevertheless gather all data required in oil exploration, the data logging system described here had to meet many secondary needs. It had to combine equipment from several sources with equipment designed and built inhouse. To simplify communication between subsystems, a standard bus was needed. The system had to be transportable, and it had to operate properly through a wide range of temperatures in the presence of dust and vibration. It was to be expandable through the addition of memory, upgradable to incorporate new technology, and fast enough to handle high speed sampling on numerous channels. All of these characteristics were combined in the final design using Series 90 memory modules and the BXP bus.

About the Authors:

Gary Wood is an engineering manager for the Memory Systems Operation Division at Intel Corp. His areas of interest are intelligent memory systems architecture, microprocessor applications, and robotics. He holds BSEE degrees from the University of Washington and the University of Santa Clara.

Paul Passmore is the founder and president of Refraction Technology, Inc, which is involved in the development, manufacture, design, and marketing of geophysical data acquisition equipment. Before founding Refraction Technology, Mr Passmore was with Aquatronics as a project engineer. He is a member of the IEEE and the Society of Exploration and Geophysicists, and has a BSEE degree from Texas Technical Institute.

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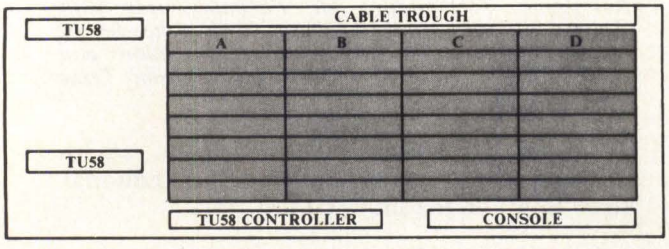

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CIRCLE 127 ON INQUIRY CARD

Canada: Ahearn & Soper Ltd., 416-245-4848 • **Finland:** Systek OY, (80) 73 72 33 • **France:** YREL, (03) 956 81 42 • **Hungary/Poland/Rumania:** Unitronex Corporation, WARSAW 39 6218 • **Italy:** ESE s.r.l., 02/607 3626 • **Netherlands:** Technitron b.v., (020) 45 87 55 • **Sweden:** M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany:** O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Yugoslavia:** Institut "Jozef Stefan", 263-261 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 544-3444 • **India:** Infosystems Private Limited, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 06 (282) 5111 • **Taiwan:** Rabbit Associates, Ltd., 7219573-5 • **Hong Kong:** Automated Systems (HK) Ltd., 5-630256-9 • **Malaysia:** Automated Systems (M) Sdn Bhd., 773777 • **Indonesia:** P. T. Daya ASL, 584306 • **Singapore:** Automated Systems (PTE) Ltd., 2354133

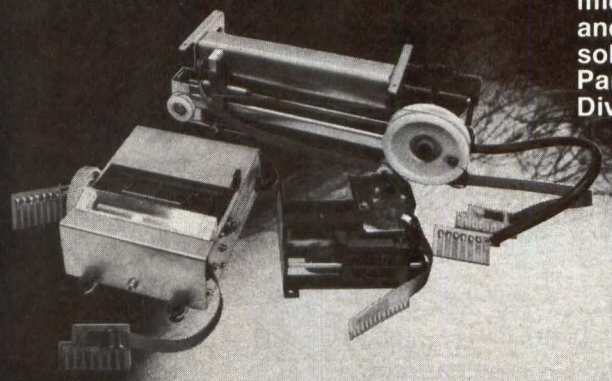
Panasonic non-impact printers:

You know how it goes. You have to design your next calculator, data logger, computer terminal or what-have-you down in size, so you need a smaller 'printer. Here's your answer: our EUY non-impact printers – the family with the envelope dimensions that leave you with room to spare.

SERIES	COLUMN CAPACITY	PAPER WIDTH	OUTSIDE DIMENSIONS
EUY-2	15	1.42″	2.83″X1.32″X2.20″
EUY-10	15,21,32,40	2.36″	3.56″X1.67″X4.33″
EUY-5	32,40,64,80	5.0″	7.68″X2.56″X2.76″

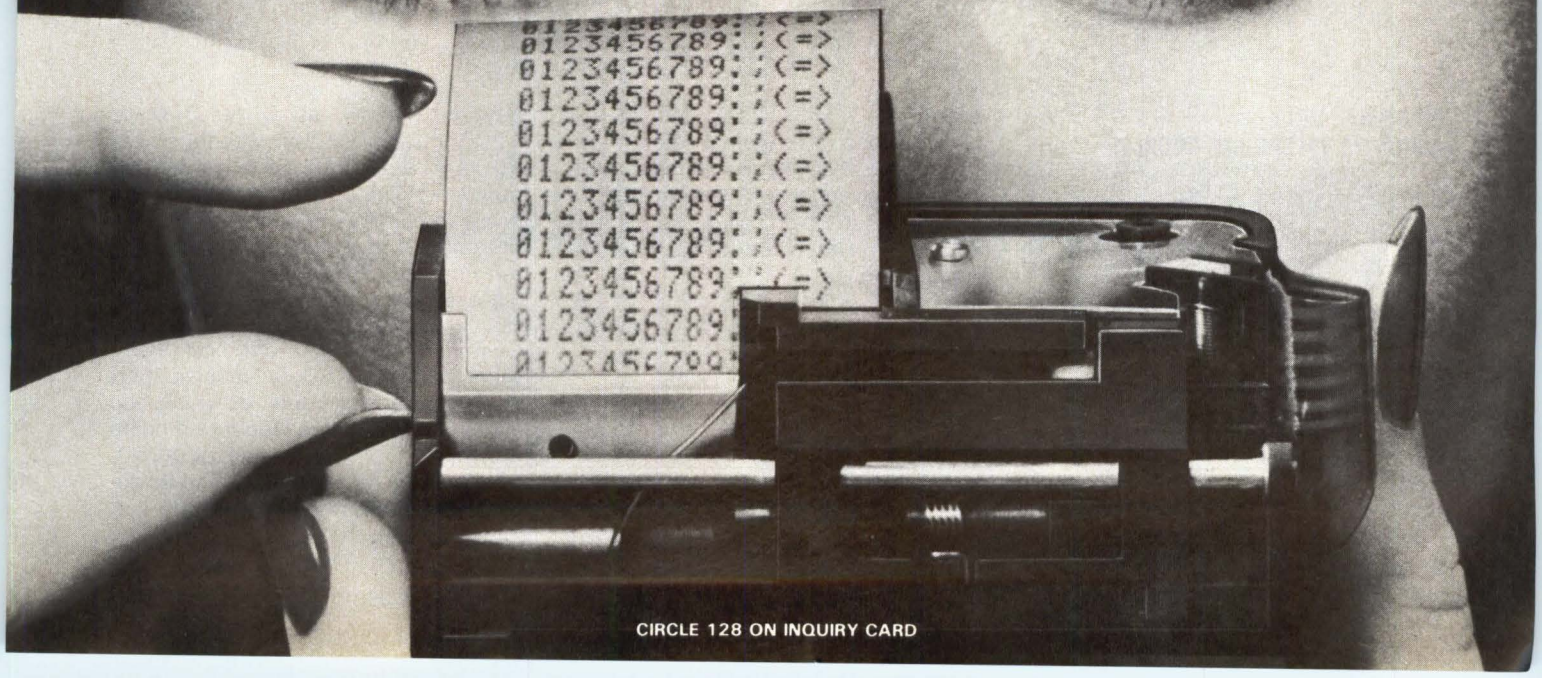
Available in both electrosensitive and thermal versions, Panasonic printers are small, low cost, quiet. All feature the reliability of a design that eliminates all moving parts except print head and paper transport. And all pack the character-forming flexibility and legibility provided by a 5 x 7 dot matrix print head that prints up to 128 alphanumeric characters and symbols, including a full ASCII character set.

Add the all-DC power requirements, plus the 8-bit parallel/bit serial compatibility of our own microprocessor-based printer interface controller, and you've got the ideal small-space printing solution. For information and prices, write to: Panasonic Company, Electronic Components Division, One Panasonic Way, Secaucus, NJ 07094; or call (201) 348-5284.



Panasonic®
just slightly ahead of our time

your answer to the "make it smaller" syndrome.



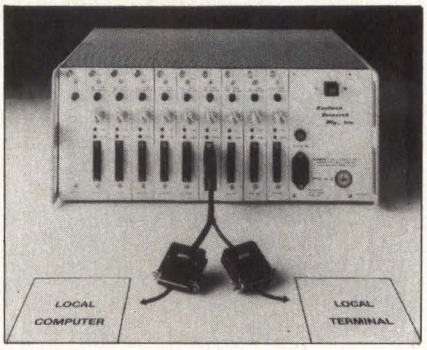
CIRCLE 128 ON INQUIRY CARD

DATA COMMUNICATIONS

Line interface module enables single terminal to communicate with two computers

"Side door" line interface module (LIM) DLA-100-SD enables connection of a terminal to both a host and a local computer. The module, used in conjunction with the company's models 870 and 871 true port concentrators (***Computer Design,*** Jan 1981, p 39), can be used to talk to nearly any local computer that has an asynchronous port. Model 870 concentrator for IBM 3270 protocol and 871 for Univac UTS 400 are both polled concentrators and emulators that support multidrop polling in multiple clusters of eight terminals each.

The side door LIM is installed by plugging into one of the LIM slots in the concentrator. (See the Figure.) A special "Y" cable supplied with the LIM allows connection of both terminal and local computer by means of an RS-232-C interface to the concentrator. No software modification is required to either the host or a local computer, and the concentrator is transparent to the local unit.



When the side door LIM is used with the model 870 concentrator, up to 32 clusters of 8 terminals each can be connected to a single IBM host computer port and virtually any asynchronous ASCII terminal can be connected to the concentrator. Host communication is under 327X BSC protocol. Used with the 871 concentrator to serve a Univac host under UTS 400 protocol, as many as 31 clusters of 8 terminals each can be connected to the Univac host. A side door LIM is used for each terminal that requires an interface to both the host and a local computer.

The side door LIM performs externally such tasks as protocol conversion, terminal emulation, and polling operations, thereby freeing the CPU of such overhead. Any requirement for additional wires or cables is eliminated and the user can talk to whichever computer he chooses. The choice can be made by a simple keyboard data entry, even when the terminal is connected on a dial-in basis. The side door LIM is also an economical alternative to port contention devices, especially when 32 or fewer terminals are involved.

True port concentrators are priced from $4890 (with one side door LIM) to $10,595 (for eight LIMs and eight side doors). The side door LIM is priced at $815 for users who wish to add them to already installed concentrators. Delivery is 45 days after receipt of order. **Kaufman Research Manufacturing, Inc,** 2260 Mora Dr, Mountain View CA 94040.

Circle 341 on Inquiry Card

ORIGINATE ONLY ACOUSTIC TELEPHONE COUPLER

Model 715 can be used with remote terminals or small computer systems to originate calls and provide bidirectional information transfer to/from a Bell 103A or equivalent data set. Coupler features full-duplex operation and offers both RS-232-C and 20-mA current loop interfacing, data rates from 0 to 450 baud, and precision sound seal cushions. It couples to a Western Electric 500 series handset or equivalent and operates at temperatures from 0 to 140 °F (−18 to 60 °C). Single unit price is $125. **Omnitec Data,** 2405 S 20th St, Phoenix, AZ 85034.

Circle 342 on Inquiry Card

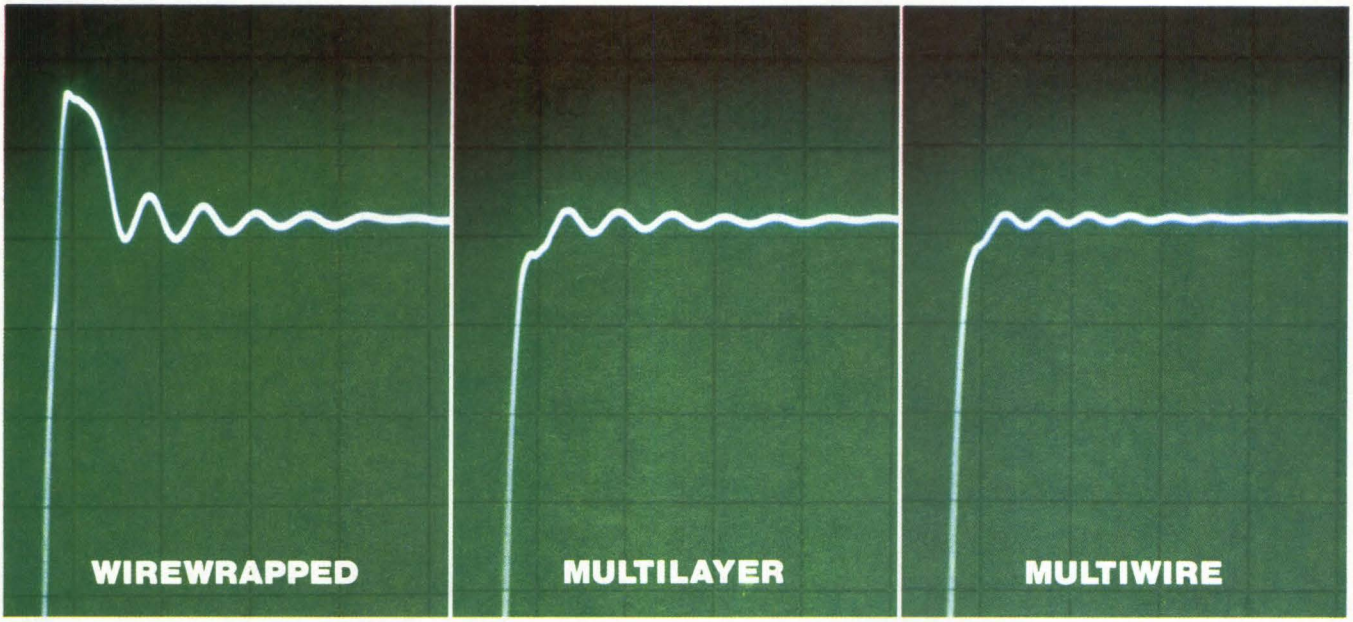
SPLIT SPEED FULL-DUPLEX MODEM

Freestanding DF03 modem, offered in AA and AC versions, operates asynchronously at 0 to 300 or 1200 bits/s, and synchronously at 1200 bits/s. Both versions feature manual originate, manual answer, and automatic answer mode; DF03-AC adds automatic originate, provides serial auto call at 1200 bits/s, and includes 16-digit storage for dialing and redialing. Units are compatible with Bell System 212A modem and DEC's communication controllers that support EIA RS-232-C std and offer Public Switched Telephone Network modem control. DF03-AA is priced at $950, and DF03-AC, at $1350. **Digital Equipment Corp,** Merrimack, NH 03054.

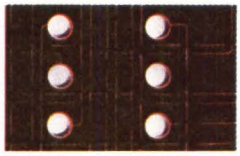
Circle 343 on Inquiry Card

Multiwire* Optimizes ECL.

These traces tell the story.



Wirewrapped and multilayer circuit boards can handle the high speeds of emitter-coupled logic. But Multiwire does it better. With Multiwire, *board impedance is precisely controlled* to meet circuit specs and is *consistent from signal to signal and board to board.* The problem of signal reflections with wirewrapped and multilayer requires the use of discrete series-damping and terminating resistors. Multiwire reduces design problems, provides consistent electrical characteristics, and results in lower cost and better circuit performance. Add to that other Multiwire advantages: less design time, shorter lead times, easy circuit changes, reduced inspection costs, and higher production yields. The choice is obvious. Multiwire is the way to go. Write or call today for details.



A typical example of the circuit density achievable with Multiwire circuit boards.

Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307

*Multiwire is a U.S. registered trademark for the Kollmorgen Corporation discrete wired circuit boards.

MULTIWIRE DIVISION
KOLLMORGEN CORPORATION

CIRCLE 129 ON INQUIRY CARD

DATA COMMUNICATIONS

32-BIT CRC GENERATOR/CHECKER

COM 8004 performs 32-bit CRC generation and detection for SDLC and HDLC type data protocols. Inserted in serial data path between USRT and modem, it uses a 32-bit polynomial (as specified in Autodin II and Ethernet) to reduce probability of undetected error to 1 in 3×10^9. CRC level provided on high level synchronous receiver/transmitters is generally 16-bit. Unit is available in both plastic and ceramic packages. Price in plastic at 100 pieces is $15. **Standard Microsystems,** 35 Marcus Blvd, Hauppauge, NY 11787.

Circle 344 on Inquiry Card

SDLC CAPABILITY FOR 68000 SYSTEM

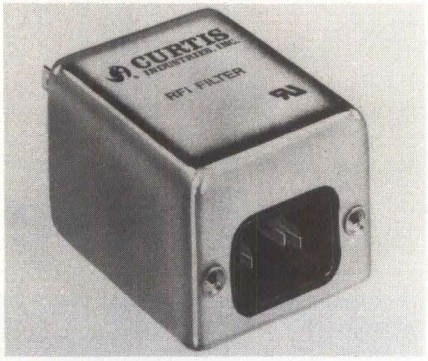
SDLC networking (QNET) capability is included in 68000 computer system for business and industry. Consisting of 8" (20-cm) floppy disc, 20M-byte Winchester disc with tape cartridge backup, 14" (36-cm) CRT, and 256k-byte main memory, the system is packed in a 19" (48-cm) rack. Its 8-MHz 68000 processor uses 16-bit external bus but operates on 32-bit internal values. QNET operates at 800k baud and interconnects up to 255 computers, terminals, or I/O devices. **Q1 Corp,** 125 Ricefield Ln, Hauppauge, NY 11787.

Circle 345 on Inquiry Card

EMI PROTECTION

RFI POWER LINE FILTERS

Series F1600 filters for attenuation of switching power supply emissions feature "T" section and dual-coil design to provide high insertion loss. Filters offer low leakage current, are designed in accordance with VDE and SEV specifications, and operate on 50/60 Hz with dual current rating of 3 A at 115 V, or 1.5 A at 250 V. IEC connector on line side and quick connects on load side increase chassis space efficiency and reduce wiring time. **Curtis Industries, Inc,** 8000 W Tower Ave, Milwaukee, WI 53223.



Circle 346 on Inquiry Card

ELECTRICALLY CONDUCTIVE MOLDING RESIN

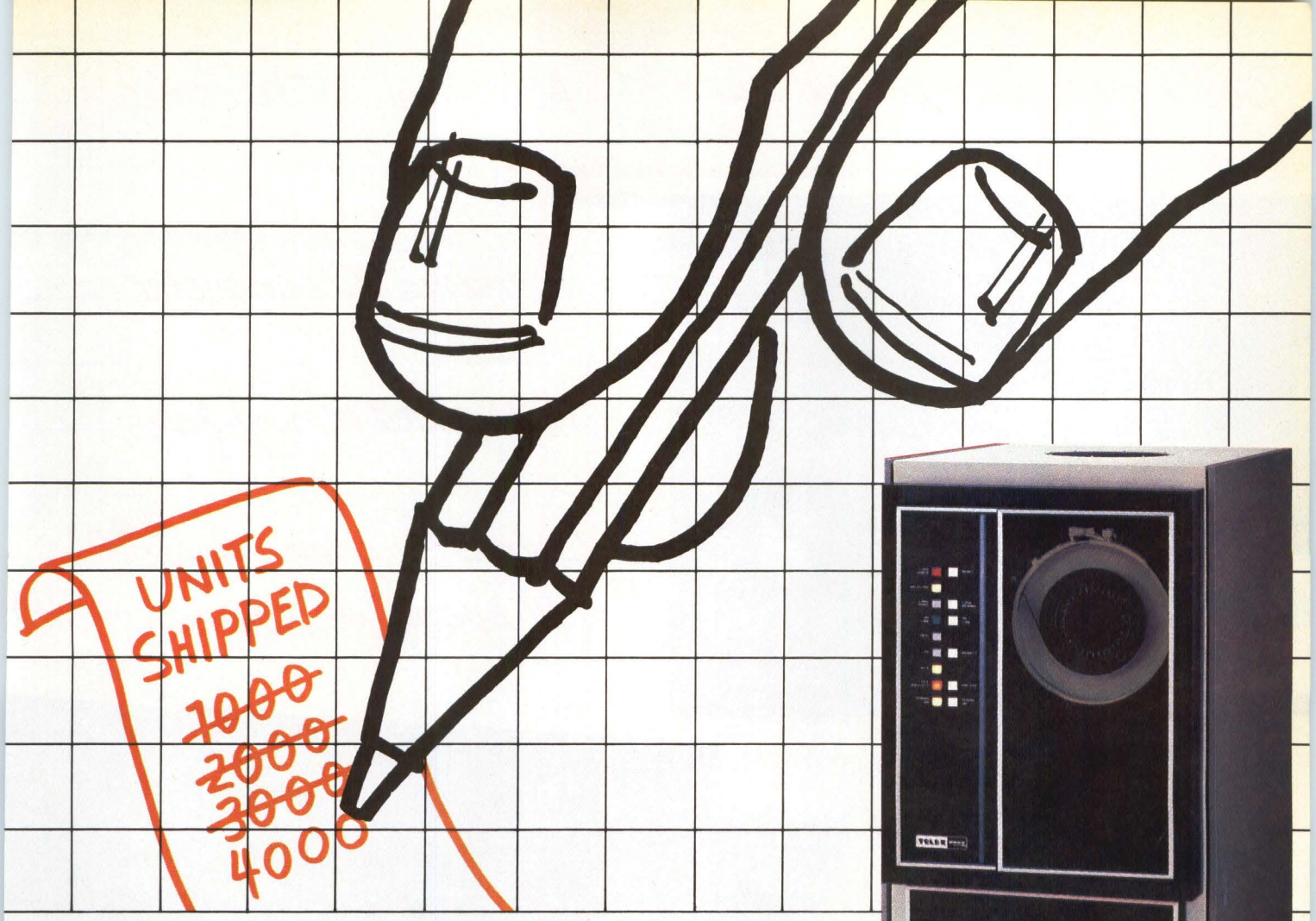
Plasticon™ EC-636 conductive nylon 6/6 molding resin for emi/rfi shielding provides 20 to 30 dB of attenuation for electronic enclosures in the 1- to 1000-MHz range. Processed by conventional thermoplastic screw injection molding technology, its proprietary composition is based on aluminum flake and graphite fillers. Typical applications include instrument housings, control modules, calculators, terminal boxes, and handheld electronic packages. **Plastic Systems, Inc,** 88 Ellsworth St, Worcester, MA 01610.

Circle 347 on Inquiry Card

RFI/EMI SHIELDING COATINGS

Stabilized nickel conductive shielding coatings withstand temperatures up to 150 °F (64 °C) and still hold 2 Ω, providing an economical way of complying with FCC regulations, including FCC 79-555-14686. Coatings are electrically calibrated to meet simple methods of bleed off and electrostatic discharge, and exceed the strictest rfi and emi shielding specifications. **Advanced Coatings & Chemicals,** 4343 Temple City Blvd, Temple City, CA 91780.

Circle 348 on Inquiry Card



Join the leading computer houses . . . specify Telex GCR.

The word is out. Telex GCR Tape Subsystems are the most proven, high performance rack-mountable GCR units available. Field proven in demanding seismic operations. Compatibility proven by five CPU manufacturers. Versatility proven in system house interfaces to sixteen different CPU's.

That's why the leading computer houses are specifying Telex GCR. The Telex 6200 family is available in the model 6253 (6250/1600/800 bpi), 6250 (6250/1600 bpi) and 6240 (1600/800 bpi) tape drives and 6850 tri-density formatters. Tape speeds of 50, 75 and 125-IPS are available. In addition, Telex engineers will provide experienced assistance in making Telex subsystems enhance your high performance computer systems.

With more than 4,000 units shipped (most for high speed 125-IPS operation with tri-density capability), customers are discovering that Telex provides a design, manufacturing and quality maturity that is unmatched in the marketplace today. They get field proven maturity and a lower total cost of ownership. With your name on the line, Telex should be in the system.

For more information, contact the nearest Telex OEM Sales Office listed or phone our OEM Marketing Department in Tulsa.

(918) 627-1111.

Model 6253
Tape Subsystem

Telex Computer Products, Inc.
Terminals/Peripherals/Systems/OEM Products
6422 East 41st/Tulsa, Oklahoma 74135
(918) 627-1111

- Amherst, NH (603) 673-9272
- Southfield, MI (313) 352-2720
- Garden Grove, CA (714) 898-9833
- Houston, TX (713) 497-6770

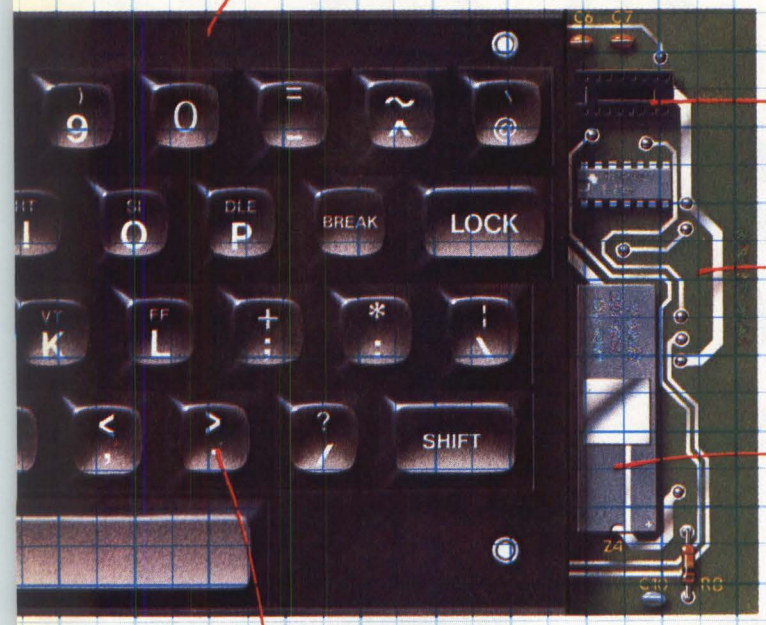
The innovation continues . . .

TELEX®

CIRCLE 131 ON INQUIRY CARD

Cover plate, no special cut-out.

Note
All normal ASCII codes.

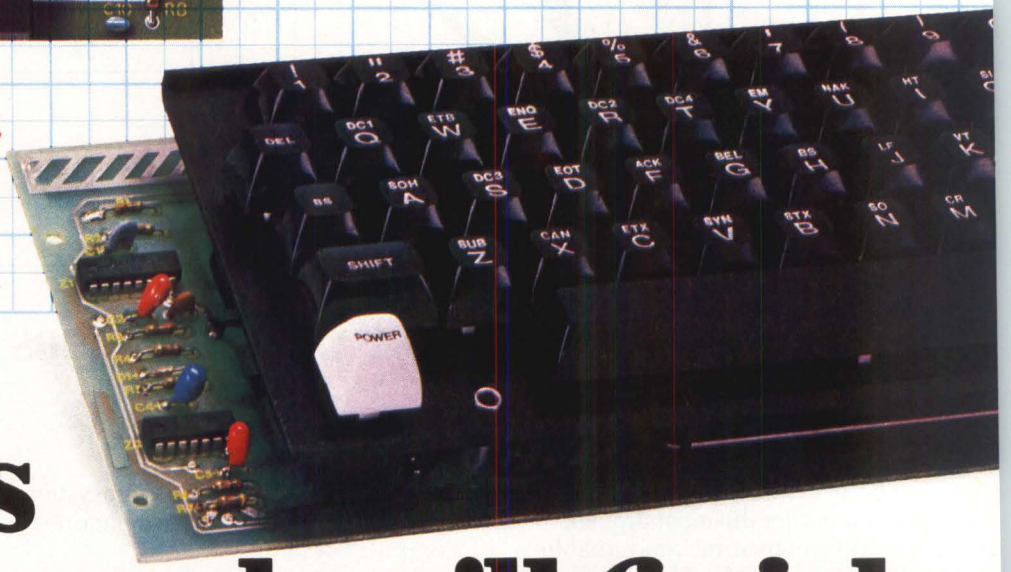


Standard IC connector.

PCB plated through-holes.

Cherry Encoder will do it!
(No special de-bounce circuit.)

2-shot molded keycaps.



Show us the spec and we'll finish the keyboard.

When you come to Cherry for a keyboard your problems are over. You pass them on to us, because we'll take over your project from conception right through to quantity production.

We have the engineering skills and experience to more than satisfy all your individual requirements, and our keyboard capability extends across the whole spectrum of keyboards. Whether you want a full word-processor or typesetting model, a board for a standard intelligent terminal or lineprinter, a point-of-sale or home-computer unit, or a special key-pad, standard design or custom, we'll provide the necessary technology and quality — at the right price.

CHERRY®

Cherry. The key name in keyboards.

CHERRY ELECTRICAL PRODUCTS CORP. 3614 Sunset Ave., Waukegan, IL 60085 ☐ 312/689-7612 ☐ TWX: 910-235-1572

Worldwide affiliates and phone numbers: Cherry Semiconductor Corp., East Greenwich, RI, U.S.A., 401-885-3600 • Cherry Mikroschalter GmbH, Auerbach, Germany, 09 643 181 • Cherry Electrical Products Ltd., Harpenden (Herts) England, (05827) 63100 • Cherco Brasil Industria E. Comercio Ltda., Sao Paulo, Brazil, 55 (011) 246-4343 • Hirose Cherry Precision Co., Ltd., Kawasaki, Japan, 044 933 3511

CIRCLE 132 ON INQUIRY CARD

EMI PROTECTION

CONDUCTIVE ELASTOMER

Designed for emi/rfi shielding applications, CHO-SEAL[R] 1285 is based on aluminum filler particles uniformly dispersed in silicon elastomer. Features include continuous use temperature of 200 °C, high aluminum content that enhances compatibility with aluminum flanges, high temperature aging stability, light weight, and vibration performance similar to silver-copper elastomers. Product is available in sheet and die cut form, and in custom molded shapes. **Chomerics, Inc,** 77 Dragon Ct, Woburn, MA 01888.

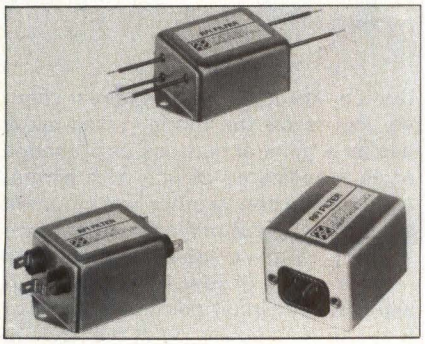
Circle 349 on Inquiry Card

EMI SHIELDING AND ENVIRONMENTAL SEAL

Composed of highly conductive, resilient, knitted wire mesh shielding strip mated to specially shaped silicone rubber, Duosil provides effective emi shielding and environmental sealing. Small cross-section structure saves space and weight without sacrificing shielding or sealing effectiveness and is suited for installation into narrow grooves in cast enclosures. **Tecknit,** 129 Dermody St, Cranford, NJ 07016.

Circle 350 on Inquiry Card

RFI POWER LINE FILTERS



SK series filters reduce conducted noise to comply with FCC specifications in U.S. and VDE 0871 requirements in West Germany, and are suited for equipment with high line to ground or line to line conducted emissions. Offered with nonrotating quick connect/solder terminals, wire termination, or an IEC connector, filters are available in 3-, 6-, and 10-A versions at 115 Vac, or 1.5-, 4-, and 6-A versions at 250 Vac. Prices range from $19.80 to $31.15 in small quantities. **Corcom Inc,** 1600 Winchester Rd, Libertyville, IL 60048.

Circle 351 on Inquiry Card

POWER SOURCES & PROTECTION

UPS FOR DC-DC CONVERTERS

Designed to deliver 100 W or less, LS500 series features integral battery charging system and operates in conjunction with the company's 1-, 2-, and 3-output dc-to-dc converters and 12-V battery. During ac line failure and on restoration of line power, output regulation is maintained and is transient free. Transition time from line to battery and vice versa is 1 ms. Input is 115/230 Vac, 47 to 440 Hz, with output of 24 Vdc at 2 A, unregulated. Battery system charges external 12-V battery during normal ac line operation. **Converter Concepts, Inc,** 435 S Main St, Pardeeville, WI 53954.

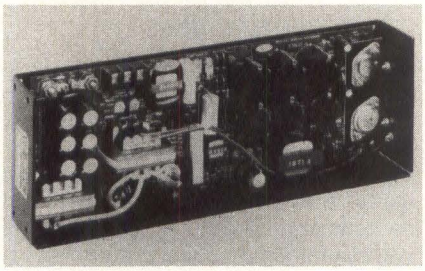
Circle 352 on Inquiry Card

TRANSIENT SURGE SUPPRESSORS

Unipolar devices connect in shunt across the power line and absorb 95% to 98% of the transient energy with a nonlinear voltage response shunt bypass, reducing transient energy to a level at which it can be controlled and managed by the zero time series devices. Zero time ac devices incorporate a line filter to eliminate differential and common mode emi/rfi and a special TSS circuit to delay the transient wavefront and eliminate overshoot. Zero time dc devices are designed for PC board mounting. Fusing to 20 A is optional. Units provide bidirectional protection from emi/rfi and transient glitches that occur on the board. **Power Integrity Corp,** 300 E Wendover Ave, Greensboro, NC 27408.

Circle 353 on Inquiry Card

250-W MULTIPLE-OUTPUT SWITCHERS

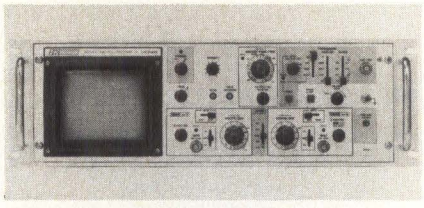


Single- and multiple-output versions in 5 different 5F-Series models feature a dual, wide input range of 90 to 132/180 to 264 Vac for greater immunity to line transients and brownouts, and an input carryover of 16 ms. Maximum power loading is 250 W. Other features include overvoltage protection, foldback current limiting, remote sensing, output voltage adjust, enable/inhibit function, and "output on" LED status indicators for each dc output. Typical prices are $249 for the single-output unit and $379 for the multiple-output unit, in quantities of 1 to 9. **Sierracin/Power Systems,** 20500 Plummer St, Chatsworth, CA, 91311.

Circle 354 on Inquiry Card

TEST & MEASUREMENT

RACKMOUNT, DUAL-TRACE 30-MHz OSCILLOSCOPE



Switch-selectable front and rear channel inputs on the model 1479R allow use as a general purpose oscilloscope or as a dedicated device with permanent connection to other rackmounted equipment. Its 2-mV/cm vertical sensitivity allows observation and measurement of low level signals. A signal delay circuit permits viewing of fast rise time pulses, with max sweep time of 0.1 ms/cm. Single-sweep operation allows observation of irregular waveforms. Video coupling permits synchronization to video frame and line. Price is $1495. **B & K Precision, Dynascan Corp,** 6460 W Cortland Ave, Chicago, IL 60635.

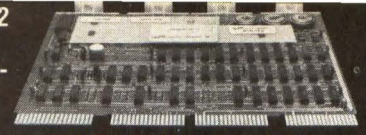
Circle 355 on Inquiry Card

OUR TIMING CONTROL UNIT HELPS YOUR COMPUTER KEEP SCORE OF TIME AND DATE.

Power-up or power-down, your computer always knows the time, *exactly*, with Digital Pathway's Timing Control Unit (TCU). Even during extended power interruptions. Rechargeable battery support makes our TCU immune from power failure of any kind. For as long as three months. And an on-board crystal-controlled oscillator ensures supreme accuracy.

No matter what model computer you have, you'll find our TCUs offer many features that make living with computer timeouts less complicated. And some models can even be set to initiate an interrupt at a chosen date and time. Or at specified intervals.

Find out how we can help make your time more productive. Call or write Digital Pathways today for more information at 1260 L'Avenida, Mountain View, CA 94043. Telephone (415) 969-7600. TWX: 910-379-5034.



*PDP-11 and LSI-11/2 are registered trademarks of Digital Equipment Corp. Others listed are trademarks, respectively, of Intel Corp., Motorola Inc., Hewlett-Packard, Lockheed Corp. and Computer Automation Inc.

*PDP-11	TCU-100	$495
	TCU-150	$460
*LSI-11/2	TCU-50D	$325
*Multi-Bus	TCU-410	$325
*EXORcisor	TCU-68	$325
*HP 2100	TCU-2100	$395
*Lockheed SUE	TCU-200	$550
*Naked Mini	TCU-310	$385
Any Model Computer (RS-232/20mA)	SLC-1	$640

DIGITAL PATHWAYS

NOW YOU'RE SAFE FROM COMPUTER TIMEOUTS EVEN AFTER THE POWER GOES.

Circle 135 on inquiry card.

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Germany: (089) 60 60 71-72 Telex: 5216290 isio d • Switzerland: 022/310587 Telex: 289191

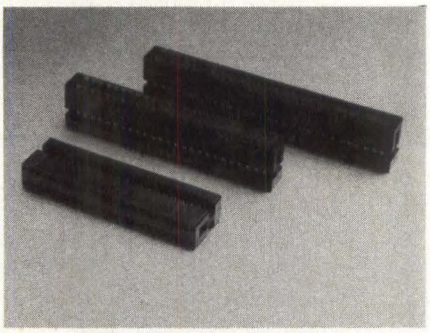
INTERCONNECTION & PACKAGING

3-, 9-, AND 18-SLOT MOTHERBOARDS

Motherboards are available in kits, bare, or assembled and tested in 3-, 9-, or 18-slot versions. MB-3 3-slot board is offered for standalone applications, using CPU, memory, and D-A or A-D cards. MB-9 9-slot card is intended for small systems using CPU, memory, I/O, graphics, and other accessories. The 18-slot MB-18 is for use in full-size system applications. Both 9- and 18-slot cards use active termination to eliminate crosstalk and reflection problems. All have extensive ground shield to eliminate interference and noise and breadboard area for customizing board. **Ackerman Digital Systems, Inc,** 110 N York Rd, Suite 208, Elmhurst, IL 60126.

Circle 356 on Inquiry Card

BACKPLANE SOCKET CONNECTOR



Series W6300 is designed for direct interface to 0.025" (0.64-mm) square wirewrap pins. Contact centers are 0.100" x 0.200" (2.54 x 5.08 mm) and feature preassembled unit construction. Selective keying of one or more of the blind cavities on the insulator, combined with mating pin loading of the backplane connectors, provides foolproof polarization. Matching planar cable is available in 26 or 28 AWG solid, and 26 or 28 AWG stranded wire sizes. Current rating is 1 A and dielectric withstanding voltage is 500 V min at sea level. **Stanford Applied Engineering, Inc,** 3520 De La Cruz Blvd, Santa Clara, CA 95050.

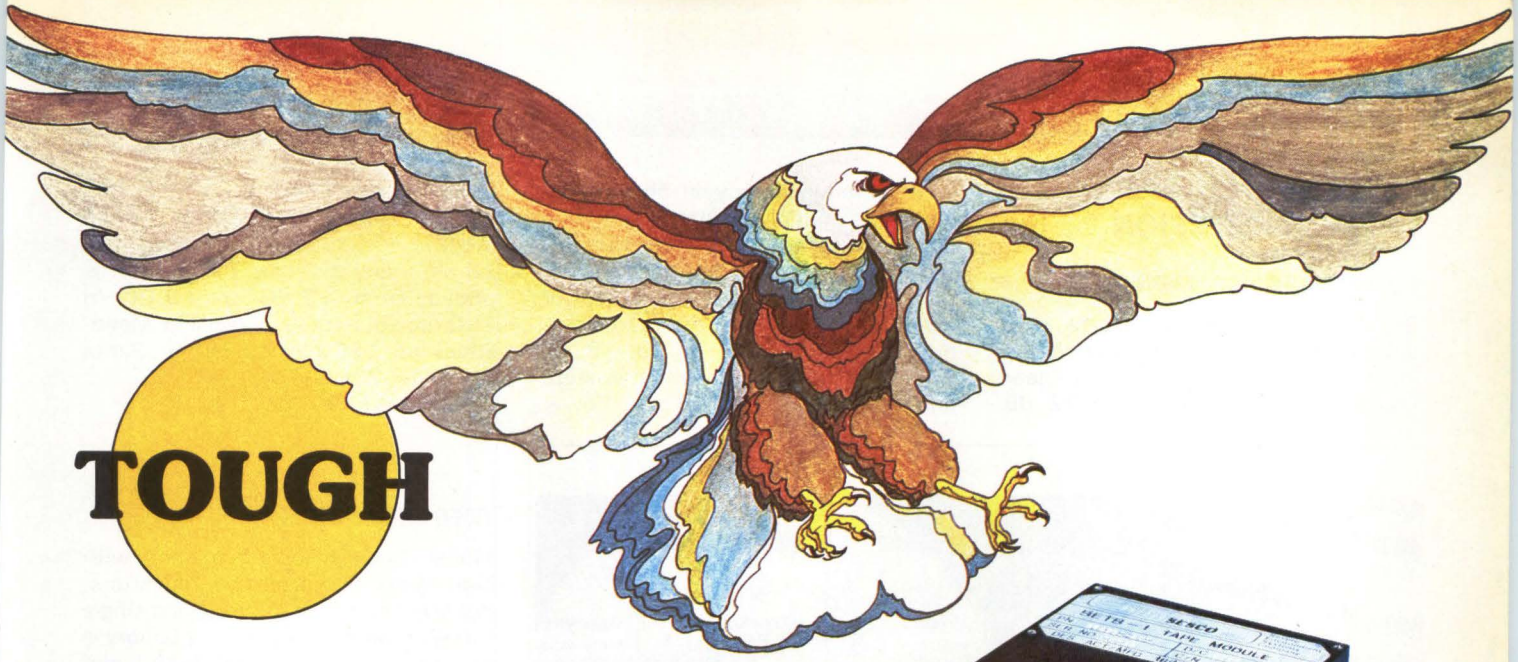
Circle 357 on Inquiry Card

MEMORY SYSTEMS

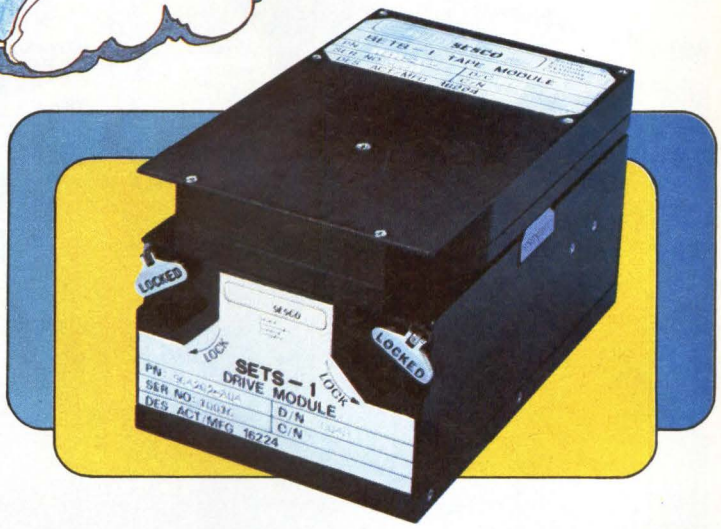
65k x 9 DYNAMIC MEMORY MODULE

Module GMS6505 offers up to 65,536 bytes in four 16k arrays, addressable in 4k increments. Arrays can be write protected. Ninth bit in each byte stores data for onboard parity generation and parity check. User can address multiple 65k banks. The 6" x 9.75" (15.2- x 24.8-cm) module uses 5-W power and directly interfaces Motorola EXORcisor II, Rockwell AIM 65, and SYSTEM 65 motherboards. Single-unit price of 65k board with no parity is $526. **General Micro Systems, Inc,** 1320 Chaffey Ct, Ontario, CA 91762.

Circle 358 on Inquiry Card



TOUGHER!



SETS-1: A 23-megabit digital tape system for severe environments

The soaring eagle is tough. Our SETS-1 digital tape system is tougher... on the ground as well as in the air.

Built Tough for Tough Jobs

Whatever the application — industrial, military or aerospace — this rugged recorder is built to take on the most hostile environments. It meets MIL-E-5400, 4158, 16400... and more.

Right now SETS-1 is being used by the Army and Air Force for bulk storage and data gathering from tanks, aircraft and remote sites. Also for mission loaders, communications and fire control systems. Its wide operating temperature range of −55°C to +71°C makes it perfect for a growing number of industrial requirements, too.

A Top Performer

As for performance, there is none higher. A removable, hermetically sealed tape cartridge stores 23 megabits of data at 1600 bits-per-inch on 300 feet of 1/4-inch magnetic tape. Plus it offers bidirectional read/write on 4 tracks with a 192K bit-per-second transfer rate.

Small, Light, Dependable

Solid throughout, SETS-1 features an all-aluminum case that measures a compact 4" by 6" by 3.6". Quick, easy maintenance is assured by plug-in modularity. The drive module holds a reliable brushless D.C. motor and all electronics while the magnetic tape, head, sensors and capstan drive are contained in a separate tape module. All together, the entire package weighs in at under 5 pounds!

See What Tough Really Means

Phone or write for complete details today. You'll soon know why our SETS-1 tape system deserves to be called the "tough one"!

Severe Environment Systems Company
A Subsidiary of Electronic Memories & Magnetics Corporation
P.O. Box 668 • Chatsworth, CA 91311
Telephone: (213) 998-9090 • TELEX: 69-1404

COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS

CIRCLE 137 ON INQUIRY CARD

DATA CONVERSION

8-BIT BIPOLAR COMPANDING DAC

Sign-magnitude coded DAC-78 provides a straight line approximation of a logarithmic curve rather than a linear response. Dynamic range is 72 dB with 12-bit accuracy in chord 0. It supplies a multiplying input and a logic threshold control that enables interfacing with all logic families, and requires no bipolar offset adjustment or zero scale trim. Device offers true output compliance of −5 to 18 V, 500-ns settling time to within ½ step, and full scale drift of 1/16 step. Power dissipation is 114 mW with 5- and −15-V supplies. Operating temp range is −25 to 85 °C. Supplied in an 18-pin hermetic DIP, the device is priced from $7.50 to $9.00 in 100-unit quantities. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.

Circle 359 on Inquiry Card

VIDEO FRAME STORE

Model 274C, a solid state memory with high speed A-D and D-A converters, digitizes, stores, and displays a single frame of video information. Memory is organized as 512 x 512 picture elements with 8 bits of gray scale (256 levels). Video output is a standard video signal synchronized to video input, and can be switched or mixed with other video signals or recorded on conventional tape recorders. Digital I/O option allows individual picture elements in stored image to be accessed by computer, processed, and returned to store memory. Price is $12,000. **Colorado Video Inc,** PO Box 928, Boulder, CO 80306.

Circle 360 on Inquiry Card

50-CHANNEL DATA LOGGER

Standalone battery operated data logger SABEL 85MC has a 50-channel capacity and accepts digital data inputs in either parallel BCD or counting inputs. Outputs can be 8-bit parallel, RS-232-C, or IEEE 488. Internal automatically charged battery operates system and memory if power fails and allows field operation where there are no power lines. It has built-in cold junction compensation, signal conversion, and linearization for types J, K, T, and S thermocouples. A-D converters are autoranging, autozeroing, and integrating. 10-digit realtime clock allows programmable, completely unattended data logging. **Consolidated Controls Corp,** 15 Durant Ave, Bethel, CT 06801.

Circle 361 on Inquiry Card

A NEW TWIST ON THE OLD PUSH AND PULL.

For a lot of applications, you're designing an interconnect system that someone will pull apart. And then push together. Over and over again. So you need connectors that can take a beating, mate quickly, handle high contact densities and stay within tight budgets.

Look no further than the Cannon® DL "ZIF" Series. Our Zero Insertion Force (ZIF) connectors can handle from 60 to 2496 contacts. Have a minimum rated life of 10,000 complete mating/unmating cycles. And can be mated in less than two seconds even with close to 2500 contacts.

ZIF connectors are flame retardant and rated for 3 amperes of current. You get crimp or wire wrap contacts that can be hand or machine terminated. And a lower cost per mated line than other competitive industrial/commercial high density connectors.

Try our ZIF Series connectors. You'll get a new twist on the old push and pull.

Contact the Rectangular Division, ITT Cannon Electric, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. (714) 964-7400. In Europe, contact ITT Cannon Electric, Avenue Louise 250, B-1050 Brussels, Belgium. Telephone: 02/640.36.00.

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CIRCLE 139 ON INQUIRY CARD

TURN ANY COMPUTER INTO A POWERFUL MEASUREMENT AND CONTROL SYSTEM.

MACSYM 20 OFFLOADS YOUR HOST AND ALSO STANDS ALONE.

MACSYM 20 is the measurement and control front end with a difference. Its superior intelligence frees up your host computer for other important tasks. And because it's programmable, MACSYM 20 can function on its own should your host go down.

MACSYM 20 CONNECTS DIRECTLY TO YOUR SENSORS.

Select the functions you need from our extensive family of I/O cards, and connect MACSYM 20 directly to the sensors. MACSYM 20 can accommodate up to 500 different I/O channels, and the signal conditioning is already done.

MACSYM 20 OPERATES IN HARSH ENVIRONMENTS.

MACSYM 20 can operate even in rugged environments because no movable mass storage devices are used. You have your choice of downline loading programs from your host computer into RAM memory on MACSYM 20, or burning the programs into PROM.

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LIMIT SWITCHES
4–20 mA
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To get more information on MACSYM 20, simply fill out and return this coupon, or call your nearest Analog Devices office listed below.

MACSYM 20

I have an immediate need for intelligent I/O front ends.

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ANALOG DEVICES

Analog Devices, Inc., Box 280, Norwood, MA 02062; Headquarters: (617) 329-4700; California: (714) 842-1717, (408) 947-0633; Illinois: (312) 653-5000; Ohio: (614) 764-8870; Pennsylvania: (215) 643-7790; Texas: (713) 664-5866; Belgium: 031/37 48 03; Denmark: 02/84 58 00; France: 01/687 34 11; Holland: 20-51080; Israel: 3/052-21023; Japan: 03/263 6826; Sweden: 08-282740; Switzerland: 022/31 57 60; United Kingdom: 01/941 0466; West Germany: 089-530319; and representatives around the world.

CIRCLE 140 ON INQUIRY CARD

DATA CONVERSION

3½-DIGIT ADC

Providing analog and digital circuitry on a single CMOS IC, 14433 dual-slope converter features automatic polarity, zero offset, rollover error of less than one count, true over- and underrange indication, multiplex BCD output, and two input ranges with 1.999 mV full scale and 1.999 V. Unit operates with virtually any display, over a wide range of power supply voltages. Device can measure physical parameters and is offered in 24-pin ceramic or plastic package. Prices in quantities of 100 are $11.86 (plastic) and $15.42 (ceramic). **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mountain View, CA 94043.

Circle 362 on Inquiry Card

6-BIT PARALLEL A-D CONVERTER

Featuring sample rate of 18 MHz, ZN440 is stackable to 8 bits by providing an underrange output and accessibility to both ends of the reference chain. Device operates in unipolar or bipolar mode. Without prescaling, it accommodates an input range of −4 to 0.5 V and operates from ±5-V supplies. TTL compatible, converter provides ± ¼-LSB linearity. Output logic is binary with an open collector structure. Up to a 7-MHz sine wave can be digitized without sample and hold; rated power dissipation is 1 W. Offered in a 24-pin ceramic DIP, the device is priced under $60 in quantities of 100. **Ferranti Electric Inc, Semiconductor Products,** 87 Modular Ave, Commack, NY 11725.

Circle 363 on Inquiry Card

12-BIT MULTIPLYING DAC

HI-7541 features CMOS construction and is fabricated using dielectric isolation technology. Device can be used in 12-bit digital-to-analog situations that require a combination of speed, accuracy, and low power. Applications include video monitors, computer terminal displays, waveform synthesizers, high speed avionics or military data acquisition and control systems, space instrumentation, and high speed industrial or scientific process control. Pricing for commercial product is $16.50 while military grade products start at $64.00, all in quantities of 100. **Harris Corp, Semiconductor Group,** PO Box 883, Melbourne, FL 32901.

Circle 364 on Inquiry Card

HYBRID 12-BIT A-D CONVERTER

Housed in industry std 24-pin DIP, ADC-5212 operates at 1-MHz clock rate and resolves analog input, bipolar −10 to 10 V to corresponding digital output in 13 μs. Two versions are offered: commercial model operates at 0 to 70 °C, and military model operates at −55 to 125 °C and is processed to MIL-STD-833, method 5088. Absolute accuracy error is ±0.05% of full scale range at 25 °C and is guaranteed not to exceed ±10 ppm/°C. Single-quantity cost ranges from $190 to $485, depending on version. **Intech Inc, Microcircuits Div,** 2270 Martin Ave, Santa Clara, CA 95050.

Circle 365 on Inquiry Card

DATA CONVERSION

12-BIT, 13-μs SUCCESSIVE APPROXIMATION ADC

Available in two unipolar (DDC-5210 and DDC-5211) and two bipolar input ranges (DDC-5212 and DDC-5216), a family of 12-bit analog to digital converters features a 13-μs conversion time. All specifications are met with an externally applied 1-MHz clock. Accuracy to ±0.05% FSR is assured and ½-LSB linearity error is guaranteed with no missing codes over the specified temperature ranges of 0 to 70 °C and −55 to 125 °C. MIL-STD-883B parts are available. Housed in hermetically sealed 24-pin double DIP, the hybrid devices consume 670 mW, typical. ILC **Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

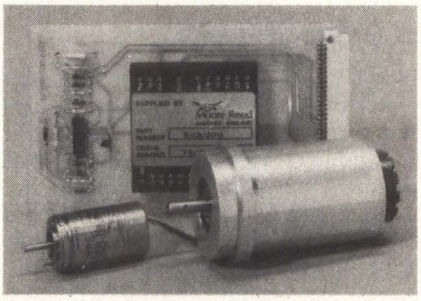
Circle 366 on Inquiry Card

SYNCHRO/RESOLVER-TO-DIGITAL CONVERTER

16-bit Type II tracking converter with zero velocity lag error, SRD546 provides built-in test feature that supplies logic 1 when tracking error exceeds ±1°. Automatic gain compensation circuit allows ±30% signal voltage variations without degradation in accuracy or change in converter hysteresis. Operating from reference voltage of 10 to 130 Vrms, units feature pin programmability for both synchro and resolver inputs and line to line signal voltages of 11.8, 26, and 90 Vrms. Price in quantities of 1 to 9 is $695. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

Circle 367 on Inquiry Card

RESOLVER-TO-DIGITAL CONVERTERS



Operating from a single 5-V supply, converters mount on 100 x 160-mm Eurocards with DIN 41612 connector. Incremental module provides 4000 counts/revolution using 2-pole resolver, or 20,000 pulses/revolution using 10-pole resolver. Maximum slew rate is 6000 r/min with 2-pole resolver (4000 count) and 1200 r/min with 10-pole resolver (20,000 count). **Moore Reed and Company Ltd,** Walworth Industrial Estate, Andover, Hampshire, England.

Circle 368 on Inquiry Card

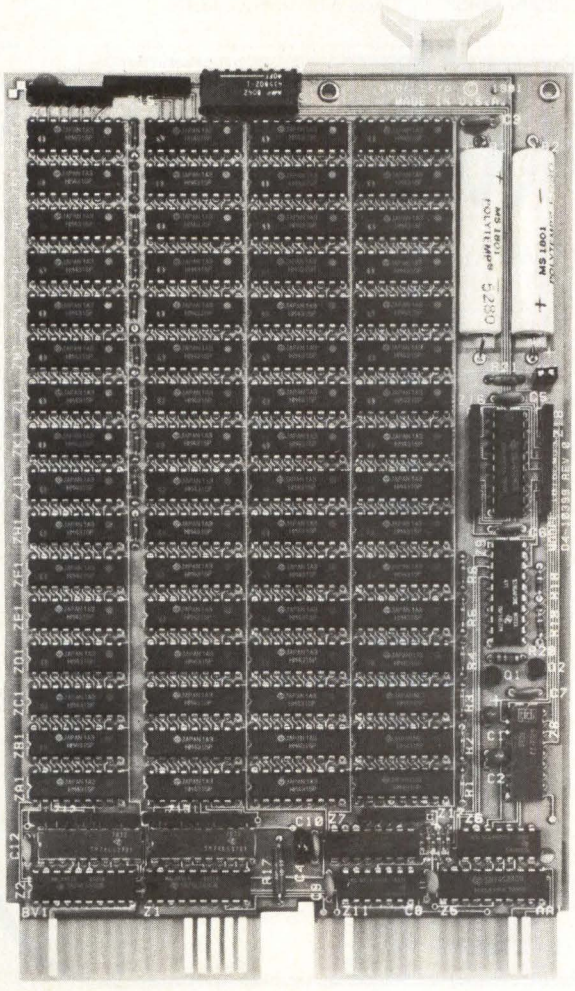
12-BIT D-A CONVERTER

HS DAC87, a direct plug-in replacement for industry std DAC87, operates over full military temp range and is packaged in 24-pin hermetically sealed ceramic DIP. Available with MIL-STD-883 screening, unit includes reference, output amplifier, and matched bipolar switches in voltage output version. Current output versions include all elements except output amplifier, which can be added externally. Input coding is complementary binary/complementary offset binary. Price ranges from $99 to $120 in quantities of 100. **Hybrid Systems Corp,** 22 Linnell Circle, Suburban Industrial Pk, Billerica, MA 01821.

Circle 369 on Inquiry Card

Only from adac...

Non-volatile CMOS memory for LSI-11 retains data during power failure.



- 16K word ADD-IN memory replaces bulky core
- On-board battery back-up assures data retention up to a full week without external power
- Decodes 18 bit address and allows the RAM to start on any 4K boundary
- Low power consumption (5 W typical)
- High speed 450 ns memory chips
- Self-recharging battery
- Long 3 year battery life
- Write protection in 4K blocks—acts like ROM
- Easily accessible switches allow card to be write-protected while in rack

The 1816 CMOS memory is another LSI-11, LSI-11/2 and LSI-11/23 compatible device from ADAC. It is ideal when it's important not to lose data during power outages. And it requires only a fraction of the space and power of comparable core memory. Contact ADAC for full details on this unique memory or any of our analog and digital function cards and complete systems for LSI-11.

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CIRCLE 144 ON INQUIRY CARD

SOFTWARE

FLOATING POINT SOFTWARE

Floating Point Forth allows users to work with decimal numbers in a manner similar to BASIC and FORTRAN. Sixteen- and 32-bit integer capability of FIG Forth is retained, but a floating point mode is added. These are single-precision floating numbers with approx 7 significant decimal digits. Addition, subtraction, negation, multiplication, division, integer conversion, and comparison are supported. Written in 8080 executable code, the package runs on Z80/8080/8085 with 24k memory under CP/M or CDOS. **Timin Engineering Co,** 9575 Genesee Ave, Suite E2, San Diego, CA 92121.
Circle 370 on Inquiry Card

MICROPROCESSOR ASSEMBLER PROGRAM

MACRO META Assembler serves as a tool for programming bit slice microprocessors such as the AMD 2900 and Fairchild Macrologic chip sets, and other wide-word microcoded processors. The package gives users the ability to define variable length microwords, define noncontiguous variable fields, and represent complex overlayed instructions with a single mnemonic. Three separate programs make up the package: a definition program, an assembly program, and a P/ROM formatting program. Written in ANSI standard FORTRAN IV, the assembler runs on any general purpose computer, including 16-bit minicomputers. **Microtec,** PO Box 60337, Sunnyvale, CA 94088.
Circle 371 on Inquiry Card

FORTRAN BASED GRAPHICS SOFTWARE

Cadregraphics, a high level FORTRAN based computer graphics language and software package designed for use in industrial automation and process control applications, provides interface with pixel addressable color graphics display systems as a method of developing customized displays. Free-format language is easily learned by computer personnel, and most display pictures are completed in less than 8 hours. Optional alarm feature alerts operator to out-of-tolerance conditions. **The Cadre Corp, Technical Facilities and Computer Applications Group,** PO Box 47837, Atlanta, GA 30362.
Circle 372 on Inquiry Card

FORTRAN 77 OPTIMIZING COMPILER

Machine independent optimization enhancements for full FORTRAN 77 compiler include invariant code movement, strength reductions, constant folding, and common subexpression elimination. Compiler also performs peephole and other machine dependent optimizations dependent upon target system. **Advanced Computer Techniques Corp,** 437 Madison Ave, New York, NY 10022.
Circle 373 on Inquiry Card

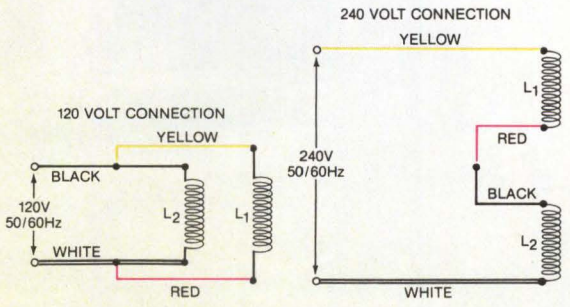
Dual voltage. For wherever in the world you connect!

Here's 60Hz and 50Hz, 120- and 240-volt versatility in one fine axial cooling fan for domestic and foreign applications. CFM ranges from 20 to 120. With or without venturi. And a choice of three designs for mounting on 4⅛" or 2 13/16" centers.

All from a top name in electric motors for just about everything—Gould. These Brutes feature Gould's open frame design and patented Recirk™ bearing lubrication system for extended life.

Metal parts are coated with a corrosion inhibitor and only flame-retardent plastics are used. U.L. recognized and CSA certified. Special modifications can be designed in.

For more details or to order these inventory-reducing fans, call (315) 788-5530. Gould Inc., Electric Motor Division, 6393 Coffeen Street, Watertown, NY 13601.



GOULD

An Electrical/Electronics Company

CIRCLE 146 ON INQUIRY CARD

INTEGRATED CIRCUITS

PULSE WIDTH MODULATOR

Designed specifically for dc motor control, SG 1731 is the control element in motor-driven servo systems for precision positioning and speed control, and in audio modulators and amplifiers using carrier frequencies to 350 kHz. The modulator provides bidirectional pulse train output in response to the magnitude and polarity of analog input signals. The circuit features externally programmable deadbands to control power consumption, stiffness, and stability; and an internal operational amplifier for error voltage generation. A triangle waveform oscillator requires only one external capacitor to set the frequency. A summing/scaling network permits level-shifting of the triangle waveform for pulse width modulation.

Output voltage for SG 1731 is ±3.5 to ±15 V. Power dissipation at 25 °C is 1000 mW. Unit is characterized for operation over the military range of −55 to 125 °C. SG 2731 is characterized for operation from −25 to 85 °C, and SG3731 is rated from 0 to 70 °C. All devices are supplied in 16-pin cerDIPs. **Silicon General, Inc,** 11651 Monarch St, Garden Grove, CA 92641.

Circle 374 on Inquiry Card

4k x 4 BIPOLAR P/ROM

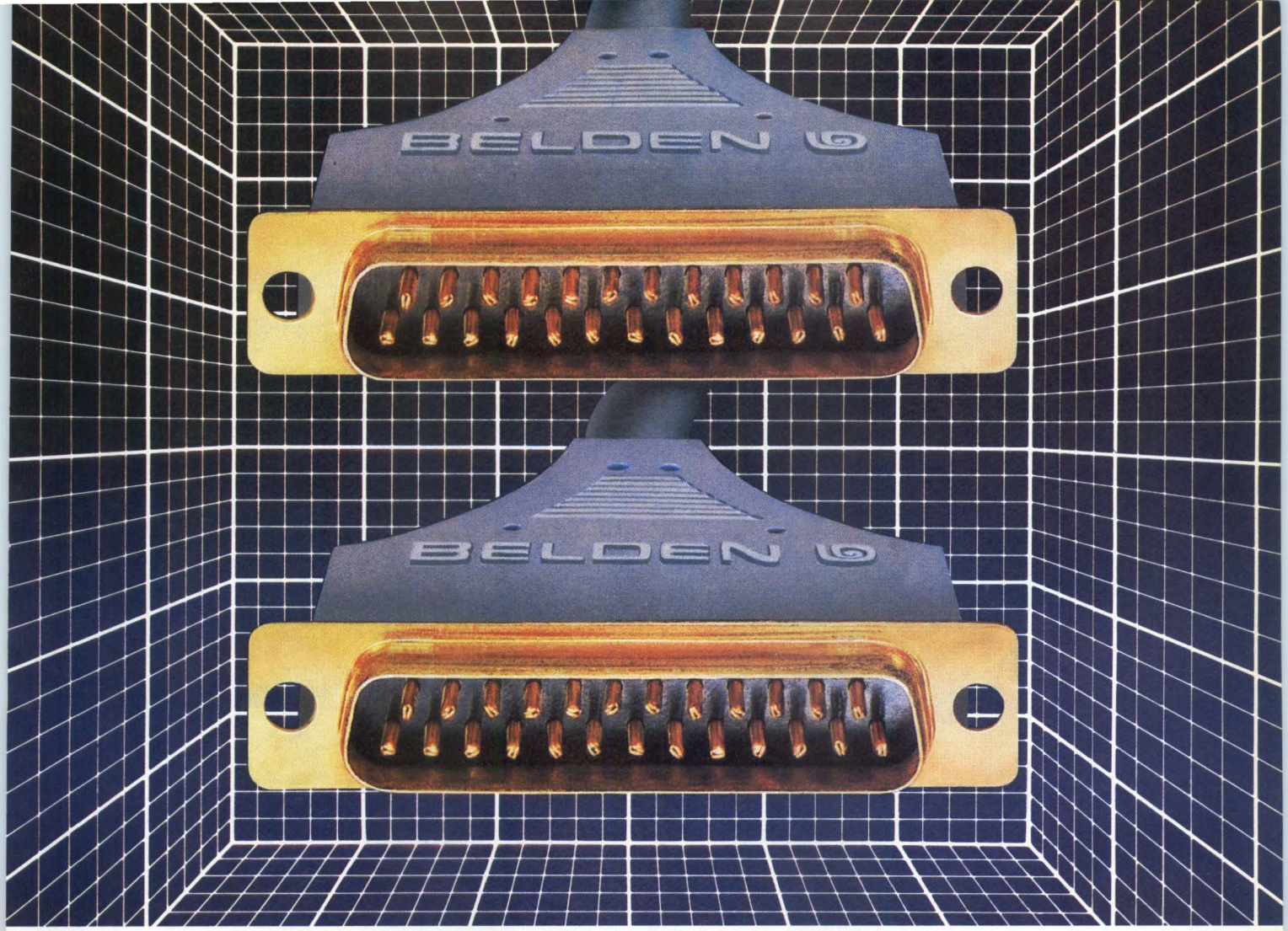
Produced in a 300-mil (0.08-mm) center, 20-pin DIP, with JEDEC approved pinout, Am27S40 (open collector output) and Am27S41 (3-state) offer a 50-ns max access time in std versions and 35-ns access in A versions. 3-state power switched Am27PS41 reduces power consumption from 875 to 425 mW when deselected. Power-up to full accessibility takes 10 ns. The devices use proprietary platinum-silicide fuse that is easy to program and has shown no failures in over 13G hours of life tests. Prices in 100-unit lots start at $44.90 each. **Advanced Micro Devices, Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 375 on Inquiry Card

FAST 16k CMOS STATIC RAM

IDT 6116 offers user selectable max access times of 70, 90, and 120 ns. Organized as 2k x 8, device consumes 180 mW in operation, and 100 μW in standby. Static operation requires no clocking or refreshing circuitry. Ratioless circuits and differential sense circuits for output sense amps allow required 5-V (±10%) power level to drop to as low as 2 V during emergency standby, with full data retention. Its 24-pin package has industry standard pinouts. Sample quantities are available for $50 (120 ns), $70 (90 ns), and $90 (70 ns). **Integrated Device Technology,** 21580 Stevens Creek Blvd, Suite 107, Cupertino, CA 95014.

Circle 376 on Inquiry Card



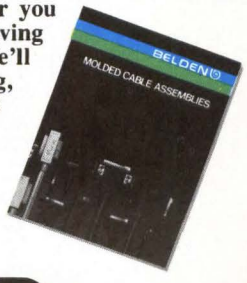
One of these cable assemblies can cut your interference levels 59 db.

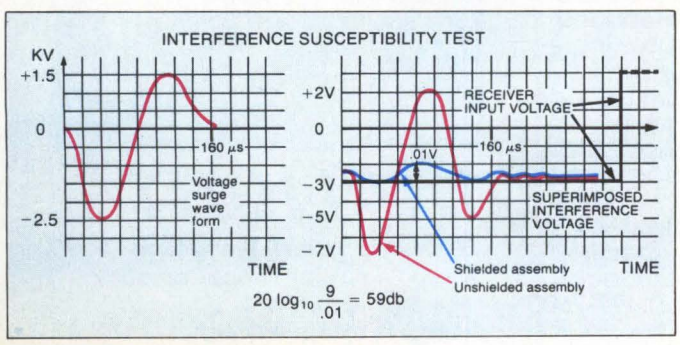
Both meet RS-232-C specifications. Both are made by Belden using rugged materials and proven designs.

But one is shielded. One is not. And that can make a big difference in critical data communications applications.

Although RS-232-C standards do not specifically call for shielded interconnect devices, our research indicates that cable *and* connector shielding is required to insure the signal integrity of the assembly. In fact, transfer impedance, leakage current power spectrum, electrostatic discharge and interference susceptibility tests at Belden all demonstrate the value of Belden totally shielded connector-cable assemblies over nonshielded assemblies.

With a complete line of rugged and highly reliable standard molded connector designs including GPIB, and complete custom design capabilities, we can make exactly what you need, when you need it. And show you ways to increase performance without increasing costs. Whenever you have a shielding need or a question involving interconnect devices, contact Belden. We'll share our experience. For a free catalog, write Belden Corporation, Interconnect Systems Operation, 105 Wolfpack Rd., Gastonia, NC 28052. Phone: (704) 865-4513.





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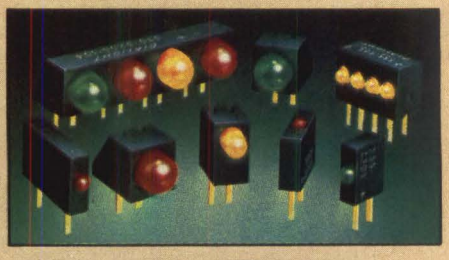
CIRCLE 148 ON INQUIRY CARD

DIALIGHT LED CIRCUIT BOARD INDICATORS STEP UP YOUR PRODUCTION BY ELIMINATING PRODUCTION STEPS.

You'll save money when you stop mounting LEDs on PC boards the old way — bending leads, inserting holders, adding resistors — and start using LED Circuit Board Indicators from Dialight.

Mounting our LED Circuit Board Indicators is easier and less time-consuming. They eliminate production steps and reduce labor costs. Not only is positioning faster, it's far more accurate. As soon as you insert the assembly you are ready for wave soldering. Dialight originated the idea of packaging LEDs for easy mounting on PC boards. And we've developed over 50 different Circuit Board Indicators in red, green, yellow and red/green bicolor. Choose single-element LEDs or QUAD-LED™ four-element arrays with a wide range of voltages with or without current limiting resistors.

Send for our catalog. And the next time you need LEDs for PC boards, eliminate steps and save money — specify Dialight. 203 Harrison Place, Bklyn., NY 11237 (212) 497-7600 TWX: 710-584-5487



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CIRCLE 149 ON INQUIRY CARD

See Us at WESCON Booth Numbers 1513, 1515 and 1517

INTEGRATED CIRCUITS

64-BIT BIPOLAR RAMs

Two RAMs with noninverting data outputs offer typical access time from address of 50 ns. Devices require single 5-V power supply, are TTL compatible, and are organized in 16-word x 4-bit format. SN74LS219A, with 3-state output, combines convenience of open collector output with speed of totem pole output; SN74LS319A also provides open collector output and has capability for direct interface with data lines that have passive pullup. Both are provided in 16-pin DIPs with 100-mil (2.5-mm) spacing and operate at 0 to 70 °C. Single-unit price for quantities of 100 is $3.60. **Texas Instruments Inc,** PO Box 202129, Dallas, TX 75220.

Circle 377 on Inquiry Card

HIGH SPEED 1k x 8 AND 2k x 8 RAMs

High speed versions of 1k x 8 and 2k x 8 static RAMs are manufactured using the Scaled POLY 5™ process. They achieve high performance and low power dissipation using Address Activated™ circuit design techniques. One of these techniques is a fast $\overline{CE}$ (50% of address access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving. MK4801, the 1k x 8 RAM is offered in a 55-ns version in 24-pin plastic or ceramic DIP. The 2k x 8 device, the MK4802, is rated at 90 ns in both plastic and ceramic 24-pin packages. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 378 on Inquiry Card

PULSE WIDTH MODULATING REGULATORS

XR-494 and XR-495 are pin-for-pin replacements of the TI 494 and TI 495. Each circuit contains an onchip 5-V regulator, 2 error amplifiers, a pulse-steering flipflop, and output control circuits. The chips feature uncommitted outputs for 200-mA sink or source. The 18-pin XR-495 is distinguished from the 494 by a 39-V zener diode that allows applications of over 40-V with a minimum of circuitry. XR-494 has 16 pins and operates up to 40 V. In quantities of 100, 494 is $3.28 (ceramic) and $2.85 (plastic); 495 is $3.99 (ceramic) and $3.56 (plastic). **Exar-Integrated Systems, Inc,** 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088.

Circle 379 on Inquiry Card

INTERFACE

DIGITAL INTERFACE

ADC11 interface, for operation with PDP-11 series computers, provides control capability to trigger simultaneous bank of sample and hold amplifiers and then to sweep a prelisted set of channels at the ADC's maximum sample rate. Data samples of 12 bits or less can be packed into 16-bit words for optimum storage utilization. Features include data chaining and random, sequential, or dwell addressing modes. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.

Circle 380 on Inquiry Card

INTERFACE

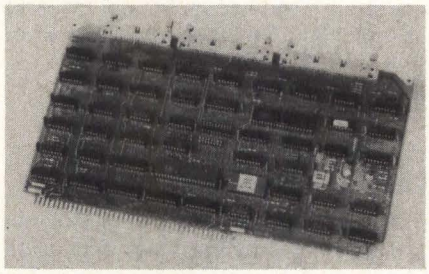
SELF-TESTING LINE PRINTER CONTROLLER

MLSI-LP11A interfaces LSI-11/2 or /23 to any Data Printer line printer with no change in system software. Controller incorporates PrinTest and Loop Back switch activated testing and diagnostic features for enhanced system serviceability. Data status is taken from 8 data lines at controller I/O connectors for both normal operation and test modes and indicated on edge mounted LEDs. Unit also features 4-level interrupt capability; interrupt vectors and device addressing are switch selectable. Price, including cable, is $650. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.

Circle 381 on Inquiry Card

FLOPPY DISC CONTROLLER

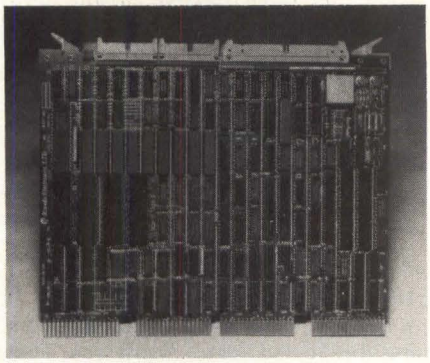
Multibus controller handles four 8" (20-cm) and three 5.25" (13.34-cm) drives. Phase lock loop design allows data transfer reliability of less than 1 error in 1.1×10^9 bits read. All drives may be either single- or double-sided and/or single- or double-density. Unit uses a 4-bit page register for 20-bit addressing, allowing DMA transfer and storage within any 64k of a 1M-byte address field. Unit price is $695. **Comark Corp,** 257 Crescent St, Waltham, MA 02154.



Circle 382 on Inquiry Card

RM02 EMULATING DISC CONTROLLER

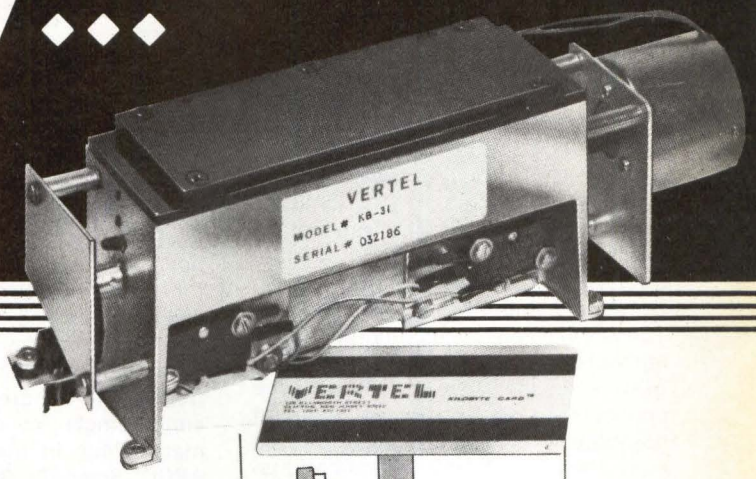
Designed for DEC's LSI-11 series computers, Atlas emulates the functions and operations of the RH11 Massbus controller and RM02 disc drives. The single quad-size board controller is software transparent to RSX11-M and RSTS/E operating systems, without need for additional drivers. Features include 3-sector buffering, automatic multifunction self-test on power turn-on with LED display, and separate register files for each disc, which allows overlapped seek emulation. Prices start at $4500 in single-unit quantities. **Rianda Electronics,** 2535 Via Palma, Anaheim, CA 92801.



Circle 383 on Inquiry Card

PARAMETER LOADING MADE EASY...

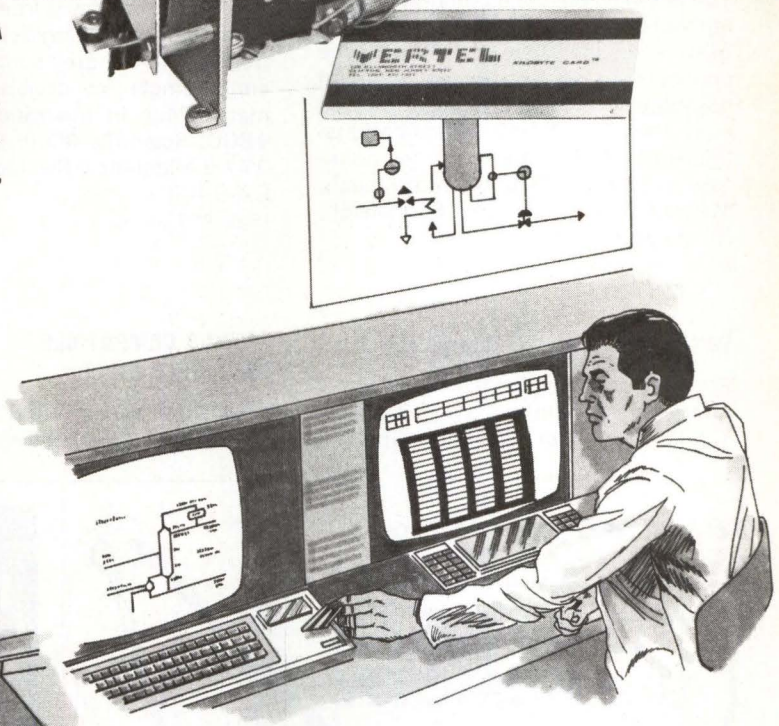
Set it up once... and forget it, with the...

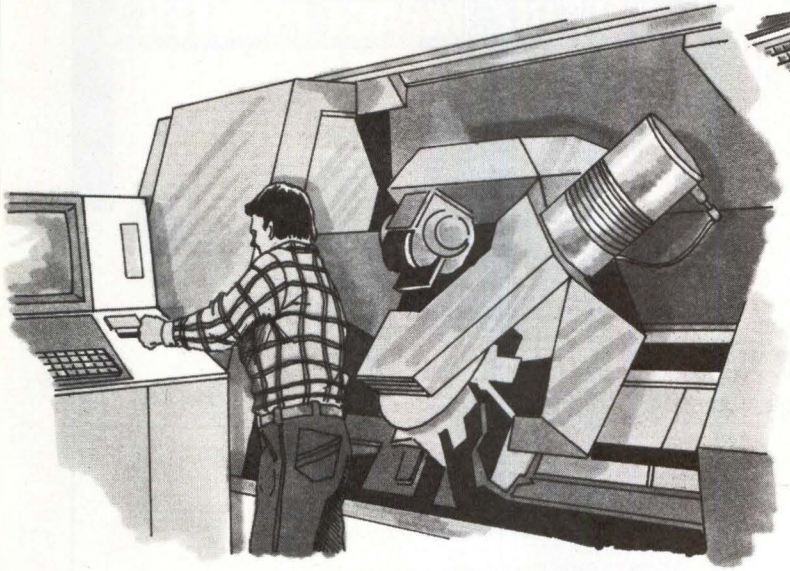


KILOBYTE CARD™ READER/WRITER

for process/machine control applications.

With the Vertel KB-31 System, there is no longer any need to manually enter the same program more than once. Simply enter the program into the system, as you normally would, then let the system record the program on our KILOBYTE CARD with our KB-31 Microloader; when you are ready to re-use that program simply insert the KILOBYTE CARD into the KB-31 and your program will be loaded automatically into your system.





Designed for microprocessor based systems, this rugged, low cost*, field-proven performer is ideally suited for everything from intelligent terminals and instrumentation to machine tool controls and test equipment.

The 4-stripe magnetic KILOBYTE CARD can record up to 1,088 eight-bit bytes and with the microloader, it is the ideal peripheral for parameter loading, field program modifications, and user activated diagnostics.

*As little as $199 in OEM quantities.

To learn how the KILOBYTE system can benefit your operations, call or write today for details on our free, thirty-day trial offer.

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CIRCLE 152 ON INQUIRY CARD

INTERFACE

STD BUS INDUSTRIAL I/O

Parallel industrial module 7911/PIM interfaces STD BUS microprocessor systems and is plug compatible with industry std I/O racks. Any channel may be configured as input or output to match type of installed I/O module. Software enables any input to generate an interrupt signal to the CPU. The module appears as four read/write registers within the STD I/O map. A 50-pin header located at card edge connects to the I/O rack. The card operates on a single 5-Vdc supply and conforms to all STD BUS specifications. Prices range from $160 (single quantity) to $120 (100 quantity) each. **Matrix Corp,** 1639 Green St, Raleigh, NC 27603.

Circle 384 on Inquiry Card

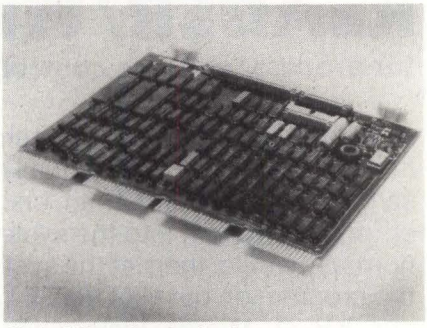
WINCHESTER/FLOPPY CONTROLLER

FWD5001 provides a general purpose interface compatible with Shugart 1403D controller, and replaces it without changing mounting provisions, connectors, cables, or power supplies. Using 40% fewer ICs, it exhibits increased reliability and requires only 5-V power. Direct data transfer mode may be selected via command to allow high performance DMA operation with host microprocessors. Need for interleave formats on Winchester disc is eliminated with direct transfer, since the controller's internal data buffer is bypassed. Single- and dual-head floppy drives are supported using either single- or double-density formats. Price in quantities of 100 is $800. **Scientific Micro Systems, Inc,** 777 E Middlefield Rd, Mountain View, CA 94043.

Circle 385 on Inquiry Card

SMD I/O COMPATIBLE DISC CONTROLLER

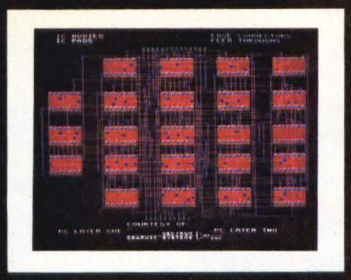
Interfacing one or two 8" or 14" (20- or 36-cm) Winchester/SMD/CMD cartridge drives with 8M- to 300M-byte storage to LSI-11 computers, model 202A uses a universal firmware set that retains no drive parameters in on-board components. This allows drives to be mixed or matched without controller or component changes. The unit plugs into one slot of LSI-11 based quad backplane and is compatible with DEC RP02/RP03 software drivers in RT-11 and RSX-11 operating systems. Price is $2775/unit. **Distributed Logic Corp,** 12800 Garden Grove Blvd, Garden Grove, CA 92643.

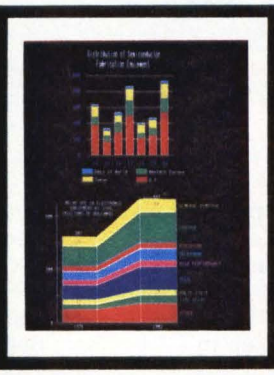


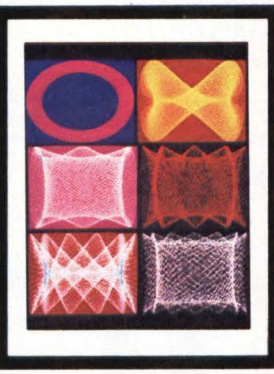
Circle 386 on Inquiry Card

CIRCLE 153 ON INQUIRY CARD

CIRCLE 154 ON INQUIRY CARD







Microfiche

Overhead Projection Transparency

Slide

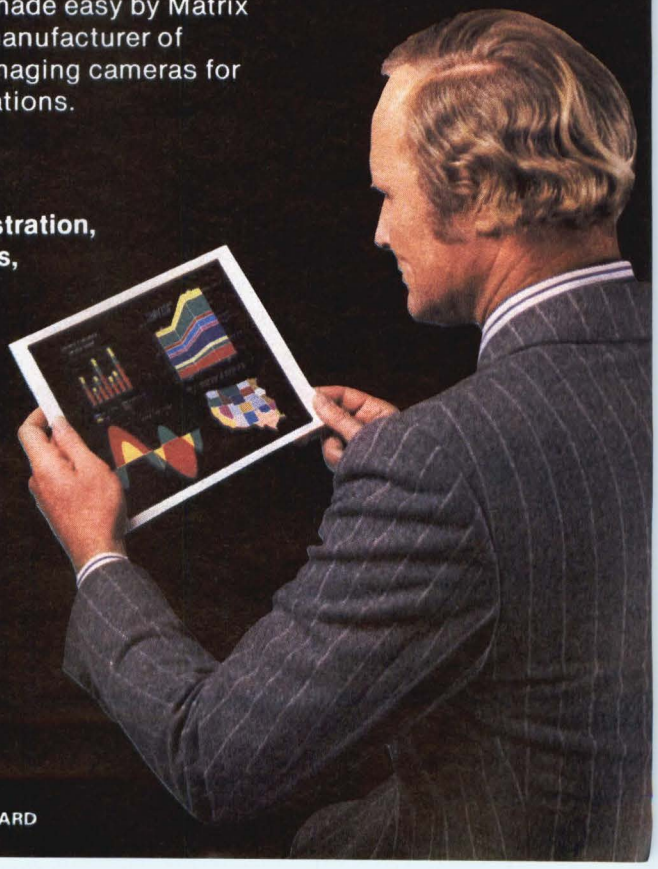
Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable. . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

For more information, film samples, or a demonstration, contact Matrix Instruments, 230 Pegasus Avenue, Northvale, New Jersey 07647. Telephone (201) 767-1750 Or call toll-free: (800) 526-0274.



 # MATRIX INSTRUMENTS

Hard copy shown reduced from original 8" x 10", slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

CIRCLE 155 ON INQUIRY CARD

INTERFACE

LOW COST ENCODER

RS-23L provides long life, solid output signals, stable and reliable performance, high noise immunity, and jitter-free operation. It features 150k-hour single LED light source design, single monolithic array of differentially connected photosensors, IC amplifiers, metal housing, and hysteresis feedback. Non-critical voltage requirement of ±10% (conservative operational range, not dropout value), combined with modest current drain, permits use of less expensive power supply. Prices start under $100. **Data Technology, Inc,** 4 Gill St, Woburn, MA 01801. Circle 387 on Inquiry Card

PERIPHERALS

300-LINE/MIN BAND PRINTER

For medium to high volume print requirements in an interactive network, the 9289 achieves 300 lines/min with a 64-char set, and 240 lines/min with a 96-char set. Horizontal and vertical margins, case selection, lines/inch, and space density can be modified or adjusted with switches on the front control panel. Printer, with 64- or 96-char band, can be purchased for $10,403. **Harris Corp,** 16001 Dallas Pkwy, PO Box 400010, Dallas, TX 75240.

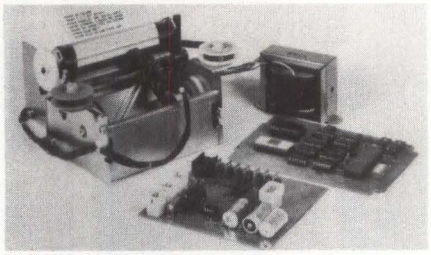
Circle 388 on Inquiry Card

LOW COST CUSTOMIZABLE INTELLIGENT TERMINAL

Terminal ZMS-35, based on Intel 8085, features 16k-byte user RAM, fully configurable keyboard, and 12" (30-cm) nonglare CRT, with 128-char set. The terminal can perform such special functions as split screen format with independent scrolling of data. Interfaces are RS-232-C for up to 9600-baud operation, and 20 mA current loop at speeds to 19.2k baud. Options include printer interface, downline loader, and debugger for user software development. Single-quantity price is $1350. **Zentec Corp,** 2400 Walsh Ave, Santa Clara, CA 95050.

Circle 389 on Inquiry Card

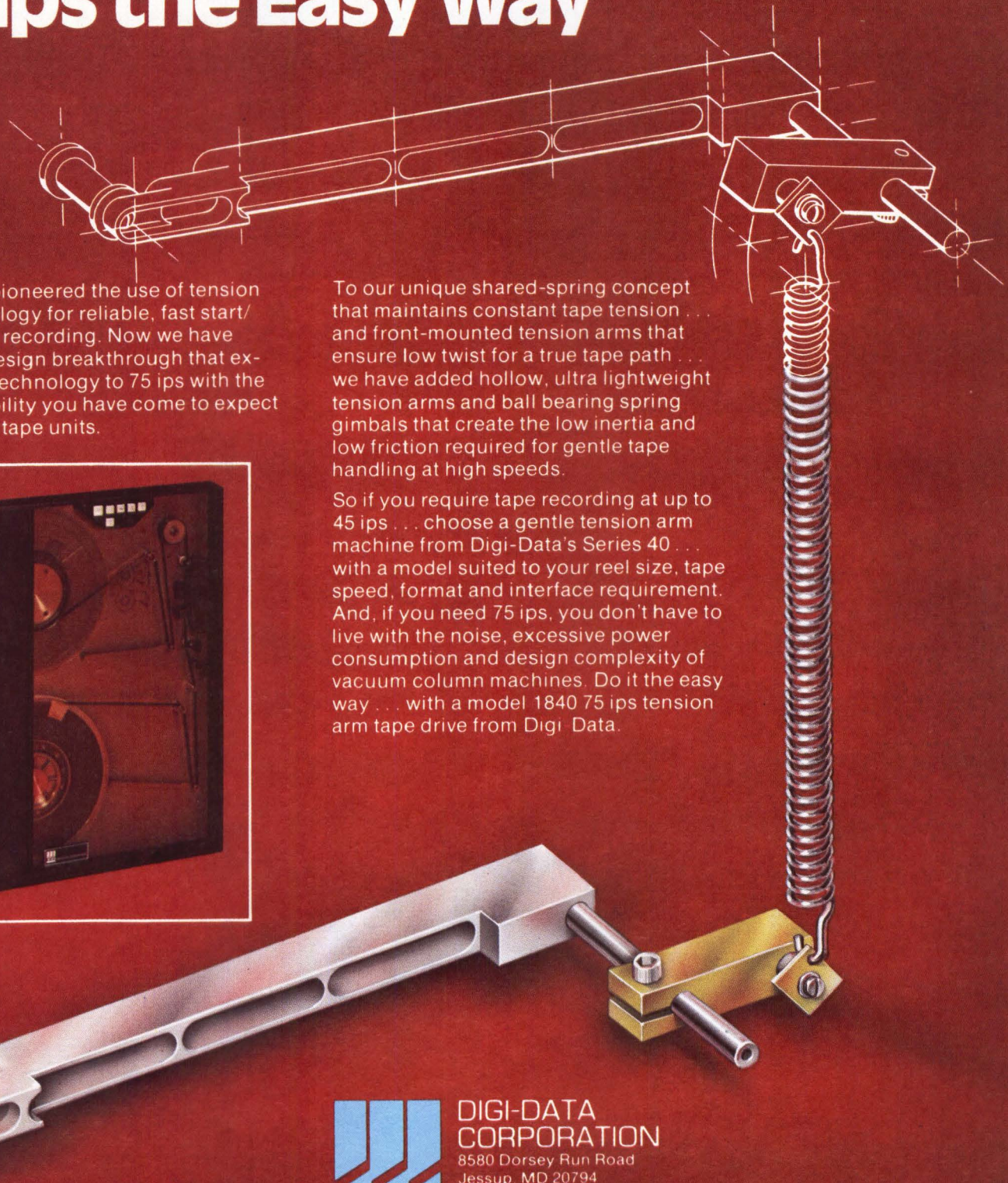
40-COL DOT MATRIX IMPACT PRINTER



SP-300 provides 5 x 7-dot matrix printing of std 64-char ASCII subset at 50 chars/s. Parallel and serial ASCII inputs are std; parallel input data rates can be up to 1k baud, while serial input rates can be up to 12.5k baud. Serial input is switch-programmable for word length, parity, and number of stop bits, and serial input error lines are provided. Selectable internal/external bit rate clock and 40-char buffer are also std. RS-232-C or current loop options are available. Total system, priced at $289 in 100-piece quantities, includes printer mechanism, all electronics, and 115-Vac power supply. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.

Circle 390 on Inquiry Card

Digi-Data's Tension Arm Design Breakthrough Brings You 75 ips the Easy Way



Digi-Data pioneered the use of tension arm technology for reliable, fast start/stop digital recording. Now we have achieved design breakthrough that extends that technology to 75 ips with the same reliability you have come to expect from 45 ips tape units.

To our unique shared-spring concept that maintains constant tape tension . . . and front-mounted tension arms that ensure low twist for a true tape path . . . we have added hollow, ultra lightweight tension arms and ball bearing spring gimbals that create the low inertia and low friction required for gentle tape handling at high speeds.

So if you require tape recording at up to 45 ips . . . choose a gentle tension arm machine from Digi-Data's Series 40 . . . with a model suited to your reel size, tape speed, format and interface requirement. And, if you need 75 ips, you don't have to live with the noise, excessive power consumption and design complexity of vacuum column machines. Do it the easy way . . . with a model 1840 75 ips tension arm tape drive from Digi-Data.

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Jessup, MD 20794
(301) 498-0200
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CIRCLE 158 ON INQUIRY CARD

Quality and delivery are two good reasons to choose Panasonic CRT data displays...

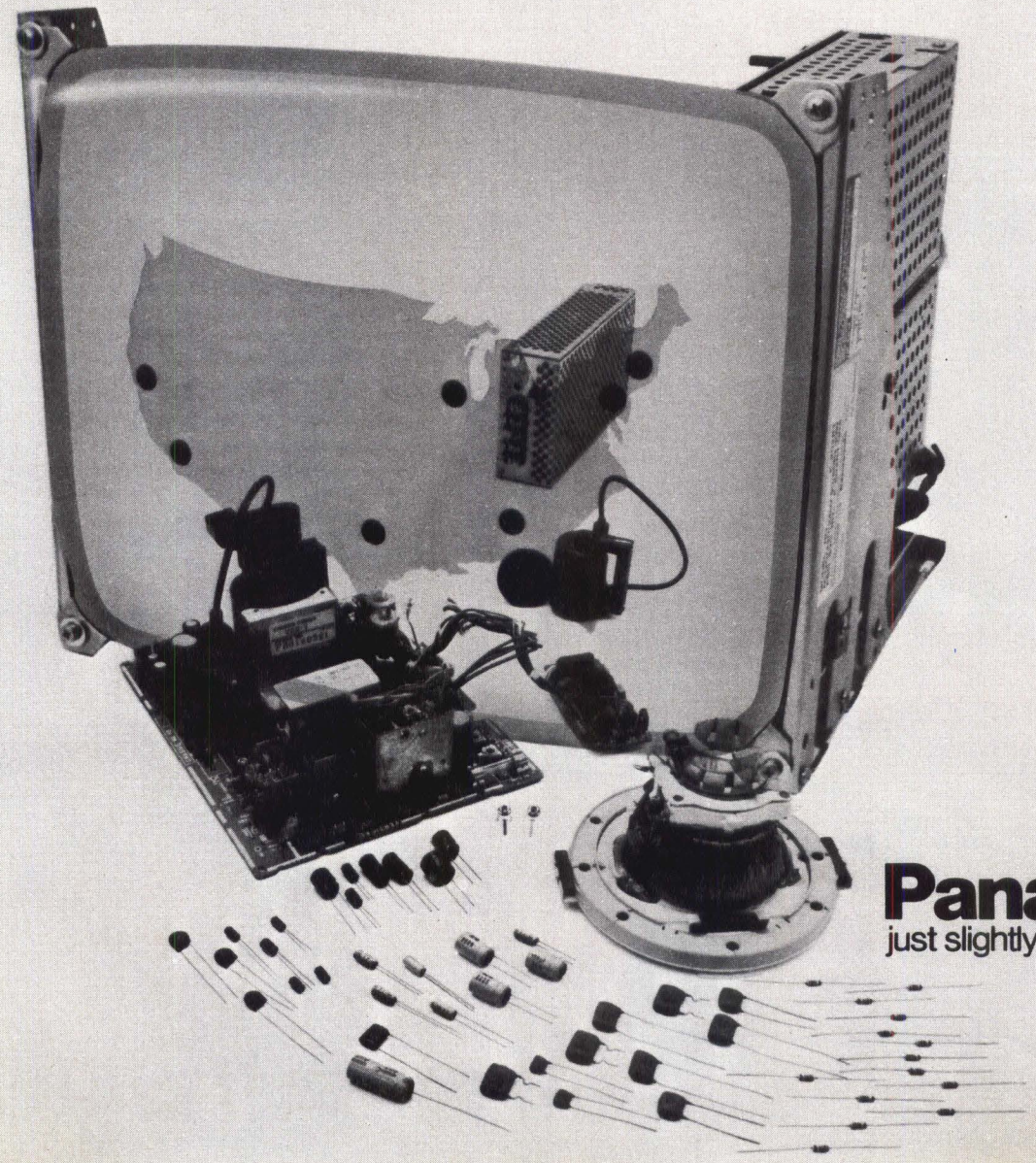
The point is, there are a lot of good reasons to choose Panasonic CRT data display modules. Like a full line of models to choose from. Quality that's built in. Delivery when promised. And a super service program that will put you in "seventh heaven".

Seven factory servicenters in the U.S. are ready to serve you – either at our facilities or on your site. Component parts for our complete line are available from our Secaucus, N.J. parts depot. And our U.S. Applications and Design Lab is fully equipped to help you with applications, design, testing, troubleshooting and problem solving.

The complete Panasonic line of CRT Data Displays includes high resolution color modules for fine line graphics. A 600-line vertical page reader. And a wide variety of other top-quality color and monochrome CRT chassis assemblies, to give you far-ranging design flexibility.

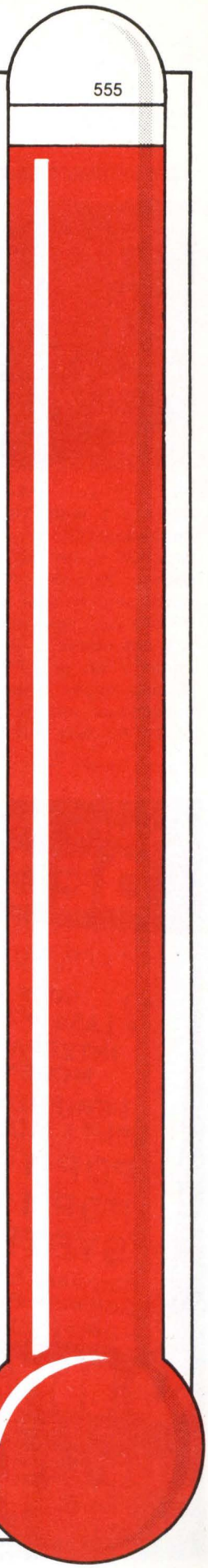
Need any more reasons to choose Panasonic? Then call one of our Application Engineers – he's got plenty more to convince you. Or write for additional data: Panasonic Company, Data Display Dept., Industrial Sales Division, One Panasonic Way, Secaucus, NJ 07094; phone (201) 348-5385.

7 servicenters make 7 more.



Panasonic®
just slightly ahead of our time

CIRCLE 170 ON INQUIRY CARD



COMDEX roster now at ~~529!~~ 540!

Will COMDEX break NCC's record? NCC '81 had 555 exhibitors.

You remember NCC '81 at McCormick Place in Chicago. Those huge, multiple exhibit floors presented hands-on displays from 555 computer-related companies. That was an all-time record for computer industry trade shows.

Now COMDEX, in only its third year, is threatening to eclipse that NCC record. More than 520 computer-related companies have already signed to exhibit in over 1,600 booths at Las Vegas Convention Center, November 19-22. And there's still a few weeks left for additional companies to get on board!

Size Without Sightseers

But if COMDEX and NCC are now roughly comparable in the number of exhibitors each can boast, **there remains one very significant difference:** COMDEX will not have tens of thousands of attendees who are students, or businessmen on their lunch hours, or computer hobbyists. **The COMDEX audience is limited to qualified ISOs (Independent Sales Organizations)!**

COMDEX '81 -- A very big show indeed, possibly even a record breaker for the computer industry. But the atmosphere WON'T be "zooey." Rather, it will be conducive to the serious negotiations so necessary to move an avalanche of computer related products.

There's still time to be an exhibitor. And there's plenty of time to pre-register as an attendee. Call us today!

COMDEX'81™

November 19-22, 1981
Las Vegas Convention Center

For further information, write to COMDEX '81,
160 Speen Street, Framingham, MA 01701.
Or call us toll-free: 800-225-4620 (in Mass., 617-879-4502).

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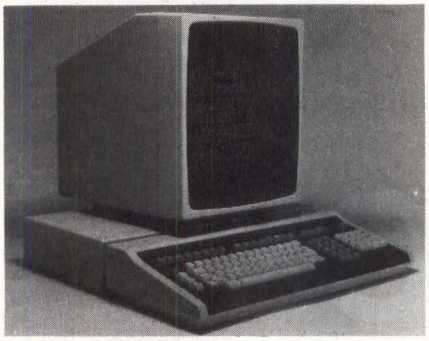
THE COMPUTER SHOWCASE EXPOSITIONS

CIRCLE 159 ON INQUIRY CARD

PERIPHERALS

USER DEFINABLE SMART TERMINAL



PM 2010 combines ANSI standard X3.64-1979 with 16-bit 8086 microcomputer, 32k-byte RAM expandable to 256k bytes, 66 x 80-char video display, 8k-byte EPROM, two RS-232-C ports, and parallel printer port. Terminal's full-page video display uses 7 x 9-dot matrix in 9 x 15 field. Any combination of 128 characters, including upper- and lowercase with descenders, can be displayed in high or low intensity with blinking, reverse, blank, and underline capability. Detachable keyboard has full alphanumeric set with N-key rollover, eight function keys, numeric keypad, and dedicated keys. OEM quantity 500 price is $2500. **Piiceon, Inc,** 2350 Bering Dr, San Jose, CA 95131.

Circle 391 on Inquiry Card

FULL-COLOR GRAPHICS IMAGING SYSTEM

AED512R adds graphics and imaging capabilities to local or remote computers. Composed of keyboard, color monitor, and rackmounted controller, unit can communicate serially via RS-232-C interface or 20-mA current loop, or function as computer peripheral under DMA control. Superoam feature, with up to 8 memory planes, allows users to pan a stored drawing, and enables memory to be configured as 512 x 512 x 8, 1024 x 512 x 4, 1024 x 1024 x 2, or other combinations. Unit also features 256 user definable symbols, 1M-byte/s data transfer rate, 3-D shading, and color blinking. **Advanced Electronics Design, Inc,** 440 Potrero Ave, Sunnyvale, CA 94086.

Circle 392 on Inquiry Card

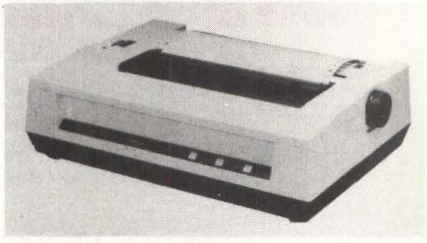
HIGH RESOLUTION COLOR RASTER DISPLAY SYSTEM

System 3400 XV7 with extended viewing option displays 704 lines of 880 pixels at 60-Hz noninterlaced refresh. Image memory is 1280 pixels x 1024 lines/plane, with 3 planes std (8 colors). Features include programmable hardware cursor, pan/zoom, serial interface, 8 x 24 color lookup table, 96 upper/lowercase characters (7 x 9-pixel format), multiple character sizes, polygon fill, weighted lines, patterned lines, chained vectors, arc generation, and logical write modes. Additional memory and overlay planes, blink, and interactive devices are optional. **Lexidata Corp,** 755 Middlesex Tpk, Billerica, MA 01865.

Circle 393 on Inquiry Card

DOT MATRIX PRINTER

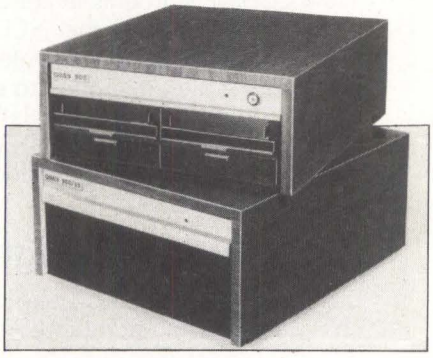
Pro-Writer has printing capability up to 136 columns, implements 5 alphabets, and offers 8 char sizes, including 2 that are proportionally spaced. Graphics capability is built-in with character generated shape and high resolution positioning—144 x 144 positions in a 1" (2.54-cm) square. Unit offers switch-selectable single- and bidirectional printing, and can handle forms up to 10" (25 cm) wide. Print speed is 100 chars/s with throughput from 44 to 152 lines/min. Friction feed, built-in bidirectional tractor feed, and roll feed combined with paper cutoff of less than 1" (2.5 cm), are standard. Industry std parallel or RS-232-C interface is provided. OEM quantity price is $399. **C. Itoh Electronics, Inc,** 5301 Beethoven St, Los Angeles, CA 90066.



Circle 394 on Inquiry Card

MICROPROCESSORS/ COMPUTERS

WINCHESTER BASED MICROCOMPUTER

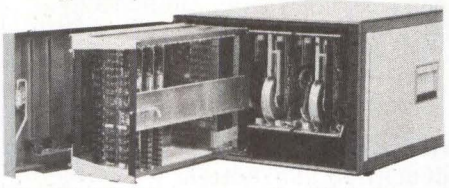


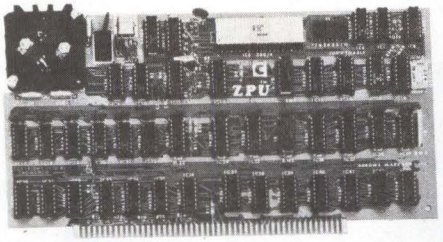
Series 900, available with 33M (model 900/33) or 66M bytes (900/66), is based on 14" (36-cm) Winchester drives that use advanced positioning and recording techniques to achieve high data capacity, fast access time, and reliability. Features include linear coil positioning to provide fast track access and reliable head positioning, and brushing landing zones to protect data integrity. The Z80 based system supports from 1 to 4 users with 48k bytes of RAM each. It also incorporates dual double-density/double-sided 8" (20-cm) floppy drives, DMA controlled disc access, and 6 serial and 2 parallel ports. Base price is under $13,000. **Quay Corp,** PO Box 386, Freehold, NJ 07728.

Circle 395 on Inquiry Card

What You Did and Didn't Know About Cromemco... Until Now.

What You Knew:
You knew Cromemco is one of the largest and most successful microcomputer manufacturers in the industry. You knew that Cromemco has a full line of S-100 bus products ranging from single card computers, 7 channel A/D, D/A board, PROM cards, RAM boards, serial, and parallel I/O to complete 22 megabyte hard disk systems. You knew that Cromemco offers you software flexibility; operating systems such as CDOS and CROMIX (UNIX™ like). Languages too: C, COBOL, FORTRAN IV, BASIC, RPG-II, LISP, assemblers, structured BASIC and more. You know that Cromemco means quality, reliability and a high price/performance ratio. Cromemco can make designing your products simpler. And isn't that what you want to know?





What You Didn't Know:
You didn't know that Consumer Computer Marketing, Inc. (CCM) is the Authorized Cromemco Distributor in the eastern United States. CCM is a full line microcomputer distributor with off the shelf deliveries for most products. Did you know that CCM offers credit terms and very attractive discounts? As well as Cromemco, did you know that CCM distributes some of the most widely recognized and highest quality names in the industry? You didn't know that, did you? Until now.

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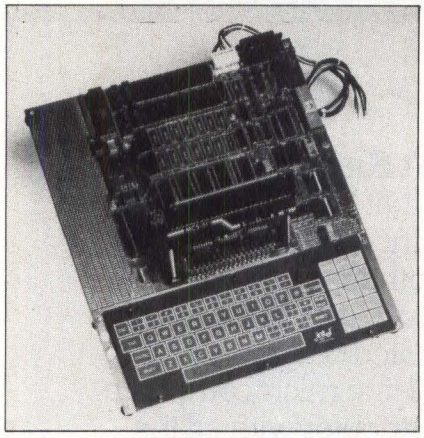
CIRCLE 161 ON INQUIRY CARD

MICROPROCESSORS/ COMPUTERS

MICROCOMPUTER SYSTEM DESIGN KIT



SDK-51 contains all hardware and software required to assemble an evaluation and prototyping tool for MCS-51 microcontrollers. Monitor package, single-line assembler/disassembler, full ASCII keyboard, and LED display are included. Kit also provides 1k byte of RAM and 8155 parallel I/O device that expands I/O capability by providing 22 dedicated parallel and TTL compatible lines. Unit interfaces to RS-232 compatible CRT, printing terminal, or current loop terminal through serial interface connectors on the board. Price is $950. **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, OR 97132.

Circle 396 on Inquiry Card

INTERACTIVE ACQUISITION CONTROLLER

MCS-16, a single-board microcomputer for monitoring and control applications, features 15 channels of analog input plus additional analog connector for external multiplexing, 16 channels of digital control output, 16 channels of digital status input, and RS-232 interface for host computer. Also included are 7-day realtime clock/calendar, ac carrier remote communications interface, high level control language interpreter, continuous system fault detector, and battery backup. Keyboard/display interface is provided for standalone operation, and EPROM socket is optional. **i/e Associates, Inc,** 3702 E Lake St, Suite 202, Minneapolis, MN 55406.

Circle 397 on Inquiry Card

MULTITASKING DESKTOP MICROCOMPUTER

Affinity 16, first in the TFC 3450 family of information systems, is priced at less than $10,000. Computer will operate as a standalone unit, online to a central computer, or in network environment, and can perform batch, online, or distributed processing. A 16-bit microprocessor and 128k bytes of memory are included in the CPU. Two minifloppy disc drives can each record 320k bytes on two dual-sided, double-density discs. CRT display features 12" (30-cm), 1920-char screen; 192 display patterns; and versatile display functions. An interactive screen format generator allows users to create, load, edit, display, and catalog screen layouts, eliminating the need to encode input/ output formats in BASIC programs. System is supplied with both business and scientific BASIC. **TRW-Fujitsu Co,** 9841 Airport Blvd, Suite 620, Los Angeles, CA 90045.

Circle 398 on Inquiry Card

Speeding μP designs into production. Saving time. And money. AMPL Development Systems from TI.

AMPL* hard disk and floppy systems to maximize software productivity.

You've read about it in the electronics press. TMS9995 — TI's enhanced performance member of the 16-bit 9900 Family, and TI's third generation 16-bit Family, and TMS7000—a new 8-bit microcomputer Series.

But there's more to our microprocessor story. There are the innovative hardware and software tools that support the design of these products and fulfill the promise of the future now with packaged AMPL systems.

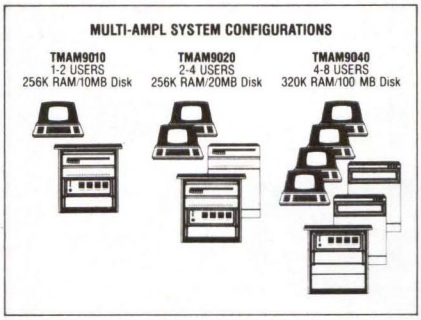
Teamwork—yours and ours

Multi-AMPL*—a complete set of hardware and software development tools to help you get your designs into production faster at lower cost. A wide selection of systems featuring: Microprocessor Pascal high-level language; Component Software with Rx Real-time Executive; AMPL Debug HLL full-speed emulators; Logic state trace analyzer for up to four simultaneous AMPL Stations*; Debugging for hardware and software through emulation.

As many as eight program designers can work concurrently using hard-disk minicomputer throughput — maintaining a single data base, sharing CPU, memory and peripherals, Multi-AMPL cuts development time while achieving the lowest cost per user.

Support, support, support

Expert assistance for installation and system generation. A network of engineers manning special "hotlines" at TI's Regional Technology Centers to provide immediate design and applications remedies or schedule service calls.



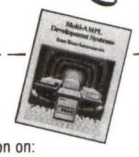
In addition to the configurations shown above, be sure and ask about TMAM9000, our new single-user floppy disk system with 64 KB RAM and more than 2 MB storage capacity.

Good today. Good tomorrow.

TI AMPL systems support all of TI's leadership microprocessor and microcomputer module families. This compatibility means your investment in the system today will be valid tomorrow. That the code you write today will be valid tomorrow. And the latest developments in microprocessor technology will continue to be supported by a total capability development system.

For ordering information, contact your local TI field sales office or authorized Distributor System Center, or call TI at (713) 778-6549.

For details, send us the coupon and we'll send you a copy of our new brochure. Free.



Texas Instruments Incorporated
Microcomputer Marketing, M/S 6404
P.O. Box 1443, Houston, Texas 77001

Please send me your free Multi-AMPL brochure, CL-599, and more information on:

Hard disk systems:
- ☐ TMAM9010
- ☐ TMAM9020
- ☐ TMAM9040

New, single-user floppy disk system:
- ☐ TMAM9000
- ☐ Have a representative call

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ACD-1

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

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CIRCLE 163 ON INQUIRY CARD

MICROPROCESSORS/ COMPUTERS

DISC ORIENTED PERSONAL MICROCOMPUTERS

Based on the Z80, PMC-81 has 16k RAM, 14k ROM, a keyboard cassette interface, and a video monitor interface. EXP-100 expander permits addition of interfaces for minifloppy discs, printer, RS-232-C, and S-100 bus. System has 15-key numeric pad and 4 function keys on professional keyboard with lowercase letters and true descenders. Features include automatic repeat on every key, print screen from keyboard command, and shift lock command to switch keyboard from BASIC to typewriter mode. Unit sells for $740; with VDM-81 green monitor screen, for $939. **Personal Micro Computers, Inc,** 475 Ellis St, Mountain View, CA 94043.

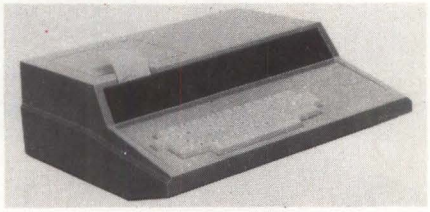
Circle 399 on Inquiry Card

8-BIT MOS/LSI MICROCOMPUTER

Fabricated with n-channel silicon gate technology, 8-bit PIC1670 microcomputer contains RAM, I/O, CPU, and customer defined ROM on a single chip. Firmware architecture is based on register file concept. Simple instruction commands optimize code for bit, byte, and register transfers, and also support computing functions. Instruction execution time is 1 μs. Single 4.5- to 5.5-V power supply is required. Device has interrupt structure and on-chip oscillator to provide operating clock, with only an external crystal or RC network to establish frequency. Cost is less than $5.00 each in 50k quantities. **General Instrument Corp, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.

Circle 400 on Inquiry Card

PORTABLE INDUSTRIAL CONTROL SYSTEM

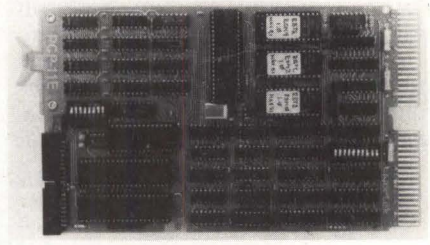


AME 1000 is composed of AME 400 enclosure, DMB 200 motherboard, and DPS 512 power supply. In a single enclosure, it allows up to 4 EXORciser- and up to 6 Eurocard-type boards to be added to a Rockwell AIM 65 microcomputer. Available modules include analog boards, D-A and A-D converters, CRT controllers, solid state relays, floppy disc controllers, RS-232-C and IEEE 488 I/O, modems, and memory. Connectors support single-sided, double-density floppy discs, Centronics compatible printer, and Braemer cassettes. System price is $625. **Dynatem Inc,** 20881 Paseo Olma, El Toro, CA 92630.

Circle 401 on Inquiry Card

LSI-11 COMPATIBLE SLAVE COMPUTER

Mid-range PCP-11E augments capabilities of LSI-11 based host systems, implementing complex serial communications protocols. Dual-width card includes 4-MHz Z80 microcomputer, 16k-byte RAM, provision for up to 24k bytes of EPROM, RS-232 serial channel, 8-bit parallel port, 4 counter/timers, and 16-bit programmed I/O interface to host Q-bus processor, with interrupt driven handshaking. System is supplied with EPROM resident operating system and Spice programming language. Unit price for quantities of 100 is $665. **Nortek Inc,** 2432 NW Johnson St, Portland, OR 97210.



Circle 402 on Inquiry Card

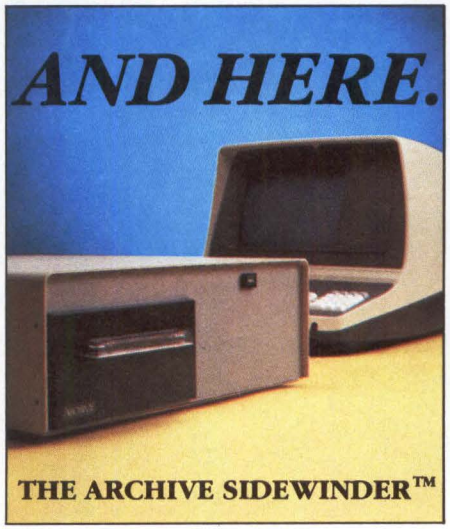
The streaming ¼-inch cartridge tape drive for your Winchester backup

YES, IT'S REALLY HERE...

The technology is really here. At Archive Corporation. Archive developed it from the ground up. Engineered and produced the product. Result: the Sidewinder, a streaming ¼-inch cartridge tape drive backup for your Winchester disk-based computer.

The Sidewinder delivers more formatted capacity—up to 20 megabytes per tape. Gives you faster transfer rates—up to 90 kilobytes per second. That's faster than any other peripheral sub-system.

Archive's intelligent Sidewinder, with its microcomputer-based controller, offers full systems flexibility in the same package size as an 8-inch floppy disk. Integrate it into your system. It's easy.



THE ARCHIVE SIDEWINDER™

The Sidewinder is packed with great features. There's file mark detection and generation, read after write, error detection and correction—all without host intervention. And the price is right.

Archive is turning out an army of Sidewinders every day—on an automated production line.

The industry is buying them. Using them. Loving them.

Talk to Archive. Evaluate the Sidewinder. See for yourself that what you need is really here.

ARCHIVE
CORPORATION

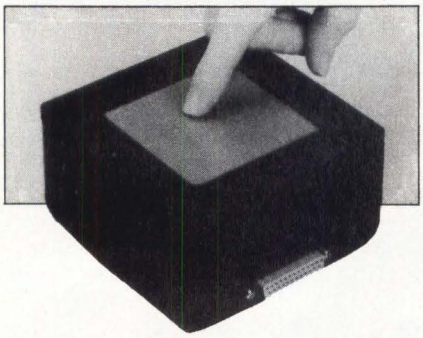
3540 Cadillac Avenue
Costa Mesa, CA 92626
(714) 641-0279
Telex 683466, TWX 910-595-2458

Making Things Happen in Tape Technology

CIRCLE 165 ON INQUIRY CARD

SYSTEM ELEMENTS

FINGER-OPERATED X-Y POSITIONER



An alternative to trackballs, joysticks, and lightpens, Trazor™ touch panel allows rapid and precise 2-axis positioning by combination of motions—sliding the finger for rough positioning and rolling the ball of the finger for precise positioning. A single pixel can be selected from a 1024 x 1024 display. Circuitry in the unit senses the finger's location in X and Y axes and produces a digital output of the position that can be directly interfaced with any computer having an RS-232-C serial port. Switch-selectable baud rates are 300, 1200, 2400, 4800, 9600, and 28,800. Entire unit measures 4.75" x 4.75" x 2.5" (12.1 x 12.1 x 6.4 cm) and contains no moving parts. **Spiral System Instruments, Inc,** 4853 Cordell Ave, Suite A-10, Bethesda, MD 20014.

Circle 403 on Inquiry Card

LIGHTPEN AND PRINTER INTERFACE FOR ENHANCED VT100 TERMINALS

Lightpen and printer interface options allow users who have upgraded their DEC VT100 terminals with Retro-Graphics package to add I/O versatility. An efficient "pointing" device for interactive graphics applications, the lightpen permits users to emulate Tektronix 4010 graphic input mode and allows the user to point at a CRT raster screen and transmit X-Y coordinates directly into computer memory. The printer interface supports a number of graphics and non-graphics printers. In Alpha mode, the interface is transparent to transmission from the terminal to the printer. If the printer being used has graphics capability, the interface allows the graphics portion of the terminal display to be dumped directly into the printer. Lightpen model VT20-LPN is priced at $360. **Digital Engineering, Inc,** 630 Bercut Dr, Sacramento, CA 95814.

Circle 404 on Inquiry Card

Capacity without Compromise

12.72 megabytes in a four-platter 5¼-inch drive.

Get big capacity without risk. The RMS-512 gives you more bytes per drive and per dollar than any other 5¼-inch drive, using field proven conventional Winchester technology. All in a minifloppy-sized package.

Better reliability. Our electrical-mechanical brake secures spindle in power-down mode to prevent media and head damage when the system is moved or shipped. No screws or locks to remember.

Worried about data separation hangups? Our **Data Express**™ data separator handles high data transfer rates, even when used with a standard SA1000 floppy-type interface.

Concerned about head landings? We give you a landing shipping zone outside the data area.

Looking for ways to reduce heat and power? We beat the heat with less than 20 watts. In standby "power save" mode, power consumption drops to 14 watts.

Do you want extra quality assurance? RMS burns in every complete disk drive system to specification limits.

Better performance. Our electronically dampened actuator provides for servo-like positioning and more stable settling. Buffered mode improves seeking speed. Integral microprocessor simplifies diagnostics and control.

And all at a better price. RMS gives you proven Winchester technology at the lowest entry cost per drive or per byte. Three models offer a range of capacities (3.18, 6.38 and 12.72 megabytes). For specifications and price information, circle our readers' service number. For an evaluation unit, call Mike Kirby at **408-730-1346.**

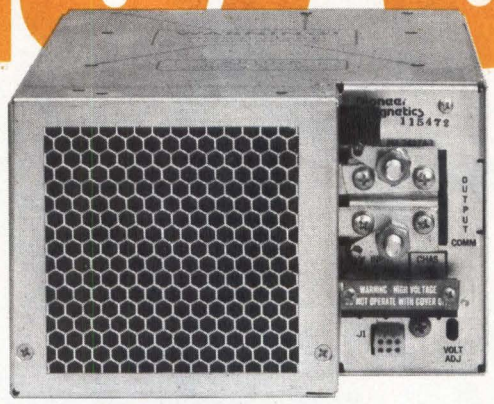
Rotating Memory Systems, Inc.
1031-A E. Duane Avenue
Sunnyvale, California 94086
(408) 730-1346

RMS

CIRCLE 166 ON INQUIRY CARD

Dependable Switchers...

1973 1981



The PM2497

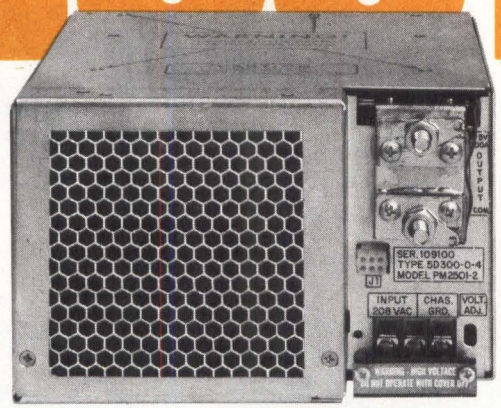
5V@100A/5"x8"x11"

In 1973 Pioneer Magnetics started building a 5VDC @ 100A switching power supply for applications requiring compact and efficient DC power. At the time, commercial switchers were considered state-of-the-art. We solved reliability and delivery problems for our customers that our contemporaries couldn't. As a result, our customers referred to the power supplies as the DEPENDABLES. In fact we're still delivering that same power supply to those same valued customers. We're proud to say that they've depended on us and we've responded by shipping over 100,000 high power switchers. After 8 years our supplies are still out there and running. A continuation of a tradition started in 1958.

STANDARD DC OUTPUT RATINGS.

MODEL	2V	3V	5V	12V	15V	18V	24V	28V	48V	60V	CASE SIZE
PM2496A	100A	60A	50A	30A	25A	22A	16A	13A	8A	6A	5"X8"X11"
PM2497A	200A	100A	100A 120A 150A	60A	50A	45A	33A	27A	16A	12A	5"X8"X11"
PM2500A		200A	200A	85A	70A	60A	45A	40A	24A	19A	5"X8"X11"
PM2498B	400A	300A	200A 300A	120A	100A	90A	66A	54A	32A	25A	5"X16"X11"
PM2501	400A	300A	300A	120A	100A	90A	66A	54A	32A	25A	5"X8"X11"
PM2502	500A	450A	450A	180A	150A	125A	90A	80A	47A	35A	5"X16"X11"

NOTES: 92-138VAC or 184-250VAC single phase, 47 to 63Hz.
DC input available.



The New PM2501

5V@300A/5"x8"x11"

Since 1973, we've been accepting new challenges. Within the same outline as the PM2497, we've developed output ratings of 5V @ 120A, 150A, 200A and now a new 5V @ 300, with full delivered power at 50°C.

The new PM2501 exhibits excellent dynamic response. Proven design concepts enable close control over those parameters that insure reliability. For instance, our unique heat transfer technology results in low component thermal stress, even lower than the PM2497. At three times the power level the PM2501 features an exceptionally high power density package.

Our product line includes switchers that deliver up to 2250 watts in single output and from 375 to 1500 watts in dual through quad output channels. AC or DC input.

Over 100,000 PMI switchers are in the field providing dependable, service free operation. After all, that's why customers have continuously come back to us since 1958.

Pioneer Magnetics

THE SWITCHING POWER SUPPLY PEOPLE SINCE 1958

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VISUAL See for yourself

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Telephone (617) 851-5000, Telex 951-539

Dasher is a trademark of Data General

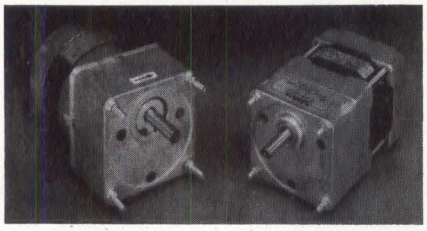
SYSTEM ELEMENTS

PERMANENT MAGNET SERVO MOTORS

Series 9030 permanent magnet field servo motors come in three lengths, from 1.78" to 2.40" (4.52 to 6.1 cm), exclusive of bearing bosses and shaft extensions. Units have 1.58" (4-cm) diameters. Variety of windings in 7-slot armature handle voltage inputs to approx 40 Vdc. Stall torques at nominal rated voltages range to 41 oz-in (0.28 N·m). Sleeve bushings or double-shielded ball bearings are available, as are metric mounting options. **The Pittman Corp,** Harleysville, PA 19438.

Circle 405 on Inquiry Card

INDUCTION GEAR MOTORS



PSC type motors have 60-, 70-, or 80-mm core diameters and are available in open-ventilated or closed construction. Standard features include die-cast aluminum on motor endbells and gear housing, ABEC 3 grease filled ball bearing on motor and output shaft of gearbox, steel gears, 16 gear ratios from 5:1 to 180:1, output ratio from 1 to 40 W (1/746 to 1/18 hp), and 115-V power. **Nidec America Corp,** 682 Transfer Rd, St Paul, MN 55114.

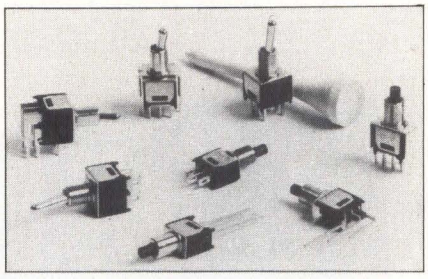
Circle 406 on Inquiry Card

MINIATURE ILLUMINATED ROCKER SWITCHES

Line of Cutler-Hammer® snap-in rocker switches is rated 6 A at 125 Vac, 3 A at 250 Vac, and 6 A at 28 Vdc. The switches come in either single- or double-pole configurations, measure less than 0.75" (19 mm) square, and require less than 0.875" (22 mm) of mounting space behind the panel. Rocker, paddle, and indicator caps are available in four colors with five incandescent lamp voltages. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216

Circle 407 on Inquiry Card

MINIATURE TOGGLE AND PUSHBUTTON SWITCHES



Added to the company's Tiny Switch line, model T211 double-pole, double-throw toggle switch can be panel or PC mounted. ON-ON-ON design allows break and/or make of one pole without disturbing the other. Contact ratings range from dry circuits to 2 A with resistive load at 120 Vac or 28 Vdc. Life is 30,000 cycles at full load, with max contact resistance of 10 mΩ. Also added to the line, TP12 pushbutton, in panel and PC mounting styles, has contact ratings to 1 A with resistive load at 120 Vac or 28 Vdc and contact resistance of 30 mΩ max. Life is 60,000 cycles at full load. Free engineering samples available upon request. **C & K Components, Inc,** 15 Riverdale Ave, Newton, MA 02158.

Circle 408 on Inquiry Card

LIGHTABLE KEYBOARD MODULES

Lightable from the backside, keyboard modules retain 0.687" (17-mm) button centers when placed side by side. PC mount design allows the 1-, 3-, and 6-button modules to be placed over a user supplied LED or incandescent lamp that can provide total illumination or be used as condition indicator. Circuitry choices include spst or dpst under each button. Contact system is a long wipe design, rated at logic loads for 1M operations/button and contact bounce of less than 10 ms. Modules are approx 0.750" (19 mm) high off the PC board. 100-piece lot price of 1-button module is $1.50. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.

Circle 409 on Inquiry Card

SERVO AMPLIFIER

A663 series PWM is designed to run any dc motor with maximum efficiency due to 1.01 form factor, and features ±120-Vdc peak voltage and ±60-A peak current; max peak current is for 1 s. Unit is protected against shorts across output before or after inductor, shorts to ground, loss of or low dc bus or bias power, overvoltage, excessive rms/peak current, system oscillation, and over temperature, and is oil and grease resistant. Op temp is 0 to 55 °C. **Westamp Inc,** 1542 15th St, Santa Monica, CA 90404.

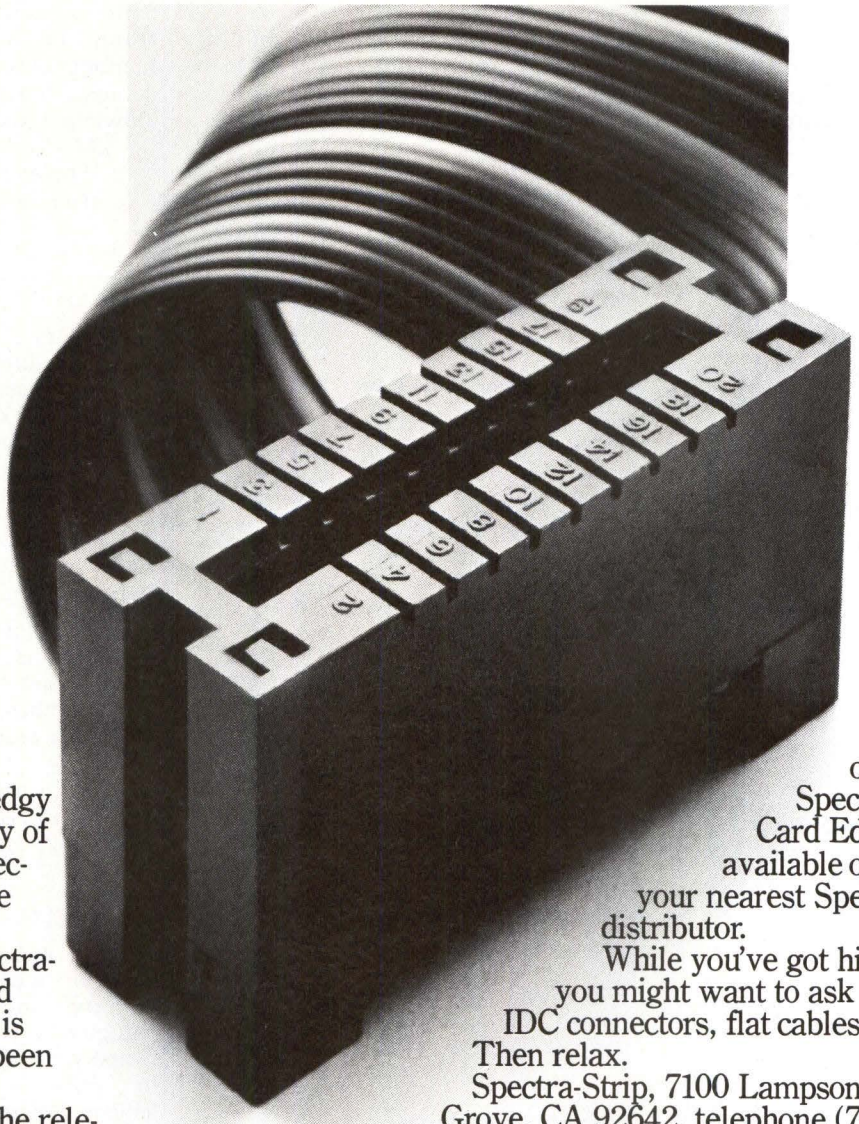
Circle 410 on Inquiry Card

DIGITAL TO SYNCHRO CONVERTERS

192E series 12- and 14-bit converters are designed primarily for driving size 8 and 11 torque receivers common to training and simulation equipment. 5-VA units feature self-contained output transformers; heat sinking; triple protection for output stage; overload and short circuit protection; and automatic thermal shutdown. Devices accept 180° input changes and offer accuracies to ±4 min. Models are available for operation at 0 to 70 or −55 to 85 °C. Prices start at $395. **Control Sciences, Inc,** 9601 Owensmouth Ave, Chatsworth, CA 91311.

Circle 411 on Inquiry Card

Advantedge



If you've been edgy about the quality of your PCB connectors, here's some good news:

The new Spectra-Strip™ IDC Card Edge connector is the one you've been waiting for.

Designed to the relevant portions of MIL-C-83503 and MIL-C-21097, the 807 Series is priced so that you can improve performance in even your most cost-sensitive systems.

With it, you can *reliably* terminate up to 60 wires at a time using our Twist 'N' Flat,® 3C® Color Coded and economical Spectra-Zip® cables. PCB contacts are bifurcated for reliability, you have a choice of three mounting configurations and covers are easily removable for daisy-chaining (cover removal tool optional).

And maybe best of all, the Spectra-Strip 807 Card Edge connector is available off-the-shelf from your nearest Spectra-Strip distributor.

While you've got him on the line, you might want to ask about our other IDC connectors, flat cables and assemblies.

Then relax.

Spectra-Strip, 7100 Lampson Ave., Garden Grove, CA 92642, telephone (714) 892-3361 and 720 Sherman Ave., Hamden, CT 06514, telephone (203) 281-3200.

In Europe, Spectra-Strip, Ltd., Romsey, Hampshire, England, telephone (0794) 517575.

For the name of our nearest distributor, call (800) 228-3900 now.

When you're down to the wire.

SPECTRA·STRIP

An ALLIED Company

CIRCLE 168 ON INQUIRY CARD

Switching, Linear, and Computer Power Supplies

Catalog lists features, specs, options, and ratings for single- to quad-output switchers, single- to triple-output linears, and CP series computer power supplies. **Deltron Inc,** North Wales, Pa.
Circle 445 on Inquiry Card

Interface Converters

IFA series is detailed in brochure featuring adapters that convert RS-232/V.24 interface to either CCITT recommended RS-449, X.20/.21, V.35, or Bell 303. **Atlantic Research Corp,** Alexandria, Va. Circle 446 on Inquiry Card

VLSI Signal Processing Components

Digital signal processing VLSI devices are described in 4-p, short form catalog that includes word size, multiply time, power dissipation, and package type. **TRW LSI Products,** La Jolla, Calif. Circle 447 on Inquiry Card

UPS Systems

Illustrated 24-p brochure presents line of UPS systems, details design and theory of operation, offers selection guidelines, and lists electrical/mechanical specs. **Sola Electric,** Elk Grove Village, Ill.
Circle 448 on Inquiry Card

Flexible Disc Unit

Total capability, operating simplicity, and programming flexibility of ENCORE 100 are discussed in bulletin and brochure that provide photos and specs. **Digitech Industries, Inc,** Ridgefield, Conn.
Circle 449 on Inquiry Card

Low Insertion Force Connectors

Listed in brochure are number of available contacts, rated current, and breakdown voltage for Hypertac® line, including modular, miniature, and subminiature units. **Hypertronics Corp,** Concord, Mass.
Circle 450 on Inquiry Card

Statistical Multiplexers

Brochure presents features, benefits, and applications of DCX 836, 840, and 850, along with photos, callout diagrams, and summary of technical information and specs. **Rixon Inc,** Silver Spring, MD. Circle 451 on Inquiry Card

Software Development System

Flowcharts and photos describe multitasking capability of 9520 system in 4-p brochure. **Millennium Systems,** Cupertino, Calif. Circle 452 on Inquiry Card

Custom Membrane Keyboards

TOUCH PANEL keyboards are discussed in 4-p brochure that includes exploded view of typical construction and description of operating characteristics. **Cherry Electrical Products Corp,** Waukegan, Ill. Circle 453 on Inquiry Card

Miniature Switches

Found on catalog sheets are photos, dimensional drawings, specs, operating characteristics, and applications for AH1, AH3, AH4, and AH7 series. **Aromat Corp,** Mountainside, NJ.
Circle 454 on Inquiry Card

FDM/PCM Converter

List of features, system description, block diagram, and technical summary are presented in brochure that discusses type 4691B converter. **GTE Lenkurt Inc,** San Carlos, Calif.
Circle 455 on Inquiry Card

Remote I/O Systems

Information on protocol, communications security, timing, time delay, latching, and counting are provided by SAMUX II catalog. **Opto 22,** Huntington Beach, Calif. Circle 456 on Inquiry Card

Pushbutton Switches

Range of panel mounted, snap-in, PC mounted, and PC right angle mounted pushbutton switches are described in 20-p catalog of specification details. **Dialight,** Brooklyn, NY.
Circle 457 on Inquiry Card

Permanent Magnet dc Motors

Selection and units conversion tables, performance data, and winding variations for motors and motor tachogenerators are supplied by catalog that includes dimensional drawings and graphs. **Moore Reed and Co Ltd,** Walworth Andover Hampshire, England.
Circle 458 on Inquiry Card

Cardedge Connectors

Catalog for 01 to 06 and 10 series includes features, specs, materials and finishes, assembly and finish codes, polarization keys, dimensions, and cross-reference chart. **Teka Products, Inc,** Woodside, NY.
Circle 459 on Inquiry Card

Microprocessor Software

Catalog describes 6800/6809 software for single-user, multi-user, and network operating systems, as well as BASIC compilers, assemblers, editors, and word processing and accounting software. **Software Dynamics,** Anaheim, Calif.
Circle 460 on Inquiry Card

Leadless Chip Carriers

Included in brochure are table of application areas for components in military, industrial, and medical categories, discussion of testing and support, comparison of screening and lot conformance, and products listings. **Mostek Corp,** Carrollton, Tex.
Circle 461 on Inquiry Card

Transformers, Inductors, and Power Supplies

Catalog features Flat Pack™ power transformer, along with filter reactors, dc power supplies, magnetic components, audio transformers, and toroidal inductors, and provides photos, specs, and drawings. **Triad-Utrad Distributor Services,** Huntington, Ind.
Circle 462 on Inquiry Card

OEM EUROPE MEETS AT THE INVITATIONAL COMPUTER CONFERENCES

In November in Amsterdam, Milan and Paris, OEM decision makers will meet the industry's top computer and peripheral manufacturers at the Invitational Computer Conferences—the only seminar/displays designed specifically for the unique requirements of the quantity user.

At these one day, regional conferences guests will have a close-up view of every type of computer and peripheral—mini/micros, disk drives, tape drives, printers, interfaces, controllers, graphic display terminals—and will be welcome to attend a program of technical seminars covering the latest state-of-the-art technology. Some of the companies displaying products will be Arsycom BV, Century Data Systems, Cii Honeywell-Bull, Cipher Data Products, Dataram, Digital Communications Associates, Genisco Computers, MDB Systems, Priam, Printronix, Remex, National Semiconductor, Kennedy and Trilog.

Technical product seminars will be presented on streaming tape drives, graphic display systems, winchester disks, matrix line printers, color printer/plotters and add-in memories.

Plan to attend the conference in your area. Invitations are available from participating companies or from the ICC sponsor. For further information contact:

B.J. Johnson & Associates, Inc.
2503 Eastbluff Drive
Newport Beach, CA 92660
Telephone: 714/644-6037
Telex: 678401 TAB IRIN

or

Tom Lewis
#27 Raleigh Road
Richmond, Surrey TW92DU
England
Telephone: 01-948-2447

Invitational Computer Conference 1981/1982 Schedule

Amsterdam	**November 5, 1981**
Milan	**November 10, 1981**
Paris	**November 17, 1981**
London	**March 1982**
Frankfurt	**March 1982**
Stockholm	**March 1982**

Invitational Computer Conferences

CIRCLE 192 ON INQUIRY CARD

ADVERTISERS' INDEX

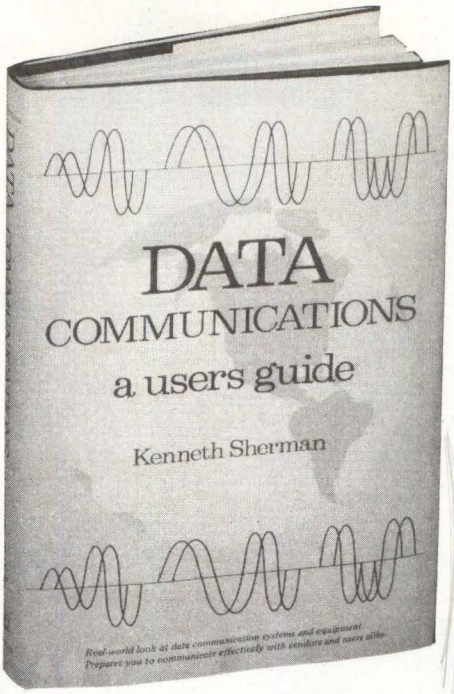
ADVERTISERS' INDEX

Designer's Bookcase

DATA COMMUNICATIONS a user's guide by *Kenneth Sherman.*

A BRAND NEW quick and effective source for pinpointing and eliminating system malfunctions, discovering new, more efficient data movement, learning effective trouble-shooting, ensuring strong, clear signal transmission and achieving maximum performance and value. Put these *all new* ideas and many others to work for you!

348 pages; 95 illustrations; Reston Publishing Company Inc; $21.95. 1981.
Circle 215 on Inquiry Card



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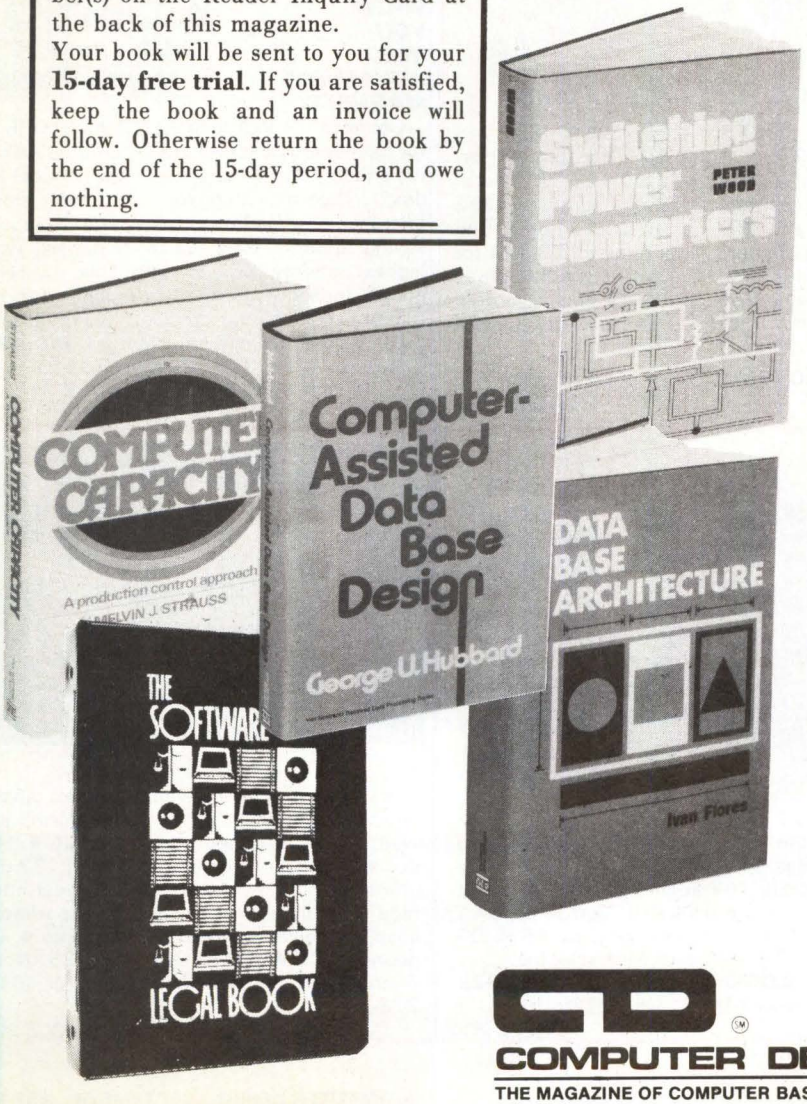
15-DAY FREE EXAMINATION

Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine.

Your book will be sent to you for your **15-day free trial.** If you are satisfied, keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period, and owe nothing.



Computer Capacity: A Production Control Approach by *Melvin J. Strauss.*

Unlike other books that treat computer performance measurement, this practical volume introduces standard industrial production control techniques that show how to deal with daily and weekly variances in utilization, how to quantify the effect of those variances on user service levels, and how to plan capacity and accommodate utilization variances.

280 pages; 6 x 9; 128 illustrations; Van Nostrand Reinhold; $24.95. July, 1981.
Circle 216 on Inquiry Card

Data Base Architecture by *Ivan Flores, Ph.D.*

This is the definitive guide to data base organization, giving the answers to the why's and how's. It describes the structure and use of information organized into a data base, and how application programs, data structures, data base management systems (DBMS), the operating system, and hardware relate to each data base organization.

408 pages; 295 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. July, 1981.
Circle 217 on Inquiry Card

Switching Power Converters by *Peter Wood.*

For the first time ever, the entire field of switching power converters is covered in one volume. *Switching Power Converters* provides vital information on basic principles, relationships and characteristics of switching power converters, giving the reader the means for acquiring solid design competence.

464 pages; 142 illustrations; 6 x 9; Van Nostrand Reinhold; $26.50. May, 1981.
Circle 218 on Inquiry Card

The Software Legal Book by *Paul S. Hoffman.*

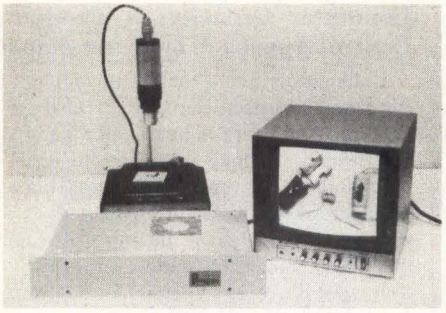
Written by a practicing attorney and CDP holder in non-legal terms. Covers: Protection of proprietary software, ownership of software and modifications, defining deliverables, basic contract provisions, warranties, excusable delays, special contract situations, bundled systems, third party leasing, arbitration, and developing software from contracts.

179 pages; L.L. bound; Carnegie Press; $59.95. 1981. Circle 219 on Inquiry Card

Computer-Assisted Data Base Design by *George U. Hubbard.*

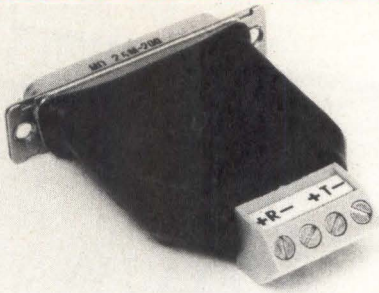
This book not only thoroughly explains the theoretical aspects, but also provides explicit directions on all data base design procedures. In addition to a practical design methodology it discusses the ways to automate the major portions of this methodology. However, all of the techniques can be utilized without computer assistance.

320 pages; 123 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; $24.95. August, 1981. Circle 220 on Inquiry Card



DIGITAL IMAGE DISPLAY

The Model 108 is a 128 x 128 by 8 bit memory providing continuous, composite video output. Easily interfaced to mini and micro systems, the 108 accepts parallel data at up to 3 MHz and is plug compatible with the GE2210A Automation Camera. Ideal for medium resolution OEM applications, prices start at $820. **POYNTING PRODUCTS, INC.**, P.O. Box 1227, Oak Park, IL 60304. Tel: (312) 236-0725. **CIRCLE 197**



SMALLEST LINE DRIVER IN THE WORLD

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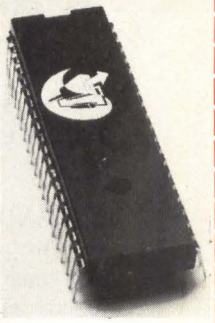

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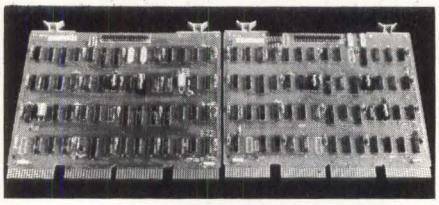

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The PPL-1 Peripheral Processor Link is a unique shared memory interface between any two Q-bus (LSI-11) and/or Unibus (PDP-11)-based DEC CPU's. Two quad boards and a connecting cable link the peripheral unit with the host. Up to 32KB of memory may be accessed by the peripheral processor *at any location* within the host. 16 vectored interrupts (8 from each direction) provide necessary hardware for protocol implementation. Multiple PPL-1's provide capability for parallel processing.

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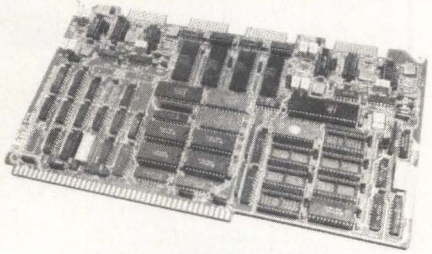

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The 8103 SCC enhances system performance with an on-board 8085A microprocessor controlling 2 on-board Bell 202 modems and 2 serial RS232C ports. The 8103 SCC features 32k bytes of EPROM for protocol and error checking routines. Data is passed through the 8k bytes of dual ported RAM to the MULTIBUS interface for system use.

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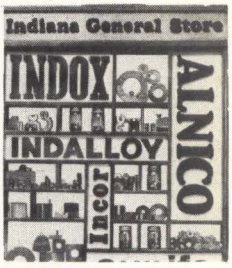

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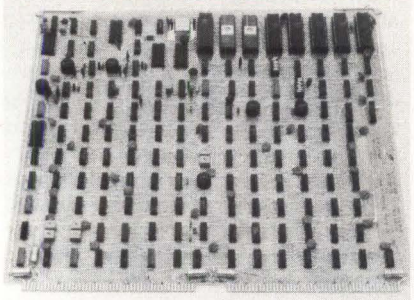

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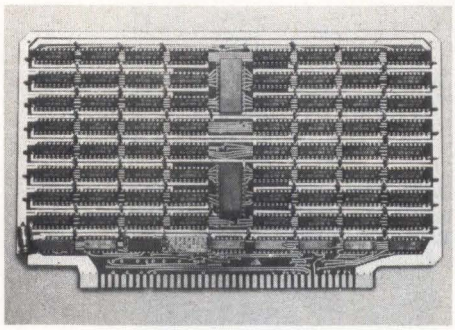

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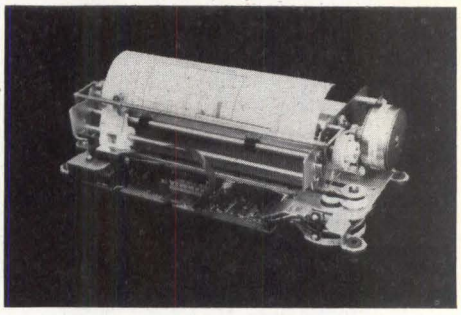

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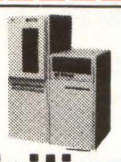

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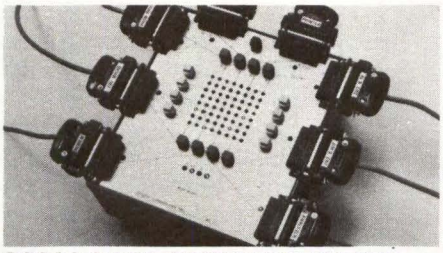

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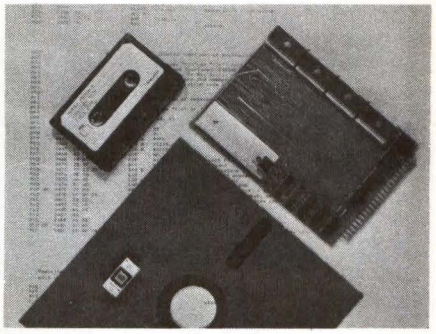

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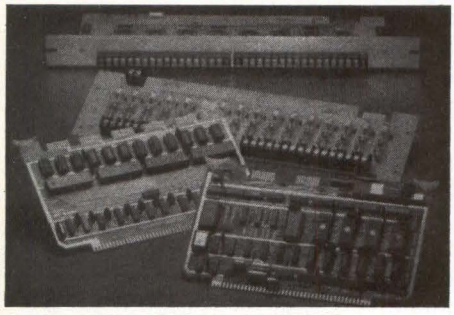

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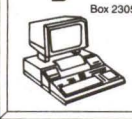

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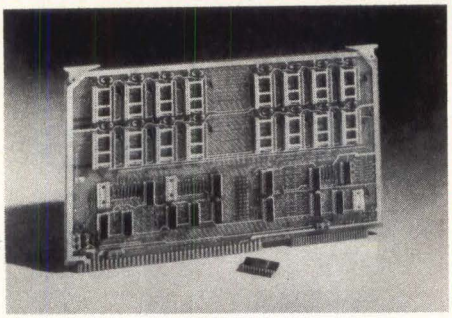

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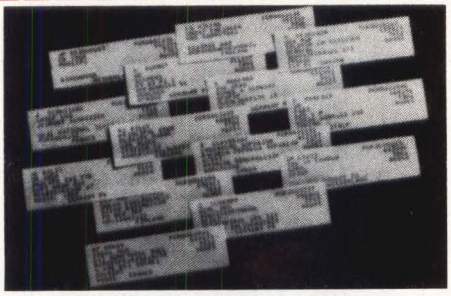

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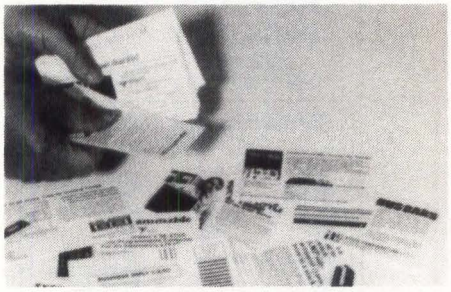

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It is with this engineering manpower requirement in mind that **COMPUTER DESIGN** is presently conducting the industry's first Career Growth Benchmark Survey. Through this study, engineers throughout the country have the opportunity to express their perceptions and opinions of these companies looking to hire them.

Subjects covered include: A determination of present salaries and anticipated salary increases through 1985. A check on how respondents feel about the area of the country where they presently reside, and a ranking of geographical areas in terms of their willingness to relocate.

Four major groups of designers (hardware, software, CAD/CAM and data communications) are evaluating a list of companies most actively seeking personnel with their specific qualifications. Respondents will also indicate whether they are aware that each of these companies is looking for people with their particular skills. Also whether or not they have seen recruitment advertisements from these companies.

Finally, they are indicating whether they would consider a job with the companies listed. Comments, both positive and negative, of these companies will also be included.

The results of this survey may have a profound effect on the approach that companies take in structuring salaries, benefits and other inducements to attract top design engineers.

This Career Growth Benchmark Survey is another significant aspect of **COMPUTER DESIGN's** commitment to the design engineer. If you have received one of these questionnaires, please fill it out and return it promptly—your answers are vital to the completed results. In this section during the months ahead, we will be reporting your collective opinions and perceptions in response to this study and others like it.

Ronald W. Evans

Ronald W. Evans,
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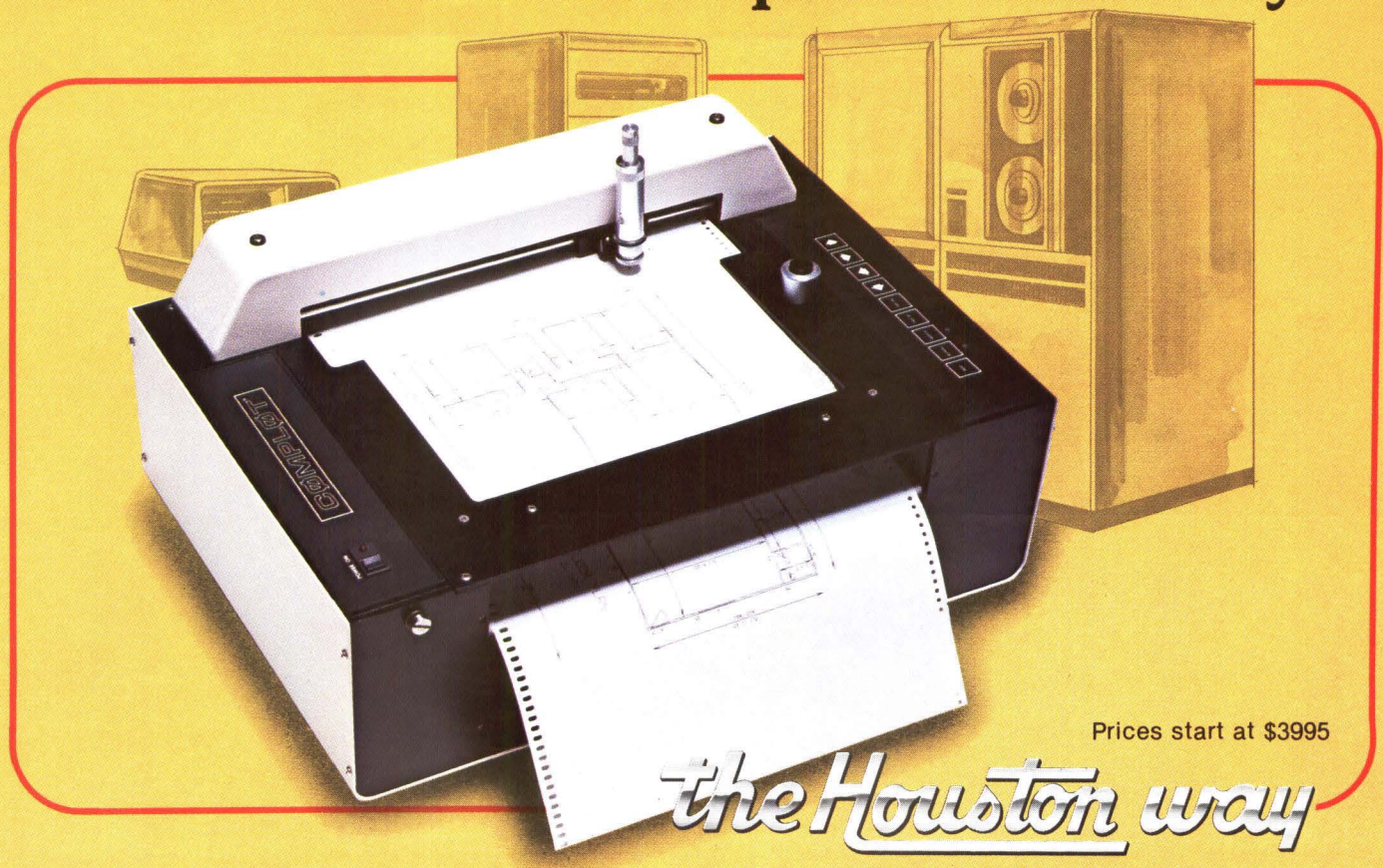

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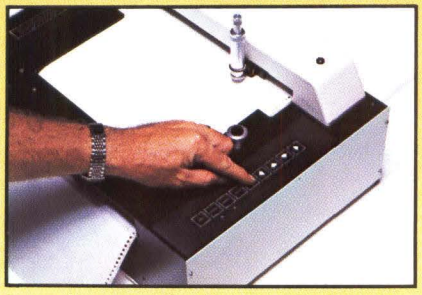

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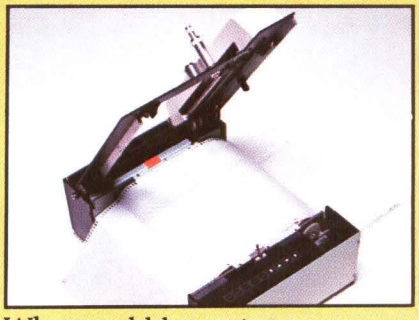

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