

COMPUTER DESIGN

SEPTEMBER 1980

THE MAGAZINE OF
COMPUTER-BASED SYSTEMS

MEETING THE CHALLENGE OF AUTOMATED ECL TESTING

SINGLE-CHIP CONTROLLER INCREASES MICROPROCESSOR THROUGHPUT

OPTIMIZING MINICOMPUTER POWER SUBSYSTEM DESIGN



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Imagine...

...the dynamics of vector graphics now in full raster color.

Introducing the Whizzard 7200 family of serial and parallel interactive graphics systems.

Included are two new high-performance color raster Whizzards so fast they can modify complex engineering displays at a remarkably high frame rate — speed that rivals the powerful refresh vector output Megatek is known for.

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We've doubled the size of our graphics microcode. New segment header formats. New command structures. New smart interrupts.

The result: More graphics power using less host computing power. Peripheral device electronics do most

of the work. You get faster updates. Better human response. More efficient memory usage and data transfers.

Teamed with RS-232C serial interfaces, Whizzard graphics power now moves squarely into the world of time-sharing and distributed processing.

You can configure the Whizzard 7200 family to fit virtually any application simply by changing output circuits. Serial or parallel vector calligraphic. Serial or parallel raster. Or both simultaneously from one electronic chassis! All are driven by one common graphics software package — Megatek's new WAND 7200.

You can add many "intelligent" microprocessor-controlled peripheral devices to boost system capability.

All work independently to free both the host computer and graphic processor for jobs they do best.

It's like taking distributed processing one more step.

Continuous real-time pan, zoom, 3-D hardware transformations, and other display capabilities are done in the terminal, not in the computer.

No wonder Megatek is fast becoming the technological leader in high-quality, high-performance refresh graphic systems.

For details, call or write Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590.



MEGATEK / WHIZZARD

COMPUTER GRAPHICS SYSTEMS

New From Kennedy

Model 6450

High Density Cartridge Tape System

Low cost, flexible and reliable backup—that's Kennedy's Model 640 Cartridge Tape Drive and Model 650 Embedded Formatter—combined in one compact package—Model 6450. Model 6450 is loaded with features, such as:

- Low power consumption—the system requires only +5 and +24 volts for a total consumption of under 40 watts.
- Serpentine recording head—eliminates time consuming rewinds between tracks during backup process.
- 6400 BPI recording density—yields up to 17 Mbytes of unformatted data capacity on a 450 ft. cartridge.
- Infrared tape position detection—virtually impervious to ambient light, a major factor in tape position sensing errors.
- Online self test—The 6450 system performs online self test before your backup operation begins.

These are only a fraction of the features that make Model 6450 the most advanced 1/4" tape cartridge available. All these features, combined with Kennedy experience and reliability guarantee it.

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CIRCLE 2 ON INQUIRY CARD

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New features from the leader in matrix line printers.

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And now you can move the printer from the computer room and locate it where the information is used. A new Asynchronous Communications Adapter gives you 300 line per minute on-line **remote printing**.

Plus, look at the standard features of every T-3000. Quiet operation. Easy, front access, straight path paper loading. A reel to reel, prethreaded ribbon system for quick and clean ribbon changing. A time saving **diagnostic status display** that reduces service calls. It tells if a fault condition is operator correctable. If a service call is needed, it tells the service man what's wrong.

Dependable and durable, the T-3000 never requires preventive maintenance. Never needs adjustment. Character formation and line registration never waver. The T-3000. High reliability. Patented **flexure technology**.

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Mannesmann Tally, 8301 South 180th Street, Kent, WA 98031. Phone (206) 251-5524.

Printers for the long run.

MANNESMANN TALLY



DEPARTMENTS

10 CALENDAR

14 COMMUNICATION CHANNEL

First of a 4-part series presents an overview of a task-oriented military distributed processing system connected on a high speed serial bus. Subsequent issues will carry detailed discussions of data bus, system computers, and software design

54 TECHNOLOGY REVIEW

Multiple instruction, multiple data stream architecture of 64-bit digital computer achieves effective processing speeds ranging from 10M to 160M instructions/s

86 DIGITAL CONTROL AND
AUTOMATION SYSTEMS

Development time and the expense inherent in manual design of printed circuit boards are reduced by an automated system

156d TECH BRIEFS

166 MICRO DATA STACK/COMPUTERS,
ELEMENTS, AND SYSTEMS

Using software driven approach, universal microprocessor development system provides realtime emulation of any 4- to 32-bit microprocessor at up to 30 MHz

188 AROUND THE IC LOOP

Design of a 32-bit floating point multiplication system involves separation of exponent from mantissa and multiplication of mantissa through summing partial products

210 PRODUCTS

244 LITERATURE

248 ADVERTISERS' INDEX

Reader Service Cards
pages 253-256

Number of copies printed this issue—88,120.

FEATURES

MEETING THE CHALLENGE
OF AUTOMATED ECL TESTING 115

by Robert L. Hopkins

ECL components offering state of the art switching speed tend to be used close to their performance limits, making it vital to determine those limits and to assure that devices used in production meet them

SINGLE-CHIP CONTROLLER INCREASES
MICROPROCESSOR THROUGHPUT 125

by Alan W. Bentley

Through use of programmed array logic, the design for a DMA controller achieves a fast, flexible data transfer capability that is custom tailored to the application environment and yet easy to modify or adapt with little or no hardware reconfiguration

OPTIMIZING MINICOMPUTER
POWER SUBSYSTEM DESIGN 133

by Ermand B. Centofanti, Allen B. Hansel,
Philip N. Lioio, and Thiagarajan Natarajan

Minicomputer power supply implements a modular design approach to satisfy performance, reliability, safety, and field support requirements. Controller and front end modules attach to nearly identical converter modules in the basic subsystem—installed in each cabinet—with a master subsystem controlling multiple slaves

MIXED FORMAT OPERATION ENABLES ECONOMICAL
OUTPUT FROM THERMAL PRINTER/PLOTTER 144

by Harold D. Schofield

Thermal printer design accepts mixed plot and character data input to achieve economical hardcopy output in microprocessor based systems



Circulation audited by
Business Publications Audit

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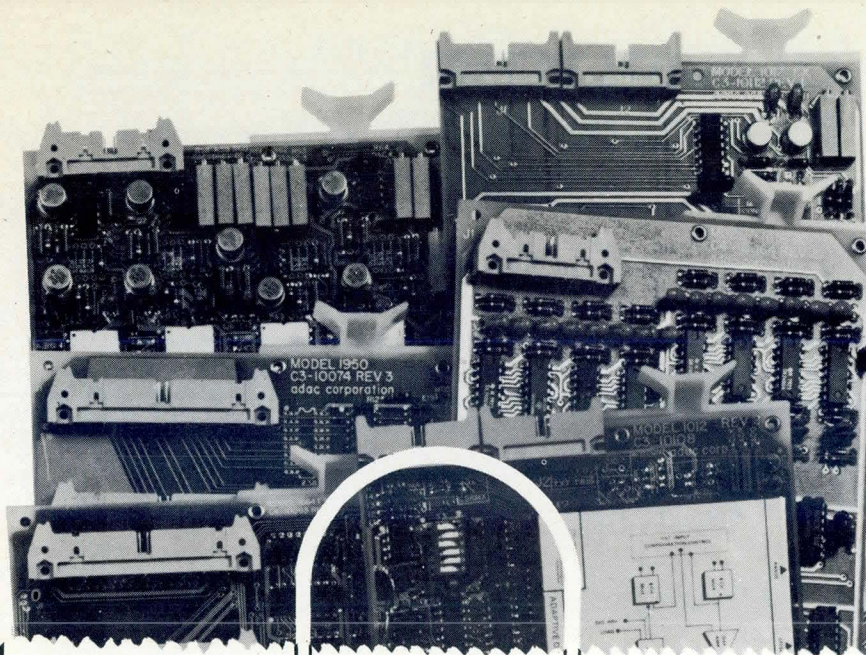
Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."



Member American Business Press, Inc.

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- 1113EX** 8-16 differential low level and thermocouple inputs, mux expander, LSI-11/23 interrupt compatible
- 1412DA** 1-4 D/A channels, voltage or current loop outputs

CLOCK CARDS

- 1601GPT** Programmable crystal clock/timer

SERIAL I/O CARDS

- 1750** Asynchronous line interface with two I/O ports

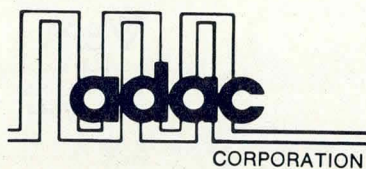
DIGITAL I/O

- 1604/OPI** 2-4 optically coupled pulse-input channels
- 1604/POC** 2-4 pulse output channels
- 1616CCI** 16 discrete inputs, contact closure detect
- 1616/MIC** 16 discrete inputs with priority encoder
- 1616/OIO** 16 parallel outputs, optically isolated
- 1616/OII** 16 parallel inputs, optically isolated, can cause interrupt
- 1620TTL** 16 latched inputs and outputs for DMA operation
- 1616HCO** 16 discrete outputs, high current drive
- 1632HCO** 32 discrete outputs, high current drive
- 1632TTL** 32 TTL I/O lines
- 1664TTL** 64 TTL I/O lines

BUS INTERFACE

- 1620DMA** Direct memory access controller
- 1900** Unibus to LSI-II translator
- 1950** Bus repeater
- 1900CT** Cable terminator card

Whatever your DEC system—Unibus, Qbus or Omnibus, write or call for full details on the industry's widest line of compatible cards and complete system enclosures.

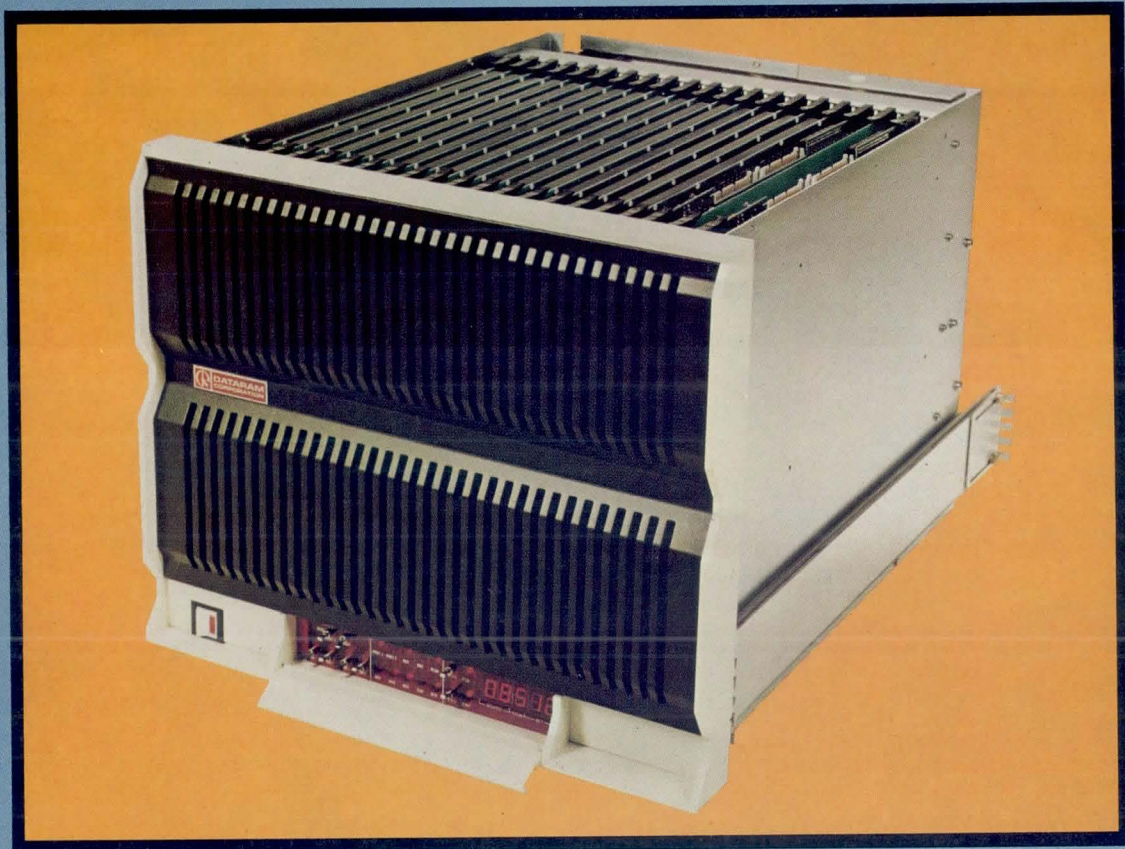


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CIRCLE 5 ON INQUIRY CARD

BIOMATION K100-D



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GLITCH
FIXER
FROM GOULD

Compare this general purpose logic analyzer with the currently accepted industry standard.

The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

mode to catch glitches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, main-frame and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

binary or ASCII. And the list goes on and on.

The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

Compare capacity.

The K100-D's 1024 word memory is *four times as deep as the 1615A's*. This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

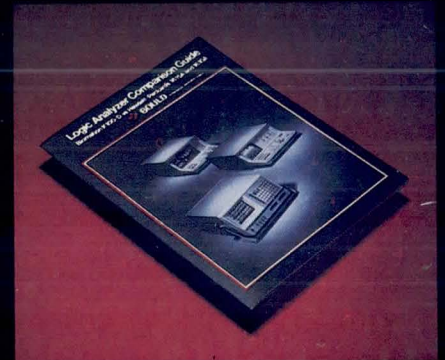
Compare your productivity.

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal,

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's*. Use the K100-D's latch



Hewlett-Packard 1615A
A very good logic analyzer



Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data,
or 24 data

Biomation K100-D
The industry's finest logic analyzer



Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data,
or 32 data



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CIRCLE 6 ON INQUIRY CARD



CalComp Can Show You

New from CalComp... Graphic 7 Display System and Talos Digitizers.

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Now CalComp brings you two more alternatives to help you meet your operational needs: The Graphic 7 stroke-refresh display system and Talos digitizers.

The Graphic 7 combines the latest technological features, including dual microprocessors, complete graphics support software and stroke-writing capabilities to give you all the benefits of interactivity, high quality image and operational ease.

Talos highlights its long line of fine digitizing devices with two new products, the Wedge and the 800 Series, each with advanced electromagnetic technology. The Wedge, with a five-degree sloped surface gives you greater operating ease. And the 800 Series, available in a variety of tablet sizes, allows for dual tablets, cursors and multiple interfaces for your varied applications.

Everything you need for most applications.

Whether for engineering, scientific, or business applications, you can be sure there's a CalComp product for you. Our family line of drum plotters includes a full range of sizes from desk tops, to our biggest drum plotter yet, the Model 1065 with an impressively large 72" drum.

For cut sheet applications, CalComp's full line of beltbed plotters delivers quality resolution and high throughput. Like our Model 970, the newest and biggest in our beltbed series, which gives you large 52" x 80" size plots usually associated with flatbed plotters.

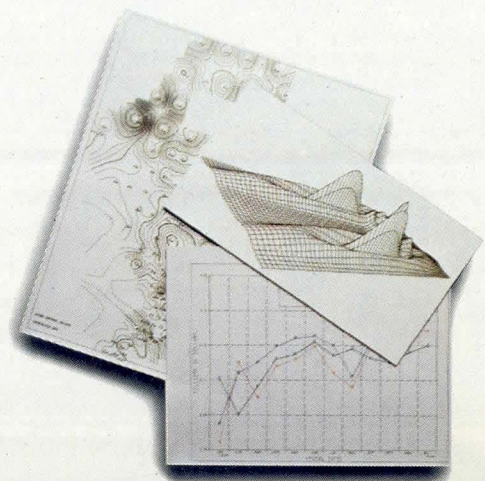
Flatbed plotters still play an important role in dozens of applications. The CalComp Model 7000 high performance drafting system features our programmable controller for added flexibility.

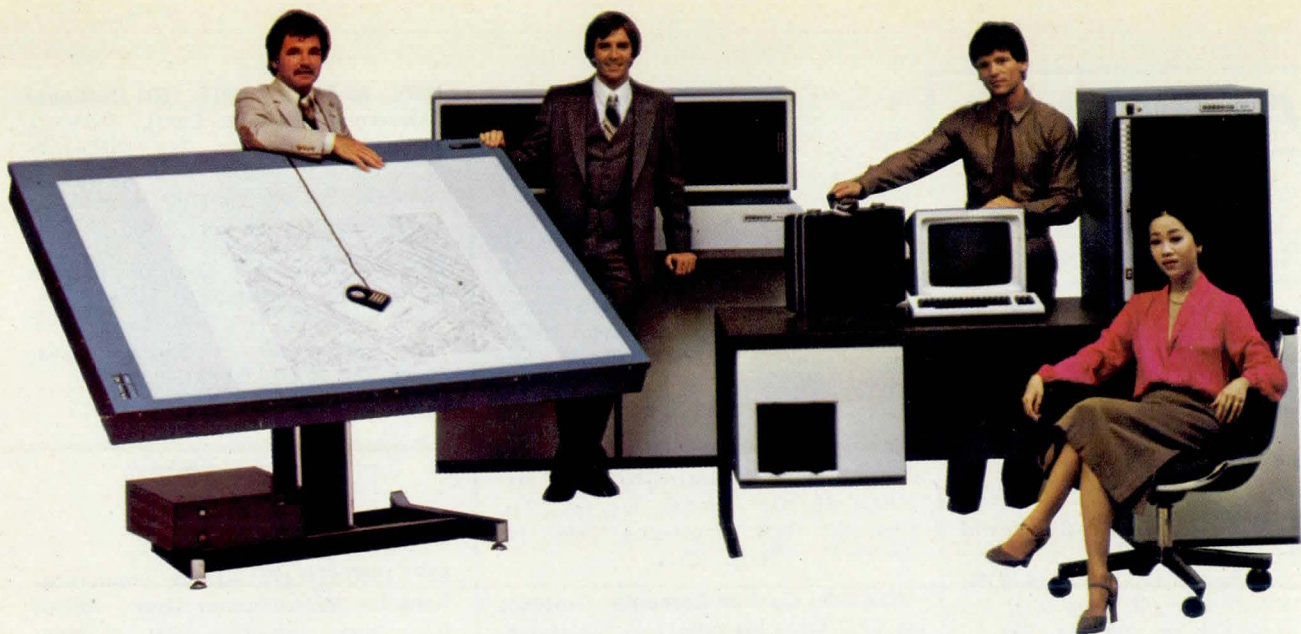
If your operation handles large volumes of work, and you find more and more valuable time is spent performing job management functions rather than creative tasks, you may want to consider CalComp COM units. COM gives you all the advantages of organizing, compacting and storing

reams of output on readily accessible microfiche, 35mm aperture cards, or 35mm and 16mm film.

CalComp 11" and 22" electrostatic plotter/printers offer an affordable solution to many applications requiring high speed production, and can also function as a high-speed line printer, while clear mylar media furnishes finished drawing quality.

What's more, our extensive library of application software packages and CalComp supplies (we can provide all types of drawing media and pens), make us your true source for everything you'll need in computer graphics.



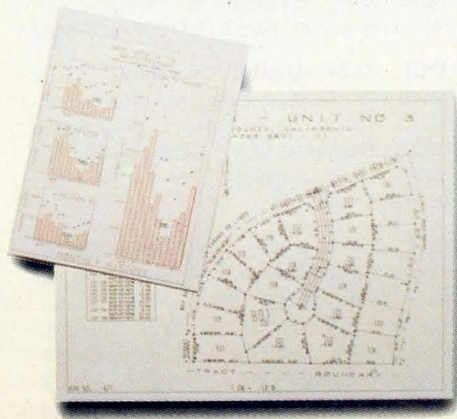


All the Alternatives.

CalComp support at any point.

The all-professional, factory-direct, CalComp team, starting with your CalComp sales representative, is there to give you all the help you may need at *any* point in your computer graphics operation.

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CALENDAR

CONFERENCES

- OCT 1-3—Internat'l Conf on Circuits and Computers for Large Scale Systems**, The Rye Town Hilton Inn, Port Chester, NY. INFORMATION: Dr NB Guy Rabbat, 32 Tor Rd, Wappingers Falls, NY 12590. Tel: 914/897-8126
- OCT 6-9 AND OCT 14-17—8th World Computer Congress**, Tokyo, Japan, and Melbourne, Australia. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100
- OCT 8-9—Connector Symposium**, Benjamin Franklin Hotel, Philadelphia, Pa. INFORMATION: Jim Pletcher, Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 717/780-8857
- OCT 13-15—Symposium on the Foundations of Computer Science**, Sheraton Inn, Syracuse, NY. INFORMATION: Prof Ronald V. Book, Dept of Math and Comp Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778, 2171
- OCT 13-15—Internat'l Computer Conf: Hong Kong 1980**, Hong Kong. INFORMATION: Dr Wellington C. P. Yu, IBM Corp, F02/61C, 5600 Cottle Rd, San Jose, CA 95193. Tel: 408/256-3426
- OCT 14-16—Mini/Micro Computer Conf and Exposition**, Civic Auditorium, San Francisco, Calif. INFORMATION: Robert D. Rankin, Mini/Micro Conference and Exposition, 32302 Camino Capistrano, Suite 202, San Juan Capistrano, CA 92675. Tel: 714/661-3301
- OCT 16-19—Mid-West Computer Show**, McCormick Place, Chicago, Ill. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000
- OCT 20-23—CPEUG '80 (Meeting of the Computer Performance Evaluation Users Group)**, Orlando, Fla. INFORMATION: Theodore F. Gonter, U.S. General Accounting Office, 441 G St, NW, Rm 6118, Washington, DC 20548. Tel: 202/275-5410
- OCT 26-29—ACM '80 (Assoc for Computing Machinery Nat'l Conf and Exhibition)**, Opryland Hotel, Nashville, Tenn. INFORMATION: Lucy Jean Johnson, Box 1980 Station B, Nashville, TN 37235. Tel: 615/322-2951
- OCT 27-30—ICCC '80 (Internat'l Conf on Computer Communication)**, Peachtree Plaza Hotel, Atlanta, Ga. INFORMATION:

ICCC '80 Executive Committee, PO Box 280, Basking Ridge, NJ 07920. Tel: 201/221-8800

OCT 28-30—Interface West, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

OCT 30-NOV 1—Nat'l Small Computer Show, New York Coliseum, New York, NY. INFORMATION: Ralph Ianuzzi, 110 Charlotte Place, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

NOV 3-5—Conf on Computer Graphics in CAD/CAM Systems, MIT, Cambridge, Mass. INFORMATION: Prof David C. Gossard, Dept of Mechanical Engineering, Rm 3-445, Massachusetts Inst of Technology, 77 Massachusetts Ave, Cambridge, MA 02139. Tel: 617/253-4465

NOV 4-6—MIDCON/80, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 6-12—Electronica '80, Munich Fairgrounds, Munich, West Germany. INFORMATION: Franc D. Manzolillo, Rm 6015, U.S. Dept of Commerce, Washington, DC 20230. Tel: 202/377-2991

NOV 10-13—INTELCOM '80 (Internat'l Telecommunications and Computer Conf and Expo), Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: Janet E. Schotta, Horizon House International, 610 Washington St, Dedham, MA 02026. Tel: 617/326-8220

NOV 11-14—Conf on Magnetism and Magnetic Materials, Dallas Hilton, Dallas, Tex. INFORMATION: D. C. Bullock, Texas Instruments, Inc, MS 974, Dallas, TX 75265

NOV 17-19—Asilomar Conf on Circuits, Systems, and Computers, Asilomar Conference Grounds, Pacific Grove, Calif. INFORMATION: A. M. Davis, Asilomar Conference, Dept of Electrical Engineering, San Jose State U, San Jose, CA 95192

NOV 19-21—GOMAC '80 (Government Microcircuit Applications Conf), Shamrock Hilton, Houston, Tex. INFORMATION: Larry W. Sumney, OUSDRE/E&PS, The Pentagon, Washington, DC 20301. Tel: 202/697-4198

NOV 20-23—Northeast Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

NOV 30-DEC 4—NTC '80 (National Telecommunications Conf), Shamrock Hilton Hotel, Houston, Tex. INFORMATION: John R. Howell, Houston Lighting and Power Co, PO Box 1700, Houston, TX 77001. Tel: 713/228-9211, X3351

DEC 1-4—Internat'l Conf on Pattern Recognition, Konover Hotel, Miami Beach, Fla. INFORMATION: Harry Hayman, 5th Pattern Recognition, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

SEMINARS

SEPT 1980-FEB 1981—Data Communications for Minicomputer Users, various U.S. cities. INFORMATION: Margaret Harveston, MICOM Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. Tel: 213/882-6890

OCT 30-31 AND NOV 17-18—Microprocessors: Hardware, Software, and Applications, Worcester Polytechnic Inst, Worcester, Mass, and Sheraton Tara, Framingham, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Professional Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/753-1411, X517

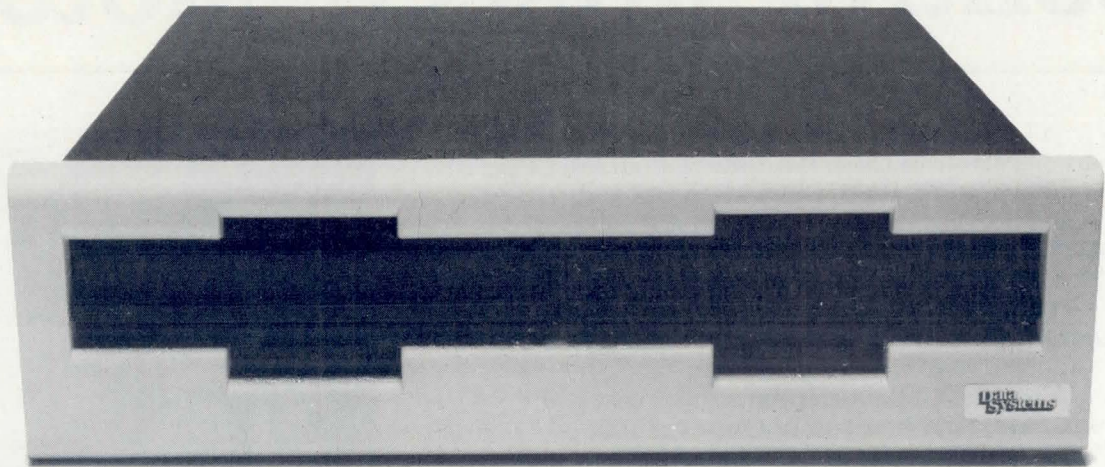
SHORT COURSES

OCT 7-10—Pascal Computer Programming; OCT 13-17—Electromagnetic Interference and Control; OCT 15-17—Recent Advances and Current Trends in Data Networks; OCT 20—Modern Software Development Techniques for Managers; OCT 20-24—Distributed Processing; AND OCT 27-31—Data Communications Systems and Networks, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

OCT 20-24—Digital Switching, U of Maryland, College Park, Md. INFORMATION: Continuing Education in Engineering and Mathematics, UCLA Extension, PO Box 24901, Los Angeles, CA 90024. Tel: 213/825-1047

OCT 20-23, 1980, AND JAN 12-15, 1981—Principles and Applications of VLSI Technology, Sheraton Tara Hotel, Boston-Braintree, Mass, and Sheraton Palace Hotel, San Francisco, Calif. INFORMATION: Leonard Klein, Palisades Institute, 201 Varick St, 9th Floor, New York, NY 10014. Tel: 212/620-3377

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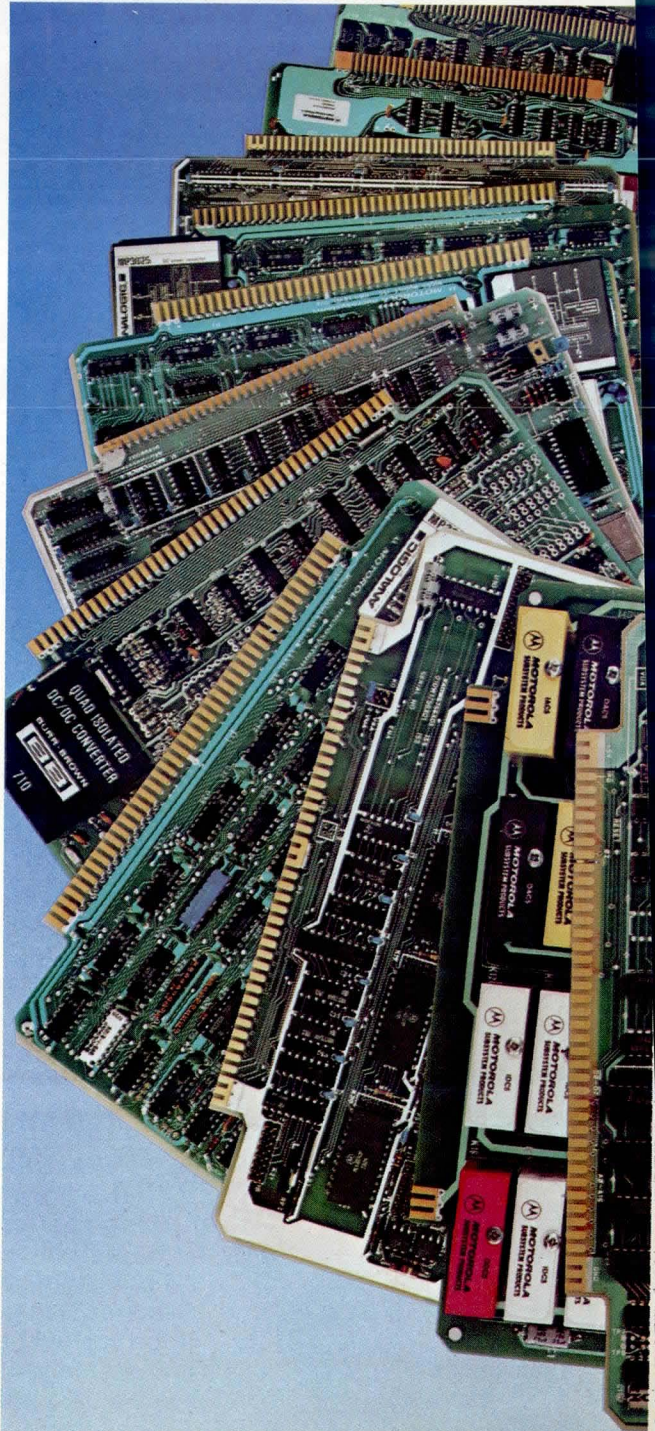
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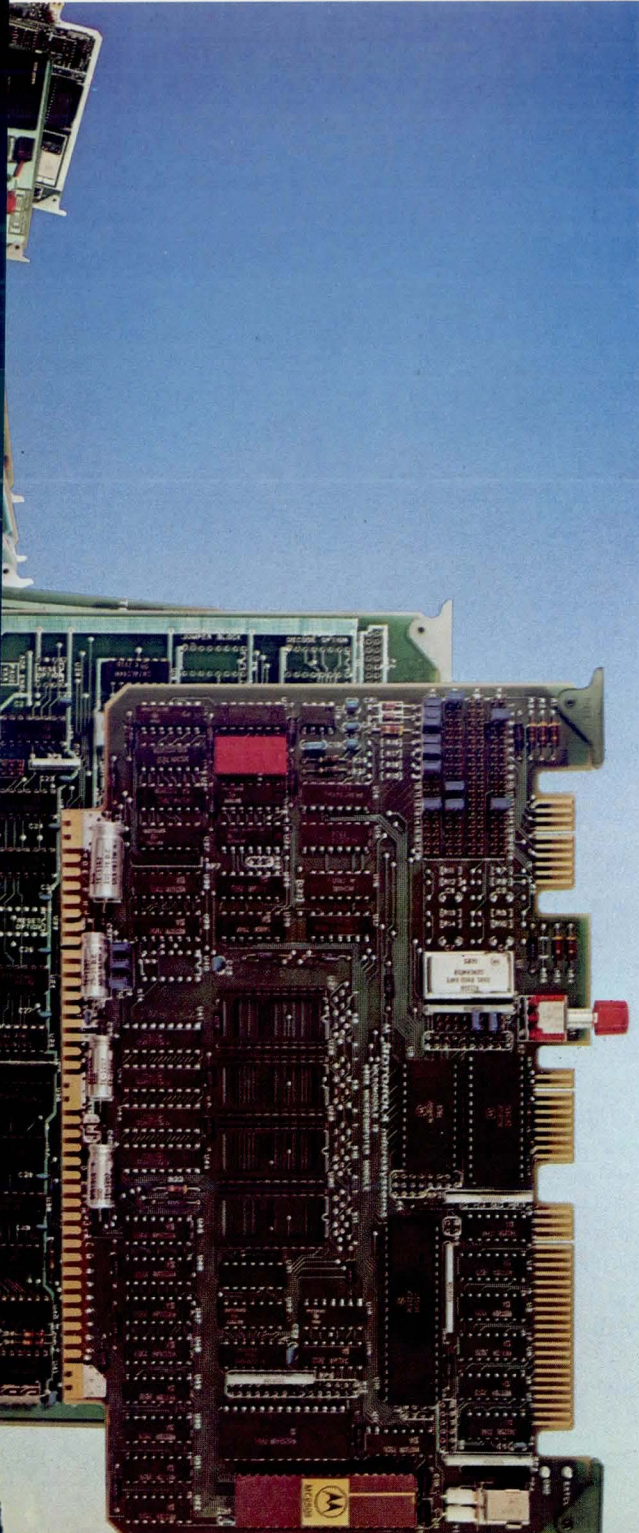
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A DISTRIBUTED PROCESSING SYSTEM FOR MILITARY APPLICATIONS— PART 1: SYSTEM OVERVIEW

Ralph Mauriello

Litton Data Systems

8000 Woodley Ave, Van Nuys, CA 91409

This series of four articles describes a geographically separated, functionally organized, task-oriented distributed processing system, connected on an efficient, high speed serial data bus. Military systems designers are given a set of hardware and software building blocks for configuring a highly responsive and adaptable system that can be phased into current applications with a minimum of disturbance by utilizing current software. There is also provision for constantly incorporating new technology.

The Litton distributed processing system was designed to satisfy military requirements with new technology hardware and newly developed software and system concepts for distributed system control. Recently, breadboard versions of the required hardware, firmware, and system control software were successfully demonstrated in a 3-node, 4-processor loop configuration. Development of MIL-Spec versions is now in progress.

A study performed before implementation focused on four key aspects: system architecture, the data bus, the data processing hardware, and system software. Considerations for the data bus included system communication connectivity, speeds, and techniques. For the data processing hardware, it was necessary to determine what distributed control (hardware and firmware) was needed to integrate the bus and the processors into an effective total system. Finally, which software processing features were optimum in a high speed data bus environment were determined.

System Characteristics

Three factors usually characterize a distributed processing system (DPS):

The processing is distributed among several processing elements. Processing capability at each node may range from a single low cost software compatible DPS microprocessor to multiple high throughput number crunchers. The application programs are also distributed. Only applications that are needed at the element are stored locally. The need for program storage within the node is determined by system response requirements. Therefore, replication of programs may be indicated.

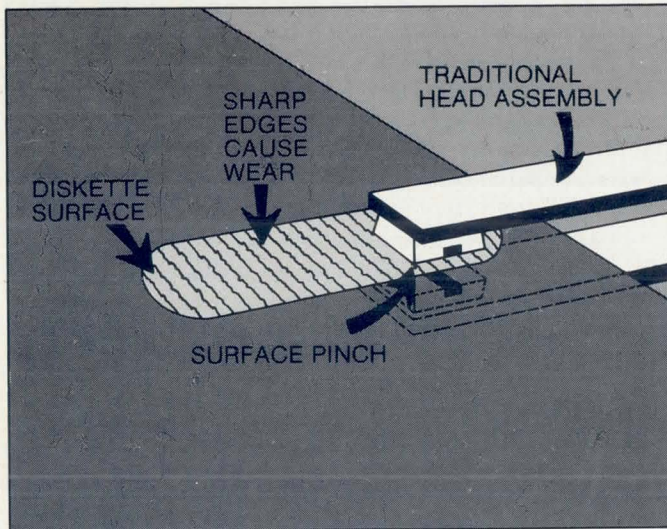
The data base is distributed among the elements. Various portions of the system data base may be replicated at various nodes to assure that system response time requirements are satisfied. However, only one change authority is allowed for each data element of the data base.

The system control is distributed. Local (or nodal) control is exercised at each node by an executive program. Overall system (or network) control is accomplished by a module of the executive that may be located at any one of the nodes in the system. Identical firmware at each node provides emulation, bus control, and special microprograms for displays or communication links.

The characteristics of the DPS provide efficient handling of functionally partitioned software tasks. Each software module may issue requests for action to other modules, whether local to the node or at a remote node, with the entire transaction being transparent to the software module.

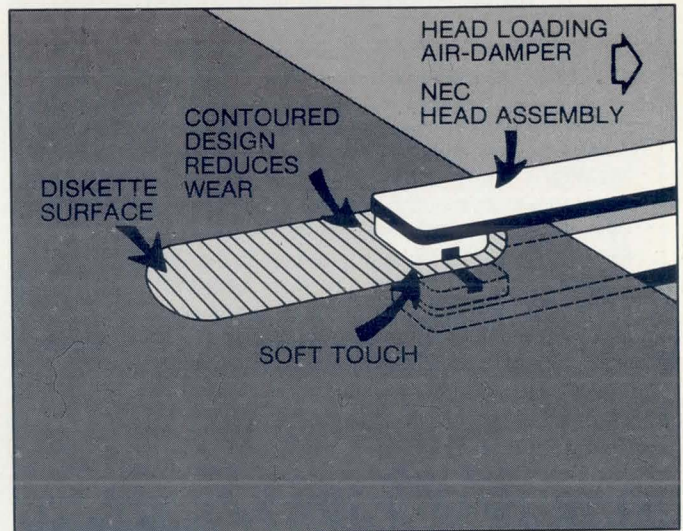
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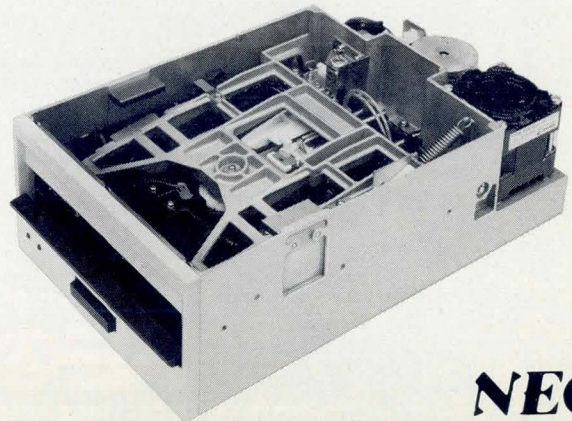
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Objectives for the DPS Project

Develop a distributed processing system architecture capable of satisfying military command and control system requirements

Develop the necessary hardware, firmware, and software to support the architecture

Satisfy a wide range of applications with a minimum set of common hardware and software modules

Design a highly maintainable and reconfigurable system

Provide orderly transition from supplementing existing systems in the field, through replacement, to introduction of new systems

Litton Approach to DPS Design

Design emulators to permit use of a variety of existing repertoires and languages

Provide architectural extensions to these emulators, which are both conventional, such as memory address extension, and specialized, for control of distributed processing

Develop a high speed bus architecture capable of either fiber optic or coaxial cable implementation

Provide system level control for loops and networks and, at each node, distributed executive software

Use functional card building block approach

Partition the hardware design for survivability, maintainability, and logistics considerations

Design for transition from existing to new systems

Objectives and Approach

Original objectives of the project, and the Litton approach to achieving these objectives, are shown in the Panel. Existing commercial distributed systems were reviewed to determine applicability of any currently operational features. None of these computers or bus architectures satisfied all the military reconfigurability and realtime requirements. As a result, it was decided to develop a new computer family and communication bus protocol. This approach permitted the identification of all requirements and an allocation of each of these either to hardware, firmware, or software as a function of the most cost-effective method of implementation.

In order to permit the use of existing software wherever possible, a family of military central processing unit (CPU) emulators has been defined for DPS. The first of the family to be implemented are two types of AN/UYSK-20¹ that are currently in operation. These emulators will be described in a subsequent article.

Architectural extensions are implemented in a fully software compatible manner to assure capture of existing software. Naturally, new software will be required to take advantage of these enhancements which come in two forms: conventional and distributed processing functions. Features such as extended memory addressing, paging, protection, and the like are typical of the conventional enhancements. Distributed system functions have been added to assure transparent communication of application programs between processing elements and to permit system control of reconfigurability in event of failures.

A review of all existing communications buses and protocols determined that none satisfied all the requirements. Synchronous data link control (SDLC)² bus architecture, defined by Bell Laboratories and used by IBM, came closest to satisfying all the requirements and was therefore chosen as the basis for the design.

Distribution of the executive software permits the use of multiple processors to solve the various computational tasks in the system. Since the executive is modular, only those portions required in each element reside in that element. The foundation for the executive is the AN/UYSK-20 SDEX-20³. Extensions to the design incorporate multiprocessing and transparency of application program interfaces in the distributed system.

Configurability and flexibility for a wide range of applications were achieved by designing a standard set of hardware, firmware, and software modules that are expected to reduce development, procurement, and logistics costs. Although the primary goal was distributed processing, implementation of conventional existing computer systems was also required from the common, standard set of hardware modules. Applications range from small, field-deployed, tactical systems to large command, control, and communications (C³) systems.

Major criteria in realtime military applications are availability of the system to perform as required and ability to operate in a variety of degraded modes in which failed hardware has little or no effect on system capability. Three factors determine availability: reliability, maintainability, and survivability (or integrity/reconfigurability). Unit reliability can generally be enhanced by derating of components for high temperature operations and other such well-understood procedures. *(continued on page 21)*

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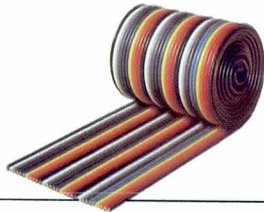
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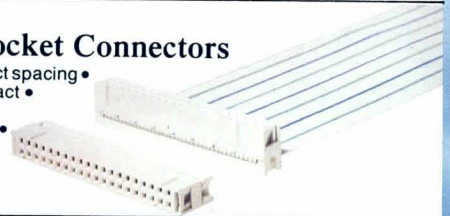
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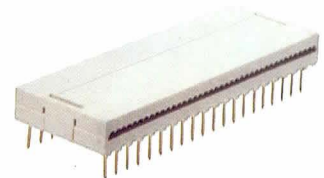
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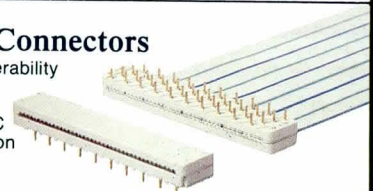
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Most important of all is the necessity to develop a system that enables orderly transition from existing systems to those using the new concepts. The design permits the addition of new DPS equipment, which will initially provide enhancements, extensions, and interconnections, to the existing subsystems. As old equipment is phased out, the functions can then be moved into the new elements/processors provided by the DPS.

System Configurations

In the Litton DPS concept, processing capability at a node ranges from a single CPU to a large multiprocessor. In its simplest form a node is called an element. Fig 1(a) shows a single CPU element, Fig 1 (b) a multiple CPU element. A standard internal bus, called the intra-element bus (IEB), is the heart of the element, and is identical for all DPS emulators. This standardization permits multiple computer architectures with a small number of card types.

The configurations shown have one or more CPUs, memory units, and several input/output (I/O) interface cards, one of which is an interface with the serial interelement bus (SIB). Memory may be accessible by all CPUs or dedicated to support a single CPU; the configuration is totally up to the system designer. I/O cards provide interface to peripheral devices that have been designed for interfacing with one of the several standard interfaces currently in use in military computer systems. Three such cards are operational and provide interface for the 188-C/RS-232, 1397-A, and 1397-B/C. Each card handles two channels.

Another configuration possible with the DPS shown in Fig 2 is defined as a cluster. The memory management function provides interface of two elements per memory management card. The memory management card can be cascaded in two ways: to increase the number of elements that have access to common memory, and to increase the number of ports provided to common memory. A logical and functional limit of 32 elements and 8 ports has been established. The memory management also provides the capability to implement more conventional existing systems where multiple processors are required to share common memory.

The memory management card can implement interrupts between the various CPUs within each of the elements and simplify communication among the processors. Full interrupt capability between processors within an element is also provided. Since multiple processors are permitted within each element, memory management is provided with four full sets of paging and memory protection registers.

Beyond the relatively simple element and its combination into more complex clusters, elements and clusters may also be tied together using the SIB. Fig 3 shows a large distributed system, configured for a typical military application. All elements and clusters are interconnected to permit

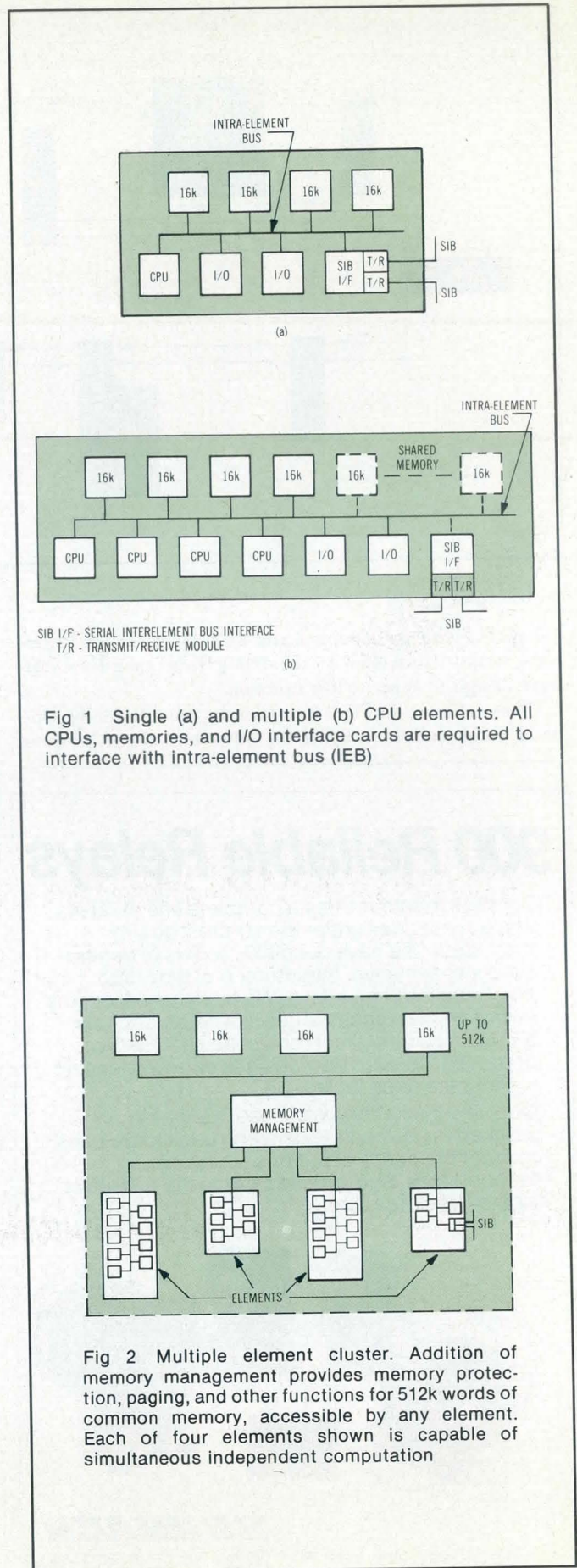


Fig 1 Single (a) and multiple (b) CPU elements. All CPUs, memories, and I/O interface cards are required to interface with intra-element bus (IEB)

Fig 2 Multiple element cluster. Addition of memory management provides memory protection, paging, and other functions for 512k words of common memory, accessible by any element. Each of four elements shown is capable of simultaneous independent computation

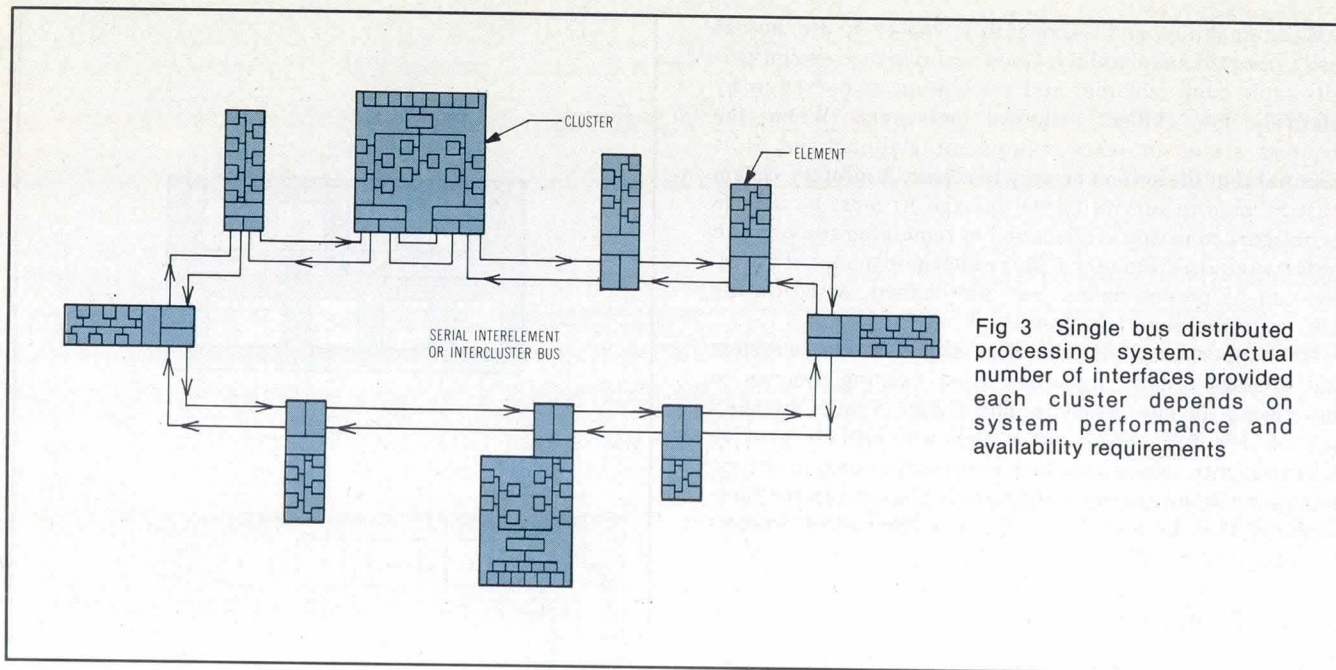


Fig 3 Single bus distributed processing system. Actual number of interfaces provided each cluster depends on system performance and availability requirements

complete exchange of control and data. Hardware and firmware support provided by the DPS greatly simplifies software design to support this function.

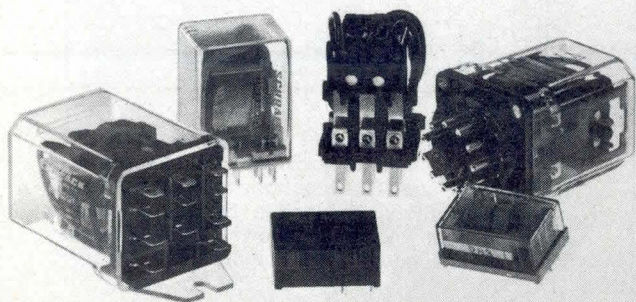
Clusters shown in Fig 3 interface the SIB differently. One has a single interface, while the other has two of its three

elements interfacing the SIB. This configuration was chosen because of the criticality of the functions being performed by this particular cluster. Interconnection to multiple loops is the final possible expansion of clusters and elements. Fig 4 shows the use of a cluster for a 3-bus interface.

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The resulting DPS bus design exhibits characteristics including dual-loop redundancy with continuous loop monitoring to permit automatic reconfiguration; reassignable bus controller function to preclude single-point failure of the bus; and direct element to element addressing. It has four addressing modes: 192 unique addresses, six collective addresses, a global address for all elements, and a bus controller address. Other design characteristics are two interchangeable types of transmission media (fiber optics and coaxial cable), support for system bootload and remote bootload request capability, and provision for multiple bus systems. At a 20M-bit/s transfer rate, there is self-determination by each node for bus address. Dual loop redundancy, automatic reconfiguration, reassignable bus controller, and replicated bus access logic all combine to eliminate the possibility of a single failure bringing down the entire system.

The SIB consists of a primary loop for data and a secondary loop for backup. Failures are automatically detected and the bus automatically reconfigured for complete

(continued on page 26)

FAIRCHILD

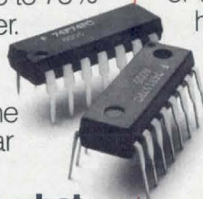
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capability in excess of 120 MHz. We have an ALU that's 40% faster than its Schottky counterpart, yet requires only 1/3 the power.

If you need a high-speed shift register, ours has a shift frequency of 150 MHz. Or an octal latch that has a propagation delay of less than 4 ns. An octal buffer with 1/2 the power of its Schottky counterpart and full 64 mA drive capability. Plus six gates to help put them all together.

When you want it fast, we've got it.

We've been shipping FAST parts for over a year. To order any of our

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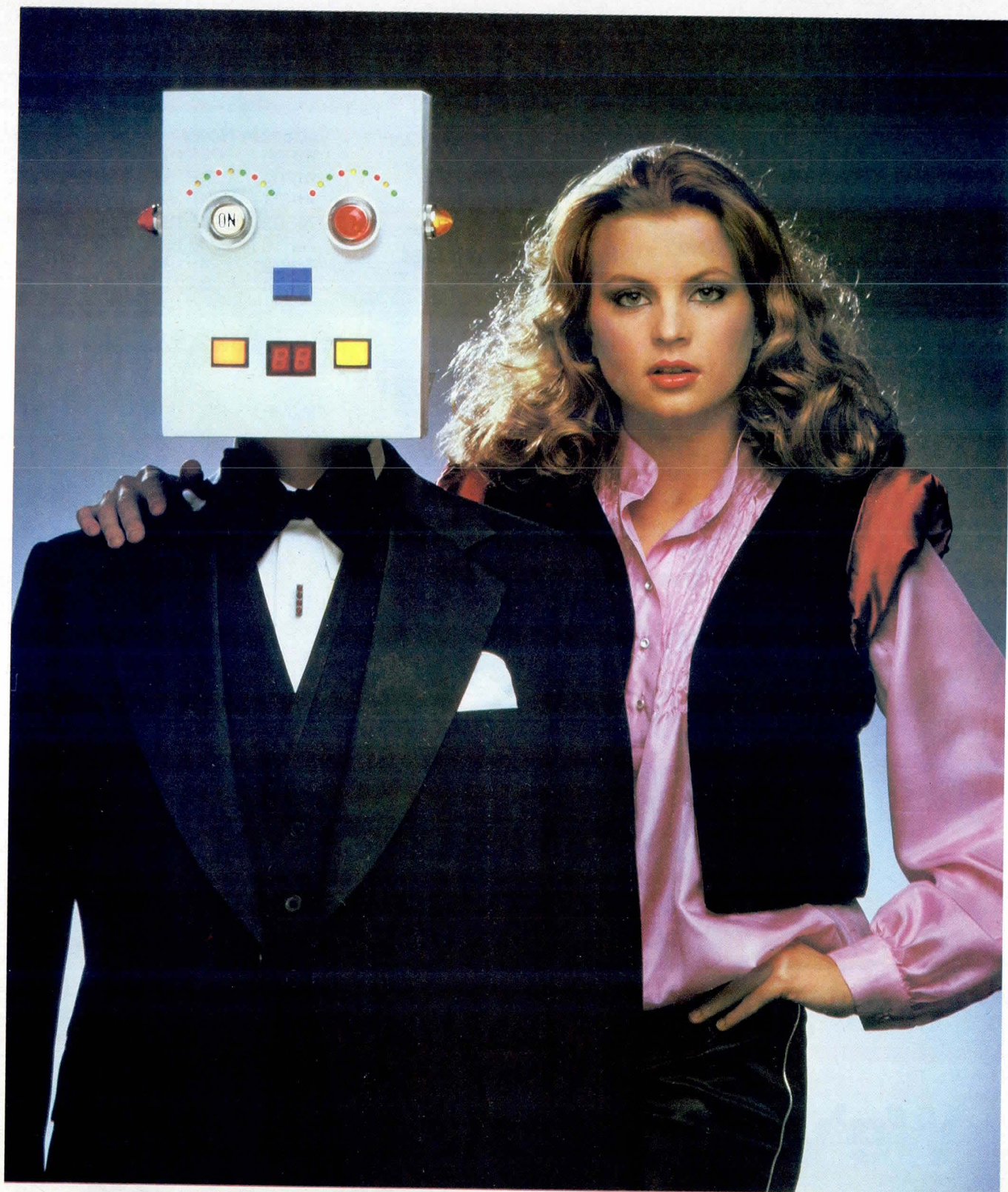
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We've been in high speed to get FAST on the shelf.

CIRCLE 16 ON INQUIRY CARD

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SUCCESSFUL FRONT PANELS DRESS IN DIALIGHT.

Even the most demanding industrial designer or design engineer will occasionally take switches, indicators and optoelectronics for granted. That's a mistake. Because they are often the first components people see and the ones they use most frequently.

That's why so many designers insist on Dialight standard products and custom designs. They know that precision Dialight products will give their computer, machine or instrument the look and feel of quality.



Choose from over 1,500,000 indicator lights.

Dialight is the world's largest manufacturer of incandescent, neon and LED indicator lights. For over 40 years we've introduced new sizes, styles and colors.

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Our rocker and toggle line contains a wide selection of actuators,

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If our catalog doesn't show exactly the switch you need, we'll design and build it to order. All it takes is a call to our Applications Engineering department.

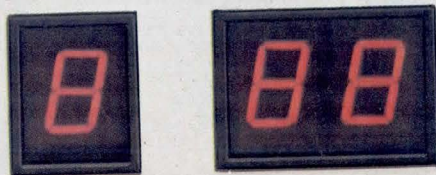


100% testing of every illuminated switch.

Dialight offers a complete line of computer-grade illuminated switches at reasonable cost. And to make sure they all work perfectly, we test every switch both electrically and mechanically before it's shipped.

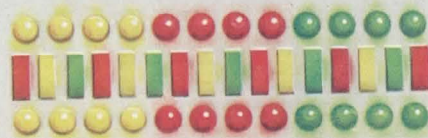
Other switch suppliers may settle for sample testing. That's like leaving reliability to chance. You don't take chances with your designs, and we never will with our illuminated switches.

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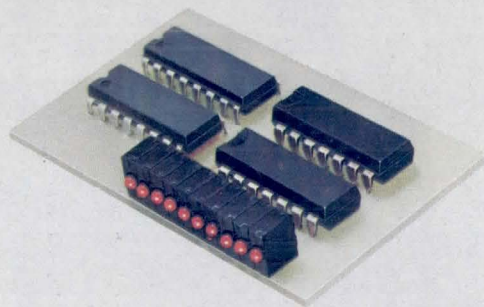
LEDs ready to mount on panels and printed circuit boards.

When it comes to optoelectronics, once again Dialight offers a wide



selection plus many unique advantages. For example, we now package LED indicators singly and in arrays for mounting on PC boards. As soon as you insert them into the board, they're precisely positioned and ready for wave soldering. Installation is far faster. And production costs are dramatically reduced.

For front-panel LED readouts, we package 7-segment displays with their associated decoder-driver circuitry and mounting bezel. The entire assembly, with as many digits as you need, is ready for instant panel mounting.



Dress your products for success.

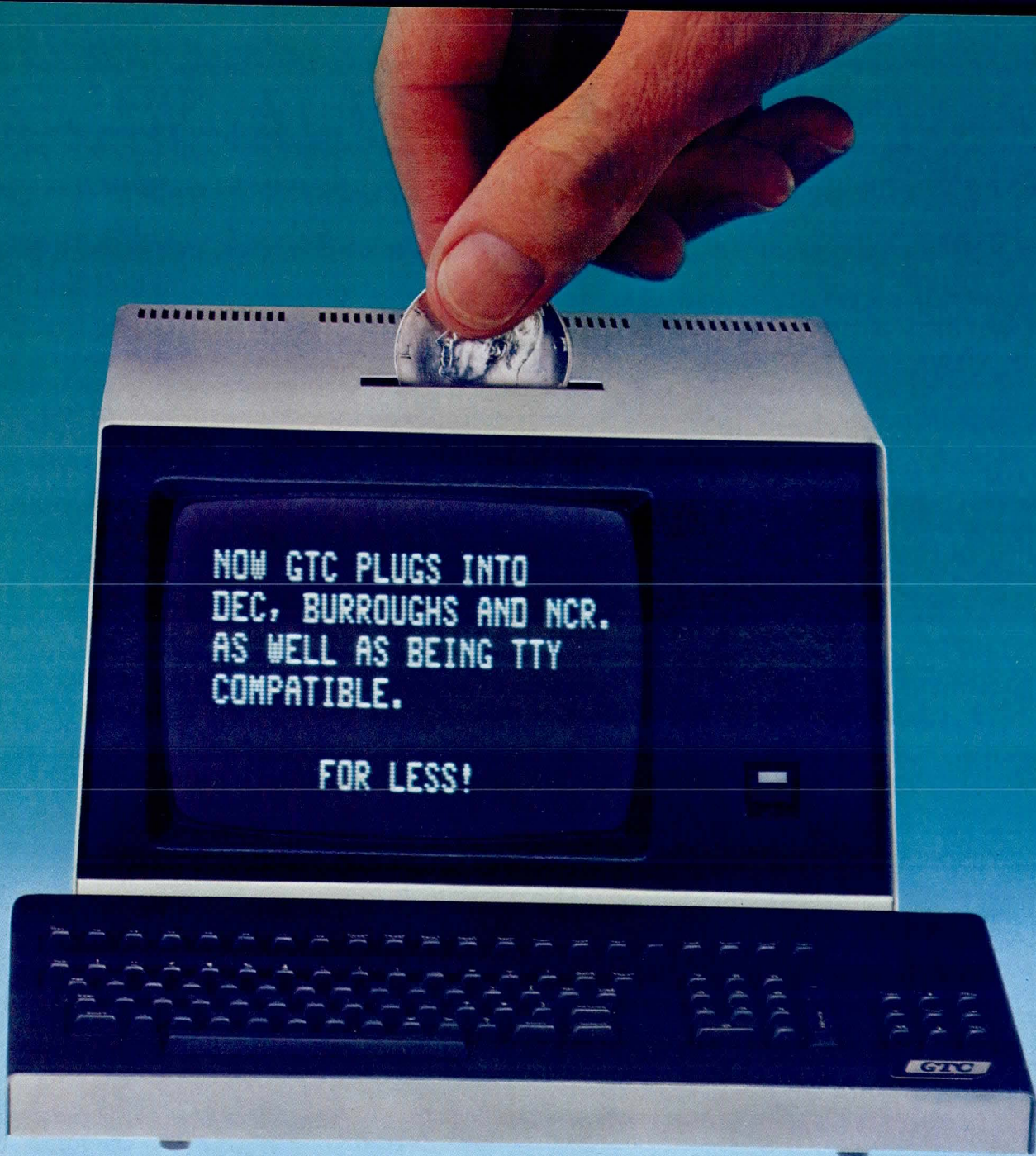
Your products never get a second chance to make a good first impression. So send them into the marketplace looking their best. Dress all your front panels and PC boards in quality indicator lights, rockers and toggles, illuminated switches and optoelectronics from Dialight.

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OUR AUTOMATIC SAVINGS PLAN.

Plugging in our line of interface-compatible terminals can automatically reduce your terminal budget—by as much as 50%. And nowadays, that's like money in the bank.

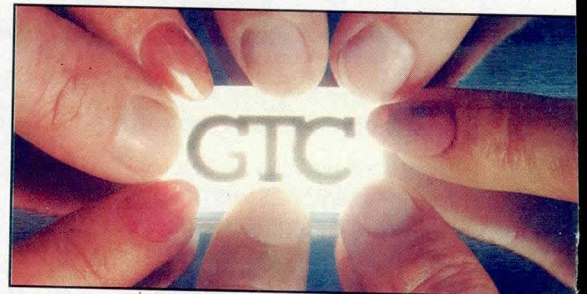
General Terminal Corporation offers models that are teletype-compatible as well as terminals that are interface-compatible with DEC, Burroughs and NCR computers. And GTC offers models that emulate other major terminals, too. All for less.

And because GTC is the only major terminal manufacturer with production facilities on both U.S. coasts, we can

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More for less, automatically. That's what happens when you push the right button.

For more information on GTC products and services, call toll-free today. In California: 800-432-7006. Anywhere else in the United States: 800-854-6781. Ask for Georgia Sand. Or write Georgia Sand at General Terminal Corporation, 14831 Franklin Avenue, Tustin, CA 92680. Telex: 910-595-2428. We have offices throughout the world. In Canada, contact Lanpar Ltd., 85 Torbay Road, Markham, Ontario L3R. Phone: 416-495-9123.



The right button to push.™

General Terminal Corporation

CIRCLE 18 ON INQUIRY CARD

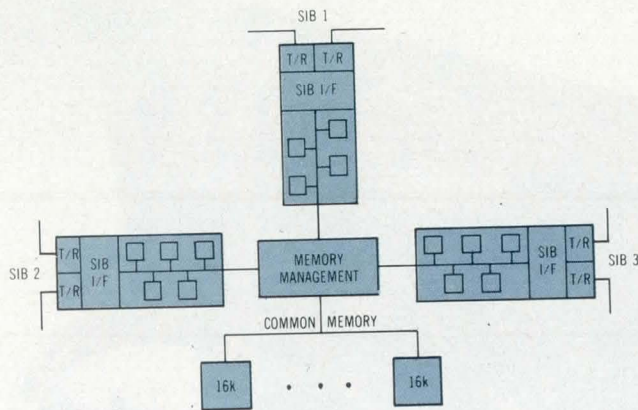


Fig 4 Multiple bus interface cluster. Each element is tied to different bus allowing totally independent and asynchronous operation of all three buses

fail-safe operation. The bus controller, which may be any node on the bus, continually monitors bus operation for abnormal conditions. A backup bus controller is also assigned, whose task is to monitor both the bus and the bus controller, and to assume control when it determines that the normal controller has failed. Control logic for bus access is fully replicated and independent in each node. Since all nodes in the DPS have processing capability, direct addressing of a message from one non-master node to another is permitted. The SIB protocol eliminates the double transmission, store and forward approach, resulting in very high efficiency. The large set of address categories provided by the SIB maximizes system throughput, and the global and device collective categories permit single transmission of a message to multiple destinations.

Both fiber optics and coaxial cable are available as transmission media for cost-effective implementation in a wide variety of applications; implementation of the bus may be in any combination of the two. Transmit/receive (T/R) assemblies at the nodes are modularly designed to permit this choice at any location in the loop. System bootload permits automatic loading and distribution of programs and data to all elements of the system from a single mass storage device. Remote bootloading permits the bootload of any node that is being added or reinserted into the system from one mass storage device, eliminating the need for the bootload media at every element.

Ready expandability of the DPS to multiple bus operation is a significant attribute. In a very large combat system, it is desirable to have several separate buses, organized on a functional basis. This approach provides autonomous subsystem design, rapid response in the sensor to weapon chain, and enhanced survivability. This configuration requires a protocol that permits efficient interbus communication. A simple and natural extension of the already

developed SIB protocol for a single bus communication was selected. This design approach permits continued use of that hardware, firmware, and software without modification while minimizing additional software required for the additional capability. No change is required to either the hardware or firmware for the implementation of the interbus communication.

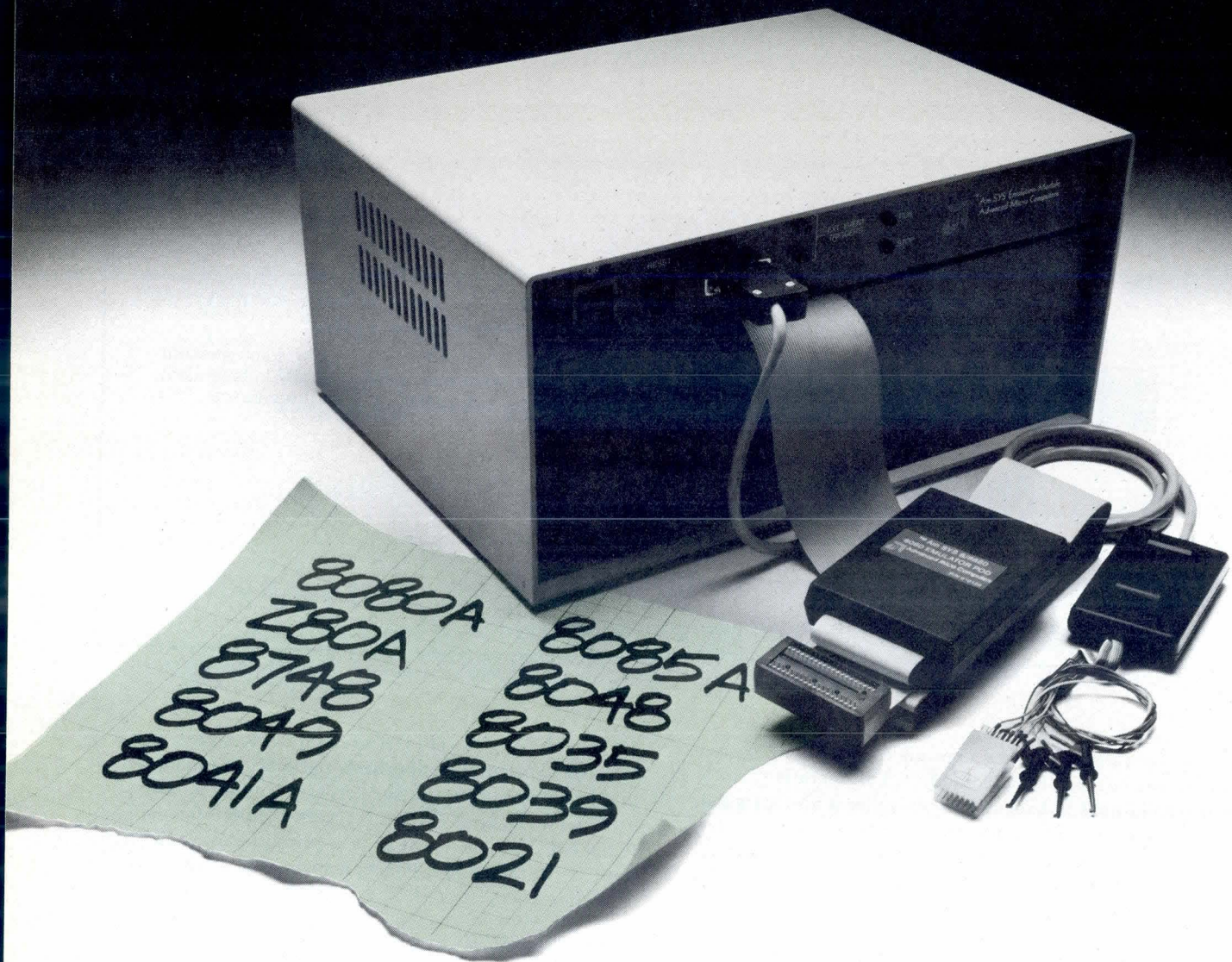
Data Processing

Hardware. Most of the general purpose digital computers currently used by the U.S. military are the AN/GYK-12 and AN/UYK-19 (Army), and AN/UYK-20 and AN/UYK-7 (Navy). In addition, the AN/UYK-41 has been recently designated a U.S. Army standard by the Military Computer Family⁵ program. Therefore, these architectures were chosen as targets in the development of emulation hardware. Software compatible, low cost, low throughput devices are also called for.

Although computer architectures differ greatly, it is possible to implement all CPUs with a small set of standard circuit card types. Commonality is also carried into the memory system since all five computers use identical complementary metal oxide semiconductor (CMOS) memory cards, either 16k words by 18 bits or 8k words by 36 bits. This modularity for each of the computer memory configurations permits cost-effective implementation of smaller computing units and facilitates growth to maximum sizes. Modular approach results in the need for only 10 types of circuit cards to implement five different CPU architectures, including memory. Logistics advantages of this design are obvious.

Software. DPS software provides three major functions: system initialization, system control, and local control. System initialization permits bootloading and system start-up of all processors from a single initiation point. Programs required by all processors reside in a single mass memory

(continued on page 30)



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ONE BOX.**

Announcing the RTE8/8800 Real-Time Emulator.

RTE8/8800 is modular. For each CPU you work with, you just plug in one of our "personality modules." We have them for 10 of the industry's most popular 8-bit microprocessors.

Your basic emulator CRT format stays the same. So does your emulation command set. You'll be able to debug your hardware and software, test and analyze your target system prototypes cheaper and easier than ever before.

And you'll do it all in *real* Real-Time. Because our emulator has its own high-speed memory. (Not just

shared development system memory.) *But that's not all.* RTE8/8800 also has its very own control microprocessor. It can continue testing and exercising target hardware and software while you and your development system go off and do something else.

And even though the RTE8/8800 is hard to beat, it's easy to use. You don't have to spend a lot of time learning long complex command syntax. Simple keystroke commands control the menu-oriented display.

Get System 8/8 with RTE8/8800 from Advanced Micro Devices. After all, you work with more than one CPU. Shouldn't your emulator?

(System 8/8)



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Right, From The Start.

bootload medium, which may be replicated. The system bootload function loads a system initialization program into the processor to which the bootload medium is attached, establishes bus operation, and interrogates all nodes for status. CPU-resident firmware at each node responds with a status message that identifies the operational capability of that node.

Status messages are compared against a system configuration table to determine if all expected capabilities are operational. A display at the bootloading node informs the operator of system status; only operational elements will be bootloaded. The appropriate programs for each processor will be retrieved from mass memory and shipped via the SIB to that processor. After all processors have been loaded, the bootload processor will load its own operational software and initialize the system for operational use.

System control software will perform the following functions once the system has been initialized: monitor performance of the bus and all processors on a periodic basis with fault recovery and degraded mode routines; return to normal operation when a unit that has been previously removed for maintenance is restored to the system; and perform the bus controller function. Since the system has been designed to permit reassignment of the bus controller function to any of the elements, this software must be capable of executing in any element. However, it is expected that it will be resident only in the bus controller element and in the element that has been designated as the backup bus controller.

Local control software, replicated in every processor, is based on the currently available AN/UYSK-20 SDEX-20 operating system. Portions of SDEX-20 not applicable to

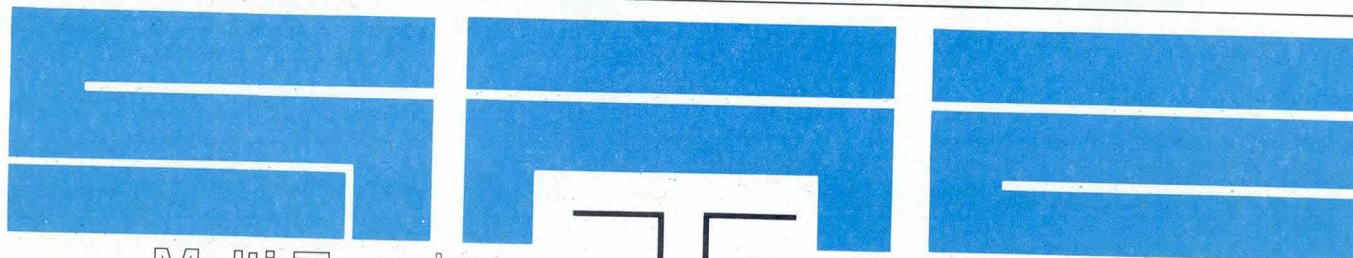
distributed processing were removed, and modules required for these functions were added.

Local software performs such functions as task scheduling, mass media device handling, and interface with displays, terminals, and peripherals. A key function performed by the local executive is recognition of availability of requested resources. When an application program requests a resource not available locally, the local executive determines where in the system the resource resides, prepares a message, and passes control and the message to the appropriate system control module. This enables coding of application programs without knowledge of the actual physical location of the required resource.

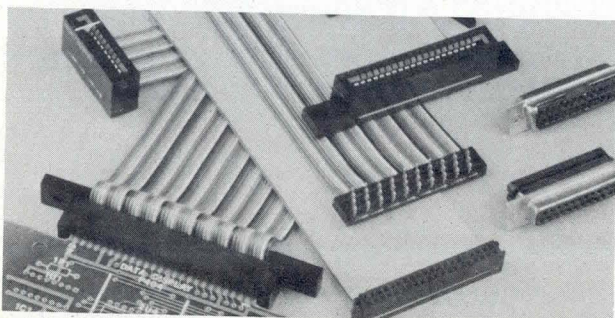
Details on the tradeoffs, design rationale, and SIB operating characteristics are provided in next month's column.

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1. "Product Function Specification, Data Processing Set AN/UYSK-20(V) and AN/UYSK-20X(V)," Specification No SB-10160, 7 Feb 1973
2. R. A. Donnan and J. R. Kersey, "Synchronous Data Link Control: A Perspective," *IBM Systems Journal*, No 2, 1974, pp 140-162
3. "User's Handbook for AN/UYSK-20(V) Computer Support Software," NAVEXLPub 0967-LP-598-2020, Vol II
4. E. T. Nakahara and R. Mauriello, "Data Bus Communications for a Distributed Processing System," *Proc IEEE Advances in Systems Technology Conference*, May 1979, pp 19-27
5. A. H. Coleman and W. R. Smith, "The Military Computer Family: A New Joint Service Approach to Military Computer Acquisition," *Computer*, Oct 1977, pp 12-15



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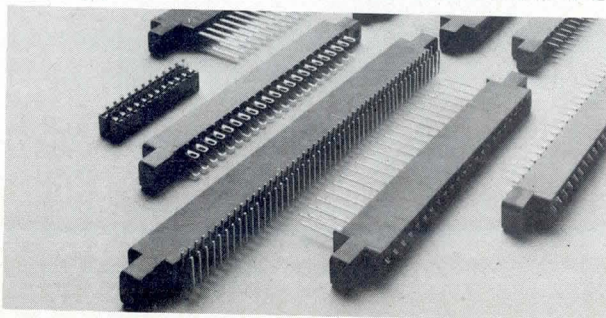
SAE's Multi-Term line of IDC connectors and cable offer a tremendous variety of mass termination components and options including jumper assemblies and cable harnesses.

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At last, there's a multi-user micro-computer system designed and built the way it should be. The CompuStar™. Our new, low-cost "shared-disk" multi-user system with mainframe performance.

Unlike any other system, our new CompuStar offers what we believe to be the most practical approach to almost any multi-user application. Data entry. Distributed processing. Small business. Scientific. Whatever! And never before has such powerful performance been available at such modest cost. Here's how we did it . . .

The system architecture of the CompuStar is based on four types of video display terminals, each of which can be connected into an auxiliary hard disk storage system. Up to 255 terminals can be connected into a single network! Each terminal (called a Video Processing Unit) contains its own microprocessor and 64K of dynamic RAM. The result? Lightning fast program execution! Even when all users are on-line performing different tasks! A special "multiplexor" in the CompuStar Disk Storage System ties all external users together to "share" the system's disk resources. So, no single user ever need wait on another. An exciting concept . . . with some awesome application possibilities!

CompuStar™ user stations can be configured in almost as many ways as you can imagine. The wide variety of terminals offered gives you the flexibility and versatility you've always wanted (but never had) in a multi-user system. The CompuStar Model 10 is a programmable, intelligent terminal with 64K of RAM. It's a real workhorse if your requirement is a data entry

or inquiry/response application. And if your terminal needs are more sophisticated, select either the CompuStar Model 20, 30 or 40. Each can be used as either a stand-alone workstation or tied into a multi-user network. The Model 20 incorporates all of the features of the Model 10 with the addition of two, double-density mini-floppies built right in. And it boasts over 350,000 bytes of local, off-line user storage. The Model 30 also features a dual drive system but offers over 700,000 bytes of disk storage. And, the Model 40 boasts nearly 1½ million bytes of dual disk storage. But no matter which model you select, you'll enjoy unparalleled versatility in configuring your multi-user network.

Add as many terminals as you like - at prices starting at less than \$2500. Now that's truly incredible!

No matter what your application, the CompuStar can handle it! Three disk storage options are available. A tabletop 10 megabyte 8" winchester-type drive complete with power supply and our special controller and multiplexor costs just \$3995. Or, if your disk storage needs are more demanding, select either a 32 or 96 megabyte Control Data CMD drive with a 16 megabyte removable, top-loading cartridge. Plus, there's no fuss in getting a CompuStar system up and running. Just plug in a Video Processing Unit and you're ready to go . . . with up to 254 more terminals in the network by simply connecting them together in a "daisy-chain" fashion. CompuStar's special parallel interface allows for system cable lengths of up to one mile . . . with data transfer rates of 1.6 million BPS!

Software costs are low, too. CompuStar's disk operating system is the industry standard CP/M*. With an impressive array of application software already available and several communication packages offered, the CompuStar can tackle even your most difficult programming tasks.

Compare for yourself. Of all the microcomputer-based multi-user systems available today, we know of only one which offers exactly what you need and should expect. Exceptional value and upward growth capability. The CompuStar™. A true price and performance leader!

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CIRCLE 21 ON INQUIRY CARD

The intelligent disk architecture in STC 2700 Series Disk

STC's new 2700 winchester disk family combines the intelligence of a micro-processor, 64 Kbytes of RAM, and a high-speed bus interface to offer you a versatile new disk architecture. An architecture that can help you achieve new dimensions in system effectiveness. Relieve CPU overhead burdens. Slash interfacing costs, and more.

Yet, even without its advanced architecture, you'd still choose the 2700 disk family for its attractive price/performance and reliability values.

The 2700 family features formatted capacities of 39, 91 and 195 Mbytes, 27 msec average seek time, and an OEM price of less than \$5,000 (195 Mbytes). With a predicted 8000 hour continuous

operation MTBF, the 2700 will not just keep your customers happy--it will keep your warranty expenses low.

Powerful bus architecture for faster data rates and greater flexibility.

Gone are the speed and configuration constraints of serial, synchronous data-line interfacing. The 2700 disk family incorporates a high-speed, byte-parallel asynchronous interface, with internal serial/parallel conversion, to give you transfer rates up to 2 Mbytes/sec. The full handshake protocol and built-in dual ports support radial, daisy chain or intermixed configurations.

The μ p can unlock your system's hidden resources.

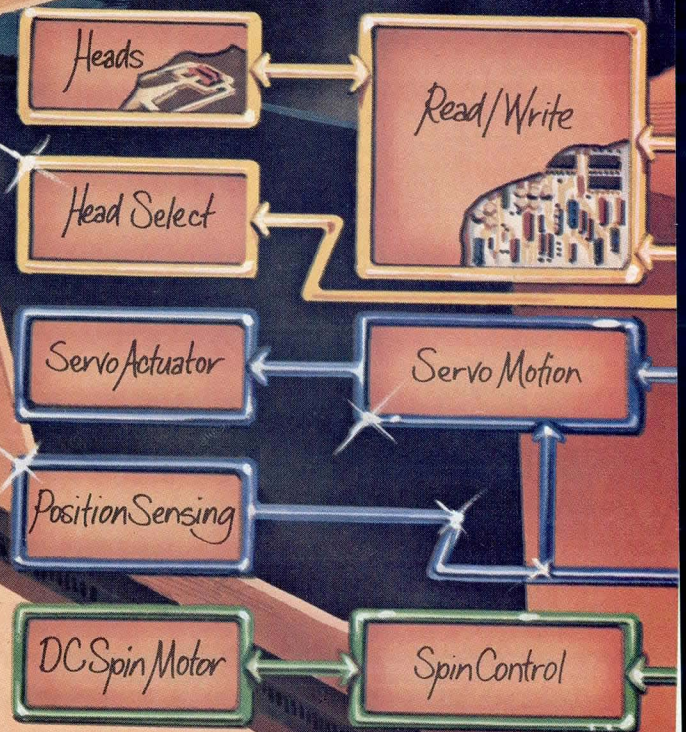
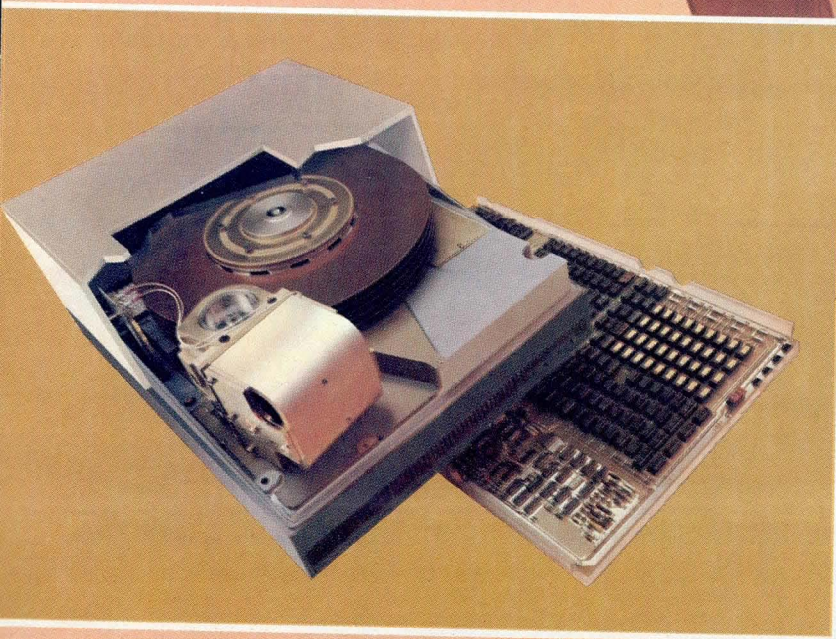
One way to boost your CPU's performance is to get it out from under system overhead and back to productive

computing. The on-board intelligence of the 2700 gives you that capability. Routines such as drivers, data management and utilities can be offloaded to the micro-processor, freeing the CPU and bus for other tasks. But that's only the beginning.

High-level software, including on-board editor and compiler, simplifies algorithm development for custom applications. And you can use the built-in RS-232 port to program right on the disk.

An intelligent controller in each drive. For free.

To help you get to the system level faster and easier, we placed most of the



of tomorrow is shipping today... Drives.

traditional controller functions within the 2700. This includes address mapping, defect management, error detection/error recovery procedures and all device-dependent functions. Since you now only have to build a low-cost interface adapter — your attachment costs are significantly reduced.

Low cost of ownership.

Fewer parts mean fewer failures. So the 2700 contains a minimum number of mechanical parts, only three of which move: spindle, actuator and power system fan. The microprocessor contributes

to this simplicity by replacing all sequencing and servo logic with firmware.

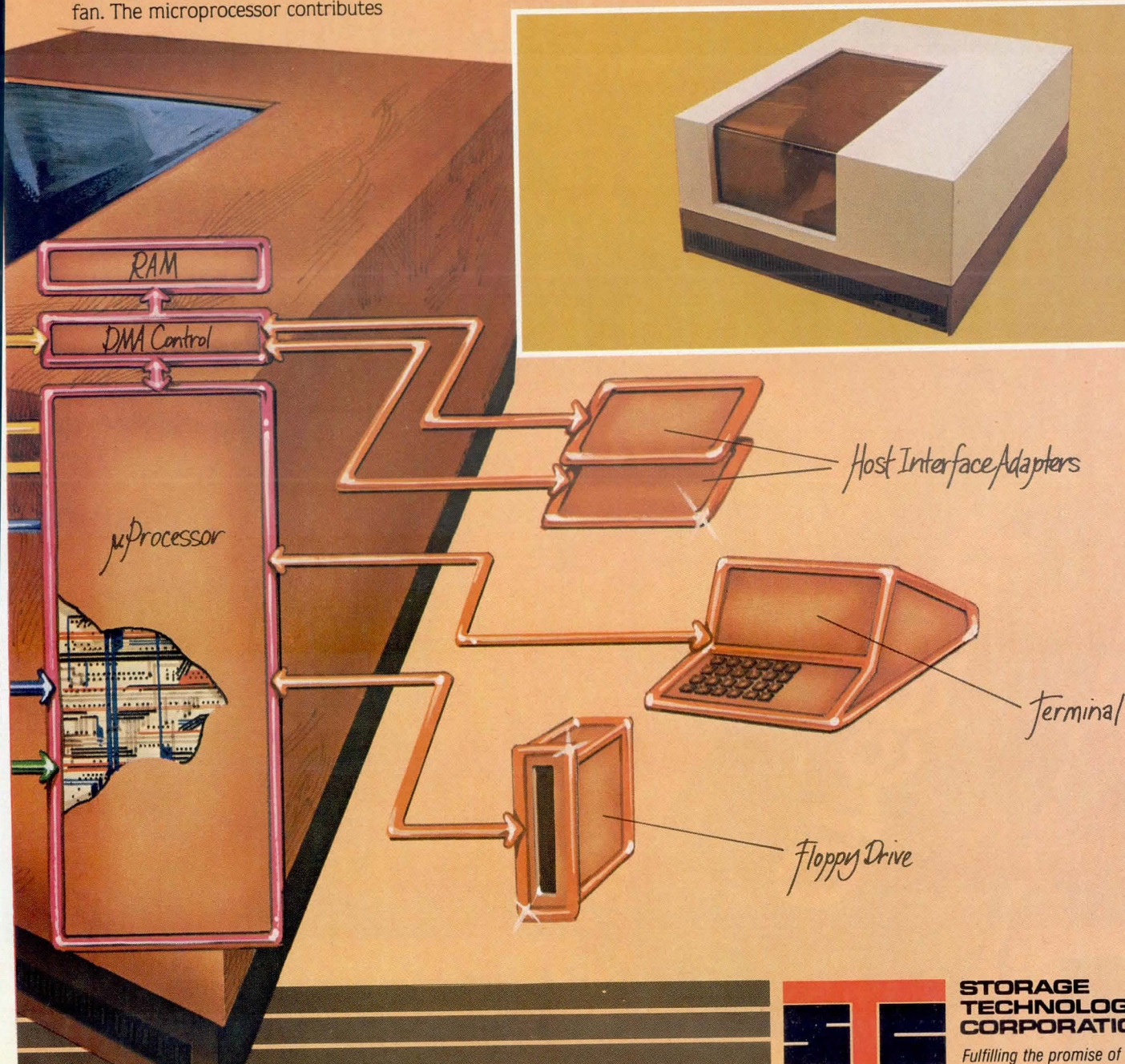
To eliminate scheduled maintenance, the 2700 dispenses with potentiometers. Dynamic adjustments are made internally under microprocessor control. And the 2700's closed-loop air system means no filter changes.

If there's ever a failure, internal diagnostics isolate the problem to one of three subassemblies: logic board, head/disk assembly or power system. And these components uncouple quickly

for fast replacement. All of this translates into high MTBF, low MTTR, to reduce your warranty and field service costs.

To learn more . . .

about tomorrow's disk architecture, today, contact OEM Marketing, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone Frank Gunn at (303) 673-3051. In Canada: Ron Reardon, STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W 5R8. Phone (416) 675-3350.

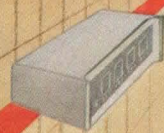
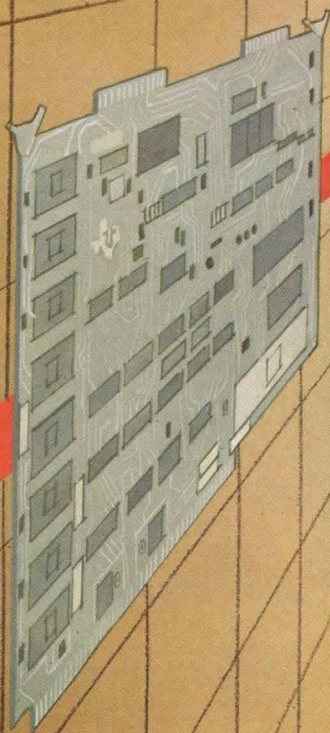


CIRCLE 22 ON INQUIRY CARD



**STORAGE
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Fulfilling the promise of technology.

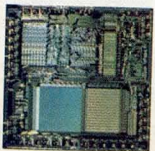


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Single-chip microcomputer

*Evolutionary computing power
from Texas Instruments continues with
a major milestone in 16-bit technology...*



TMS9940

16-bit single-chip microcomputer.

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With the TMS9940, Texas Instruments significantly advances its 16-bit leadership.

With the TMS9940, Texas Instruments expands on what is already by far the industry's most complete 16-bit family. The 9900 Family of microprocessors, microcomputers, peripherals, microcomputer modules and software and hardware development systems, offers a unique software compatibility. So you can move from one product level to another, confidently, protecting your development system and software investment with no need for translators, code converters, etc.

TI's 9900 Family is the *only* family that maintains architectural and software compatibility from single-chips to multi-chips to modules to systems — all the way to the object code level.

With the TMS9940, Texas Instruments brings you high-volume, cost-effective solutions to tough system design problems, combining the computing power of a multi-chip 16-bit system with the reliability and compactness of a single-chip solution.

With its high-speed processing, bit I/O, and advanced memory-to-memory architecture, the TMS9940 offers computation power unequalled by any other single-chip product on the market, while retaining the programming ease of 16-bits.

High-speed number crunching and bit I/O

Powerful instructions — like BCD add, BCD subtract, 16-bit multiply with 32-bit results, and compatible divide — provide a number-crunching capability unsurpassed by any single-chip product.

Thirty-two on-chip, flexible, individually configurable input/output bits are addressable for manipulation by powerful bit I/O instructions.

I/O expansion modes permit up to 256 bits of external I/O to be added, allowing easy interface to 9900 Family peripherals and most industry peripherals.

Advanced memory-to-memory architecture

Advanced memory-to-memory architecture makes the TMS9940 ideal for interrupt-driven and extensive I/O applications.

This innovative architecture features multiple register files that provide ease of programming and unsurpassed interrupt response time.

The TMS9940 memory consists of 128 bytes of RAM and 2048 bytes of ROM. Other features include 4 levels of interrupts, plus an internal decrementer which can be programmed as a timer or event counter.

TMS9940 — Key Features

- 16-bit instruction word
- Instruction set includes 16-bit multiply and divide, BCD add and BCD subtract
- 128 bytes of RAM on chip
- 2048 bytes of ROM (or EPROM) on chip
- 64 general-purpose 16-bit registers
- Program execution from RAM or ROM
- 4 prioritized interrupts
- On-chip timer/event counter
- 32-bits integral general-purpose I/O bits — expandable to 256 external I/O bits
- 4 MHz crystal operation — up to 117,000 interrupts per second
- 5-volt MOS technology
- Offered in a 40-pin, 600-mil DIP

Here-and-now availability

Perhaps just as important as the unmatched capacity for design flexibility, the 9900 Family is here-and-now and readily available. It's the lowest cost 16-bit CPU family. And proven where it counts most. In the marketplace. The choice of hundreds of companies for a wide range of systems and end products.

Microcomputers mean high volume and TI has unequalled production capacity and experience. In fact, TI is the

largest supplier of single-chip microcomputers and has shipped more than the next two suppliers — combined.

9900 Family development tools

Reliable, available, economical development systems designed to boost programmer efficiency and cut costs.

The AMPL* prototyping lab: A complete set of the software and hardware development tools for the TMS9940 as well as for other 9900 Family CPUs. The AMPL system provides a real-time TMS9940 emulator and a logic-analyzer function to solve complex programming and hardware debug problems.

TMS9940E: This EPROM version of the TMS9940 is the ultimate prototyping tool, allowing in-field system check-out, reducing turnaround time and expense for code revisions.

Leadership staying power

TI has paced the industry through generations of semiconductor innovation, pioneering the lion's share of major milestones.

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The continuing introduction of new, advanced 9900 Family CPUs, with TI's state-of-the-art technology and proven production resources, demonstrates TI's total commitment to 16-bit leadership.

That's why you can design with the TMS9940, confident in a family that's a reality today. Confident that the family will grow with your needs to keep your systems competitive at the leading edge of tomorrow's technology.

For more information about the TMS9940, or any other 9900 Family member, contact the TI field sales office nearest you. For details and specifications, write to Texas Instruments Incorporated, P. O. Box 1443, M/S 6404, Houston, Texas 77001.



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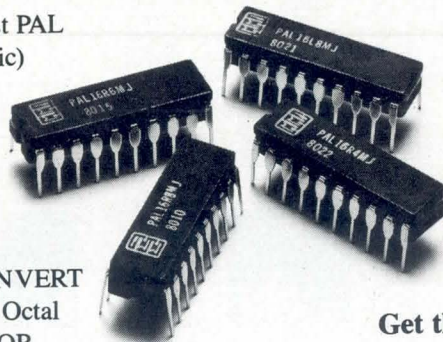


Four new PAL[®] devices join the family that's making TTL logic obsolete.

They're here. Our 4 newest PAL (Programmable Array Logic) devices make a total of 13 in the instant custom logic family that replaces up to 90% of the entire 54/74 S and LS series logic. Meet PAL 16L8, an Octal 16 Input AND/OR/INVERT Gate Array, PAL 16R8, an Octal 16 Input Registered AND/OR Gate Array, PAL 16R6, a Hex 16 Input Registered AND/OR Gate Array, and PAL 16R4, a Quad 16 Input Registered AND/OR Gate Array. And soon MMI will introduce two additional PALs with arithmetic functions.

PAL — The Programmable Solution™
— saves you space, time and aggravation.

A single PAL 20 pin SKINNYDIP™ can replace from 4 to 12 TTL devices. But pc board space isn't all you save. Lower system cost, smaller inventory requirements, reduced parts



count and high-volume, off-the-shelf, multiple sourced availability,* make PALs the most cost-efficient logic devices on the market. And every PAL can be programmed by any PROM programmer with a PAL personality module.

Get the right data book. Free.

For your complimentary copy of the new Bipolar LSI Data Book and further information on the revolutionary PAL logic family, contact your local MMI stocking distributor or sales representative. Monolithic Memories, Inc., 1165 East Arques Avenue, Sunnyvale, California 94086.

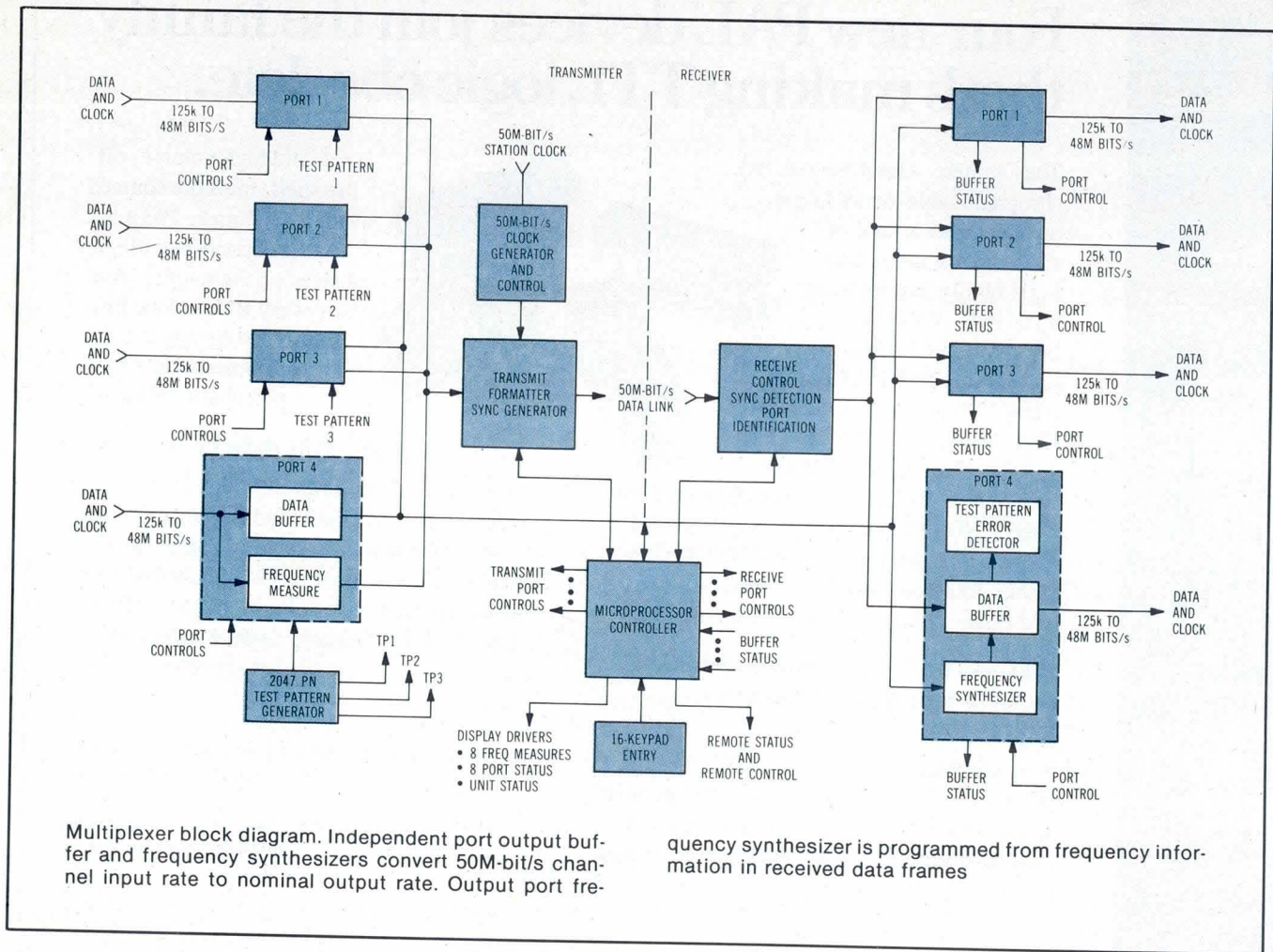
PAL, The Programmable Solution, and SKINNYDIP are trademarks of Monolithic Memories, Inc.

*National Semiconductor Corporation is a licensed alternate source for PAL.

Monolithic Memories 

CIRCLE 24 ON INQUIRY CARD

High Bit Rate Satellite Data Communications Supported by Statistical Multiplexer



Up to four lines of serial synchronous data, each at any bit rate from 100k to 48M bits/s (48M bits/s aggregate) can be multiplexed and demultiplexed by a model 781 statistical multiplexer when connected to a full duplex 50M-bit/s satellite communication channel. The device is an outgrowth of a NASA contract award to Aydin Monitor Systems, 401 Commerce Dr, Fort Washington, PA 19034, to support high rate communications in the space shuttle program.

The multiplexer output can operate slaved to an external primary standard or to the communication channel modem's 50M-bit/s clock. In a free running mode the unit outputs data under control of an internal 50M-bit/s clock that is accurate to within one part in

10⁷. A second identical data and clock port is provided for use by a backup recorder.

A transparent 4-channel data link is made up of a multiplexer/demultiplexer connected in tandem through a communications channel. Output of channel data is continuous and at the same nominal rate as the input. Statistical multiplexing techniques, partitioning input data streams, using control information to format data in equal size blocks, and transmitting data from each port a block at a time based on rate-determined priorities make optimum use of the 50M-bit/s channel bandwidth.

The demultiplexer recognizes blocks or frames by detecting distributed synchronization patterns in the received

data stream. Information is decoded to the appropriate output channel which buffers the data and smooths the 50M-bit/s burst rate input to the nominal channel rate output.

Microprocessor control at the operator/unit interface provides for adaptive assignment of port priorities based on input rate so that the highest priority goes to the highest rate channel. It also detects and compensates for channel output rate variation caused by Doppler effects in the communication link and prevents either loss or interruption of data due to uncorrected differences between measured and actual channel rate.

Circle 517 on Inquiry Card

PENRIL'S DATACOMM SOLUTION

Means Over 25 Modem Products to Choose From...

In selecting the best modem for your data communication system, consider existing equipment compatibility, data volume, data rate, transmission distance and cost. Then choose from our FCC registered modems... compatible with Bell 103, 113, 202, 201, 212 or 208... or CCITT V.22, V.26, V.27, V.29 compatible units for European installation... or our low-cost, short-haul modems for local data communication.

...With Complete User Support.

Before your modems leave our factory, they have been extensively tested and burned-in by our quality assurance team. Once your Penril modems are installed, you choose the field service plan... factory return, on-site service by one of our four hundred service locations or overnight spares delivery. But what really makes the Penril solution unique is our self-contained diagnostics. From the analog and digital loop-back of our 300/1200 modem to the more sophisticated integral network diagnostics of our 2400, 4800 and 9600, Penril modems help you avoid or shorten down-time.

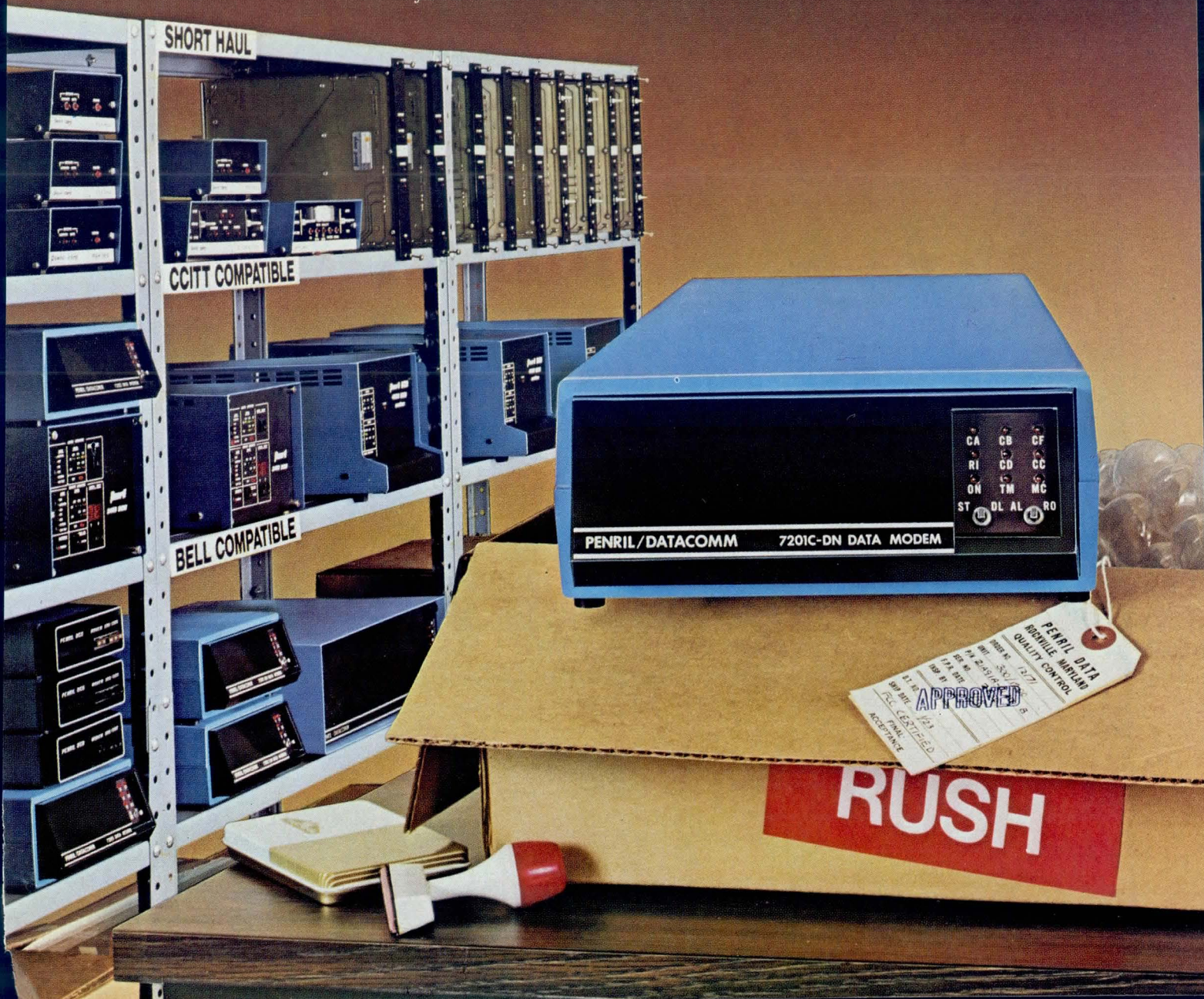
And, Penril Modems Are Competitively Priced and Ready to Deliver.

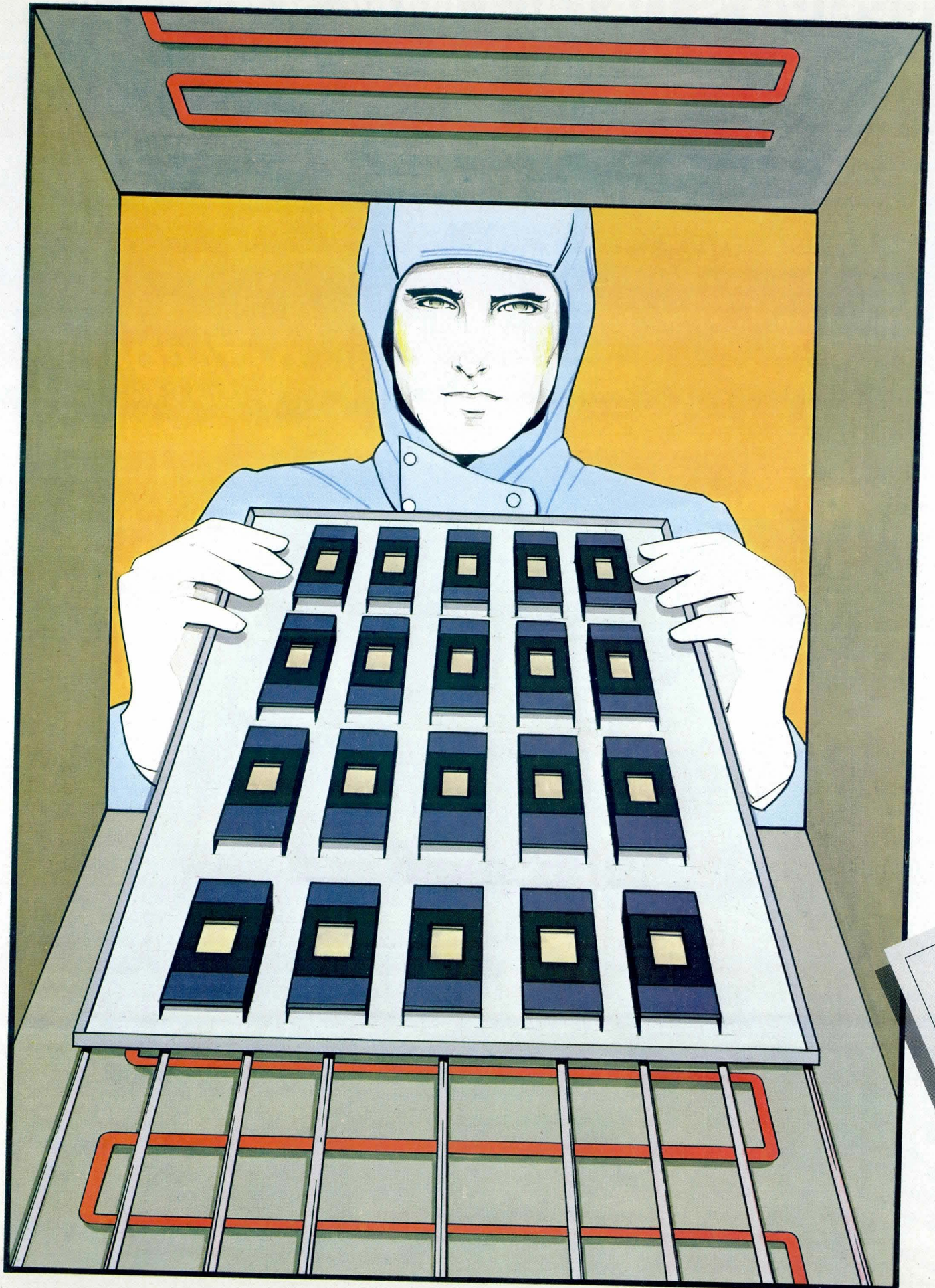
For additional information, call or write Penril Corp., Data Communications Division, 5520 Randolph Road, Rockville, Maryland 20852. 301/881-8151; TWX 710-828-0522.

Penril DATACOMM

... We Still Care.

CIRCLE 25 ON INQUIRY CARD





Cer
,

Recipe for Reliability

Your system is only as reliable as its EPROMs. That's why Intel delivers every 2716 with an Arrhenius Forecast.

All the ingredients in a microcomputer system have to be reliable. But one component is especially critical. Your EPROMs.

How EPROMs protect your "value added."

EPROMs, like our 2716, contain a big part of the value your company adds to its products. EPROMs store the special program that makes your product perform uniquely. And that program typically represents an investment of thousands of engineering hours—and hundreds of thousands of dollars. If program memory fails, your entire system goes down.

Intel invented EPROMs, so we know their importance in your product. In fact, we've delivered over 7 million EPROMs—

more than any other manufacturer. This experience has helped us perfect EPROM technology. And it's the reason we're able to include an Arrhenius Forecast with every shipment of 2716s.

How we make them reliable.

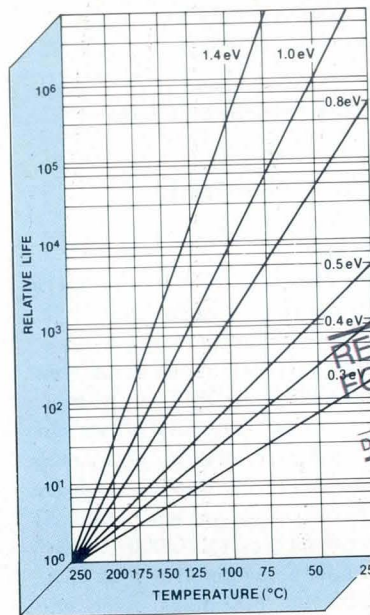
The Arrhenius Forecast you receive with Intel® EPROMs certifies that each

Our Arrhenius Forecast also gives you confidence that you can count on Intel's 2716s for years to come. Our 5 million hours of accelerated life tests prove it. By simulating extended EPROM operation in your system and using Arrhenius extrapolation techniques, we're able to forecast reliable bit storage of today's 2716s until at least the year 2002 A.D.* It's one more example of the steps we take to build safety into your EPROM purchase.

Send for our recipe.

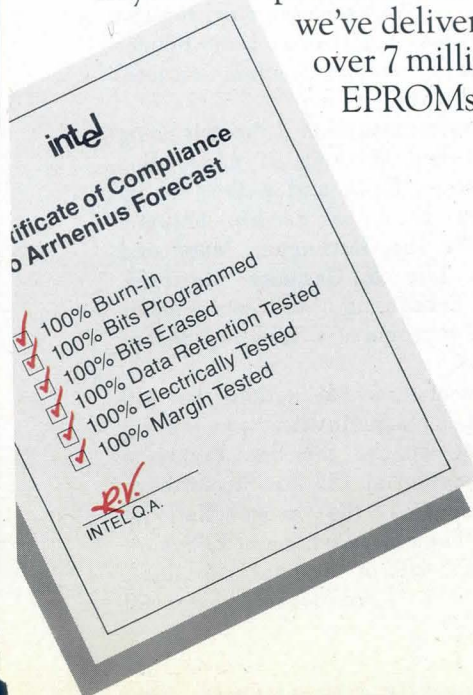
Because your whole system depends on its EPROMs, it pays to insist on an Arrhenius Forecast with every shipment of 2716s. For a complete summary of Intel's latest EPROM reliability study and Arrhenius extrapolation techniques, get our 2716 Reliability Report, RR19. For your free copy, contact your local distributor or Intel sales office. Or write Intel Corporation, Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051. Or call (408) 987-8080.

*Statistical calculation



Arrhenius Plot, above, projects component longevity at different temperatures. By increasing temperatures, Intel simulates extended EPROM operation to predict life expectancy. Such a Reliability Forecast is included in every shipment of Intel 2716 EPROMs.

of 16,384 bits in every 2716 has been tested under extreme conditions. All 2716s undergo six critical tests: burn-in, programming test, electrical test, data retention bake at 150°C, voltage margin test, and erasure testing.



intel delivers.

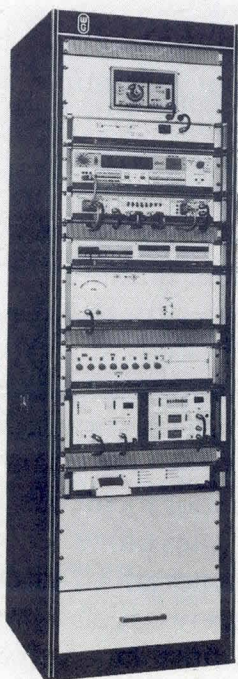
Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

CIRCLE 26 ON INQUIRY CARD

Instrument Provides Half-Channel Testing of μ Law Codecs

Separate, direct A-D and D-A measurements, as well as analog to analog measurements of codecs using the μ 255 encoding law are enabled by the AMS-952 automatic measuring system. According to the manufacturer, W & G Instruments, Inc, 119 Naylor Ave, Livingston, NJ 07039, the system provides the first feasible means by which codec manufacturers can enter a bit stream to make such measurements.

The system is housed in a standard 72" (183-cm) high rack. It is controlled by a Hewlett-Packard 9825S desktop calculator and is comprised of a frequency selective level meter, wideband noise meter, level generator, 4-tone noise source, PCM channel demultiplexer, PCM channel generator,



Automatic measuring system. Codecs are checked by accurate and repeatable measurements of coder and decoder transmission test parameters using μ 255 encoding law

and impedance/switching panel. It can be expanded for card, channel bank, and switch testing, as well as for use with A-Law PCM equipment with a minimum of hardware and software reconfiguration.

Key transmission tests on the codec include signal to distortion ratio (quantizing noise), idle channel noise, level tracking, insertion loss, frequency response, intermodulation distortion, and crosstalk.

Frequency response is measured over the entire voice channel to ± 0.05 dB accuracy. Level tracking measurements from 3 to below -60 dBm0 can be made in steps of 0.1 dB with accuracies to a hundredth of a dB. Signal to distortion values of better than 40 dB are measured, as well as idle channel noise figures below 0 dBmCO. Measurements of the 60-Hz and out of band rejection characteristics are also provided.

When configured for μ Law codecs, the system meets the appropriate recommendations of AT&T Compatibility Specification 43801 and Bell System Publication 41009.

Circle 518 on Inquiry Card

Module Implements Serial Data Link

Another module added to the TM990 family (*Computer Design*, July 1980, p 44) provides interface logic required to implement a long range serial communications link between two or more TM990 systems. The TM990/308 industrial control module (ICM) extends the range of the CPU module and can communicate with an additional 31 308s over distances to 10,000 ft (3048 m) at jumper selectable rates of 1200, 2400, 4800, or 9600 bits/s. Each unit provides an industrial line or RS-232-C interface that can be used with twisted pair or telephone lines, respectively, for long range communications in distributed processing systems.

Available from Texas Instruments Inc, PO Box 1443, Houston, TX 77001, the module communicates in three modes: by serial transmission over the link from one ICM to another; through interrupts between microcomputer and ICM; and by handshaking using the communications register unit (CRU) for byte and status bit transmission to

and from host microcomputer and the ICM. CRU interface is used to transmit data bytes, error codes, and status bits used for handshaking.

The module features jumper selected point to point or multipoint operation. It has a 1k-byte RAM expandable to 2k bytes, and a 2k-byte EPROM expandable to 4k-byte EPROM. A separate RS-232-C interface is compatible with Bell 203 modems. The industrial interface uses isolated (1500-Vrms) differential twisted pair line driver/receiver stages. Hardware cyclic redundancy checking by the onboard TMS 9903 serial I/O controller, and 15 jumper selectable interrupt levels are provided.

The module is compatible with the company's 990 minicomputers and PM550 controllers. It is built on a standard TI 990 format with board dimensions of 11 x 7.5" (28 x 19 cm).

Circle 519 on Inquiry Card

Satellite Network to Test Local Data Distribution Methods

Earth stations owned, operated, and installed by Satellite Business Systems (SBS) of McLean, VA, will be located at sites in San Francisco, Calif, and New York City, NY, to form a demonstration network that will test alternative techniques for local distribution of high speed data in metropolitan areas. In each city existing cable TV facilities will be used for local distribution to user locations at data rates to 56k bits/s. In San Francisco only, the test will include a microwave radio cellular system as another medium for local area distribution.

The demonstration network is being established by SBS; Tymnet, Inc, Cupertino, Calif; and a third entity formed as a partnership between M/A-COM, Inc, Burlington, Mass, and Aetna Life & Casualty, Hartford, Conn. Scheduling of the tests depends on the outcome of a filing now before the FCC.

First of three SBS stations that will provide communications services via satellite will be the San Francisco earth station at 155 5th St, northern data center of the Crocker National Bank. The second will be at El Segundo, Calif, site of the bank's southern

(continued on page 44)

CENTRONICS COVERS THE COURT

...with new, low-priced printers for small businesses

Now small businesses can have the advantage of Centronics performance. We have new models to meet the needs of small businesses — a selection that covers the court. And we've followed-through by pricing them lower than other printers that can't match Centronics' features and reliability.

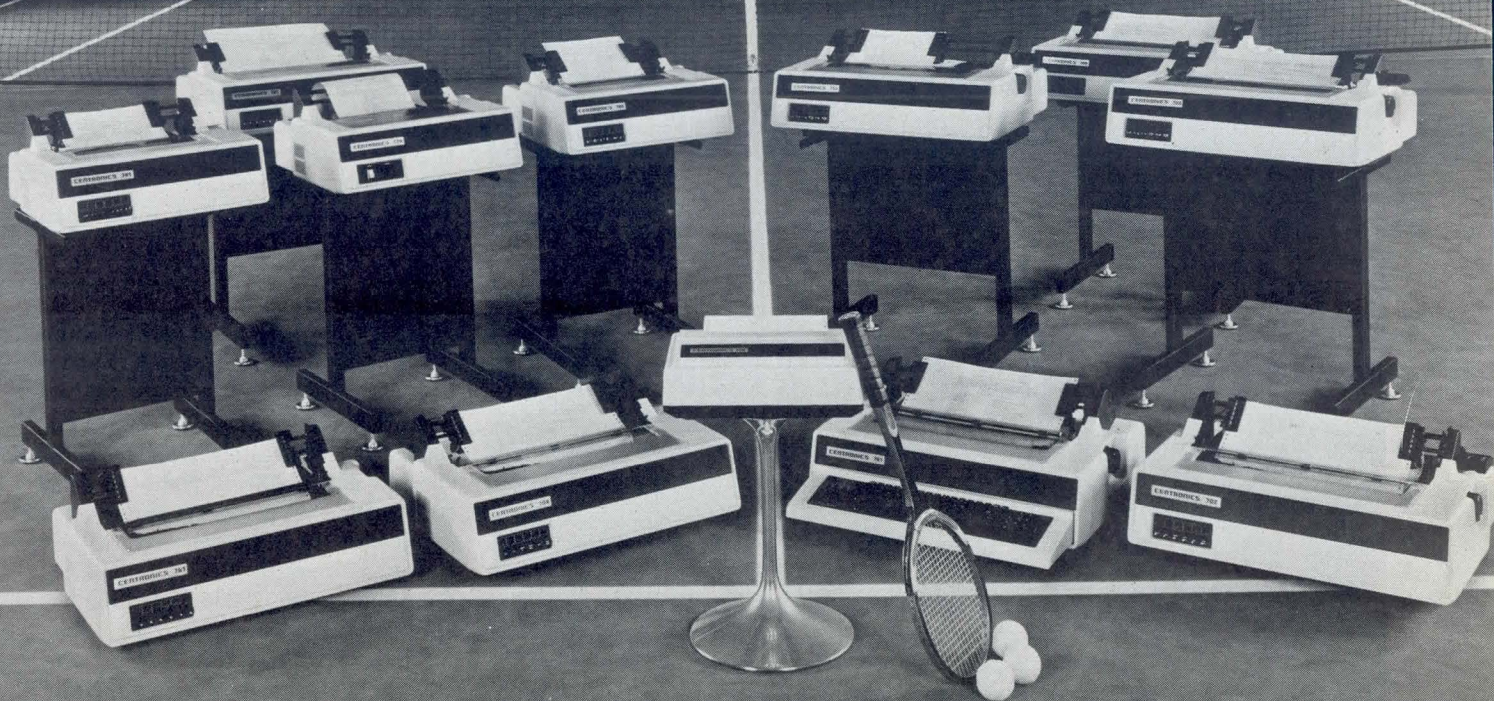
TOP-RANKED TEAM We understand your small business needs — that's why Centronics has sold more printers to the small business market than anyone else. We have new, fully-featured models designed for small business applications. High throughput for inventory control. Full 132-column width for accounts receivable. Versatile forms handling capability for invoicing, payroll, and statements. Plus

excellent print quality for labels and listings. The bottom line: with Centronics, small businesses can have mainframe performance at micro prices.

READY FOR ANY TOUR These printers are designed to deliver maximum in-service time, a key consideration for a small business. And we have the largest worldwide service organization of any independent printer company.

For more information on the 700 Series: call (603) 883-0111, or contact any of our 15 U.S.A. or 9 international sales offices. Centronics Data Computer Corporation, Hudson, New Hampshire 03051.

Always use genuine Centronics ribbons and accessories.



CENTRONICS® PRINTERS
...the advantage

CIRCLE 27 ON INQUIRY CARD

data center, and the third will be in the Wall Street area of New York City.

This system includes relatively small earth stations, most with 5.5-m dish antennas, that can be placed on customer premises. Featuring all

digital high capacity channels, the system enables integration of voice and data communications into a single network and addition of such applications as high speed document transfer and video teleconferencing.

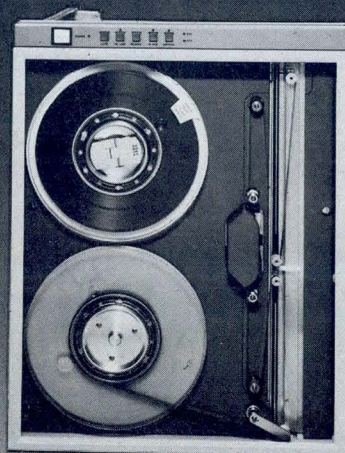
\$3550.

The new 75 ips TDX Series II Tape Drives – Priced from \$3550 in OEM quantities.*

Fully IBM compatible. No program restrictions. Industry standard interface. Patented low inertia tape tensioning system.

*Includes complete 800 or 1600 bpi tape drives in 100 per year quantity. Dual Density 800/1600 bpi version — \$3750.

Contact Tad Richardson for additional details.



TDX PERIPHERALS

Division of GAW Control Corp.
150 New York Avenue, Halesite, NY 11743
(516) 423-3232

IOOC '81 Calls for Papers

The third international conference on integrated optics and optical fiber communication, IOOC '81, jointly sponsored by the IEEE Quantum Electronics and Applications Society and the Optical Society of America, has issued a call for papers. The conference is to be held at the Hyatt Regency San Francisco, San Francisco, Calif, Apr 27-29, 1981, and will provide an interdisciplinary forum for information exchange in the areas of basic research, component development, system engineering, and hardware manufacture.

Prospective authors are invited to submit original papers, not previously presented or published, that describe new technical contributions in such subject areas as

Fibers and cables: Basic waveguide phenomena, fabrication techniques, materials, characterization, installation techniques, reliability testing, and prediction;

Connectors, couplers, equipment, systems, and transmission techniques: Couplers, connectors, splicing techniques, devices, test equipment, transmitter and receiver equipment, modulating and multiplexing formats and techniques, telecommunication and special applications systems, system trends and costs, performance, reliability considerations, and future projections;

Integrated optics and active devices: Dielectric waveguide and optical circuit phenomena, planar waveguide fabrication techniques, passive waveguide devices, integration of optical devices into circuits, applications of integrated optical technology, active waveguide devices, laser diode fabrication and performance characterization, and developmental photodetector progress.

Authors are requested to submit two copies of a separately typed 35-word abstract and a 200- to 500-word summary, with a set of figures suitable for publication to IOOC '81, c/o Optical Society of America, 1816 Jefferson Pl, Washington, DC 20036. Deadline for submission of papers is Nov 28, 1980.

Further information about the technical program may be obtained by writing the Conference Manager, Barbara Hicks, at the above address, or by calling 202/223-8130.



THE NEW PRIMARY SOURCE FOR 16K DYNAMIC RAMs.

Toshiba offers 16K Dynamic RAMs in all three speeds: 150, 200, and 250 nanoseconds. And our actual customer rejection rate is well below $\frac{1}{10}$ of 1%.

But that's nothing new. Toshiba's reputation for quality has been well-known for years.

For that matter, so has our reputation for quantity. And now we've got more to back it up with than ever before.

We've got a new manufacturing plant in Sunnyvale, California. And the capacity to deliver a wide variety of memory and microprocessor products. Send for your free "Memory and Microprocessor Product Guide."

Like NMOS and CMOS static RAMs, EPROMs, and microprocessors.

Remember.

We don't plan on being a primary source by offering second-rate service.

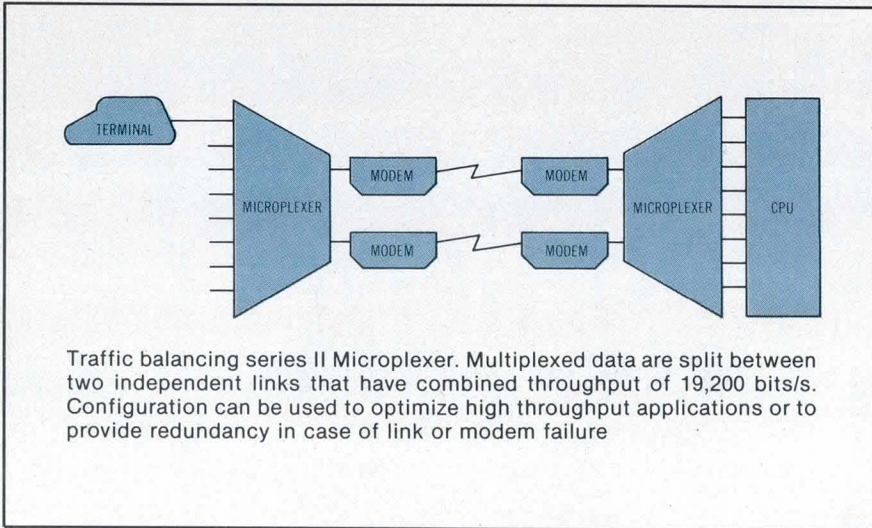


TOSHIBA AMERICA, INC.

2151 Michelson Drive, Suite 190, Irvine, CA 92715 (714) 955-1155

CIRCLE 29 ON INQUIRY CARD

Statistical Multiplexer Incorporates Dual Data Links



As additions to the series II MICROPLEXER™ family of statistical multiplexers by Timeplex, Inc, One

Communications Plaza, Rochelle Park, NJ 07662, traffic balance multiplexers M2407 and M2427 are used at both

remote site and CPU. They incorporate two built-in data links, each connected to a similar unit at the same or at a remote site. The units automatically assign channels to each of their links and reassign them dynamically depending on traffic volume and link efficiency.

When loading nears a peak on one link the devices automatically shift channels to the other link for troublefree throughput. In the event of failure or line quality degradation on one link, all channels will be assigned to the other.

The M2427 incorporates a supervisory port that allows system monitoring and the furnishing of network operating statistics. The units have four 9600-bit/s data channels, expandable to 24, with an aggregate input rate of 38.4k bits/s, expandable to 230.4k bits/s. Each of the two synchronous links has a data rate of 9.6k bits/s.

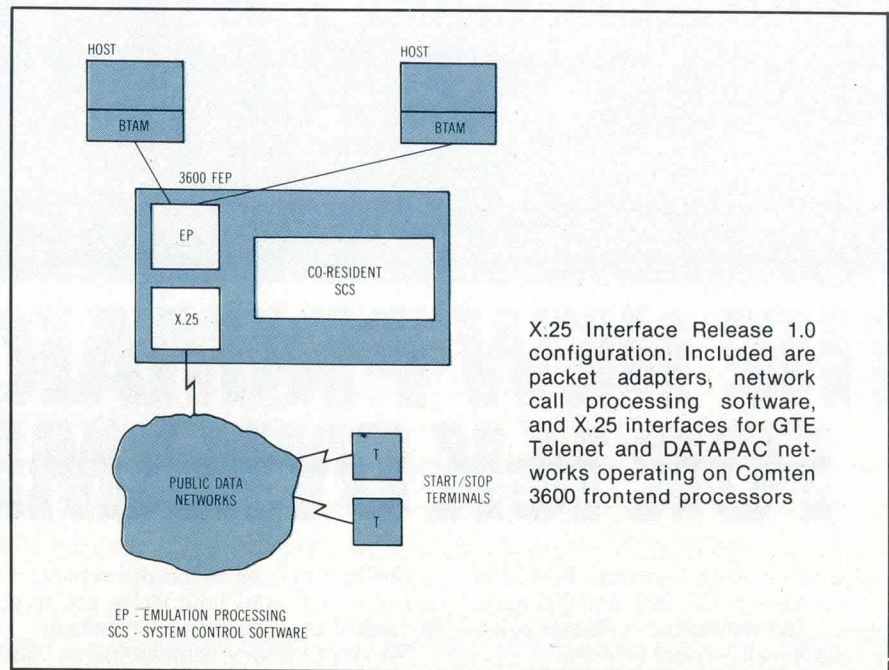
Circle 520 on Inquiry Card

Processor System Adds X.25 Interface Software

A licensed software program product called X.25 Interface for public data networks has been announced by NCR Comten, Inc, 1950 W County Rd B-2, St Paul, MN 55113. It enables the firm's 3600 communications processors to function as packet mode data terminal equipment (DTE). Users can attach their terminals to public data networks and terminate them at a 3600 frontend processor connected to an IBM compatible host.

Release 1.0 of the product allows interface with GTE Telenet in the U.S. and with DATAPAC in Canada. Support for additional public data networks that conform to CCITT Recommendation X.25 will be added in the future.

The interface can be generated to support more than one public data network in the same processor. It performs call establishment, virtual circuit management, packet assembly and disassembly, and statistics collection functions of a packet mode DTE.



Start/stop terminals attached to an X.25 public data network can access host resident applications through the processor nodes without modifications to

those applications, application supervisors, or access methods.

Circle 521 on Inquiry Card

De Anza **GIVES YOU A BETTER IMAGE...**

DeAnza's new IP8500 is *the* better image processing and display system . . . by a factor of four.

Four times more powerful. Four times more memory. Four times more interaction.

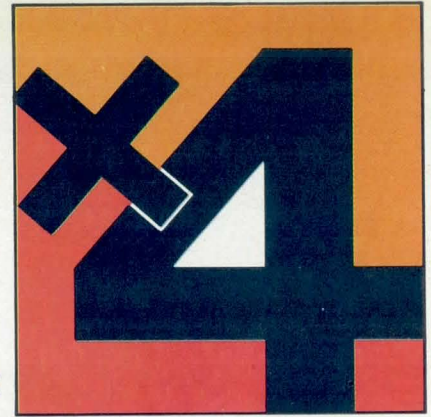
Four memory controllers handle up to four image memories per controller. This gives you an unprecedented capacity of up to sixteen 512x512x8 bit image memories to easily process 8 and 16 bit data with 32 bit results.

To meet your growing image processing needs, the IP8500 offers features you'd expect to pay much more for. Features like independent integer zoom in both the X and Y axis from 2:1 to 8:1 on each memory channel; special functions for histograms, real-time multiplication, rotation and warping, as well as high speed vector generation, up to four separately controlled dual cursor generators, four ASCII overlays and four special function generators.

The IP8500 is the better image for people respon-

sible for LANDSAT analysis, non-destructive testing, process control synthesis, remote sensing, three-dimensional computer graphics or other image processing and analysis applications calling for single or multi-station high resolution color, multi-image monochrome or pseudo color displays.

To improve your image X4, find out more about the DeAnza 8500 today. Call or write:

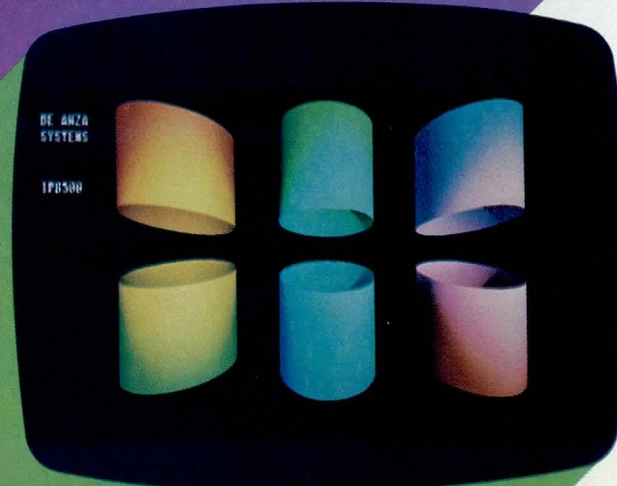
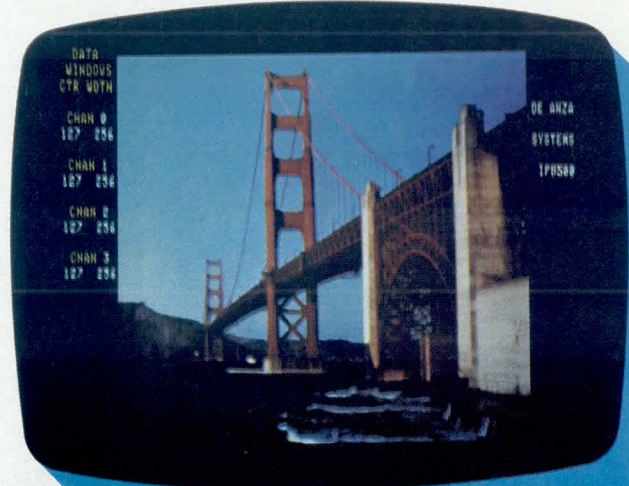


De Anza Systems Incorporated

118 Charcot Avenue • San Jose, CA 95131 • (408) 263-7155
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GIVE YOURSELF A BETTER IMAGE

CIRCLE 30 ON INQUIRY CARD



IMAGINE

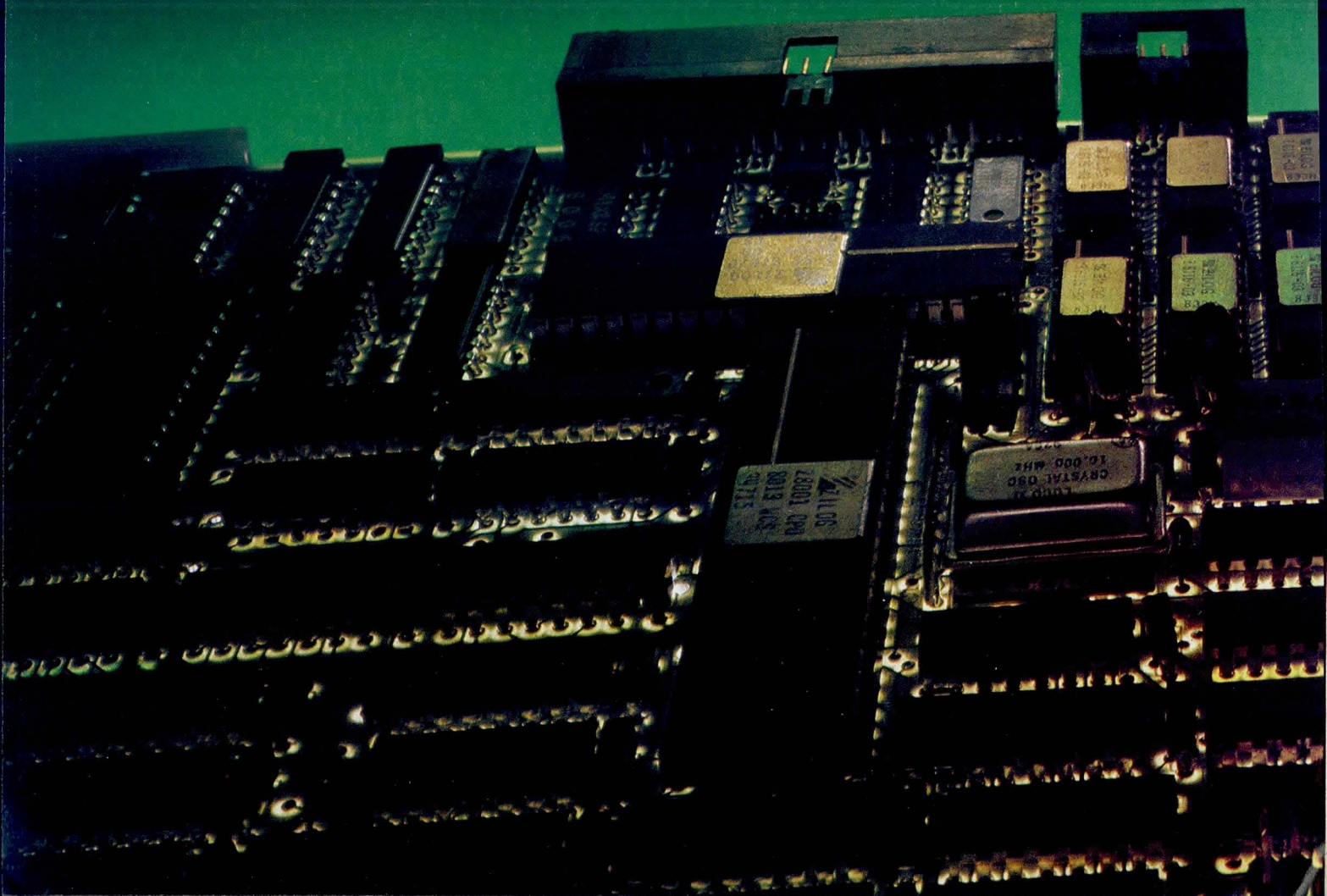
It's possible to select the precise board functions you need for your application while enjoying the power of the most advanced microprocessors made, Zilog's Z8, Z80 and Z8000.

The Zilog Computer Module concept is built around the high-performance Z-Bus™ Backplane Interconnect system, and its complementary family of microcomputer board designs and software tools. Applications oriented, the ZCM concept lets you take full advantage of the capabilities of each Zilog microprocessor—

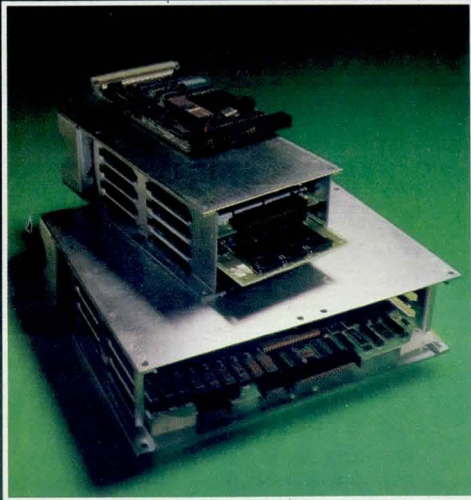
plus tomorrow's 32-bit data structures.

Select from either of two sizes of board families, both of which can share the same backplane. ZCM™-1 Single-Size Boards (6.3" x 3.9") provide a full menu of basic functions. ZCM-2 Double-Size Boards (6.3" x 9.2") provide the power you need for more complex applications.

The Zilog Computer Module concept is exciting—and cost effective. For the details, write: Zilog, Dept. G, 10460 Bubb Road, Cupertino, CA 95014. Or, call your nearby Zilog distributor.

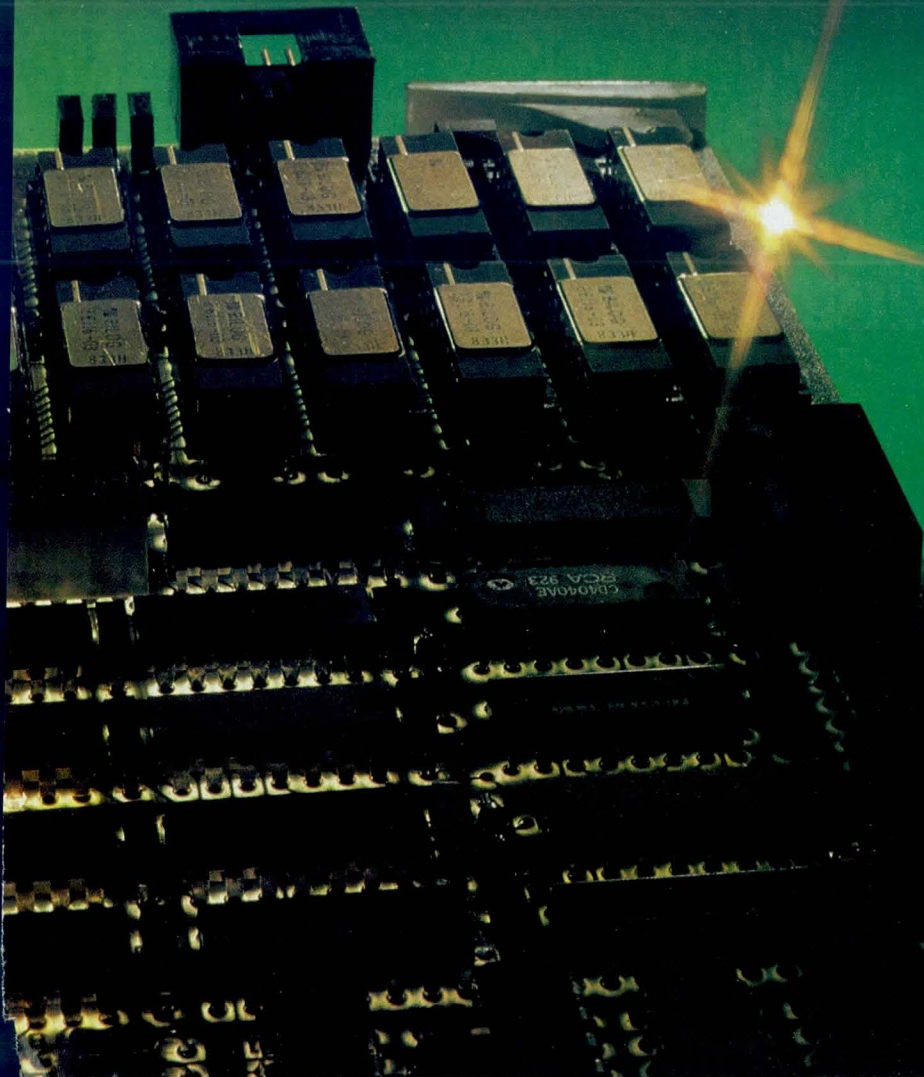


UNPRECEDENTED FREEDOM TO SOLVE YOUR SYSTEMS APPLICATION PROBLEMS. ZILOG'S COMPUTER MODULE CONCEPT. TODAY. FROM ZILOG.



**"Mix and match"
board sizes make
Z8, Z80 and Z8000 systems
design easier than ever.**

Zilog's single function ZCM-1 Single-Size Boards can be combined on the same backplane with the more powerful ZCM-2 Double-Size Boards. You build up the precise solution you need for your application without the need to pay for—or support—unnecessary electronics.



An affiliate of **EXON** ENTERPRISES INC.
CIRCLE 31 ON INQUIRY CARD

System Locates Faults in Fiber Optic Cables

A proprietary optical coupler that minimizes mode selectivity of the backscatter signal is a feature of the FIBERSCAN™ series 50 optical time do-

main reflectometer (OTDR) offered by Times Fiber Communications, Inc, 358 Hall Ave, Wallingford, CT 06492. Detection of all backscatter signals without modification or energy loss is assured by a single fiber interface, equal to or larger than most fibers under test.

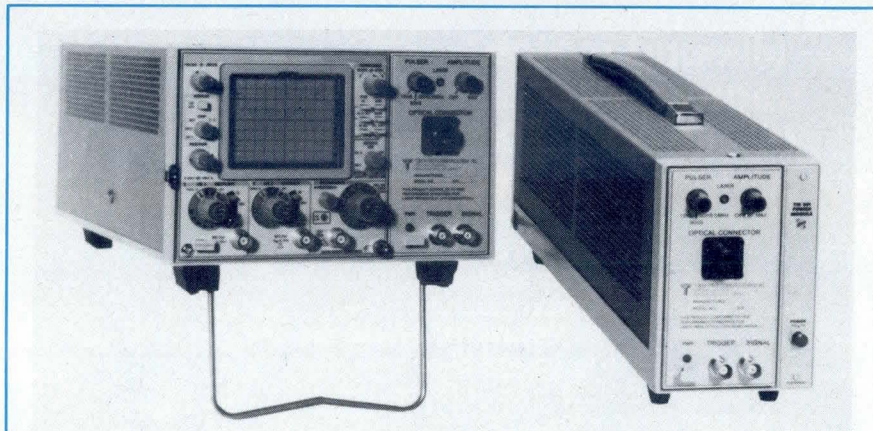
Included in the portable modular instrument are series 50 plug-in module,

Tektronix series 503 mainframe with integral power supply, and SC504 oscilloscope. Both the OTDR, as a module for use with any wideband oscilloscope, and the compatible Tektronix 501 power supply may be purchased separately.

The fiber to be tested is aligned to a specially designed coupler that permits accurate and consistent analysis of all mode structures. A variety of connector mountings is available.

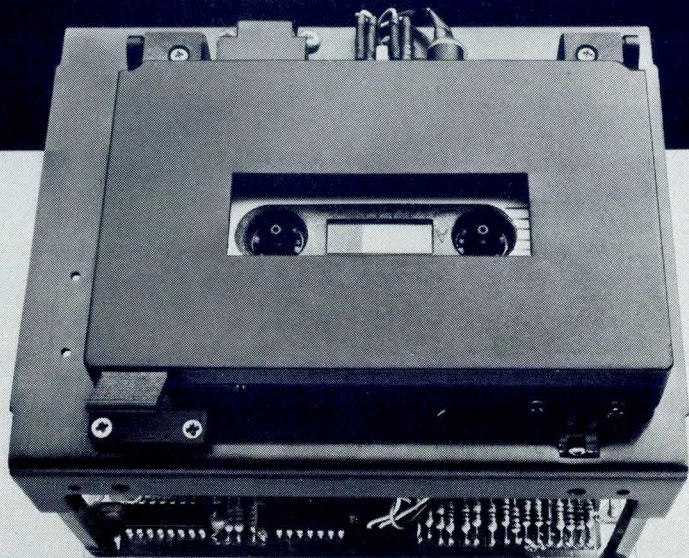
By generating high intensity optical pulses and measuring backscatter attenuation and time intervals, the unit determines waveguide characteristics and locates a broad range of faults in fiber optic cables. Use of an avalanche photodetector instead of a photomultiplier tube to optimize spectral response and linearity provides high sensitivity to breaks, splice and connector losses, distributed attenuation, and other parameters. The instrument has a 70-dB end enhanced loss capability and has been health certified by the U.S. Bureau of Radiological Health.

Circle 522 on Inquiry Card



Series 50 OTDR shown at left with mainframe and oscilloscope, and at right with power supply

WANT TO SEE HOW TO RELOAD OUR TWO-TRACK TRANSPORT?



WANT TO SEE IT AGAIN?

MFE's auto-reloading, one-megabyte, two-track cassette transport.

MFE's 452 series two-track transport automatically reloads itself for the second track. So in effect you get twice the storage of ordinary transports from a single load — up to one megabyte.

In addition, the 452 has the industry's only permanently aligned tape head. It's actually bolted down to the baseplate so it never needs adjusting.

You'll like MFE's new door design, too. It's extremely easy to load, and there are no linkages or complicated mechanical parts to go wrong.

And our tape handling system is so advanced it's virtually mistake-proof. Even if you accidentally eject the cassette while it's running at 120 ips, you won't damage the tape.

MFE's 452 series is available with or without a door. We also offer the 250 series single-track transport.

If you'd like to see a demonstration of our auto-reloading cassette, contact us.

But we can tell you now. You won't see a thing.

Call **800-258-3884**.

Or write MFE Corporation, Keewaydin Drive, Salem, NH 03079.



Ultimately, all terminals require servicing.

So why not buy the one with the ultimate service policy?

No other daisywheel terminal manufacturer offers a more complete service policy than Qume. It works basically like this:

All Qume Sprint 5[®] dealers are distinguished as either "service" or "standard" dealers. Service dealers provide end-user warranty service on all machines they sell, including spare parts and trained personnel.

Standard dealers offer a 90-day on-site service warranty with Sorbus, Inc., which has service centers in 32 major cities.

But if you don't work near one of these service centers, for warranty service you can send your terminal to the nearest Qume "depot," located in Texas, California or New Jersey.

Even the most reliable terminals in the business are ultimately going to need servicing. But with Qume, you'll never have to worry about service problems. For further information call or write Qume, 2350 Qume Drive, San Jose, California 95131. Tel: (408) 942-4000. TWX: 910-338-0232.



Qume[®]

Printer Products Division

CIRCLE 33 ON INQUIRY CARD

ITTM is the difference between too smart and too dumb.

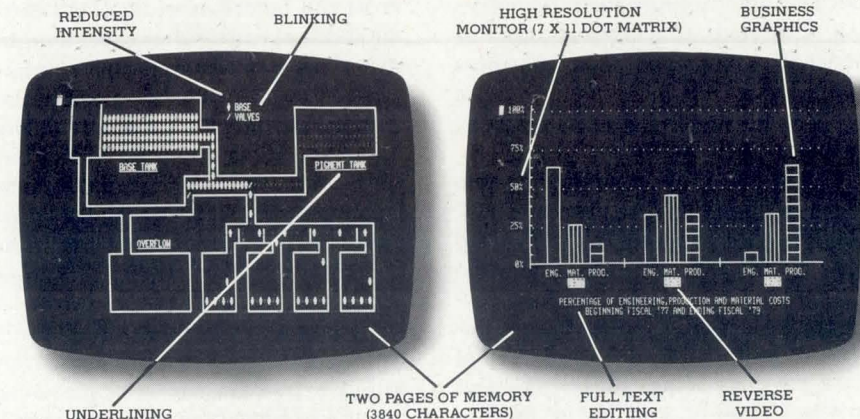
SALES ORDER ENTRY		P.O.# <u>A 475662-9</u>	S.O.# <u>01789-56</u>
CUSTOMER: LEAR SIEGLER DATA PRODUCTS DIV. 714 N. BROOKHURST STREET ANN ARBOR, MI. 48103 PHONE: (714) 774-1818 TELEX: 65-5444 TIX: 910-591-1157		DATE: <u>08/25/88</u>	SHIP VIA: <u>AIR EXPRESS</u>
		DELIVER TO: <u>ENGINEERING DEPT.</u>	
ITEM #	DESCRIPTION	QUAN.	PRICE
1			
2			
3			
4			
REMARKS:		TOTAL	

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Intermediate Terminal

Just when you thought you were totally confused by the incredible variety of "smart" computer terminals on the market, Lear Siegler brings you exactly what you need. It is IT, the Intermediate Terminal™ video display.

IT banishes all the confusing claims being made in the computer marketplace by compressing the broad spectrum of "smart" termi-

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ns into ITself. Now, when you're looking for a terminal that isn't too smart but isn't too dumb either, IT is perfect for the job. And instead of having to weave your way through the confusing forest of "smart" terminals, just look for IT. Because IT is enough.

IT brings you the same high standards and solid workmanship that made its cousin, the Dumb Terminal® video display, a legend in its own time. IT may be of average intelligence, but there's nothing average about IT's consistent, quality performance and sensible features.

IT is completely self-contained, with full editing, formatting and protected field capabilities. Not to mention a microprocessor which increases reliability and ease of use.

TWO PAGES ARE BETTER THAN ONE.

The list of IT's special features

could go on all afternoon. Outstanding among them are the two pages of display that are standard with IT. Use them both and get up to 3840 characters of display potential. Or, allocate the second as a print buffer and be sending data on page two while entering data on page one.

Each page has the following independent page characteristics:

protect, program mode and cursor retention. And when you change from one page to another, these characteristics are stored in memory to be recalled at another time, letter perfect.

IT™ HAS QUITE A DISPLAY.

With IT, specific areas are designated as protected fields. They can't be typed over unless you remove the terminal from the protected mode. Even your remote computer can't overwrite the protected fields until IT is removed from the protected mode. Background (protected data) can be displayed at a lower intensity, while foreground is displayed at normal intensity and may be modified. You can even tab the cursor forward and backward to the start of each unprotected field.

And when you depress IT's special function key, a special function sequence is transmitted. The

remote computer is then in full control. And all control functions that can be initiated from the keyboard can also be executed from the remote computer.

Also on IT, full or half duplex operation is switch and keyboard selectable. You can also choose from conversation or block transmission, which can be initiated by you or the computer. In block mode, a line, a message or a page can be transmitted in its entirety.

IT™ IS NOT JUST ANOTHER PRETTY FACE.

IT's editing capabilities allow you to clear the screen, or use the cursor for a character change. In addition, IT comes complete with character insert and delete, line insert and delete, erase to end of line/field/screen, and tab and back tab. IT's full controls also allow you to skip protected fields, backspace, forespace, move up, down, return, home, and new line.

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FIND OUT THE WHOLE STORY ABOUT IT.™

The people at Lear Siegler would be more than happy to fill you in on all the details about IT. Just drop us a line or call. Because IT is worth it.



IT™, the Intermediate Terminal from Lear Siegler.

Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, CA 92803 800/854-3805. In California 714/774-1010. TWX: 910-591-1157 Telex: 65-5444. Regional Sales Offices: • San Francisco 408/263-0506 • Los Angeles 213/454-9941 • Chicago 312/279-5250 • Houston 713/780-2585 • Philadelphia 215/245-1520 • New York 212/594-6762 • Boston 617/423-1510 • Washington, D.C. 301/459-1826 • England (04867) 80666.

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CIRCLE 34 ON INQUIRY CARD

TECHNOLOGY REVIEW

64-Bit Parallel Processor Implemented With MIMD Architecture for Throughput

Heterogeneous Element Processor (HEP) is a 64-bit high speed digital computer that provides high speed parallel processing of heterogeneous data elements. Denelcor, Inc, 3115 E 40th Ave, Denver, CO 80205, designed the system for use in scientific or commercial applications that effectively use its 10M- to 160M-instruction/s processing speeds. This throughput is made possible by the unit's implementation of multiple instruction/multiple data stream architecture.

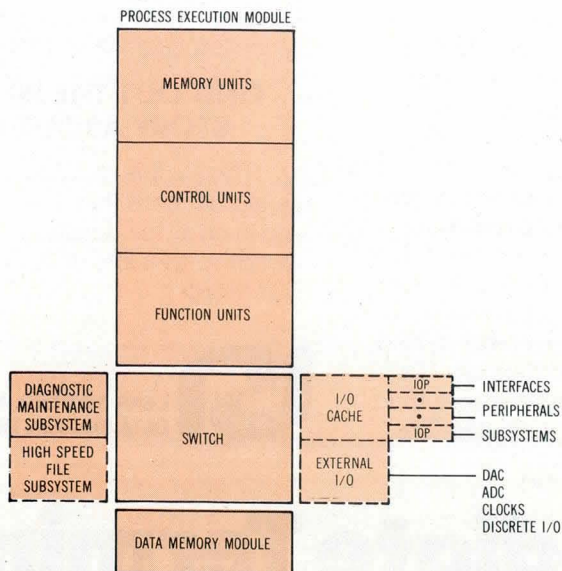
This concept, called MIMD architecture, achieves high performance at low cost by keeping all processor hardware active executing multiple parallel programs simultaneously. With this architecture, there may be several cooperating programs or processes within each independent program.

Because the multiple instructions being executed concurrently are independent of one another, execution of one has no influence on execution of the others, allowing processing to be fully parallel at all times.

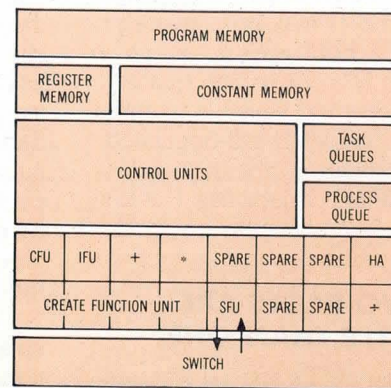
HEP consists of process execution modules (PEMs), data memory modules, and support processors interconnected by a high speed data switch network. All data memory modules are accessible by all PEMs. Thus processes executing in parallel in one or several PEMs may cooperate by reading and writing shared information in the data memories. Parallel processes synchronize and pass information back and forth using the full/empty attribute of each data memory location. HEP instructions may automatically wait for an input data memory location

to be full before execution, and leave the location empty after execution. Instructions may also wait for an output location to be empty before execution and leave it full after execution. This communications discipline allows processes to conveniently and unambiguously pass information to other processes while executing. The full/empty attribute ensures that reads and writes of interprocess variables will alternate and no information will be lost. For locations used exclusively within a process, the attribute is ignored and memory is accessed conventionally.

To efficiently manipulate data, each PEM contains 2048 internal general purpose registers. PEMs automatically detect and flag normal arithmetic
(continued on page 58)



Designed for high speed large scale scientific computing, Denelcor's 64-bit HEP computer is capable of executing up to 160M instructions/s. System contains multiple process execution modules, data memory modules, and support processors interconnected by high speed data switch network



Process execution modules within HEP contain 2048 internal general purpose 64-bit registers. Up to 64 user processes may exist simultaneously in each PEM. Data memory reference instructions allow partial word and byte addressing. Each module executes up to 10M instructions/s and up to 16 modules can exist in system

The OEM Tape Transport For The 80's.

Now, Datum innovation brings you the next generation in mini-computer magnetic tape transports, the D-451. A transport that thinks for itself thanks to Datum's smart new single-board microprocessor.

Self diagnostics, a reduced electronic component count and hybrid chip read amplifiers are examples of Datum's entirely new microprocessor design architecture.

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CIRCLE 35 ON INQUIRY CARD



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HD46821	PIA	Now	6821
HD46846	ROM, I/O, Timer	Now	6846
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HD46503	FDC	Now	6843
HD46504	DMAC	Now	6844
HD46505	CRTC	Now	6845
HD46508	A/D Converter	Now	NEW

Part No.	Description	Availability	Replaces
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HD6801	1 chip, clock, 2K Byte ROM, 128 Byte RAM, I/O	Now	6801
HD6805	1 chip, clock, 1.1K Byte ROM, 64 Byte RAM, I/O	Now	6805
8-Bit Multi-Chip (Enhanced)			
HD6809	High performance microprocessor	Now	6809
16-Bit Multi-Chip			
HD68000	16-Bit CPU	4th Quarter	68000
HD68450	16-Bit DMAC	TBA	68450



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CIRCLE 36 ON INQUIRY CARD

errors (overflow, underflow, etc) and may generate traps on occurrence of these errors. Programs within a system are protected from each other and relocated in memory by a set of relocation/protection registers in each PEM. This allows multiprogramming with full isolation of one user from another.

All data and instruction words are 64 bits long, although PEM data memory reference instructions allow partial word and byte addressing. Memory bandwidth is 20M words/s/PEM, including the data switch network. Each PEM executes up to 10M instructions/s. The architecture of the switch network allows up to 128 memory modules of up to 1M words each and up to 16 PEMs. This range of system configurations results in speeds up to 160M instructions/s on 64-bit data and memory sizes up to 1G bytes.

Systems may include high speed realtime I/O devices connected to the data switch network. These devices operate at memory speeds up to 80M

bytes/s. Normal I/O devices are connected to the HEP system through support processors; thus standard commercial I/O devices and controllers may be used for routine I/O functions. All standard I/O devices are accessible through operating system and FORTRAN I/O.

Both normal and synchronized memory access are available to the FORTRAN programmer as well as the assembly language programmer. Software modules in both FORTRAN and assembly language may be distributed across several PEMs to achieve increased throughput. In general, design of a parallel program is not affected by whether the program runs in one or in several PEMs.

Creation and termination of parallel processes in an MIMD program is a hardware capability directly available to the programmer. Processes are created or terminated in 100 ns by execution of a single system instruction. Thus processes may be created at any

point in a program where additional parallelism is required and terminated as soon as their function is accomplished. Up to 64 user processes may exist simultaneously within each PEM in a HEP system.

HEP systems support a batch operating system with FORTRAN and assembler programming languages. The operating system provides input and output spooling, batch job scheduling, and full operator control of the system. FORTRAN is an extended ANSI FORTRAN IV with added parallel capabilities, providing the programmer with the means for explicit parallel programming. Assembly language allows users to access all system capabilities efficiently. The interactive maintenance language provides sophisticated debugging capabilities. It is used in conjunction with maintenance hardware, either test slots in the mainframe or offline test fixtures.

Circle 420 on Inquiry Card

THE IBM CONNECTION

The spotlight is on the BAC-HASP protocol converter from KMW Systems. The KMW Model BAC-HASP allows operation of a variety of peripheral equipment at high telecommunications data rates and ensures error-free operation by utilizing the popular IBM HASP multi-leaving RJE workstation binary synchronous protocol. BAC-HASP sends and receives EBCDIC data via IBM binary synchronous protocol, performs all required error-checking functions, translates the data to ASCII, and outputs it in serial asynchronous or byte parallel format to and from user-attached devices.

The BAC-HASP features:

- Console support, duplicate character compression, and bi-directional communications allowing multiple devices to operate at the same time
- Optional modem eliminator configuration for local attachment
- 4k bytes of buffer storage for improved throughput
- Exceptional versatility, providing several applications to the user

Applications: Printers, Plotters, Graphic CRT's, Mini Computers, Card Readers, Cassettes, Cartridges, Mag Tape

KMW Systems produces a variety of protocol converters including 2780, 3780, 3270 and Honeywell GRTS protocols. For more information, call or write:



**KMW
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CORPORATION**

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Austin, Texas 78735
512-288-1453

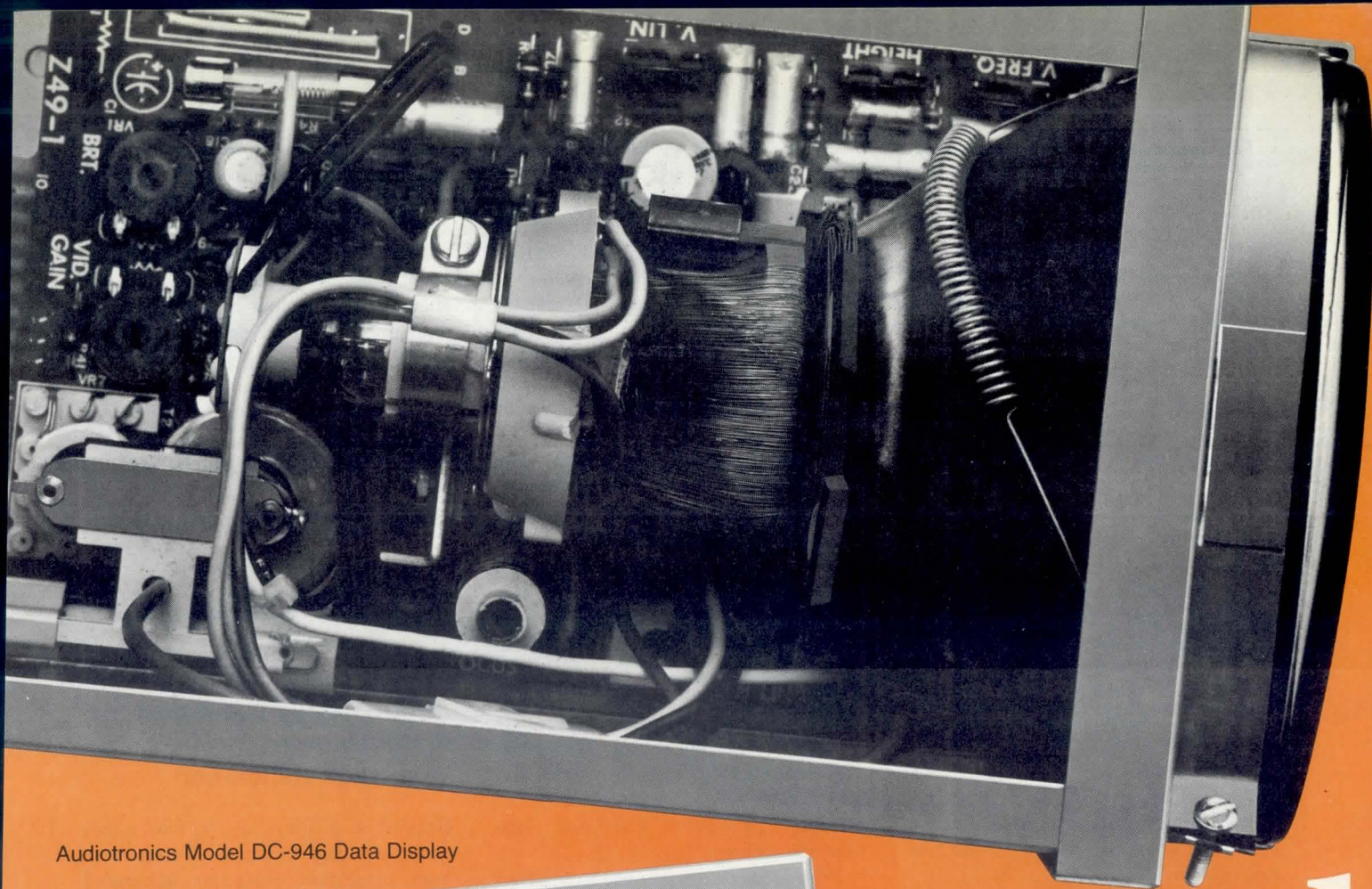


Switching Facility, Disc Units Increase 303X Performance

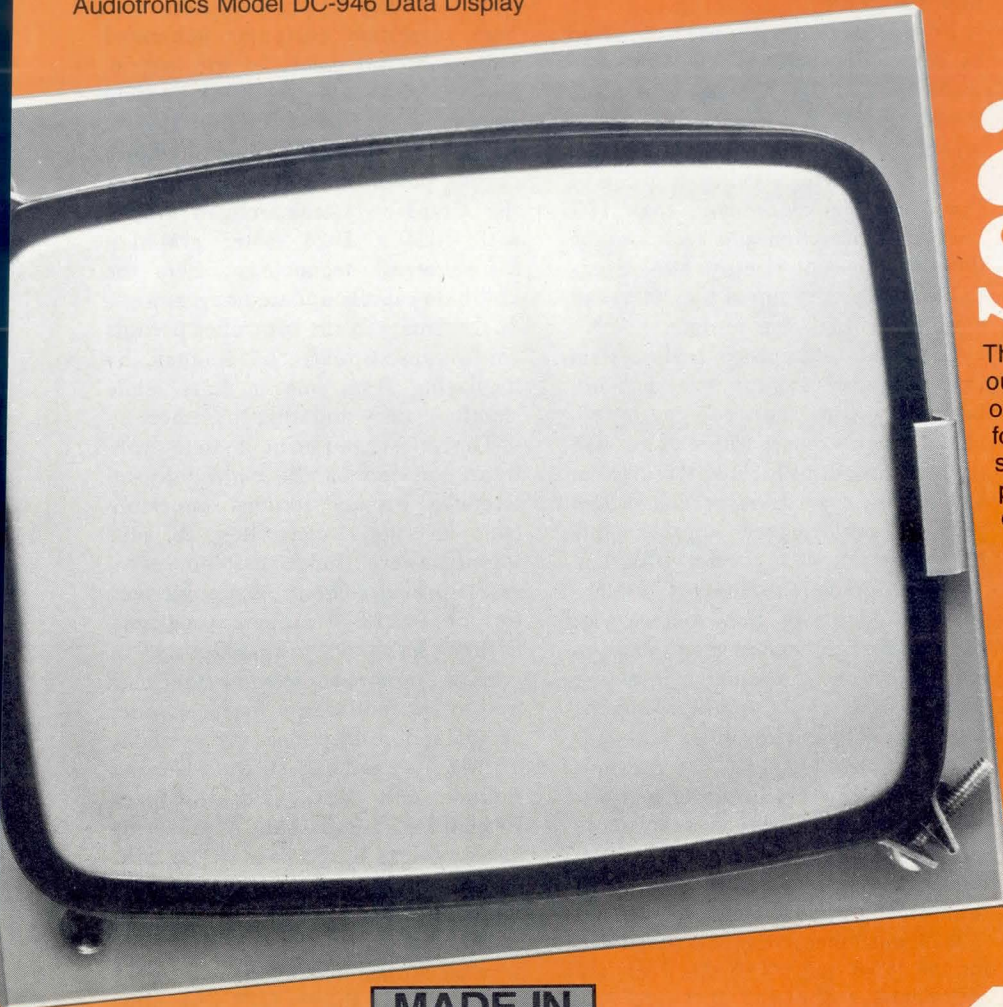
Products and programming announced by International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604, including an attached processor, a switching facility, and two direct access storage devices (one of which can store over 2.5G char of information), significantly increase the capacity and performance of large 303X computer systems. Enhancements to the large system control program, multiple virtual storage (MVS), provide improved systems and processor storage management for 303X processors.

Attached processor 3042 model 2 offers up to 12 channels (six as stand-alone and an optional group of six), expanding the maximum number of channels available to users of the 3033 attached processor complex to 28 in order to supply greater system capacity and versatility. The 3814 switching management system permits computer operators to electronically vary the interconnections between processors and

(continued on page 60)



Audiotronics Model DC-946 Data Display



actual size

This popular Audiotronics data display is one of our 48 standard models. We have sold thousands of them to giants in the industry. Maybe it's perfect for your requirements. If not, talk to us about your specifications. We're dedicated to innovative product design, quality production standards and complete customer satisfaction. Whatever you need, we have the experience and talent to design it, or improve it. Contact us today.

Model DC-946 features:

- modular construction
- 5" cathode ray tube (12.7 cm)
- solid state
- DC operation—12V dc inputs
- choice of signal inputs:
 - TTL (standard)
 - Composite video (plug-in module)
- standard 15,750 KHz horizontal scan frequency
- 650 lines resolution



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CIRCLE 38 ON INQUIRY CARD

peripheral equipment in large systems. The system can store up to 78 configuration descriptions and help manage interconnections of control units including 3380 storage control models and processor channels.

Controlled by one or two 3604 model 6 keyboard/display units, the 3814s support interconnection of up to 128 switching nodes—managing as many as 16 channels and 8 control units or 8 channels and 16 control units. In complex data processing installations, this can result in simplified operations and increased efficiency.

Direct access storage devices feature advanced technology and compact design and attach to most large processors. The 3380 can store up to 2.52G char of information—almost four times the capacity of a 3350. With the data streaming feature available on 3031, 3032, and 3033 processors, the 3380 can transfer data at up to 3M char/s.

The 3375 disc storage device holds more than 800M char of data and attaches to 4331 group 2 and 4341 processors as well as to 3031, 3032, and 3033 processors equipped with data streaming. Average seek time is 19 ms.

An extension of channel protocols, data streaming doubles the data rate on the first two channels in a processor channel group, enabling users to take advantage of the data transfer rate of the direct access storage device. Maximum aggregate data rate of a 6-channel group can be increased from 6.7M to 10M bytes/s. An optional speed matching buffer feature allows the high density storage available with the 3380 direct access storage device to be used at data rates of 1.5M char/s on 3031, 3032, and 3033 processors and 3042 model 2 attached processors, and System/370 models 158, 158-3, 168 and 168-3.

A combination of film head technology and compact design helps reduce power consumption on the 3380 by up to 70%, floor space requirements by up to 65%, and heat generation by up to 75% compared to equivalent storage in 3350 devices. In the units, read and write heads, discs, and two actuators are integrated into head/disc assemblies to improve reliability and efficiency. Two

head/disc assemblies are contained in each 3380, one in each 3375.

Dynamic path selection, an optional internal architectural function of the 3380, provides a second data path for attachment of the 3380 to a second storage director which controls the transfer of data. This alternate path provides concurrent access to data and can improve availability if access is lost through malfunction of a channel, storage director, or controller.

Both devices utilize count-key-data architecture that can facilitate migration from other direct access storage devices. 3380 units may attach to 3031, 3032, or 3033 processors and 3042 model 2 attached processors through the data streaming feature to permit use of the 3M char/s data rate. The optional speed matching buffer feature allows devices to be used at the 1.5M-char/s data rate of the processors. The 3375 attaches to 4331 model group 2 and 4341 processors, as well as to 3031, 3032, and 3033 processors and 3042 model 2 attached processors equipped with data streaming.

Both storage devices are supported by appropriate models of the 3880 controller. When data streaming is used, the 3880 can be placed up to 400 ft (124 m) from a processor channel. To meet needs for growth, a string or group of four 3380s can store more than 10G char of information and each storage director can control up to two strings of four 3380s. A group of four 3375s can store up to 3.2G char of data.

Designed to improve both system and processor storage management, large system control program enhancements incorporated in the MVS licensed programs include MVS/System Extensions, a program product which provides performance improvements to the basic MVS control program. These programs also support 3033 Extended Addressing and enhance VMS system, storage, management, and job entry functions. Extended addressing enables users of 3033 multiprocessors, for example to address up to 32M char of information—double the previous capability. This expansion of addressable processor storage enables more information and programs to be contained in the processor and can result in improved performance.

With customer shipments scheduled for the third quarter of this year, the 3042 model 2 is priced at \$1,255,000. Shipments of the 3814 switching

management system are scheduled to begin in second quarter 1981; prices are \$205,000 for a system that includes Model A unit with integrated controller, B remote unit, and C expansion unit. First shipments of 3380 and 3375 disc storage devices are to be in the first and third quarters of 1981, respectively; purchase price for a 3380 model A which contains features for attaching up to three 3380 model B units ranges from \$97,650 to \$142,200. The 3375 sells at \$46,450 for model A1 and \$31,000 for B1.

Circle 421 on Inquiry Card

Color Display Combines Rapid Update With High Resolution

Graphic 8 displays up to 256 colors simultaneously to provide users with high resolution computer generated images in full color. In the system, Sanders Associates, Inc, Information Products Div, Daniel Webster Hwy S, Nashua, NH 03061, has combined processing power and image dynamics of the Graphic 7 stroke/refresh system with 1024 x 1024 raster graphics. Stroke/refresh technology offers the ability to rapidly update images, while dual memory in the controller permits continuous update of images by displaying from one memory while simultaneously updating the other.

The most powerful system configuration can handle eight fully interactive display stations operating from a single controller. A software/firmware supported microprocessor provides choice of graphic control or FORTRAN support programs. Either handles programming of graphic terminals, leaving the user free to concentrate on host computer programming. Interfaces are available for DEC VAX and PDP-11, Data General Eclipse and Nova, Perkin-Elmer, Hewlett-Packard, Systems Engineering Laboratories, Harris, and HTDS computers. An RS-232-C interface handles communication.

The unit provides a choice of color or monochrome display with up to 256 colors or gray shades (128 with blink
(continued on page 62)

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MTOS 86

MTOS-80

Real-time operating system for the 8080.
In service since 1976

MTOS-68

Real-time operating system for the 6800.
In service since 1976

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MTOS is sold in source form; the user can specialize MTOS for his own applications.

MTOS-11

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In service since 1976

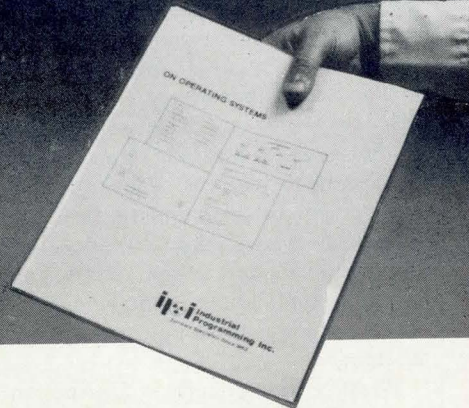
These MULTI-TASKING OPERATING SYSTEMS are sold under a liberal licensing policy which allows resale of the object program, when embedded within a product, without further charge.

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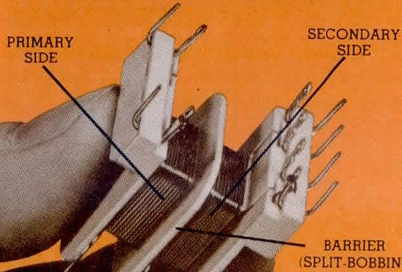
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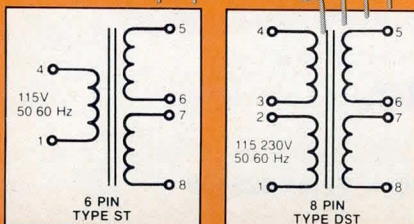
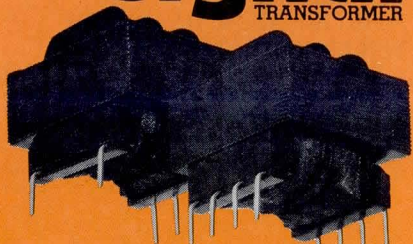
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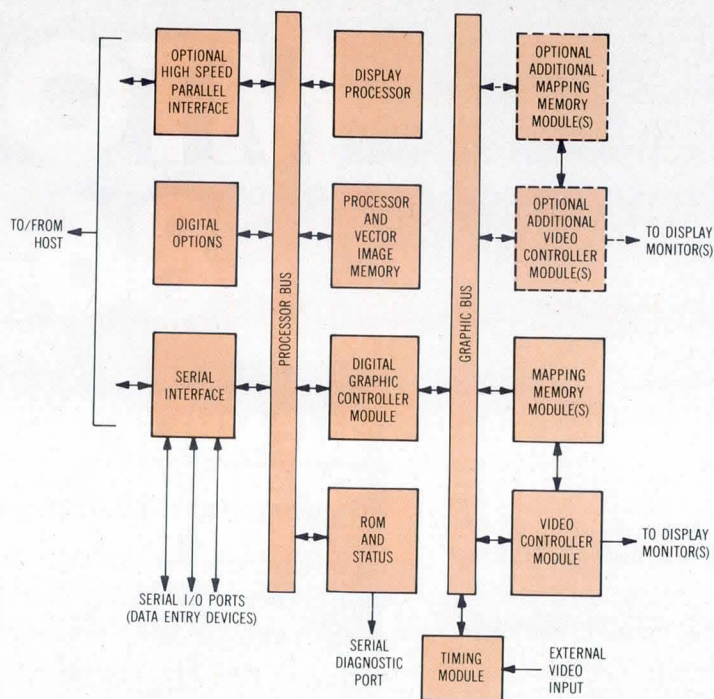
signal

TRANSFORMER



CIRCLE 40 ON INQUIRY CARD

TECHNOLOGY REVIEW



Sanders' Graphics 8 intelligent computer graphic display system offers 1024 x 1024 resolution raster graphics to provide computer generated images with up to 256 simultaneous colors

capability). Display memory provides storage for up to 1024 x 1024 picture elements (pixels)—up to 8 bits/pixel/display. Other features of the 19" (38-cm) display are multiple character fonts and sizes, external video input, and high speed cursor and high speed erase. Resolutions range from 512 x 512 to 1024 x 1024; others are available at 4 x 3 aspect ratios. Image enhancement features of lookup table and polygon fill are standard. Buffered refresh memory in the 8200 series controller offers rapid image update, and permits applications requiring continuous update of complex images to be handled.

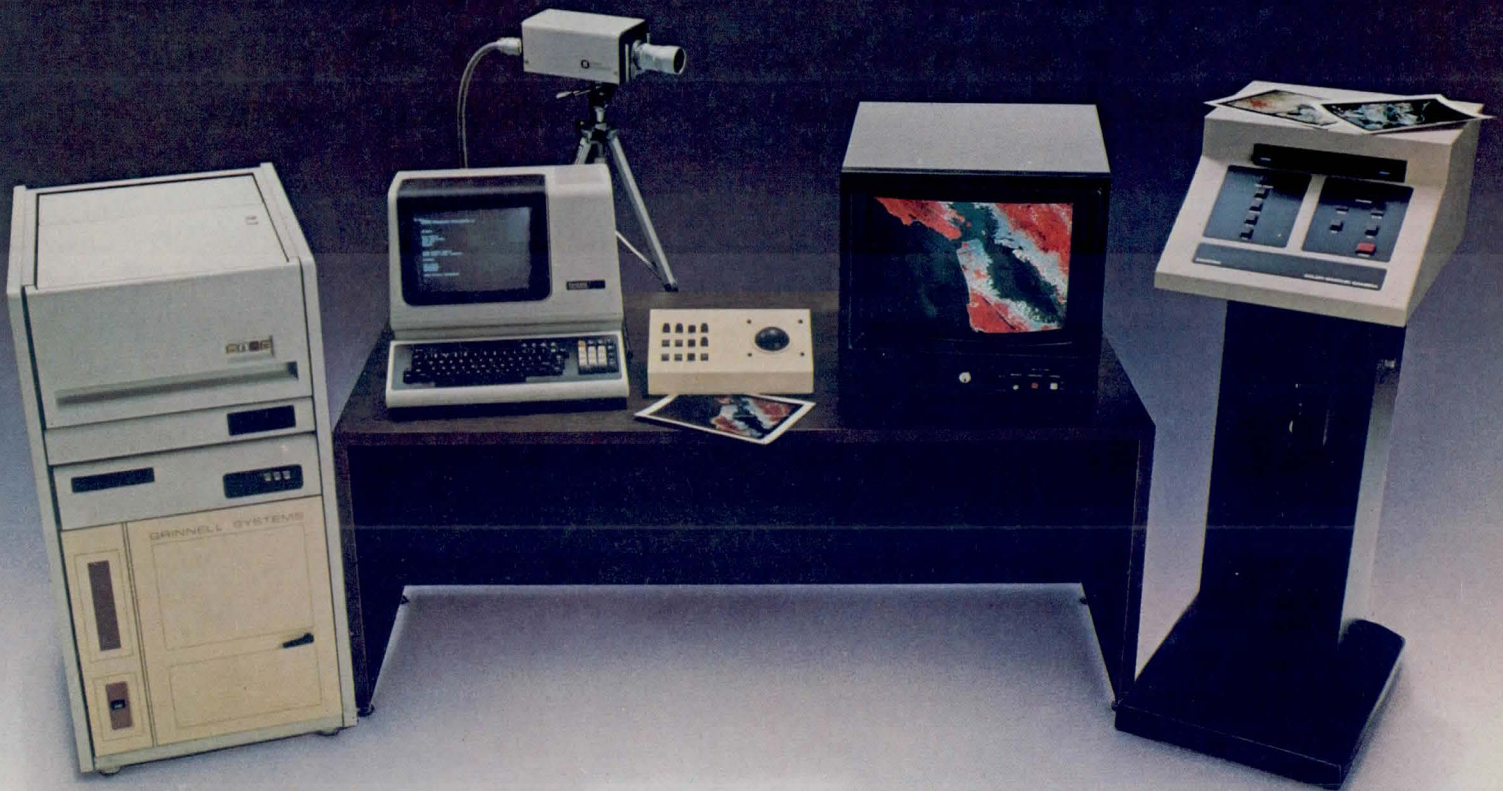
Because the system is instruction compatible with the Graphic 7 stroke/refresh display system, programs developed for that system are rapidly made operational. Raster enhancements such as polygon area fill can be applied to the original outline images in this case.

Distributed processing capability is provided by the unit's built-in minicomputer level CPU. This processor, based on high speed bipolar bit slice chips, uses a popular instruction set with more than 400 instructions. Programmability of the processor permits the user to tailor operations at the terminal to the application. Available processor read/write memory ranges from 32k to 256k bytes in addition to the image refresh memory.

The graphic control program, which is included in basic firmware, contains built-in test features that allow verification of system operability without involving the host computer. The FORTRAN support package option permits images to be generated using FORTRAN subroutine calls. This enables users to work in their own coordinate system to generate images, even if the programmers are not familiar with computer graphics.

Circle 422 on Inquiry Card

Complete systems for computer graphics and image processing.



And, we do mean complete! Grinnell systems can include computers, disc drives, terminals and software operating systems. Plus a FORTRAN software and driver package; high resolution TV monitor, camera, and hard copy color printer.

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That's why Grinnell systems work with standard TV monitors and cameras, and why plug-compatible interfaces are available for most minicomputers.

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GMR 270 Series: 512 x 512 resolution frame buffers and full color pipeline image processing systems.

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So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a complete system that can do it. For complete specifications and/or a quotation, call or write today.

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63

CIRCLE 41 ON INQUIRY CARD

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MC68000

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31 0

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USER STACK POINTER

SUPERVISOR STACK POINTER

31 0

PROGRAM COUNTER

15 0

STATUS REGISTER

SYSTEM BYTE USER BYTE

HIGH-EFFICIENCY INSTRUCTIONS

```
* INVOKE SUBROUTINE WITH CALL BY NAME ARGUMENT
*
*   PEA ARG          CALCULATE ARGUMENT ADDRESS
*   BSR SUB          AND PLACE ONTO STACK
*                   CALL THE SUBROUTINE
*
* SUBROUTINE
* SUB:  MOVEM D0/D7/A3+-(SP) SAVE REGISTERS D0, D7, AND
*                   A3 ONTO THE STACK
*                   USE A6 AS NEW FRAME
*                   POINTER AND ALLOCATE 80000
*                   LINK A6, #80000
*                   BYTES OF LOCAL WORK AREA
```

ASYNCHRONOUS BUS

ADDRESS STROBE

ADDRESS BUS

DATA BUS

PERIPHERALS

DATA TRANSFER ACKNOWLEDGE

The best available 16-bit microprocessor is now available from authorized Motorola distributors everywhere. The MC68000. Since its introduction in September, 1979, the MC68000 generally has been recognized as the most advanced high-performance 16-bit microprocessor in the industry.

The MC68000 is the first, the only, 16-bit microprocessor with a large set of seventeen 32-bit registers, and the only one with 16-megabyte direct memory addressing.

Its uniquely powerful yet easy-to-use micro-coded architecture, combined with the inherently high-performance characteristics and reliability of Motorola's HMOS VLSI technology, offers the designer unmatched advantages in system design, software cost reduction and product capabilities.

As a vital aspect of future systems, efficient multiprocessing capability received special attention in design of the MC68000. With the asynchronous bus, a multiple bus-master

technique is used to achieve high-efficiency multiprocessing.

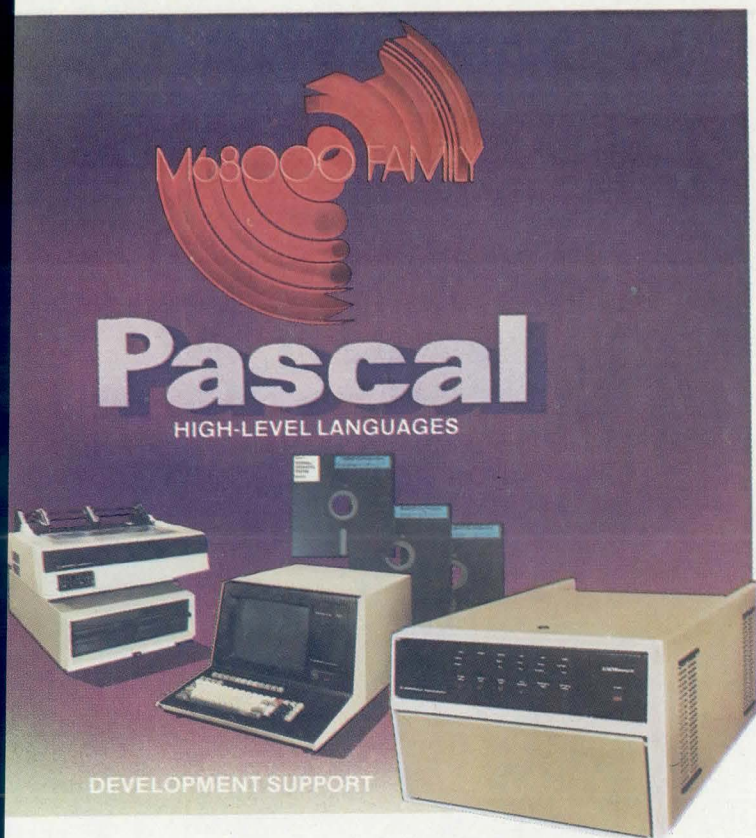
Expanded register set allows enhanced performance.

The 32-bit registers eliminate the need for pairing, and data and address registers are separated to allow the performance enhancements of parallel operation. All the registers can be used as index registers, and all address registers may be used as index stack pointers to reduce programming bottlenecks.

High-efficiency instruction set.

The simple, efficient instruction set was designed on information developed in extensive instruction-usage studies. The 56 powerful instruction types are designed to minimize the number of mnemonics a programmer must remember. Addressing modes are usable with all applicable instructions for additional ease-of-use

for advanced systems from Motorola distributors.



and reduced software debugging time, with resulting software development-cost reduction.

Asynchronous, non-multiplexed bus.

Implementation of the asynchronous bus allows optimum utilization when supporting devices requiring different access times, and allows implementation of cache memory or other hierarchical memory schemes without bus rule changes. The non-multiplexed bus is up to 30% faster than a multiplexed bus, and improves overall system performance because interface to the processor is not a bottleneck.

Designed for high-level language support.

As the processor for the '80s, the MC68000 was carefully designed for the high-level languages of the '80s. With Link and Unlink instructions, the large number of general-purpose registers, address manipulation on stack, and a variety of

additional features, the MC68000 is, by design, the ideal MPU for an easy-to-use, block-structured high-level language. It's equally fluent with Pascal or assembly language.

Efficient operating system support.

Numerous features offer valuable operating system support. Among the most important is the distinction between the user mode and the supervisor mode which improves system reliability and allows resource protection. Also included for such support are specific instructions such as the Test and Set instruction (for semaphore operations), Traps (for efficient operating system calls), and the Move Multiple instruction (for streamlined context switching).

Code reliability for system integrity.

Code reliability and maintainability are key issues for any system designer in this day of large software development efforts. Illegal instruction and illegal addressing mode detection aid system designers in guaranteeing system reliability.

The user/supervisor distinction, privileged instructions, and traps on unauthorized activity aid the system designer in guaranteeing systems integrity.

The choice of winners.

The power and versatility of this total system approach is more apparent than ever as the tremendous scope of the entire M68000 family concept is revealed.

Designers who require the very best in advanced high-performance microprocessors turn to Motorola. The M68000 family, present and future, will be the choice of winners throughout the '80s. Shouldn't it be yours?

With the flexibility of the developing total-system M68000 family, and the system-development support of EXORmacs™, VERSAbus™ and the VERSAdos™ multi-tasking, multiprocessing operating system, there is no contemporary approach to microcomputers that offers so much for so many systems. The MC68000 is your best bet for the '80s for

Innovative systems
through silicon.



MOTOROLA INC.

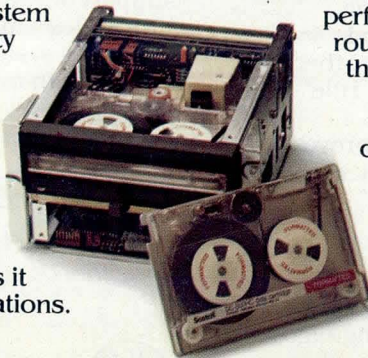
NEVER BEFORE HAS SOMETHING SO SMALL
BEEN ABLE TO HOLD SO MUCH
AT SUCH A LOW COST.



This is 3M's DC-600 HC Data Cartridge for disk back-up. It's just 4" x 6" x 1/2". Yet it holds a full 67 megabytes of formatted user information (144 megabytes unformatted). And most surprisingly, it only costs about thirty dollars.

The marvel that makes it work is our HCD-75 Data Cartridge Drive. At 4.6" x 7" x 8.6" (19" deep with controller/formatter module) it's the smallest full-capability back-up system available today. And its storage capacity makes it the most economical, too.

You see, the HCD-75 drive unit eliminates the need for costly multi-track heads. Instead, it uses a new tape head which features automatic positioning to any of the tape's sixteen tracks. The result is a storage capacity much larger than ever before possible with data cartridges. Which also makes it suitable for other mass storage applications.



Extensive use of microprocessors in the HCD-75 make it the world's first truly intelligent cartridge drive system. Other than initial commands, all tape drive functions are controlled locally. So the host computer system can remain free for other functions. What's more, the HCD-75 features sophisticated error detection and correction capabilities. And to insure system performance, self-test diagnostic routines run continuously. Even when the system is not in use.

Will wonders never cease?

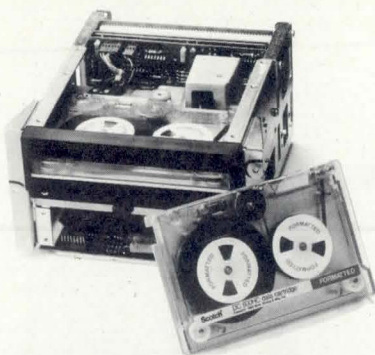
For more information, check the listing on the next page for the representative nearest you.

Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.

**THE DISK BACK-UP SYSTEM
THAT'S SUDDENLY WAY OUT FRONT.**

CIRCLE 43 ON INQUIRY CARD

3M



3M DATA PRODUCTS REPRESENTATIVES

Data Products/3M
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CTI Data Systems, Inc.
Long Beach, CA
213/426-7375

P.A.R. Associates
Denver, CO
303/355-2363

PSI Systems, Inc.
Albuquerque, NM
505/881-5000

MIDWEST

OASIS Sales Corporation
Elk Grove Village, IL
312/640-1850

Carter, McCormick & Pierce, Inc.
Farmington, MI
313/477-7700

The Cunningham Co.
Houston, TX
713/461-4197

EAST

J.J. Wild of New England, Inc.
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617/444-2366

Wild & Rutkowski, Inc.
Jericho, Long Island, NY
516/935-6600

COL-INS-CO., Inc.
Orlando, FL
305/423-7615

Optical Wand Reads Barcoded Programs and Data into Calculator

Barcode reading model HP-82153A optical wand enables quick accurate entry of programs and data for the HP-41C calculator. Plugging into the calculator, the wand, developed by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, reads HP barcode printed on paper, allowing economical reproduction and distribution of software.

When the user guides it by hand along a line of barcode, the device can read up to 30 in (76 cm)/s of program or data, scanning from either left to right or right to left. It emits a scan tone to indicate that the last line of program or data has been correctly read. An error tone with an error message display, or no tone, means that the last line of code must be rescanned. The display automatically updates itself to indicate the next line to be scanned. It is also possible to scan a line and have it converted into a binary display on the calculator. This feature assures that code is not faulty and is not being misread. In addition, a running program may be halted to allow a subroutine in code to be scanned and immediately executed or stored until called, or to permit one or more rows of coded data to be scanned and used by the program.

Barcode for use with the device is formed of narrow bars, wide bars, and spaces printed on paper, usually black on white. Maximum length of a row of barcode is 132 bars. The wand contains a light emitting diode (LED) and photosensor that detects changes in the light reflected from the sheet being scanned. The detected signal is digitized and translated by two integrated circuits into instructions that the calculator understands. The code offers built-in checksums and ability to handle alphanumeric data.

Users can obtain barcode versions of their software by sending magnetic card or handwritten versions of programs to an independent printer who

will return barcoded data in no more than seven days. For short programs all calculator and peripheral functions can be executed by scanning a barcode sequence on a paper keyboard—a sheet of paper with barcoded versions of the calculator's keyboard or barcode labels that are included with the wand.

Circle 423 on Inquiry Card

Video Imaging Unit Produces Photographic Quality Output

Quality continuous tone copies are produced from raster scan video sources in seconds by the 4634 imaging hard copy unit. Designed by Tektronix, Inc, PO Box 500, Beaverton, OR 97077, the device is a cost-effective alternative to other photographic quality display recording devices for use in digital image processing, pattern recognition, remote sensing, video disc, and high resolution display environments.

The unit records on dry silver paper using a fiber optic CRT, producing copies having a broad gray scale range (12 levels) that reveals fine image detail. The 6 x 8" (15 x 20-cm) image size on 8.5 x 11" (21.5 x 27.9-cm) paper facilitates enhanced interpretation of gray scale information. Approximate copy cost is \$0.20, compared to from \$0.60 to \$5.00/copy for competitive copiers.

Front paper load and paper exit, and front panel controls make it easy to integrate the unit into video system configurations. It is self-contained, usually requiring a single cable connection, and can be interfaced to most analog or digital raster scan video sources. An automatic gain control circuit tracks the input signal making the copier less sensitive to input signal variations. Image quality is thus more consistent over time with minimum adjustment.

Circle 424 on Inquiry Card

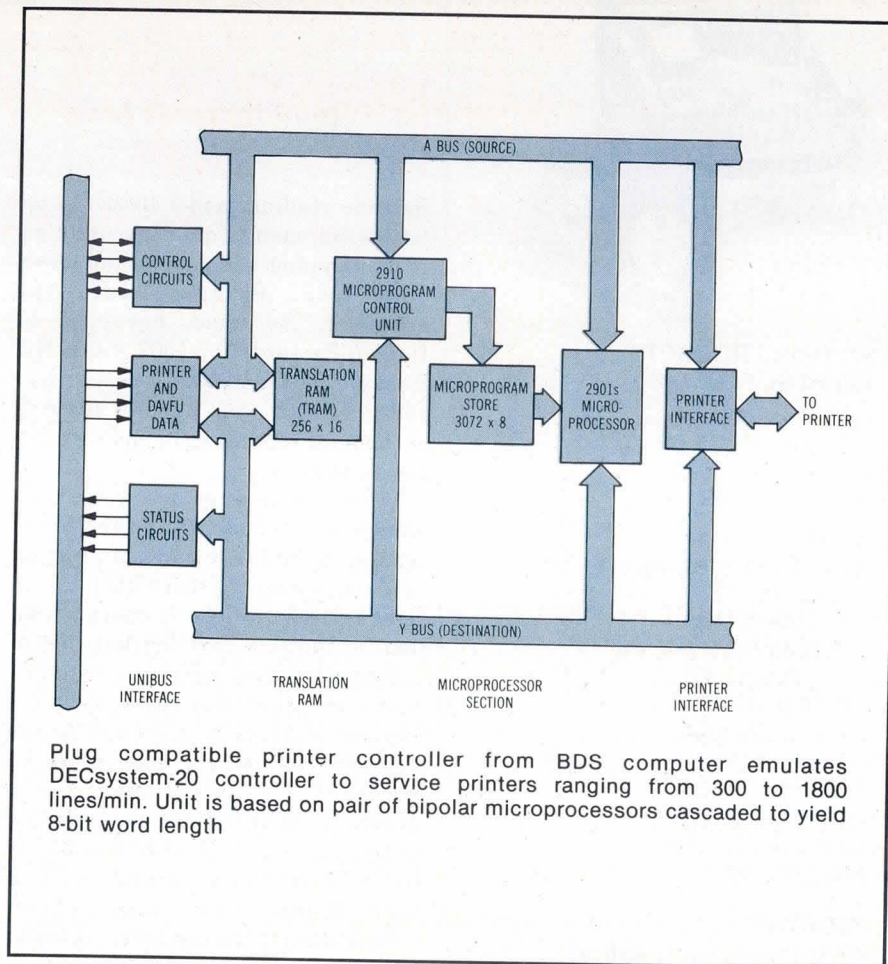
Microprocessor Controlled Printer System Emulates DEC-20 Controller

A plug compatible controller and line of printers extend the range of printing speeds attainable with DEC-system-10 and -20 computers, and are priced about 50% lower than comparable DEC units. Designated LPC-20, the microprocessor based controller requires one and one-half card slots in the utility processor and handles printers with speeds of 300, 600, 900, 1200, 1500, and 1800 lines/min, replacing a DEC controller that uses three slots and services 300- or 1200-line/min units.

BDS Computer Corp, 1120 Crane St, Menlo Park, CA 94025, has made the controller fully software compatible with the the TOPS-20 operating system. It emulates the DEC unit and has the logic and buffers necessary for program controlled or direct memory access data transfer between the Unibus and the line printer. It also includes logic for command, monitoring, and control functions. The complete controller and printer interface are contained on one quad- and one hex-sized board.

A pair of bipolar 2901 bit-slice microprocessors and a 2910 microprogram control unit form the nucleus of the controller. The 2901s are cascaded to give an 8-bit word length. A 256-word by 16-bit translation random access memory (TRAM) holds control and print characters while a 3k-byte microprogram storage P/ROM controls the 2901 data manipulation. All microprocessor instructions are executed in one 200-ns microcycle.

Other logic includes a Unibus control section that provides communications between computer and printer controller. Elements within the controller are linked with an "A" or source bus and a "Y" or destination bus. The A-bus supplies input data to the 2901s and 2910. The Y-bus transfers information from the microprocessors to the printer interface and Unibus interface. Printer interface logic supplies data and I/O control information to the printer.



Plug compatible printer controller from BDS computer emulates DECsystem-20 controller to service printers ranging from 300 to 1800 lines/min. Unit is based on pair of bipolar microprocessors cascaded to yield 8-bit word length

In operation, TRAM is loaded by the computer under program control or with DMA cycles in order to free the CPU for other tasks until an interrupt signals that the buffer is full. The controller's microprocessors control all bus requests, transfers, and handshake signals. In addition, under DMA, it handles the loading of a 12-channel direct access vertical format unit (DAVFU), which designates printer paper advancement and positioning. The system also accommodates 12-channel paper tape DAVFU.

Once TRAM and DAVFU are loaded, the controller releases the Unibus, manipulates TRAM data, and passes it to the printer interface circuits along with appropriate printer control signals. Printing continues until the TRAM is empty, at which time loading begins again.

Serving the DECsystem-10 KL processors or any DECsystem-20, the unit controls any of the company's line printers from 300 to 1800 lines/min, requiring only jumper or cable modifications. Printers employ band, charaband, or drum technology. The 300- and 600-line/min band printers, intended for low to medium speed applications, use a steel band print font carrier, and have an internal microprocessor for printer control, diagnostics, and operator prompting. Drum printers operate from 300 to 1800 lines/min and are intended for high duty cycle printing. The charaband printer is a 1200-line/min unit with a 132-col line width. All printers have a standard 64-char set with 96-char optional.

Circle 425 on Inquiry Card

RELIABILITY. IT'S WHAT MAKES FUJITSU THE WORLD'S LARGEST MANUFACTURER OF OEM WINCHESTERS.

**10,000
MTBF**

That's right! Fujitsu produces more Winchester technology disk drives for the OEM market than any other

manufacturer in the industry. The reason for this success is the unequalled reliability of Fujitsu products.

For instance, Fujitsu's M228X Winchester drive delivers more than 10,000 MTBF power on hours of high performance. That's 40% better than the industry standard. And the M228X is fast: 6ms track-to-track (27 ms average) access time. With this kind of performance, up to 169 megabytes of unformatted storage,

and Fujitsu's competitive pricing—there is no other choice! Optional head-per-track capacity of 655 kilobytes also available with this series.

80 and 50 MB cartridge drives with SMD interfacing

Fujitsu's advanced technology does not stop at Winchester! The two front-loading cartridge drives with SMD capability shown here, have statistics only Fujitsu could guarantee. Like access times of 6ms track-to-track (30 ms average), and a reliability factor of over 6,000 poh MTBF. That's 50% better than the industry standard.

And whether you order the M2211 (80 MB) or the M2201 (50 MB) drive you can say goodbye to data staging. Plus you get a servo/track record system that assures the cartridge interchangeability

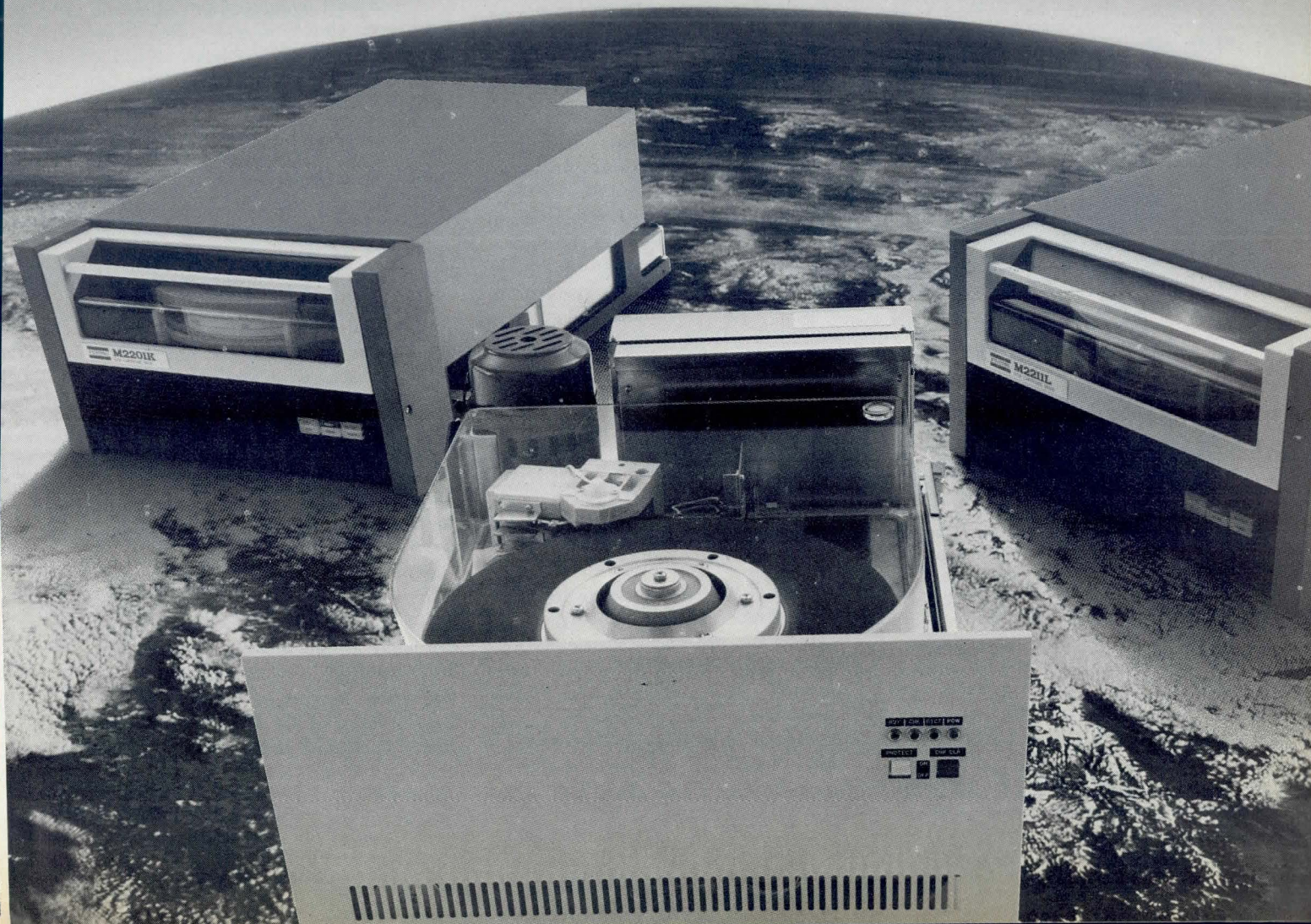
you need. With features like these it's no wonder Fujitsu's got the world on a platter.

For technical information, (outside California only) phone toll-free 800-538-8175. For sales and service, or evaluation unit, contact: Fujitsu America, Inc., 2945 Oakmead Village Court, Santa Clara, CA 95051. Phone 408-727-4300, Telex 171-182, TWX 910-338-0047.



**The first word in reliability.
The last word in performance.**

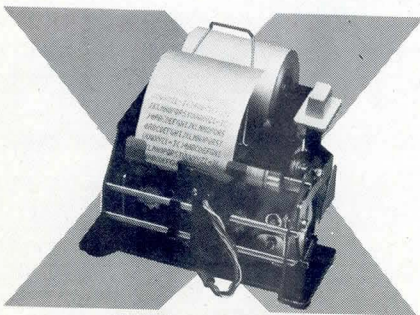
CIRCLE 44 ON INQUIRY CARD



High End Units Raise Performance Levels of Laboratory Computer Family

Several members added to the MINC family of laboratory computer systems incorporate the PDP-11/23 processor to achieve greater capacity and performance than entry level units. Included in the announcement made by the Laboratory Data Products Group, Digital Equipment Corp, Maynard, MA 01754, are the MINC-23, MINC/DECLAB23-RT, and MINC/DECLAB23-RSX systems.

MINC-23 and MINC/DECLAB23-RT enable researchers to configure optimum system elements for specific data acquisition and control applications through use of MINC modules. The MINC-23 is a portable system employing diskette storage, and DECLAB23 incorporates dual 5M- or 10M-byte disc cartridges. DECLAB23



Fast reliable printer.

The DC-1606B/DC-2106D discharge printer prints 16 or 21 column alpha- numerics in a 5 x 7 dot matrix format. Its MTBF is 3.0 million lines on 2.25" paper costing about 3/4¢ per foot. Just 3.8" H x 5.4" W x 5.5" D, it is as low as \$120 in 100 quantity. Other printers with interface electronics available.

Call or write HYCOM, 16841 Armstrong Ave., Irvine, CA 92714 — (714) 557-5252

HYCOM

CIRCLE 45 ON INQUIRY CARD

configurations replace the DECLAB-11/MNC systems (see *Computer Design*, Dec 1978, p 48), providing twice the processor speed and four times the memory capacity.

The MINC-23 extends capabilities of previous members of the family offering at least double the performance of the MINC-11. DECLAB23-RT systems include both floating point and IEEE-488 bus interface as standard items, providing extra versatility in both interfacing and data reduction. All systems can operate on a standalone basis or can be tied to other DEC computers operating under DECnet, using the MINC NFT file transfer software. Such capacity enables establishment of laboratory wide data management and data acquisition systems.

MINC BASIC is used both for individual programs and the operating system on the MINC-23. As an option, the unit can also run RT-11 FORTRAN; MINC/DECLAB23-RT uses RT-11/FORTRAN. RSX uses the RSX-11M multiuser, multi-tasking operating system. All provide full floating point functions as standard.

Minimum configuration for a -23 includes PDP-11/23 processor, MINC box, VT105 terminal, and dual 512k-byte diskette drives. For DECLAB23 configurations, minimum equipment includes PDP-11/23, 10M-byte hard disc, VT105 terminal, and MINC box mounted in a 30" (76-cm) cabinet. Prices range from \$15,600 to \$30,300. First shipments are scheduled for December.

Circle 426 on Inquiry Card

Series 1100 Extensions Increase Capability in Scientific Data Processing

A general purpose large scale computer system suited for scientific and engineering applications, 1100/80S is based on Series 1100 architecture and software, and incorporates a scientific accelerator module, a very high speed LSI bipolar gate array device. Performance of the current entry level 1100/80 system has been increased by at least 25% with the 1100/80S.

Included in a basic /80S are a central processing complex with scientific accelerator module, 524k words of main storage, 4k words of buffer storage, and one input/output unit. The 1100/80S uses 36-bit single-precision floating point representation. Main storage expansion to 1048k words is available. Buffer expansion to 32k words allows additional main storage as well as multiprocessor configurations up to four CPUs, four IOUs, and 8M words of main storage.

Also announced by Sperry Univac, PO Box 500, Blue Bell, PA 19424, was a memory expansion feature for the current 4M-word 1100/80 systems, which permits memory to be added in 2M word increments up to a maximum of 8M words or 32M bytes. Operating in association with 1100/80 computers, a high performance special purpose scientific processor, the Array Processor Subsystem (APS) significantly extends computer capabilities for processing vast quantities of numeric data. The APS increases the speed of floating point arithmetic operations, eliminates data transfer bottlenecks between host computer and scientific processor elements, and solves large multidimensional problems. With a maximum execution burst rate of 120M floating point operations/s (FLOPS) and a sustainable rate for suitable algorithms of 80M FLOPS, the subsystem represents a significant performance increase over earlier systems. Maximum system performance of 245M FLOPS, including host performance, is realized when two units are attached to an 1100/84 system.

Potential data transfer bottlenecks are eliminated by a direct interface to main storage and a high speed cache memory. Together these features ensure that the system is continuously supplied with data and is thus capable of maximum processing efficiency. Data rates between main storage and the subsystem are 35M to 40M 36-bit words/s.

Built using ECL and TTL devices, the unit is user microprogrammable, with a 288-bit instruction word size. Data words are 36 bits and all arithmetic is fully compatible with the /80 host. Capability to execute memory problems as large as 8M words in a single vector operation enables the unit to process large multidimensional problems.

Circle 427 on Inquiry Card

See SCOUT save.

SCOUT™ has a red light. It does not mean what you think. The red light says one of SCOUT's boards does not feel well.

Will this make you sad because your minicomputer can't play anymore?

Will the expensive repairman take a long time to get it fixed?

No no, silly. Since SCOUT's ISOLITE™

showed you which card is bad, all

you do is pull it out and put in a spare 6.25" x 8.3" card.

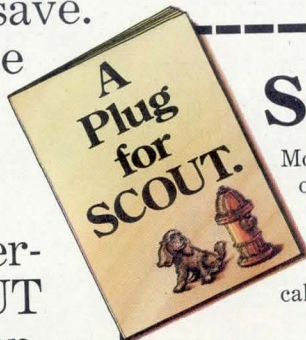
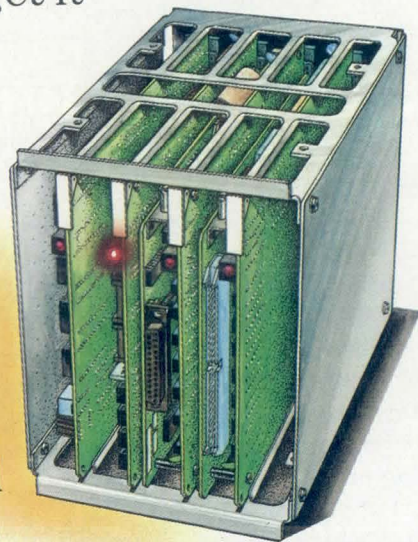
What fun! Now SCOUT can run and play again. And save you a lot of jack.

Save SCOUT, save.

Save on service costs. Save on system costs.

Save on 16-bit minicomputer performance. SCOUT starts at less than \$1000 for a CPU, I/O, 32K Byte RAM and card cage.

Isn't saving fun? Save SCOUT, save.



See SCOUT save.

Money. Time. And end user aggravation. Plus other ways to save in our how-to-save-on-maintenance primer, *A Plug for SCOUT*. Get your free copy with this coupon and a business card. Or, for immediate information call 714/833-8830, Ext. 455.

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Company _____
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Computer Automation

NAKED MINI® Division

Where OEM's come first.

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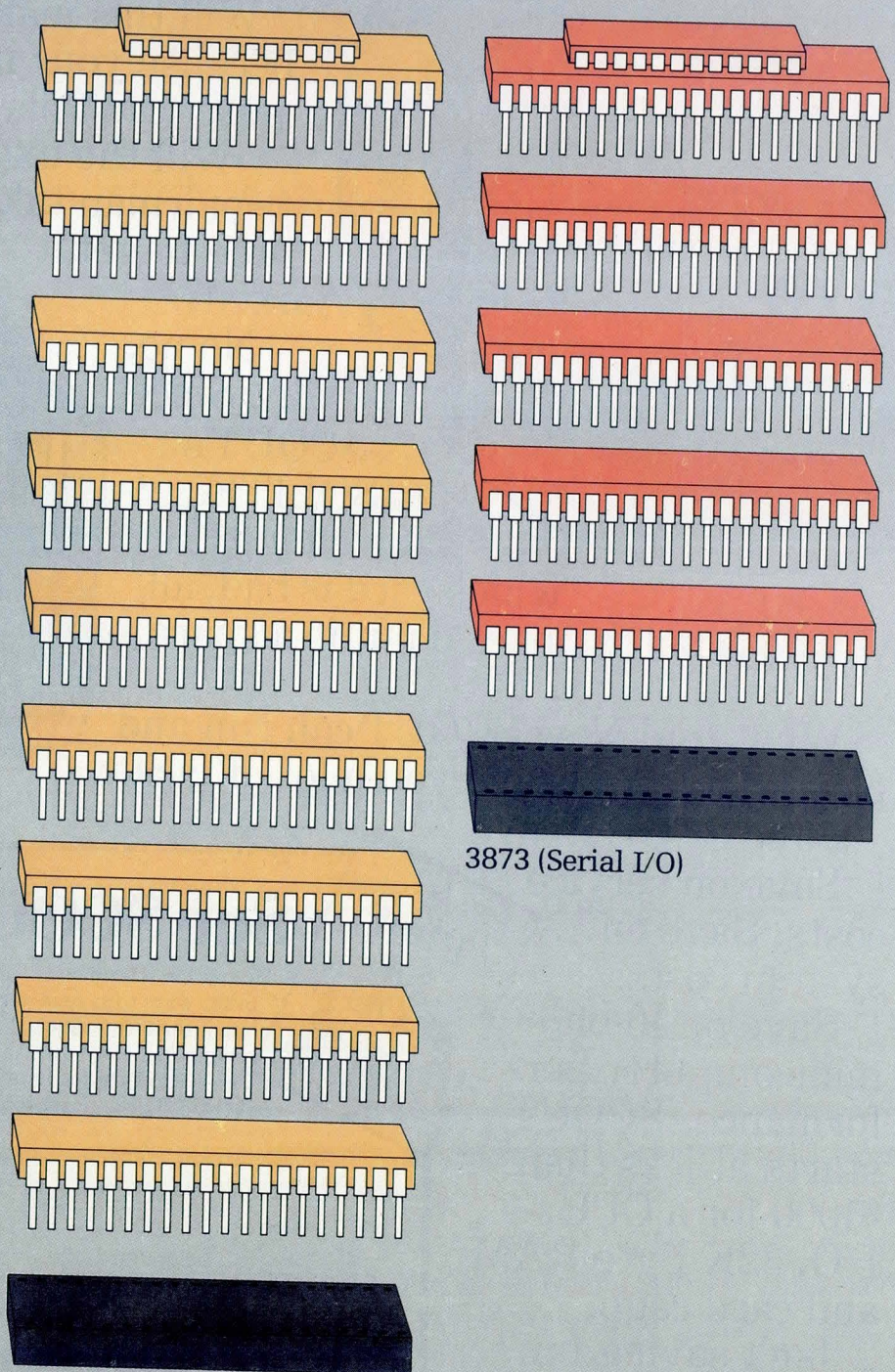
3870 momentum continues.

For single-chip applications, no other microcomputer family offers you more design momentum than the 3870 family from Mostek. Now there's even more momentum because eight new parts give you ROM and RAM options never before available. A total of 16 choices. You save by buying only what you need now, yet you'll also be designing in future flexibility.

That's because all our 3870 microcomputers are software compatible and basically pin-for-pin hardware compatible. So expansion or upgrading from 1K ROM to 4K ROM can be as easy as exchanging one 3870 device for another. In the same socket. There's no new architecture to learn. No retooling of artwork. No new vendors to qualify. In other words, there's no loss of design momentum.

This ongoing product line expansion is all part of our commitment and response to your unprecedented demand for Mostek 3870 microcomputers. A demand so strong for so many different applications that we literally ran out of 3870 numbers for all the variations you requested.

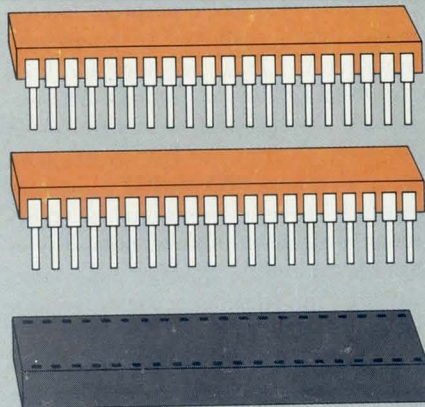
So to simplify identification of all our 3870 devices, we developed an expanded, easy to understand numbering system. In this system, the first four numbers designate three generic families: MK3870, MK3873, and MK3875. All three families have multiple combinations of ROM and RAM. The first slash number indicates the amount of ROM available in 1K byte increments; the second slash number identifies the amount of executable RAM in multiples of 32 bytes.



3870

8 new ROM and RAM options give you 16 compatible single-chip choices.

MOSTEK.



3875 (Battery Back-up)

Designation	ROM (bytes)	Executable RAM (bytes)	Parallel I/O (bits)	Special I/O	Old Part Number
MK3870/10	1K	0	32		• New
MK3870/12	1K	64	32		• New
MK3870/20	2K	0	32		MK3870
MK3870/22	2K	64	32		MK3876
MK3870/30	3K	0	32		• New
MK3870/32	3K	64	32		• New
MK3870/40	4K	0	32		• New
MK3870/42	4032	64	32		MK3872
MK3873/10	1K	0	29	SI, SO, SCLK	• New
MK3873/12	1K	64	29	SI, SO, SCLK	• New
MK3873/20	2K	0	29	SI, SO, SCLK	MK3873
MK3873/22	2K	64	29	SI, SO, SCLK	• New
MK3875/22	2K	64	30	V _{SB} , V _{BB}	MK3876/w Standby
MK3875/42	4032	64	30	V _{SB} , V _{BB}	MK3872/w Standby
MK38P70/02	External	64	32		MK3874
MK38P73/02	External	64	29	SI, SO, SCLK	MK38P73

387X/XX

Generic Part Type

Amount of ROM in 1K increments
 1 = 1K
 2 = 2K
 3 = 3K
 4 = 4K

Amount of executable RAM in 32 byte increments
 0 = 0
 2 = 64 bytes

Since all our 3870 devices have 64 bytes of scratchpad RAM, that portion of the memory isn't included in the part number.

The basic Mostek 3870 microcomputer family, with 32 bits (4 ports) of parallel I/O, presently has 8 versions. ROM options range from 1K to 4K bytes with an executable RAM option of 64 bytes.

MOSTEK®, Matrix, MK3870, MK3873, MK3875, and P-PROM are trademarks of Mostek Corporation © 1980 Mostek Corporation.

The Mostek 3873 family has 29 bits (4 ports) of parallel I/O plus a hardware serial I/O port capable of handling either synchronous or asynchronous data transfers. Two different ROM versions are currently available, and executable RAM options are coming soon.

The MK3875 microcomputer family features 30 lines (4 ports) of parallel I/O and a standby power mode to protect the executable RAM during low-power situations. Both our 3875 versions have 64 bytes of executable RAM; ROM is 2048 bytes or 4032 bytes.

Unique to the entire 3870 line are our piggyback EPROM (P-PROM™) microcomputers. Designated MK38P70/02 and MK38P73/02, these devices let you prototype and field test your software programs prior to ordering masked-ROM versions. P-PROM microcomputers are also ideal as production circuits in low volume applications.

To simplify software as well, choose our Matrix™ floppy disk development system with real-time in-circuit emulation. The Matrix system can support our entire 3870 line, including low power CMOS versions now being developed.

Three basic 3870 families. EPROM versions. And comprehensive software tools to back it up. It all adds up to more momentum. The kind of momentum that can simplify your design, and extend your product life. To find out how, call or write Mostek Corporation, 1215 W. Crosby Road, Carrollton, Texas 75006; phone 214/323-1000. In Europe, contact Mostek Brussels; phone 660.69.24.

How to Improve Your Image



The Problem: Glare. And poor image-to-background contrast. They wash out displayed information, cutting operator efficiency and lowering productivity.

The Solution: OCLI Contrast Enhancement. It reduces glare by 17 to 1 over untreated glass. It's working now for some of the biggest names in display technology, including IBM, Four-Phase and Tektronix. Write us. We'll explain how it can work for you.

I'd like to improve my image.

Tell me more about OCLI Contrast Enhancement for CRTs.

Name: _____

Title: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____

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CD-80

TECHNOLOGY REVIEW

Portable ASR Terminal Uses Bubble Memory For Nonvolatile Storage

Execuport 4000B is a multi-microprocessor based portable ASR terminal that provides a keyboard and nonvolatile bubble memory for both offline and online operations. The terminal, developed by Computer Transceiver Systems Inc, E Midland Ave, Paramus, NJ 07652, operates similarly to a conventional teletypewriter with the additional capability of bubble memory storage and text editing for data preparation and manipulation.

Containing one or two magnetic bubble memory (MBM) devices and a flexible easy to use operating system firmware package, the unit is capable of asynchronous serial binary data interchange. A powerful editing feature enhances the terminal's use as an offline data entry and storage unit. A buffer within the terminal enables interactive communications in bursts at programmable rates up to 9600 baud, via an RS-232 acoustic coupler.

Each memory device is capable of holding 11,538 bytes of data. The standard terminal has one resident, nonremovable MBM device; an optional cassette-like removable MBM located on the keyboard raises capacity to over 23k bytes. Usable data capacity is arranged in 641 sectors or pages. Numbered 0 through 640, each sector is 18 characters long, and is the smallest unit of memory accessible by the operating system.

Data stored in user available memory are organized in files. A record is kept for each file in a memory directory which maintains and prints file name, first sector position, number of sectors, and attribute (protection level of file) as directory information. By implementing various commands one at a time or chained, the operator can perform various operations, including create and delete files, merge and extend files, and edit files, clear memory, copy one memory to the other, print directory, and print terminal communications configuration.

TECHNOLOGY REVIEW

A full ASCII keyboard with upper and lower case and ASCII/APL special function keys is organized in typewriter format for efficient operation by nontechnical personnel. Editor commands entered from the keyboard allow existing files to be modified and new files to be created within the bubble memory. The editor is initiated by entering command mode and keying in the edit command. Commands can be grouped into two major categories:

pointer moving commands, and text display and manipulation commands.

The virtually silent thermal printer operates at 40 char/s on 136 columns. Features include printhead position indicator LED, built-in self-test, bidirectional one-quarter line step plotting, true upper and lower case characters, and single or double vertical spacing. The nonimpact printer outputs 5 x 7 dot matrix characters 0.110" high x 0.080" wide (2.79 x 2.03 mm).

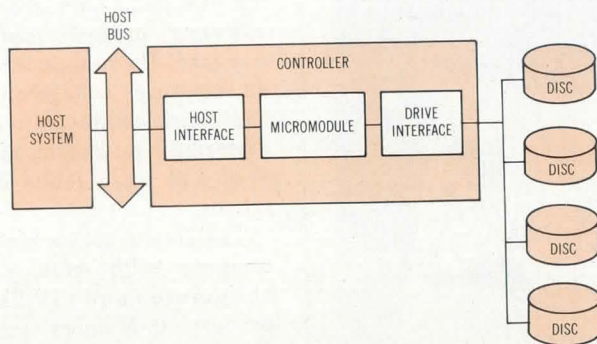
Terminal design makes its use ideal for the field. Weighing just 17 lb (7.6 kg), it is readily transportable and is sized to fit conveniently under an airline passenger seat.

Circle 428 on Inquiry Card

Micromodule Based Controllers Cut Costs of Winchester Disc Storage

Micromodule 9000 contains all essential common functions of a universal controller in less than one-eighth the

space of previous designs. All that is needed to incorporate the unit into a system is the addition of interface capability for host computer and disc drive. Microcomputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086, designed the module in answer



Micromodule 9000 developed by Microcomputer Systems contains all central common intelligence necessary to control Winchester disc units, reducing chips necessary to implement system from 200 to less than 25 to increase reliability and reduce cost

to the industry's search for a low cost, high volume intelligent controller that can be easily customized to link most small computers with 8" (20-cm) Winchester discs.

The design reduces the number of chips in a complete disc controller system from about 200 to typically less than 25. This results in far greater reliability, saves valuable space in system design, and leads to manufacturing efficiencies and significantly lower prices. The compact 3 x 3 x 0.6" (7.6 x 7.6 x 1.5 cm) module is housed in a 40-pin DIP, ensuring easy integration even when space restrictions are stringent. Power consumption is 7 W.

Data integrity is assured by the module's ability to detect 22-bit burst errors and to correct bursts of up to 11 bits. The controller also provides read with implied seek, write with implied seek, format full track, and recalibrate functions. A full sector data buffer allows flexible data rates without affecting data transfer integrity. Overlap seek capability is provided to enhance multiple drive performance. Automatic verification of position ensures data base integrity.

Other functions performed by the module include disc control and data handling, serial/parallel conversions, and high level command communication such as read, write, and format. It also monitors and provides status indication of disc functions.

To incorporate the unit into a system, host and drive interfaces must be provided. The host interface supplies electrical and logical interfaces tailored to the host bus. Consisting of 5 or 15 ICs, it also provides termination or filter networks unique to the host bus. The drive interface serves to multiplex signals for multiple drives and provides driver and receiver circuits that match impedance characteristics of the disc bus.

First use of the module is with the Memorex 101 Winchester drive. The company will incorporate the module into a controller PCB system tailored to OEM applications. This board may then be supplied complete or manufactured by the OEM.

Circle 429 on Inquiry Card

TECHNOLOGY REVIEW

Digital In-Circuit Tester Has 2400 Point Capacity To Handle Large Boards

FF323 offers full LSI, MSI, and SSI testing of large circuit boards with integrated hardware and software, and optional 2400 test point capacity. Fairchild

Camera and Instrument Corp, Subassembly Test Systems Div, 299 Old Niskayuna Rd, Latham, NY 12110, designed the tester for use in the main-frame computer and peripherals market where large boards represent a significant investment and the manufacturing process is typified by high reject rates.

The standard test unit, equipped with a 1200 test point capacity, offers low cost per point. In the 2400 test

point configuration it has more than twice the capacity of any other system. Thirty-two point switching modules may be added, allowing economical expansion as test point requirements increase. The switching system has been engineered for optional driver/receiver characteristics with minimal noise and crosstalk.

SSI and MSI tests are executed in flexible single-user BASIC and a complete library of small and medium scale devices is available on the system's hard disc storage. Universal LSI testing routines, such as cyclic redundancy check and transition counting, accommodate LSI devices from microprocessors to memories. LSI testing procedures execute independently of BASIC through a high level compiler, CHIPS, and utility software which links the LSI tests to the BASIC management program. LSI test procedures can be easily altered and special user generated tests added to the library. Automatic program generation, data log analysis, and utility programs engineered for high throughput at the test station are all standard.

Measurement hardware has been designed specifically for digital board testing. Digital stimulus driving capability is 500-mA (source) and 350-mA (sink) current. Software verification, CRC, transition counting, and gray code generation circuitry have been integrated into the measurement system. Switching modules feature controlled impedance to maintain test point homogeneity.

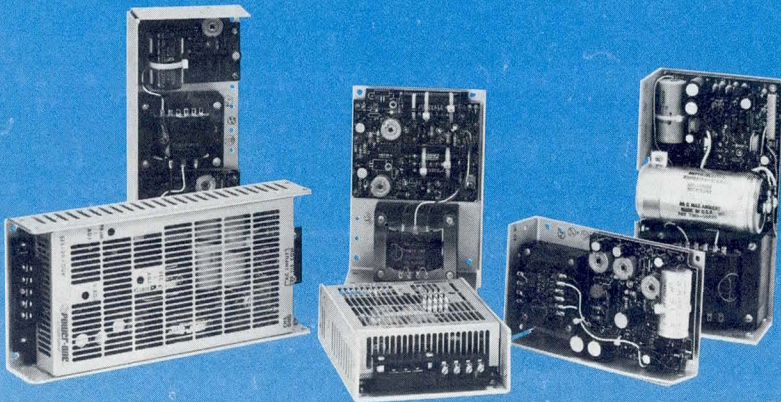
Analog in-circuit measurement is standard. Dc voltage level, resistance, dc measure voltage/source current, and shorts/continuity testing may be performed to isolate analog component and trace faults on digital PC boards.

The system uses a high speed mini-computer with multiaccumulator architecture and 19.2k-baud rate primary I/O. Memory cycle time is 400 ns. A 10M-byte cartridge disc subsystem provides program and data storage. Optional peripheral equipment supports a wide range of testing applications. Housed in a table height, 4½-bay cabinet, the system includes a test results printer, operator's control console, video display terminal, and Thinline[®] receiver.

Circle 430 on Inquiry Card

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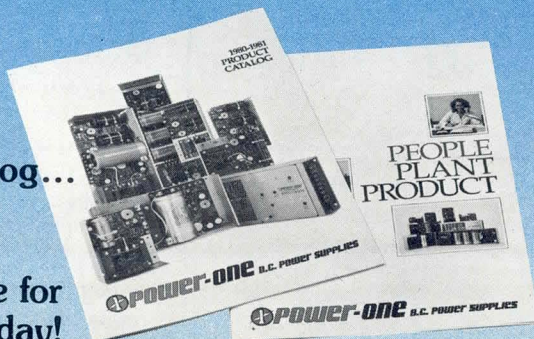
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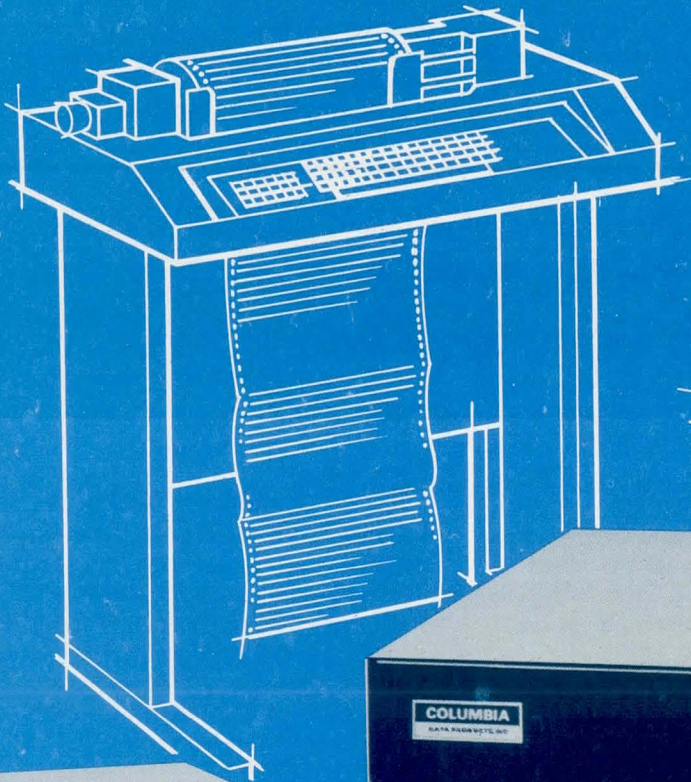
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CIRCLE 50 ON INQUIRY CARD

Conferences to Cover Electronic Components, Computer Science

Theoretical computer science will be the subject of the 8th International Colloquium on Automata Languages and Programming, scheduled for July 13 to 17, 1981, in Technion City, Haifa, Israel. Sponsors of the meeting—the European Association for Theoretical Computer Science—are seeking original contributions for presentation.

Papers covering automata theory, formal languages, analysis of algorithms, computational complexity, and computability theory are invited. Other subjects of interest include mathematical aspects of programming language definition, semantics of pro-

gramming languages, program verification, theory of data structures, and theory of data bases.

For consideration submit four copies of an extended abstract or full draft paper before November 15 to the Chairman of the program committee: Prof S. Even, ICALP 81, Computer Science Dept, Technion, Haifa, Israel.

Sponsored by the IEEE Components, Hybrids, and Manufacturing Technology Society and the Electronic Industries Association, the 31st Electronic Components Conference is slated for the Colony Square Hotel in Atlanta, Ga, from May 11 to 13, 1981. For this meeting, papers discussing recent developments in the areas of passive, active, and connector components, thin and thick film hybrids,

assembly, packaging, testing, and computer aided manufacturing are being solicited.

To be considered submit 10 copies of a 500-word abstract or extended outline describing the scope, content, and keypoint of the proposed paper by November 15. Send to T. G. Grau, Bell Telephone Laboratories, Rm 3B-312, Whippany Rd, Whippany, NJ 07981.

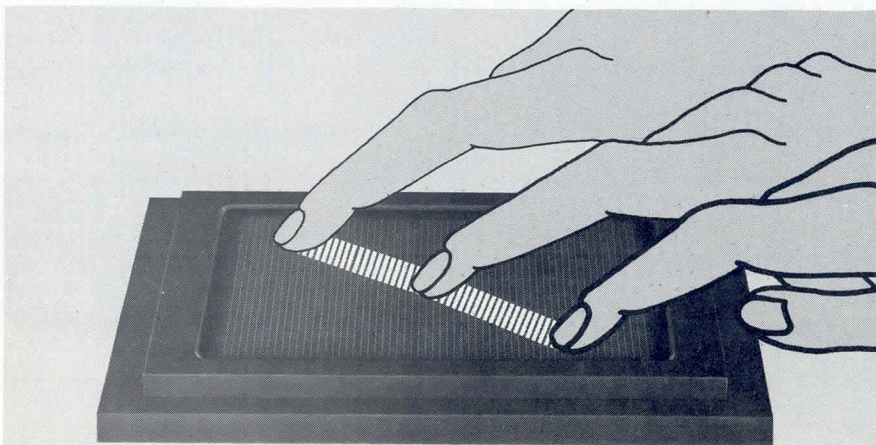
Information System Includes Tutorial Programs And Application Software

C. A. T. (Computer Aided Tutor) is a system composed of computer and display keyboard, printer, financial accounting packages, word processing package, inquiry and reporting system, and data diskettes. By packaging together self-teaching tutorial software and hardware designed specifically for the small businessman, CADO Systems Corp, 2771 Toledo St, Torrance, CA 90503, has enabled entry level users to start with no extra cost items.

A dual-tasking machine that will perform two tasks such as data entry and printing simultaneously, the computer is equipped with 32k bytes of RAM storage and two dual-density diskette drives, each storing 620k bytes. The system incorporates a CRT displaying 24 lines of 80 characters and a separate 96-char ASCII keyboard. Basic is a 150-char/s matrix printer; a letter quality unit that operates at 55-char/s is optional.

Software included with the system consists of accounts receivable/payable, billing, inventory, payroll, and general ledger packages. The word processing package handles correspondence and documentation. The Just Ask II inquiry and report writing program interprets unformatted English language inquiries, sorts lists, and prints reports in requested formats. Tutorial packages stored on diskettes are provided for each package.

Circle 431 on Inquiry Card



A new X-Y controller that operates from fingertip glide

A lower-cost, long-life alternative to trackballs, joysticks, light pens, etc.

With this new X-Y controller all you do is slide your fingertip in the desired direction.

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The PM3500 100MHz 16 Channel Logic Analyzer

- Performs state and timing analysis both synchronously and asynchronously.
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- Digital delay of up to 9999 clock pulses.
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For more information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, New Jersey, 07430.



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Our new HP 1000 L-Series is designed to give you outstanding processing performance—even in the most demanding applications.

The reason is our innovative distributed intelligence architecture. Each I/O interface has its own processor—made with our exclusive SOS LSI process—and its own direct memory channel. Which means each interface can control and monitor data transfers—without interrupting the central processor.

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And you get faster response, higher throughput and superior system performance.

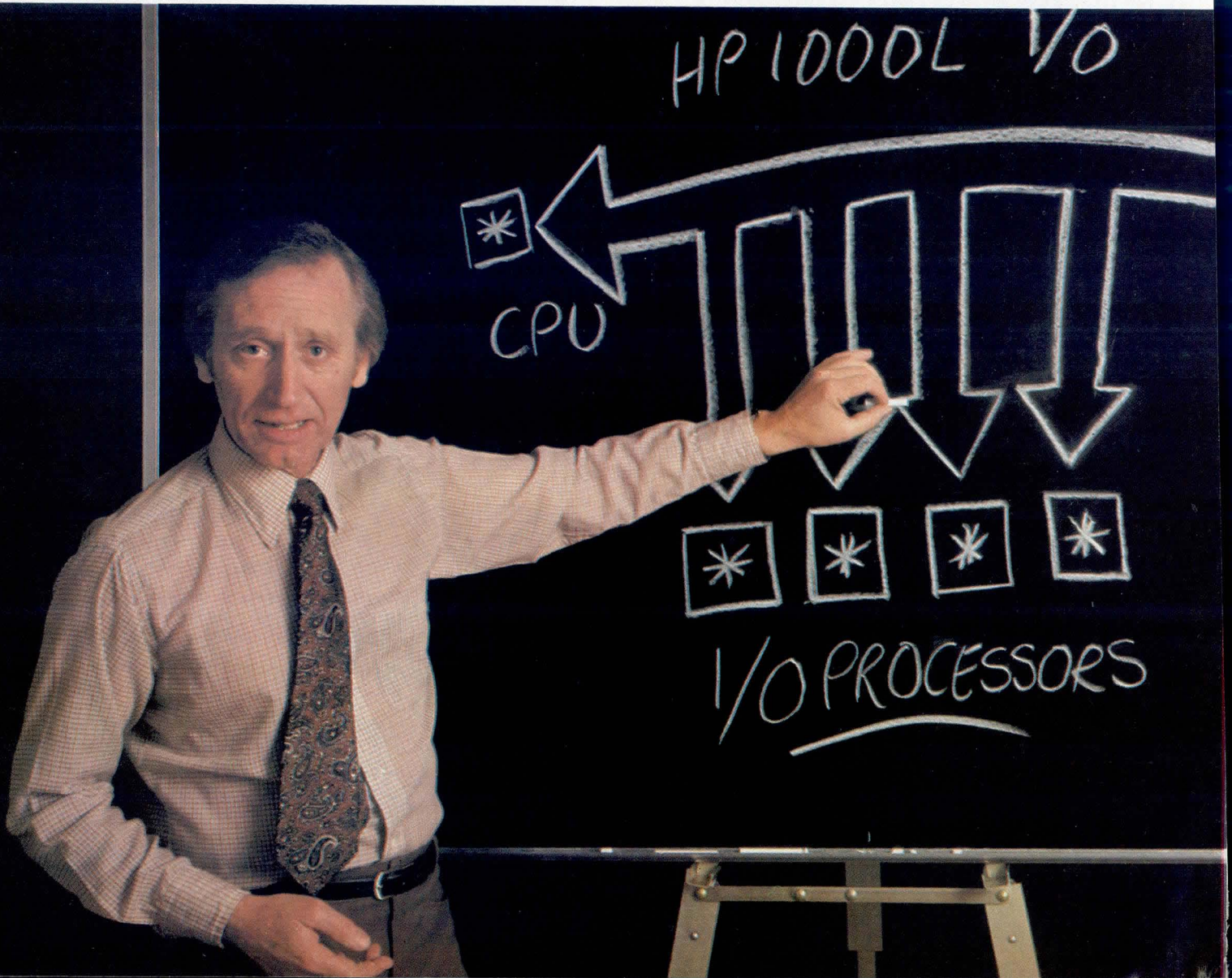
But what's really surprising about the L-Series is that you get all this performance at prices

that start as low as \$1968 for our starter set.† Or \$15,510 for a complete disc-based system.††

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makes processors
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The key to the HP-1000 L-Series' impressive new architecture is our own Silicon-On-Sapphire technology. SOS lets us make CPU and I/O chips with extremely high circuit density, low power consumption, high processing speeds and high reliability—at a very low cost.

It's this combination of high performance and low cost that make the L-Series appropriate for the whole range of OEM and industrial appli-



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CPU concentrate on computation.

cations — including data management, process control and instrumentation.

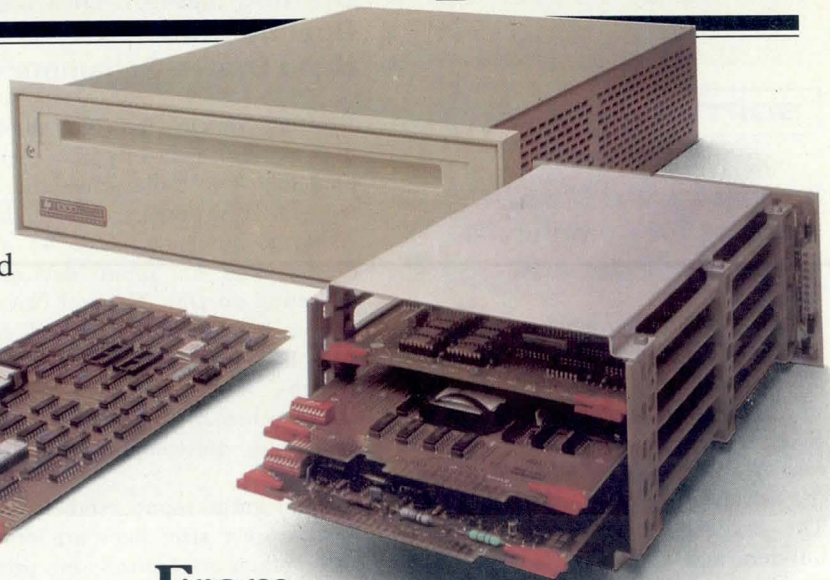
And to insure you can get the exact configuration you need for your specific application, the L-Series is available in a wide choice of board, box and system packages.

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fewer things can go wrong. In addition, the L-Series has its own self-test programs and diagnostics.

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† Starter Set: CPU, 64KB memory, one I/O board.
†† Disc-Based System: HP's new 12MB Winchester disc drive and 2621 display console.
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CIRCLE 53 ON INQUIRY CARD

SOFTWARE

Business BASIC Meets Demand for Commercial Language Under AOS

Business BASIC programming language is being offered by Data General Corp, Rt 9, Westboro, MA 01581, for use with computer systems as large as Eclipse^R Data Systems and as small as microNovaTM systems operating with the advanced operating system (AOS). The language benefits both system builders and end users because it is easy to use, yet provides sophisticated capabilities for complex business demands. Many users prefer BASIC because it has multiterminal capabilities and allows concurrent development and execution regardless of operating system or processor.

AOS Business BASIC features multiple-keyed, indexed sequential file access, dynamic record allocation, screen management, common area, direct block I/O, and IF-THEN-ELSE logic, which make the language appropriate for developing business applications in a wide variety of commercial environments. Business BASIC utility programs simplify program development, optimize program size, and offer ability to sort files, to build, initialize, and print indices, and to rebuild index files. It also includes extensive utilities for producing printed output for documentation purposes.

AOS offers multifunction features for up to 64 users to develop or execute combinations of applications supporting multiple concurrent activities such as batch, timesharing, and/or realtime tasks. Multiprogramming capability lets multiple users perform a mix of functions including enter, test, debug, or execute programs.

Software fee for the initial license including installation, one year software subscription service, one year comprehensive support service, and one training credit is \$6100. Deliveries are 120 ARO. Quantity and OEM discounts are available.

Circle 432 on Inquiry Card

Drafting System Digitizes Directly from Hand Drawn Schematics

Drafting System One (DS1) allows the user to digitize directly from the scribbled logic/electronic schematic drawings initially prepared by engineers. Using a Summagraphics 42 x 60" digitizer as an input device, and operating on Data General Nova and Eclipse RDOS machines, as well as DEC VAX, IBM, Univac, and Control Data systems, the system can digitize a D-size schematic in 1 to 1.5 h max depending on complexity and associated text.

Upon initial input, symbols are not their correct size, lines are crooked, and symbols are typically not properly aligned. In processing the digitized data, the software system, developed by Design Aids, Inc, 1661 E Chapman Ave, Suite 1F, Fullerton, CA 92631, straightens the crooked lines, inputs correct size symbols in specified rotation, and adheres to alignment among symbols previously implied by the user during input.

On a Nova 4X CPU, processing time is approximately 7 min, after which the drawing data are automatically spooled directly to the plotter. Digitizing, processing, and plotting occur simultaneously. Six digitizers can be active with no system degradation.

To edit a drawing, the user simply tapes the drawing back onto the digitizer, touches alignment points, and within 10-min maximum digitizing time completes changes or additions. The user merely indicates whether a change is a label change, symbol addition or deletion, line addition or deletion, or an alignment change. The system spreads the drawing to incorporate new symbols or make room for additional text. The parameter file, resident on the CPU, controls lettering sizes, line spacing, protected areas around symbols as well as a myriad of other items. The system always uses minimum drawing room and always centers the drawing on the format chosen.

When the drawing has been edited and is correct, the user automatically obtains a connection net list, or bill of materials. Data produced from this process can drive a wirewrapping or PC

board routing system. After routing is complete, back annotation can be performed to assure totally correct documents.

Circle 433 on Inquiry Card

Multitasking System Uses Extended Memory Capabilities of PDP/LSI-11

TSX-Plus, a high performance, multitasking timesharing operating system for DEC PDP-11 and LSI-11 with extended memory hardware has been announced by S & H Computer Systems, Inc, 1027 17th Ave S, Nashville, TN 37212. The system provides the support and functionality of RT-11 to multiple users.

Designed to take full advantage of the 256k of memory now available on many PDP-11 and LSI-11 computers and to allow larger job partitions than previously possible, the software replaces the RT-11 monitor rather than running in conjunction with it as does standard TSX. (A RT-11 license is still required, as RT-11 utilities and handlers are used.) The product partitions memory, allowing a maximum address space of 56k for each of the maximum of 30 jobs supported by the system.

Hardware requirements are a PDP-11 or LSI-11 with memory management hardware and at least 96k of memory. Terminal interface is via DLV11-J, DL-11, and DZ-11 communication lines. Dial-up and hardware lines are supported.

Job priorities are handled by an event driven job scheduling system that uses five user-adjustable time-slice values to control job execution. Other system features include a transparent spooling system that schedules printing based on form names associated with print files, a shared file record locking system to synchronize access to shared files being updated by multiple users, an interjob message communications facility whereby messages may be sent between running jobs, a virtual timesharing line facility allowing one terminal to control several simultaneously running jobs, and a log-on and usage accounting facility that controls disc and file access based on log-on user number. □

Circle 434 on Inquiry Card

MAKE YOUR SMART TERMINAL SMARTER.

Automatic Date/Time Entry. Simply install the SLC-1 Time Machine between your computer and terminal and it will automatically log the correct date and time of each transaction into your computer. The SLC-1 Time Machine will save you money, both in reduced operator time and the elimination of costly human errors.

The Time Machine contains a precision 24-hour clock and a 100-year self-correcting calendar that automatically adjust for leap years. Time and date functions include: hours, minutes, seconds, day, month and year.

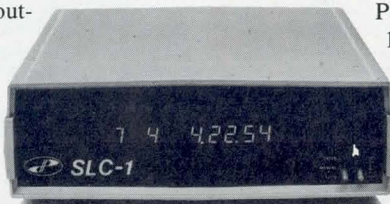
But the SLC-1 is more than a clock. It constantly monitors the output from any computer and provides instant responses to a number of user-defined key

phrases. This makes it ideal for use with unattended process control or data acquisition systems. And since the Time Machine is a 6502 microprocessor system, it adds computing power to any terminal.

The Time Machine is easily installed without modification to your operating system. Both RS-232 and 20mA current loop serial link are provided. And because it's battery-supported, the time will always be correct, even after a power failure.

The single quantity price is only \$640. Ten-digit display option, \$190. For more information or literature on the SLC-1 Time Machine, contact Digital

Pathways, Inc.,
1260 L'Avenida,
Mountain View,
California 94043, or
phone (415) 969-7600.



**GET INTO THE TIME MACHINE.
DIGITAL PATHWAYS**

CIRCLE 169 ON INQUIRY CARD

Anyone can build great performance into a micro.
Only Digital helps you get it all out.



This Bridgeport CNC Vertical Milling Machine, controlled by Digital's powerful LSI-11/2 microcomputer, is cutting production times for customers by up to 85%.

In 16-bit micros, great hardware doesn't guarantee great performance.

You need high-powered software too.

And only Digital gives you both.

Because while everyone else is just getting started in high-performance micros, we've been shipping them for years.

So we give you all the software tools you need to make the most of great hardware.

We start where the others leave off.

Digital's LSI-11/23 micros offer the only double-precision floating point processor in the industry. Built right into the hardware so it doesn't cost you memory overhead.

You also get a memory management unit so efficient, you can run several real-time programs at once.

And you get the basic instruction set of our PDP-11 minicomputer family. It can do in one memory cycle what others would take four to accomplish.

But like we said, hardware is only half the story.

The industry's only high-performance micro software.

Digital's software systems are literally years ahead of the competition.

The RSX-11M operating system, for example, is the industry-standard real-time software for superminis.

Proven and refined over five years. And you can get it with our LSI-11/23 micros, with high-powered languages like an optimized FORTRAN IV-PLUS compiler and BASIC-PLUS-2.

And for your run-time software you can use RSX-11S, a streamlined version of 11M that takes up an incredibly small amount of memory.

Advanced development tools.

Digital's programming tools are easily the most advanced in the business. So you can concentrate on refining your application software, instead of struggling with it.

For example, you get an interactive debugger that's built right into the processor. With English diagnostics for the linkage editor, FORTRAN, and even MACRO, so you can catch bugs before your programs ever run.

And if you ever need help in your development work, Digital's Command Language will help you solve your problem with clear, English-like statements.

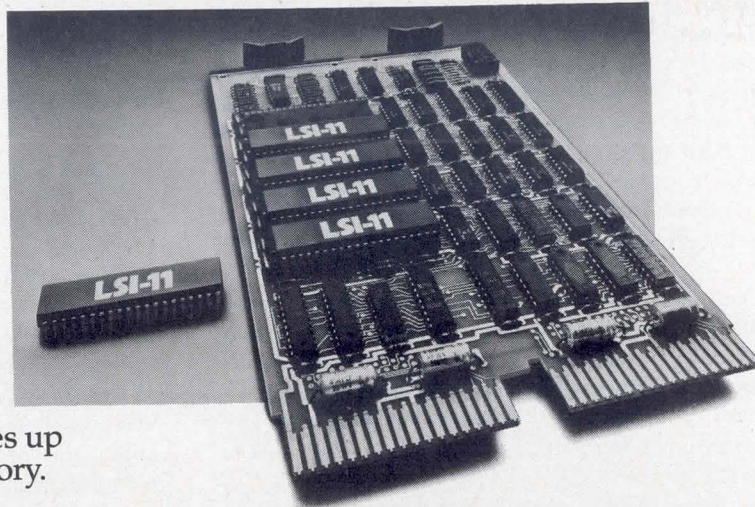
The total approach to micros.

At Digital, we look at micros with a systems understanding. Which is why we offer our microcomputer family — in boards, boxes and systems — with the most advanced high-performance software in the industry.

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For more information, contact: **Digital Equipment Corporation**, MR2-2/M65, One Iron Way, Marlboro, MA 01752. Or call toll-free 800-225-9220. (In MA, HI, AK, and Canada, call 617-467-7000.) In Europe: Digital Equipment Co. Limited, Acre Rd., Reading, RG2 OSU, England. In Canada: Digital Equipment of Canada, Ltd. Or contact your local Hamilton/Avnet distributor.



It took the minicomputer company to make micros this easy.

digital

Automated PCB Design Documentation Reduces Development Time and Costs

All stages in the development of electronic systems—from functional design through acceptance testing at the end of the production line—will eventually be controlled or supported by computers. Necessary hardware and software technologies are already available and, under pressure of steadily rising costs in all areas, the economic benefits of maximum computerization are becoming more and more attractive. Ultimately, too, the three major stages of development automation—computer aided engineering, computer aided documentation, and computer aided manufacturing—will be linked in one integrated computer system.

Many electronics development firms have already taken the first steps in computerization. Computers are widely used in circuit design and analysis, computer based digitizers automatically generate artwork for printed circuit boards (PCBs), and numerically controlled machines and computer controlled fabrication processes are common in manufacturing plants.

However, these systems are often independent of each other and most of the transfer, adaptation, and interpretation of shared information is done by people. Manual operations remain—generating schematic drawings in particular—that are inherently slow and expensive and too often introduce errors and inconsistencies into the development process.

Bell-Northern Research's Circuit Pack System automates and integrates all elements of computer aided documentation for PCBs. The system was implemented in the company's laboratories more than two years ago and made available to other electronics firms in early 1979. Design of

the system eases further integration back from computer aided documentation into computer aided engineering (CAE) and forward into computer aided manufacturing (CAM). More recently, the company introduced two software modules that provide CAE and CAM functions interfacing directly with the circuit design system.

System Structure

The circuit design system consists of computer software and functional procedures for the three major elements of computer aided documentation: design capture, board layout, and documentation. Its purpose is to provide each development group with the computer based tools it needs to perform its documentation functions. Activities of these groups are coordinated through their access to common symbol and component libraries and to a single file of information about the product as it evolves from concept through manufacturing. Basically, the system is concerned with developing only electronic hardware (not the software that makes it work) and only at the level of the PCB (or, technically, the printed circuit pack, which includes the board and all components assembled to it).

Five major functional modules—design capture, PCB layout, library control, documentation, and design file—make up the system (Fig 1). Each module, with its backup software, interacts with the others to maintain the system. In addition, the system provides automatic data validation, in that design information that has been captured and stored in the design file is controlled to maintain accuracy and consistency throughout.

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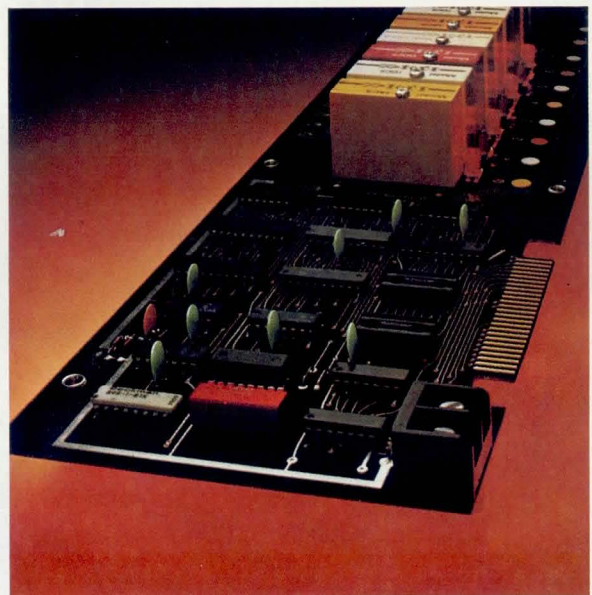
Dark, illegible markings at the bottom of the page, possibly bleed-through or scanning artifacts.



ADDRESSABLE I/O SYSTEMS FROM OPTO 22



(PB 16S1)



(PB 16P1)

Huntington Beach, California . . . Opto 22, originators of the industry standard I/O system, announces the second generation in I/O Systems in both serial and parallel configurations.

SERIAL ADDRESSABLE RACK (PB 16S1)

Communication with multiple input/output stations.
32 station address capability per serial loop.
Up to 16 power I/O modules per station.
Switch selectable baud rate.

Opto 22 provided firmware includes message protocol, event counter, self test, watch dog timer and more.

Plug in modules provide choice of:

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2. RS 422 Balanced Differential Drivers and Receivers.
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4. RS 232

PARALLEL ADDRESSABLE RACK (PB 16P1)

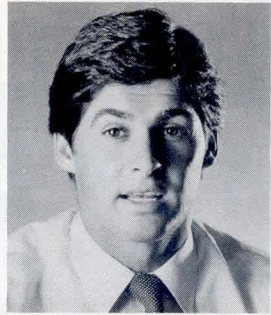
Bidirectional Communication with input or output modules.
64 station address capability.
Up to 16 Power Input/Output modules per station.
50 Conductor Daisy-Chain cable connects all racks to host controller.
On-board station address select switch.

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(714) 892-3313

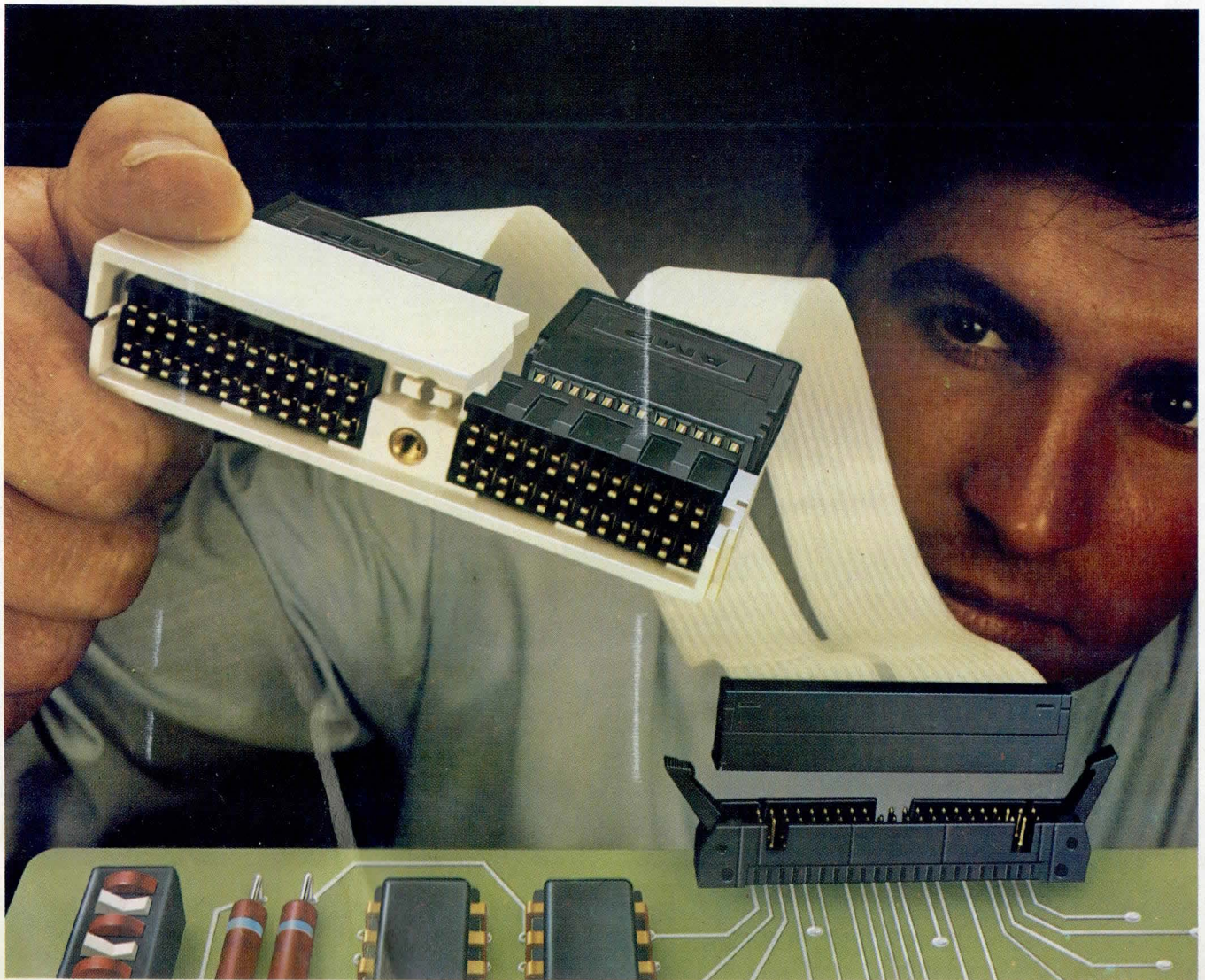
opto 22

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Physically separates and electrically isolates grounds from signal conductors. And allows us to offer you the most economical assemblies on the market.

All AMP transmission cable assemblies are equally cost and performance effective—and are available in different interconnect configurations to match your requirements.

The header receptacle, on .100 x .100 inch grid, is ideal for use with our

universal vertical or right angle eject headers. It comes in 10 through 50 positions, with or without center polarization.

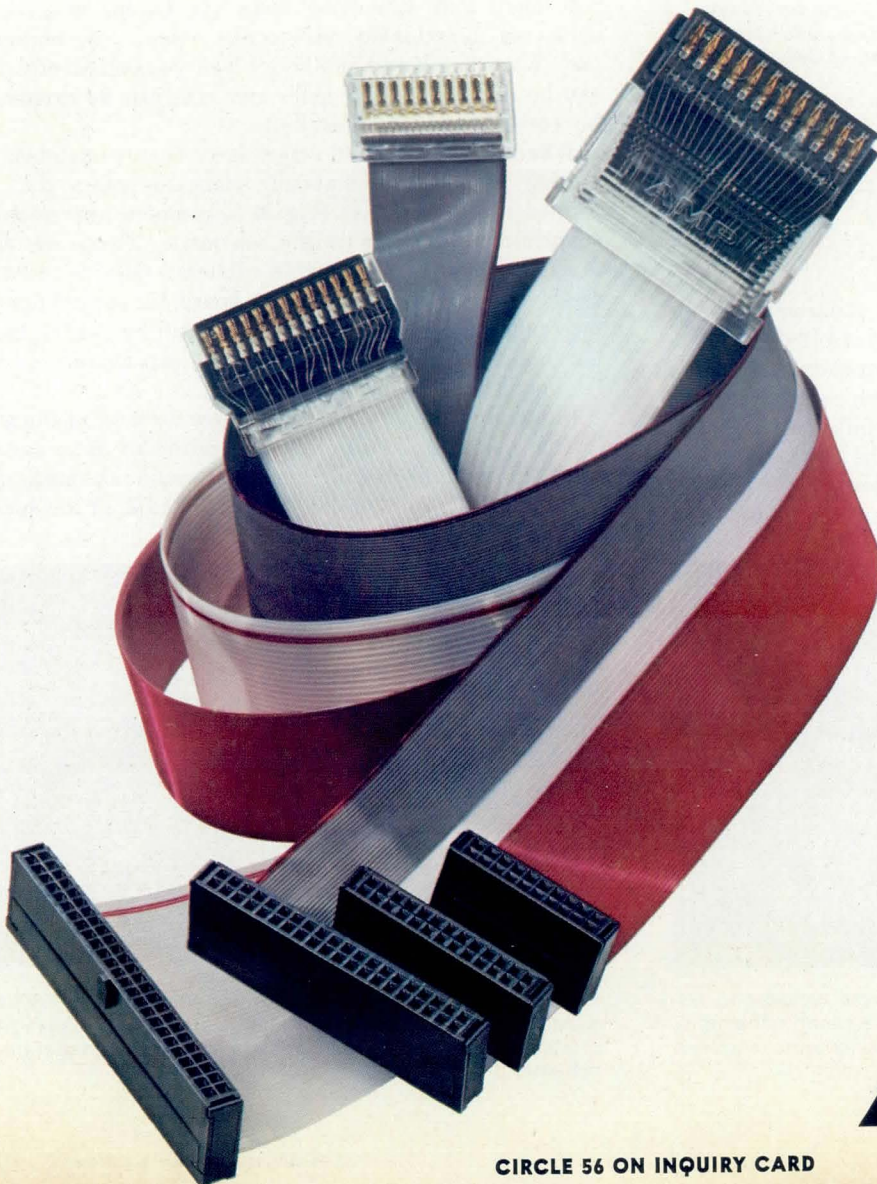
The pinfield style, which mates to backplane posts on .100 x .100 inch grid, is stackable end-to-end or side-by-side. Post stops are optional to permit wrap-type interconnects on posts.

The SLT style, a 24-position unit with .125 x .250 inch spacing, interconnects with industry standard computer interface connectors.

For full details, call the Transmission Cable Assembly Information Desk (717) 780-8400. Or write us. AMP Incorporated, Harrisburg, PA 17105.

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Some facts worth knowing about AMP Transmission Cable Assemblies

Mechanical

Mating Force. 8 oz. max./contact
Unmating Force. 1½ oz. min./contact
Mating and Unmating. 200 cycles
Vibration. 15 G's, 10-2000 Hz
Physical Shock. 100 G's, 6 millisec

Electrical

Current. 1.0 ampere max./contact
Contact Resistance. 25 milliohms max.
Insulation Resistance. 5000 megohms min.
Dielectric Withstanding Voltage. 500 volts RMS (sea level)

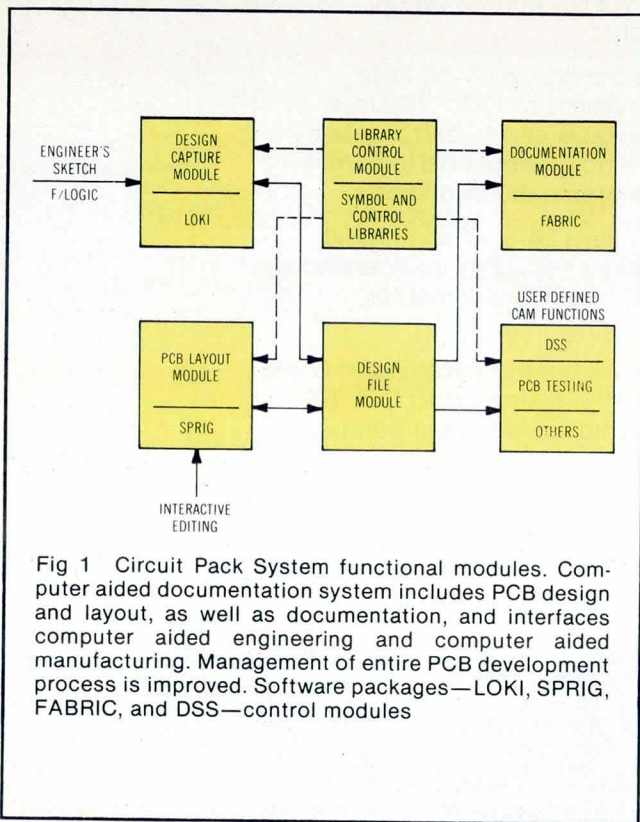
Environmental

Temperature. -65°C to 105°C
Thermal Shock. 5 cycles: -65°C to 105°C
Moisture Resistance. 10 days, 25°C to 65°C, 80-98% R.H.
Salt Spray. 5% solution, 48 hours
Industrial Gas. 10% SO₂, 24 hours

AMP

CIRCLE 56 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS



Design Capture Module

An interactive schematic editor, called LOKI, provides for the capture, modification, and validation of PCB design data at graphics terminals. End product is an electronic circuit schematic drawing created by the system operator on the screen of a graphics terminal (Fig 2) following a design engineer's rough schematic drawing. The LOKI editor permits the operator to specify (and display) schematic symbols at the gate and component level, component types, and

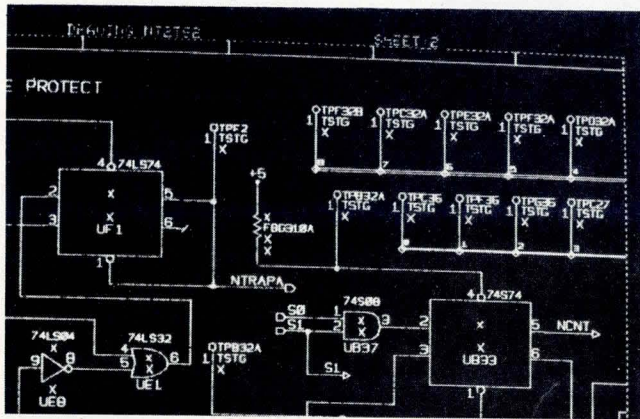


Fig 2 Portion of preliminary electronic circuit schematic. Using LOKI editor, and on basis of engineer's rough schematic, system operator creates diagram of PCB schematic on screen of graphics terminal

complete electrical connectivity of a circuit. Schematic symbols and connectivity are validated at the point of capture, and the operator can systematically check the schematic to ensure that the circuit description is complete, self consistent, and consistent with the circuit logic. Drawing data are stored on magnetic disc for later generation as hardcopy.

PCB Layout Module

SPRIG (System for Placement and Routing using Interactive Graphics) provides automatic and interactive tools for designing physical PCB layouts at graphics terminals. The system operator works with LOKI connectivity data already in the design file and any common or special layout constraints on placing components and routing circuits on the PCB. Stages in the SPRIG process consist of *assignment*, a subsystem that uses the gate and connectivity data to create devices so that logical gates can be assigned to physical circuits; *placement*, a subsystem that distributes devices over the surface of the board to maximize routability; and *automatic optimizer*, a subsystem that uses the placement information to optimize the gate and pin assignments for maximum routability.

Computer algorithms that establish routability in the placement and optimizing steps are based, in part, on achieving functionally satisfactory circuits at minimum cost. Wire length and number of logic connection crossings can be minimized, and gates and pins can be exchanged between circuits for lowest cost.

When the three SPRIG stages have been completed, the routing function automatically plans the paths that the printed wires must take (Fig 3) to complete the electrical connections described in the schematic. There are three separate, operator selectable routers. One is used to establish an initial pattern on the board, the second handles the random logic, and a maze router can be used to locate the final optimal paths as the layout nears completion and the board becomes congested.

Although these automatic processes do most of the work for the operator, handle large quantities of data, and accomplish in relatively little time what would take many days to do manually, they usually cannot handle all the special

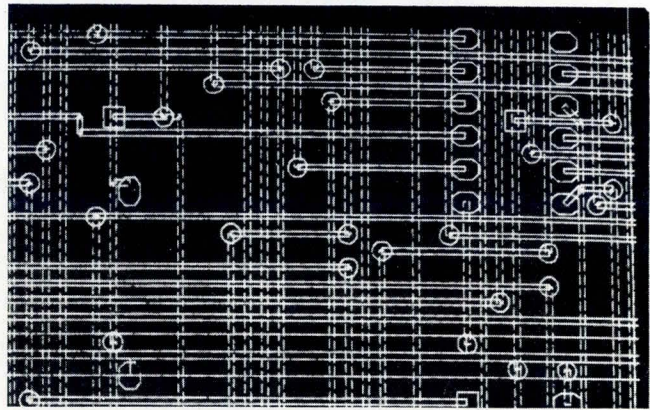
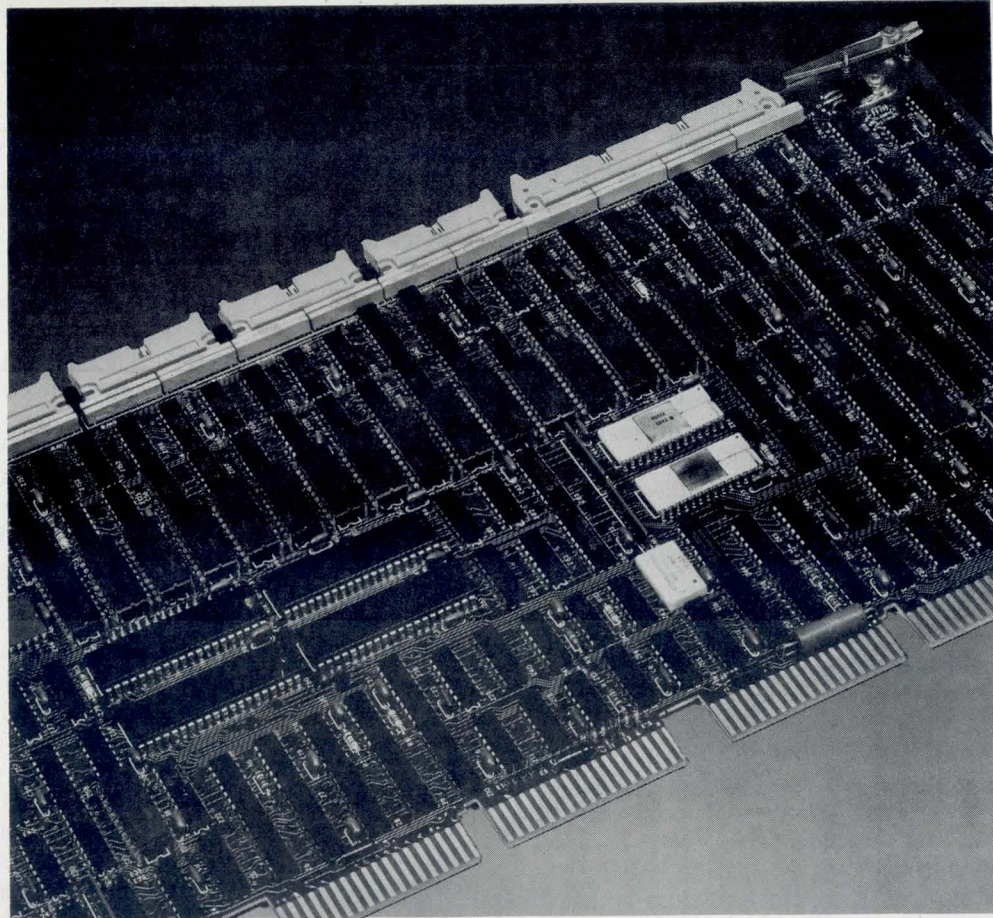


Fig 3 Portion of routing diagram for schematic. SPRIG software package assimilates LOKI connectivity data to plan paths printed wires must take to match electrical connections in schematic



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CIRCLE 57 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

considerations specified by the engineers. SPRIG, therefore, provides a set of interactive editing commands to take care of special assignment, placement, and routing cases. The operator can apply SPRIG's interactive editing mode before, after, or between stages of the automatic routing process, and can delete, add, or modify any printed connection, move devices around, or reassign logic gates. In addition, a conventional digitizer can be linked into the system for large scale editing operations or to create design files for previously developed PCBs.

When the operator is satisfied with the SPRIG-generated layout, the system is requested to perform verification functions to check for short circuits and other logic violations. The board is also "cleaned up" by, among other things, optimizing small sections to minimize the need for drill holes in the board and increasing space between printed wires wherever possible.

Finally, the SPRIG and LOKI records in the design file are quickly and automatically matched by the computer system to validate connectivity between the schematic drawing and the PCB layout. In contrast, the time consumed in manual validation and the possibility of overlooking errors and inconsistencies are major difficulties in development procedures in which digitizing is the only automated function. The end product of this exercise is a layout that is stored on magnetic disc or tape for subsequent electronic or hardcopy transfer to manufacturing.

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Library Control Module

This unit creates, modifies, and controls schematic symbol and component libraries used by development groups. A cross matching mechanism ensures both consistency and compliance with predetermined standards. The two libraries are interactively changed and updated for access as necessary by all the other system modules during PCB design progress. Flexibility is maintained to meet changing environments.

Graphical and electrical descriptions of all schematic symbols to be used (Fig 4) are contained in the schematic symbol library. These symbols are gate level (such as NAND and NOR), integrated circuit level (such as 7400, 74S00, and 74LS00), and documentation level (such as sheet borders); all of these may be used in the design capture and documentation modules. The component library contains a complete description of all components, subdivided into graphical, electrical, physical, and general descriptions. Electrical descriptions cross-reference to the corresponding schematic symbol library entries for the component. Both corporate and project databases are included. The corporate database consists of standard approved components and component data common to all projects in an organization, while the project databases contain components and general descriptions that are useful only in particular projects.

Documentation Module

A software package called FABRIC provides the working documentation that accompanies a PCB design into manufacturing steps. The documentation module generates a variety of manufacturing data from the design file. Among them are check plots (paper copies) of the circuit schematic and PCB layout, with associated engineering information; a stock list of component codes, quantities, suppliers, and other electrical component information; phototools (photoplotter board layer transparencies and solder resist masks); and assembly drawings (paper plots detailing component assembly information). These assembly drawings are

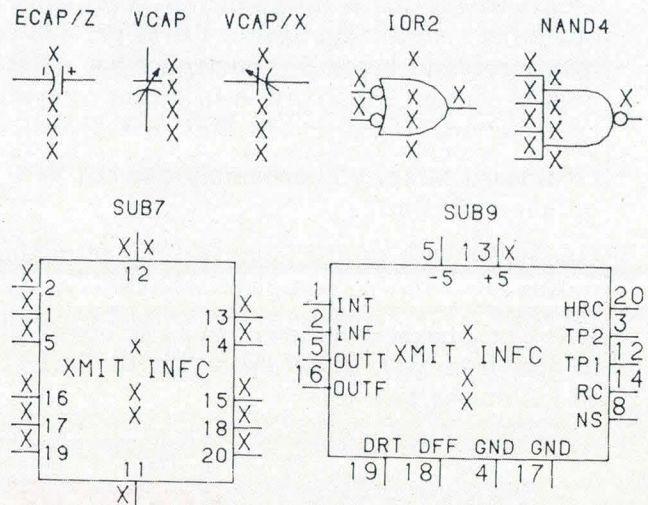


Fig 4 Typical graphical and electrical descriptions in symbol library. Top row, from left to right, shows three discrete components and two logic gates; bottom row illustrates two integrated circuits

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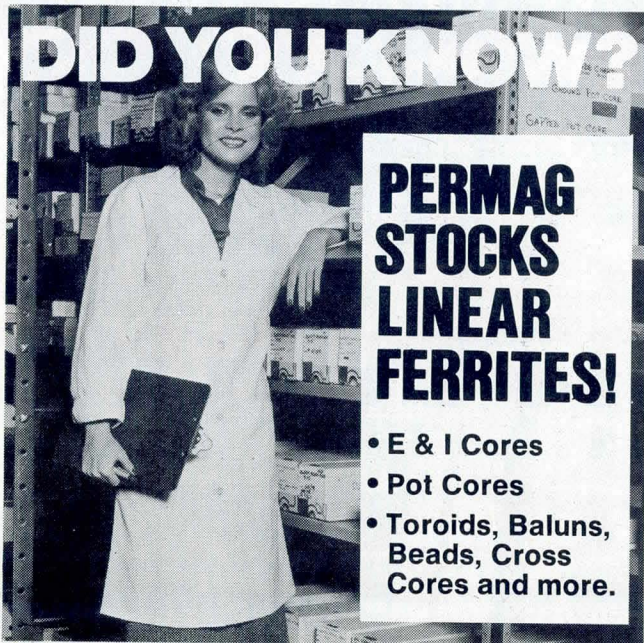
Circle 60 for Information only

DIGITAL CONTROL AND AUTOMATION SYSTEMS

automatically cross-referenced to the schematic drawing to facilitate correlation of circuit logic with physical components and tracking.

Other data generated include tapes containing positioning information for numerically controlled drilling machines; autoinsertion data for component sequencers and dual inline device insertion equipment; a pack usage and spares report summarizing integrated circuit use and spares listed by component type and X-Y coordinate position; an X-Y hole and land data table that lists each hole and land size/aspect ratio in relation to coordinate position; and two "from-to" lists that summarize all tracking on a board.

The manufacturing department either applies these data as they are in hardcopy form or processes them further to develop customized control data for particular equipment on the production line, such as an autoinsertion machine. Applicable portions of the design file may be transferred to the production computer offline as magnetic tape; or, in a fully integrated system, the production computer may have direct online access to the design file as needed. The ultimate advent of CAM in an integrated system will require no fundamental change in the design and documentation processes.



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Design File Module

This unit provides for the exchange of PCB design data between system modules. As a PCB goes through the development process, its design file grows with the addition of the LOKI schematic, SPRIG PCB layout, and documentation data. Both the design file and the documentation module provide product data for other user defined functions beyond the system scope.

System Computer

The Circuit Pack System operates on the DECsystem-20 family of computers manufactured by Digital Equipment Corp. Video display devices are Tektronix 4014 graphics terminals. Other computer equipment in a full configuration include alphanumeric video terminals and a pen or electrostatic plotter. A digitizer and a Gerber 740 photoplotter are optional. Color raster scan terminals can also be used with the storage devices.

A typical system configuration is shown in Fig 5. Computer model and the number and variety of terminals and peripheral devices depend on the particular needs of the organization. All computer models run on DEC's TOPS-20 operating system. Selection of terminals is controlled mainly by the distribution of personnel who must have access to the design system.

Choice of computer model is determined mainly by the expected design system work load. As a rule of thumb, interactive LOKI or SPRIG editing can be considered one unit of load, while SPRIG autorouting of PCBs—an intensive number crunching task—constitutes about four units of load. Optimum system response can be obtained with the

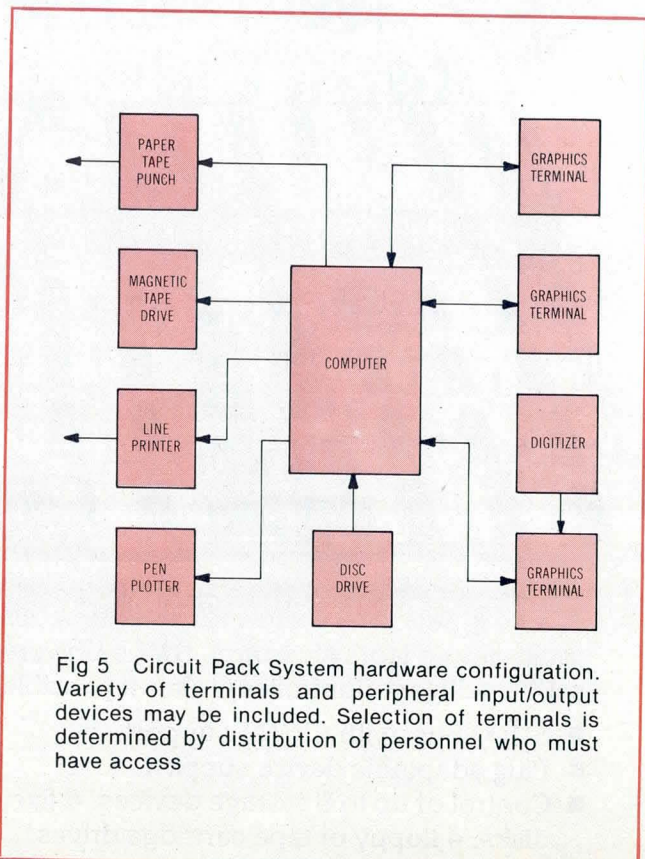


Fig 5 Circuit Pack System hardware configuration. Variety of terminals and peripheral input/output devices may be included. Selection of terminals is determined by distribution of personnel who must have access

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CIRCLE 62 ON INQUIRY CARD

High cost wrap/pin boards made **OBSOLETE**

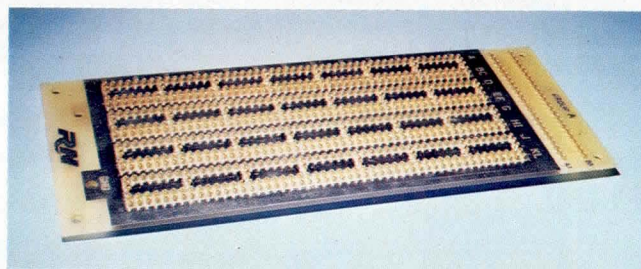
Save money, save time! Wire your boards faster, easier than ever before —with the RN QUICK/CONNECT point-to-point IDC wiring system.

Here is a wiring system that does what wrap/pin does — but does it faster, easier. The wire is simply pushed into the “Quick/Connect” tine which pierces the insulation (IDC) making a gas-tight connection between wire and terminal. “Daisy chain” wiring is accomplished with no break in the wire, no insulation stripping.

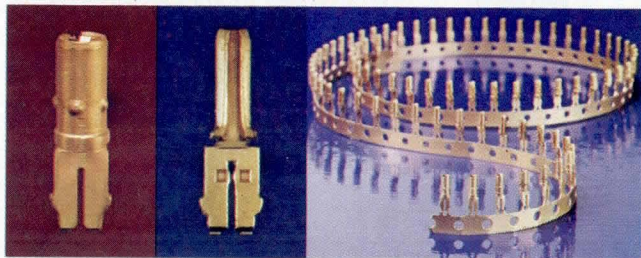
You'll never willingly use wrap/pin for boards again. Consider these advantages:

- 1 High speed wiring simplicity**— You connect just **one** wire per connection. There is **no time-consuming insulation stripping** as needed with wrap/pin.
- 2 Fast, easy wiring changes**— Repair or modify boards by simply removing the individual wires and quickly re-wiring. Field wiring modifications are simple and fast.
- 3 Meets highest reliability standards**— Durable four-finger BeCu contacts and fully heat treated IDC tines insure gas-tight performance.
- 4 High density low profile boards**— The “Q/C” board profile is only 0.235” compared to the 0.703” wrap/pin board. “Quick/Connect” boards go right into production racks.
- 5 Wiring machines available**— The semi-automatic wiring machines now in use can be readily modified for the “Q/C” system. Also, semi-automatic “Q/C” machines are available.

This is not just a “dream” system. A major electronics firm is currently using the “Quick/Connect” system on a regular basis.



“Quick/Connect” socket boards, ready for wiring, are available in several standard configurations or can be developed to meet customer specifications.



Socket

Terminal

Sockets and terminals supplied on strips for easy board insertion.

Write or call today for full details on this new point-to-point wiring system that will obsolete wrap/pin boards. The time and money savings are truly phenomenal!



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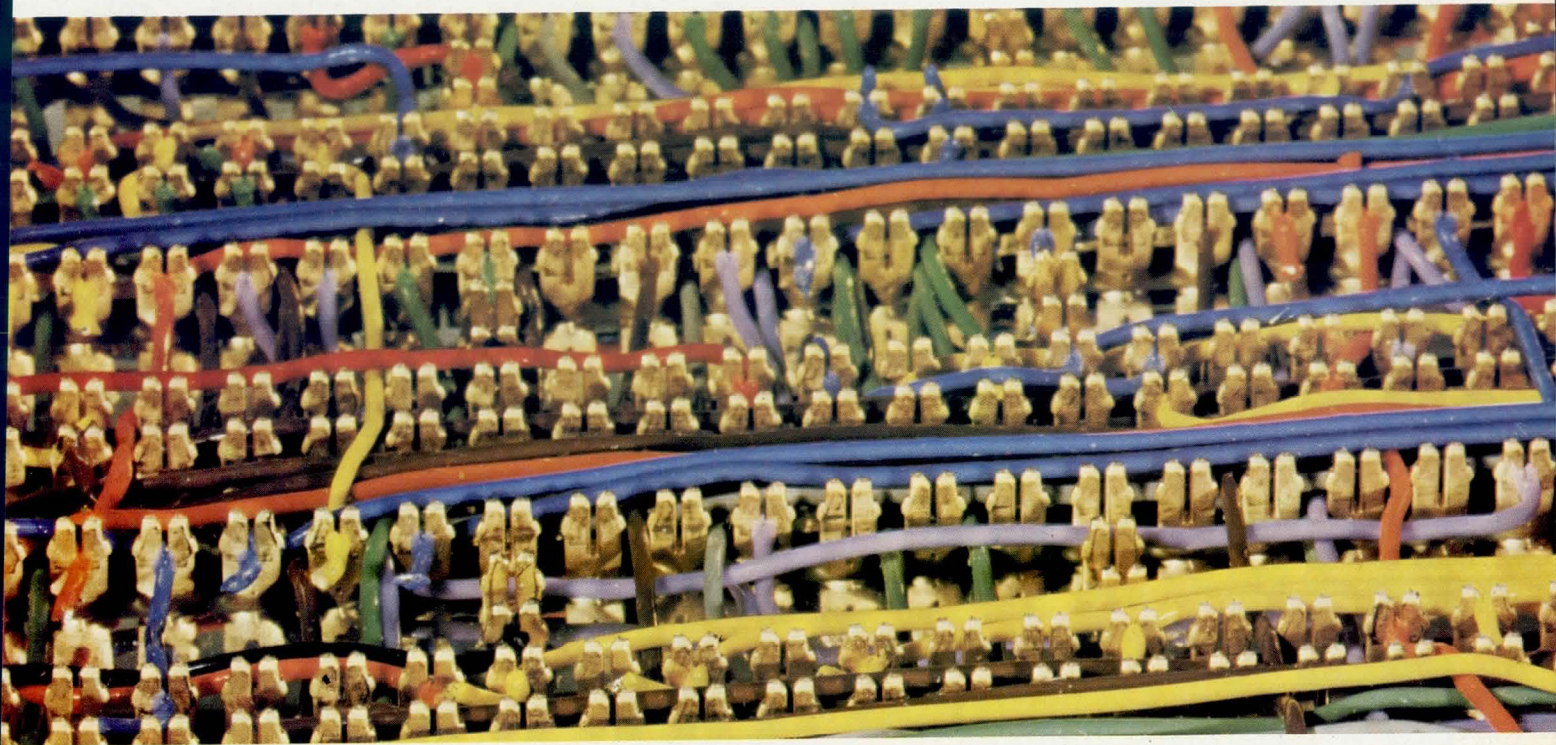
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An "eyeball" comparison tells you instantly that "Quick/Connect" has got to be faster to wire, far less costly than wrap/pin boards!



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Send me full details on your new "Quick/Connect" board wiring system.

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My possible application is _____

CD-980

DIGITAL CONTROL AND AUTOMATION SYSTEMS

following total loads on the indicated computers: 6 on model 2020, 11 on model 2040, 20 on model 2050, and 40 on model 2060. The number of simultaneous system users depends on which system functions are being performed. If there are more than the indicated number of simultaneous users, such as might be expected in peak work periods, a consequent degradation in response will result.

At Bell-Northern Research, the system is divided among three buildings in the Ottawa area (Fig 6). Most of the actual system activity involves users, who spend roughly 85% of their time at graphics terminals. These users, who are former printed circuit design draftsmen, are organized into small groups in central offices serving major development organizations at various locations. A first-shift user and second-shift user share a graphics terminal between their desks.

The procedure in developing a new PCB design follows a set sequence:

- (1) The design engineer brings his circuit sketch to a screening group, which verifies that the connections are complete, each lead has a name, and all symbols and components are in the libraries.
- (2) The user applies LOKI to enter the drawing into the system (Fig 2). When satisfied with the result, the user requests generation of a check plot of the schematic drawing on a plotter and reviews the plot with the design engineer. This is a purely functional check since there are no pin numbers or reference designations yet on the drawing.
- (3) The user applies SPRIG to prepare a PCB layout on the basis of the LOKI design file.
- (4) At a command from the user, the system compares the SPRIG record of the PCB layout with the LOKI record of the schematic drawings to ensure consistency. In this process pin numbers, reference designations, and other data required on the schematic drawing are generated. (In manual

documentation systems, comparison of the schematic drawing and PCB layout, which usually is done by the design engineer, is a long, tedious process that often results in errors and oversights.)

(5) Check plots of the schematic drawing and PCB layout are generated and given to the design engineer for approval.

(6) Under control of a phototool tape generated out of the design file, the photoplotter creates a physical image of the PCB and a layout negative is made.

(7) The printed circuit fabrication shop makes PCBs from the layout negative.

(8) The design file for the PCB is recorded on magnetic tape for the engineering archives.

Circuit Modifications

While the time analysis for a typical design with 75 integrated circuits assumes a single-design cycle, development of PCBs in electronics manufacture generally involves two and a half to three recycles for each new design. Recycling is likely to include changes in perhaps a third of the wire layout and integrated circuit selection.

Modifications originated by design engineers usually lead to changes in both the schematic drawing and the PCB layout. In conventional digitizing, a layout draftsman must first update the engineer's revised schematic. Then the drawing is redigitized, a process that requires another round of checking and validating by the engineer and layout draftsman.

In modifying a PCB with this design system, the user applies SPRIG to correct the PCB layout (probably in the interactive editing mode since only a few changes usually need to be made). Then the user has the system compare the modified SPRIG record in the design file with the updated LOKI file, and a revised schematic drawing is generated

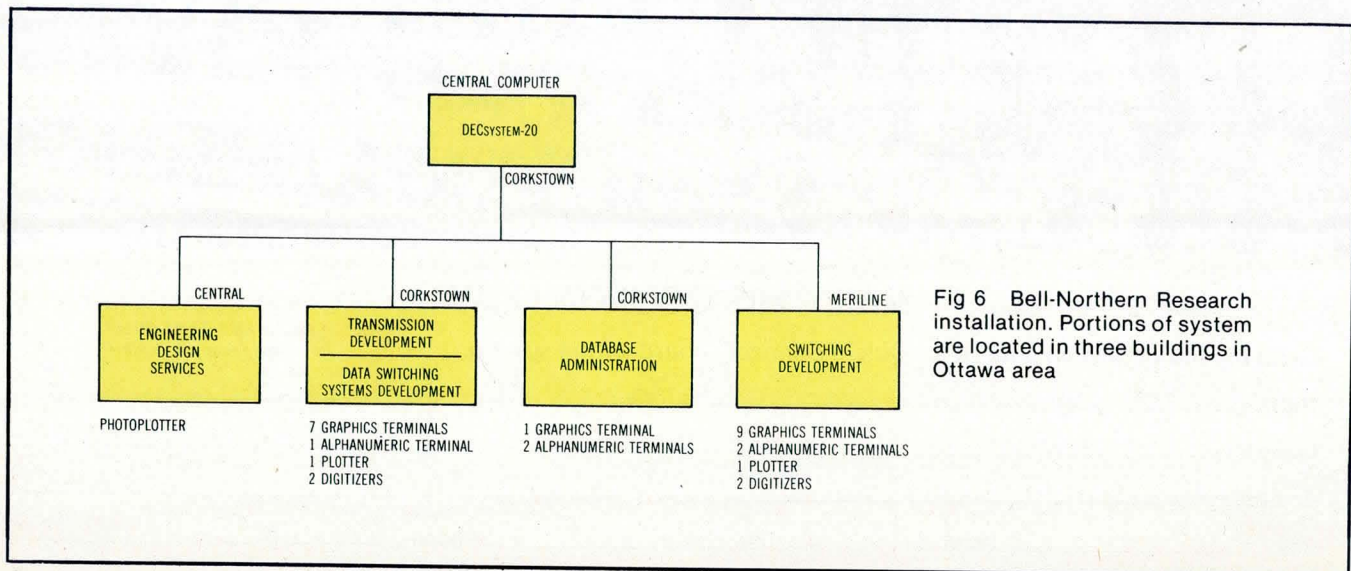


Fig 6 Bell-Northern Research installation. Portions of system are located in three buildings in Ottawa area

DIGITAL CONTROL AND AUTOMATION SYSTEMS

from the modified LOKI file on a plotter. (In contrast, minor PCB changes are often neglected in the schematic drawing in conventional digitizing.) Further, the documentation module is also updated to account for the changes produced by the design modification. If only a schematic update is needed, the user applies LOKI in revising the drawing without having to use SPRIG, with the assurance that necessary documentation changes will be made.

Proven System Benefits

The first two years of experience with the design system at Bell-Northern Research have demonstrated several benefits over PCB development employing conventional digitizing. For example, there has been a 30 to 40% reduction in elapsed time between the engineer's sketch and PCB layout negative, a 35% reduction in the cost of people and computer equipment time, and a 50% reduction in technical time to produce a design modification. There are also fewer design recycles to produce optimal products, as well as immediate compatibility of schematic drawing, PCB layout, and documentation following modification. The PCB design file is fully transferable between computer devices and geographical locations. Overall, there is improved management of the entire PCB development process.

This design system is a part of the company's COPES (Customer Optimized Product Engineering System), a hard-

ware development concept that includes CAE and CAM as well as computer aided documentation. The first two COPES modules added are called F/LOGIC and DSS. F/LOGIC is an interactive gate level simulation program that simplifies the design and analysis of digital circuits. Among other things, F/LOGIC simulates the results that can be expected from manufactured circuits; for example, it gives tolerance timing with minimum and maximum rise and fall time delays and loaded time delays or pinout-dependent delays. Simulation capacity is up to 4000 gates with standard computer memory, and up to 32,000 gates maximum with add-on memory. F/LOGIC simulation produces some of the connectivity data that are used in LOKI generation of schematic drawings and thereby simplifies the design system user's task.

DSS (Data Storage System) is a database system that provides extensive facilities for management of the design file and generation of reports tailored to the users' needs. It also merges mechanical data with the electrical information that has been stored in the design file. Both F/LOGIC and DSS software can be run without adding to existing design system hardware.

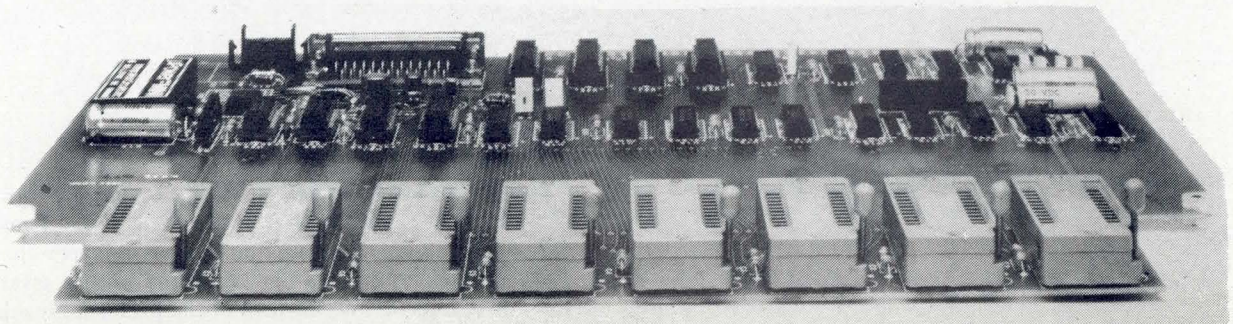
Development of electronic products has been considered here specifically at the PCB hardware level. Beyond that, the COPES concept and computer based systems such as the Circuit Pack System can also be applied at higher levels of hardware, that is, to frame assemblies and entire electronic systems. A parallel approach can be visualized to support the creation of electronic system software, and ISES (Integrated Software Engineering System), a complementary software system, is now under development.

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Hardware compatible to MDS-UPP-103 via 25 pin cable. Software compatible to ISIS-JPM.

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For 2716, 2732 or 2732A model EPROMs, the ZX-908 can program up to 16K Bytes of storage in one operation. Zero-Insertion-Force sockets are provided for quick insertion/withdrawal.



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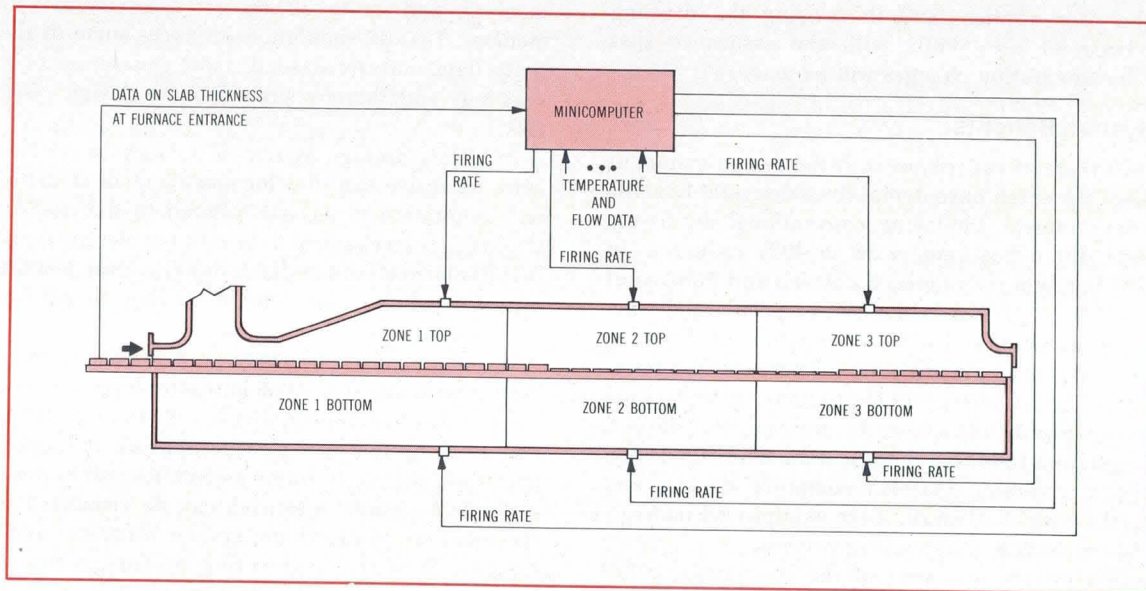
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CIRCLE 64 ON INQUIRY CARD

Fuel Consumption on Steel Mill Furnace to be Controlled by Minicomputer



A furnace control system being developed in a joint program by the Holcroft Div of Thermo Electron Corp, 12068 Market St, Livonia, MI 48150, and the Oregon Steel Div of Gilmore Steel Corp is expected to reduce fuel consumption by anticipating changes in the load entering the furnace. Because one part of the furnace may be reheating slabs of one thickness while another part may be reheating either thicker or thinner slabs, the actual heat required in each furnace area differs. In the minicomputer control system,

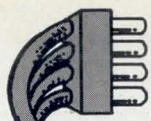
a mathematical model will be used to determine the average fuel required by each zone and to adjust the fuel input for that level. Setpoints for furnace temperatures will also be adjusted to improve furnace economy.

This control system is being developed for a walking beam steel slab reheat furnace with a 140-ton (142 metric)/hour capacity. Pressure cast slabs varying from 6 to 8" (15 to 20 cm) in thickness and 6 to 24' (1.8 to 7.3 m) in length are heated to 2350 °F (1288 °C).

Fiber Drawing System Controls Diameter to Accuracy of 0.1 μm

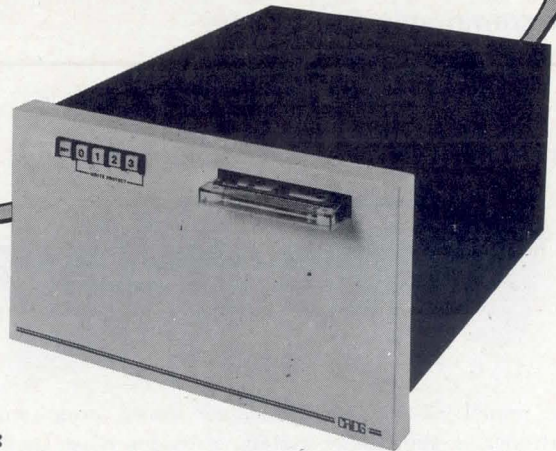
Manufacture of optical fiber to within less than 1% of any specified diameter is made possible by a microprocessor controlled system called FOCSL (for fiber optic characterization by scattered light). In the procedure, the fiber is illuminated by a laser beam that generates a pattern of interference fringes. A fiber diameter measurement, proportional to the number of fringes within a fixed angular range, is fed into a microprocessor controller for comparison to the desired value. Then the microprocessor adjusts draw speed of the fiber manufacturing unit.

Fibers are produced by drawing them from a molten tip of a cylindrical preform that has been heated to about 2000 °C. A die might damage the fiber's surface; therefore, precise diameter is maintained by controlling several factors, including the rate of feed of the preform into the heat zone and the rate the fiber is drawn. The control system, developed at Western Electric's Engineering Research Center in Princeton, NJ, can measure fiber diameters of from 50 to 225 μm , with 0.1- μm resolution and $\pm 0.25\text{-}\mu\text{m}$ absolute accuracy at 500 measurements/s.



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systems
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a.r.o.**



Software

Your choice of:

- RT-11
- RSX-11M
- U/V6 (UNIX*)

MF-211/411

- LSI-11/2 with 32K words or LSI-11/23 with 64K, 96K or 128K words
- RX02 Equivalent Dual Floppy Systems, Single-Sided or Double-Sided, Dual Density
- Quad Serial Interface
- 8 Quad Slot Backplane

HD-11/HD-11T

- Shugart Winchester Drive with 21 Megabyte Capacity, Software Equivalent to Four RL01's
- DEI Cartridge Tape Back-up (HD-11T)
- Controller Card with RL01 Instruction Set Compatibility

When you plug in to Charles River Data Systems you plug in to innovative, practical solutions to your system design requirements. Solutions like our double-sided, double-density floppy disk systems—offering one megabyte of RX02 equivalent storage per drive. Or our Winchester drive with cartridge tape back-up for fail-safe reliability—in a single enclosure, with a common controller card.

You can purchase each of our compact, reliable components separately to expand or complete a system. Or combine them in your choice of configurations for powerful, multi-user, general purpose computers in a single, cost-effective package.

Equally at home as R & D systems or as the basis for business and process control sys-

tems, CRDS systems are based on the DEC LSI-11/2 or LSI-11/23, with from 32K to 128K words of MOS memory. Peripherals available include a 21 megabyte Winchester fixed disk system; single- or double-sided floppy disk drives; and a 3M cartridge tape back-up for the Winchester disk. Software systems available include RT-11, RSX-11, and U/V6 (UNIX*).

Whichever configuration you choose, you're assured of plugging in your system fast, because CRDS delivers most products in 30 days!

For complete specifications, and to discuss the configuration or components that best meet your needs, call CRDS Marketing at (617) 655-1800. And plug in to CRDS today.

*Trademark of Digital Equipment Corporation.

*UNIX is a registered trademark of Bell Laboratories.



Charles River Data Systems, Inc.

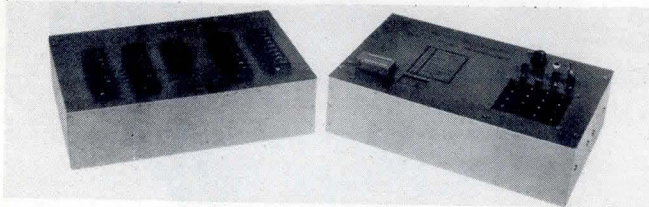
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CIRCLE 65 ON INQUIRY CARD

DC & AS BRIEFS

**Programmable Controllers
And Support Modules**

Replacement for Relay/Timer Control Systems



The model SK-1506 microprocessor based programmable controller, a standalone system, provides noise immunity through use of optically isolated inputs. Up to 16 dc or ac inputs can be monitored, and an additional 16 I/O channels are available for future expansion. Each of 16 optically isolated Triac outputs is individually fused as protection against transient voltage surges.

Entertron Industries, Inc, Ellicot Sta Box 15, Buffalo, NY 14203, has introduced this controller as a replacement for systems now using conventional relays and timers. An optional model 8k P-ROM programmer has LED display, hexadecimal keyboard, and 1k x 8 RAM for data manipulation.

Circle 440 on Inquiry Card

Setpoint Controller

Adaptive gain as well as the standard proportional, integral, and derivative control is offered in the model 2300A microprocessor based process controller. Iveron Pacific, 1152 Morena Blvd, San Diego, CA 92110 states that the availability of adaptive gain is useful where setpoint value changes may be very large, where setpoint control may be very close, or when the process variable is nonlinear. The controller features front panel keyboard entry of all control parameters, memory module storage of control programs, external RS-232-C interface for operation from a host computer, and programmable setpoint.



Circle 441 on Inquiry Card

Servo Interface Module

An I/O board that plugs into both contact and data buses on the company's programmable controllers, this servo interface module operates with data and stepping motor feedrate modules to drive dc servomotors. Because an encoder serves as the feedback element, sin/cos excitation and phase digitizing circuits are unnecessary. This module from Cincinnati Milacron, Electronic Systems Div, Mason Rd & Rt 48, Lebanon, OH 45036, has an 18k-step/s maximum feedrate and a maximum span of 9,999,999 steps. Built-in diagnostics indicate status of coils programmed and errors per item via board edge LEDs.

Circle 442 on Inquiry Card

Floppy Disc Based Programming Terminal



Significant savings in programming time and costs for users of the EPTAK programmable controller are promised through introduction of the CP783 CRT programming system. This dual-floppy disc based programming terminal offered by Eagle Signal Industrial Systems, 736 Federal St, Davenport, IA 52803, permits program storage of 0.5M bytes/diskette, expandable up to 4M bytes—compared to up to 120k bytes/side for cassette based systems. Editing time can be reduced by a factor between 10 and 20, compiling time by between 7 and 10, and copying time by 20 (from 60 down to 3 min). User memory is 60k bytes instead of 16k.

This programming system eliminates the need for multiple cassette tapes or discs for different types of programming software such as editing, compiling, and debugging. All programs can be called from a single disc and control/assembly language label capacity can be increased from 750 to approximately 8000. Four programming languages are available. The CRT display consists of 24 lines of 80 characters when entering or editing a program, or for monitoring EPTAK system operation, and can be scrolled up or down while generating programs.

Circle 443 on Inquiry Card

MEASUREMENT AND CONTROL. NEVER HAS SO MUCH COST SO LITTLE.

MACSYM 20 is the first low-cost analog and digital I/O system that can stand alone or operate as a front end to your host computer.

Whether you're an OEM or an end user, MACSYM 20 is your best choice for distributed data acquisition and industrial control at a truly affordable price.

Your signal conditioning is already done. With MACSYM 20, just choose the exact measure-

RS232C, RS422, 20mA and IEEE capabilities give you local, remote or long distance communications flexibility.

host computer.

And by simply combining the command set with the optional MACSYM EPROM programmer and any low cost terminal, MACSYM 20 becomes its own complete software development system.

MACSYM 20 offers significant performance advantages over data loggers, front ends and micro-computers. At a base rate of only \$3,645*, it's easily your most cost effective measurement and control choice. For more information on the MACSYM 20, call your local Analog Devices office listed below.

*U.S. Domestic price only.

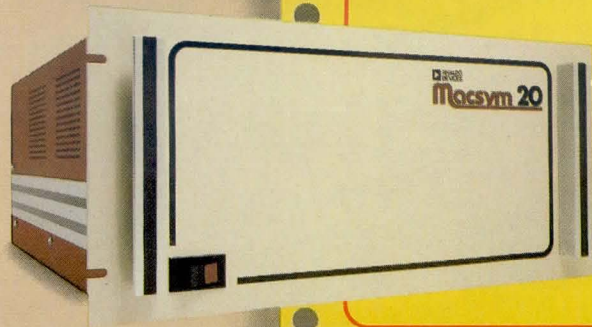
ANALOG DEVICES

Macsym 20

MACSYM 20 A COMPLETE SYSTEM FOR LABORATORY DATA ACQUISITION AND INDUSTRIAL CONTROL:

STANDARD FEATURES:

Z-80 MICROPROCESSOR	N/C
16K RAM (RANDOM ACCESS MEMORY)	N/C
DUAL RS-232C SERIAL INTERFACES	N/C
PRECISION 12-BIT ADC AND SAMPLE/HOLD	N/C
SOFTWARE PROGRAMMABLE GAIN AMPLIFIER	N/C
REAL TIME CLOCK	N/C
16 SLOTS FOR I/O SIGNAL CONDITIONING BOARDS	N/C
USER PROGRAMMABLE EPROM	N/C



BASE PRICE

\$3,645.00*

*SUBSTANTIAL OEM DISCOUNTS STARTING AT 5 SYSTEMS.

ment and control functions you need from our wide library of sensor I/O cards.

MACSYM 20's powerful, task-oriented command set comes for only \$995*. Not only does it simplify applications programming, but it also significantly unburdens your

ANALOG DEVICES

WAY OUT IN FRONT.

Analog Devices, Inc., Measurement and Control Products Division, Box 280, Norwood, MA 02062; East Coast: (617) 329-4700 Ext. 1500; Midwest: (312) 894-3300; West Coast: (714) 842-1717; Texas: (713) 664-6704; Belgium: 031/37 48 03; Denmark: 02/84 58 00; England: 01/941 0466; France: 01/687 3411; Germany: 089/53 03 19; Japan: 03/263 6826; Netherlands: 076/87 92 51; Switzerland: 022/31 57 60; and representatives around the world.

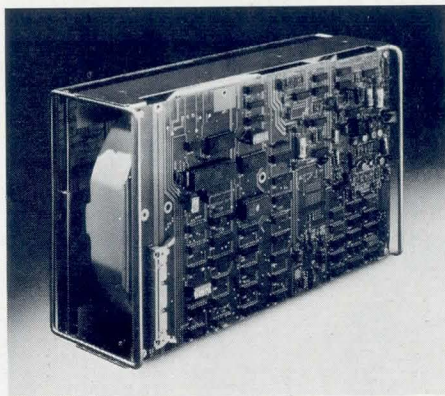
CIRCLE 66 ON INQUIRY CARD

DISKOS 2050 AND 3450 8" WINCHESTER DISC DRIVES

This Tune May Sound Familiar . . .

Variations are created from the elements of a composition, changed to create a new and interesting idea. PRIAM's DISKOS 2050 and 3450 are variations on a Winchester disc drive design theme that has been proved in concept, performance, and production.

PRIAM design engineers followed the same design composition that has made the 14-inch-disc DISKOS 3350 efficient, reliable and cost effective. They scaled the DISKOS 2050 and 3450 to fit exactly into the space required by a standard floppy disc drive. This noteworthy accomplishment provides capacities of 21 and 35 megabytes, with 40 and 70-megabyte capacities to follow, with the same size and weight.



Interface Harmony

PRIAM's DISKOS 2050 and 3450 play from the same interface music as the DISKOS 3350, so that a single controller can be used with PRIAM Winchester disc drives covering the capacity scale from 10 to 158 megabytes. Head positioning times, data transfer rate, data and command functions and lines . . . every pin connection is the same. And *data separation is included* in all PRIAM drives, saving you expense in interfacing.

Sing Along With SMD

An optional interface permits you to use PRIAM drives with existing controllers for CDC Storage Module Drives. You can stretch the life of your SMD controller and get on the air more quickly with the low cost, high capacity, and splendid reliability of PRIAM Winchester disc drives.



Presto Positioning

PRIAM's proprietary linear voice coil head positioner provides fast access to data and still lets the DISKOS 2050 and 3450 exactly replace a standard floppy disc drive. Positioning is fast and precise, with an average access time of 45 milliseconds, and a track-to-track time of only 8 milliseconds. Because of the exact positioning provided by PRIAM'S voice coil system, data recovery is positive and reliable. DISKOS drives will tolerate the harsher environments in which computers, word processors, and communications systems of the future will operate.

Brushless DC Spindle Motor

A brushless DC spindle motor provides reliable operation with a simple, low-cost design, doing away with belts and pulleys and extra bearings. PRIAM's DC spindle motor eliminates alternating current entirely from the DISKOS 2050 and 3450. They will operate anywhere in the world without change.

Microprocessor Maestro

Economy, flexibility and reliability result from PRIAM's use of a microprocessor to control head positioning and to perform self test and diagnostics. The number of parts and electrical connections in the system are reduced to lower cost and improve reliability.

Welded Steel Rod Frame

PRIAM's DISKOS 2050 and 3450 main-frame castings are mounted in sturdy welded steel rod frames that permit ready circulation of cooling air. These frames also reduce weight and cost. Heavy metal is used only where it is needed, so the DISKOS 2050 and 3450 weigh only 20 pounds. Shock mounts protect the drives and isolate them from system ground.

Air for Reliability

PRIAM disc drives use a unique air management system to prevent contamination. Valuable data is protected by creating positive air pressure at the spindle bearings, where contamination is most likely to enter. PRIAM drives include permanent absolute filters that constantly purge the air inside the sealed disc assembly.

Specifications

DISKOS 2050 Capacity (unformatted)	21 Megabytes
DISKOS 3450 Capacity (unformatted)	35 Megabytes
Transfer rate	0.8 Mbytes/Sec
Track-to-track positioning	8 milliseconds
Average positioning	45 milliseconds
Tracks per inch	480
Bits per inch	6670
Height	4.62 inches
Width	8.55 inches
Depth	14.25 inches
Weight	20 pounds

Interface Efficiency

Interfacing DISKOS 2050 and 3450 disc drives to your controller is economical and efficient because it is designed for connection to the most widely used 8-bit and 16-bit microprocessors. Daisy chaining is easy and functional, and overlapped seeks may be used. Data separation is included in drive electronics, so controller design is simplified and reduced in cost.

SMART Interface Option

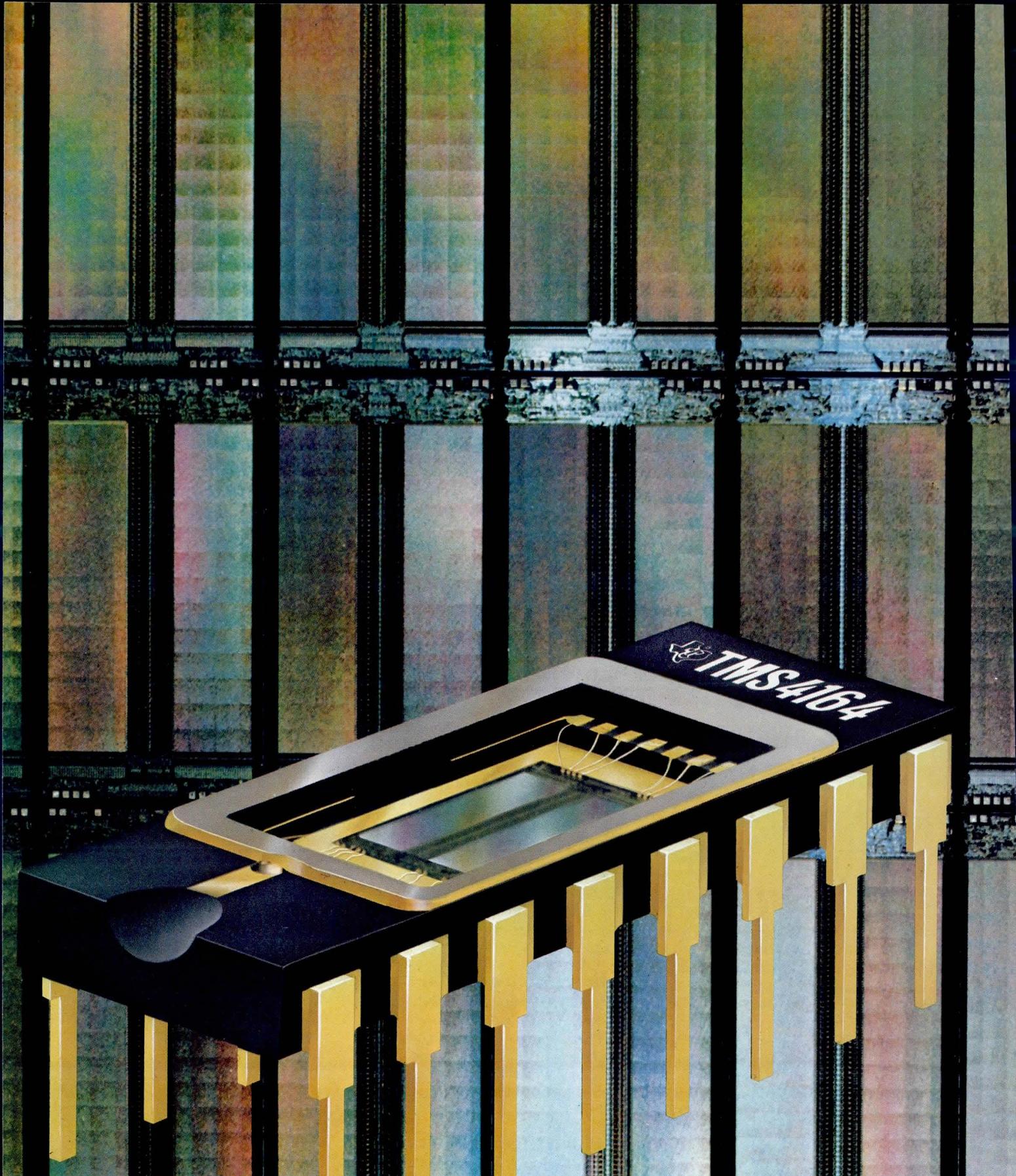
PRIAM's SMART Interface Adapter provides serialization and deserialization of data, disc formatting, sector buffer, polled or interrupt operation, defect mapping, overlapped commands, implied seek, selectable sector sizes and microdiagnostics. Up to four drives can be interfaced easily to the I/O bus at the byte level.

For a brief and handy history of Winchester technology and its advantages, call or write to PRIAM and ask for a copy of WHO'S SELLING RIFLES TO THE INDIANS? A Winchester Disc Drive Technology Primer. It's FREE!



PRIAM

3096 Orchard Drive, San Jose, CA 95134
Telephone (408) 946-4600 TWX 910-338-0293



*Another major milestone in MOS memory technology
from Texas Instruments ...*

TI's 64K dynamic RAM is ready for delivery. Now.

TI has paced the industry through generation after generation of semiconductor innovation, pioneering a lion's share of the major milestones in technology and production capability.

The new TMS4164 from Texas Instruments represents the fourth generation of dynamic RAM computer memories, and continues to fulfill the bright promise of innovative MOS technology.

TMS4164. Advanced architecture. Superior performance. High speed. High reliability. Low power. *And ready for delivery.*

Ready with 4 times the capacity of 16K RAMs in the same size package.

Ready with 65,536 bits of random access memory — and that's more than many board-level computers.

Ready with 256 cycle, 4 ms refresh architecture — the optimum organization evolving from all previous industry-standard dynamic RAMs.

Performance has been dramatically enhanced. Speed's up. Power's down. And design innovation makes this the *smallest 64K chip (35K mil²) available anywhere.* From anyone.

Improvements in density, reliability,

system cost and ease of use are some of the features, functions and benefits system designers will appreciate. Here's more:

- 64K bits in a standard, 300-mil, 16-pin package saves valuable board space and reduces system size
- Single 5-volt operation lowers power supply cost and system cooling requirements and improves reliability

- Lowest power dissipation available: 125 mW typical
- 256 cycle architecture means lower current peaks and reduced system noise
- State-of-the-art SMOS (Scaled MOS) processing

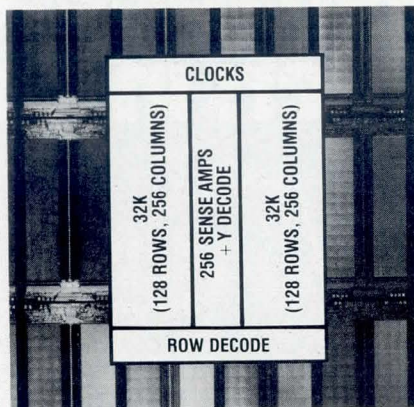
TI's new TMS4164 is perfectly suited for use in mainframe computers and large minicomputers. It also finds ideal application in microprocessor-based systems where smaller size, lower cost and improved performance are important considerations.

TMS4164. The deliverable, practical, usable 64K dynamic RAM. Compare our 256 cycle refresh architecture ... then compare our performance.

TMS4164. Truly another major milestone in MOS memory technology. Truly another example of the total commitment Texas Instruments is making to leadership MOS memory products.

For more information about the deliverable 64K RAM, call your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6965, Houston, Texas 77001.

TMS4164 256 CYCLE
REFRESH ARCHITECTURE



- JEDEC-approved pinout with N/C on pin one assures standardization and guaranteed availability
- High speed: 150-ns access and 280-ns cycle times (min.)
- TTL compatible I/O and clocks



TEXAS INSTRUMENTS
INCORPORATED

DC & AS BRIEFS

Machine Tool Control

Programmable Motion and Position Control Devices

Two products designed for use with the model 484 programmable controller (PC) extend the capabilities of that unit to include control of the motion and position of machine tools and process equipment. Gould Inc, Modicon Div, 155 W Big Beaver Rd, Troy, MI 48084, claims that because all stops and limits are programmed, there are considerable savings in time for both setup and operation.

Stepping motor control module B575 provides accurate control of stepping motors and dc servos with appropriate motor drives by issuing commands in the form of pulses from 0 to 9999/s. It operates with either open or closed loop systems under commands programmed into the PC in relay ladder logic by the user, but independent of PC scanning. In addition, it can ignore preset values and extend range indefinitely and can program linear/nonlinear acceleration and deceleration. There are four independent logical stop inputs. The device is compatible with incremental encoders having quadrature output.

Absolute encoder input module B581 serves as a link between the PC and an absolute encoder and is a replacement for cam switches. It detects angular shaft position changes at rates of up to 30 kHz. This device can be used to develop cam logic and to provide a means for entering data from external devices into a PC synchronous with the controller's scan; it is compatible with other parallel data input devices and can be cascaded to input parallel numerical values above 999. If data from encoders are in Gray or BCD codes, the device converts them to binary for compatibility with PC registers.

Circle 444 on Inquiry Card

Programmable Machine Tool Controller

Up to 4-axis simultaneous, continuous path positioning can be attained with the Smart™ 9 CNC. It permits resolution from 0.09 to 1.8 deg/motor step, speeds to 4500 r/min, and torques from 30 to 5500 oz-in (0.2 to 38.5 N·m). Offered by Aerotech, Inc, 101 Zeta Dr, Pittsburgh, PA 15238, the microprocessor based unit can be used with open loop (stepping motor) or closed loop (encoded dc motor) drives. Features include 2-axis circular and 2-axis linear contouring, CRT display, full edit capability with absolute/incremental encoding, manual data input, and nested subroutines. Other features are program storage of up to 20k bytes, inch/metric programming, and ability to accept magnetic tape, TTY, RS-232, or paper tape reader inputs. □

Circle 445 on Inquiry Card

New ultra high speed Silicon Rectifiers in epoxy cases.

Axial lead Silicon Rectifiers with very fast recovery characteristics are now available in low cost epoxy case styles. An ideal alternative to high priced glass units, these high surge devices give unsurpassed performance through 400 volts.

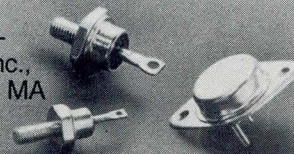
Field proven in countless industrial and computer applications, these units are especially attractive for high efficiency switching power supplies.

And that's not all. You can choose from the industry's widest range of very fast rectifiers with recovery times from 30 to 50 nsec max. Features include 20 to 70 amp ratings, low V_F , high surge and low leakage.

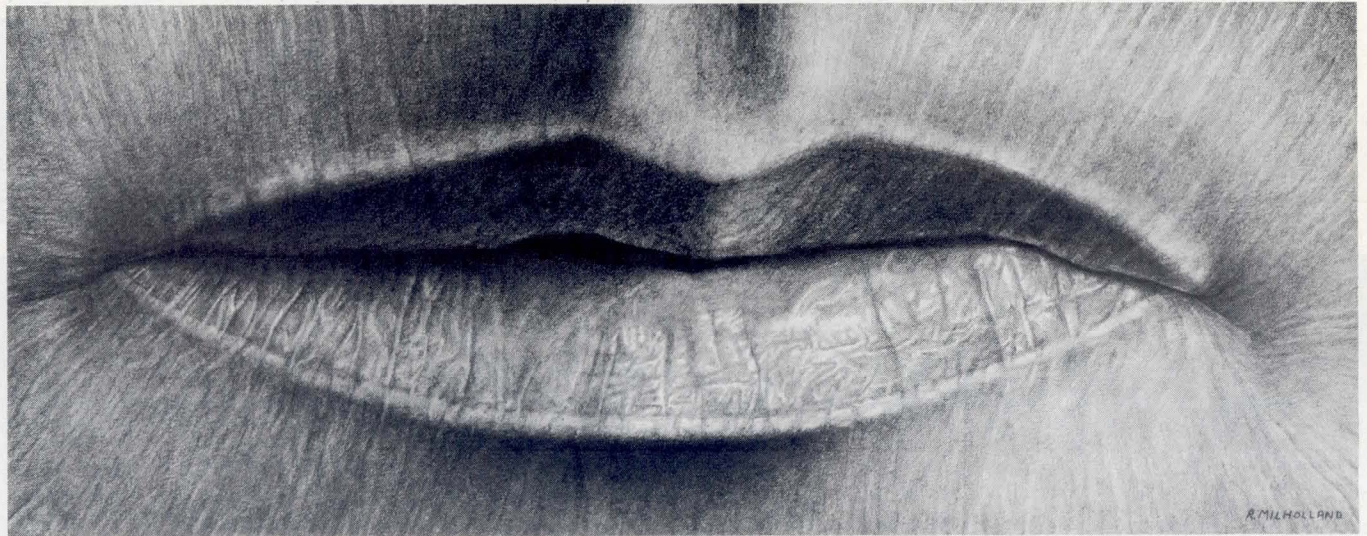
So when it comes to high speed rectifiers, come to Semicon for price and performance you'll like. Semicon Inc., 10 North Avenue, Burlington, MA 01803, (617) 272-9015.



Semicon
INC.



Promises, promises, promises.



We've made over 80,000 promises. And we've delivered every one of them.

Pertec® has shipped more tape drives into the minicomputer market than any other independent manufacturer in the world. Tension arm models. Vacuum column models. Microformatters and mini-size drives. Tape drives that set the industry standards. Available in thousands of final feature and specification configurations.

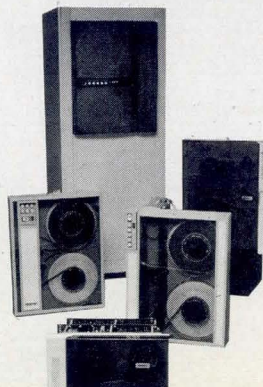
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Thanks to our sophisticated, high-volume production facilities, we're geared to meet your most

demanding time schedules. But then, that's what our promises are all about.

Write for our new full-line peripherals brochure. Pertec Computer Corporation, Peripherals Division, 21111 Erwin Street, Woodland Hills, California 91367. Or call (213) 996-1333 (Western Region); (603) 883-2100 (Northern Region); or (305) 784-5220 (Southern Region).

You don't get lip service... you get delivery.

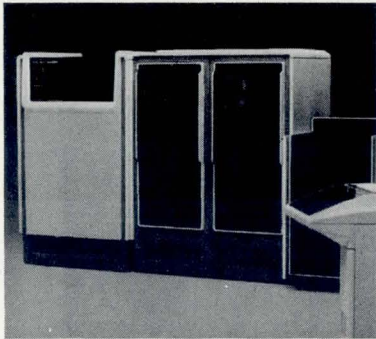


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WE SAW THE 32-BITS. AND



INDUSTRY'S RAISED 'EM.



INTRODUCING ECLIPSE® MV/8000, the fast new processor that gives you high throughput, high performance, and unmatched reliability, and the most compatible 32-bit computer system in the industry.

You need a 32-bit system that thinks fast. MV/8000's 36.4 MB/sec. memory bandwidth is two-to four-times faster than its nearest competitor. And it features a unique three-level I/O system using independent processors that drive high-speed busses and as many as 128 terminals.

Need hot architecture? MV/8000 gives you one of the industry's most advanced virtual memory management techniques, plus 4 gigabytes of logical address space, 6.6 gigabytes of on-line storage, and user programs as large as 512 megabytes—that's 16 times larger than the competition's.

Your MV/8000 also has unmatched reliability and maintainability. It comes with its own independent microNOVA™-based System Control Processor that continuously monitors a diagnostic bus, and identifies hardware faults right down to the field-replaceable unit. Plus, you get enhanced maintainability with a totally alterable control store—the first ever on a 32-bit mini-mainframe.

How about system security? MV/8000 gives you an 8-ring security system that divides the address space into eight imbedded protection areas, each with a unique privilege level. That secures system resources and user's privileged routines.

You need a 32-bit computer that speaks your language. MV/8000 speaks just about all of them, based on its new, ultra-sophisticated AOS/VS operating system that's compatible with our time-tested AOS (Advanced Operating System). AOS/VS has optimized micro-code for high-level languages like ANSI FORTRAN 77, ANSI BASIC, and ANSI PL/I. What's more, AOS/VS can run COBOL, DG/L, DG/DBMS, TPMS, INFOS II, AZ-TEXT™ word processing, RCX70 (3270) and RJE (2780/3780).

Compatibility? Forget about emulation, mode bits or rewrites. Along with its new 32-bit applications, MV/8000 executes all existing AOS-based ECLIPSE programs. You don't have to change programs, peripherals, interfacing, documentation, or people.

MV/8000, new from Data General. From now on we hold all the cards in 32-bit systems. Bet on it. And win.

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 Your MV/8000 sounds like a winner. Send
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CIRCLE 71 ON INQUIRY CARD

CD/9/80

Tektronix' new 7D02. logic analyzer with the

Now, a total solution to problems encountered either on or off the bus. Tektronix' new 7D02 Logic Analyzer. Featuring a unique user language that reduces even the most complex testing to a few simple statements. You supply the overview and the 7D02 does all the detail work for you. With a sophistication never before possible.

A simple, yet sophisticated user language.

Writing a test program is no more complicated than responding to a few simple prompts. A handful of basic phrases let you configure the 7D02's resources into almost any combination needed to solve the problem at hand. Often you'll find the 7D02 has an intelligence equal to the software you're integrating into your prototype.

Individualized 8- and 16-bit mnemonics.

Through a series of personality modules, the 7D02 can adapt to the characteristics of specific microprocessors. Familiar mnemonics let you work faster and more accurately. Support today extends to the 6800, 6802, 8085, 8086, Z80 and Z8002 with more to come. There's also a personality module available for general purpose logic analysis.

Up to 52 channels of information.

Flexibility is the key. You start with the basic 28 channels used for state acquisition, then the expansion option increases this to 44. For timing applications or wider state acquisition, there's an additional synchronous or asynchronous 8-channel timing option complete with its own memory, word recognizer and glitch trigger.

```

TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=18000
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1 THEN DO
1
1 1 COUNTER # 1 2-MS
1 1 2-RESET AND RUN
1 1 GOTO 2
1
1 END TEST 1
TEST 2
1IF
1 WORD RECOGNIZER # 2
1 DATA=XX
1 ADDRESS=F820
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1 THEN DO
1
1 GOTO 1
OR IF
1 COUNTER # 1 = 00100 2-MS
1 THEN DO
1 TRIGGER 0-MAIN
1 0-BEFORE DATA
1 0-SYSTEM UNDER TEST CONT.
1 0-STANDARD CLOCK QUAL.
1 END TEST 2
    
```

```

END TEST 1
TEST 2
1IF
1 WORD RECOGNIZER # 2
1 DATA=XX
1 ADDRESS=F820
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1 THEN DO
1
1 GOTO 1
OR IF
1 COUNTER # 1 = 00100 2-MS
1 THEN DO
1 TRIGGER 0-MAIN
1 0-BEFORE DATA
1 0-SYSTEM UNDER TEST CONT.
1 0-STANDARD CLOCK QUAL.
1 END TEST 2
    
```

All test parameters supplied by prompts.

IF clause defines a data stream event, which may be either single or compound.

THEN clause defines a response to the event. In this case, setting counter #1 to zero and then incrementing every millisecond.

At the same time the counter is set, branch to the second test. (bracketing allows simultaneous actions).

The 7D02 now monitors the data stream for an event to satisfy the second test's IF clause.

If the event occurs, then activate the trigger.

Or if counter #1 has reached 100 mS, then branch back to the first test and start the program over.

7D02 LOGIC ANALYZER

A user-programmable smartest triggering ever.

And there's more. The 7D02's user language takes advantage of four separate word recognizers, each up to 48 bits wide. Plus two counters usable in either the time or event mode. In addition to clock qualifications, there are two types of data qualification to provide selective data storage.

The Tektronix 7D02 Logic Analyzer can give you a whole new approach to μ P-based design.

Locating an intermittent fault. The following program gives a limited demonstration of the simplicity and power behind the 7D02's user language. Here the object is to trigger when a second event on the bus occurs within 100 mS of a first event.

```
CTR1=00100 HS TRIG LOC = 015
CTR2=00000 EUT TRIG IN TEST 2
```

LOC	ADDRESS	OPERATION	IRQ/NMT
00100	F8334	BNE \$F82C	11
00101	F8335	F6 READ	11
00102	F8220	INOC \$0006	11
00103	F8220	000 READ	11
00104	F8220	006 READ	11
00105	00006	000 READ	11
00106	00006	000 READ	11
00107	00006	000 WRITE	11
00108	F822F	BEOO \$F865	11
00109	F8230	004 READ	11
00110	F8231	T0004 \$0004	11
00111	F8232	000 READ	11
00112	F8233	004 READ	11
00113	F8234	004 READ	11
00114	F8234	BNE \$F82C	11
00115	F8235	F6 READ	11
00116	F8235	INOC \$0005	11
00117	F8235	000 READ	11

DISPLAY ← ACQMEM 0-MAIN
MNEMONIC
0 ABSOLUTE
1 MNEMONIC

By using the proper personality module, software flow can be displayed using the mnemonics of the chip under test, here the Motorola MC6802.



The 7D02 is a 3-wide plug-in for the popular Tektronix 7000 Series oscilloscope. Shown above is a Tek 7603 mainframe housing the 7D02 logic analyzer with a personality module supporting the 6802 microprocessor.

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 72 ON INQUIRY CARD

For the address of your nearest Tektronix Field Office, contact:

U.S.A., Asia, Australia, Central & South America, Japan Tektronix, Inc., P.O. Box 1700, Beaverton, OR 97075, Phone: 800/547-1512. Oregon only 800/644-9051, 503/644-0161, Telex: 910-467-8708, Cable: TEKTRONIX

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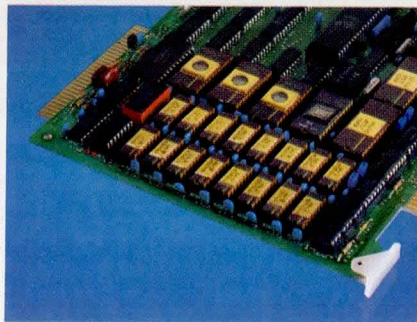
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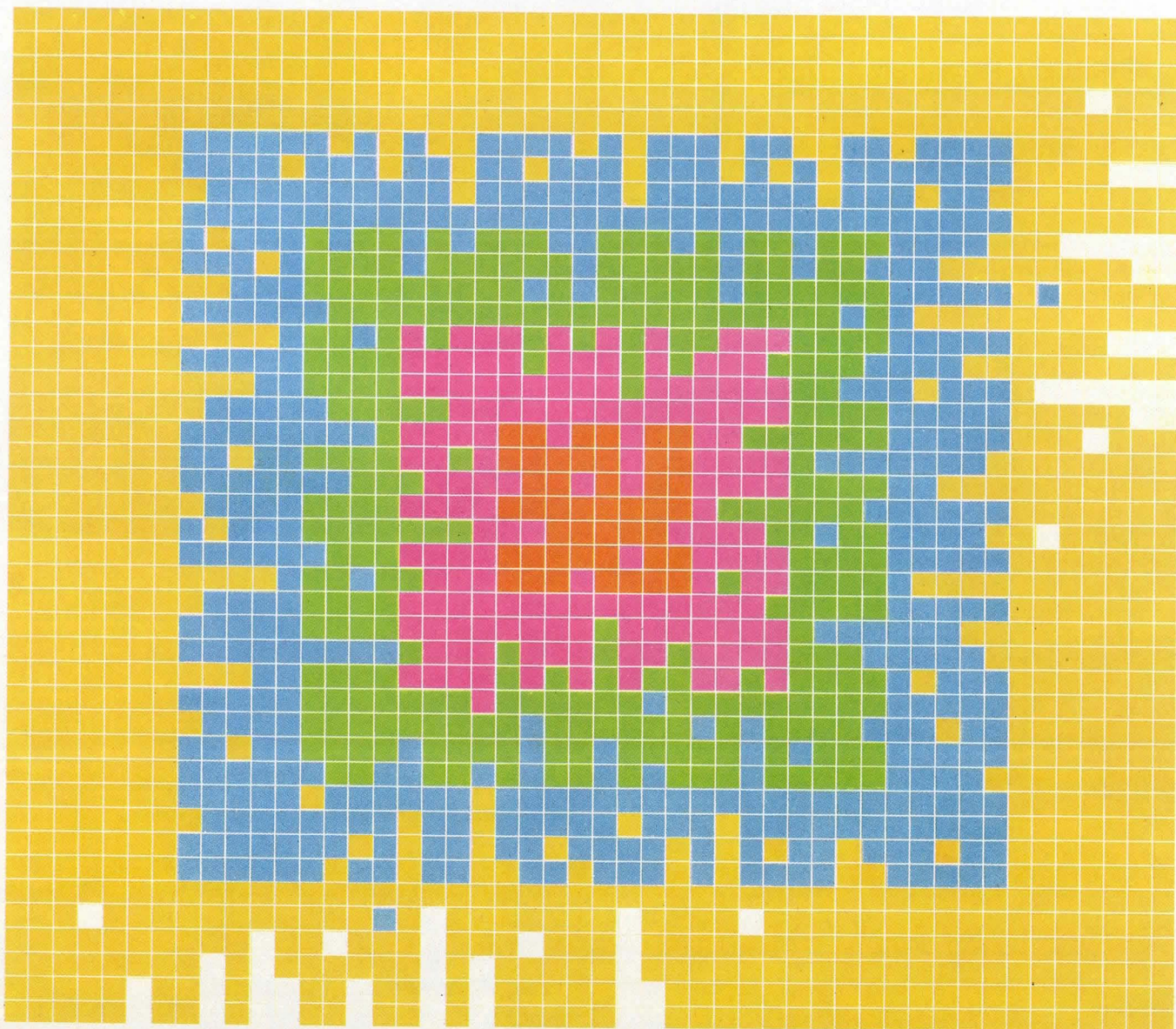
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MEETING THE CHALLENGE OF AUTOMATED ECL TESTING

High speed, nonsaturating operation, high power consumption, and the low impedance environment of ECL challenge automated test equipment as these devices find new application and grow in complexity

Robert L. Hopkins

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As the quest for speed in digital electronics continues, so does the growth of emitter coupled logic and closely related current mode logic device usage. Current mode devices, long familiar in large computer mainframes, are finding increasing application in speeding up functions of smaller computers and computer peripherals. An example is emitter coupled logic floating point multiplier chips, which provide smaller machines with cost effective, high speed scientific computation capability. These devices are finding new applications, are growing in complexity, and as they have already moved from small to medium scale integration, are moving now to large scale integration.

As with all device technologies, it is desirable to reduce the time and material expense involved in testing and reworking at the printed circuit (PC) board and system stages. Thorough device testing prior to these stages can sharply reduce the expense of finding and replacing defective devices later. For example, programs of 100% device testing regularly achieve an order of magnitude reduction in the number of defective devices reaching the PC board stage.

Automated test systems are commonly available for thorough testing of most logic families ranging in complexity from small scale integration (SSI) to very large scale integration (VLSI). The capabilities of these systems do not,

however, generally extend to high speed and the other special requirements of emitter coupled logic (ECL). ECL circuitry is distinguished from other logic families by speed, nonsaturating operation, high power consumption, and a low impedance environment. Clearly, high speed ac parametric testing, high current supplies, and careful design of fixtures become important characteristics of the required test system.

At the same time, fully automated operation also is required. In the past, ECL testing has commonly been handled with manual or, at best, semiautomated equipment. With the expansion in the number of devices and the increase in device complexity, these approaches no longer suffice.

ECL Testing Requires Thoroughness

If the applications of ECL were essentially the same as those of other logic families, the problems of testing would be greatly reduced as any of a number of commonly available automated test systems might be employed. But the applications are not the same. Since transistor-transistor logic (TTL) and metal oxide semiconductor (MOS) devices are readily available and relatively inexpensive, they unfortunately are often used in applications that do not begin to

tax their capabilities. ECL components, on the other hand, represent the state of the art for switching speed. This results in a tendency to use them closer to their specified limits. Obviously, this tendency makes it vital first to ascertain precisely what the limits are and then to assure that production devices meet those limits.

At the same time, the high power dissipation of ECL parts contributes to thermal fatigue, which can shorten life and may cause thermal drift of critical parameters. Thus, thorough testing takes on increased importance because of the need for reliability and the necessity of understanding parameter tolerances. This importance is emphasized again with the possibility of cost increases. ECL devices are normally soldered into PC boards to minimize stray capacitance. Without thorough testing, a bad device may not be discovered until the PC board level or system level and will be costly to replace.

Analog Aspects of ECL

ECL devices operate essentially as class A amplifiers. Their linear operation dictates a greater need for close attention to analog parameters than is the case in the testing of other logic families. Preshoot must be minimized in order to avoid saturation, and overshoot must be minimized to avoid circuit imbalance or possible damage to the device.

In addition, precise levels of supply and signal voltage are more critical in analog circuits than in digital circuits. This results in a need for greater resolution in sensing ECL voltage levels than might be required for other logic families. ECL's small signal swings and the variations with temperature in the signal levels compound this need.

What Will Test ECL?

A general rule of accuracy for any test equipment is that its maximum error contribution must be at least three times smaller but preferably ten times smaller than the smallest quantity to be measured. A problem arises when this criterion is applied to measurement of ECL time quantities. For other logic families such as TTL, timing measurements can be made using ECL circuitry to insure that tester delay times and rise and fall times will be small compared with those of the device being tested. Indeed, today's commercial device testers use ECL extensively. But what happens when testing ECL itself? No faster family is available to implement the tester.

For 100k ECL devices, a typical propagation delay is approximately 1.2 ns with a tolerance of ± 400 ps. A typical rise time is 800 ps ± 300 ps. Fortunately, it is not necessary that the tester propagation delay and rise times actually be three to ten times faster than those of the circuit under test. If careful attention is given to tester calibration and stability considerations, the time quantities contributed by the tester can be made to cancel out of the measurement. The same is not true, however, of tolerances on those quantities. Variations in tester propagation delay and rise time will occur from one tester to another and from one channel to another. What is more, the amount of variation can change with temperature and over time.

Use of the threefold criterion requires that tester propagation delay variations be held within ± 133 ps and rise time variations within ± 100 ps. For a tenfold improvement,

the tolerances become ± 40 ps and ± 30 ps, respectively. Absolute accuracies of this order can be achieved, but only with constant attention to calibration.

The most accurate measurements are those made by comparison with a known reference. If the comparator error is negligible, a very important "if," the only remaining error source is in the reference itself. The reference error can be made negligible by use of a known good device or standard for which a desired parameter, such as propagation delay, is measured under controlled laboratory conditions using precision instruments. If the propagation delay measured in the laboratory is 1.2 ns and the automated tester measures 1.7 ns, the tester has contributed an error of 500 ps. As long as this 500-ps discrepancy remains the same from measurement to measurement, it can be subtracted out to arrive at the correct propagation delay.

The need for the 500-ps discrepancy to remain constant is critical to the procedure just described. This requirement depends on the stability and linearity of the tester. Since absolute inaccuracies can be subtracted out, tester stability and linearity are probably more important than initial accuracy for testing ECL with its small signal swings, fast switching speed, and large temperature variations.

A careful study of measurement error sources shows a breakdown into three categories: (1) offset (such as the 500-ps error just discussed); (2) linearity (slope of measurement); and (3), repeatability (How much does the measurement vary over time?). Fig 1 illustrates all three of these factors graphically.

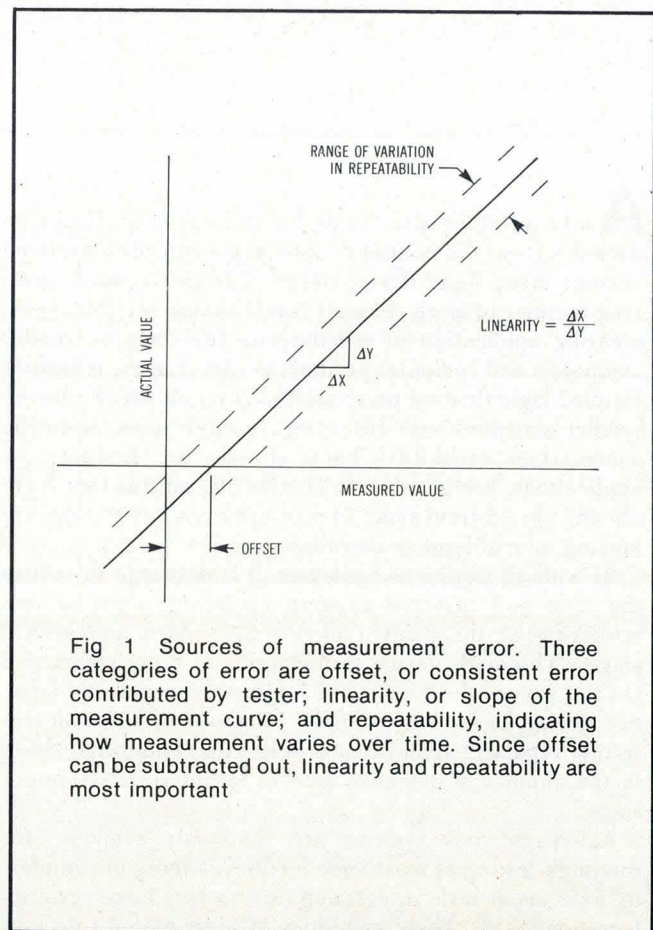


Fig 1 Sources of measurement error. Three categories of error are offset, or consistent error contributed by tester; linearity, or slope of the measurement curve; and repeatability, indicating how measurement varies over time. Since offset can be subtracted out, linearity and repeatability are most important

Offset can be accounted for by the means already described. Linearity and repeatability of the tester must be studied and specified over the expected range of values for propagation delay, rise time, and other desired parametric measurements. Once determined, both the offset and the linearity factors can be considered permanently established. Lack of exact repeatability, on the other hand, must be handled by periodic calibration. This periodic calibration is accomplished with an auto-calibrator, which consists of a sensor, a feedback loop, and a correction amplifier. The sensor in this case is a measurement routine designed to qualify or quantify the tester measurements against a standard. Some form of storage medium containing past error corrections constitutes the feedback loop. The correction amplifier consists of realtime hardware or software in the tester that adds the necessary corrections to the raw measurements.

Repeatability is important to more than tester accuracy. If the tester is relatively stable, calibration may be limited to perhaps once a day and will have little effect on testing. At the other extreme, variations over much shorter periods may necessitate incorporating the auto-calibration elements into the test program. It may then be necessary to dispense with some tests in the interest of maintaining throughput.

Relationships between ECL Elements

Rise time and propagation delay for a single ECL channel cannot be considered by themselves. Relative timing between channels or between functions also must be tested. Race conditions, the relative times at which two or more input signals reach a particular gate in a logic network, must receive consideration in testing as well as in design. Not only must race conditions be tested for in the device under test, but they must also be eliminated or compensated for in the tester. Fast switching speed makes testing for race conditions in ECL devices critical and aggravates the problem of minimizing these conditions in the tester.

Channel to channel skew in the tester (Fig 2) is probably the biggest contributing error source in race condition measurements. The tester skew can be calibrated for zero by subtracting out initially measured channel to channel variations. How long the calibration can be maintained across temperature variations is another matter. This error source is further complicated by channel to channel variations in rise time which may interact slightly differently with voltage thresholds, thereby affecting delay time. The net result is a desire to vary the position of switching edges from channel to channel under program control. Such control becomes a firm requirement if edges are to be deliberately offset from channel to channel in order to test a part's tolerance for skew. In fact, the capability is generally referred to as programmed skew control.

To implement effective skew control, programmable edge resolution must be finer for testing ECL than for other logic families. If channel to channel skew varies over a range of 500 ps and the tester has only 1-ns programmed edge resolution, programmed skew control is not possible. Instead, resolution on the order of 100 ps is required.

Setup and hold time are another type of measurement in the time relationships category. Both are critical to ECL testing. Setup time is defined as the time data reaching a storage latch must have been valid before a clock edge in

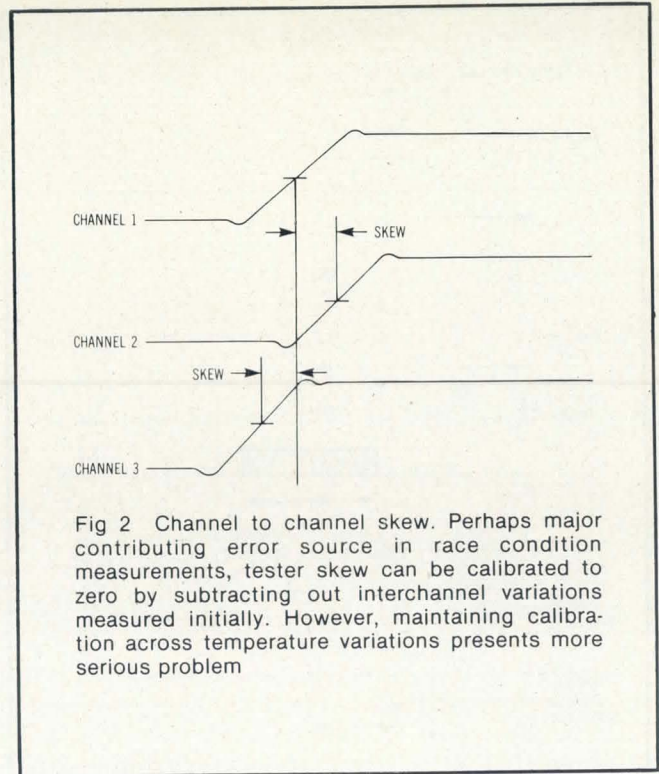


Fig 2 Channel to channel skew. Perhaps major contributing error source in race condition measurements, tester skew can be calibrated to zero by subtracting out interchannel variations measured initially. However, maintaining calibration across temperature variations presents more serious problem

order to be accepted. Hold time is the time data must remain valid after the clock edge to guarantee latching.

Consider a 300-MHz flipflop. Fig 3(a) shows the clock pulse train and a pulse that satisfies minimum setup and hold time requirements. Now consider Fig 3(b), where the same clock train is shown along with a data pulse, assumed to have zero tolerance on its time position with respect to the clock. In this example, both the nominal setup time and hold time are 1 ns. The nominal data pulse starts 2.3 ns before the second clock pulse and extends 1.5 ns beyond it. No problem is experienced in storing this data. Even if an extra gate must be added, causing a nominal 1.2-ns delay (100k ECL), the leading edge still occurs 1.1 ns before the clock, and capture is assured. However, if the delay has a 10% tolerance and the worst case leading edge of the data pulse is considered, only 980-ps setup time is available before the clock pulse. Nominal setup time is not satisfied, and storage cannot be guaranteed. If the setup time also has a 10% tolerance (worst case requirement of 1.1 ns), the situation becomes even worse. Absolute differences between a solidly reliable device and one that occasionally fails are very small when devices of these clock periods and delay times are involved. To resolve the edges adequately, the tester again must be able to position them with a resolution of approximately 100 ps in order to simulate worst case input conditions on the device under test.

Capacitance and Inductance Effects

As has been noted, aberrations in the high and low logic levels have a particularly deleterious effect on ECL. Maintaining a 50- Ω transmission line between tester pulse generator and the input pin of the device under test minimizes aberrations. Often the approach to stimulus in general purpose testers uses a single pulse generator with

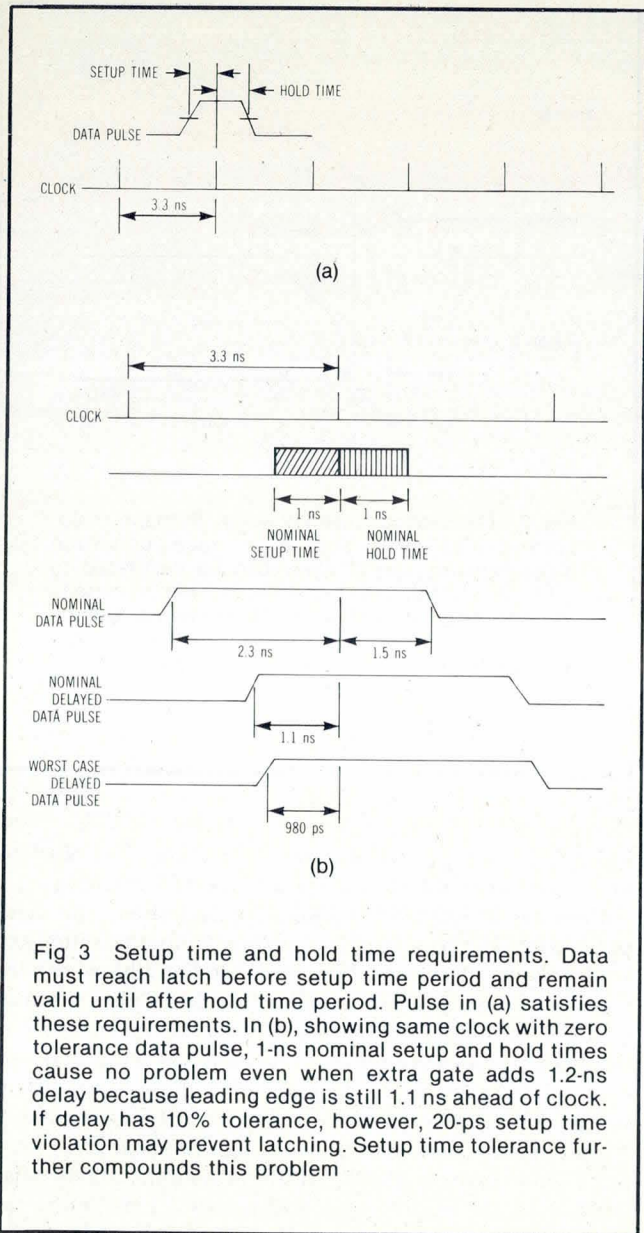


Fig 3 Setup time and hold time requirements. Data must reach latch before setup time period and remain valid until after hold time period. Pulse in (a) satisfies these requirements. In (b), showing same clock with zero tolerance data pulse, 1-ns nominal setup and hold times cause no problem even when extra gate adds 1.2-ns delay because leading edge is still 1.1 ns ahead of clock. If delay has 10% tolerance, however, 20-ps setup time violation may prevent latching. Setup time tolerance further compounds this problem

relays to switch its output to multiple input pins of the device under test. The added signal runs introduce stray capacitance; the relays add inductance. The resulting added delays and aberrations may be tolerable for testing many logic families, but they have disastrous effects on ECL measurement results. Compensation circuits that remedy the aberration problem generally add undesired attenuation of the signal. A better solution to this problem is discussed in the section entitled "Meeting ECL Test Criteria."

Tester Rise Time Effects

Another way to view the problem of ac parametric testing of ECL is by examining the effect of tester rise time on actual device timing measurements. Since tester rise time is not much faster than device rise time, unlike the case of TTL or MOS, the effect will not be negligible. Both device rise time and propagation delay measurements are affected.

Rise time of a 100k ECL device may be 700 ps. If tester rise time is 1 ns, the measured rise time for the device becomes

$$\text{measured } t_r = \sqrt{(0.700)^2 + (1)^2} = 1.221 \text{ ns}$$

This result can be read from the graph in Fig 4. The 521-ps departure from the actual value is far from negligible. Even if the tester rise time matches the 700-ps rise time of 100k ECL, the measured rise time is still 990 ps with an error of 290 ps.

In principle, the actual value can be recovered by using a software routine to calculate

$$\text{actual } t_r = \sqrt{(\text{measured } t_r)^2 - (\text{tester } t_r)^2}$$

However, this software recovery decreases tester throughput. In addition, there is some degradation due to the tester's finite timing measurement resolution. For a resolution of 100 ps, the 990-ps measurement cited above actually could be read as 900 ps. The resulting value for actual t_r recovered by software would be 566 ps. This error of 134 ps even with software compensation, while better than 290 ps, is still significant. The means for further reducing this error are explored in the next section.

Tester rise time also adds a potential error to propagation delay measurements. Any increase in rise time causes an increase in edge position uncertainty due to the voltage

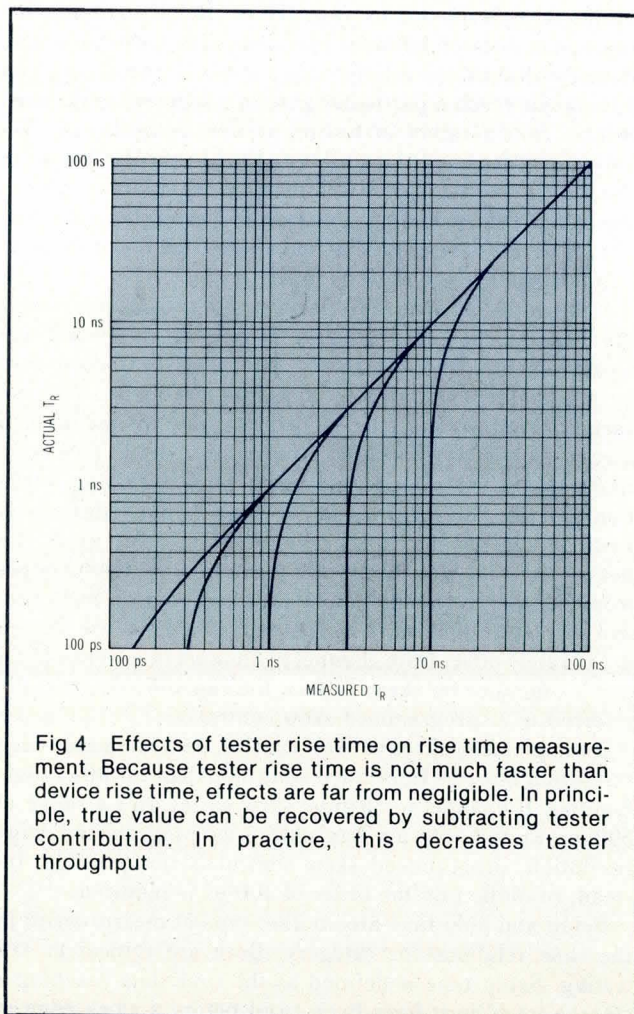
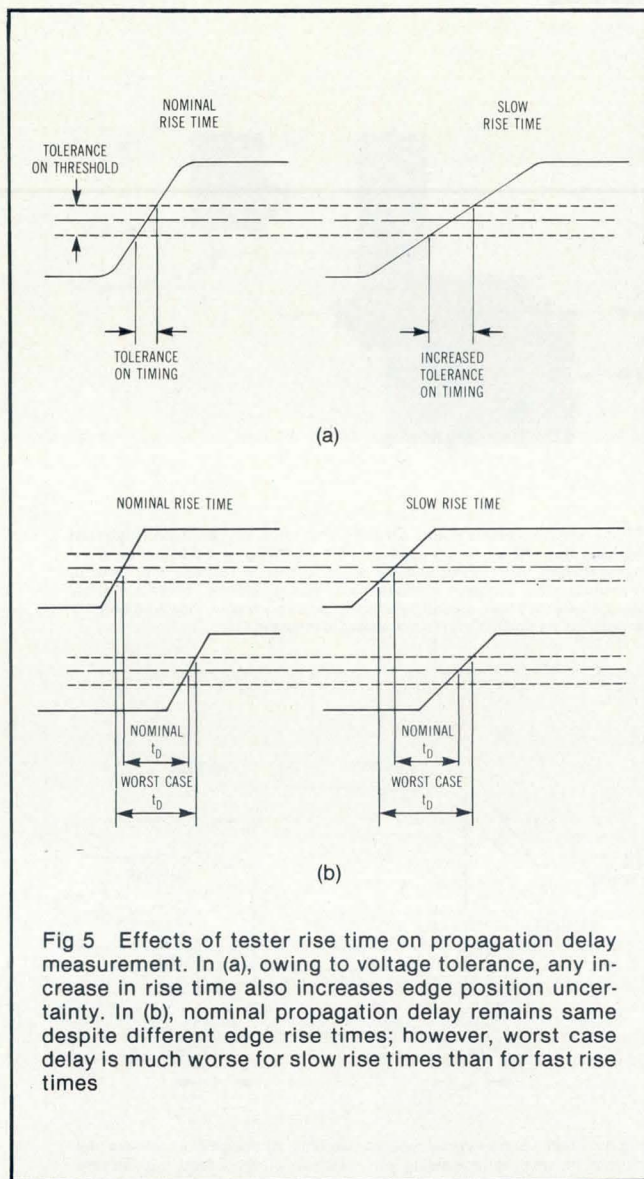


Fig 4 Effects of tester rise time on rise time measurement. Because tester rise time is not much faster than device rise time, effects are far from negligible. In principle, true value can be recovered by subtracting tester contribution. In practice, this decreases tester throughput

threshold tolerance [Fig 5(a)]. As shown in Fig 5(b), nominal delay remains the same regardless of rise times of the two edges. Worst case delay, however, is much worse for slow rise times than for fast ones.



Meeting ECL Test Criteria

The major functional blocks of any general purpose integrated test system include device fixturing, device stimulus, parametric measurement system, test pattern source, local memory for handling device inputs and storing test results at high speed, central controller/computer, mass storage, and various input/output devices to allow communication with the test programmer/operator. Performance of all of these blocks affects the quality of ECL testing. Requirements for most of them, however, are no different for ECL than for other devices. The exceptions to this are device fixturing, device stimulus, and the parametric measurement system. Following sections discuss these three

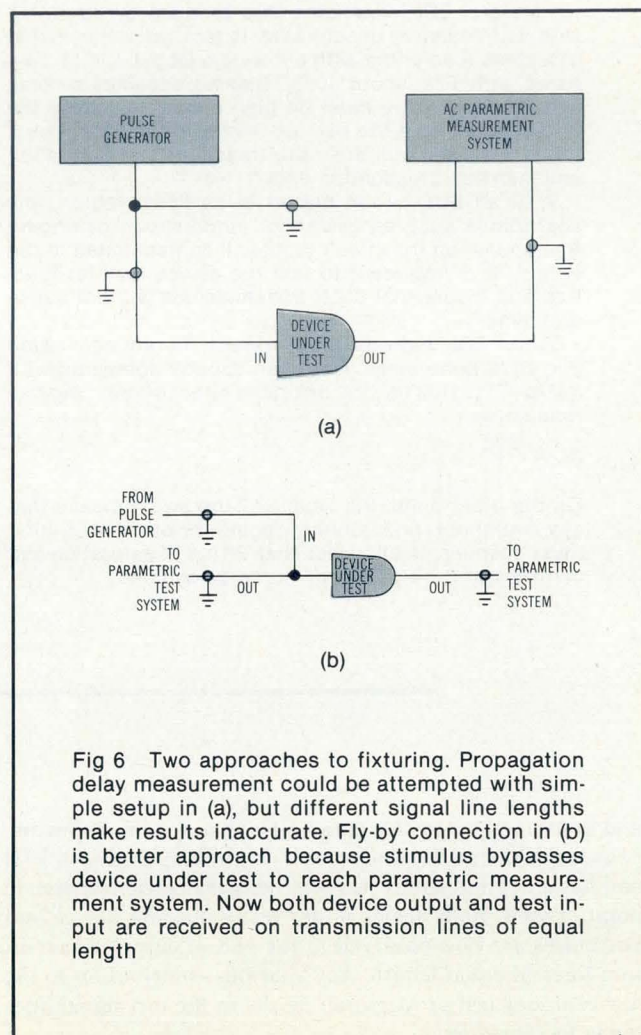
areas and draw examples from an actual functioning ECL tester, the S-3280, to illustrate results that are currently achievable.

Test Fixturing

Fixturing refers to the part of the tester that actually delivers input signals to the device under test and returns output from this device to the parametric measurement system. The need to maintain a 50-Ω transmission path all the way to the device under test is satisfied by using coaxial cable and connectors, strip line on PC boards, and proper line terminations.

A 50-Ω environment is not all there is to fixturing, however. For example, a propagation delay measurement could be attempted with the simple setup shown in Fig 6(a), but results are not likely to be very accurate. The electrical length of the signal line from the pulse generator to the parametric measurement system is probably quite different from that between the device under test and the measurement system. Propagation delay of these transmission lines is not negligible compared with ECL propagation delays.

The configuration shown in Fig 6(b) is a better approach. This configuration is called a fly-by connection because the stimulus pulse literally flies by the device under test input



The Basics of ECL

ECL is designed to achieve two advantages: the ability to drive a 50-Ω transmission line and higher gate speed than is possible with other logic families, with up to a sixfold speed increase over TTL (Fig A). Added speed can either implement faster devices or reduce component count. The two advantages are definitely related. For example, high speed serial data can be multiplexed, transmitted over coaxial cable, and demultiplexed using only ECL components at a minimum cost per unit of bandwidth despite the premium cost of ECL components. Current drive necessary for the 50-Ω transmission line capability helps ensure that stray capacitance will charge rapidly, thus increasing switching speed.

These advantages are not gained without cost. The increased current to charge the capacitance and drive the transmission line causes both switching and standby power to exceed that of TTL circuitry. Since the increased power must be dissipated throughout the device, ECL chips tend to be larger than those of other logic families.

Most logic devices, such as TTL devices, suffer substantial increases in propagation delay due to the capacitance of the collector base junctions of saturated transistors. ECL eliminates this problem by operating with its transistors unsaturated. In fact, operation is that of a class A amplifier with a low gain (about 4 to 5) compared with TTL (about 1000). Biasing becomes critical, and the input drive must be high enough to cause the output to achieve the desired level. On the other hand, too much input will drive the transistor into saturation and increase propagation delay.

With an ECL circuit biased in its linear region, any aberrations such as overshoot, undershoot, or ringing that appear on the circuit input will be transmitted to the output. It is important to test the device transfer function and insure that such transmissions will not cause problems.

While ECL delivers high current, its voltage swing (Fig B) is quite small, less than 850 mV compared with 3 V for TTL. This has the desirable effect of reducing rise time since

$$\Delta t = \frac{\Delta Vc}{I}$$

On the other hand, the small voltage swing means that any overshoot, undershoot, ringing, or other aberration must be much smaller, less than 25 mV, if saturation and insufficient drive problems are to be avoided.

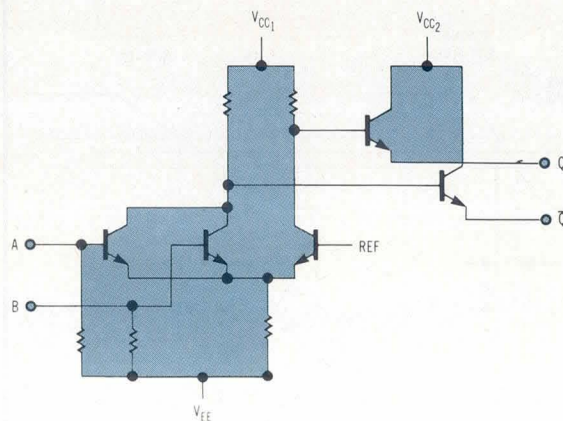


Fig A Emitter coupled logic. AND/OR logic implementation has high cost per gate but offers 5-ns propagation time, 50-mW power dissipation, 0.4-V noise margin, with fan in and fan out of 5 and 25 respectively. Difficult manufacturing process compromises active device characteristics. Devices are very fast, inherently uniform, and very stable, requiring only 1-V swing in 1 ns against a 3- to 5-V swing in 3 ns for TTL

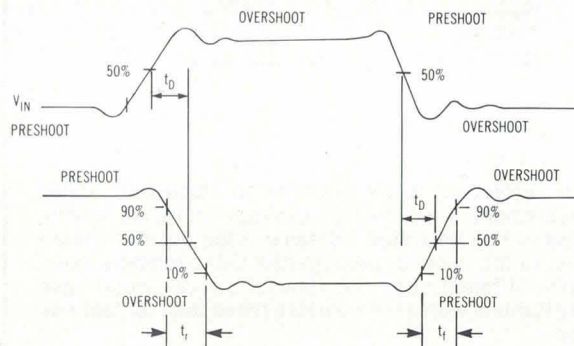


Fig B Small voltage swing reduces rise time. Although ECL delivers high current, its small voltage swing, with desirable effect of reducing rise time, means that overshoot, undershoot, and ringing must be kept very low to avoid saturation and insufficient drive problems

and continues on to the parametric test system. Input impedance of the device under test is high compared with 50 Ω and has a negligible effect. From the parametric test system point of view, both device under test input and device output pulses are now observed at the end of output transmission lines of equal length. Any spurious contribution to the device under test propagation delays in the two signal lines tends to cancel out.

To make the fly-by connection work, the input and output paths leading to the device input must be kept separated (eg, placed on opposite sides of a PC board), but must be able to be readily strapped together within the last 0.25 in before the device pin. It is necessary to provide an optional strap rather than a permanent connection between the lines because, for devices in general, a given pin location may be either an input or an output.

In order to avoid aberrations due to crosstalk, capacitance between input and output lines and between channels must be minimized. Fig 7 shows a fly-by connection fixture board for 100k ECL devices in 24-pin flat packages. Input and output paths for each pin result in 48 transmission lines. Low capacitance spring contacts mate the device under test to the fixture. Typical pin to pin capacitance is 0.1 pF, assuring extremely low crosstalk.

Stimulus

Input pins, output loads, and power supply voltages are all stimuli that must be precisely controlled for an ECL tester to achieve accurate measurement results. Power supply voltages must be independently programmable to allow margin testing. The real demand for accuracy and resolution on dc levels, however, comes from the signal pulses themselves. High and low signal levels must be independently programmable. Accuracy achieved must be on the order of 10 mV. If levels can be programmed with ten times greater resolution (1 mV), auto-calibration can be employed to achieve even greater accuracy by subtracting out known inaccuracies. Aberrations to the pulse must be held within 25 mV of the high and low levels.

As noted earlier, pulse drivers with subnanosecond rise times are required. In addition, variations in rise time from channel to channel must be minimal. Using hybrid integrated circuit technology, a tester has been implemented with drivers having less than 800-ps rise time for a 1-V signal into a 50- Ω load, making high and low levels programmable with the desired 1-mV resolution and minimal aberrations. A typical rise time for this driver appears in Fig 8.

Parametric Measurement

For ECL testing, parametric measurement is the most critical part of the test system. Without accuracy here, all of the speed and precision of the stimulus system and all of the care in fixturing are wasted. Aspects of the parametric measurement system that are especially critical include time/position resolution of the pulse edges of the high speed drivers, comparator speed and precision of threshold, resolution of signal level measurement, single-shot time interval measurements, and enhanced time interval measurement using sampling. In addition to basic measurement accuracy, repeatability for parametric measurement must be considered.

It has been noted that measurement of the short delay times and critical setup and hold times of ECL make it necessary to have fine resolution of the edge positioning on driver pulses. Deskewing of multiple driver channels also requires rather fine resolution of edge positioning. If automated calibration and correction for known delay errors are to take place, edge positioning must occur under program control. Fully programmed control with resolution between 100 and 200 ps has been achieved in practice.

Turning to the output of the device under test, comparators must have rise times faster than the ECL propagation delays to be measured if accurate results are to be obtained. More importantly, the channel to channel variation in comparator rise times must be small, as must the variation

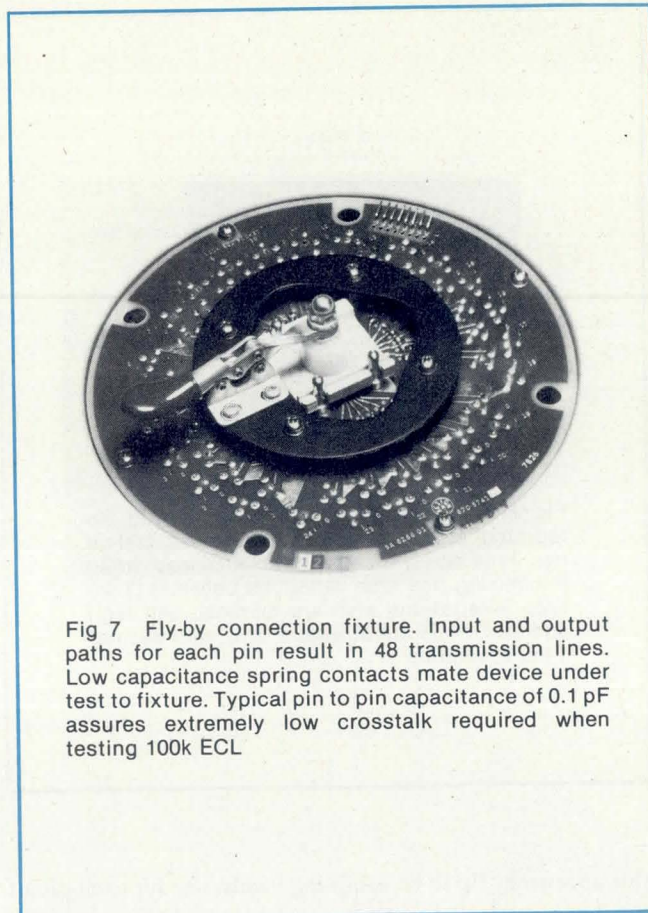


Fig 7 Fly-by connection fixture. Input and output paths for each pin result in 48 transmission lines. Low capacitance spring contacts mate device under test to fixture. Typical pin to pin capacitance of 0.1 pF assures extremely low crosstalk required when testing 100k ECL

from one measurement to the next. Programming resolution for the comparator threshold level must be small if errors of the type illustrated in Figs 4 and 5 are to be minimized. Equivalent comparator rise time of less than 500 ps has been achieved. Resolution of the programmed threshold setting is within 1 mV.

In addition to being repeatable, linear, and accurate, an ECL time interval measurement system should be capable of single-shot operation. This capability allows maximum testing throughput. To capture time intervals on a single pass, an analog time to voltage circuit has been employed successfully to generate a voltage proportional to the interval. Initial resolution of 50 ps has been achieved, with repeatability within 100 ps. An overall measurement accuracy within 300 ps is guaranteed.

Where greater accuracy on time interval measurement is desired, or where detailed information on the ECL waveform is needed, a multichannel sampling oscilloscope and waveform digitizer is a valuable supplement to single-channel time interval measurement. The tradeoff is increased test time, since many repetitions of the waveforms are required for the sampler to build up an accurate representation. The waveforms are digitized and stored in memory. Rise time, propagation delay, or overshoot can be calculated readily from the stored information. An equivalent tester rise time of 300 ps has been achieved with

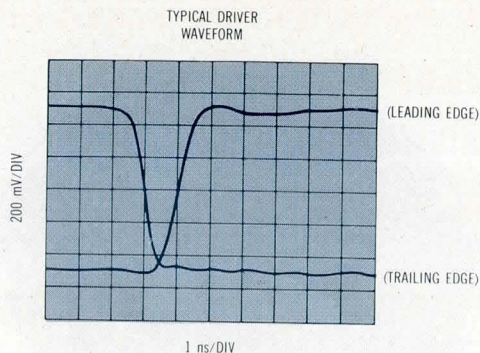


Fig 8 Typical driver rise time. Hybrid integrated circuit technology achieves 800-ps rise time for 1-V signal into 50-Ω load while minimizing rise time variations between channels. Aberrations also are minimal, and high and low levels are programmable with desired 1-mV resolution

this approach. Up to 64 sampling heads, one for each pin of the device under test, can be used on an S-3280 test system.

The 300-ps rise time of the sampling approach makes possible an accuracy gain in rise time measurements. It has been noted that a measurement on a 700-ps rise time could be in error by as much as 134 ps for a tester rise time of 700 ps, even when software correction was employed. By reducing tester rise time to 300 ps, the measured value without software correction becomes

$$\text{measured } t_r = \sqrt{(700)^2 + (300)^2} = 762 \text{ ps}$$

The error has been reduced from 134 ps to 62 ps without using software compensation.

For determining the precise values of ECL high and low voltage levels, high gain sample and hold circuits have been used. This approach allows a more leisurely measurement of the levels than would be possible on the high speed pulse itself. A separate sample and hold circuit has been used for each pin of the device under test. With this approach, voltage levels can be resolved well within 1 mV.

Conclusion

In the past few years, ECL devices have evolved in speed, in increasingly sophisticated temperature compensation, and in increased complexity. The movement from the 3-ns propagation delay of 10k ECL to the 1.2-ns delay of 100k ECL has placed increased demands on the ac parametric system of device testers. Sophisticated temperature compensation on the chip has made ECL a more stable logic family.

LSI ECL has recently become available. An example is the 4-bit slice microprocessor. This development required a reduction in the power dissipation per gate. One approach to the problem uses CML, which removes the final emitter-follower stage from an ECL gate circuit. This technique eliminates the ability to drive 50 Ω but greatly reduces power consumption. A number of these chips can now be mounted closely together on a common hybrid substrate. In this close coupled configuration, 50-Ω signal paths are not required, and very complex functions can be assembled, minimizing total device power dissipation. The final hybrid outputs can be designed to drive 50 Ω but now with the power of an LSI device behind them.

Obviously, increasing device speed and complexity continues to push tester capability. Whether tomorrow's fastest logic family is ECL or something else, that fastest family will represent the best that can be used to implement tester hardware. The techniques discussed will continue to apply. For testing high speed devices, tester vendors and users must continue to pay close attention to timing and measurement error sources, equipment calibration, equipment stability, and error correction schemes.



Robert L. Hopkins is a senior applications engineer for the semiconductor test systems group at Tektronix. An expert in high speed logic testing, he is currently responsible for evaluating systems from an applications standpoint. During the past nine years, he has been involved with hardware and software development for the company's S-3200 line of testers. He holds an associate in electronics technology degree from Idaho State University.

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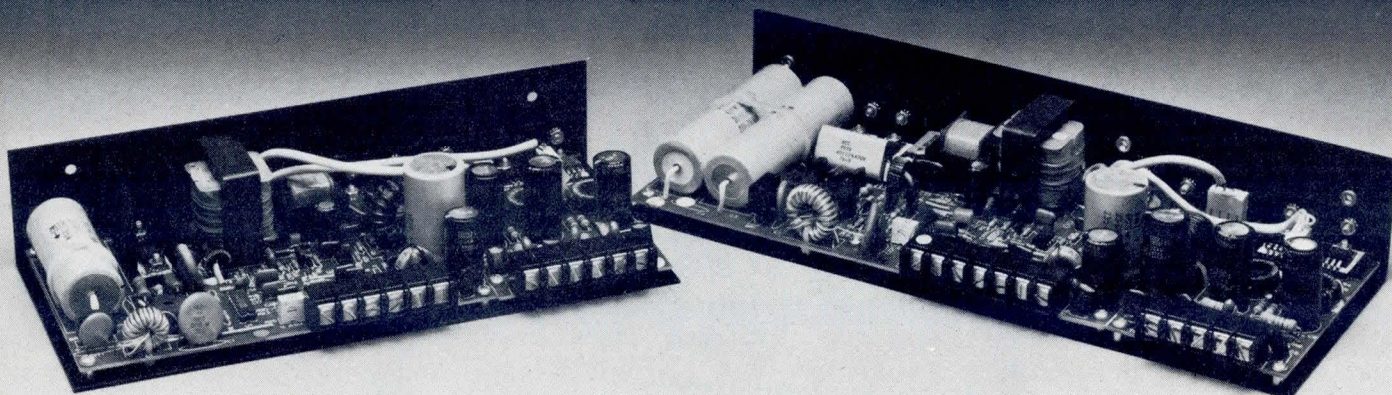
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	LMGT 75/15	5-15	15-1	15-1	
	LMGQ 75/12	5-15	12-1	12-1	5-1
	LMGQ 75/15	5-15	15-1	15-1	5-1
150 watts	LMG 5-20	5-20			
	LMGT 150/12	5-20	12-3	12-3	
	LMGT 150/15	5-20	15-2.4	15-2.4	
	LMGT 150/24	5-20	24-1.5	5-1	
	LMGQ 150/12	5-20	12-3	12-3	5-1
	LMGQ 150/15	5-20	15-2.4	15-2.4	5-1
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SINGLE-CHIP CONTROLLER INCREASES MICROPROCESSOR THROUGHPUT

Design technique uses semicustom logic to minimize hardware in a DMA controller that combines fast response with the potential to service multiple input or output devices and the flexibility to handle many different applications

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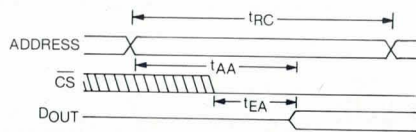
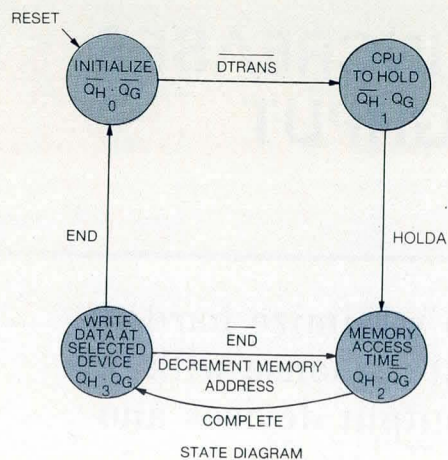
Microprocessors have a broad range of capabilities; yet they are unable to perform specific functions efficiently without hardware augmentation. One such function is transfer of blocks of data to or from processor controlled memory. Under specific conditions, such blocks may be moved efficiently by direct memory access. Data must be sequentially ordered, a starting address must be specified for both the processor associated memory and the external source or destination, and the data block length must be specified. When these three conditions are met, data transfer responsibility passes to a hardware controller, and data moves rapidly because instruction processing is eliminated during the transfer.

Although direct memory access (DMA) efficiently transfers blocks of data between a source and a destination, it normally interfaces memory with only a single external device and is unable to move data between memory and a distributed network. The need to interface a microprocessor with a network of distributed devices led to a generalized concept that can be structured to transfer data rapidly in either direction.

This concept is analogous to the DMA function in that blocks of sequential data are transferred to or from memory. It differs in that, externally, each data word has an associated device location. Implementing the transfer function in terms of this concept increases the data transfer rate while imposing four constraints on the system: the data block length must be constant; data must occupy sequential memory locations; the distributed devices are always serviced in the same sequence; and each implementation is committed to either input or output.

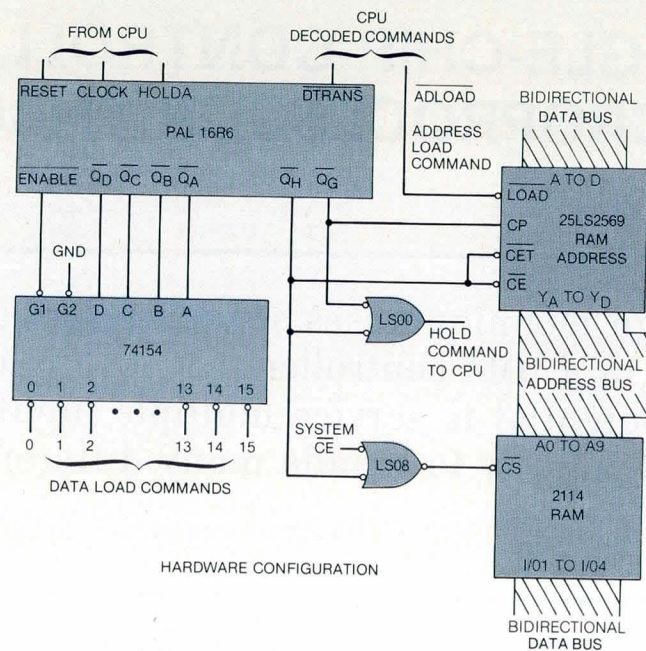
Controller Design Objectives

Conceptually, the controller accepts data transfer responsibility from the microprocessor upon command; steps through the data block, sequentially creating data paths between memory and various external devices; then returns control to the microprocessor. Functionally, upon receipt of the transfer mode command, the controller places the central processing unit (CPU) in the 3-state mode, generates all



t_{RC} = READ CYCLE TIME
 t_{AA} = ACCESS TIME - ADDRESS TO DOUT
 t_{EA} = ACCESS TIME - CHIP SELECT TO DOUT

RAM TIMING REQUIREMENTS



HARDWARE CONFIGURATION

GENERAL

1. CPU HOLD COMMAND IS $Q_G + Q_H$ (STATE 1, 2, OR 3)
2. STATE 2 IS ENTERED UPON RECEIPT OF HOLDA (CPU IN HOLD, CPU ADDRESS AND DATA BUSES 3-STATE)
3. IN STATES 2 AND 3 RAM ADDRESS COUNTER OUTPUT IS REMOVED FROM 3-STATE MODE AND ITS COUNT CAPABILITY ENABLED THROUGH CET
4. AT TRANSITION FROM STATE 3 TO STATE 2, BOTH DATA COUNTER AND RAM COUNTER ADDRESS ARE DECREMENTED BY RISING EDGE OF Q_G
5. UPON COMPLETION OF DATA TRANSFER (END), STATE 0 IS ENTERED FROM STATE 3. DATA COUNTER IS SET AT ITS INITIAL COUNT, ADDRESS COUNTER IS PLACED IN 3-STATE MODE, AND HOLD COMMAND TO CPU IS RELEASED

SPECIFIC (TRANSFER CPU MEMORY TO EXTERNAL DEVICES)

1. RAM IS SELECTED IN STATES 2 AND 3, $\overline{Q_H}$
2. IN STATE 3, ENABLE SELECTS DEMULTIPLEXER, AND CONTENTS OF DATA COUNTER (Q_A THROUGH Q_D) ARE DECODED TO GENERATE DATA LOAD (WRITE ENABLE) PULSE

SEQUENCE OF EVENTS

equations that control sequence of events shown in state diagram

Fig 1 Transfer from CPU memory to device. PAL implements two categories of Boolean expressions, data counters that control destination selection and state

required timing and control signals, sequentially creates the data paths, and transfers data through each path. Upon completion of the data transfer, it relinquishes control to the microprocessor, which then resumes instruction processing.

Increased throughput is the implementation rationale; therefore, the two primary design objectives are to enter and leave the data transfer mode in a minimum number of clock periods and to transfer one data word every two clock periods. This transfer rate allows one clock period to establish each data path, with the write pulse created in the second period to complete the transfer. Secondary design objectives relate to implementation and allow modification to meet varying applications using a minimal amount of additional circuitry.

Design approaches that meet these objectives include use of a state sequencer to meet the control transfer and data transmission timing requirements, and use of fusible link, semicustom logic to meet the circuit flexibility and minimization requirements. A simplified microprocessor interface is achieved by incorporating the microprocessor clock and hold capabilities into the sequencer design.

State Sequencer

The state sequencer organizes and concentrates logical functions to realize the high density capabilities of semicustom logic. What determines the number of control flipflops is the number of required states; therefore,

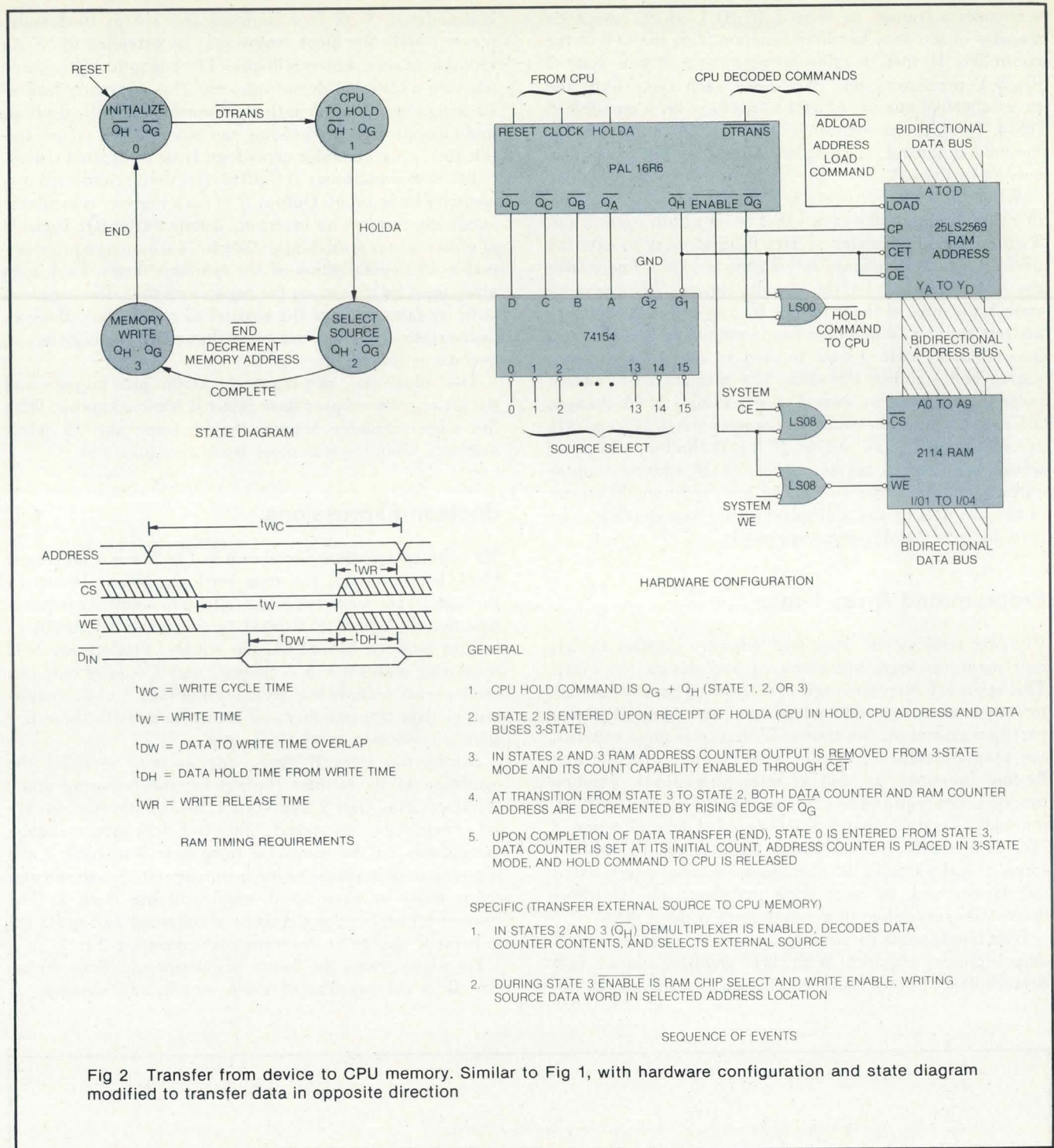


Fig 2 Transfer from device to CPU memory. Similar to Fig 1, with hardware configuration and state diagram modified to transfer data in opposite direction

performing all logic functions in four states reduces the sequencer design requirement to two flipflops and helps meet the secondary design objective. These four states are idle, when the CPU has system control; transitional, while the CPU is entering the hold mode and relinquishing control; and two data transfer, one permitting address and data stabilization, and the other creating the write command (Figs 1 and 2).

In this application, both flipflops are reset in the idle state ($\overline{Q_H}, \overline{Q_G}$, state 0) awaiting a software generated com-

mand (\overline{DTRANS}), which sets the G flipflop, advances the sequencer to state 1 ($\overline{Q_H}, \overline{Q_G}$), and initiates a CPU hold command, sustained until the sequencer returns to state 0. The CPU tests its hold command input each machine cycle and, upon sensing a command, enters the hold state, placing its data bus, address bus, and some control lines in the 3-state mode. It remains in this state until the hold command is released by the sequencer.

When it enters the hold state, the CPU issues a hold acknowledge (HOLD). Upon receipt of HOLD, the

sequencer advances to state 2 (Q_H, Q_C), which completes transfer of the data handling function from the CPU to the controller. It then toggles between state 2 and state 3 (Q_H, Q_C), processing one data word each cycle until the preestablished number of data words have been transferred (END). Then, the sequencer returns to state 0 and releases the hold command, allowing resumption of instruction processing by the CPU.

While the sequence of states is the same for data transfer in either direction, the events that occur within states 2 and 3 differ. During transfer of data from memory to external devices, state 2 is memory access time and state 3 generates the load command for the specific device. When leaving state 3, the edge of the G flipflop (\bar{Q}_G) advances the memory address counter. When data from external devices are read into memory, state 2 time is used to select the external source and stabilize the data. The memory write enable pulse is generated by state 3, and leaving state 3 changes the memory address counter. Transfer states ST2 and ST3 are identified by the output of the H flipflop, which activates the random access memory (RAM) address counter outputs, enables address counting, and, additionally, selects either the RAM or the multiplexer when transferring to or from the external devices, respectively.

Programmed Array Logic

Utilizing semicustom integrated circuitry satisfies the requirement for logic minimization and design flexibility. This approach increases logic density by mitigating two factors that increase random logic package count: function partitioning and pin limitation. To maximize these benefits, the programmable logic chip must contain AND, OR, and flipflop functions, as well as internal feedback. Flipflop functions are required to implement the sequencer and, additionally, a counter that is decremented at the completion of each data transfer (state 3 to state 2 transition). The counter serves a dual purpose: the demultiplexed count selects external devices and, by monitoring the count, the controller determines completion of the data block transfer (END).

Data block length determines the number of counters and demultiplexers required. With three counters and a 3 to 8 demultiplexer (74138), block lengths up to eight may be ac-

commodated. With four counters and a 4 to 16 demultiplexer (74157), the block length may be extended to 16. An increase to six counters will allow block length expansion to 64, with additional demultiplexers. This approach focuses on design for a block length of 16 words so that the flipflops and associated input decoding can be contained on one fusible link, programmable array logic (PAL) integrated circuit.

PAL 16R6 contains six D flipflops (registers) connected to a common clock input. Output Q of each register is available externally through an inverting, 3-state buffer (\bar{Q}). Input D of each register is an 8-input OR gate, each input a programmable AND combination of the available terms. Each gate array must be true to set the register on the following clock pulse or false to allow the register to reset. Thus, Boolean expressions state the conditions that cause the registers to become or remain set.

Two additional, non-register, AND-OR gate outputs and the six register outputs have internal feedback paths. With the eight available inputs, they become the 16 terms available when implementing Boolean expressions.

Boolean Expressions

Six counter equations are shown in Fig 3. For a maximum block length of 16, the four least significant counts (A through D) are required; expansion up to length 32 requires equation E; equation F must be implemented for block lengths between 33 and 64. The counter flipflops are held set during states 0 and 1. States 2 and 3 require only one clock period each; hence, from leaving state 1 until completion of data transmission and return to state 0, there is a state transition in every clock cycle.

During this interval, each equation must establish the condition of its counter flipflop for the following state. When entering state 2 from state 1, the counter flipflops are set as established by state 1. Since it is necessary to change the counter on the transition from state 3 to state 2, the counting decision must be made during state 3, and the new count must be established when entering state 2. The counter register content must be maintained during state 2 to prevent change at the transition from state 2 to 3.

Fig 3 also shows the 2-state sequencer equations. Equation G is independent of block length, and equation H

$$\begin{aligned}
 Q_F &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_F + Q_H \cdot Q_G (Q_F \cdot Q_E + Q_F \cdot Q_D + Q_F \cdot Q_C + Q_F \cdot Q_B + Q_F \cdot Q_A) \\
 Q_E &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_E + Q_H \cdot Q_G (Q_E \cdot Q_D + Q_E \cdot Q_C + Q_E \cdot Q_B + Q_E \cdot Q_A + \bar{Q}_E \cdot \bar{Q}_D \cdot \bar{Q}_C \cdot \bar{Q}_B \cdot \bar{Q}_A) \\
 Q_D &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_D + Q_H \cdot Q_G (Q_D \cdot Q_C + Q_D \cdot Q_B + Q_D \cdot Q_A + \bar{Q}_D \cdot \bar{Q}_C \cdot \bar{Q}_B \cdot \bar{Q}_A) \\
 Q_C &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_C + Q_H \cdot Q_G (Q_C \cdot Q_B + Q_C \cdot Q_A + \bar{Q}_C \cdot \bar{Q}_B \cdot \bar{Q}_A) \\
 Q_B &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_B + Q_H \cdot Q_G (Q_B \cdot Q_A + \bar{Q}_B \cdot \bar{Q}_A) \\
 Q_A &= \bar{Q}_H + Q_H \cdot \bar{Q}_G \cdot Q_A + Q_H \cdot Q_G \cdot \bar{Q}_A \\
 Q_G &= \text{RESET} (\bar{Q}_H \cdot \bar{Q}_G \cdot \overline{\text{DTRANS}} + \bar{Q}_H \cdot Q_G \cdot \overline{\text{HOLDA}} + Q_H \cdot \bar{Q}_G) \\
 Q_H &= \text{RESET} (\bar{Q}_H \cdot Q_G \cdot \text{HOLDA} + Q_H \cdot \bar{Q}_G + Q_H \cdot Q_G (\text{END}))
 \end{aligned}$$

Fig 3 Boolean statements. PAL registers implement data counter and state controller equations. Control equation G is independent of block length. Control equation H must be expanded by expression for END to establish block length

incorporates the block length ($\overline{\text{END}}$) decoding. The table, Block Length Control, shows the expressions for $\overline{\text{END}}$, when six counters are used, organized by remainder of a modulo 16 number. For shorter block lengths, references to unimplemented counters are ignored. Both control flipflops are reset (expressions false) when the computer issues a RESET command, establishing state 0. This state is maintained until the CPU issues $\overline{\text{DTRANS}}$, advancing the sequencer to state 1 by setting G.

A hold command is generated by the sequencer, which waits in state 1 until the CPU responds with $\overline{\text{HOLDA}}$, verifying that it has stopped instruction processing and that its buses are 3-stated. $\overline{\text{HOLDA}}$ resets G and sets H, advancing the sequencer to state 2. The G flipflop then toggles, causing the sequencer to cycle between states 2 and 3. H remains set during both states but tests the content of the data counter during state 3 to determine if data transmission is complete ($\overline{\text{END}}$ expression false). $\overline{\text{END}}$ false also causes the H flipflop to reset at the completion of state 3, returning the sequencer to state 0 and releasing the hold command to the CPU.

Implementation

System parameters were developed for use with the model 8085 microprocessor, the 2114 bidirectional RAM, and the 25LS2569 binary up/down counter. Attributes of these components that help meet the design goals are (a) availability of the CPU interface signals reset, clock out, hold, and hold

Block Length Control*

Remainder	$\overline{\text{END}}$ Expression
1	$Q_F + Q_E$
2	$Q_F + Q_E + Q_A$
3	$Q_F + Q_E + Q_B$
4	$Q_F + Q_E + Q_B + Q_A$
5	$Q_F + Q_E + Q_C$
6	$Q_F + Q_E + Q_C + Q_A$
7	$Q_F + Q_E + Q_C + Q_B$
8	$Q_F + Q_E + Q_C + Q_B + Q_A$
9	$Q_F + Q_E + Q_D$
10	$Q_F + Q_E + Q_D + Q_A$
11	$Q_F + Q_E + Q_D + Q_B$
12	$Q_F + Q_E + Q_D + Q_B + Q_A$
13	$Q_F + Q_E + Q_D + Q_C$
14	$Q_F + Q_E + Q_D + Q_C + Q_A$
15	$Q_F + Q_E + Q_D + Q_C + Q_B$
0	$Q_F + Q_E + Q_D + Q_C + Q_B + Q_A$

*Required to complete equation H in Fig 3, $\overline{\text{END}}$ expressions are listed by modulo 16 remainder of data word count. Counter F is not required for block sizes less than 33. Counter E is not required for block sizes less than 17. Single word transmission is a trivial solution

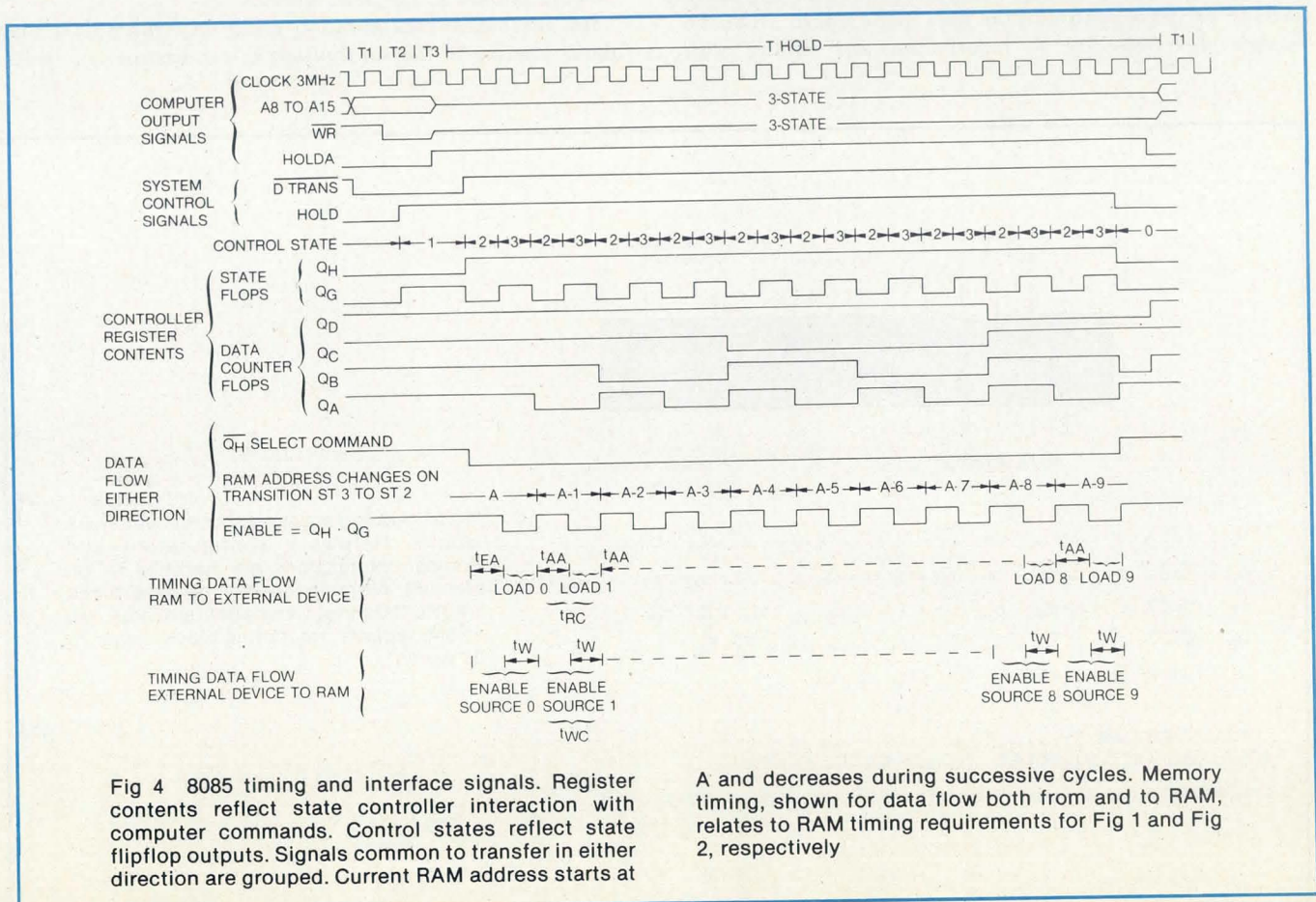


Fig 4 8085 timing and interface signals. Register contents reflect state controller interaction with computer commands. Control states reflect state flipflop outputs. Signals common to transfer in either direction are grouped. Current RAM address starts at

A and decreases during successive cycles. Memory timing, shown for data flow both from and to RAM, relates to RAM timing requirements for Fig 1 and Fig 2, respectively

acknowledge; (b) the RAM's high density, 4-bit data word, bidirectional data bus, and simplified dual control line interface; and (c) the counter synchronized load, increment, and decrement controls, and also its 3-state output and cascading capabilities. Additionally, the response and operating speeds of the RAM and counter are compatible with the microprocessor clock.

Figs 1, 2, and 4 show the configuration and timing relationships achieved by using these components. Microprocessor choice establishes the system clock rate and the method of passing control between the microprocessor and the data controller. The method of implementing the data controller, which meets the dual requirements of simplicity and high throughput, restricts RAM selection. In Figs 1 and 2, t_{RC} and t_{WC} cannot exceed two clock periods. When moving data to external devices, the devices must be able to function within the constraints of t_{AA} and t_{EA} . When moving data to the CPU memory, its write requirements, t_W and t_{DW} , must be less than one clock period. Because of the controller structure, t_{DH} and t_{WR} must both be zero, a restriction satisfied by many RAMs currently available.

Adaptation

Distributed data port servicing is the primary functional requirement of the data controller, and the specific number of ports is a parameter written into the Boolean expressions implemented by a member of the PAL family. The inherent flexibility arising from implementation of many of the logic functions by easily modified Boolean expressions can be demonstrated by extending the application requirements to include program control of the data block length. Now, the design objectives are to incorporate this feature with

minimal hardware reconfiguration and to retain all the operational attributes of the original DMA controller.

Although the state sequencer remains conceptually unchanged, its interaction with the data counter must be modified to implement a variable block length. The original concept has a fixed data block length, with the data counter starting at all 1s and decrementing to a predetermined end count. Its advantages are that the CPU interface is minimized and that all data ports are serviced during each DMA cycle. To implement the variable block length feature, the CPU loads the data counter with the actual count; then during data transfer, the state sequencer decrements the count to 0, the end count that terminates the operation.

It is desirable to implement the state sequencer and data counter on a single programmable chip while maximizing the data counter length. To achieve this, a 16R8 programmable logic chip replaces the 16R6 used previously. This change increases the number of registers by two at the expense of the two gated outputs. The chip configuration now offers eight data inputs; eight D registers, each with an inverting output; a register clock input; and a 3-state control input.

Of the eight registers, two are required for the state sequencer, allowing a maximum block length of 64 in a single-chip implementation. However, three control lines are required: \overline{HOLDA} and \overline{DTRANS} , as in the original concept, plus a software generated \overline{LOADA} , which transfers the content of the data bus to the data registers. Additionally, the \overline{LOADA} command must be used to initialize the state counter (Fig 5). With this approach, five inputs remain for the data bus, limiting the block size to 32 words.

An alternative configuration using only three data bits allows loading of the six flipflops in two instruction cycles

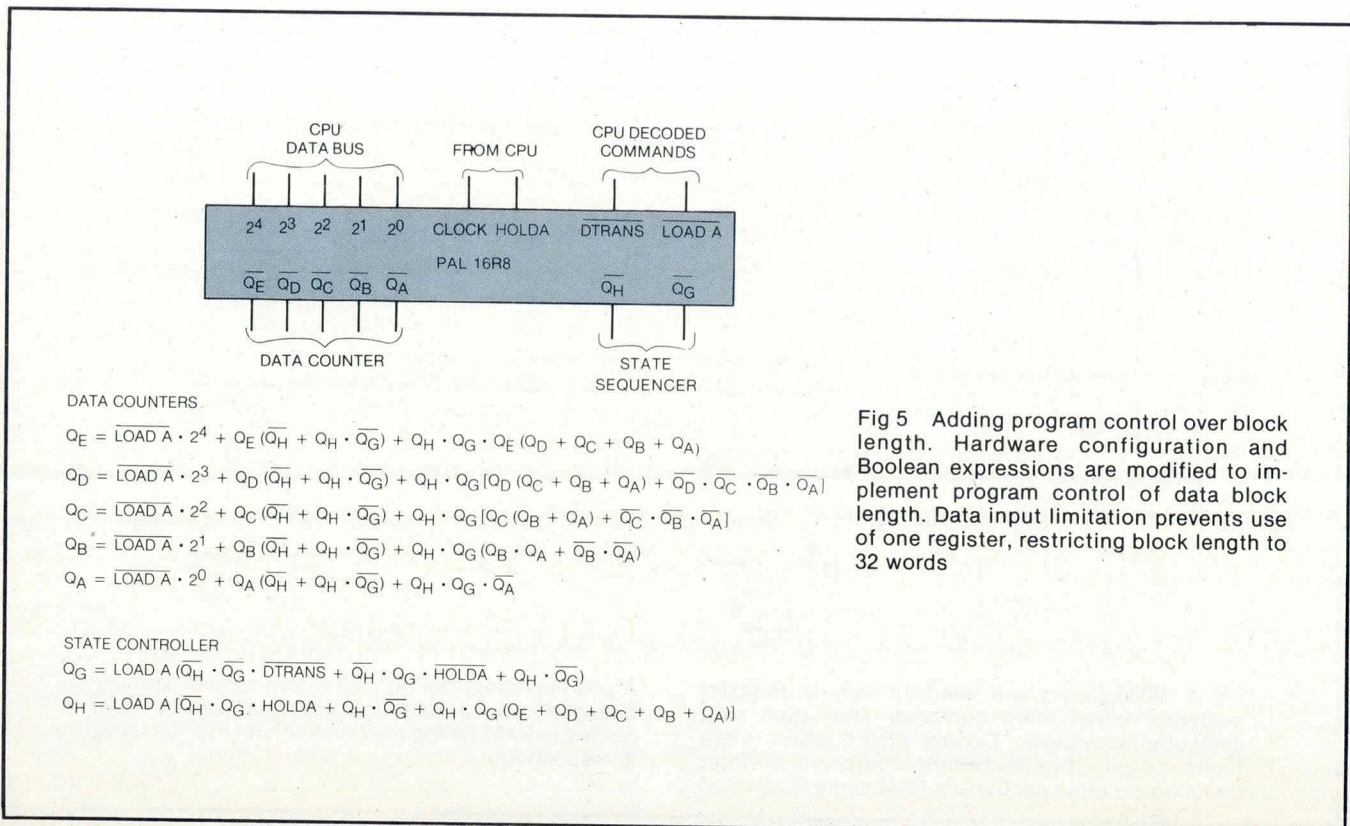
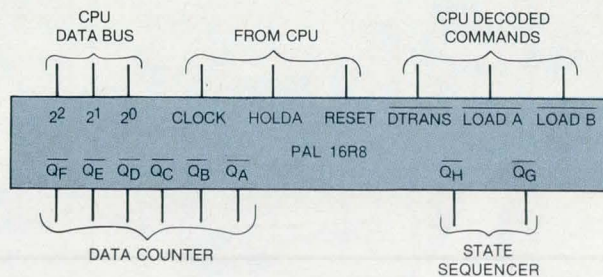


Fig 5 Adding program control over block length. Hardware configuration and Boolean expressions are modified to implement program control of data block length. Data input limitation prevents use of one register, restricting block length to 32 words



DATA COUNTERS

$$Q_F = \overline{\text{LOAD B}} \cdot 2^2 + Q_F (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G \cdot Q_F (Q_E + Q_D + Q_C + Q_B + Q_A)$$

$$Q_E = \overline{\text{LOAD B}} \cdot 2^1 + Q_E (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G [Q_E (Q_D + Q_C + Q_B + Q_A) + \overline{Q_E} \cdot \overline{Q_D} \cdot \overline{Q_C} \cdot \overline{Q_B} \cdot \overline{Q_A}]$$

$$Q_D = \overline{\text{LOAD B}} \cdot 2^0 + Q_D (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G [Q_D (Q_C + Q_B + Q_A) + \overline{Q_D} \cdot \overline{Q_C} \cdot \overline{Q_B} \cdot \overline{Q_A}]$$

$$Q_C = \overline{\text{LOAD A}} \cdot 2^2 + Q_C (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G [Q_C (Q_B + Q_A) + \overline{Q_C} \cdot \overline{Q_B} \cdot \overline{Q_A}]$$

$$Q_B = \overline{\text{LOAD A}} \cdot 2^1 + Q_B (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G (Q_B \cdot Q_A + \overline{Q_B} \cdot \overline{Q_A})$$

$$Q_A = \overline{\text{LOAD A}} \cdot 2^0 + Q_A (\overline{Q_H} + Q_H \cdot \overline{Q_G}) + Q_H \cdot Q_G \cdot \overline{Q_A}$$

STATE CONTROLLER

$$Q_G = \text{RESET} (\overline{Q_H} \cdot \overline{Q_G} \cdot \text{DTRANS} + \overline{Q_H} \cdot Q_G \cdot \text{HOLDA} + Q_H \cdot \overline{Q_G})$$

$$Q_H = \text{RESET} (\overline{Q_H} \cdot Q_G \cdot \text{HOLDA} + Q_H \cdot \overline{Q_G} + Q_H \cdot Q_G (Q_F + Q_E + Q_D + Q_C + Q_B + Q_A))$$

Fig 6 Extending block length. Additional modification increases block length to 64 words by using all internal registers. All capabilities of previous configuration have been maintained across both modifications

by implementing a second load command, $\overline{\text{LOAD B}}$. The DMA controller now handles block lengths as long as 64 data words, and the RESET command can be used to initialize the state counter as in the original concept (Fig 6).

Summary

Generally, a design approach and its means of implementation should be complementary. Specifically, the controller design objectives are met by utilizing a state sequencer, and implementation compatibility is assured by such features of semicustom logic as multiple storage elements with internal feedback paths, dense gating arrays, and interconnection flexibility.

The process of creating a state sequencer to solve a design problem results in a series of Boolean expressions that define the controller capability and the gate array that must be effected. Several partially dedicated gating and register arrays constitute the semicustom logic family. After the most suitable array configuration is selected, the interconnections, as expressed by Boolean statements, are completed to implement the design. This creates a unique logic pattern whose dense gating contributes to chip count minimization. Design variations can be accommodated by restructuring the gating arrays with minimal hardware reconfiguration. Thus, the system can be tailored to the original operating requirements and yet be easily adapted if modifications are desired.

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OPTIMIZING MINICOMPUTER POWER SUBSYSTEM DESIGN

Modular power supply design aids minicomputer expansion and repair by interfacing controller and front end modules to three nearly identical converter modules in a basic subsystem that can be replicated for each cabinet

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Tinton Falls, NJ 07724

A successful minicomputer calls for a number of basic design elements. Of these, three related features are most important: availability of a spectrum of configuration options, field expandability, and field repairability. Each feature contributes to cost effectiveness; when all are present, a customer is able to start with a configuration that meets minimal needs and gradually augment the computer capability as requirements increase. Modular design of the major subassemblies can provide the minicomputer with these required features.

In its most basic form, the final system design implements a minicomputer, housed in a single cabinet, comprised of a central processing unit (requiring 5-V power), memory system (requiring 5-V and 12-V power), input/output unit (requiring 5-V power), power subsystem (supplying all dc

power and controlling signals to the other subassemblies), and ac distribution panel. Expansion cabinets containing additional memory and input/output (I/O) subassemblies can be added to upgrade this basic configuration (Fig 1).

Power Subsystem Requirements

Modular design in minicomputer power subsystems presents several challenges: (1) an overall packaging concept must be determined so that each major subassembly can be allocated sufficient cabinet space; (2) required regulation budgets to individual loads in the cabinet must be satisfied; (3) high reliability must be ensured through circuit design and component selection, (4) system power-up

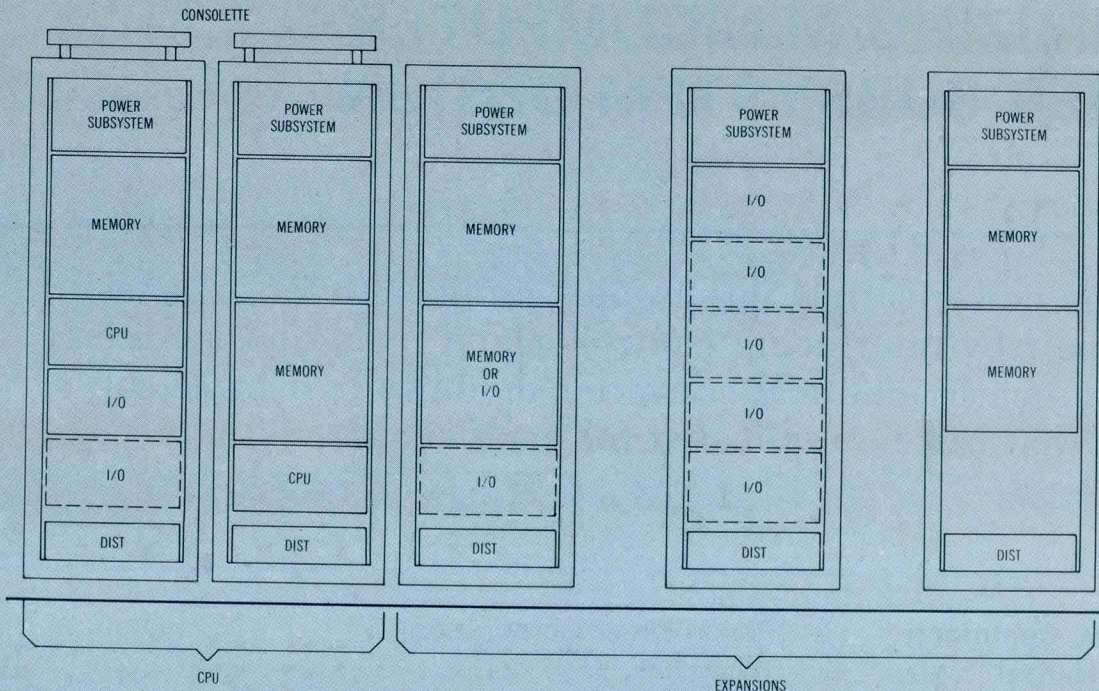


Fig 1 Typical multicabinet system. Each expansion cabinet includes power subsystem. Interfacing

signal cables link all power subsystems together, with CPU power subsystem acting as master

and power-down sequences must be controlled; (5) high noise immunity must be achieved in all power and signal circuits; (6) a unipoint cabinet and chassis grounding method must be devised; and (7) protection of metal oxide semiconductor (MOS) memory against power failure must be provided. Satisfying the requirements of Underwriters' Laboratories (UL) and other safety specifications for data processing equipment makes additional demands on power subsystem designers. The approach to each of these design problems, however, must not weaken the power subsystem link in the minicomputer subassembly chain.

Cabinet power requirements are crucial to packaging concept design. Several questions about partitioning must be answered at the outset. Is cabinet cooling (air flow) required? Is single or multiphase power required? What ac voltage range(s) should be specified? What levels of output current are needed to partition the individual modules? Also, how can the dc output current be increased when required?

Assuming a single source of dc power, power source outputs and interconnections from the power subsystem to each load must be regulated. Transistor transistor logic (TTL) and MOS memory voltage loads must be 4.75 to 5.25 and 11.4 to 12.6 V, respectively.

Circuit design and the management of components are two important reliability factors. Maximum junction temperatures, voltage and current design margins, satisfaction of minimum betas, source and sink currents, elimina-

tion of race conditions, and many other items must be emphasized. Operating modes must be well defined, their currents and voltages kept under control with no blips or uncertainties, and adequate phase margins designed into the feedback loops.

System power sequence control is tied to the reliability of the design in that all operating modes should be well defined from the power subsystem controller (PSC). Some basic considerations are defining inrush current during power turn on, starting converters in a defined state, issuing signals that indicate when all dc voltages are in regulation, issuing signals during power shutdown at levels that guarantee sufficient hold up time (this maintains regulation for the CPU to halt in an orderly manner after ac power is removed), and intercabinet communication in large configurations.

Noise immunity is always a design need. Instead of 1-V noise immunity for a multicabinet minicomputer PSC, 5.5-V immunity can be implemented by optical coupling and quad comparators using a 15-V bus, rather than TTL signals operating at 5 V. Another noise immunity factor in circuitry design requires pulses exceeding a minimum width to activate a threshold.

Unipoint grounding ties in with noise immunity and many designers avoid ground loops entirely. The overall design of each cabinet in a multicabinet situation should be geared toward optical coupling of signals. Optical coupling allows the cabinets to be daisy chained together with their

dc returns tied to earth at one point, and every subassembly isolated from the cabinetry (Fig 2).

Some minicomputer designs use MOS memory. Since this memory system is volatile, the memory content is lost when dc power is lost. Magnetic (or core) type memories, on the other hand, maintain memory elements in any state until power is restored. Although MOS memory requires battery backup power for memory retention during power loss, this does not power the entire unit. Furthermore, upon receipt of a signal indicating that prime power is being lost, memory should enter a burst refresh mode, and draw about 50% less power than normal.

Power Subsystem Design

A blower system for air flow to the CPU, memory, and I/O cards is standard design for minicomputer power subsystems. The blower is placed at the bottom of the cabinet, feeding air to the duct work along the cabinetry. Air flow deflects to move horizontally across each card and exhausts at the top of the cabinet. Ambient temperature design limit ranges from 0 to 50 °C, and air temperature at the exhaust is 65 °C. This 15 °C increase does not include heat dissipated within the power subsystem. Using commercial logic families, whose ambient temperature range is from 0 to 70 °C, the power subsystem should not preheat incoming ambient air. For this reason, major power subsystem modules are mounted at the top of the cabinet.

Modular power subsystem design utilizes a front end module (FEM), 5-V master power module at 150 A (converter), 5-V slave power module at 150 A (converter), 12-V power module at 50 A (converter), power subsystem controller (PSC), battery backup module, ac distribution box (with electromagnetic interference filter), and dc distribution system (bus bars, connectors, etc). All modules except the battery module and ac distribution box are mounted at the top of the cabinet (Fig 3). The 5- and 12-V converter modules each have a cooling fan independent of the cabinet's cooling system. The FEM and PSC module are cooled only by convection. Heat generated in the converter modules exhausts out the top and does not contribute significantly to ambient temperature at the PSC and FEM.

For fault isolation, the PSC has front panel light emitting diodes (LEDs) and three front panel maintenance switches providing 5-V margin high/low, 12-V margin high/low, and maintenance reset with LED test. Margin switches are used during troubleshooting procedures. When a cabinet exhibits errors, use of a higher or lower V_{CC} expedites isolation to a faulty card and, ultimately, to a faulty integrated circuit. When a processor or memory card has to be changed, the reset switch commands the 5- and 12-V converters to shut down their dc outputs. LED test function is a quick check to demonstrate that all LEDs are working.

Battery storage is hinged at the back of the cabinet and employs a switching regulator for battery charging. The battery box is cooled by convection only, since its internal heat dissipation is low and no other system element adds to its ambient temperature.

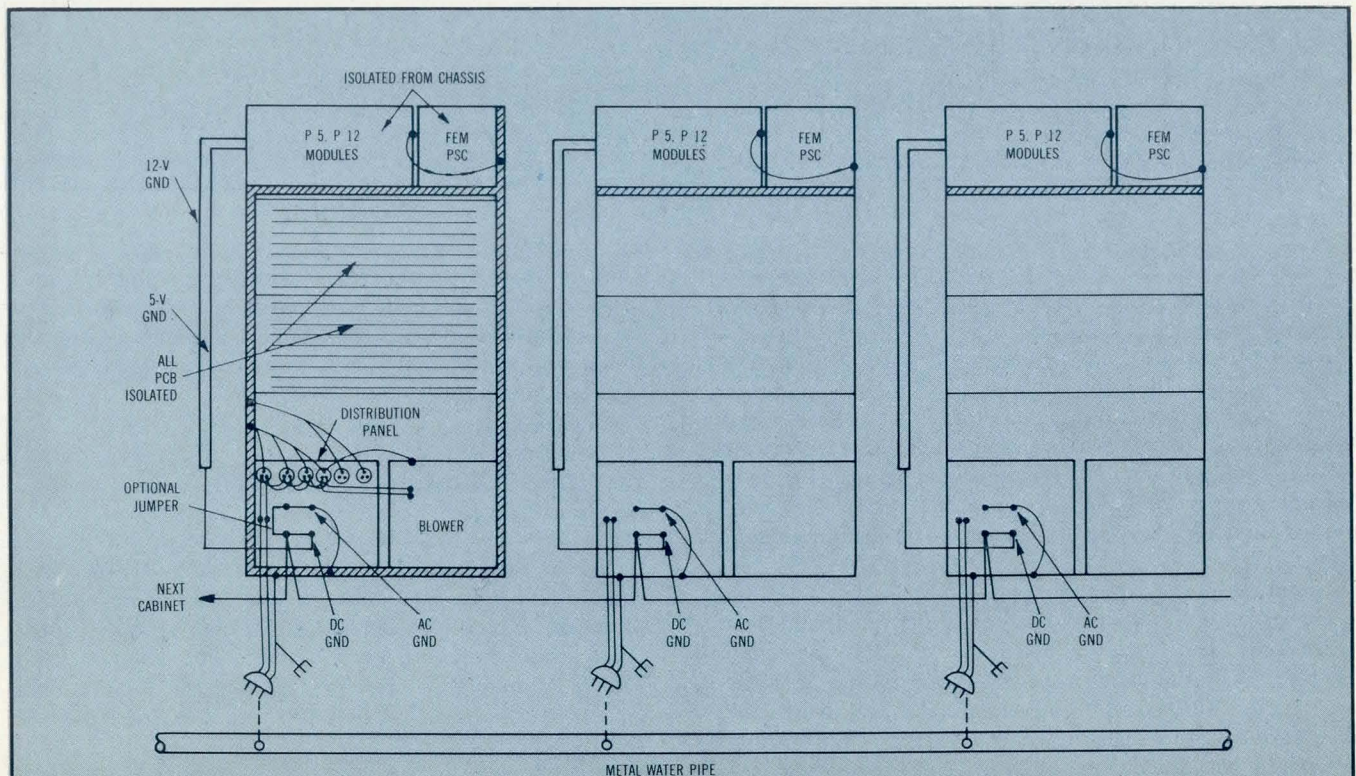


Fig 2 Noise immunity through unipoint grounding. Optically coupled signals isolate cabinets; dc

returns tie in to earth at one point to avoid ground loops

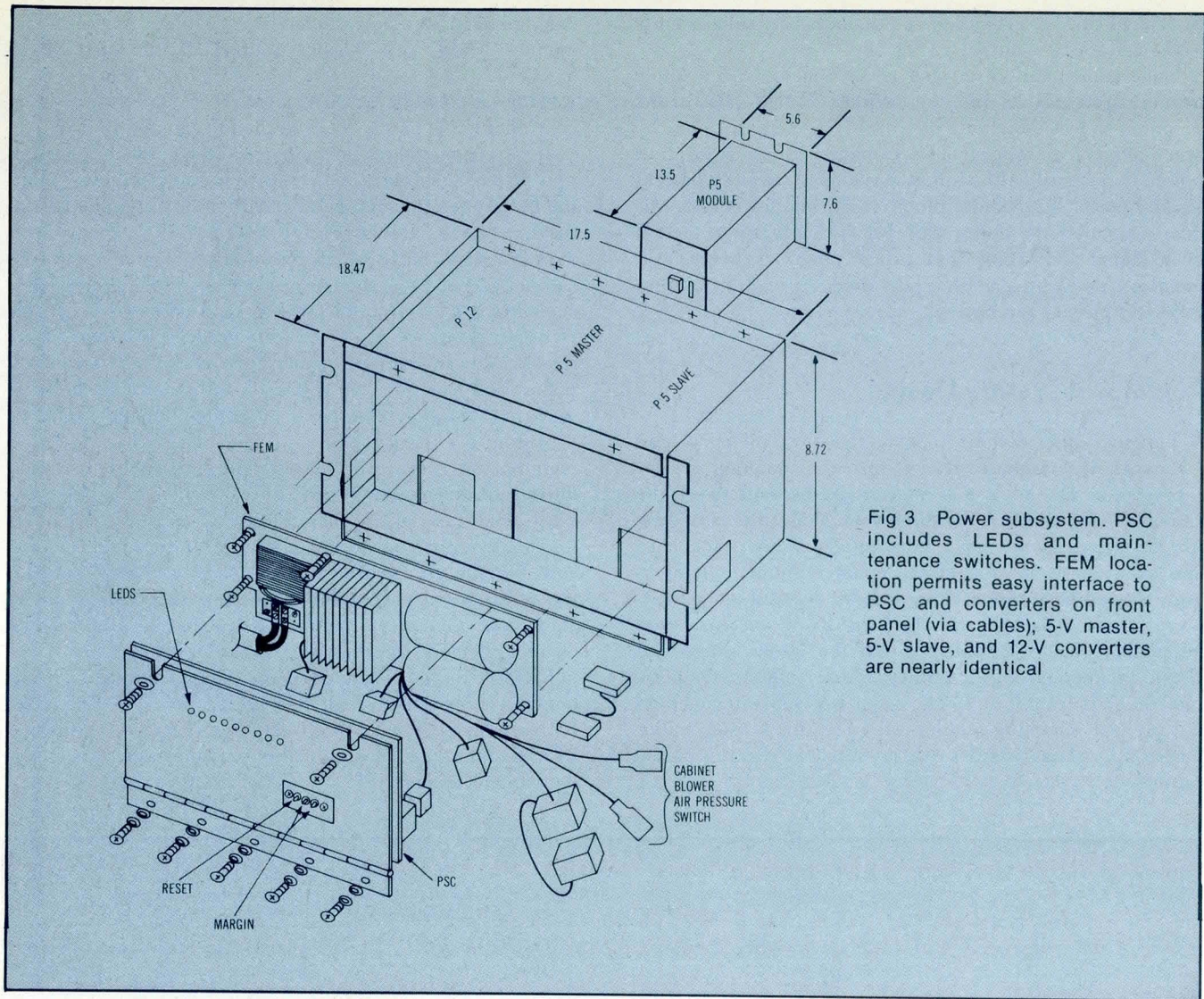


Fig 3 Power subsystem. PSC includes LEDs and maintenance switches. FEM location permits easy interface to PSC and converters on front panel (via cables); 5-V master, 5-V slave, and 12-V converters are nearly identical

The ac distribution box, at the bottom of the cabinet, contains the system electromagnetic interference (emi) filter. A shielded line cord delivers ac power to the power subsystem components at the top of the cabinet, protecting other subassemblies within the cabinet from line cord radiation.

From the converter outputs, a short length of #2 AWG wire goes to the copper bus bars, where bullet connectors pick off the high current for each card. Each processor card is allocated up to 20 A of 5-V power. Memory cards receive both 5- and 12-V power, but the total is still a maximum of 100 W.

Input (ac power from a single- or 2-phase source) ranges from 180 to 264 V rms (assuming no distortion) and is applied to the ac distribution box at the bottom of the cabinet (Fig 4). This input capability is necessary for use in Europe where single phase 230 V rms is nominal. UL requires a 20% line current safety margin, which is satisfied by allowing a maximum rms line current of 24 A. This also permits use of readily available 30-A hardware.

Convenience receptacles for field service personnel, the circuit breaker, and the line filter are in the distribution box. Throwing the circuit breaker off opens both sides of the ac line and disconnects the negative side of the battery

pack. This is the only way to remove all power from a cabinet, since pulling the plug leaves dc power available for the MOS memory. The ac exits the distribution box and goes to the power subsystem FEM at the top of the cabinet via the shielded line cord.

Front End Module

With associated filter capacitors, the FEM provides offline rectification, ac inrush current control, and bias power generation for other modules. Inrush current control uses a solid state relay in parallel with a resistance; the PSC signals the relay to short out the resistance. The filter capacitor voltage is monitored continuously, and the relay is energized 700 ms after it reaches $180 \times \sqrt{2}$ or 254 Vdc. This 700-ms delay eliminates the secondary surge.

Converter Modules

Three converter modules, 12-V, 5-V master, and 5-V slave, were designed to be as identical as possible yet independent

of each other. Each converter has its own power cable from the front end, local high voltage filter capacitor, and input fuse. Pulse width modulation at 20 kHz with a full bridge inverter operates from 175 to 370 Vdc. Using identical printed circuit boards (PCBs), the converters differ only in assembly drawing and cable variations. Design features include the SG3524 chip, high temperature Schottky diodes, stacked foil capacitor, flux reset in the base drive, precision voltage reference, zero duty cycle turn on, and optically coupled control signals. The 12-V converter uses fast recovery, low loss output rectifiers, and a low equivalent series resistance output capacitor. Thermostatic sensors in the rectifier heat sinks shut off overheated converters.

A current sharing, paralleling technique fulfills the 5-V, 300-A current requirement, as shown in Fig 5. Each converter's overcurrent limit point is set to account for current sharing imbalance. Oscillators in the master and slave 5-V converters are synchronized to maintain the same output ripple as in the case of one 5-V converter only. When no synchronization is employed, ripple doubles in amplitude and contains a low frequency component (about 2 kHz).

Various circuit techniques control and protect the power section; among these are dead band circuit, 3-piece snubbers and clamp diodes (for power transistors), power rectifier snubbers, and separation of the reference for voltage regulation from the overvoltage and undervoltage functions. When it hits the overcurrent threshold, the converter output shuts down in 40 μ s. Overcurrent conditions such as processor or memory board solder splashes and misapplication of metering probes commonly occur during development and production testing, and require a fast shutdown to prevent board loss.

Power Subsystem Controller

The PSC uses the LM339 quad comparator (the active circuit element) and a regulated 15-V rail. Voltage threshold detectors use precision 10-V references and discrete, precision resistor dividers in conjunction with the comparator. This combination of circuitry yields tight tolerance voltage threshold detectors which do not require trimming. Input switch-sensing filters out bounce by means of resistance-capacitance networks operating into comparator stages. When the internal logic circuitry implements additional discretely with the comparator stages to form a family of logic, the following design goals are satisfied: (1) 5-V minimum noise margin (operating from a nominal 15-Vdc supply voltage), (2) level sensitive (rather than edge sensitive) sequential logic gates, (3) low power consumption (quiescent load current for the comparator is 4 mA), and (4) wide operating voltage range for the PSC (PSC maintains control over a line range of 75 to 264 V rms; up to 75 V rms, the converters hold themselves off).

In the output circuitry, comparator stages connect either directly or through transistors to other system elements within a single cabinet. Switched, 3-terminal regulators with integral current limit protection drive the signals transmitted between cabinets. On the receiving end of the inter-cabinet communications link are optically coupled LED transistors with an isolated ground return line to the transmitting source.

Monitoring the high voltage capacitors, the PSC allows 700-ms time for continued capacitor charging from the point at which 250 Vdc is reached, T_0 (see Fig 6). This prevents a secondary current surge when the solid state

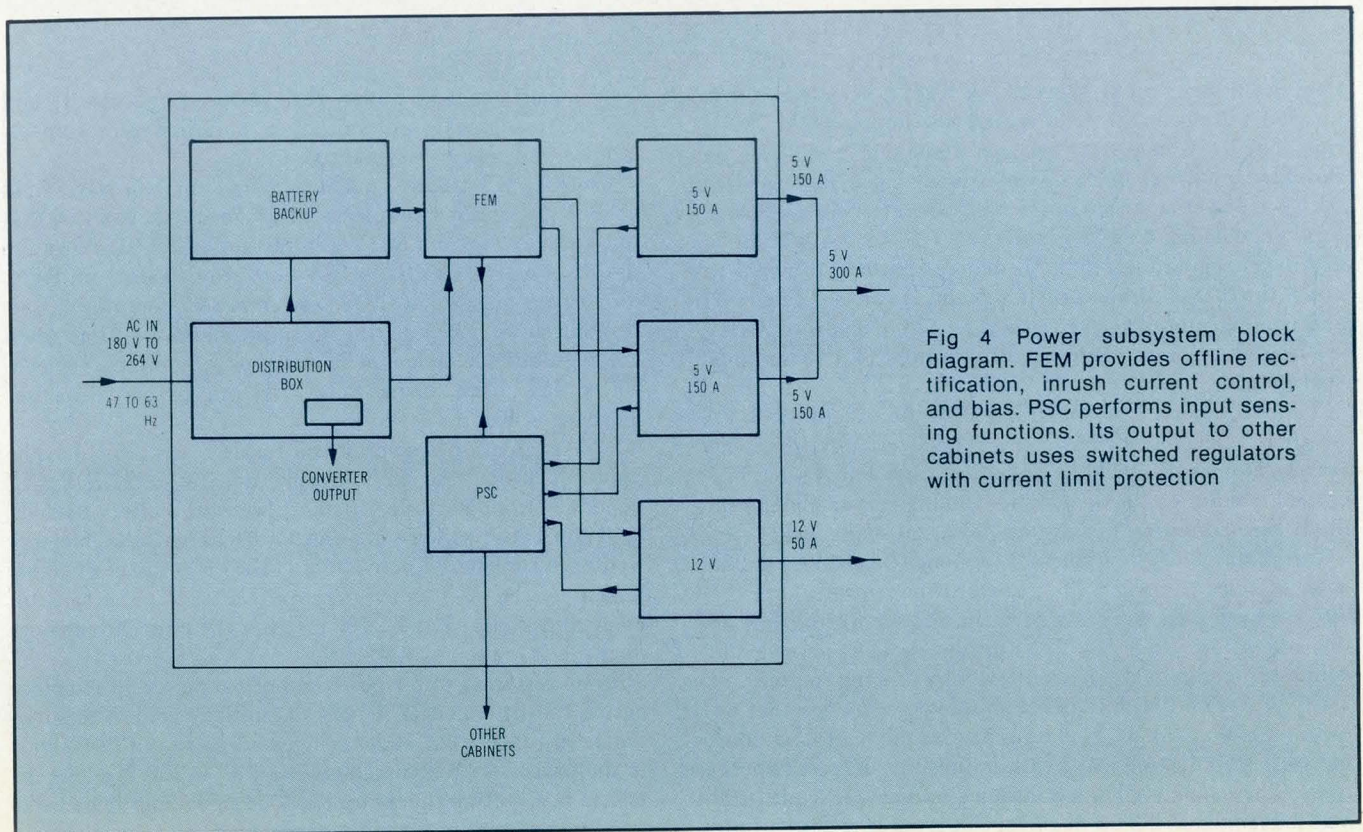


Fig 4 Power subsystem block diagram. FEM provides offline rectification, inrush current control, and bias. PSC performs input sensing functions. Its output to other cabinets uses switched regulators with current limit protection

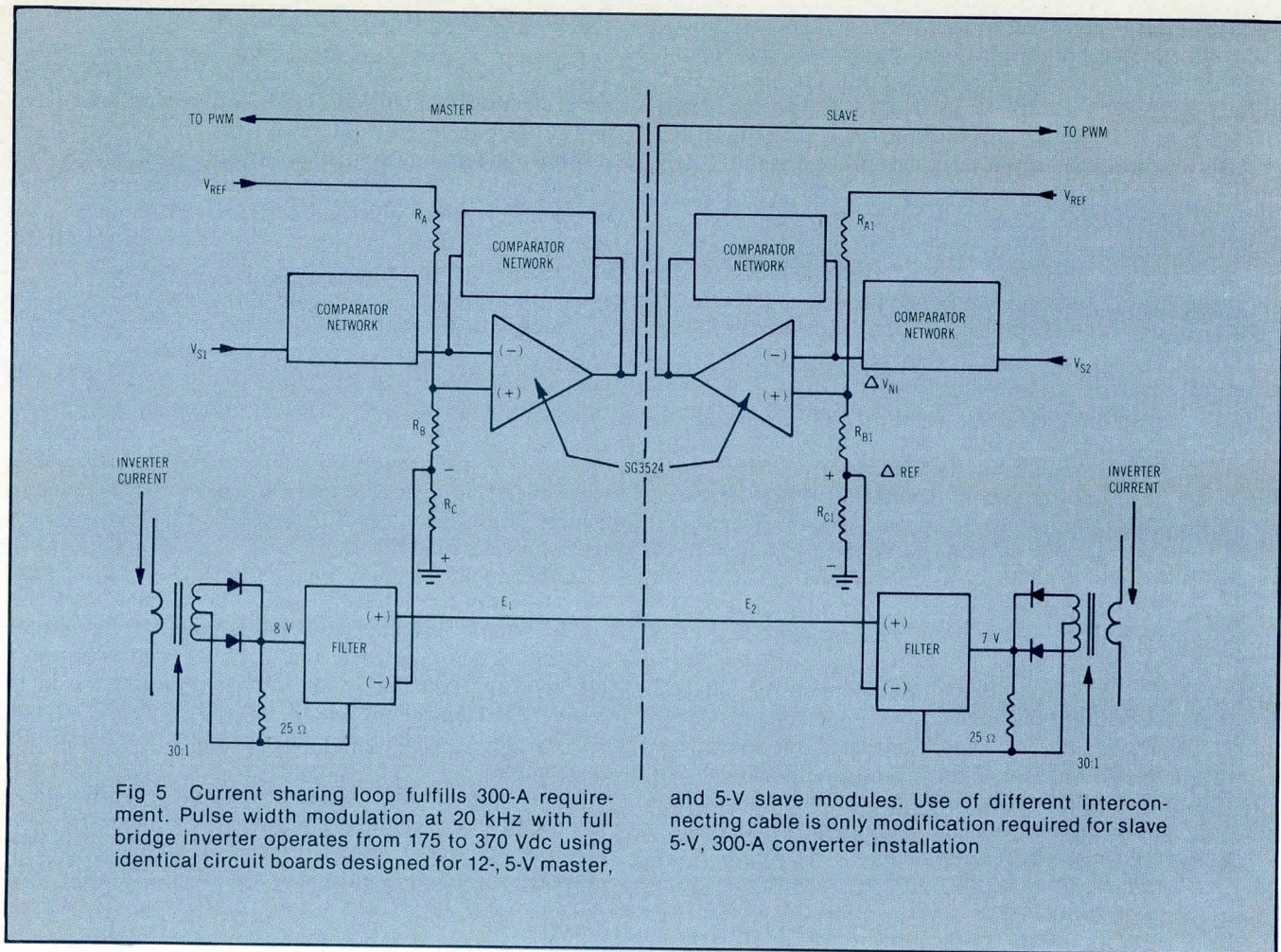


Fig 5 Current sharing loop fulfills 300-A requirement. Pulse width modulation at 20 kHz with full bridge inverter operates from 175 to 370 Vdc using identical circuit boards designed for 12-, 5-V master,

and 5-V slave modules. Use of different interconnecting cable is only modification required for slave 5-V, 300-A converter installation

relay (SSR) turns on at T_1 . A 250-V level is selected so that turn on will occur at the specified low line value of 180 V rms. The 12-V converter receives its signal and starts its slow turn on 500 ms after the relay is set. Then, 300 ms after the 12-V power is turned on, the 5-V converters receive their turn on command (T_4). Finally, at T_5 , the 5-V output is within its regulation band. T_6 denotes an output signal to notify the CPU that the cabinet is ready. Ac power, dc power, and cooling are all operational. The CPU acknowledges by sending a systems clear to all cabinets (T_7), beginning operation.

Times are somewhat arbitrary, with the exception of T_1 , which is selected to charge the capacitors fully when the system is energized at the specified high line value. The crosshatched area for the cabinet cooling sensor indicates a don't care condition during the power-on sequence.

Initiation of a system turn off sequence takes place at 220 Vdc, as shown in Fig 7 (T_0). For brownout protection, the 30-Vdc hysteresis prevents turn on chatter during low ac line operation. Once the 220-Vdc threshold is passed, the computer commits to a shutdown by issuing power not ready (T_1). The CPU initiates a shutdown sequence that requires less than 3.2 ms hold up time. Systems clear, a changing state, is indicated at T_2 ; this defines the end of all operations. The capacitor bank continues to discharge until 190 Vdc is reached at T_3 , when a decision is made to shut off the

5-V converters. If ac power were restored between T_0 and T_3 , the machine would initiate a modified power-up sequence and resume normal operation.

From T_3 to T_4 there is a 4.5-ms delay, which provides hold up time for another requirement, ie, for the key switch that turns the CPU on and off. When the key switch signal enters the PSC, the PSC signals the 5-V converter to turn off. Here, too, 3.2 ms must be available for an orderly shutdown. Corresponding to 175 Vdc, the T_5 point marks the time when 5-V regulation is no longer required or guaranteed; the converter has been turned off, and its output capacitor discharges into the load.

12-V regulation is guaranteed until T_6 , or 170 Vdc. The point at which the 12-V supply decays to 11.2 V (T_7) depends on memory size. If there were no battery backup, or if the batteries were allowed to discharge fully, memory would be considered nonvalid at 11.2 V. No turn off signal is sent to the 12-V converters until after T_7 ; the turn off command is issued at T_8 , 100 ms after the nonvalid memory decision is made at 11.2 V.

Upon restoring prime power, a normal power-up sequence occurs during which 12-V power is initially zero. A monitoring circuit in the PSC issues a nonvalid memory (NVM) signal to the processor. When systems clear (T_7 in Fig 7) allows the CPU to run, software picks up the NVM signal and reloads the operating system into main memory from disc.

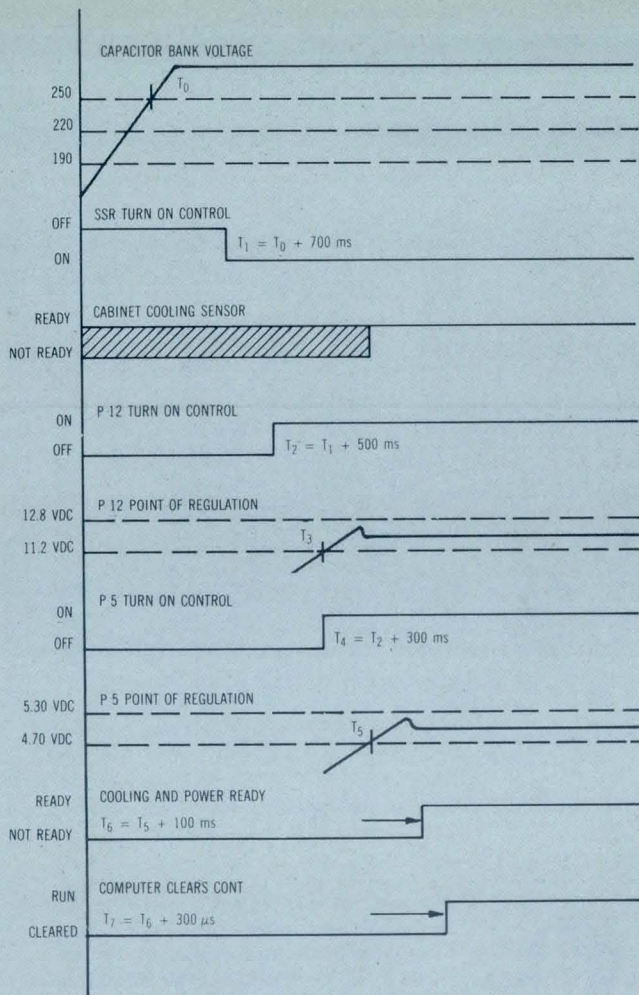


Fig 6 Power-on sequence. SSR turns on 700 ms after capacitors reach 250 V. 12-V converter turns on 500 ms later. 5-V converters turn on once 12-V power is within regulation

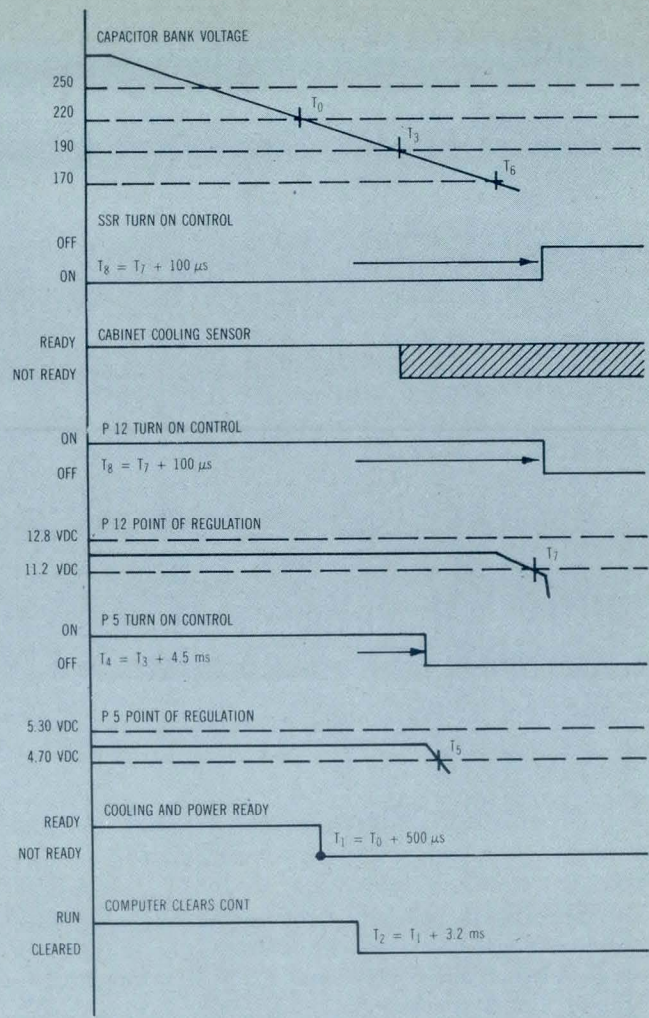


Fig 7 Power-off sequence. Crossing 220-V threshold commits to shutdown, but modified power-up can be used until 5-V converters turn off at 190 V. 12-V regulation is maintained until 170 V

Battery Backup Module

Low risk in transferring from ac to dc power and back again provided the basis for the battery backup approach. The sealed, lead-acid pack is nominally at 180 V. Its charger draws power from the high voltage bus. An isolated inverter supplies charger bias power from the 12-V output (Fig 8). Charging (0.25-A current) begins at 207 Vdc and cuts off at 220 Vdc. When the bus decays below the battery voltage, CR1 is forward biased and sources the 12-V converter; the PSC and the converter fan draw power from the battery backup. Battery voltage drops to about 187 Vdc as it initially supplies the 12-V converter. Drain continues until the output falls to 11.2 Vdc, causing the converter to turn off.

The inverter stage transformer has an extra winding whose secondary voltage is rectified, filtered, and supplied to the PSC. When prime power goes down a step, the converter is still running and supplies required bias to the PSC and itself. The PSC receives bias power from either the 5- or the 12-V converter. For example, when a cabinet contains only 5-V output, as an I/O cabinet, the 5-V inverter stage feeds the bias power.

Battery hold up time depends on the amount of memory in each cabinet and varies from 20 min (for 8M bytes) to 82 min (for 0.25M bytes). Several battery backup methods other than the one just described are possible. One method uses a lower voltage battery with a converter boosting the voltage to 215 Vdc. This has the disadvantages of needing an additional converter and offering lower conversion efficiency because the battery has to feed two converters in cascade. Another low voltage method uses a battery with an additional regulator whose output is tied to the 12-V regulation band. The disadvantages here include higher current battery charger and additional high power 12-V regulator.

Safety

Handling the 180-V battery is a major safety concern. Batteries are handled in groups of 18- and 36-V until final assembly. After the two 18-V packs are put in series, connecting the five 36-V units is possible only by closing the battery compartment. Also a protection for service

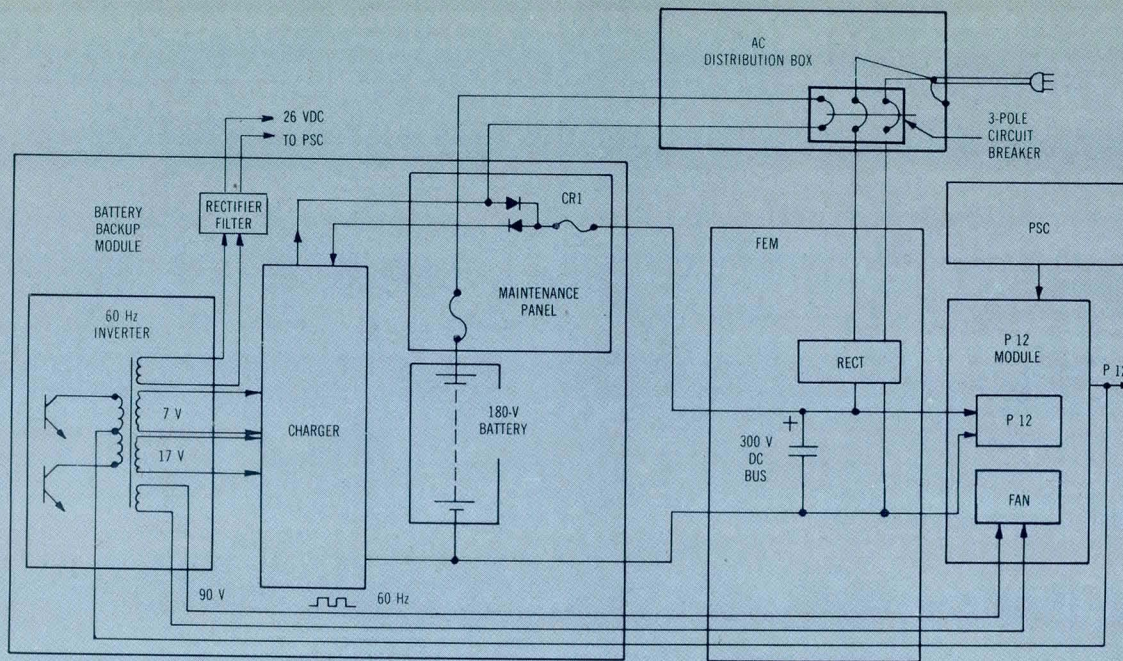


Fig 8 Battery backup module block diagram. Charger draws 0.25 A from high voltage bus above

212 V. Below 212 V, CR1 sources 12-V converter until 11.2-V threshold is reached and converter shuts off

personnel is the warning light on the side panel of the printed circuit board, which indicates when voltage is present. A switch allows individual, external testing of each of the ten battery packs.

Certain safety considerations are required apart from any that might be self-imposed. One example is the overall cabinet leakage limitation of 5.0 mA at nominal line voltage. A 100%, high voltage test is a required purchase specification for all frontend components such as transformers, bridge rectifiers, relays, and emi filters; each component receives a portion of the leakage budget. This voltage test is performed at both subassembly and final assembly levels.



Ermand Centofanti, currently a design engineer at Perkin-Elmer Computer Systems Division, has been involved in design of minicomputer power systems for the past six years. Prior to that, his work experience included core memory circuit design, logic design, and power supply design. He holds an associate's degree from Temple University.



Allen Hansel received his BS at Long Island University, and completed requirements for his MSEE at Fairleigh Dickinson. A design engineer at Perkin-Elmer Computer Systems Division, he has been involved in high power converter design for 10 years and has been actively working in the area of minicomputer power system controls since 1977.



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Thiagarajan Natarajan is a design engineer at Perkin-Elmer Computer Systems Division. He holds a BS, an MS, and a PhD degree in electrical engineering. He has been involved in calculator and minicomputer power system design since 1974. Prior to that, his work experience included research and teaching on analog computers, control theory, and optimization theory.

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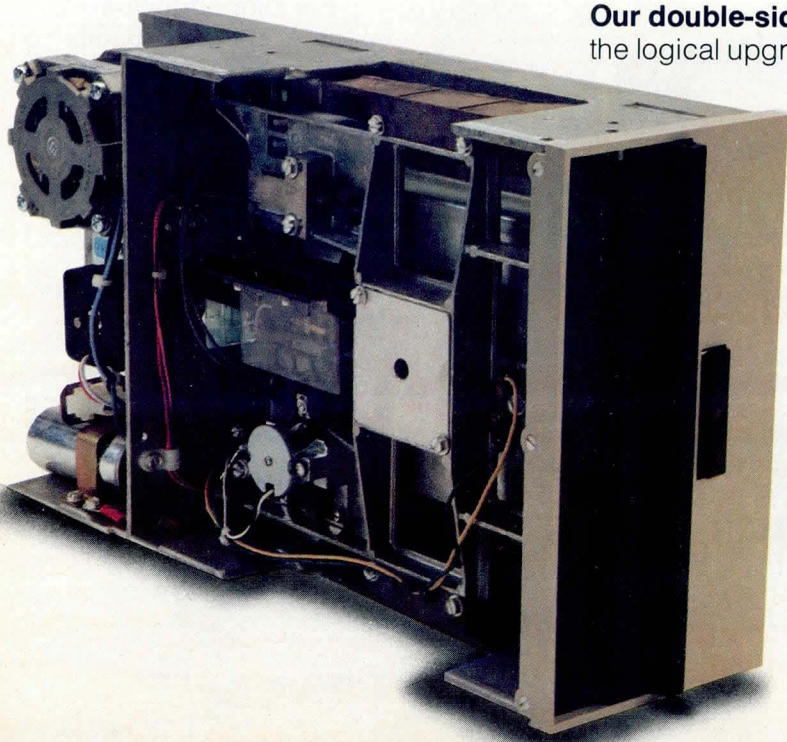
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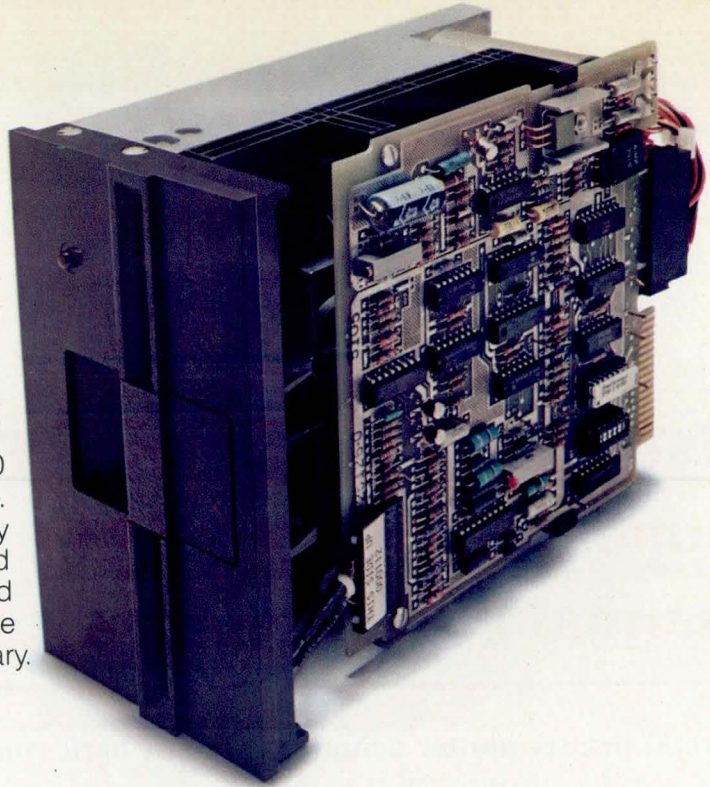
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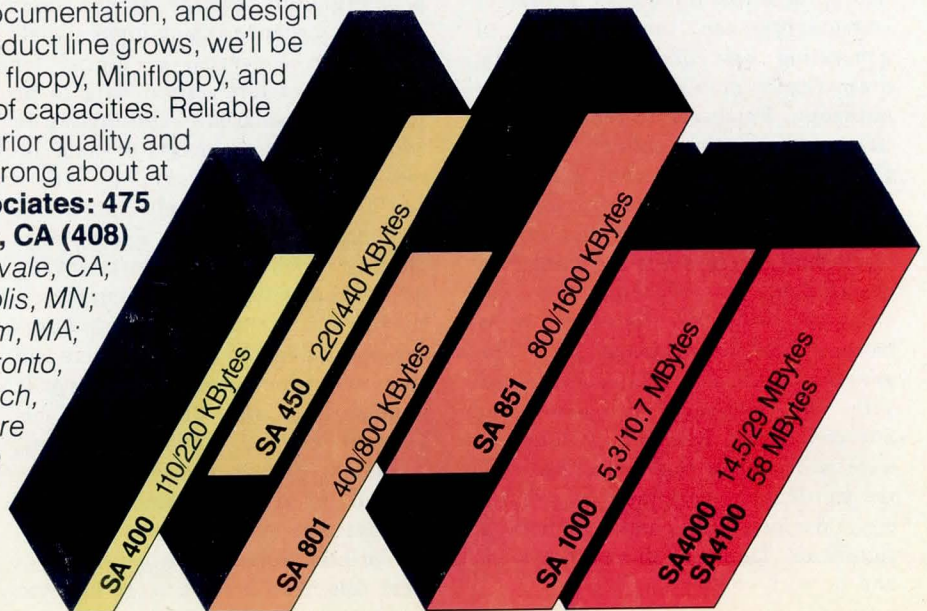
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Mixed Format Operation Enables Economical Output From Thermal Printer/Plotter

Thermal printer/plotter achieves low cost hard copy by mixing character and graphical data without burdening the host system with lengthy software driver requirements

Harold D. Schofield

Gulton Industries Incorporated

Gulton Industrial Park, East Greenwich, RI 02818

Due to the widespread use of microprocessors, intelligent laboratory instruments are now capable of generating vast quantities of data, dramatically increasing demands for hardcopy. Furthermore, computerization is eliminating manual intervention by automating decision making as a function of data analysis, making realtime chart recordings and similar input data displays less essential than descriptions or representations of analyzed results in the form of a listing, chart, or graphical plot. The growing volume of data, combined with the emphasis on displaying analyzed results derived from data that were collected in real time, increases the burden on instrumentation hardcopy devices, thus making them a significant factor in the total system and its cost.

Of the hardcopy devices, digital printer/plotters emerge as the most desirable because analog input signals have been converted to digital for analysis, therefore output data to be printed or displayed is also digital. In addition, as the amount of data increases, so does the need to extract and display critical results and trends in pictorial form; hence, the graphics plotting capability of the printer/plotter becomes especially important. Historically, the use of printer/plotters has been limited to minicomputers and large mainframe computers, primarily because most were designed for this segment of the industry. Lengthy, tabulated, printer listings were supplanted by printer/plotter graphics displays wherever possible. However, the printer/plotters that emerged to meet this need are too large and too

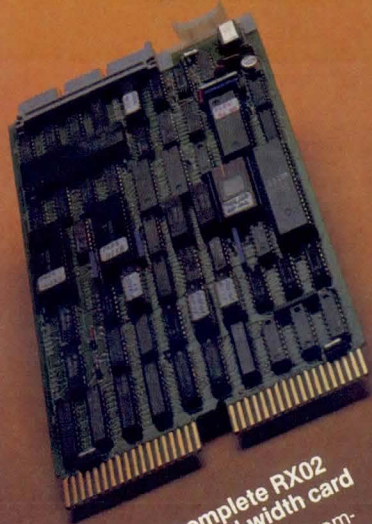
expensive to fulfill the needs of instrumentation and other microcomputer applications.

The three classic types of printer/plotters currently available are electrostatic, flat bed, and drum units. All offer higher performance than is necessary for microprocessor based instrumentation applications in terms of speed and resolution. More importantly, they require sizable software drivers, programs that interface the output unit with the operating system to supply page or plot output on a line or a vector basis.

The Thermal Printing Alternative

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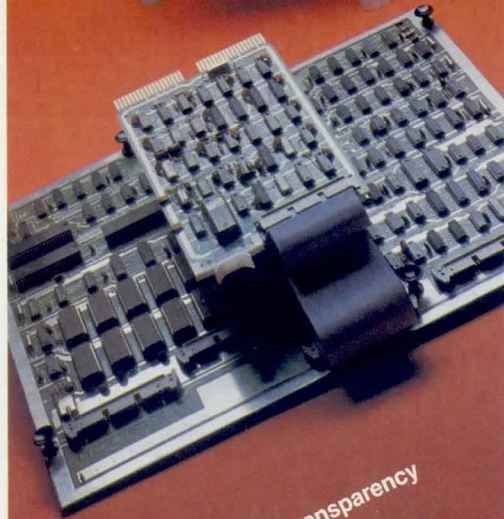
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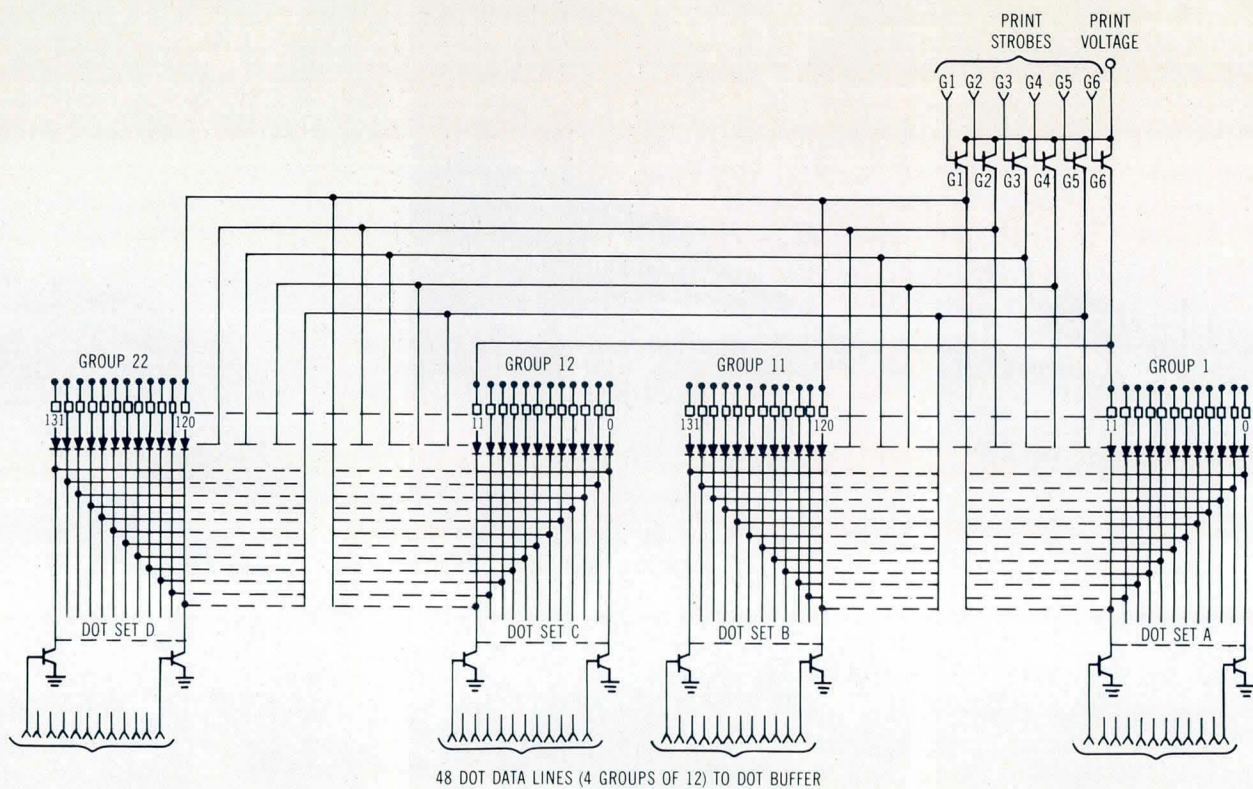


Fig 1 Multiplexed printhead. Diodes multiplex printhead in 22 12-dot groups, allowing hardware dedication of character columns

to simplify software addressing requirements. Each group of dots may contain two X axis columns or one Y axis line

Quiet operation, reliability, straightforward digital interface, and attainable high speed characterize the thermal printing technology. It does not present inductive loads, such as the solenoids required to drive needle matrix devices, or the design problems of wheels, hammers, high voltages, or radio frequency interference. Complementing use of integrated circuits and large scale integration devices, the thermal printer/plotter offers an entirely electronic means of printing that reduces the number of moving parts to only one per mechanism.

The MICROPLOT-44, a 5" (12.7-cm) unit designed especially for instrumentation and microcomputer applications, illustrates thermal printing technology. Its stationary printhead implements a 4.6-in (11.7-cm) wide linear array of dots spaced 0.017 in (0.432 mm) apart. For plotting, 256 uniquely addressable, contiguous dots provide 8-bit resolution compatible with most of the microprocessor applications. Character printing uses all 264 dots in 44 X axis columns of a 5 x 7 dot matrix

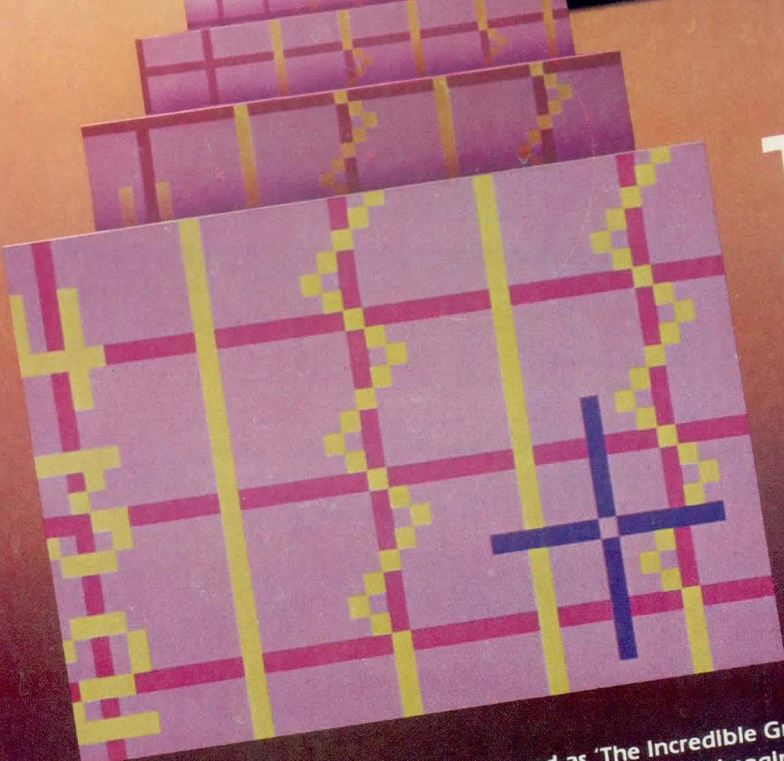
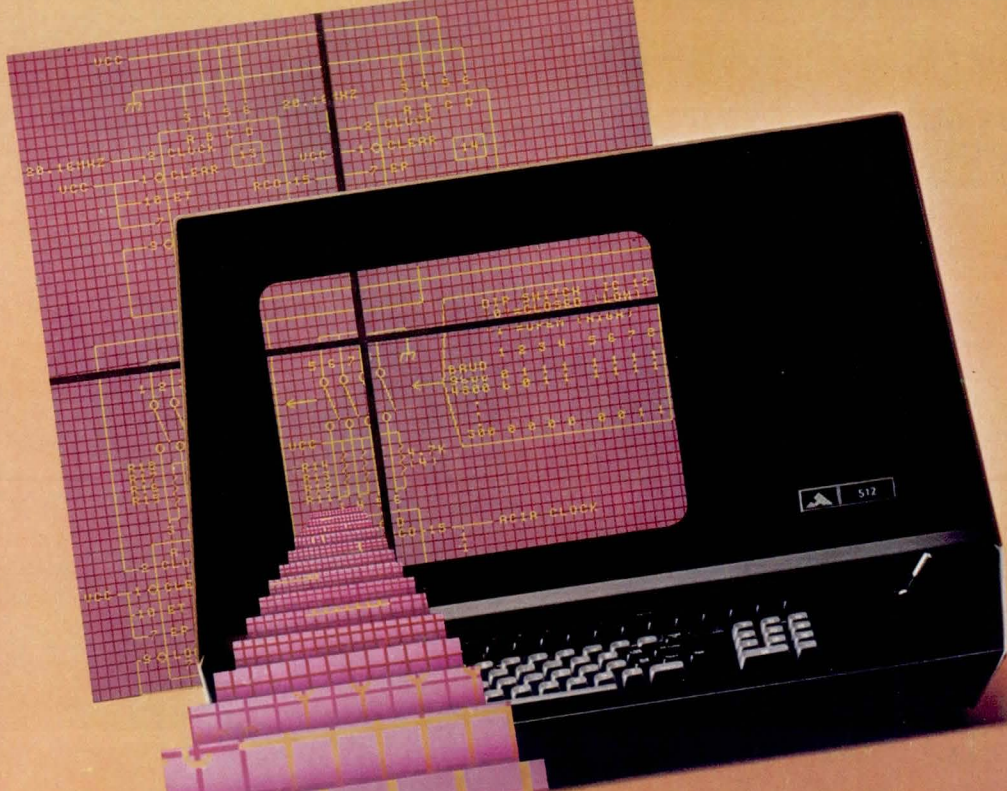
with one dot space between columns (Fig 1). Using an 8 x 6 dot matrix, the Y axis provides 22 lines of characters with a 4-dot space between lines.

For the graphics interface, the ability to address each dot uniquely in a single-byte transfer, complements the fixed printhead design, whereby all dots are in continuous paper contact. Plot data can then enter the buffer on a random access basis. Unlike moving head designs, this approach eliminates any need for sequential loading of data that increases in magnitude across the chart or for loading blank data bytes to space across the chart. In addition, the two enhanced plotting modes eliminate the lengthy data transfers that can occur when printing a horizontal vector consisting of many dots. The line segment plotting automatically fills in all of the dots between two designated endpoints on a horizontal vector and allows many such vectors on a single horizontal line, with overlap. The shaded plotting fills in all of the dots between the leftmost dot and a designated horizontal vector endpoint.

Character Data

Four combinations of the format and print commands make possible four character types from the two basic X and Y axis fonts. The normal print formats produce standard 5 x 7 dot matrix characters on the X axis and 8 x 6 characters on the Y axis, while the enhanced print formats generate double height, 5 x 14 dot matrix characters on the X axis and double width, 8 x 12 characters on the Y axis.

A byte level handshake between data available (\overline{DAV}) and data accepted (DAC) signals controls parallel data flow into the unit (Fig 2). \overline{DAV} flags a new word valid on the data bus; then the state of the format control (FMTCTL) line designates either an internal data request bit (if high) or a control word request bit (if low). These are sampled regularly at a priority that depends on the selected mode. Once a valid \overline{DAV} has been established, DAC is pulled low until the data are read into the system buffer. DAC then returns high, to the idle state, to indicate data acceptance.



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Each full line of dot or character data entered in this manner is followed by a print command and an optional paper motion command.

Plot Data

The BUSY line, activated when a print cycle has been initiated, may be sensed by the host computer to interrupt data flow during printing, providing a character line level or dot line level handshake with LDATA that can be used to reset LDATA when printing begins. LDATA is itself a qualifier that may be held low to prevent acceptance of unwanted data during idle periods or tied high for applications that do not need this function. Once set, BUSY remains high for the duration of a print cycle. When only plot data are present, the cycle will end and BUSY will be reset after one line of dots has been printed. With character data present, BUSY remains high until all character dot lines have been printed. However, plot data to be intermixed with characters can be entered during

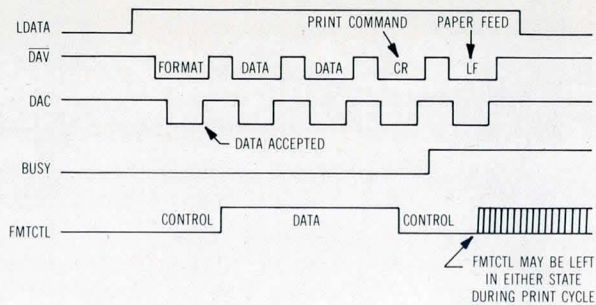


Fig 2 Byte transfer timing diagram. Byte level handshaking arrangement using DAV and DAC controls parallel data flow. LDATA qualifier provides line level handshake that can prevent acceptance of unwanted data. Once set, BUSY remains high for duration of print cycle—one line of dots if plotting 7 or 14 lines if printing characters. FMTCTL distinguishes between format and data requests

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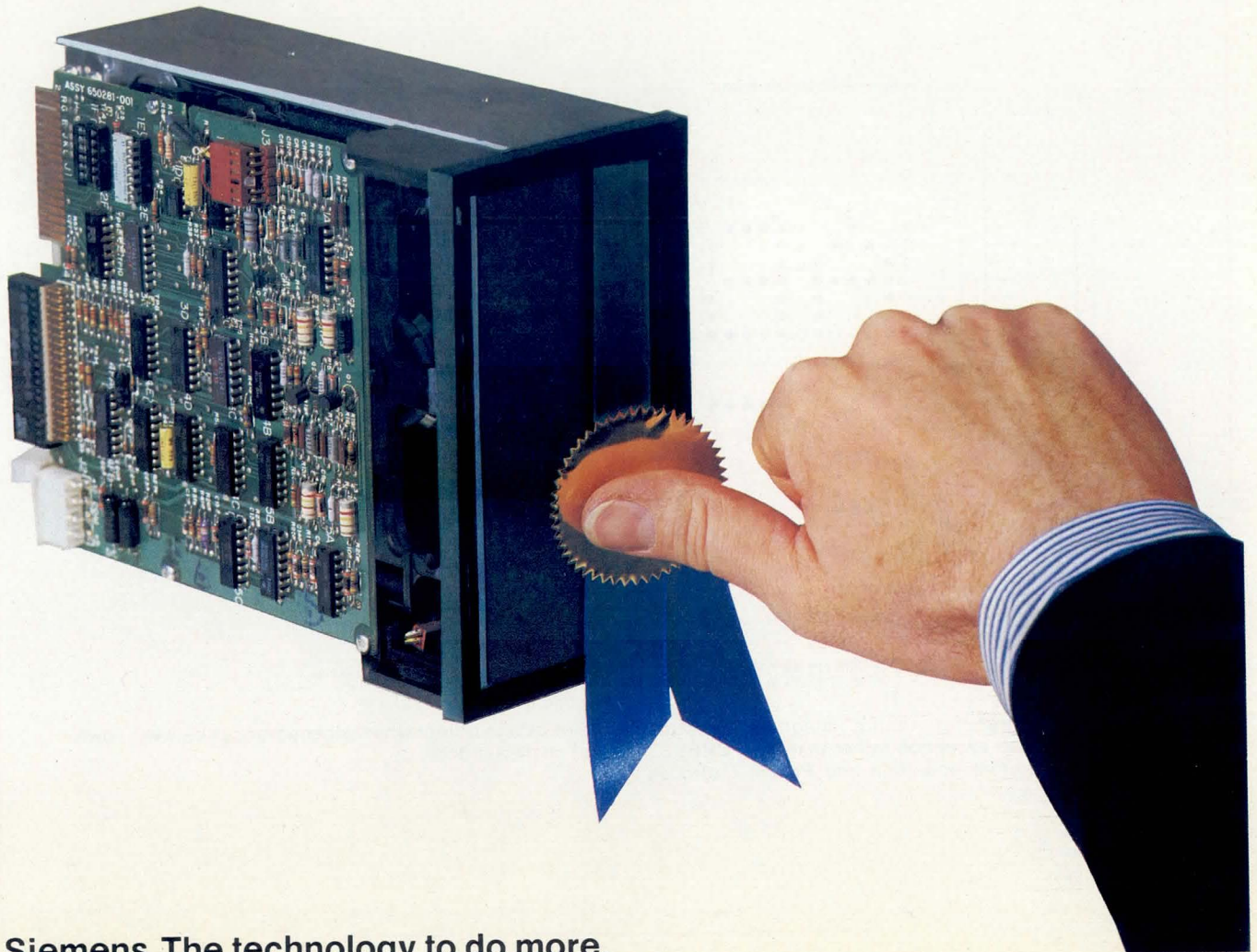
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CIRCLE 83 ON INQUIRY CARD

a character print cycle for mixed format operation. In this case, as shown in Fig 3, the presence of BUSY during a paper advance drives a plot data only (PDONLY) signal active high for the duration of the paper advance to strobe plot data transfers within paper advance periods.

Mixed Format Operation

The PDONLY strobe during each paper advance achieves the potential for mixed format operation, which is most useful for chart annotations as it intersperses line by line plot data with annotation character data. For most straight plotting applications, such as Y(t) plots, plot data transfers occur much more frequently than character transfers. Character printing is the ex-

ception. A character busy (CHBUSY) line senses this exception and notifies the host system to shift into mixed format mode whenever character printing occurs.

Once a character print cycle has been detected, output continues by detecting successive PDONLY pulses during the character cycle and interlacing new plot data on each character cycle dot line. PDONLY data windows accept plot data only; a valid plot format must be detected by each pulse before data transfer may proceed. Character printing is then slaved to plot data transfers, and CHBUSY is reset to flag the end of mixed format operation, avoiding the sampling for PDONLY beyond the final pulse of the sequence. To further reduce software

overhead, four switches allow manual format selection, using the same protocol as the software commands to manually choose the most suitable format without sacrificing full device capability.

Hardware Implementation

Programmable Interface Adapters (PIAs) are included in the 6802 circuitry—one to interface with the print-head and stepper motor circuitry and one to provide input/output (I/O) for the graphics interface (Fig 4). The I/O PIA devotes port B to the data bus. Port A's first four bits are driven by the format switches, the fifth line providing the CHBUSY output. The three most significant lines, corresponding to

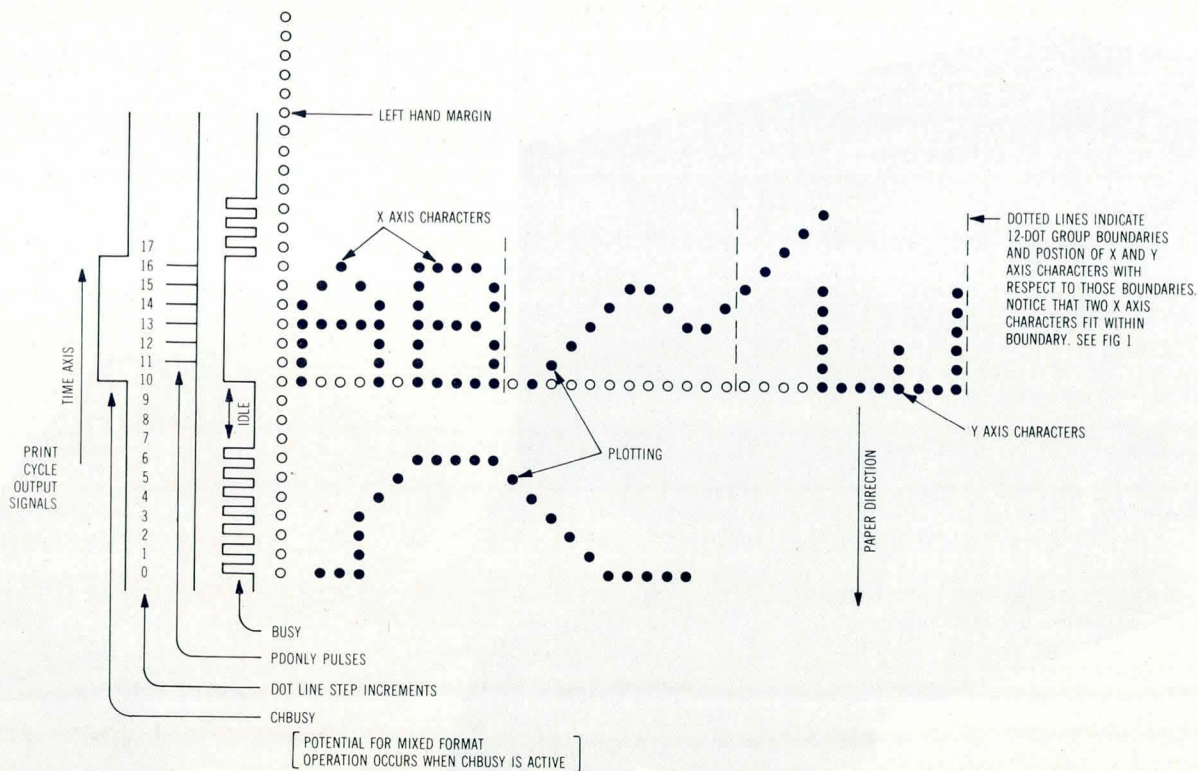
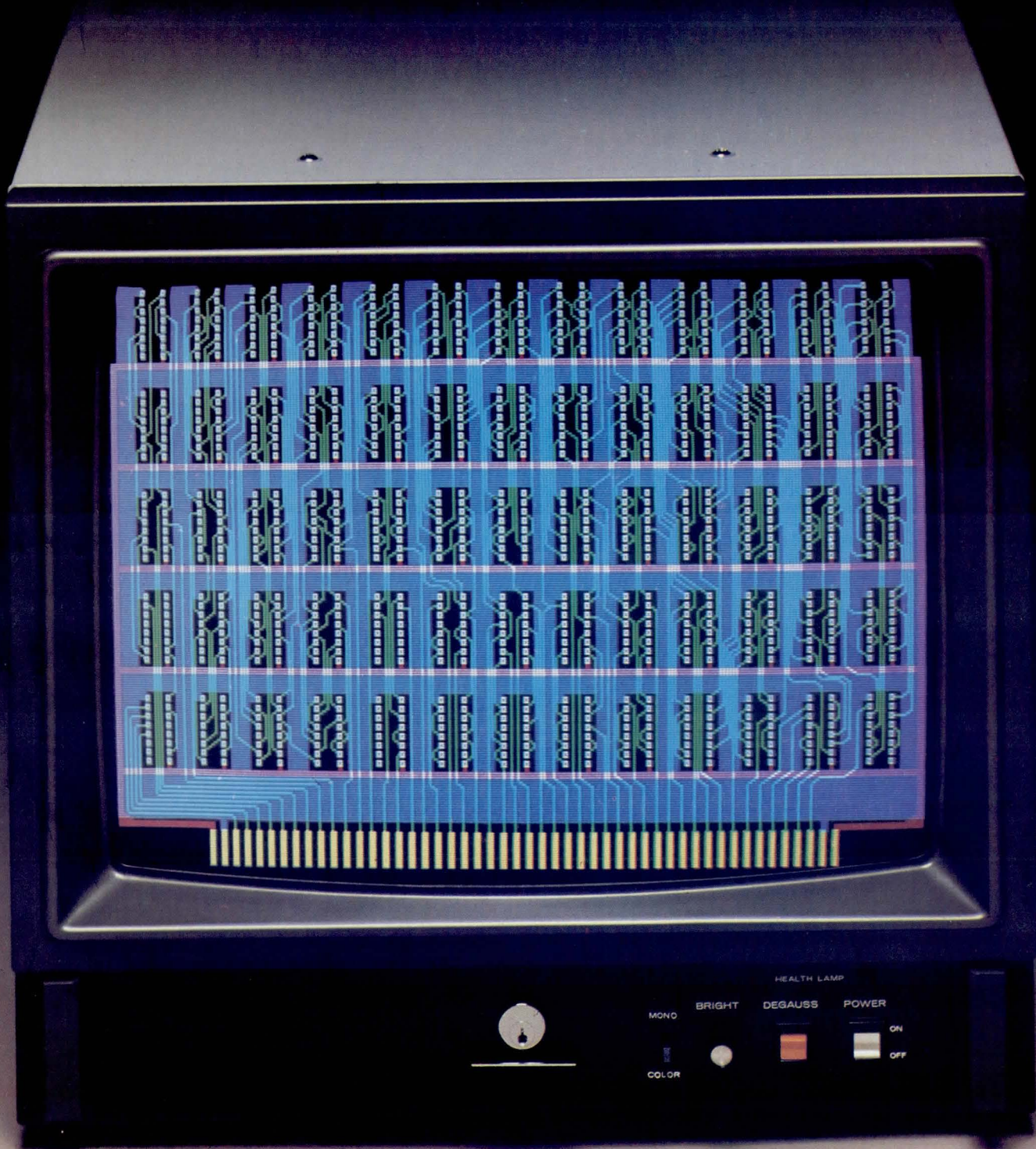


Fig 3 Line transfer timing diagram. Treating character data as exception rather than rule, CHBUSY flags mixed format operation and PDONLY strobes

plot data to printer while paper advances between rows of character dots



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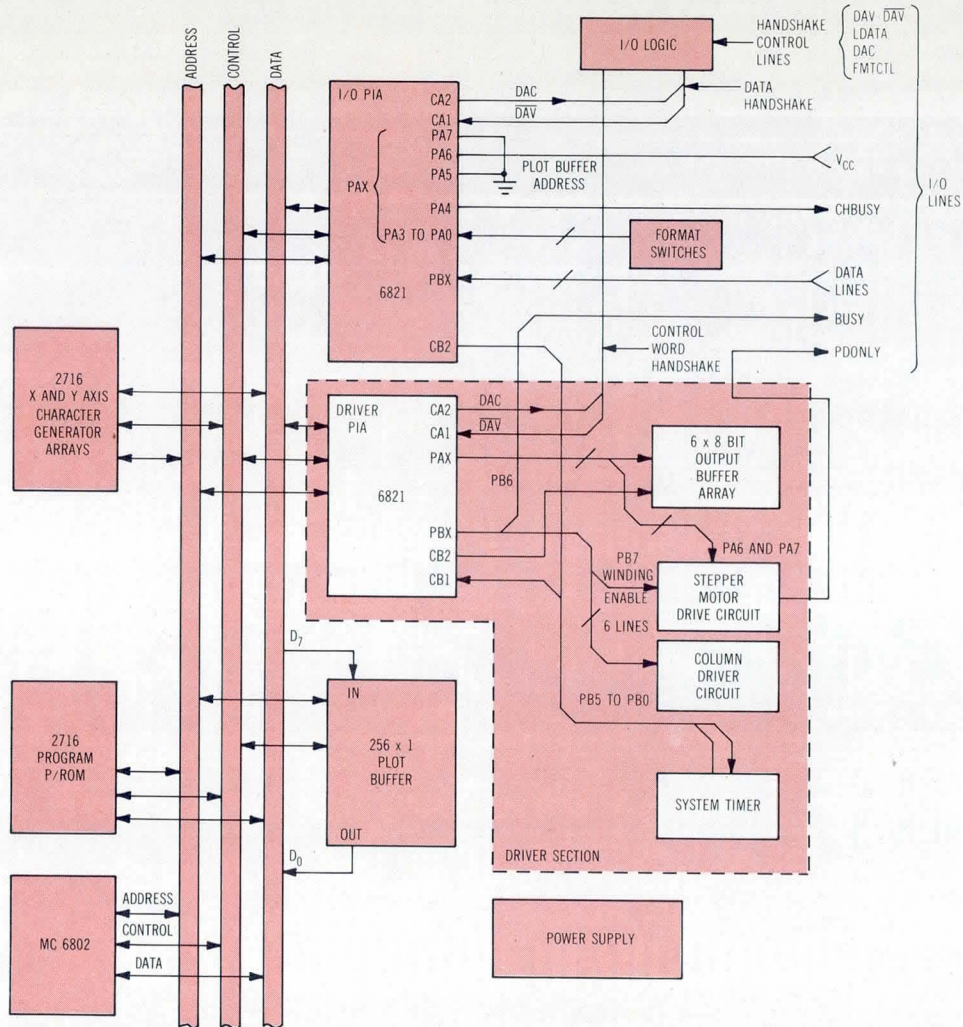


Fig 4 Printer/plotter block diagram. Two PIAs connect with printhead, stepper motor drive circuitry, and graphics interface. On-chip RAM in 6802 provides X and Y axis character buffers. P/ROMs contain main

program and character templates. Timer frees processor to assemble dot data for next print interval during output of current data

address lines A13 to A15 on the partially decoded bus, are hardwired to the most significant address byte of the plot buffer. During plot formats, this arrangement allows the data bus to be read by a double byte LDX instruction, which automatically loads the most significant byte from port A and the least significant byte from the port B data bus. Thus, plot data are actually an input to the address bus via the index register. The most significant data bit, D7, drives the 2102 input, and the least significant bit is connected to the output. Once the dot address is entered into the index register, a hexa-

decimal 80 is loaded into the indexed address; the plot buffer is read during a print cycle; and a hexadecimal 01 produces a dot at its corresponding output address. Then the 1-bit plot data patterns combine with the character generator dot patterns to drive the printhead.

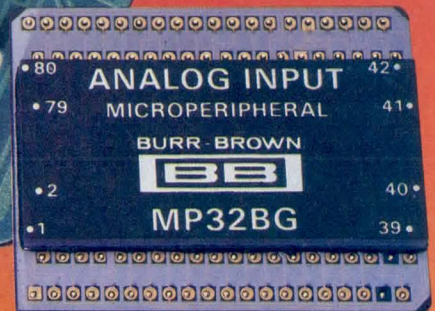
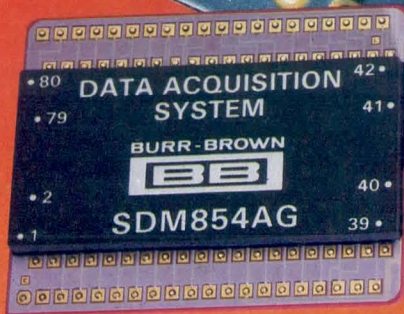
A complete line of dots requires six sequential, multiplexed print intervals to interlace printing of 264 dots (up to 48 per interval). The hardware print timer frees the processor to assemble dot data for the next print interval during the current print interval. The new dot data are then stored in a tem-

porary buffer until the current interval is complete, at which time they shift into the dot buffer, a 48-bit register; the timer triggers; and the next print strobe is applied to the head. If no dots need be energized for a given interval, the timer is not triggered and the strobe is bypassed, increasing the speed of the print cycle by triggering the timer for only those strobes for which there are dots to be printed. The X and Y axis character data buffers reside within the 128 bytes of 6802 internal random access memory (RAM), while the remainder of that internal RAM provides necessary temporary

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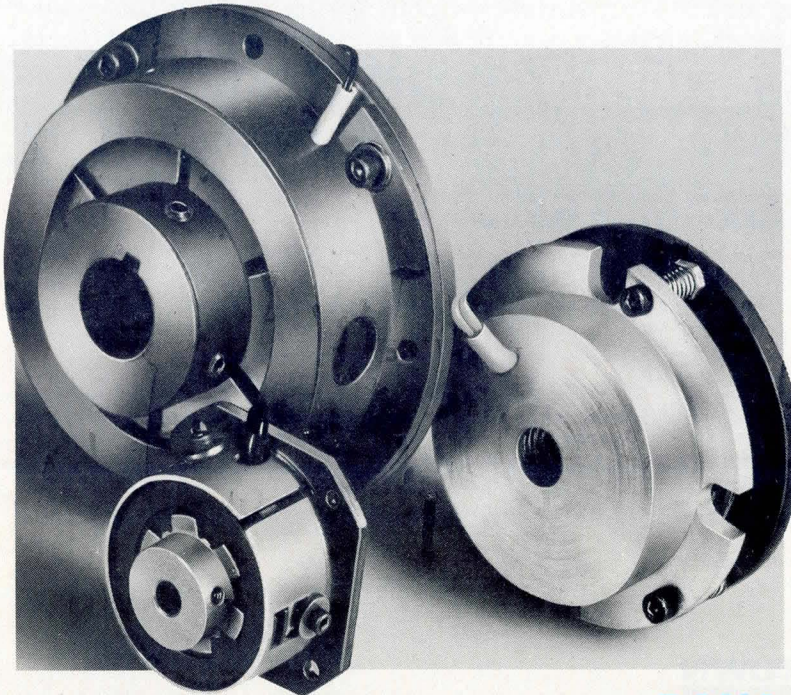
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registers and stack space to support the 4k-byte control program. Use of the 1-bit plot data buffer in conjunction with internal RAM minimizes the cost and board space required by data storage.

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Summary

A fixed head thermal printer/plotter addresses the expanded hardcopy needs of microprocessor based systems and their laboratory instrumentation applications by combining the quiet, low voltage, nonmechanical characteristics of thermal printing with byte and line level protocols. This permits mixed format operation to combine plot data and character data on a single line of output. While a special signal detects the need for mixed format operation and signals the host to implement mixed format protocol, another signal identifies windows where plot data can be accepted during the character paper advance, thus achieving low cost, high quality hardcopy output with minimal host system overhead.

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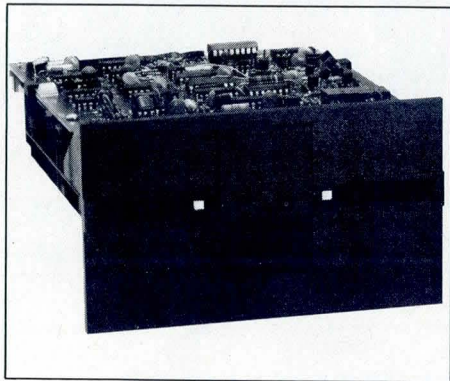
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HCMP 1835/6	2048 x 8 ROM
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HCMP 1852	I/O Adapter
HCMP 1853	3 to 8 Decoder
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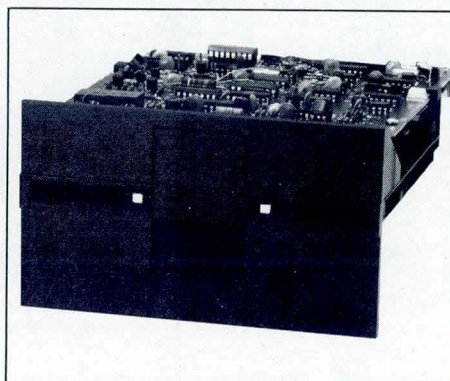
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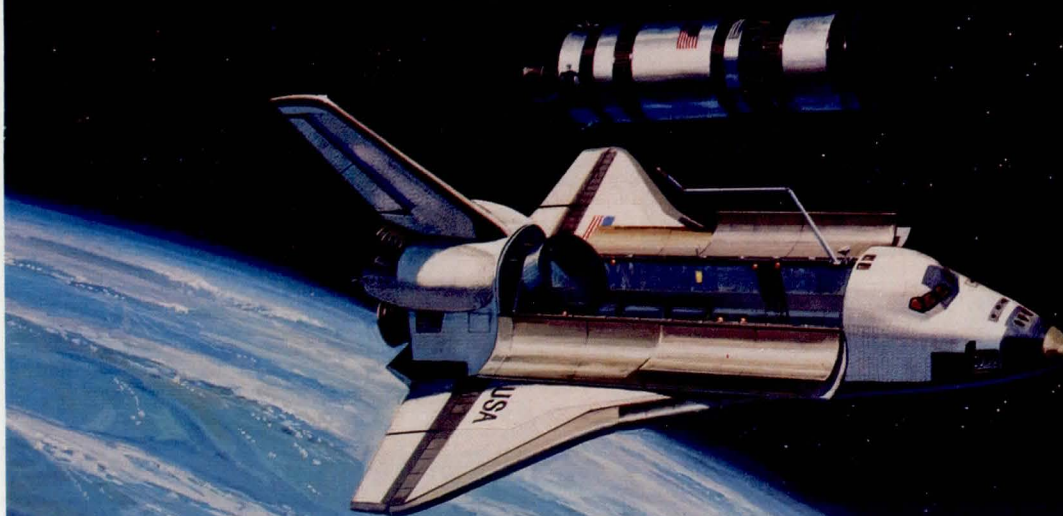
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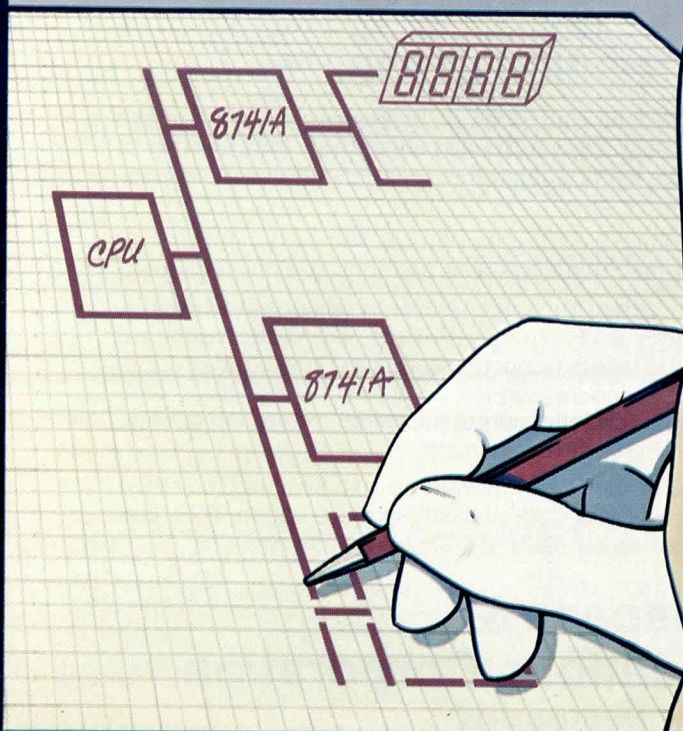
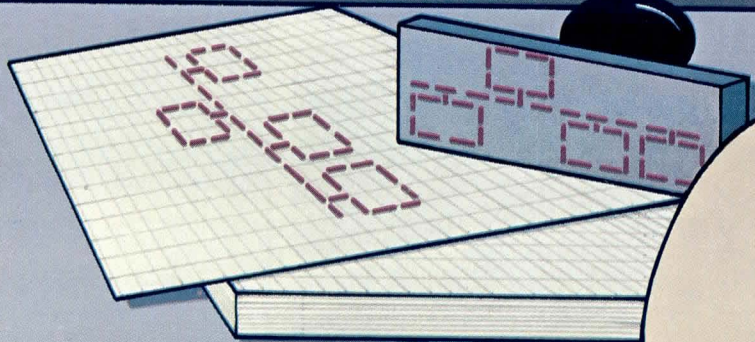
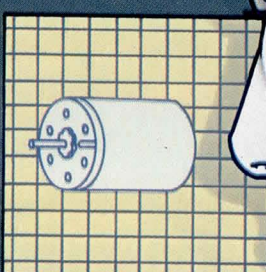
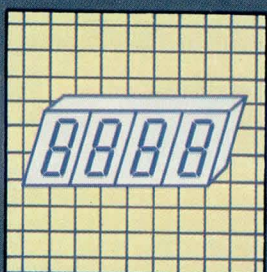
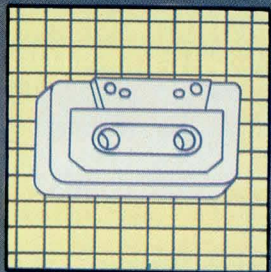
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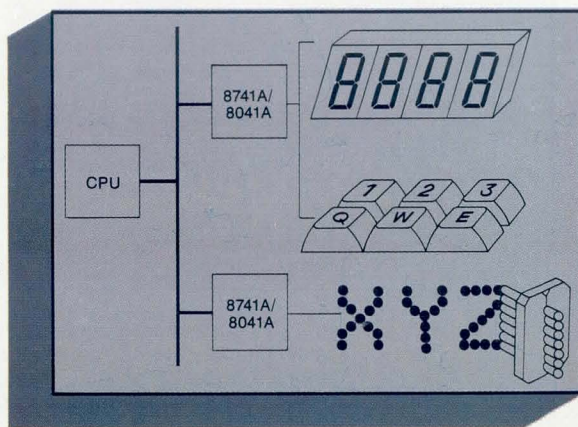
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Potential uses of multiport optical memories

High capacity optical memories with a relatively high data transfer rate and multiport simultaneous access capability may serve as the basis for new computer architectures. Several computer structures that might profitably use such a memory are a simultaneous record access system, a simultaneously shared memory computer system, and a parallel digital processing structure.

Fig 1 shows the proposed application of a high capacity optical memory in a simultaneous record access system involving the storage of vast quantities of information. Data are stored in page format in the optical memory, and requirements of each terminal are, in some cases, low enough to have one memory port feed several terminals through a multiplexer.

There are tradeoffs between port speed, multiplexer speed, and the number of ports. The most effective system would match the total number of users at one port to an economical multiplexer such that the average access time for any user is reasonable (about 1 min). This access time, divided by the number of users per port, fixes the multiplexer speed and memory access time per page.

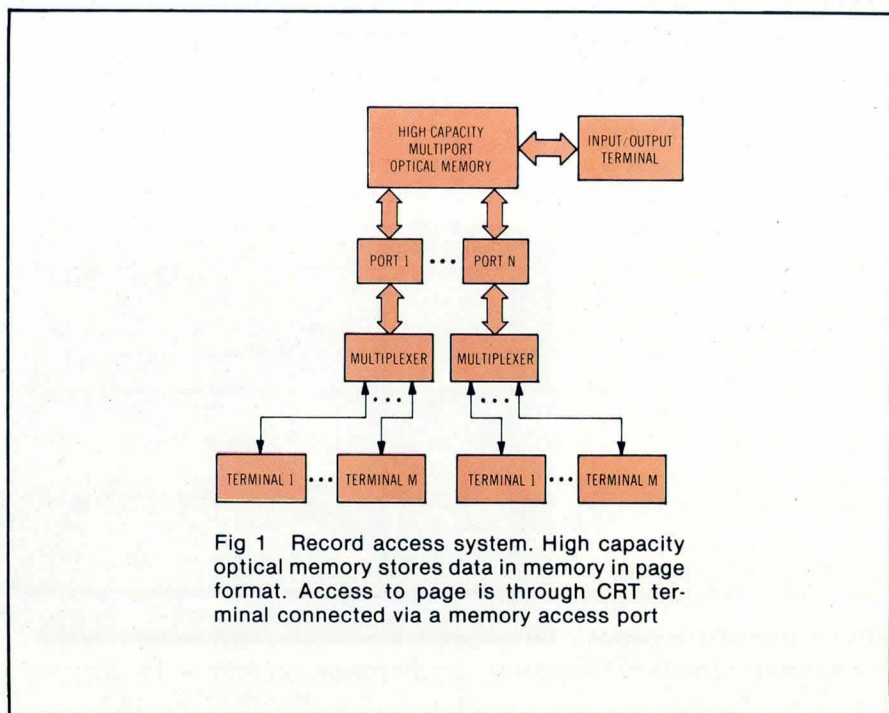


Fig 1 Record access system. High capacity optical memory stores data in memory in page format. Access to page is through CRT terminal connected via a memory access port

The user terminals are normally applied in the read only mode and are not allowed to perform write operations to memory. Writing is introduced through the input terminal through a separate memory port.

Fig 2 illustrates the simultaneously shared memory computer system. It is essentially the same as most current timesharing structures. Several users are allowed access to a processing unit. Primary memory is allocated, and user

programs are executed independently of the multiport secondary, if possible. Calls to special application programs and large blocks of data are obtained by swapping the data in and out of the multiport memory.

Since swapping of information between memories is a common problem in timesharing systems, the potential access ease and speed of moving pages in and out of the optical memory is a definite improvement. Some of the parameters needed to characterize such a system are number of bits per page, number of pages, number of ports, access time, primary memory size, write protection scheme, and division of the operating system between the primary memory and the multiport memory.

Fig 3 shows the computer structure for parallel processing. This arrangement is important in applications requiring an enormous number of computations.

The proposed structure is based on a single bus that allows this module to function independently of the other processors and the multiport memory. Each minicomputer (module) is connected to multiport memory through a port and a page memory buffer. This buffer is then tied to the bus for transferring to the processor and other memory units. Transfers between modules are made on an outer bus connecting each module.

An alternate configuration that places the control of all processors under one computer is also proposed. Instructions are kept in the optical memory and fetched by the control computer. Characteristic parameters of both systems are the number of bits per page, the number of pages, the number of ports, page transfer rates, bus transfer rates, and the types of synchronization signals.

Note

This work was done by C. O. Alford and T. K. Gaylord of Georgia Institute of Technology for Marshall Space Flight Center, Alabama.

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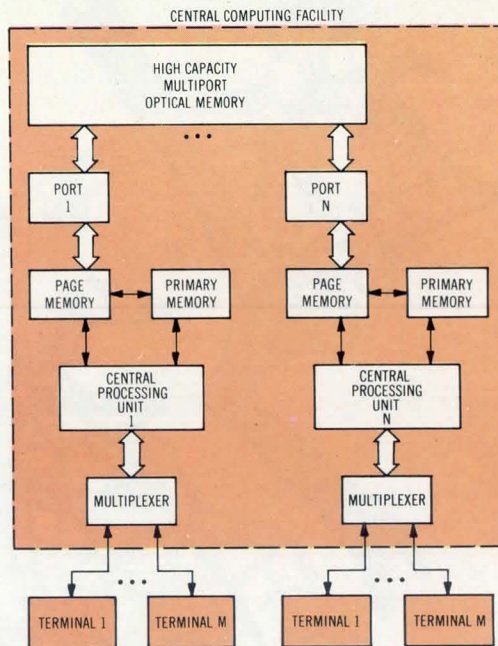


Fig 2 Simultaneously shared memory computer system. Secondary multiport optical memory is backing store mass memory device. Multiport structure makes it equivalent to several disc drives, and transport rate is superior to disc systems

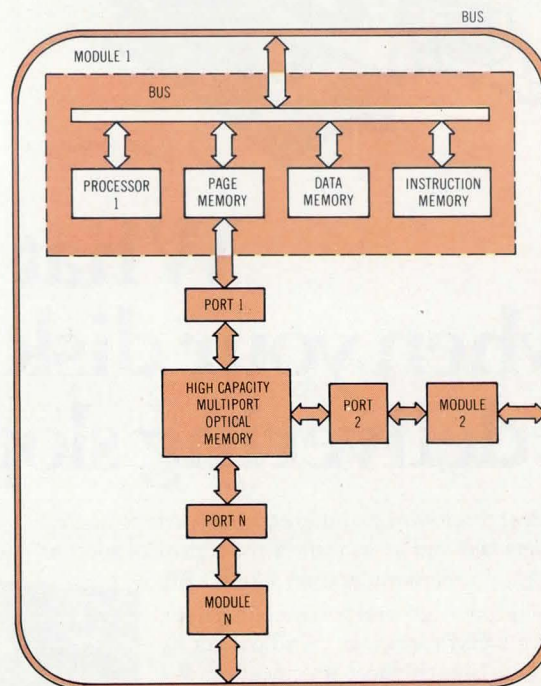


Fig 3 Computer structure for parallel processing. Configuration has several minicomputers (modules), each containing its own processor, data source, and instruction memory



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Computation-Saving Digital Filter

Less processor time is needed because low pass filter circuit first averages its input

A digital low pass filter circuit extracts slowly varying data signals from a high speed data stream with a minimum of computation. The circuit first averages the high speed signal, reducing its high frequency content, and then filters out the signal components within the flow frequency passband.

The new 2-stage filter requires less computation from a central processor. Thus, more inputs can be fed to the processor, or a slower processor can be used. Moreover, the 2-stage filter is not subject to the word length truncation

problem that afflicts conventional filters.

The usual digital filters, with sampling rates twice the highest frequency in the passband, demand considerable computation. However, if the input is averaged over a given period and the average is filtered at a comparatively slow rate, significantly less computation is required. The output is updated less frequently, but often enough to follow the slow output variations.

One application of the 2-stage filter is preprocessing sensor data before they are sent to a central processor.

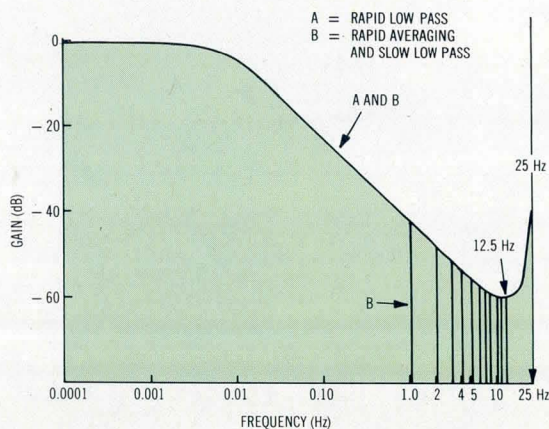
For example, the effectiveness of the 2-stage filter has been calculated for an instrument that measures the frequency difference between two similar rate gyros. The filter sends an updated output signal to a central processor every 960 ms. A conventional digital filter, in contrast, would present data more frequently—every 40 ms—but it would require many more central processor computations to do the same job. In this example, the conventional filter requires 24 multiplies, 72 add/subtract operations, and 48 load/store operations over a 1 s period (approximately), for a total processor time of 576 μ s. Over the same period, the 2-stage filter requires 2 multiplies, 50 add/subtracts, and 48 load/stores, for a total processor time of only 218 μ s. Yet the gain characteristic of the two types is virtually identical (see the figure).

In general, the 2-stage filter reduces speed and word length requirements, and the reduction can be substantial when many filters are needed. In instrumentation for correcting the biases of 12 gyros in the space shuttle, the speed requirement was reduced by 90%.

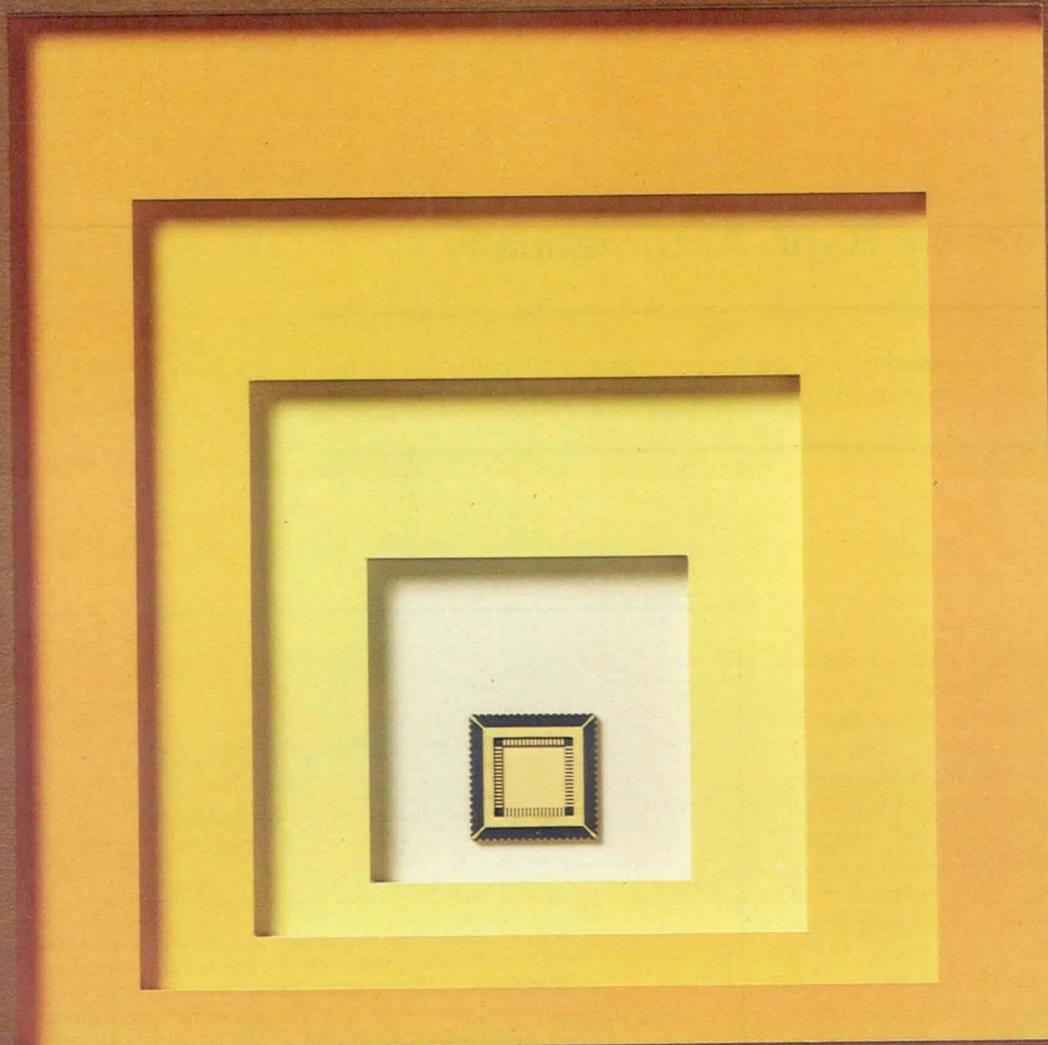
Note

This work was done by Delroy J. Sowada of Honeywell Inc for Johnson Space Center, Texas.

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Gain characteristic for 2-stage filter. Gain characteristic of rapid averaging followed by slow low pass is virtually same as single-stage (rapid low pass) digital filter. Two-stage filter has series of nodes near top of frequency range, but nodes have negligible effect on performance



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Measuring S/N Ratio Automatically

Fast bit error rate measurements are the basis of the S/N calculations for digital communication channel

An automated method of measuring signal to noise (S/N) ratio in digital communication channels is more precise and 100 times faster than a previously used method. The new method can be used with cable, microwave radio, or optical fiber links. It measures burst noise and channel capacity as well as S/N ratio and takes into account the effects of bandlimiting, cross talk, timing jitter, and power level.

The new method is based on bit error rate (BER) measurement. As in other BER techniques, the channel is stimulated with a pseudorandom digital signal with spectral characteristics resembling those of an actual data signal.

Unlike earlier BER methods, however, the new method varies the slicing threshold in the decision stage of the receiver—the level at which a bit is regarded as a 0 rather than a 1. Although this level is customarily fixed in a receiver, in the new method it is swept from its optimum value to the 1-level, while a pseudorandom signal is sent through the link until a specified BER is obtained. At that point, most of the errors are from noise superimposed on the 1-level, and thus the magnitude of the 1-level may be ascertained (Fig 1). From that magnitude, the S/N ratio can be computed by a simple formula. S/N measurements accurate within ± 0.01 dB can be made in a minute or less.

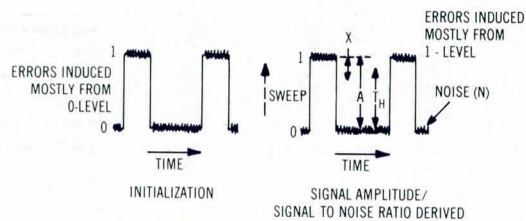


Fig 1 Zero/One threshold. When predetermined BER is reached, distance X separating 1-level and threshold is then known, permitting determination of signal level: $A = X + T_H$. S/N ratio is calculated by using signal amplitude (A) and noise amplitude (N); N can be determined at initialization (low threshold)

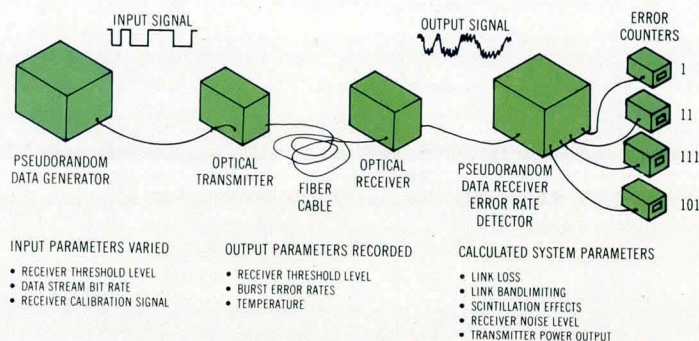


Fig 2 Measurements on fiber optic channel. In addition to S/N ratio, burst noise and channel capacity can be measured simultaneously by employing multiple error counters

A pseudorandom data generator drives the channel to be measured (Fig 2 illustrates the setup for an optical fiber link). The data pass through the link where they are corrupted by noise, bandlimited, regenerated, and finally transferred to a pseudorandom data receiver. The receiver contains a data generator identical to the one in the pseudorandom data transmitter and runs in synchronism with the data coming out of the link. The receiver makes a bit by bit comparison of the data coming out of the link and those generated in the receiver. When a discrepancy occurs, the receiver sends an error pulse to a counter. The measurement is usually terminated when the counter accumulates 100 errors; this total provides a sample size large enough for accurate determination of BER.

The procedure is repeated for a range of threshold values so that the S/N ratio can be calculated. In addition, various other calculations of channel performance can be made, such as burst noise and channel capacity. The measurement setup can be automated by a microprocessor that controls the test variables, monitors the data collection process, and formats the data.

The prototype automated test system is contained on five circuit boards: a high speed BER test block, a central processing unit, a power controller, a temperature sensor array, and the fiber optic link terminal module. The circuitry employs 140 integrated circuits.

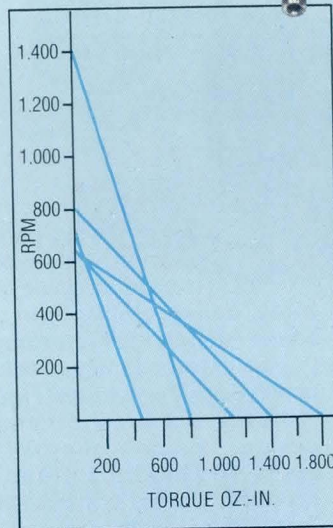
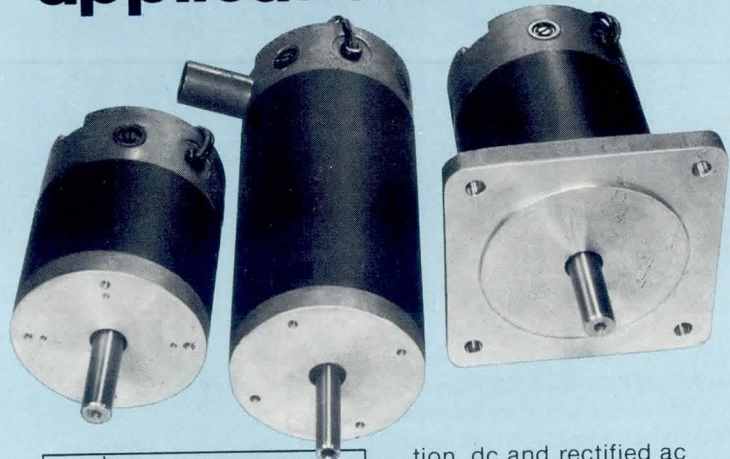
An important practical advantage of the BER approach is that most of the test circuitry is digital, reducing calibration and temperature stabilization requirements to a minimum.

Note

This work was done by Larry A. Bergman and Alan R. Johnston of California Institute of Technology for NASA's Jet Propulsion Laboratory, Pasadena, California.

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To aid you in your tube decisions, we give you clear, numeric definitions of the performance characteristics of our CRTs. When you specify Amperex CRTs, you know what you're ordering.

For example, our all-new M38-320 and M38-330 series of CRTs for data/graphic displays can achieve 1500 TV lines resolution even at 20 ft-L screen brightness with Grid 2 at 630 V. On the other hand, if you need 40 ft-L screen brightness, you can still obtain 1400 TV lines by raising Grid 2 to 650 V. By referring to our information-packed spec sheets, you can select the optimum operating point for your particular requirement.

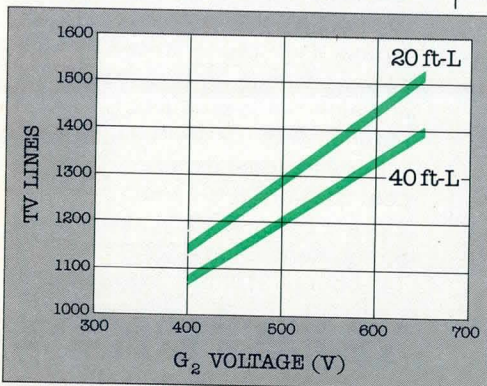
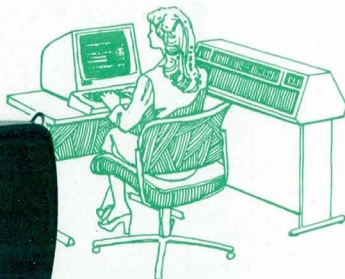


FIG. 1 — M38-320 and M38-330 CRT Resolution (TV lines) as a function of Grid #2 potential with P-4 phosphor.



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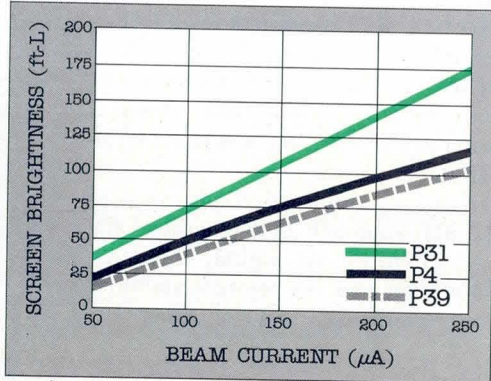


FIG. 2 — M38-320 and M38-330 CRT Screen Brightness as a function of beam current with screen potential 17 kV. (P4, P31 and P39 phosphors.)

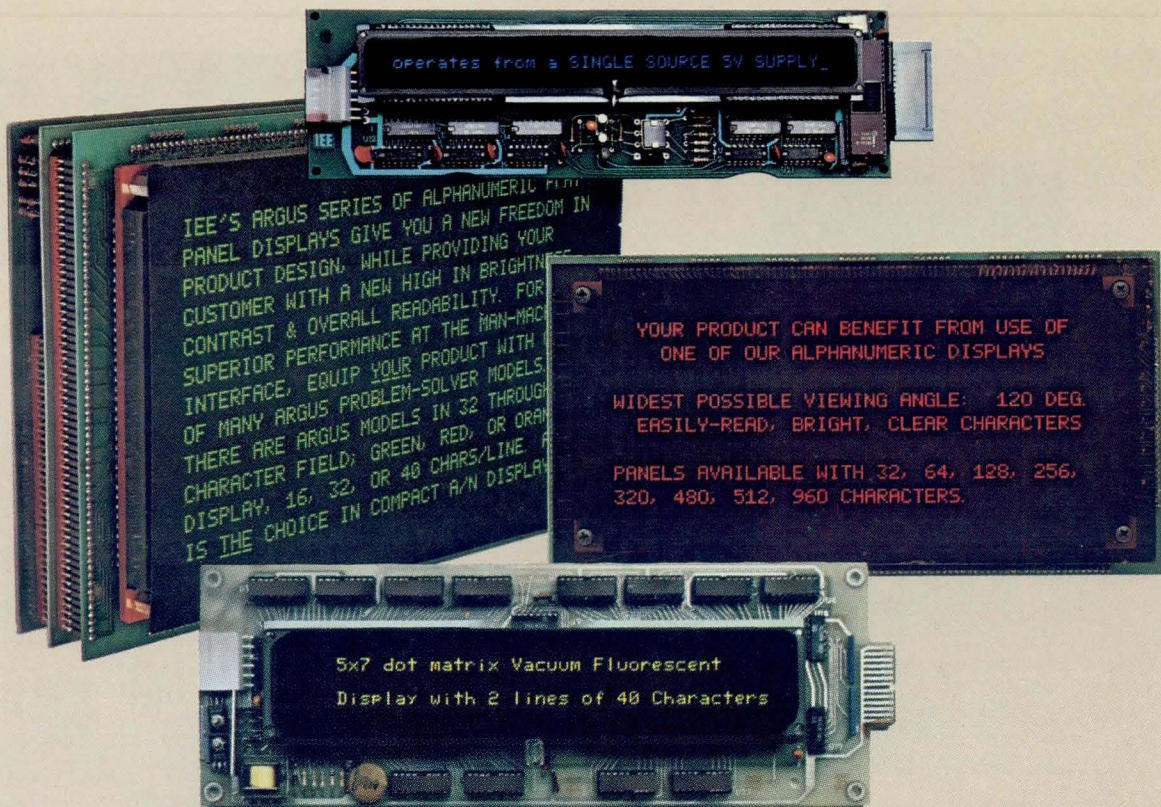
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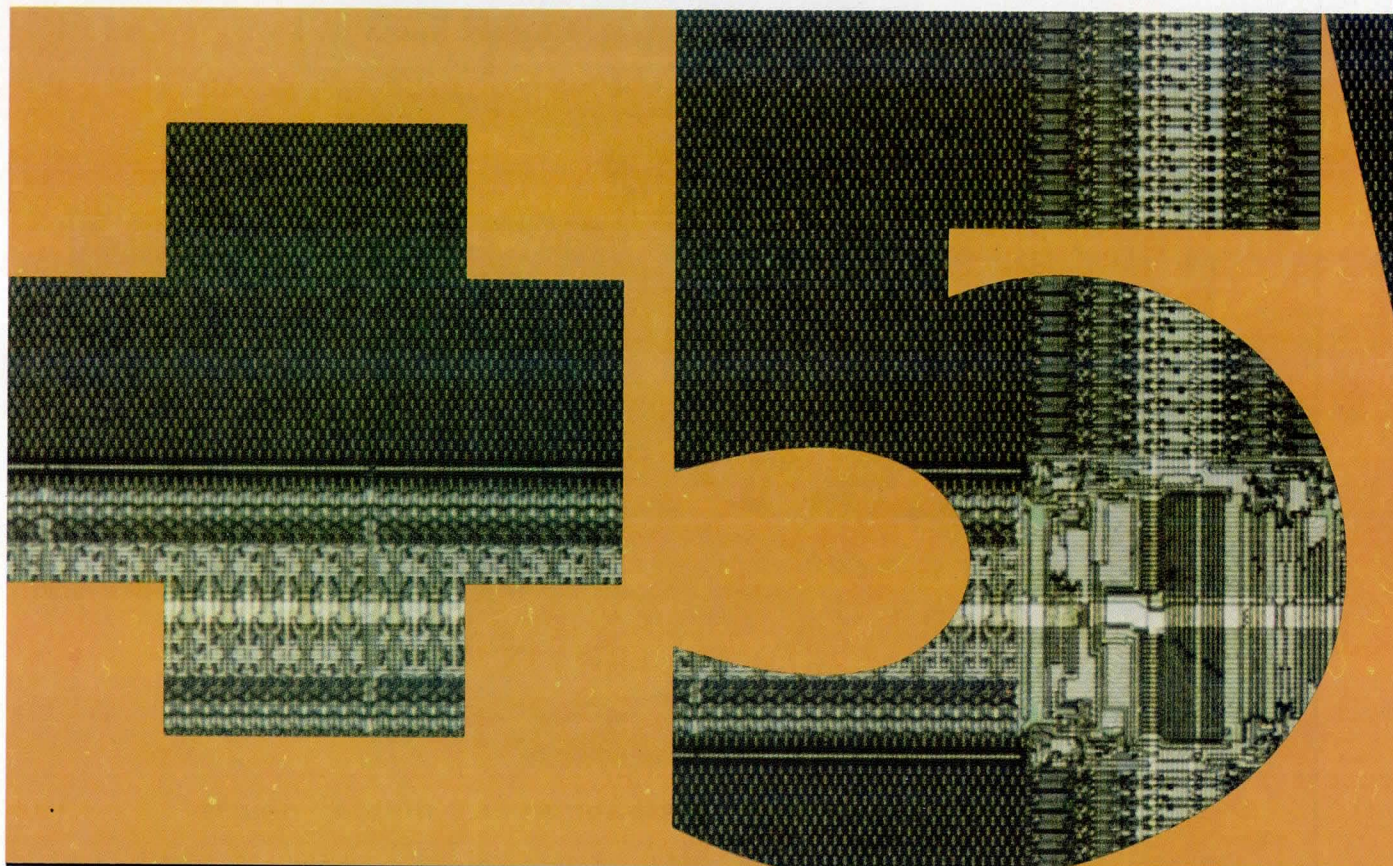
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V dynamic RAM family today, from Motorola.



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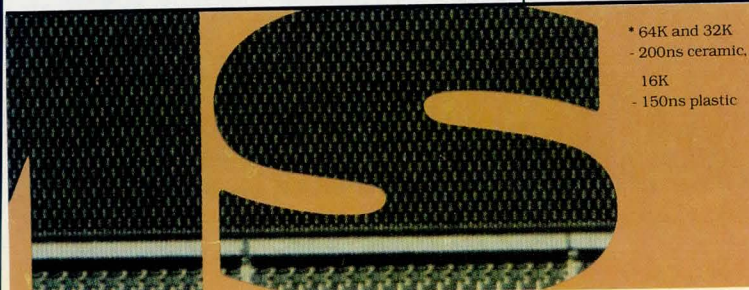
Motorola's +5 V 64K RAM was the first in volume production. Now, two versions are available. The original MCM6664 has the leadership Pin 1 self-refresh and auto-refresh functions. The MCM6665, without Pin 1 refresh, is now also in volume production.

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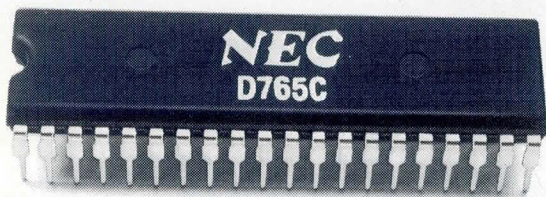
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The μ PD765 is completely IBM-compatible and can control any combination of up to four floppy drives—8" or 5¼", single- or double-density, single- or double-sided. It's



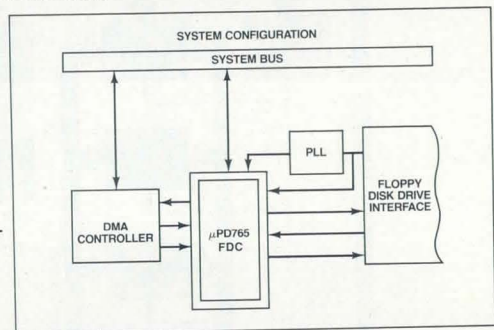
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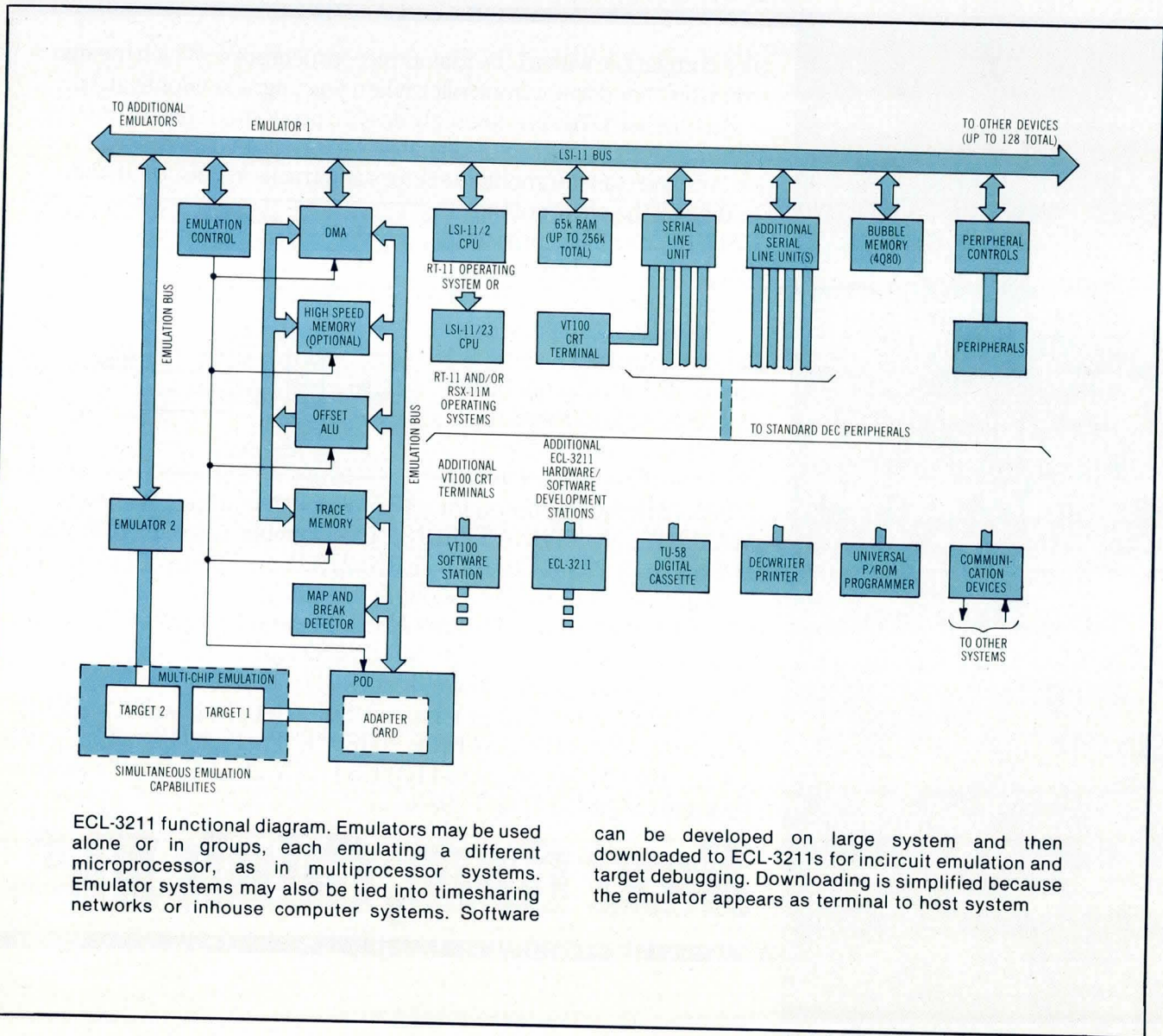


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Universal Development System Offers Realtime Emulation of 4- to 32-Bit Microprocessors



ECL-3211 functional diagram. Emulators may be used alone or in groups, each emulating a different microprocessor, as in multiprocessor systems. Emulator systems may also be tied into timesharing networks or inhouse computer systems. Software

can be developed on large system and then downloaded to ECL-3211s for incircuit emulation and target debugging. Downloading is simplified because the emulator appears as terminal to host system

Any microprocessor from any 4- to 32-bit family may be emulated in real time at up to 30 MHz by the ECL-3211 microprocessor development system. Multiple microprocessors can be emulated simultaneously by adding boards and pods.

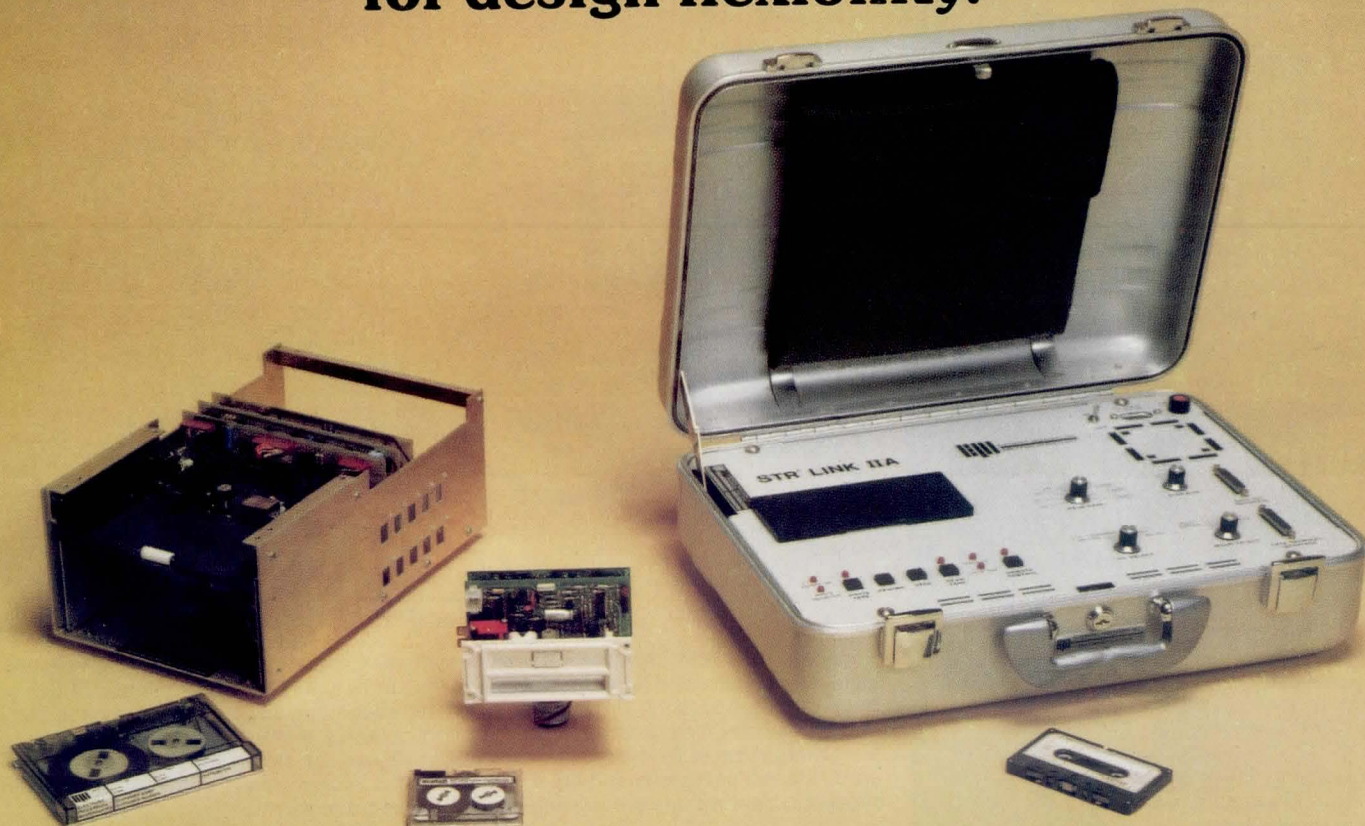
Also functioning in standalone or downloaded applications, the system

uses a software driven approach that eliminates the need to install new emulator hardware each time a new chip becomes available; the only task required is the loading of the new chip software and the plugging in of an adapter card for the chip family. Emulation support, including assemblers and linkers for each new

microprocessor is available from Emulogic, Inc, 362 University Ave, Westwood, MA 02090.

A basic system includes an LSI-11/2 CPU, 64k bytes of 210-ns RAM (expandable to 256k bytes), 1M-byte double-density dual-floppy disc, 512 x 64-bit trace buffer, VT103 terminal with full
(continued on page 168)

STR[®] technology for high data integrity. Three major tape formats for design flexibility.



We don't forget the OEM's needs.

The **STR-810** digital recorder is designed for data logging, data acquisition and as a system loader. Using either the 3M DC-300A or DC-300XL cartridges, packing density is 1600 bpi, for respective data capacities of 2.3M bytes and 3.4M bytes per cartridge, using four tracks. Features include microprocessor-controlled tape movement and read/write electronics. For maximum versatility, interfaces include RS-232 and IEEE-488. Or, using control and status lines available, you can interface to specific microcomputers such as LSI-11 and 8080. EPI's optional ANSI X3.56 formatter, with NRZI or phase-encoded personality cards, turns the 810 into a plug-in component for industrial instrumentation and mini/microcomputer-interfaced peripheral markets. Price: \$756 in quantities of 100. **STR-STREAM** is a high-speed, high-capacity version of the 810 designed for Winchester disc backup. Density is 6400 bpi for 17M bytes capacity per cartridge. Features include advanced head design, MFM formatting and compatibility with 8" or 14" discs.

EPI's **STR-610** is a compact, low cost digital recorder that's ideal for use with POS terminals, smart CRT terminals and as a general peripheral for mini/microcomputer-based systems. The 610's recording density is 800 bpi for a capacity of 168K bytes/track, using a two-track 3M DC-100 mini-cartridge. Formatting is ANSI Standard and interfacing is parallel, with a variety of options. Price: \$280 in quantities of 1,000. **The STR-LINK III** is a high-speed (9600 baud), portable program loader that uses the STR-610's drive system and shares the same specifications. It is used as a field service tool for diagnostic work or as a peripheral in a mini/microcomputer system. STR-LINK III uses a serial RS-232 interface for data communications or data terminal applications, and it can be controlled through RS-232, ASCII control codes, or manually. Price: \$1,561 in single quantity.

STR-LINK II is EPI's proven medium-speed (1200 baud) universal portable program loader for programmable controllers and process control systems. Using a standard cassette, it features switch-selectable transmission modes for maximum flexibility. Price: \$1,735 in single quantity.

For maximum design freedom, proven reliability and high data integrity through Speed Tolerant Recording technology, remember EPI—the company that doesn't forget the OEM's needs. For more information, contact Electronic Processors Inc., P.O. Box 569, Englewood, Colorado 80110. Phone (303) 761-8540.

E0/3

Let EPI remember for you.

EPI ELECTRONIC PROCESSORS
INCORPORATED

CIRCLE 91 ON INQUIRY CARD

MAGSTRIPE™

Readers and Reader/Encoders



Model 40 Reader

7.75" x 1.64" x 1.37" H

Model 44 Reader/Encoder

7.75" x 1.64" x 1.37" H

Field proven, economical means for reading and encoding magnetic stripe cards, badges and passbooks.

Our Magstripe™ product line of Readers, Encoders and Reader/Encoders features:

- Reading and encoding to ANSI X 4.16-1976; tracks 1, 2 and 3.
- Non-standard densities, including IBM's 127.5 BPI.
- LSI circuitry.
- Spatial decoding*; card velocity range 5-60 IPS; insensitive to acceleration, low amplitude and jitter.
- Rugged construction; permits outdoor installation; virtually maintenance free.
- **Unique Magstripe™ Heads***, independently suspended and gimbal-mounted. Minimum head and card wear. Highest reliability with warped and contaminated cards.

Proven, world-wide performance in a variety of applications including:

- Airline ticketing terminals
- Bank terminals
- Building access systems
- Bulk fuel dispensing terminals
- Data input for CRT terminals
- POS terminals
- Computer access devices
- Identification and badges
- Self-service gas stations
- Fare collection systems
- Time and attendance terminals
- Plant communication systems

MAGSTRIPE™ SYSTEMS — Readers and Reader/Encoders Available with RS-232C Interface

- DTE or DCE connection under EIA RS-232C and RS-449 standards; ASCII characters.
- Provide all control functions and ANSI formatting for Magstripe™ units.
- Baud rates to 2400; strap change to current loop.
- Available PCB only, or in enclosure with power supply.

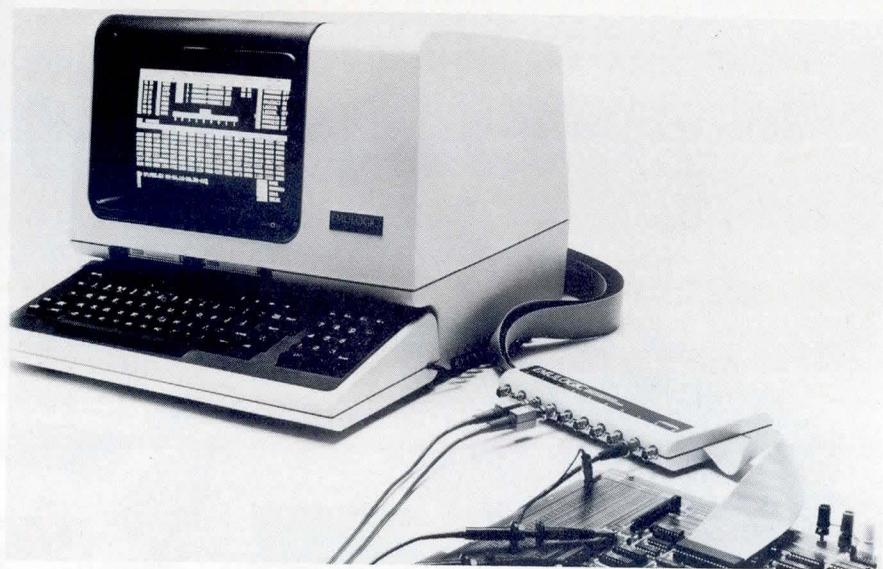
*Patented

For more information,
contact:

**American
Magnetics
Corporation**

MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS



Emulogic ECL-3211 universal emulation system. General purpose emulator pod provides eight inputs and two trigger outputs that allow simultaneous emulation of two or more microprocessors. Provision is made for scope and logic analyzer hookup. Any microprocessor may be emulated, regardless of family or word length at up to 30 MHz. Built around the PDP-11, software driven system also can stand alone or operate in network. Display of register and external input status, memory map, and trace control and breakpoint definitions are provided on full screen display

screen display and keyboard editor, DEC RT-11 operating system and software, and full hardware/software emulation support for any one chip family.

In emulation operation, the system is genuinely transparent to the target processor. Debugging is aided by a full screen display, specific to each chip; trace buffer; and eight breakpoints, defined as logical functions. All are transparent in time and location to the target. Combined with event counters and an elapsed time counter, a built-in 64-channel realtime logic state analyzer is available.

Any combination of address, data, control, and external lines can be examined, and BNC connectors are included for probe connection. Two trigger outputs also are provided. The display features split screen smooth scrolling, allowing user scan of RAM, ROM, or trace buffer at will, displayed in either hexadecimal or disassembled mnemonics.

A breakpoint function allows users to inject a phantom program anywhere

in the target program without using any target memory space. Up to 64 stations may be tied together in any combination of software development and incircuit emulation stations.

Included in the VT103 CRT terminal are a 4-quad size slot LSI-11 bus card cage, 80 x 24 display format, smooth scrolling, split screen, reverse video or underline, and composite video I/O. The terminal operates on full-duplex asynchronous communications lines.

Serial I/O provided includes 4-channel asynchronous capability compatible with RS-232-C, RS-423/422, or current loop. Baud rates are from 150 to 38.4k, individually configurable, with one line dedicated to the CRT terminal.

Macro relocatable assemblers are provided for each microprocessor chip family. A consistent command structure and standard PDP-11 pseudo-ops are used throughout. Mnemonics used with each assembler are identical with those of the chip being used.

Circle 465 on Inquiry Card

Introducing quality print at matrix speed. For only \$1295*.



Until now, you could pay thousands for a slow, letter-quality character printer. Or hundreds for a dot matrix printer, giving up print quality for speed and price.

But that was before Paper Tiger™ 460 offered you a better choice.

The new Paper Tiger 460 is the first matrix printer with high-density dot matrix characters plus high speed. At a low price.

The secret? A unique nine-wire, staggered matrix head provides overlapping dots in both horizontal and vertical planes. The result is dense, high-quality characters you'll be proud to show off.

What's more, Paper Tiger 460 gives you a combination of features simply not available on any other printer, at any price. Like bi-directional, logic-seeking printing at speeds in excess of 150 cps. Microprocessor electronics, with field-installable character sets. Proportional spacing. Automatic text justifica-

Integral Data Systems stands ready to provide you with the performance printers ideally suited to your needs. In fact, the printer, the IDS 460, offers features that are not available on any other printer, at any price.

Automatic proportional spacing, logic-seeking printing at speeds in excess of 150 cps. Microprocessor electronics, with field-installable character sets. Proportional spacing. Automatic text justification. DotPlot™ high resolution graphics option. RS232 and parallel interfaces. And more.

Paper Tiger 460 Print Sample

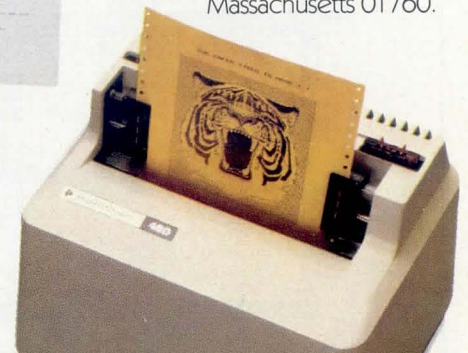
tion. DotPlot™ high resolution graphics option. RS232 and parallel interfaces. And more.

But its most important feature is high reliability. The Paper Tiger 460 is designed to be tough and dependable. It has rugged, stepper-motor head and paper drives. A new 300-million-character ballistic-type print


head. And its simple, chassis-mounted cartridge ribbon lasts up to four times longer than cassette or spool ribbons.

All this means that Paper Tiger 460 is perfect for word processing, data processing, or electronic mail. It's also perfect for anyone who requires the flexibility of a matrix printer but wants superior quality printing. Without trading off speed or price.

Get your paws on the Paper Tiger 460, and join the tens of thousands of satisfied Integral Data Systems users. Call us toll-free: 800-343-6412. (In Massachusetts, Alaska, and Hawaii, call (617) 237-7610.) Or, write for complete specifications. Integral Data Systems, 14 Tech Circle, Natick, Massachusetts 01760.



Paper Tiger 460

 Integral Data Systems, Inc.

CIRCLE 93 ON INQUIRY CARD

*Suggested single-unit, U.S. price. Generous OEM discounts available.

CPU Module Permits Flexible Memory Arrangement

Based on the Z80, the MDX-CPU2 central processor module is part of the MD series STD-Z80 BUS system from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006. Six 24-pin memory sockets enable the user to populate the module with any combination of designated ROM, RAM, and EPROM. Flexible address decoding allows configuration

of each memory device within any 1k-byte boundary of the 64k-byte memory map.

A P/ROM decoder permits a choice of one of four preselected memory configurations. Also, by programming a decoder P/ROM, any of the six sockets may be assigned memory addresses as required. Address, data, and control buses are bidirectional to allow external masters to directly access CPU memory.

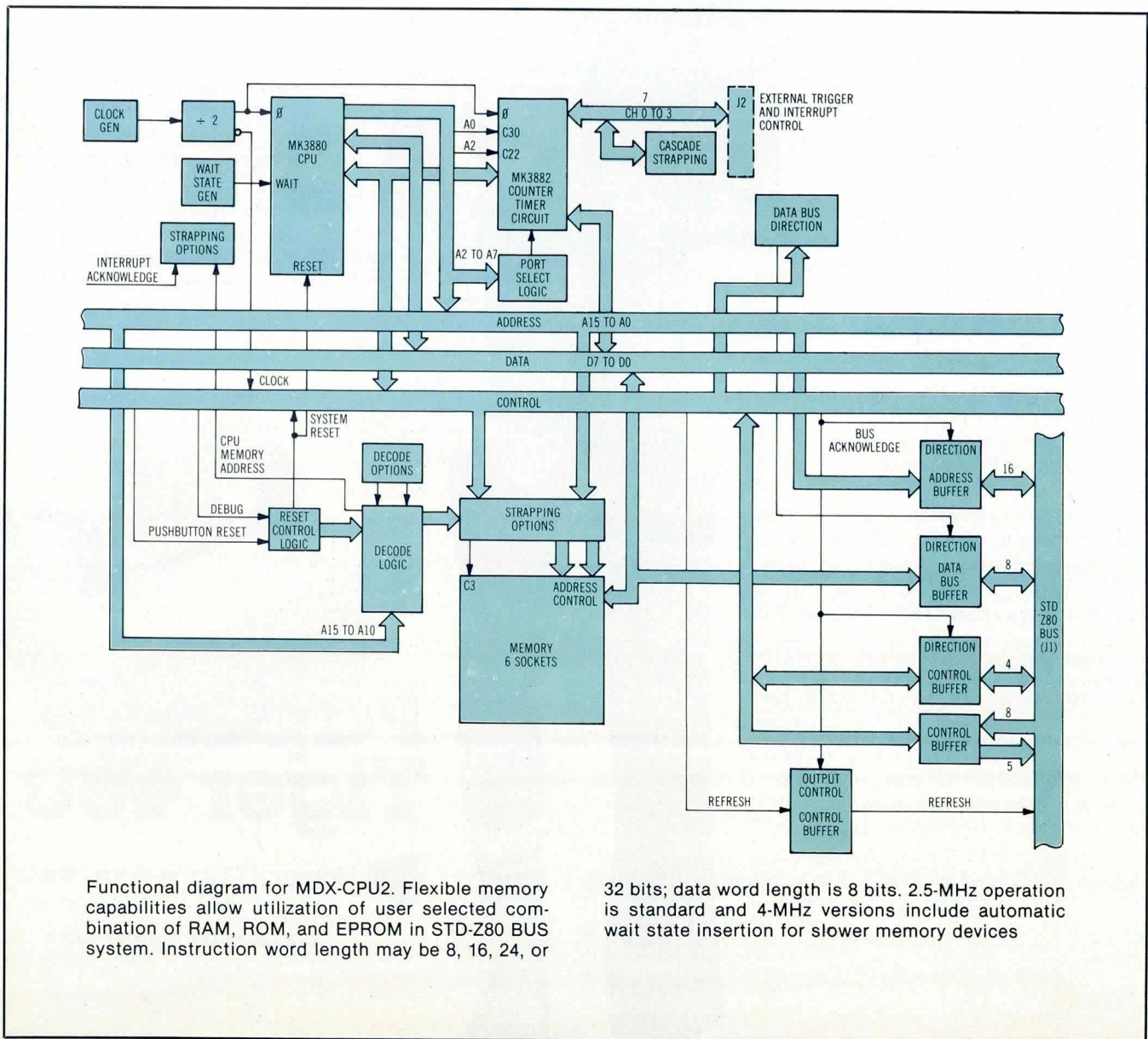
All address and control signals necessary to refresh dynamic RAM are generated by the module. Refresh occurs automatically during each op code fetch cycle and is transparent to system throughput. Offboard expansion to a total of 64k bytes is possible.

Interrupt processing may occur in any of three different modes, including vectored. Multilevel interrupt processing is also possible, with the level of stacking limited only by available memory space.

Circle 466 on Inquiry Card

Memory Management Device Affords Segmented Addressing

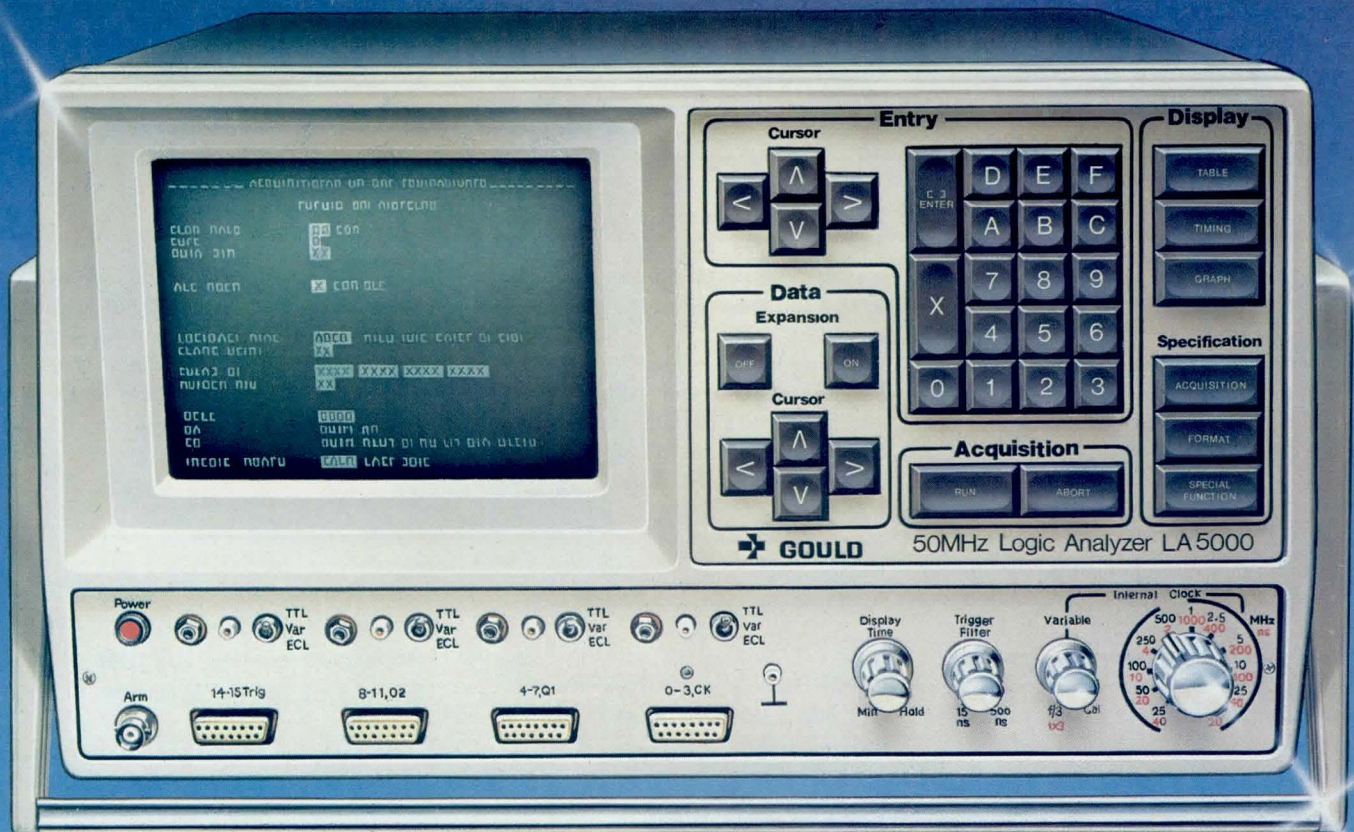
Designed to afford memory protection and dynamic segment relocation for each of the Z8001 CPU's 8M-byte address spaces, the Z8010 memory



Functional diagram for MDX-CPU2. Flexible memory capabilities allow utilization of user selected combination of RAM, ROM, and EPROM in STD-Z80 BUS system. Instruction word length may be 8, 16, 24, or

32 bits; data word length is 8 bits. 2.5-MHz operation is standard and 4-MHz versions include automatic wait state insertion for slower memory devices

MICROPROCESSOR GLITCHES: MEET YOUR FIXER.



Biomation's new LA-5000 50MHz logic analyzer brings the convenience of our K100-D to microprocessor designers.

Following our K100-D, which sets the industry standards for digital system debugging, Biomation brings you a new glitch fixer, the LA-5000. A logic analyzer matched in cost and capability to the needs of microprocessor system designers.

The LA-5000 is ideal for data domain and timing analysis with clock rates from 12.5 MHz with 16 recording channels, to 50 MHz with 4 channels. Three display modes give you: data domain information in binary, octal or hexadecimal; timing diagrams; even a graphic plot of successive word values.

Three full screen interactive menus—Acquisition, Format, and Special Function—make set-up fast and simple. There are also partial menus of frequently needed parameters as part of the display modes.

Convenience features? The LA-5000 features two

memories with an auto-stop function to simplify fault-finding. Reverse video highlighting calls attention to memory differences. The reference memory is easily accessible via the keyboard. And, a memory search feature matches like sequences in both working and reference memories.

Introduce the glitches plaguing your system to their fixer. You'll enjoy efficient system debugging at a price well below what you'd expect to pay. For more information on the LA-5000, or any of Gould's full line of logic analyzers, write: Gould Instrument Division, Santa Clara Operations, 4600 Old Ironsides Drive, Santa Clara, CA 95050. Or call (408) 988-6800.

 **GOULD**
An Electrical/Electronics Company

*Got a glitch?
Get a*
**GLITCH
FIXER
FROM GOULD**

CIRCLE 94 ON INQUIRY CARD

management unit also supports high level language requirements. The device provides memory space with a logical structure, largely independent of the physical location of data. It also protects a system from inadvertent and unauthorized operations such as attempts at execution of data, access to memory resources or data, or operating system access.

Each device has 64 randomly accessible segments ranging in size from 256 to 64k bytes that can be mapped into a total physical address space of 16M bytes. The combination of the device and the CPU greatly simplifies the complex task of managing large address space of up to 48M bytes in systems having multiple processors or virtual memory configurations.

Segmented addressing capabilities offered by the Z8001/Z8010 combination from Zilog, 10340 Bubb Rd, Cupertino, CA 95014, facilitate modular programming, which allocates the total available address space to various program modules and data areas. Unlike linear addressing, segmented address space allows assignment of each procedure and data set to a separate segment.

Circle 467 on Inquiry Card

Software Development Tool Supports iSBC Small Program Development

Intended for low cost, small program development and debugging in iSBC single-board computer based systems, the model 810 software development module adds resident text entry, editing, assembly, and debug facilities. All five iSBC Multibus compatible architecture computers are supported.

Typical minimum system configuration for software development includes iSBC chassis or iCS™ industrial control system chassis, an iSBC, model 810 module, RAM expansion board, TTY adapter, and serial I/O cable set. The

system interface supports use of a TTY keyboard, printer, and paper tape reader/punch.

Supplied with the module are text editor, 8080/8085 symbolic assembler, and three debug monitors, all on ROM. All editor commands are single character and permit programs to be entered and updated from a teletype-writer terminal. The symbolic assembler is a subset of the full 8080/8085 assembler from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, and produces absolute code, which may also be stored on paper tape or in RAM, for immediate loading and execution.

Debug monitors allow the user to examine, modify, and dump registers and memory locations, and to interrupt the program at user specified breakpoints, while controlling system I/O.

Circle 468 on Inquiry Card

Handheld μ C Includes 1-Line Display and Typewriter Keyboard

Known as NewBrain, a product of Newbury Laboratories, Ltd, King St, Odiham, Hampshire RG25 1NN, England, the microcomputer uses compiled BASIC software, high speed arithmetic processing, and full screen and line editors. The unit features a standard typewriter keyboard layout and generates output on a single-line fluorescent alphanumeric display. Printer, monitor, and television receiver display interface are provided for.

The unit measures 6.25 x 10.25 x 1.5" (15.8 x 26.7 x 3.8-cm) and is available in three versions. Model MB is ac powered and includes rechargeable batteries; model MBS employs low dissipation components for extended battery use; model M operates on ac only with an external TV receiver or video monitor and does not have a built-in display.

Connectors are provided for TV, video monitor, printer, or modem. A user port and analog interface connectors adapt user equipment to the system. Dual 1200-baud audio cassette interface connectors permit flexible manipulation of data and program storage. Floating point calculations include all trigonometric and inverse trigonometric functions.

Up to 224 characters may be generated by the keyboard, including 96 ASCII upper- and lowercase characters, and 32 control codes. A graphics key generates 64 Viewdata graphics symbols for external display. User defined keys are software programmable, while software extension modules can expand memory up to 4M bytes.

Circle 469 on Inquiry Card

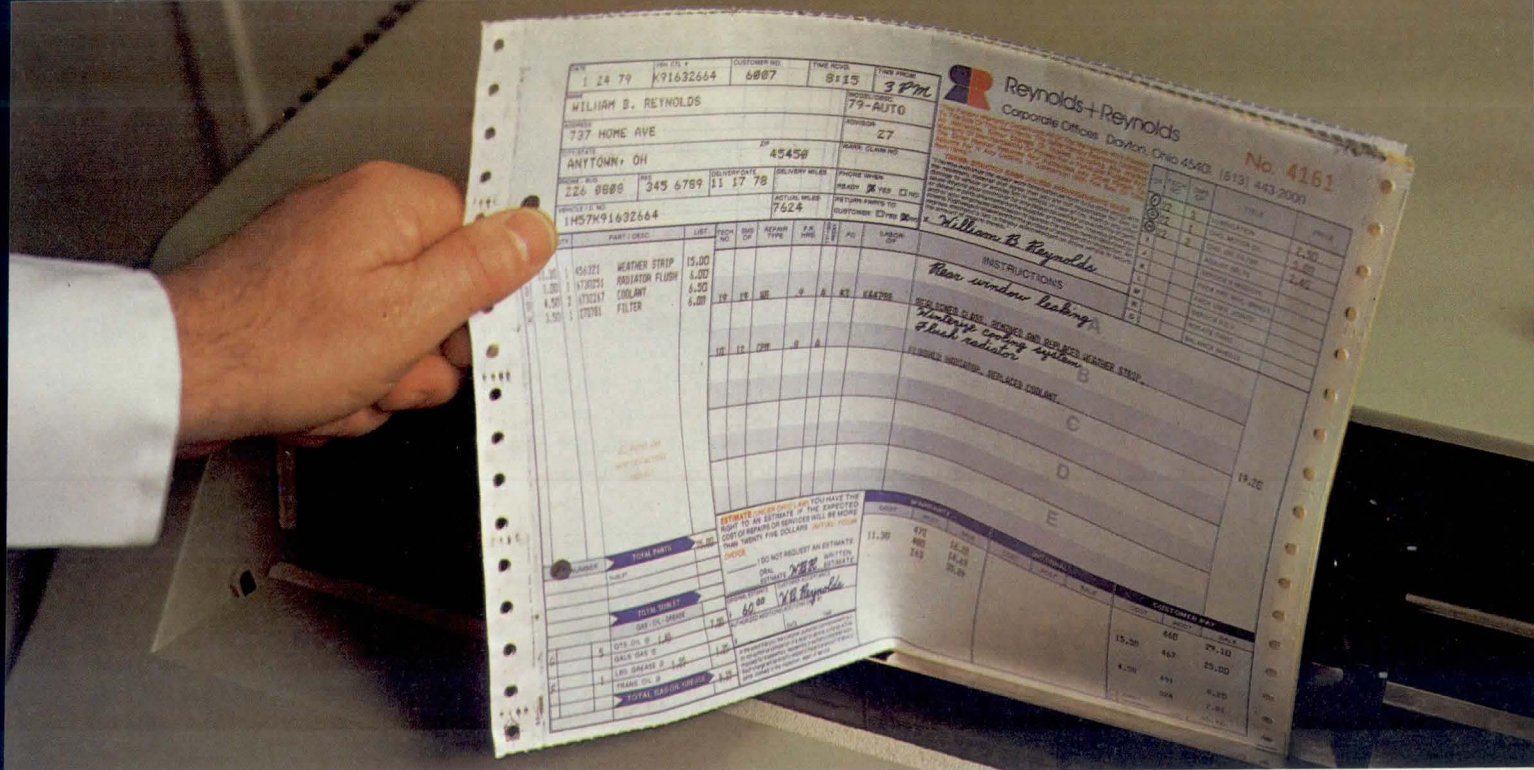
Diskette Subsystem Provides up to 1.26M Bytes of Data Storage

Data transfer rate of the DG/diskette subsystems in 62.5k bytes/s, utilizing the double-sided, double-density diskettes. On each side, 512 bytes are contained in 16 sectors on each of 77 tracks. The 8" (20.3-cm) model 6096 drives from Data General Corp, Rte 9, Westboro, MA 01581, may be arranged in 1-, 2-, or 3-drive configurations to provide up to 3.78M bytes of storage capacity.

Intended for use with the company's microNOVA™ computer family, one or two drives may be housed in a 7.5" (19-cm) high rackmount unit. The subsystem diskette controller is a 7.5 x 9.5" (19 x 24-cm) board that mounts in one slot of the microcomputer chassis.

Comprehensive software support, as a master system disc or as an I/O device, is provided by the company's MP/OS operating systems. Up to four consecutive sectors can be transferred using a single I/O command.

Circle 470 on Inquiry Card



Push-n-pull tractors, adjustable tear bar and 1-to-9 part forms handling: all in one printer.

Finally, real-time forms access plus continuous forms output in one printer. Perfect for such applications as airline ticketing, invoicing, order preparation and more. And another example of the expanding TermiNet 200 printer family's application versatility.

No-waste, flexible forms control

One reason: an adjustable tear bar that lets you use standard forms with different header lengths. For precise alignment, no paper waste and clean paper tear. Every time.

More reasons: servo-driven tractors that allow infinite manual adjustment in both forward and reverse. A non-volatile electronic VFU that makes forms set-up easy and permits storage of up to 8 vertical formats. A down-line loading option enabling you to load formats directly from your data source. Plus straight-through paper path and push-n-pull tractors that give you perfect first-to-last-copy registration. As well as smoother paper handling for all types of forms, including single-part paper.

More features add up to more application versatility

With TermiNet 200 printers, you can also get a 9 x 9 printhead for exceptionally legible underlining and lower-case descenders. Two complete 96-character switchable print fonts for ASCII/APL use or your own special needs. A choice of Magnetic Tape or Edit Buffer Accessory. Plus a 100% duty cycle capability, excellent print quality at speeds up to 200 cps and low cost of ownership. All of which help make TermiNet 200 teleprinters and line printers the industry workhorses.

Immediate delivery instead of piecemeal allocation

Why wait months for other printers when TermiNet 200 printers are available now? When you need them. Mail the coupon today and find out how the expanding TermiNet 200 printer family can meet your range of application needs and generate real cost savings.

**Great rip-offs:
Just one way TermiNet[®] 200 printers give you no-waste forms access**

Quality that will make a lasting impression



CIRCLE 95 ON INQUIRY CARD

Mail today to:
J. Walsh,
General Electric
Company,
TermiNet 794-49
Waynesboro, VA 22980.
Telephone: (703) 949-1474.

Send me more information about the expanding TermiNet 200 printer family.

Have a sales representative contact me.

I'm also interested in a TermiNet 200 printer demonstration.

Name _____

Title _____

Company _____

City _____ State _____ Zip _____

Telephone _____

Disc Controller Adapter Allows Double-Density Storage

Using the Doubler™, a double-density disc controller adapter designed for

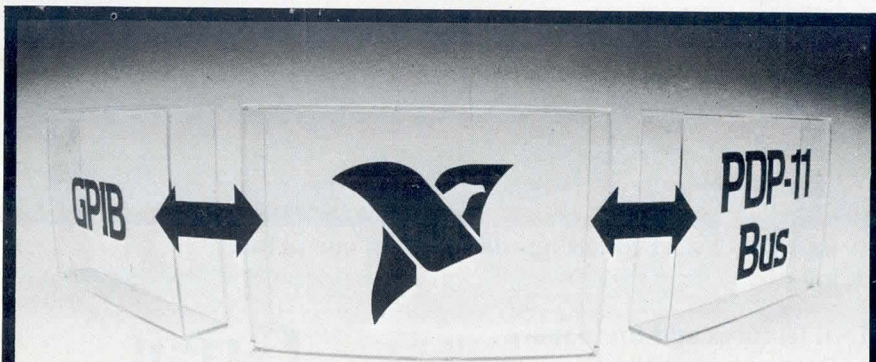
operation with TRS-80 Model I computers, formatted storage of 5.25" (13.34-cm) discs may be increased to 354k bytes. The device, from Percom Data Co, Inc, 211 N Kirby, Garland TX 75042, plugs into the controller chip socket of the computer expansion interface; no circuit modifications are required.

Any 5.25" (13.34-cm) disc drive rated for double-density storage can use the device, as it reads, writes, and formats single- or double-density discs.

Data separator and write precompensation circuits are included.

Designed to operate with the company's DBLDOS™ double-density disc operating system, the controller adapter is compatible with TRSDOS, NEWDOS, and the company's OS-80™ single-density programs without hardware or software changes.

Circle 471 on Inquiry Card



National offers complete PDP-11 Interface systems for your IEEE-488 Bus.

Interface Hardware

National Instruments is an instrumentation specialist in GPIB products. The GPIB11 series of plug-in cards for your UNIBUS™ or Q-BUS™ handles all handshake protocols for controlling and moving data between multiple instruments on the GPIB. Performs talker, listener, controller, system controller and extended addressing functions.

Companion Software

We've developed complete software packages which can be edited to do what you want, in the language you want. Software is provided as MACRO source files for use with FORTRAN, BASIC or MACRO under the RT-11™ and RSX-11™ operating systems. Optional software is available for UNIX™ operating systems. User level calling syntax is identical for all interface cards. We provide full software consultation for all our systems.

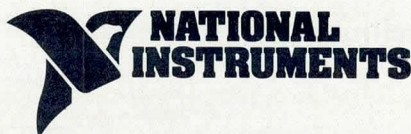
Off-the-shelf Delivery

To provide the best service and quality, our products are available from stock and carry a one year warranty.

Other Products

We also offer the low-cost GPIB-100 Bus Extender and the GPIB-400 Bus Tester.

National Instruments provides complete GPIB Interface packages with full support. For detailed information on products and accessories, contact:



8900 Shoal Creek Building A117 Austin, Texas 78758 512/454-3526

Matrix Printer Affords Multiple Font Selection

Users may select 80, 132, or 136 columns, 6 or 8 lines/in (2.4 or 3.2 lines/cm), with the MQI 150 printer. The device has a speed of 150 char/s, is bidirectional logic seeking, and utilizes a 9 x 9 matrix to produce upper- and lowercase characters with descenders. Accommodating multipart forms up to original plus five copies, from 2 to 15" (5 to 38 cm) in width, other paper handling features include top of form printing, tractor feed, and skip around perforations.



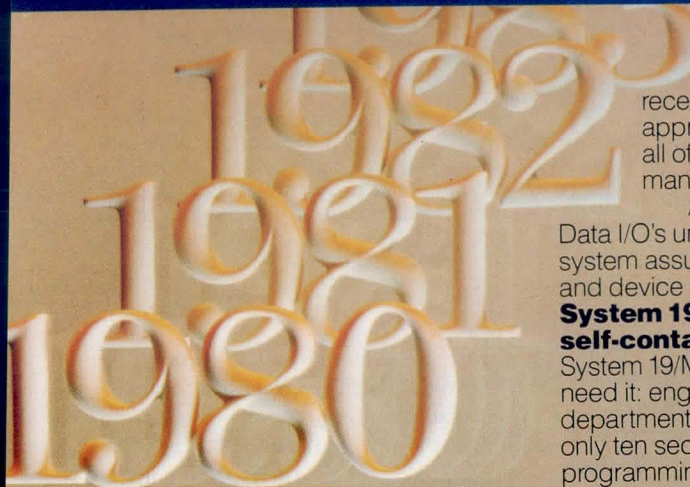
MQI 150 matrix printer. Bidirectional 150-char/s print capability provides upper- and lowercase characters with descenders. Options include 600M-char printhead life, multiple font selection, and IEEE-488 interface

Rated at 100% duty cycle with a minimum head life of 200M characters, the unit is a product of MQI Computer Products, 18381 Bandilier Circle, Fountain Valley, CA 92708. Options include 600M character printhead, multiple font selection, and IEEE-488 interface.

Front panel controls include paper out indicator, line advance, and forms control, as well as an integral self-test feature. Measuring 23 x 8 x 14" (58.4 x 20.3 x 35.6 cm), the unit weighs 28 lb (12.7 kg) and will operate on 110/220 Vac, ±10%, 50 or 60 Hz.

Circle 472 on Inquiry Card

DATA I/O INTRODUCES A UNIVERSAL MOS EPROM PROGRAMMER FOR PEOPLE WHO THINK AHEAD.



System 19/MOS Pak programs all of today's EPROMs and offers plenty of room for future growth. MOS Pak lets you program all currently available EPROMs including the 2704, 2708, 2758, 2508, 2516, 2716, 2532, 2732, 2732A, 2564, 2764, 68764, and the new Hitachi 48016 EEPROM.

And what about the future? Simple software changes to the MOS Pak will enable you to program new devices as they're developed—even if you decide to design a 128K EPROM into your product.

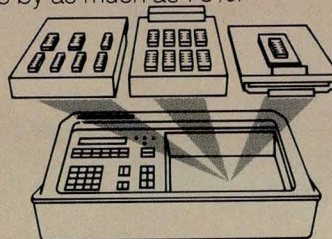
Semiconductor manufacturers' approval provides user security. System 19/MOS Pak is the first "MOS only" programmer to meet the high programming standards set by the

semiconductor industry. Programming algorithms and waveforms have received written approval from all of the manufacturers.



Approval plus Data I/O's unique built-in calibration system assure you of high reliability and device yield. **System 19/MOS Pak is self-contained and easy to use.** System 19/MOS Pak goes where you need it: engineering lab, service department or in the field. It requires only ten seconds to set up and begin programming. Simply key in a four digit code for the particular type of EPROM you want to program. A lighted LED on the MOS Pak will tell you which socket to use.

And the MOS Pak's new programming algorithm for 64K devices can shorten programming time by as much as 75%.



System 19's modular concept incorporates a mainframe and a variety of programming paks.

With the System 19/MOS Pak, Data I/O now offers three great ways to program MOS EPROMs.

- For EPROMs*
- MOS Pak programs single MOS devices
 - Gang Module programs eight EPROMs at once
 - Unipak programs more than 200 MOS and bipolar PROMs
- For individual PROM and logic families*
- More than 40 approved programming paks

Let us show you the future. The Data I/O MOS Pak is available now. To make arrangements for a demonstration or to get your free copy of our MOS programming brochure, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. Phone 206/455-3990 or Toll Free 800/426-9016.



DATA I/O

CIRCLE 97 ON INQUIRY CARD

16-Bit CPU Module Consists of Bit-Slice Processor and Controller

Constructed on two 7.5 x 11" (19 x 28-cm) boards, the TM990/1481 central processing unit consists of a bit-slice processor with major operating registers, and a controller with control memory. The controller memory stores microinstructions that emulate the TMS9900 instruction set and implement additional instructions to enhance integer and floating point arithmetic.

Designed for 5-MHz operation, the CPU includes 94 distinct instructions, including floating point and extended arithmetic. Also included are 15 levels of prioritized and maskable interrupts, memory to memory architecture, 8 different addressing modes, special arithmetic overflow interrupt, 2 programmable interval timers, and 17 interrupt levels.

A product of Texas Instruments, Inc, PO Box 1443 M/S 6404, Houston, TX 77001, the controller also contains the instruction register, clock control logic, RS-232 serial communications controller, and memory speed delay logic to enable the module to operate with different types of memory boards.

Circle 473 on Inquiry Card

Single Board Generates Graphics And Characters

Compatible with Multibus systems, the SBV single-board video interface allows users to switch from text display to graphic representation of data. High resolution black/white graphics and characters approximately four times the size of other processing displays are available at an RS-170 composite video output. Produced by Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070, resolution of the graphic display is 256 x 240 x 1 pixels; memory capacity is 65k bits.

Both upper- and lowercase ASCII characters are generated using a 9 x 7 character matrix in an 8 x 16 cell. Up to 480 characters can be displayed at one time. The interface memory can store two pages of 480 characters at a time. Characters can be inverted or blinked, and vertically scrolled.

Graphic displays can be scrolled horizontally from right to left, which allows a user to pan across a graph or trend plot; fields also can be blanked or inverted. In addition, a lightpen input is provided.

Circle 474 on Inquiry Card

LSI-11 Compatible Chassis Features Dual Tape Drives

Eight quad-size slots, two DEC TU58 cartridge tape drives, drive controller, operator controls, and power supply are provided in the model B04 system chassis. A product of Dataram Corp, Princeton-Hightstown Rd, Cranbury, NJ 08512, the system provides front loading capabilities for tape cartridges and LSI-11 system modules.

Measuring 19 x 7 x 16.5" (48.5 x 17.8 x 41.9 cm), the LSI-11 backplane provides the LSI-11 bus on the A and B, and C and D connectors except for rows six and seven on the C and D side, which have interconnections to allow R101 capability. The system provides 5 Vdc at 24 A and 12 Vdc at 4 A and is switch selectable for 115 or 230 Vac.

Up to 262k bytes, arranged in 512-byte blocks, may be stored in each tape cartridge. Operating with full-duplex, asynchronous 4-wire lines at selectable baud rates of 150 to 38.4k, the controller interface is RS-232-C compatible. An SMU contains all necessary circuitry and controls for operation of the LSI-11. Power sequencing logic, line clock, and operator control interface circuits also are located on the SMU module.

System backplane slots accept any quad- or dual-width device compatible to the LSI-11 bus, including memory and peripheral controllers. Slots 6 and 7 are wired with the LSI-11 bus on the A and B connectors. C and D connectors are wired with the DEC C-D bus.

Circle 475 on Inquiry Card

Test Instrument Offers Microprocessor Signature Analysis Capability

Troubleshooting 6800 type microprocessor based products are facilitated by the HP 5100A microprocessor exerciser through a signature analysis technique even though exercise and signature analysis routines were not initially designed into the product. The unit operates in conjunction with the HP 5004A signature analyzer, also a product of Hewlett-Packard, 1507 Page Mill Rd, Palo Alto, CA 94304.



HP 5100A microprocessor exerciser. When used in conjunction with HP 5004A signature analyzer, troubleshooting 6800 based products to component level is possible. Signature analysis and exercise routines need not be built into tested equipment

Interconnection consists of plugging the product's microprocessor into the unit and plugging the unit's cable into the empty microprocessor socket. The product's buses are then under control of the 5001A, and test stimulus programs from its own ROM are run while a signature analyzer takes signatures at designated circuit points for each test stimulus.

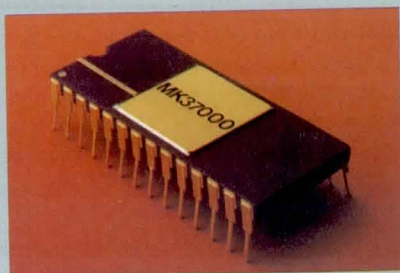
Operating modes include 51 preprogrammed test stimuli for signature analysis troubleshooting of the MPU, ROM, RAM, I/O, buffers, bus lines, and custom test stimulus programs via external ROMs. Other modes are single signature tests, bus signature output, qualify input, and gating signal outputs for a signature analyzer.

Circle 476 on Inquiry Card

64K BYTEWYDE ROM

MK37000: 4 to 1 density
upgrade expands RAM, ROM,
EPROM interchangeability
options.

MOSTEK®



Perhaps the best way to characterize the MK37000 is to think of it as everything you want in a 64K ROM. Because that's exactly what it has.

Fast access - 250ns (max).
Low power - 220mW (max) active
and just 35mW (typ) standby.
Quick, efficient prototype cycling
and code processing.
And of course, volume

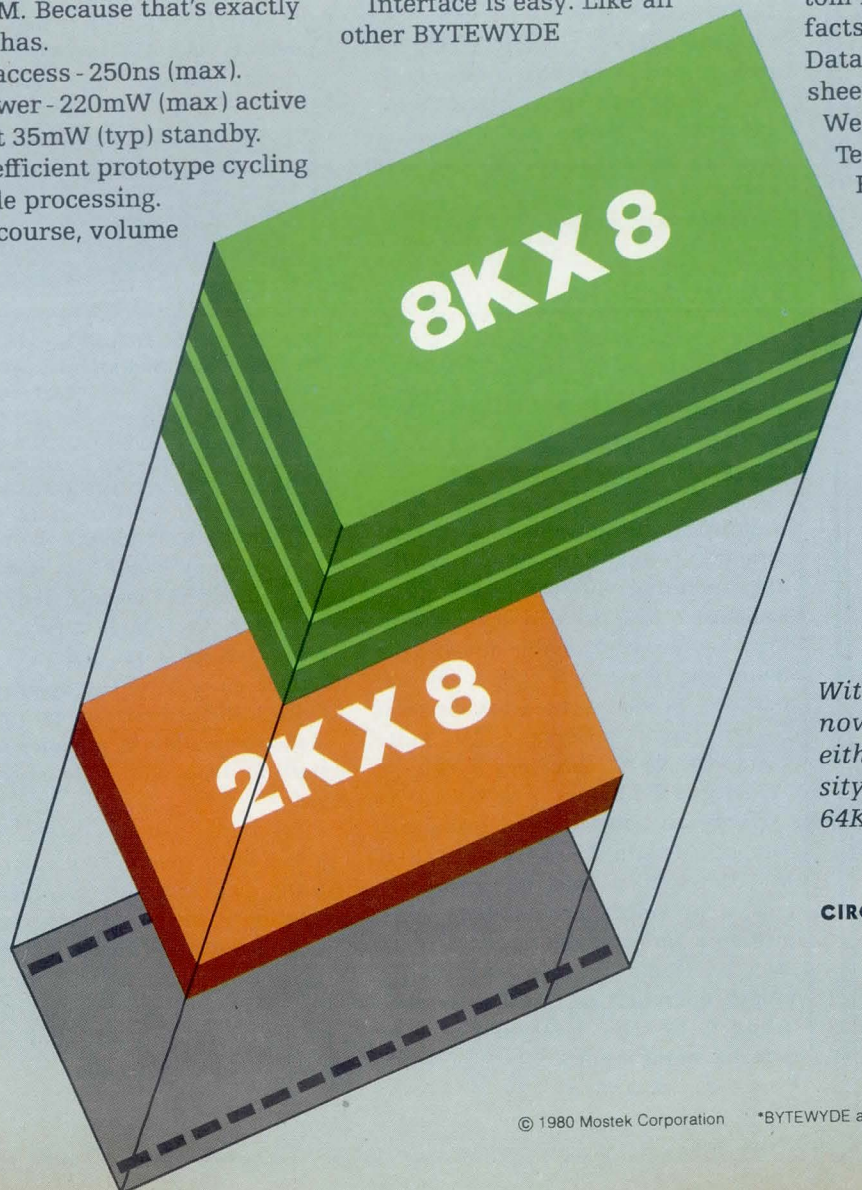
availability, supported by 2½ years of production experience at the 64K level.

But that's only part of the story. This 28-pin JEDEC-approved package and pinout is also fully compatible with the Mostek* family of n-words x 8 BYTEWYDE* memories. So now you'll only need one matrix of 28-pin sockets to design or upgrade a compact 8K, 16K or 64K array of RAMs, ROMs/EPROMs.

Interface is easy. Like all other BYTEWYDE

memories, the MK37000 interfaces directly with all present and future generation 8-bit and 16-bit microprocessors. An Output Enable control provides easy user control of the bus in all bus configurations. Together, the Output Enable and the Chip Enable control functions also prevent any bus contention problems.

If you want to simplify and streamline the design of your custom memory arrays, get all the facts. Ask for the BYTEWYDE Data Book and the MK37000 data sheet by contacting: Mostek, 1215 West Crosby Road, Carrollton, Texas 75006 (214) 323-1000. In Europe, contact Mostek Brussels, 660.69.24.



Within the BYTEWYDE family you now have a wide choice of ROMs: either a 16K ROM or a 4 to 1 density upgrade with the MK37000 64K ROM.

CIRCLE 98 ON INQUIRY CARD

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MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

Impact Printer Has User Defined Character Set

Five print densities, from 72 to 132 char/line, and 15 selectable baud rates, 75 to 19.2k, are available on the model 800 impact printer from Base 2, Inc, PO Box 2076, Yorba Linda, CA 92686. Up to six different character sets may be selected under program control; two are standard, one may be downloaded from a host, and three additional sets are available as options.

I/O provisions included are RS-232, 20-mA loop, IEEE-488, and Centronics type parallel. Using a 7-wire dot matrix, the device provides bidirectional capability with 96 ASCII characters in a 5 x 7 format. Options include a programmable stepper motor that provides high speed paper advance and dot-resolution graphics, tractor feed, and 1920 character buffer.

Circle 477 on Inquiry Card

DEC Compatible Disc System Has User Oriented Features

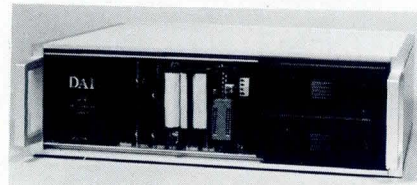
Built-in hardware bootstrap, diskette formatting, and onboard diagnostics are included in the DEC RX02-compatible disc drive system. Featuring a double-sided, double-density configuration, the two 8" (20.3-cm) disc DSD 470, produced by Data Systems Design, Inc, 3130 Coronado Dr, Santa Clara, CA 95051, provides a storage capacity of 2M bytes.

Hardware, software, and media are compatible with LSI-11 systems, and LSI-11/23 multiple level interrupt support is provided. System diagnostics include a series of microprogrammed user selectable routines that verify proper operation of the disc system, debug to the chip level, and provide detailed status reports.

Circle 478 on Inquiry Card

Microcomputer Operates In Industrial Control And Software Development

Modular construction permits the DSK industrial computer system to function in industrial control applications and as an 8080/8085 software development station. A product of Data Applications International, Dreve des Renards 6, Bte 8, 1180 Brussels, Belgium, the system is housed in a standard 19" (48-cm) eurobox and includes two minifloppy disc drives, disc controller card with P/R0M-resident disc operating system, up to 60k bytes of RAM, and 2708 or 2716 EPROM programmer card. Also included are power supply module with battery backup, interfaces to a serial terminal, parallel printer, and paper tape reader/punch.



DSK industrial microcomputer system. Including two minifloppy drives, system may be used as industrial control application or software development station. In programming development phase, interface modules may be inserted directly into eurobox enclosure

Modular architecture is based on the company's DCE-BUS and can be configured for specific requirements by using the single-eurocard microcomputer, memory, and industrial interface modules of the DCE family. An automatic hardware bootstrap feature makes low address memory locations starting from zero available to the user.

Standard system software includes text editor, macro assembler, and a utility package that provides debug functions, including program trace with automatic display of all CPU registers after each instruction execution. The system supports the company's realtime BASIC and FORTRAN programming languages.

Circle 479 on Inquiry Card

Single-Board μ Computer Includes 64k Bytes Of Dynamic RAM

Console configurations for the NOBUS-Z microcomputer system include keyboard and TV receiver or integral keyboard/display terminal. Featuring a Z80A CPU, CP/M operating system, 64k-byte dynamic RAM, dual-density 8" (20.3-cm) disc drives with 600k bytes/side, and 6k-byte color text/graphics capability, the single-board LSI system provides business and scientific capabilities.

Available software in BASIC, FORTRAN, Pascal, COBOL, APL, and PL/I includes integrated business, engineering, and word processing systems. Utilities included are disc formatter, single disc copy, diagnostics, and graphics support. Up to four disc drives may be supported for a double-sided, double-density 4M-byte storage capacity.

Eight graphics modes provide 64 x 64 elements in four colors, lowest resolution; 256 x 192 elements in two colors, highest resolution; and 16 rows of 32 columns of mixed text and 8 color semi-graphics. Additional features included from Exo Electronics Co, PO Box 3571, Culver City, CA 90230, are two serial and two parallel I/O ports, four counter/timers, and an onboard sound generator.

Circle 480 on Inquiry Card

Expander Cards Increase Channel Capacities of Analog Input Boards

Fully DEC compatible, three dual-height expander cards plug directly into LSI-11 or LSI-11/2 backplanes. Products of Data Translation, Inc, 4 Strathmore Rd, Natick, MA 01760, the cards provide up to 64 single-ended or 32 differential analog input channels when used with the company's DT2760 series of analog input systems. Each board includes required control logic

and break-before-make new channel selection circuitry and exhibits LSI-11 Q-bus compatibility.

Model DT2772 extends the company's DT2762 high level input analog interface board from an original 16 single-ended (SE) or 8 differential input (DI) channels to 64 SE or 32 DI channels. To the same degree, model DT2774 extends the DT2764 low level wide range analog interface board. Both cards maintain full specified performance for maximum input signal to ± 10.5 V and can withstand up to a ± 30 V input. Off channel resistance is in excess of 100M Ω , and both boards are available with a 4- to 20-mA (-M) input option.

Model DT2775 extends the DT2765 flying capacitor isolated low level interface board from four DI channels in eight channel increments for each expander board. Up to seven boards may be combined to provide a maximum of 60 DI channels, each capable of resolving 10-mV to 10-V full-scale input signals in the presence of ± 250 V of common mode voltage.

Circle 481 on Inquiry Card

Modular Design Promotes Rapid System Configuration

Consisting of 54 plug-in cards for CPU, timing, memory, digital and analog I/O, and communications, the DACS 5000 system is built around Cyberbus, a structure developed by Cybersystems, Inc, 8300 Whitesburg Dr, Huntsville, AL 35802. Power supply and front panel also plug into the bus, providing flexible system configuration and troubleshooting capabilities. Each 4.5 x 6.4" (11.43 x 16.51-cm) card plugs into one of 18 available card slots in the 19" (48-cm) wide card cabinet.

Features of the 72-line bus system include 16-bit data bus, DMA, vectored interrupts, and memory mapped I/O. Basic systems include CPU, 2k EPROM, 32k static RAM, and interfaces to all system peripherals. CPU configurations include 6502, 6802, 6909, Z80, and 8085. A complete line of peripherals and software is available.

Circle 482 on Inquiry Card

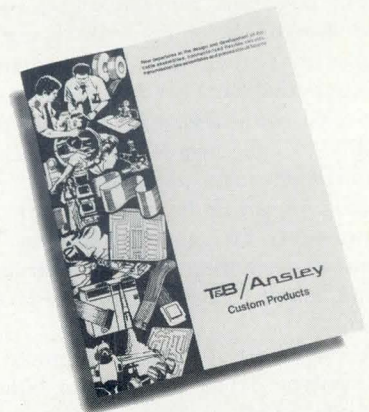
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SOFTWARE

Development Tools Expand 8086 and Z8000 Support

Microprocessor development tools from Tektronix, Inc, PO Box 500, Beaverton, OR 97077, for the company's 8002A MDL have been expanded to include assemblers for the 8086/8088 and Z8002 microprocessors and prototype debug packages for the iSBC 86/12A and Zilog Z8000 development module single board computers (SBC). Each assembler package consists of a core assembler manual and an assembler manual insert for the specific microprocessor, reference card, and floppy disc with the assembler, linker, and editor.

The assembler converts source code into executable object code using a source file that has been created through the 8002A's editing software. Included with the assembler is the ability to call macros through easily identifiable name parameters and inclusion of an indefinite number of arguments. String manipulation is allowed, including use of varying string lengths inside and outside of macros.

A second set of software products is a prototype debug package for either the iSBC 86/12A or Z8000 development module. This package allows an absolute object code or a linked file to be transferred from the 8002A to the SBC, and then executed under the control of debug software. Execution can take place in real time with predetermined breakpoints or in single steps. Contents of the SBC memory and processor registers may be examined during debugging. Each debug package consists of a user's manual, reference card, two 2716 EPROMs, which contain the onboard monitor, RS-232 cable, and floppy disc with additional monitor software and system programs.

Circle 483 on Inquiry Card

Operating System Also Functions as Programming Language

Intended to operate with STD BUS or PC44 BUS Z80 systems that use the 4301 diskette controller and IBM 3740 format diskettes, AFORTH is a dictionary oriented system available from Applied Micro Technology, Inc, 1842 W Grant Rd, Tucson, AZ 85705. Working simultaneously as the operating system and programming language, programming elements as fundamental as DO, LOOP, IF, or ELSE are definitions in the dictionary.

A linked list of named commands referred to as definitions comprise the entire system. Any definition may be executed at any time by typing the definition name at a terminal. New definitions may be added to the dictionary at any time, and all definitions are entered on a completely equal footing with all other definitions. A new command can be defined in terms of assembly language or composed of references to other definitions.

Other features of the system include resident memory, a re-entrant code, which permits several programs to execute the same definition residing in EPROM, and multitasking, math, virtual memory, and graphics packages. The system is available in 5.25" (13.34-cm) or 8" (20.3-cm) IBM 3740 format diskettes or in 2716 EPROM form and includes full documentation.

Circle 484 on Inquiry Card

FORTRAN Compiler Increases UCSD System Capabilities

Designed to operate with the UCSD system software package, FORTRAN-77, a FORTRAN compiler from Softech Microsystems, Inc, 9494 Black Mountain Rd, San Diego, CA 92126, facilitates program development on a variety of microcomputers.

Fully compatible with UCSD Pascal, portability of programs among most

microcomputer systems is said to be assured. Systems based on the 6502, 6800, 6809, 9900, Z80, 8080, and LSI-11 microprocessors can use the compiler.

Use of the UCSD system and FORTRAN compiler permits screen editing, random accessing of disc files, separate compilation of individual program modules, cross assembly, linkage of assembly language routines with Pascal and FORTRAN modules, and interactive I/O.

Language utilized for the computer is the ANSI-77 version of FORTRAN. Programs developed with the UCSD system are compiled into a universal pseudo-code (P-code) that can be executed using the UCSD system interpreter and operating system. This technique allows the same program to run on many microcomputers without change and permits hardware change without sacrificing software usability.

Circle 485 on Inquiry Card

Software System Produces Automatic Program Improvements

Constructed to remove remarks, spaces, or both from programs, as specified by the user, PACK8 is said to reduce program size by as much as 40%. The program is designed to operate on the TRS-80, model I, with 32k- or 48k-byte memory, and a single-disc drive. Operating on blocks of strings, size of the program to be compacted is limited only by disc space availability.

All lines in a program can be compacted, or the user can specify a block of numbers, inclusive, to be packed. At the end of the packing process, a summary is presented of the number of bytes and lines in the original program and in the packed version. The packing fractions are also computed and shown in the program from Data Associates, Box 882, Framingham, MA 01701.

Circle 486 on Inquiry Card

SOFTWARE

**Application Software
Available for OASIS
Operating System Users**

Financial, industrial, and specialized application system software written in COBOL is intended for computer systems that utilize the OASIS operating system. Each software package requires a minimum of 64k bytes of memory and is available on diskette or tape cartridge from American Business Systems, 439 Littleton Rd, Westford, MA 01886.

Included in the financial application system are order entry/inventory control, accounts payable, accounts receivable, general ledger, and payroll modules. All are designed to operate as standalone modules on limited memory floppy disc based hardware configurations, but the five modules run as an integrated system using the larger capacity of hard disc storage.

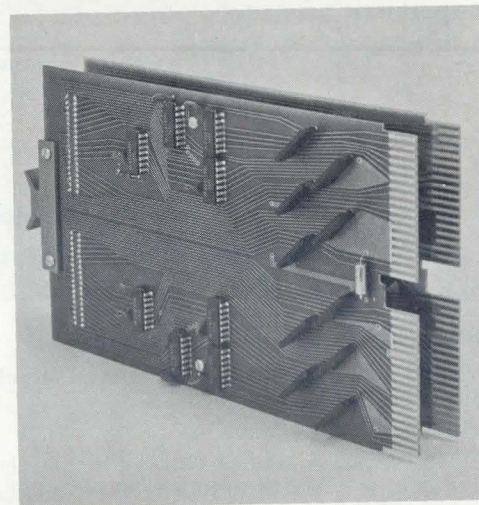
Industry application systems include three modules. A real estate system provides property listing, client/listing correlation, and financial processing aids to brokers. A construction job management system is an integrated system that manages complete job costs, work orders, and change orders associated with multiple ongoing projects while interacting with accounts receivable, accounts payable, payroll, and general ledger portions of the system. A client accounting system is a fully automated package for maintaining complete business records and features a report writer to allow users to create financial reports.

The specialized application system is composed of two packages. A financial modeling system produces projections and forecasts with the level of detail and complexity defined by the user. A correspondence management system utilizes word processing functions for the creation of mailing lists, proposals, and mailers.

Circle 487 on Inquiry Card

Unibus* repeater for PDP11 series systems.

Do you need to add peripherals or additional cable lengths to an overloaded bus? Do you have unknown system crashes such as caused by a type 4 trap — delayed response from a slave sync? Is your current repeater too slow for your current system?



If these questions are relevant, then Datafusion Corporation has a device that can answer your needs, the OSB11-A Bus Repeater. It is a functional equivalent of DEC's* DB11-A, and is designed to drive at least 19 bus loads and 50 foot of bus cables.

Ultra Fast: 80 nanoseconds MSYNC to return SSYNC maximum (40 nsec one way). This is due, primarily, to the specially designed patented integrated circuit employed by the OSB11-A.

Reliable: Only 34 operational circuit components. Tested in environments from 0° to 70°C with virtually no degradation of signal quality.

Easy to Install: Remove a M920 Jumper and replace it with a OSB11-A. No extra system unit is needed; no wires or plugs to connect (or disconnect); no lost time in reconfiguration.

Available: Off-the-shelf. And, it's fully supported and warranted.

Cost: About 25% below DEC.* Quantity discounts are available.

Other PDP11 products available are a Busrouter (a Unibus* Switch) to reconnect multiple peripherals to one or more PDP11 cpu's, a Unibus* Cable Tester, and an Associative File Processor for high speed text search — a hardware approach.

We also have some ideas for the application of our products which might not have occurred to you. If you can't get the performance that you would like from your PDP11 system, maybe we can help. Telephone our marketing Manager at (213) 887-9523 or write to Datafusion Corporation, 21031 Ventura Boulevard, Woodland Hills, California 91364.



*TRADEMARK OF DIGITAL EQUIPMENT CORPORATION

SOFTWARE

Software Package Adapted to Include Additional μ C Systems

Speeding up and simplifying repetitious calculations through an interactive display is accomplished by VisiCalc, available for Commodore PET and CBM 8032 and Atari 800 systems. The product creates a matrix display arranged as 64 columns wide and 254 rows high.

Operationally identical to the Apple II version, the Commodore version automatically senses whether it is running on a PET machine with 40-character wide screen or on a CBM 8032, which has a screen that is 80 characters wide.

Each package from Personal Software, Inc, 1330 Bordeaux Dr, Sunnyvale, CA 94086, contains an instruction manual that includes a step by step tutorial for first time computer users. Also included is an expanded reference section organized by program feature to aid experienced users. Circle 488 on Inquiry Card

LISP Programming Language Offers System Adaptability

LISP is a programming language developed for artificial intelligence applications but is also used in interactive database and natural language systems, symbolic manipulations of mathematical expressions, control, and computer aided design functions.

From Cromemco, Inc, 280 Bernardo Ave, Mountain View, CA 94043, the language is available on 5.25" (13.34-cm) or 8" (20.3-cm) diskette for the company's Z80 based systems. The language incorporates standard control constructs, complete string and character processing capabilities, fixed and floating point arithmetic, a full complement of property list functions, and the capability of interfacing with non-LISP procedures.

Also included is a virtual storage capability in which an autoloader feature permits infrequently used functions and symbols to be stored on disc, allowing larger user programs. Comprehensive error trapping capabilities are also incorporated.

Circle 489 on Inquiry Card

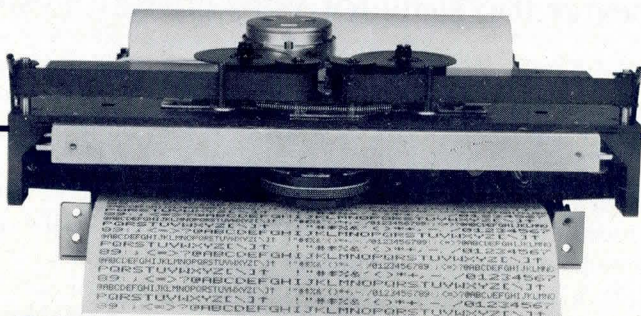
Statistical Package Utilizes Machine Graphics Routines

Curve fitting, probability, general statistics, distribution mathematics, and test statistics, along with a scientific data management system are included in a package for the TRS-80, Level II, Apple II, and Apple II Plus computers. A product of Charles Mann and Associates, Micro Software Div, 7594 San Remo Trail, Yucca Valley, CA 92284, the system requires 32k bytes of RAM and a minimum of one disc drive.

Capable of handling up to five 100 x 1 matrices containing raw data, grouped data, or frequency arrays, a quick reference chart of legal variables is also included. A built-in data base is available to produce a complete set of working examples useful in learning statistical principles.

System probability elements include analysis for permutations, combinations and factorials, and random number tables, random numbers within intervals, or one by one for game theory. Distributions include binomial, Poisson, normal, chi-square, and student t-distribution.

Circle 490 on Inquiry Card



Our Printer's Strength Of Character Is Enhanced By Its Self-Control


Don't let the low price tag fool you; our DMT-6 μ P is stronger on capabilities than any printer in its class. Its unique matrix impact print head lets you program any desired character pitch. You can print data or text, single-stroke or enhanced from 36 to 132 columns. And, print up to four copies without adjustment on standard 8 1/2" roll paper, fan-fold forms and labels.

What's more, it packs a built-in controller that includes all needle drivers and diagnostic routines, while providing a choice of interface functions-parallel ASCII, RS-232C/I-Loop, or switch-selectable baud rates from 110 to 1200. Now that's self-control worth having! Add the continuing economy of a 10-million character life ribbon and re-inking rollers, and you've got an unbeatable buy. Call or write for details. Ask for Bulletin 922A.



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CIRCLE 103 ON INQUIRY CARD

DS BRIEFS

Bus Control Unit Provides Flexible Interface for LSI-11—Operating as a bus controller, multiple remote terminal, or bus monitor, the BCU-11LA is bit slice microprocessor based. Available from SCI Systems, Inc, PO Box 4000, Huntsville, AL 35802, the two, quad-wide plug compatible cards contain microprogrammed DMA capability and self-test diagnostics. Circle 550 on Inquiry Card

One Board Holds up to 512k Bytes—From 32 to 512k x 9 bytes are available on the CI-8086 memory module from Chrislin Industries, Inc, Computer Products Div, 31352 Via Colinas #102, Westlake Village, CA 91361. Multibus compatible, the module employs onboard refresh logic and operates with both 8- and 16-bit systems. Circle 551 on Inquiry Card

Comprehensive Graphic Display Capability Offered in Desktop Microcomputer—Bar and pie charts, histograms, and complex point to point plots can be displayed on the model 900 Commander microcomputer from Columbia Data Products, Inc, 9050 Red Branch Rd, Columbia, MD 21045. Included in the system are 9" (22.9-cm) CRT and 512 x 256 resolution vector graphics. Circle 552 on Inquiry Card

Single-Board Microcomputer Features All CMOS Circuitry—Model SBC-6100 includes 2k of EPROM, 1k of RAM, memory expansion and DMA controller, realtime clock, and 20-bit programmable parallel I/O port. Power requirements for the board from Eagle Research Corp, Ste 5, Municipal Parking Bldg, Charleston, WV 25301, are 5 Vdc at less than 60 mA. Circle 553 on Inquiry Card

I/O Port Includes User Selectable Device and Interrupt Addresses—A product of General Robotics Corp, 57 N Main St, Hartford, WI 53027, the DRV11 is a general purpose parallel I/O port fully compatible with LSI-11 applications. Standard features include individual 16-bit connectors, handshaking logic, and a 40k word/s data transfer rate. Circle 554 on Inquiry Card

Graphic Display Board Provides Software Selectable Video—Video, graphic video, or both for PET computers is provided by the K-1008-6 PET graphic interface board. Included on the board from Micro Technology Unlimited, PO Box 12106, Raleigh, NC 27605, are five ROM sockets with software selectable enable. The board serves as an 8k-byte memory expansion when not used for graphics. Circle 555 on Inquiry Card

Memory Board Includes Onboard CPU—Utilizing 16k bytes of static RAM and sockets for eight 2716 EPROMs, the Multibus compatible IM-1680 intelligent memory board features onboard Z80 CPU. Produced by Microsignal, 3704 State St, Ste 214A, Santa Ana, CA 93105, the board can be used as regular memory or the Z80 may be activated under program control to process data in parallel with the Multibus master. Circle 556 on Inquiry Card

Power Supply Permits Orderly Emergency Shutdown—Up to one hour of emergency power can be provided to Apple II users by Apple-juice™, a reserve power supply system from High Technology, Inc, PO Box 14665, Oklahoma City, OK 73113. The supplies provide visual and audible warning during power flickers, temporary failures, and prolonged outages. Automatic power transfer and supply reset are provided. Circle 557 on Inquiry Card

Multibus Compatible Chassis Holds Eight Boards—Capable of holding up to eight Multibus boards, the IMC-400 Multibus chassis includes dual 110 ft³ (3 m³)/min fans, a temperature detection and interrupt generation circuit, line frequency clock, and linear power supplies. The chassis, from Rela Systems, Inc, 1322 Arapahoe Ave, Boulder, CO 80302, mounts on the backplate of NEMA type industrial enclosures. Circle 558 on Inquiry Card

RAM Board Offers Flexible Byte Size—Either 64k 16-bit or 128k 8-bit bytes are provided on the ZX-028A RAM board. Zendex Corp, 6398 Dougherty Rd, M/S 32, Dublin, CA 94566, includes provisions for 64 5-V only or 3-supply RAMs. An 8-position DIP switch allows deselect and depopulation of the board in 16k-byte increments and a rotary switch selects one of eight double address segments. Circle 559 on Inquiry Card

Evaluation Package Is Designed for Single Task Applications—PicoFORTH™, a subset of polyFORTH™, is designed for interactive evaluation of a single task application. FORTH, Inc, 2309 Pacific Coast Hwy, Hermosa Beach, CA 90254, has included in its complete operating system a polyFORTH assembler, compiler, text interpreter, editor, and disc utilities. Circle 560 on Inquiry Card

Utility Program Facilitates Medium Transferral—Disk-o-tape, a utility program from Dan McCreary, Box 16435-V, San Diego, CA 92116, is designed to transfer an entire disc's data to cassette tape and back again. Intended to run on an Apple II or Apple II Plus, the program requires 32k bytes of RAM and provides true read after write verification. Circle 561 on Inquiry Card

Multimemory Board Adapts to User Requirements—Memory type is independently configured by a header for each socket such that the Multibus compatible Multimemory board can contain both static RAMs and EPROMs or ROMs and static RAMs. Each of the boards from Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070, can operate with only one socket filled. Up to 16 24-pin memory devices may be accommodated. Circle 562 on Inquiry Card

Low Cost Data Storage Utilizes RS-232 Port—Designed to store up to 80k bytes of RS-232 formatted data, Micro-Sponge from Exatron, 181 Commercial St, Sunnyvale, CA 94086, buffers up to 1k in internal RAM. Jumper selectable baud rates available are 300, 1200, 9600, and 76,800. Transfer time at 9600 baud is 4.5 s for 5.3k bytes. Utilizing the company's stringy floppy wafer (consisting of a continuous loop tape cartridge), 5.3k-byte blocks of data may be stored on 5' (1.52-m) increments of tape. Circle 563 on Inquiry Card

Rack Mountable, Complete LSI-11 Computer Systems Packages Are Available—LSI-11/2 or -11/23 systems can include 32k to 128k of memory, dual floppy disc system, 21M-byte Winchester drive, quad serial interface, tape backup, and RT-11, RSX-11, or UNIX (U/V6) software. Each of the components also is available as a stand-alone peripheral from Charles River Data Systems, Inc, 4 Tech Circle, Natick, MA 01760. Circle 564 on Inquiry Card

DS BRIEFS

Microcomputer Down-Loader Facilitates Program Final Debugging—Programs developed on the SPRINT 68 microcomputer may be automatically down-loaded to a target system using the approach from Wintek Corp, 1801 S St, Lafayette, IN 47904. A switched RS-232 cable assembly and diskette containing the software comprise the system. Circle 565 on Inquiry Card

Flexible Cable Assembly for PDP-11 Available in Custom Lengths—Supplied completely terminated and tested, single-layer cables are designed for use with PDP-11 computers with UNIBUS interface, and include strain relief and card-puller handles. A product of T & B/Ansley Corp, 3208 Humboldt St, Los Angeles, CA 90031, the highly flexible cables reduce cable thickness and decrease space requirements. Circle 566 on Inquiry Card

11-MHz μ C Increases System Speed—An 11-MHz 8048 single-chip microcomputer provides the user with a less expensive solution to upgrade system speed. Internal ROM capability for the device from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, ranges from 1k for the INS 8048 to 4k for the 8050.

Microprocessor Board Functions as CPU or Intelligent Disc Controller—Composed of Z80A, two parallel and two serial ports, double-density floppy disc controller, 8k memory capacity, and 2716 chip, the FDC-1 accommodates three 5.25" (13.34-cm) or four 8" (20-cm) drives. A product of Teletek, 9767F Business Park Dr, Sacramento, CA 95827, the board may be configured as a CPU in an S-100 or as a smart controller. Disc operating systems available include CP/M, FAMOS, and OASIS. The board reads single- and double-density IBM 3740 or System 34 formats. Circle 567 on Inquiry Card

Card Cage Provides for Forced Air Cooling—Series 126/F prototype systems can hold up to 11 cards at 0.6" (1.52-cm) spacing and includes decoupled power buses. Prototek, Inc, PO Box 46512, Cincinnati, OH 45246, designed the card cage to accept two 3.125" (7.94-cm) fans to be mounted on threaded standoffs. The Multibus compatible backplane provides for either bused or wirewrap options. Circle 568 on Inquiry Card

Quad-Output Power Supplies Mate with Card Cages—Compatible with iSBC, iCS, and BLC modules, CP640/CP665 power supplies have input/output connectors that mate with card cage assemblies. From Deltron, Inc, PO Box 1369, North Wales, PA 19454, the supplies operate on 115/230 Vac, and include overvoltage and current limiting as well as power failure sense and signal circuitry. Circle 569 on Inquiry Card

Development Tool May Be Used as Single-Board Computer—CONCEPT-48, offered in two models, may be used as a development tool or as a tutorial device. Based on the 8048 CPU, model 6942 from Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014, includes CPU, keyboard, LCD display, ROM based monitor, serial I/O port, and programming/debug capabilities. The tutorial system has limited memory and no serial I/O. Circle 570 on Inquiry Card

EPROM Programmer Implements All Programming Algorithms—Utilizing scrambler plugs to customize the single Firedrake™ 3000 40-pin socket, the device accommodates many industry standard EPROMs while permitting total software programming control. The 8048 based system is a product of Microcomputer Applications, PO Box E, Suisun City, CA 94585, and interfaces to CRT or computer system via an RS-232-C connector. Circle 571 on Inquiry Card

Data Collection Software Offers Comprehensive Capabilities—Features such as data security, realtime editing, validation, and table lookups are provided in the Micro/Data data entry software system from the Minicomputer Div of Data Communications Corp, 3000 Directors Row, Memphis, TN 38131. Hardware includes MP100 CPU, display/keyboard, dual-floppy drives, and 60-char/s printer. Circle 572 on Inquiry Card

Multifunction CPU Board Addresses up to 1M Byte—Featuring 2-MHz operation, 1k of RAM, onboard EPROM monitor, and space for up to 20k of EPROM, the 6809 based SCB-69 can be used as a dedicated microcontroller, business processor, or single-board computer. Smoke Signal Broadcasting, 31336 Via Colinas, Westlake Village, CA 91361, has included realtime clock, battery backup, and programmable interrupt generating capability. Circle 573 on Inquiry Card

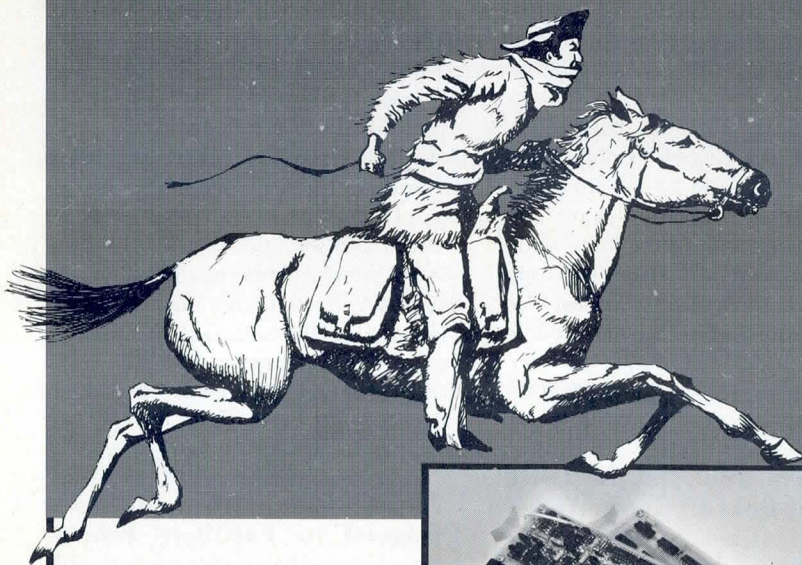
Adapter Provides GPIB-488/TRS-80 Interface—Any TRS-80, model 1, with 16k of RAM and Level 2 BASIC may be utilized as a 488 controller by using the 488-80B interface adapter. Produced by Scientific Engineering Laboratories, 11 Neil Dr, Old Bethpage, NY 11804, the device includes a machine-level driver program, on tape or disc, which interacts with Level 2 and 3 BASIC and Disc BASIC. Circle 574 on Inquiry Card

STD BUS-Compatible Modules Designed to Facilitate Emulation—Consisting of three MSI boards from Microcomputer Systems, Inc, 1814 Ryder Dr, Baton Rouge, LA 70808, the STD BUS series includes the 8088 based 7888 CPU, 7550 I/O and interrupt, and 7880 CPU. The 7888 CPU can accommodate up to 8k of P/ROM and 4k of RAM. The 7550 provides a flexible interface, and the 7880 is a 8080A based version of the 7888. Circle 575 on Inquiry Card

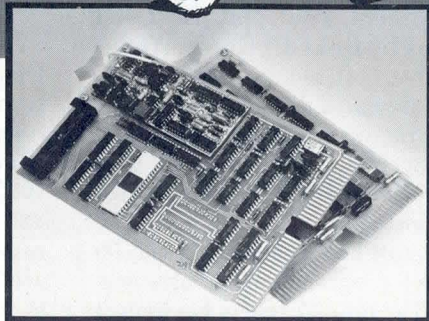
Pascal Availability Increases Program Development Capabilities—Available to operate with the C8001 microcomputer system designed by Onyx Systems, Inc, 10375 Bandlely Dr, Cupertino, CA 95014, the Pascal operating system includes 2 editors (screen and line oriented), compiler, Z80 assembler, and a file handler. Disc data may be backed up to tape using this software system. Circle 576 on Inquiry Card

Emulator Modules Permit Functional Software System Checks—Intended to provide pin for pin emulation of the S2150 single-chip microcomputer from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, the SES 2150 contains 2k bytes of EPROM. Provision for operation from a separate power supply decreases the possibility of distorting a prototype system's characteristics. Circle 577 on Inquiry Card

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MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

Development System Features ROM Emulator and Logic Analyzer—2900 series bit slice and other high speed microprogrammed processors can utilize the DS200, a product of Hilevel Technology Inc, 14661 Myford Rd, Tustin, CA 92680. ROM emulation can be expanded to 16M bits, and a 16-bit address trace and up to 64 channels of data trace are available. Circle 578 on Inquiry Card

Microprocessor Power Supply Features Dual Output—Outputs available from the μ PS series are 5 to 24 Vdc at up to 15 W/output. Elpac Power Systems, 3131 S Standard Ave, Santa Ana, CA 92705, provides a remote sense feature on some models, isolated outputs for positive or negative operation, short circuit and current limiting capabilities, and 115/230-Vac operation. Circle 579 on Inquiry Card

P/ROM Programmer Module Provides Check, Read, and Verify Functions—Data load, verify and dump, and object code edit functions are included in the A65-901 module from Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803. Designed as a plug-on peripheral for the AIM 65, the module includes 1k of R2114 static RAM. Circle 580 on Inquiry Card

Multichannel Video Controller Board Provides Display Versatility—Use of the MCV-1023 allows intermixable text and graphics, three software selectable character fonts, and user defined custom characters. A product of Metacomp, Inc, 7290 Engineer Rd, San Diego, CA 92111, the board interfaces user systems through the use of programmed I/O and a shared 2k-byte block of addressable RAM. Circle 581 on Inquiry Card

Quad-Size Disc Controller Has LSI-11 Compatibility—Produced by Dilog, 12800-G Garden Grove Blvd, Garden Grove, CA 92643, model DQ202 interfaces two 8" (20-cm) or 14" (36-cm) drives with SMD interface. Contained in one card slot, without external circuitry, power, or chassis, the board runs RT-11, RSX-11, and RSTS operating systems. Drives handled may be of different types with different storage capacities. Circle 582 on Inquiry Card

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DIGITAL SIGNAL PROCESSING SYSTEMS MOVE TO FLOATING POINT ARITHMETIC— PART 2: IMPLEMENTING 32-BIT MULTIPLICATION

Louis Schirm IV

TRW LSI Products

2525 E El Segundo Blvd, El Segundo, CA 90245

Dynamic range requirements of applications such as speech recognition have spurred the trend toward greater use of floating point arithmetic in digital signal processing systems. Part 1 of this series (*Computer Design*, Aug 1980, pp 156-160) describes the background behind this trend; this month's discussion presents hardware details of implementing a 32-bit floating point multiplication system.

In this multiplication system (see block diagram, Fig 1), interface registers accept and store the 32-bit multiplier (X) and multiplicand (Y). The 8-bit exponents are sent to the exponent accumulator where the new exponent is calculated. Multiplication of the mantissas, a 24- x 24-bit operation, is performed by a multiplier circuit. This multiplication utilizes a summation of partial 12- by 12-bit products, as

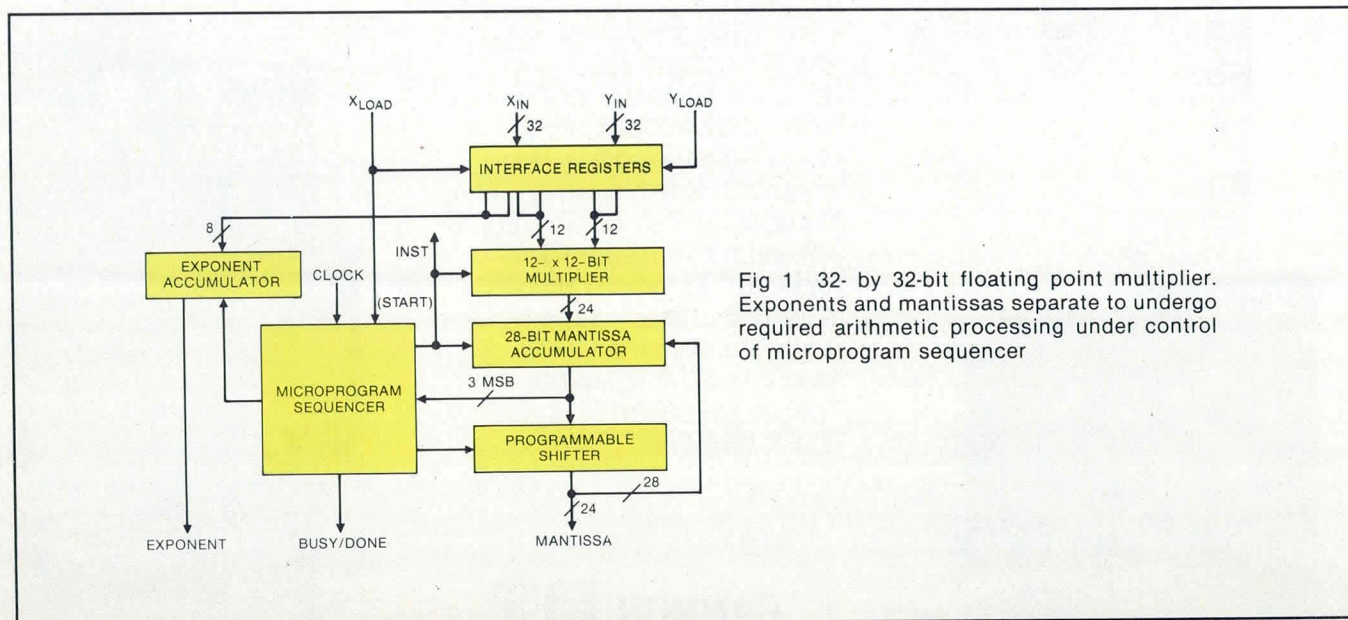
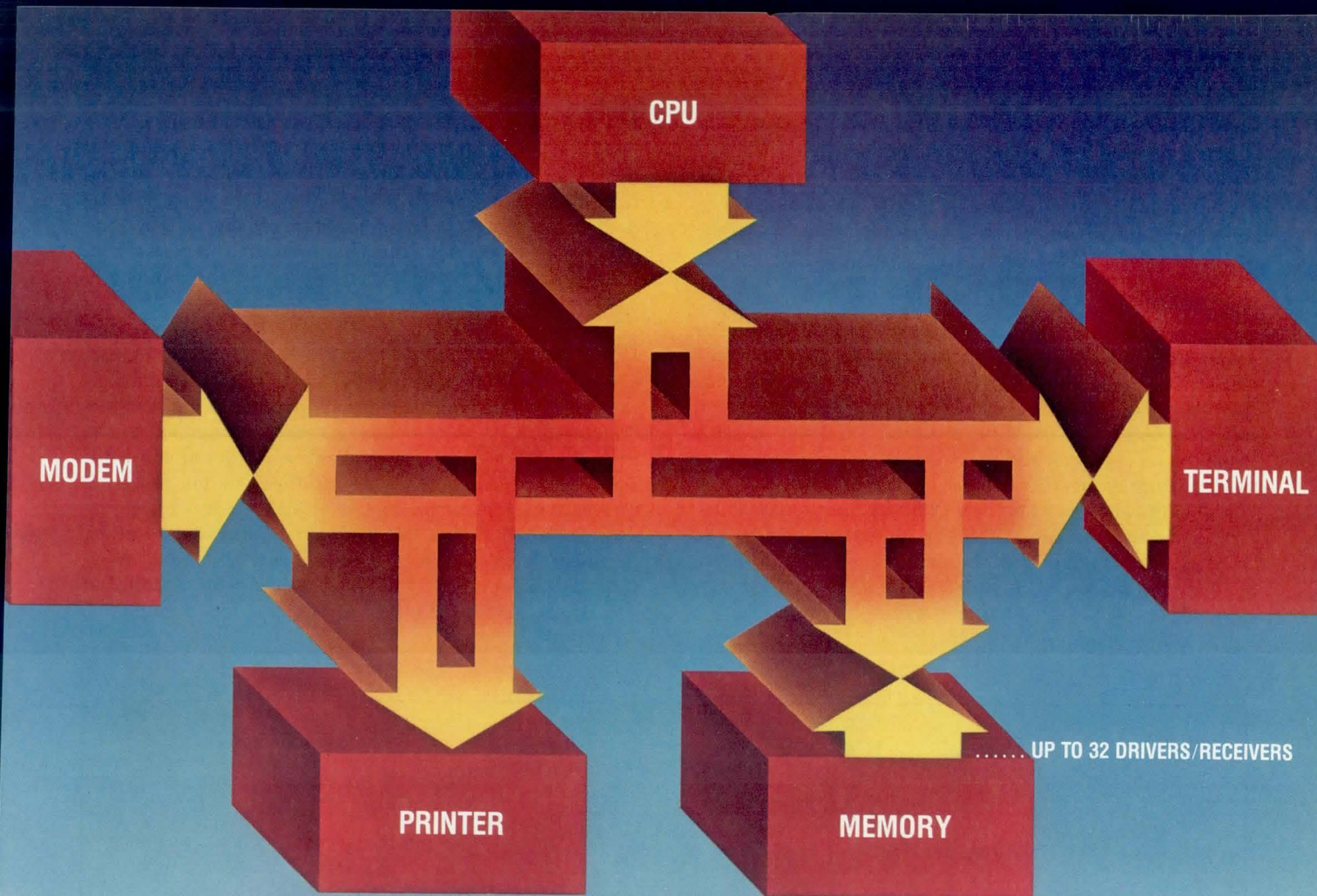


Fig 1 32- by 32-bit floating point multiplier. Exponents and mantissas separate to undergo required arithmetic processing under control of microprogram sequencer



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described in Part 1. The microprogram sequencer controls the mantissa multiplication as well as the exponent operations.

Summation and shifting of the partial products are performed by the 28-bit mantissa accumulator and programmable shifter, producing a 24-bit, single-precision, normalized, and rounded product. The entire process is accomplished in 1.2 μ s, using an 8-MHz clock.

Hardware details for part of the floating point multiplier (excluding the mantissa accumulator and programmable shifter) are presented in Fig 2, including interface registers for the mantissas that consist of three 25LS2520 octal registers for each of the X and Y inputs. The 3-state outputs from these registers and the 74LS244 octal buffers allow multiplexing of the X and Y most significant bits (MSBs) and least significant bits (LSBs) into 12-bit half-mantissas, which are then applied to the multiplier. Output enables for the registers and buffers are obtained from P/ROM 2. These enables are labeled \overline{XLOE} , \overline{XMOE} , \overline{YLOE} , and \overline{YMOE} , and correspond to the X and Y LSBs and MSBs.

A number of different Schottky transistor-transistor logic (TTL) registered P/ROMs may be used; for example, the 27S27 is organized as 512- x 8-bits. P/ROMs are employed as configurable gate arrays to provide the 10 firmware instructions developed by the microprogram sequencer. These instructions include such functions as multiplication and summation of partial products, normalizing, and rounding (see Table 1).

Four-Cycle Mantissa Multiplication

The MPY-12HJ multiplier (Fig 3) is a 12- x 12-bit parallel array device with a typical 80-ns multiply time. X and Y inputs are stored in clocked input registers, then applied to the multiplier array. For the present application, the most significant product (MSP) is downshifted one bit, removing the least significant product (LSP) sign bit by connecting right shift (RS) to 5 V. In this floating point configuration, rounding is accomplished by external circuits, and therefore onchip rounding is disabled by tying the RND pin to ground. To obtain the fastest throughput, feedthrough (FT)

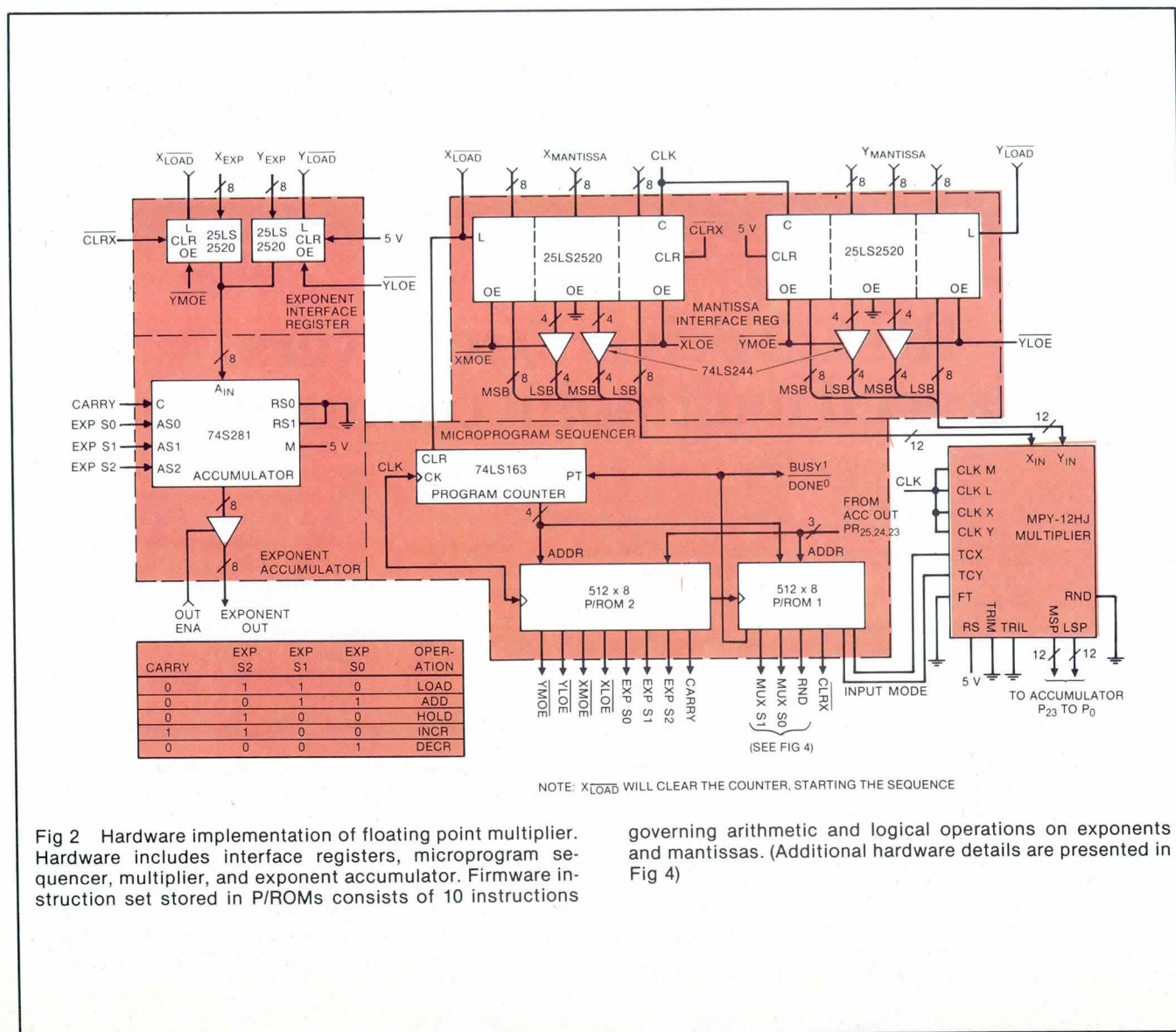


Fig 2 Hardware implementation of floating point multiplier. Hardware includes interface registers, microprogram sequencer, multiplier, and exponent accumulator. Firmware instruction set stored in P/ROMs consists of 10 instructions

governing arithmetic and logical operations on exponents and mantissas. (Additional hardware details are presented in Fig 4)

TABLE 1

Program Details for Multiplication, Normalization, and Rounding

P/PROM OUT	MPY		ACCUMULATOR OUT	SWITCH MUX	EXPONENT		COMMENT
	IN	OUT			IN	OUT	
DONE = 0 RND = 0	-	0	0	-	-	0	OLD ANS CLEARED
(INST 0) DONE = 1 RND = 0	$Y_L X_L$	0	0	-	STORE Y	0	
(INST 1) RND = 0	$Y_L X_M$	0	0	-	HOLD	Y	
(INST 2) RND = 0	$Y_M X_L$	$Y_L \times X_L$ (PROD 1)	0	-	ADD X TO Y AND STORE	X + Y	
(INST 3) RND = 0	$Y_M X_M$	$Y_L \times X_M$ (PROD 2)	PART 1 = PROD 1 + 0	$\div 2^{12}$	HOLD	X + Y	
(INST 4) CLR X RND = 0	$Y_M O$	$Y_M \times X_L$ (PROD 3)	PART 2 = PART 1 + PROD 2 2^{12}	X1	HOLD	X + Y	
(INST 5) RND = 0	0	$Y_M \times X_M$ (PROD 4)	PART 3 = PART 2 + PROD 3	$\div 2^{12}$	HOLD	X + Y	
(INST 6) RND = 0	0	0	PART 4 = PART 3 + PROD 4 2^{12}	X1	HOLD	X + Y	
(INST 7) A RND = 1 B C	0	0	PART 4	X2 X1 $\div 2$	DEC STORE HOLD INC STORE	X + Y - 1 X + Y X + Y + 1	ADJUST EXPONENT AND RND
(INST 8) RND = 0	0	0	PART 4 + RND $\times 2$ IF 7A $\times 1$ IF 7B $\div 2$ IF 7C	X1	HOLD	PARTIALLY NORMALIZED EXPONENT	CHECK OVF DUE TO RND
(INST 9) B RND = 0 C DONE = 0 = HALT	0	0	MANTISSA READY	X1 $\div 2$	HOLD INC	NORMALIZED EXPONENT	FINAL ANS READY
(INST 10 = INST 9)							COUNTER FROZEN

NOTES: ANS = ANSWER; RND = ROUND; INST (N) are the instructions appearing in the outputs of the registered P/PROMs; INST 7A, 7B, or 7C, and INST 9B or 9C are selected according to the states of the 3 MSBs of the final product before normalization (PR₂₅, PR₂₄, PR₂₃)

also is grounded to enable the output pipeline registers. Grounding TRIM and TRIL, the 3-state output controls, enables both the MSP and LSP outputs.

Unsigned magnitude, 2's complement, and mixed input formats are required to assemble the product. Therefore, P/PROM 1 establishes the appropriate coding for TCX and TCY, which control the input modes.

Circuitry used to accumulate and shift the partial products obtained from the multiplier is shown in Fig 4. The accumulator consists of seven 74S283, 4-bit full adders. Four 74LS273 8-bit registers and 14 dual 4-input multiplexers (74LS153) form the programmable shifter, organized in 28-bit sections. The 24 bits of the multiplier are applied to the middle 24 bits of the shifter. This allows the circuit to

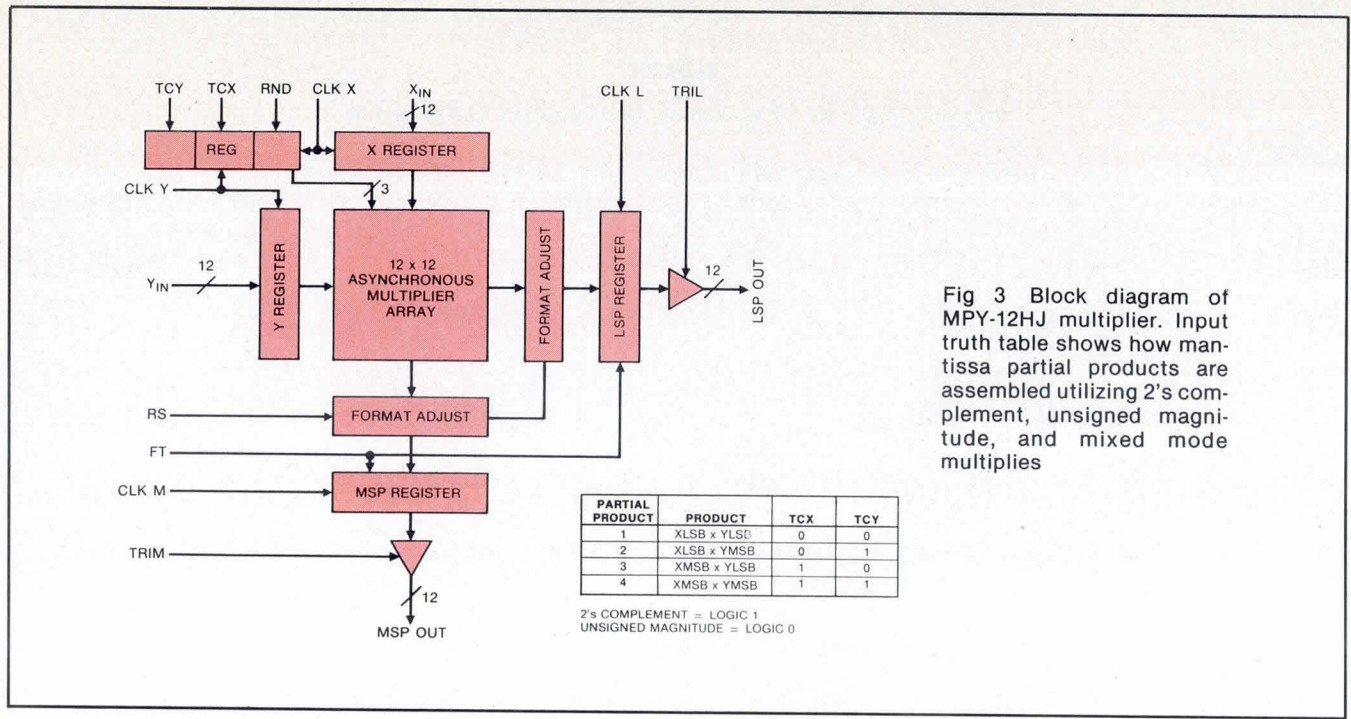


Fig 3 Block diagram of MPY-12HJ multiplier. Input truth table shows how mantissa partial products are assembled utilizing 2's complement, unsigned magnitude, and mixed mode multiplies

maintain two bits of precision (PR₀ and PR₁) below the LSB to eliminate truncation errors before rounding, and two bits above the MSB (PR₂₆ and PR₂₇) to provide for word growth during accumulation of the partial products.

Shifting Controls Normalization

Multiplexing provides the capability to shift the mantissa one bit up or down, 12 bits down, or not at all. The 12-bit

shift is used to accumulate the partial products and the 1-bit shifts are used for normalization. This is accomplished by hardwiring the 28 outputs (PR₀ to PR₂₇) of the 28-bit register to the appropriate inputs of the multiplexer (Fig 4). Multiplexer control is obtained from MUX S0 and MUX S1, produced by P/ROM 1.

After firmware instructions 0 to 6, involving the accumulation of partial products, the normalization procedure is

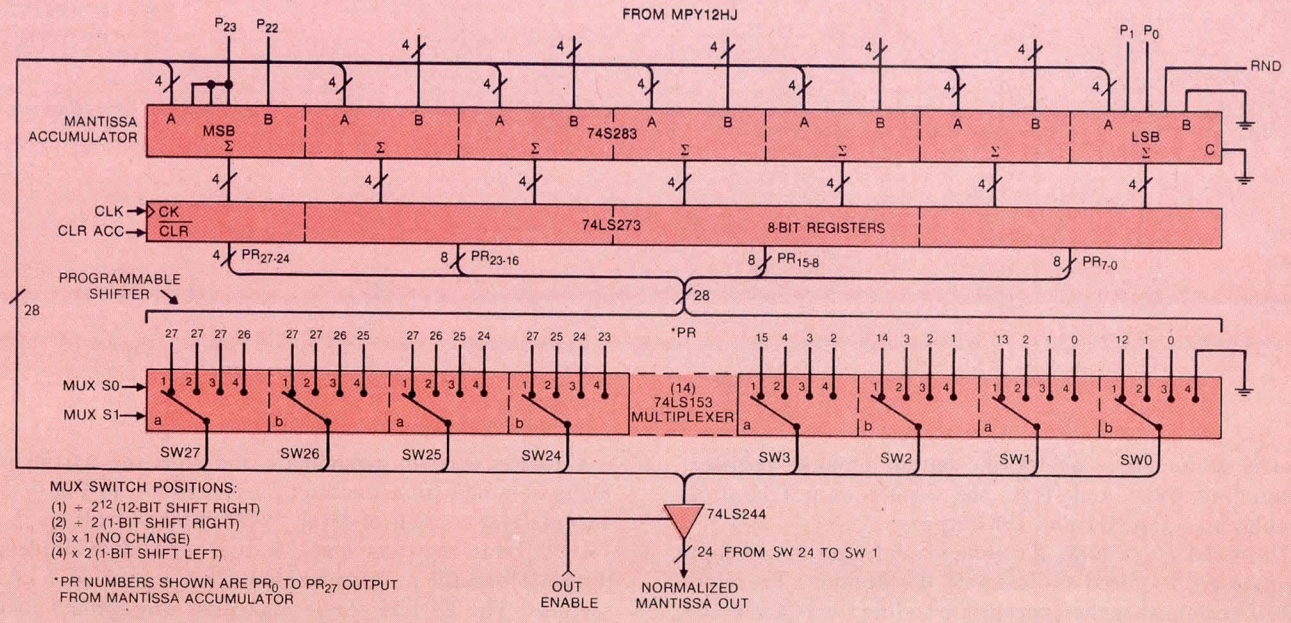


Fig 4 Mantissa accumulator and programmable shifter. Multiplier inputs 24-bit products to 24 middle bits of shifter,

leaving two bits of precision below LSB and two bits above MSB for word growth during partial product accumulation

TABLE 2
Programmable Shifter Truth Table

PR 25	PR 24	PR 23	CONDITION	SHIFTER	INSTRUCTION
0	0	0	UNDERFLOW	×2	7A
0	0	1	NORMAL	×1	7B, 9B
0	1	0	OVERFLOW	+2	7C, 9C
0	1	1	—	×1	—
1	0	0	—	×1	—
1	0	1	—	×1	—
1	1	0	NORMAL	×1	7B
1	1	1	UNDERFLOW	×2	7A

×2 = 1-BIT UPSHIFT
+2 = 1-BIT DOWNSHIFT
×1 = NO CHANGE

initiated with instruction 7. This starts by raising the RND signal applied to the mantissa accumulator from P/ROM 1. PR₂₃ to PR₂₅ are examined. These are the MSBs of the 24 bits from the multiplication. These bits are decoded (through their use as addresses in the P/ROMs) to produce the normalizing and rounding instructions (see Table 2).

The calculated exponent (Fig 2) is also modified according to underflow/overflow conditions. For an underflow, the exponent is decremented and stored, while an overflow causes the exponent to be incremented and stored. If the mantissa is already normalized, there is no change in the

exponent. The sequence is controlled by signals EXP S0, EXP S1, EXP S2, and carry, stored in P/ROM 2.

If an overflow occurs during rounding, the mantissa must be downshifted one bit, and the exponent incremented one bit. This overflow condition is checked in instruction 8. If there is no overflow due to rounding, P/ROM 2 generates subinstruction 9B, indicating that the final answer is ready, and no further change is made. Completion of the process is indicated by the BUSY/DONE flag going low. The counter is then frozen and stays there until an X-load is received and the sequence can start over again.

This circuit assumes that both the exponent and mantissa are signed 2's complement numbers. That is, the mantissa has a range of -1.0 to (1.0 - 2⁻²³), and the exponent is represented by 2⁻¹²⁸ up to 2¹²⁷. Other common usage formats can also be handled; however, they require minor coding changes in the P/ROMs and/or simple wiring changes.

Summary

Design of a 32- x 32-bit floating point multiplier, as described, is a comparatively straightforward process that involves separation of 8-bit exponents from 24-bit mantissas. Addition of the 8-bit exponents is accomplished directly, while multiplication of the mantissas is carried out through the summing of partial products. Instructions stored in P/ROMs govern accumulation of partial products, normalization, and rounding.

A more difficult task is posed by floating point addition. The third, and last, column in this series will address that issue.

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Single-Chip LSI Speech Synthesizer Produces Unlimited Vocabulary Using Phonemes

A speech synthesis circuit, the SC-01, implemented on a single LSI chip, and available in OEM quantities at under \$12/unit, combines phonemes (speech sounds) to produce an unlimited vocabulary. Manufactured by Votrax, Div of Federal Screw Works, 500 Stephenson Highway, Troy, MI 48084, the 22-pin CMOS device operates at a data rate of only 70 to 100 bits/s. The advantages of unlimited speech and low memory requirements are the direct result of the chip's use of phoneme based speech rather than reconstituted human speech, differentiating the circuit from existing synthesizer chips, which are limited to modeling the human vocal tract through a word or phrase reconstitution scheme.

The synthesizer utilizes a switched capacitor filter (SCF) technology provided by Silicon Systems, Inc of Tustin, Calif, a company specializing in custom chip design. Illustrative of the power of the IC is its ability to produce a word of three phonetic sounds, such as "cat," using only 18 bits of memory. By contrast, the reconstitution of the same word from human speech data could require more than 500 bits.

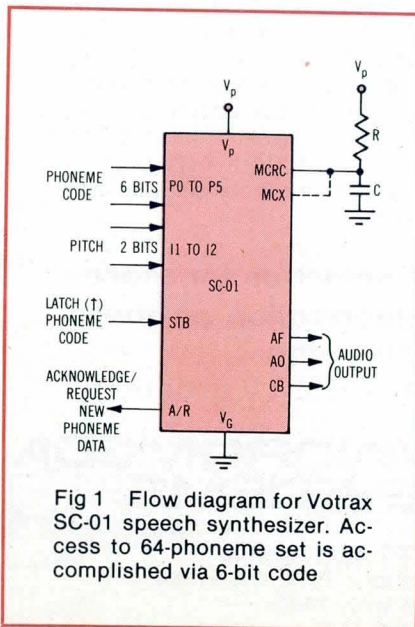


Fig 1 Flow diagram for Votrax SC-01 speech synthesizer. Access to 64-phoneme set is accomplished via 6-bit code

Most previous speech devices have needed several large memory chips on which to store speech data. Some have also required a dedicated microprocessor to control the voice synthesizer chip. The phoneme chip, however, does not require any microprocessor controller in order to produce speech. A common configuration requires only the synthesizer and one memory chip to generate the specific vocabulary.

Initial programming and reprogramming of the vocabulary sequence does not require the services of the chip vendor. A vocabulary development system, the CDS-1, containing the algorithm that automatically translates English text to phonemes, will be available to the user. The system consists of a tabletop keyboard terminal

with a display, a speaker, and a line printer. The user types English text into the system, and a phonetic transcription is provided in numeric form and symbolic representations. These data can be selectively displayed on the terminal or the accompanying line printer.

Duration of each phoneme is fixed, the slowest being 40 ms and the fastest 250 ms. In the synthesis process, a sequence of four events occurs. First, a phoneme command is presented to the chip, and the strobe input is pulsed. Second, a duration timer is reset when phoneme production begins. Next, the request for a new phoneme command occurs when the duration of the previous phoneme ends (acknowledge/request signal high). Finally, the next phoneme command is presented (acknowledge/request signal low).

Pitch variation per phoneme, a parameter important to the intelligibility of speech output, varies automatically. Two input bits are provided to control the average pitch level of the speech
(continued on page 196)

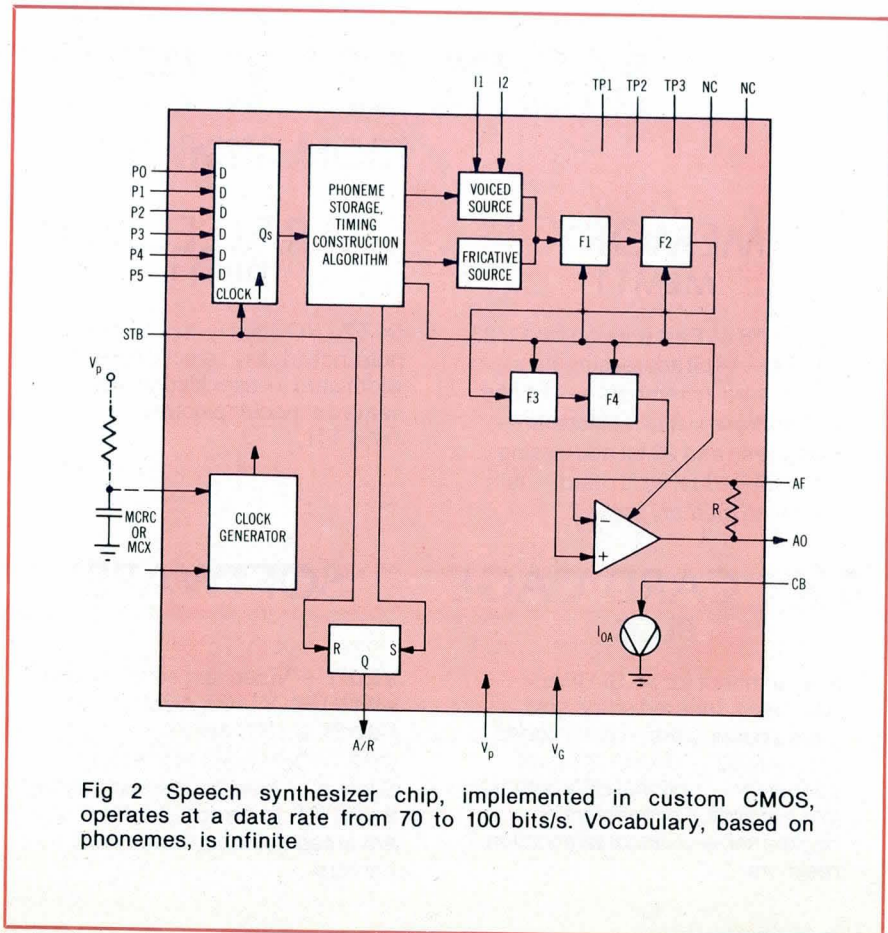
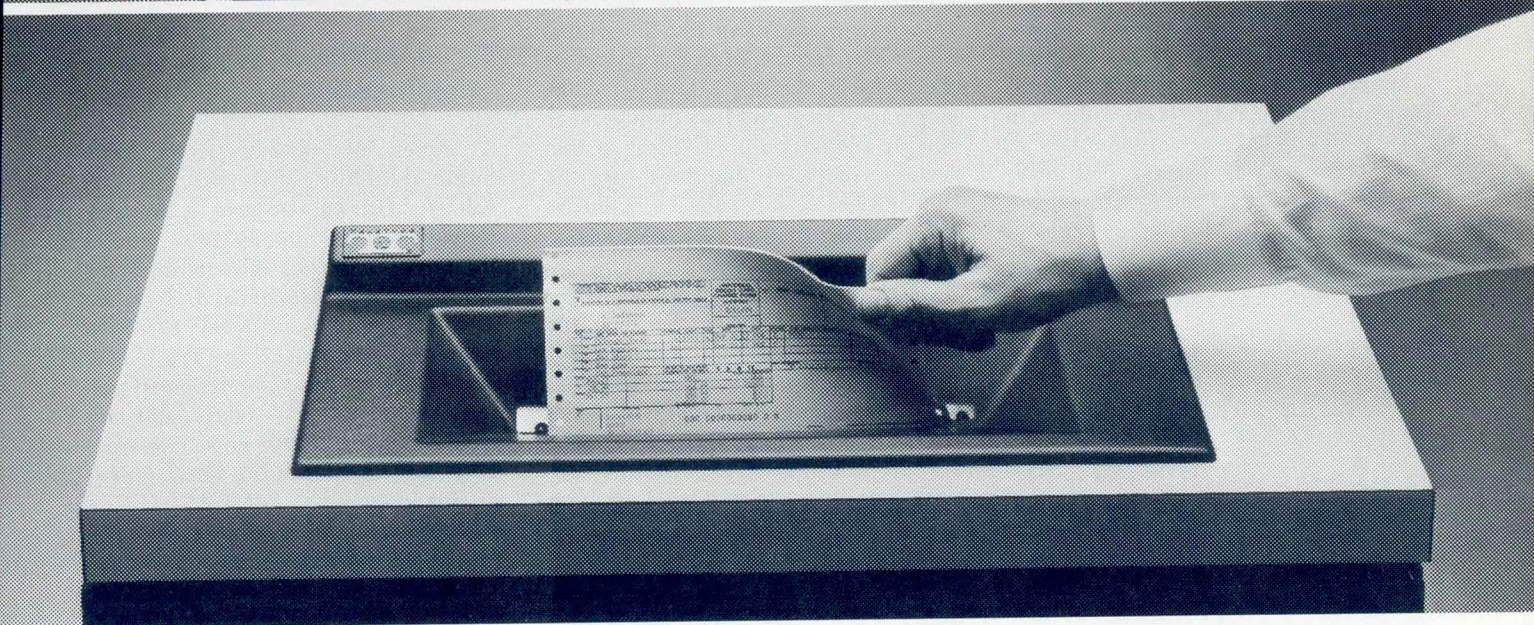
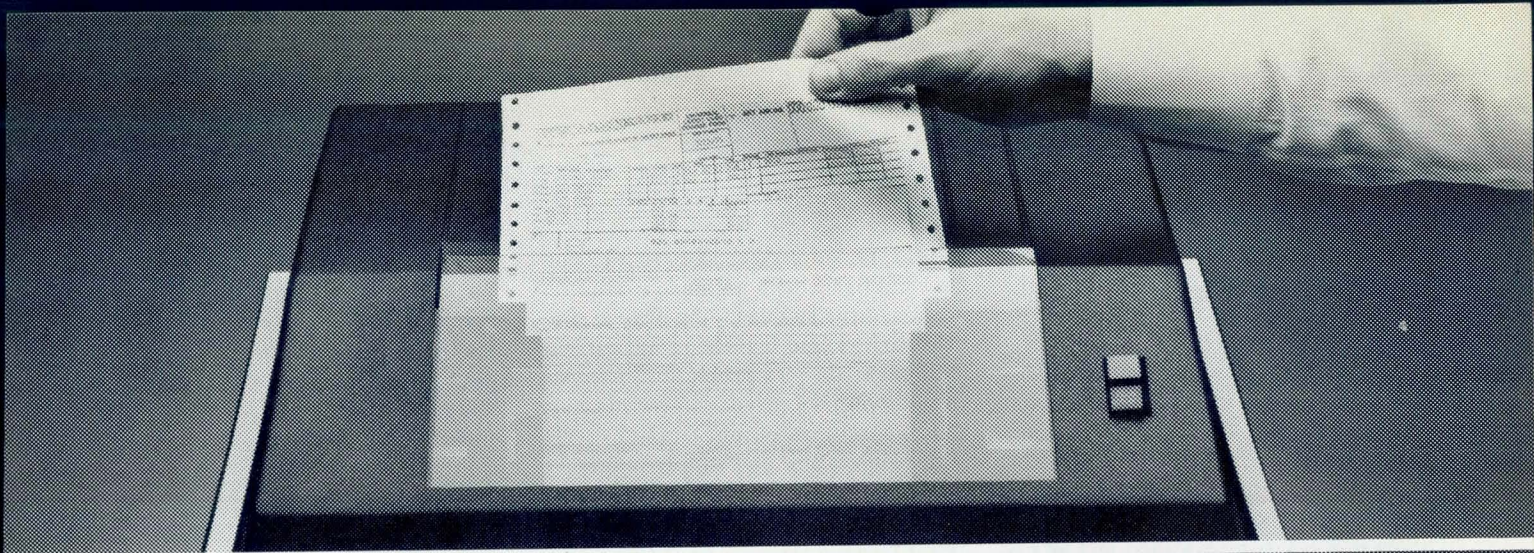


Fig 2 Speech synthesizer chip, implemented in custom CMOS, operates at a data rate from 70 to 100 bits/s. Vocabulary, based on phonemes, is infinite



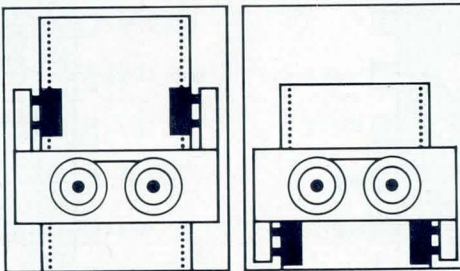
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output. When special sound effects instead of speech output are desired, the overall pitch may be controlled by varying the master clock input frequency. Pitch manipulation may also be achieved by utilizing an external clock or varying the resistor capacitor value.

Additional characteristics include a current drain of 9 V (typ), latched inputs with 5-V compatibility, and an on-chip 720-kHz master clock circuit. Absolute maximum ratings limit supply voltage, V_p , to a max of 20 V, and input voltage to a range from -0.5 V to $V_p + 0.5$ V. Power dissipation at 25 °C must not exceed 650 mW, derated above that temperature by 5 mW/°C. Acceptable temperature ranges are 0 to 70 °C (ambient) in operation, and -55 to 125 °C in storage.

Circle 501 on Inquiry Card

Quad Line Drivers Provide Fault Protection

Specifically developed to meet the updated IBM 360/370 peripheral I/O standard, two single-ended quad line drivers have been introduced by Motorola Semiconductors, PO Box

20912, Phoenix, AZ 85036. In addition to compliance with parametric requirements of the standard, the devices provide driven line fault flagging, current foldback driver protection, power-up/power-down protection for the bus, and guaranteed output levels over the full temperature and supply range.

Although identical in function, the drivers differ in enable and fault flagging organization. The MC3481 provides two enables and four individual fault flags for the four drivers, while the MC3485 provides a single enable, single fault flag, and four individual LS complemented outputs. Their manufacturer indicates that these are the first devices to meet the stringent requirements of the IBM GA22 6974-3 specification.

As they are specified in I/O driver and select out driver applications, the devices feature Schottky circuitry for high speed, PNP input structure, and internal bootstraps for fast rise times. They are appropriate for IBM peripheral and general purpose I/O applications and are available in both ceramic and plastic dual inline packages.

Maximum ratings limit power supply voltage (V_{CC}) to 7 V, input voltage (V_i) to 10 V, and driver output voltage (V_o) to 5.5 V. The maximum allowable power dissipation is 1150 mW for the

ceramic and 962 mW for the plastic package, both derated above 25 °C by 7.7 mW/°C. The temperature must stay between 0 and 70 °C in operation and between -65 and 150 °C in storage.

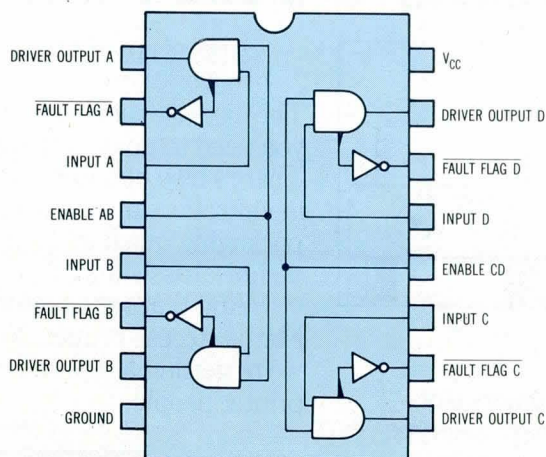
Circle 502 on Inquiry Card

Octal Interface Circuits Implemented in CMOS

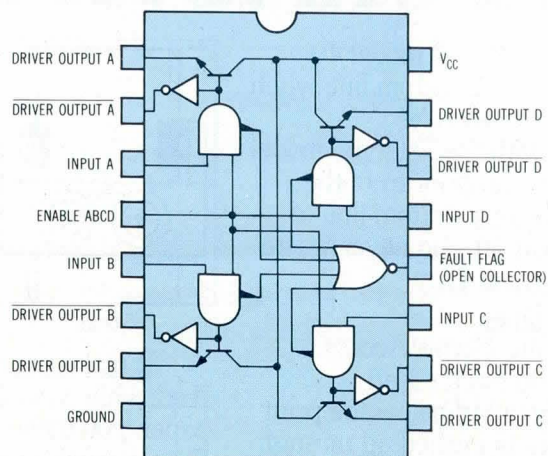
A series of devices from Mitel Semiconductor, PO Box 13089, Kanata, Ottawa, Ontario K2K 1X3, Canada, utilizes an ISO-CMOS process to provide a variety of octal interface capabilities. Described by the manufacturer as a cost effective upgrade replacement for low power Schottky designs, these circuits provide 5-ns typ gate delays and are characterized by CMOS noise immunity and negligible quiescent power dissipation.

One of the three families included in this series consists of 3-state, D-type, transparent, 8-bit latches and edge triggered flipflops, designed for use in high speed, bus oriented systems. The MD74SC373 appears transparent to data

(continued on page 198)



Quad single-ended line drivers from Motorola Semiconductors. Left diagram shows MC3481, having dual-enable and individual fault flags. At right is



MC3485, offering common enable and common fault flag



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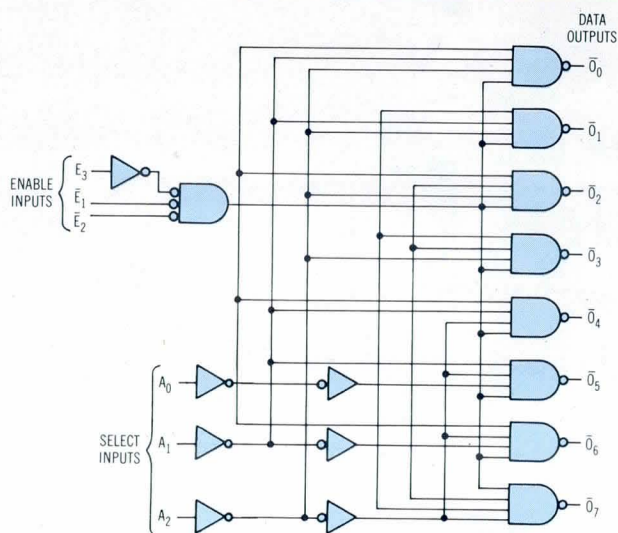
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CIRCLE 109 ON INQUIRY CARD



Octal decoder MD74SC138 from Mitel. Enable inputs \bar{E}_1 , \bar{E}_2 , and E_3 reduce output gate requirements. Device decodes binary inputs A_0 to A_2 , outputs 1 of 8 mutually exclusive outputs \bar{O}_0 to \bar{O}_7 .

(outputs changing asynchronously) when latch enable (LE) is high. When LE is low, data meeting the setup times become latched. In the /374 version, latches hold their individual data when meeting setup times with the clock low to high transition. With both devices \bar{OE} does not affect the state of the latches, but when \bar{OE} is high the output is put into high impedance. Data may thus be latched even when the device is deselected. A selection of packages offers a choice of inverted or noninverted outputs.

Single 1-of-8, latched or unlatched, and dual 1-of-4 configurations make up the decoder MD74SC138 family. These circuits are designed for use in high speed memory and peripheral address decoding systems. The /138 decodes three binary inputs to select 1-of-8 mutually exclusive outputs. Three enable inputs, two active low and one active high, reduce the need for external gates in an expanded system. Version /137 features additional latches on inputs for use in glitch free applications. A 1-of-32 decoder requires only four of these devices and one inverter. The /139 contains two individual 2-line to 4-line decoders. Corresponding to each of these inverted versions is a non-inverted version (/237, /238, /239).

Finally, the MD74SC240 series consists of 3-state octal buffers and line drivers. These are designed to improve PCB density and performance in 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters. A range of devices covers a selection of differing I/O pin layouts, inverting and noninverting buffers, and a choice of similar or complementary output controls.

Absolute maximum ratings for devices in all of these families require that supply voltage (V_{CC}) stay between -0.5 and 7.0 V and that input voltage stay between -0.3 V and $V_{CC} + 0.3$ V. Output current must not exceed ± 75 mA/output nor may power dissipation rise above 450 mW. Allowable temperature ranges are -40 to 85 °C in operation and -65 to 150 °C in storage.

Circle 503 on Inquiry Card

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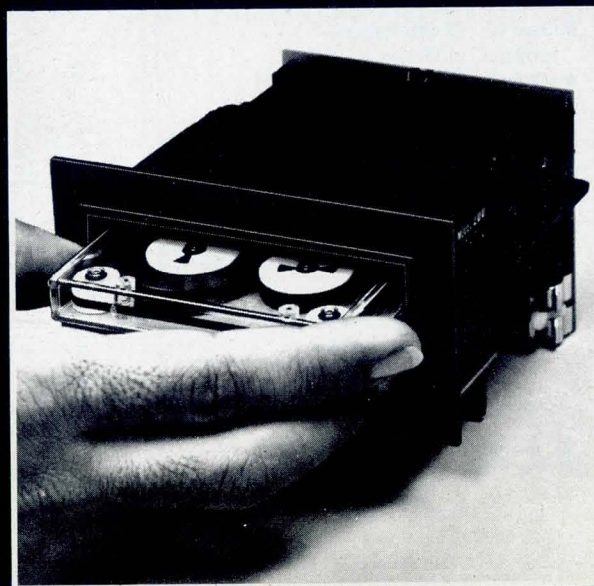
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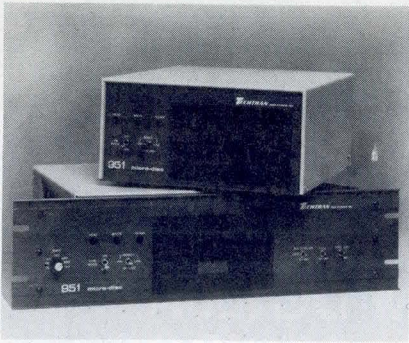
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CIRCLE 112 ON INQUIRY CARD

AROUND THE IC LOOP

Military RAM Saves Power On Standby

An access time of 70 ns (max), true static operation with cycle time equal to access time, low power standby, and operation from a single 5-V $\pm 10\%$ supply characterize a 4096-bit, static RAM from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Introduced three months after the 2148H, the M2148H is the military version. It is fabricated with a proprietary HMOS II technology, operates over a temperature range from -55 to 125 °C, and meets requirements of MIL-STD-883B.

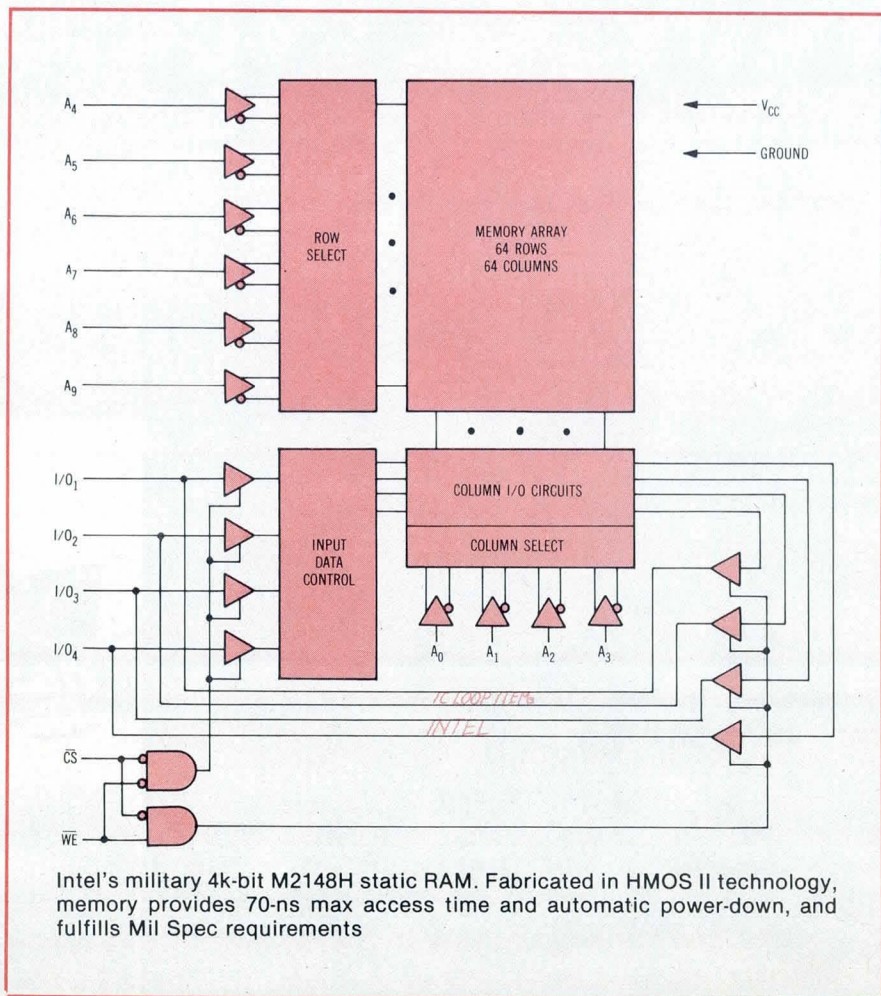
Organized as $1k \times 4$, the RAM draws a max supply current of 180 mA in active operation. Current drain is automatically reduced to 30 mA when the chip is disabled via the chip select (\overline{CS})

input. It is useful in applications such as signal processing with bit-slice processors, buffer memories, and large high speed memory systems.

The automatic power-down feature reduces system power requirements as much as 85%. Moreover, the power savings tend to increase with system size, since in larger systems only a small percentage of the RAM devices are selected simultaneously. In addition to new system applications, the device is suitable for many performance upgrade applications and is pin compatible with the company's M2114A static RAM.

Additional features include common data input and output pins utilizing three state outputs, direct TTL-compatible I/O, and packaging in an 18-pin ceramic DIP. Data are read out nondestructively with the same polarity as the input data.

Circle 504 on Inquiry Card



Intel's military 4k-bit M2148H static RAM. Fabricated in HMOS II technology, memory provides 70-ns max access time and automatic power-down, and fulfills Mil Spec requirements

**16-Bit ADC
Offers Speed
At Low Cost**

A 16-bit successive approximation analog to digital converter from Micro Networks Co, 324 Clark St, Worcester, MA 01606, provides a conversion time of 50 μ s max and 40 μ s typ. It is available at \$187 in 100 lots.

The MN5282 features an internal reference, an internal clock, six user selectable input ranges, short cycling capability, optional gain and offset adjustments, and DIP packaging. For operation over temperature, it is fully specified with absolute accuracies for the user who is not utilizing initial gain and offset adjustments and with gain and offset drift specifications for the user who is adjusting at room temperature.

Thin film, laser trimmed resistor networks provide a guaranteed $\pm 0.003\%$ linearity at 25 °C and $\pm 0.006\%$ linearity over the entire 0 to 70 °C operating range. Specifications include values of ± 10 ppm/°C (typ) for gain drift and typ unipolar and bipolar offset drifts of ± 3 and ± 7 ppm of FSR/°C. Power consumption is 1400 mW typ and 1800 mW max.

The device was designed to be a low cost, physically small alternative to currently available modular and PCB high resolution ADCs. It fills the need for a reliable, high resolution converter in a microprocessor compatible package. Applications include precision measurement and data acquisition systems, high resolution biomedical scanning equipment, nuclear accelerator and seismological instrumentation, and other uses requiring high resolution data digitizing capability.

Absolute maximum ratings limit supply voltages to ± 18 V, logic supply to 7 V, and analog inputs to ± 25 V. Digital inputs must remain between 0 and 5.5 V. Allowable temperature ranges are 0 to 70 °C in operation and -65 to 150 °C in storage. The converter is provided in a 32-pin dual in-line package.

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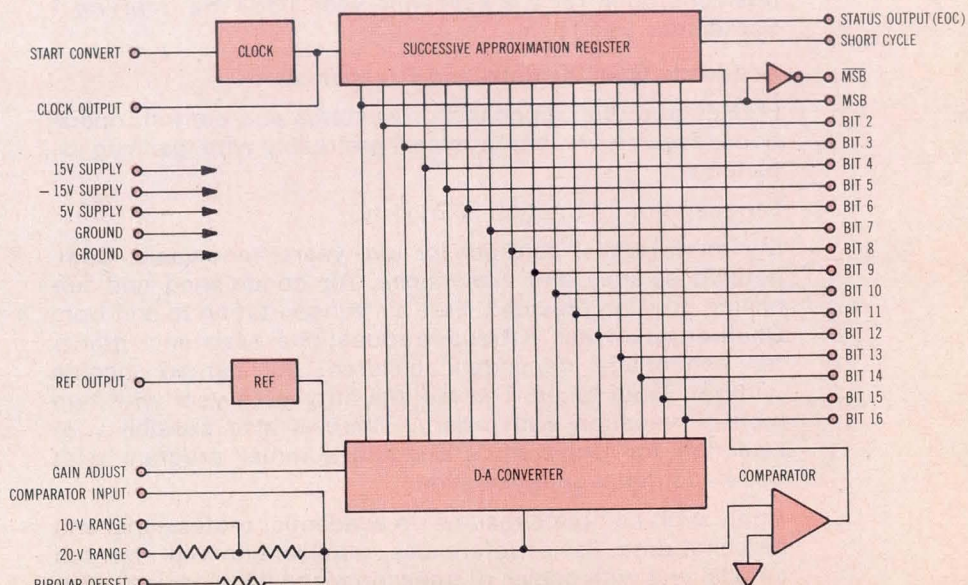


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CIRCLE 113 ON INQUIRY CARD

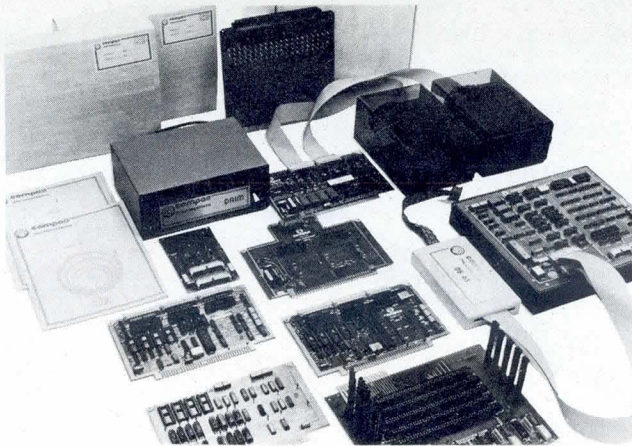


16-bit successive approximation ADC, MN5282, from Micro Networks. Device provides low cost, compact alternative to modular and PCB high resolution converters



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CIRCLE 115 ON INQUIRY CARD

AROUND THE IC LOOP

Memory Control ICs Manage Dynamic RAMs

Two series of integrated circuits from Texas Instruments Inc, PO Box 225012, M/S 308, Dallas, TX 75265, operating either as standalone devices or as elements in a 3-chip set, provide memory management for dynamic RAMs. One series, SN54LS/74LS600, consists of memory refresh controllers, and the other, SN54LS/74LS604 consists of 16- to 8-line multiplexers with input latches. In the 3-chip configuration, a refresh controller and a MUX will be accompanied by a memory cycle controller that is to be announced.

The refresh controller provides bus driving peripheral control capabilities for the refresh of dynamic RAMs to create a static RAM appearance. Each IC in this series contains an 8-bit synchronous counter, nine 3-state buffers, four RC-controlled multivibrators, and other related circuitry. Critical times are user RC-programmable to optimize system performance.

Transparent or burst refresh modes characterize the LS600 (for 4k or 16k RAMs) and the LS601 (for 64k RAMs). Similarly, cycle steal or burst modes are provided by the LS602 (for 4k or 16k RAMs) and the LS603 (for 64k RAMs).

The 16 to 8 multiplexer contains 16 input latches divided into two 8-bit words for sequential loading to the RAM during row and column selection. Versions LS604 and LS606 have 3-state outputs and clock to output times of 23 and 31 ns, respectively. The LS605 and LS607 furnish open collector outputs and clock to output times of 26 and 31 ns.

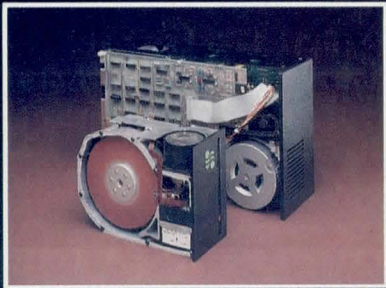
All of the devices in the two series are compatible with this manufacturer's TMS9900 16-bit microprocessor, as well as other 8- and 16-bit microprocessors. When used with the 9900, the two series are redesignated as TIM99600 and TIM99604. The chips are available in 20- and 28-pin plastic packages and will also be offered in full military temperature versions in ceramic DIPs.

Circle 506 on Inquiry Card

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**A better choice than
eight-inch Winchester.**

Our drive is smaller, more cost-effective and easier to back up. Some eight-inch Winchester drives require AC power. This complicates system integration and produces extra heat that can mean additional cooling. We use only 22 watts.



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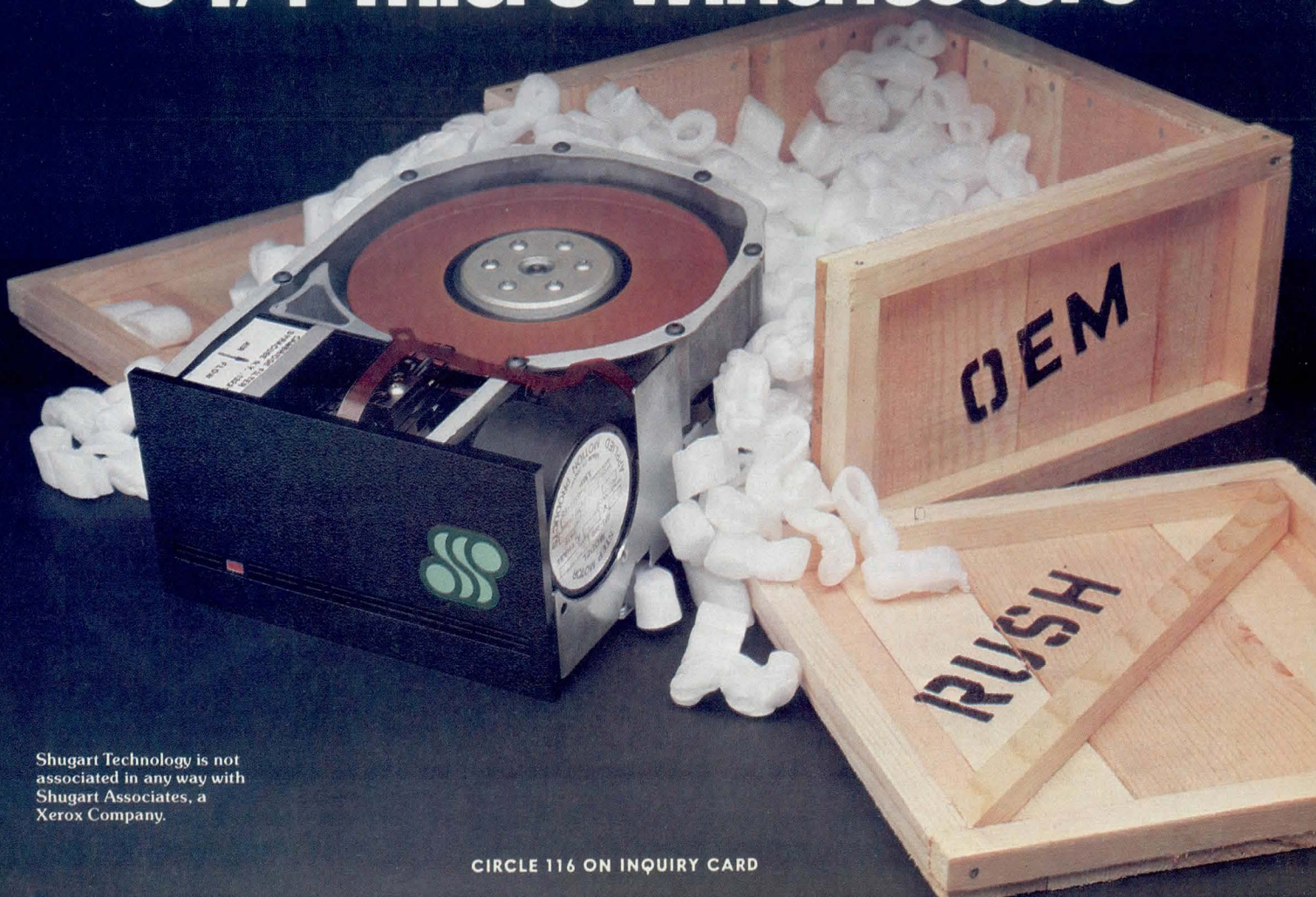
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CIRCLE 116 ON INQUIRY CARD

6-Decade Up Counter Contains MNOS Memory

An integrated circuit from Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714, includes a 6-decade up counter in parallel with a 25-bit metal nitride oxide semiconductor memory. This MNOS memory provides a capability for nonvolatile storage of a specified count position, with data retention guaranteed for 1 yr in the absence of applied power, over a temperature range of -40 to 70 °C.

The device is available in three variations. The MN9106 is a batch counter with an overflow latch that is activated when the counter hits 999999. Both of the other versions are lapsed time indicators, the MN9107 displaying up to 99 h, 59 min, 59 s, and the MN9108 up to 9999 h, 59 min or 9999 min, 59 s.

An overflow latch and memory bit are available to indicate a counter overflow condition. In addition to the conventional counter controls, recall and save inputs are provided to control the transfer of data between the counter and memory. Output data are presented in the form of multiplexed 7-segment outputs and 6-digit strobes. The multiplexing sequence is controlled by an internal oscillator that may also be forced from an external oscillator on the scan input.

A single 12-V supply fulfills power requirements. The higher voltage required for the MNOS memory is provided internally by a generator that requires only a single external capacitor.

Operating from dc to 200 kHz, the circuit contains a self-scanning multiplexer and seven segment drivers. Additional capabilities include leading zero and full blanking facilities, CMOS compatible inputs, and the option of utilizing split supplies (5 and -7 V) to allow inputs to interface with TTL. The series offers an alternative to existing approaches, such as the use of CMOS chips with battery backup and offchip nonvolatile logic requiring 35 to 40 V of external power.

Circle 507 on Inquiry Card

Low Cost CRT Controller Uses ROM Programs, No Software Registers

The S68045 CRT controller is a ROM programmable device for pin compatible replacement of software programmable CRT controllers at price reductions as great as 40%. This chip from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, is designed to reduce the manufacturing cost of high volume intelligent CRT terminals, word processors, and information display equipment.

Terminals designed with the software programmable MC6845 or SY6545 can directly substitute this controller, once character fonts and display formats have been established. The device stores two complete character and display programs in ROM. Use of ROM instead of RAM, modulo-N counters instead of binary counters, and elimination of the lightpen option reduce chip size and lower price in high volume quantities. Power supplies and clocks remain unchanged.

The controller consists of counting circuits, a linear address counter, and control registers. Horizontal and vertical counting circuits generate display enable, hsync, vsync, and scan line count signals (RA0 to RA4) to the external character generator ROM. Four cursor modes provide for nonblink, slow blink, fast blink, and (with addition of a single TTL gate) reverse video. The cursor control register determines cursor location on the screen. Cursor and/or display can be delayed 0, 1, or 2 clock cycles.

Additional features of the NMOS silicon gate device include three interlace modes (normal sync, interlace sync, or interlace sync and video), the capability to address 16k bytes of memory, and full hardware scrolling. Text can be scrolled on a character, line, or page basis. The screen can be up to 128 characters tall by 256 wide, and the character font can be 32 lines high at any width.

This circuit is TTL-compatible and operates off a single 5-V supply. Its

maximum ratings require that its supply and input voltage remain between -0.3 and 7.0 V. Allowable temperature ranges are 0 to 70 °C in operation and -55 to 150 °C in storage.

Circle 508 on Inquiry Card

CRT Controller Offers Full Programmability

Designed to provide the interface between a microprocessor system and a conventional raster scan CRT display, the HD46505/MC6845 generates the refresh address and video timings according to display format. Offered by Hitachi America Ltd, 707 W Algonquin Rd, Arlington Heights, IL 60005, this IC is one of a series of controller chips in the HMCS6800 family. It is applicable to a wide range of raster scan displays. Applications include intelligent CRT terminals and information display systems.

The device is optimized for hardware/software balance in order to achieve integration of complex CRT interface functions and to maintain flexibility. It provides a programmable screen and character format, line bufferless refreshing, 14-bit refresh memory address, a cursor control function, programmable cursor format and blink, and a lightpen detection function. Options allow a programmable interlace or noninterlace scan, as well as limited or full graphic display capability. Additional features include character by character video control (color, blink, inverse, etc) and hardware scrolling and paging functions.

With refresh memory time multiplexed between the CRT controller and the microprocessor, no direct memory access is required. The device is directly interfaceable to the microprocessor bus, operates off a single 5-V power supply, and provides direct TTL compatibility on all inputs and outputs. It is fabricated utilizing N-channel enhancement/depletion MOS technology and is provided in a 40-pin dual inline package.

Circle 509 on Inquiry Card

Miniature DIPs House Analog ICs

A microminiaturized package having approximately one-fourth the linear dimensions of conventional 24-pin dual inline packages has been introduced by Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Thirteen of this manufacturer's standard analog ICs are being provided in this configuration. The microminiature circuits include comparators, single and dual operational amplifiers, encoders and decoders for radio control systems, and precision voltage regulators.

Designated the S.O. series, the packages measure approximately 0.188 to 0.196 × 0.149 to 0.157" (4.775 to 4.978 × 3.785 to 3.988 mm). Pin spacings, also one-fourth those of conventional devices, are 0.049" (1.2 mm).

It is anticipated that hybrid circuit manufacturers and users will be the major immediate beneficiaries of this packaging concept, since it cuts out the costly, time consuming, and low yield assembly and wiring of naked silicon chips with discrete components on expensive hybrid substrates. Available in 8-, 14-, and 16-pin configurations, the package can be mounted on PCBs or on thick film substrates using conventional reflow soldering techniques.

Circle 510 on Inquiry Card

Fast 12-Bit DAC Has Unipolar, Bipolar Operating Modes

Offering settling times of 300 ns to 0.01% and accuracies to 12 bits, a monolithic digital to analog converter of 12-bit resolution is available from Teledyne Philbrick, Allied Dr at Rt 128, Dedham, MA 02026. The 4068 converter provides externally selectable operation in unipolar or bipolar mode.

High stability, thin film resistor processing results in a guaranteed 12-bit linearity within $\pm 1/2$ LSB max, or (for the military version, suffix -83) $\pm 1/4$ LSB max. Zero offset error as a function of temperature is ± 2 ppm FSR/°C

for unipolar and ± 4 ppm FSR/°C for bipolar operation. Gain error vs temperature is ± 10 ppm FSR/°C.

Applications are found in CRT display generation, high speed ADCs, video signal reconstruction, waveform synthesizers, high speed data acquisition, and precision instrumentation. The commercial version operates over a 0 to 70 °C range, while the military version (screened to MIL-STD-883, Method 5004, Class B) operates over -55 to 125 °C.

Circle 511 on Inquiry Card

32k ROM Offers Compatibility With Standard ROMs, EPROMs

Organized as 4k x 8, the RO-3-9333 read only memory from General Instrument, 600 W John St, Hicksville, NY 11802, features fully static operation with no clocks required and has a 450-ns max access time. This ROM is pin for pin compatible with Intel's 2732 EPROM and with ROMs 2332 (Intel), SY2333 (Synertek), and Am9233 (AMD).

The N-channel device, oriented particularly toward microprocessor memory applications, operates from a single 5-V supply, is TTL compatible on all I/O, and provides 3-state outputs under the control of two mask programmable chip select inputs to simplify memory expansion. Additional features include Zener protected inputs, glass passivation protection, totally automated custom programming, and packaging in a 24-pin DIP.

Circle 512 on Inquiry Card

IC Product Line Operates at High Temperatures

A family of integrated circuits providing a guaranteed operating temperature range of -55 to 200 °C, with characterized performance as high as 250 °C, has been announced by Harris Semiconductor Products Div, PO Box 883, Melbourne, FL 32901. Six circuits are currently available, including two amplifiers (the HA-2600-1 and the HA-2620-1), a quad comparator (the HA-4920-1), two analog switches

(the HI-200-1 and the HI-201-1), and a multiplexer (the HI-508-1).

These devices, manufactured using a proprietary dielectric isolation process, have the ability to withstand stringent environmental requirements. Included in the manufacturing flow is a burn-in for 160 hours followed by a final electrical test at 200 °C.

Four other circuits will be added to the family soon. They will include two quad op amps (the HA-4602-1 and the HA-4622-1), a DAC (the HI-562-1), and a voltage reference circuit (the HA-1610-1).

Circle 513 on Inquiry Card

Voltage Protection Chip Senses Threshold Within $\pm 2\%$

Over- and under-voltage protection for electronic circuitry is provided by an IC from Silicon General Inc, 11651 Monarch St, Garden Grove, CA 92641, that uses an onchip 2.6-V reference to obtain sensing thresholds accurate to $\pm 2\%$ without the need for potentiometers. In case of an over-voltage condition, the SG1542 provides immediate shutdown of the power supply via a 200-mA output drive current into an external SCR crowbar. Furthermore, logic level outputs permit regulator turnoff and operator or system warning indicators. Outputs for both in tolerance and out of tolerance conditions are provided.

Both polarity inputs to the sensing comparator are uncommitted. This allows either over- or undervoltage sensing with a wide common mode range, which includes the ability to sense voltages less than the reference output. Accurate time delay between fault occurrence and crowbar triggering can be programmed by means of an external capacitor. However, this delay can be either bypassed or overridden by remote command.

Additional features include an operating range from 4.5 to 40 V, a 0- to 35-V sensing capability, and built-in input hysteresis. The device is available in a 14-pin cerdip (J) package and is characterized for operation from -55 to 125 °C. Operating temperature range for the SG2542 version is -25 to 85 °C and for the SG3542, 0 to 70 °C.

Circle 514 on Inquiry Card

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leading U.S. manufacturer of diesel engines, and the world's largest energy management system designed to tri-service specifications.

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 **AVCO** ELECTRONICS DIVISION

CIRCLE 117 ON INQUIRY CARD

Avco Electronics Division • Earl R. Tillman • Systems Marketing Director • 4807 Bradford Drive • Huntsville, Alabama 35805

AROUND THE IC LOOP

ICs Drive Plasma Displays

A high voltage display driver chip from Exar Integrated Systems, Inc, 750 Palomar Ave, Sunnyvale, CA 94088, replaces most of the drive circuitry necessary for ac plasma displays, reducing both system cost and power dissipation. The XR-2284, packaged in a 14-pin DIP, is a 4-channel driver, while the XR-2288, packaged in a 20-pin DIP, is an 8-channel driver. All channels have independent I/Os but share a common toggle or clock switch and a common substrate or ground connection.

The circuit is designed as a series connection of two controlled switches (SCR), each formed by two transistors. An internal junction capacitance turns on the appropriate switches during positive and negative edges of the toggle input. During the negative excursions of the toggle voltage, an external diode decouples the substrate from ground. This external decoupling is common to all channels so that many driver ICs can be stacked to drive a large number of display columns with only one backing side and a common toggle input.

Under dc conditions (no ac toggle drive), the driver ICs do not dissipate any appreciable standby power. When ac toggle voltage is applied, corresponding output can follow pk-pk toggle voltage and sink or source up to 100 mA of current to the capacitive load (ie, the plasma panel).

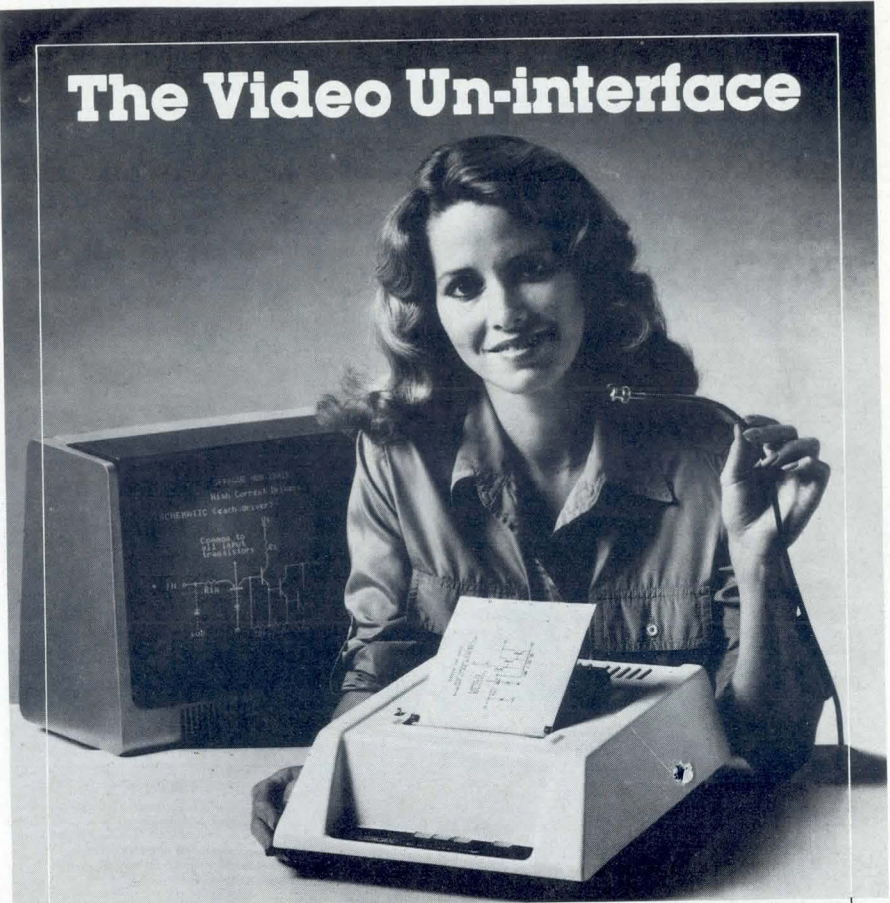
Both versions operate with toggle frequencies up to 200 kHz. Typical power dissipation is about 50 mW per channel, at 200-kHz operation, with 180-kHz ac drive. Dissipation decreases as toggle frequency and drive voltage are reduced. Input logic threshold levels of the drive channels are chosen to be compatible with TTL or CMOS logic levels.

The 4- and 8-channel display driver ICs are available in plastic dual inline packages. Prime grade devices are

designed for 360-V plasma display systems and exhibit a minimum of 90-V sustaining voltage. Commercial versions are designed for 240-V

systems and have ≥ 60 -V breakdown characteristics. Operating temperature for all versions ranges from 0 to 75 °C. Circle 515 on Inquiry Card

The Video Un-interface



Just connect two wires and print what you see

The Axiom EX-850 Video Printer is uniquely different because it requires absolutely no hardware or software interface. Instead, it connects to the standard video input of your CRT terminal, video monitor or TV set. You can even select normal or high resolution, and positive or negative image.

Because the EX-850 operates from

the video signal, it prints exactly what you see on the screen. It handles a news headline in Greek or a street map of Tokyo just as easily as it prints English alphanumeric and graphics.

No doubt about it, the EX-850 is the ultimate in simplicity. The price is amazingly low, too. Just \$1250. Even less in OEM quantities.

AXIOM
AXIOM CORPORATION

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CIRCLE 118 ON INQUIRY CARD

**16k-Bit Static RAM
Utilizes 3- μ m Technology**

Organized as 2k x 8, and providing a max access time of 200 ns and max power dissipation of 660 mW, the MSM2128-1 is a monolithic, fully static

RAM requiring no clocks or refresh. This 16k-bit RAM from OKI Semiconductor, 1333 Lawrence Expy, Suite 401, Santa Clara, CA 95051, is designed, through the use of electron beam lithography, to attain a 3- μ m technology.

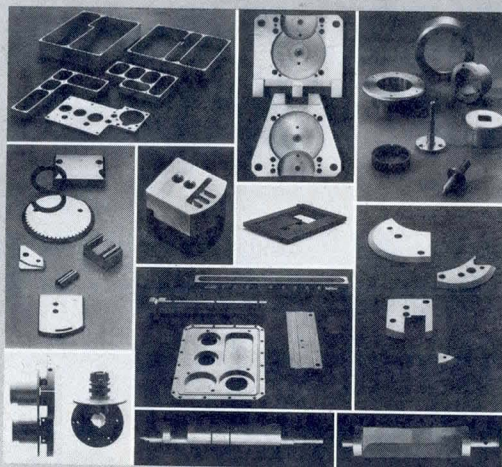
Characteristics of the chip include TTL-compatible I/O, operation from a single 5-V power supply, and common data I/O pins with 3-state outputs. Utilizing advanced N-channel silicon gate MOS technology, it is compatible with the MSM2716 16k-bit EPROM from the same manufacturer and replaces four MSM2114 4k static RAMs.

The RAM is offered in a 24-pin dual inline ceramic package, with operation guaranteed from 0 to 70 °C. Absolute maximum ratings require that supply, input, and output voltages with respect to ground remain between -0.5 and 7.0 V. Power dissipation must not exceed 1.0 W.

Circle 516 on Inquiry Card

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**Vacuum Fluorescent
Display Driver
Joins Controller Family**

The COP470 is a display driver that directly interfaces to multiplexed 4-digit x 8-segment vacuum fluorescent displays. It is a peripheral member of the COPS™ microcontroller family from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, and is compatible with all members of that family.

Data are loaded serially and held in internal latches. The device includes an onchip oscillator to multiplex four digits of 8-segment display and may be cascaded and/or stacked to drive more digits, more segments, or both. With the addition of external drivers, it also provides a convenient means of interfacing to a large digit LED display.

This IC needs no refresh from the processor, introduces no glitches on outputs when loading data, and provides a programmable display brightness. It can be operated from 4.5- to 9.5-V supplies and the outputs switch 35 V without external resistors. The package is a 20-pin DIP.

Absolute maximum ratings require that voltage stay between 0.3 and -35 V at the display outputs and between 0.3 and -20 V at all other pins. The permissible temperature range is 0 to 70 °C in operation and -65 to 150 °C in storage. □

From concept...to prototype...to production. Faster. With Multiwire® circuit boards.

Just give us a net list and board layout. You'll get a computer-generated design, prototypes, and delivery of production boards in a fraction of the time you would expect.

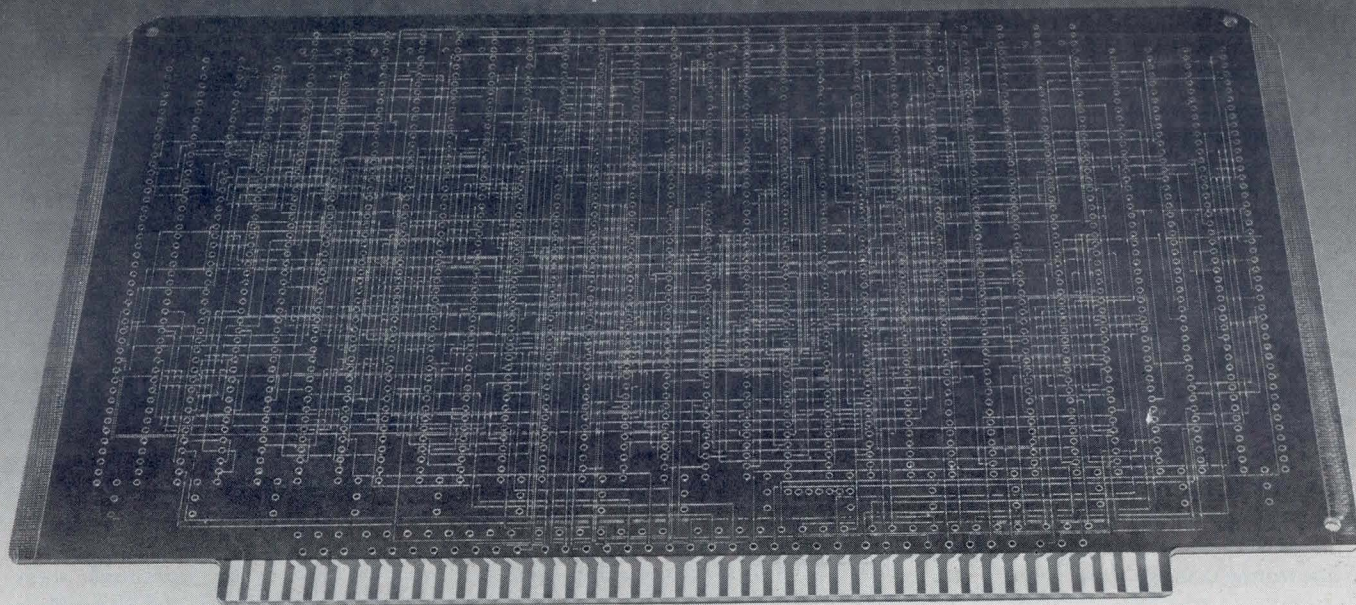
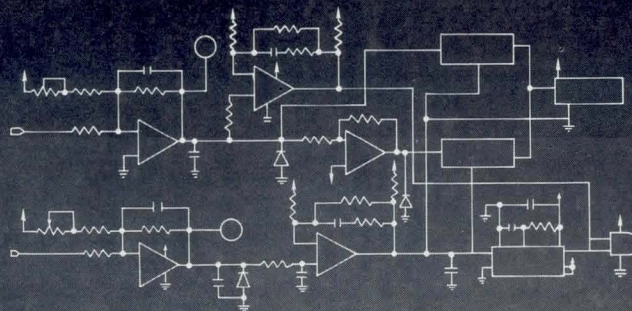
The Multiwire process is simply *faster* than multilayer... all the way from board design through manufacture to function. Especially working with high density interconnects.

A Multiwire circuit board is a pattern of insulated wires bonded to an epoxy glass substrate by a high-speed CNC machine, and

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Multiwire is new. And different. And it has been proved in demanding applications by over 200 of the world's leading electronic manufacturers.

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Licenses to design and manufacture Multiwire circuit boards are available from PCK Technology Division, Kollmorgen Corporation, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone: (516) 448-1166.

Call your nearest Multiwire producer for full details
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Dallas/Ft. Worth
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Inquiry Card

Middle Atlantic
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Ocean, NJ 07712
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TWX 710 723-4620
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Canada, Minn., Utah, upstate N.Y.
Space Circuits, Ltd.
P.O. Box 367
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Waterloo, Ontario
N2J4A4
(519) 742-5896
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PRODUCT FEATURE

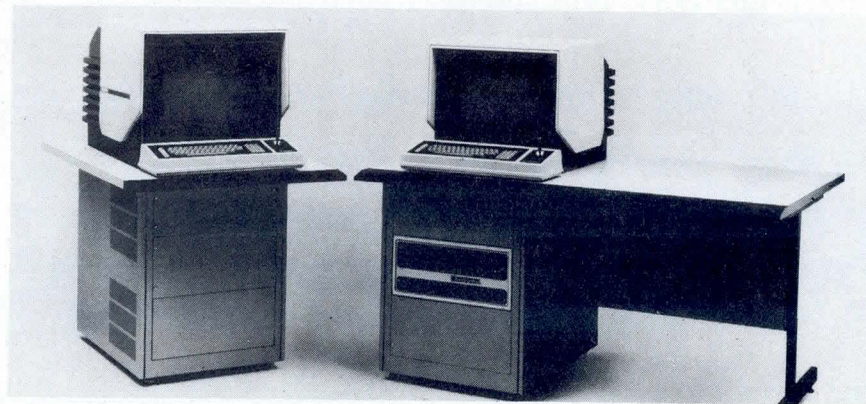
Dual Output Computer Graphics System

Both dynamic design and analysis requirements for computer aided design and manufacturing as well as laboratory applications can be met by a unified system that uses a single controller for both a black and white vector refresh display and a color raster display. Claimed by Megatek Corp to be the "world's first and only dual output computer graphics system," the Whizzard 7290 is based on the 7200 Graphics Engine™. The latter unit consists of host computer interface, graphics processor, vector memory, and optional 2- and 3-dimensional transformation modules. It drives both an analog vector generator, which supports one or two electromagnetic deflection monitors, and a digital vector generator, which supports one or two color raster monitors.

The dual output graphics system can be used with nearly any mini or medium scale computer that has high speed parallel interfacing, such as those from Digital Equipment Corp, Data General Corp, or Prime Computer. Further operator interaction is provided by intelligent peripherals and hardcopy output options.

Functional Description

Display commands are transferred between graphics system and host computer in either programmed input/output (I/O) or direct memory access modes. System design includes dual multidirectional buses. A 32-bit wide, 3-state graphics bus handles data transfers for vector calculations and refresh, and a 16-bit wide peripheral bus ensures that high speed data transfers are not degraded by I/O transfers and routine interrupt servicing. Vector memory modules contain from 16k to 48k words of 32-bit random access memory for display



refresh and can accept 2k words of 32-bit programmable read only memory.

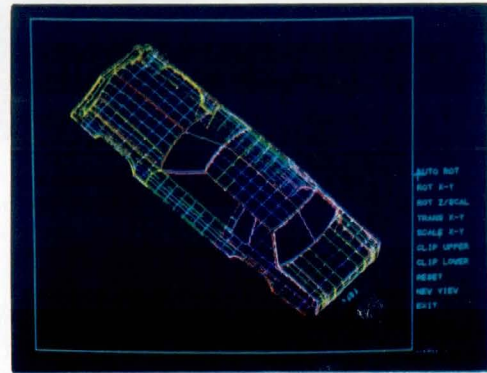
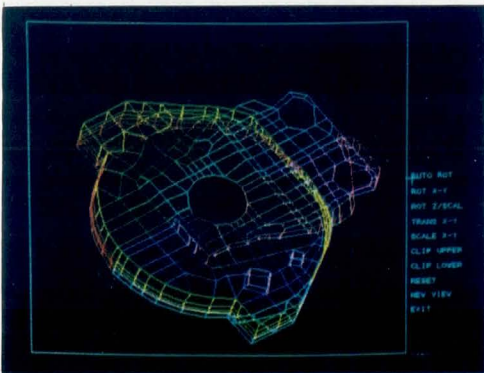
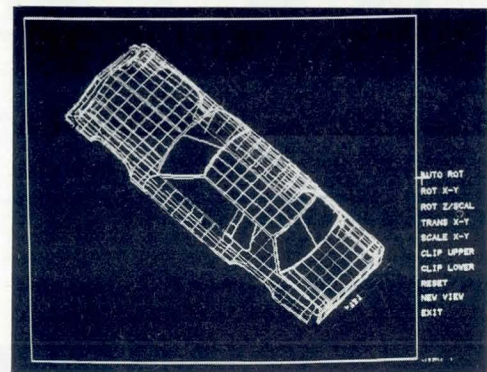
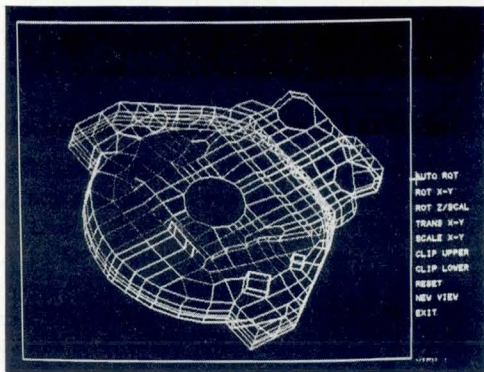
Each analog vector generator can control two electromagnetic deflection type black and white or color monitors having either the same or different images. A first in, first out (FIFO) buffer optimizes maximum average throughput and enables the digital portion of the system to match the fast analog circuitry. High speed normalization circuits ensure constant vector intensity regardless of vector length. An adaptive timing technique assures precise end-point matching and vector quality. Throughput is maximized by reducing setup time on short vectors.

One or more double-buffered bit planes of raster memory along with timing, control, and video output circuitry are included to assist the digital vector generator. This generator performs a high speed rasterization of the vector information received from the Graphics Engine and writes the result into raster memory. The video output circuitry reads from the raster memory to drive the raster monitors. Writing speed of the digital vector generator allows realtime dynamics, with an average writing time of only 160 ns/pixel.

The graphics processor is built around a 32-bit wide bipolar bit slice microprocessor that controls access to the graphics display list stored in the memory module. This microprocessor interprets the display data, controls microcode implemented graphics functions, and prepares X-Y coordinate pairs for input to the vector generator FIFO memory. Included in the instruction set are a variety of 2D and 3D vector formats, selective erase, textured and blinking lines, 16 levels of intensity and beam penetration color control on vector refresh displays, 16 colors and color lookup table control on raster displays, hardware character generation with optional user definable symbol sets, and 12-bit (4k x 4k) virtual space addressing.

A single software package, WAND 7200, supports all system hardware. The package is written entirely in ANSI FORTRAN and follows CORE guidelines established by ACM SIGGRAPH. It provides multilevel functionality using high efficiency work station level routines as well as more convenient user routines that operate in world coordinates. Operators may move from small to large systems, from stroke to raster systems, or from high speed parallel to remote terminal configurations without the need to modify

Combines Vector Refresh and Color Raster Displays



Dual output 7290 computer graphics system combines separate vector refresh (top) and color raster displays in one system, sharing common software

and hardware—including host computer interface, graphics processor, vector memory, and optional hardware modules and peripheral devices

existing application programs or change programming techniques for new applications. One set of FORTRAN programs can support both vector refresh and color raster displays using both parallel and serial communications interfaces to 9600 baud.

Options to the system include a microprocessor based intelligent peripheral control unit that acts as an interface for keyboards, joysticks, data tablets/digitizers, and asynchronous consoles; a "pick" module, an in-

telligent processor that interfaces a lightpen and/or a digital comparator to the system and provides two modes of interactive processing; function switches and control dials that provide 2-way general purpose I/O for communication with the graphics processor through an intelligent control unit; and a microprocessor based hardware vector to raster converter for fast hardcopy or film output without any software sorting or tedious host conversions.

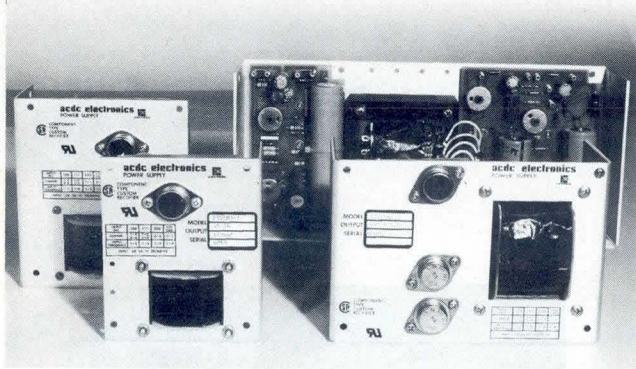
Price and Delivery

A sample configuration Whizzard 7290 system, including one 21" vector refresh monitor and one 21" color raster monitor, is priced at less than \$40,000. Systems are available for immediate delivery. Megatek Corp, 3931 Sorrento Valley Blvd, San Diego, CA 92121. Tel: 714/455-5590.

For additional information circle 199 on Inquiry Card.

PRODUCTS

Open Frame Linear Power Supplies Meet Both U.S. and International Requirements



Eighty-three separate models of competitively priced single-, dual-, and triple-output open frame linear power supplies in 18

different industry standard case sizes are said to include many features usually found only in high-priced modular units. All meet isolation requirements of VDE Spec 0804 and include transformers for worldwide voltage requirements. All models are UL and CSA approved and have programmable outputs on triples and duals for greater flexibility in microprocessor applications. Overvoltage protection is standard on all 5-V outputs, and optional from 4.5 to 32 V on all other models. Ripple performance is improved over other open frames, down from 20 mV to 3 mV pk-pk, and output operating temperature is to 50 °C, up from 40 °C. Remote sense is standard on all 30-W and higher models. Other features include open sense lead and reverse polarity protection; on triples, outputs 2 and 3 continuously adjustable from 9 through 15 V and output 3 programmable to -5 V; a ceramic, pretested regulator chip on a socket; metal film resistors; and vacuum impregnated transformers. **ACDC Electronics**, 401 Jones Rd, Oceanside, CA 92054.

Circle 200 on Inquiry Card

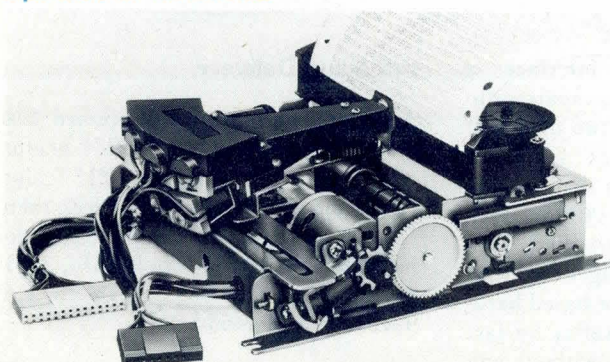
Analyzer Checks Digital Chips In-circuit with 100% Accuracy



ROMs, RAMs, P/ROMs, microprocessors, and other digital chips can be checked with 100% accuracy probability for single-bit and 99.998% for multi-bit errors, without removing the devices from their circuits. The Signature II circuit analyzer consists of a dc to 100-MHz data probe, control probe, associated data compression, memory, and digital display circuits within an emi shielded metal case. In operation, once a repetitive mode of operation is established, the bit stream at each microprocessor active node, associated memory, and logic forms a unique repeating pattern that is common to all similar units that are operating normally. Color coded control probe leads connect to start, stop, and clock signals of the unit under test; choice of rising or falling edges is switch-selectable. Data necessary to create a window are acquired by the control probe. Then a repeatable data stream, detected by the data probe, is fed to a circuit that compresses, stores, and displays it as a 4-digit hexadecimal signature. This signature is compared with up to 256 previously stored signatures from that node. **Kurz-Kasch, Inc**, 2271 Arbor Blvd, Dayton, OH 45439.

Circle 201 on Inquiry Card

40-Col Dot Matrix Impact Printer Operates at 1.2 Lines/s



A variety of print material—3.5" (8.9-cm) adding machine tape, double-stock carbonless tape for simultaneous preparation of

file and removable copies, fan folded paper, and up to 4.5" (11.4-cm) wide gummed or pressure sensitive labels—can be used on the model DP-824. Max print width is 3.3" (8.4 cm) on all. The unit prints up to 40 col at 1.2 lines/s and is claimed to have a life expectancy of more than 2M lines. Life expectancy of the replaceable printhead is about 15M char. Any alphanumeric font, including Japanese, Arabic, Cyrillic, and other non-Roman scripts, can be reproduced, depending on the customer's control unit. Typ matrix size, under software control, is 5 x 7, 7 x 7, or 9 x 7. Char size in a 5 x 7 matrix is 0.071" (1.8 mm) W x 0.114" (2.9 mm) H, at line spacing of 0.167" (4.24 mm). A single 24-Vdc motor drives printhead, paper feed, and ribbon mechanism. Printhead wires are driven by solenoids. The device can be mounted horizontally or vertically and attaches electronically via 2 connectors. Size is 6.265" W x 5.792" D x 2.246" H (159 x 147 x 57 mm); weight is 1.8 lb (816 g). **Star Micronics, Inc**, 200 Park Ave, New York, NY 10166.

Circle 202 on Inquiry Card

The First Family of Mark Sense Readers



...including the one chosen
by the New York Stock Exchange

The Complete Line

If you're looking for a mark sense reader, the place to start is Chatsworth Data, a pioneer in the art. We have small ones, large ones, sophisticated ones, simple ones, versatile ones, and microprocessor-controlled ones... with interfaces and options for most computers and terminals. Our standard readers can satisfy the most diverse requirements.

Stock Brokers' Delight

Take our Model 4900 (center rear). Originally designed for the New York Stock Exchange, this intelligent reader will communicate with NYSE computers to provide data used to drive ticker tapes throughout the world. The versatility of the 4900 with its microprocessor and built-in printer to serialize, plus its three output stackers, make it ideal for a multitude of different applications.

The Pioneers

Our 4000 series has been a mainstay in industrial, educational and business systems for a decade.

Model 4400 (left) can handle cards and forms up to 8½ inches wide. So, in addition to the mark sense area, a large space is provided to write or type additional notes. The 4200 (right) reads single-side reflective card data containing timing marks. Model 4300 and 4800 are variations of the 4200. The former reads both standard tabs and timing marked cards, while the 4800 scans both sides of timing marked cards simultaneously.

The Mighty Mite

Last but not least, there's our incredibly compact MR500 (center front). Priced at just \$750, this little beauty comes with interfaces to most personal computers. It provides automatic turn-on and card feed, and accepts any length card, making it perfect for education and business applications.

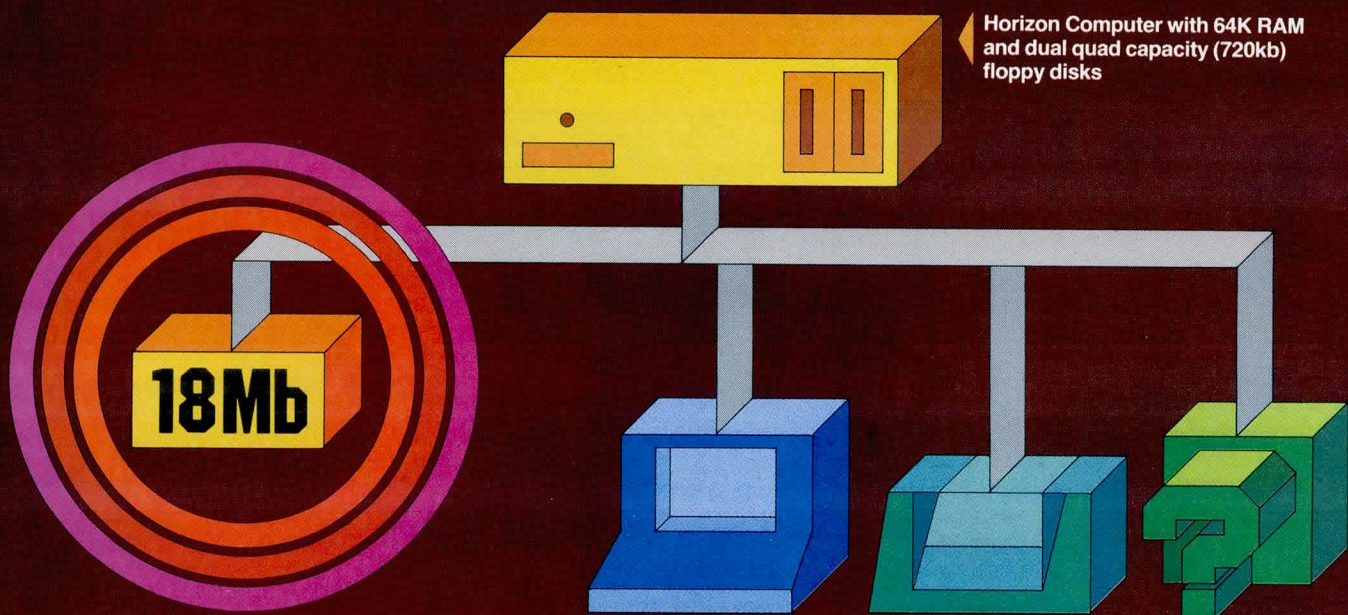
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North Star now gives you hard disk capacity and processing performance never before possible at such a low price! Horizon® is a proven, reliable, affordable computer system with unique hardware and software. Now the Horizon's capabilities are expanded to meet your growing system requirements. In addition to hard disk performance, the Horizon has I/O versatility and an optional hardware floating point board for high-performance number crunching. The North Star large disk is a Winchester-type drive that holds 18 million bytes of formatted data. The North Star controller interfaces the drive(s) to the Horizon and takes full advantage of the high-performance characteristics of the drive. Our hard disk operating system

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Software Is The Key!

The Horizon's success to date has been built on the quality of its system software (BASIC, DOS, Pascal) and the very broad range and availability of application software. This reputation continues with our new hard disk system. Existing software is upward compatible for use with the hard disk system. And, with the dramatic increase in on-line storage and speed, there will be a continually expanding library of readily available application software. For further information and OEM prices, please contact the OEM Sales Department at North Star Computers, Inc.

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Yes!! Please Send More Information On North Star's
18 Megabyte Hard Disk System!!

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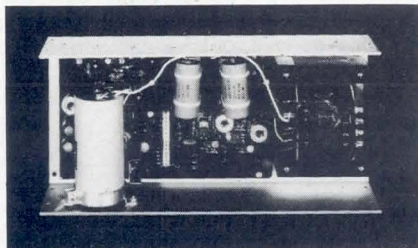
PRODUCTS

PORTABLE PRINTING TERMINAL

Thermal printer 2675A operates at 120 char/s and produces 132 col on 8.5" (21.6-cm) wide paper. It also has 40-char/line expanded mode. Char are 7 x 11 dot matrix. Full 128 ASCII u/lc char set is std; optional sets are available. Keyboard has 8 user-definable function keys. Integral dual cartridge drive can store 320k bytes/tape. Optional built-in 300-baud modem permits direct connection to phone line and features auto dial and auto answer. Communication is asynchronous point to point at up to 9600 baud. I/O buffer permits online interactive editing. Unit weighs 22 lb (9.9 kg). **Hewlett-Packard Co.**, 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 217 on Inquiry Card

FLOPPY DISC POWER SUPPLIES



Open frame CP 564 power supplies are specifically designed for Micropolis, Century, Shugart, and Winchester floppy disc drives. Inputs are 115/230 \pm 10% Vac, 47/440 Hz. Output #1 is 5 Vdc at 6 A with overvoltage protection; output #2, -12 Vdc at 1 A; and output #3, 24 Vdc at 4.2 A/5.5 A peak. Line regulation for 10% line change is \pm 0.02%. For a 50% load change, load regulation is \pm 0.02% and transient response, 30 μ s. **Condor, Inc.**, 4880 Adohr Ln, Camarillo, CA 93010.

Circle 218 on Inquiry Card.

SMALL SYSTEM DISPLAY STATION

Attached through workstation controller or an IBM 5251-12 cluster controller, 2051-11 display station is fully compatible with System/34, /38, Series 1, and 5250. "Cablethru" feature allows attachment of additional display stations or printers in a series. 15" (38.1-cm) monitor has 24-line by 80-char display of 8 x 16 dot matrix characters. 25th line provides operator prompting and system status data. Optional extension cable allows separate keyboard to be placed up to 10 ft (3.04 m) from monitor. Low power consumption eliminates need for cooling fan. **Memorex Business Systems Div.**, 3015 Daimler St, Santa Ana, CA 92705

Circle 219 on Inquiry Card

MULTIPLE OUTPUT SWITCHER

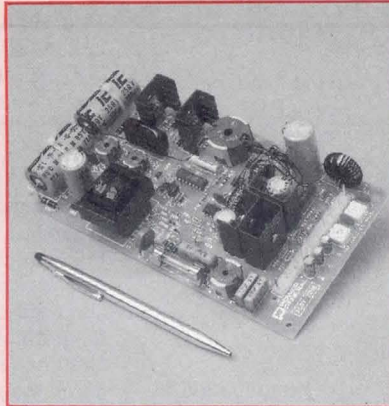
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MODEL 4027-2

5V @ 4A, \pm 12V @ 0.4A
(other output voltages available)

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- Up to four outputs, 30 watts, 0.1 to 0.5% Regulation
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CIRCLE 125 ON INQUIRY CARD

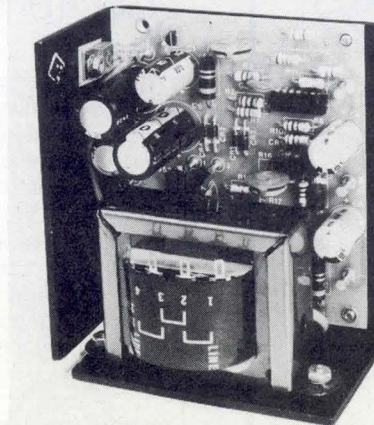
10-W DUAL OUTPUT POWER SUPPLY

An addition to the "Ugly" line of micro-processor power supplies, μ PS18 dual output unit provides nominal 10 W on both outputs. Voltages are available in \pm 12 V at 0.7 A and \pm 15 V at 0.5 A. The supply is built for positive and negative operation and is supplied with dual 115/230 Vac input. The open frame unit has case size of 4.75 x 4.0 x 2.25" (12.1 x 10.2 x 5.7 cm). **Elpac Power Systems**, 3131 S Standard Ave, Santa Ana, CA 92705.

203-DOT/IN THERMAL PRINTHEAD

Integrated thermal printhead KH106 produces approx 203 dots/in (8/mm). A 1-piece 8.5" (21.6-cm) wide heating element creates numerals, char, lines, and solids of any desired size, width, and density. Dot size is 0.0041 x 0.0137" (0.104 x 0.35 mm) and print speed is 4 ms/line max. All enabling electronics are integrated into the head in 40-pin IC flat-packs. Specified life is 30M pulses or 20-mi (32-km) paper length, whichever comes first. Op temp range is -5 to 45 $^{\circ}$ C. **R-Ohm Corp.**, PO Box 19515, Irvine, CA 92713.

Circle 221 on Inquiry Card



Circle 220 on Inquiry Card

DISC CONTROL UNIT

Either 2 or 4 independent control unit paths for data transfer and file positioning commands can be provided by the 8880 disc control units. The 8880-12, with 2 independent storage directors, and the 8880-14, with 4, each have dedicated microprocessor and power supply and isolated director functions. Configurations include 1-, 2-, 4-, and 8-channel interface switching. **Storage Technology Corp.**, 2270 S 88th St, Louisville, CO 80027.

Circle 223 on Inquiry Card

PRODUCTS

DATA TERMINAL WITH BAR CODE READING CAPABILITIES

An attached lightpen provides automatic data entry capability to the model 4610 bar code reader. A variety of printer bar code patterns—including 2 of 5, interleaved 2 of 5, alphanumeric 3 of 9, Codabar™, UPC, NDC, IBM delta distance, AS-6, and AS-10—can be read. Internal memory, multiplexing, and daisy chain interconnection to existing systems, 2 serial T/R ports, and 24 parallel lines for special user requirements are std features. Enhancements can provide alphanumeric display, numeric keypad, or alphanumeric keyboard. **Accu-Sort Systems, Inc.**, Telford, PA 18969.

Circle 203 on Inquiry Card



DATA ENTRY/VOICE RESPONSE UNIT

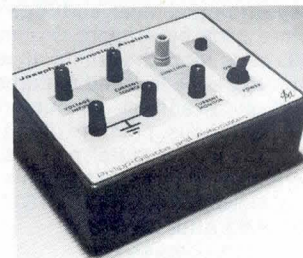
A gp man-machine interface to computer or communications systems, the ADC 1550 audio/data communications unit provides a realistic sounding computer voice response to remote terminal devices. One unit handles as many as 8 I/O lines simultaneously with Touch-Tone receiver data sets and provides up to 240 words in 120 s (32 words/16-s increment). ASCII

output speeds are 110, 150, and 300 baud. Terminals are multiplexed through a single serial synchronous or asynchronous communications channel. Voice response is made up of prerecorded and digitally encoded words or phrases. TTY protocol is RS-232-C; BSC3 protocol is IBM 3270 subset. **Wavetek Data Communications**, 9045 Balboa Ave, San Diego, CA 92123.

Circle 204 on Inquiry Card

JOSEPHSON JUNCTION ANALOG

Realtime simulation of Josephson junction action, but at slower speeds and larger voltages than for true conditions, allows researchers to preview actual behavior and modify circuits quickly. In comparison with a true cryogenic Josephson junction, which works at 10 to 15



ps and at approx 3 mV, the analog switches at speeds of 100 μ s and runs at 1 V. Because it simulates superconducting at room temperature and at speeds and voltage that can be observed and analyzed on common test equipment, but permits circuit parameters to be changed readily, the JA-100 Josephson junction analog can be used as a true circuit element in developing cryogenic circuit prototypes, as well as for classroom or lab demonstrations. **Philipp-Gillette and Associates**, Box 1511, Beaverton, OR 97075.

Circle 205 on Inquiry Card.

KYNAR® gives you another advantage.

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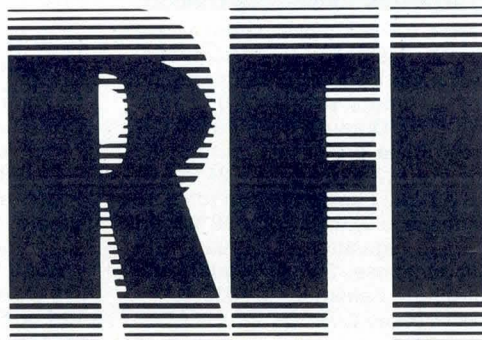
KYNAR PVDF was born to handle solvents and corrosives in chemical plants. You get that protection in KYNAR wire insulation. Resists UV and nuclear radiation, too. Get full information. Write KYNAR, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. Or call (215) 587-7514.



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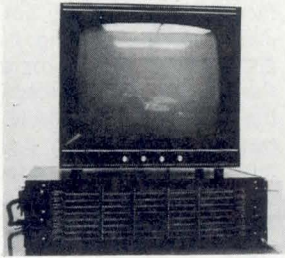
CIRCLE 127 ON INQUIRY CARD

PRODUCTS

REALTIME IMAGE PROCESSING SYSTEM

RIP-260, a high speed arithmetic computation unit, operates with a gp computer for realtime image processing at a raster scan display resolution of 256 lines x 256 elements, with 8 bits (256 levels) of intensity (grey scale). Arithmetic operations on an entire 65k image memory array require 16.7 ms. Minimum assembly includes a std interface to either a DEC PDP-11 series Unibus or a DEC LSI-11 Q-Bus, a memory management board, processor exchange board, pipeline image processor, two image memory arrays, master timing, and a digital to video converter. Image memory is directly addressable through a block of memory addresses. **Recognition Concepts, Inc.**, 916 Forbes St, Lakeport, CA 95453.

Circle 206 on Inquiry Card.



COMPUTER CONTROLLED DATA COMMUNICATIONS STATION

Intended for systems in which SDLC/HDLC/X.25 is implemented as a discrete unit, the Multibus compatible DTSX module offers up to 64k-baud data bandwidth. An RS-232/V.64

interface is provided for modem connection. Communication hardware includes I/O memory mapping of RAM extended by bank switching capability. Space is available for up to 32k bytes of onboard program. 16k or 32k bytes of dual-ported dynamic storage are provided onboard. Software package SS1 contains programs for HDLC; SS2 includes SS1 plus 255 simultaneous virtual circuits, a set of transport station primitives for application usage, full implementation to CCITT X.25, and flow control management at all levels. **Symicron Ltd.**, 44 Little Bornes, Dulwich, London SE21 8SE, England.

Circle 207 on Inquiry Card

EXPANDED IN-CIRCUIT PCB TESTING CAPABILITY

When used with the company's Troubleshooter 800 in-circuit inspection system, the Data Director expands the variety of digital LSI components that can be checked. It is of value primarily in testing complex devices that require sequential stimuli of enable, clock, and other control lines, as well as manipulation of data and address buses. A high level language allows the programmer to talk to a device with its own mnemonic instructions. Support includes a library of test template programs for several popular microprocessor families. After the operator defines a device test sequence, the test unit generates the proper sequence of control and test stimuli. Data and address lines may be addressed in a fixed byte width with the stimulus program made up of a sequence of device instructions supplied from the device instruction set. **Zehntel, Inc.**, 2625 Shadelands Dr, Walnut Creek, CA 94598.

Circle 208 on Inquiry Card

MINI-STEPS MAXI-STEPPERS

PM and VR steppers — responsive and precise — with slewing rates to 20,000 steps/sec. and higher. We offer an unlimited range of step angles, frame sizes and configurations. And high torque/size ratios. Options include: dampers, heat sinks, encoders, pulse sources, drivers, preset indexers, gearheads, and more. Standards and specials — the best of both.

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Motor Div. of Electro Audio Dynamics Inc. Dover, N. H. 03820
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EAD, Holtzer-Cabot and Janette motors

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KYNAR PVDF wire insulation gives you excellent abrasion and cut-through protection even though you may pay less for KYNAR than other fluorinated plastics. Get full information. Write KYNAR, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. Or call (215) 587-7514.



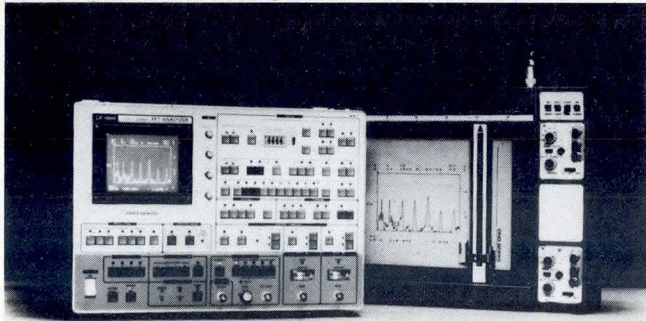
PENWALT
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HEALTH PRODUCTS

*KYNAR is a registered trademark of Pennwalt Corporation for its polyvinylidene fluoride.

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

DUAL CHANNEL FFT ANALYZER WITH 67k-BYTE USER STORAGE



The Ono Sokki CF-500 dual channel FFT sound and vibration analyzer displays 28k 12-bit words on a CRT display. Mass storage capacity is 67k bytes. Analyzed frequency data are continuously stored realtime in 28 blocks; any desired block can be simultaneously displayed on the CRT. Std programs include 3-dimensional displays on an optional CX-445 X-Y recorder. The analyzer operates on a realtime basis in dual channels by analyzing sound and vibration over a wide range, from dc to 1 Hz and to 20 kHz, by measuring transfer functions and continuously recording long period waveforms. Multiple functions include digital wave memory, $\frac{1}{3}$ octave noise analysis, 3-dimensional power spectrum recording, coherence functions, and transfer functions. Linear, exponent, and peak values are averaged to improved S/N ratios. **Shigma, Inc.**, 80 Martin Lane, Elk Grove, IL 60007.

Circle 209 on Inquiry Card

LOW COST LOGIC ANALYZER

Two 16-channel fixed threshold probes for 0- to 15-V logic families, a 32-channel by 250-word deep logic state analyzer, an auxiliary memory for storing up to eight reference tests in RAM and UV P/ROM, software signature analysis on all 32 channels, and a comprehensive logic analysis self-study course that includes a test board to simulate microprocessor address and data flow for training purposes are all part of the PI 532-SP. The unit collects realtime data from a system bus running as fast as 5M operations/s and displays captured data in hexadecimal on front panel readouts, or in both hexadecimal and binary on an ordinary scope or video terminal. Octal display capability is optional. Other options include an IEEE-488 interface, and dedicated probes for RS-232 serial communication testing and for monitoring specific microprocessors. **Paratronics Inc.**, 2140 Bering Dr, San Jose, CA 95131.

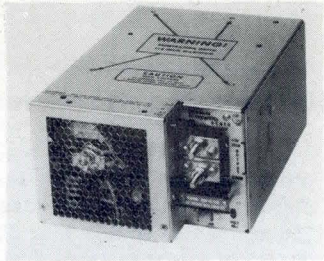


Circle 210 on Inquiry Card.

DIGITALLY PROGRAMMABLE SWITCHING POWER SUPPLY

Model PM 2497, digitally programmable when used with an RS-232 compatible interface, is available in power configurations ranging from 200 to 750 W and is programmable in 256 discrete steps of the rated output voltage. A tracking power good signal option may be specified to indicate when the output is within $\pm 4\%$ of the selected voltage. The power supply can be configured to accept an 8-bit parallel signal for connection to a computer, and a constant current mode version is available. Operation is over an input range of 92 to 138 or 184 to 250 Vdc. The unit provides uninterrupted power under severe brownout conditions and regulates through line dips to 80 or 160 Vrms. If a total input power failure occurs, output voltage will hold up for a min of 30 ms. **Pioneer Magnetics, Inc.**, 1745 Berkeley St, Santa Monica, CA 90404.

Circle 211 on Inquiry Card



CHARACTER MODE VIDEO DISPLAY TERMINAL

PT25, a microprocessor controlled video display terminal for the company's 50 series gp computer systems, features user function keys, auxiliary printer port, and numeric pad. Intended for any application requiring non-buffered, interactive operation, the terminal has an 80-char x 24-line format on a 12" (30.5-cm) diag screen and displays u/lc 8 x 8 dot matrix char. An integral keyboard offers a 14-key numeric pad, 8 function keys, 5 cursor control keys, and the auxiliary port key. Function keys allow users to implement special applications with a single key stroke, and the auxiliary port enables one communication line to provide for both CRT and printer. Other visual features include reverse video, underlining, blinking, and full, half, and zero intensity. A 25th status line on the screen reports the terminal status. **Prime Computer, Inc.**, 40 Walnut St, Wellesley Hills, MA 02181.

Circle 212 on Inquiry Card

RS-232-C COMPATIBLE FLOPPY DISC SUBSYSTEMS

DynaSTOR models 7111 and 7112, plug compatible with all serial asynchronous RS-232-C (CCITT V.24) equipment, are single- and dual-diskette drive subsystems. Data transfer rate is as high as 19.2k baud. Because data are recorded on the diskette in EBCDIC fashion while the code used to communicate is ASCII, software interface exists between the computer and drive programmed in a high level language such as BASIC, FORTRAN, or COBOL. The two models are capable of reading, writing, and initializing diskettes that are fully compatible and interchangeable with diskettes from the IBM 3740 series of systems. Additional std commands include reading the status of the diskettes, duplicating one diskette to another, deleting records, and R/W in binary mode. **Dynalogic Corp Ltd.**, 141 Bentley Ave, Ottawa K2E 6T7, Canada.

Circle 213 on Inquiry Card



Meet two new Printers from Anadex:

Revolutionary!



Introducing two totally new line printers from Anadex - Models DP-9500 and DP-9501 - offering 132/158/176 and 132/165/198/220 columns, respectively, and featuring true high-density graphics under direct control of the data source.

Both models employ a rugged, Anadex-built 9-wire print head life-tested to 650 million characters. Combining long life with high resolution, this new head provides dot resolutions of 72 dots/inch vertical and up to 75 dots/inch horizontal.

The full standard ASCII 96 character set, including descenders and underlining of all upper and lower case letters, is printed bi-directionally on the original and up to 5 crisp copies at speeds up to 200 CPS. Print densities are switch- or data-source selectable from 10 up to 16.7 characters/inch, and all can be printed double-width by communications command.

The three ASCII compatible interfaces (parallel, RS-232-C, and Current Loop) are standard in both models; so interfacing is usually a matter of "plug it in and print." Also standard is a sophisticated communications interface providing control of Vertical Spacing (6 or 8 lines/inch), Form Length and Width, Skip-Over Perforation, Auto Line Feed, and full point-to-point communications capability.

Other standard features are: forms width adjustment from 1.75 to 15.6 inches, shortest-distance sensing logic, self-test, quick-change ribbon cartridge with 6 million character life, and a 600 character FIFO buffer. (An additional 2048 character plug-in buffer is optional).

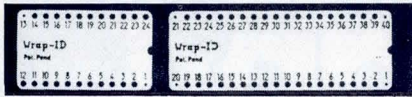
For complete details, quantity discounts and a demonstration, contact Anadex today.



CIRCLE 130 ON INQUIRY CARD

PRODUCTS

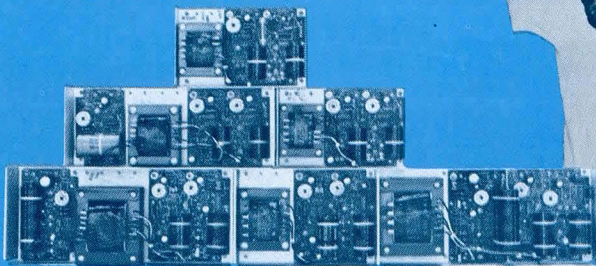
WIREWRAP SOCKET PIN IDENTIFIER



Socket Wrap-ID, a socket sized plastic panel with numbered holes at pin locations, identifies pin numbers on wirewrap sockets. Panels may be marked on for identification of location, IC part number, and function, and then slipped onto the sockets before wrapping. They are available in 14-, 16-, 18-, 20-, 24-, 28-, and 40-pin configurations, as well as sequential bus strips. **OK Machine and Tool Corp.**, 3455 Conner St, Bronx, NY 10475.

Circle 224 on Inquiry Card

Best Buy For Your Buck Power Supply & T-Shirt Promotion



Our prices and specs are as good or better than competition. Prices below and present prices on ALL Condor open frame power supplies are guaranteed thru Dec. 31, 1980. Our delivery (stock to 4 wks.) is better than competition! And a

FREE Condor T-Shirt goes along with every order postmarked by Dec. 31, 1980. Specify S M L or XL. Call or write for FREE CATALOG covering over 150 Condor open frame supplies.

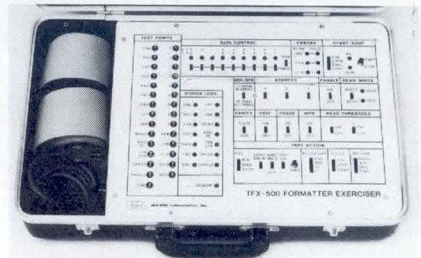
1st Output	2nd Output	3rd Output	Model	Price(1-9)
HARD DISC - Micropolis, Century, Shugart, Winchester				
+5V@9A	-5Vor-12V@1A	+24V@.8/4.5A PK	FCBB-70W	\$120.00
+5V@6A	-12V@1A	+24V@4.2/5.5A PK	CP564	144.95
MINI-FLOPPY - 5 1/4" - Shugart, Pertec, BASF, Siemens				
+5V@.7A PK	+12V@1.1/1.7A PK	N/A	FAA512	\$39.95
+5V@2A	+12V@4A	N/A	FBB512	74.95
DISC DRIVE & PRINTER SERIES - Persci, Shugart, Wangco, CDC				
+5V@2A	+5V@.5A	+24V@1.5/1.7A PK	FBAA-45W	\$69.95
+5V@3A	+5V@1A	+24V@3A/3.5A PK	FCBB-90W	91.95
+5V@3A	+5V@1A	+24V@5A/6A PK	FNBB-140W	120.00
+5V@3A	+12V@1.7A	+24V@3A/3.5 PK	FCBB512	91.95
N/A	N/A	+24V@2.4/6A PK	FC24-2.4	55.95
N/A	N/A	+35V@1.5/6A PK	FC35-1.5	55.95
ROCKWELL - AIM 65 Microprocessor				
+5V@2A	+24V@.5/2.5 PK unregulated	N/A	AA524-AIM65	\$44.95

CONDOR INC.

DC Power Supplies
4880 Adohr Lane, Camarillo, CA 93010
(805) 484-2851

TAPE FORMATTER EXERCISER

Cable-end adapters make the TFX-500 usable with all microstreamer-formatter interfaced drives, and such dual-mode embedded formatters as Cipher, Pertec, Kennedy, Datum, and Perkin-Elmer. Unit can be operated manually or in program mode. It has 15 sections of test points and LED indicators for all signals from the formatter. From 1 to 8 linked drives can be tested. Tester operates on 115/230 Vac, weighs 10 lb (4.5 kg), and measures 17 x 10 x 4.5" (43.2 x 25.4 x 11.4 cm). **Wilson Laboratories, Inc.**, 2237 N Batavia St, Orange, CA 92665.



Circle 225 on Inquiry Card

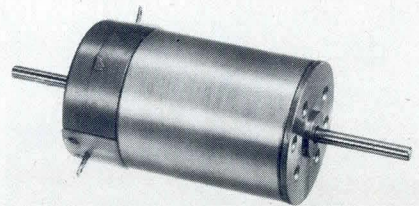
LETTER QUALITY COMPUTER PRINTER

Intelligent, daisy wheel Typewriter 221™ has 5 built-in microprocessors for complete text formatting including right justify and proportional spacing. It is computer compatible and uses a parallel Centronics interface; RS-232-C and IEEE-488 interfaces are available. Unit can print white on black background for highlighting critical data. Alphanumeric display shows current line, column position, and lines remaining to end of page. Device can also function as advanced electronic typewriter. **Howard Industries, Inc.**, 2031 Cerritos Ave, Bldg 7K, Anaheim, CA 92806.

Circle 226 on Inquiry Card

BIDIRECTIONAL DC MOTORS

Intended for use in small printer carriage and tape drives and other servo and drive related applications, the series 6000 dc motors include ferrite PM and iron-core rotor, silver graphite brushes, and a max speed of 10,000 r/min. Stall torque is 10 to 19 oz-in (0.07 to 0.13 N·m) and torque constant is 2.8 to 6.0 oz-in (0.02 to 0.04 N·m/A). Options include skewed armature and rfi suppression. **Transicoil Inc.**, subsidiary Portescap U.S., 31 Fairfield Pl, West Caldwell, NJ 07006.



Circle 227 on Inquiry Card.

The Idea:

To offer OEM's a full-featured graphics display terminal for about half the comparable cost.

It's a great idea if you can get it from the idea stage to the reality stage. Digital Engineering did just that with a concept called Retro-Graphics.[™]

Retro-Graphics works like this. A printed circuit card designed by Digital Engineering plugs into Lear Siegler's ADM-3A or ADM-3A+ Dumb Terminal.[®] Installation takes minutes. There is no soldering. No special tools. No service brigade. Once in, what was before an alphanumeric workhorse is transformed into a versatile graphics powerhouse.

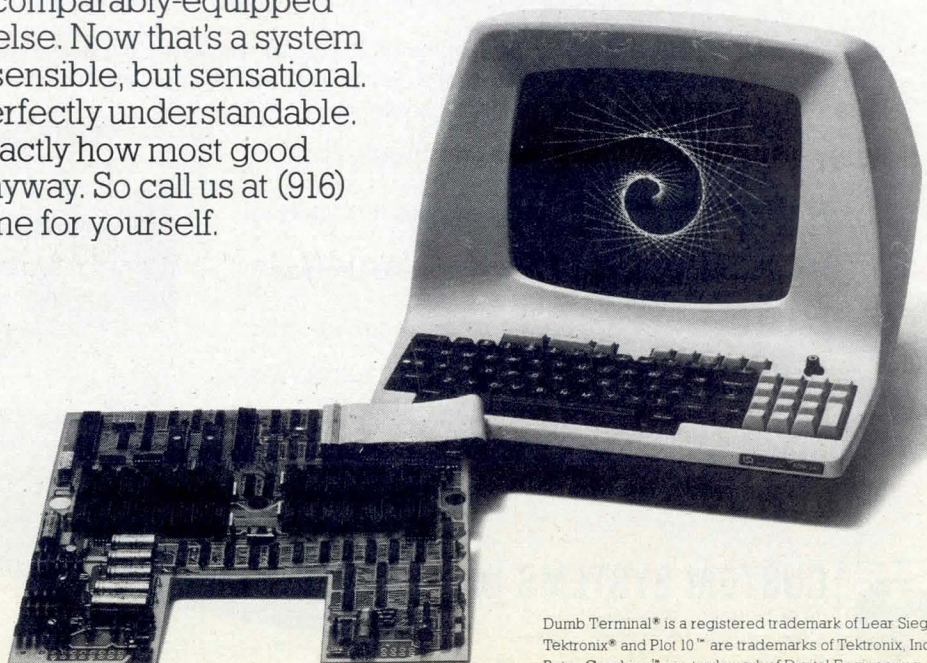
How versatile? Very. You get full vector drawing and point plotting capabilities. Bar charts. Pie diagrams. Histograms. Function plots. You get high light output, selective erase, 512 x 250 "flicker free" plotting grid and, most important, complete compatibility with Tektronix[®] Plot 10[™] software.

Retro-Graphics is a powerful idea. And half of its power is in its price. Because our RG-512 card and the Dumb Terminal, *together*, are about half the price of a comparably-equipped terminal from someone else. Now that's a system alternative that isn't just sensible, but sensational.

Skeptical? That's perfectly understandable. Frankly, skepticism is exactly how most good ideas are discovered, anyway. So call us at (916) 920-5600 and discover one for yourself. Retro-Graphics.

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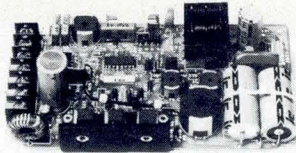
Dumb Terminal[®] is a registered trademark of Lear Siegler, Inc.
Tektronix[®] and Plot 10[™] are trademarks of Tektronix, Inc.
Retro-Graphics[™] is a trademark of Digital Engineering, Inc.

PRODUCTS

30-W SWITCHING POWER SUPPLY

Available in 15-oz (0.425-kg) PCB, 1.5-lb (0.68-kg) open frame, or 1.7-lb (0.78-kg) completely enclosed aluminum housing form, the 1030 series power supplies provide 5 Vdc at 6 A and are adjustable from 4.5 to 5.5 V, over an ambient temperature range of 0 to 50 °C with a 2%/°C derating at 71 °C. The input offers pin strappable voltage ranges of either 85 to 130 Vac or 170 to 260 Vac at 47 to 470 Hz. An rfi input line filter is std. Other basic specs include 30-mV pk-pk max output ripple and noise, 0.1% line and load regulation, $\pm 0.02\%/^{\circ}\text{C}$ tempco, 80% efficiency, and 200- μs transient response recovery to 1% of the final value. Over-voltage protections and output current limiting are provided. **Power General**, 152 Will Dr, Canton, MA 02021.

Circle 214 on Inquiry Card



OPEN FRAME SWITCHING POWER SUPPLIES

Series 19 ValuSwitcher™ dc power supplies are available in 50-, 100-, 150-, 200-, 300-, and 400-W open frame configurations. Outputs are 5 V regulated primary as well as ± 12 or ± 15 V and -5 or 24 V unregulated. Strappable ac input is 90 to 132 or 180 to 264 Vac, 47 to 440 Hz with brownout set at 85 or 170 V. Load

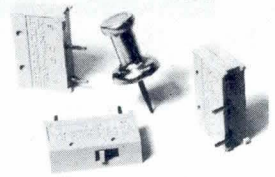
regulation for regulated outputs is $\pm 0.2\%$ for a 10 to 100% load change and $\pm 3\%$ for a 40 to 100% load change on unregulated outputs. Line regulation for both regulated and unregulated models is a $\pm 0.2\%$ variation from nom set at 90 to 132 Vac with all outputs at 50% of rated load. Options include power fail and overvoltage protection. **Powertec**, 20550 Nordhoff St, Chatsworth, CA 91311.

Circle 215 on Inquiry Card

SUBMINIATURE LOW CURRENT PCB CIRCUIT BREAKERS

A bimetallic element used in low current circuit breakers designed for overload protection on PCBs is able to withstand current buildups caused by capacitors. Because they are not polarized, the devices can be used with either ac or dc, up to 24 V max. The breaker isolates the line at fault and protects other components from damage. A slide reset switch indicates when a device has tripped. Right angle mounting versions are available for edgeboard use. Trip ranges include 100, 250, and 500 mA, 1.0, 1.5, and 3.0 A. Size is 0.70 x 0.44 x 0.20" (17.8 x 11.2 x 5.1 mm). Applications include power supplies, test instruments, and communications circuits. **Alco Electronic Products, Inc.**, 1551 Osgood St, N Andover, MA 01845.

Circle 216 on Inquiry Card



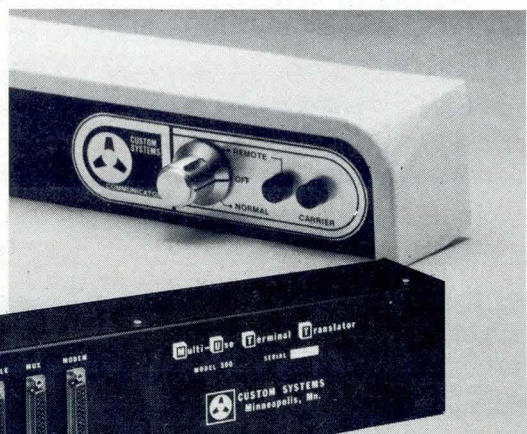
SYSTEM OEMS... THINK CUSTOM SYSTEMS!

Our MUTT* gives you instant access
to your customers' systems

The Custom Systems Multi-Use Terminal Translator provides a convenient means for remote console control of your customer's computer from an off-site location. MUTT allows for instant response capability to customer questions or operator problems.

- Simple installation requires no modification of existing equipment.
- Logic automatically compensates for differing data rates.
- Allows exercising of diagnostics and program debugging from your own office.
- Eliminates unnecessary and costly service calls.

Centralized servicing improves customer relations and reduces labor costs. Ask for information on the economical and easily-installed MUTT from Custom Systems.



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2415 Annapolis Lane
Minneapolis, Minnesota 55441
Telephone: (612) 553-1112 Telex: 290975

*Trademark Terminal Translator

MDB makes modules that let you program PROMs on the board.

Imagine what else we can do!



Nobody else can do it! MDB LSI*-11 and PDP*-11 compatible plug-in boards (MRV-004 and MR-004) let you develop firmware internally — up to eight EPROMs — without the need for a costly, time consuming external programmer box. Produce application and bootstrap programs, replace peripheral device loading in small systems or do special bootstrap loading in large systems — these boards will allow programming of 24 pin EPROMs ranging from the 2716 to the 2732. After programming, you can also transfer to the economical MDB MRV-005 and MR-005 ROM modules. These unique boards let you combine RAM, ROM and PROM for maximum systems flexibility.

And MDB's problem solving doesn't stop there — because MDB makes a complete line of PROM boards with every kind of PROM organization from 256 x 4 to 4K x 8. You'll find the one you need for your application.

What else can we do? More than anyone else for DEC, Data General, IBM Series/1, Perkin-Elmer (and sometimes HP) computers. Look at our communications modules — we even have Unibus* compatible interfaces for Q-bus* computers. Our renowned line of controllers will interface your CPU to every major line printer in the world. MDB foundation modules are designed to use only one card slot. And we're doing multiplexors and interprocessor links with features you've never been able to get before.

MDB products are warranted for a full year, delivered in 30 days or less and are available under GSA contract #GS-00C-01960. Write or call and tell us what we can do for you.

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714-998-6900
SYSTEMS INC. TWX: 910-593-1339

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Circle 134 for LSI, 135 for PDP, 136 for DG, 137 for P-E, 138 for IBM.

PRODUCTS

54" DIGITAL DRUM PLOTTER

Model 5400 offers 35-in (89-cm)/s speed, 4-G acceleration, 0.0125-mm resolution, and 240-ft (73-m) roll continuous feed paper for high throughput in CAD/CAM

applications. Two 16-bit microprocessors and special servomotor drive abet system performance. Plotter supports ballpoint, liquid ink, nylon tip, and liquid roller pens, and translucent, vellum, mylar, and clear acetate film media. RS-232 interface provides for local and remote operation with terminal/modem. Selectable data rates range from 110 to 9600 baud asynchronous. **Nicolet Zeta Corp**, 2300 Stanwell Dr, Concord, CA 94520.

Circle 228 on Inquiry Card

SILVER-PLATED CONTACT SWITCHES

Available with optional silver-plated copper contacts in place of solid silver contacts, silver-saver versions of snap action switches are rated at 125 to 250 Vac at 8 A. Miniature versions are rated at 125 to 250 Vac at 6 A. Pushbutton, plunger, or lever actuated models with or without rollers are available with operating forces of 2 to 10 oz (0.56 to 2.8 N). **McGill Manufacturing Co, Inc, Electrical Div**, Valparaiso, IN 46383.

Circle 229 on Inquiry Card



TEAC.
A newcomer?

Well, Yes and No.

YES, we are introducing 5¼" floppy disk drives.

NO, we are not new in the digital recording field; in fact we are a leader in digital cassette recorders with over 200,000 units already sold.

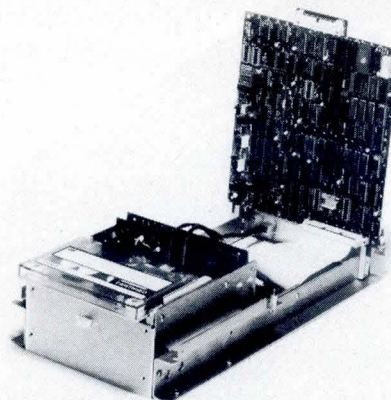
And with a solid 25 years of expertise in magnetic recording technologies - digital, analog, video, and of course our popular stereo tape decks - we *know* how to design and build recorders (to put it modestly).

Now you can have a reliable Floppy Disk Drive or Digital Cassette Recorder - when it bears the name TEAC.

TEAC

TEAC Corporation of America
Industrial Products Division
7733 Telegraph Road Montebello, California 90640 (213) 726-0303

CARTRIDGE SYSTEM BACKUP FOR 8" WINCHESTER DISCS



Model 6450 with embedded formatter measures 8.5 x 4.5 x 16.5" (21.6 x 11.4 x 42 cm) allowing disc and transport to be placed side by side in 19" (48.3-cm) rack. Serpentine serial recording with 6400-bit/in (2520/cm) density gives unformatted capacity of 17.3M bytes with 450-ft (137-m) cartridge, and 11.5M bytes with 300-ft (91.4-m) cartridge. Transfer rate is 192k bits/s, R/W speed 30 in (76.2 cm)/s, and fast-motion speed 90 in (228.6 cm)/s. Power consumption is 21 W at idle, 27 W during R/W, and 31 W during rewind/track select. Unit weighs 10 lb (4.5 kg). **Kennedy Co**, 1600 S Shamrock Ave, Monrovia, CA 91016.

Circle 230 on Inquiry Card

PORTABLE ERROR RATE ANALYZER

RS-232 printer interface is std and HP 5150A interface is optional for the Fireberd 1501 portable error rate analyzer. Error/monitor functions include a range of 10^{-1} to 10^{-10} BER, total errors, EFS, total time, total block errors, total blocks in error, and signal lead status for DSR, CTS, and RLSD. Plug-in interface modules include MIL-188C, RS-449/422, RS-449/423, DS1, WECCO 303, and lab interface (50, 75, and 100 Ω). **Telecommunications Techniques Corp**, 112 Frederick Ave, Rockville, MD 20850.

Circle 231 on Inquiry Card

DISCOVER

The FPS-100 Solution



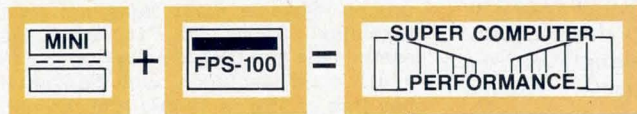
EIGHT MILLION FLOATING-POINT OPERATIONS PER SECOND

THE SYSTEM BUILDERS' CHALLENGE

Your customers demand quicker results, more throughput, higher precision, better resolution, or higher quality output. Your challenge: How to offer a significant increase in performance or capabilities without pricing yourself out of the market.

THE FPS SOLUTION

If your product uses a general purpose minicomputer for numerically intensive computations, you should investigate the FPS-100. When connected to a mini, the FPS-100 makes a low-cost system with supercomputer capabilities.



Performance improvements of more than 200 times are possible, depending upon your application.

EASY TO INCORPORATE

An extremely high performance real-time arithmetic processor designed to crunch reams of data and handle complex computational tasks with relative ease ... and at minimal cost*. The FPS-100 is completely programmable and it's adaptable to a variety of host computers, using either integer

or floating-point formats. It executes up to 8-million floating-point operations per second with 8-decimal digits of precision ... satisfying most applications.

EASY TO USE

We make the FPS-100 easy to use with two FPS-100 Resident Real-Time Operating Systems, and comprehensive development software such as a special FORTRAN Cross Compiler, Assembler, Simulator, Debugger, General Math Library of 250 routines, an Image Processing Library and a Signal Processing Library. With these effective tools, your investment in development time is minimized.

THE TREND IS CLEAR

Discover the FPS-100 solution, as have those OEMs and System builders who are leaping ahead of their competitors in applications such as CAD/CAM, Image Analysis, Real-Time Signal Processing, Seismic Analysis, and Non-destructive Testing.

Contact your nearest FPS Sales Engineer for more information or call, toll free, Jim Strelchun, FPS-100 Product Manager.

*as low as \$17,899 in OEM quantities.



FLOATING POINT
SYSTEMS, INC.

...the world leader in array processors.

FPS Sales and Service Worldwide: Boston, Calgary, Chicago, Dallas, Denver, Detroit, Houston, Huntsville, Los Angeles, New York, Orlando, Ottawa, Philadelphia, Phoenix, Portland, San Francisco, Toronto, Washington, D.C. International offices: Geneva, London, Munich, Paris, Tel Aviv (Eastronix, Ltd.), Tokyo (Hakuto Co. Ltd.)

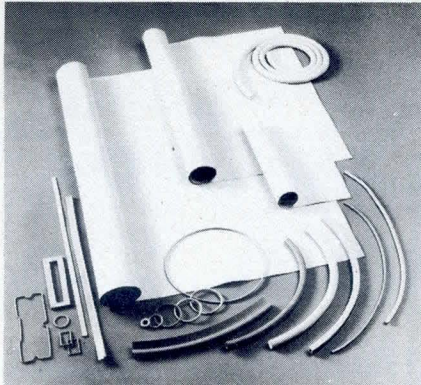
CALL TOLL FREE (800) 547-1445
Ex. 4999, P.O. Box 23489 (S 500),
Portland, OR 97223 (503) 641-3151,
TLX: 360470 FLOATPOINT PTL

Circle 140 for More Information.

Circle 170 for Contact by FPS.

PRODUCTS

CONDUCTIVE ELASTOMER EMI/RFI SHIELD



Consisting of microscopic silver-plated copper particles suspended in silicone and available in strip or molded form, Xecon[®] SPC, a conductive elastomer, provides an environmentally tight, wide-band emi/rfi shield for panels, access ports, doors, waveguides, and cable connectors. Shielding is better than 110 dB at 18 MHz, 72 dB at 10 GHz. **Metex Corp, Electronic Products Div**, 970 New Durham Rd, Edison, NJ 08817.

Circle 232 on Inquiry Card

750-W SWITCHING POWER SUPPLY

Intended for use with telecommunications systems and other applications requiring battery backup, this 48-Vdc input, 750-W output switching regulated power supply features inrush current limiting and emi filtering. Unit, packaged in 5 x 8 x 11" (12.7 x 20.3 x 27.9-cm) slot configuration, incorporates long life fan for cooling. Clock sync input option achieves low system noise levels. Other options include battery low and power good indicators, and constant current output for battery charging. **Qualidyne Systems, Inc**, 2256 Main St, Chula Vista, CA 92011.

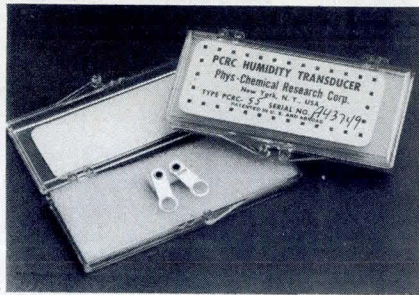
Circle 233 on Inquiry Card

REPLACEMENT FOR GOLD EUTECTIC BONDING

Uniset C-927-42-1 high temp conductive adhesive is a 1-component, heat cured, silver filled compound featuring very high electrical and thermal conductivity. Capable of withstanding long exposures at up to 370 °C, the adhesive is specifically designed for die (chip bonding) applications and can be applied by syringe, transfer stamping, or screen printing. **Amicon Corp**, 25 Hartwell Ave, Lexington, MA 02173.

Circle 234 on Inquiry Card

RELATIVE HUMIDITY TRANSDUCER



Incorporating an electrically conductive surface layer integral with a nonconductive dielectric substrate, the PCRC-55 RH transducer measures 0.25 x 0.5 x 0.0625" (0.635 x 1.27 x 0.159 cm). The sensor utilizes an electric hygrometric circuit element whose impedance varies with RH changes. Operating range of the device is 0 to 100% RH within a temperature range of -60 to 200 °F (-51 to 93 °C). **Phys-Chemical Research Corp**, 36 W 20th St, New York, NY 10011.

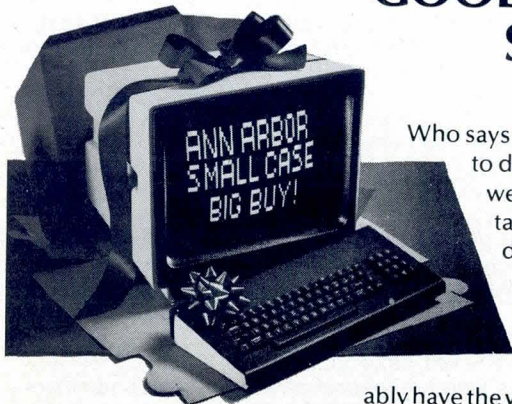
Circle 235 on Inquiry Card

OPTICAL FIBER TRANSMISSION EMITTER AND DETECTOR

Capable of full-duplex transmission over a single optical fiber, the CED-1 combined emitter/detector can utilize an 820-nm LED, sensitive silicon detector, and step index fiber to transmit data at up to 10M bits/s over distances in excess of 1 km. Available in Europe, the device includes an installed optic connector and optical pigtail. **Fibronics, Ltd**, Science Based Industries Center, Technion City, Haifa 32 000, Israel.

Circle 236 on Inquiry Card

GOOD CRT'S COME IN SMALL PACKAGES



Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen and detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep.

We're known throughout the industry for our high quality and reliability. On top of this, we probably

have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign

language character sets. Special command sets. Custom keyboards. Editing, protected fields and block transmit.

And if your application doesn't lend itself to a desktop terminal, we offer display controllers (especially good in industrial environments) for use with free-standing monitors. Or buy our terminal without the case and mount it in your own console.

So when the CRT is the focal point of your system, why settle for a large case and small screen? You can have excellent readability without taking up a lot of room. And get the features you need. Call us for more information at Ann Arbor Terminals, Inc., 6175 Jackson Road, Ann Arbor, Michigan 48103. Tel: (313)663-8000. TWX: 810-223-6033.

ANN ARBOR
TERMINALS, INC.

CRT COLOR MONITORS

Thousand-line GM 865C color monitor uses newly developed color shadow mask 25" (63.5-cm) CRT with 0.367-mm vertical pitch. It provides large screen direct view presentation for small groups. Shadow mask does not limit resolution. Series GM 714, using the same inline gun CRT, displays up to 640 x 512 pixel resolution, with horizontal line freq of 15.5 to 19 kHz (516 through 633 total lines at 2:1 interlace, 30/60 Hz). Units are available in cabinet or rack-mount and with std or long persistence phosphors. **Ramtek Corp**, 2211 Lawson Ln, Santa Clara, CA 95050.



Circle 237 on Inquiry Card

Quality at Your Fingertips.

Datanetics builds keyboards as reliable as the systems and products they go into.

And that isn't so easy, considering what they have to go through.

Keyboards are exposed to everything from settling dust to cracker crumbs. And they're

subjected to individual keystroke styles ranging from "feather touch" to "jackhammer"

But in spite of everything, Datanetics keyboards keep right on working. We even make one kind that's been tested to over 100 million trouble-free cycles.

Put quality at your customers' fingertips. Call us today.



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Phone: (714) 549-1191
TWX: 910-596-1301



CIRCLE 142 ON INQUIRY CARD

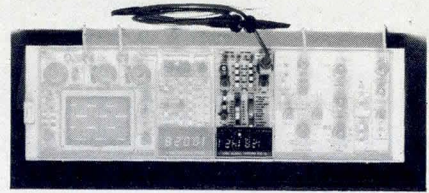
PRODUCTS

INTERFACE OPTION FOR FFT SPECTRUM ANALYZER

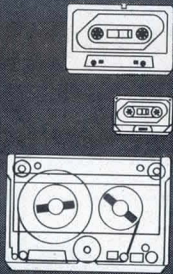
Plug-in circuit card "-3" option enables SD345 FFT signal analyzer to communicate directly with commercial

calculators, computers, and digital plotters. Both IEEE 488-1978 and RS-232-C are available and addressable via customized software in P/ROM sets on the card. Option allows spectrum analysis complete with full engineering annotation and grids to be directly recorded on digital plotters. New data may be averaged by the analyzer without affecting the plot. **Spectral Dynamics**, PO Box 671, San Diego, CA 92112. Circle 238 on Inquiry Card.

UNIVERSAL COUNTER/TIMER PLUG-IN MODULE



Designed to operate in a TM 500 power module, DC 503A provides 11 measurement functions: frequency, period, period avg, width, width avg, time A→B, time A→B avg, ratio A/B avg, events A during B avg, totalize, and time manual. Measurements can be averaged from 1 to 10⁸ times. Single-shot resolution is 100 ns. 2 input channels each provide 0-to 125-MHz frequency range and 20-mV rms sensitivity. Module can be equipped with optional oven-controlled 10-MHz ± 0.2-ppm crystal oscillator time base. **Tektronix, Inc.**, PO Box 1700, Beaverton, OR 97075. Circle 239 on Inquiry Card



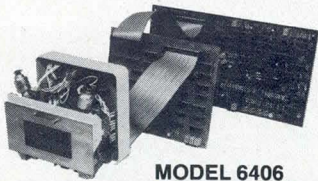
**CASSETTE...
MINI-CASSETTE...
CARTRIDGE...**

**NO MATTER WHAT YOUR
SMALL TAPE-DRIVE REQUIREMENT,**

**THERE'S A RAYCORDER
YOU CAN DEPEND ON.**

The Raycorder Products Division of Raymond Engineering Inc. has been building cassette/cartridge tape drives for 10 years. We're the small tape drive experts. Whatever your choice of media — cassette, mini-cassette, or cartridge — Raymond builds a tape drive for all of the standards.

Whether you require an OEM drive with typical tape recorder interface, a standard interface such as RS232C or IEEE 488, a custom interface, or a stand-alone system, Raymond builds the configurations that you want. Our software driven interfaces provide the flexibility to make this possible. Let us show you how.



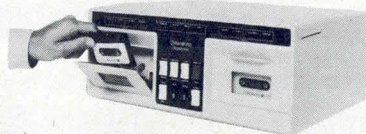
**MODEL 6406
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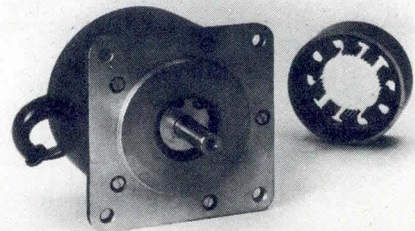
Raycorder Products Division
Raymond Engineering Inc.

217 Smith Street, Middletown, Connecticut 06457·(203) 632-1000

HIGH OUTPUT INFRARED EMITTERS

Featuring GaAlAs heterostructure p-n diode construction, Super IR emitters produce noncoherent energy at 880-nm wavelengths and switch in 1 μs. Power conversion efficiencies for packaged devices can reach 20%. The devices are available in TO-46 hermetic, T-1 3/4 plastic, and T-1 plastic packages and may be graded by total power output or peak axial radiant intensity. **Xcitor Corp.**, 5 Hemlock St, Shaker Pk, Latham, NY 12110. Circle 240 on Inquiry Card

5φ PM STEPPING MOTOR



Capable of full steps (0.72°) and half steps (0.36°) (0.126 and 0.0063 rad) with ± 3-min (8.7 x 10⁻⁴-rad) accuracy, the 5φ RDM 596/50 stepping motor can be micro-stepped electronically without closely controlled individual phase current loops. Specifications include a stepping rate of 30 kHz, start/stop speed of up to 2500 full steps/s, and slow speed of up to 100k steps/s at 6000 r/min. Rated torque is 115 N·cm and rotor inertia is 0.7 kg/cm². **Berger-Lahr Corp.**, Fitzgerald Dr, Jaffrey, NH 03452. Circle 241 on Inquiry Card

A lot of smarts.

The Hazeltine Executive 80™ isn't just a smart new terminal. It's a complete family of smart terminals, easily customized to fit the precise needs of your application.

There are two basic models. Executive 80, Model 20, is optimized for top price/performance in conversational or buffered environments. Model 30 is a fully featured high performance editing terminal. Both models have a long list of smart features, like programmable function keys, separate numeric key pad, scrolling, split screen display, blinking and reverse video fields, even a forms-drawing capability. Starting with either model, you can add all the other features and choose all the options you need to match the terminal precisely to the system you've designed.

Detachable keyboards and tilt display, for example, are options with Model 20 and standard with Model 30. These features allow the operator to position the screen at the most comfortable viewing angle. There's also a video enhancement option that gives you a

15-inch smooth scrolling monitor which selectively displays either 80 or 132 column formats in normal size or double height and width.

No matter how you configure Executive 80 terminals, you can be sure of high reliability. In addition to Hazeltine's high quality, Executive 80 has a very smart diagnostic capability that enables it to trouble-shoot its own failures.

It takes a smart terminal to handle all the new applications of the eighties. That's why Executive 80 has lots of smarts.

Hazeltine Corporation, Computer Terminal Equipment, Greenlawn, NY 11740 (516) 549-8800 Telex: 96-1435

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**Hazeltine
Executive** 
Answers for the Eighties



CIRCLE144 ON INQUIRY CARD

**clock oscillator
for Zilog
Z8000 or Z80A
or Mostek
MK3880-4
microprocessors**



see us at WESCON
Booth 1555

**Model K1160A
4 MHz
crystal clock
oscillator**

This thick film hybrid oscillator with active pull-up provides the precise 4 MHz waveform required to drive the Z8000, Z80A or MK3880-4.

The single DIP saves board space needed by up to 17 discrete components it replaces, and eliminates production man-hours wasted analyzing oscillator circuits and matching crystals to circuit components.

Plug the K1160A into your 4 MHz microprocessor circuit design and forget your crystal oscillator problems.

Mostek and MK3880 are trademarks of Mostek Corporation. Zilog, Z80 and Z8000 are trademarks of Zilog, Inc.  and Motorola are trademarks of Motorola Inc.



MOTOROLA INC.

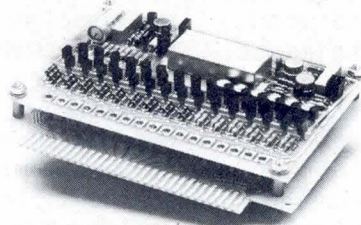
COMPONENT PRODUCTS

2553 N. Edgington
Franklin Park, Ill. 60131
312/451-1000
TWX: 910-227-0799
Telex: 025-4400

PRODUCTS

HIGH SPEED ADC

Successive approximation ADC 1555S provides complete conversion of an analog voltage to a 15-bit digital number in less than 5 μ s. Device consists of 2 piggyback epoxy-filled glass-etched circuit cards that plug together to form single plug-in module. Open circuit construction allows complete repairability. Except for power supplies, unit contains all functions necessary to perform conversion. Device can be used alone or with other analog modules to form a complete system. **Tustin Electronics Co**, 1431 E St Andrews Pl, Santa Ana, CA 92705.



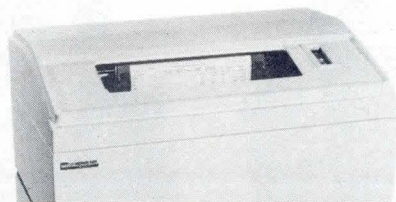
Circle 242 on Inquiry Card

**8-BIT HYBRID ADC
WITH 1- μ s CONVERSION**

Featuring 6 pin-programmable input voltage ranges (0 to 5, 10, and 20, and ± 2.5 , 5, and 10 V), the ADC-825 has a logic input that switches the device from unipolar to bipolar operation. Specifications include 20-ppm/ $^{\circ}$ C max gain temp-co $\pm 1/2$ LSB max integral and differential linearity error, and basic operating range of 0 to 70 $^{\circ}$ C. Packaging is hermetic 24-pin DIP. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.

Circle 243 on Inquiry Card

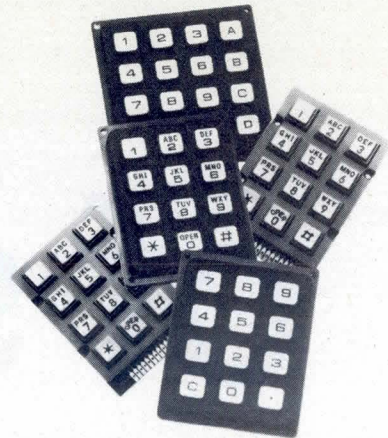
650- TO 1000-LINE/MIN PRINTERS



Three printers provide speeds of 650, 800, and 1000 lines/min, are IBM compatible, and include full field upgrade and interchange capabilities. Each unit has electronic partitioning to accommodate a variety of computer interfaces and controllers. Models 6665 (650 lines/min) and 6680 (800 lines/min) may be field upgraded to a 6610 (1000 lines/min). **Decision Data Computer Corp**, 100 Witmer Rd, Horsham, PA 19044.

Circle 244 on Inquiry Card

LOW COST KEYBOARDS



THRIFTSWITCH keyboard line features positive tactile feedback, 2-color molded key legends, and electrostatic shield. Op temp range is -20 to 60 $^{\circ}$ C. Contacts and circuits on UL-approved PCB are gold plated. One of the 2 std configurations has white keys on black background in both 3 x 4 and 4 x 4 layouts. Other has grey background with black letters on white in 3 x 4 telephone format. Circuitry choices include matrix code, single-pole/common bus, and 2-of-7 code (2-of-8 for 4 x 4). Circuit termination allows wirewrap, solder, or connector plug connections. **Industrial Electronic Engineers, Inc**, 7740 Lemona Ave, Van Nuys, CA 91405.

Circle 245 on Inquiry Card

**PLASTIC CLAD
SILICA OPTICAL FIBERS**

Step index optical fibers have a short gauge length tensile strength of over 3.45×10^9 N/m², and attenuation of 10 dB/km at 790 nm. Designed for medium distance and medium bandwidth data transmission and high power optical applications, the fibers consist of a silica core, plastic optical cladding, and protective jacket. Core diameters available are 125, 200, 400, and 600 μ m. **EOTec Corp**, 200 Frontage Rd, West Haven, CT 06516.

Circle 246 on Inquiry Card

FILM CAPACITOR LINE

Line of film capacitors comes in both axial and radial lead styles and in std and tight tolerances. Range of film materials includes polystyrene (100 pF to 1 μ F, 63 to 400 Vdc, to 85 $^{\circ}$ C); metallized polycarbonate (1000 pF to 22 μ F, 40 to 400 Vdc, to 125 $^{\circ}$ C); polyester (1000 pF to 39 μ F, 63 to 630 Vdc, to 125 $^{\circ}$ C); and polypropylene units of high stability with frequency that includes both metallized and non-metallized film and foil types in voltages from 160 to 2000 Vdc. **Thomson-CSF**, 6660 Variel Ave, Canoga Park, CA 91303.

Circle 247 on Inquiry Card

Color it Dunn.

Communicate with Color Hard Copy from the 630 Series



Exciting computer images, digitally processed or original graphics, should not be confined to your color terminal. Their communication value is wasted. That's why Dunn

Instruments invented versatile, affordable photographic hard copy. Made by the 630 Color Camera Series.

Since early 1979, 630 Series cameras have been at work in applications ranging from

remote sensing to animation, from business presentation graphics to NASA's Saturn mission.

Media versatility
Instant 8x10 prints on Polaroid® Type 808 film, overhead transparencies, 35mm slides, animated 16mm film — all these and more are within the capabilities of a single camera system. Their incredible resolution, chromatic vividness and accuracy will astonish you. So, too, will the speed, ease and assurance with which you

produce them, thanks to microprocessor-automated camera operation and exposure control.

Multi-imaging power

Recording images side by side aids in comparative analysis and presentation planning. It also reduces film cost. Our software-based format selection means the freedom



to tailor the configuration of images to your needs. It's a Dunn Instruments exclusive.

THE 630 COLOR CAMERA SERIES

Interfacing ease

The 630 Series interface with ease to every kind of computer system and color terminal. They are sold complete, and installed worldwide by an experienced sales and service force.

Call 415/957-1600 and we'll put you in touch with your nearest Dunn Instruments representative. Or write us at 544 Second Street, P.O. Box 77172, San Francisco, CA 94107.



DUNN INSTRUMENTS

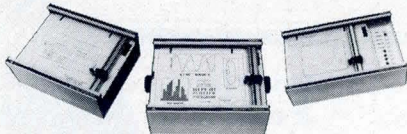
"Polaroid" is a registered trademark of Polaroid Corporation

Outside the U.S., the 630 Series is distributed by CalComp International.

LANDSAT image courtesy NASA-Ames Research. Cartographic studies courtesy Harvard Laboratory for Computer Graphics.

PRODUCTS

HIGH PERFORMANCE DIGITAL PLOTTERS



Five models have been added to the HI PLOT family. DMP-2 8.5 x 11" (21.6 x 28-cm) and DMP-5 11 x 17" (28 x 43.2-cm) basic units have built-in RS-232-C and parallel interface. Pen speed is 2.4" (6.1 cm)/s; plotting is at either 100 or 200 increments/in (39.3 or 78.7/cm). DMP-3 (8.5 x 11") and DMP-6 (11 x 17") intelligent plotters have pen speeds to 3" (7.6 cm)/s for the DMP-3 and 2.4"/s for DMP-6. DM/PL™ instructions minimize software burden on host. DMP-4 (8.5 x 11") and DMP-7 (11 x 17") include electronic controls for X, Y axis positioning and self-diagnostics. **Houston Instrument, Div Bausch & Lomb**, One Houston Sq, Austin, TX 78753.

Circle 248 on Inquiry Card

SMALL TOGGLE AND PUSHBUTTON SWITCHES

Both solder and PCB mounting terminations are available on the Tiny Toggle and Tiny Pushbutton lines of switches. Specs for the toggle switches include 120 Vac or 28 Vdc at up to 3 A resistive with contact resistance of 10 mΩ. The pushbutton switches are rated at 120 Vac or 28 Vdc at 1 A resistive with contact resistance of 20 mΩ. Both switch lines have a dielectric strength of 1 kV rms at sea level. **C & K Components, Inc.**, 15 Riverdale Ave, Newton, MA 02158.

Circle 249 on Inquiry Card

BURN-IN/TEST IC SOCKET

Designed for IC devices with 0.300" (0.762-cm) pin row centers, the 613 Mid-Rise™ is a burn-in/test socket series available in 14-, 16-, and 18-lead configurations. Beryllium copper face-wiping contacts are selectively gold plated over nickel, and the Ryton-molded socket withstands burn-in applications of up to 200 °C. Contacts are visible for probing during burn-in/test. **Wells Electronics, Inc.**, 1701 S Main St, South Bend, IN 46613.

Circle 250 on Inquiry Card

SINGLE BOARD 16-CHANNEL MUX

Microprocessor based DZ/16 MUX controls 16 asynchronous communication lines by emulating functions of 2 full hex-width DEC DZ11 8-line boards. It occupies half the space and presents only 1 load to the Unibus. Compatible with DEC diagnostic software, it has onboard self-test with LED display and switches for address and vector selection. Data format is program selectable for each channel. All DZ11 baud rates are supported. MUX installs in any available hex-width SPC slot of a std DZ11 backplane. **Able Computer**, 1751 Langley Ave, Irvine, CA 92714.

Circle 251 on Inquiry Card

ELECTROSENSITIVE GRAPHICS PRINTER



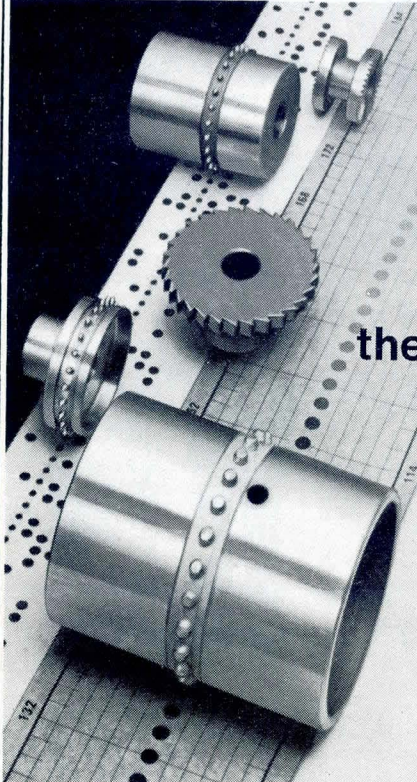
GP-100 Graphx-Printer plugs directly into the company's RG-512 Retro-Graphics card, a Tektronix software-compatible field upgrade for the Lear Siegler ADM-3A dumb terminal. The device prints the graphics within a 6.7 x 5" (17 x 12.7-cm) area on 8.5" (21.6-cm) roll-fed aluminum coated paper in less than 20 s. Alphanumeric can also be printed at 170 lines/min. The silver toned paper is archival and will not fade with age. **Digital Engineering, Inc.**, 1775-C Tribute Rd, Sacramento, CA 95815.

Circle 252 on Inquiry Card

IMAGE DISPLAY SYSTEMS

Video display system ID 1100 is compatible with DEC PDP-11 Unibus and offers full true color, or up to 4 multi-image monochrome or pseudo color displays with 1k x 1k x 8-, 16-, 24-, or 32-bit resolution. There are 4 1024 x 1024 x 8 overlay memories on each image channel, with independent zoom of 2:1, 4:1, and 8:1 on up to 4 channels, plus independent scroll on each channel. Optional interactive devices include cursor-controlling joystick, trackball, and lightpen. **DeAnza Systems, Inc.**, 118 Charcot Ave, San Jose, CA 95131.

Circle 253 on Inquiry Card




designing tape mechanisms?

LaVeZZi is
the source for
the HIGH PRECISION
machined parts

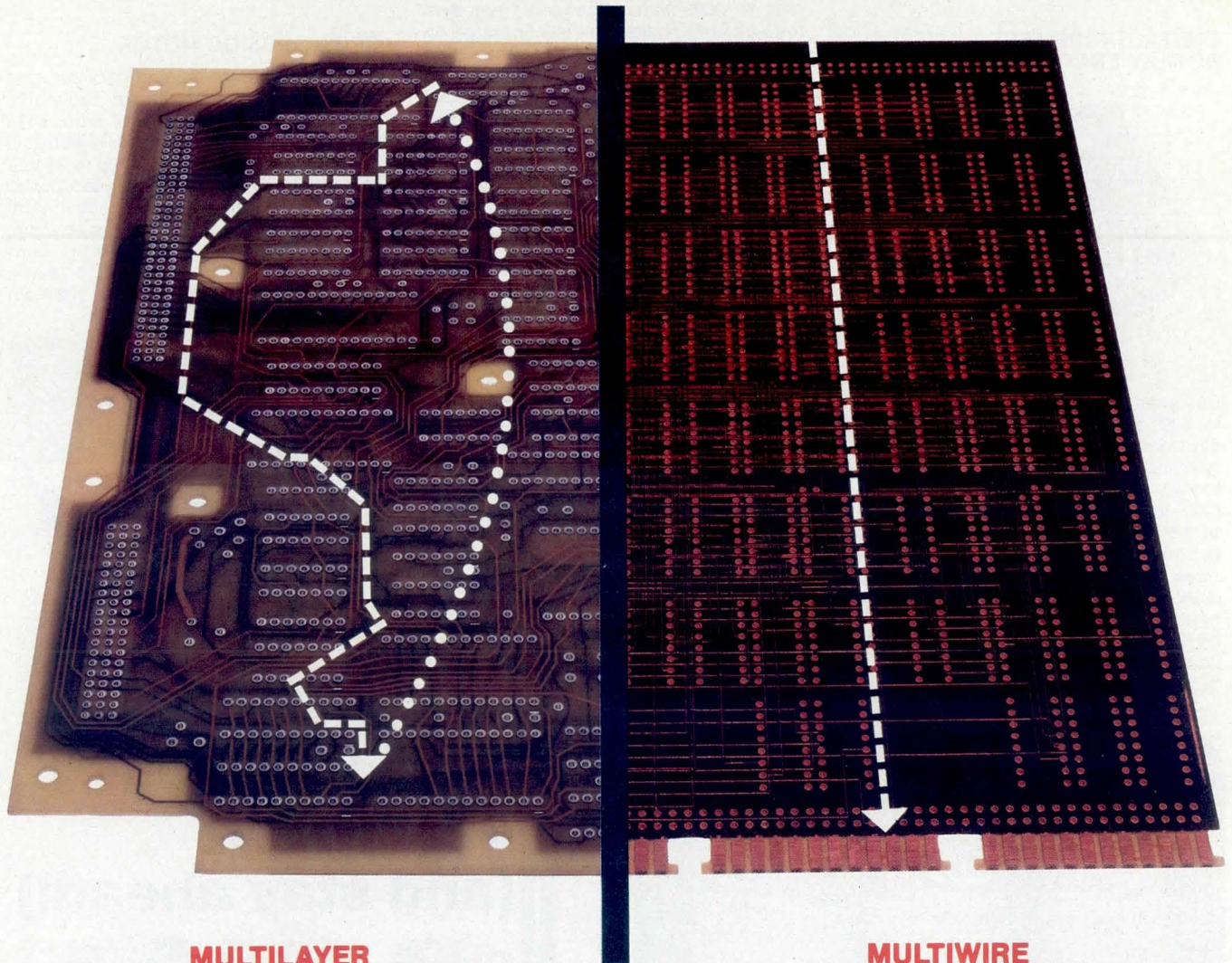
We specialize in the manufacture of small machined parts involving unique machining requirements, extremely close tolerances, fine finishes. A variety of sprockets and other high precision parts are in stock for immediate delivery—or made exactly to your specifications. Inquiries invited. Described in detail in catalog L70-5

sprockets
ratchets
starwheels
etc.



LaVeZZi Machine Works, Inc.
900 North Larch Avenue
Elmhurst, Illinois 60126
(312) 832-8990

The Shortest Line Between Design Points is Multiwire.



MULTILAYER

Regardless of what design technique you use — even with a computer aided system — designing multilayer PC boards can be a guessing game. Many times, in the last 5% of the routing, you find yourself up a "blind alley" and you have to go back to "start".

MULTIWIRE

With Multiwire, you can easily avoid such blind alleys . . . for design-time savings in your circuit boards. Routing is under complete computer control. All you have to do is prepare artwork for the power and ground planes, the net or "from-to" list, and a fabrication print showing component location and board configuration. The Multiwire design program takes over from there. Results: your design time is cut. And, when design changes are needed, Multiwire lets you make them . . . quickly, easily. Electrical characteristics are consistent and controllable, inspection costs are cut and production yields go up.



A typical example of the circuit density achievable with Multiwire circuit boards.

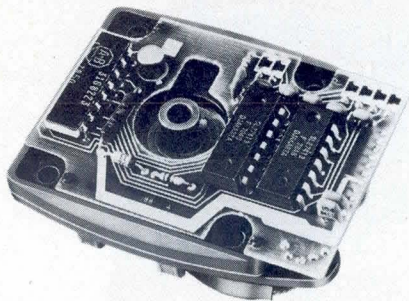
Why wait? For complete details write or call today. Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307.

 **MULTIWIRE**
DIVISION
KOLLMORGEN CORPORATION

CIRCLE 147 ON INQUIRY CARD

PRODUCTS

DIGITAL INCREMENTAL ROTARY ENCODER



Designed for applications requiring up to 400 counts/rev, STRE 2014 provides symmetry, broad dynamic range, tolerance to power supply variations (3.5 to 8 V), and low jitter. Device has a single LED light source with temp compensated feedback loop for the LED drive current. A single monolithic array provides the encoder with a push-pull readout system. Phase shift is $90^\circ \pm 10\%$. **Sensor Technology, sub of Dyneer Corp**, 21012 Lassen St, Chatsworth, CA 91311.

Circle 254 on Inquiry Card.

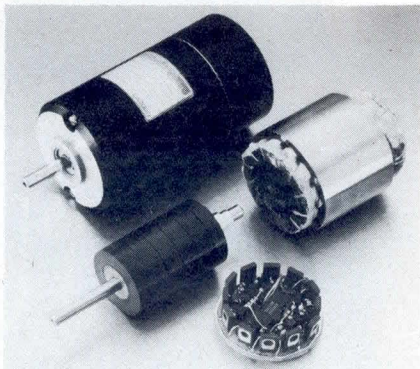
BYTE ORIENTED DMA CONTROLLER FOR UNIBUS

Controller module PDI-11 for Unibus computers performs DMA transfers at 80k to 200k bytes/s to and from byte oriented peripherals usually operated on a serial basis. The quad-board mounted controller allows a peripheral device to appear to the computer as a DEC DL serial line unit. The module functions in parallel using RS-422 receivers and drivers at distances to 3000 ft (914 m) at full speed. **MDB Systems, Inc**, 1995 N Batavia St, Orange, CA 92665.

Circle 255 on Inquiry Card

BRUSHLESS DC MOTOR

Utilizing a shaft encoder/decoder that commands drive circuits for sequential stator coil activation, the type 3414 brushless dc motor achieves electronic commutation. It operates at up to 24 Vdc and requires only a single-ended power supply. Features include low emi characteristics, bidirectional operation, constant speed and current limit capabilities, and high torque to inertia ratio. **Electric Indicator Co, Inc**, 272 Main Ave, Norwalk, CT 06851.

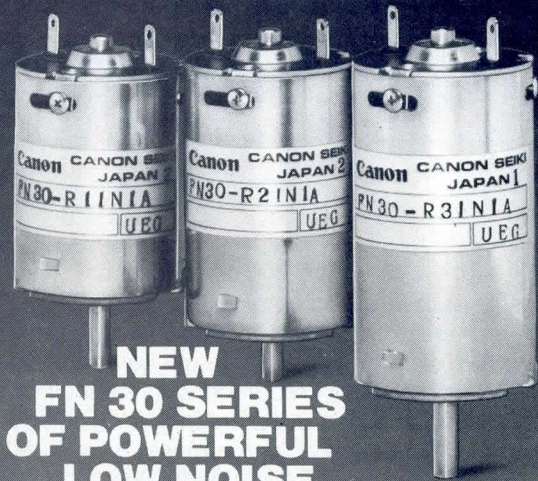


Circle 257 on Inquiry Card

SWITCH MODE REGULATED DC-DC CONVERTER

A 2:1 input range is featured in the switch mode regulated UM and UMC series dc-dc converters. Input ranges of 9 to 18, 18 to 36, and 35 to 70 Vdc can withstand 8-ms surges of 25, 40, and 100 V, respectively. Single outputs of 5, 12, and 15 Vdc at 800 mA to 3 A are available. Overcurrent and overvoltage circuitry is included, along with 1500-Vdc I/O isolation. **Semiconductor Circuits, Inc**, 218 River St, Haverhill, MA 01830.

Circle 256 on Inquiry Card



NEW FN 30 SERIES OF POWERFUL LOW NOISE 30 mm DC MOTORS

Available in nine different combinations of motor length (41, 48 and 55 mm) and voltage (6, 12, 24 V) this new series features extremely low electrical noise, very high efficiency, long service life, smooth operation and low mechanical noise.

- Starting torques from 280 to 500 g-cm
- Maximum efficiency as high as 65% at 24 Volts.
- Varistor ring and high quality brush material.
- 7 bar armature for smooth operation.
- Available with AC tach, gearheads and AMP 110 terminals

For complete technical information:

Canon

Canon U.S.A., Inc.
Electronic Components Division
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Lake Success, L.I., N.Y. 11042
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Precision Mount,
(Azimuth $\pm 6'$)

WP-1D2

4-track/2-channel
Extended
low-frequency
response head
for .250" tape

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2-track/2-channel
cassette head,
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Exceptionally versatile.

Three typical Vikron magnetic heads that come equipped with total service. That simply means we're not done helping you until you're done needing help.

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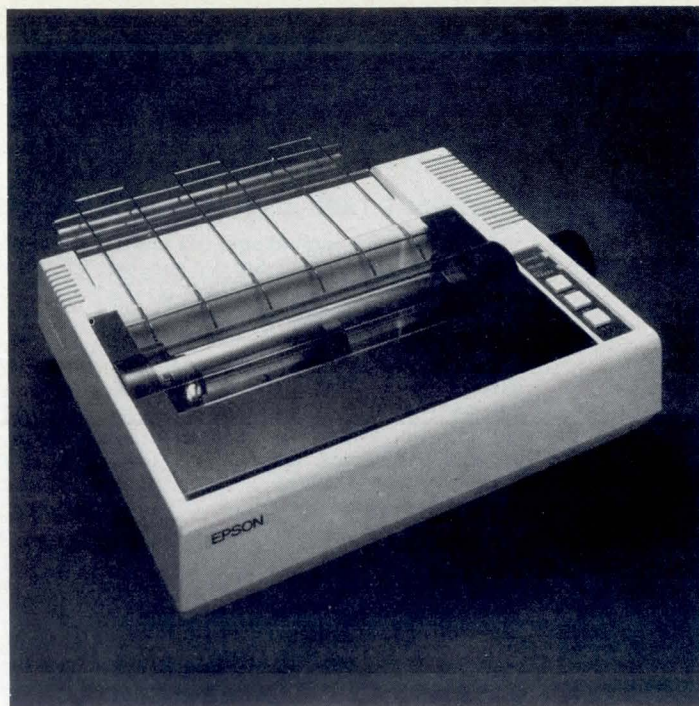


VIKRON

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The
MX-80.
It not
only does
everything,
it does
everything
well.



Epson.

This is the new Epson MX-80 dot matrix printer. It does just about everything you could ask a printer to do. Quickly. Quietly. Reliably. In fact, for OEM installations, the MX-80 may be the single best, all-round printer you can buy. But that's not the best reason to buy it.

The MX-80 prints bidirectionally at 80 CPS in a user-defined choice of 40, 80, 66 or 132 columns. And if that's not fast enough, its logical seeking function minimizes print head travel time. The MX-80 prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. For a long time. Epson printers are known for reliability and the MX-80 is no exception. But that's not the best reason to buy it either.

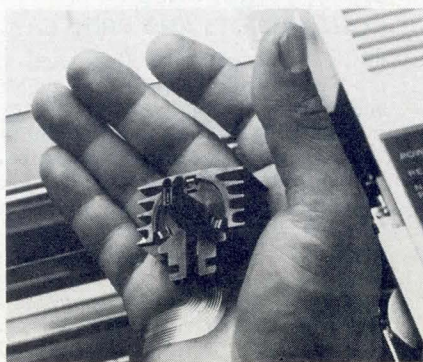
The print head has a life expectancy of up to 100×10^6

characters, and when it wears out, just throw it away. A new one costs less than \$30 and the only tool you need to change it is attached to the end of your arm. The MX-80 is compact, weighs only 12 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor. But even that isn't why you should specify the MX-80.

The best reason is this: because Epson makes more printers than anyone else in the world, we can afford to sell each one for a little less. So you can get one Epson MX-80 Printer for less than \$650. And more than one for even less than that.

That's what we call a small price to pay for a printer that does everything well.

The world's first disposable print head. When it wears out, just throw it away. A new one costs less than \$30, yet it's so simple, you can change it with one hand.



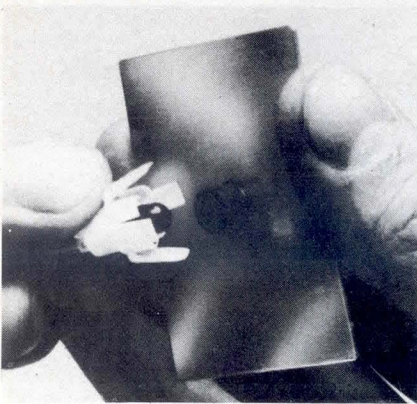
EPSON
EPSON AMERICA, INC.

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CIRCLE 150 ON INQUIRY CARD

PRODUCTS

REAR MOUNT PANEL LED INDICATOR ASSEMBLY



Consisting of separate lens and LED housing assembly, the panel mount LED indicator assembly snapmounts onto its lens from the rear of the panel. The 5400 series is available in red, green, or yellow and accommodates panel thicknesses of 0.0156 to 0.0938" (0.397 to 2.38 mm). Power requirement is 2 Vdc at 20 mA for a luminous intensity of 34 to 45 mcd, depending on color. The device requires a 0.3125" (0.8-cm) mounting hole. **Industrial Devices, Inc.**, 7 Hudson Ave, Edgewater, NJ 07020.

Circle 258 on Inquiry Card

14-BIT D-S CONVERTER

4.5-VA drive capability, increased efficiency, and 5-V only power requirement are featured in the DSC-544 digital to synchro converter module. Accuracy of the device is ± 4 min ($\pm 1 \times 10^{-3}$ rad) and it meets MIL-STD-202E requirements. A transformer isolated output is protected against overloads and short circuits, and overheating is prevented by a built-in thermal cutoff. Std operating ranges are 0 to 70 and -55 to 85 °C. **ILC Data Device Corp.**, 105 Wilbur Pl, Bohemia, NY 11716.

Circle 259 on Inquiry Card

LED ILLUMINATED PUSHBUTTON SWITCHES

Available with red, yellow, or green LED light source and NO, NC, or 2-circuit configurations, the 913 series of pushbutton switches requires a max of 5 Vdc at 20 mA. Short travel momentary contact construction is used along with the long life and high efficiency provided by the LED illumination source. Designed for panel mounting, the switches provide high visibility. **Dialight**, 203 Harrison Pl, Brooklyn, NY 11237.

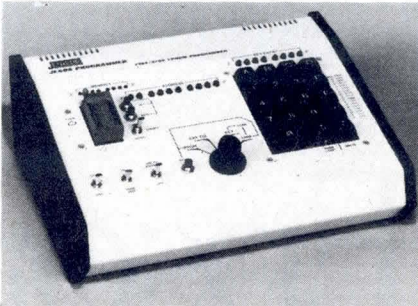
Circle 260 on Inquiry Card

CARTRIDGE TAPE CONTROLLER

Utilizing bit-slice technology, the model 570 cartridge tape controller will support up to 68M bytes of tape storage on the DEC Q-bus. Resident on 1 quad-size board, the emulating controller provides software compatibility with operating systems having TM11/TU10 support. Additional features include data integrity verification and mixed tape drive capability. **Xylogics, Inc.**, 42 Third Ave, Burlington, MA 01803.

Circle 261 on Inquiry Card

EPROM PROGRAMMER



Designed for programming 2704 or 2708 EPROMs, JE608 can also be connected to emulate 2704, 2708, or other compatible ROMs. Programming is achieved via instrument's internal RAMs and onboard hex keyboard or by copying program of previously programmed devices. Unit permits examination, change, and validation of program content. Microprocessor system development is enabled by ribbon cable connection from panel test socket to EPROM socket on microprocessor board. Unit comes as kit, or completely wired and tested. **Jameco Electronics**, 1355 Shoreway Rd, Belmont, CA 94002.

Circle 262 on Inquiry Card

PDP-11 COMPATIBLE CONTROLLERS AND PRINTERS

LPC-11 line of controllers and line printers provides 300 to 1200 lines/min and is plug compatible with PDP-11/04 through VAX-11/780 minicomputers. Controllers are compatible with the Unibus and occupy one quad slot in the system backplane. They are transparent to RSX-11, IAS, RSTS, DSM-11, and RT-11 operating systems; no reprogramming is required. Parallel char data transfer rate is 66.8 kHz. 64-char ASCII char sets are std, with 96-char or foreign language sets optional. **BDS Computer Corp.**, 1120 Crane St, Menlo Park, CA 94025.

Circle 263 on Inquiry Card

S-D CONVERTER MODULE

Measuring 2.6 x 3.1 x 0.82" (6.60 x 7.87 x 2.08 cm) and designed for PCB mounting, SDC410C synchro to digital converter modules provide dc output voltage proportional to velocity, in addition to 10-, 12-, or 14-bit digital outputs. Synchro resolver inputs of 11.8 or 90 Vac, 400 Hz, or 90 Vac, 60 Hz, are converted into binary output angle representations accurate up to ± 4 min of arc ($\pm 1 \times 10^{-3}$ rad). **Computer Conversions Corp.**, 6 Duntun Ct, East Northport, NY 11731.

Circle 264 on Inquiry Card

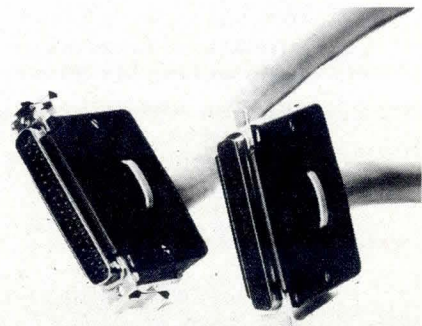
160-CONTACT LOW INSERTION FORCE CONNECTOR

Constructed to provide low contact resistance along with low insertion force, the KA160 PCB connector features 216 keying combinations and easily removable contacts. Contacts may be removed from the front and rear, facilitating motherboard and backplane repairs. The Hypertac^R contact is a hyperboloid-shaped sleeve available in crimp, wirewrap, and straight and right angle dip solder cup configurations. **Hypertronics Corp.**, 2352 Main St, Acton, MA 01742.

Circle 265 on Inquiry Card

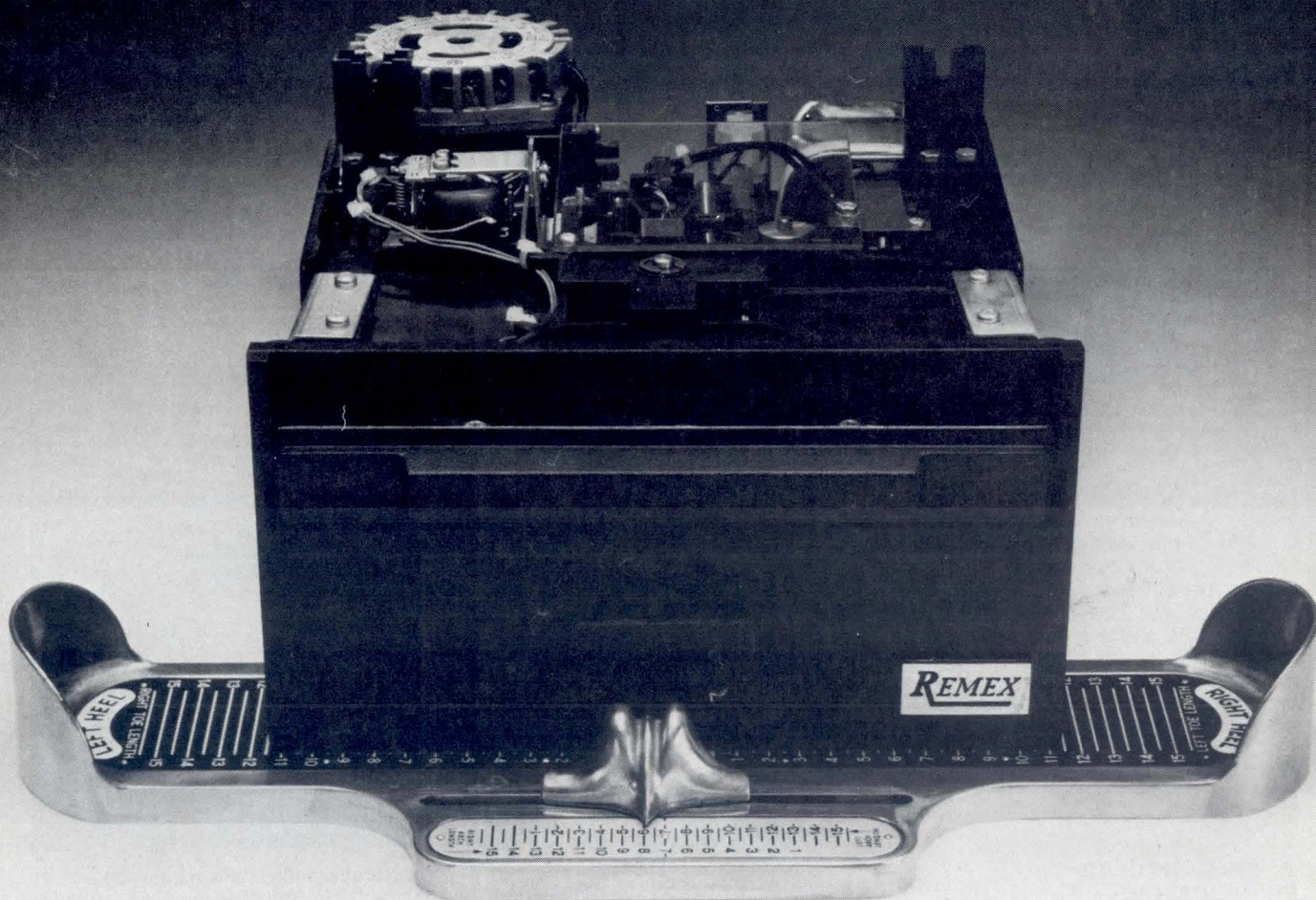
RS-449 DATA CABLES

Cable assemblies meeting full RS-449 specs provide a capacitance of 10 to 13 pF/ft (33 to 43 pF/m) in the 37-conductor configuration. Construction consists of 18 twisted pairs and 1 single AWG 24 stranded tinned copper conductor covered by an overall aluminum foil and mylar shield, with a single AWG 24 drain wire. Both screw locks or RS-449 special mounting clips can be supplied. **Kertech Corp.**, 10 Babson Park Ave, Babson Park, MA 02157.



Circle 266 on Inquiry Card

If the Shugart fits...



If you've taken a shine to Shugart, you're in luck.

Specifying Shugart means you're also specifying Remex. We're your alternate source for fast, volume delivery.

Remex single and dual-headed drives, single or double density, are physically and electrically compatible to Shugart SA850R/851R units. So you can switch over to Remex without re-design.

Our drives are also available packaged two drives to a Remex subsystem, in the head/density combination you specify and with their own dc power supply. The subsystem includes rack-mountable guide rails. Just slide it into your system, plug it in and go. Even your operating manuals

remain unchanged.

What's more, Remex has solved the dual-head media wear problem for good with a new, improved head and carriage assembly.

So remember this: If the Shugart fits, Remex fits, too.

Call today for more details or to get your order rolling. Ex-Cell-O Corporation, Remex Division, 1733 East Alton Street, Irvine, CA 92713. (714) 957-0039 TWX: 910-595-1715

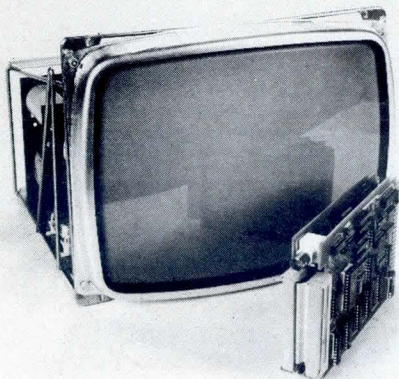
Ex-Cell-O Corporation

REMEX DIVISION

DATA WAREHOUSE

PRODUCTS

CRT MODULES



Video interface and video memory modules provide from 12- to 80-char/line and 6- to 25-line format, full u/lc ASCII char, and up to 64 custom graphic symbols per memory module. Intended to operate with the PC400 programmable controller, the module provides a data rate of 15,750 char/s, and cursor location, size, and blink rate are user programmable. **Giddings & Lewis Electronics**, 142 Doty St, Fond du Lac, WI 54935.

Circle 267 on Inquiry Card

0.5" RECTANGULAR LED INDICATORS

Series CM4-65 red LEDs feature a 0.5 x 0.25" (1.27 x 0.64-cm) lighted area with a wide viewing angle because of the combination of 2 LED chip outputs in each unit. Twin LEDs can be lighted independently or simultaneously and typical operation is 2.0 Vdc at 20 mA. A 400-ns switching time allows multiplexing. Max power dissipation is 200 mW and operating range is -40 to 85 °C. **General Instrument Corp, Lamp Div**, 4433 Ravenwood Ave, Chicago, IL 60640.

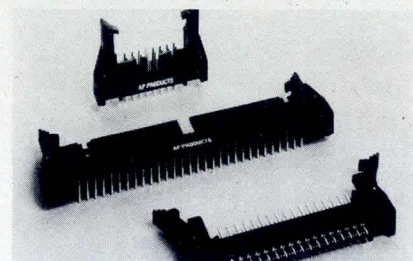
Circle 268 on Inquiry Card

HARD DISC CONTROLLER

SM/S controller for drives with standard storage module (SMD) interface consists of 2 S-100 boards. Adaptation to specific drive is accomplished by changing the I/O driver software. Testing of the controller is simplified by fault isolation software run on the host computer. The unit's custom microprogrammable processor controls data transfers. Custom microcode is stored in writable control memory. The controller uses 256-byte sector format and has full sector buffer. **XCOMP, Inc**, 9915A Businesspark Ave, San Diego, CA 92131.

Circle 269 on Inquiry Card

PROTECTED INTERCONNECTION HEADERS



A line of 0.1 x 0.1" (0.254 x 0.254-cm) pin matrix protected headers for board to cable interconnections offers 9 sizes and 3 configurations. Designed in straight, right angle, and wirewrap types, header sizes range from 10 to 60 pins. All headers are available with or without lock/ejector hooks. Contact material is selectively plated phosphor-bronze. **AP Products, Inc**, 1359 W Jackson St, Painesville, OH 44077.

Circle 270 on Inquiry Card

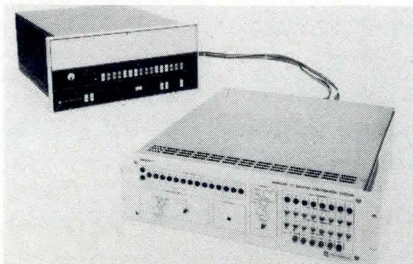
SMART CRT TERMINAL

Model 930 features a 25th status and message line, 22 programmable function keys, expandable definable data, split screen, 13 special char, and sophisticated printer controls. Printer controls allow an operator to move data through the printer via the CRT, talk to host computer via CRT, or move data from host to printer. An operator can use CRT at same time the system is printing. Heart of the unit is MOS Technology's 6502 microprocessor. **Televideo, Inc**, 2149 Paragon Dr, San Jose, CA 95131.

Circle 271 on Inquiry Card

ADC SYSTEMS

Including all interface circuits and functions necessary to operate with H-P 1000 series computer systems, GM/PL series units have conversion rates as high as 500 kHz and resolution and corresponding accuracy as high as 15 bits. Compatible with computers using std HP 93596L interface option, they provide DMA operation via the pacer and high speed pacer modes and programmed I/O via the non-pacer mode. TTL compatible signals include pacer mode clock, enable functions, STC commands, and control words for channel selection. **Preston Scientific, Inc**, 805 E Cerritos Ave, Anaheim, CA 92805.



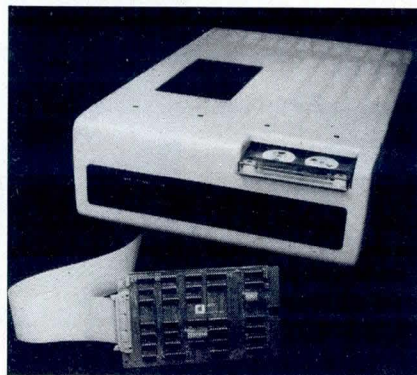
Circle 272 on Inquiry Card

BI-PIN LED PACKAGE

Wide viewing angle LEDy Bug[®] lamps, now available in the common bi-pin package, come with or without built-in resistors for drive voltage selection. High brightness LB202 and LB203 series lamps come in either red, amber or green, and can be driven by 2.4 to 28 V depending on model. LB202 is for mounting in std BPS-1 socket; LB203 is designed for soldering in place. More than 180° viewing angle is achieved by use of flat topped cylindrical fresnel lens. **Data Display Products**, 303 N Oak St, Inglewood, CA 90302.

Circle 273 on Inquiry Card

DISC/TAPE STORAGE SUBSYSTEM



A storage subsystem, consisting of an 8" (20.3-cm) Winchester disc, cartridge tape, and LSI-11 Q-bus interface, features a dual port I/O processor capable of interfacing up to 8 Winchester drives and 8 0.25" (0.635-cm) tape cartridge drives. The Compact Storage System 11 includes 32k bytes of RAM, 10M- to 20M-byte disc capacity, and 13.8M-byte tape cartridge. **United States Design Corp**, 100 Severn Ave, Ste 102, Annapolis, MD 21403.

Circle 274 on Inquiry Card

I/O CONNECTOR

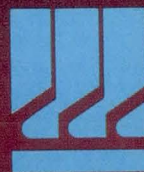
Series 6900 unprotected header connector is designed for simple installation on logic panels, PCBs, and backplanes. A high precision 1-piece molded header featuring 0.025" (0.65-mm) sq posts, device has an insulator that facilitates automatic pin loading and selective cutting of long strips to desired pin configuration. Selective gold plating of contact area cuts costs. Interconnection portion of post is selectively plated with 0.254, 0.508, or 0.762 μm of gold. **Stanford Applied Engineering, Inc**, 340 Martin Ave, Santa Clara, CA 95050.

Circle 275 on Inquiry Card

Digi-Data's Best Customers Have Switched From the Competition...

Here's Why:

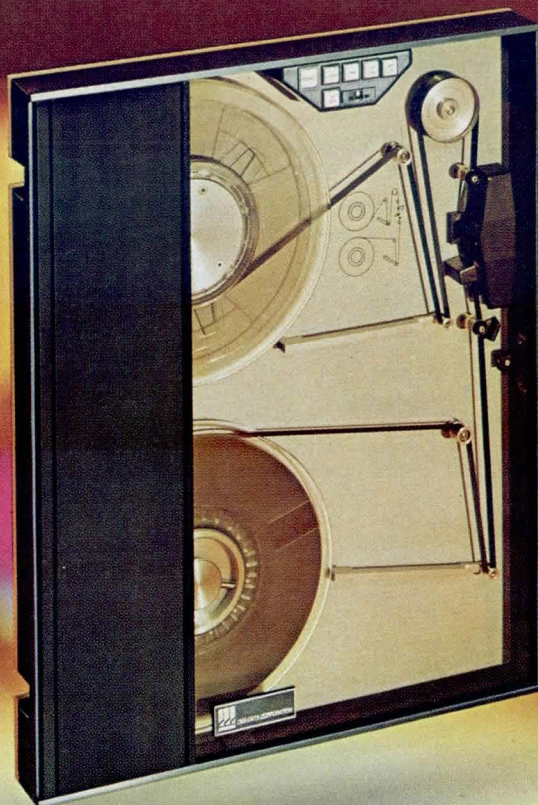
- they can depend on Digi-Data's product performance and reliability . . . assured by clean, simple design and proven in over 10,000 installations.
- they choose from 192 recorder models to get the speed, format and reel size to meet their every need.
- they receive guaranteed industry compatibility at the transport, formatter and computer levels.
- and, they always pay less.



**DIGI-DATA
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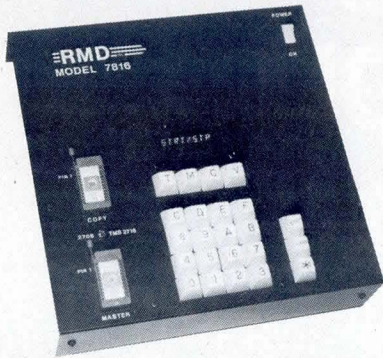
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7 SERIES EPROM PROGRAMMERS

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- Completely Self-contained
- Read Only Master Socket
- Alpha Numeric Display
- Data Entry Keyboard
- Merge and Edit Capability

Models Available for All Industry Standard EPROMs

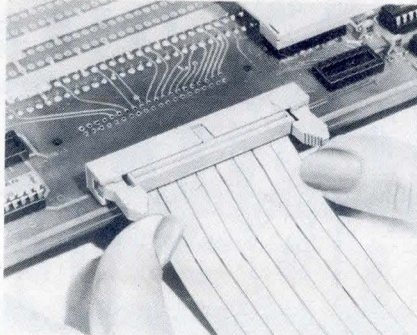
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PRODUCTS

LOW PROFILE LOCK AND EJECT HEADERS

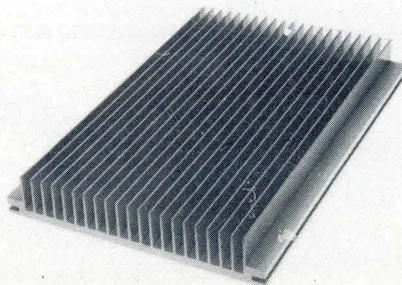


Header series BLUE MACS[®] is available with right angle straight soldertail contacts for use with 0.062" (1.57-mm) and 1.25" (3.18-mm) thick PCBs and in right angle and straight wrap post tail configurations. Locking ears eliminate possibility of unintentional disengagements. Ejector ear design eliminates stress at cable/connector and header/PCB solder joint areas in disconnect/reconnect actions. Full line is available in 11 contact sizes from 10 to 60 and in a variety of pin layouts. **T&B/Ansley Corp**, 3208 Humboldt St, Los Angeles, CA 90031.

Circle 276 on Inquiry Card

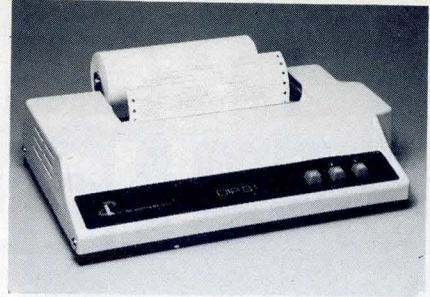
HEAT SINK EXTRUSION WITH SLIDE CHANNEL

Material can be used as a cabinet back panel, rack support, or sliding rack. Extrusion 2046 has 2 0.125" (0.3-cm) high slide channels to enable a variety of mountings. It weighs 3.94 lb/ft (0.6 kg/cm) and has a heat dissipating surface of 57.38 in²/in (145 cm²/cm). The heat sink extrusion, made of 6063-T5 aluminum, is 7.3" (18.5 cm) wide with overall height of 1.25" (3.2 cm). It has 21 evenly spaced fins of 1" (2.54 cm) height, with thermal resistance of 1.7 °C/W per 3" (7.6-cm) section. **AHAM tor**, 27901 Front Street, Rancho California, CA 92390.



Circle 277 on Inquiry Card.

DOT MATRIX IMPACT PRINTER



Full 96-char ASCII set, u/lc char, and 40 and 80 char/line are featured in the model DIP-81 data impact printer. Either 7 x 7 or expanded 14 x 7 matrix capability is included along with 100-char/s bidirectional printing. The unit measures 17 x 9.75 x 3.5" (43.2 x 24.8 x 8.9 cm) and includes Centronics type parallel interface, with RS-232-C or 20-mA current loop optional. **DIP, Inc**, 121 Beach St, Boston, MA 02111.

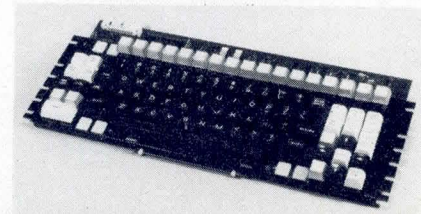
Circle 278 on Inquiry Card

NOISE SUPPRESSION INTERFACE MODULE

Designed as a noise suppression and ground isolation interface module between RS-232-C DCE/DTE devices, the OPTO232 handles from 2 to 16 signal/data lines as well as both signal and protective ground lines. 6N139 type optoisolators provide 1500 V of isolation for individual unidirectional signal/data lines, each of which can support transmission rates of 40k bits/s. **Interface of Illinois**, 9020 Niles Center Rd, Skokie, IL 60076.

Circle 279 on Inquiry Card

P/ROM PROGRAMMABLE CAPACITANCE KEYBOARD



Capacitance operated switching, N-key rollover, and operation from a single 5-Vdc supply are features of the MPNK-100 microprocessor keyboard. The onboard microprocessor functions with 2 512 x 4 P/ROMs, and the same PCB accommodates both P/ROMs and masked ROM applications. Intended for operation in word processing, prototyping, data entry, and custom use, the keyboard operates in 5 modes. **Amkey, Inc**, 7 Andover St, Andover, MA 01810.

Circle 280 on Inquiry Card

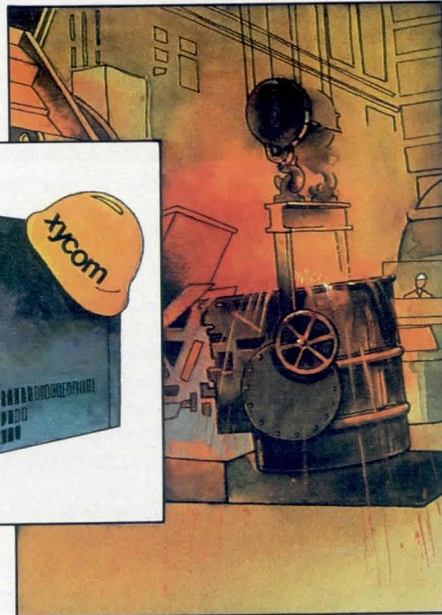
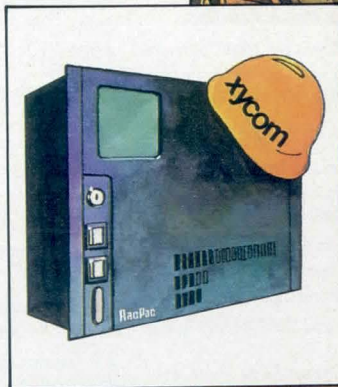
Our computers and modules wear hardhats

While others modified their existing general purpose computers to try to do factory work, we specially designed a full line of modules and microcomputer packages for rugged "hardhat" plant environments.

On Line, On the Firing Line— Full Time

The reason our customers want to hang computers such as RacPac right at the job is simple. The computer functions are more reliable when the microcomputer puts on a hardhat and goes right out on the job. Also, it puts the controls of the machine and the information with the operator for more efficient operation and maintenance.

In a manner of speaking, our computers do wear hardhats. We don't want our industrial computers going out in the plant looking like bankers. They're engineered to withstand the industrial environment—dust, dirt, vibration and wide temperature variations.



Wide Variety of Modules

There are over 20,000 XYCOM microcomputers working around the world, covering virtually every conceivable industrial application. We have a wide variety of modules readily available to quickly solve your unique application — sensors, resolvers, process

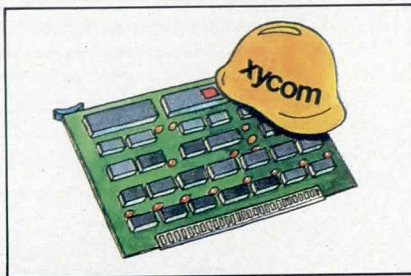


loops, A.C. motors or almost any other industrial control application. So, we probably have the modules to solve an OEM or Integrator problem now—faster, better, and more cost effectively.

Shake and Bake. It isn't for chickens.

Most general purpose computers are tested prior to shipment. But test specifications vary widely. In fact, many marginal component flaws that may show up in a hostile plant, may not be discovered during typical general purpose tests.

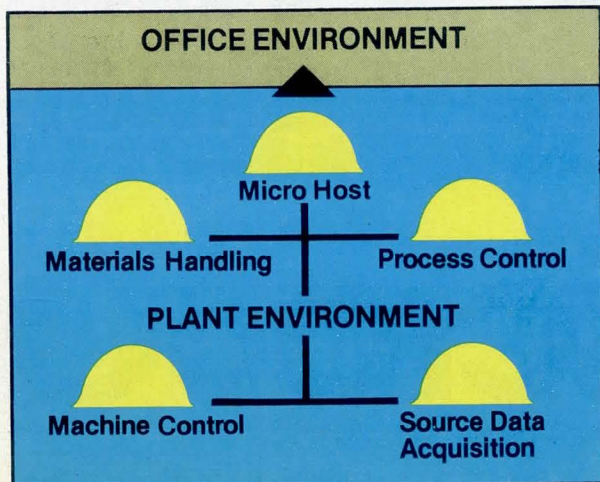
But, the plant environment requires tougher components. That's why we test to industrial specifications.



One Stop Shopping

XYCOM takes you a step closer. We supply all the tools you need (module level, package level, software, documentation) to interface our computers with your equipment.

So, give us a call and see how quickly XYCOM can help solve your problem.



Plant to office Interface

Our systems go right out into the hostile plant environment to control machines, processes, materials flow and acquire data at the source. Production data can then be supplied to a MicroHost computer located in a supervisors office and transmitted to data processing. It supplies management information that is vital for cost effective operation.

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A big week for small computer specialists

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Everything that's new and significant about small computers and systems will be on display on Mini/Micro's show floor and reviewed by experts in the Civic's four spacious auditoriums.

And there are some important extras! The Association of Computer Programmers and Analysts will hold its 10th anniversary conference just preceding Mini/Micro (call (800) 556-6882 for full details) and U.S.U.S. (the UCSD system users' society) will meet for three days during and following Mini/Micro. There will also be a day-long, Introduction to Pascal seminar.

Mini/Micro's professional program, previewed below, offers 60 hours of up-to-the-minute information in 24 half-day sessions.

Mark your calendar now, and use the coupon to request the Mini/Micro detailed preview program, available September 1.

TUESDAY, OCTOBER 14, 9:30 AM

1. The Small Business Computer in the Next Five Years
S. Henry Sacks, Mini/Micro Systems
2. Pascal Applications in the Minicomputer Environment
A. Winsor Brown, Point 4 Data Corp.
3. Professional Programmers/Analysts' Role with Small Computers
John Prior, Consultant
4. Impact of New Technologies on Marketing Opportunities for OEMs
Richard Able, Christman/Able Advertising

TUESDAY, OCTOBER 14, 1:30 PM

5. Quality Assurance for Small Computer Software
Murray Zuckerman, Consultant
6. Are Programmers Really Necessary?
Richard Dalton, Open Systems
7. Microcomputers in Banking
Robert Reffelt, Chase Manhattan Bank
8. Data Communications for Minicomputer Users
Roger Evans, Micom Systems

WEDNESDAY, OCTOBER 15, 9:30 AM

9. Pascal Open Forum: Implementation Interfacing to Existing Systems
A. Winsor Brown, Point 4 Data Corp.
10. Design Objectives for Color-Graphics Desktop Computing Systems
Ed Bride, Hewlett-Packard (DCD)
11. Winchester Disk and the Backup Issue: What's Happening?
Larry Hemmerich, Cipher Data Products
12. Effects of Microcomputers on Marketing
Jim Jordan, Moxon Electronics

WEDNESDAY, OCTOBER 15, 1:30 PM

13. IBM Watching: New Directions for Small Computers
John Rehfeld, International Data Corp.
14. Software Evaluation and Selection
Bill Fisher, Arthur Young & Co.
15. Session title and organizer to be announced.
16. Current trends in Computer Graphics
Dr. John Moreland, Megatek Corp.

THURSDAY, OCTOBER 16, 9:30 AM

17. Latest Armament in the Winchester Revolution
Randy Knapp, Wespercorp
18. Data Base Capabilities in Small Computers
Susan Kolb, Hewlett-Packard (DCD)
19. Computer Security in the Mini/Micro Environment
Bill Fisher, Arthur Young & Co.
20. Information Processing and Reporting: State of the Art in the "Paperless Society"
Mike Helft, Arthur Young & Co.

THURSDAY, OCTOBER 16, 1:30 PM

21. Distribution Alternatives for Small Business Computers
Robert R. Mueller, Office Products Dealer Magazine
22. Increasing Market Potential for Minicomputer Distribution
Bill McNamara, Systel Corp.
23. Systems in Hospitals and Health Care
Neil D. Kelley, Infosystems Magazine
24. Session title and organizer to be announced

Mini/Micro 80 32302 Camino Capistrano, Suite 202, San Juan Capistrano, Ca 92675

Please send me the detailed Mini/Micro preview program (Sept. 1)

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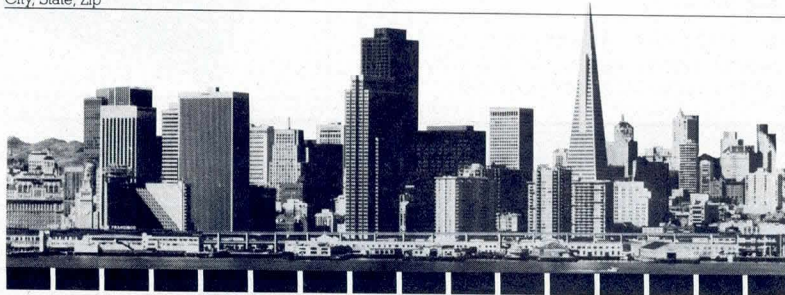
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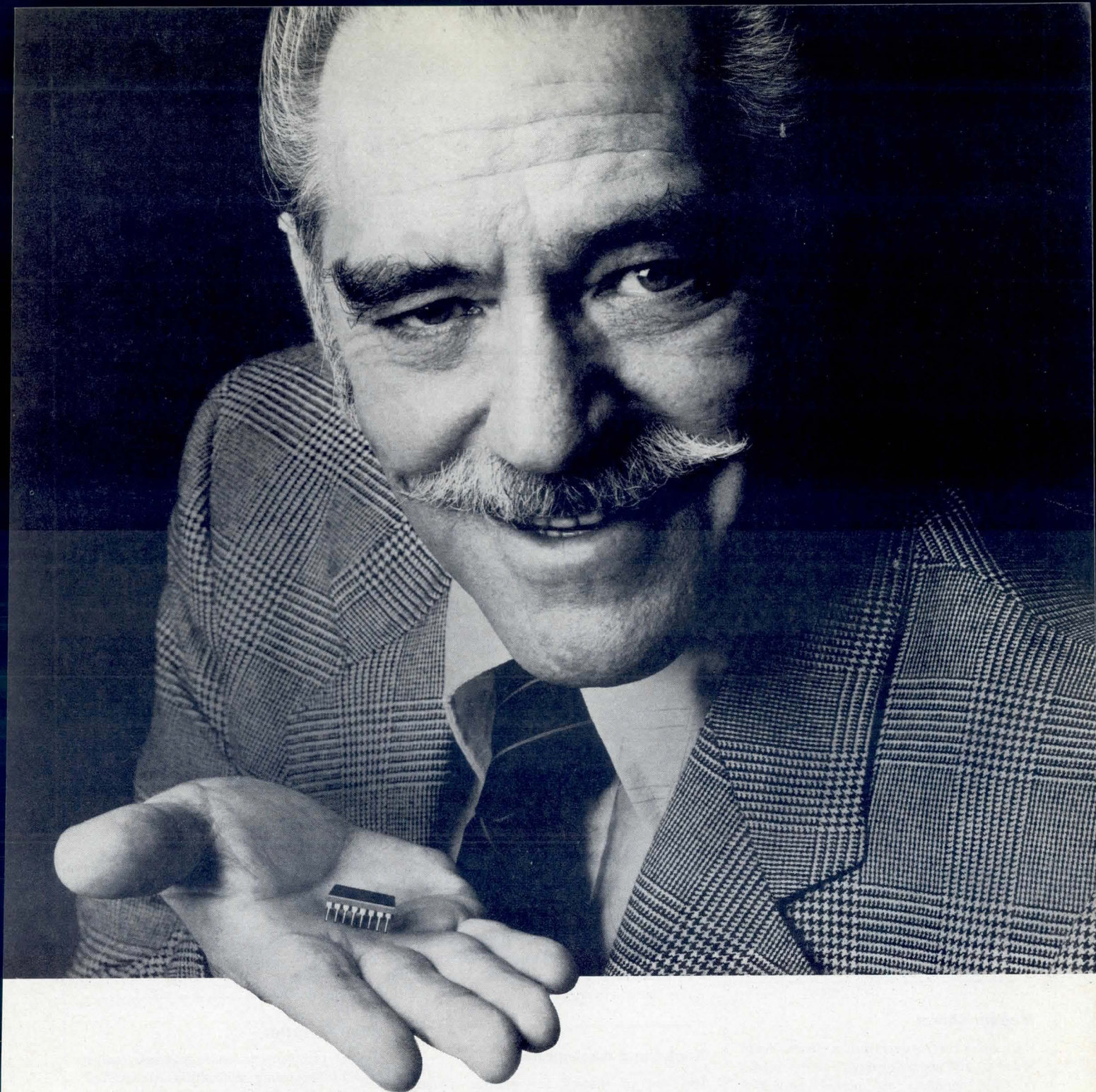
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LITERATURE

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Engineering data, cross-reference, specs, selection tables, application charts, photos, and dimensional drawings are given for components described in catalog. **Cornell-Dubilier Electronics**, Newark, NJ. Circle 300 on Inquiry Card

Data Conversion Components

Catalog/applications guide includes tutorial on A-D and D-A converter specs, data sheets, notes for military and commercial applications, tech briefs, and selection guide. **Micro Networks Co.**, Worcester, Mass. Circle 301 on Inquiry Card

Network Management Equipment

Guide discusses features, specs, and applications of switching, remote control, diagnostic, and data transmission components and supplies photos, diagrams, and systems engineering and wiring information. **Dynatech Data Systems**, Springfield, Va. Circle 302 on Inquiry Card

Digital Circuit Analyzer

Discussed in brochure with operational and technical specs and photos are field service and checkout applications of Signature II. **Kurz-Kasch, Inc.**, Dayton, Ohio. Circle 303 on Inquiry Card

Modem Sharer

Data sheet carries description, photo, list of features, and specs for device that replaces multiple modems in polled networks. **Xyquad Inc.**, St Louis, Mo. Circle 304 on Inquiry Card

Electrostatic Systems And Components

Static and its eliminators are explained in catalog furnishing specs, photos, and dimensional drawings for shockless bars and points, 5- and 8-kV power supplies, meters, generators, cables, connectors, adapters, and junctions. **Chapman Corp.**, Portland, Me. Circle 305 on Inquiry Card

MOS/LSI Devices

Charts, circuit diagrams, graphs, flowcharts, photos, and specs are furnished in catalog describing data communications devices, CRT displays, printers, baud rate generators, keyboard encoders, and microprocessor peripherals. **Standard Microsystems Corp.**, Hauppauge, NY. Circle 306 on Inquiry Card

Network Support Systems

Featured in illustrated brochure are monitoring and control equipment, intelligent matrix switch, and enhancement products, including LC 3600 loop controller for use with IBM 3600 financial communications system. **Codex Corp.**, Mansfield, Mass. Circle 307 on Inquiry Card

Tape and Disc Drives And Formatters

Brochure discusses features of Vanguard I disc drives, 6 models of tape drives, and tape formatters and supplies performance specs and photos. **Perkin-Elmer, Memory Products Div.**, Garden Grove, Calif. Circle 308 on Inquiry Card

Microprocessor Compatible 12-Bit A-D Converters

Bulletin presents series 7555 and 7556 with list of features, performance and physical specs, applications information, circuit and logic diagrams, and photos. **Beckman Instruments, Inc., Advanced Electro-Products Div.**, Fullerton, Calif. Circle 309 on Inquiry Card

Knobs and Accessories

Included in catalog are photos, dimensional drawings, color coded guide to 5 separate size series, and section on special hardware, as well as metric conversion table. **Power Dynamics, Inc.**, South Orange, NJ. Circle 310 on Inquiry Card

Analog Data Acquisition Systems

Catalog offers features, descriptions, operational characteristics, specs, charts, and photos of systems capable of up to 16 bits and lists subsystems and interfaces. **Phoenix Data, Inc.**, Phoenix, Ariz. Circle 311 on Inquiry Card

Microprocessor Controlled Dot Matrix Printers

Brochure describes features of IPS[®] 5000 and 7000 series, lists applications, and provides photos and selection guide. **Dataroyal, Inc.**, Nashua, NH. Circle 312 on Inquiry Card

Power Semiconductor Devices

Featured in catalog are selection charts and tables, photos, schematics, and dimensional drawings for HEXFET[™], rectifiers, thyristors, protective and optoelectric devices, diode bridges, and standard and custom assemblies. **International Rectifier, Semiconductor Div.**, El Segundo, Calif. Circle 313 on Inquiry Card

Analog, Digital, And Microprocessor ICs

Catalog lists features and specs for discrete and data acquisition devices, vertical power MOSFETS, linear circuits, counters, timers, display drivers, and military components. **Intersil, Inc.**, Cupertino, Calif. Circle 314 on Inquiry Card

Fiber Optic Cables

Brochure contains discussion of capabilities, matrix showing comparison with 6 conventional coaxial cables, selection guide, and photos. **Brand-Rex Co.**, Willimantic, Conn. Circle 315 on Inquiry Card

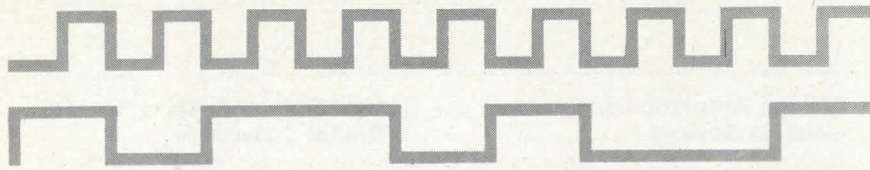
Digital Plotter

Driver programs in BASIC and interfacing and programming instructions are offered in 3 illustrated bulletins describing use of HI PLOT DMP-2[™] with Apple II[™], PET[™], and TRS-80[™] personal computers. **Houston Instrument**, Austin, Tex. Circle 316 on Inquiry Card

Rotary Solenoids

Listing over 225 types in 10 sizes, catalog provides electrical and mechanical specs, dimensional drawings, photos, and custom engineering sections illustrated with sample problems. **Ledex Inc.**, Vandalia, Ohio. Circle 317 on Inquiry Card

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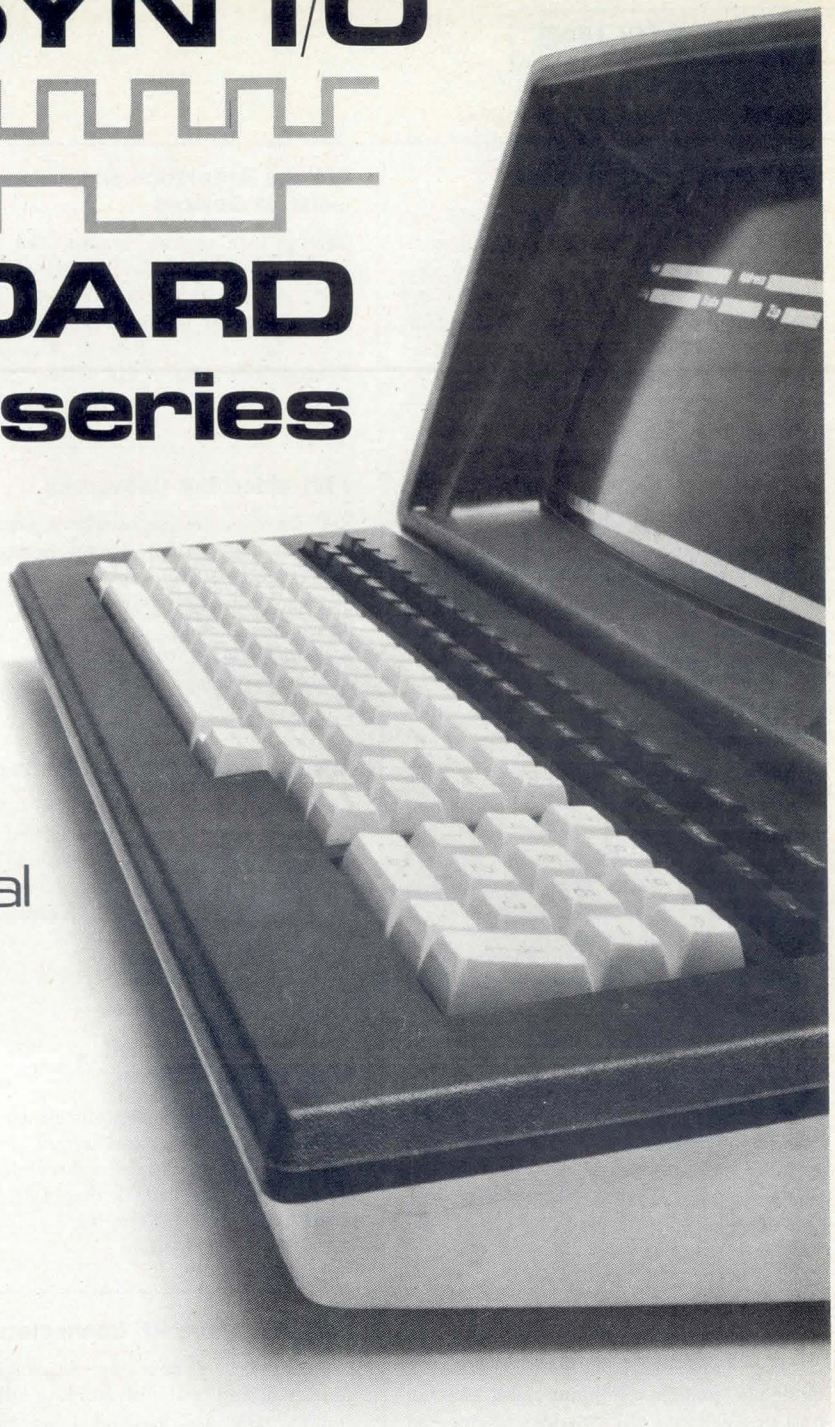
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Matrix Switching Systems

Illustrated brochure lists features of 3000 series for use with IBM and IBM plug compatible peripherals and provides configurations and specs for 3915/16/17 systems and 3934 remote channel activator. **T-Bar Inc.**, Wilton, Conn. Circle 318 on Inquiry Card

Fire Fighting Agent

BCFR Halon 1211, used in portable extinguishers and suitable for protection of electronic equipment against class A, B, and C fires, is illustrated and described in brochure. **ICI Americas Inc.**, Wilmington, Del. Circle 319 on Inquiry Card

Membrane Switch Keyboards

Illustrated brochure comparing 3 touch-in-panel families includes specs and discussion of design, construction, operation, application, design options, and standard switch panels. **Oak Technology Inc., Switch Div.**, Crystal Lake, Ill. Circle 320 on Inquiry Card

Small Angle Stepping Motors

Catalog comprises specs and selection chart for 38 models with angles of 1.8°, 2°, and 5° in frame sizes 23, 34, and 42, with torque range from 30 to 2000 oz-in (0.2 to 41 N.m). **Astrosyn America Inc.**, Van Nuys, Calif. Circle 321 on Inquiry Card

Data Communications Devices

Catalog describes 3 limited distance modems, modem eliminator, and sharing unit in 6000 series and provides photos and tables of operating distances in miles. **International Data Sciences, Inc.**, Lincoln, RI. Circle 322 on Inquiry Card

Microprocessor Crystals

Found in pamphlet describing standard quartz crystals from 1 to 48 MHz and custom crystals from 1 to 100 MHz are dimensional drawings of holder types, photo, specs, and electrical characteristics. **Bomar Crystal Co.**, Middlesex, NJ. Circle 323 on Inquiry Card

Voltage Regulation and Isolation Devices

Catalog with photos, graphs, and performance curves includes models for 50-Hz power systems and details features like protection against extreme fluctuations and noise filtering capabilities. **Frequency Technology, Inc., TDC Div.**, Littleton, Mass. Circle 324 on Inquiry Card

8-Bit Video D-A Converters

Bulletin discusses use of MP8308 and MP8318 in video and graphic display applications and supplies list of features, block diagrams, specs, operating details, outline dimensions, and glossary of terms. **Analogic Corp.**, Wakefield, Mass. Circle 325 on Inquiry Card

Keyboard Switches and Keytops

Found in catalog featuring series T-5, 138, and 142, leveling devices, and lighted switch lenses are photos, specs, dimensional drawings, PC board layouts, and mounting requirements. **Mechanical Enterprises, Inc.**, Springfield, Va. Circle 326 on Inquiry Card

Solid State Dedicated Programmable Timer

Features and functional controls are listed and modular concept and factory programmable P/ROMS explained in brochure supplying photos and block diagrams. **Electroid Corp.**, Springfield, NJ. Circle 327 on Inquiry Card

3-mm Miniature RF Connectors

Photos, specs, dimensional drawings, and mounting and assembly tooling information are provided in catalog highlighting hermetically sealed units. **Sealectro Corp.**, Mamaroneck, NY. Circle 328 on Inquiry Card

Electronic Components

Dimensional drawings, specs, and photos are incorporated in catalog describing ceramic disc and monolithic capacitors, rotary, touch, key, and pushbutton switches, and thick film circuits. **Centralab, Inc., A North American Philips Co.**, Milwaukee, Wis. Circle 329 on Inquiry Card

Synchro and Resolver to Digital Converters

Summarized in selection guide with photos are performance data and physical characteristics of single- and 2-speed, and multiplexed units and models ranging from 1.5 to 125 VA. **Control Sciences, Inc.**, Chatsworth, Calif. Circle 330 on Inquiry Card

Portable Oscilloscopes

Bulletin supplies descriptions, photos, and specs for dual-trace, true dual-beam, and digital storage scopes, together with output options and model and accessory list. **Gould Inc., Instruments Div.**, Cleveland, Ohio. Circle 331 on Inquiry Card

1/2" Streaming Tape Drive

Outline of comparative advantages for minicomputers, comparison of leading memory technologies, and selection and applications data are found in brochure. **Cipher Data Products, Inc.**, San Diego, Calif. Circle 332 on Inquiry Card

Luminous Gas Discharge Displays

Brochure lists applications and features of 50- and 80-mm devices and includes electrical and mechanical specs and circuit diagrams. **Boston Electronics Corp.**, Brookline, Mass. Circle 333 on Inquiry Card

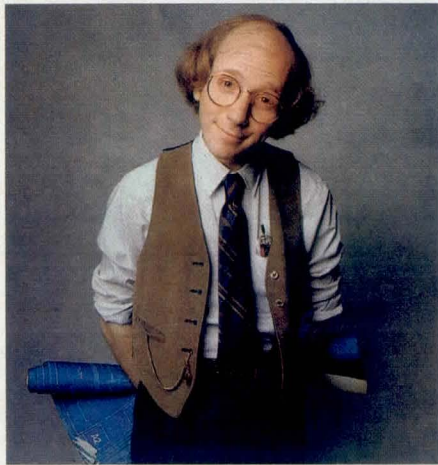
10M- and 20M-Byte Streaming Magnetic Tape Drives

Data sheet presents photo, specs, and description of "The Streamer," S-3 series for Winchester disc backup, using 1/4-in ANSI/ECMA tape cartridges. **Data Electronics, Inc.**, San Diego, Calif. Circle 334 on Inquiry Card

Bus Compatible Boards

Features of CPUs, RAMs, ROMs, EPROMs, I/Os, analog devices, and backplanes, with names, addresses, and phone numbers of vendors, are listed in PUB-MR2 Multibus™ Market Report. Available for \$17.00 (prepaid) from **Perfect Information Associates**, PO Box 2751, Woburn, MA 01888.

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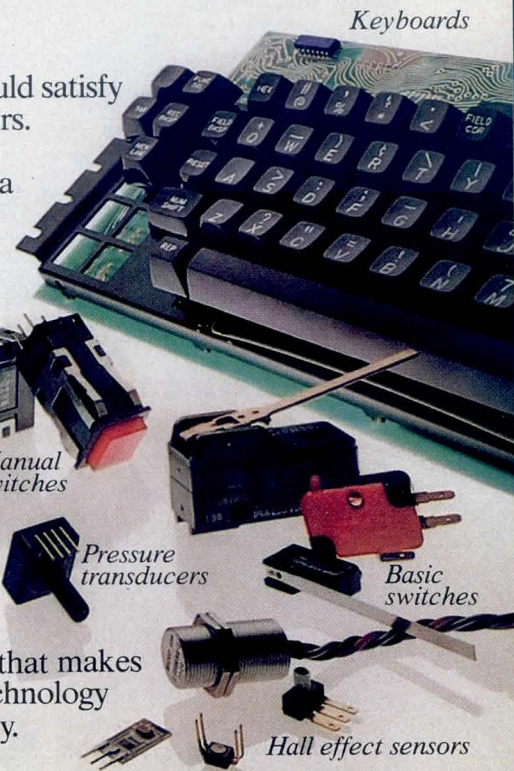
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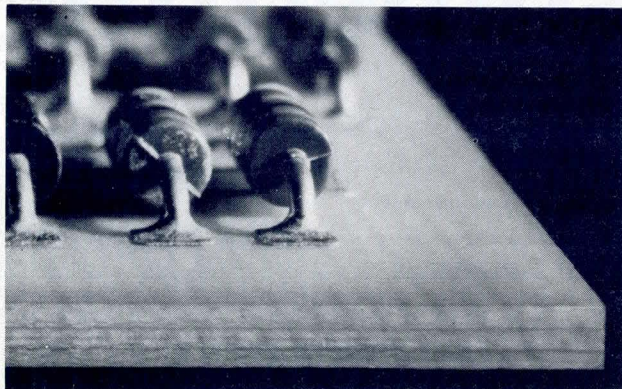
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ADVERTISERS' INDEX

ADAC Corp.....	4
Adaptive Science Corp.....	198
Advanced Electronics Design.....	145, 147
Advanced Micro Devices.....	28, 29
American Magnetics Corp.....	168
Ametek.....	159
AMP.....	88, 89
Amperex Electronic Corp, an NA Philips Co.....	160
Ampex Memory Products.....	141
Anadex.....	219
Analog Devices.....	103
Andromeda Systems.....	193
Ann Arbor Terminals.....	226
Audiotronics.....	59
Avco.....	206
Axiom.....	207
Aydin Controls.....	95
Beehive International.....	245
Belden Corp.....	17-20, 183
Bulova.....	252
Burr-Brown.....	153
CalComp.....	8, 9
Canon, USA.....	234
Centronics.....	43
Chapman Corp.....	201
Charles River Data Systems.....	101
Chatsworth Data.....	213
Columbia Data Products.....	77, 148
Compas Microsystems.....	202
Computer Automation, Naked Mini Div.....	71
Computer Sciences.....	251
Computrol.....	186
Condor.....	220
Custom Systems.....	222
Datafusion Corp.....	181
Data General Corp.....	110, 111
Data I/O.....	175
Data Management Labs.....	93
Dataram Corp.....	5, 91
Data Systems Design.....	11
Datum.....	55
DeAnza Systems.....	47
Dennison KYBE Corp.....	156f
Dialight.....	24, 25
Digi-Data Corp.....	239
Digital Engineering.....	221
Digital Equipment Corp.....	84, 85
Digital Pathways.....	83
Distributed Logic Corp.....	132
Dunn Instruments.....	231
The Dylon Corp.....	92
Eastern Air Devices.....	217
Electronic Processors.....	167
Epson America.....	235
Ex-Cell-O Corp, Remex Div.....	237
Fairchild Semiconductor.....	23
Floating Point Systems.....	225
Ford Aerospace & Communications.....	156a
Frost & Sullivan.....	252
Fujitsu America.....	69
GAW Control Corp, TDX Peripherals Div.....	44
General Electric Co, Terminet Div.....	173
General Terminal Corp.....	26
Gould.....	123, 124
Biomation Div.....	6, 7, 171
Foil Div.....	248
Grinnell Systems.....	63
Hazeltine Corp.....	229
Hewlett-Packard.....	80, 81, 197
High Precision Grinding & Mfg.....	208
Hitachi.....	56, 57
Houston Instrument.....	Cover III
Hughes Aircraft Co.....	155, 249
Hycom.....	70
Hytek Microsystems.....	248
IEE (Industrial Electronic Engineers).....	161
Industrial Programming.....	61
Integral Data Systems.....	169



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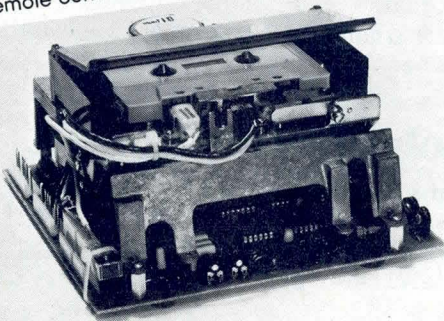


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ADVERTISERS' INDEX

Intel Corp.	40, 41, 156b, 156c
Intertec Data Systems	31
ITT Cannon Electronic	187
ITT Datanetics Corp.	227
Kennedy Co.	1
KMW	58
Kyocera International	157
LaVezzi Machine Works	232
Lear Siegler	52, 53
Mannesmann Tally	2
MDB Systems	223
Megatek Corp.	Cover II
MFE Corp.	50
Michigan Plastics	216
MicroSwitch, a Honeywell Div.	247
Mini Micro/80	242
Mitsubishi	151
Monolithic Memories	36, 37
Monolithic Systems	114
Mostek	72, 73, 177
Motorola	
Component Products	230
Semiconductor Products	12, 13, 64, 65, 162, 163
Multiwire	233
National Electric Cable	16
National Instruments	174
NEC Information Systems	15
NEC Microcomputers	164, 165
North Star Computers	214
OK Machine & Tool Corp.	156g
Optical Coating Laboratories	74
Opto 22	87
PCK Technology	209
Pennwalt Corp.	216, 217
Penril Corp.	39
Permag Corp.	94
Pertec Computer Corp, Peripherals Div.	109
Philips Test & Measuring Instruments	79
Power General	215
Power-One	76
Practical Automation	182
Priam	104, 105
Qantex, Div NOAT	199
Qume	51
Ramtek	Cover IV
Raymond Engineering	228
RMD	240
Robinson-Nugent	96, 97
Schrack Relay	22
Semicon	108
Shugart Associates	142, 143
Shugart Technology	203
Siemens Corp.	149
Signal Transformer Co.	62
Simplatrol Products	154
Stanford Applied Engineering	30
Storage Technology Corp.	32, 33
T&B/Ansley	179
Tandon Magnetics	156
TASA	78
TEAC Corp of America	224
Technology Transfer Institute	178
Techtran Industries	200
Tektronix, Inc.	112, 113
Teletype Corp.	195
TEXAS INSTRUMENTS	34, 35, 106, 107, 189
3M Company	66, 67
Toshiba America	45, 243
TransNet Corp.	250
Triple I	250
Univ. of Petroleum & Minerals	202
Vikron	234
Xycom	241
Zendex Corp.	99
Zilog	48, 49

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