

# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

SEPTEMBER 1976

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CCDs IN MEMORY SYSTEMS  
MOVE INTO SIGHT

MICROPROCESSORS AID EXPERIMENTATION  
IN SCIENTIFIC LABORATORY

TOP-DOWN DESIGN STREAMLINES DIGITAL SYSTEM PROJECTS



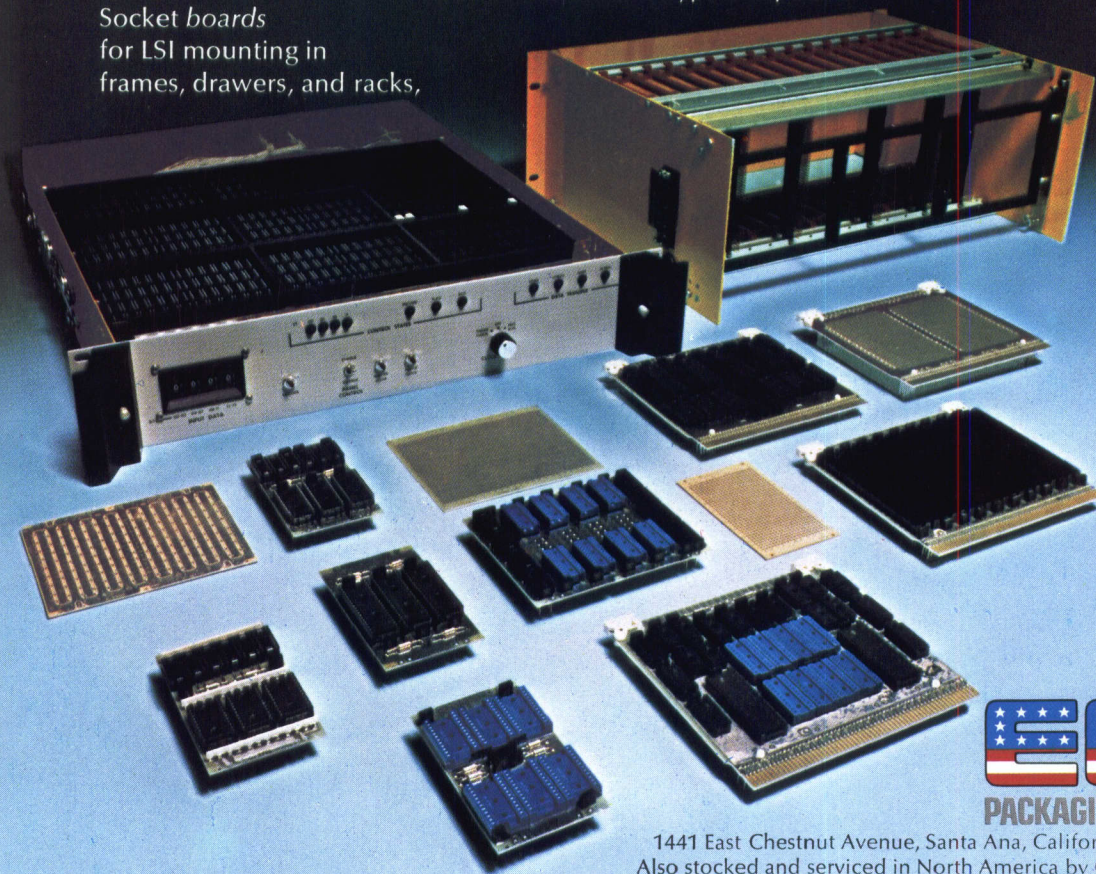
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The Model T-1202 is the newest member of the T-1000 Series—Tally's fine line of serial printers that offer microprocessor electronics, low acoustic noise level, digitally controlled print head advancement, dual tractor engagement and a convenient snap-in ribbon cartridge.

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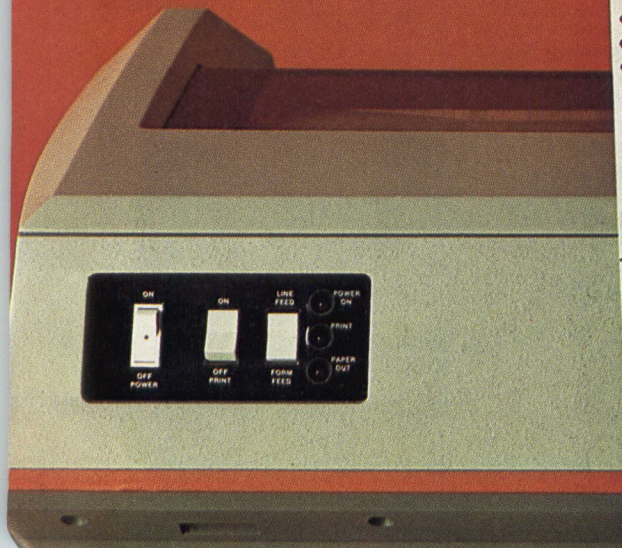
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PRINT WIDTH	132 COLUMNS
MATRIX	9 x 7
SLEW SPEED	7 INCHES PER SECOND
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PAPER WIDTH	4 TO 15.5 INCHES
RIBBON LIFE	1.5 BILLION CHARACTERS

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# THE MAGAZINE OF DIGITAL ELECTRONICS

# COMPUTER DESIGN

SEPTEMBER 1976 • VOLUME 15 • NUMBER 9

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### 75 CCDs IN MEMORY SYSTEMS MOVE INTO SIGHT

by H. B. Crouch, J. B. Cornett, and R. S. Eward

Just beginning to become commercially available, CCD devices should soon move into the gap that exists between rotating magnetic memories and RAMs, where they will provide reliable performance and low power dissipation at low cost per bit

### 83 MICROPROCESSORS AID EXPERIMENTATION IN SCIENTIFIC LABORATORY

by Thomas A. Seim

To achieve their full potential, microprocessors will require that the designer change his attitude and overcome his conditioning to hardware design limitations

### 91 TOP-DOWN DESIGN STREAMLINES DIGITAL SYSTEM PROJECTS

by Matthew L. Fichtenbaum

Top-down design not only aids in organizing and managing design of large digital systems, but reduces errors, decreases necessary debugging time, and permits changes to be incorporated late in the design cycle

### 98 SIMPLE ENCODING SCHEMES DOUBLE CAPACITY OF A FLEXIBLE DISC

by David J. Kalstrom

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### 104 MINICOMPUTER PERIPHERAL AIDS PROGRAM DEBUGGING

by Stephen R. Alpert

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Half the size of a standard floppy drive and with one third the storage capacity, this unit offers superior data integrity, fast data throughput, and random-access capability to designers of small computer systems

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OVER 55,000

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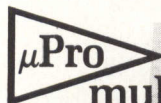
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## CORTRON DIVISION FORMED BY ITW

With a strong market demand and a promising future for keyboard products, ITW formed a new division, CORTRON, to handle full responsibilities for electronic keyboards and key switches. Following a proven ITW strategy, CORTRON concentrates a special division team of experienced Licon design, manufacturing and marketing people on this new major business opportunity.

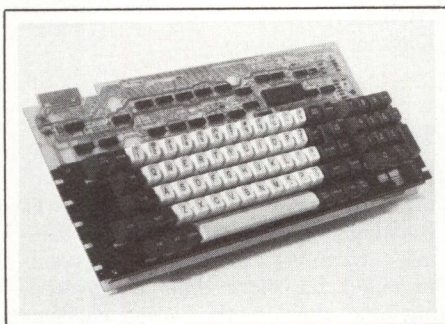
## KEYBOARD MARKET DIVERSIFIED

Typical applications for CORTRON™ Keyboards include data and word processing, computerized accounting, production and inventory control systems, retail point-of-sale and remote banking terminals, airline reservation and seat assignment stations, typesetting and text editing systems. And new applications are continually surfacing.

## PROVEN PRODUCT RELIABILITY

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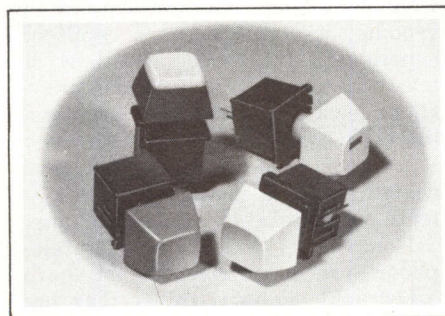
established reputation for excellence and reliability. The



CORTRON Series 555 Solid State Keyboard is a sophisticated electronic device. Its high reliability protects against costly service calls and the hardship of downtime. The low profile alpha numeric keyboard has the human engineered "feel" required by your marketplace. This promotes speed, accuracy and greater operator productivity.

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Key Switch is respected throughout the industry for its ultra reliable 100 million cycle life rating. Utilizing a ferrite core switching technology, the key switch is mechanically simple with only four basic parts.

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CORTRON is writing the solid state keyboard success story.

TO BE CONTINUED . . .



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**THE KEYBOARD  
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## LETTERS TO THE EDITOR

To the Editor:

"Shortcut to Logarithms Combines Table Lookup and Computation" proposed by San-Yen Shi (May 1976) appears to achieve exactly the opposite of its intended goal, requiring both a large table and heavy computation.

There is extensive literature relating to computation of such functions, which Mr Shi would have done well to consult. A particularly simple introduction is *Scientific Analysis on the Pocket Calculator* by Jon Smith (Wiley, 1975) which describes several practical methods for computing logarithms and other functions, along with techniques for deriving additional special-purpose methods when required. Such methods are often based on construction of an "interpolation function" which passes through tabulated values of the desired function in the region of interest.

Real numbers are usually stored as an exponent (base 2) and a fractional part, so the log of such a number is simply  $\log(\text{fraction}) + \text{exponent} \times \log(2)$ , and the problem reduces to computation of the log of a number between 0 and 1.

Smith describes several such methods, normally of the form  $\log(x) = y(a_1 + y(a_2 + y(a_3 + y(a_4 + ya_5))))$ , where  $a_i$  are constants and  $y$  is a simple function of  $x$ . Each term requires one constant, one addition, and one multiplication; 6-digit accuracy need not require more than six terms. The particular method used in the subroutine library on our mini-computer uses five constants, six additions, four multiplications, and two divisions to compute logs of any number from  $10^{-19}$  to  $10^{19}$  to 7-digit accuracy.

Mr Shi's method is restricted to arguments between  $10^{-9}$  to  $10^9$ , and requires a table of 63 constants; the rather involved computation requires a search process which uses at least one multiplication and one addition per digit, for the optimal case where the search succeeds on the first try for each digit. The particular example given in the paper required 11 multiplications and 11 additions, not to mention the search overhead.

Dr Brad J. Cox  
University of Chicago  
Chicago, Ill

*The Author Replies:*

The arithmetical operations that Dr Cox mentions must be in floating-point arithmetic, but my algorithm does not require any floating-point computation. On the contrary, it can be carried out on an ordinary 4-function calculator, as well as in a computer. The algorithm's speed can be improved for numbers of many decimal places by noting that in column 6 of the table, and in all columns to its right, the table entry is 1 plus the particular digit of  $x$  being looked up—a consequence of the approximation  $e^x \approx 1 + x$ , valid when  $x$  is less than  $10^{-5}$ . This approximation reduces the table search time considerably.

San-Yen Shi  
NCR Corp  
Dayton, Ohio

To the Editor:

For several months I have been reading with great interest Mr John E. Buckley's "Communication Channel." However, each column seems to anger me more than the preceding one due to the misconceptions and falsehoods that are spread. The May column ("Computerized PBX Systems") particularly incensed me with its many misconceptions.

First, since the early 1920s all common control switches (including the step-by-step, which was the first switch ever used, and was installed as early as 1894) have had stored program control. Programmable computer-controlled switches date from the late 1930s (predating Univac, et al). The telephone industry not only kept up with early technology, but also developed as fast as, if not faster than, the computer industry. This is because most computer technology did not develop in a vacuum; it developed as a result of experiments in development labs of telephone equipment manufacturers. Older switches have not been replaced just because new technology has come forward; rather they have waited until the components and systems were reliable enough to use.

Components and systems for telephone use generally do not have catastrophic failures, rather they are replaced after being maintained for

20 to 30 years or more. Another reason for not replacing older switches is economic rather than technological. Switches are depreciated over 10 to 20 years, and with regular maintenance (as explained above) at least 40 years or more. Some switches now being replaced have been in service 50 to 60 years, and for the most part still have original components. How many early computers can you say that about?

Robert Schoenfeld  
LD Networks Inc  
East Meadow, NY

*The Author Replies:*

It is regrettable that the May "Communication Channel" was a cause of anxiety and irritation to Mr Schoenfeld. To begin with, I suggest that he re-evaluate his personal concept of the term "stored program control." Early telephone switching systems definitely were not stored-program systems and the step-by-step systems, such as the present Western Electric 701 PBX systems, are not even common control systems. If his contention that "programmable computer-controlled switches date from the late 1930s . . ." is true, the U.S. Patent Office, Drs Mauchley and Eckert, and the whole computer industry must be thoroughly shocked.

The observation that today's computer industry must acknowledge that its beginnings and developments emanated from ". . . development labs of telephone equipment manufacturers" should certainly stimulate an interesting response from readers of *Computer Design*. Many of the readers who authored those developments thought they were employed by computer manufacturers.

For years I have been under the impression that the free enterprise system in the U.S. with its inherent profit motivations stimulated independent manufacturers to continually advance their product sophistications. In this environment, a better product at an equal or lower cost usually could be equated to a greater profit in an expanding marketplace.

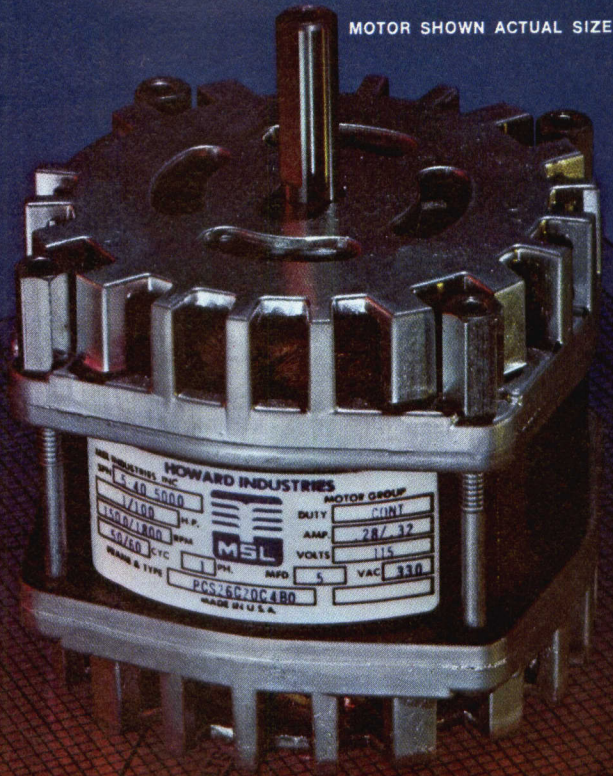
John E. Buckley  
Telecommunications Management  
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Cornwells Heights, Pa

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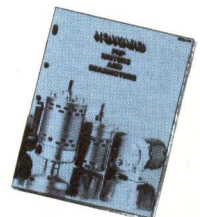
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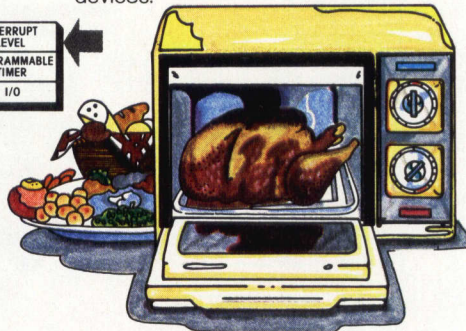
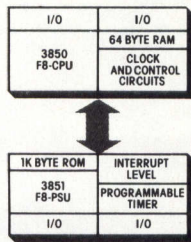
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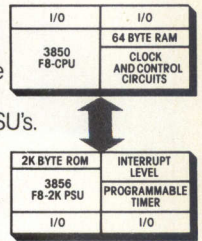
Two chips do it all – a \$9.95 PSU (Program Storage Unit) and F8 CPU (Central Processing Unit) for \$9.95. The CPU is an 8-bit device, with a cycle time of 2 micro-seconds. It's the heart of all F8 microprocessors. It includes 70 instructions, 64-byte RAM (Random Access Memory), instruction register, accumulator, 16 individually controllable I/O lines, power-on reset, on-chip clock and control lines to other devices.

The PSU features a 1K byte ROM (Read Only Memory), program counter, 16 individually controllable I/O lines, 8-bit data port, stack register, incrementer/adder, and programmable timer and interrupt.

We're the only manufacturer in the world to offer this 2-chip performance. The 8080 requires 7 chips (9 chips with timer) to do the same thing.

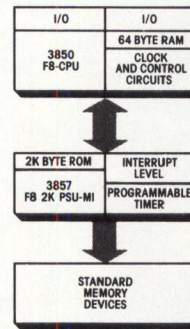
**Double the program storage**

If you need more program space, just substitute PSU's. Our new 2K byte PSU offers twice the ROM for only \$14.95.

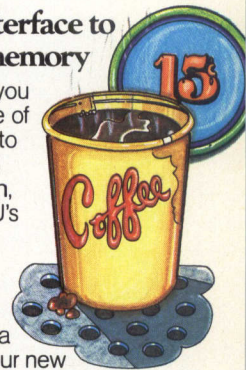


**Built-in interface to external memory**

But suppose you need a couple of RAM's added to your CPU and 2K/PSU. Again, substitute PSU's for one with a built in memory interface. Avoid paying for extra chips. Order our new 2K/PSU-MI for \$14.95. This is super microprocessor power on 4 chips.



The 8080 takes 10 chips (12 with timer) to do the same thing.



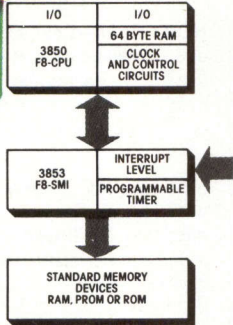
# Fairchild's \$9.95 F8 Microprocessor

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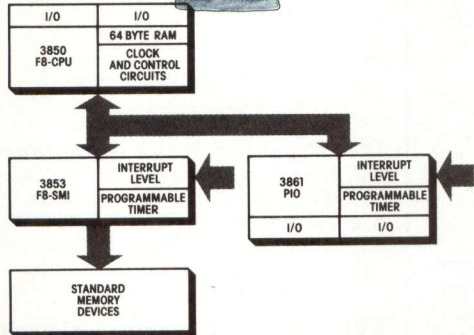
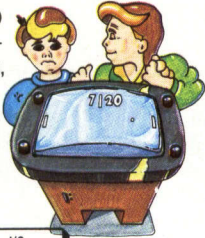
If you don't want to commit to ROM, consider interfacing RAM and/or PROM (Programmable Read Only Memory) directly into the CPU. This approach is ideal when your production run is under 1,000 units, and for development prior to long production runs.



This F8 configuration uses only four chips: a CPU, a \$7.45 SMI (Static Memory Interface with interrupt and programmable timer) and two 2K PROMs. Competitors take twice as many chips to do the same thing.

## Where more I/O is needed

By adding our \$6.45 PIO (Parallel I/O) to this aforementioned configuration, you gain 16 I/O ports, another level of interrupt and a programmable timer. Now you have the perfect 5-chip microprocessor system for electronic scales, paper tape and cassette tape handlers, electronic games, traffic light control, cash register and similar applications.



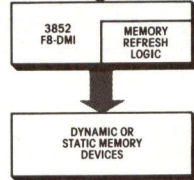
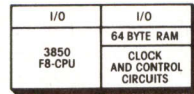
Competitors take 10 chips to do the same thing.

## Memory intensive systems

In memory intensive applications like message concentrators, floppy disc controllers, and store-and-forward message switching you'll enjoy big benefits with the F8's DMI (Dynamic Memory Interface).



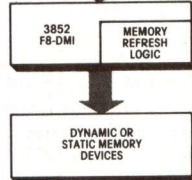
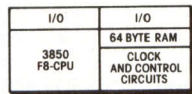
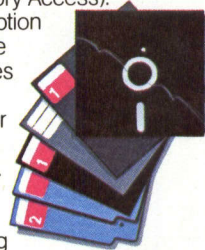
This \$7.45 device fits between your CPU and dynamic (or static) memory WITHOUT A MEMORY REFRESH CHIP.



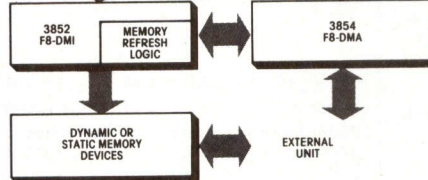
Memory refresh logic is built into the DMI, and operates in sync with the CPU. Your CPU never stops. There's no cycle stealing. No performance degradation. We are the only manufacturer in the world to offer this advantage.

A supercharger for this memory intensive configuration is DMA (Direct Memory Access).

This \$5.95 option comes in one chip. It creates a direct link between your memory and external data. All functional and internal system timing



is built in. The DMA can run at 500K bytes/sec and never slows down the rest of the system.



## Expand your system

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# CALENDAR

## CONFERENCES

**SEPT 21—Sym on Microprocessor Reliability in Severe Environments**, UCLA, Los Angeles, Calif. INFORMATION: Bruce Kaufman, Controlex Corp, 16005 Sherman Way, Van Nuys, CA 91406. Tel: (213) 780-8877

**OCT 6-7 and 19-20—Instrumentation and Computer Fair**, Sheraton/Valley Forge Hotel, King of Prussia, Pa and Sheraton Inn/Washington-Northeast, Lanham, Md. INFORMATION: Robert E. Harar, Executive Director, Instrumentation and Computer Fair, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

**OCT 11-13—Internat'l Society for Hybrid Microelectronics Internationale '76**, Hotel Vancouver, Vancouver, BC Canada. INFORMATION: ISHM, PO Box 3255, Montgomery, AL 36109

**OCT 11-14—First Cryogenics Instrumentation Sym, ISA-76 Conf and Exhibit**, Houston, Tex. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

**OCT 12-14—EUROMICRO, Second Sym on Micro Architecture**, Venice, Italy. INFORMATION: Jan Wilmink, Program Chm, Euro-micro Symposium, Twente U of Technology, PO Box 217, Enschede 7801, Netherlands

**OCT 12-15—Micro/Minicomputer Exhibit**, U.S. Trade Center, Frankfurt, Germany. INFORMATION: Bureau of International Commerce, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3748

**OCT 13-15—Second Internat'l Conf on Software Engineering**, San Francisco, Calif. INFORMATION: Dr C. V. Ramamoorthy, Program Chm, Dept of Electrical Engineering and Computer Sciences, U of California-Berkeley, Berkeley, CA 94720

**OCT 19-21—Mini/Micro Computer Conf and Exposition**, Brooks Hall/Civic Auditorium, San Francisco, Calif. INFORMATION: Mini/Micro Computer Conf and Exposition, 5544 E La Palma Ave, Anaheim, CA 92807. Tel: (714) 528-2400

**OCT 19-21—IEEE Semiconductor Test Equipment Sym**, Cherry Hill Inn, Cherry Hill, NJ. INFORMATION: Annual Test Symposium Committee, IEEE Philadelphia Section, U of Pennsylvania, Moore School of EE, Philadelphia, PA 19174

**OCT 20-21—9th Annual Connector Sym**, Hyatt House, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014

**OCT 21-22—IEEE Canadian Conf on Communications and Power**, Montreal, Canada. INFORMATION: Jean Jacques Archambault, Chm, IEEE Conf, CP/PO 958, Succ "A," Montreal, Quebec H3C 2W3 Canada

**OCT 25-27—17th Annual Sym on Foundations of Computer Science**, Houston, Tex. INFORMATION: Prof Michael J. Fischer, Program Chm, Dept of Computer Science, FR-35, U of Washington, Seattle, WA 98195

**OCT 26, OCT 28, and NOV 18—1976/77 Invitational Computer Conferences**, Chicago, Ill; Minneapolis, Minn; and Dallas, Tex. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

**NOV 1-3—Cybernetics and Society Internat'l Conf**, Mayflower Hotel, Washington, DC. INFORMATION: W. H. vonAlven, FCC, 1919 M St, NW, Washington, DC 20554

**NOV 8-11—Third Internat'l Joint Conf on Pattern Recognition**, Del Coronado Hotel, Coronado, Calif. INFORMATION: A. Rosenfeld, U of Maryland, Computer Science Center, College Park, MD 20742

**NOV 8-11—Mini and Microcomputers**, Hotel Toronto, Toronto, Canada. INFORMATION: Mini and Microcomputers—Hamza, PO Box 3243, Station B, Calgary, Alberta T2M 4L8 Canada

**NOV 8-12—Exhibition of U.S. Computers and Peripheral Equipment**, U.S. Trade Center, Sydney, Australia. INFORMATION: Irwin D. Nathanson, Office of International Marketing, DIB-233, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4957

**NOV 15-18—CAD/CAM IV (Fourth Computer-Aided Design and Computer-Aided Manufacturing Conf and Exposition)**, Dallas Hilton Hotel, Dallas, Tex. INFORMATION: CAD/CAM IV, Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128

**NOV 17—Computer Networks: Trends and Applications**, Gaithersburg, Md. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

**NOV 23-25—COMPEC'76 (Computer Peripheral, Small Computer, and Systems Exhibition)**, Wembley Conf Centre, Wembley, Middlesex, England. INFORMATION: Trident Conferences and Exhibitions Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU England

**NOV 23-27—Conf-Exhibition of Automation and Instrumentation**, Milan, Italy. INFORMATION: Federation of Scientific and Technical Associations, Piazzale Rodolfo Morandi, 2 (Piazza Cavour)-20121 Milano, Italy

**NOV 25-DEC 1—electronica 76 (7th Internat'l Trade Fair for Components and Production Facilities)**, Munich Fairgrounds, Munich, Germany. INFORMATION: Münchener Messe- u. Ausstellungsgesellschaft mbH, München 12, Postfach 12 10 09, Messegelände, Germany

**NOV 29-DEC 1—Nat'l Telecommunications Conf**, Fairmont Hotel, Dallas, Tex. INFORMATION: J. H. Tilley, Gen Chm, Collins Radio Group, 1200 N Alma Rd, Richardson, TX 75080

**DEC 6-8—IEEE International Electron Devices Meeting**, Washington Hilton Hotel, Washington, DC. INFORMATION: C. Neil Berglund, Bell-Northern Research, POB 3511, Station C, Ottawa, Ontario K1Y 4H7 Canada

## SEMINARS

**OCT 13-15—Workshop on Human Engineering Aspects in Design Automation Systems**, Michigan State U, East Lansing. INFORMATION: Edward A. Vrablik, ML1/E24, Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Tel: (617) 897-5111, X4931

**OCT 21-22—Principles and Applications of Digital Communications**, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: Dr K. Feher, Eng, Concordia University, 1455 de Maisonneuve Blvd W, Montreal, Quebec H3G 1M8 Canada

## SHORT COURSES

**SEPT 27-OCT 1—Modern Data Communications, OCT 6-8—Digital Satellite Systems and Technology**, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

**SEPT 27-OCT 1 and OCT 11-15—Microcomputer Design and Applications**, Atlanta Townhouse Motor Inn, Atlanta, Ga and New Mexico State U, Las Cruces, NM. INFORMATION: Educational Registrar, IEEE, 445 Hoes Lane, Piscataway, NJ 08854



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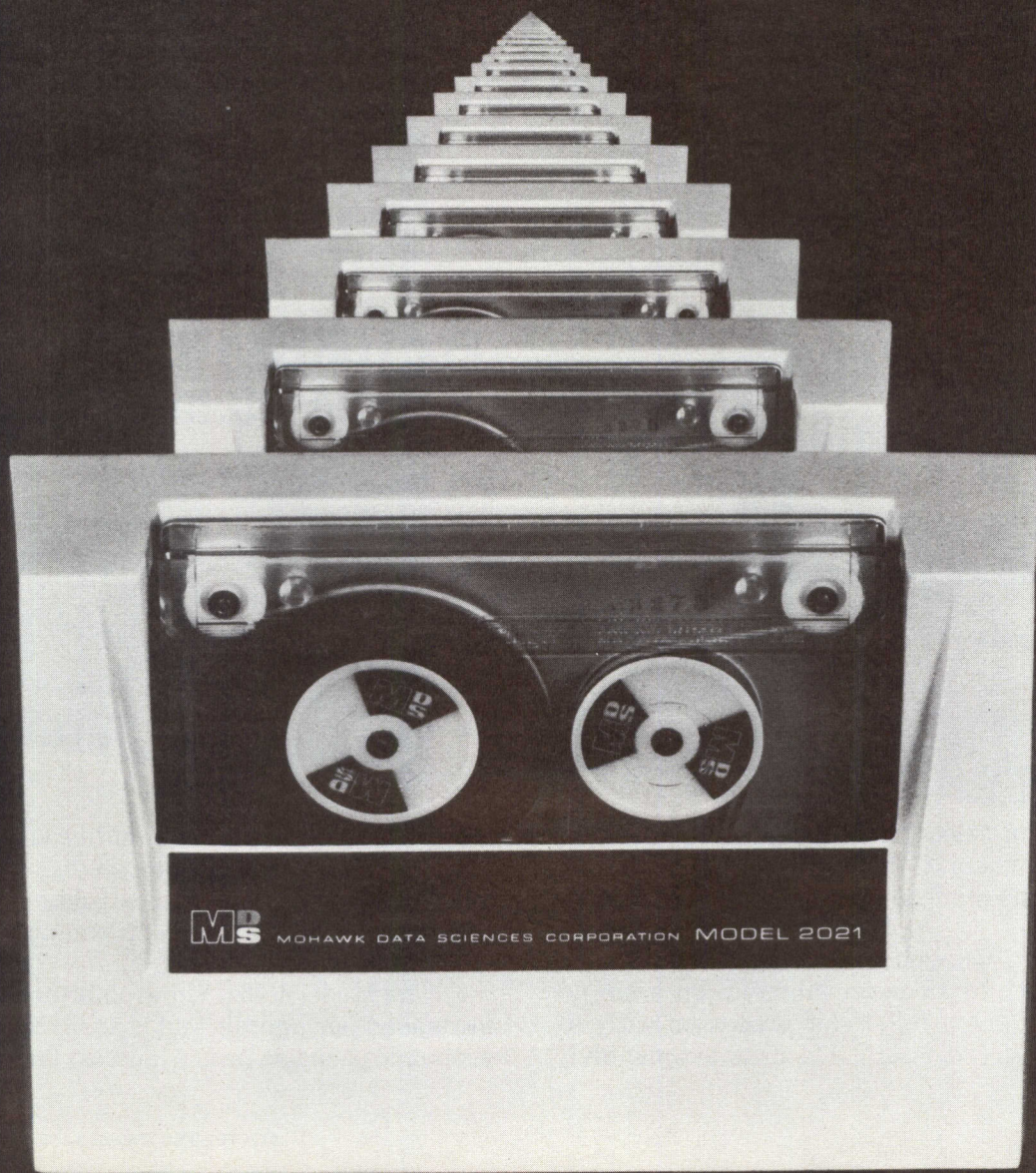
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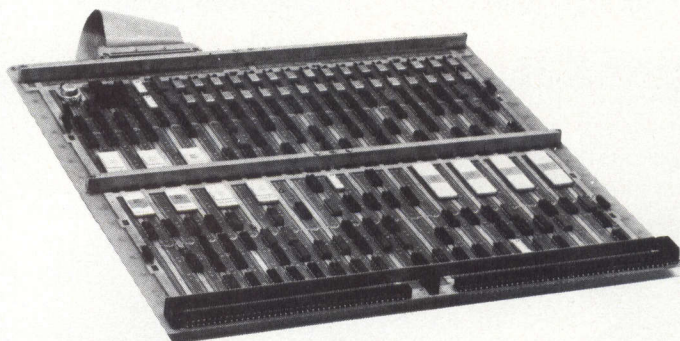
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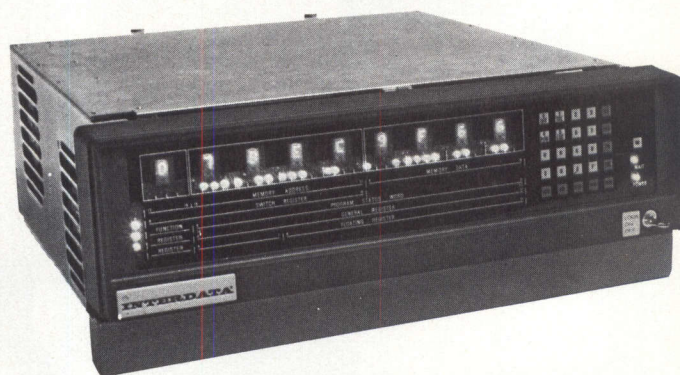
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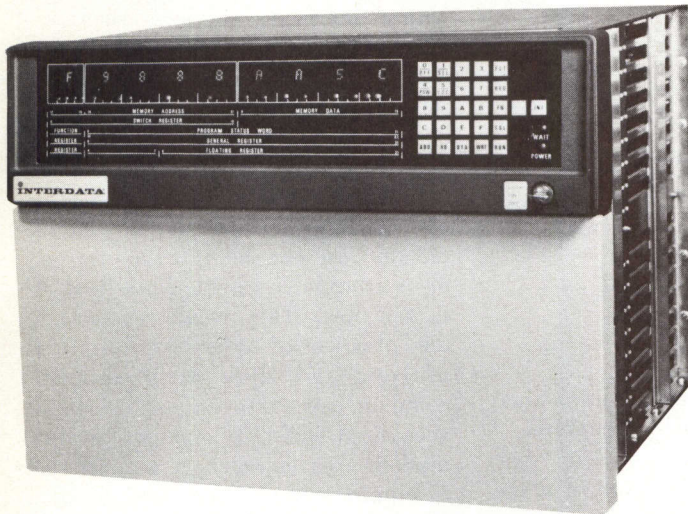


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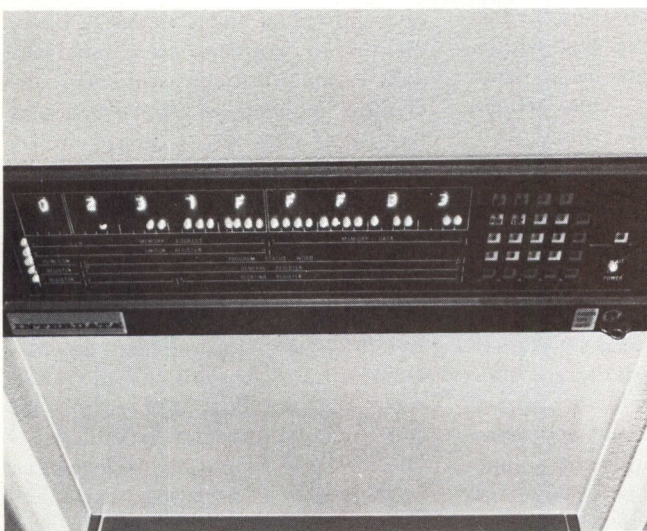


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by **John E. Buckley**  
Telecommunications Management Corp  
Cornwells Heights, Pa.

## Implications of the Communications Reform Act

All of the various decisions of the Federal Communications Commission (FCC), including the historic Carterfone Decision of 1968, have been based on the Communications Act of 1934. These decisions which have permitted the existence of competition in the telecommunications industry are now threatened with reversal if pending legislation is passed by the United States Congress. It would eliminate the ability of data communications system users to purchase and install their own modems, multiplexers, and other network components. Availability of competitive communications facilities and services from specialized common carriers, such as Datran, Teletnet, and MCI, would be nonexistent. Economic and operational flexibility and effectiveness which have stimulated the growth of today's information systems would be dramatically curtailed.

This specter of a return to a monopoly with a sole vendor of communications equipment and services is not an alarmist illusion but a stark reality. The vehicle by which this return to the past will be effected is a replacement for the Communications Act of 1934, recently introduced in Congress under the title of Consumer Communications Reform Act of 1976 (S3192). This law is intended to legally prohibit all competition to the American Telephone and Telegraph Co (AT&T). The FCC recently ruled that AT&T must maintain a separate accounting of the 100 million dollars it is spending on lobbying and

promotional activities to have this bill promptly passed by Congress.

AT&T's basis for supporting this act is that present and future competition will cause home rates to increase by 75% if business users of telephone and data communications systems obtain their systems from AT&T competitors. This unsubstantiated prediction is based on AT&T's alleged policy of overcharging business users to subsidize residential telephone equipment and service. With respect to this question of subsidization, the only public documentation is a recent study by the New York Public Service Commission. Indicating that business communications equipment charges imposed by the New York Telephone Co (an AT&T operating company) were deficient by 61% in compensating for the actual cost of providing that equipment, this report establishes that home telephone rates were actually subsidizing business communications rates, and not the reverse as contended by AT&T. This is significant since 30% of all U.S. communications terminal equipment is located in New York State.

Many federal legislators apparently are being influenced by connotations of the legislation's title. Naturally we are all for consumer reform, particularly since the term implies that some significant abuses previously have been perpetrated at the expense of the defenseless consumer. Upon examination of this proposed act's provisions, the object of the implied protection does not appear to be the consumer but

rather the traditional monopoly. An analysis of the major provisions clearly illustrates this objective.

Section 2 states that an integrated system of common carrier telecommunications services has resulted in reasonable charges and uniform or universal services. This section therefore prohibits authorization of competing interstate services, such as provided by MCI, Datran, and Teletnet, and requires that all interstate services and transmission facilities be of the same types and be provided at the same rates.

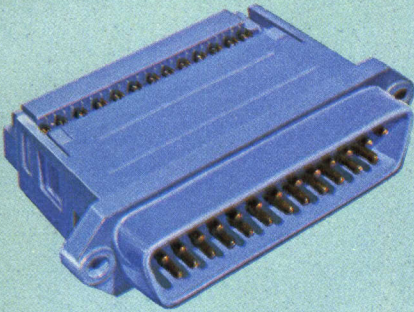
Section 3 provides that no charge that equals or exceeds its incremental cost can be ruled as unjust or unreasonable on the basis that it is too low. This would encourage the practice of cross subsidization of costs and allow the traditional common carrier to underprice on a subsidized basis any communications market area in such a manner as to eliminate competitive activities.

Sections 4 and 5 exempt AT&T from antitrust laws and approve acquisition of existing specialized common carriers. It is interesting to consider that the Justice Department is currently in litigation against AT&T in Federal District Court for violation of present antitrust laws. Sections 3, 4, and 5 of this bill would grant AT&T congressional sanction to underprice any competition and then to buy out its competitors.

Ironically, Sections 6 and 7 are entitled "Reaffirmation of State Jurisdiction over Local Terminal and Station Equipment." These provisions give individual states exclusive jurisdiction to regulate telephone and data communications equipment, including modems, multiplexers, and terminals, plus any customer-owned equipment even though it may be used for interstate communications. The FCC has decreed that states are not allowed to prohibit the use of customer-owned equipment. This decision, based on the Communications Act of 1934, was upheld by the U.S. Court of Appeals. Based on the same act, the FCC also ruled that states cannot preempt federal regulation of interstate usage of telephone facilities by restricting customer-owned equipment. This ruling was upheld by the Fourth Circuit Court of Appeals as recently as April 1976. Other court decisions also have continually ruled in favor of total fed-

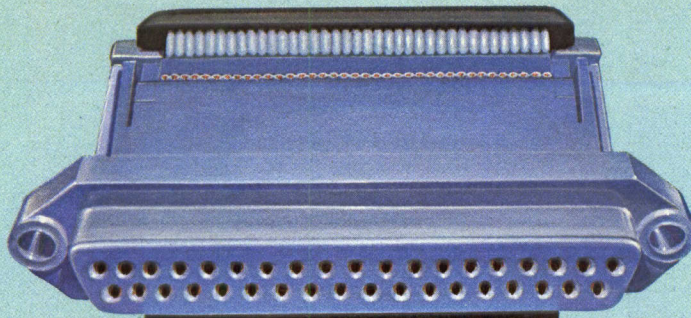


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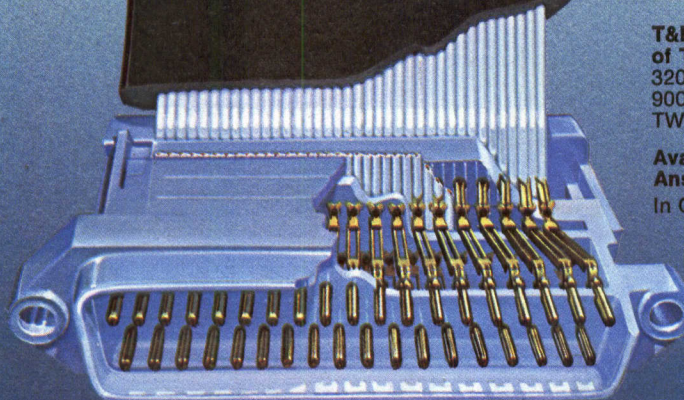
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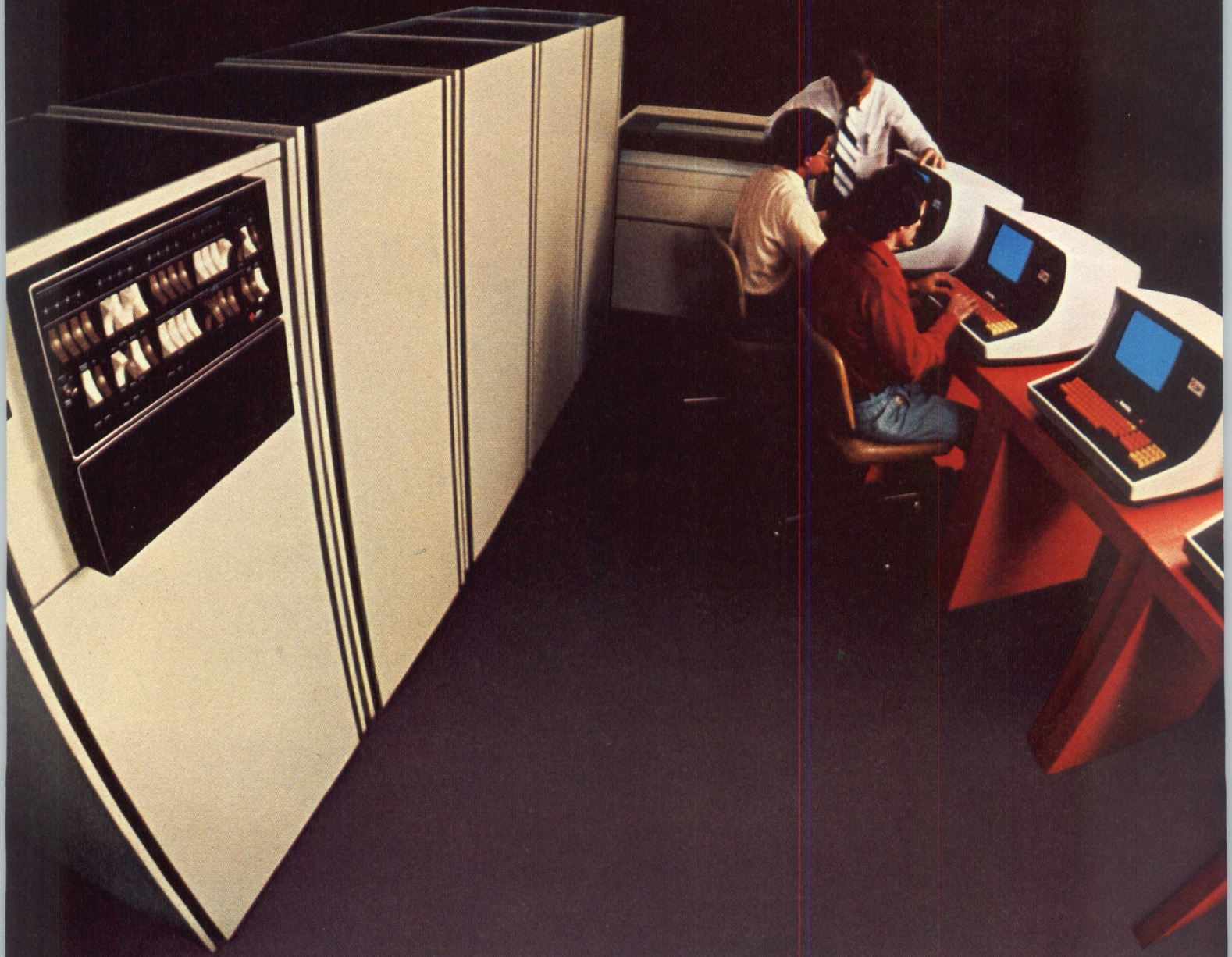
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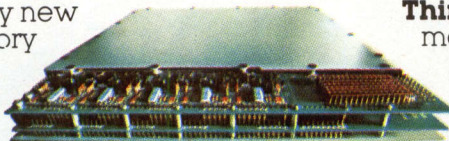
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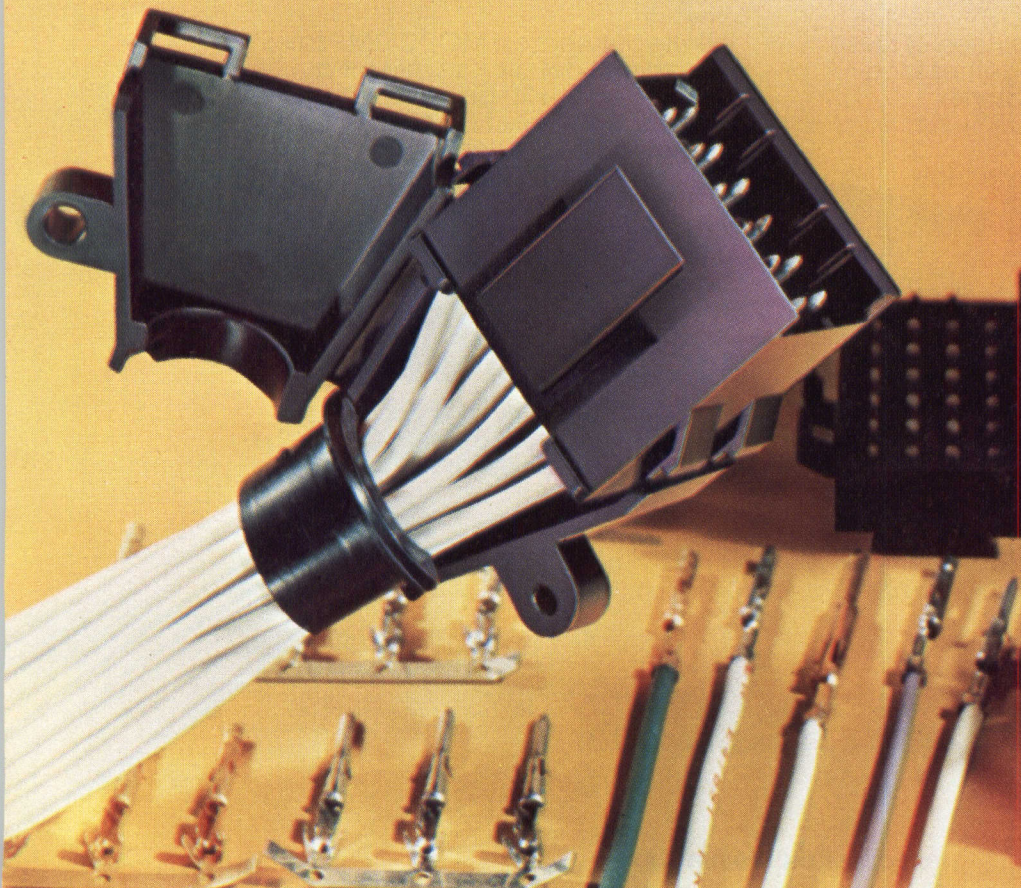
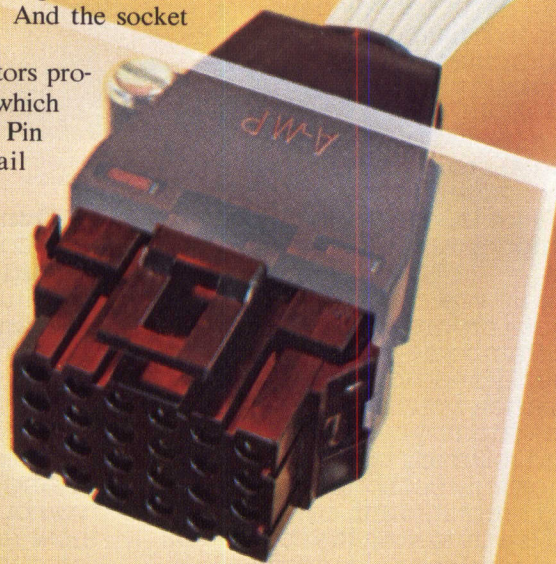
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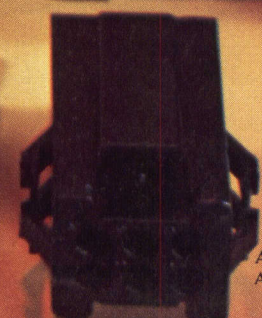
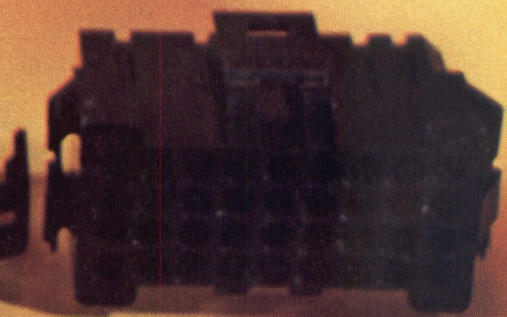
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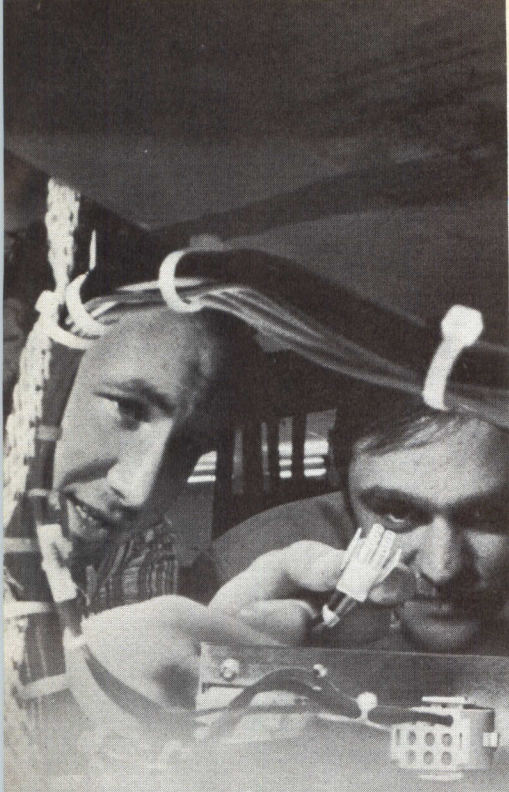
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eral jurisdiction over communications services and facilities which encompass more than one state. "Reaffirmation," a term which appears a number of times in the proposed legislation, actually conflicts with these numerous decisions.

Authored by AT&T and introduced in the U.S. Senate by Senator Vance Hartke (D-Ind), the legislation would provide AT&T with a telecommunications monopoly, therefore exclusively assigning future development of telecommunications technology and products to the jurisdiction of that monopoly. There can be little debate that competitive factors in the telecommunications industry have resulted in rapid growth, development, and innovation of information system applications since the 1968 Carterfone Decision. Returning to a single supplier who is virtually devoid of motivation to respond to market requirements would be a catastrophe. On May 25, 1976, in a letter to Congressman Lionel Van Deerlin (D-Calif), Chairman of the House Subcommittee on Communications, FCC Chairman Richard Wiley stated that this legislation ". . . will impede the development of the flexibility and options a national communications network can offer the American consumer."

In the past, the "Communication Channel" has been used primarily to present and discuss technology and application concepts, systems, and services relating to data communications. This month's column may appear to be a change from tradition and a blatant step into a political arena; however, in the same context as reviewing and analyzing a proposed tariff or service, a piece of proposed legislation which would control all future tariffs and communications services is being examined.

This legislation is AT&T's latest attempt to obtain approval of a monopoly. Within regulatory and judicial communities AT&T has challenged the implementation of the Carterfone Decision. In nearly all decisions rendered by judicial bodies, the FCC rulings have been upheld and the principle of introducing competition has been clearly reinforced. Certain states have attempted to prohibit use of customer-owned communications equipment (eg, North Carolina, 1974) only to have

the courts reaffirm the primary jurisdiction of the FCC in matters of both customer-owned equipment and systems.

Assigning the legislation a title as supportable as apple pie and introducing it in Congress in an election year have significantly enhanced its chances of passage. These facts, coupled with such subtle provisions that only those experienced in the environment's interaction can project its ultimate intention and conclusion, virtually assure its enactment. Unless different views and opinions are made known to Congress, those organizations which can finance appropriate lobbying efforts can realize the passage of special interest legislation. It is interesting to note that Ralph Nader who tends to be synonomous with consumer interests issued a strong appeal to Congress on June 29, 1976 to defeat this proposed legislation. On July 1, 1976, a poll taken of U.S. Congressional Representatives and Senators who have endorsed the Consumer Communications Reform Act of 1976 numbered 147 representatives and 13 senators.

Congressman Van Deerlin has indicated an intention to begin exploratory hearings by the end of September 1976. Senator Hartke, Chairman of the Senate Subcommittee on Communications, does not plan to begin hearings until the next session of Congress, scheduled for January 20, 1977. Senator Hartke is presently campaigning for reelection in November 1976.

Readers who wish to obtain more information concerning this situation can refer to the June 12, 1976 issue of the *National Journal*, pp 816-820. Additional material can be obtained from CBEMA (Computer Business Equipment Manufacturers Association) and NATA (North American Telephone Association), both located in Washington, DC. The outcome of this legislation will profoundly influence the future of the telecommunications industry, as well as those dependent on that industry for present and future information systems. It is critical that all segments become knowledgeable of this proposed act and exercise their privileges to influence its ultimate disposition. □

Opinions or statements in this column are those of the author and do not necessarily reflect the position of *Computer Design*.



## Bulk Storage Tape Unit Offers High Performance In Severe Environments

An environmentally sealed magnetic tape unit, the Bulk Data Storage Unit stores 16.8M bytes using standard block recording, or twice that with high density techniques. Basic unit consists of compact transport module and removable sealed tape modules. A dual transport configuration, packaged as a standalone module unit, contains I/O signal adapter, controller, two independent transports, and two tape modules.

The removable tape module contains 300' of  $\frac{1}{4}$ " wide-temperature magnetic tape, the 4-track read/write head, and coaxial reels with capstan drive, tape guides, and tape position sensor. An electro-optical tape position sensor detects tape ends and center; an electrochemical elapsed time indicator provides a running time record. Transport assembly houses drive motor and electronics and accepts the fully interchangeable plug-in tape module.

Developed by Electronic Memories & Magnetics Corp, Severe Environment Products Div, 20630 Plummer St, Chatsworth, CA 91311, the unit can be installed directly into or on the host system, is ATR-case compatible, and has an all digital signal interface. Subsystem modularity eliminates additional enclosures, power supplies, interface circuits and interconnect cables, and other significant added-on costs.

Available in single, dual, and custom transport configurations, the tape drive has bidirectional read/write capability at a preset speed of up to 30 in./s. Search/rewind at 120 in./s provides worst-case access of 15 s from center to either end of tape. Bit density is up to 1600 bits/in. in parallel operation, providing 23M bits of parallel storage or up to 2400 bits/in., single track, for 34.5M bits in bit-serial applications.

The signal adapter in the dual configuration provides the processor functions required to interface the unit's controller with a MIL-STD-

1553A multiplex I/O channel; the controller accepts signals from the I/O signal adapter as well as an EIA standard RS-232-C asynchronous channel, generates transport command signals, and performs Manchester data encoding and decoding.

Evaluation units will be available beginning in December on a 5-month ARO schedule. Production models will be available in mid-1977. The units are specified with a  $-54$  to  $95^{\circ}\text{C}$  operating temperature range per MIL-E-5400, Class 2. Operating power is less than 30 W and standby power is 5 W.

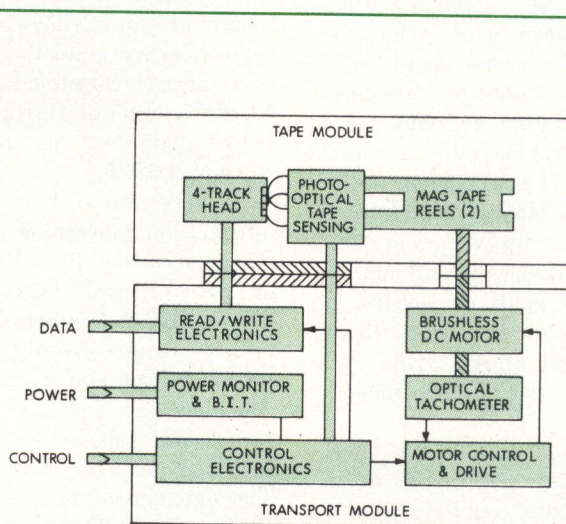
Circle 140 on Inquiry Card

## Display Terminals Prove Compatibility with SNA Communications Methods

Expandable and compatible with SNA teleprocessing methods, 8170 series systems are intelligent, clustered, interactive display terminals designed to provide effective data entry and retrieval in an IBM 3270 compatible environment. Built around a processor programmed to emulate the 3270, the series was designed by Sanders Associates, Inc, Daniel Webster Hwy, S, Nashua, NH 03060 to provide both local and remote capabilities. Programming allows such enhancements as local printing without mainframe intervention, self-test diagnostics, local format storage, local editing and arithmetic, and local data storage for backup.

Expected to become the predominant communications architecture within the next year, Systems Network Architecture (SNA) communications structure incorporates Synchronous Data Link Control (SDLC). It was designed by IBM to achieve uniformity and increase efficiency in the teleprocessing networks. Using SNA and SDLC instead of current communications techniques, it is practical to send at least ten times as much data in a transmission with the same amount of handshaking, greatly increasing communications efficiency.

To optimize system performance in the SNA environment, a complex trade-off has been made to determine which SNA protocols to build into



High performance in severe environments is attained with the Bulk Storage Tape Unit from Electronic Memories & Magnetics. Consisting of transport module (1.4 x 4 x 6") and removable sealed tape module (1 x 4 x 6"), the unit records 16.8M bytes on 300' of  $\frac{1}{4}$ " magnetic tape. Tape module incorporates 4-track read/write head, coaxial reels, and tape position sensor



# We made them first. To last.

Available now from Singer: Size 8 and 11 Bu/weps synchros designed to meet the latest requirements of MIL-S-20708C specifications.



Kearfott, the first to design Bu/weps size 5, 8 and 11 synchros, has over the years constantly made them better. These units are used in fire control systems, radar, navigation, missile functions and other applications requiring a high level of precision, endurance and reliability.

These Kearfott synchros operate over the entire temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . They are DOD qualified and listed in the QPL.

(They can also meet reasonable cost requirements in computers, electronics and other types of business equipment.)

You can get these synchros in the following Bu/weps types:

Size 8	Size 11
26V 08CX4c	26V 11CX4c
26V 08CDX4c	11CX4e
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	26V 11CDX4c
	11CDX4b
	26V 11CT4d
	11CT4E

We'll be happy to send you drawings and technical details on request. Also for Kearfott Size 5 Bu/weps CX, CDX and CT units, and Size 11 and 15 resolvers. Units with the same characteristics but different Bu/weps shaft variations are also available. Write for information to the Singer Company, Kearfott Division, 1150 McBride Avenue, Little Falls, N.J. 07424.

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terminal hardware (hardwire) and which to program into the terminal using software. The decision was made to hardwire in the SDLC portion and to provide the remaining protocols with programming.

Basic system consists of a programmable 12K-byte terminal processor, CRT displays with 480, 960, or 1920 characters, and a choice of three styles of detachable keyboards. Basic processor supports eight displays and eight printers. With added device adapters, 32 terminals and 32 printers all connected by coaxial cable can be supported. The processor operates at 600 to 4800 bits/s, with multipoint binary synchronous, EBCDIC, RS-232-C, and CCITT line disciplines.

Hardware programmability allows special functions to be added to the system program. Built-in redundancy permits controllers/adapters to be independently serviced when the system has clusters with more than eight terminals. Built-in test and line monitoring features permit rapid fault isolation and system servicing.

Local format storage reduces line charges and increases operator productivity. By holding display formats at the terminal controller instead of the host processor, the burden of repeatedly transmitting formats is eliminated, making it possible to multidrop more operator stations on a single line or use a lower transmission speed to get the same throughput. The resulting improvement in system response times improves effective keystroke rates, increasing productivity. Media for local format storage include buffer memory, diskette, or disc for requirements of 10K, 500K, or 5M bytes, respectively.

Queued transaction handling allows data entry to a mass storage device at the terminal controller without host intervention. This prevents a backlog of unentered data from accumulating during an outage, by allowing data entry to proceed continuously, whether or not the terminal system is online to the host. It can also be used to reduce line traffic during peak activity periods in a mixed application environment. The function is supported by a minimum of one and a maximum of two 500K-byte capacity dual diskette drives or 5M-byte disc drives for each group of eight displays. Three modes of operation are provided: normal,

offline data entry, and online recovery.

The programmable 8170 terminals can be installed in existing computer networks and later upgraded with the SNA communications option with only minor modifications. First production deliveries are scheduled for January 1977. Purchase price of the SNA option for an average size cluster is \$1000.

Circle 141 on Inquiry Card

### 2K-Byte Cache Buffer Increases PDP-11/45 Processing Speed

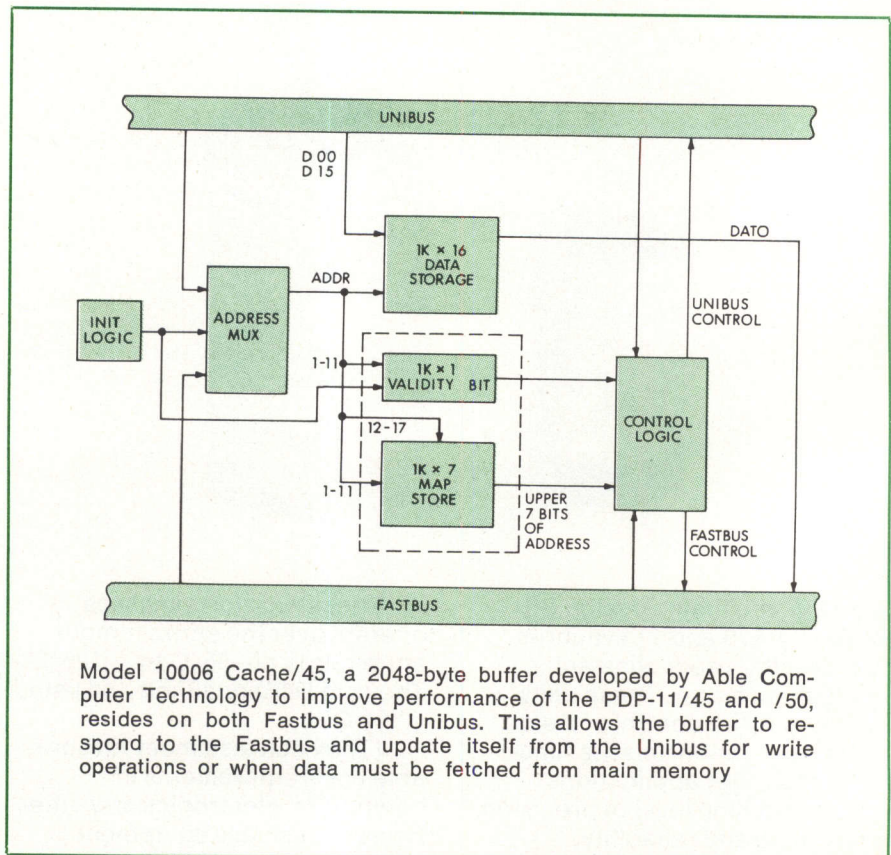
A 2048-byte cache buffer on a single PC board, the Cache/45™ can increase processing speed of the PDP-11/45 from 30 to 100%, enabling users to realize maximum computer capability without MOS or bipolar memory on the computer's Fastbus™. The 2048-byte buffer (using Schottky bipolar RAMs with 300-ns cycle time) is twice the size of others on

the market, and is expected to provide a 95% hit ratio in most applications.

Buffer control is maintained over every core memory address location on the Unibus™. This provides the user with up to 124K words of memory that run at Fastbus speed, instead of the 32K words available if the Fastbus MOS or bipolar memory option is obtained from the computer manufacturer. However, the cache is also totally compatible with up to 4K words of bipolar or 16K words of MOS memory if they are installed on the Fastbus.

Most software consists of many repetitive loops or subroutines. The Cache/45 concept is designed with this fact in mind. Able Computer Technology, 1538-E E Chestnut St, Santa Ana, CA 92705 based the buffer design on a write-through algorithm. For all computer DATI operations (read from memory), the 1K block address and corresponding data are mapped into the buffer. On successive processor DATI operations (reads) from an address that has been mapped, data will be supplied on the Fastbus of the PDP-11/45 by the buffer.

All processor DATO operations (write to memory) take place on the Unibus for any address selected in core memory. The cache will automatical-





# Graphic hardcopy output from IBM systems: the Plotmaster<sup>®</sup> makes it a reality, not a dream.

If you have an IBM System 360/370 computer operating under DOS, OS or VS, you know what a nightmare it is to get graphic hardcopy output.

That's why the Gould Plotmaster Systems are like a dream come true. They deliver crisp, high quality graphics output from the computer, with no intermediate processing steps. They also work at incomparably fast speeds, without demanding additional system resources. No hours or days of waiting as when you use a slow pen plotter attached to the computer. No waiting for post-processing film development and blow-up as when you use graphic microfilm units.

Plus, Plotmaster Systems are economical as well as efficient. Initial and recurring costs are surprisingly low. And fast turn-around and high capacity adds up to additional savings.

Plotmaster Systems have three major components. Efficient and flexible graphics software. A Gould electrostatic printer/plotter that you can tailor to your exact application. And hardware to link the two—an on-line controller, or a tape drive for off-line operation.

In addition to this basic package, specialized software is available for business, scientific and engineering applications. Full printing capability is optional.

Let us tell you more about the

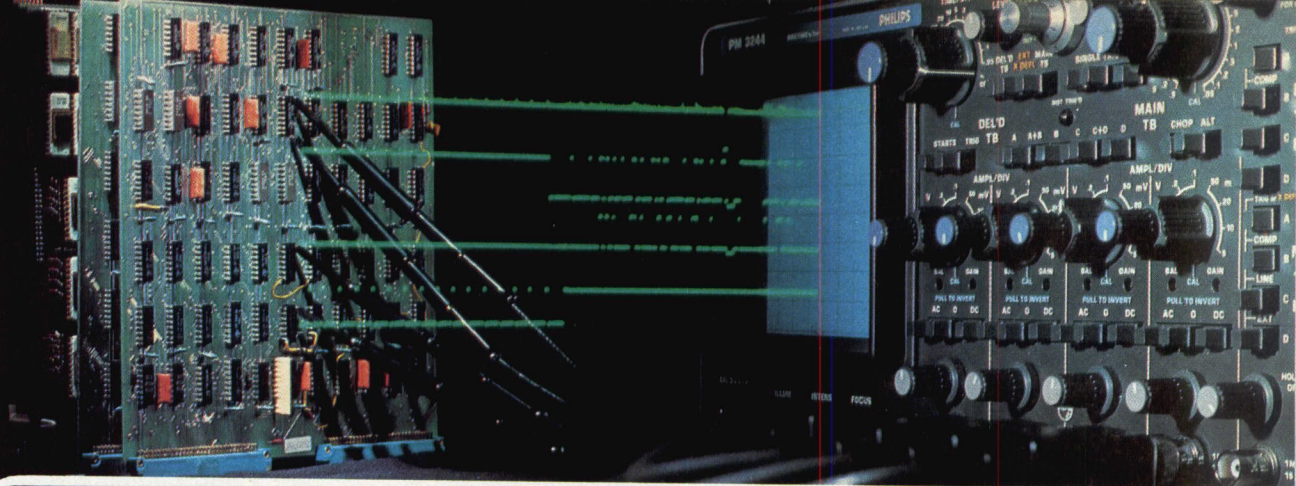
fast, powerful, versatile Plotmaster Systems. They can be purchased or leased and are supported by Gould's specially trained service force.

For a free brochure, write Gould Inc., Instrument Systems Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Or Gould Advance Ltd., Raynham Road, Bishop Stortford, Herts, United Kingdom. Or call Gould toll-free at (800) 325-6400, Ext. 77. In Missouri: (800) 342-6600.

 **GOULD**  
The product development company

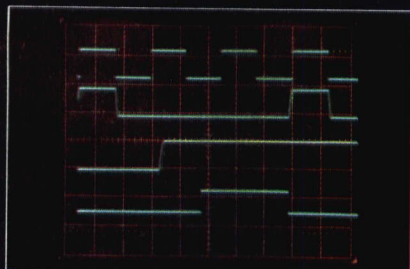




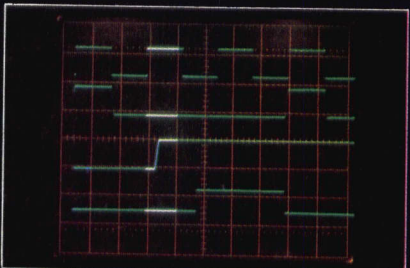


**Four 50 MHz channels. Unique triggering facilities.  
Ideal for parallel data analysis.**

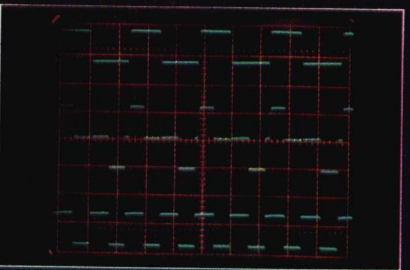
# Zero in on



*As illustrated on the front panel detail, triggering is fully independent and multi-sourced. This gives a number of unique triggering possibilities and is just as useful for more conventional dual-trace measurements.*



*Here the main and delayed timebases are triggered from different channels, one example of the PM 3244's unique triggering facilities. Signals can therefore be shown even when they are not related to the main timebase.*



*Differential measurements can be made on the PM 3244 in the conventional manner or by using the composite triggering mode.*

Four traces give you the logic story: show the relationships at a glance. But only the PM 3244 gives you four traces and fully independent triggering of main and delayed timebases. Thus the main timebase can be triggered on any of the four channels plus composite, external and line. The delayed timebase can be triggered on any of the four channels plus composite: independently! This gives a number of unique triggering possibilities, for example showing relationships that are not directly related to the main timebase, like the information in a data line when the main timebase is triggered on an address line.

## **Doubles for dual-trace with extra performance.**

PM 3244 is the world's first four-channel compact and all channels have full display facilities i.e. sensitivity, attenuation, invert, etc. It can therefore be used to make isolated or differential measurements and when you need conventional dual-trace displays, this scope also gives them, with two traces in reserve plus unmatched triggering facilities.

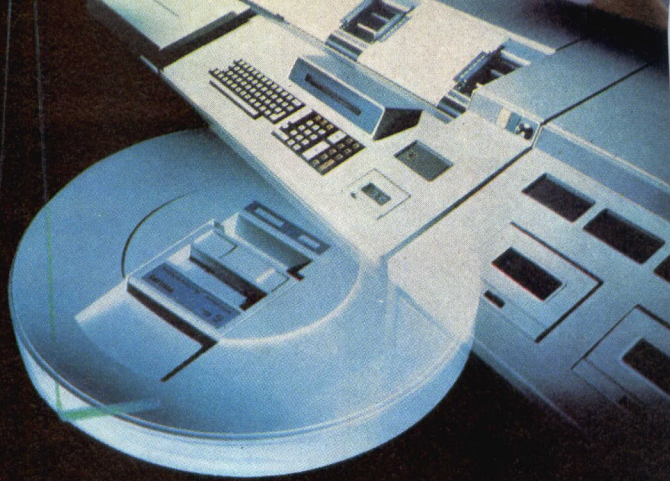
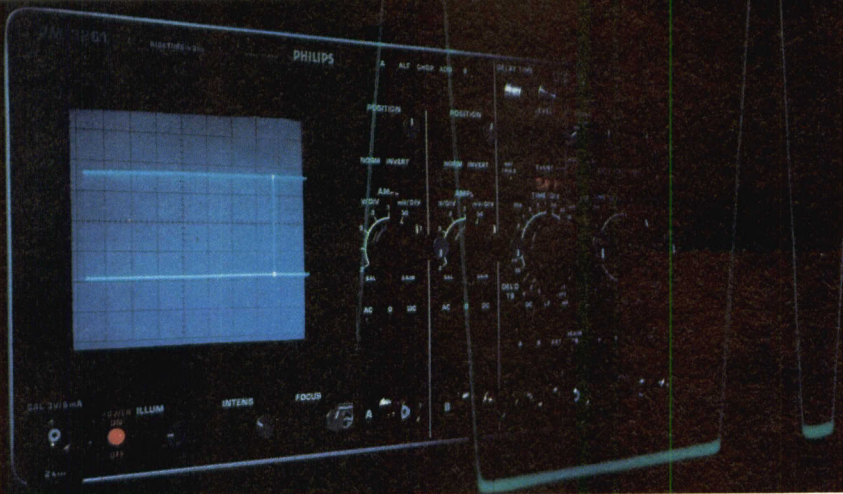
All displays are on a large 8 x 10 cm screen and the compact construction weighs in at a mere 9.6 kg (21 lb). The price is rather compact too!

Write for more details. Read opposite about another data breakthrough.



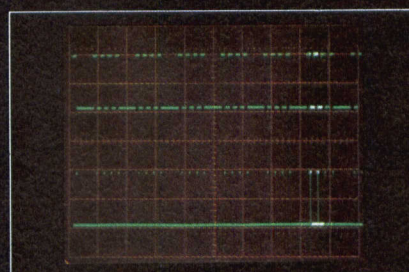
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120 MHz with digitally delayed triggering to over 200 MHz.  
Ideal for serial data.

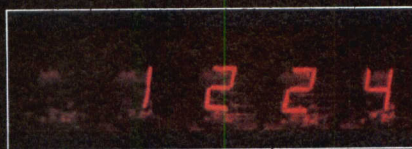
# ones and zeros



As illustrated on the front panel detail, one push button and one control knob are all that's needed to operate the digital delay. The required event in the data stream 'lights up', as shown, and can then be displayed using the normal delayed timebase in order to make accurate time interval measurements.



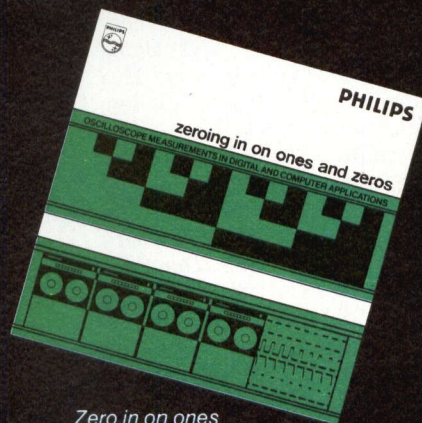
The PM 3261 is another world first. In addition to conventional triggering facilities, the instrument features a digitally delayed timebase that can be set to trigger on a particular pulse in a data stream, the position being displayed on the built-in, five-digit LED. This facility allows individual events to be located quickly and accurately in data streams of up to 100,000 bits and then be 'trapped' for detailed display.



The event is located using the illustrated delay counter, which can be set to count up or down at an adjustable speed as low as one step every two seconds. Specific sections can thus be examined and the counting stopped and stepped back to pick up and locate any irregularities.

The digitally delayed counter also overcomes problems of jitter, such as occur in mechanical systems like disk memories, tape drives, etc. In such cases, if the jitter is longer than one period, a conventional delayed timebase cannot be effectively employed. Once that display has been trapped, accurate time interval measurements can be made using the normal delayed timebase controls.

In addition, the main timebase has a TTL triggering facility to eliminate triggering problems on preshoot, overshoot, ringing, etc.



Zero in on ones and zeros with the aid of this useful 64-page booklet. For further information simply circle the reader service number.

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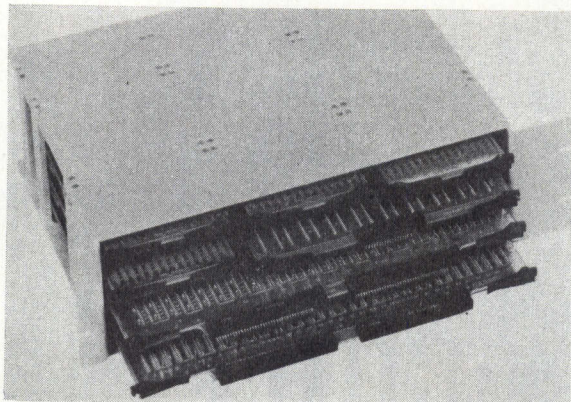
ly update itself simultaneously with core if the selected address is mapped in the buffer. This operation assures that data in the buffer will always be identical with those in core.

Installed by simply plugging the hex-wide electronics board into the computer chassis, the cache is totally compatible with Unibus and Fastbus, and requires no system software changes. A switch on the board permits a choice of on or offline operation. A 5-Vdc power supply is electrically and mechanically compatible with power cabling and mounting facilities in the 11/45 and 11/50.

Circle 142 on Inquiry Card

### Packaging System Concept Permits Panel Sizes To Be Mixed in Rack

When an electronic system design engineer sits down to package his logic system he faces a number of compromises or design trade-offs. When his system diagram is divided into functional modules or building blocks the differing requirements of each function, such as IC devices, signal lines necessary for interconnection, and individual I/O signal requirements, become apparent. If a board containing 30 ICs is chosen, the designer must divide large functions into multiple boards, and lose identity of the total function, as well as run the risk of longer lines on critical signals. If a 200-IC board size is chosen, multiple functions must be put together on one board, increasing troubleshooting technical skill requirements, and resulting in greater replacement or spare board costs.



Permitting the logic design engineer to split his logic into multiple size functions, Mupac's packaging system concept allows a variety of wirewrap panel sizes and IC densities to be mixed in the same rack assembly. High I/O ratios on the panels are provided by multiple 2-piece wirewrap-to-wirewrap connectors. The small panel contains 32 ICs and has 108 I/O pins, the largest 192 ICs and 540 I/O pins

Many of the boards will have to contain multiple voltage supply distribution planes, because of the needs of microprocessors and other new devices. The possibility of design changes due to more advanced technology and IC complexity also must be considered, since these changes will again affect board size, modularity, and I/O requirements.

Addressing these problems, Mupac Corp, 646 Summer St, Brockton, MA 02402 has developed a packaging system which permits a variety of wirewrap panel sizes and IC densities to be mixed in the same rack assembly. Panels containing from 32 to 192 ICs and ranging in size from 4.5 x 6" to 14.9 x 8.0" may be inserted and intermixed in multiple and varied combinations within the same rack assembly. The concept permits the packaging or design engineer the flexibility of subdividing his logic into multiple size functions, thus keeping on one board those functions he does not wish to be split electrically or mechanically. Multiples of a 2-piece wirewrap-to-wirewrap connector containing 108 I/O pins permit interchangeability, as well as afford high I/O ratios on each panel. The smallest panel contains 32 ICs and has 108 I/O pins (a ratio greater than 3:1). This ratio is well maintained up to the largest panel, which contains 192 ICs and 540 I/O pins.

Each panel size or family contains a wide variety of IC socket layout options, as well as multiple voltage supply planes. Some panels contain as many as four voltage planes (V1, V2, V3, and gnd). Panels plug into three independent backplanes, each of which may contain as many as three voltage distribution planes. This flexible backplane

system permits the designer the use of multiple supply requirements where needed.

Also part of the system concept is a data signal bus backplane which handles the parallel signal requirements of memories or parallel data bus systems. Since the data signal bus backplane contains wirewrap pins, as well as hardwired connectors, the data bus signals may be altered and/or expanded for added system requirements.

Circle 143 on Inquiry Card

### Word Processor Adds Communications/Cassette Storage for Power

Communications capabilities, expanded storage, and typing output of 46 words/min. added to the Videotype<sup>®</sup> text processor enable users to store up to 125 pages of 8000 characters each, and to transfer seven pages a minute to another similar system. According to Lexitron Corp, 9600 De Soto Ave, Chatsworth, CA 91311, the added features significantly enhance the cost-effectiveness of the office typing system.

Interact communications device, by literally turning a central computer into a quick reference file, makes it easy to retrieve information for update, modification, or printout. This, coupled with the ability to transfer volumes of data at a high rate, provides increased operational power and a significant reduction in telephone line charges. The open-ended feature not only allows communication between text processors, via modem or telephone lines, but also enables users to access a data processing system for remote job entry and other terminal-initiated functions, combining elements of both word processing and data processing disciplines. Interact consists of a programmed communications microprocessor that can be added to any of the company's text processors.

Tape II, a 2-reel, 4-track magnetic tape cassette, has 508 sq in. of useable magnetic surface compared to only 38 sq in. for a standard floppy disc. Its capacity is 125 pages (8000 characters each)—four times more data than a floppy disc. Magnetic tape is used for primary storage instead of floppy discs because it is felt to provide more efficient retrieval.

Word processing, instead of emphasizing character or bit manipulation, involves operating in context,



# Now, Intel delivers memory for PDP-11/04 and PDP-11/34.

Intel is now shipping high speed, low cost memory for two of the hottest new minicomputers, DEC's PDP-11/04 and PDP-11/34.

That means you can get 30-day delivery and 30 to 50% savings by specifying Intel, the largest independent manufacturer of semiconductor memory.

We can give you add-in memory and add-on memory, both totally compatible with PDP-11 hardware and software. Our in-4711 is an add-in memory for the PDP-11 family and slides into an available memory slot, without modifications. For add-on memory capacity, simply attach the in-4011 memory system. You can add memory in 16K x 16 bit increments, up to 128K words.

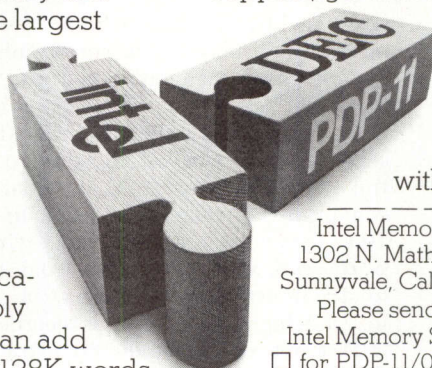
Built with the proven Intel 2107B 4K RAM, the in-4711 memory is fully transparent to the CPU, with greater processing speed. For maximum throughput you can interleave two memories.

The in-4711's lower power consumption permits wider operating margins on the main

frame power supply and results in a cooler running, more reliable system.

If you've picked DEC to be your computer supplier, go with the best for memory, too. Intel delivers a complete line of add-in and add-on memory for the entire PDP-11 family.

That puts two good names together. Add a third — yours — with the coupon.



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retrieving a document and moving from page to page. Serial text storage allows the operator to immediately identify the location of stored data for retrieval. It is claimed to provide the least expensive cost per page of storage as well as the fastest access time for retrieval of a specific item. Transfer rate is 580 kilobits/s (or six full 8000-char pages)—twice that of a floppy disc.

System consists of a standard desktop typewriter keyboard with control keys to accommodate system functions. The page-sized CRT screen displays what is being typed, and allows the operator to clearly see delete, insert, erase, merge, and edit functions without retyping. The video display provides an illuminated page outline exactly replicating the borders of the page to be fed into the system's printer; automatic pagination; and indexing. A typewriter-style platen control is used to scroll the display up and down.

Finished text is stored on magnetic tape. Hardcopy is generated exactly as the page was last displayed; while printing occurs the operator may key in the next page of data. In addition to magnetic tape, the system has in essence three different types of memories: display buffer—which contains text being displayed; pagination buffer—which has copy flowing in and out during revision; and printer memory—which holds text called out for printing.

Circle 144 on Inquiry Card

### **Flexible Disc Drives Add Low Cost Mass Storage to Programmable Calculator**

Two flexible disc drives intended to expand the usefulness of the 9825 programmable calculator have been introduced by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304. Coupled with the calculator's interfacing capability, the multiple disc systems' capacity of 468,480 bytes/disc allows users to gather large quantities of data from instruments and store them for later manipulation; and to record, store, and run large complex programs.

Each 9985M master unit, with built-in controller, can manage the operations of up to three 9885S slave units simultaneously. The calculator

can direct up to eight master units, for a total of 32 separate discs with 14,991,360 bytes of user-available memory. Both models transfer at 32K bytes/s using the calculator's direct memory access feature. Double density read/write provides a 304-ms random access time and high storage capacity. Control of the discs is handled by a high level command system which uses a directory to keep track of 320 named files. Both models have a write-verify mode to ensure that information recorded on the disc is identical to source information in calculator memory.

Manufactured by HP's Calculator Products Div in Loveland, Colo, the drives are priced at \$3900 for master and \$2500 for slave. Flexible discs cost \$14. Deliveries will begin in mid-October.

Circle 145 on Inquiry Card

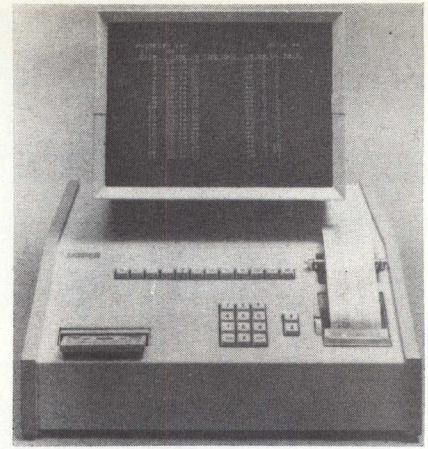
### **Dictation System Displays Unit Status/Location For Efficient Management**

A dictation system that tells the supervisor the nature of all dictated work, the Visualizer provides efficient management and fast user turnaround time. Lanier Business Products, 1700 Chantilly Dr NE, Atlanta, GA 30324 incorporated CRT display and microprocessor into the unit to control and report on individual units of dictation.

Control center is a CRT monitor and keyboard; the monitor automatically displays and stores information about each individual unit of dictation; the keyboard accepts human language commands from the supervisor for efficient dictation control and processing. One monitor can process the dictation from up to 700 telephone or 96 direct-wired word originators. It controls from one to 16 direct-wired recorders, or up to 32 telephone-connected recorders.

Previous systems required extra or dedicated recorders for special dictation; the Visualizer makes every recorder available for both priority and routine dictation for maximum efficiency.

Word originators can choose direct-wired Lanier phones or on/off premise standard telephones. Users have full recorder control, including fast forward and electronic indexing to mark special instructions and ends



Lanier's Visualizer cassette reader instantly identifies recorded cassettes from any system recorder. Cassette number and recorder, day and time of input, author identity, and length of dictation are automatically displayed while the printer makes a paper copy of the screen

of letters. The monitor receives and automatically displays a 5-point description of every unit of incoming dictation: cassette/recorder number, day/time of input, author identity, and length of dictation.

The supervisor can request status reports of work in progress, recall from memory a record of all past work up to 1000 cassettes back, instantly compute individual or system totals for dictation input, transcription output, turnaround time, and much more. The keyboard allows individual attention to be given to each individual unit of dictation. Units requiring priority treatment can be located immediately for assignment.

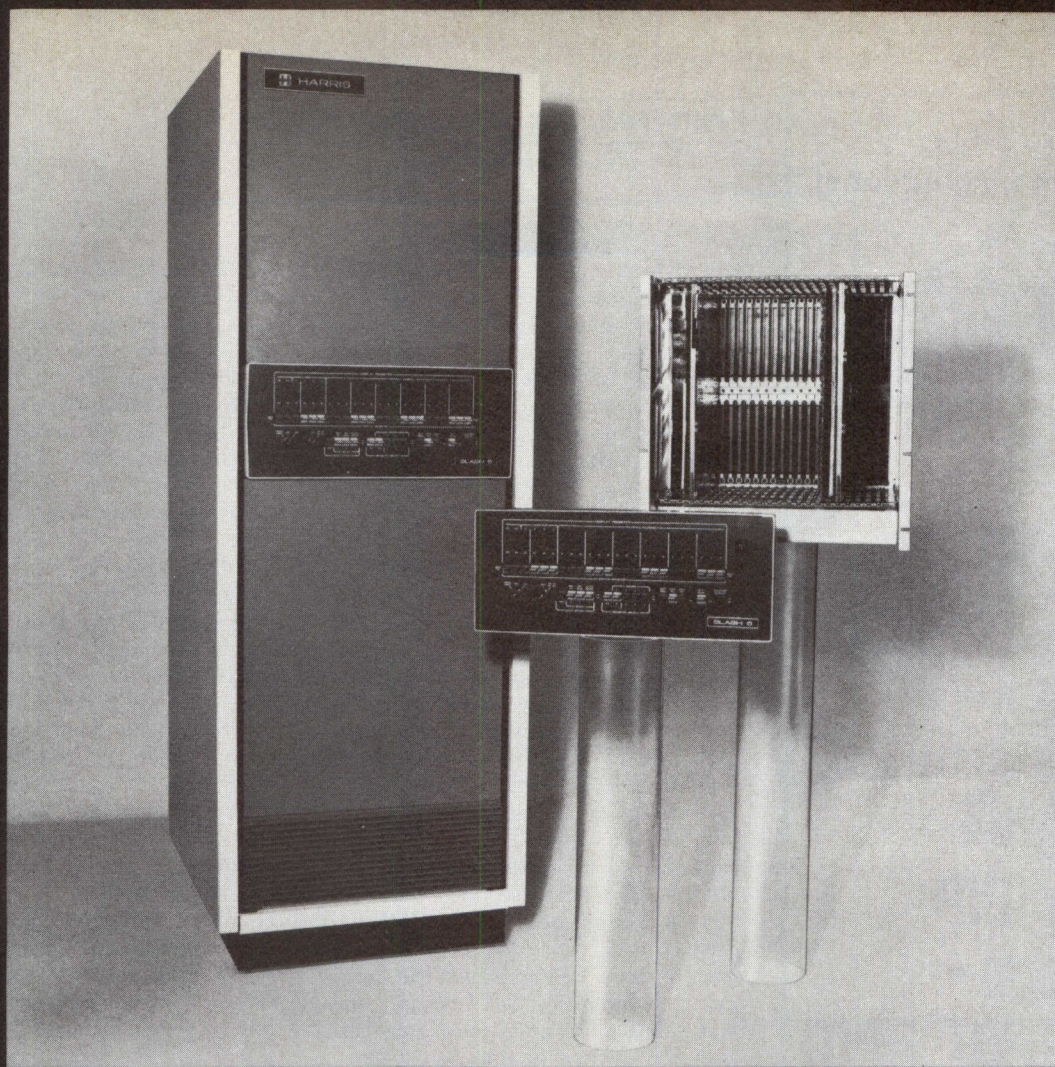
Circle 146 on Inquiry Card

### **System/3 Improvements Allow Batch-Only Users To Add Teleprocessing**

Improvements announced by IBM Corp, General Systems Div, PO Box 2150, Atlanta, GA 30301 for its System/3 line provide a method for current users of batch-only applications to add teleprocessing and for current teleprocessing applications to expand to larger online applications. Disc expansions allow greater file and application expansion capacity for both types of applications.

The changes include a System/3 model D with 160K, 192K, 224K, or 256K bytes of main memory. Compared with other processors in the line, the model D provides a faster instruction fetch time for certain non-





## The Harris Slash 6. Supermini performance. At super minicost.

If you recognize optimum price/performance value when you see it, you should see our new SLASH 6. It outperforms most 32-bit minis, at a price that's better than many 16-bit minis.

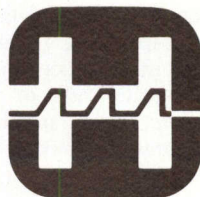
The Harris Slash 6 costs only \$14,500\*. You get 600 nanosecond cycle time; 48KB of MOS memory with error correction; hardware multiply, divide, and square root; 8 priority interrupts; and a turnkey control panel.

You get building-block architecture

that lets you expand your systems as your needs expand. And sophisticated real-time software that no other machines offer in this price/performance range.

The Harris Slash 6. The first truly low-cost/high performance computer for all of you who were waiting for optimum price performance value. Harris Computer Systems, 1200 Gateway Dr., Ft. Lauderdale, FL. 33309. Europe: Techmation N.V., Gebouw 105/106, Schiphol-Oost, The Netherlands.

**HARRIS**



**COMMUNICATIONS AND  
INFORMATION HANDLING**

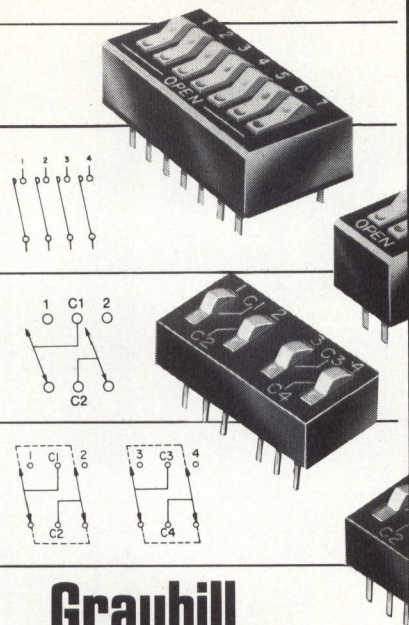
\*Volume discounts available.

CIRCLE 17 ON INQUIRY CARD

29



Now there are 3  
circuitry configurations!



## Grayhill Rocker DIP Switches - SPST, SPDT, DPDT

All with exclusive spring loaded, sliding ball contact system...life rated at 50,000 operations.

- Positive wiping action and immunity to normal shock and vibration
- SPST in 9 sizes, from 2 to 10 rockers; SPDT and DPDT in 1, 2, 3, and 4 rocker versions
- Double throw versions provide simpler, more positive actuation than bridging rockers, satisfy logic '0' and logic '1' input requirements with a single rocker.

Now Grayhill's DOUBLE-DIP™ Rocker DIP Switch (DPDT) joins the DIP-C™ (SPDT) and the plain vanilla SPST, in the industry's most comprehensive line for cost-effective on-board switching. Grayhill's Series 76 Rocker DIP Switches offer the important advantages of IC compatibility, compact high-density design, and ease of mounting by direct wave soldering or insertion into standard DIP sockets. Positive positioning through the exclusive spring-loaded sliding ball contact system provides immunity to shock and vibration and life with 50,000 operations. Detailed specifications and pricing are available from Grayhill, 561 Hillgrove, La Grange, Illinois 60525 or phone (312) 354-1040 for your free Rocker DIP family literature packet.



I/O instructions. In one machine cycle two bytes instead of one are fetched from main memory into the instruction register. Purpose of the faster fetch time is to complement requirements of the programming support.

System control program (SCP) features enhanced file sharing, a third program partition, online library capacity up to 25M bytes, and Communications Control Program (CCP) improvements. These allow definition of four times more active files (192 compared to 40); provide library flexibility through an option that allows the user to catalog programs directly from a batch partition into a CCP library, and permit a user task to be initiated by another task without operator intervention.

Four possible disc configurations offered for the D version permit capacity up to 506M bytes with a 3340 model A2 and 3344 B2. The 3344 is a fixed medium disc with two drives, each approximately equivalent to four 3340s. Thus the maximum configuration has two and one-half times more main data area than that previously available.

Price for the processor will be from \$127,740 to \$143,940. First shipments are scheduled to begin in December.

Circle 147 on Inquiry Card

### Central Computer Distributes Processing Through Small Computers

A high speed central computer that distributes processing of system information through a network of 10 to 20 smaller computers, the CYBER 70, model 71 can handle both batch processing and time-sharing applications and can support a network of up to 500 simultaneous remote terminal users. The smaller computers perform data formatting, address calculations, directory and pointer processing, character comparisons, and conversions. All directly interface to system peripheral equipment through a group of 12 to 24 bidirectional I/O channels. The system was introduced by Control Data Corp, Box O, Minneapolis, MN 55440.

The distributed processing system can include either one or two central processors; each processor features 24 operating registers divided equally among operand, address,

and index functions. Instructions are handled on a register-to-register basis that results in instruction issue rates of 1.2 million/s with a single processor and 2 million/s in a 2-processor configuration. A hardware capability called register exchange jump allows the CPU to quickly save all registers from one job as it moves to another. This speed permits all jobs to keep processing simultaneously in a multiprogramming environment.

System CPU has 65K, 98K, or 131K words of main memory, with a 1- $\mu$ s read/write time for each 60-bit word. The memory is organized in logically independent banks of 4096 words, each overlapped and phased to provide high data transfer rates when relocating memory addresses and in time-sharing environments that require fast movement of data into and out of memory without noticeable conflicts. Data transfer rate up to 10 million words/s can be achieved when block transfers of data occur between main memory and an extended memory unit.

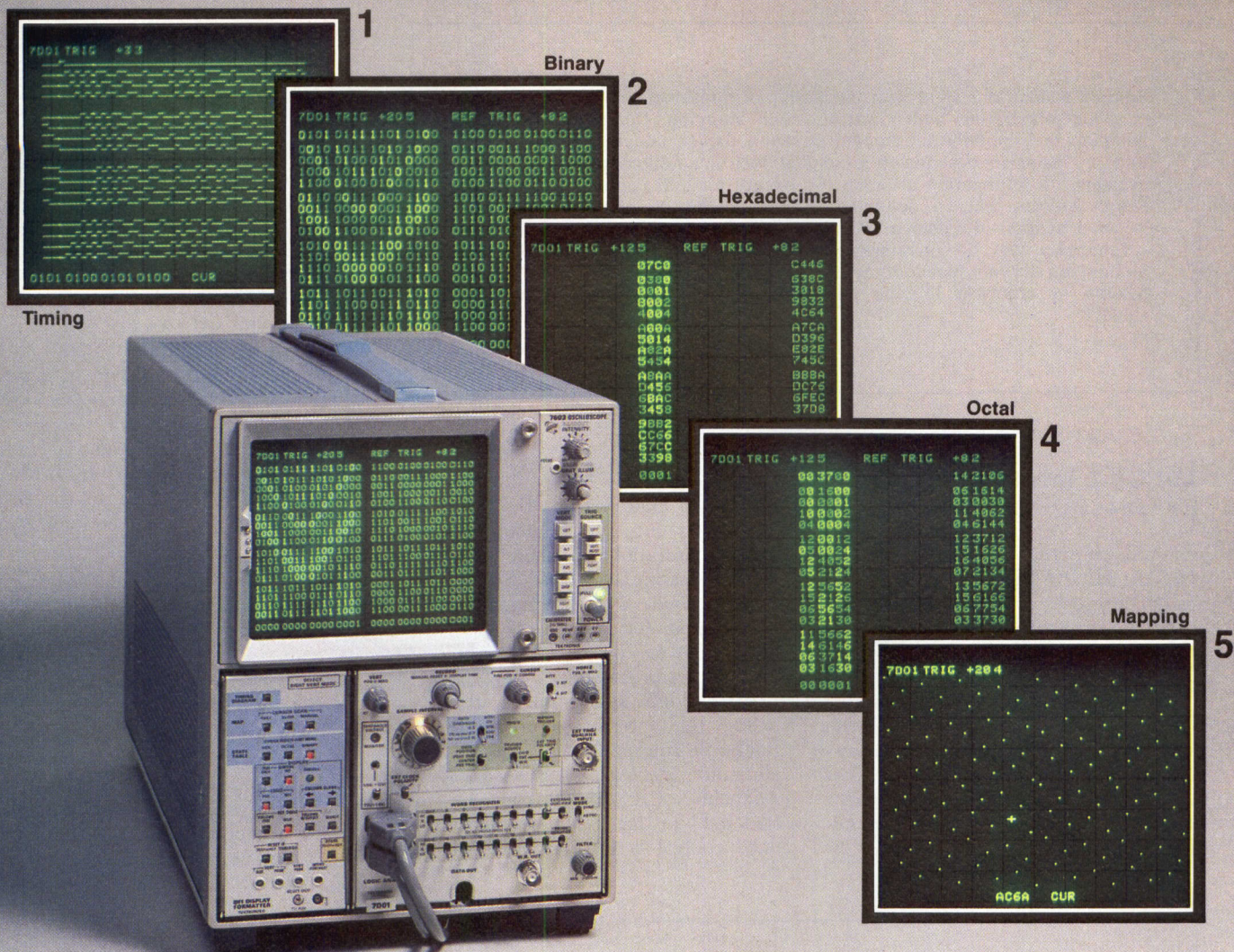
Each of the small independent programmable computers contains 4096 words of memory, instructions, registers, and I/O capabilities. The small computers perform data formatting address calculations, directory, and pointer processing, and character comparisons and conversions. All use an identical instruction set and operate with a 1- $\mu$ s cycle time.

The distributed approach to data processing provided by the system hardware architecture is further enhanced by use of network software operating systems—Network Operating System (NOS) and Network Operating System/Batch Environment (NOS/BE). NOS, oriented toward support of hundreds of remote interactive terminals, can handle concurrent high speed local and remote batch processing. Its elements allow secure access to files, provide full mass storage capabilities, and include job control, resource executive, and system management routines. In batch user environments, NOS/BE implements the system's distributed processing hardware design. This architecture reserves high speed computation to the CPU and control of I/O and system functions to the peripheral computers. It also provides data management, time-sharing, and communications support. □

Circle 148 on Inquiry Card



# TEKTRONIX now has 5 ways to look at logic.



## The New DF1 Formatter

First, we gave you the timing display and binary readout with our 7D01 Logic Analyzer. Now, with the DF1 Display Formatter, which is dedicated to the 7D01, you have five display formats to operate from, all in a 7000-Series mainframe. Now you can convert a timing display into tables of words in Binary, Hexadecimal, Octal ... or a mapping configuration ... whatever your application requires.

A STATE TABLE mode of operation produces standard tables of up to 16 lines of 16-bit words. Using the 7D01's cursor, you can step through these tables word-by-word in Binary, Hex, or Octal. A 17th word is added to each table emerging from the 7D01's memory, to serve as a "key" and indicate you are indeed scrolling correctly through the long memory. The 7D01's fine cursor

control steps the display line-by-line, while the coarse control advances it table-by-table.

One of the most powerful analytical capabilities provided by the STATE TABLE mode is that you can display two tables—a reference table of "proved" data plus a "new" data table drawn from a system under test—on the same crt for side-by-side comparison. New data that is different from the reference data is automatically intensified ... you immediately know faulty data exists, and you know its location.

With the DF1 you can map, not just one, but three ways. The ability to map FAST, SLOW, or MANUAL lets you quickly recognize a word of interest, track it, isolate it, then pinpoint it for detailed analysis. The importance of mapping is derived from the speed with which you can isolate problems.

The logic analyzer package shown (7603 Option 1, 7D01, DF1) starts as low as \$5790. If you already own a 7000-

Series mainframe, add the 7D01-1 (7D01/DF1 combination) for only \$4390. Also consider that your money buys you these important 7D01 features: 1) Word recognition, 2) 16 channel operation, 3) 15-ns asynchronous timing resolution, 4) 4k formattable memory (4, 8 or 16 channels), and 5) High Z probes.

For more information or a demonstration of the DF1, contact a Tektronix Field Engineer near you. Or write Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077.

United States sales prices are F.O.B. Beaverton, OR. For price and availability outside the United States, please contact the nearest Tektronix Field Office, Distributor, or Representative.



**TEKTRONIX®**  
committed to  
technical excellence

For technical data, circle 19 on Inquiry Card.  
For a demonstration, circle 20 on Inquiry Card.



# AROUND THE IC LOOP

**Editor's Note:** Consistent with our policy of stressing technological areas of digital electronics which warrant such attention, *Computer Design* is initiating this monthly department covering digital, linear, and hybrid ICs that are used in the design of digital instrumentation, equipment, and systems. All information on such ICs except for that contained in feature length articles will be collected in this section to offer readers with relevant special interests a concentration of data in one location.

Emphasis will be on newly introduced product developments and techniques for all types of applications. However, content will remain flexible in order to provide our readers with information of current value.

## LSI Chip Interfaces $\mu$ Processor and RAMs

An LSI chip that interfaces n-MOS, 16-pin, 4K RAMs with PPS-4 and -8 microprocessor systems without need for any supporting TTL circuitry, the 10929 fully buffers the PPS bus from dynamic RAM loading effects and provides all address multiplexing, system control and refresh functions. Memory refreshing is transparent to the PPS system so that conflicts between its use of memory and refresh operations are eliminated.

On-chip logic permits the interface to float its output to memory, allowing configuration of shared-memory multiprocessing systems. Sharing is accomplished by stealing a clock phase used for refresh so that the transaction is completely transparent to the other processor.

In a high speed block transfer mode, the interface—announced by Rockwell International Corp's Micro-electronic Device Div, PO Box 3669, Anaheim, CA 92803—can be instructed to float the memory bus until control is returned to the PPS

system. Up to 32 n-MOS, 16-pin 4K RAMs can be controlled and directly addressed by a single pair of interfaces, and additional pairs combined with bank switching can access up to 16 banks of 16K bytes each (256K bytes total) in one PPS-8 system.

The company has also announced that it is producing its own n-MOS, 16-pin, 4K RAMs. The 1604-8P is intended for microprocessor and related functions.

Large standard memory options are supported by the PPS-8 system's ability to move blocks of data at a rate of up to 4  $\mu$ s/byte. Existing memories of already designed PPS microcomputers can be converted in most cases to standard 16-pin, 4K n-MOS systems with no change in the program software by using the interfaces. Circle 350 on Inquiry Card

## Low Dynamic Impedance of IC Zeners Simplifies Biasing Circuitry

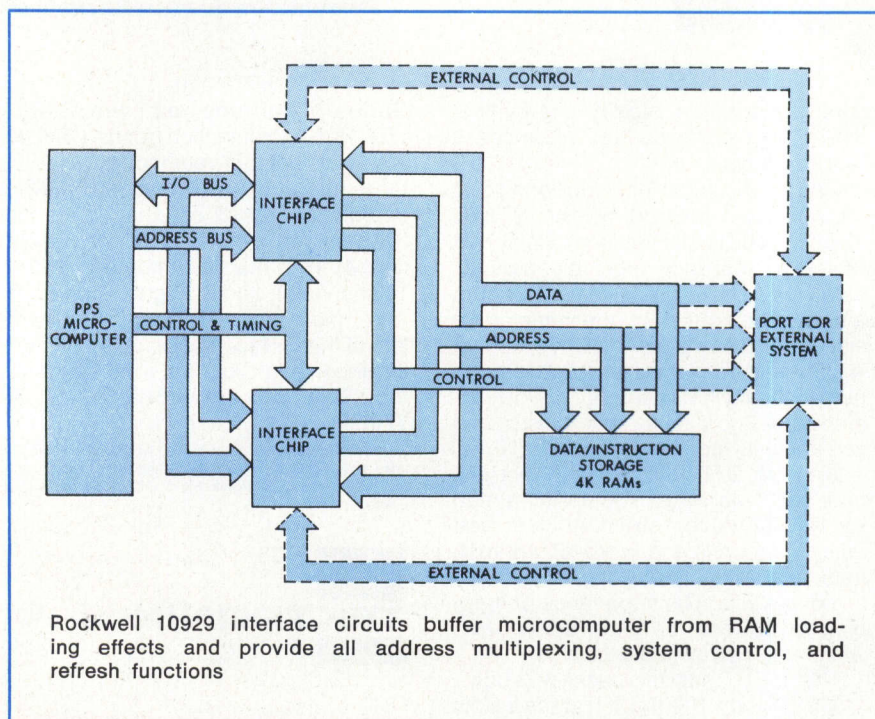
Dynamic impedances 10 to 100 times less than those of discrete zener diodes are claimed for the LM329/129 family of precision 6.9-V reference diodes. The multicurrent, temperature-compensated devices will reportedly simplify biasing circuitry required for a voltage reference to a single additional resistor. LM329 versions cover the 0 to 70°C commercial operating temperature range while LM129 versions meet mil-spec -55 to 125°C requirements.

Capability to operate over a 0.5- to 15-mA current range with virtually no change in performance permits use as replacements for a wide variety of discrete devices. All operating characteristics are essentially independent of operating current.

Introduced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, the devices are available with selected tempcos of 0.001, 0.002, 0.005, and 0.01%/°C (typ 6, 15, and 30 ppm/°C).

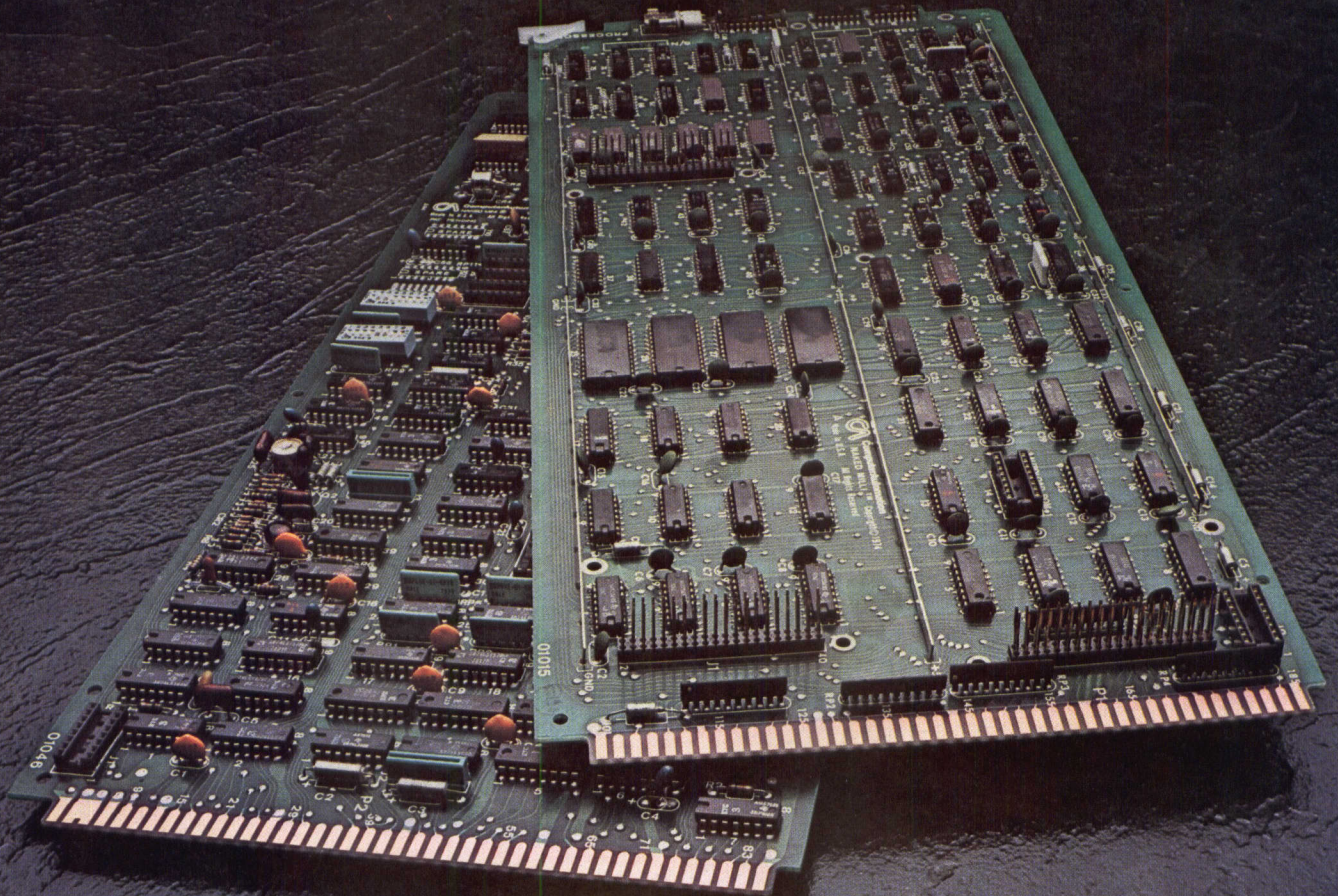
A subsurface breakdown zener yields low noise (typ 7  $\mu$ V rms) and high long term stability (0.002% or 20 ppm typ). Because this zener and temperature compensating transistor are made by a planar process,

(Continued on p 41)



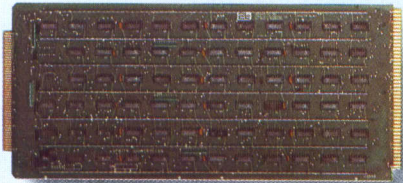


# Computer.

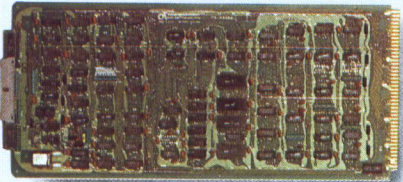




# ComputerA



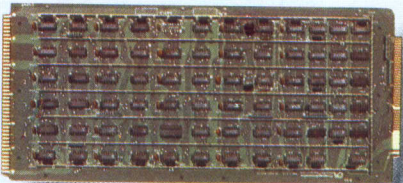
**Paper Peripheral Controller.** Model 14223-00. Single device controller for paper tape reader, paper tape punch, line printer or card reader. Cabling separate.



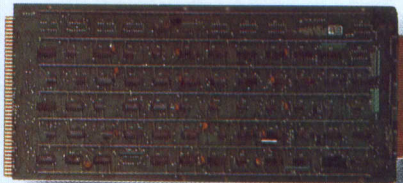
**Floppy Disk Controller.** Model 14566-01. Provides interfaces for one to four IBM-compatible standard floppy disks, or equivalent. Cabling separate.



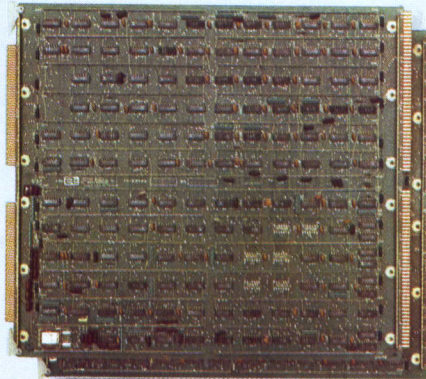
**64-bit Input Module.** Model 13219-00. Provides 64, 32, 16 or 8-bit inputs with individual strobes.



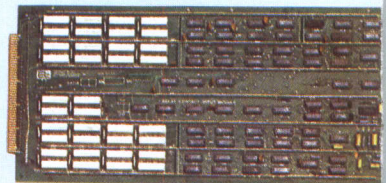
**16-bit Digital Input/Output Module.** Model 13213-00. Provides input and output registers which may be used as one 16-bit or two 8-bit registers. DTL/TTL compatible.



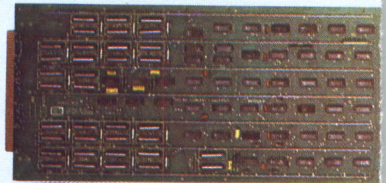
**I/O Driver Module.** Model 13222-00. Units drive the computer I/O bus up to 25 feet, buffer internal I/O bus from external noise. Does not include memory signals.



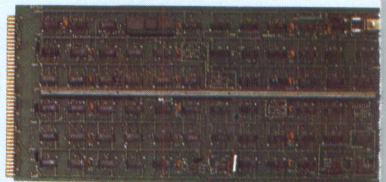
**Moving Head Disk Controller.** Model 14530-XX. Provides interfaces for one to four standard moving head disk drives, or equivalent. 1500 or 2400 RPM. Cabling separate.



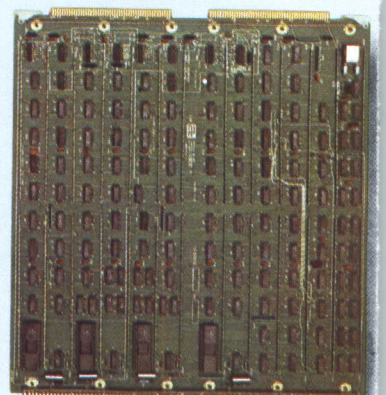
**32-bit Relay Input Module.** Model 13215-00. Operates as one 32-bit, two 16-bit, or four 8-bit inputs.



**32-bit Relay Output Module.** Model 13214-20. Operates as one 32-bit, two 16-bit, or four 8-bit outputs.



**Asynchronous Modem Control.** Model 14535-0X. For one asynchronous line (point-to-point, multipoint, or dial). Fully programmable for mode, character size, parity, echoplex, diagonal loop-back, special character detect, variable stop bits. Send/receive speed individually selectable with jumpers - to 9600 baud. Available as EIA Interface with full Data Set Controls or as Current Loop Interface.



**Asynchronous Modem Multiple.** Model 14512-XX. As above, but for two or four independent asynchronous lines. Multiple vectored interrupts for each line.

**Piggyback Teletype Interface.** Model 12635-01. For LSI-3/05 processor. On-board mounting provides bit-serial interface. (For byte-serial interface, use Distributed I/O System with Current-Loop Serial Intelligent Cable.)

**I/O Terminator Module.** Model 14511-00. Convenient means for terminating user-designed I/O cables. Plugs onto rear of I/O cards (uses 100 pin connector) with rigid termination. Pads for mounting termination components provided.

**Utility I/O Interface Module.** Model 14223-00. General purpose interface with 8 or 12-bit output transfers with 4 control bits in parallel.

NOTE: Products shown are representative only. For information on products, accessories...



# erization.

picked doesn't offer all the interface he needs.

Or, in some cases, the supplier's interface solution is so expensive it forces the OEM to go his own way.

So, at a time when he needs to concentrate all his energies on his own product development, the OEM finds himself committing substantial resources to a peripheral project. One that can be deceptively time-consuming and costly.

Suddenly the designers are coming in, more test equipment is being designed/built/ordered, ditto for new jigs and test fixturing, the documentation hassle is getting under way, and the dollar and time costs start really piling up.

ComputerAutomation is the only computer company that has solved that problem. You can see it here in the picture. Our exclusive Distributed I/O System. Probably the closest thing to a universal interface you'll ever come across.



The Distributed I/O System only works with our computers, but it works with *all* our computers.

The way it works is this: one half-card I/O Distributor handles the commonalities for up to eight interfaces. (There's a four interface version, too.) The actual interface is accomplished by an Intelligent Cable — so-called because of the microcoded PicoProcessor molded into the cable.

This system offers amazing versatility: any and all kinds of interface can be mixed in any combination — serial, parallel or whatever. And not just standard peripherals, either. The Distributed I/O System accommodates special purpose black box kinds of things, too. There's even a version you can custom microcode yourself.

The cost? Typically under \$200 per interface in OEM quantities of 100.

### **Maintenance Costs.**

The cost of keeping a computer in service over the long haul can be enormous. The proof of which is the huge service revenues reported by some computer companies. (Up to \$2,000 per year per computer!)

ComputerAutomation's service revenues, by comparison, are minuscule. The reason is that our equipment is so reliable that breakdowns are few and far between. And when there is a malfunction, the fix is almost always a matter of plugging in a spare board and sending the bad board back to us. No tricky fine-tuning to worry about and no high-priced junior technician in there messing around with your customer's equipment.

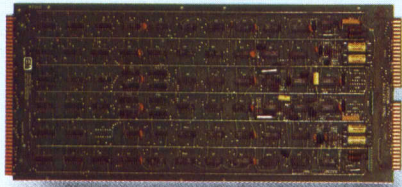
### **The Computerization Solution.**

The computerization problem obviously goes far beyond computers. So it makes sense that the solution is not only a computer solution, but a systems solution as well.

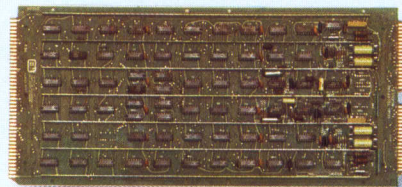
To find that solution you have to look at the big picture... which we invite you to do by turning the page.



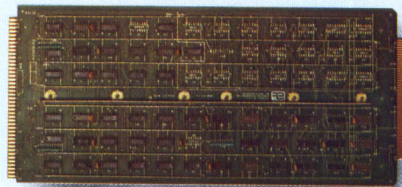
# Automation



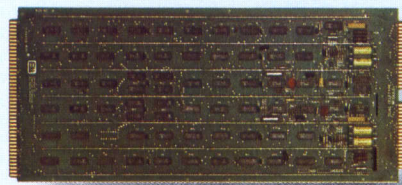
**Dual TTY Interface.** Model 14236-21. For two modified ASR-33 Teletypes. 20 mA Current loop, 110 baud, two half-duplex channels. Has circuit for programmed motor on/off.



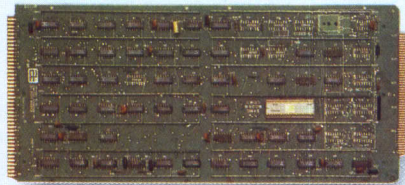
**EIA RS232 Interface.** Model 14236-5X. For one CRT at baud rates from 110 to 9600. Half-duplex operations only.



**Automatic Calling Unit (ACU) Multiplexer.** Model 13523-0X. Provides interfaces for one to four Model 801 ACU's, or equivalent. Simultaneous operations, full digit buffering and sense date-line busy. Four vectored interrupts per ACU. Available for either two or four ACU's.

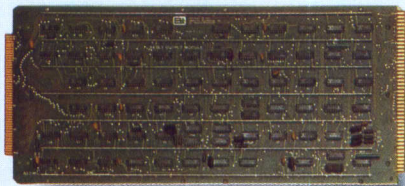


**Dual CRT Interface.** Model 14236-1X. For two CRT's or leased line modems. EIA RS232 interface with two half-duplex channels, each with one output control line and one input status line. Baud rates from 110 to 9600.



**Synchronous Modem Controller.** Model 14513-00. Double buffered, half or full-duplex interface for synchronous communications line (point-to-point, multipoint, or direct dial). EIA RS232C/CCITT compatible, programmable synchronous character, and one special character detect. Odd, even or no parity and 5-8 bit frame size program selectable. Transfer to 9600 baud.

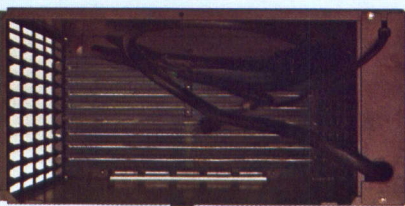
Model 14513-01 provides internal clock with strappable options for 1200, 2400, 3600, 4800, 7200 or 9600 baud operation and full Data Set Controls.



**64-bit Output Module.** Model 13216-00. Provides output for use as 64-bit word or multiples of 32, 16, or 8-bits with individual strobes.

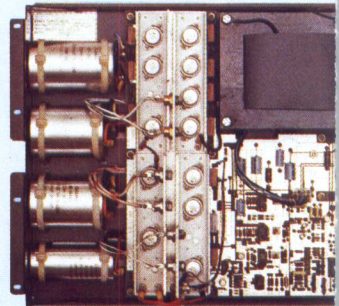


**Processor Chassis.** Model 12034-00/20500-01. Full-card chassis. Available in 5-slot and 9-slot versions. Includes motherboard and fans.

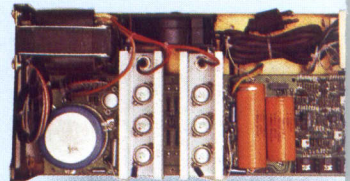


**Card Expansion Modules.** Model 12098-00/12099-00. Five and nine-slot versions include chassis, blank panel with expansion buffer controller, interconnecting cables and power supply.

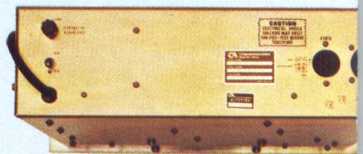
**Card Cage, LSI-3/05.** Model 12095-0X. Available in either 3-card or 5-card versions. Includes motherboard, card guides, and retaining hardware.



**Standard Power Supply.** Model 12044-00. Supplies +5V @ 25 Amps, +12V @ 4 Amps and -12V @ 9 Amps.



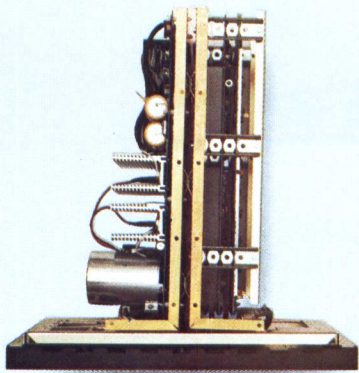
**Power supplies for LSI-3/05.** Model 12046-0X. Open frame power supplies mount in any plane. Supplies +5V @ 10 Amps, +12V @ 0.8 Amps, -12V @ 0.8 Amps; +12V @ 1 Amp, -12V @ 1.5 Amps. With fan.



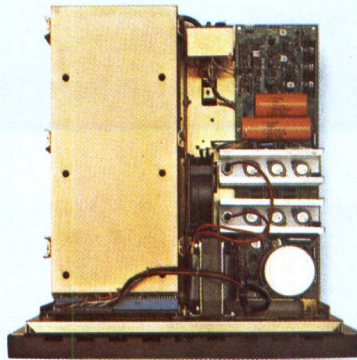
**Jumbo Power Supply.** Model 20441-00. Supplies +5V @ 36 Amps, +12V @ 5.6 Amps, -12V @ 10.7 Amps.

**MegaByters.** Model 109 Series High-speed 16-bit systems for real-time, communications and business applications. Features include LSI Family compatibility; four standard input-output modes including Direct Memory Access vectored priority interrupts; and a comprehensive set of 224 instructions. Includes Jumbo Chassis, Jumbo Power Supply, Programmer's Console, Power Fail Restart, Basic Time Clock, AutoLoad

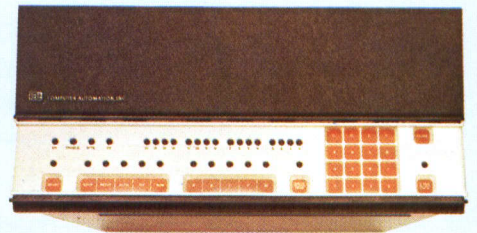




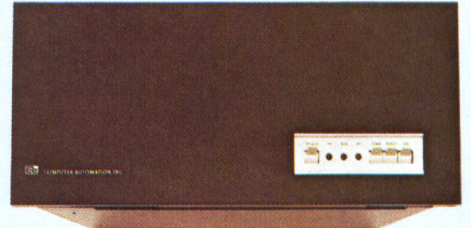
**ALPHA LSI-3/05, NAKED MILLI Series.** Model 10373-XX. Includes LSI-3/05 CPU (Type 1), with LSI Family compatibility, three half-card chassis, 10-Amp power supply and Operator's Console. This small, low-cost computer offers exceptional power and features, including 95 instructions, Power Fail Restart, vectored priority interrupts, Real-Time Clock, AutoLoad capability and 16-bit DMA port. Full memory options.



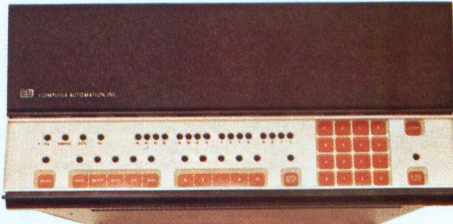
**ALPHA LSI-3/05 B, NAKED MILLI Series.** Model 10375-XX. Includes LSI-3/05 CPU (Type 1) described at left, plus 5 half-card chassis with fan, 15-Amp power supply and Operator's Console. Full memory options.



**ALPHA LSI-3/05 C, NAKED MILLI Series.** Model 10376-XX. Same as LSI-3/05 B configuration with addition of Programmer's Console.



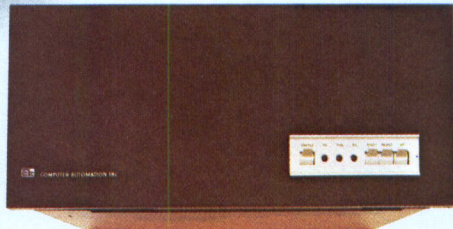
**ALPHA LSI-3/05 D, NAKED MILLI Series.** Model 10356-XX. Includes LSI-3/05 CPU (Type 1) as above, standard five full-slot processor chassis, 25-Amp power supply and Operator's Console. Core memory in either 4K, 8K or 16K word sizes.



**ALPHA LSI-3/05 E, NAKED MILLI Series.** Model 10366-XX. Same as LSI-3/05 D configuration with addition of Programmer's Console. Either RAM-only or Core Memory in 4K, 8K, or 16K sizes.

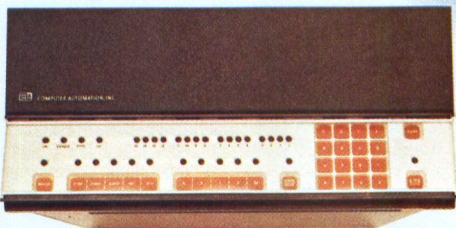


**ALPHA LSI-2/20 T, NAKED MINI Series.** Model 1055X-XX. Same as LSI-2/10 configuration except with high performance LSI-2/20 CPU offering twice the speed of the LSI-2/10.

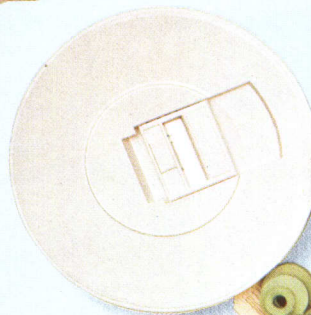
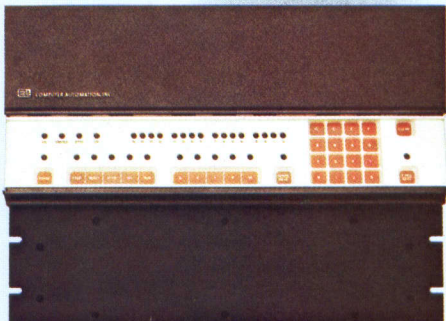


**ALPHA LSI-2/20 G, NAKED MINI Series.** Model 1055X-XX. Same as LSI-2/10 G configuration except with high performance LSI-2/20 CPU, as above.

**ALPHA LSI-2/10 T, NAKED MINI Series.** Model 1074X-XX. A 16-bit mini-computer offering twice the speed of our LSI-3/05 computers. CPU provides 188 major instructions, including multiple stack handling, hardware multiply/divide, memory scan, and extensive byte capability. Five vectored priority interrupts are expandable to 256; two direct memory channels may be increased to 64. Direct Memory Access is standard. Includes Power Fail Restart. Also includes chassis with power supply and Operator's Console. Available in either 5-card or 9-card (Jumbo) versions. 4K or 8K Core 980 Memory or 16K Core 1200 Memory. Memory modules may be added up to 256K words using Memory Bank Control.



**ALPHA LSI-2/10 G, NAKED MINI Series.** Model 1074X-XX. Same as LSI-2/10 T configuration with addition of Programmer's Console.



**Software and Documentation Packages.**

Advanced software and documentation packages, including BASIC, FORTRAN IV, Real-Time Executive and Operating System are available. Plus a complete inventory of diagnostics, editors, assemblers.

Variables, Teletype or EIA CRT interface, Real-Time and AutoLoad ROM Set. Full Memory options.



# Compute

The cost of an OEM computer can be a lot different than the price on the P.O.

In fact, everything considered, the purchase price could be as little as ten percent of the costs incurred over the life of the computer.

To be brutally blunt, it all depends on whose hardware you buy. That's because the cost of computerizing goes way up with most machines.

The cost of hardware integration, for example.

The cost of developing interface electronics.

The cost of developing software.

The cost to maintain the machine once it's out in the field.

Any one of which could seriously impact the profitability of your product. Given that possibility, here's what you need to know to protect those profits.

## **Engineering Costs.**

Prototyping and systems integration is a high-cost area where, traditionally, the OEM has been left to his own devices, so to speak.

ComputerAutomation doesn't work that way. We've accumulated enormous experience in systems integration because we get involved in our customer's projects.

What's more, we've put together a program for sharing that experience with our customers... free, of course. Part of it includes extraordinarily comprehensive documentation provided on an on-going basis. But more importantly, it's a people-to-people program that even provides on-board support personnel when they're needed.

## **Programming Costs.**

No other endeavor consumes time and money quite like programming. For the OEM who's usually racing to release a new product ASAP, even a minor programming effort can be a major setback.

The solution is to concentrate on the applications end of it and not re-invent software that's already on somebody's shelf — ours.

ComputerAutomation has an enormous library of powerful software that will cost you next-to-nothing. Everything from humble assemblers to high-powered compilers in BASIC and FORTRAN IV.

The powerful instruction set that comes with our computers will spare you countless hours of programming effort, too, because it's designed with that objective in mind.

Remember, too, that all our computers are buss compatible. Which means you won't have to start programming all over again when you switch to another computer in our LSI Family.

## **Interface Costs.**

Many times an OEM is forced to invent his own interface... usually a very expensive proposition... because the supplier he's





# ComputerAutomation cuts the cost of computerizing.

Knowing what the OEM needs... understanding the OEM predicament. That's what sets ComputerAutomation apart. It's the reason we ship over 100 computers per week — the second highest shipping rate in the industry.

## Guaranteed savings.

OEM's buy our computers because they're the most reliable machines made.

Every IC, subassembly, memory subsystem and completed computer is temperature, shock and vibration tested.

That's why ComputerAutomation can offer the only one-year warranty in the industry — when we send a computer out, we know it's not coming back for a long time.

## We deliver.

In an industry where one delinquent diode can (and sooner or later will) shut down an entire assembly line, that's saying a lot.

It especially says a lot to OEM's who know they're at the mercy of their sole source computer supplier. One thing you can't do is stick somebody else's machine in that slot.

So here's a thought you might want to stick in the back of your mind for future use:

ComputerAutomation delivers on time.

The reason is that we deliver from inventory — usually a comfortable 30-day cushion of computers sitting around getting more reliable by the minute because they're kept under power and constant test scrutiny.

A lot more trouble for us, but a lot less worry for you. And it does tend to prove our point. We understand the problem.

## From the people who brought you the NAKED MINI.<sup>®</sup>

The people who brought you the first solution to high-cost computers.

And the most recent solution as well.

And all the solutions in between. Including low-cost memory. And the Distributed I/O System.

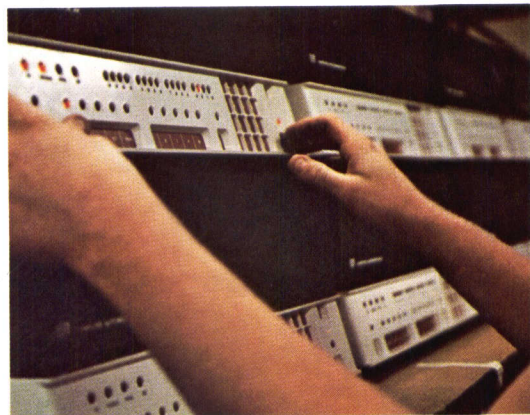
Plus on-time delivery. And the only full-year warranty in the business.

The total solution to computerization.

So if you can't spare the time and money to re-invent the wheel, there's a simple solution... from the people who came up with all the other solutions.



Temperature chambers stress computers to isolate marginal components. Computers are continuously tested during 72-hour burn-in at 50°C. Any error starts the test over from the beginning. To further stress the computer, power is cycled on and off approximately 2000 times during test.



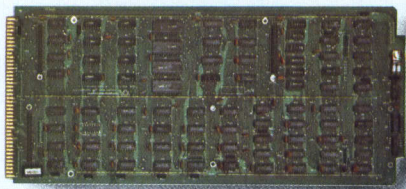
Computers awaiting shipment idle away the hours under test. Reliability benefits from the additional component aging.

 **ComputerAutomation**  
Naked Mini<sup>®</sup> Division

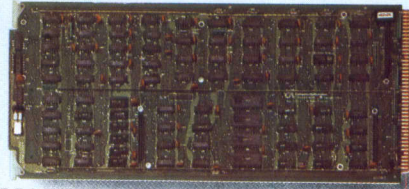
ComputerAutomation, Naked Mini Division, 18651 Von Karman, Irvine, California 92713/Eastern Regional Office, 79 North Franklin Turnpike, Ramsey, New Jersey 07446, (201) 825-0990/Midwestern Regional Office, 2621 Greenleaf Avenue, Elk Grove Village, Illinois 60007, (312) 956-6400/Western Regional Office, 18651 Von Karman, Irvine, California 92713, (714) 833-8830/Europe, CAI Ltd., Hertford House, Denham Way, Maple Cross, Rickmansworth, Hertfordshire, WD3, 2XD, England, Telephone Rickmansworth 71211.

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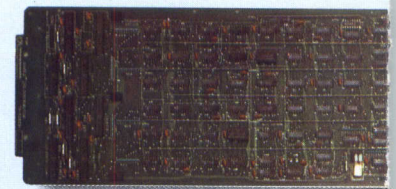




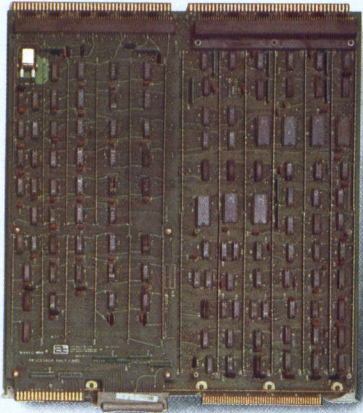
**NAKED MILLI LSI-3/05 CPU, Type 0.** Model 10300-00. Small low-cost processor offers exceptional power and features. 95 instructions, Power Fail Restart, vectored priority interrupts and 16-bit DMA port.



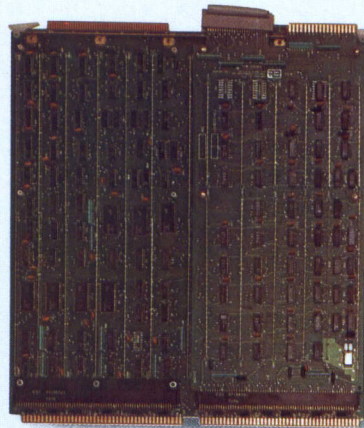
**NAKED MILLI LSI-3/05 CPU, Type 1.** Model 10300-01. Same as Type 0 at left, but also includes Real-Time Clock and AutoLoad capability.



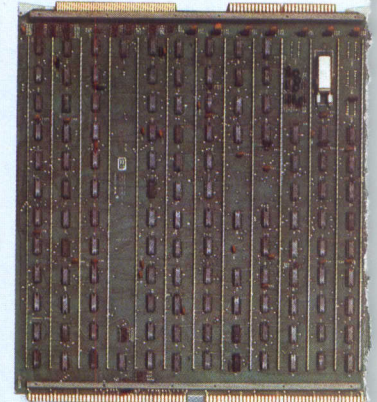
**I/O Distributor.** Model 14629-XX. In conjunction with Intelligent Cable (see text), the I/O Distributor provides up to eight interfaces—serial or parallel in any mix. Small version accommodates four interfaces. A DMA version allows data transfer rates up to 250K bytes per second.



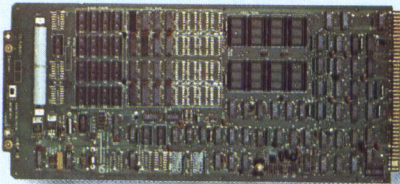
**NAKED MINI LSI-2/10 CPU.** Model 10600-00. 16-bit minicomputer processor offers twice the speed of LSI-3/05 processors. Includes Power Fail Restart option. See ALPHA LSI-2/10 description.



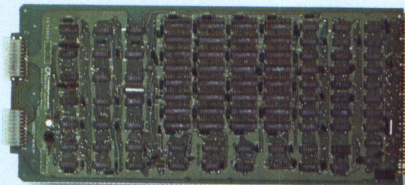
**NAKED MINI LSI-2/20 CPU.** Model 10400-00. Designed for high-performance applications. Twice the performance of the LSI-2/10 for only a nominal increase in cost. Also includes Power Fail Restart.



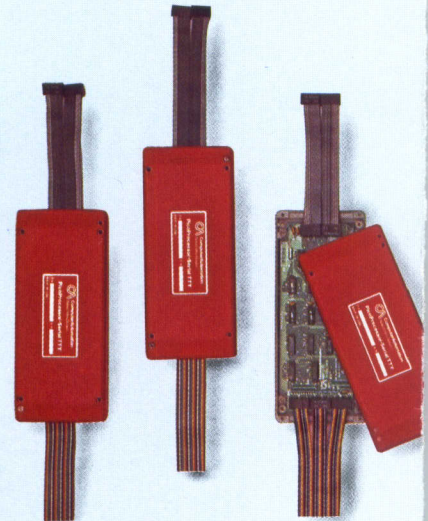
**Magnetic Tape Controller.** Model 14224-00. Provides interfaces for one or four 9-track standard tape units, or equivalent. Cabling separate.



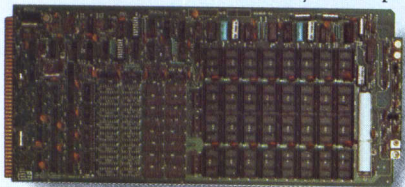
**RAM/ROM/PROM Memories.** Model 11650-XX. Includes semiconductor RAM in choice of 256, 1K or 2K words; sockets for 8K words of ROM and sockets for 2K words of PROM. Available with On-card Battery Backup.



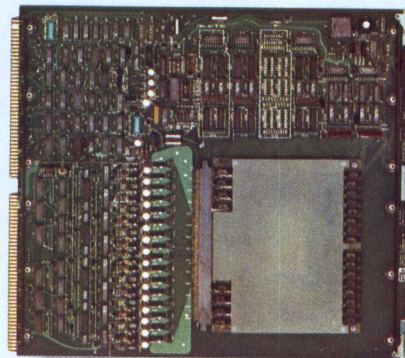
**RAM-only Memories.** Model 11642-XX. Choice of 4K or 8K words. Available with Battery Pack.



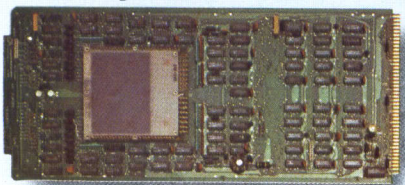
**Intelligent Cables.** Model 14631-XX. A broad assortment of models offers off-the-shelf interface for most standard and special user devices: Line Printer, Reader, Paper Tape Reader, Paper Tape Punch, Current Loop, CRT, Modem, General Purpose and Custom Program versions.



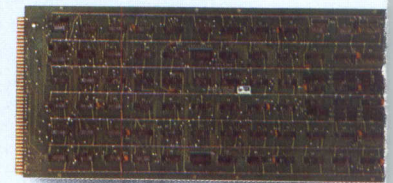
**RAM/EPROM Memories.** Model 11530-XX. Includes semiconductor RAM in choice of 1K or 2K words and sockets for 4K words of ultra-violet Erasable Programmable ROM. Available with On-card Battery Backup; also, optional EPROM Programmer.



**Full-card Core Memories.** Model 115X0-XX. Choice of 8K words of Core 980 Memory or 16K words of Core 1200 Memory. For Standard or Jumbo Chassis only.

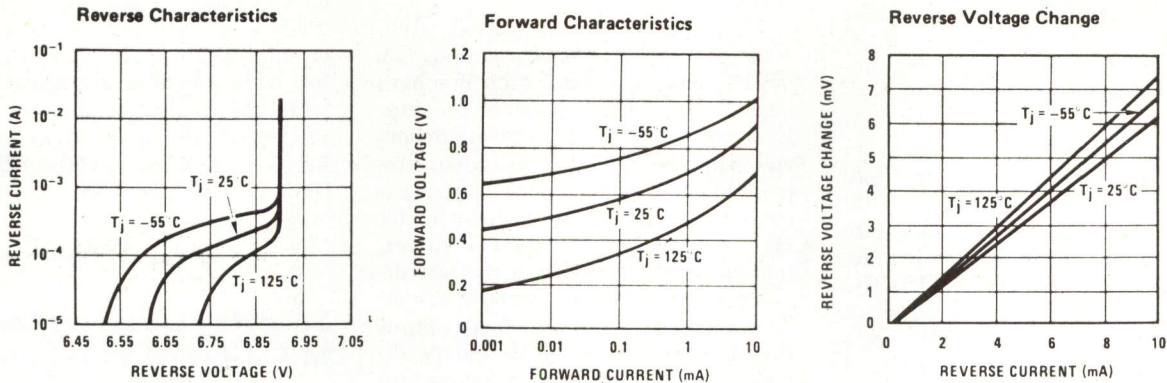


**Half-card Core Memory.** Model 11671-XX. 4K words. For either NAKED MILLI/ALPHA LSI-3/05 or NAKED MINI/ALPHA LSI-2 Series Computers.



**16-channel Priority Interrupt Module.** Model 13220-00. 16 interrupts with acknowledgement lines.





Typical performance characteristics of LM329/129 precision references

they are immune to problems such as shifts in zener voltage caused by temperature cycling that are found in ordinary zeners.

Active circuitry around the zener buffers external current changes to

give a 1-Ω dynamic impedance. Absolute max ratings include: reverse breakdown current, 30 mA; forward current, 2 mA; and lead temperature (soldering, 10 s), 300°C.

Packaging is in either a TO-46

metal can or a plastic TO-92. Hundred quantity pricing for the LM-329DZ—0.01%/°C tempco, 0 to 70°C operating temperature—is \$0.75; the LM129AH—0.001%/°C, -55 to 125°C—is \$15.

### μProcessor Interface Circuit Has Improved Performance/Capabilities

Peripheral interface adapter (PIA) MK 6820, a high performance circuit for interfacing peripheral equipment with the 6800 microprocessor, is a pin-for-pin replacement for Motorola and AMI 6820s but is claimed to have improved performance. In addition, it functions as a generalized I/O for any microprocessor bus.

The device is available from Mos-tek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 in two low power versions—300 mW max/250 mW typ and 400 mW max/300 mW typ—and provides 2 MHz/1 MHz bus operation rather than 1 MHz only, has fully TTL-compatible inputs including ENABLE, and has two TTL loads on outputs instead of one. It is completely static, requiring no dynamic limitations on the ENABLE input, and is specified over the entire 0 to 70°C temperature range.

High impedance 3-state and direct transistor drive peripheral lines are CMOS compatible. A single 5-V power supply is required.

Communication to peripheral equipment is through two, 8-bit bidirectional ports and four software programmable control/interrupt lines

which provide peripheral activity management. Interrupt/control lines for each port can be configured as two interrupt/status inputs or as one interrupt/status input and one control output.

Circle 351 on Inquiry Card

### 1K Bipolar and 4K MOS RAMs Added to Memory Product Line

One 1K and two 4K RAMs—the μPB2205, μPD410, and μPD414—have been announced by NEC Micro-computer Inc, 5 Militia Dr, Lexington, MA 02173 as additions to its memory product line. The 1K device will be available in the third quarter of 1976, the 4K RAMs will be available in the fourth quarter.

The 1K x 1-bit bipolar, TTL-compatible μPB2205 has 50-ns access time and serves as an alternate source to the Fairchild 93415A and equivalent memories. It is fully decoded, has open collector output, and comes in a 16-pin ceramic DIP.

μPD410, a 4K x 1-bit static device, is pin-compatible with the company's μPD411 dynamic RAM. It has a 100-ns access time. Standby power is typ 50 mW max. Fabricated using n-chan-

nel, silicon gate MOS technology, the industry-standard 22-pin ceramic DIP requires 12-, 5-, or -5-V power supplies.

μPD414, a 4K x 1-bit dynamic n-channel MOS RAM uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation. It is pin-compatible with existing 16-pin devices, and will be available in both ceramic and plastic packages.

### Data Converters Match Wide Range of Applications

A 4-product family of TTL-compatible converters has been announced by Beckman Instruments, Inc, Helipot Div, 2500 Harbor Blvd, Fullerton, CA 92634. The two digital-to-analog and analog-to-digital converters utilize simplified internal and external circuitry, thin-film ladder networks for stability over time and temperature, and improved packaging.

Both DACs are 12-bit binary devices with external connection options for bipolar and unipolar outputs of ±2½, ±5, ±10, 5, and 10 V full scale. Current output options



are also available. The two ADCs, designed as companions to the DACs, are high speed devices using the successive approximation method.

Model 877-80 DAC and model 873-78 ADC are low priced devices in 24-pin glass DIPs, selling for \$20 and \$45 each, respectively, in 100 quantities. Operating temperature range is 0 to 70°C. Conversion accuracy of both is  $\pm\frac{1}{2}$  LSB in 12. The ADC has  $\pm\frac{1}{2}$  LSB quantizing error and is available with full scale voltages of 10 V unipolar and 5 and 10 V bipolar.

Models 877-80 DAC and 873-88 ADC are higher performance industrial units meeting the specifications of their respective lower priced counterparts but operate over a -25 to 85°C temperature range and are in 24-pin metal DIPs. Prices are \$70 and \$120, respectively, per unit in quantities of 100. Both are also available screened to MIL-STD-883A for the -55 to 125°C military application temperature range.

Circle 352 on Inquiry Card

### Low Power Plastic-Package ADCs Meet Commercial Requirements

Availability of its 8-bit monolithic A-D converter in a plastic package for use in commercial environments (0 to 70°C temperature range) has been announced by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94040. The single chip CMOS devices feature differential and overall linearity error of  $<\frac{1}{4}$  LSB and power dissipation of typically  $<20$  mW. No active auxiliary components are required. Latched parallel outputs facilitate inputting to microprocessors and other digital logic. Price for the 8700CJ in a 24-pin DIP is \$9.95 in 100 unit lots.

Circle 353 on Inquiry Card

### CMOS Clock Circuit Operates from 1.5 V

Power consumption, size, and cost of quartz clock modules are reduced through use of a CMOS circuit that operates from a 1.5-V battery. De-

signed primarily for applications using oscillator frequencies of between 2 and 10 MHz, the ICM7038B performs the functions of oscillator, frequency divider, and output driver for synchronous single-phase, micropower motors.

The circuit, from Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014, uses an inverter oscillator having all biasing components on-chip. Everything except tuning components and a quartz crystal is included. Sixteen binary dividers permit frequency division from 4 MHz down to 64 Hz. An incorporated power driver, tapped off the third from the last divider, can be used as an alarm driver. The D version has the final output divider stage at the 17th binary divider, while E and G versions are 18- and 19-stage divider options.

Output from the divider network drives a bridge output circuit which provides a 50% duty cycle ac square wave having virtually zero dc component. Total output driver saturation is typically 350  $\Omega$ . In addition, the alarm output has a low saturation resistance.

Typical circuit consumption is 105  $\mu$ W at 1.5 V. Current drive is 1 mA min. Operating temperature range is -20 to 70°C. Custom versions of the circuit include low current oscillators for use with high quality crystals and low value capacitor tuning loads.

Circuits are available in standard 8-lead plastic DIPs and as dice. DIP unit prices range from \$4.70 in 1 to 24 quantities to \$3.15 for 100 to 999. Dice unit prices are \$3.00 for 25 to 99, \$2.52 for 100 to 999.

Circle 354 on Inquiry Card

### Display Drivers Contain Current Feedback System

Parts count in a closed-loop system for display applications can be reduced by up to 11 components through use of the NE584/585 gas discharge display drives. The pair of 22-pin DIP ICs, made by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, are claimed to form "the first such unit available that incorporates a completely integrated closed-loop current feedback system for self adjusting to accommodate changing load conditions."

The NE584 cathode driver is current programmable and can drive up to nine segments, while the NE585 anode driver can drive up to nine digits. Current capability is rated at 5 mA/segment for the signal and 35 mA/digit for the digit driver.

Only a single pair is required between the logic segment of a display system and the high voltage output; no capacitors or resistors are needed.

The units are fully compatible with MOS and TTL inputs and have internal current limiting protection. NE585 is available in units for six or nine digits, while 584 is available for eight or nine segments for use with gas discharge displays. Typical pricing in 100 and up quantities is \$2.75 for 584 and \$2.50 for 585.

Circle 355 on Inquiry Card

### Schottky Counters Meet MIL/Commercial Temps

Low power Schottky, 4-bit, up/down BCD and binary counters, the Am54/74LS192 and Am54/74LS193 offer a guaranteed minimum count rate of 25 MHz (min). They feature separate up and down clocks and an asynchronous parallel load capability, and are pin-compatible with like-numbered units from Texas Instruments.

Am25LS192 and Am25LS193 are proprietary, high performance versions with guaranteed minimum count rate of 35 MHz. Maximum carry propagation delay is 17 ns, 94% faster than the standard 54/74LS design. They are specified with improved noise margins over the commercial range and twice the fanout over the military temperature range.

Units, made by Advanced Micro Devices Inc, 901 Thompson Place, Sunnyvale, CA 94086, are available in 16-head molded, hermetic DIL and ceramic flat packages and as dice. Temperature ranges of various versions are 0 to 70°, and -55 to 125°C. Prices start at \$1.22 for 100-piece quantities.

Circle 356 on Inquiry Card

### Decoder Converts Touch-Tone Signals

A microcircuit decoder, the 7516 detects 2-of-8 tone signals generated by Touch-Tone™ telephones and decodes them into either discrete digital 1-of-16 or BCD logic level outputs. Proprietary MOS/LSI and thick-film hybrid circuits are combined by Telenetics, Inc, 4120 Birch St, Newport Beach, CA 92660 in a 32-pin, 0.3 x 0.9 x 1.9" DIP.

Touch-Tone to dial-pulse conversion may be accomplished by adding a dial pulse generator. Selec-



# Your Single Bored Computer can be the life of the party.

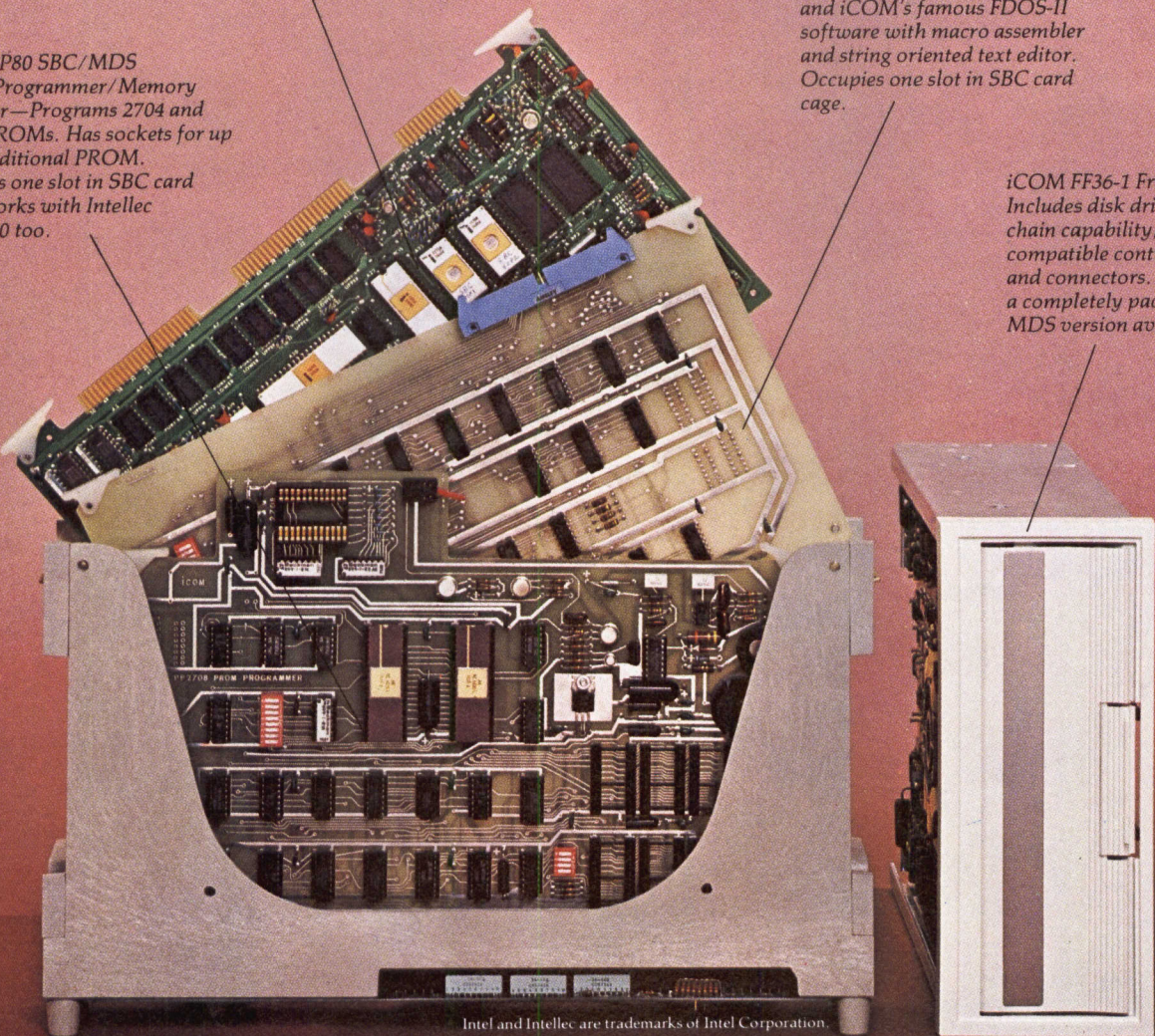
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Computer and Card Cage

iCOM PP80 SBC/MDS  
PROM Programmer/Memory  
Expander—Programs 2704 and  
2708 EPROMs. Has sockets for up  
to 8K additional PROM.  
Occupies one slot in SBC card  
cage. Works with Intellec  
MDS-800 too.

iCOM 360-56 SBC80/10 Interface  
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Includes software driver PROM  
and iCOM's famous FDOS-II  
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and string oriented text editor.  
Occupies one slot in SBC card  
cage.

iCOM FF36-1 Frugal Floppy<sup>TM</sup>—  
Includes disk drive with daisy  
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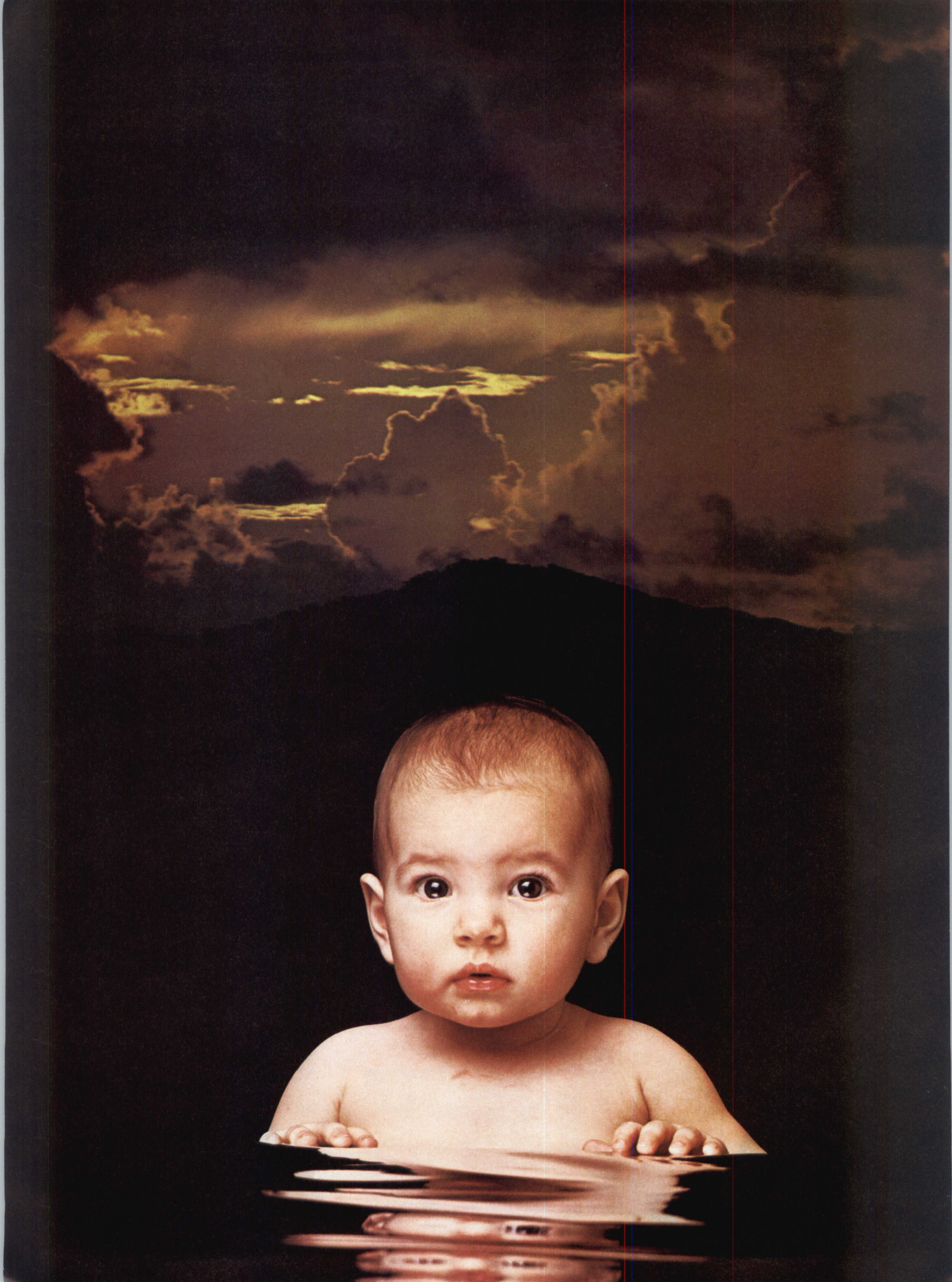
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# The emergence of a new thinking machine.

## The SEL 32/35.

**Twice the power for half  
the price.**

If your computing needs could be answered by such machines as Data General's Eclipse, or DEC's PDP 11 series or Interdata's 7/32, consider the SEL 32/35.

Rather than get into bits and bytes, there's really only one thing you need to know about the SEL 32/35: You get two to four times the power for every "compute" dollar spent. Period.

That's a pretty powerful statement. But the SEL 32/35 is a very powerful machine.

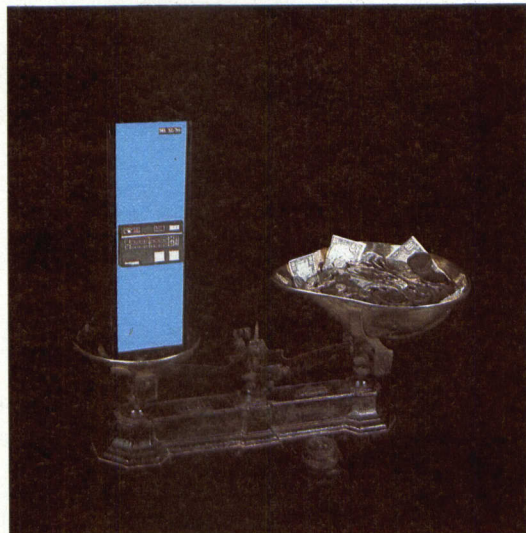
Extra power can go a long way to maintain the balance you need in your computer system, so essential for reliable, peak performance.

And extra power, for fewer dollars, can do wonders when you're trying to balance a corporate budget.

For more information about the new arrival in our family of computers, just circle our number on the Reader Service Card. Or, for faster action, call us direct.

Either way, we'll see that you get all the vital statistics on our new baby.

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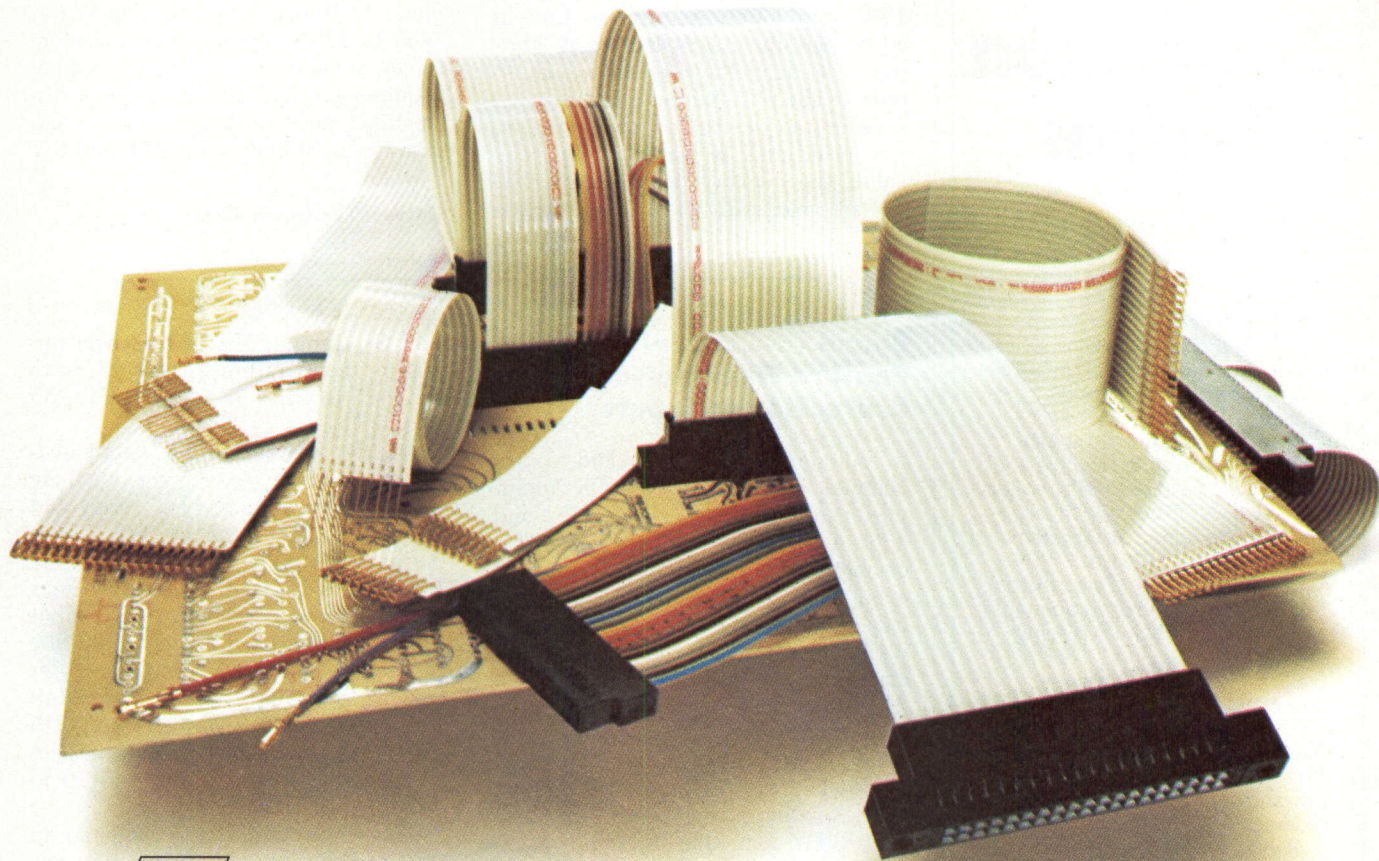
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# LSI-11 Micro- computer Data Acquisition System

The ADAC Model 600-LSI-11 is the first data acquisition system available for use with the DEC LSI-11/PDP-11/03 microcomputers.

Both software and hardware compatible, the Model 600-LSI-11 A/D system plugs directly into the bus of the LSI-11/PDP-11/03 systems.

Features include a 12 bit A/D converter, high speed sample and hold circuit, from 16 to 64 channels of MUX., DC/DC power converter and bus interfacing. A/D system throughput rate is 35 KHz.

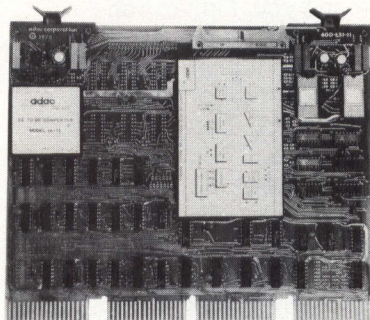
Optionally available are: one or two 12 bit D/As and programmable gain amplifier with auto zeroing circuit.

Basic system price in single quantity is \$895.

Send for full technical data on the Model 600-LSI-11 and other ADAC minicomputer data acquisition and control systems and modules.

ADAC Corporation,  
15 Cummings Park, Woburn,  
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## AROUND THE IC LOOP

### Peak Sense and Hold Analog Memory In a DIP

Claimed to be the first peak sense and hold analog memory in a dual in-line package, the 5902 provides a 100-ns max acquisition time for a 10-V step input. Acquisition time is 30 ns max for a 1-V step input. Output is a dc voltage equal in amplitude to the positive peak input.

Once the device has sensed an input peak and is holding the peak value, the memory decay rate is 100 mV/ms max with no external capac-

ity. External memory capacity may be added to decrease the memory decay rate at the expense of increasing acquisition time.

Other features of the 16-pin device from Optical Electronics, Inc, PO Box 11140, Tucson, AZ 85734 include  $\pm 10$ -mV max sensing error,  $-65$  to  $125^\circ\text{C}$  operating temperature range, standard  $\pm 15$ -V power supply requirement, 270-mW max power dissipation, and reset and gate command compatibility with TTL and 5-V CMOS.

Circle 360 on Inquiry Card

### 8- and 16-Channel MUXs Feature Over-Voltage Protection on Inputs

A differential 8-channel and a 16-channel single-ended CMOS multiplexer, respectively, devices 4551 and 4552 feature over-voltage protection on both analog and digital inputs—even with power removed, break-before-make operation—Schmitt trigger inputs, and CMOS- and TTL/DTL-compatibility, and are offered in a 28-pin hermetic package for optimum reliability. Typ break-before-make delay of 80 ns assures optimum channel-to-channel isolation. Switching time is 500 ns typ. Input resistance is 1.8 k $\Omega$  max and is tightly controlled.

Teledyne Philbrick, Allied Dr at Rt 128, Dedham, MA 02026 has priced the devices at \$28 in domestic USA OEM quantities. Applications include multichannel data acquisition, multichannel data distribution, and variable time delay generation.

Circle 361 on Inquiry Card

### Data Converters Cover Wide Range of Speeds and Temperatures

Three series of data converters with qualifications that match both industrial and military requirements comprise 12 different digital-to-analog and six analog-to-digital converters. Various devices within the line of 12-bit hybrid converters introduced by Datel Systems, Inc, 1020 Turn-

pike St, Canton, MA 02021 cover operating temperature ranges of 0 to 70,  $-25$  to 85,  $-55$  to 100, and  $-55$  to  $125^\circ\text{C}$ .

Of the six successive approximation type ADCs, conversion times are 8  $\mu\text{s}$  for three in the HZ series and 20  $\mu\text{s}$  for three in the HX series. All have 20-ppm/ $^\circ\text{C}$  max tempco, are binary coded, and have  $\pm 1/2$ -LSB max nonlinearity. A self-contained input buffer amplifier provides 100-M $\Omega$  input impedance. Single-unit prices for the 8- $\mu\text{s}$  units range from \$149 for a 0 to  $70^\circ\text{C}$  glass DIP to \$215 for a  $-55$  to  $100^\circ\text{C}$  metal; respective range for 20- $\mu\text{s}$  units is \$119 to \$185.

HZ series DACs are available in either complementary binary or complementary BCD output, with 12-bit and 3-digit resolutions, respectively. Binary units have 0- to  $-2$ -mA  $\pm 10\%$  unipolar output current; pin-programmable output voltage ranges of 0 to 5 and 0 to 10 V unipolar and  $\pm 2.5$ ,  $\pm 5$ , and  $\pm 10$  V bipolar; and  $\pm 1/2$  LSB max nonlinearity. BCD devices have 0- to  $-1.25$ -mA unipolar output current; 0 to 2.5, 0 to 5, and 0 to 10 V unipolar output voltage ranges; and  $\pm 1/4$  LSB max nonlinearity.

Ten units have 20 ppm/ $^\circ\text{C}$  max tempco; the other two have 10 ppm/ $^\circ\text{C}$ . All have settling times of 3  $\mu\text{s}$ , DTL/TTL-compatible inputs, and power requirements of  $\pm 15$  Vdc  $\pm 0.5$  V and 35 mA. Outputs are monotonic over the respective operating temperature ranges. Single unit DAC prices range from \$49 for a 0 to  $70^\circ\text{C}$  glass DIP to \$175 for a  $-55$  to  $125^\circ\text{C}$  metal device.  $\square$

Circle 362 on Inquiry Card



# The 40+ Data Display System.

## More than just a pretty case.



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Reliable system logic operates well within the limits of the bipolar and MOS/LSI circuitry.

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Power supply designed and built by ICC specifically for the 40+ facilitates trouble-free operation.

Gold-plated connectors assure positive electrical contact even after long service.

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Users of ICC's 40+ Data Display System are pleased with the appearance of their terminals. But, more important, they're impressed with their operation. Because, inside the sculptured case of every 40+ Data Display Terminal is a superbly designed electronic system. It offers a wide selection of built-in and optional features, and a choice of configurations to fill changing needs. It's the optimum terminal for many of today's business applications. Our new 12-page brochure tells why. Send for your copy.

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**CIRCLE 26 ON INQUIRY CARD**

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# DIGITAL CONTROL AND AUTOMATION SYSTEMS

## Microprocessors and LSI Devices Are Prime Contributors to Design of Automatic Bowling Scorer

Sophisticated automation—especially since the advent of the microprocessor—is no longer unique to aerospace, military, and costly industrial applications. More and more utilization is taking place in situations where the general public can benefit from the automated procedures without ever knowing—or caring—that a computer is involved. People now not only accept the benefits, they expect them.

One example is an automated component scoring system developed by AMF Inc, Stamford, Conn under the guidance of Dr Reg A. Kaenel, Electronics Member Corporate Technical Staff. Experimental, automatic scoring systems are not new and preceded the availability of microprocessors. However, they have been too cumbersome and expensive to be readily accepted. Now, AMF's MagicScore, claimed to be the first fully automatic scoring system, takes advantage of the small space and low cost benefits of large scale integration (LSI) technology to overcome those handicaps. The system is fully controlled by a Motorola 6800 microprocessor and is totally dependent on associated LSI circuitry. A second 6800 microprocessor in an "acoustical pinsensing unit" receives signals from transducers, decodes and processes the data, and forwards the translated information to a scorer unit for pinfall display.

### Automated Scoring System

Both automatic pinsetters and automated scorers were introduced to the public in 1946, and human pinsetters disappeared almost completely in the ensuing 30 years, but many bowlers still mark their scores on paper or translucent sheets with grease pencils. Automated scoring systems from several manufacturers are, however, steadily supplanting the older, manual systems as new alleys are built or old ones remodeled.

Despite the common temporary reluctance to accept automation, "to be controlled by a computer," the automated scoring systems have been favorably received for several very basic reasons: they eliminate the need to perform even simple arithmetic and the possibility of arguments over supposed errors, they minimize the need for one player to concentrate on scoring and therefore miss some of the important socializing, and they permit all players to be fully involved in the game.

Key unit in the MagicScore system is the player console (Fig. 1). Before the game begins, the scorekeeper defines certain data by pressing keys (Fig. 2) on the keyboard, eg, names of players in bowling sequence, team names, handicaps, and mode of play. As each name is entered, it is displayed in full at the bottom of one of the 17-in. CRT screens and that player's initials automatically appear in the identifying boxes to the left of the proper screen.

When the system is operating in fully automatic mode, players are cued in the order they should bowl by a full name display at the bottom line of the screen in the laneside they should bowl (Fig. 3) and by flashing arrows in the pertinent box alongside the player's initials. After the button is pressed for a player, the scorer does the rest, determining scores from data supplied by the pinsensor and automatically displaying totals. (In manual mode the players must touch keyboard buttons to indicate pinfall.)

Each ball rolled is automatically recorded and games are computed based on the number of frames. This information is displayed on the CRT for each lane next to the game and frame symbols (G and F). The score for each of the two balls in a player's frame is shown separately; eg, in frame 3 of Fig. 3 player "FLG" knocked down seven pins on the first ball and two on the second. Common symbols are used, such as X for strike and / for spare. Subtotals are not indicated for each frame, but a running subtotal for all frames is maintained in the "TOT" column. Instead of the two CRTs on the player's console, 23-in. remote CRT monitors may be included in some installations. These would be located above the console at their respective lanes.

Corrections are made by pressing the "Correct" key on the keyboard for the proper lane. When the cursor (half-frame wide) appears, it is moved to the proper half-box position by pressing buttons marked with arrows for left, right, up, and down. Then the player touches the button indicating the correct pinfall. The corrected pinfall is shown as a smaller number with a line under it, indicating that a correction has been made. Individual and team scores are automatically updated.

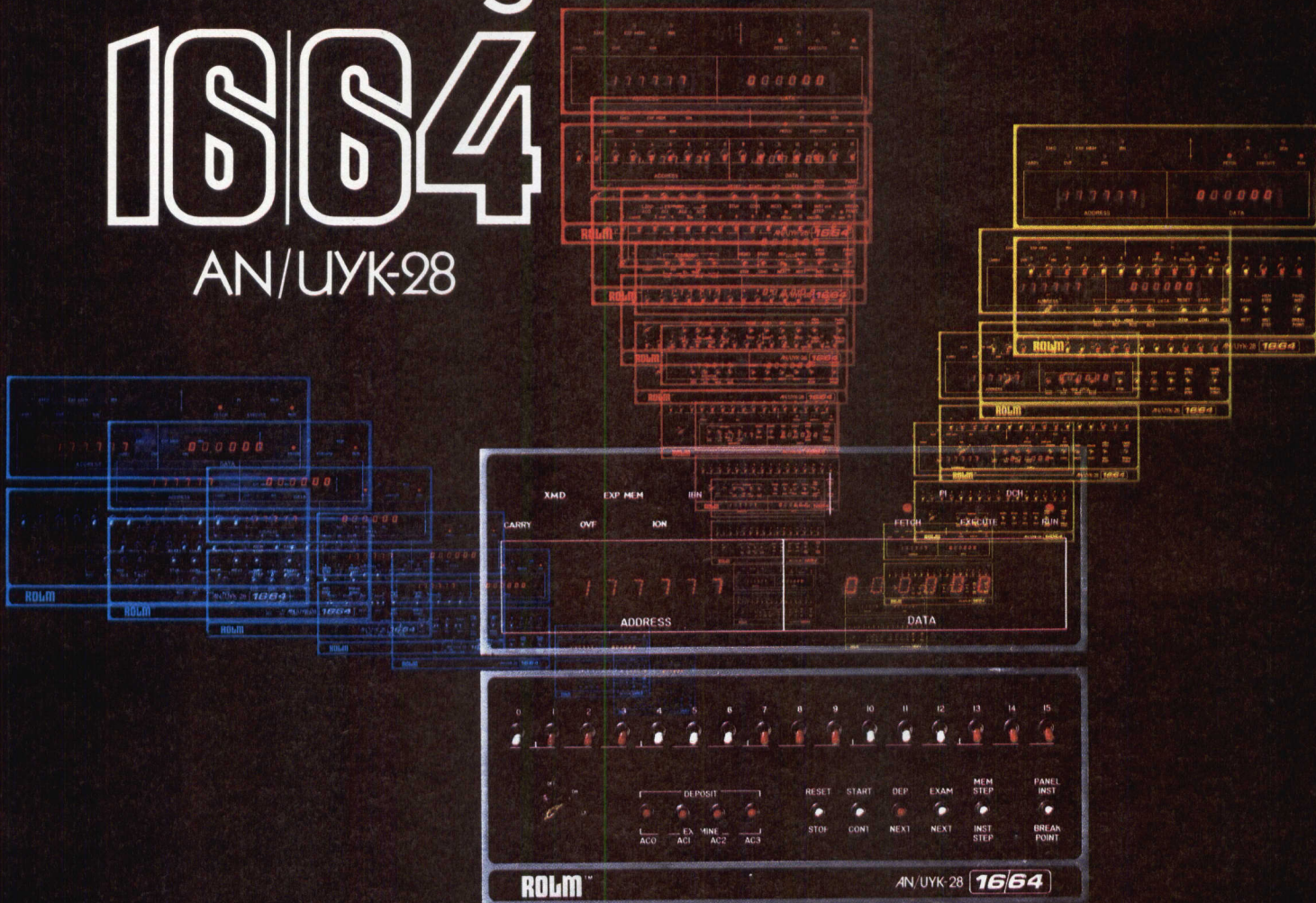
Two PC boards mounted behind the keyboards on the front panel contain the controlling electronics



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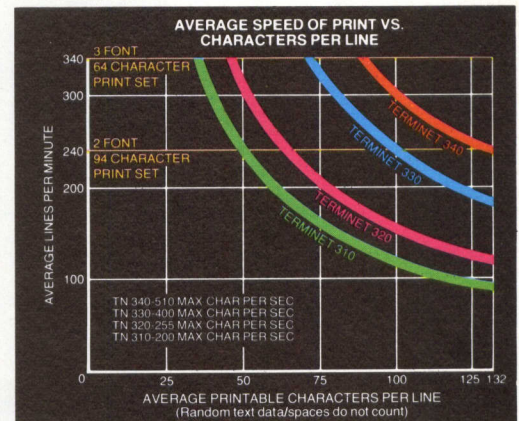
rear loading. 132 columns. Original and 5 copies. A unique ribbon cartridge. With a life span of 50 million print characters. Operators can replace in less than a minute. Easily. Cleanly.

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GENERAL  ELECTRIC



# DIGITAL CONTROL AND AUTOMATION SYSTEMS

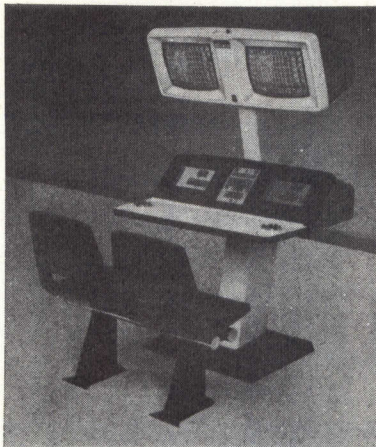


Fig. 1 Player console for AMF's MagicScore automated scoring system. CRTs, one for each lane controlled by a console, may alternately be mounted at a remote position above the lanes

(Figs. 4 and 5). An MPU board on the right contains 6800 microprocessor, three peripheral interface adapters (PIAs), asynchronous communications interface adapter (ACIA), and five 16K-bit read-only memories (ROMs) which store control software. All are Motorola Semiconductor products. (ROMs are configured as 2K words x 8 bits.) A 6-position DIP switch array permits assignment of a unique address for each scorer which is used to recognize messages. On the left of Fig. 4 is the video display board containing 1K bytes of random-access memory (RAM) in the eight devices at bottom left. The front panel is hinged to permit easy access to PC boards, printer, and other electronic components.

A PC board mounted on top of the thermal printer (Fig. 6) contains printer drive electronics. The printer itself, included in the system to provide a hardcopy printout at the end of a game, has only one moving part—a timing motor used as a stepping motor to advance the paper. In addition to including information displayed on each CRT, the hardcopy also has subtotals for each frame.

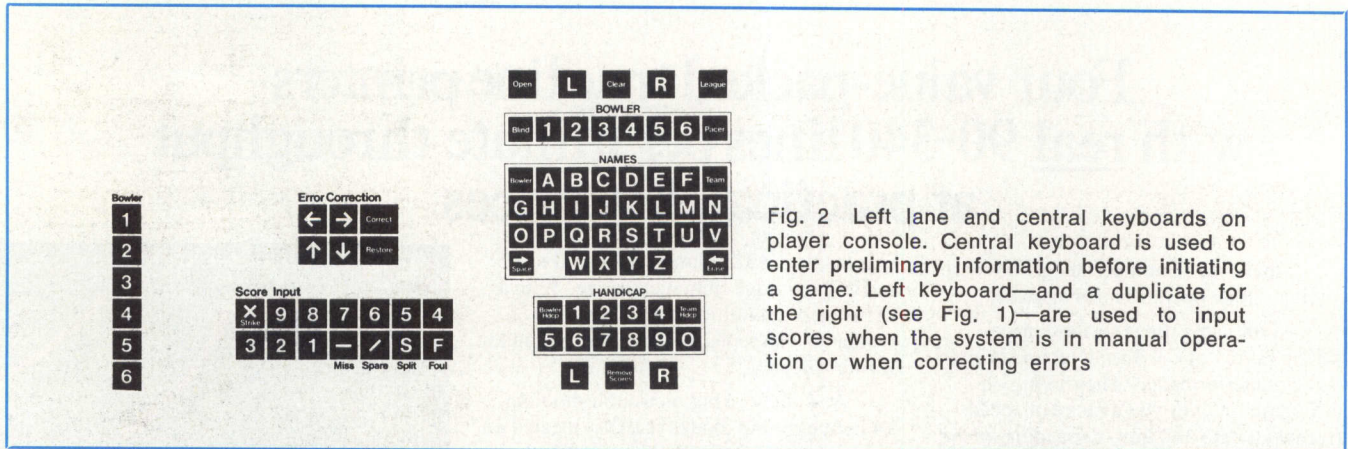


Fig. 2 Left lane and central keyboards on player console. Central keyboard is used to enter preliminary information before initiating a game. Left keyboard—the right (see Fig. 1)—are used to input scores when the system is in manual operation or when correcting errors

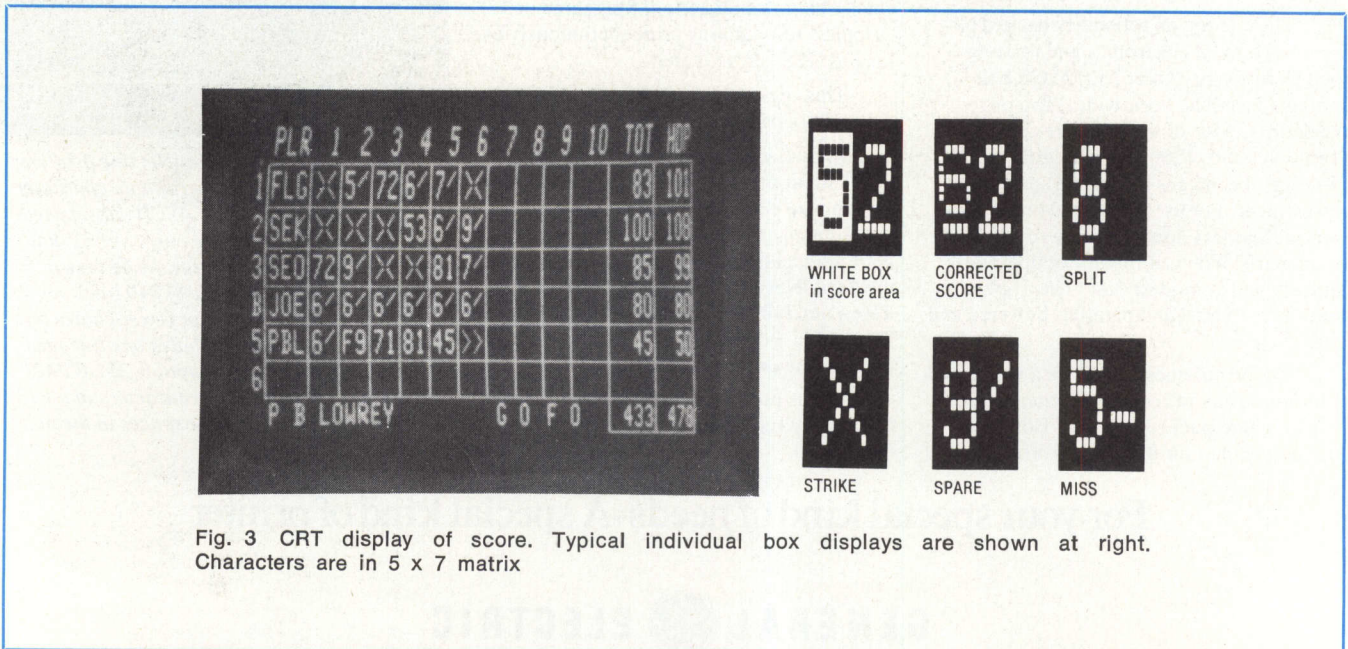
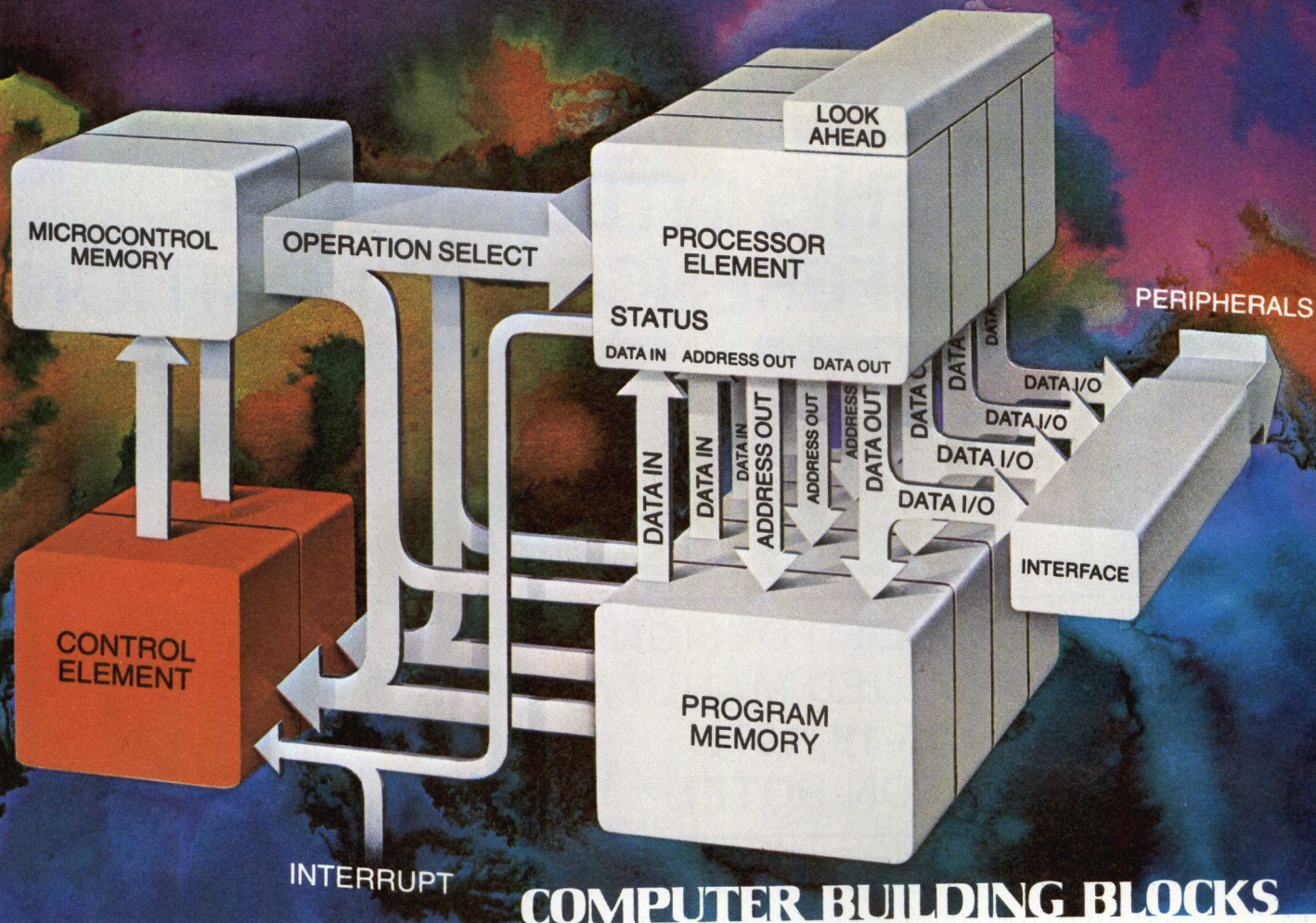


Fig. 3 CRT display of score. Typical individual box displays are shown at right. Characters are in 5 x 7 matrix



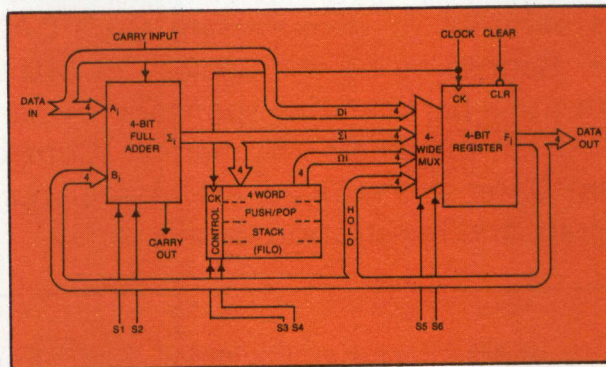


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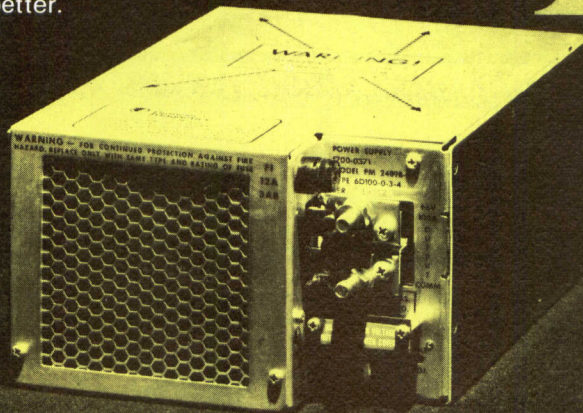
MODEL	PM2408		PM2486		PM2478		PM2480		PM2462	
	500W		600W		800W		1500W		2000W	
	Volts	Amps	Volts	Amps	Volts	Amps	Volts	Amps	Volts	Amps
CHANNEL 1	5	50	5	75	5	100	5	200	5	200
CHANNEL 2	15	10	15	10	15	15	15	15	2	200
CHANNEL 3	15	5	15	5	15	5	15	15	15	15
CHANNEL 4	See Mfr.		See Mfr.		See Mfr.		See Mfr.		15	15

#### SINGLE OUTPUT SUPPLIES

MODEL	PM2496	PM2497	PM2498
OUTPUT VOLTS	OUTPUT AMPS	OUTPUT AMPS	OUTPUT AMPS
2	100	200	400
3	60	100	300
5	50	100	200
5	—	150	300
12	23	60	120
15	20	50	100
18	17	45	90
21	14	38	76
24	13	33	66
SIZE (inches)	5x8x11	5x8x11	5x16x11



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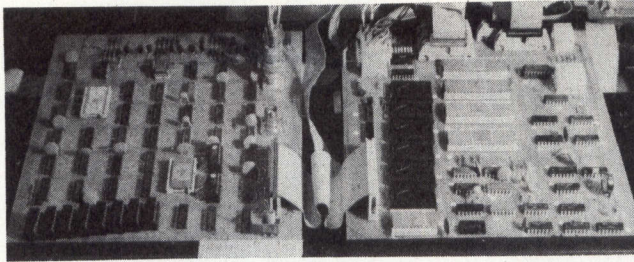


Fig. 4 Video display and MPU boards, located behind hinged front panel of player console. Video display board contains eight RAM DIPs totaling 1K bytes; MPU board contains 6800 microprocessor, three peripheral interface adapters, an asynchronous communications interface adapter, and 10K bytes of ROM in 16K-bit devices

Characters on the CRTs are formed in a 5 x 7 matrix (Fig. 3) with a non-interlaced horizontal raster scan with the same pattern of dots appearing on adjacent pairs of scan lines. The printer, however, forms characters in a 5 x 5 dot matrix and contains extra print-head dot elements to form grid lines on the hardcopy.

Half of all RAM is used for display; the other half provides temporary storage (scrtachpad for various programs). A chopper on the video display board allows the other half to be displayed for diagnostic purposes.

A rechargeable standby battery keeps RAM alive if power is lost. Pinfall data are preserved up to 12 hours. If the system includes an available emergency power unit, the bowler can obtain a printout of the

incomplete game for a record in the event power is off more than 12 hours (a requirement of the American Bowling Congress for any automated scoring system).

Each installation can include a manager console, located at a central spot, that can monitor, control, and communicate with up to 98 lanes. Currently this unit contains 8K bytes of ROM, but as further capabilities are added the total may be increased to 10K.

Most of the program in this ROM is used for provisions against failure of the overall scoring system or to check on activities at various lanes. The manager can also page bowlers or relay messages to the player console, obtain a video display of the scores from any lane, and control visual display of advertising messages. Among the functions that can be called into operation are "list lanes powered," "list lanes in open play," "remove score," "prevent remove score," and "list lanes with no score input for three minutes." The last function, for example, allows the manager to determine if there are any lanes where problems potentially exist—since no scores are being input to those lanes.

By pressing buttons on this keyboard, the manager can activate a RAM location at the player console and interrogate it. This is accomplished through the ACIA (Fig. 5) on the MPU board to the RAM on the video display board.

#### Ultrasonic Pinsensor

Acoustics and ultrasonics are well-known sciences. This is especially true of acoustics, since as an applied science or technology its characteristics are quite thoroughly understood, particularly in air. Ultrasonics as a technology is considerably newer but is usually related to liquids—eg, undersea detection or immersible cleaning devices. When combined with a microprocessor for detection of objects through the medium

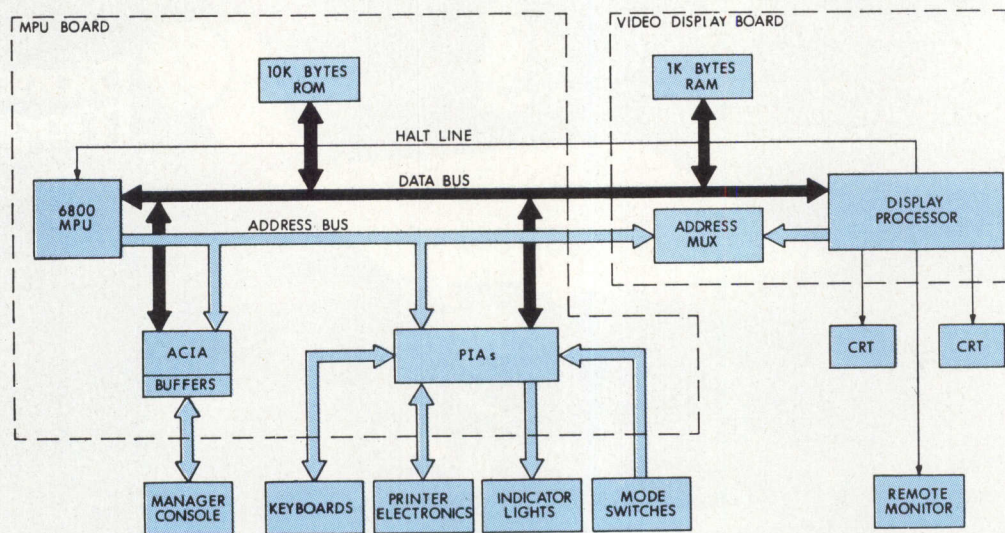
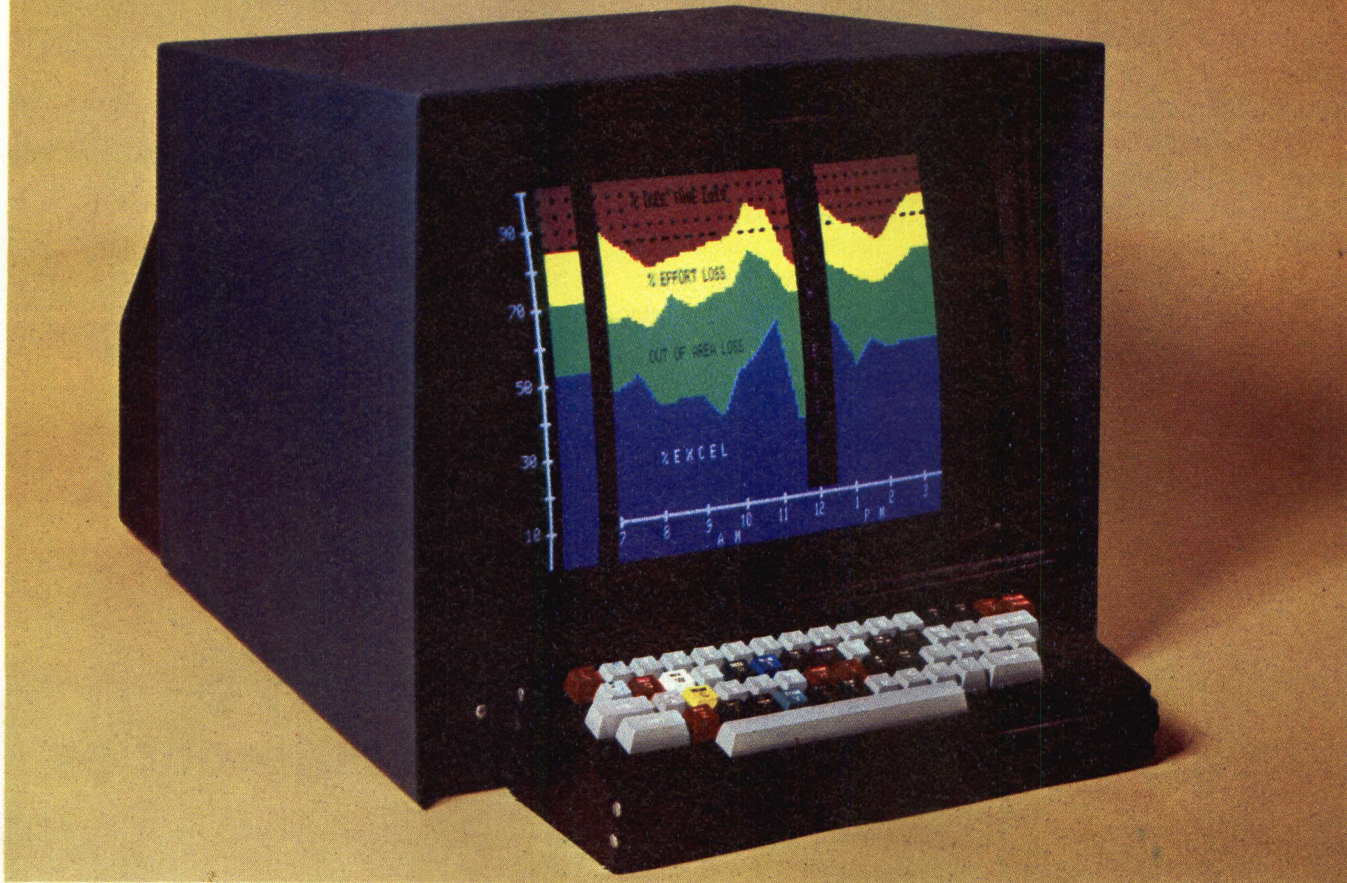


Fig. 5 Simplified block diagram of scorer logic. Manager console can interrogate program in RAM via ACIA. MPU controls both boards and remainder of devices associated with system except pinsensor



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of air—to sense and count bowling pins—the application likely becomes unique.

Located above the kickback plates at the end of the alley, entirely out of sight of the bowlers, is an "acoustical pinsensing unit," probably the first use of air ultrasonics for a commercial installation. Specific details cannot be provided at this time because of patent rights involved, but Dr Kaenel said that detection occurs when pulses from arrays of high efficiency transducers on either side of the alley reflect from standing pins.

Although there are some "blind" areas for each array, those areas are covered by the opposite array. In reality, the beams from the transducers are overlapped significantly to avoid tolerance problems. However, a procedure has been conceived that creates the appearance of non-overlapping beams. A microprocessor in this unit, again a Motorola 6800, queries transducer preamplifiers located near each transducer array and causes each of the transducers in turn to emit a sonic pulse. Amplified return signals are multiplexed on a common bus to the processor.

The MPU massages the data to locate peaks. Essentially, a count of those peaks is equal to the number of pins that are standing. This information is forwarded via a 2-conductor cable to the player console. That MPU-based system then displays the pinfall, and automatically determines individual score and team totals.

### Software

As described in a paper presented by Dr Kaenel\* at the 1976 NCC, the scorer software provides for processing score data from the keyboard, the pinsensor, and the manager console. During program execution, the scorer microprocessor deposits data in RAM and retrieves such data when needed. The display processor electronics also fetches data from RAM and processes it for display.

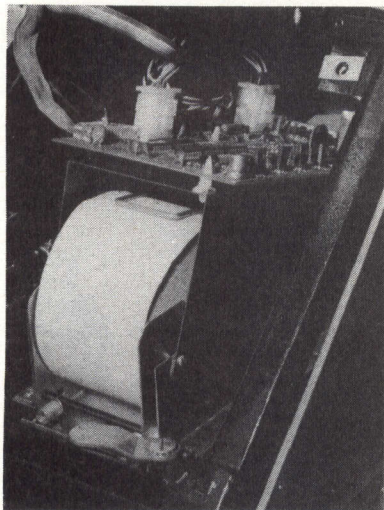


Fig. 6 Thermal printer, located in player console. Special printhead produces 5 x 5 dot matrix characters; extra dot elements produce grid lines for hardcopy printout

Each row of display characters is made up from 28 scan lines. A complete line of display characters from both display sides is transferred from RAM into a recirculating shift register during the first two scan lines of each character row, and recirculates there for the full duration of this row. Characters of the left screen are located at even RAM addresses, those of the right screen at odd addresses; points to the left and right side display characters are similarly interspersed in that shift register. A character column counter identifies the column number of the character that is being scanned by the CRT beam. It also designates left side data from the RAM during the top scan line of each character row and right side data during the second scan line.

As the character count is advanced, a character ROM converts the left side character into a suitable 7-dot pattern which is stored in the left side buffer shift register. The same process is immediately repeated for the right side characters, and these dots are serialized and output to the respective display monitors. A state ROM defines the width of each character, the presence of a horizontal grid line, and the presence of a horizontal synchronization signal.

### In Retrospect

Since no product is really viable unless it is both reliable and priced at a level that is reasonable for what it provides, this scoring system could not have been designed in its present form if low cost, dependable components had not become available when needed. Key component is the 8-bit 6800 microprocessor. When the overall system design was initiated, this MPU was available only in sample quantities; by the time the pinsensor unit was designed, the MPU was an off-the-shelf item.

However, even the availability of a reliable, low cost MPU did not solve all problems. Dr Kaenel stresses that the development of individual portions of the system as well as the overall system really depended very much on tools, in particular analyzers such as the EXORCISER.<sup>TM</sup> If various types of analyzers had not become available at the times they were required, debugging would likely have added prohibitive costs.

Other system components were also important to reliability and price. Particularly notable are developments of a low cost thermal printer, a low cost tactile-feel keyboard, and the transducers for the air ultrasonic pinsensor.

Many of the items incorporated in the automated scoring system were designed and developed specifically for the system. The player console and the pinsensor were developed by Motorola Semiconductor Products Div, Phoenix, Ariz, with production accomplished by Motorola Display Products of Carol Stream, Ill and Rectec, Inc of Fairfield, Conn, respectively. Rectec also designed the thermal printer, using a special printhead designed by Gulston Industries Inc, Electronic Components Div, Metuchen, NJ. Keyboards were developed jointly by Motorola Semiconductor and Texas

\*R. A. Kaenel, "MagicScore Bowling Scorer—A Microprocessor Application for Fun and Profit," *Proceedings of the 1976 National Computer Conference*, pp 341-347.



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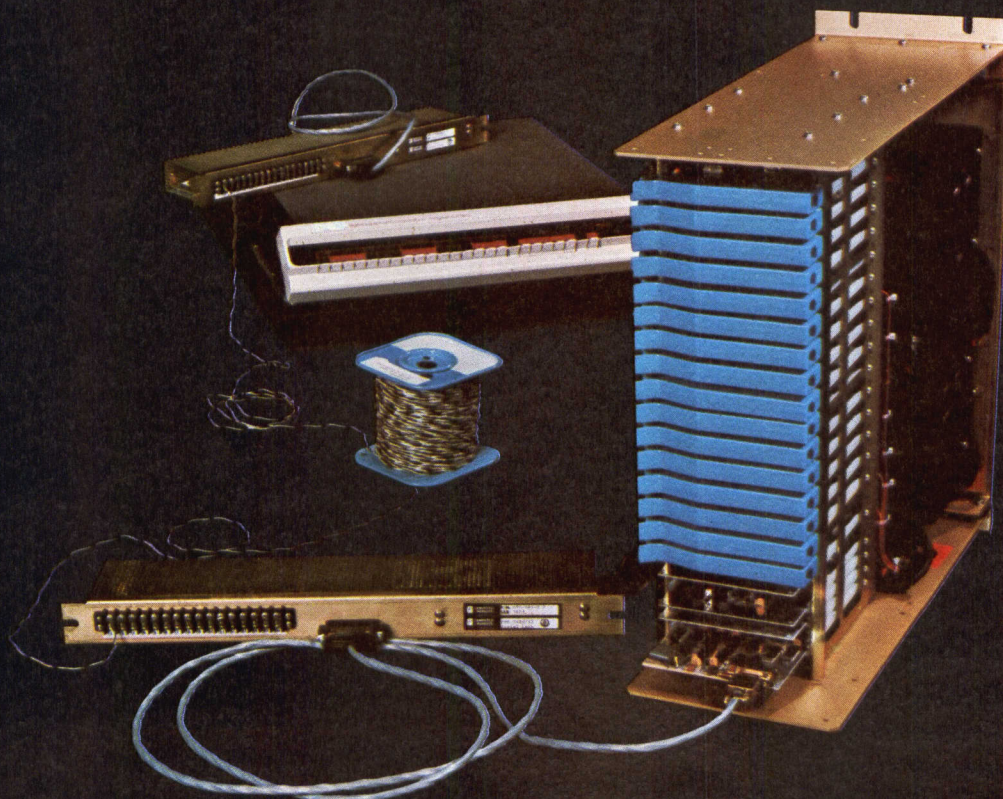
and multi-drop stations, try Procom I, our microprocessor-based communications controller.

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**Computer Products, inc.**



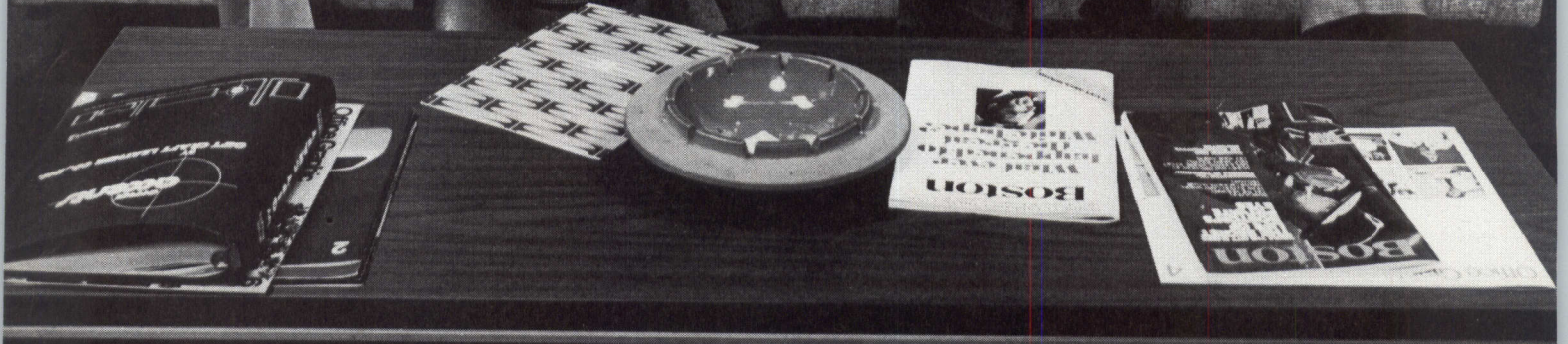
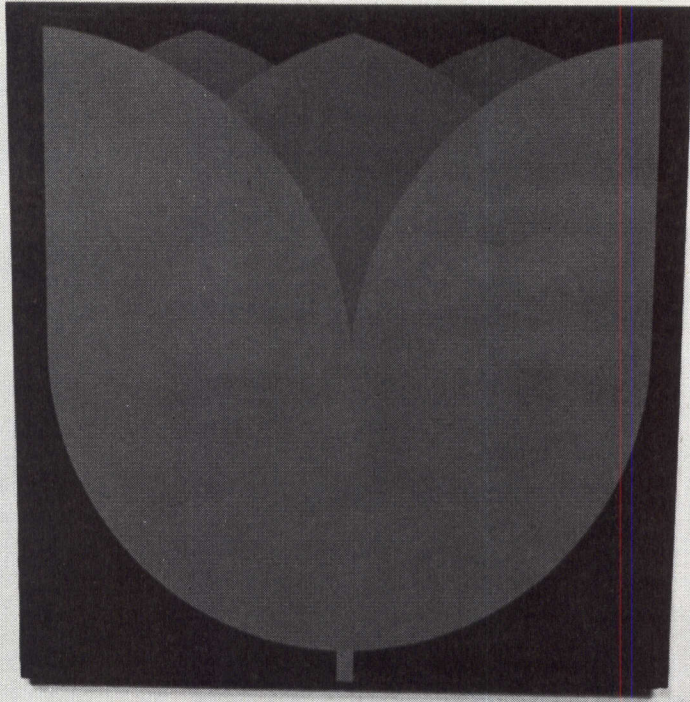
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CIRCLE 32 ON INQUIRY CARD







# Five tough questions to ask our 8080A competitors.

1. Do you have an 8K Electrically Erasable PROM? You know, like NEC Microcomputer's  $\mu$ PD458 that's compatible with 2708's but can be erased in 1 minute, programmed in 80 seconds, only needs two voltages for reading and programming, has conventional retention time of 10 years, and an access time of 450/650ns, making it the first practical non-volatile RAM storage.

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4. Do you have a Floppy Disk

Controller? You know, like NEC's  $\mu$ PD372 that can control up to four IBM 3740-compatible drives.

5. Do you have a Tape Cassette Controller? You know, like NEC's  $\mu$ PD371 that can control up to two cassette drives with International Standard Data Format.

Go ahead, ask any competitor you like. What you'll find is that if you want these super 8080A peripherals, you'll simply have to come to NEC.

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 $\mu$ PD2308  
 $\mu$ PD369  
 $\mu$ PD758

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 $\mu$ PB8224

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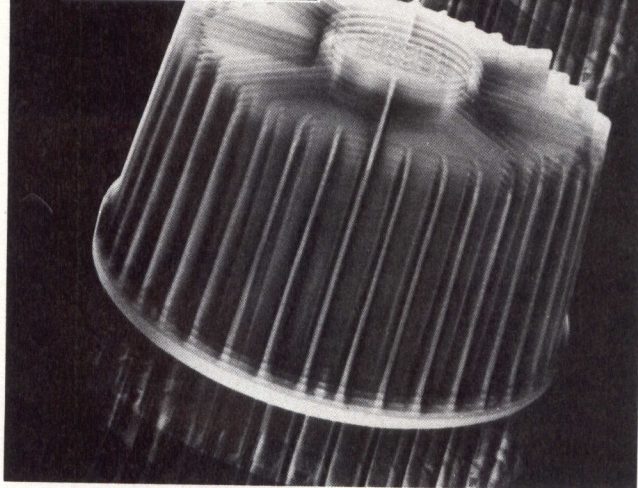
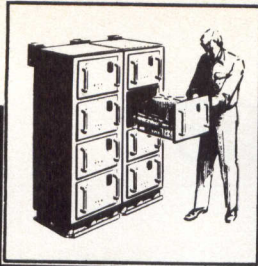
$\mu$ PD8255

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1.25 MHz MPU  
2.5 MHz MPU  
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1K STATIC RAM  
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1K STATIC RAM  
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■ If your ADP installation shakes, rattles, rolls, sweats or freezes, Librascope's Series L107 fixed head per track disc memories should be there. Fully militarized, the L107s meet the specifications of Mil-E-16400 and Mil-E-5400, including Mil-S-901C, the drop hammer shock test.

■ Series L107 disc memories have been purchased for 11 major ongoing military programs in the United States and four in other countries. Successful installations include shipboard, transportable hut, van and aircraft.

■ The illustrated multi-disc system provides 8 million words of fast access storage. Modular construction permits complete freedom of installation layout since units can be placed where space is available, as in locations very remote from the central processor.

■ Interface is provided for computers such as the AN/UYK 7, 15 and 20 with NTDS fast I/O, as well as for the Rolm militarized computers.

■ For complete information call (213) 245-8711 or write to Librascope Division of The Singer Company, 833 Sonora Avenue, Glendale, California 91201.



**SINGER**  
LIBRASCOPE DIVISION

## DIGITAL CONTROL AND AUTOMATION SYSTEMS

Instruments Inc, Attleboro, Mass; and Massa Corp of Hingham, Mass developed the critical air transducers.

MagicScore systems without the ultrasonic pinsensor have been in use for over a year in bowling alleys all over the country. The first ultrasonic pinsensor unit is now installed and being tested in Shelby, Ohio. At the completion of a satisfactory test period it will be submitted to the American Bowling Congress for approval, a necessity for any automatic scoring system. Circle 160 on Inquiry Card

## DC&AS BRIEF

### Simplified System Eases Multi-Loop Process Control Interface

According to the manufacturer, the modular 7000-M universal computer interface offers easier, lower cost field installation for process control systems. Bailey Meter Co, a subsidiary of Babcock & Wilcox, Wickliffe, Ohio, says that the heart of its pre-engineered system is a line of multi-circuited modular termination units which simplify and consolidate all system interconnections in standard modular termination cabinets. A comprehensive fill-in-the-blanks documentation package simplifies system specification, design, and scheduling for the customer.

With this concept, up to 70% of the system can be completed during the initial engineering phase. Manufacture of system cabinets requires only a few general decisions and an approximate instrument count. Input-output cabinets can be shipped to the job site for complete field wiring in advance of final console decisions. Standard mounting shelves and universal 19-conductor plug-in instrument cables offer complete flexibility for instrument locations, permitting the operator's console to be interconnected by plug-in cables later.

The system is suited for medium to large applications involving 50 or more control and measurement loops. Typically, systems of this size benefit substantially from reducible installation costs, more effective schedule control, improved customer/vendor communication, and the ability to easily accommodate control changes and additions. Documentation package consists of design configurator sheets, external connection drawings, loop schematic drawings, computer interfacing data sheets, dimension drawings, and a project schedule guide. All are standard documents for completion by manufacturer and customer, arranged in a coordinated format to simplify engineering, scheduling, and detailed design of the system.

Control room space requirements are claimed to be 20% less than for conventional system wiring cabinets. Front access design of the assemblies allows the 18" deep cabinets to be mounted against a wall (eliminating a rear aisle). □




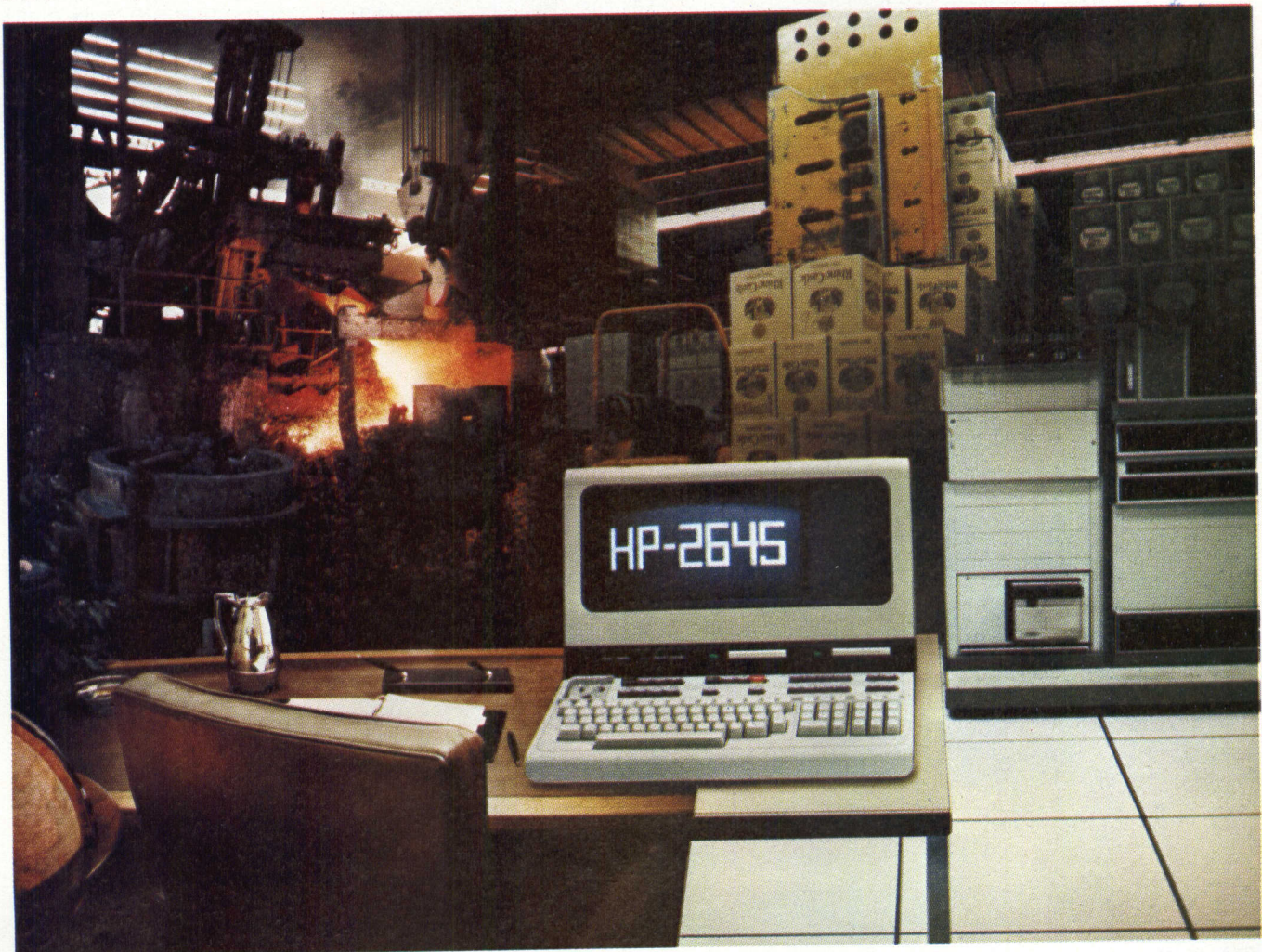
**HEWLETT-PACKARD****COMPUTER ADVANCES**

Fast, flexible and efficient—the HP 2645 is a powerful addition to Hewlett-Packard's growing family of multipurpose display terminals. With extensive features, the HP 2645 was designed to adapt to a diversity of application requirements. The microprogrammed HP 2645 offers simplicity of operation through user defined Soft Keys that match the keyboard to the application.

**HEWLETT-PACKARD  
ANNOUNCES THE 2645**

Up to 12 kilobytes of display memory "stretch" the display to fit the application. Added Mini Cartridge mass storage for off-line operation decreases the application's dependence on the com-

puter. Flexibility in data communication, speeds up to 9600 bits per second and polling (async. and sync.) facilitate "hardware fitting" an application. Forms drawing capability, field checking, adjustable margins and full editing make the HP 2645 perfect for data handling applications. The HP 2645 is simple to use; yet adept with complex applications. 

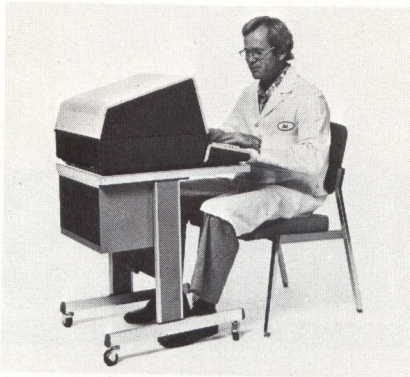


**A DISPLAY STATION WITH CAPABILITIES  
AS DIVERSE AS YOUR COMPANY'S REQUIREMENTS.**



# THE HP 2645 DISPLAY STATION

A company wide information link to plant, warehouse, computer center, and sales offices.

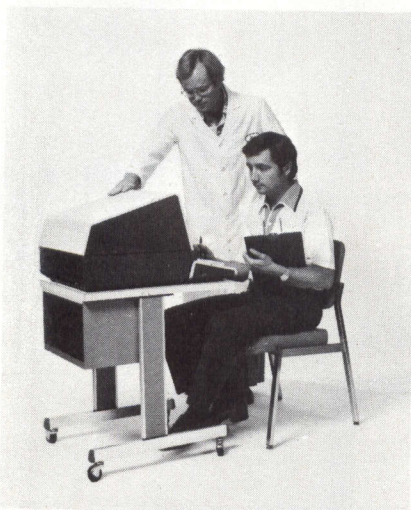


**Job management improves with HP 2645's daisy chained throughout the manufacturing plant.**

Imagine a hypothetical manufacturing plant . . . To solve the problem of locating, expediting and reporting the status of production jobs in process, a number of HP 2645's are placed strategically around the factory. At a terminal, production workers simply enter jobs as they begin them and log them off when they are finished. For those unfamiliar with computers, the terminal's Soft Keys simplify data entry and reduce errors.

Soft Keys are a Hewlett-Packard innovation which shorten data input time and ease interaction with the computer. Each of the HP 2645's eight Soft Keys can be user defined to issue up to 80 characters or to execute several control sequences with only a single keystroke.

With the HP 2645's polling capability, as many as 32 terminals can be spread at distances of several thousand feet and can share a single line and computer I/O port. The results are minimum network costs, fewer wiring tangles and convenient job control.



**Inventory control tightens with a remote HP 2645 and inventory transactions stored locally on internal mini cartridges.**

At warehouses several miles from the main plant, tighter inventory control results from use of the HP 2645's powerful stand alone capabilities made possible by optional internal mass storage on two magnetic tape Mini Cartridges. Personnel enter transactions onto forms displayed on the 2645's screen. One cartridge stores the new inventory entries for periodic batch transmission to the computer. The second cartridge receives and stores both the forms and the updated inventory. Here, the HP 2645 reduces paperwork and its costs, minimizes charges for telephone lines and computer connect time, and also assures a duplicate inventory record separate from the central computer.



**Programming is fast and simple with an on-line HP 2645 in the operations center.**

Programmers find that the HP 2645's line drawing capability simplifies their preparation of display forms that look like those printed forms company people already are familiar with and accustomed to using. Soft Keys, when programmed to automatically enter multiple keystroke sequences, shorten the time necessary to input repetitive subroutines. Altering programs is a snap with the terminal's many editing features, such as insertion, deletion, writeover and adjustable margins for multiple columns.



**Secretarial efficiency improves with a stand alone HP 2645 and printer.**


Secretarial efficiency improves by using the HP 2645 with a printer in a stand alone combination to retype original form letters and to revise drafts of text. The HP 2645 displays upper or lower case letters, tabulates and backspaces. An executive secretary types management memoranda onto cartridges for later transmission to terminals throughout the company.



**Communications costs and order entry errors decrease with HP 2645's in distant sales offices.**


Field sales offices dramatically reduce line charges by using HP 2645's. Whereas before, each terminal needed its own leased line, daisy chained HP 2645's clustered in a single office share a common modem, and single communication line. With the choice of asynchronous or synchronous (Bisync) modes of operation, the sales office has chosen synchronous (Bisync) to gain the speed of 9600 baud remote transmission. Order errors diminish with the terminal's field



checking capability (fields are the blanks in displayed forms.) Alpha/numeric field checking, for instance, prevents entering numbers where letters go and vice versa. The high speed cursor, showing where the next entry will go, simply passes over a protected field (one containing the order heading, for example) and goes to the next open blank. Page scrolling for lengthy forms and full edit features help prepare, correct and change orders before transmission. 

## THE HP 2645 DISPLAY STATION

The 2645 is a high resolution display station that operates at up to 9600 baud and offers async, point-to-point data communications. Optional capabilities include both async. and sync. (Bisync) polling for multi-point communications. Internal mass storage extends the 2645's capabilities. User defined Soft Keys allow the keyboard to adapt to specialized applications. Forms mode and full editing capability round out the data entry characteristics of the 2645.

For more information describing the HP 2645's extensive features, indicate A on the reply card. 

# INNOVATIONS IN DATA COMMUNICATIONS

Detecting the Undetectable: New Insight Speeds Network Setup & Debugging.


The HP 2640, the first display terminal introduced by Hewlett-Packard, began a tradition. The pressing of a single key initiates a Self-Test and instantly verifies that the HP 2640 terminal is working properly. The newest of the family, the HP 2645 Display Station continues this Self-Test tradition and adds a new concept—Monitor/Driver Mode.

When a problem appears in a data communication network, the list of possible malfunctions is long. Perhaps the modem is faulty, or maybe there is transmission interference on the telephone lines. But then . . . it could be a problem with the computer itself. Or the fault could reside in any of a number of plugs, cables and connectors. The Self-Test feature helps clear the confusion and isolate the fault so that immediate corrective action can be taken.

The Self-Test feature is a firmware program that assures that the HP 2645 is working. It checks the HP 2645's power supply, ROM and RAM memory, microprocessor, data communications interface, etc., and displays the results in a complete test pattern. Self-Test can also capitalize on the analog and digital loop back capability of modems. The HP 2645 sends out 128 different characters which upon reaching a modem or special Self-Test

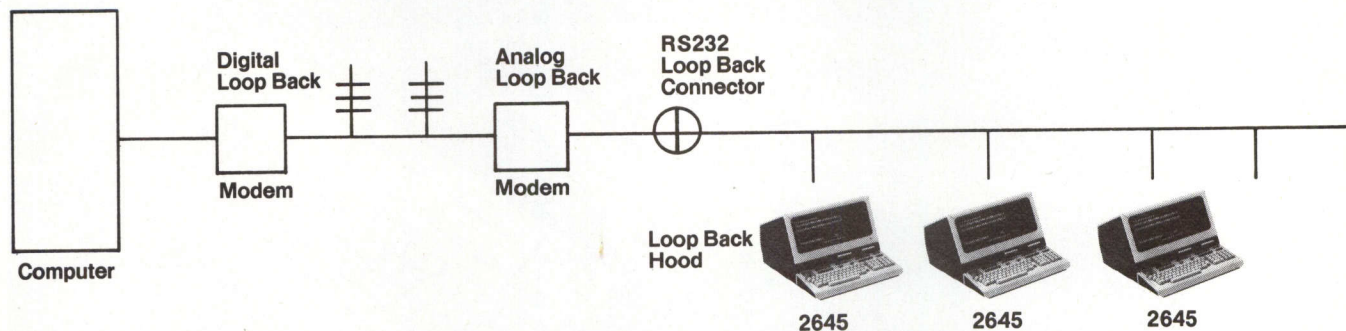
Plug are looped back to the terminal. A simple comparison indicates if a problem exists in the part of the network under test. Full documentation, including flow charts, assists a user to systematically "Self-Test" in tracking down problems.

To help further isolate problems in the communication network, the HP 2645 has an optional feature called Monitor/Driver Mode which is used in a polling environment. In Monitor Mode, a daisy chained terminal actually allows the user to view data being transmitted because the HP 2645 displays the data as it passes by. This "insight" helps analyze and determine which terminal sent data out of sequence, prematurely, or not at all. In addition, Driver Mode allows one terminal to generate typical polling and selection sequences for other terminals on the same communications line, a handy debugging tool for really tricky problems. Data transfer is a dynamic process and has been difficult, until now, to capture in a single transmission snapshot. Once flowing data can actually be seen on the display, problems are easier to see and simpler to resolve.

Monitor/Driver Mode plus Self-Test speed debugging a system and help get an on-line system quickly on the air. What was previously mystery is now detectable. 

## ISOLATE HARDWARE PROBLEMS

Self-Test feature permits fast hardware fault isolation in a communication network. Faults can be easily isolated by looping back data from any of four logical points.



## SEE LOGICAL PROBLEMS

With Monitor/Mode's "insight," dynamic data transfers from both the computer and terminal can be seen and analyzed.

For more information on the HP 2645 data communication's innovations indicate B on your reply card.



# NEW: HEWLETT-PACKARD COMPONENTS

Help OEM's maximize value added opportunities.

In a major extension of its OEM line, HP is introducing two products in component form: the HP 2649 terminal and 21MX-K Series Minicomputer. Developed for the OEM designer who needs greater flexibility, both products consist of hardware subassemblies that can be ordered in the most cost-effective configuration for a particular application. Both permit functional customization through microprogramming.

Comprehensive documentation is available for both products so that technically oriented users can take full advantage of the products' flexibility. These products broaden HP's OEM product line to range from components, terminals and other peripherals through minicomputers, discomputers and the new HP 3000 Series II general purpose computer system.

## Now: a way to get a custom terminal without paying a custom price.

With HP's new 2649 Mainframe Terminal, designers can create a variety of specialized terminals from multiple hardware building blocks—all controlled by custom, proprietary firmware without costs associated with developing a specialized terminal from scratch.

All information needed to develop source code for custom firmware is available in a technical support package. Object code can be assembled on an HP RTE Minicomputer system using a 13290 Development Terminal as the system console and a firmware support package.

With the 13290 Development Terminal, object code can be loaded from Mini Cartridges to 24K bytes of Writable Control Store (WCS) for verification of user-developed programs.

Once developed and debugged, custom firmware coding can be easily transferred to programmable-read-only-memory (PROM) chips for installation in multiple HP 2649 Mainframe Terminals. For high-volume applications, read-only-memory (ROM) chips are available from specified vendors.

Technical assistance in developing custom firmware is available directly from Hewlett-Packard. Among other services, HP will offer a series of in-depth "how to do it" seminars for customers wishing to get the most out of the new HP 2649 Mainframe Terminal.

Hardware options for the terminal include two keyboards, four character sets and fonts, six memory modules, four data communications modules and two I/O modules. A display enhancement module and two



HP's new 2649 Mainframe Terminal offers an easy way to develop specialized display stations for specific system applications. Multiple hardware options are available and custom firmware can be used to redefine the Terminal's operating characteristics. Minimum contract quantity is 20 units; OEM and Volume End User discounts are available.



printer subsystems are also available.

For more information on the easy way to create specialized terminals for your next systems application, indicate C on the attached reply card.

**Now: microprogrammable computer power in component form.**

For the OEM designer who needs the power of a minicomputer and the flexibility of a microprocessor in his next system, HP has a new and intriguing product: 21MX K-Series Minicomputer Components.

Designed to fill the need for high-power processing in a low-cost form that integrates easily into OEM systems, K-Series Components offer unique flexibility through microprogramming. Systems engineers can now gain direct access to an extraordinarily fast processor which features a 325 nano-second cycle time and 210 powerful microinstructions. And, by adding a 21MX read-only-memory (ROM), get a full minicomputer that is hardware- and software-compatible with HP's entire line of 21MX memory systems, software, peripherals and accessories.

In any systems design, K-Series

Components provide:

- A high-performance "computer-on-a-board" that can run up to five times faster than MOS/LSI microprocessors and support large amounts of memory for complex tasks like array processing or pattern recognition.
- Access to a full set of microprogramming tools which let OEM designers develop custom firmware for high-speed execution of specialized routines.
- A choice of easy-to-install components that can be hidden in an OEM system and operated through a custom front panel.
- The opportunity to maximize added value while taking advantage of 21MX-compatible software.


Among the many systems applications which can use the speed and power of K-Series Components are spectrophotometers, numerical control units, smart data-entry terminals, word processing equipment, graphic display systems, medical diagnostic systems, and many kinds of test equipment.

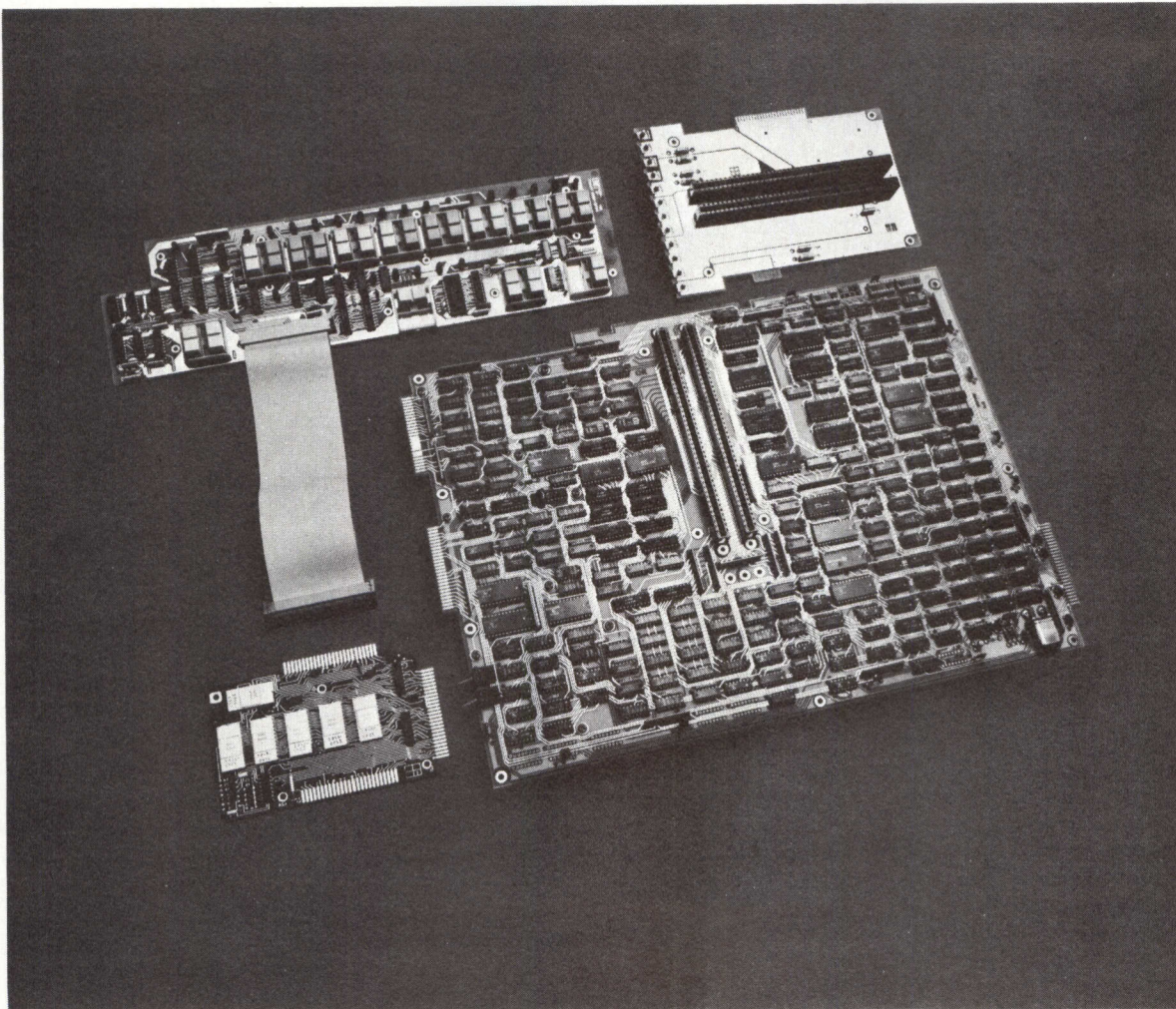
K-Series Components include the processor board, 21MX Instruction

ROM, a front panel assembly and card cages with either eight or 18 slots for memory and I/O cards. Accessories include all 21MX memory systems, Writable Control and User Control Store boards for storage of microprograms, a Dynamic Mapping System which permits addressing of up to 256k words of memory, a Dual Channel Port Controller, a fast FORTRAN processor and a Memory Protect System.

A wide selection of I/O subsystems is also available for use with K-Series Components. These include the HP-IB\* I/O Kit which simplifies configuration of automated test/measurement systems by allowing the computer to control multiple cluster of up to 14 compatible instruments each.

In short, HP's new K-Series Components offer unusual design flexibility at a very attractive price. U.S. prices for the processor board (OEM quantity 100) are \$975 without and \$1205 with the 21MX Instruction ROM.

For more information about HP's latest addition to the 21MX Minicomputer family, indicate D on the attached reply card. 



**HP's new K-Series Minicomputer Components offer the speed, power and flexibility of 21MX Minicomputers in a form that integrates easily into OEM systems. The high-speed processor-on-a-board can be used with custom firmware and with a 21MX Instruction ROM as a full, microprogrammable minicomputer.**

\*The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation."



## USER TESTED PERFORMANCE

Standard Oil of California provides next day shipment to customers.

The computerized corner drugstore relieves 90% of behind-counter clerical workload.



Standard Oil Company of California's computing resources now are available to their service stations and direct buying customers as they place phone orders for the company's products as a result of a recently launched distributed processing network.

SOCAL's Southwest area customers now can receive next-day shipment from the company's inventory of approximately 3,000 packaged petroleum and TBA (tire, battery and accessory) products.

In addition to providing the company's order entry personnel with on-line video display terminals, the multi-functional network controls a host of other operations: inventory adjustment, warehouse control, manpower projections and fill line scheduling.

Making this possible are two remote Hewlett-Packard minicomputers, the first of a national network of up to 18 planned distributed processors, initially running at two of the company's Southern California distribution points: its Los Angeles TBA warehouse and its El Segundo package petroleum warehouse.

The online, real time model HP 21MX minicomputers will be controlled by a HP 21MX central mini, which in turn will transmit confirmed orders and inventory data to a System 370/168.

The network, designed to en-

hance customer service was developed jointly by SOCAL and its systems contractor, MST (Management Systems Technology) of Chicago.

A Chevron dealer can place one phone order through the Los Angeles TBA warehouse for any of 1,200 TBA items and package petroleum products sold at service stations. The order can be delivered in one shipment within 24 hours.

Order entry personnel may access account files by customer name, service station number or account number. Displays alert them to special promotions and quantity price breaks. Products are accessed by either codes or a specially designed alpha technique that allows the same product to be identified by different input keys.

### The computerized corner drugstore...

Computerized pharmacy is no longer a prediction. It is a reality. Management Systems Technology of Chicago installed its first Script Control™ dispensing system last fall at the Midwest's largest drug wholesaler.

Eight separate steps involved in dispensing drugs manually are reduced to a simple one step entry. As a result, approximately 90% of the pharmacists' behind-counter clerical workload is eliminated and up to 80

prescriptions per hour can be filled.

A Hewlett-Packard 21MX based Minicomputer System maintains a central data base accessible 24 hours daily and controls remote video displays and hard copy printers at subscribing pharmacies that will number 400 by the end of this year.

One of the HP 21MX Minicomputers with 64-K bytes of memory, together with varied HP peripherals, located at the central wholesaler site, can accommodate 16 pharmacies. Proprietary MST software was designed by pharmacists with pharmacists in mind. Druggists can interact with a Script Control system simply and with no previous computer knowledge.

For example, instantly after entering prescription number and drug identification, Script Control, in one step, accomplishes the following: prices the prescription; maintains the patient's profile; checks for drug interactions and allergic reactions; prints the label, receipt, alert messages and refill sticker; and prepares all tapes and documents for third party and state billing.

Savings derived from the use of Script Control are real and directly improve the profit picture for the pharmacist. Average third party rejection rate has been reduced to less than 1%. Headaches associated with constant price changes of pharmaceuticals are eliminated. Script Control uses the latest price and in addition lists generically equal drugs that when appropriate can be substituted at a cost savings to the patient.

The 22 functions of Script Control are under the complete control of the pharmacists. Changing from activity to activity is done simply by entering 3 keystrokes.

Byproducts of Script Control automatically filter into pharmacy record keeping and gives the pharmacist a new level of management control that was previously unattainable. Gross profit analysis, item movement and labor scheduling reports are three such examples.

Several years ago, MST also using HP computers, developed a predecessor system, CPS™ (Consulting Pharmacy System). Used by pharmacists who specialize in serving skilled nursing centers, CPS presently is processing more prescriptions than any other available computerized system.



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**Memory spectrum, where magnetic discs are too slow and semiconductor RAMs are too costly, is likely soon to be supplemented by systems based on charge-coupled devices, which are interconnected MOS capacitors**

## **CCDs in Memory Systems Move Into Sight**

**Harry R. Crouch and John B. Cornett, Jr**

**Scientific Systems Services, Incorporated  
Satellite Beach, Florida**

**Ronald S. Eward**

**and MarTech Strategies, Incorporated  
Indialantic, Florida**

Memory systems based on charge-coupled devices will have many potential applications within the next few years, ranging from refresh memories for video displays through data storage for point-of-sale terminals all the way to replacements for magnetic disc and drum storage systems. Their importance is based on their price and performance, reliability and maintainability, power dissipation, size, and weight.

"Semiconductor discs" using charge-coupled device (CCD) chips are currently being offered commercially by Intel Corp and have been fabricated by Bell Northern Research Laboratory. Based on commercially available CCD memory chips, such systems fill a gap in the storage market between random access semiconductor memories and magnetic discs and drums—in both price and performance. Performance is limited by access time, which for CCD memories is in the tens and hundreds of microseconds, as compared to submicrosecond access to semiconductor random access memories (RAMs) and typically 5 to 100 ms for rotating memories. Discs are low cost storage devices, but in capacities of 1 megabit or less, cost per bit is excessive. Thus CCD memories offer a cost-effective alternative in the capacity range overlapping large semiconductor and core memories at one end and small discs and drums at the other.

Other characteristics of CCD memories offer advantages that are important to certain applications. Compared to disc and drum, CCD memories are more reliable and far easier to maintain. Power dissipation

per bit is lower for CCD than for any other major memory technology, simplifying the corresponding cooling requirements; size and weight are also very low.

In addition to these secondary memory applications, CCD memories also may be useful for primary storage—the main memory of a computer. Cost projections for CCD memories are that they may be less than one-fifth the cost of metal-oxide semiconductor (MOS) RAMs by the end of 1977. Furthermore, the rate of CCD cost improvement is two to ten times better than that of MOS—that is, they are getting cheaper very quickly. At that price, CCD memories should be the inevitable choice for medium to large main memories. However, since CCD chips have serial, not random, access, computer system architectures will change to accommodate their cyclic access characteristics, perhaps by using cache or virtual memory. A cache combining a fast RAM and a CCD-based subsystem may prove to be the most cost-effective approach; program execution could be performed from RAM and inactive pages retained in CCD. In fact, at the 1976 National Computer Conference, a representative of Siemens AG in Germany described a combination of a bipolar cache, a MOS "page buffer," and a CCD main memory with a projected cost of one-half to one-quarter that of MOS RAM.

Other architectural changes will include longer processor words, which will enable larger main memories to be addressed directly and eliminate memory mapping and other cumbersome memory management



hardware and software currently in use, and new input/output (I/O) techniques, which will be necessary to utilize the sequential nature of CCD transfers effectively.

Design concepts that effectively utilize CCD chips in main memories could reduce memory costs as much as 90% from current prices, which would have a major impact on mini and microcomputers. These advances in turn would provoke software development, and hence lower cost software, high-level languages with fewer memory restrictions, self-diagnostic features, and fault isolation by software. Overall CCD memory advances should produce lower cost systems, fulfilling many new applications and increasing the market for computers and computer-like products.

First announced in early 1970 by Bell Telephone Laboratories as a new concept in MOS integrated circuit devices, the CCD is a shift register for analog signals that is constructed from a string of MOS capacitors. Its primary significance is high storage density—much greater than that of a MOS RAM, yet potentially at a much lower cost per bit. Capacities of 16,384 and 32,768 bits per device are being fabricated today, while transfer efficiencies, a vital measure of CCD performance, have improved from 99% per stage in the early days to 99.999% at present. CCD chips are available commercially from Fairchild and Intel.

## CCD Technology

The charge-coupled device, as a serial shift register, might be visualized as a set of flip-flops organized serially, through which information is propagated bit by bit at a rate established by an external clock. However, the CCD is not in fact a series of flip-flops; therefore it has different and valuable properties. In contrast to the ordinary digital shift register, bits stored in the CCD are represented by variable quanti-

ties of electrical charge rather than on-off states of fixed magnitude.

A circuit analogy (Fig. 1) is a set of RC networks (or charge cells) coupled by gated amplifiers that are activated by the clock pulses. In this analogy, the presence of a clock pulse gates the charge of each capacitor cell into its successive amplifier; the amplifier, in turn, charges the next cell accordingly. Although the analogy is oversimplified, eg, it does not provide for charge transfer both in and out of a capacitor at the same time, or for quick discharge of a capacitor when it shifts a 1 out and a 0 in, it does show that the CCD is an analog serial shift register device.

As an analog serial shift register, the CCD opens the door to many novel applications. For example, in graphic image sensing, the CCD can be storage for compact solid-state TV cameras and photodetector array displays. In signal processing, the CCD may serve as a delay line and filtering device. Other applications are in low cost function generators and voice synthesizing devices. Apparently, too, in computer memory applications, each storage cell can hold more than a single bit.

Though these applications are important in their own rights, computer engineers are interested in the CCD as a digital serial memory with cost, size, reliability, and power advantages. The CCD is an outgrowth of n-channel MOS technology. In the MOS unipolar transistor, the control electrode, or "gate," is insulated from the substrate material and forms a capacitive coupling with it. A voltage applied to the gate charges the capacitance, and the charge regulates current flow in the substrate.

Charging and discharging of this capacitance is the principal factor that limits the speed of MOS devices and makes bipolar technology preferable for high performance applications. This capacitance is also the storage site for charge in dynamic memories, which

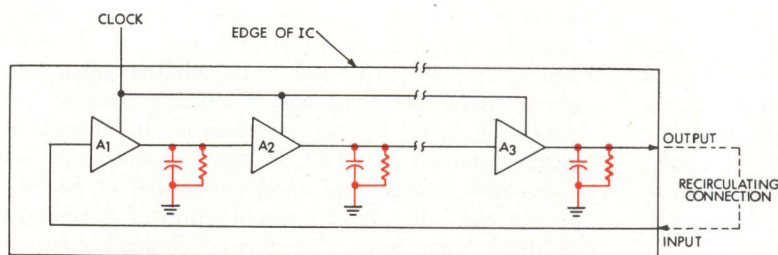


Fig. 1 CCD analogy. A charge-coupled device consists of a number of leaky capacitors interconnected with means to shift charge unidirectionally from one to the next, under clock control, plus a way of regenerating stored charge as it dissipates and of shifting states of discharge as well as charge. When used as a memory, stored charge is binary (either present or absent); CCDs can be used as analog storage devices as well, notably in imaging applications



must be refreshed every few milliseconds as the charge leaks away.

Physically the CCD is a linear array of closely spaced MOS capacitors or gates. Beneath the gates are "potential wells" at or near the surface of the silicon; the device operates by storing and transferring charge (data) between these potential wells, which are the unit storage elements or cells of a CCD memory. The wells are formed and controlled by the closely spaced MOS capacitors and a phased voltage applied to the gates. Charge-coupling is the process of transferring the mobile electric charge within a storage element or well to an adjacent well when a periodic clock voltage is applied to the gates. Quantity of stored electric charge in this mobile packet can vary considerably, depending on capacitance of the storage element and applied voltages.

In CCDs, as in most MOS structures, the gate is aluminum and the insulating layer is silicon oxide (Fig. 2). When a positive voltage is applied to the gate, the majority carriers, which are holes in the p-type substrate, are repelled from the vicinity of the gate, forming a potential well under it, storing a negative charge packet. This charge will eventually dissipate if left undisturbed; therefore it must be periodically refreshed or regenerated to retain the charge signal.

Depth of the well is a function of the gate voltage; the higher the voltage, the deeper the well. This is important in controlling the direction and movement of the electric charge. As minority carriers (the charge) are introduced into the potential well, they reduce its depth, much as a fluid fills up a container.

In a linear array of closely spaced MOS capacitors (Fig. 3), a 3-phase clock signal is used, and every third capacitor is connected to the same clock voltage. If wells of different depths are closely spaced, they overlap; their shape follows the shape of the clock voltages, so that charge is transferred from one storage cell to the next, and electrons move in packets

through the semiconductor in a potential-energy trough or channel. Either 2- or 4-phase operation is also feasible, but the principle is the same as with 3-phase.

## CCD Memory Organization

Various organizations have been proposed and developed for CCD memory construction; the choice depends on desired system performance. There are important trade-offs involving clock frequency, number of phases, access times, chip overhead for peripheral circuits, and temperature range, as well as other parameters.

Frequency of the clock that shifts data through the CCD shift register can have a wide range, limited at one extreme by the circuit's maximum switching speed, and at the other by maximum allowable refresh time required to maintain the data bits. Between these extremes, the CCD memory can be used as a direct replacement of conventional dynamic shift registers; or, with novel organizational schemes, its flexibility can be significantly enhanced. Of these schemes, three basic organizations have evolved: synchronous or serpentine, serial-parallel-serial (SPS), and line-addressable random-access memory (LARAM).

In synchronous or serpentine organization, storage cells are laid out along a winding path with signal refreshing stages at each corner (Fig. 4). Alternatively, this organization consists of several interconnected shift registers with read/write/refresh cells. All bits traverse the same path through the loop at the same frequency. Each bit passes through every storage element in one trip through the device. Therefore, internal shift frequency is equal to I/O data rate. The number of CCD storage elements between refresh stages depends on transfer efficiency (recoverable charge per bit shift) and the lowest shift rate to be used in standby or idle mode. Highest shift rate and number

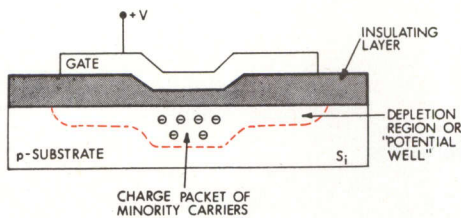


Fig. 2 MOS capacitor. Basis of CCD storage cell is the capacitance between a p-type semiconductor substrate and a metal overlay, separated by a thin insulating layer. Voltage applied to overlay (gate) induces charge accumulation in substrate immediately below, in a "potential well," which can be propelled from cell to cell

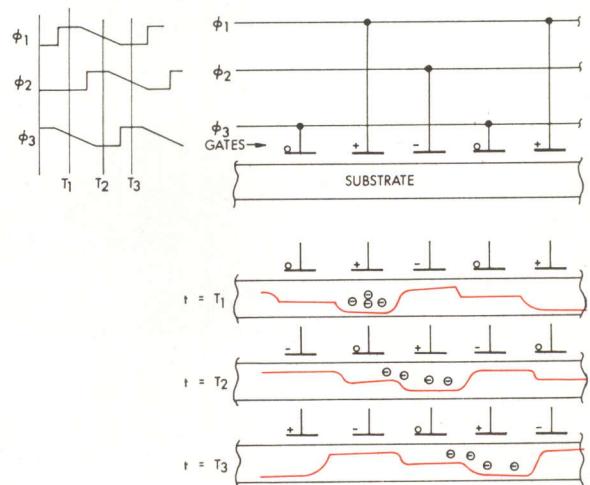


Fig. 3 Shift control. Three-phase voltage (upper left) applied to series of cells (upper right) causes accumulated charge to move from cell to cell (lower right)



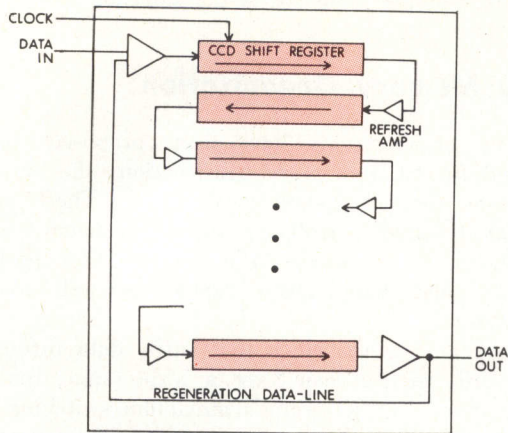


Fig. 4 Synchronous organization. Simplest CCD layout moves data from cell to cell and from register to register in one continuous stream. It has the longest access time and highest power dissipation of conventional layouts

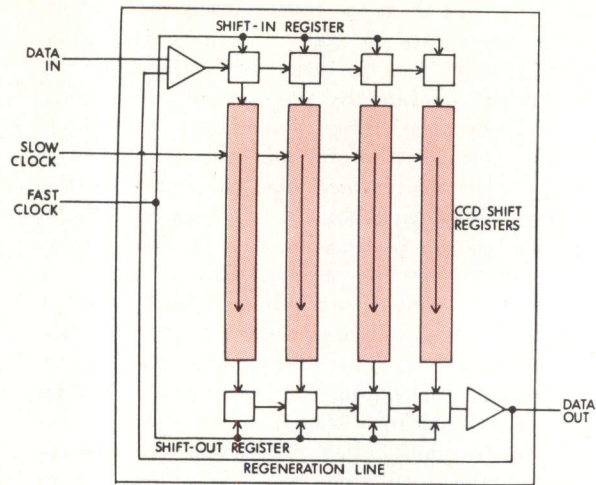


Fig. 5 SPS organization. Numerous parallel storage registers placed between two serial registers, one for input and one for output, form a more complex layout that dissipates less power but requires two clocks and has long access time

of bits between input and output points determine the maximum access time; for random addressing the average access time is half the maximum. Power dissipation is high for this organization because all bits of data are moving at the same frequency. Also, clock drive requirements for a large memory are high because clock line loading is relatively high.

In serial-parallel-serial (SPS) organization (Fig. 5), two single-channel serial shift registers of N bits serve one large multichannel shift register consisting of N serial registers operating in step. A series of bits is fed into the input shift register at a high rate, then transferred in parallel into the multichannel register, and fed out through the other serial register. This arrangement accommodates more storage elements be-

tween refresh stages and has both high data rate and low power dissipation, because most data bits are transferred at the slower clock frequency of the multichannel shift registers, 1/N that of the serial registers. Disadvantages are the requirement for one fast and one slow clock, and long access times.

LARAM organization integrates CCD and MOS memory concepts, to provide shorter access times and reduced capacitive drive requirements. It has a MOS address selection matrix and a number of CCD serial shift registers or lines (Fig. 6). As the name implies, any line is randomly accessible, but its contents are accessible only serially.

When a given line is addressed, a fast clock is applied only to that line, while other lines remain

#### Comparison of Three Memory Organizations

Characteristic	Serpentine	SPS	LARAM
Capacity, bits	16,384	16,384	16,384
Organization	256 x 16 x 4	4096 x 4	128 x 32 x 4
Access time, (at 5 MHz)	51.2 $\mu$ s	819.2 $\mu$ s	25.6 $\mu$ s
Power dissipation	400 mW	150 mW	250 mW
Temperature range	85°C	70°C	55°C
Relative chip area	1.0	0.9	1.1
Clock drive requirements	1000 pF 1000 pF	1000 pF 40 pF	100 pF 15 pF
Relative cost	1.0	0.8	1.1



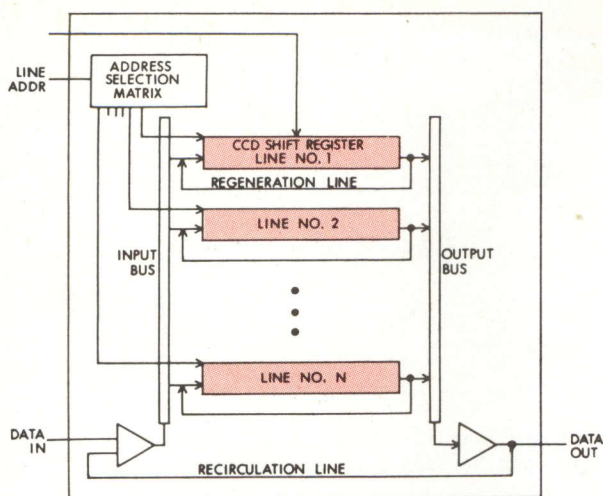


Fig. 6 LARAM organization. Parallel storage registers that circulate data individually, and are separately addressable at random, form most complex layout. Power dissipation is minimal because only one register at a time need operate at higher than standby rate

in an idle or slow refresh mode. Data are read or written only in the addressed line. Since only one line is operative at any one time, driving requirements and power dissipation are minimal. Access time depends on number of bits per line and clock frequency or rate. Either word-organized (each line containing one or more words) or bit-organized (each line containing one bit of many words) memory can be assembled.

Quantitative comparison of these basic organizations (see Table) shows SPS to have lowest cost per bit and lowest power dissipation. Serpentine offers the best temperature range performance, while LARAM has shortest access times and lowest clock capacitance drive requirements. Thus the designer must be aware of all three organizations when working with CCDs.

## CCD Chips Available Today

As the cost of CCD memories decreases, a greater variety of charge-coupled devices will become available to the user. Four that are currently on the market are the Fairchild CCD 450, Fairchild CCD 460, Intel 2416, and very recent Mnemonics MN2.5.

Simplest of the three, the CCD 450 stores 9216 bits organized 1024 words by 9 bits. Its nine 1024-bit shift registers are shifted in parallel, storing 9-bit bytes serially by byte. All registers connect to external circuits through 3-state output buffers for wired-OR applications. Design data rate is 50 kHz to 3.0 MHz at 70°C ambient temperature.

All nine shift registers are controlled by two common data-enable signals, read and write, which have TTL levels. The device operates in these two modes as well as in read/modify/write and recirculate modes.

Although the two 16K units, Intel 2416 and Fairchild CCD 460, both have LARAM organization, different compromises are offered between access time and storage capacity. Quick access times are obtained by keeping shift registers short; however, on-chip peripheral circuitry is reduced (and space for storage is increased), by making shift registers longer.

Intel 2416 contains 16,384 bits. To minimize latency time (access time to any given bit in the device), it is organized as 64 registers of 256 bits each; therefore, any bit is accessible with a maximum of 255 shift operations. Since the fastest shift cycle is 750 ns long, maximum latency time for the 2416 is less than 200  $\mu$ s.

However, at this shift rate (1.33 MHz) data appearing at the register outputs are lost for another 200- $\mu$ s cycle. At slower shift rates the 64 recirculating registers are randomly accessible. A 6-bit address selects one of the 64 registers between shifts, in any sequence. Up to 16 random access cycles can be taken between shifts, at about 500 ns each; but to satisfy the device's refresh requirements, one shift operation must be taken every 9  $\mu$ s. Thus the shift rate varies from 111K bits/s to 1.33M bits/s, and the corresponding average data rates are 1.78M bits/s to 794K bits/s.

CCD 460 also holds 16,384 bits, but it is much faster—its data rate is 20M bits/s. This high rate results from the combination of an operating frequency of 5 MHz and 4-bit parallel readout. The four bits come from four independent sections each consisting of thirty-two 128-bit registers with random access in each section but with corresponding registers in the four sections always selected together. Average access time is 12.8  $\mu$ s; and power dissipation is less than 200 mW, except in low power standby mode, when the recirculate/refresh period can be as long as 10 ms and power dissipation is only 50 mW.

## CCD Application and Potential

CCD memories neatly fit into the memory hierarchy to fill the gap between very fast but expensive semiconductor random access memories and cheap but relatively slow magnetic discs and drums (Fig. 7). Today, CCD serial- and block-oriented memories provide more capacity per chip, yet cost less than RAMs. However, differences in access time will keep CCDs from completely replacing RAMs. Likewise, discs and drums have a significant edge in storage capacity over CCDs.

Nevertheless, CCDs will exert some design influence within overlapping regions of the diagram. Their initial thrust will be in fast block-oriented rotating memories with limited capacity, and in applications such as CRT refresh and communication buffers. However, for the most part, CCDs will evolve into their own domain. They will be considered a new and viable storage medium with unique characteristics.

The auxiliary memory market is now in the neighborhood of \$3 billion a year—an attractive market to semiconductor suppliers. This market has traditionally been served by electromechanical rotating memories such as drums and small discs. However, all such units require much maintenance and dissipate much power. At the lower end of capacity, say from 100K



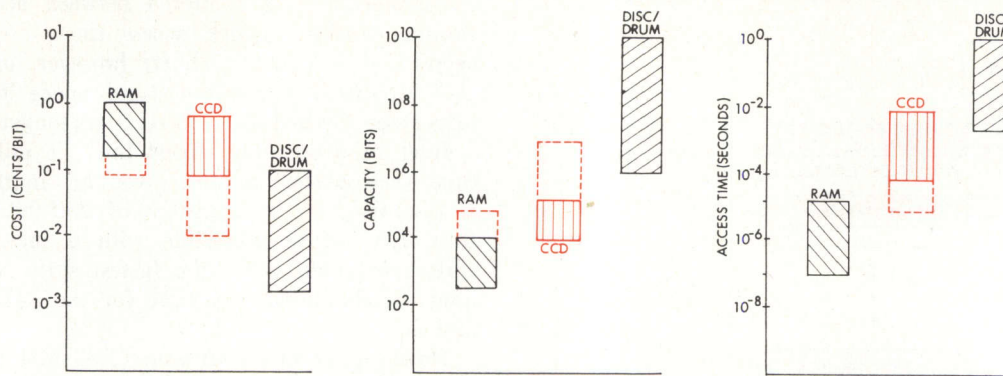


Fig. 7 Gap filler. Semiconductor RAMs are fast but costly; magnetic electromechanical devices are cheap but slow. CCDs have potential to fill the gap between these technologies in cost, capacity, and access time

to 2M bits, cost per bit is relatively high because of fixed overhead costs of motor, power supplies, and electronic circuits. CCD memories offer significant cost advantages at these capacities. Some computer manufacturers are already developing stacked CCD chips to build systems of 10M bytes, with data rates of 32M bits/s and average access times of 250  $\mu$ s to a block of 256 words.

CCD memory can address many specialized applications with cost/performance improvements over conventional techniques. These include severe environment applications that otherwise would require highly reliable ruggedized rotating memories. They are also useful for temporary low cost storage in radar digital signal processing, where delay lines have been used.

## Outlook

Fairchild Semiconductor is expected to have a 65K bit chip ready for sampling this fall, while Texas Instruments will probably have a 65K prototype ready by the end of the year. In volume, this could sell for \$15, which would place the cost per bit well under 0.1¢. Within the next two to three years, chip density should increase to 128K, on a 200 x 200-mil chip. Density is restricted only by current technological limits of photolithographic processing; electron beam lithography will permit higher resolution on larger chips of 300 to 400 mils square, permitting capacities of 400K to 500K bits on a single CCD chip.

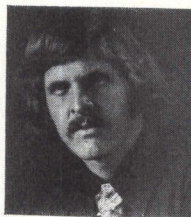
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Specializing in systems analysis including generation of mathematical models and utilization of other simulation techniques, Harry R. Crouch is also responsible for design and development of various programming assignments. He received his PhD in physics from Brown University.



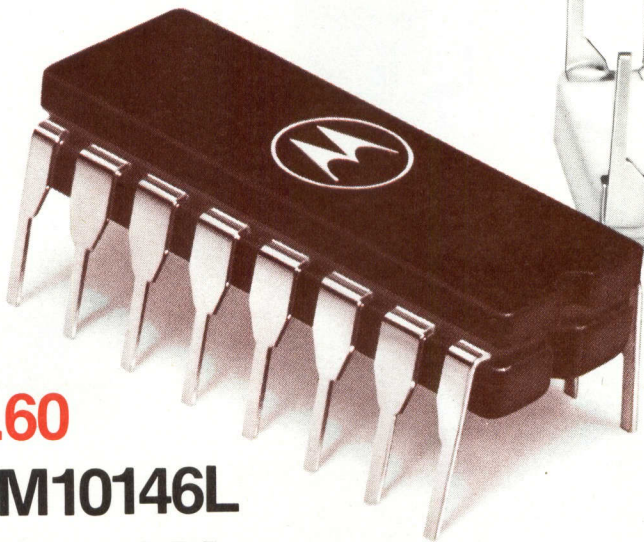
John B. Cornett, Jr is responsible for development and implementation of project programs, and has participated in programming applications such as a data acquisition system for a nuclear reactor and a numerical control computation and measurement program. He holds a BS degree in computer science from Florida Institute of Technology.



Ronald S. Eward, president of MarTech Strategies, received his MBA from Florida State University. His experience includes market research and planning, as well as positions in computer systems analysis, operations research, and product planning.

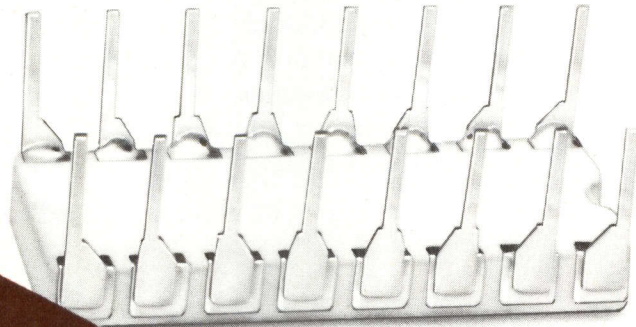


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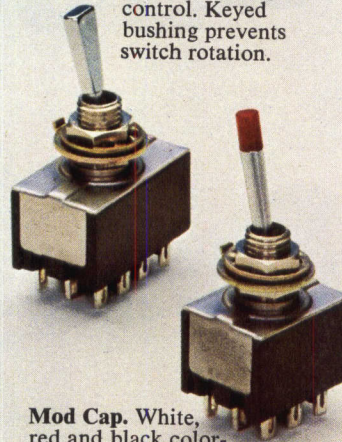
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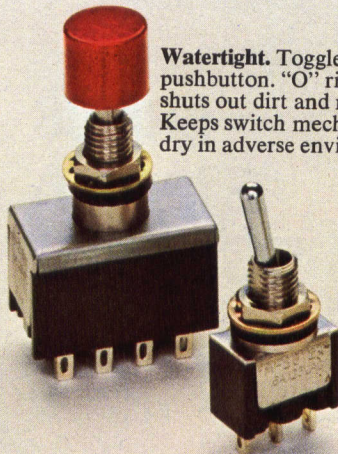
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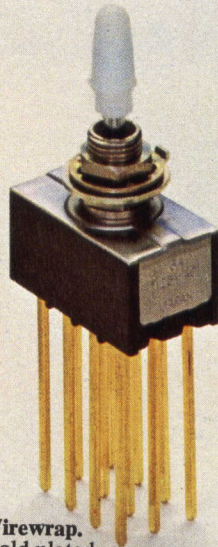
**Lever Lock.** Locks in position to assure precise control of vital or sensitive functions and equipment. No accidental operation.



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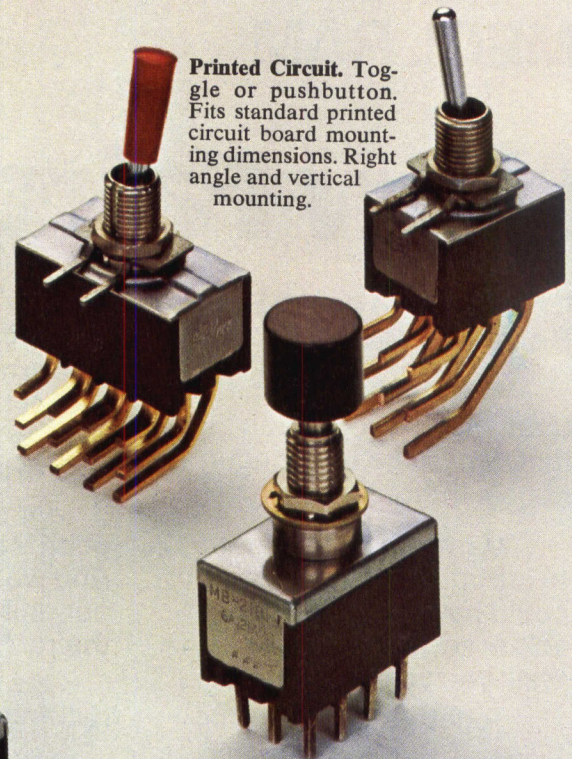
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CIRCLE 35 ON INQUIRY CARD



*As scientists apply microprocessors to complex experiments,  
they sometimes fall victim to the complexities of the technology*

# Microprocessors Aid Experimentation in Scientific Laboratory

**Thomas A. Seim**

**Battelle Memorial Institute  
Pacific Northwest Laboratories  
Richland, Washington**

Scientists in a wide variety of disciplines are learning how to apply microprocessors to their computing needs. Usually they do so with the help of system engineers, who therefore must not only understand the functional aspects of microprocessors, but also know in reasonable detail the scientist's problem and his other computing requirements. Sometimes both scientist and engineer fall short in both respects, leading to great difficulties in completing a series of experiments; other times a well-thought-out process carefully instrumented leads to better results than could be obtained otherwise.

Examples of various applications are found at Battelle Pacific Northwest Laboratories. They include measurement of simulated events inside nuclear reactors, automatic control of experiments, monitoring reactors for safe operation, accumulating data generated in complex or long-running experiments, and interfacing between experiments and a large central computer.

Not surprisingly the most useful research tools are those that are most flexible. While programmability gives computer systems a degree of inherent flexibility, it is not sufficient for a useful research tool. Another important factor is a minimum amount of system hardware. However, less hardware usually means more software, and software today absorbs the majority of a typical computer system development effort. Since custom laboratory instrumentation is seldom built in quantities of more than one or two, economy may dictate more than the minimum hardware.

The trend in selection of microprocessors for the laboratory is toward the most capability that is reason-

ably possible. If the choice were between a 4- and an 8-bit processor, the 8-bit device would be selected; and if the microprocessor had optional hardware arithmetic it would be purchased fully equipped. Other purchase options that simplify software design are usually favored.

However, most projects cannot support a large capital outlay for special-purpose development systems, and a single microprocessor cannot be chosen for long-term support, because of the technology's volatility.

To provide a powerful alternative to costly development systems Battelle has successfully developed microprocessor software on existing computer systems. This is highly cost-effective, since the capital investment is spread over several projects, each of which is charged for use of the equipment at a rate perhaps less than one-tenth of the cost of time-sharing services.

## Macro Definitions

A useful technique in adapting general-purpose computing systems to microprocessor software development is the description of machine languages with macro-instructions, or macros. A macro describes a repetitive series of machine instructions once, and assigns it a name. When assembler software encounters the macro name outside of the definition, it replaces the macro with the code within the definition. Cross-assembly of microprocessor programs can be accomplished by defining each microprocessor instruction with a macro.



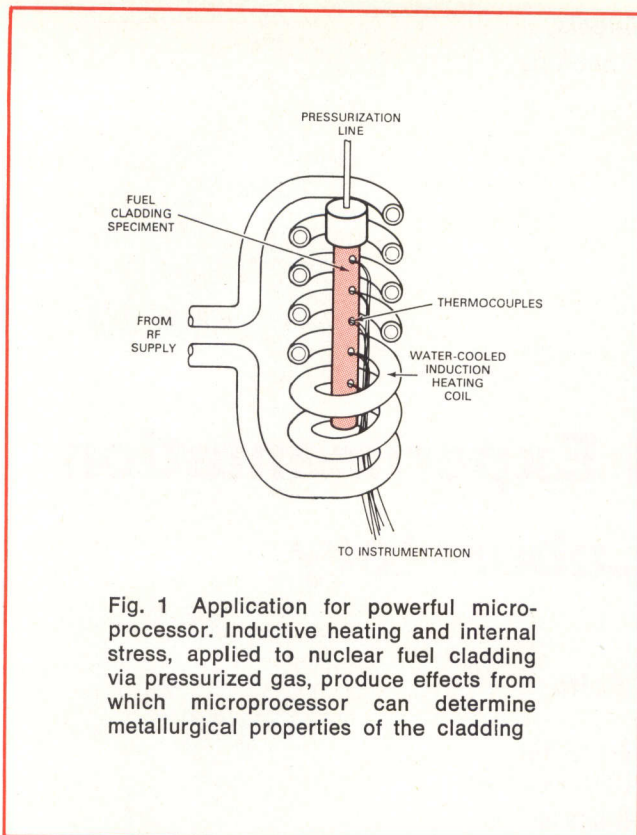


Fig. 1 Application for powerful microprocessor. Inductive heating and internal stress, applied to nuclear fuel cladding via pressurized gas, produce effects from which microprocessor can determine metallurgical properties of the cladding

The macro generates equivalent machine code for a particular instruction. Macros can pass arguments, do arithmetic operations on arguments, and conditionally test argument values and status. Some operations common to several macros may also be written as a macro; calling a macro from within a macro is termed "nesting." Typically a nested macro is used to translate addresses for memory reference instructions, which can be quite involved if the microprocessor has many addressing modes, each requiring separate treatment.

Macros are also useful in languages more complex than assembly language, but less complex than compiler-level languages such as FORTRAN. For example, an application language can be designed for a particular use with macros that execute a function directly correlated to the application. The application might

be an automated laboratory instrument, and a language could have commands that duplicate the functions of the manual controls. These kinds of languages are easily understood by personnel not professionally trained in computer programming, more so than FORTRAN or BASIC; macros are a way of implementing the languages.

### Choosing a Microprocessor

Much of the literature on microprocessors is aimed at designing commercial products, which are usually the final result of a carefully orchestrated effort beginning with a market survey. Designing systems for the laboratory, however, is almost diametrically opposed to designing for production. Laboratory applications generally evolve from problem definitions that are initially vague because of a limited knowledge of the research subject. As a result, matching microprocessor characteristics to the application is difficult. If the processor is much more powerful than necessary, the "overkill" is little noticed; but if an insufficiently endowed microprocessor is chosen, the effects can be devastating. Not only is the program difficult to write and voracious of memory, it is difficult to change to a more powerful microprocessor part way through the project. Starting with adequate or even a little too much processing power is well worth the extra cost.

Such an improper selection was made in using an Intel 4004 microprocessor as a transient recorder and controller. The application measured material properties of nuclear fuel pin cladding under conditions of failure (Fig. 1). The cladding is a metal jacket bonded to a fuel element to prevent corrosion and release of fission products. When inside a reactor core, cladding is subject to temperature extremes and temperature changes that can reach 2000°F/s during a hypothetical reactor accident, while the specimen is subject to internal stresses of around 10,000 lb/in.<sup>2</sup> As temperature and stress increase, the specimen expands. Intent of the experiment is to raise the temperature of the specimen linearly to a plateau while holding stress constant (controlled by manipulating internal pressure), then to raise stress at a controlled rate while holding temperature constant. During the entire cycle the specimen expansion is recorded. If expansion

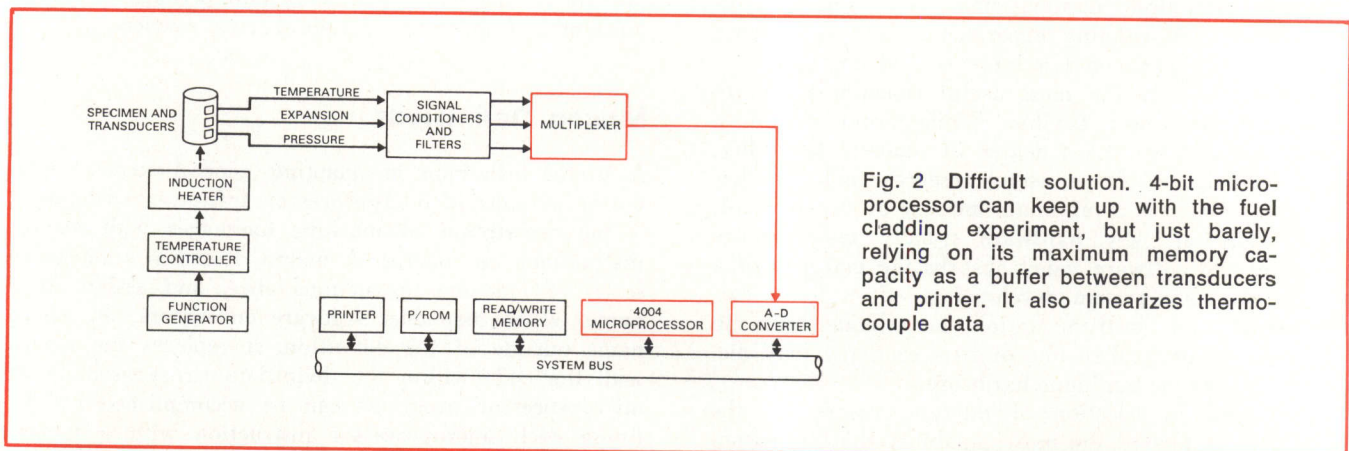


Fig. 2 Difficult solution. 4-bit microprocessor can keep up with the fuel cladding experiment, but just barely, relying on its maximum memory capacity as a buffer between transducers and printer. It also linearizes thermocouple data



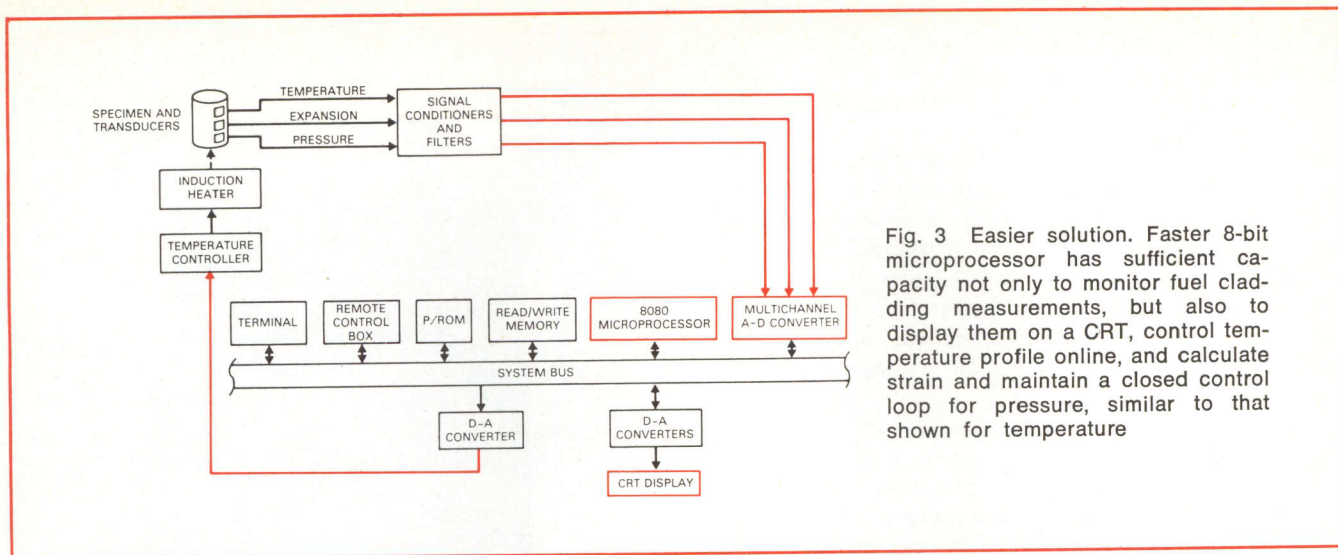


Fig. 3 Easier solution. Faster 8-bit microprocessor has sufficient capacity not only to monitor fuel cladding measurements, but also to display them on a CRT, control temperature profile online, and calculate strain and maintain a closed control loop for pressure, similar to that shown for temperature

is accurately known, the specimen's strain can be calculated. Ratio of stress (computed from applied pressure) to strain (expansion per unit length) is the modulus of elasticity, which, at the temperatures of the reactor core, is a critical parameter in the simulation of emergency conditions. Other mechanical properties such as ductility and strength can also be determined.

The controller also continuously monitors the specimen for imminent failure—that is, rupture—and aborts the experiment as soon as it detects such conditions. This preserves the specimen for later examination and prevents it from making a short circuit between the high voltage and the instrumentation as it ruptures.

In the laboratory, temperature change is induced by a high power rf induction furnace. The rf power supply produces 10 kW at 10 kV and 250 kHz. Measurements are made by thermocouples attached to the fuel cladding specimen, which has a mass of a few grams. Noise coupled into the thermocouple leads from the rf supply is in the range of 10 to 20 V peak-to-peak, and requires both passive and active filtering of the analog signals.

Under these difficult conditions, fast data collection (500 to 800 points/s) is necessary (Fig. 2). Measurements are stored in the system's read/write memory (RWM) when the sampling rate exceeds the printing rate. However, the 4004 uses 12-bit addresses but has a data path only four bits wide. Transferring data to or from the memory requires three separate instructions to send out the address in 4-bit chunks, and a fourth instruction to read or write the data. Still other instructions initialize the processor registers that store the 12 address bits. Furthermore, input and output (I/O) operations use the same procedure, so that they interfere with memory operations. These characteristics limited the 4004 to data collection at only 500 points/s and no control functions.

Other difficulties are posed by the separation of programmable read-only memory (p/ROM) and RWM in the 4004, which precludes easily altering the program as errors are discovered. Furthermore, since the 4004 cannot be halted or single-stepped, discovering the problem to begin with is a challenge. The p/ROM

of the 4004 was simulated with RWM from another microprocessor, which had a paper tape reader for loading the object code. Buffering of the memory address lines permitted both microprocessors to address the RWM. Because of these difficulties, the program took about twice the time to develop and twice the memory that would have been required with an 8-bit Intel 8008.

Eventually the 4004 was replaced with an Intel 8080 microprocessor, architecturally similar to the 8008 but substantially faster. This higher speed and the doubled width of the data path permitted a high resolution CRT display to be added to the system, refreshed directly by the microprocessor (Fig. 3). The

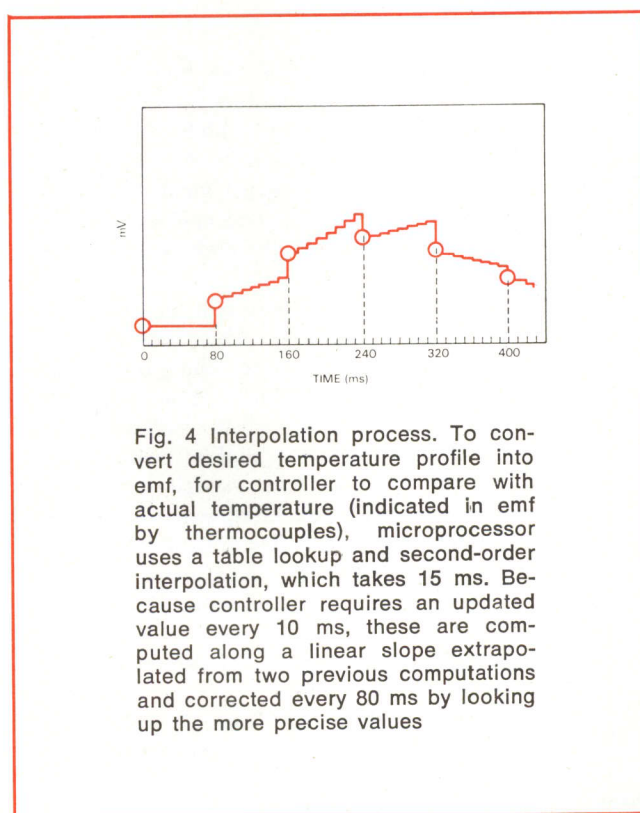


Fig. 4 Interpolation process. To convert desired temperature profile into emf, for controller to compare with actual temperature (indicated in emf by thermocouples), microprocessor uses a table lookup and second-order interpolation, which takes 15 ms. Because controller requires an updated value every 10 ms, these are computed along a linear slope extrapolated from two previous computations and corrected every 80 ms by looking up the more precise values



8080 can also generate a temperature profile for the heater control—the combination linear ramp and plateau mentioned previously—replacing an electro-mechanical function generator that was required with the 4004. Not only is the 8080 fast enough to carry out this added task, but its output is smoother and more reliable than that of the mechanical device. The conversion from temperature to thermocouple emf, for comparison in the temperature controller, is computed at intervals of 80 ms by a rather slow table lookup and second-order interpolation, and approximated every 10 ms by extending a slope from two previous computations (Fig. 4).

After a run, the experimenter can request all or any part of the data to be printed out, or display any part on the CRT screen. In general, data represented graphically are easier to interpret than columns of numerical data, and microprocessors can save considerable time that manual plotting of data would require. Decisions on future experiments and conclusions from available data can be made faster with greater reliability. The experimenter's input, besides the controls on the CRT, is through a control box (Fig. 5), which is connected as a peripheral to the microprocessor's I/O bus. Its specific functions are controlled by microprocessor software and can be changed from one experiment to another.

Even with the display, function generator, and control box, the 8080 has a comfortable margin for more functions. For instance, while the specimen's expansion is measured dynamically now and the strain computed afterward, soon a dynamic calculation of the strain will be added to the system, permitting it to control strain by manipulating pressure.

## Automatic Control of Experiments

While some scientific experiments use highly sophisticated instrumentation and computers, many are collections of unrelated instruments which require constant supervision. Such supervision could be relegated to microprocessors, freeing the experiment to run unattended, perhaps overnight. Microprocessors might be retrofitted into the instruments themselves to upgrade their capabilities.

Often the purpose of an experiment is to observe controlled change in a variable. This may be complicated when other variables are changing at the same time. While isolating the effect of a single variable is mathematically feasible given sufficient data, measuring that effect directly is highly preferable. A case in point is the fuel cladding experiment.

There are two complications. First, expansion of the specimen is the result of two factors: applied stress and temperature rise. Changing temperature and pressure independently, as described previously, helps separate their effects; but since the two parameters are thermodynamically related, keeping them separate is more easily said than done.

Second, controlling internal pressure is difficult because it is applied with an inert gas and reaches levels of 15,000 lb/in.<sup>2</sup> Difficulties include the lack of commercially available high pressure servo valves, and

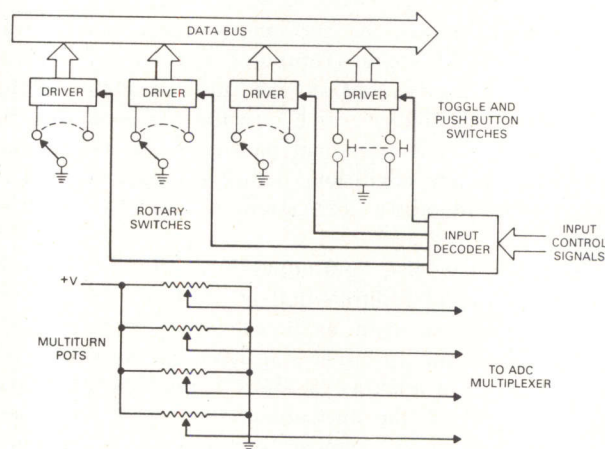
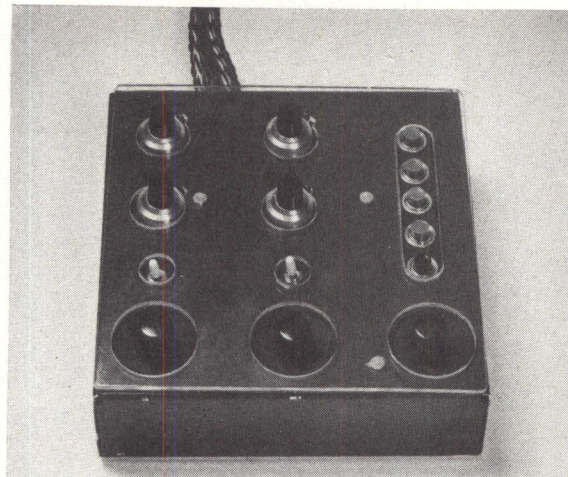


Fig. 5 Control box. Connected to the microprocessor as an I/O device, this unit controls the CRT display under software supervision. With different software, the same box could be used for other functions

the transport lag between the valve and the specimen. Slow experiments can use a controlled low pressure hydraulic fluid stage coupled to a high pressure gas stage through a pressure intensifier, but such equipment is completely inadequate in fast experiments, which run their course in a few seconds—sometimes as little as a fraction of a second. A direct-acting control valve works better than pressure intensification, but suffers from backpressure against the valve stem. Backpressure is a function of the pressure differential between gas supply and the valve's outlet.

A microprocessor can be programmed to close the pressure control loop. Its control algorithm can easily include an offset factor to compensate for backpressure, in the form of a table that correlates current pressure to appropriate control action offsets. At the same time the microprocessor can generate time profiles for temperature and pressure. Errors due to transport lag can be minimized by using a feedforward



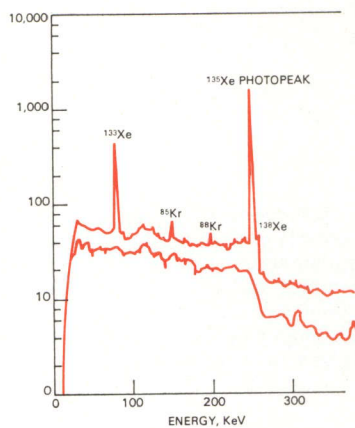


Fig. 6 Detection method. Uniqueness of gamma ray spectra of different radioactive isotopes, one of which is shown here, is exploited to detect leaks of trace gases sealed in nuclear fuel pins. Microprocessor counts output pulses from a scintillation detector tuned to a particular peak, such as the one circled, subtracts the background count from a separate mistuned detector and analyzes average count per second to discover presence of a particular gas and hence existence of a leak in a particular fuel pin

control strategy, which anticipates future pressures and takes appropriate control action soon enough to compensate for the transport delay factor.

Reactor safety systems are understandably important in nuclear reactor operation. An important safety factor is integrity of the fuel pins, which consist of fuel pellets sealed in tubes along with small quantities of radioactive trace gases. Each gas is uniquely characterized by the energy spectrum of the gamma rays it emits, and can be identified by distinguishing peaks. If a fuel pin cracks or ruptures, the trace gas is released into the reactor vessel; its gamma rays trigger a scintillation detector, which consists of a crystal and a photomultiplier tube. The crystal, which is a material such as sodium iodide, emits a photon of visible light when struck by gamma rays; the photomultiplier generates and amplifies a pulse when struck by one of these emitted photons. Magnitude of each pulse is proportional to the gamma's energy, which in turn

depends on the atomic weight of the gas; the logarithm of the number of pulses during a given interval of time is proportional to the amount of the element emitting the particles. Thus the presence of different elements can be determined by differentiating and counting the pulses. Using several trace gases in different proportions in each fuel pin identifies the particular one that has failed, out of more than 16,000 in a reactor.

In one such system developed for the Fast Flux Test Facility (FFTF), Richland, Wash, a microprocessor monitors four elements continuously by counting the outputs of eight signal differentiators, or single-channel analyzers. Of each pair of analyzers, one is tuned to the energy level of a peak in the gamma ray spectrum for a particular element and the other is tuned to a nearby energy with low activity.

Because the second analyzer is not tuned to a spectrum peak, it responds only to background radiation, which is always present and must be subtracted from the count caused by the presence of radioactive gas (Fig. 6). The scintillation detector's range is extended in the FFTF system by a slide assembly containing absorbers and collimators, which respectively reduce gamma radiation intensity selectively and uniformly.

The microprocessor counts the two signals over a period of time selected by the operator, and divides their difference by the time interval to obtain average count per second. These computations are performed by the microprocessor by looking up the log of the difference in a table, and subtracting the log of the time interval to obtain the average.

Counting rate ranges from 0.1 Hz to 100 kHz. Successive pulses increment 12-bit hardware counters, which are monitored every 16.7 ms for overflow. When an overflow is detected, 12-bit software counters are incremented. At the end of the counting period the 24-bit combined total is read out and converted to log form.

When the microprocessor is not checking hardware counters for overflow or calculating outputs, it monitors the control panel for operator interaction. This may include a time base change or coefficients that multiply the outputs to compensate for effects of absorber and collimator for each element. The absorber-collimator slide assembly, when not under manual control, is positioned automatically by the microprocessor through a stepping motor (Fig. 7), when any input exceeds preset trip points specified by the operator. Counts coming from the scintillation detector are valid only when the slide is in position. Thus no other duties are necessary while the slide is moving, and step commands can be generated by software delays. This would not work if other functions had to be performed simultaneously; their execution time would probably vary, resulting in poor regulation of slide velocity, because stepping motors are very susceptible to phase jitter in the stepping frequency.

A key aspect of this application is reliability, which prompted inclusion of hardware and software failure monitors. A failure in the microprocessor might not be noticed by operation personnel, because the levels of the trace gases are unlikely to vary appreciably for months at a time. To counter such a possibility, the microprocessor periodically resets a failure



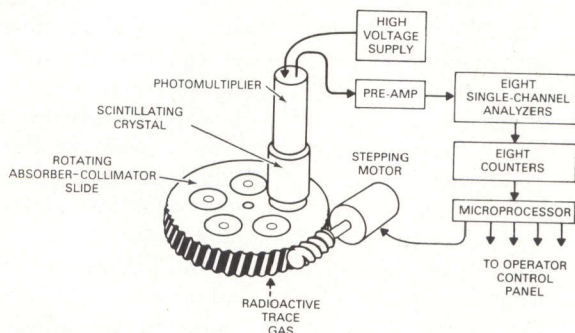


Fig. 7 Range selection. Because radiation levels of different elements range widely, detection method of Fig. 6 is enhanced by incorporating absorbers or collimators in path of radioactive particles toward scintillation detector. Microprocessor controls choice of absorbing material on basis of particle count during given time interval

detection circuit. If the microprocessor fails, reset signals stop, permitting the failure detector to actuate, zero the digital-to-analog converter, and alert operations personnel.

## Life Sciences

Sophisticated electronic instrumentation is being used increasingly in the life sciences in an effort to make more quantitative measurements. For example, one research program at Battelle was to monitor respiratory parameters of laboratory animals and display them as histograms on a CRT screen. Cost analysis showed that an instrument designed with a microprocessor would be cheaper than one using hardwired logic.

The instrument was to accumulate breathing rate and volume data and generate a dynamic histogram display as data were being collected. The researcher could adjust the bounds of the histogram to produce an optimum display; too few points would reduce horizontal resolution, while too many would reduce vertical resolution. The instrument also generated a vertical cursor which the operator could move across the display and, with a numeric readout, obtain an accurate value for a point of interest.

An Intel 8008-1 microprocessor was used in the instrument, along with 762 words of p/ROM and 1K words of RWM. Breathing rate was determined by counting the time interval between breaths. Breath volume was an external analog measurement converted to digital form for input to the microprocessor. Its output was a real-time display of 256 points, coordinates on the histogram. Two buffers of 256 words each were used for rate and volume parameters.

Following a display scan, the microprocessor tests control panel switches and signal inputs, and incre-

ments one word in each buffer, choosing the word on the basis of the corresponding input value. Each word is thus a count of the times a particular input value has been measured. After both buffers have been updated, the microprocessor begins another display scan, during which the accumulated total in each word of each buffer is translated into a vertical deflection of the CRT sweep. Horizontal scale is set just before each scan, since it may change during data collection. Finest resolution is used as data are being collected; if the operator has selected a lower resolution, setting the panel switches accordingly, several points are summed for each point displayed.

The 8008-1 can generate about 20 scans/s, during which it displays the two parameters alternately at 10/s each. Although a flicker-free display would require at least 30 scans/s, these slower scans do not produce operator discomfort because the display generally does not change or changes only slowly; 5 scans/s would have been adequate.

## Biology

Programs in biology conducted at Battelle range from inhalation toxicology to plant physiology and involve many types of experimental animals. Animal experiments are generally long term—some animals are 14 years old. A typical program studies the effects of inhaled plutonium of different dosage levels in 120 dogs, continuing over their life span (about five years). During this time they undergo extensive testing; for instance a gas chromatograph of a blood sample from each dog is made daily.

Although the experiments may be quite complex, the level of automation is fairly primitive. Most data are recorded by hand into laboratory notebooks, or by



stripchart recorders. Because data for any experiment can exist in many different forms in many different places, there is a real need for integrated data management. Microprocessors can serve as a buffer between an experimenter or an analytical instrument and a large scale computer. Equipped with moderate mass storage such as a floppy disc, the microprocessor can record data for a few days at a time, and then transmit accumulated data to the central computer. This also serves to isolate the scientist from "crashes" of the central computer. Data can be transmitted over dial-up telephone lines at slow rates during off hours, which is more reliable and considerably less expensive than a high speed communication line.

A crucial consideration in such an application is to leave the operational procedures essentially the same with the microprocessor as with manual methods. Scientists are justifiably irritated at any innovation that is more of a hindrance than a help.

Microprocessors can improve the reliability of the life support systems that many laboratory animals require. The Aquatic Facility, for instance, has numerous fish tanks with temperature, lighting, and chemical composition control. Failure of one control can do irreparable damage to an experiment, representing considerable expense in view of the facilities and intensive care given over a long period of time. The microprocessor can monitor vital parameters of a facility as well as assist in data acquisition. In one experiment fishes were tested for the rate of exhaustion when dosed with plutonium compared to an undosed control group. They were placed, one at a time, upstream in a flow tank with an electrified grid at the downstream end. External circuitry limited the current so that the water in the tank did not short-circuit the grid; nevertheless, the potential was high enough to give an unpleasant though harmless shock to any fish that touched it. Therefore the fish would swim upstream, away from the grid, as long as possible, until it became exhausted and was no longer able to make headway against the current. At that point the fish would be released and the test repeated with another fish.

At present this kind of test is carried out manually; technicians admit and release the fish and measure their time to exhaustion with stopwatches. Because many fish must be tested for each variation in experimental conditions, measurements are extremely tedious and time-consuming. However, they are easily within a microprocessor's capacities; it can open and close gates that admit and release the fish, measure the swimming rate, and detect when a fish has stopped swimming—perhaps by photoelectric sensors to monitor fish location.

## Future Potential of Microprocessors

More than any other thing the future of microprocessors is limited by the human element. While tech-

nical limitations of microprocessors are being quickly identified and solved, needs of designers who use them are sorely in need of attention. A great gulf exists between computer scientists and the logic-turned-microprocessor designer.

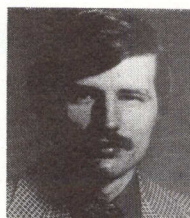
Microprocessors are a microcosm of computing in general. They demand a wide variety of talents from designers, who have a minimal amount of assistance. For this reason the designer tends to visualize a hardwired solution to a problem which he can translate to an equivalent microprocessor application. This is a seriously limiting outlook, because the majority of potential microprocessor applications are not practically solvable with hardwired logic.

The hardwired logic solution is a special-purpose sequential machine capable of fast clock rates. On the other hand, the microprocessor is a general-purpose sequential machine that operates on data stored in its memory—often treating even I/O devices as memory. It can be programmed to emulate a special-purpose machine, but very inefficiently; emulation reduces speed between one and two orders of magnitude or more, increasing its inherent speed disadvantage.

To achieve full potential, microprocessors should be considered for applications that maximize their strong points (one of which is definitely not logic emulation). An excellent example is systems that require man-machine interaction, which could use microprocessors at the man-machine interface. Some simple, yet effective, tasks amenable to microprocessors include error recovery, error checking, free-field-format entry, default conditions, qualified output, "quick look" output, step-by-step prompters, and status monitoring. Yet many applications of microprocessors in man-machine interaction abound with fixed-field formats, cryptic user commands, and no error recovery—as a direct result of the designer being conditioned to the limitations of hardware design. Consequently the future of microprocessors will depend in part on a change in the attitude of the designers most likely to use the devices.

## Acknowledgement

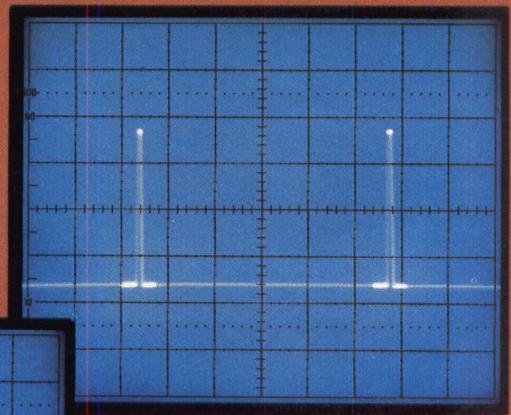
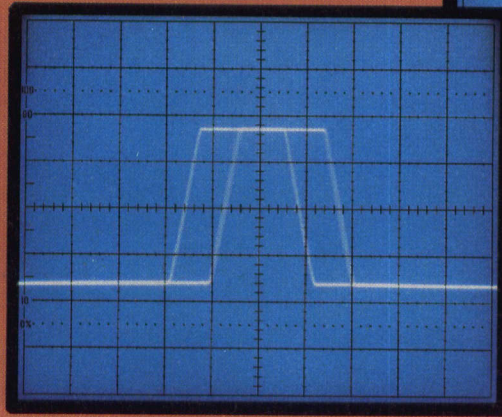
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*Thomas Seim, a development engineer on the staff of Battelle-Northwest, is responsible for microcomputer and mini-computer system design and development in materials research, data communications, and reactor safety. He holds BS degrees from Oregon State University and an MS degree from Washington State University.*



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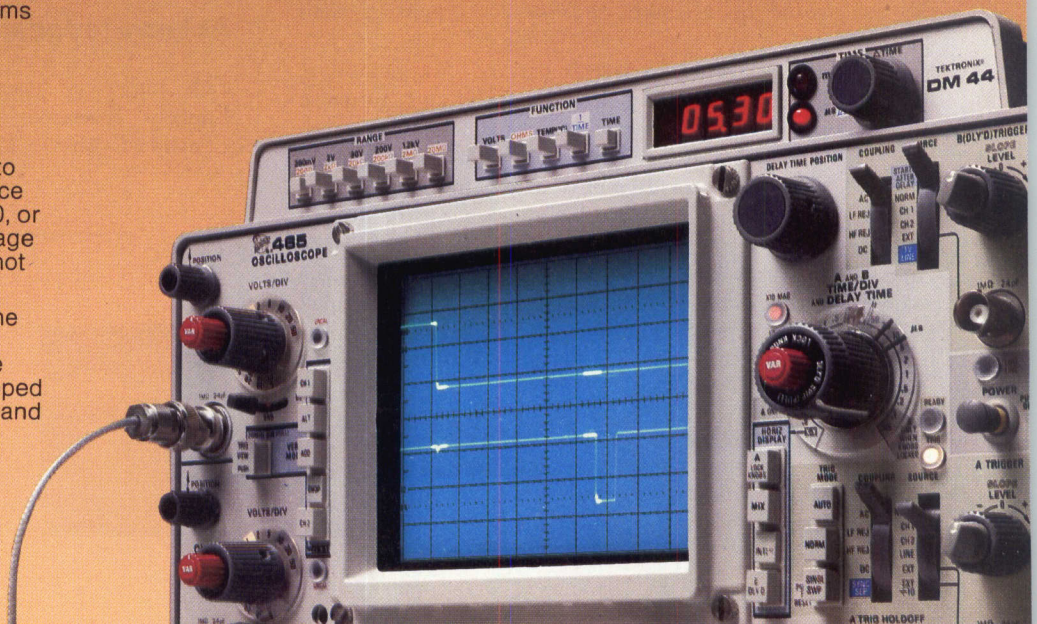
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**Beginning the design of a digital system with a good functional analysis, and progressing to logically increasing levels of detail, can lead to an orderly, highly structured, modular design**

# Top-Down Design Streamlines Digital System Projects

**Matthew L. Fichtenbaum**

**GenRad Incorporated\*  
Concord, Massachusetts**

Digital logic elements, very well characterized and with few "black-magic" device dependencies, approach the concept of the ideal device. Because of this near perfection, one might infer that design of arbitrarily complex digital systems is straightforward and can be executed quickly and efficiently. In fact, large systems too often turn out chaotic in nature, a patchwork of small designs rather than a single conceptually-integrated large design. As a result they are unnecessarily difficult to analyze, design, debug on paper or in hardware, or later modify and expand. Given the amount of work absorbed by these activities over the life of a design, additional planning and design seem well worth the effort to improve the result.

Design of large digital systems is strongly analogous to design of large computer programs. Difficulties of organizing and managing such programming projects have long been recognized, and with this recognition has gone much effort in developing tools and methodologies to help. One technique, top-down design,<sup>1,2</sup> is directly applicable to the design of logic systems, and offers to such systems the same benefits that it does to programming.

## Procedure

Concisely stated, top-down design starts a solution at the highest level, or most global view, of a problem, and proceeds downward to levels of increased detail only after the analysis and decision process has been

completed at higher levels. Decisions made at any given level are based upon information identified at higher levels, and affect lower-level problems as yet unattacked.

A set of discrete levels of decomposition may be chosen that makes sense for the general problem of digital system design, and a procedure defined based on this choice. An example of such a procedure is:

- (1) Analyze the problem on a totally functional level; describe the behavior of the system to be designed in terms of features of the problem, not of some supposed solution.
- (2) Identify from this description the functional elements that are required to implement a solution. For example, data elements need storage places, a string of decisions implies a sequencing element, and so on.
- (3) Define interfaces among identified elements, again functionally in terms of communications required between elements. With these interfaces defined, drawing a complete *functional* block diagram of the intended system should be possible. Some choice of the approach to implementation of each block may be required or desirable at this stage, but actual implementation occurs later.
- (4) Realize interfaces physically, identifying trade-offs that exist and choosing among possible realizations so as to attack the trade-offs coherently. This

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\*Mr Fichtenbaum is currently on leave of absence to the Dept of Electrical Engineering, Linköping University, Linköping, Sweden.



physical realization may take the form of establishing a set of real specifications for the interfaces; for example, numbers of bits and logic polarity for digital data, definition of control signals and procedures for handshaking sequences between blocks, analog signal levels and frequencies, and so on. In general, different parameters can be traded off against one another, for example, the choice of a high speed serial data channel or several parallel data lines, but the scope of considerations for any trade-off is limited to a single functional interface as defined in the previous step.

(At this stage, if the system is complex, some elements may require further decomposition, using the same procedure. Following the last such decomposition, functional behavior of the entire system is known; therefore functional behavior of each individual block is also known, and physical interfaces among blocks are defined. Each block thus represents a well-defined implementation problem in its own right.)

(5) Implement individual blocks, performing these implementations with whatever degree of mutual independence is most natural.

These five steps reduce the initial system, far too complex to think about in detail, to a group of separated small blocks, and delay implementation decisions until they can properly help define a solution. Now the small blocks can be approached as individual design projects, while the ultimate solution is not artificially constrained by prematurely forcing certain paths and ruling out others.

## Example

The approach is easily illustrated by its application to a design problem. Although the particular problem is small in scope, the top-down technique is fully applicable and the solution's simplicity makes it easy to understand.

The system to be designed is a telephone-dialing machine (Fig. 1). This device will have a mechanical-switch keyboard, similar to that of a pushbutton telephone, through which the telephone number to be dialed is entered. When the user pushes an eleventh button, "Dial," the number is converted to a sequence of dial pulses (Fig. 2) like those of a conventional rotary dial sequence. If the called number is busy, or the connection is not completed, the number may be dialed again simply by pressing the dial button. Telephone numbers may range in length from one digit ("0" for operator) to eleven digits (1, area code, number); and the dialer must accept keyboard entries as fast as they occur.

Design progresses according to the defined procedure:

### Step 1: Functional Analysis

Partial description of the system must be completed, perhaps in this way: A keyboard contains 10 keys for the digits 0 through 9, and an eleventh key, "Dial." A telephone number is entered as a string of 11 or fewer digits, and stored internally. Pressing the Dial key terminates the digit string, recalls the digits in the order in which they were entered, and produces a series of dial pulses corresponding to each digit. Pulse

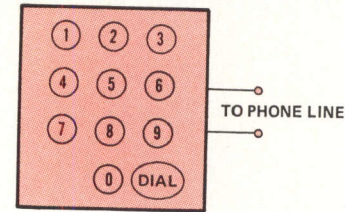


Fig. 1 Top of design. Telephone dialer, at level of detail represented by verbal description, is the first step in top-down design

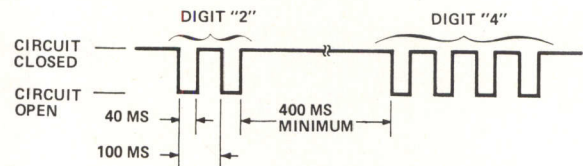


Fig. 2 Dialer output. Pulse sequence as generated by dialer. Each digit is represented by the corresponding number of pulses on the phone line, with pulse period, pulse duration, and interdigit spaces meeting telephone industry standards

rate, duty ratio, and spacing between digits conform to the parameters of a rotary dial. After the pulse string for all digits has been generated, it may be regenerated by again pressing Dial. Pressing any digit key after pressing Dial erases the stored number and begins entering a new number.

### Step 2: Element Identification

Initially, the only elements of the dialer appear to be keyboard and phone line driver. These form the complete system's external interfaces, and are explicitly mentioned in the definition. A more detailed examination of the definition, however, shows that other elements are necessary.

For example, input and output of telephone numbers imply that memory is needed to store the number as the digits are entered. Entering and recalling the digits, one at a time, implies a sequencing or addressing mechanism to keep track of their order. The variable-length string requires the dialer to keep track of the number of digits in a sequence, with a counting mechanism.



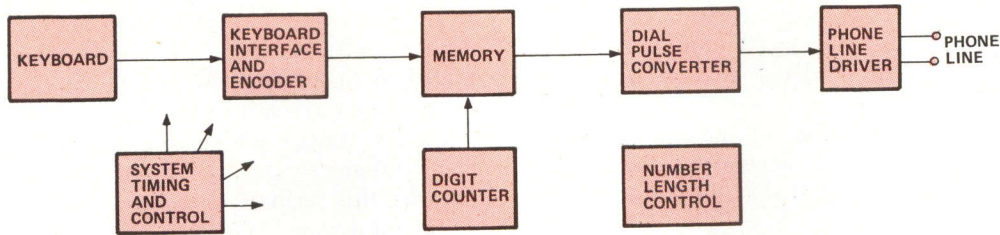


Fig. 3 Functional elements. Next step in dialer design defines functional elements and their logical interconnections. At this stage, design is still conceptual, without considerations of implementation

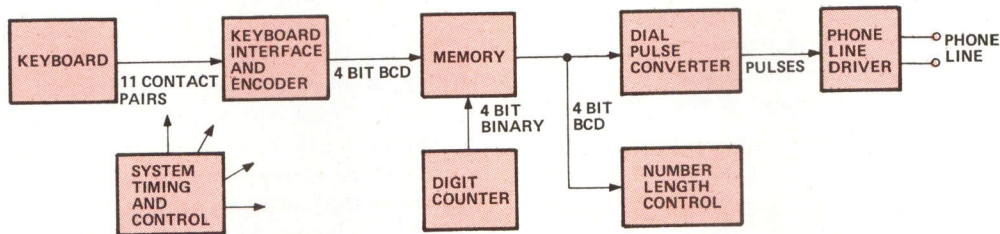


Fig. 4 Interface specifications. This is first stage where any implementation decisions are made. Data types and interconnections have been chosen, and each block's interface specifications and functional behavior are known

Two additional logical elements of the dialer are the interfaces at its input and output ports. These connect its internal elements to keyboard and telephone line driver, and convert voltage levels, data formats, etc as required by the choice of implementation.

Finally, any system that performs a sequential task must include some internal timing and control. Since this is associated with the complete system rather than with any single block, it should be considered as a separate element.

These elements, shown in Fig. 3, are functional. Some may be combined at implementation; other single elements may be implemented as multiple blocks.

### Step 3: Interface Identification

In such a small system, interface identification is simple. The keyboard communicates with the keyboard interface, which in turn sends data to the memory. Memory is addressed by the digit counter and sends its data to the phone line driver interface. The number length control's exact interface is still unclear, as the necessary information cannot be identified until the working of

this block is better known. The timing and control element communicates with all elements. These interfaces are also shown in the functional block diagram (Fig. 3).

### Step 4: Interface Realization

Interfaces (Fig. 4) are also quite simple to realize. By definition of the keyboard, keyboard-to-encoder interface must be the switch contacts themselves—one pair for each of the 11 keys.

First major implementation decision is at the encoder-to-memory interface, which depends on the form in which data are stored. Some possible choices for storage are binary-coded decimal (BCD) representation, keyboard row-and-column code, 1-of-11 code, and pulse string code for the whole number.

BCD requires four bits per digit. Because the keyboard has four rows and three columns, keyboard location code requires two 2-bit fields, or another four bits per digit. Eleven bits per digit are required for 1-of-11 code while dial pulse string, including inter-digit spaces, requires a maximum of 289 bits for the



whole number. BCD and keyboard locations seem preferable, since they imply the smallest memory requirements. Since BCD is a familiar code, it is best for this example. However, keyboard location is equivalent to the standard format for pushbutton telephones, and might be preferred for a dialer version that uses tone dialing, as these telephones do.

The most direct implementation of the interface between memory and dial pulse generator reads data from memory in the same format that they are stored, namely, 4-bit BCD.

The maximum of 11 digits can be specified by four binary digits in the digit-counter-to-memory interface. If the memory is a random-access device, these four bits are its address.

As previously mentioned, interface to the number length control depends on implementation of the block. One method of handling variable-length numbers stores the length of the number in a register, and determines with a comparator when the proper number of digits have been dialed; in this case interface to the number length control is the output from the digit counter. A better method takes advantage of the 4-bit representation of 10 digits; one of the six unused codes is an end-of-number mark that appears after the last digit. Although this method requires one additional memory location to store the end mark, it requires less hardware. This interface is thus the data output from memory.

### Step 5: Block Realization

In this small system the blocks are all straightforward. One workable set of realizations is 11 mechanical switches for the keyboard; a 10-line to 4-line priority encoder chip for the keyboard encoder, plus a few gates for the eleventh button and a one-shot to de-

bounce key activations; a single 64-bit TTL chip, organized as sixteen 4-bit words, for memory; a 4-bit TTL chip for the digit counter; a gate to detect the end mark code; a 4-bit counter to convert each BCD digit to a train of pulses, which themselves are generated in the timing and control block; and an optical isolator and transistor to drive the phone line.

Finally, timing and control can be implemented along many different paths. In keeping with an orderly approach, this example's control logic is implemented as a finite-state machine, using standard well-documented techniques.<sup>3,4</sup> Control of the dialer requires 14 states, with a maximum of one decision per state. The detailed block diagram of Fig. 5 includes the machine's decision inputs and control outputs.

### Advantages of This Technique

By forcing the designer to have a clear comprehension of a project before undertaking any one part, the top-down approach encourages him to think through his whole approach at the early stages. In addition to producing a more orderly design, this approach uncovers a large number of potential bugs and special cases, which can be corrected on paper, before any hardware is built. A design project that is based on a completely unworkable idea can begin, but the fundamental wrong assumptions will be discovered early enough to permit a new start rather than requiring the system to be patched in the late stages at high cost.

A high degree of modularity results almost automatically from use of the top-down approach to design. Because boundaries around its blocks are clearer, and interactions between blocks are fewer and better-defined, the modular design that results is easier to make work initially as well as to understand and fix

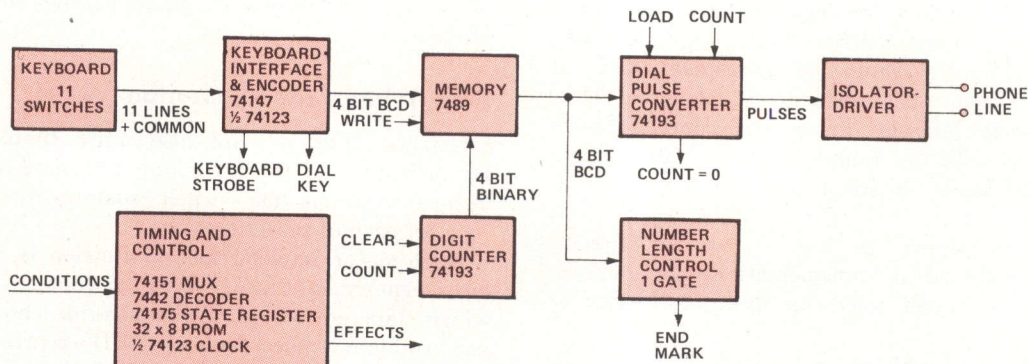


Fig. 5 Complete system. At final stage each block has been realized and implementation is essentially complete. All levels of block diagram are identical in form; level of detail and amount of information presented increase at each stage



in the field. Furthermore, the modular structure increases the likelihood that part of a design, from a concept to a physical block, will be usable in a later system. In the example of the telephone dialer, a change to tone instead of pulse dialing requires only the dial pulse counter to be replaced with a digitally-programmed tone generator, and the phone line driver to be modified for the different kind of signals. An extension that stores several frequently-called numbers requires only expansion of the memory and a means of additional addressing to select a particular number. Both additions fit well into the existing structure.

Developments in technology often motivate re-implementation of an existing design, to obtain increased performance, improved reliability and serviceability, and lower cost. Under the top-down approach, implementation is important only at later design stages; therefore re-implementation repeats only a small fraction of the original design effort.

### Some Larger Benefits

Other advantages of the approach extend beyond any one project. For example, the design engineer can be more orderly and productive, while the engineering manager can identify people who are the most creative system architects, and have them perform the top-level stages of all system designs. Other people can work on the implementation, while still using the approach of the "super-designers."

As more people work on a project, more time is spent communicating, and more administrative effort is required to coordinate their efforts.<sup>5</sup> Thus time and effort are much reduced by the top-down approach, because it separates a large system design into multiple small blocks whose specifications are well defined. When each block is implemented by a smaller team, their need for communication is much reduced.

An orderly design approach provides a good framework for transferring information about the inner workings of a system. For example, increasing levels of design detail parallel the structure of good documentation (overall purpose, general structure, individual detailed description), which simplifies documentation of projects (and thus encourages engineers to do the documentation). Functional areas outside of engineering, but needing engineering contact, such as technical writing and field service groups, may understand new designs more easily when they are presented in this logical order; the same is true of corporate management or a design review committee when it is necessary to justify a design to them.

Another important area of information transfer is education of new or unfamiliar people. An inexperienced engineer might work initially on later stages of a design project, where most decisions have been made and approaches are constrained. When such a person achieves more freedom and responsibility, he or she can progress to the earlier design stages. At all levels, the engineer builds on the previous work of people of greater experience, and from their use of a logical, consistent design methodology he becomes increasingly skilled in the same techniques.

Value of this design approach is illustrated by GenRad's experience with an instrument, the 2205 CRT Display Panel. This is a mostly digital system of moderate complexity which displays alphanumeric and graphic data. It is used in automatic test and measurement systems to communicate with the system's operator.

When the design of this system had progressed to drawing of full schematics, next step was to build a wirewrapped breadboard. Probably because of the design's good logical organization, design errors which were found on the breadboard were relatively minor in nature. Their correction required no changes to the display's fundamental organization and operation. A major part of the design effort went into the paper design stages—debugging and checking the breadboard consumed only about three weeks of work.

Availability of the functioning breadboard on a test system led to many suggestions from users for added features and capabilities. After a series of discussions identified a list of desired changes, these changes were easily incorporated into the design, again taking advantage of the logical organization and modularity.

### Potential Pitfalls

Top-down design is not a cure-all. As with any design methodology, the primary designer must be fully competent to do the job, and each subgroup's work must still be checked and approved by a designer who understands the overall objectives. Even when these conditions are present, application of any formal methodology to design can cause problems in at least four areas:

(1) Many designers are creative, highly individualistic people who have evolved their own styles of work. Bringing such people into conformance with any externally dictated style can precipitate problems of authority and control that require a skilled manager to handle.

(2) The increased independence of implementation groups in a top-down structure requires the overall design manager to monitor each group's activity closely. Small changes in specifications, made by one group for the sake of its module, may have major effects on another group or on the overall system. Only through sufficient, knowledgeable coordination will such ripples dissipate smoothly rather than wreaking havoc on the final result.

(3) An engineering manager can easily lose sight of the project objective, concentrating on top-down design as an end in itself. Proper design engineering management must concern itself primarily with the quality of the design and its conformance to project objectives, and only secondarily with the methodologies used, to insure that they contribute to these objectives.

(4) There will always be cases where a device can be built more cheaply or with higher performance at the cost of obscure or less general design. The professional engineer who recognizes these trade-offs among cost, performance, understandability, and potential later value can resolve them with the best choices for the overall system.



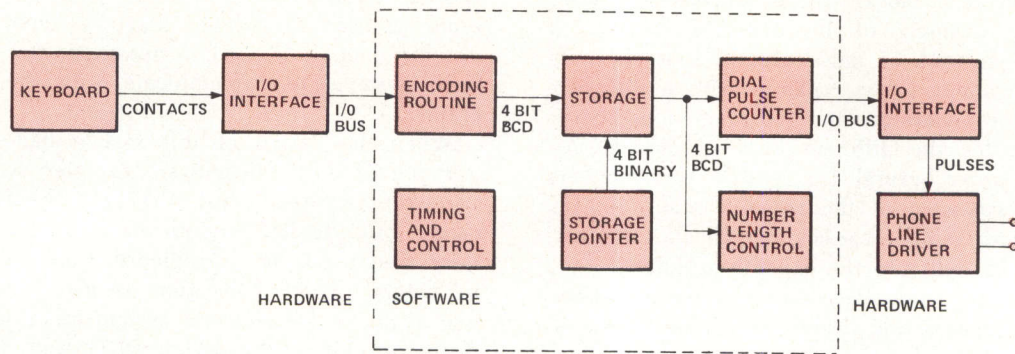


Fig. 6 Software version. When a microprocessor and its program replace hardwired dialer logic, design remains fundamentally unchanged. Although the same functional elements are present, they are implemented as programmed routines instead of logic networks

## Software and Hardware

Top-down design was first formalized in the context of computer programming. Programs were "ideal devices" long before digital circuits were, and the problems of maintaining order in large system designs surfaced first in software.

Top-down design, however, does not distinguish between hardware and software design at all—the choice of one or the other is an implementation decision. Indeed, digital hardware and computer programs have far more in common than the applicability of a design technique. Although historically the two areas have been treated separately, they are very comparable as digital system implementation tools. Availability of inexpensive integrated-circuit processors has increased the importance of being able to implement some part of a system in software.

Top-down design in software as well as the hardware-software choice as an implementation decision can be illustrated with the telephone dialer. To do so, it is implemented with a microprocessor and program (Fig. 6). The two devices at the extreme input and output—keyboard and phone line interface—remain unchanged; the rest of the system is implemented in software.

The block diagram remains fundamentally unchanged. The keyboard encoder, now a programmed procedure, still transforms a keystroke into four bits of BCD data to be stored in a 16-location memory, which is now an area in the processor's main memory. It is addressed by means of another memory location. Even the timing and control block is a programmed routine, but it is the same finite-state machine implemented as a program rather than in hardware.

One point in favor of top-down design may be made more specific in a very significant way, namely, that implementation decisions are postponed until the functional decomposition of a design into individual blocks is complete. The designer may then implement indi-

vidual elements in either hardware or software, to optimize the system. This decision deferral has a second-order benefit in that it encourages the hardware designer and the programmer to become more familiar with each other's area of expertise.

## Summary

The top-down approach to system design is by no means the only workable way to design a digital system, nor will it in itself guarantee a good design. In fact, no set of design rules exists that can completely preclude a bad design. However, this approach does make it relatively easy to engineer good designs, communicate them to others, and implement them with a minimum of lost effort.

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Matthew Fichtenbaum is a senior development engineer at GenRad (formerly General Radio). He has been active in the design and development of computer-controlled automatic test equipment, and has worked on the design of intelligent terminals and CPUs. He holds BS, MS, and Electrical Engineer degrees from Massachusetts Institute of Technology.



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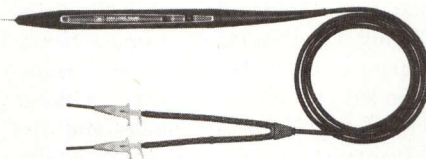
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# Simple Encoding Schemes Double Capacity of a Flexible Disc

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Irvine, California

*No matter how reliable or how fast a new storage device is, most designers want it to hold more data; getting it to do so is a matter of choosing the right encoding method and implementing it*

Technological advances in data storage devices almost always seem to involve increases in capacity. Other improvements are usually considered: shorter access time, smaller error rate, better reliability, and so on. Yet designers ask themselves this question more often than any other: "How can I squeeze more data onto this device?" Flexible discs are no exception.

The diskette used with the IBM 3740 is presently the de facto industry standard. With this medium, double density encoding offers the best hope for significant increases in capacity with present technology. However, this conclusion does not discount increasing the number of flux changes per unit of track length, which might be possible with a different substrate or coating on the disc; or increasing the number of tracks per unit of radius, or recording on both sides of the disc, which require different disc drive designs.

Double density encoding schemes enable system designers to double standard flexible disc capacity from 3.2M bits to 6.4M bits, unformatted, with the same number of flux reversals per inch on the disc. However, system designers should understand the trade-offs involved in selecting a particular encoding scheme. Various methods may be recommended to the designer; without knowledge of the advantages and disadvantages of each method, an intelligent decision is impossible.

## What is MFM?

With either single or double density schemes, the stream of data to or from the drive is divided into bit cells. Each bit cell is encoded as either 0 or 1. The key to various encoding schemes lies in the definition of 0 or 1 within a bit cell.

Single density applications use double frequency encoding. If a data

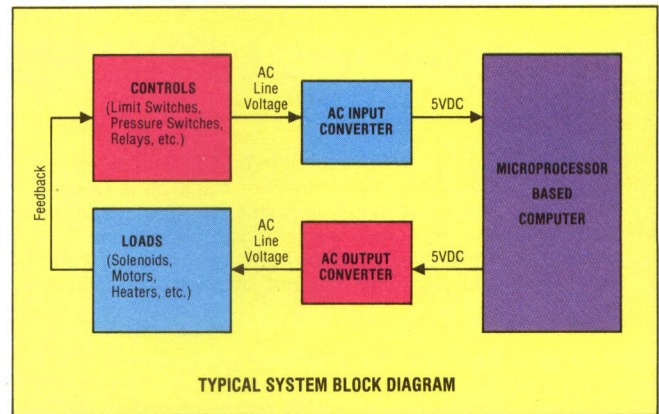
pulse is present at the center of a bit cell, that bit cell represents a 1. If no data pulse is present between clock pulses, that bit cell represents a 0. Double frequency arises from a clock pulse placed at the beginning of each bit cell, required to maintain synchronization in the event of a long stream of 0 bit cells. As a result, more than half of the flux reversals are clock pulses, not useful data pulses.

Modified frequency modulation (MFM) is also a self-clocking encoding scheme, which doubles the number of recorded data bits without increasing the number of flux changes. Rules for MFM encoding define 1 as a pulse occurring at the *center* of a bit cell, and 0 as a pulse occurring at the *beginning* of a bit cell, except when preceded by a 1. In that case, no pulse occurs during the bit cell for a 0 (Fig. 1).

Minimum time between pulses is 2  $\mu$ s for both double frequency and



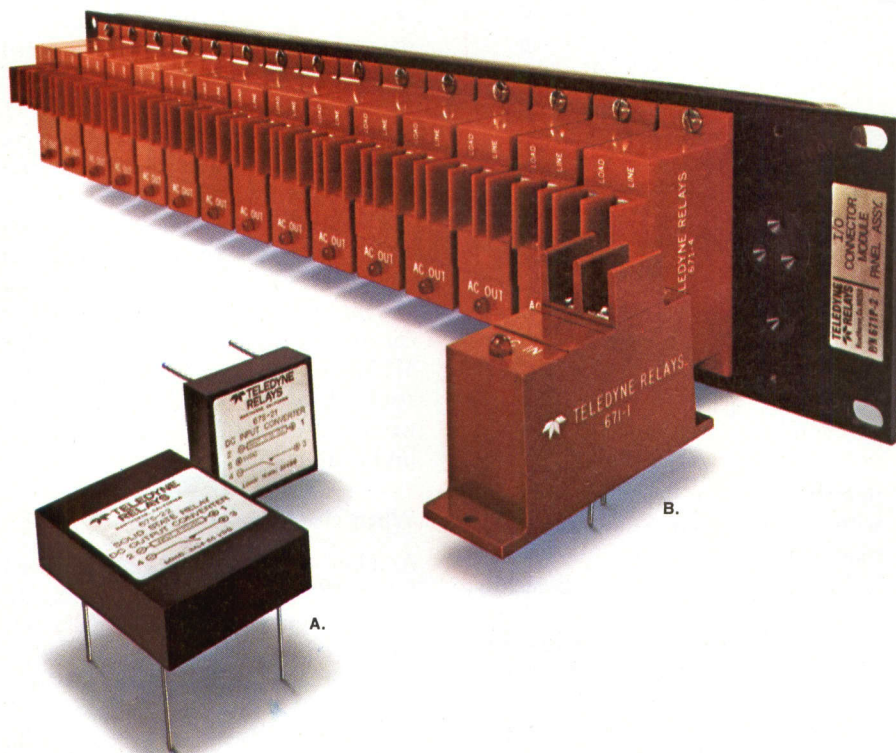
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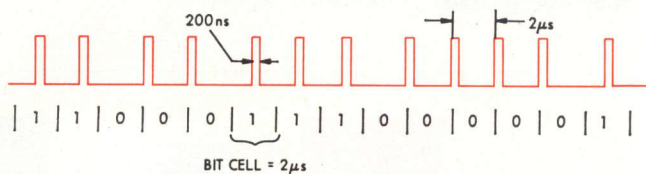


Fig. 1 MFM encoding. To double number of bits stored per linear inch of track on a flexible disc without exceeding medium's physical capacity to record flux reversals, some clock pulses can be eliminated. They remain primarily to delineate bit cells storing 0s, and therefore are not otherwise identifiable

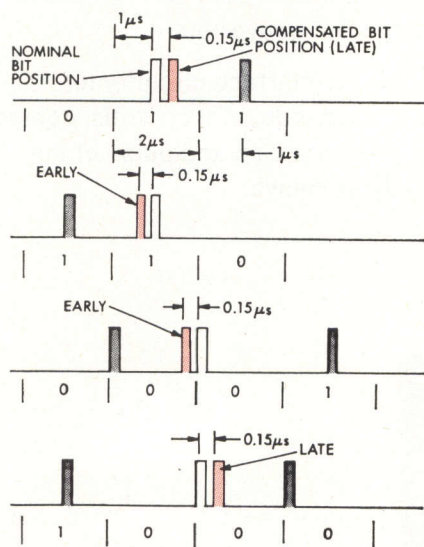


Fig. 2 Bit shift correction. Flux changes recorded at high density, which tend to move away from one another, can be kept in place by recording data slightly early or late. Thus the bit moves into its correct location, not away from it. Movement is apparent, not real; it is actually a time displacement caused by characteristics of magnetic medium and read/write head's response

MFM encoding, but data transfer rate for MFM encoding is twice that for double frequency encoding. Therefore MFM encoding is 100% efficient because of a 1 for 1 relationship between flux changes per inch and bits per inch recorded on the diskette. Double frequency encoding is only 50% efficient.

### Implementation of MFM

MFM encoding and decoding require additional components in a system,

namely, a write encoding circuit with write precompensation, and a read decoding circuit with a phase locked oscillator (PLO). Basically, the write encoding circuit transforms serial NRZ (nonreturn to zero) data from the controller into MFM encoded data pulses. The circuit usually is combined with the write precompensation circuit, which reduces the effect of bit shifting. This effect is much more critical at double density, since bit cell time is reduced from 4 to 2  $\mu$ s, and the allowable

window for detecting a data pulse is only half as wide as with single density.

Bit shifting occurs as recorded flux reversals apparently move from denser toward less dense regions of the track. Nothing actually moves, but magnetic field components surrounding two adjacent flux reversals interfere with each other, reducing the signal amplitude and making peaks seem farther apart than reversals. Because of this interference, shifting is most pronounced with certain data patterns (Fig. 2).

A write precompensation circuit counteracts this read data bit shift with an equivalent, but opposite, bit shift on the write data stream. Optimum compensation is approximately 150 ns implemented by transmitting NRZ write data to a data stream storage circuit with a capacity of at least four bits of data. A logical data sampler determines if each bit should be early, on time, or late, in accordance with rules implied in Fig. 2, and stated in the previous paragraph.

Meanwhile a parallel path transmits NRZ write data to an MFM encoder, output of which is early data. Two delays of 150 and 300 ns respectively yield on-time and late data. All three data streams are fed to the compensated data selector, which determines (for each bit cell) on the basis of input from the data sampler which data pulse becomes the MFM write data.

Providing the opposite function from the write encoding circuit is the read decoding circuit. Data stream at the output of the drive consists of 200-ns pulses encoded in MFM. A PLO synchronized to the read data stream generates 1- $\mu$ s windows centered on the expected bit location (Fig. 3).

### What is M<sup>2</sup>FM?

Another encoding scheme, derived from MFM, is termed modified, modified frequency modulation (M<sup>2</sup>FM). Its encoding rules define 1 as a pulse at the center of a bit cell, as in MFM, and 0 as a pulse occurring at the beginning of a bit cell, except when preceded by a cell containing a pulse (either 0 or 1). In that case, no pulse occurs during the bit cell for 0. An example of M<sup>2</sup>FM encoding shows that M<sup>2</sup>FM



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**TABLE 1**

**Proposed Standard for Group Code Recording**

Data Value	Record Value
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

generates fewer pulses during a stream of 0s. Since time between pulses has increased during a stream of 0s, nearly all bit shifting will occur on 1 pulses, not on 0 pulses. As a result, the PLO can synchronize on 0 bits only, ignoring all 1 bits. Therefore it is an extremely stable clock, which is a distinct advantage during read data recovery. However, the PLO may be more complicated than that used for MFM, and it would have difficulty synchronizing on a pattern with few or no 0 pulses.

An additional advantage of M<sup>2</sup>FM over MFM is that asymmetrical data recovery windows may be used with M<sup>2</sup>FM. Since 1 pulses have most of the bit shifts and 0 pulses have very little shifting, windows do not have to be equal in width. For example, the data recovery circuit could

allow 60% of the cell time for 1-pulse detection and 40% of the cell time for 0-pulse detection (0 pulse is essentially a clock pulse). However, this advantage could be completely negated because M<sup>2</sup>FM has greater potential for bit shifting than MFM due to the longer spaces between pulses.

**What About GCR?**

A third method of encoding, called group coded recording (GCR), avoids loss of synchronization in the data recovery circuit by not allowing more than two consecutive 0 bits, but at the same time requires no additional clock pulses.

To encode GCR, 4-bit blocks of data are translated into 5-bit blocks defined to eliminate the possibility of more than two consecutive 0 bits (Table 1). A decoder at the read output converts data back to its actual value. With no more than two consecutive 0s actually recorded, no clock pulses need be added.

Using the 5-for-4 code, data capacity of a standard flexible disc can be doubled by reducing the bit cell time to 1.6 μs. Assuming that the data transfer rate into the write encoder is 500K bits/s (as with MFM and M<sup>2</sup>FM), coding alone would increase the data transfer rate into the disc to 625K bits/s. The window for data recovery can be 1.6 μs wide, the full width of the bit cell, centered on the expected pulse location. Because of the wider data recovery window, write pre-compensation is probably not necessary.

Disadvantages of GCR recording are the complexity of encoding and decoding circuits, including a PLO, and band width of the read electronics. As shown in Table 2, GCR requires substantially larger band width than MFM or double frequency, a complication in its read circuits and a potential source of error.

In summary, although other double density encoding schemes have certain advantages, MFM gives the best performance with least complexity.

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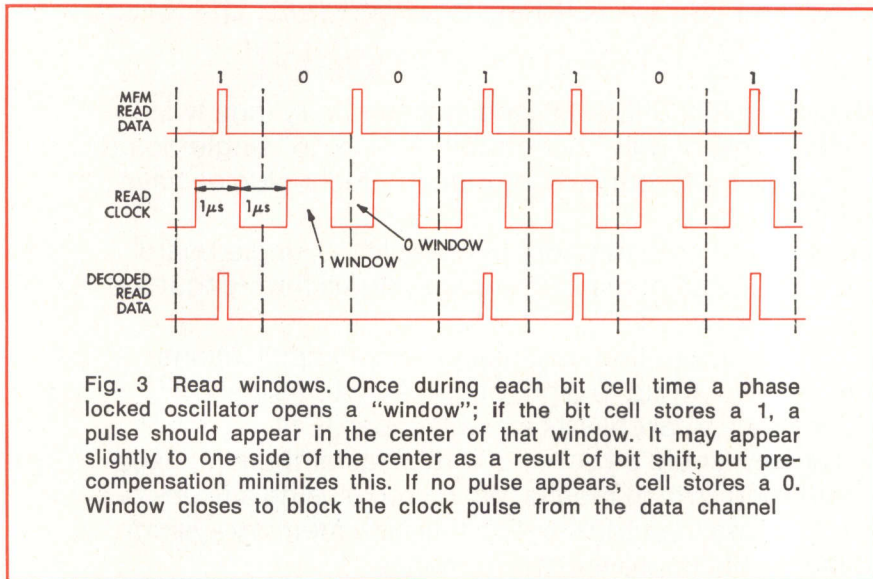


Fig. 3 Read windows. Once during each bit cell time a phase locked oscillator opens a "window"; if the bit cell stores a 1, a pulse should appear in the center of that window. It may appear slightly to one side of the center as a result of bit shift, but pre-compensation minimizes this. If no pulse appears, cell stores a 0. Window closes to block the clock pulse from the data channel

**TABLE 2**  
**Comparisons of Encoding Methods**

	Double Frequency	MFM	M <sup>2</sup> FM	GCR
Basic Cell Time	4 μs	2 μs	2 μs	1.6 μs
Possible Pulse Spacings	2 μs	2 μs	2 μs	1.6 μs
	4 μs	3 μs	3 μs	3.2 μs
		4 μs	4 μs	4.8 μs
			5 μs	
Frequency Components of Read Head Signal	250 kHz	250 kHz	250 kHz	312.5 kHz
	125 kHz	166.7 kHz	166.7 kHz	156.25 kHz
		125 kHz	125 kHz	104.17 kHz
			100 kHz	
Maximum Frequency Ratio	2:1	2:1	2.5:1	3:1



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# Minicomputer Peripheral Aids Program Debugging

Stephen R. Alpert

Worcester Polytechnic Institute  
Worcester, Massachusetts

*A highly portable debugging box is a significant tool to help correct errors in asynchronous programs*

For an assembly language programmer, one of the most difficult program errors to correct is improper reference or modification of data by an asynchronous procedure. This problem has been eased for minicomputers by a hardware assembly that allows the programmer to selectively monitor specific locations for the occurrence of a read or store operation, but does not require any internal modification to the processor itself.

A similar problem was uncovered, and a solution worked out long ago, for large general-purpose computers. Such computers usually are controlled by operating systems or other interrupt-driven programs, modules of which may communicate only via a special module or by

use of flag or semaphore bits. If some locations are inadvertently modified because a register was improperly initialized, the task of finding which instructions need correction becomes complex. In particular, the programmer cannot simply halt the processor periodically to check if the error has occurred. On the contrary, the processor must be allowed to run at full speed to permit peripheral devices to interact correctly with their associated interrupt routines.

In these large computers the solution was to add a hardware monitor that could perform the functions mentioned previously. In many cases the monitor also notified the user when a specific reference occurred, but took no further action.

Continued operation was important in such cases, because one erroneous reference might normally be preceded by many correct references to the location; halting the processor at each correct reference could eliminate the error by causing asynchronous routines to become skewed significantly in their execution times. When the error is thus not permitted to occur, conditions that accompany it remain obscure and cannot be corrected.

Design of such a hardware monitor, or debug box, of course, depends on processor architecture. Nevertheless, its principles apply as well to most minicomputers. The usual peripheral, say a teleprinter interface, interrupts the processor when an external event occurs. A



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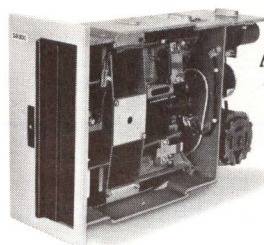
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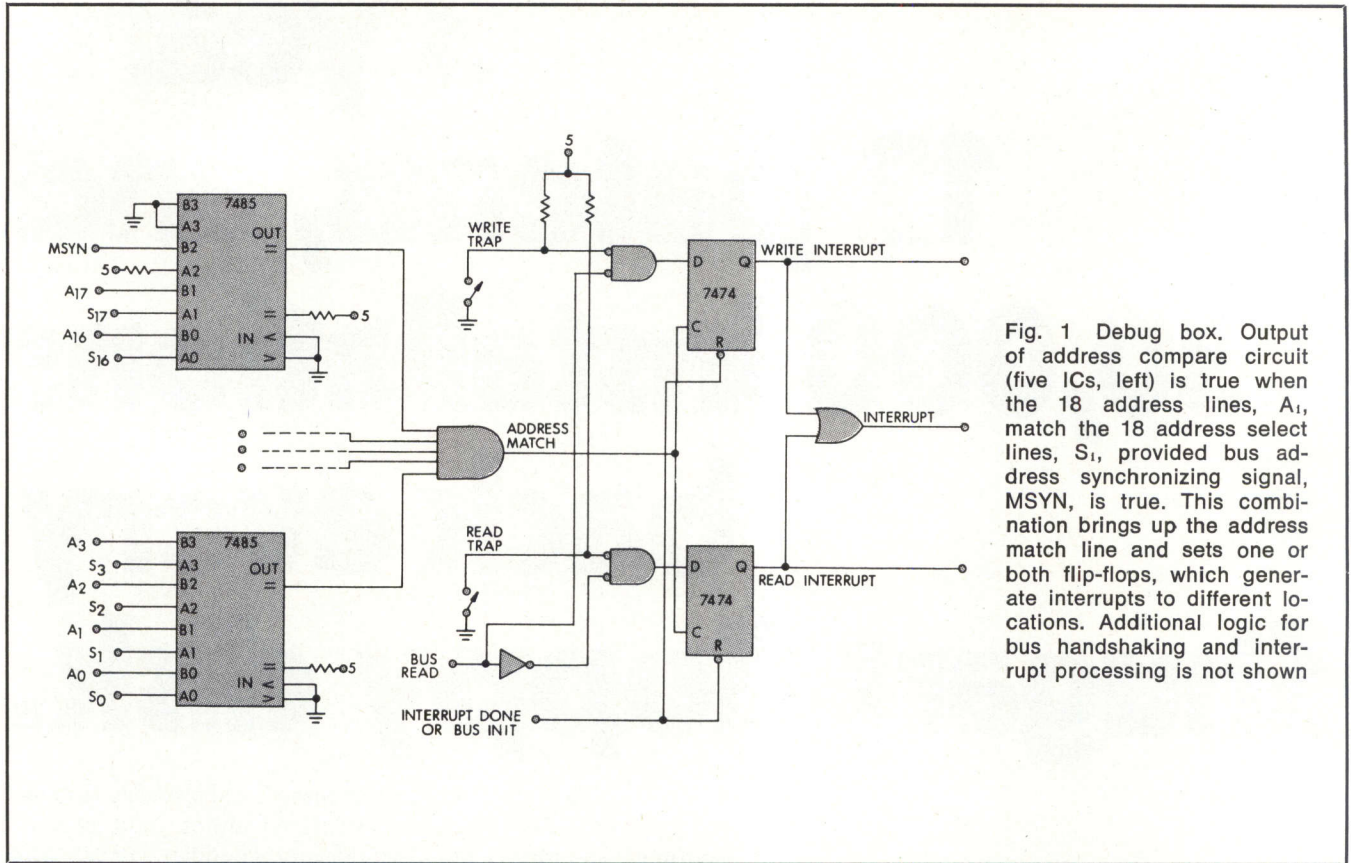


Fig. 1 Debug box. Output of address compare circuit (five ICs, left) is true when the 18 address lines, A<sub>i</sub>, match the 18 address select lines, S<sub>i</sub>, provided bus address synchronizing signal, MSYN, is true. This combination brings up the address match line and sets one or both flip-flops, which generate interrupts to different locations. Additional logic for bus handshaking and interrupt processing is not shown

WRITE TRAP								
R0	R1	R2	R3	R4	R5	SP	PC	PS
000000	142462	000377	141244	157602	014606	156304	156666	000240
READ TRAP								
R0	R1	R2	R3	R4	R5	SP	PC	PS
000116	156220	141000	001000	005752	142076	001000	014610	000010

Fig. 2 Interrupt output. Reference to a selected address causes machine status to be printed out for analysis

device handler can be designed to monitor the combination of CPU address lines and read/write control lines. When a specified address is generated in the required mode (read, write, or whatever), an interrupt is generated; the processor executes an interrupt routine that re-

ports the state of the machine when the reference occurred. The interrupt routine can halt the CPU if desired, but, as pointed out previously, a halt may be self-defeating; more likely the routine prints or records it on a disc file for later printing.

A debug box was constructed for a Digital Equipment Corp PDP-11 minicomputer (Fig. 1). Residing on part of one wirewrap board, the entire unit gets all its information from the computer's unified bus. It occupies one small peripheral controller slot and can be inserted with



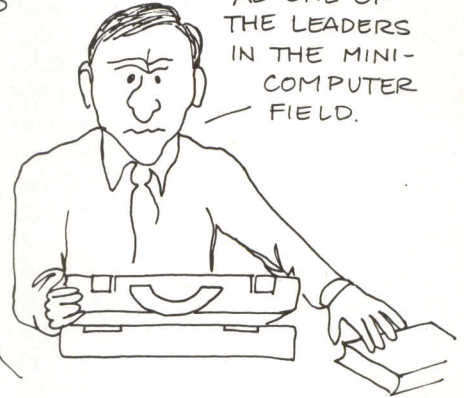
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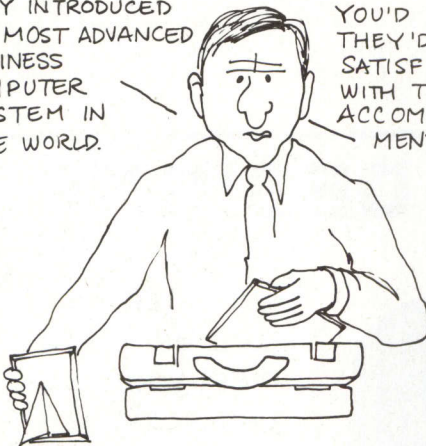


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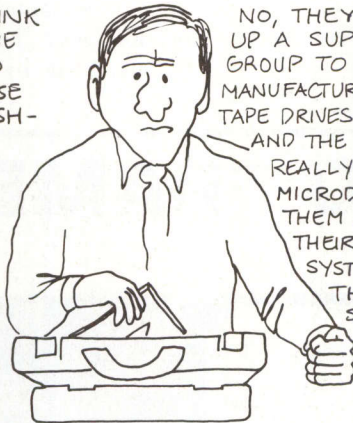


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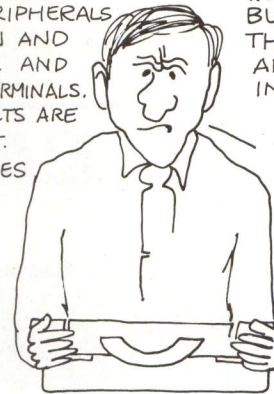
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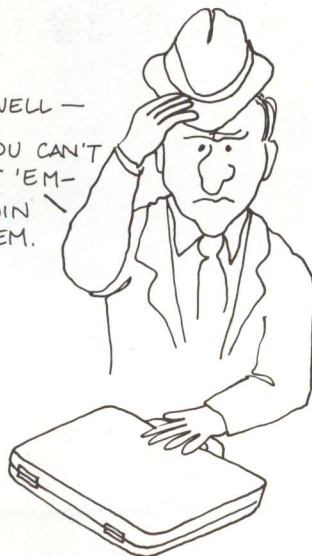


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## Microdata



no hardware modification, which makes the unit extremely portable and easy to use. Standard modules are available from DEC to implement address decoding or interrupt sequencing or both. Address comparators may be built with either exclusive OR-gates or quad comparators in parallel.

With thumbwheel switches the user dials in an address and arms the device to respond when that address coincides with a read, a write, or both. Under control of the debug box, the processor executes two routines in different locations—one for a read reference and one for write reference. The user's interrupt routines determine whether reference was made from an illegitimate part of the program, or if the location contains a value known to be in error. Action to be taken following this determination is entirely up to the user's routine and not predetermined by hardware. This device interrupts the processor at the highest interrupt level to catch all possible references, but it could be altered in software to catch only

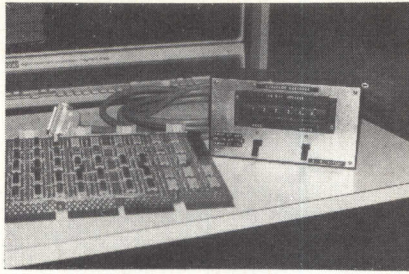


Fig. 3 Portable. Thumbwheel switches and other controls are housed in small chassis (right); remaining logic is on part of PC board. All signals and power originate in PDP-11 minicomputer (background)

those references that occur when the CPU is below, above, or equal to some specific priority level.

In a sample of teleprinter output from a simple program (Fig. 2), contents of several registers are displayed in octal notation following two references to memory location 14604—once when writing and once when reading. Since register 5 (R5) in the first line contains 014606, target location may have had something written in it by a

write instruction that used R5 as an address or index, incrementing it afterward (just before the interrupt took over). Similarly, in the second line the program counter (PC) contains 14610, suggesting that whatever was in the target location may have just previously been fetched as part of an instruction.

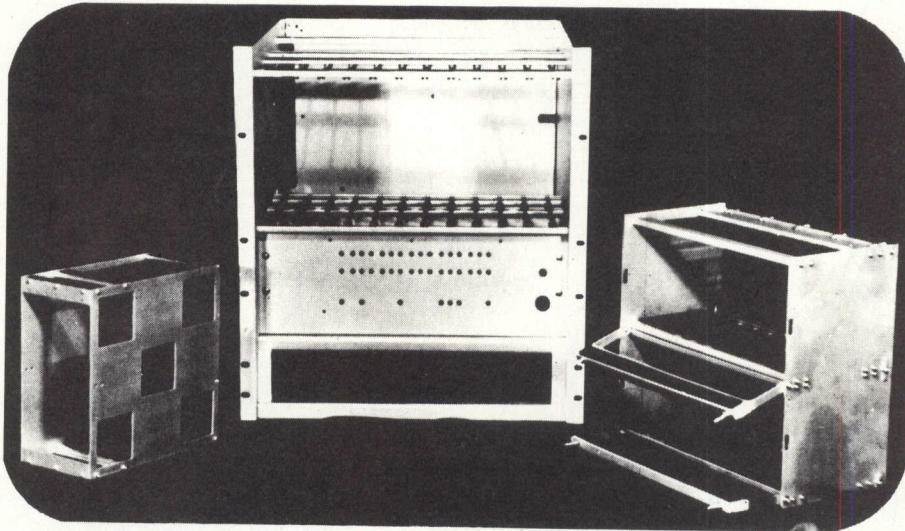
Modifications to this design could include an OR-gate in the address decoder, to catch a block of addresses; and a silo or first-in/first-out register of perhaps eight to 16 words, to store an immediate address history preceding the reference.

Tested and used extensively in a system with several devices operating asynchronously, the unit (Fig. 3) causes no apparent degradation of performance. Such a system also can be used successfully with microprocessors.

#### Bibliography

*PDP-11 Peripherals Handbook*, Digital Equipment Corp, Maynard, Mass, 1975  
A. T. Chen and R. S. Siebert, "A Data-Triggerable Program Debugging Aid," *Computer Design*, Sept 1973, pp 90-93

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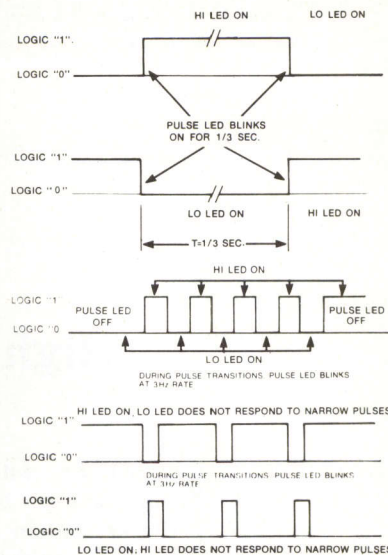
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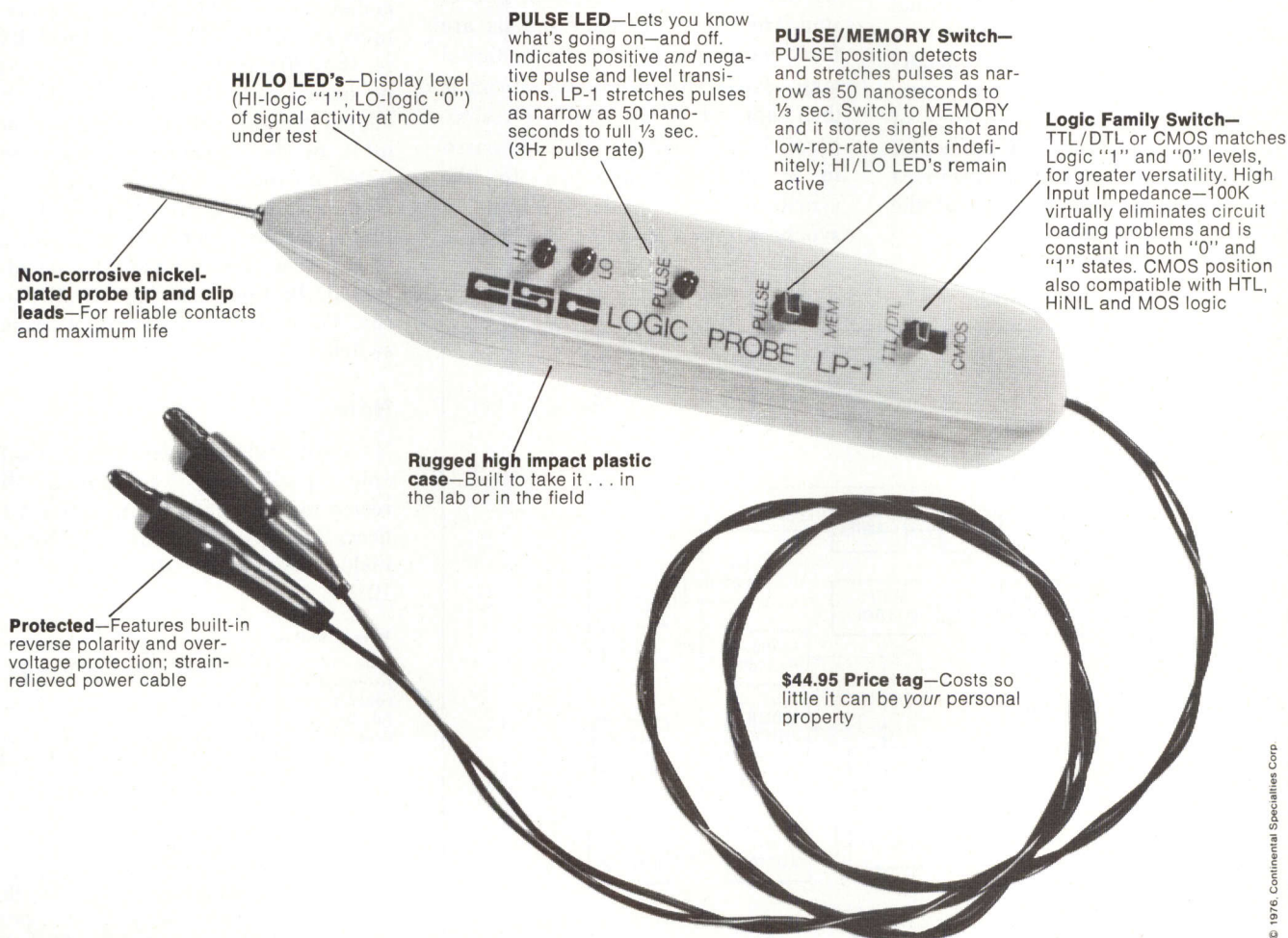
By setting the PULSE/MEMORY switch to MEMORY, single-shot events as well as low-rep-rate events can be stored indefinitely.

While high-frequency (5-10MHz) signals cause the "pulse" LED to blink at a 3Hz rate, there is an additional indication with unsymmetrical pulses: with duty cycles of less than 30%, the LO LED will light, while duty cycles over 70% will light the HI LED.

In all modes, high input impedance (100K) virtually eliminates loading problems, and impedance is constant for all states. LP-1 also features over-voltage and reverse-polarity protection. Housed in a rugged, high-impact plastic case with strain-relieved power cables, it's built to provide reliable day-in, day-out service for years to come.



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## High Speed Data Word Monitor

Digital data transmitted by data modems are usually in the form of fixed-length blocks. Blocks contain a synchronization code and, in addition to actual data, may contain data type codes, source codes, destination codes, serial numbers, and error codes. If the input data rate is lower than the transmission rate, the position in the block that normally contains data is filled with a fixed "filler" pattern. When receiving terminal equipment fails to process the data, the transmission equipment is usually considered at fault; thus it is necessary to make a visual examination of any portion of the block, in particular the identification codes discussed above. A high speed display of the bit pattern is required.

A small, portable, self-contained device that provides high speed display of the bit pattern of any selected portion of the transmission can suppress filler patterns so that the display is not updated, and can freeze the display so that a specific event may be observed in detail.

### How It's Done

As indicated in the diagram, bilevel standard clock and data signals are first converted to standard digital logic levels. The serial data stream is then applied to a 24-bit serial-to-parallel shift register and compared in a digital comparator to the synchronization code. When a synchronization code is detected, a

divide-by-N counter is started and pulses are counted until a selected event is reached; at this time, the data shift register contains the selected 24-bit word. Then the counter is stopped and the 24-bit latch is enabled, thus holding and displaying the selected word. The divide-by-N counter is programmed by panel switches.

When a fixed filler pattern is decoded and enabled on the front panel, updating of the display is inhibited so that the selected data word can be observed continuously. Additionally, a stop-bit select switch will inhibit display update when one selected bit in the 24-bit word changes from a logical 0 to a logical 1, so that a specific event, such as presence of an error status code, can be observed. In this instance, the display can be updated again by a panel switch.

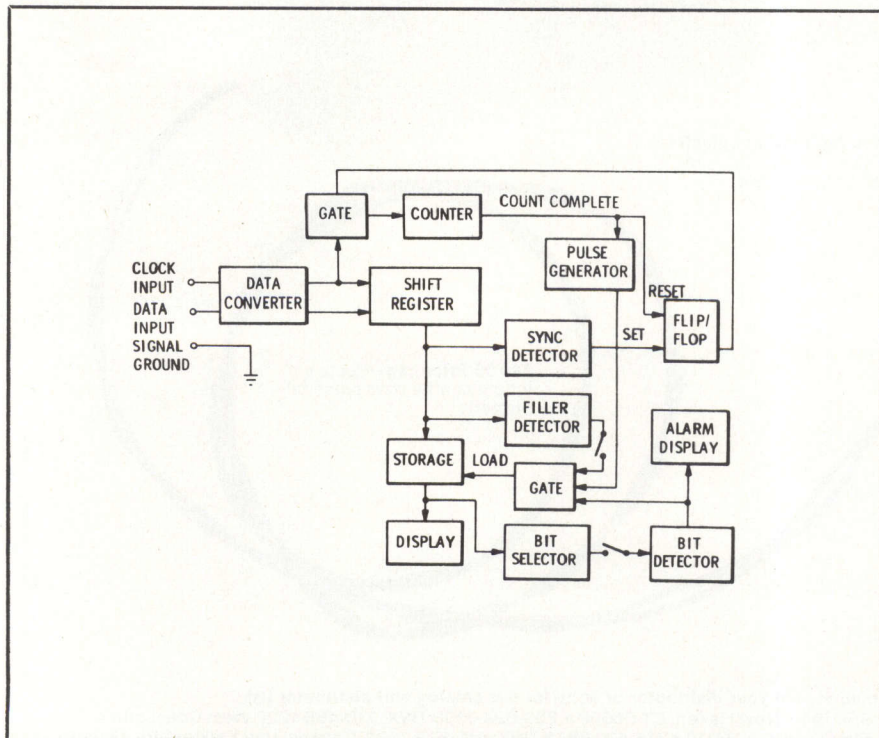
### Note

No additional documentation is available. Specific questions may be directed to: Technology Utilization Officer, Ames Research Center, Moffett Field, CA 94035. Reference: B75-10129.

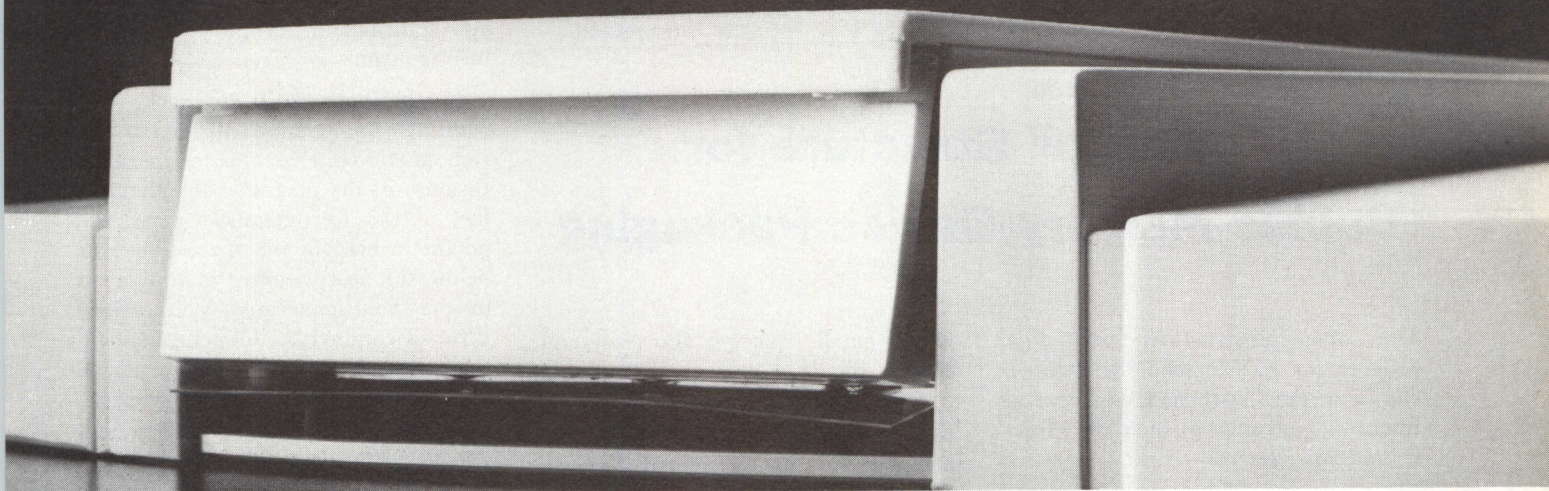
### Patent Status

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to: NASA Patent Counsel, Mail Code 200-11A, Ames Research Center, Moffett Field, CA 94035. Source: Manfred N. Wirth, Ames Research Center (ARC-10899).

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## Open Coil Structure for Bubble-Memory-Device Packaging

The open-coil-structure packaging concept for bubble memory devices, shown in the illustration, has several important advantages over the close-wound coil system.

(1) All memory and coil chips are separate and interchangeable. Indi-

vidual small packages for each coil are not required.

(2) Most interconnections in the coil level are eliminated by packing memory chip and associated electronics in a single structure.

(3) Coil windings are separated

from the device; therefore coil size can be independently adjusted to an optimum value in terms of power dissipation and field uniformity.

(4) Forced air cooling can be easily implemented, for better thermal equilibrium, as the whole structure is open.

In the open coil approach, coil windings are wrapped around a ferromagnetic plate such as ferrite plate. Because of the magnetic shielding effect of the ferromagnetic plate, the magnetic field in the space above or below the coil winding is equivalent to the field generated by a single layer of conductors. (When two identical magnetic plate coils are placed in parallel, the magnetic field between the plates is identical to that generated inside a close-wound coil.)

A rotating field network is achieved by winding two orthogonal windings around the magnetic chips and stacking a number of these chip coils in a bias structure. Bubble devices are inserted between these coils as illustrated.

This approach can be extended to bubble-memory-module packaging where a large number of chips have to be driven in several independent rotating fields. All memory devices and their associated electronics can be mounted in planes, called device planes, and all magnetic chip coils and their driver electronics can be mounted in separate field planes. Device planes are then inserted between coil planes and are placed in the bias structure. All memory chips under the same coil windings can be operated as an independent unit.

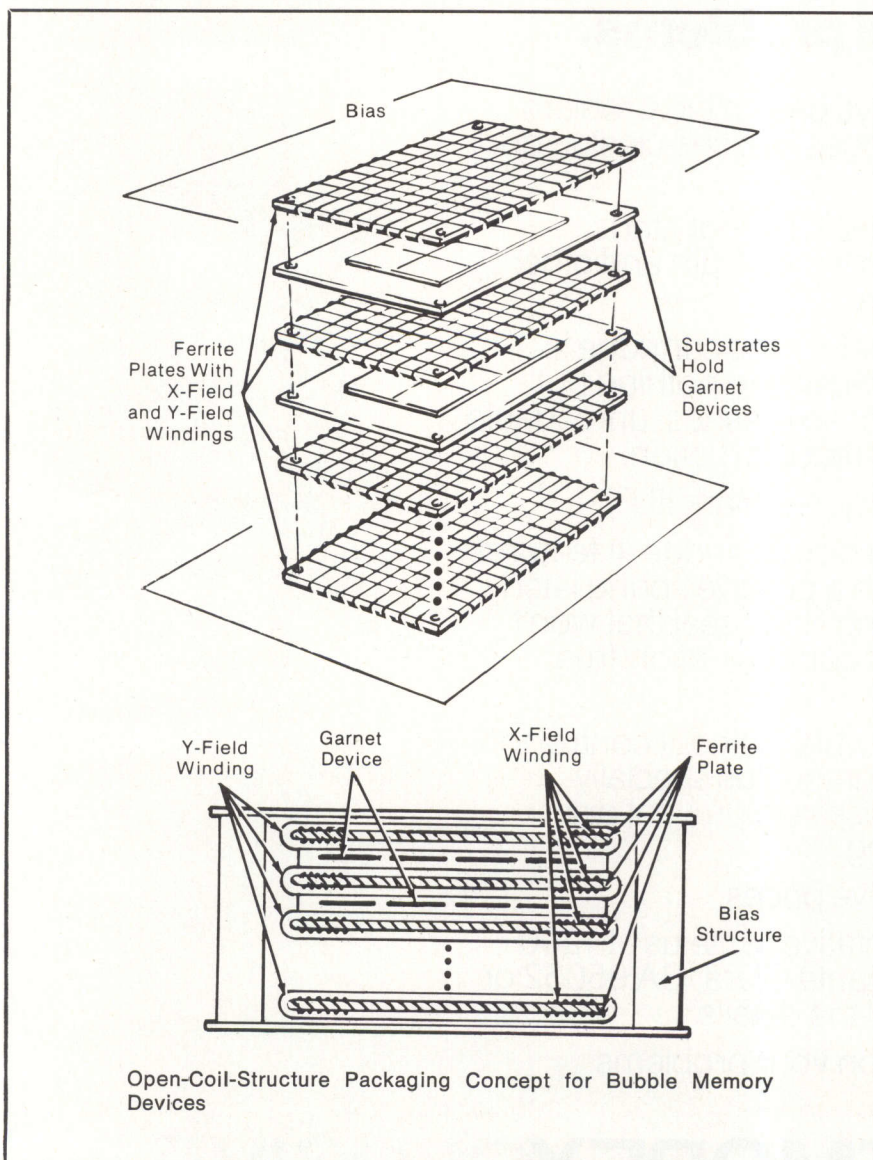
### Note

Requests for further information may be directed to: Technology Utilization Officer, Langley Research Center, Mail Stop 139-A, Hampton, VA 23665. Reference: B75-10219.

### Patent Status

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the Rockwell International Corp, 3370 Miraloma Ave, Anaheim, CA 92803. Source: Thomas T. Chen and John E. Ypma of Rockwell International Corp (LAR-11704).

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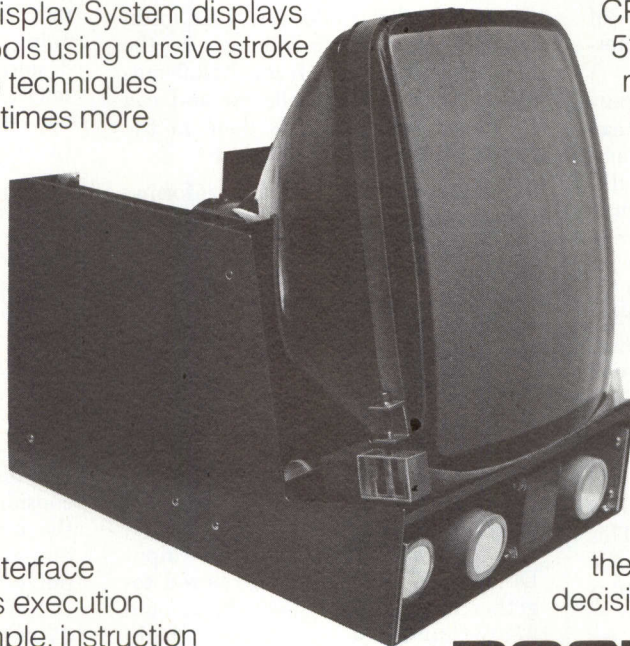


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## Microcomputer Interfacing: Interfacing a Digital Multimeter

Jonathan A. Titus  
Tychon, Inc

Peter R. Rony  
Virginia Polytechnic Institute  
& State University

David G. Larsen  
Virginia Polytechnic Institute  
& State University

This month, we shall discuss interfacing an 8080-based microcomputer to a versatile laboratory instrument, the Keithley model 160B digital multimeter with model 1602B digital output. This multimeter has been found to be an excellent example of how manufacturers can facilitate interfacing of their instruments.

The instrument is a general-purpose 3½-digit multimeter that can function as a dc voltmeter, dc ammeter, or ohmmeter. Twenty-six different ranges are provided in three modes of operation. Lowest range scales provide maximum readings of 1.999 mV, 19.99 nA, and 1.999 Ω. The 1.999-mV scale has an accuracy of ±0.1% of reading ±1 digit. Thus, a display reading of 1.000 mV will have an uncertainty of ±0.002 mV, or 2 μV. Highest possible readings associated with the three different modes are 1200 V, 1999 mA, and 1999 MΩ, with the megohm reading being accurate to only ±30%. This multimeter can be viewed as the digital complement of the ubiquitous multirange chart-paper recorder.

Basically a sophisticated analog-to-digital converter (ADC), the multimeter can handle most laboratory requirements for digital data acquisition, provided that the data acquisition rate is no greater than 1 data point/s.\* Switching between the 26 different ranges is performed manually. In the future, such switching will probably be performed by a built-in microprocessor operating under control of an external computer.

In the full interface circuit (see Figure), two OR gates and the SN74154 decoder generate three different device-select pulses<sup>1</sup> required to input data from the multimeter to the microcomputer. Note the IN input at pin 18 of the decoder. This interface circuit takes advantage of the fact that all outputs from digital output board are open collector and can be bused together as is done in the Figure. Bus can be defined as:<sup>2</sup>

A path over which digital information is transferred, from any of several sources to any of several destinations. Only one transfer of information can take place at any one time. While such transfer is taking place, all other sources that are tied to the bus must be disabled.

Notice how pins 16, 12, and 10 on the multimeter are connected to the same input (D7) to the microcomputer, such that these three pins are in effect bused together. Pins 35, 31, and 28 are bused together to input D6; pins 17, 13, and 9 are bused together to input D5; pins 36, 32, and 27 to input D4; and so on. Eight inputs to the microcomputer, D0 through D7, comprise an 8-bit data bus over which information passes, one group at a time, from multimeter to microcomputer.

In the definition of a bus, it is indicated that only one transfer of information can take place at any one time. In the Figure, this transfer is accomplished with the aid of three sets of two strobe inputs. When logic 0 is applied at strobes 1 and 2,

binary coded decimal (BCD) codes corresponding to the 10<sup>0</sup> and 10<sup>1</sup> digits are transferred to the accumulator of the microcomputer. Strobe signal for strobe inputs 1 and 2 is provided as a negative device-select pulse from channel 5 of the decoder chip. In a similar manner, strobes 3 and 4, and 5 and 6 permit the microcomputer to acquire the remaining output data from the multimeter. In summary, three device-select pulses allow strobing of 20 output bits of data from multimeter to microcomputer over a set of eight data bus lines labeled D0 through D7.

A simple program that accomplishes data transfer from multimeter to microcomputer is provided (see Data Transfer Program). Entire data acquisition and movement to registers C, D, and E occurs in 21 μs, fast when compared to the rate of 5 conversions/s by the multimeter. Clearly, considerable time is still available to the microcomputer to manipulate acquired data before new data are input into the accumulator.

Not shown in the Figure are eight 4700-Ω resistors that are the required pull-up resistors for the eight open collector bus lines, one resistor for each of the eight data bus inputs. One end of each resistor is tied to 5 V, and the other end to the bus line.

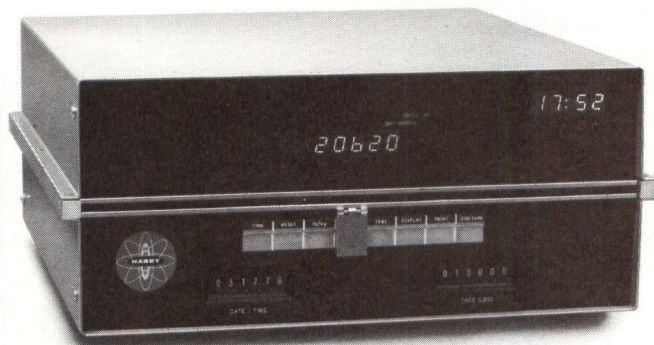
\*Settling time of the multimeter is about 2 s. Although five data conversions can be made each second, it may take about 1 s for the precision of a typical data point to reach 0.1 or 0.2%.



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The Model 2070 is a programmable, self-contained, data-oriented, NBS compatible industrial weighing system priced under \$3,000. It has the full range of standard features and a selection of sophisticated optional expansion capabilities. It provides display, drives printers, and interfaces with computers and process controllers. Motorola's MC6800 is the heart of the system.

## KRAUS INDUSTRIES, LTD.

MICRO-IP, designed around the microprocessor, introduced a totally new concept in data and control systems for self-service gas stations. Most of its standard features for complete station control were previously available only as options, or not at all. Kraus Industries credits Motorola's M6800 Family for this advanced system, and for keeping it price competitive.

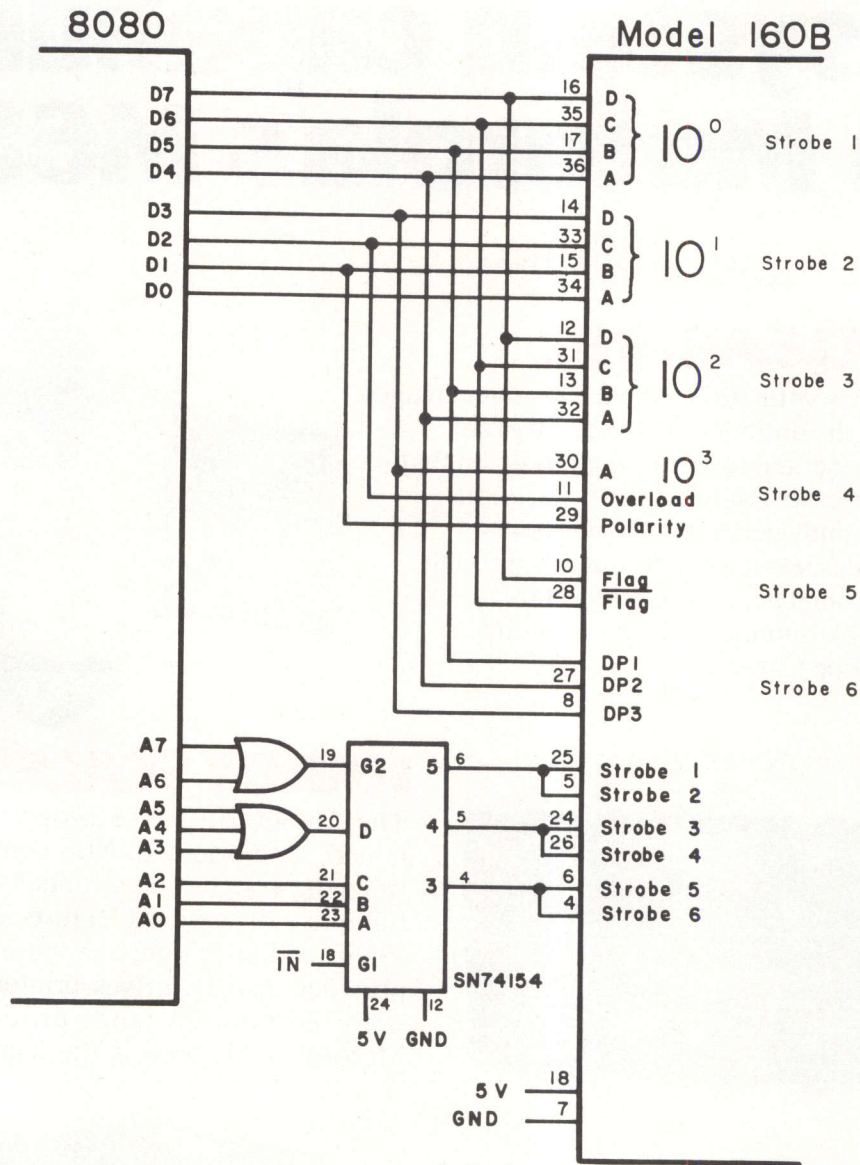


Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036



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Interface circuit between Keithley model 160B multimeter and an 8080-based microcomputer

These resistors are not included in the diagram because they can be added to the circuit board within the multimeter. The microcomputer data bus normally employs an alternative busing technique called 3-state busing. Interface circuit shown in the

Figure represents a marriage of the two busing techniques: open collector and 3-state. The resistors do add a load to the data bus, but this does not prevent other devices from being tied to the bus provided that each bus connection in the other de-

vices can sink, in logic 0 state, the additional 1-mA current produced by the pull-up resistor.

Previously we stated that the Keithley multimeter is an example of what manufacturers can do to facilitate interfacing of their instru-



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- Austria 425451 or 421675 • TLX 847-74737
- Switzerland 041-831043 • TLX 845-72231
- Netherlands 01720-94044 • TLX 844-34111



### Data Transfer Program

LO Memory Address	Instruction Byte	Mnemonic	Clock Cycles	Description
000	333	IN 5	10	Generate device-select pulse that strobes the $10^0$ and $10^1$ digits into accumulator
001	005	—	—	Device code for strobe inputs 1 and 2
002	117	MOV C,A	4	Move accumulator contents to register C
003	333	IN 4	10	Generate device-select pulse that strobes the $10^2$ digit, $10^3$ bit, and overload and polarity outputs into accumulator
004	004	—	—	Device code for strobe inputs 3 and 4
005	127	MOV D,A	4	Move accumulator contents to register D
006	333	IN 3	10	Generate device-select pulse that strobes the Flag, Flag, DP1, DP2, and DP3 outputs into accumulator
007	003	—	—	Device code for strobe inputs 5 and 6
010	137	MOV E,A	4	Move accumulator contents to register E

At this point, 20 data bits are stored in registers C, D, and E. The microcomputer can now take this information and manipulate it in different ways. With the aid of BCD digits and DP1, DP2, and DP3, it can determine the magnitude of the input decimal number. With the aid of polarity input, the sign of the decimal number can be determined.

ments. In this case, open collector outputs were provided for all 20 output pins on the model 1602B digital output board. Added cost was small when compared to added value of the instrument. We expect future instruments to be microcomputer-oriented in the sense that data bus outputs will be provided to permit direct interfacing of instruments to microcomputers via simple wire interconnections. Hopefully, these columns will encourage manufacturers to provide minicomputer- and microcomputer-oriented digital outputs, and also to document such outputs as was done with the 160B.

### References

1. D. G. Larsen, J. A. Titus, and P. R. Rony, "Generating Input/Output Device Select Pulses For Microcomputer Interfacing," *Computer Design*, May 1976, pp 196-199
2. *Bugbook III. Microcomputer Interfacing Experiments Using the Mark 80<sup>®</sup> Microcomputer, an 8080 System*, E & L Instruments, Inc, Derby, Conn, 1975

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

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## Logic Analyzers Monitor State Flow of Hardware and Software In Debugging Microprocessor Systems

Keyboard-controlled logic state analyzers are dedicated to the design and troubleshooting of systems using 8080 or 6800 microprocessors. Dedicated to one type of system or the other by choice of "personality module" (with others to be added), the HP 1611A analyzer is available from Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304.

When an analyzer is connected to circuitry, system activity can be displayed on the instrument's CRT directly in the alphanumeric mnemonics of the microprocessor's own instruction set. This can be done without interfering with the instrument under test. With powerful qualifiers, a real-time window can be framed around virtually any event, or set of related events—any desired sequence of system operations. At a point defined by the user, the instrument can halt microprocessor operations; then, if desired, transactions that follow can be controlled, in single- or multiple-keyed steps.

Trace is specified by entries on the keyboard, determining conditions that must be met for a trigger to occur. Specifications can be: appearance in the data stream of a specified address or data word; occurrence of a specified combination of 1s, 0s, or "don't cares" on the eight auxiliary probes; or a combination of address, data, and auxiliary-probe conditions.

However, instead of a simple breakpoint trigger, the user may choose ranges of addresses to be used, ie, "greater than or equal to," and "less than or equal to" limits on the address magnitude. Any or all trigger specifications can be modified further by requiring a predetermined "pass count" of up to 256 repetitions before trigger can occur. Finally, trigger Enable and Disable condi-

tions can be specified, establishing boundary conditions in which the selected window may appear.

Trigger causes a 64-transaction sequence to be stored for display. It can be made to occur at the beginning or end of the sequence, displaying events following or preceding the trigger. With trigger digitally set in-between, the user may study a mixture of before-and-after events in whatever proportion is desired. Before the instrument begins to trace, digital delay of one to 65,472 memory transactions can be imposed, after other conditions are met.

Alphanumeric information about the keyboard settings, as well as the data captured, appears on the CRT screen. As directed by the keyboard, the instrument traces and identifies one memory transaction after another. It stores 64 of these, displaying the top 16 transactions until scroll keys are used.

A switch selects either octal or hexadecimal data listing. Op code readout may be numeric, or alphanumeric mnemonics may be spelled out, as in the microprocessor manufacturer's programming manual.

Selective trace of only the occasions when preset trigger conditions are met can be made, as well as counting selected events and measuring true execution time against the analyzer's internal crystal reference. Readout is given directly on the display.

The analyzer itself, an 8080 microprocessor-controlled instrument operated from a keyboard, includes power supply, CRT, character generators, and controller in the mainframe. It also has 2K words of ROM. Most of the circuitry and all controls individual to the 8080 or 6800 version are contained in a personality

module. These are not plug-in; however, exchanging one for the other takes only approximately 15 minutes.

Connection to the system is through multiconductor cables and probes. Where circuitry is readily accessible, a clip over the microprocessor makes the connection; or a plug-in connector may be inserted in the microprocessor socket, with the microprocessor itself relocated to the probe. Eight auxiliary miniature probes are included for simultaneous connection as needed to qualify triggering or to trace events in the system outside the microprocessor bus. Circle 170 on Inquiry Card

## Dual Floppy Disc Drive Is Low Cost Peripheral for $\mu$ Processor Systems

Introduced as a standalone subsystem to interface with Data General microNova™ and Monolithic Memory  $\mu$ mini 2 and 3 processors, the 3190G system is a low cost package consisting of two floppy disc drives and single board controller. Ball Computer Products, Inc, 860 E Arques Ave, Sunnyvale, CA 94086 states that the system combines proven disc controller design and superior packaging to provide an efficient and economical solution to flexible media requirements. It connects to the I/O bus and does not have to reside within the computer. In addition, the chassis will pass the I/O bus to other peripherals, if desired. The compact unit occupies 7" vertically in a standard 19" rack.

Floppy disc drives feature storage capacity of 3.2M bits (IBM compatible), ferrite R/W heads, superior track seeking accuracy due to a positioner that uses 3-step movement track to track, dc motor with direct drive spindle for user speed control, and precision steel chassis for higher data reliability. Drive has start/stop time of 5 s maximum, seek time of 10 ms track to track, and transfer rate of 250K bits/s.

Drives are rated for 7.5M passes on any one track with heads loaded and in use. Packaging is with hinged drives, providing full access to controller and drive electronics while in operating condition.

Controller includes features such as read-before-write address verifica-



Microprocessor - controlled Logic State Analyzer for 8080 or 6800 microprocessor systems traces and displays memory transaction after memory transaction in its own mnemonics. Instrument is useful for both design and production debugging



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Comm-Stor is much more than just a bulk storage unit. It's a microprocessor based system which has capabilities ranging from batch processing to converting your dumb terminal into a complete file management system.

Comm-Stor automatically keeps a directory of user-assigned message names for ease in storing and retrieving data. The directory allows the user to retrieve a message or group of messages in either the

order it is stored or in alphabetical order by message name.

Comm-Stor will respond to commands from terminal and modem ports, and is operator configurable to specific system parameters such as English (or foreign) language commands, special codes, command set, control functions and RS-232 interface parameters.

**Some of the main features of Comm-Stor are:**

- User Configurable
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- Off Line/On Line Operation
- Up to 9600 Baud Operation
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- Current Loop Interface (optional)

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tion, polynomial divisor CRC, diagnostic mode, and individual write protect. Longest media life possible is ensured by automatically unloading heads when reading and writing operations are not in progress. Board interfaces up to eight disc drives and can also accommodate a real-time clock and teletypewriter interface.

Features are combined on controller logic board, which is either installed on a single CPU I/O sub-assembly slot or mounted within disc drive chassis, external to the microprocessor. Each chassis can accommodate two floppy disc drives and

the controller. External I/O bus cables, drive cables, and internal power supplies are included in the complete system, which is put through a comprehensive inspection, testing, and verification checkout program.

Either the company's DOS disc operating system compatibility or IBM 3740 media compatibility may be selected for each drive in the system under program control. This provides media transfer ability with IBM systems as well as operating system compatibility with the company's larger disc systems.

Circle 171 on Inquiry Card

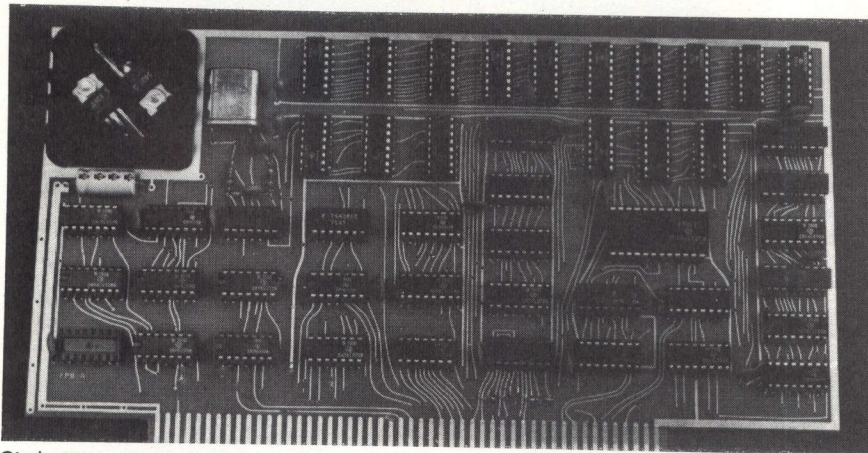
### Arithmetic FPU Permits High Speed Microcomputer Operation

Model A performs high speed add, subtract, multiply, and divide on BCD (binary coded decimal) format floating point values. Precision (up to 14 digits) is under program control.

Typical add/subtract time is 20  $\mu$ s, and multiply/divide time is 100  $\mu$ s, approximately 25 to 50 times faster

than operations performed by software on the host microcomputer. Replacement of software floating point routines also can save up to 1K bytes of memory.

Developed by North Star Computers, Inc, PO Box 4672, Berkeley, CA 94704, the single PC board device is designed for use with the 8080 microcomputer. Extended BASIC software utilizing floating point hardware is available.



Circle 172 on Inquiry Card

### Companies Sign Microprocessor Product Second-Source Agreement

Thomson-CSF, Paris, France has announced its intention to second-source the M6800 microprocessor family, as well as associated memories and circuits of Motorola Inc, Semiconductor Group, 5005 E McDowell Rd, Phoenix, Ariz. The agreement permits Thom-

son-CSF, a European electronics producer, to manufacture and sell present and future Motorola microprocessors and associated memories and circuits. Both companies have agreed to exchange information concerning developments in device production to insure interchangeability of products in serving their respective customers. Motorola products will be manufactured by Thomson-CSF's semiconductor division, SESCOSEM, in France.

### Display and Printer Expand Microcomputer Development System

Two peripherals available from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 for Intellect<sup>®</sup> MDS Microcomputer Development System permit utilization of system capabilities with maximum efficiency. Intellect MDS-CRT keyboard display and Intellect MDS-PRN printer can be used for all communications normally required during programming, software emulation, prototyping, in-circuit emulation, documentation, production test troubleshooting, and field engineering with the system. A teletypewriter can be used, if desired, for low speed I/O operations. Both peripherals are compatible with the diskette system, which contains its own controller and comprehensive operating software.

#### Keyboard Display

Features of the interactive console expedite debugging, program text editing, and assembly. The unit supports all I/O functions of the system monitor and provides immediate results of programming and diagnostic functions. Capable of being used for local or remote communications, it includes a quiet, detachable keyboard that is TTY compatible, RS-232-C communications interface, 6.5 x 8.4" CRT display, standard ASCII 64-character alphanumeric generator, refresh memory, and power supplies.

The screen displays up to 2000 5 x 7-dot characters on 25 lines of 80 characters. Cursor functions can be programmed to facilitate interactive communications with the development system. Transmission rates are 300, 1200, 2400, and 9600 baud. Odd, even, mark, and space parity checks are provided.

Basic operating modes include full- or half-duplex asynchronous communications; character by character transmission; control mode with escape sequence for CRT functions; and erase to end of line, to end of memory, and to clear screen.

#### High Speed Printer

Also a self-contained unit, the MDS-PRN prints 5 x 7-dot characters with an impact printing mechanism that provides original and up to four carbon copies. For quieter operation, motor turns on and off automatically as a standard feature.

Line printer operation is 10 to 16 times that of TTY print rates. Characters are received in parallel at



# The *Silent 700* ASR Data Terminal. It shares time with good company.



The twin-cassette *Silent 700*<sup>®</sup> Model 733 ASR data terminal from Texas Instruments is supported by every leading U.S. timesharing service company, a few of which are indicated here.

What's more, it's a powerful alternative to conventional teletype-writers. It's quiet. It transmits and prints data at 30 characters per second. And it reduces connect time and user cost.

Programs are prepared off-line and stored on cassettes, avoiding expensive connect time during data preparation. Result: More users can access the system without loss in response time. More computing time is delivered for the dollars spent.

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 NATIONAL CSS, INC.	 UNITED <sup>®</sup> COMPUTING SYSTEMS, INC.
<b>COMSHARE</b>	Optimum Systems Incorporated
 On-Line Systems, Inc.	<b>CSC</b> COMPUTER SCIENCES CORPORATION
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User programs are stored on cassette locally, reducing the cost of disc file storage at the remote computer.

The Model 733 ASR lists for \$2895\*, including printer and twin cassettes. Attractive lease rates are available. And it is backed by worldwide TI service and support.

For more information, contact your nearest TI office. Or write Texas Instruments Incorporated, P.O. Box 1444, M/S 784, Houston, Texas 77001. Or call 713/494-5115, extension 2124.



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up to 75K char/s by line buffer, and printed at rate of 55 lines/s. Data are printed in 132-char lines at 165 char/s, and in 80-char lines at 100 char/s.

Character size is approximately 10 points. Spacing between characters is adjusted automatically for two line widths. Also featured are format and speed controls required for either copying display or printing data

from diskettes at high speed. Special format controls implement MDS applications; a standard 2-channel vertical format control is provided.

Printer uses fanfold paper. Slew is adjustable for 8½ to 9½" widths. Paper can be fed from the rear for table use, or from the bottom. Optional accessories include metal stand and paper takeup tray.

Circle 173 on Inquiry Card

### Design Center Network Offers Opportunity to Examine $\mu$ Computers

Establishment of a nationwide network of Microcomputer Design Centers has been announced by Cramer Electronics, Inc, 85 Wells Ave, Newton, MA 02159, to offer companies interested in microprocessing an opportunity to examine different hardware and software options, and consult with specially trained microprocessing applications engineers and technicians.

Available on a rental basis (by

hour or day), two types of centers are operating, each offering different kinds of equipment. "Group A" centers are equipped with Intel MDS-800, Motorola EXORCISER™, RCA COSMAC-CDS, and Texas Instruments TI990 prototyping systems, along with one or more functional Cramerkits: AMD 9080A-1, Intel 8080A, Mostek F-8, RCA COSMAC, and Texas Instruments TMS 9900. "Group B" centers are equipped with Intel MDS-800 developmental systems and all seven Cramerkit models, plus EPROM programming kit.

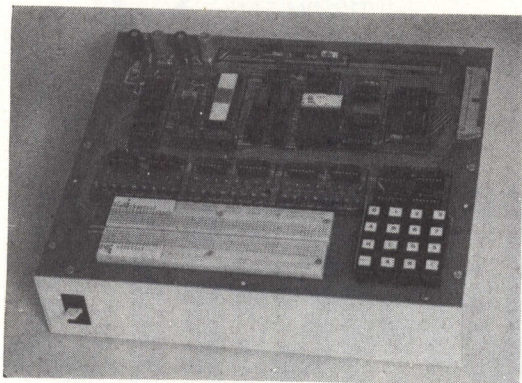
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### Low Cost System Serves as Basic Educational Tool

Mini-Micro Computer (MMD-1), a system based on the 8-bit 8080A microprocessor, contains all hardware, firmware, and instructions necessary to learn basic programming and interfacing. Included are a clock generator and driver, 1024-bit (256 x 4) static MOS R/W memory, 4-bit parallel bidirectional bus drivers, and 2048-bit (256 x 8) p/ROM.

Data entry is with a 16-switch keyboard organized for machine programming in octal code. Three groups of eight LEDs display status of high and low addresses and memory contents. The 256 8-bit words of R/W memory are expandable to 512 words; 256 words of p/ROM are preprogrammed to control the keyboard and may be supplemented with an additional 256 words for the user's own programs.

Breadboarding socket, with immediate access to control lines and



Including hardware, firmware, and necessary instructions, microcomputer system contains 8-bit microprocessor, 1024-bit RAM, 2048-bit p/ROM, self-contained power supply, and 16-switch keyboard

I/O buses, also accommodates up to six 16-pin ICs and a wide range of discrete components. Supplemental connections provide for additional sockets; an internal power supply provides 5 V,  $\pm 12$  V, and ground.

MMD-1 instruction text, based on the Bugbook series, covers practical operating control circuits, omitting needless technical explanations, mathematics, and complex specifications. Instruction method employed, adaptable to either classroom or home study, is based on carrying out a series of experiments intended to demonstrate principles.

Offered by E & L Instruments, Inc, 61 First St, Derby, CT 06418, the system measures 10 x 12 x 3" and weighs 7 lb. Assembled and tested unit costs \$500. In kit form (including instructional material), price is \$350. Set of PC boards with interface sockets and keyboard, and sets of ICs and hardware are available separately.

Circle 175 on Inquiry Card

### $\mu$ Computer Development Center Consolidates Three Functions

MDC 6800 combines three functions into a single configuration: it serves as a system for cost-effective hardware and software design and development of microcomputer systems; a general-purpose data processing system with 16K bytes of memory; and an intelligent communications terminal. According to American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, the system is up to 80 times faster for software development than other microcomputer development stations employing tape cassettes or paper tape storage.

For hardware development, the system offers remote front panel and ROM simulator functions, modular bus-oriented PC card cage supported by general-purpose breadboard cards, extender cards, EPROM programming capability, and self-testing firmware. It can also be used as an incoming parts tester.

Software development programs include FIDOS-II disc operating and file management system, text editor, symbolic assembler, extensive debugger (which automates functions of computer control panel), trace program (which allows debug program to display on CRT a trace of machine register contents, instruction mnemonics, and operands before execution of any instruction or





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You're looking at five insurance policies. Each capable of lowering your tape-drive operating costs. While reducing down-time. *And* maintenance costs. *And* service costs. *And* headaches.

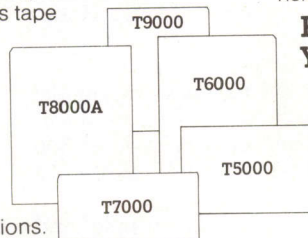
## 50,000 tape-drives are in good hands.

Pertec tape transports are known world-wide: Over 50,000 units have been sold. Making Pertec tape drives the most popular, most successful in the history of independent tape drives. (Today, every competitor designs his tape drives to be Pertec interface compatible.)

## Our five models work: Day in. Day out.

OEMs know about Pertec tape drives. Because they work when they're supposed to work.

And they can be configured to offer OEM customers over 400 tape drive variations.



## We take the risk out of buying.

Each of the five Pertec tape transports has a solid performance record. (Let's face it, you can't very well make and sell over 50,000 units and have a poor performance record.)

And to top it off, our customers get a service resource that is one of the largest, most available, best-trained *in the world*.

In short, we've taken the fault out of tape drives. And the risk out of buying.

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subroutine in the user's program), self-test programs, and COM telecommunications package.

System has conventional minicomputer-like front panel operations designed into the CRT terminal, which has full 256-character encoded ASCII keyboard. Control keys include such functions as reset, load, execute, continue, single step, examine, modify, automatic loading bootstrap, set breakpoint, set monitor point, and halt. Separate auxiliary 20-key edit keyboard permits cursor control and editing functions.

A 16-position card cage and power supply are contained in the CRT chassis. Standard card modules include: MPU; EPROM/ROM program storage; RAM; keyboard/telecommunications; debug; peripheral interface; EPROM programmer; and CRT driver and dynamic RAM cards. Dual-drive IBM-compatible floppy disc system is housed separately, with an optional matrix printer available for production of hard copy.

Circle 176 on Inquiry Card

### Microprocessor Kit Converts Computer to Development System

Containing cross assembler, simulator, and p/ROM programmer, MAX-11 converts the Digital Equipment Corp PDP-11 into a microprocessor development system. Both assembler and simulator are designed to run on the PDP-11/04 or larger, which has 16K memory with a system device (floppy or full disc).

Written in macro assembly language, cross assembler features user defined macro library, local symbols, symbolic cross reference, assembly list control, full nested macros, and conditional assembly. It executes under DOS at the rate of, and uses the same kind of format as, Macro-11.

Simulator also is written in macro assembly language on the Macro-11. It is able to examine and modify location and register, search ROM, modify object file output on the system, and change radix of typeout. Other features include eight break points, external device and interrupt simulation, real-time cycle counter, and single step with trace. In addition, simulator keeps track of program cycles run on host machine,

for later use when run on target machine.

Data are transferred directly from the PDP-11 disc through serial TTY interface to the programmer, eliminating need for paper tapes. Programmer both reads and writes ROMs. Presently available for Intel 4040 and 8080 and Motorola 6800, the kit can be obtained from Aivex, Inc, 6 Preston Ct, Bedford, MA 01730. Simulator and assembler cost \$1250; programmer is \$2300.

Circle 177 on Inquiry Card

### Heat, Noise, and Size Problems Eliminated by External Power Supplies

Line of microprocessor power supplies is designed in both wall plug-in (only slightly larger than conventional wall plugs) and desktop configurations that keep power supply external to the customer's product enclosure. Supplies convert 120 Vac into low voltage regulated dc for use by the microprocessor outside of the unit proper, keeping the transformer and 120 Vdc out of the enclosure.

Separate supply permits reduced enclosure size, and eliminates heat and noise problems, need for shielding, and need for UL approval of the customer's product. Microprocessor power supplies are designed for



UL and CSA listing and are made in the U.S.A. by Dynamic Instrument Corp, 933 L I Motor Pkwy, Hauppauge, NY 11787.

Most versatile power supply for use with popular microprocessors, model M5-1212 (desktop model) produces simultaneous outputs of 5 Vdc at 500 mA, 12 Vdc at 150 mA, and -12 Vdc at 150 mA. Line regulation is 3%, load regulation, 2%. Ripple and

noise are 3.5 mV rms, 10 mV pk-pk. Temperature range is 0 to 40°C.

Two plug-in models, M12-250 and M9-100, are low cost standard power supplies designed for high volume applications, and produce 12 Vdc at 250 mA and 9 Vdc at 100 mA, respectively.

Circle 178 on Inquiry Card

### Video Response Controller Turns Cassette Player Into Teaching Unit

As a microcomputer-based device that allows a videocassette player to become an interactive teaching unit, VRC-100 Video Response Controller applies basic teaching and testing philosophies of audio response systems to a video response system. Since precise control and positioning of helical video tape players is difficult, microprocessor techniques and components have been incorporated to solve these complex functions.

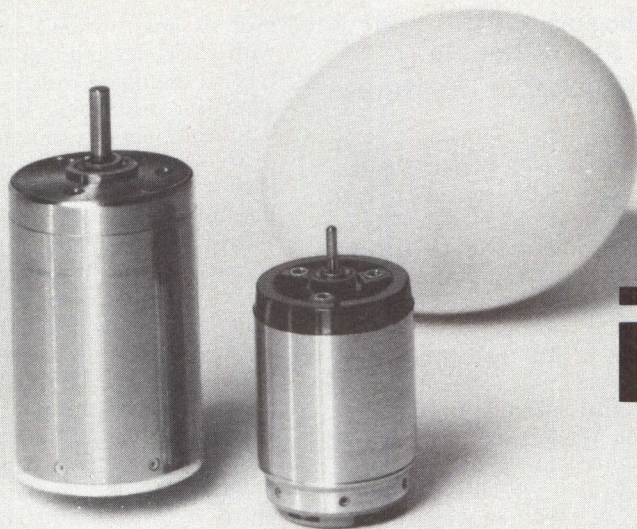
Used in a training film environment, the controller enables a student operator to respond to questions displayed on a video screen, entering responses through the keyboard. Every response corresponds to a predetermined response address (position) on the tape; the VRC accepts the student response, positions tape to required address, and resumes playing the tape.

Prepositioning of a tape can also be accomplished. A digit display on the face of the unit indicates the current tape address in "counts" from rewind address zero. Second display segment indicates last "search" address entered. An optional encoder feature from Microcomputer Associates Inc, 2589 Scott Blvd, Santa Clara, CA 95050 enables recording of response address data on the videocassette audio channel.

Consisting of control electronics contained in an 8 x 10 x 4" plastic enclosure, the controller attaches to videocassette player via a cable with connector. All signals required to perform VRC functions are made available at the videocassette player connector by the controller. The enclosure's console supports keyboard and display. Keyboard section includes 10-key unit (0-9) and 10 function keys; display section consists of two 4-digit decimal display segments, each capable of displaying values from 0000 to 9999.

Functions which the unit performs are maintenance and display of current videocassette position address,





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## escap<sup>®</sup> miniature dc servomotors

No other micromotor on the market today offers the high reliability and optimum performance efficiency of an escap<sup>®</sup> miniature dc servomotor. We earned our reputation by building a quality line of motors that not only deliver superior performance, but superior cost effectiveness as well. We're ahead of our competition in such areas as space-saving design, low current consumption, high efficiency, and ripple-free torque, just to name a few, because for over 15 years we have made a continuous investment in

new product development, as well as product line reliability and performance.

When you're tops in your field, you're often imitated. In fact, competitors have copied our electrical specifications, our dimensions, our integral magnet designs, and even our innovative lead strain relief cap. They've even tried to copy our most important design element - our precision skew wound armature. But they can't copy our reliability . . . THEY MUST PROVE IT. Reliability is a result of years of experience.

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So you see, it's not enough to be merely an "imitator" in the micromotor industry. escap<sup>®</sup> motors are designed and engineered BETTER - that's the key to long life and high reliability.

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**CIRCLE 53 ON INQUIRY CARD**

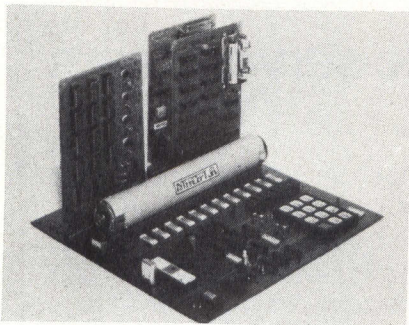


and response to search, play, pause, and clear requests from the keyboard. Control electronics consist of Intel MCS 4 microcomputer, console interface card, and power supply (via a 3-wire ac plug). Power on/off is controlled by the cassette-in switch on the enclosure.

Circle 179 on Inquiry Card

### CMOS Tutorial System Offers Exposure to Microprocessors

Intercept Jr, a low cost system utilizing the company's IM6100 CMOS microprocessor and related family of CMOS devices, provides students, hobbyists, and designers with an opportunity to gain practical experience in microprocessors, RAMs, p/ROMs, and I/O interfacing. Basic module



provides an operating all-CMOS microcomputer on a 10 x 11" double-sided PC board. It features a multi-function keyboard, two 4-digit LED displays, and a resident microinterpreter, and is battery powered. Unit recognizes the Digital Equipment Corp PDP-8/E minicomputer instruction set.

Nonvolatile CMOS RAM module provides convenient memory extension in the form of 12 1024 x 1 CMOS RAMs. Power-strobed p/ROM module supplies up to 2K words of user program on a 4½ x 6½" board. Serial I/O module with both RS-232 and 20-mA current loop interfaces is also available.

Developed by Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014, the system comes fully assembled and factory tested, complete with batteries. Terminals are provided, enabling system to run off an external 5- or 10-V power source.

Circle 180 on Inquiry Card

### 8080A-Based CPU Allows Flexibility in 8-Bit $\mu$ Computer Systems

Capable of implementing the 8-bit 8080A as a fully TTL buffered microprocessor, the 8821 processor card includes separate 8-bit data bus in and out; 16 address lines (65K bytes of memory address); 3-state data, address, and memory control for DMA; crystal clock; power-on and external reset; 1K bytes of R/W memory; capacity for 4K bytes of ROM; external memory control; and I/O control. When used with an I/O card, the processor card, developed by Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940, provides a complete 2-card 8-bit microcomputer system. By adding more cards, the 8821 can be expanded to use full memory and I/O capability of the 8080A.

Cards, which measure 4.5 x 6.5" with 56-pin card edge connectors on 0.125" centers, fit into standard racks. Circle 181 on Inquiry Card

### Compact Memory Expands Microcomputer, Frees Bus Loads

Add-in expansion for the DEC LSI-11 16-bit microcomputer is available with Monostore<sup>R</sup> XI/Planar semiconductor memory. Designed around 4K n-MOS dynamic RAM technology, the 16K x 16 quad board allows LSI-11 memory expansion within the present chassis, eliminating the need for add-on hardware for memory or peripheral interfacing. It also carries "on-board refresh," to eliminate direct memory access problems.

Supplied with 4K x 16 MOS memory, LSI-11 requires utilization of all six bus loads that the computer can drive to fulfill its 28K memory capacity with DEC boards. With use of a Monostore half board (8K) and full board (16K), only two bus loads are used to bring the LSI-11 to full capacity. Other bus loads are free for interfacing peripherals, while the computer is used to its full extent.

Boards developed by Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110 use "cycle steal refresh," which interferes less than 2.3% of the time, thereby facilitating direct memory access. If the

user desires, memory can be linked with DEC refresh via a switch setting on the board. Additional switches allow for addressing anywhere from 0 to 28K in the computer bus.

Memory is fully software and hardware compatible with the LSI-11. Because of faster access time (450 ns) and cycle time (600 ns), Monostore permits existing programs to be used without modifications. More reliable than core memory, it has a calculated MTBF of over 100K hours and actual expected MTBF of 300K hours. Board operates from two power sources of 5 and 12 V.

Computer can be ordered with minimum memory, and boards can be added as needed. Standard configuration is full quad board (16K x 16), but four models allow expansion in 4K, 8K, 12K, or 16K sizes.

Circle 182 on Inquiry Card

### Redesigned $\mu$ Computer Is Based on 8080A Processor

Altair<sup>TM</sup> 8800b, a second generation design of the Altair 8800, is built around the 8800A microprocessor, and, like the original, is an open-ended machine. Compatible with all existing Altair 8800 hardware and software, it can be configured to meet most system needs.

Included in the computer are a redesigned front panel, CPU board, power supply, and 18-slot motherboard. In addition to the microprocessor which has over 200 machine instructions, instruction cycle time of 2  $\mu$ s, and capability to directly address 256 I/O devices and 65K words of memory, CPU board includes an 8224 clock generator and 8216 bus drivers. Clock pulse widths and phasing as well as frequency are crystal controlled. A totally synchronous logic design with the same switch and LED arrangement as the original model, front panel also includes back-lit Duralitch (laminated plastic and mylar, bonded to aluminum) dress panel with multicolor graphics; longer flat toggle switches; and five functions stored on front panel p/ROM.

Front panel is interfaced to the CPU via two, 34-conductor ribbon cable assemblies, thus eliminating complicated wire harness. These cables connect the front panel to an interface board which buffers all



# Ask Control Data for the first horizontal font 300-600-900 lpm family of OEM printers with the print band any operator can change in 30 seconds.

## We have it.

GET 1130 LPM FOR LESS THAN \$10,000 IN 48-CHARACTER SET APPLICATIONS, OEM QUANTITIES.

Here now: CDC horizontal font Band Printers with truly operator-interchangeable bands—plus exclusive choice of 10 and 15 cpi bands! Just look at their advantages:

**Users can switch bands in 30 seconds!** Single-piece band weighs less than an ounce! Stores conveniently in cabinet. No need to lift out the ribbon! Insert a new band—the printer automatically adjusts for pitch and character set (adjustment between 64/96 characters standard; 48/64/96 or 64/96/128 optional). Eleven bands now available.

**Paper-saving condensed pitch!** Prints 132-character lines either on 14<sup>7</sup>/<sub>8</sub>" or 11" paper! Unique 15 cpi bands cut user paper costs and storage needs by reducing paper volume 40%!

**Three look-alike models.** Only six differences between units; identical spare parts kits. Offer a choice of speeds—without tying up capital in spare parts inventories!

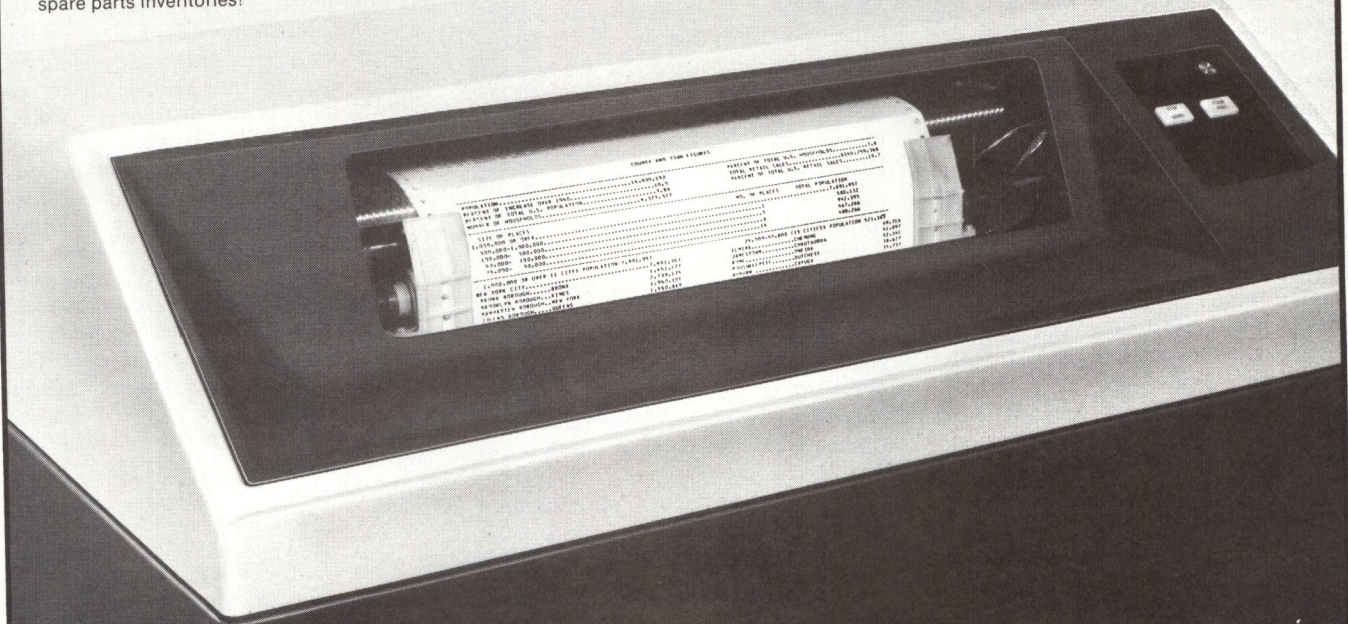
**Minimum operator attention.** Exclusive patented control permits use of double-length 48-yard ribbon, cuts ribbon changes 50%! Electric eye automatically reacts to any paper feed jam-up, permits use of lighter-weight paper.

**Superior readability.** These CDC Band Printers deliver full, solid strokes—top to bottom—even on super- and sub-scripts.

**Make these advantages your advantages!**

Write for complete information plus sample printout. Compare our sample with copy from any printer. See how CDC Band Printers offer print quality and printer features never before available in a medium-to-high-speed printer under \$10,000!

New compact 34" width. Takes a minimum of precious floor space; produces up to 900 lpm (using 64-character sets).



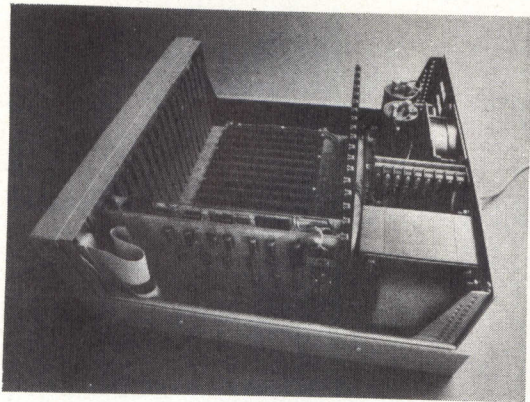
Phone (313) 651-8810 or write: Harrison Craig, Peripheral Products Sales Manager, Control Data Corporation, 1480 N. Rochester Road, Rochester, Michigan 48063.  Ask a CDC Sales Representative to bring me a Band Printer evaluation unit.  Send more information and sample print-out.

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Ask the CDC OEM people

**CD** CONTROL DATA CORPORATION





Second generation Altair 8800b contains CPU board, power supply, 18-slot motherboard, and redesigned front panel. Compatible with existing Altair 8800 hardware and software, microcomputer features 8080A microprocessor and five new functions stored on front panel p/ROM

lines to and from the bus. Power is heavy duty supply rated 8 V at 18 A, 18 V at 2 A, and -18 V at 2 A. Computer can operate at 110 or 220 V (50/60 Hz). Primary is tapped for either high or low line operation.

The manufacturer, MITS, Inc, 2450 Alamo SE, Albuquerque, NM 87106, also has available plug-in compatible boards. Introductory prices are \$840 for kit; \$1100, assembled.

Circle 183 on Inquiry Card

### Nonvolatile Memories for Two Microprocessors Eliminate Data Loss

Two memory systems, MM16P and MM8080, are designed for nonvolatile operation with National IMP-16P microprocessor and Intel Intellec<sup>®</sup> 8, respectively. Systems eliminate data loss upon power removal, a feature characteristic of semiconductor memories found in microprocessor development systems. Available from Micro Memory, Inc, 9438 Irondale Ave, Chatsworth, CA 91311, both memory systems are compatible with existing processor boards through use of memory boards that plug directly into existing connectors.

MM16P, an 8K x 16 RAM core memory system that can also be operated as 16K x 8, measures 8.5 x 11 x 1"; MM8080 is an 8K x 8 RAM measuring 6.18 x 8 x 1". Both systems allow the microcomputer user to fulfill the function of RAM and p/ROM on the same unit. Data access time is 350 ns; cycle time is 1.0  $\mu$ s. On-board memory module expansion is available in 4K increments up to 64K words. Memory module contains timing, control, decode, drive circuits, address registers, and data registers. Power status signal is available as a power interrupt vector or as a power reset signal. The MM16P also has byte control feature.

Circle 184 on Inquiry Card

### 8-Bit Microprocessor Family Allows Flexible System Design

INS8080A, a general-purpose 8-bit microprocessor family, is a direct pin-for-pin and function-for-function replacement for the Intel 8080A. Developed by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, the device is the company's first n-channel MOS microprocessor.

Plans are being made to build most of the popular support circuits in the family; an on-going program also supports the device with hardware, software, and development tools. Applications range from complex controls to sophisticated communications applications, permitting design of flexible systems.

Offering powerful programming capability with 72 problem-solving instructions and multiple register pairs for general-purpose operation, the device has an instruction time of better than 2  $\mu$ s. Addressing capability is broad—up to 65K of memory and up to 512 I/O ports.

Operation can easily be interrupted because the program counter automatically is saved during interruption. System also has the ability to provide vectored interrupts. Device permits controlled suspension of processor operations, which is useful when the CPU is operating with low

speed memory. It also provides direct memory access input capability to the system.

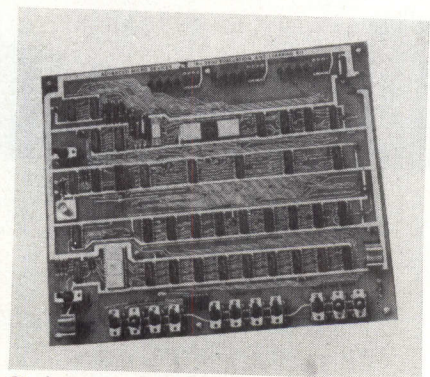
Schottky bipolar technology is used in supporting circuits for the device. It is planned for use in the INS8224 clock generator, which provides timing signals for the CPU and system; and the INS8228 system controller which provides buffering of the data bus.

### Programming Techniques Are Learned From Bipolar Microprocessor Kit

A bipolar microprocessor kit to demonstrate microprogramming techniques and allow evaluation of the Am2900 microprocessor family is available from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. Utilizing the industry standard Am2900 family of components, this kit allows the designer to write and execute 32-bit microinstructions in high performance pipelined control unit.

Microinstructions control an Am2901, including A and B addresses, instruction, carry-in, and data-in. Other bits control shift logic to allow logical and arithmetic shifts, and rotates; still others control selection of next microinstruction addresses utilizing the sequencer. Sixteen sequencer functions are built-in.

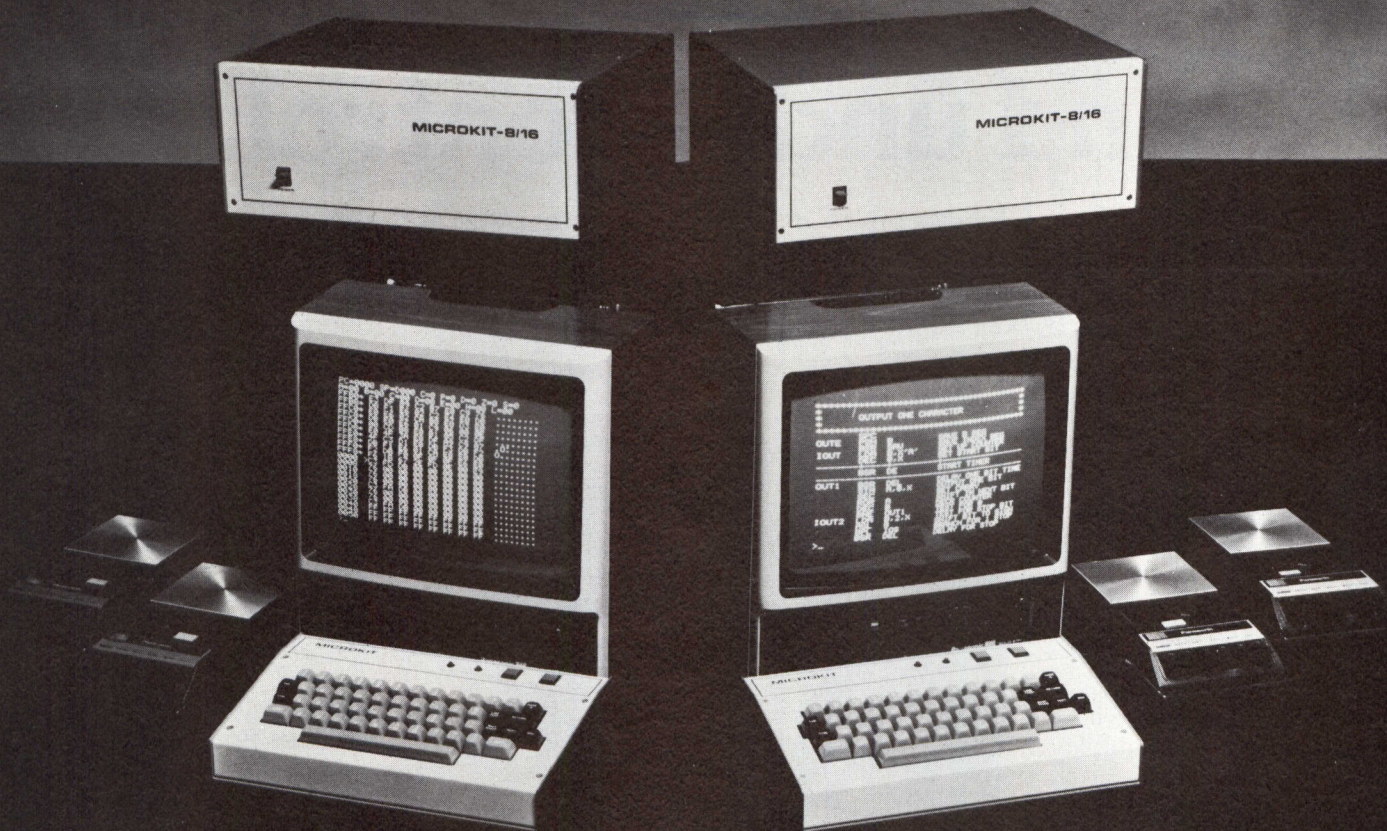
Kit (Am2900K1) also may be driven in real time by a pulse generator, which enables evaluation of components under real conditions. Included in kit are 40 ICs, LEDs, switches, resistors, decoupling capacitors, PC board, and manual covering theory, assembly instructions, testing, and experiments. A 5-V power supply is all that is needed.



Circle 185 on Inquiry Card



# The Most POWERFUL 8080 or 6800 Microcomputer Development System at any price... \$3,850<sup>00</sup> COMPLETE.



Only a truly powerful microcomputer development system allows you to accomplish your design task quickly, efficiently, and at a minimum cost. **MICROKIT** has the powerful microcomputer development system you need.

## OTHER SYSTEMS OBSOLETE

The MICROKIT-8/16 has a unique CRT display refreshed directly from the microcomputer memory so it can write the full 960 character screen at 20,000 cps, faster than the blink-of-an-eye. Using the fast CRT, our interactive debugger gives you full screen hexadecimal memory dump displays instantaneously. With this kind of fast system response, debugging is a snap.

To match our fast debugger we have a screen based editor that is quickly learned and easy to use, because it lets you see the changes you make instantly and in full context on the CRT display. Rounding out our outstanding software package is a complete microcomputer resident assembler. Any system without a display as fast as ours and without software like ours cannot possibly match the powerful debugging and editing features we offer.

## EVERYTHING FOR \$3,850

But how is it that the MICROKIT-8/16 has everything (keyboard, display, tape units, and software) included in the basic price? We keep your cost low by using a standard television set for the high-speed display, and by using audio cassette units for mass storage. And with MICROKIT's proprietary recording technique, you get data reliability comparable to digital cassette units while data is transferred to the cassettes at the rate of 2000 bps — 20 times faster than TTY paper tape.

## BOTH 8080 AND 6800

The MICROKIT-8/16 can be ordered as either an 8080 or a 6800 based system. At \$3,850 either system is the best buy in microcomputer development systems today because they both include the 8K memory, the display and keyboard, the two audio cassette units, and the full complement of development software — debugger/monitor, editor, and assembler. Furthermore, either system can be easily switched to the other processor with our conversion packages that consist of a plug-in processor module and software.

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Rest assured that we also back you up with a complete line of enhancements including In-Circuit Emulators, EPROM programmers, add-on RAM or EPROM memories, line printers, "semiconductor disk" memory resident operating systems, and single or dual drive floppy disks with a super disk operating system.

## MICROKIT-8/16'S ARRIVE READY TO GO TO WORK FOR YOU

But don't be misled by our name, our system comes fully assembled, fully tested, fully warranted, and ready to begin helping you with microcomputer development the very day it arrives. The MICROKIT-8/16 is a proven and reliable system which over the past year has received enthusiastic customer acceptance.

Our unbeatable features make the MICROKIT-8/16 an obvious choice for the designer requiring a microcomputer development system. Write or call MICROKIT INC. today, (213) 828-8539, to see just how well the MICROKIT-8/16 fits your microcomputer development requirements.

Wescon Booth No. 960 — CIRCLE 55 ON INQUIRY CARD

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# The new generation of Diskette Drives is here and under control.

PerSci has it—a family of diskette drives “design-years” ahead of competitive drives—now available in complete low cost subsystems for interface to 8080, 6800 and other major micro-processors.

## The Highest Performance Diskette Drives:

PerSci diskette drives, both single and dual head units, offer a combination of performance features unique in the marketplace while still maintaining compatibility in existing systems:

- Voice coil positioning for access speeds seven times faster than competitive drives (76 tracks in 100 ms)
- A low power all DC system reduces cost and assures high reliability
- Automatic electric loading simplifies operation and protects media
- Small size permits 5 single drives or 4 dual drives to be mounted vertically in a 19 in. rack

## The Most Powerful Diskette Drive Controller

The PerSci Model 1070 Diskette Drive Controller puts the advanced performance of PerSci drives to work in microprocessor based systems. An IBM format compatible, “intelligent” controller, the Model 1070 will handle from 1-4 drives with minimum demand on the host system.

In fact, with addition of a power supply and keyboard to the PerSci subsystem, the user can

perform many floppy disk routines without additional hardware or software.

Controller features include:

- Interface to most micro-processors including 8080, 6800 & Z80
- Internal disk operating software including IBM formatting
- RS232 interface option
- Rom options allowing copy data transfer between diskettes and data transfer between RS232 interface and diskette

## An Economical Diskette Drive Subsystem

A complete subsystem including a single diskette drive (Model 70), the Model 1070 controller with interface and a controller-to-disk-drive cable is available in single units for \$1,195. For double capacity, a dual diskette drive (Model 270) subsystem is available for \$1,495.

OEM discounts available.

Don't settle for yesterday's diskette drive. Get the new generation under control from PerSci, 4087 Glencoe Avenue, Marina Del Rey, CA 90291 (213) 822-7545.



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Maybe we haven't been visible quite as long as some of the other guys but that can be an advantage too. For example, the light source in our readers is state-of-the-art fiber optics. It's superior to LED's and you'll even find it in our least expensive reader. (Which incidentally is the least expensive reader on the market.) Some competitors are just switching to fiber optics. We introduced it long ago with our first reader.

Another Decitek advantage is the simplicity of design, which makes it easy to adapt our equipment to specific OEM requirements. And because Decitek is an aggressive little outfit we'll go out of our way to accommodate you and your needs. Now go ahead and ignore us if you can.

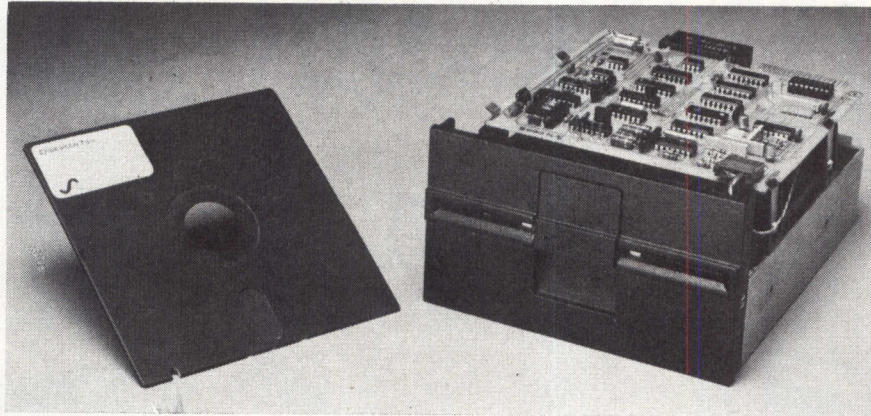
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# PRODUCT FEATURE

## Small Floppy Disc Drive Meets Microcomputer System Requirements



Formatted storage capacity of 89.6K bytes in a flexible disc package that is the size of most cassette tape units provides microcomputer and mini-computer systems designers with fast data throughput and superior data integrity. Half the size of a standard flexible disc drive, Shugart Associates' SA 400 minifloppy™ offers 109.4K bytes of unformatted storage, 125K-bit/s data transfer rate, and error rate of 1 per 10<sup>8</sup> bits soft and 1 per 10<sup>11</sup> hard. Reductions in recording density (2480 bits/in. inside track vs 3200 for a standard floppy) and in rotational speed (300 rpm vs 360) provide wide drive design margins and increase media life, respectively.

The 3.25 x 5.75 x 8.0" package is of die cast construction to maintain high mechanical integrity, yet weighs only 3 lb. Use of a dc servo-controlled spindle drive motor totally eliminates ac power requirements.

Precise speed control is maintained by an integral tachometer. A unique direct drive stepping motor actuator features a spiral cam with a v-groove positive detent that assures track registration as the groove wears. Proprietary glass bonded ferrite/ceramic read/write

recording head technology proven in the company's full size floppy drives is used in the small unit.

### Diskette

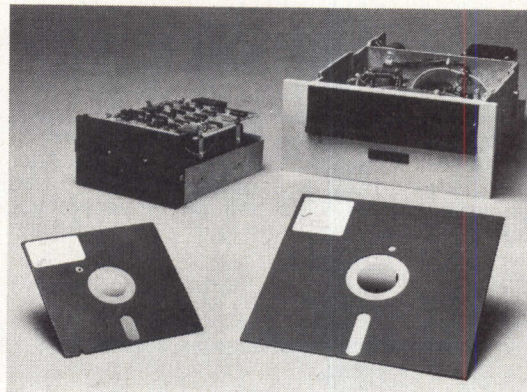
A 5.25" minidiskette™ has been developed specifically for use with the minifloppy. It uses the same oxide formulation as standard diskettes and the same media technology. The small diskettes, in either hard or soft sectored formats, will be available from several media manufacturers.

Positive media interlock to prevent the door from closing without

total diskette insertion and expandable cone diskette centering for proper media alignment minimize diskette damage and thereby maintain data integrity. Write protect circuitry protects written diskette information.

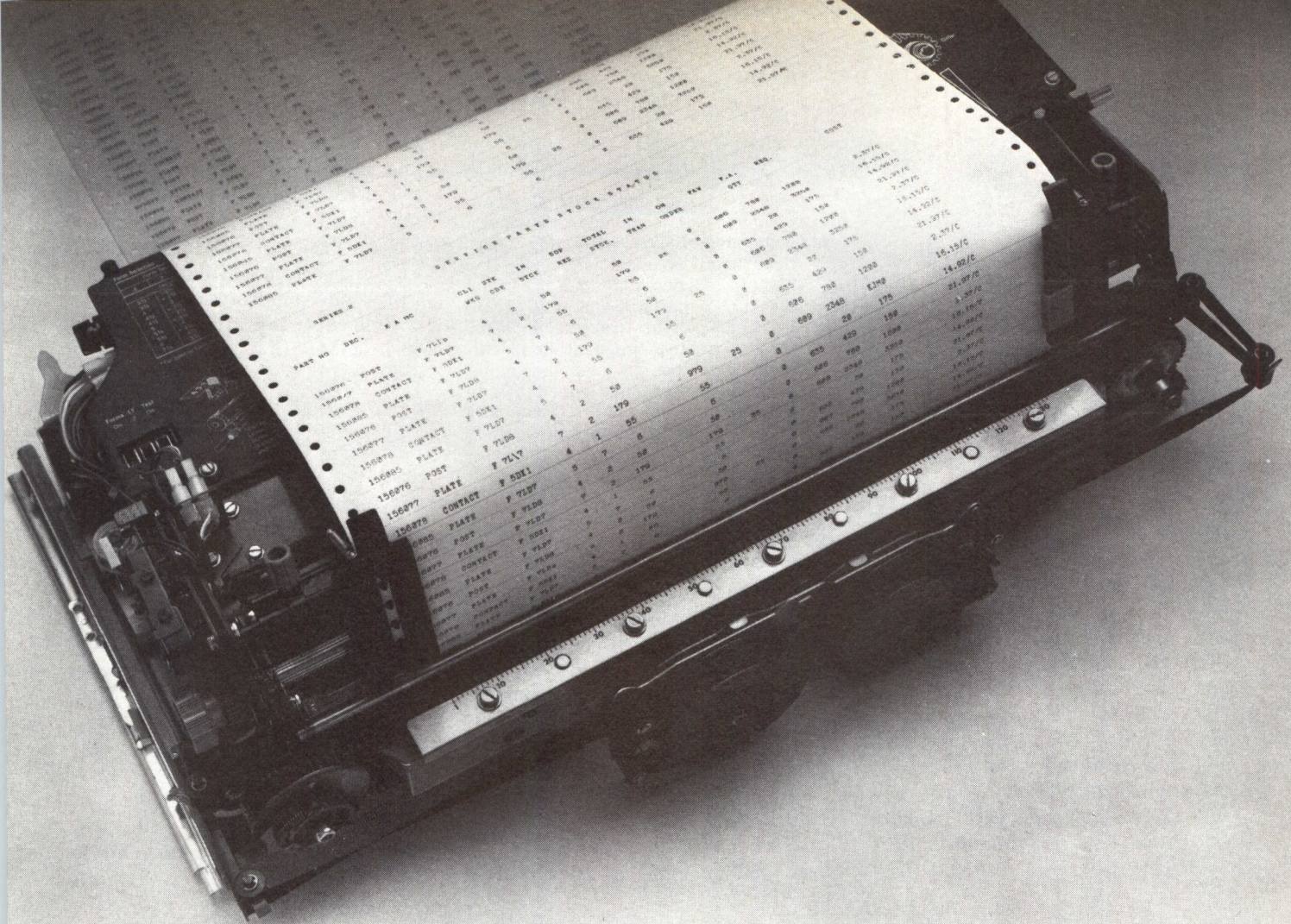
### Applications

According to the manufacturer, the minifloppy provides enhanced performance and reliability over cassette and magnetic card devices while remaining cost and size competitive. Because virtually no preventive main-



Size comparisons of Shugart Associates' SA 400 minifloppy and SA 104 minidiskette (left) and standard SA 800 floppy and SA 100 diskette. Smaller drive is half the size and has one third the storage capacity of a standard unit; minidiskette is only 5.25 in. sq





**The Teletype® model 40 OEM printer.  
When you look at it from price and performance,  
you'll find it difficult to look at anything else.**

The fact of the matter is simply this:  
We don't think any other printer can even come close to the model 40.

And that's no idle boast. Not when you consider the facts.

Consider: Where else can you get a 132-column, heavy-duty impact printer that delivers over 300 lines per minute for less than \$2000, or an 80-column printer for under \$1400?

The big reason behind the model 40's price/performance advantage is our unique design.

Even though it operates at speeds of more than 300 lpm, wear and tear is less than you'd find in a conventional printer operating at considerably slower speed. Fewer moving parts and solid-state components add up to greater reliability and reduced maintenance.

Here's something else to consider: Where else can you get a printer that delivers the kind of flexibility and reliability the model 40 offers?

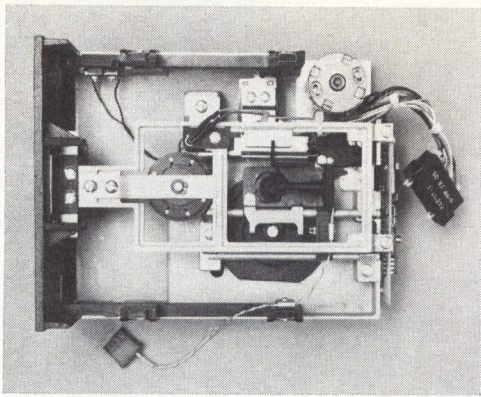
For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.



**The Teletype model 40 OEM printer.  
Nothing even comes close.**

CIRCLE 57 ON INQUIRY CARD





Bottom view of minifloppy. Components include dc spindle drive motor with integral tachometer (top right), head load solenoid and bail (top center), expandable cone for mini-diskette centering and LED/photo transistor pair for index/sector sensing (left center), magnetic head/carriage mounted on stepping motor actuator (center), and speed control PC board (far right). Connectors shown attach to motherboard which has been removed for this photo

tenance is required and because it does not require a cooling fan in most applications (16-W continuous duty, 5-W standby power consumption—therefore, low heat generation) the unit meets the reliability and low noise requirements of office environments. General applications include word processing and text editing systems, micro and minicomputer program storage, power typing systems, "intelligent" desktop calculators, and the microcomputer hobby market.

### Specifications

Track capacity is 3125 bytes unformatted, 2560 bytes formatted. Track sector size is 256 bytes with 10 sectors, 35 tracks, and a single read/write recording head. An available alternative format, based on a 128-byte record, provides 18 sectors/track. This format results in a reduced capacity of 2304 bytes/track (80.6K bytes/diskette).

Track-to-track seek time is 40 ms, head settling time is 10 ms, and

head load time is 75 ms. Average latency time is 100 ms.

Power requirements are 12 Vdc  $\pm 5\%$  at 1.1 A and 5 Vdc  $\pm 5\%$  at 0.5 A. Typical power dissipation is 51 Btu/h continuous duty, 17 Btu/h with the drive motor off.

Ambient temperature ranges are 40 to 115°F (4 to 46°C) operating, -40 to 144°F (-40 to 62°C) shipping, and -8 to 117°F (-22 to 47°C) storage. Relative humidity ranges are 20 to 80% operating, 1 to 95% no condensation shipping and storage. MTBF is 8000 power-on hours typical duty; MTTR is 30 min.

### Price and Delivery

Single unit list price for the SA 400 minifloppy drive is \$390. In large OEM quantities the price is about \$250. Delivery is 45 days ARO. Shugart Associates, 435 Indio Way, Sunnyvale, CA 94086. Tel: (408) 733-0100.

For additional information circle 199 on inquiry card.

## SUB-MINI Computer Systems - Series 70

Microprocessor technology integrated into computer systems

### One Board Computer

- Intel 8080
- ROM - 1K to 4K bytes
- RAM - 4K to 16K bytes
- Async I/O Controller
- DMA Bus
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  - Memory to 64K
  - Operator front panel
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### Integrated Computer/Mini Peripheral Systems with IBM Compatible Floppy Disk or 3M Tape Cartridge

- RS232 Storage System
- Intelligent Terminal
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- Sub-Mini Computer System with Peripherals\*

\*Complete peripheral support - enclosures, desks, floppy disk, tape cartridge, printers, 9 track tape, communication controllers, 5 and 10 megabyte disks, general purpose controller, clock, paper tape, ROM programmer.



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# 3M got there first. Again.

We put the features of our 1/4" DC300A cartridge into a shirt-pocket size. Then we designed a drive—small in size, small in price, for applications where high data reliability must be combined with compact size.

The new DCD-1 system will fit in a 5 inch cube—the cartridge alone measures just 2.4 x 3.2 x .5 inches. Enough about size, let's talk performance.

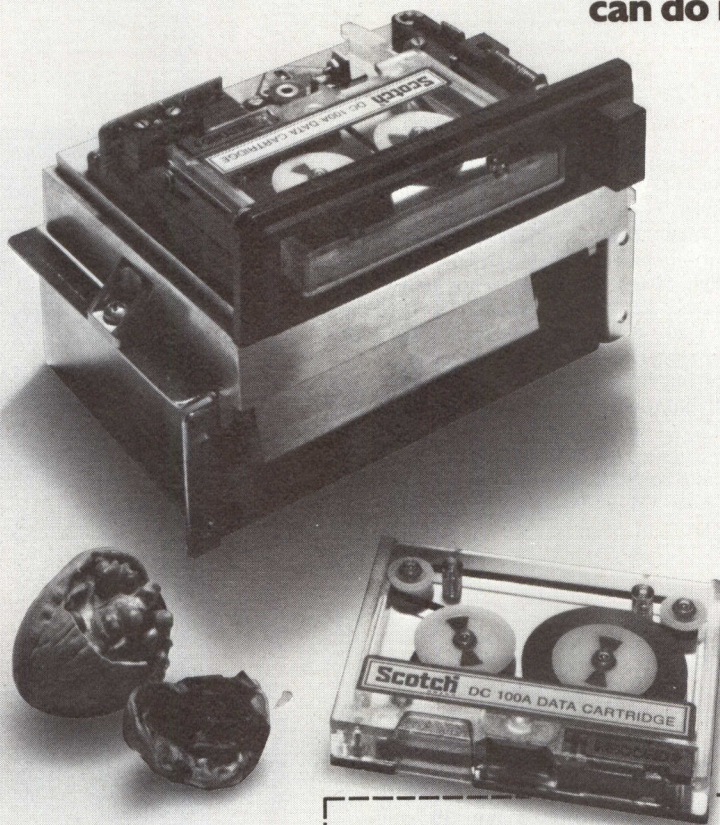
The drive records *full width* across the entire tape, which virtually eliminates errors. It has an encoding method virtually independent of tape speed, and control logic that prevents the drive from accepting any command that might harm the cartridge.

The electronics are designed to give the system engineer the greatest application flexibility—

has byte oriented data input and output and 100,000 byte storage capacity. It's also designed to permit battery operation.

This new system will change the industry much like our 1/4" cartridge. So it's time for our competitors to play follow the leader again—if they can. That's the story in a nutshell. Just send the coupon for more details.

**All our competitors  
can do is follow us.**



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DATA PRODUCTS  
**Mincom Division** **3M**  
COMPANY  
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CIRCLE 59 ON INQUIRY CARD

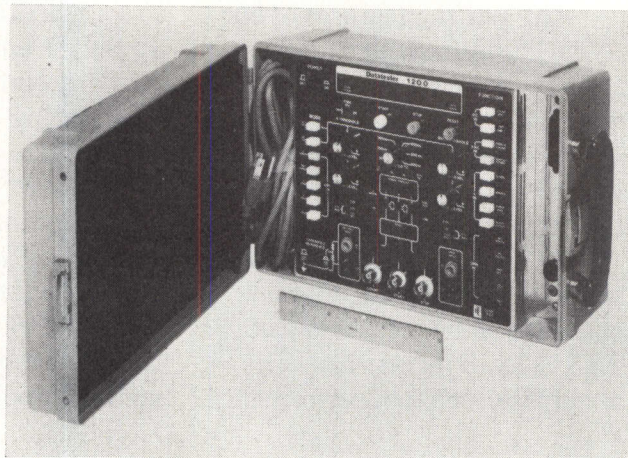


## PRODUCTS

### Single-Unit Field Tester Can Service Complex Digital Systems

A replacement for separate oscilloscope, frequency meter, pulse timer, digital multimeter, peak reading voltmeter, and duty cycle meter, the field-portable Datatester 1200 can diagnose entire system logic arrays and isolate faults down to the component. Frequencies can be measured to 35 MHz; rise/fall times, widths, and periods are measured in 10-ns resolutions. Signals can be measured from ECL/MECL through MOS/CMOS; a preset position is provided for TTL/DTL thresholds. Measuring 2-pulse coincidence and aligning tape and disc drives are built-in. Individual + and - peak detectors are provided on each of the three input channels and threshold levels are digitally set on the front panel display. Duty cycle is measured directly in percent. DMM functions include Vdc from  $\pm 100 \mu\text{V}$  to  $\pm 1000 \text{ V}$ , Vac from  $100 \mu\text{V}$  to 500 V, and resistance from  $0.1 \Omega$  to  $100 \text{ M}\Omega$ . Autoranging is provided on dc, ac, and frequency functions. **Data Test Corp.**, 2450 Whitman Rd, Concord, CA 94518.

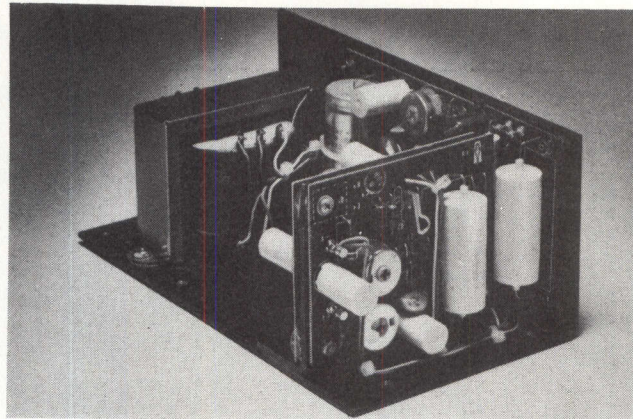
Circle 200 on Inquiry Card



### Power Supplies Specially Designed For Use With Most Microprocessors

Specific performance requirements of major microprocessor families including 6800, 8080, 9080, Pace, SC/MP, and F-8 are met by the SMP series of open frame power supplies. The multiple-output microprocessor-compatible models offer various combinations of 5, 9, and 12 Vdc that directly interface with individual microprocessor operating levels. Power is regulated to within  $\pm 0.1\%$  for both line and load. Several ranges are available from 40 to 160 W. Typ ripple is  $0.1\%$  (0.5 to 2 mV rms). Universal 115/230-Vac inputs are fully rated from 47 to 440 Hz. Automatic foldback current limiting short-circuit protection is adjustable from 20 to 150% of the load (factory preset at 110%). Response time is  $50 \mu\text{s}$ , tempco is  $0.02\%/^{\circ}\text{C}$ , and operating temperature range is 0 to  $50^{\circ}\text{C}$ . **Standard Power, Inc.**, 1400 S Village Way, Santa Ana, CA 92705.

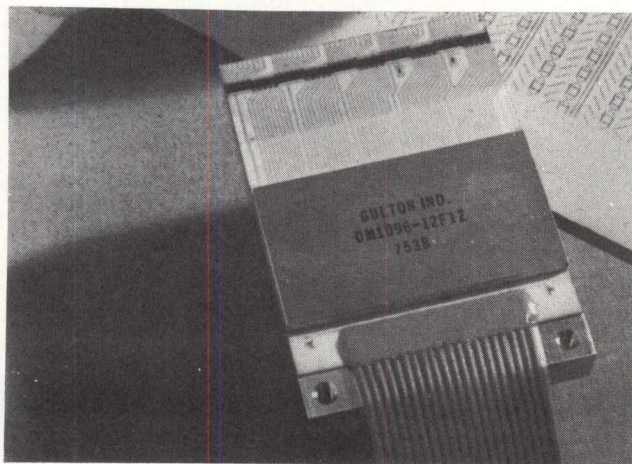
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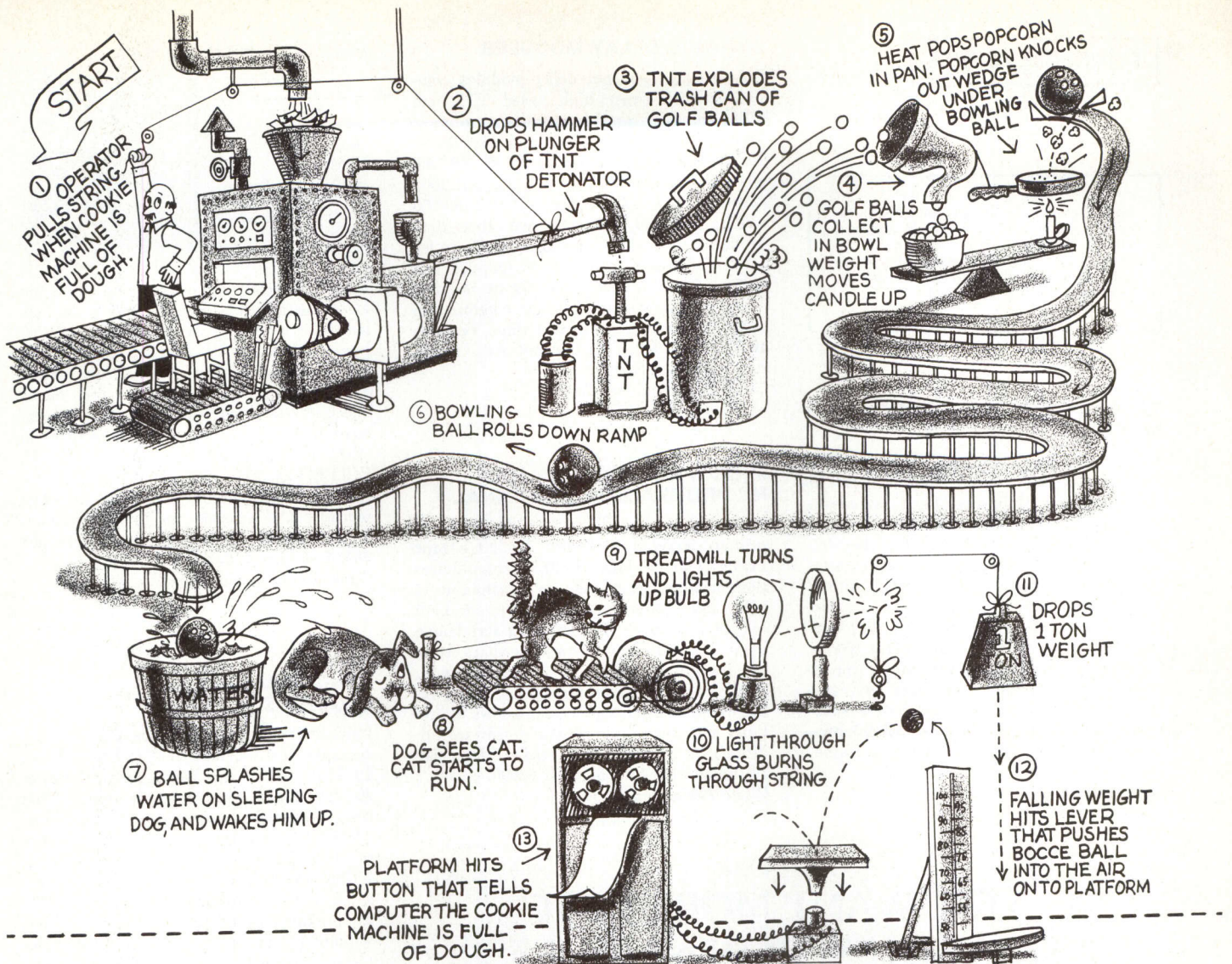
### Dot Matrix Thermal Printhead Has Multiple Capability Output

Claimed to be the first dot matrix thermal printhead capable of analog, graphic, and alphanumeric data printout onto thermally sensitive paper, the DM1096 contains a single row of 99 dots on a pitch of 24 dots/cm, with dots organized into 10 groups for multiplexed operation. Closely spaced, square shaped dots produce a high density printout. Designed to allow multiple operation for trace width expansion, the printhead incorporates complete diode isolation and integral heatsink. Since the only moving parts required with the fixed head are those for moving the paper, simplified and more reliable printer mechanisms are possible. Multiple analog traces, graphic symbols, and alphanumeric text can be simultaneously printed; and grid patterns can be thermally printed to eliminate chart tracking problems and permit complete scale flexibility in real time or for stored data printout. **Gulton Industries Inc, Electronic Components Div.**, 212 Durham Ave, Metuchen, NJ 08840.

Circle 202 on Inquiry Card







## How to avoid the interfacing nightmare.

If you've got a computer, the easiest way to avoid the kind of nightmare interfacing can become with *anybody's* machine is to simply come to us—the world's largest supplier of interface modules.

Besides being number one in sheer volume, we're also number one in technology. With a new line of microcomputer products for the LSI-11: A DMA module, an expansion backplane that doubles card capacity, and a foundation module for custom interfacing. Plus a new

line of high density wire wrap cards for our larger machines. All part of our substantial library of off-the-shelf solid state modules and compatible hardware featuring the best cost-performance ratio in the business.

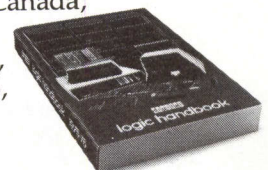
The Logic Products Group can also help you establish new designs, give all kinds of applications assistance, even develop custom designs from scratch.

Why not send for our new Logic Handbook describing all our products. It'll give you a pretty good

idea of how we can take on the interfacing nightmare.

And turn it into one sweet dream.

For your free Logic Handbook, call 800-225-9480 (Mass. 617-481-7400 ext. 6608). Or write: Components Group, Digital Equipment Corp., One Iron Way, Marlborough, Ma 01752. Canada: Digital Equipment of Canada, Ltd. Europe: 81 Route de l'Aire, 1211 Geneva 26, Tel. 42 70 50.



**digital**  
**COMPONENTS**  
**GROUP**



## PRODUCTS

**Note:** Integrated circuit and microprocessor/microcomputer products are covered separately in the "Around the IC Loop" and "Microprocessor/Microcomputer Data Stack" sections, respectively, beginning on pages 32 and 120.

### FAST FOURIER TRANSFORM MODULES

Self-contained and compact SPM-01 and -02 are based on high speed 16-bit Miproc 16 microcomputer. Modules have transform characteristic of 1024 complex points in 600 ms for -01 and 250-ms for the -02. Data input may be in either digital or analog format at inputs up to 50 kHz, with a user-optional Hanning window as a std feature. Devices will perform either forward or inverse FFT and output transformed data in analog or digital form as either real, imaginary, alternate real and imaginary, or as a computed power spectrum. **Plessey Microsystems, Microcomputer Products**, 1674 McGaw Ave, Irvine, CA 92714.

Circle 203 on Inquiry Card

### DYNAMIC DELAY MODULES

Six dynamic 5-output delay modules compatible with super high speed TTL, std TTL, and DTL provide outputs as follows: TTLDL025—5, 10, 15, 20, and 25; -050—10, 20, 30, 40, and 50; -075—15, 30, 45, 60, and 75; -100—20, 40, 60, 80, and 100; -250—50, 100, 150, 200, and 250; and -500—100, 200, 300, 400, and 500. Rise time at  $V_{CC} = 5\text{ V}$ ,  $25^\circ\text{C}$ , no load is  $\leq 1\text{ ns}$  for models -025 and -050;  $\leq 2\text{ ns}$  for -075 and -100;  $\leq 5\text{ ns}$  for -250; and  $\leq 9\text{ ns}$  for -500. Units may be cascaded in any combination without deterioration of rise time. **Technirol, Inc**, 1952 E Allegheny Ave, Philadelphia, PA 19134.

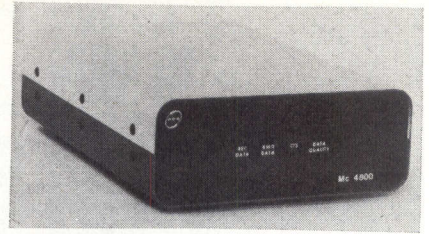
Circle 204 on Inquiry Card

### MICROPROCESSOR-BASED NC PROGRAMMING TERMINAL

Std features of the 9800 include 30-char/s printer, 300-char/s reader, 75-char/s tape punch (for Mylar), built-in communications modem, 5K of memory expandable to 64K, and winders and unwinders for both reader and punch. For use as a standalone manual terminal or as a time-share computer-assist terminal to generate, edit, duplicate, and verify tapes, the added reprogrammable microprocessor allows alterations and upgrading without hardware additions or changes. **Numeridex, Inc**, 241 Holbrook Dr, Wheeling, IL 60090.

Circle 205 on Inquiry Card

### PRIVATE LINE DATA SET



Model Mc-4800 is capable of operating on local distribution lines (loaded or unloaded) at speeds from 1200 to 19,200 bits/s. Modulation scheme meets Bell Technical Publication 43401 at all speeds. Set is both synchronous or asynchronous and operates in point-to-point or multipoint environment. For use on 2- or 4-wire facility, it is available with an EIA RS-232, CCITT V24, MIL-188C, or 20-mA loop interface. Operation on a private line 3002 facility is at speeds up to 4800 bits/s. **Data-Control Systems, Inc**, PO Box 584, Danbury, CT 06810.

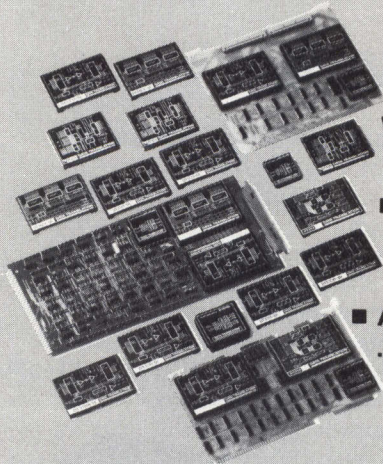
Circle 206 on Inquiry Card

### DIP-COMPATIBLE CLOCK OSCILLATOR

Including a tuning adjustment for setting accuracy of  $\pm 0.0001\%$ , CO-238T drives 10 TTL loads at any frequency in the 3- to 20-MHz range. Unit operates from 5 Vdc and provides stability better than  $\pm 0.0025\%$  over 0 to  $70^\circ\text{C}$ , with stability to  $\pm 0.0003\%$  optional. Module plugs directly into 14-pin DIL socket and measures  $0.5 \times 0.8 \times 0.35\text{''}$ . Optional module (CO-238T-2) operates over  $-55$  to  $125^\circ\text{C}$ . Models without tuning are available at frequencies up to 100 MHz. **Vectron Laboratories, Inc**, 121 Water St, Norwalk, CT 06854.

Circle 207 on Inquiry Card

## IF YOU WANT MORE IN $\mu\text{C}$ DATA ACQUISITION MODULES, YOU'LL JUST HAVE TO SPEND LESS MONEY.



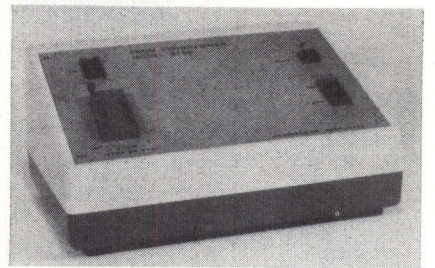
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## DATA TRANSLATION INC

23 Strathmore Rd., Natick, MA 01760/(617) 655-5300 Telex 948474

### p/ROM PROGRAMMER KIT



The 9700 kit is designed to build a completely self-contained programmer for 2708 and 2704 type p/ROMs. Housed in a high impact polystyrene case with integral power supplies, the unit features internal timing circuitry to handle p/ROM timing requirements, allowing asynchronous operation and easy interfacing with virtually any microcomputer system, and requiring only simple programs for its control. Kit includes all hardware and design documentation to build the programmer. **Engineering Resources**, 1903 Alameda Padre Serra, Santa Barbara, CA 93103.

Circle 208 on Inquiry Card



# TANDBERG

introduces the TDC 3000 Cartridge Recorder with the key to reliability: Mechanical stability.



The new Tandberg TDC 3000 Digital Cartridge Recorder uses the quarter-inch 3M cartridge. Tape format and cartridge referencing on top of the baseplate complies with the proposed ANSI/ECMA/ISO standards.

Special features in cartridge convenience and reliability are offered:

- Easy cartridge insertion, yet very positive locking in position with high forces (and electrical ejection).
- Rugged capstan motor with optical encoder for servo feedback, write clock generation and formatting by means of distance measurements, thus making the data handling completely insensitive to speed variations.
- The optional formatter can handle up to 4 drives on a bus.
- Tape speed of 10-30 ips in read/write and 90 ips in search result in 48 k bits/s data rate and low search times.
- Packing density is 1600 bpi phase-encoded and cartridge capacity is over 2,5M bytes when using all four tracks.

The modular construction enables you to configure a system to your special needs:

Built-in, single and double table top, single and double rack mount models.

Optional power supply, formatter and interfaces for PDP11, NOVA, HP, Alpha LSI, Philips P852/56, and V24 (RS 232C).

# TANDBERG

P.O.Box 9, Korsvoll, Oslo 8. NORWAY. Tel.: (47-2) 23 20 80. Telex 16441 tanra n.

Tandberg of America INC., Labriola Court, Armonk,

New York 10504 USA,

Tel.: (914) 273 - 9150 (212) 892 - 7010

RRA 41



## PRODUCTS

### INTELLIGENT REMOTE-BATCH DATA ENTRY TERMINAL



A self-contained intelligent terminal using a microprocessor with 8K of RAM storage (expandable to 12K), the Datacoder is about the size of an electric typewriter and weighs <30 lb. Data are entered via a full alphanumeric keyboard with calculator pad. Prompting messages and keyed input are displayed on a 32-char electronic display. All data are stored on a Philips type cassette; a journal tape printer gives an audit trail of data entered. Stored data are transmitted over the phone line using a built-in modem. **International Entry Systems Inc.**, 408 NE 72nd St, Seattle, WA 98115.

Circle 209 on Inquiry Card

### LIQUID CRYSTAL DISPLAYS

The DYNA SCAT™ model LCD-100 alphanumeric display is based on the principle of dynamic scattering and features a patented pins-in-glass technique that permits the LCD electrode contacts to be routed through the LCD backplate, making more dense character arrangement possible. A specially developed CMOS circuit integral with the display provides a low power ac drive to the liquid crystal. Display lines are available from four to 72 char. Avg char power requirements are 25  $\mu$ W from a 15-Vdc supply voltage. **Itek Applied Technology, a Div of Itek Corp.**, 645 Almanor Ave, Sunnyvale, CA 94086.

Circle 210 on Inquiry Card

### "CLOSED GAP" LCDs

Proprietary liquid crystal watch display process produces displays with 0.001" (0.025 mm) between segments, compared with 0.004 to 0.008" generally found. Process allows economical production and no loss of display yields. With 0.0015" between segments the D8154A series of field-effect alphanumeric LCDs feature am, pm, and data annunciators, 3-Vac drive, wide viewing angle, high stability, glass-to-glass seal, and availability with or without polarizers/reflectors. **American Microsystems, Inc.**, 3800 Homestead Rd, Santa Clara, CA 95051.

Circle 211 on Inquiry Card

### HIGH SPEED ANALOG DATA ACQUISITION SYSTEM

AI-1100, for use with mini and microcomputers, features a 32,000:1 dynamic range with complete channel processing time of <35  $\mu$ s. Each channel includes a low drift, low input bias (less than 50 pA) amp which can be set up to operate in either inverting or noninverting mode, and has an independent offset adjustment and externally accessible test points. Control panel switches allow operation in manual or automatic modes. **Recognition Systems, Inc.**, 15531 Cabrito Rd, Van Nuys, CA 91406.

Circle 212 on Inquiry Card

### LIMITED-DISTANCE MODEM

Model 7300 features a phase-delay data encoding system which generates a narrower transmitted spectrum than other 2-level techniques. Spectrum restriction results in lower transmission frequencies and allows higher transmit levels for a greater communications range. A compromise transversal equalizer offsets transmission effects of the cable and further extends the range. Range of 100,000 ft was attained at 1800 bits/s using a -6-dBm transmit level and simulated lines of #19 wire; at 19,200 bit/s, range was 52,000 ft. **Tele-Dynamics Div of Ambac Industries, Inc.**, 525 Virginia Dr, Fort Washington, PA 19034.

Circle 213 on Inquiry Card

# Your best design deserves it.

A Motorola CRT module offers the extra quality and performance a good terminal design deserves.

It's the quality you expect from a name like Motorola. The finest materials. Creative and sensible engineering. All the ingredients that make up reliability—and produce the performance that can make your system look good.

Whether your terminal is intelligent, passive, interactive, or remote. Whether it's used for order entry, inventory control, point-of-sale, situation display, text editing or video games—there's a Motorola CRT module to fit right in.

Whether you need a 5, 9, 12, 15, 20 or 23 inch screen. Whether it's for U.S. or European operation. Your design deserves a Motorola CRT module.



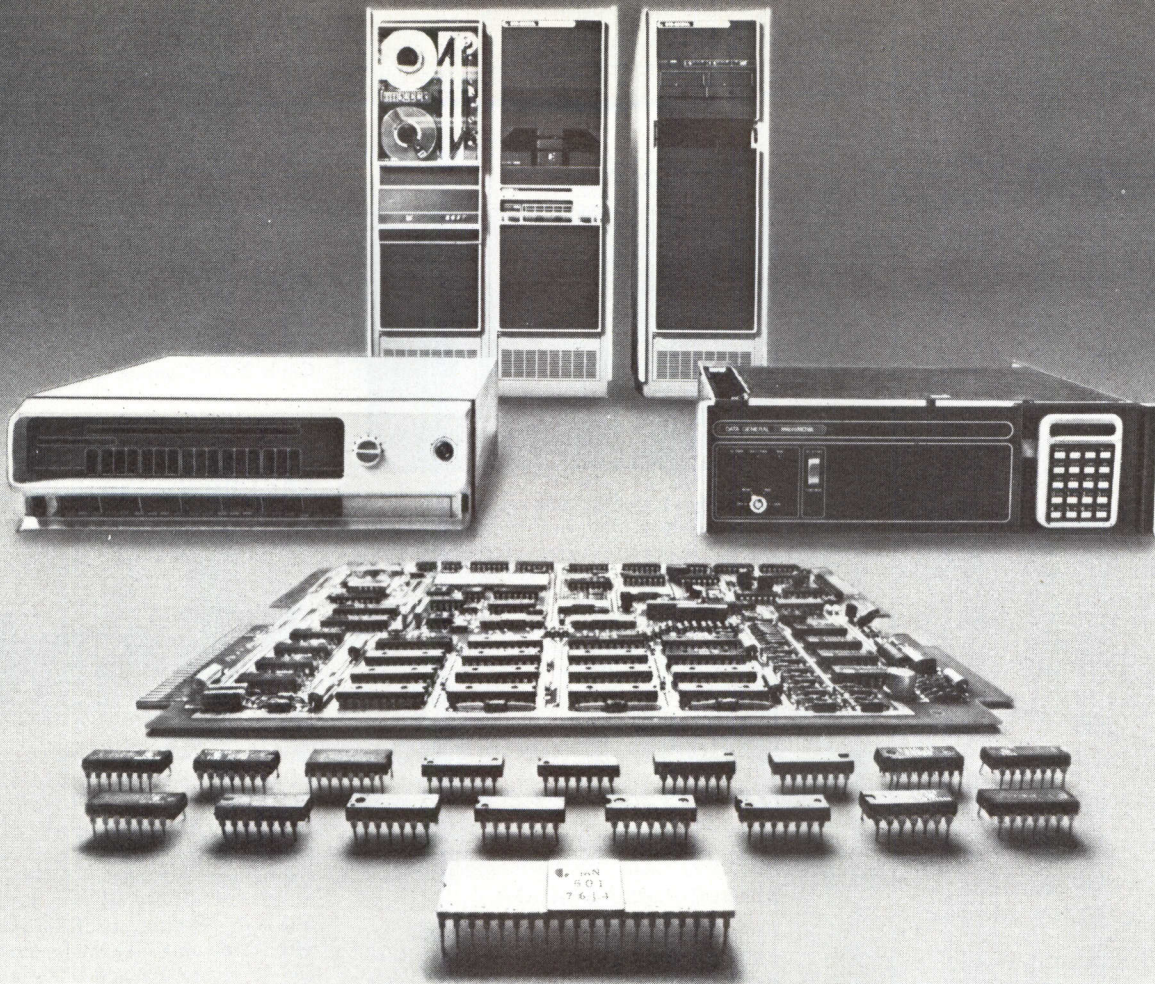
## MOTOROLA Data Products

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# With a line of minis and micros like ours, we don't have to push any one of them.

With other companies, you might set out to buy a microprocessor chip and end up with the whole chassis. Or get a box when all you need is a board.

But Data General doesn't work that way. We don't have to push you into buying something you weren't really looking for. Because we can let you choose from microprocessor chip sets, microcomputer boards, completely packaged MOS minis and full-blown NOVA 3 systems. All four are compatible. And they give you a range of performance with a range of prices.

So, if you're a component user, there are both high-performance microNOVA chip sets and microcomputer boards that feature Data General's mN601 microprocessor. The mN601 is a full 16-bit NOVA-on-a-chip. And the microcomputer is a full 4K-word computer-on-a-board. You package them yourself, for greatest economy. (Speaking of economy, the board costs only \$589 in OEM quantities of 100.)

And if you're not ready for components yet, there's our fully-packaged microNOVA MOS minicomputer. It's available with up to 32K words of MOS memory and peripherals like

our diskette subsystem. And it's supported by our Real-Time Operating System and diskette-based Disc Operating System. You can get our mini with 4K words of MOS memory for only \$1995. Or as a complete development system with the diskette.

If you need bigger systems capabilities, take a look at our NOVA 3 computer. It's compatible with our microNOVA family. And it runs with high-performance peripherals, sophisticated software like Real-Time Disc Operating System, high-level languages like FORTRAN 5 and BASIC, and memory expansion to a full 128K words.

We've got it all. But we won't try to sell it all. Unless it's what you really need. If you don't believe that line, call us. Dial 800-225-9497 (in Massachusetts, 1-617-485-9100, extension 2509) and ask for information on microNOVA and on the free half-day microNOVA seminars that happen this fall all over the country.

Or write for our microNOVA and NOVA 3 brochures. And see for yourself.

## DataGeneral

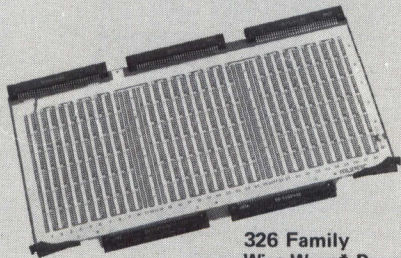
Data General, Route 9, Southboro, Mass. 01772 (617) 485-9100. Data General (Canada) Ltd., Ontario.  
Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361  
NOVA is a registered trademark of Data General Corp.

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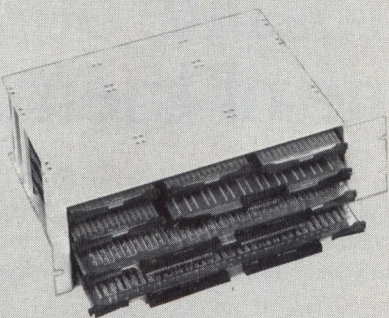
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  - panels and backplanes
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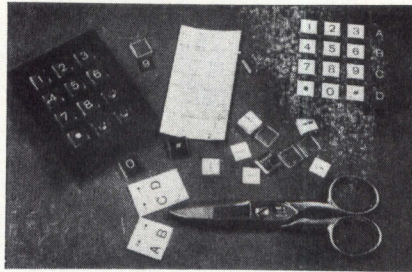


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## PRODUCTS

### MICROPROCESSOR KEYBOARD



Keyboard features removable clear cap key tops permitting easy exchange of key legends to match programming needs. Conductive elastomer sealed switches are standard with X-Y matrix, X-common, and Y-common; no interface circuitry is required. Form A with single common also is available. Keys have 0.075" travel and are on 0.650" centers. Tactile snap is optional. Both 12- and 16-key versions are available. **Flex-Key Corp.**, 18 Sargent St, Gloucester, MA 01930.

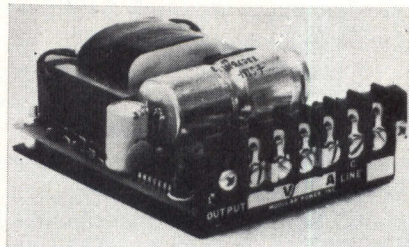
Circle 214 on Inquiry Card

### SINGLE-POINT SENSOR

The -115, a solid-state optoelectronic assembly, contains a silicon phototransistor and waveshaping hybrid circuitry. This combination of optoelectronics and solid-state electronics provides a complete square wave output, TTL-compatible subsystem. Broadband spectral response is coupled with an output capability of 10 std TTL gates to offer extensive application versatility. **HEI Inc.**, Jonathan Industrial Ctr, Chaska, MN 55318.

Circle 215 on Inquiry Card

### MINIATURE POWER SUPPLIES



PSM series feature MTBF of >100K h at 25°C. Directly interchangeable with many popular encapsulated types, the supplies provide superior thermal characteristics and ease of maintenance. Models are available in single output voltages of 5, 12, 15, 24, 28, and 250 Vdc. Output currents range from 0.05 to 1.5 A. Typ regulation is 0.03% line and load, ripple 500  $\mu$ V, and 1% pre-set voltage accuracy. All models have full protection against short circuit and overload conditions. **Modular Power, Inc.**, 4818 Ronson Ct, San Diego, CA 92111.

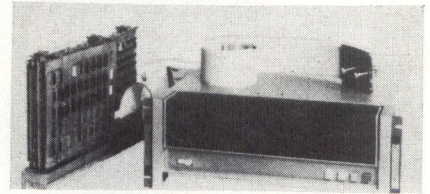
Circle 216 on Inquiry Card

### STEPPED KEYBOARD SWITCH

With a 12-deg plunger, model DI-120 has two sets of normally open cross-point contacts internally connected in parallel. Features include a double set of cross-point gold alloy contacts, rugged construction, and low contact bounce. Contact elements are in a separate assembly inside the switch enclosure. Terminals are sealed to allow soldering. Switch life is specified for 20M operations min; >6.5G test operations have been accumulated without failure. **Data Interfaces Inc.**, 12 Cambridge St, Burlington, MA 01803.

Circle 217 on Inquiry Card

### CARTRIDGE DISC DRIVE CONTROLLERS

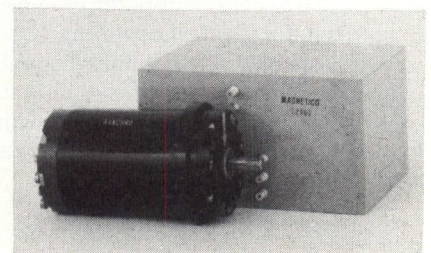


Three models, Phoenix 35, 40, and 45, are media and software interchangeable with DG 4046, DG 4234, and DEC RK-11, respectively. Additional mode of operation provides sector address verification while maintaining software compatibility. Built-in self-test verifies all data path and control logic circuitry at full operating speeds with disc units switched offline. The 35 and 40 occupy a single I/O slot in a Nova-type processor. Packaged in a std system unit, the 45 plugs into the PDP-11 power distribution panel. **Xylogic OEM Components Group, Inc.**, 42 Third Ave, Burlington, MA 01803.

Circle 218 on Inquiry Card

### HIGH POWER SYNCHRO DRIVER

Driver takes 9-V rms sine and cosine information, 60 Hz, and converts it to 90-V line-to-line synchro information, capable of driving a 25-VA load. Linear design and balanced construction techniques provide 2-arc minute accuracies; balance is such that accuracy is not affected by load. In a 3 x 4 $\frac{3}{4}$  x 2 $\frac{1}{4}$ " hermetic can, unit meets all rugged environment specs of MIL-T-27 and is operable from -55 to 125°C. Input impedance is more than four times the reflected load impedance. A 90-V line-to-line, 100-VA, 400-Hz unit is available in the same size. **Magneto, Inc.**, 182 Morris Ave, Holtsville, NY 11742.



Circle 219 on Inquiry Card



# THESE LOW-COST CASSETTE PROGRAM LOADERS DELIVER TOP PERFORMANCE FOR YOUR MICROPROCESSOR BASED SYSTEMS.

All four of these program loaders use EPI's patented Speed Tolerant Recording (STR®) technique to give you bit error rates of less than 1 soft error in  $10^7$  bits and less than 1 hard error in  $10^8$  bits. With STR, you get high data reliability in read and write modes while using a relatively low-cost recorder

and inexpensive tape cassettes.

Interfacing is similar to most paper-tape reader/punch units now in use. And with better data reliability, faster loading, more storage, lower price, and briefcase or rack mounting, EPI cassette program loaders make sense for both the

end user and OEM.

For more information on these low-cost alternatives to paper tape loading, contact Electronic Processors Inc., 1265 West Dartmouth Ave., Englewood, Colorado 80110. Phone (303) 761-8540.

**ELECTRONIC PROCESSORS  
INCORPORATED**

**Custom designs**, like this STR-110T for the Texas Instruments 5TI Programmable Control System, can handle your special loader needs. You can get an intelligent loader... automatic verification in both read and write modes... remote control. Tell us what you need. Chances are an EPI STR loader can handle it.



**8-bit parallel** loading at standard TTL levels and at transfer rates to 125 characters per second is provided by the STR-210. Its high speed and storage capacity of 100,000 characters on a 300-foot cassette makes it ideal for memory dumps as well as program loading. Priced at just \$700.

**OEM systems recorder**, the STR-100, is a complete tape-drive unit that provides full remote signal or character control of all transport functions. It includes read-write electronics, control and timing logic, and motor-control logic. All you need to supply is a mounting location, power supply, and an interface with the controlling I/O device and you have a reliable unit for program storage and retrieval.

**8-bit serial** loading with switch-selectable rates to 1,200 baud are provided by the STR-LINK. The transmission mode (half or full duplex) is also switch selectable for maximum flexibility. Data capacity is 100,000 characters on a 300-foot cassette. Priced at \$1,190.



## PRODUCTS

### PAPER TAPE TRANSMITTER



A self-contained punched tape reader-transmitter with an integral power supply and RS-232-C serial interface with dual outputs (modem and terminal), model 1200 interfaces directly to intelligent terminals, CRT displays, printers, and data terminals. It plugs directly into the LA36 DECwriter. Features include switch-selectable transmission rates of 110, 150, 300, 600, and 1200 baud; built-in carriage return delay of 0, 200, and 600 ms; parity selection; and either line or local operation. **BAI Data Products Div**, PO Box 681, Cherry Hill, NJ 08003.

Circle 220 on Inquiry Card

### VIDEO-TO-ANALOG CONVERTER MODULES

Model 6280 provides a means of converting a single input composite video signal into three separate analog outputs: video only, vertical ramp, and horizontal ramp. Vertical sync pulses and horizontal plus vertical sync pulses are also available. Video output is selectable as either positive or negative. Horizontal and vertical deflection ramp outputs and video outputs have 10-V full scale amplitude. The unit allows std composite video to be monitored on conventional XY analog displays. **Optical Electronics, Inc**, PO Box 11140, Tucson, AZ 85734.

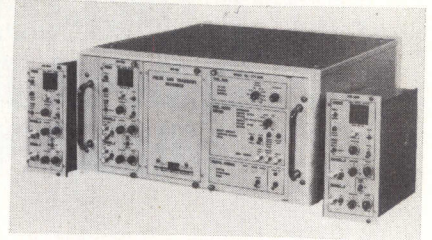
Circle 221 on Inquiry Card

### GRAPHICS DISPLAY JOYSTICK

An interactive device for computer graphics, Megagraphic Joy-A and -B allow the operator to quickly and accurately position a cursor on the CRT. -B has a user-controlled switch at the end of the stick to provide status information. In actual use, the operator depresses the button when he has positioned the cursor at the desired location on the CRT. Electronics provide minicomputer interrupts at a 100-Hz rate. Interfaces are available for Data General Nova and Eclipse series, and DEC PDP-11. **Megatek Corp**, 1055 Shafter St, San Diego, CA 92106.

Circle 222 on Inquiry Card

### TRANSIENT RECORDER SYSTEMS



PTR-9000 series records at sample rates to 100 MHz with 8-bit resolution; the recorded waveform may be continuously displayed, plotted, or transmitted to a computer. Systems feature high impedance interchangeable input modules and simplified control. Access of appropriate control signals simplify system integration. Memory is expandable from 2K to 8K samples by use of a RAM, which provides access to any sample for reading, modifying, and rewriting data into that cell. **American Electronic Laboratories, Inc**, PO Box 552, Lansdale, PA 19446.

Circle 223 on Inquiry Card

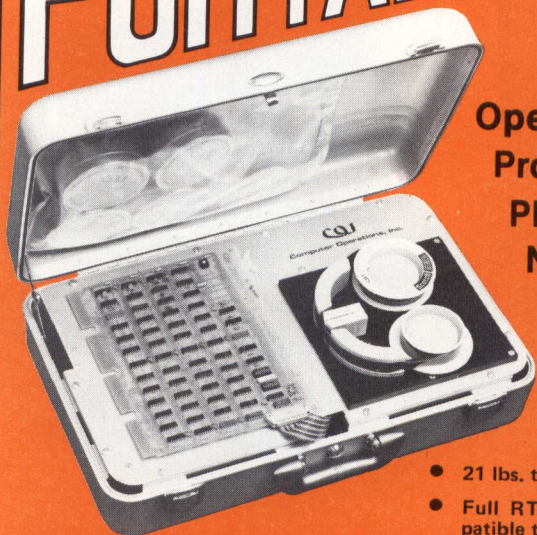
### CNC CONTROL

Model 380C2 control is aimed at 3-axis machine tool applications. Unit features cutter radius compensation; linear, circular, and helical contouring; absolute and incremental programming and jog modes; automatic EIA/ASCII code recognition; and automatic search to block number. Options provide multilevel program storage of up to 470 ft of tape input, program editing at the control, and 4th, 5th, and 6th axis drive systems configured to suit the application. Unit can program linear motion simultaneously with execution of circular commands. **Icon Div, USM Corp**, 156 Sixth St, Cambridge, MA 02142.

Circle 224 on Inquiry Card

# PORTABLE

# COU



**Operating System/  
Program Loader for  
PDP-11<sup>®</sup>/LSI-11,  
NOVA<sup>®</sup> and  
Micro-Computers  
The Linear Disc-  
LINC TAPE**

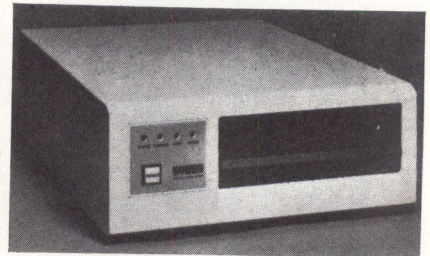
- 21 lbs. total weight
- Full RT-11 support on DECTape<sup>®</sup> compatible tapes for PDP-11/LSI-11
- Full SOS with named files support for NOVA computers
- Edit, Assemble, Compile programs in the field
- Fill 16K word, 16 bit memory in 4 sec.
- Load diagnostics quickly and reliably
- Fits under airline seat or check as baggage
- XXDP support for PDP-11

**\$2295 (unit qty)  
w/controller**

**Computer  
Operations, Inc.**

9700-B GEORGE PALMER HWY.  
LANHAM, MARYLAND 20801  
(301) 459-2100 • TELEX 89-8327

### FLOPPY DISC SYSTEM

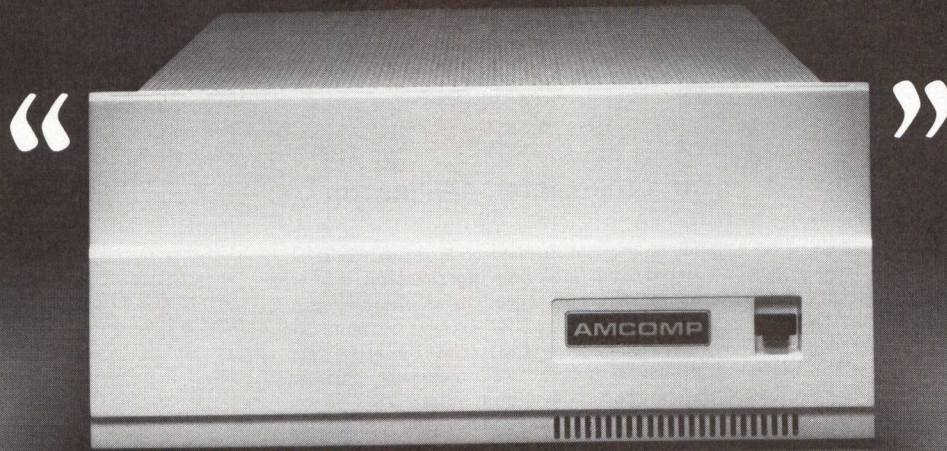


Series 8000 communications RS-232 Comm-Stor system interfaces directly with all RS-232 terminals, printers, and modems. Unit is designed around a microprocessor which uses a message (file) oriented directory for flexibility in storing and retrieving data. Main features include nine selectable baud rates up to 9600, single- or dual-drive unit, off/online operation, alpha or sequential message sort, full message editing, forms operations, printer port, and capacity of over 240K char/disc. **Sykes Datatronics Inc**, 375 Orchard St, Rochester, NY 14606.

Circle 225 on Inquiry Card



# Our statement on high density head-per-track disc technology:



For quite some time now, there's been a real need for a low profile, high capacity head-per-track disc.

To reduce system space requirements. To reduce system complexity. To reduce system costs.

And while the need was there, the technology wasn't.

Until now.

Introducing the AMCOMP 8500 Series Disc Memory Unit. It has a capacity of 38.4 million bits. It's only 8.75" tall, including power supply, and fits a standard 19" rack. It has a phenomenally low cost of 0.019 of a cent/bit in typical OEM quantities.

And it's available – right now.

There's even more:

A choice of speeds – 1800 or 3600 rpm – at no extra cost.

International voltage handling capability – standard.

And two special options: A sealed disc cavity with sustaining gas supply, and a ruggedized chassis – both to insure the 8500 working under the most difficult working conditions.

The 8500 low profile, high density, head-per-track disc. Proof of AMCOMP's commitment to design for tomorrow, and manufacture for delivery today.

To find out more about the 8500 or our other products and services, please call your nearest AMCOMP office, or AMCOMP, INC., 686 West Maude Avenue, Sunnyvale, CA 94086, phone (408) 732-7330.

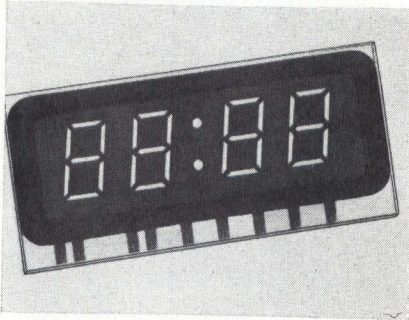
AMCOMP – technology that delivers.

## AMCOMP



## PRODUCTS

### 4-DIGIT GAS DISCHARGE DISPLAY



Display, featuring 1/2" high numerals in a compact envelope, measures 1 1/4 x 2 3/4" long and has colon for minutes and seconds indication. W04-0003 offers visibility from up to 20 ft. Each digit, in neon orange color which may be filtered to deep red or bright orange-yellow, has uniform brightness. Multiplexed to minimize external connections, unit is available with unitized connector that has bifurcated pins for added reliability. **Cherry Electrical Products Corp.**, 3600 Sunset Ave, Waukegan, IL 60085.

Circle 226 on Inquiry Card

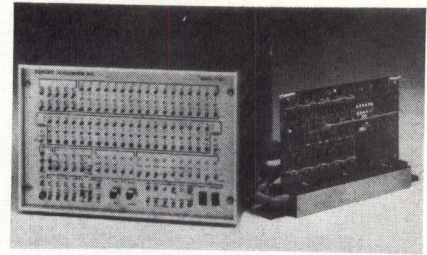
### IEEE STD INTERFACE FOR COUNTER/TIMERS

An internal bus interface option, 1953A Option 15 permits interconnection between the 1953A and other bus-compatible instruments having the standard interface. The option uses the recommended ASCII code format and permits full remote operation of range and function selection, control of A and B trigger slopes, ac-dc coupling, attenuation selection, and separate-common input status between channels A and B. Output consists of nine digits of display data plus decimal point and exponent for frequency or time units. **John Fluke Mfg Co, Inc.**, PO Box 43210, Mountlake Terrace, WA 98043. Circle 227 on Inquiry Card

### AC TACHOMETER GENERATOR

An easily installed, low cost, low maintenance way of supplying a speed feedback signal from motor to the regulator section of an adjustable-speed drive, the -050 provides a 12-Hz/rev ac signal. Outputs are rated 50 Vac at 1000 rpm. Double C-face design permits direct mounting between motor and driven unit, eliminating power transmission components and alignment problems. No tachometer mounting kit is required. Both 56C and 140TC sizes are offered. **Reliance Electric Co.**, 25001 Tungsten Rd, Cleveland, OH 44117. Circle 228 on Inquiry Card

### RANDOM-ACCESS MEMORY TESTER



Bench-top T-115 provides high speed, low cost memory testing suitable for production, acceptance, and incoming inspection. Basic unit tests configurations up to 512K words x 20 bits. The standalone self-contained system includes performance board, test fixture, and power supplies, and tests multiple memory types by using different plug-in performance boards. Schottky logic and 3-state computer type buses provide flexibility previously not available in table-top memory testers. **Concept Development, Inc.**, 3198 G Airport Loop Dr, Costa Mesa, CA 92626.

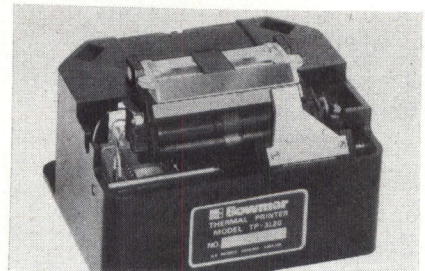
Circle 229 on Inquiry Card

### REFLECTIVE TRANSDUCER

A combination of high efficiency solution grown LED with a silicon phototransistor assures maximum reliability of the transducer. Model OPB 704 features hermetically sealed glass-metal-ceramic package, offering high reliability and stable performance. Usable continuous operating life is >5 yr when operated at avg LED device current of 20 mA. Phototransistor senses radiation from LED only when reflective object is within its field of view. LED input current is 50 mA. **Optron, Inc.**, 1201 Tappan Cir, Carrollton, TX 75006.

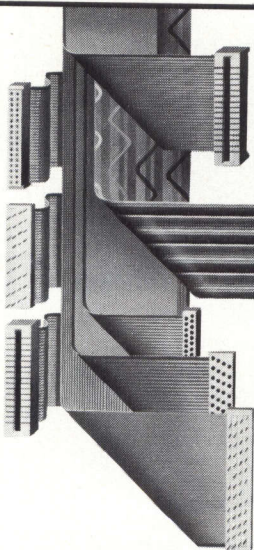
Circle 230 on Inquiry Card

### THERMAL PRINTER



Fully MOS compatible with right/left justification and 5 x 5 matrix design, the TP-3120 has an MTBF rate for the thermal printhead of >3M characters, with a general operating life of >1M lines of printing. Operating at a speed of 29.4 chars/s and 1.07 printed lines/s, the printer also features complete alphanumeric printout, low power consumption, quiet operation, economical high contrast nonsmear paper usage, and 12-position dual readout std connector. **Bowmar Instrument Corp.**, 8000 Bluffton Rd, Fort Wayne, IN 46809. Circle 231 on Inquiry Card

## Other flat cable/connector systems just became old fashioned.



Meet the new Great Jumpers™ and Great Daisy Jumpers™ from A P Products. They come from our factory fully pre-assembled and fully pre-tested, complete with molded-on connectors featuring integral strain relief and complete line-by-line probeability, yet can cost half as much as the jumpers you're using now.

Just name your jump and watch us hop to it. We offer the three most popular connectors, the five most popular flat cable widths, solid or stranded Electric Pink or rainbow cable, single ended, double ended or daisy chained. And Great Jumpers are directly-interchangeable replacements for the jumpers you're using now.

Connect with the A P rep nearest you.

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(212) 682-5844	(303) 420-4646	(414) 421-2300	(602) 946-4437	(714) 560-6266
(214) 238-0408	(305) 894-3351	(415) 328-3232	(602) 949-8424	(714) 833-1802
(215) 923-5195	(312) 298-4830	(416) 638-1322	(609) 429-4013	(816) 765-2998
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Faster and easier is what we're all about.



**A P PRODUCTS INCORPORATED**

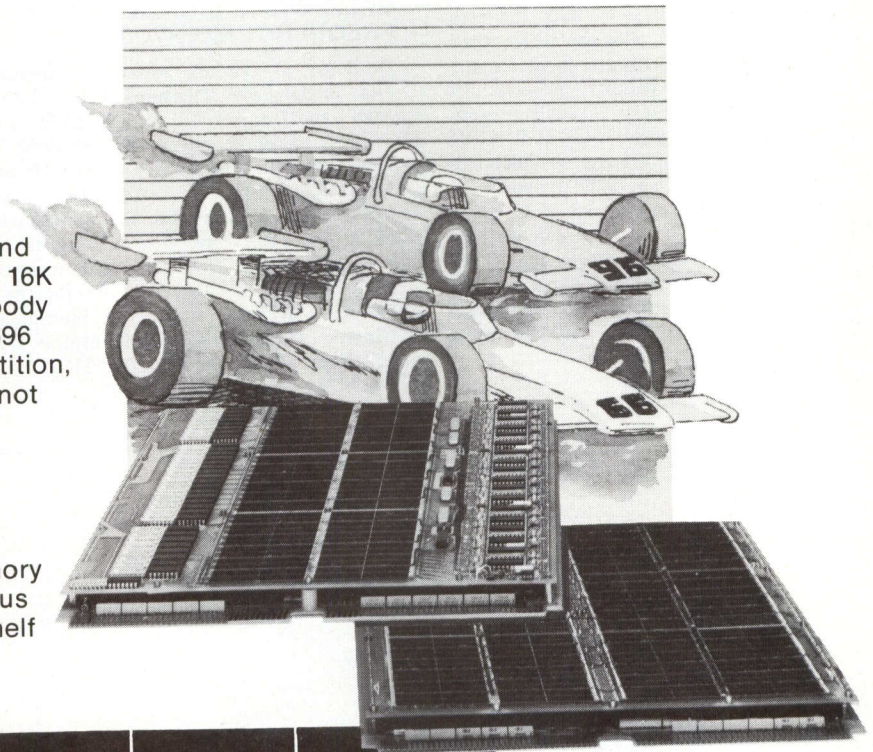
Box 110-CD Painesville, OH 44077 (216) 354-2101 TWX: 810-425-2250



# Who's the performance winner in 16k and 32k memory systems?

## Check the specs.

Fabri-Tek has packed more speed and total performance into single-board 16K and 32K memory systems than anybody else in the business. Compare our 696 and 698 systems against the competition, and you'll see what we mean. We'll not only beat them in specifications—we're the only company that offers you total upward compatibility to 32K. At competitive prices, too. It's what you'd expect from a company with years of leadership in the memory business. Go with the winner—call us today for the best in both off-the-shelf and custom memory systems.



MODEL	FABRI-TEK		EMM		DATA PRODUCTS		DATARAM	
	696	698	Micro 3000 D.D.	Micro 3000 Q.D.	Store 1680		DR-103	DR-103
MEMORY SIZE	16K	32K	16K	32K	16K	32K	16K	32K
CYCLE TIME	650	650	650	850	650		650	750
ACCESS TIME	250	250	270	300	280		265	300
PHYSICAL SIZE	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0		11.5x13.7 x1.0	11.5x13.7 x1.0
COMPATIBILITY 16K TO 32K	YES		NO		NO		NO	

**FABRI-TEK** INC.  
COMPUTER SYSTEMS

5901 South County Road 18 • Minneapolis, MN 55436 • (612) 935-8811

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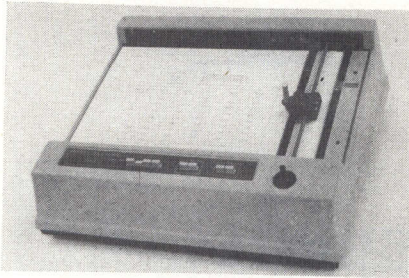
San Jose, Calif.  
(408) 246-8391  
John French

Minneapolis  
(612) 935-8811  
Jack Graham



## PRODUCTS

### INTERACTIVE DIGITAL PLOTTER



The 4662 can interface to both the company's products and alphanumeric terminals. Plotter has a hardware character generator, digitizing capability, 22-in./s pen speed, 0.005" accuracy,  $\pm 0.0025$  repeatability, and both RS-232-C and GPIB (IEEE 488-1975) interfaces. A 1600-byte input buffer optimizes data transfers, allowing data to be transferred at 110, 150, 300, 600, and 1200 baud. Unit couples with 4051 graphic system through the GPIB interface to provide hardcopy up to 10 x 15" image size. **Tektronix, Inc., Information Display Div**, PO Box 500, Beaverton, OR 97077.

Circle 232 on Inquiry Card

### INTERACTIVE GRAPHICS SYSTEM

A tool for creating finished schematics, PC board artwork, design rule checking, and assembly documentation, CDS (Circuit Design System) treats design and documentation as one task made up of a series of related steps, providing specific tools for each step. Component catalog eliminates need for typed or digitized input; schematic is input via a data tablet and CRT. Component placement and interconnection routing are completed using automatic and interactive techniques with no design constraints. **Adage, Inc.**, 1079 Commonwealth Ave, Boston, MA 02215.

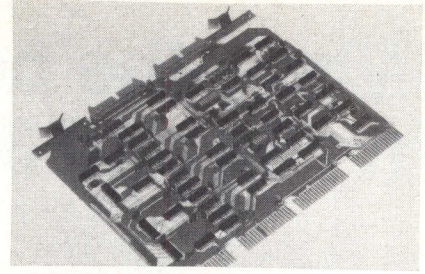
Circle 233 on Inquiry Card

### SOLID-STATE DIGITAL FREQUENCY MONITOR

Designed to monitor power line frequencies, model LF60 measures 4.75 x 3.25 x 3.40", and features 4-digit, 0.4" LEDs. Frequency measurement range is 10.00 to 99.99 Hz, with an accuracy of 0.01 Hz and an update rate of 1 s. Accuracy is controlled by a crystal with an aging factor of 20 ppm/20 years. Power input is 110 V  $\pm 20\%$  or 220 V  $\pm 20\%$ , with measurement input from 1 to 300 V. Parallel BCD output is available for remote interfacing. **Electro Industries, Panel Meter Div**, 109 Nassau Dr, Albertson, NY 11507.

Circle 234 on Inquiry Card

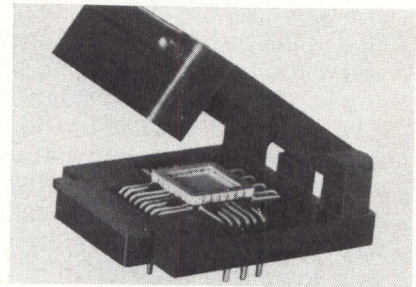
### I/O BUS CONVERTER



RTP7410/65 converter is contained on a single PC board that is plug compatible with the DEC PDP-11/03 computer and can adapt to the LSI-11 by using std 4-section DEC connectors. Board allows RTP family of analog and digital I/O measurement and control equipment to be operated under control of the computer using the computer's std software. Up to eight RTP controllers can be connected to one converter in daisy-chain fashion using RTP I/O cables. **Computer Products, Inc.**, 1400 NW 70 St, Fort Lauderdale, FL 33309.

Circle 235 on Inquiry Card

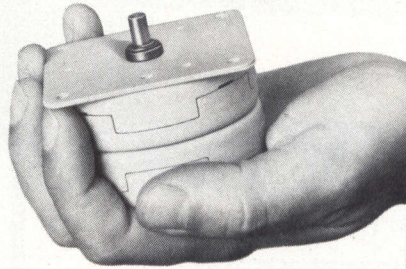
### SEMICONDUCTOR TEST SOCKET



"Chip carrier" series offers models capable of accepting carriers with from 14 to 18 leads and body sizes up to and including 0.500" square. Minor tooling changes allow the socket to accept plastic "leaded" packages <0.500" square with 2- or 4-side, straight or formed leads. Positive locking system enables loading and unloading with the fingers. Pressure pad in the socket lid is adjustable for thick or thin packages. Lid eliminates shorting against contacts or PC board. **Textool Products, Inc.**, 1410 W Pioneer Dr, Irving, TX 75061.

Circle 236 on Inquiry Card

## Introducing the efficient little 82900 stepper motor



It gives you an edge on compactness, torque and price.

It's new. It's bidirectional. It has a 7.5° step angle. It gives you maximum pull-in/pull-out torque of 23 oz-in @ 200 pps. It's rated at 12.38w @ 5vdc and runs at lower than average temperatures.

The 82900 has a lot to offer, particularly in impact and non-impact printers, small X-Y plotters and computer peripherals. It's powerful, compact and moderately priced. And it's reliable. So reliable — in fact — that it can also be used to control pumps and valves in medical instruments and similar devices. In many applications it can replace larger, bulkier steppers at much lower cost.

Standard construction provides 2-phase operation (requiring simplified, low-cost circuitry), a 7.5° step angle and roller bearings. However, 4-phase operation, a 15° step angle or sleeve bearings can be furnished as options.

Write for information today!

A. W. HAYDON CO. PRODUCTS

NORTH AMERICAN PHILIPS CONTROLS CORP.


Cheshire, Conn. 06410 • (203) 272-0301

### HYBRID SOLID-STATE RELAY

The TTL-compatible 241 series miniature relay for low power applications is UL recognized under file #E47012, and provides a reliable switch with a ¼-A rating at 120 Vac. Its one cycle surge current rating is 2.5 A peak. Isolation specs are 1500-Vac min dielectric withstanding voltage and 10<sup>10</sup> Ω insulation resistance. Std input ratings of 5, 12, or 24 Vdc are available. Other features include reed relay input and triac output. **C. P. Clare & Co., a General Instrument Co.**, 3101 W Pratt Ave, Chicago, IL 60645.

Circle 237 on Inquiry Card





**LSi** **Dumb Terminal**  
**NOW FORTIFIED WITH DCA!**

A single Dumb Terminal currently provides all of the following key ingredients:

- ..... DIRECT CURSOR ADDRESSING
- 12" ..... Diagonal Screen
- 960 ..... Upper Case Character Display
- 59 ..... Data Entry Keys
- 32 ..... Positive Action Switches
- 11 ..... Selectable Baud Rates† (from 75 to 19,200)
- 1 ..... RS232S Interface
- 1 ..... 20mA Current-loop
- 1 ..... Hatchback Bonnet

†No official minimum requirements have yet been established.

NET WEIGHT: 25 lbs.  
 The Dumb Terminal (ADM-3A) is a product of Lear Siegler Inc. Anaheim, California

# NOW FORTIFIED WITH DCA\*!

\*DCA means Direct Cursor Addressing. And that's exactly what you'll find added to each and every ADM-3A Dumb Terminal from Lear Siegler. As a basic, standard ingredient.

Now our Dumb Terminal's even more of a snap to use. Because direct addressing lets the operator tell the cursor—quite literally—where to go. Up. Down. Right. Left. Any X and Y location you choose. Even where to home.

Your operators will tell you it's "GRRRRREAT!" Not to mention fast and simple. For tracking down typos. Typing in additions. Even for retyping entire passages. Because if the problem's still on the screen, it's open to instant improvement.

What's more, the Dumb Terminal still provides a balanced diet of your favorite standard features. Like a bright 12" diagonal screen. Fifty-nine data entry keys. A 960 character display. Plus 32 positive action switches that let you activate goodies like 1 of 11 different baud rates, an RS232S interface, or a 20mA current-loop. And more. All handsomely packaged in a handy hatchback bonnet.

And if you want to sweeten up the deal by adding switch-selectable options, you've got your pick of plenty. Like a complete upper and lower case USASCII character set, a 1920 character display, or even an "answer-back" capability.

So forget the flaky imitations with their puffed-up, premium prices. (And join the thousands who already start their day, in an LSI kind of way.)

Because what the Dumb Terminal—now fortified with DCA—really delivers, you won't find anywhere else. Not even in Battle Creek.



**DUMB TERMINAL. SMARTER BUY.**

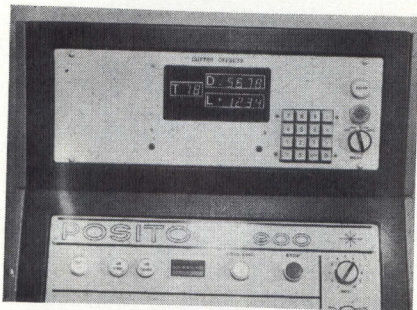
Forget the box tops, for more information contact:  
 Lear Siegler, Inc./E.I.D., Data Products

714 N. Brookhurst St., Anaheim, CA 92803  
 Tel. (714) 774-1010



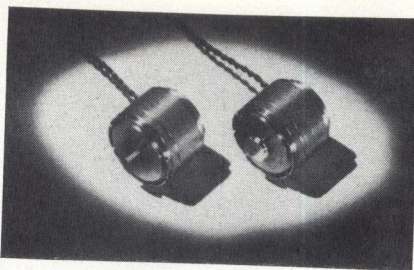
## PRODUCTS

### OFFSET ENTRY SYSTEM



Keyboard and memory system, with length and diameter display, has 78 pairs of offsets available to the programmer. System is supplied for applying tool length compensation alone, or tool length with cutter diameter compensation. Offset information is entered via a keyboard and is shown on  $\frac{1}{2}$ " high, 7-bar gas discharge displays to verify correct entry. Offset values in actual use are also displayed during a tape run. A 72-h backup battery system ensures memory retention when the control is switched off. **Posidata Ltd**, Whitney Rd, Daneshill East, Basingstoke, Hampshire RG24 0NS England.  
Circle 238 on Inquiry Card

### COMPACT IRONLESS ROTOR DC MOTOR



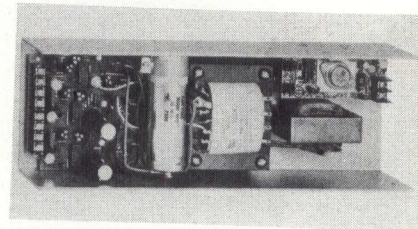
Series 4322-010-77000 motor, designed for 9-Vdc operation, has a 0.76-gcm<sup>2</sup> moment of inertia, 8.5-gcm starting torque, and a motor constant of 50 ms typ. Gold-plated 5-segment commutator and silver-plated brushes are used for optimal commutation. Features include low noise levels, rapid acceleration, and low cogging. Basic motor is available with a premounted 8.1 x 1.5-mm pulley. **North American Philips Controls Corp**, Cheshire Industrial Park, Cheshire, CT 06410.  
Circle 239 on Inquiry Card

### MINIATURE SLIDE SWITCHES

The design for wave soldering this family of switches allows accessible cleaning and facilitates automatic handling. Engineering permits easy installation while eliminating failures due to residual contamination from wave soldering processes. With

contacts of hard gold over a nickel barrier, Mr Clean™ switches are designed for low energy applications. Available in spst, spdt, dpdt, and form Z circuit configurations, switches measure 0.50 x 0.30 x 0.25". **Chicago Switch, Inc**, 2035 Wabansia, Chicago, IL 60647.  
Circle 240 on Inquiry Card

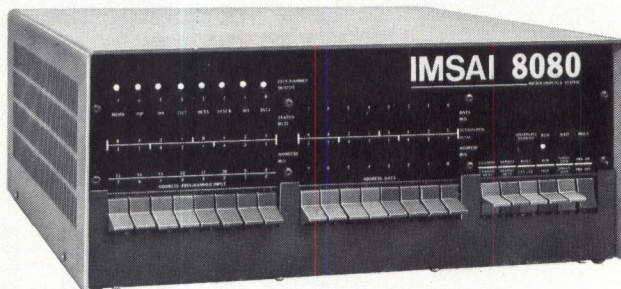
### MICROPROCESSOR POWER SUPPLIES



Six models of "Quad" series 4-output supplies consist of either MPS-2 and QPS series, or QT-2 and QPS series power supplies mounted on a common chassis. Model 8888 consists of a QT-2 triple output supply rated 5 Vdc at 6 A, and  $\pm 12$  to  $\pm 15$  Vdc at 1 A, assembled with any of the three QPS models. Model 8899 consists of an MPS-2 triple output supply rated 5 Vdc at 7 A, 12 Vdc at 1 A, and 9 Vdc at 1.2 A or 5 Vdc at 0.75 A, also assembled with any of the three QPS models. **Deltron, Inc**, Wissahickon Ave, North Wales, PA 19454.  
Circle 241 on Inquiry Card

# If you thought computerizing your system for less than a grand was impossible,

## think IMSAI 8080.



The IMSAI 8080. It's rugged, reliable, commercial grade. It's everything you'd expect from a \$5,000 computer, for under a grand. Fully assembled, the 8080 is \$931. Unassembled, \$599. For dedicated applications, it's available without the front panel for \$749 and \$529. At those prices, now you can have true computer power in applications unheard-of before.

The microprocessor card uses INTEL's 8080A processor chip and includes clock, tri-state bus drivers, control signal timing. The IMSAI 8080 is optionally expandable to a substantial system with 22 card slots in a single printed circuit board. It will

accommodate 64K of software protectable memory plus an intelligent floppy disk controller with DOS. And an 8 level priority interrupt system. Asynchronous and synchronous RS232, current loop, serial I/O and TTL parallel I/O.

A unique multiprocessor shared memory facility is available. Extended BASIC available.

The heavy duty front panel has an extra 8 program controlled LED's, and it plugs directly into the Mother Board without a wire harness. The switches are rugged, commercial-quality, and are backed up by reliable debouncing circuits.

For a free, complete illustrated IMSAI 8080 brochure describing options, peripherals, software, prices and specifications, write IMS.

The IMSAI 8080. From the same technology that developed the HYPERCUBE Computer architecture and Intelligent Disk systems.

# IMS

**IMS Associates, Inc.**  
14860 Wicks Boulevard  
San Leandro, CA 94577  
(415) 483-2093

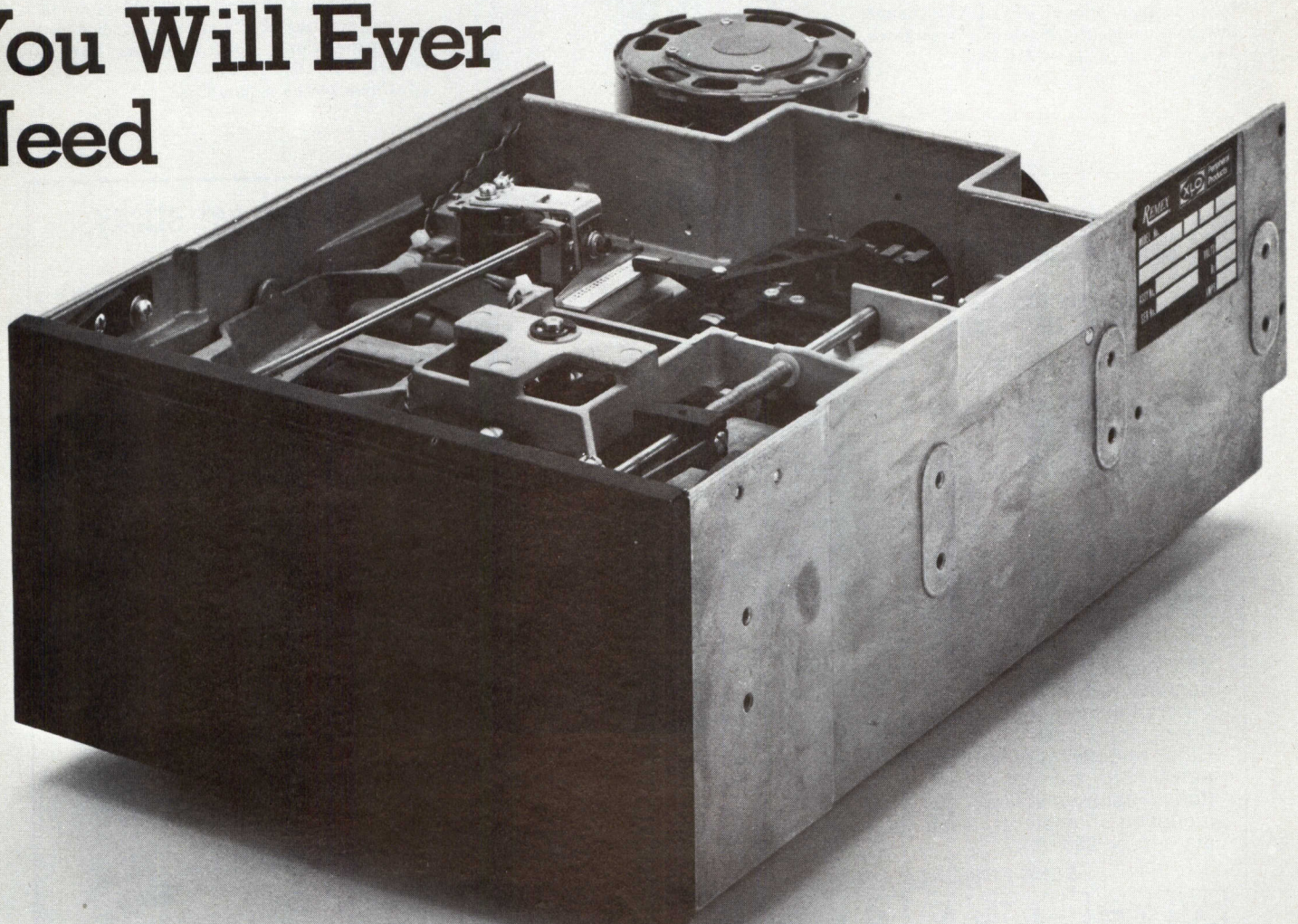


**The REMEX RFD 1000 — Because It's Versatile.** Double or single density with capacity up to 6.4 Mbits... IBM standard or 32 hole hard sectored media without drive modification... IBM compatible or expanded hard and soft sectored formats for application flexibility... Unit select daisy chain capability for maximum controller efficiency... Selectable DC negative voltage for system compatibility... Individual drive housing or two drives horizontally side by side in a 19 inch rack configuration.

**The REMEX RFD 1000 — Because It's Reliable.** Ceramic head for extended life... Precision machined, die-cast construction... Operator interlock and expandable clutch for media protection... Front panel "head in contact" indicator and optional "head in contact" door lock... Optical write protect to assure data security... Stylus ball lead screw positioning system for long-lived accuracy... Optical track 00 sensing for drive carriage protection.

The Remex RFD 1000 is the RIGHT peripheral from Remex.

# This Is The Only Flexible Disk Drive You Will Ever Need



**Ex-Cell-O Corporation**

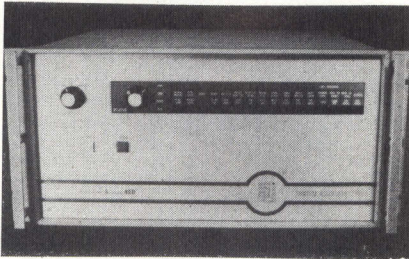
**REMEX DIVISION**

1733 E. Alton Street, P.O. Box C19533, Irvine, California 92713  
(714) 557-6860, TWX (910) 595-1715. In Europe and the U.K.: SpA, Microtecnica  
Via Madama Christina 147, Torino, Italy 10126.



## PRODUCTS

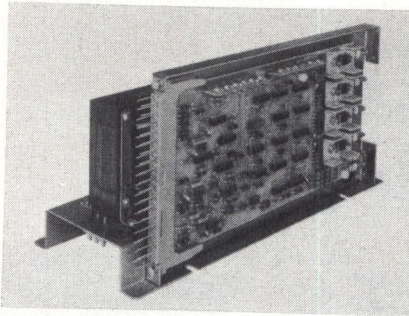
### HIGH SPEED COMMUNICATION SUPPORT



Software and hardware support for high speed communication under DEC RT11 and COMTEX executives is provided by Long Line Adapter hardware which, using a single coax, sends data up to 1.5 miles at 277K char/s. Software support and DMA hardware operation allow networks of computers using FORTRAN and assembly language programs to communicate with low overhead. High performance IBM 370/360 frontend applications can be implemented by including optional DEC DX11 channel interface support. **System Associates, Inc.**, 55 Park St, Troy, MI 48084. Circle 242 on Inquiry Card

### PRESET INDEXER MODULE

Designed to provide the correct switching sequence necessary to control bifilar wound dc stepping motors, PIM151 is a 5 3/4" x 11" plug-in module capable of complete control of motor speed, direction, and distance. It can be incorporated into microprocessor systems. Internal oscillator provides stepping rates to 1000 pulses/s; counting circuits assure that motors are driven the correct number of steps. Steps up to 99,999 max are selected by external conventional BCD logic switches. **Superior Electric Co.**, 383 Middle St, Bristol, CT 06010.



Circle 243 on Inquiry Card

### PRINTER TESTING DEVICE



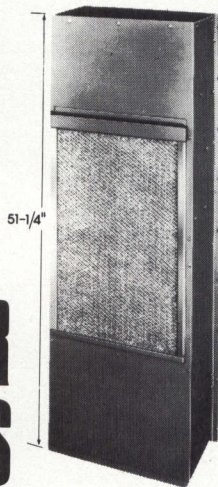
A palm-sized black box that works in conjunction with the Sprint Micro 3 printer's MOS/LSI microprocessor, the Micro 3 activity monitor conducts a diagnostic check of the printers in 35 s. Operating without extra power sources or special tools, it surveys printer microprocessor and ROM memory, checks all I/O lines sequentially, then drives the printer carriage through 100 separate print maneuvers. Printwheel is exercised through 96 positions; and paper feed, ribbon advance, and printing ability are performance tested. **Qume Corp.**, 2323 Industrial Pkwy W, Hayward, CA 94545. Circle 244 on Inquiry Card

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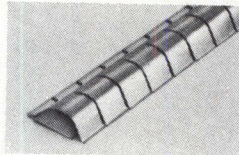
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**MCLEAN** ENGINEERING LABORATORIES

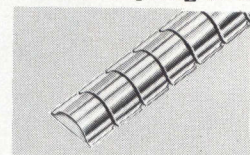
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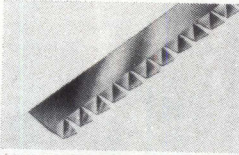
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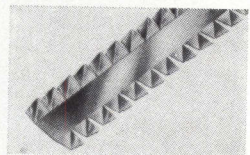
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### COURSE OUTLINE

1. BASIC ELEMENTS OF A MICROPROCESSOR SYSTEM
2. LSI TECHNOLOGIES
  - TTL, SOS, CMOS,  $1^2L$ , PMOS, NMOS • Comparison in terms of: radiation hardness, noise immunity, temperature, humidity, shock and vibration, power instability
3. TECHNICAL SURVEY OF MIL-SPEC DEVICES
  - Comparison of: availability, architecture, speed, power, required support circuitry, development-aids, software, and environmental considerations • AMD, Intel, Intersil, Hughes, RCA, Rockwell, Teledyne • Progress in standardization
4. SYSTEM DESIGN CONSIDERATIONS
  - Flexibility, maintainability, mobility, reliability (MTBF)
  - Development time and cost • Software vs. hardware cost
5. SOFTWARE DEVELOPMENT OF A MICROPROCESSOR SYSTEM
  - Design cycle (why it differs for microprocessors) • Software development aids • High level vs. assembly language
6. APPLICATIONS OF MICROPROCESSORS
  - Avionics • Communications • Shipboard systems
7. ADVANCED SYSTEM CONFIGURATIONS

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U.S. & Canada	\$395
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Lectures, Course Notes (see below), reference materials, completion certificate, hardware demonstrations, luncheons and coffee breaks.

### U.S. and Canadian Course Locations:

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SAN DIEGO	November 2-3
MONTREAL	November 23-24
LOS ANGELES	December 7-8

### European Course Locations:

WEISBADEN, WEST GERMANY (at the time of the Military Electronics Exposition)	October 5-6
PARIS, FRANCE	October 19-20

### Note: BIT-SLICE MICROPROCESSORS, PLA's and MICROPROGRAMMING (Course 187)

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**COURSE BOOKS** — each bound in a handsome 3-ring binder, includes 300-400 pages of up-to-date ICS course notes illustrated with system and circuit diagrams, flow charts, code, etc. . . and other vital "know-how" to save WEEKS of research and more WEEKS by avoiding making false steps in microcomputer-based system design and development.

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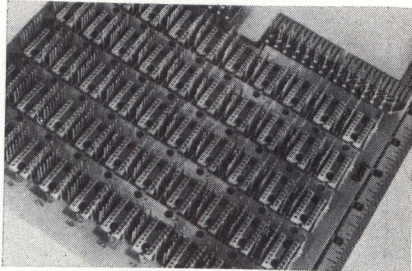
### ICS EUROPE

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1040 Brussels, Belgium  
Telephone: (02) 735 60 03  
Telex: 62473



## PRODUCTS

### IC PLUGGABLE PACKAGING ASSEMBLY



Compatibility of assemblies with DEC PDP-8 and -11 minicomputers is made possible by space-saving "single-sided" construction of the panels, in which both wire-wrappable pins and sockets are on the same side. Panels permit center-to-center spacing as close as 0.500", and each 16-position IC socket is provided with individual 0.025" square wirewrappable terminals, long enough to permit 2- or 3-level top-side solderless wiring. **Garry Manufacturing Co.**, 1010 Jersey Ave, New Brunswick, NJ 08902.  
Circle 245 on Inquiry Card

### 9600-BIT/s DATA SET

The 9601 solid-state LSI data set has 9600-, 7200-, and 4800-bit/s operation, RS-232-C, CCITT V24 interfaces, and operation over basic 3002 lines. Features include constant monitoring by data lamp, marginal circuit and line signal detector indicators, local and remote testing, and voice capability for communication with remote operator. Configuration flexibility is provided by strap options, switch-selectable bit rates, and optional 2- or 4-port multiplexer. **General DataComm Industries Inc.**, 131 Danbury Rd, Wilton, CT 06897.  
Circle 246 on Inquiry Card

### DC/DC CONVERTER POWER SUPPLIES

RA series is pin, package, and performance compatible with equivalent units. With operating efficiencies of 50 to 65% at full load, each model contains high performance pi input filter which reduces input reflected ripple to 1% (max) of the input voltage, minimizing "chopper spike" contamination of the input voltage source. Output ripple and noise are 1 mV rms max and 30 mV pk-pk typ. Line and load regulation for single output models are 0.05 and 0.1%, respectively; dual output models are regulated to within 0.05%, line and load. **Semiconductor Circuits, Inc.**, 306 River St, Haverhill, MA 01830.  
Circle 247 on Inquiry Card

### WIDE ANGLE STATUS/FAULT INDICATOR

Red, solid-state indicator with wide viewing angle from both top and front is designed for operation on low power with long life, shock resistance, and reliability. Series 6310 has consistent visibility from all angles for PC board, back panel, circuit fault, and DIP switch status indication. The 5.0-V, 16-mA device, available with built-in current limiting resistor, features 0.300" pin spacing that is compatible with std DIP pin spacing. Tinned plated copper leads and 0.100" mounting centers are featured. **Chicago Miniature Lamp Works**, 4433 N Ravenswood Ave, Chicago, IL 60640.  
Circle 248 on Inquiry Card

### FLOPPY DISC SYSTEM

Floppy disc system which consists of a controller, interface, and up to four IBM 3740 compatible disc drives is available for use with the PDS-4 interactive computer graphics system. Minimum system requirements are 12K to 16K core memory and a 2-drive floppy system. Developed applications can be executed on a single drive system. Compatibility with IBM 3740 hardware allows media transfer. Applications software can be written to provide data format and program compatibility. **IMLAC Corp.**, 150 A St, Needham, MA 02194.  
Circle 249 on Inquiry Card

## Miniature Toggle Switches



U. L. listed at 5 amps resistive 120VAC, these toggle switches are miniature in size, but big in quality and long life. Many combinations of circuits, actuators and terminals, available from stock. Panel or printed circuit mounting make for easy installation where speed, size and cost are at a premium.  
Sample switches will be provided on request.

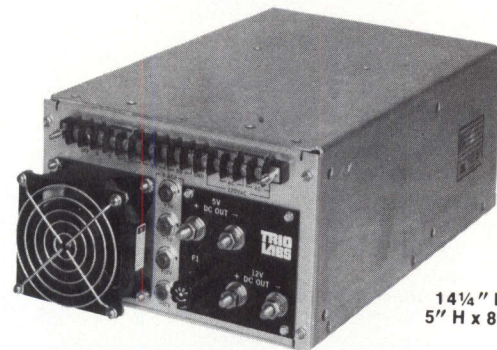
### FREE CATALOG

See the complete line of Rocker Switches in our informative 24 page, 2 color catalog which includes photos, line drawings, specifications and ordering information on over 250 different switches.

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Trio Labs Model 674/675 Multi-Output Switching Regulator Power Supplies will provide all your MPU power needs in only box for less cost than you could do it yourself!



Up to 4 outputs—475 watts. A main 2 or 5 VDC @ 50 or 70 amps for your logic. A second rail @ up to 10 amps to power your memory. And two outputs @ up to 4 amps for your accessories.

Internal Cooling—Overvoltage, Overtemperature and Overload Protection—Remote Sense—Independent V adj.—U.L. rec.—are just some of the features of Trios Model 674-675.

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Winners deserve each other. — Call or write:

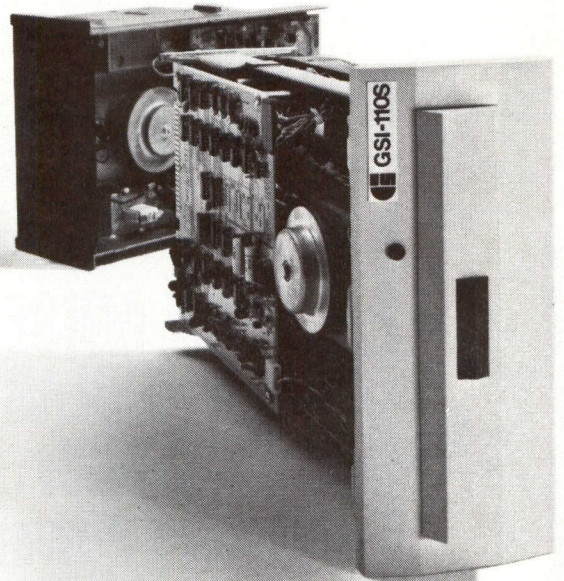
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# The number 1 Floppy Disk Drive in America can be replaced.



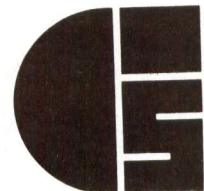
The new GSI-110S Flexible Disk Drive is functionally compatible with the Shugart SA800 and SA900 drives. Use the GSI-110S as a replacement or a second source unit.

Why buy the GSI drive? Because it offers more. While maintaining compatibility, the GSI-110S is faster—6 ms track to track versus 10 ms. A total reliability "anti-crunch" feature assures media protection. The 110S cut-away casting increases air-flow and dissipates heat, thereby increasing reliability. And, best of all, the GSI-110S costs less.

Right now, in diagnostic program loaders, phototypesetting systems, terminals and calculators

throughout the world, America's number 1 selling floppy disk drive is being second sourced or replaced with the GSI-110S. May we show it to you?

**General Systems International, Inc.**, 1440 Allec Street, Anaheim, CA 92805 / (714) 956-7183.

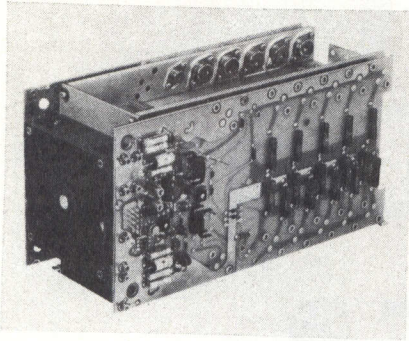


CIRCLE 75 ON INQUIRY CARD



## PRODUCTS

### CRT DEFLECTION AMPLIFIER



Capable of momentarily providing a yoke voltage up to  $\pm 90$  V in the standard power-on demand configuration for high slewing rates, the Mark I magnetic X & Y deflection amplifier ensures that only power necessary for rapid and accurate beam control is used. Current capacities up to 20 A pk-pk are provided to handle wide deflection CRT requirements. Only unregulated low voltage power supplies are required to support this performance capability. **CPS, Inc.**, 722 E Evelyn Ave, Sunnyvale, CA 94086.

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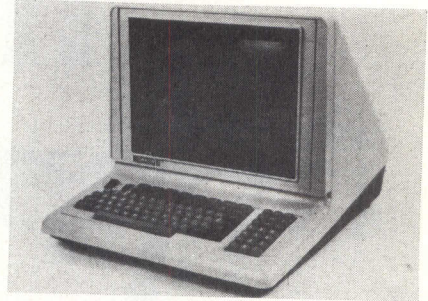
### HIGH EFFICIENCY SWITCHING POWER SUPPLIES



Designed to meet UL478, JP series supplies include ratings of 2 V at 100 A, 5 V at 100 A, 6 V at 100 A, 12 V at 43 A, 15 V at 35 A, and 24 V at 23 A. All models operate from an input of 90 to 132 or 180 to 264 Vac, 48 to 63 Hz, single phase. Output is floating; either positive or negative output terminal may be grounded. Overload, overvoltage, and reverse voltage, and thermal protection is inherent. Devices are housed in a 5 x 7 x 15" case and weigh <20 lb. **ACDC Electronics Inc.**, 401 Jones Rd, Oceanside, CA 92054.

Circle 251 on Inquiry Card

### INTELLIGENT TERMINAL



The 8030 display terminal is a firmware programmed CRT with communications speeds to 9600 baud, which permits user programming of communications functions from the terminal keyboard. Without terminal adjustments, the operator can set up communications speed, parity, bits per word, and stop/start bits. End-of-block terminating character is also user-programmable. A 2-page refresh memory, a total of 3840 char, permits the operator to scroll through both pages of stored display data and edit before transmission of data. **Omron Corp of America, Information Products Div.**, 432 Toyama Dr, Sunnyvale, CA 94086.

Circle 252 on Inquiry Card

## LOW NOISE MODULAR DESIGN

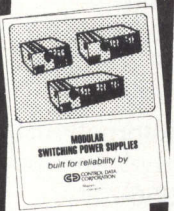
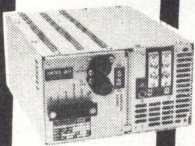
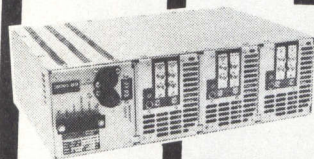
## Switching Power Supplies!

A new line of compact, modular-design switchers that simplify design for 300-600 watt applications and sell for less than 90¢ per watt! End users benefit from low EMI noise levels and highly reliable operation plus easy add-on and maintenance features. Get everything you need to know to evaluate this high quality, money-saving line from:

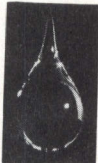
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**GD CONTROL DATA CORPORATION**

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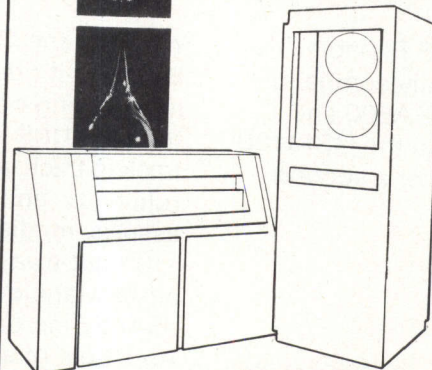


The old Chinese Water Torture. Slow, but effective.

The exact same effect in the computer room means DOWNTIME... frustration for you... due to water, humidity and temperature. EWA is an early warning system that alerts you when these conditions appear in excess of the designed limits of your equipment.

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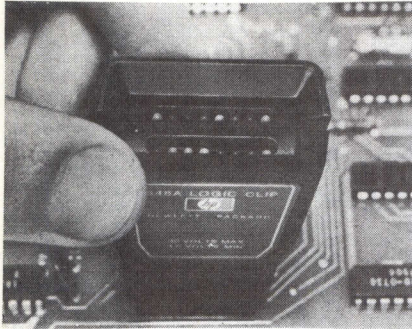


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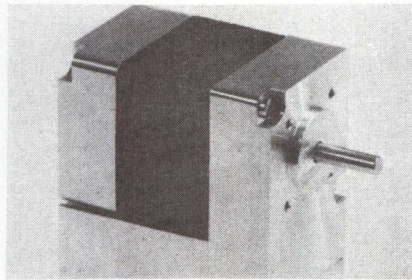
### MULTIFAMILY LOGIC CLIP



Model 548A clips onto a 16-pin DIP IC and provides a LED display of the logic state of each IC pin simultaneously. It is automatic for all logic families from 4 to 18 Vdc, which includes TTL, DTL, RTL, CMOS, and HTL; 3-V CMOS is tested by connecting a 4.5-V supply to an auxiliary power pin. With internal, self-seeking logic circuitry, the clip locates supply and ground pins automatically. Total current drawn is <math><40\text{ mA}</math> with 15 LEDs on. Input current is <math><15\ \mu\text{A}</math>. **Hewlett-Packard Co.**, 1501 Page Mill Rd, Palo Alto, CA 94304.

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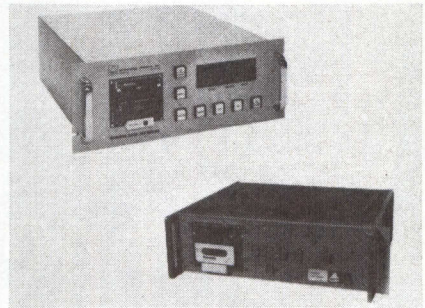
### SERVOMOTOR WITH IC COMMUTATOR



Electronic dc (brushless) type servomotor with IC commutation offers compact design and choice of low or high rotor inertia, as well as a stator winding technique which reduces the size-to-power ratio and increases efficiency. Solid-state commutator with IC can be integral with the motor or connected through a plug-in cable. It has provisions for TTL signal input for motor reversal and tachometer signal output for speed regulation to 1 to 2%. Model 1AD42 has speed of 4000 rpm and stall torque of 7.00 oz-in. **Siemens Corp, Power Engineering Div, Electronic Motors Dept.**, 186 Wood Ave S, Iselin, NJ 08830.

Circle 254 on Inquiry Card

### REMOTE STATION COMMUNICATING DATA SYSTEM



Main functional modules of the 1770 Tele-Measure are cassette recorder, digital clock, modem and telephone interface, and command decoder. Basic terminal accepts 0- to 5-Vdc analog signals from 15 data channels. It scans input channels, formats and codes the signals, and delivers 11-bit serial ASCII and 8-bit parallel RS-232-C data signals to the communications lines. Data can be received automatically by any ASCII-compatible terminal, including teleprinters, typewriter terminals, and CRT devices. **Meteorology Research, Inc.**, Box 637, Altadena, CA 91001.

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It's the new Belden Electronic Catalog. Coming through with on-the-shelf answers to some extraordinary wiring applications. In computers—both digital and analog—instrumentation and controls, data processing, communications. Belden application-engineers wire, cable and cord to fit specific design parameters and environmental conditions. We put most of it up in UNREEL™ to save you time and money. We back it with complete service: Custom designs; information on shielding, jacketing, the codes: Availability; Fast delivery; "Hot Line" engineering assistance (317-966-6681). Let Belden come through for you. Get this catalog today. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374. Phone: 317-966-6661.

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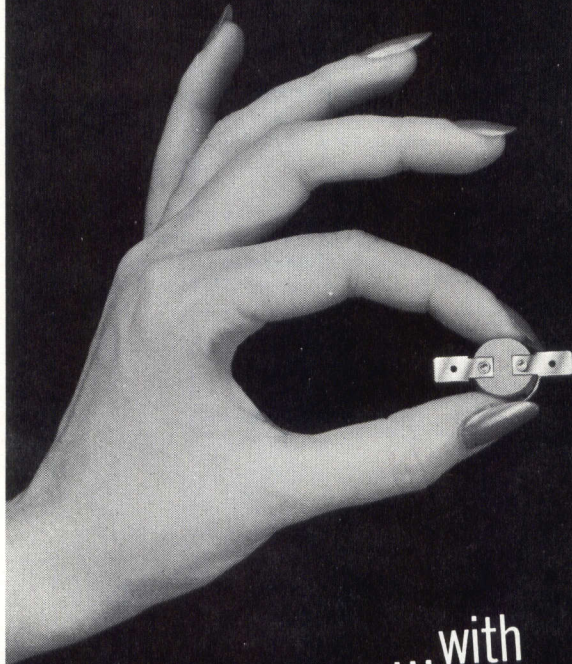
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**BELDEN**



# New Hi-Temp Thermostat



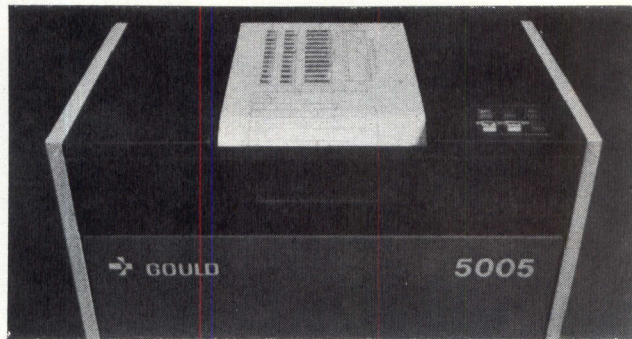
...with  
European Acceptance

Ideal for a variety of high temperature applications! Elmwood's new snap-action RC thermostats include a glass-bonded mica (ceramo-plastic) base that allows set points to 550°F (290°C). The patented metal sleeve insert and rivet construction permit listings by European agencies as well as U.L. and C.S.A. The RC's are SPST, pre-set, tamperproof, and available with mountings, terminals and brackets to suit. Want more? Call or write Elmwood Sensors, Inc., 1659 Elmwood Ave., Cranston, R. I. 02907. Phone 401/781-6500. European Div., Elmwood Sensors Ltd., North Shields, Tyne and Wear, England.

## ELMWOOD SENSORS

## PRODUCTS

### ELECTROSTATIC PRINTER/PLOTTER



High speed 5005 prints 1600 lines/min. (132-char/line) with a 64-char set and plots graphics at a max speed of 3.25 in./s. Resolution is 100 dots/in., overlapped, horizontal and vertical. Key to the image quality is the electrostatic writing system which includes a staggered-stylii writing head, a matrix approach to putting dot charges on paper, and design of the paper. The 11" wide paper is available as 400-ft rolls and 1000-sheet fanfold. Online direct memory access interfaces are available for IBM 360/370, PDP-11, HP 2100, and Nova/Supernova computers. Software includes a PLOT graphics package and specialized application packages. **Gould Inc, Instrument Systems Div**, 3631 Perkins Ave, Cleveland, OH 44114.

Circle 256 on Inquiry Card

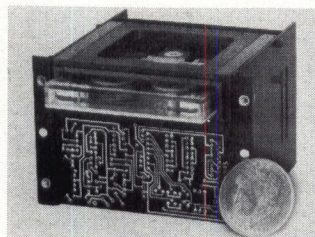
### ROTARY SWITCH

Capable of up to 60 positions, the Communicator features a rotor (patent pending) designed for long term contact registry and integrity. Design features include contacts that pass from electrically dead metal to live metal as they wipe the rotor surface, never touching the laminate; dead and live metal areas on the rotor that are separated by grooves that clean each contact as it passes over them; and PC rotor with an integral cam that functions as the precision detent. Design simplicity eliminates functional backlash from loose rotors and stack-up tolerance problems. Mounting flexibility is provided by small package, four mounting methods, actuation by right-angle drive shaft where necessary, and compatible terminations. **Oak Industries Inc, Switch Div**, Crystal Lake, IL 60014.

Circle 257 on Inquiry Card

### DATA CARTRIDGE TRANSPORT

Micro-Drive model 101 is designed for use as a transport with the 3M DC100A data cartridge, in micro and minicomputer, data terminal, and battery-operated portable systems. Drive unit measures 4½ x 4 x 3", and has a simple cartridge retaining mechanism that assures dependable performance. Features include positive tape motion control for tape handling reliability. Read/write tape speed is 25 in./s; rewind/search speed is 75 in./s. Recording density is 1600 fepi. The unit requires one supply

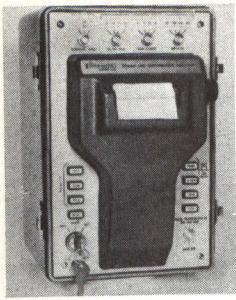


voltage of 15 Vdc at 700-mA avg running current; standby current is 15 mA. Cartridge can store up to 1,340,000 bits and data can be transferred at 20K bits/s. **Instrumentation Technology Corp**, 18333 Eddy St, Northridge, CA 91325.

Circle 258 on Inquiry Card



## POWER LINE DISTURBANCE ANALYZER



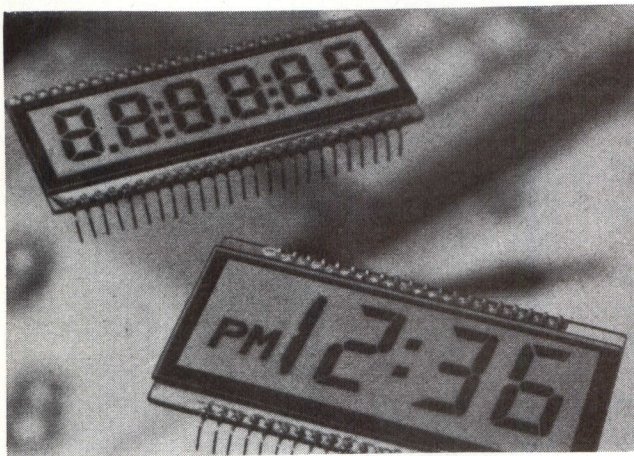
Model 606-101 uses microcomputer and digital measurement technology to analyze, classify, store, and printout disturbance data. Transformer-isolated input networks discriminate among three types of voltage variations as well as line-frequency variations to detect momentary voltage excursions of 0.5- to 100- $\mu$ s duration—impulse; cycle-to-cycle changes in rms voltage levels—surge or sag; slow changes in rms levels (over 10-s periods)—avg + or avg -; and variation in line frequency (monitored

over 1-s sampling periods—freq + or freq -). Internal computer samples all three input channels, converts to digital format, and compares with preset thresholds. When preset value is exceeded, printer provides channel, time, type of disturbance, magnitude, and duration. **Dranetz Engineering Laboratories Inc.**, 2385 S Clinton Ave, South Plainfield, NJ 07080. Circle 259 on Inquiry Card

## 3330-CLASS DISC SUBSYSTEM

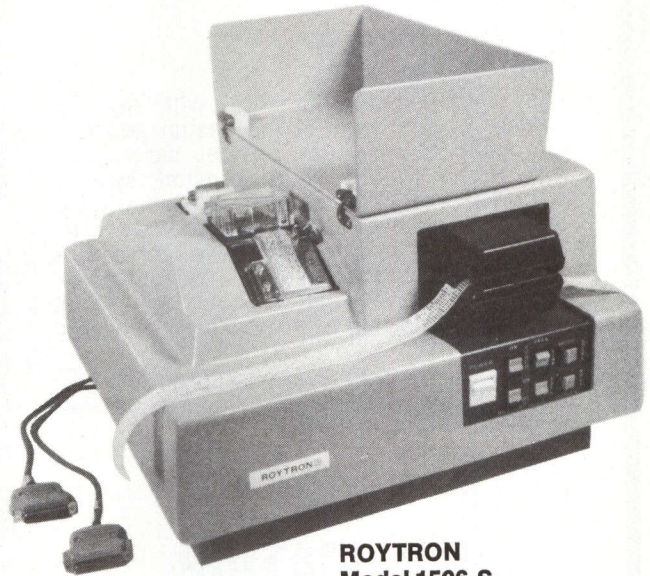
Model 3250A subsystem, for Data General minicomputers, incorporates BD-50 disc which offers 50M bytes of online capacity, with a single-card controller that is fully buffered and able to support up to four drives. Basic drive incorporates a 3330-type spindle interface and a track-following servo system that requires no external reference or reference temperature compensation. The 50M-byte short stack disc packs contain 815 cylinders at 370 tracks/in.; recording densities are 4040 bits/in., 13,440 bytes/track. Controller contains an internal RAM with capacity of 512 words, expandable in 256-word increments to 1024 words for a max of 991 16-bit data words/sector. Disc reads and writes are fully buffered to accommodate high data rates. **Ball Computer Products Inc.**, 860 E Arques Ave, Sunnyvale, CA 94086. Circle 260 on Inquiry Card

## DIL LIQUID CRYSTAL DISPLAYS



Series 3900 field-effect units provide readout for instruments, numeric or clocks. Integrated terminals insert directly into sockets or a PC board eliminating the need for separate connectors. A proprietary "speed enhancer" reduces operating time—particularly in cold temperatures. 3927 is a 3 1/2-digit clock display with 0.7" (17.78 mm) high char, 3918 is a 6-digit display with 0.5" (12.70 mm) char. Both can be read easily without distortion throughout a wide viewing cone. Digits may be black or clear with a choice of transmissive or reflective background. Entire display is protected from humidity by a special coating. Operating voltage is 5-V pk typ; current consumption with all segments on is 150  $\mu$ W; and operating temperature is -5 to 50°C. **Hamlin Inc.**, Lake & Grove Sts, Lake Mills, WI 53551. Circle 261 on Inquiry Card

# a plug for our quiet one



## ROYTRON Model 1506-S Reader/Punch Serial Interface

High speed, compact, with integral electronics power supply and asynchronous serial interface. Self-contained in a quietized housing.

We've just made our popular Model 1560, RS-232C plug compatible. For OEM's who don't want the interface hassle. We added the "S" for Serial and Switching.

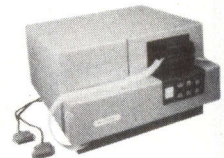
The 1560-S is designed to be connected between a terminal device (keyboard printer or CRT) and its associated modem or data coupler. And to the serial port of most minicomputers and microprocessors.

It satisfies NC, data communications, graphic arts and computer peripheral applications.

The punch accommodates oiled paper, dry paper, metallized mylar, sandwich paper/mylar/paper and polyester . . . 5, 6, 7 or 8-level tapes. It operates at data rates of 50, 75, 110, 134.5, 150, 300 or 600 baud.

The reader is a photoelectric unit with a highly reliable, stepping motor tape transport. It operates at rates of 50, 75, 110, 134.5, 150, 300, 600, 1200 or 2400 baud.

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DIVISION  
Cambridge, Ohio**

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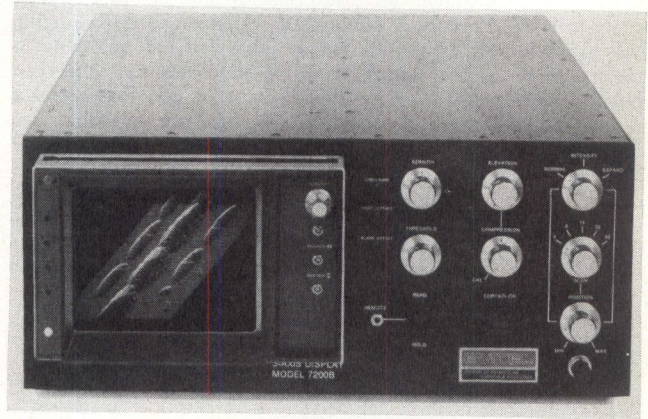
**PRODUCTS**

**TV-DISPLAY SYSTEM**

Two versions of a system for displaying alphanumeric char on a std TV receiver or monitor provide 32 char/line, 16 lines with 2-page capacity (3216) or 64 char/line, 16 lines with 1-page capacity (6416). Both have cursor controls for up/down/left/right/home and parallel address loading. Cursor may be turned off or flashed. On a single 9½ x 9¼" PC board, devices require a single 5-Vdc power supply. Cards are designed to be used with microprocessors and I/O is taken from a 70-pin connector supplied with the unit. Input data are 7-bit parallel and will load at an 80K-bit rate. Carriage return and line feed control characters are decoded and there are six spare codes. Units are available in kit and assembled form. **Interactive Systems**, PO Box 335, Jamison, PA 18929.

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**3-DIMENSIONAL REAL-TIME DISPLAY**



Model 7200B presents frequency, time, and amplitude varying properties of signals and noise in blocks of spectrum space, speeding analysis and understanding of electromagnetic spectra. Features include real-time 3-axis orthographic presentation and moving pictorial views. Geometry of both vertical and horizontal views can be controlled. All axes can be calibrated during geometry variations. Variable time base can be locked to the signal source. Time axis can be expanded and the amplitude axis compressed. Digital control of the threshold level is offered. The unit is 7" high and 21" deep, and weighs 56 lb. Optional equipment includes additional memory, digital interface, larger CRT, video interface, and LED display of scan parameters. **Emtel, Div of Develco**, 404 Tasman Dr, Sunnyvale, CA 94086.

Circle 263 on Inquiry Card

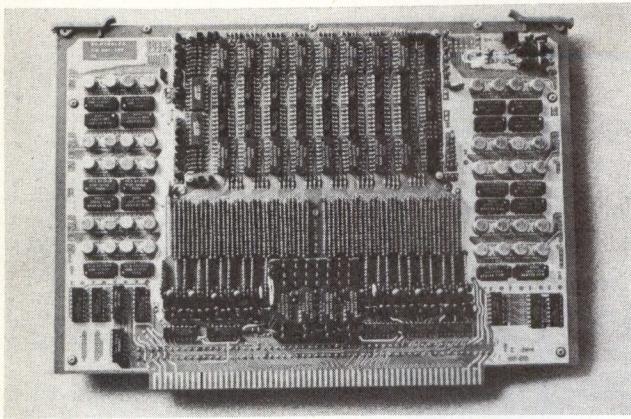
**COMMUNICATION INTERFACES**

Single-line synchronous interface (DMC11), single-line multi-protocol synchronous interface (DUP11), and asynchronous 8- and 16-line multiplexer (DZ11) provide communications related capabilities from computer-to-computer transfers to terminal multiplexing. DMC11 provides high speed links between PDP-11 computers using DDCMP. DDCMP functions are implemented using a microprocessor in the interface, permitting 56K or 1M bit/s operation over coaxial cable between computers in the same facility. DUP11 is capable of handling bit-stuffing protocols such as SDLC and HDLC, and will handle DDCMP as well as BISYNC, operating with synchronous modems at 9600 bits/s. DZ11 interfaces 8 or 16 local or remote asynchronous terminals or modems to PDP-11 computers. Both EIA and 20-mA interface versions are available. **Digital Equipment Corp**, Maynard, MA 01754.

Circle 264 on Inquiry Card



## ELECTRICALLY ALTERABLE CORE ROM



For standalone control systems where severe environments, high electrical noise, and power outage are normal, model CM203 is a complete nonvolatile 4K-byte memory that is fully compatible with a variety of microprocessor bus structures. Conventional ferrite cores are operated in an NDRO (non-destructive readout) mode. Data may be selectively read and written at any random address without affecting data stored at other locations; thus the device functions as a true nonvolatile RAM. Portions of the system may be write disabled by a simple switch control, allowing a powerful RAM/ROM mix that may be varied by the user. Cycle time is 1  $\mu$ s read or write (10- $\mu$ s delay between write and read). Access time is 350 ns, latched and stable at the output port. Power requirements are 5 V  $\pm$ 5%, 2 A max; 12 V  $\pm$ 2%, 1 A max; and -12 V  $\pm$ 2%, 250 mA. **Controlex Corp**, 16005 Sherman Way, Van Nuys, CA 91406.

Circle 265 on Inquiry Card

## 4K MEMORY MODULE

With max access time of 60 ns, bipolar memory module contains 4096 words of 18 bits and memory-select circuitry for operation on 512-word boundaries. Each module has a dedicated I/O bus, and each bit may be independently write-masked. Nine low-order address bits select words within a 512-word block; eight select lines provide access to any one block. After a location is selected and a write signal is issued, any combination of bits may be selected. The device measures 6 x 7 $\frac{1}{2}$ " and can be stacked on  $\frac{1}{2}$ " centers. Control module provides for buffering, timing, and selection of required signals. Input data lines and low order addresses are buffered to meet system fan-in requirements. Control module also generates timing for write control signal and for each write-enable bit. **Nanodata Corp**, 2457 Wehrle Dr, Williamsville, NY 14221.

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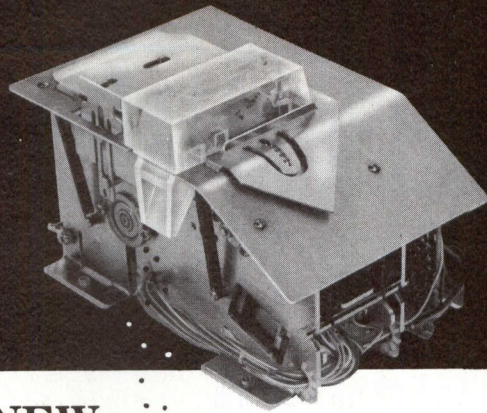
## SYSTEM/3-COMPATIBLE LINE PRINTER



Compatible with System/3 models 8, 10, 12, and 15, the /550 prints at 550 lines/min., and is field-upgradeable to a 750-line/min. rating. Using chain-train printing mechanism, the unit is fully buffered to enable the CPU to continue processing between line settings for increased throughput. Features include paper low, paper out, and paper runaway sensing devices, plus paper jam and clutch-out indicators. Clutch-out indicator halts the computer when the clutch is not properly

engaged, preventing output loss and the need to rerun the entire program. By using one printing hammer for each of the 132 print positions, the printer operates efficiently and makes up to six quality print copies. Multipart forms from 3 $\frac{1}{2}$  to 19 $\frac{1}{2}$ " wide can be used. **Business Systems Technology, Inc**, 3015 Daimler St, Santa Ana, CA 92705.

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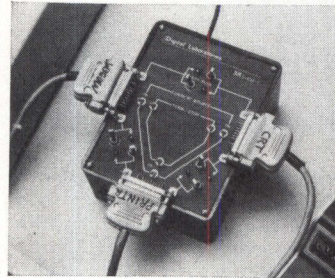
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## PRODUCTS

### UNIVERSAL JUNCTION UNIT

Solving circuit connection problems often encountered when connecting different manufacturer's RS-232-C devices, a compact connection unit, the "3R," permits three devices, such as teleprinters, modems, printing terminals, video displays, and computers, to be combined in a common system. Junction units themselves may be connected together indefinitely, expanding the number of devices that can be combined. Each of the unit's three ports has associated switches that interchange transmit and receive signals, and set up operation in either voltage or current loop mode. Key RS-232-C control lines are acti-



uated to satisfy control conditions required by most terminals. Six additional switches establish any combination of the 63 communication connections that are possible among three I/O devices, and each data path has an associated LED monitor. **Digital Laboratories**, 600 Pleasant St, Watertown, MA 02172. Circle 268 on Inquiry Card

### POCKET-SIZE DIGITAL MULTIMETER



Battery-operated DM-50 uses a push-to-read probe for extended battery life, has full overload protection for all functions, and provides autopolarity and basic auto-zero plus a 3000-count LED display. Ac and dc voltages from 1000 V and down are measured with 1-mV resolution; ac and dc currents from 2A and down with 1- $\mu$ A resolution; and resistance from 3 M $\Omega$  and down, with a 1- $\Omega$  resolution. Basic accuracy is 0.1% plus or minus one digit. Input impedance is 10 M $\Omega$ . Measuring 1.4 x 3 x 5.6" and weighing

10 oz, the multimeter comes with test leads, rechargeable Ni-Cad batteries, and charger/adaptor. Optional are push-to-read and 30-kV high voltage probes. **Innovative Electronics Technology Laboratories, Inc**, 335 Bear Hill Rd, Waltham, MA 02154. Circle 269 on Inquiry Card

### FIELD-PORTABLE RECORDING SYSTEMS

Series SE7000 magnetic-tape systems feature direct-record/reproduce bandwidths up to 1 MHz, with input sensitivity of 0.1 to 2.5 V rms, 20-k $\Omega$  input impedance, 75- $\Omega$  output impedance, and 1-V rms output into 75  $\Omega$ . Units record and reproduce pulse-



code modulated (NRZ L) signals at rates to 1M bit/s, are TTL compatible, and provide link-selectable NRZ L, biphase L, or delay modulation and decoding, and data clock and marker inputs. A phase-locked oscillator, adjustable over a 3:1 range, permits use of any external

clock frequency within the range. Unit measures 25.6 x 16.1 x 15" (65 x 41 x 38 cm) and weighs 95 lb. It is available with built-in power units (interchangeable) for 95 to 130 Vac, 48 to 420 Hz/190 to 250 Vac, 48 to 62 Hz, or 20 to 39 Vdc. **EMI Technology, Inc**, 20 Old Ridgebury Rd, Danbury, CT 06810. Circle 270 on Inquiry Card



# LITERATURE

## MicroNova Family

Brochure includes information on CPU and chip sets, board computers, minicomputers, and development systems, as well as software, support, and applications. **Data General Corp.**, Southboro, Mass.  
Circle 300 on Inquiry Card

## Microprocessor Batteries

Curves, charging circuits, and cell configurations illustrate guide which supplies selection and performance characteristics of rechargeable nickel-cadmium batteries. **General Electric Co.**, Gainesville, Fla.  
Circle 301 on Inquiry Card

## Analog Microcomputer Peripherals

Comparison tables and diagrams provide specs on peripherals for Motorola EXORciser, and Intel Intellec MDS800, SBC80/10, and Intellec 8 systems. **Burr-Brown Research Corp.**, Tucson, Ariz.  
Circle 302 on Inquiry Card

## Synchro-Digital Conversion

Detailed 46-page handbook contains basic terminology, theory, and illustrated applications of synchro-digital and digital-synchro conversions. **Analog Devices, Inc.**, Norwood, Mass.  
Circle 303 on Inquiry Card

## Frequency Counters

Brochure offers general information, technical specs, performance charts, and options of PM 6610 family. **Philips Test & Measuring Instruments, Inc.**, a North American Philips Co., Woodbury, NY.  
Circle 304 on Inquiry Card

## Digital ICs Test Systems

Features of series MSI-400, and listing of MSI and SSI devices tested by computer-controlled systems are furnished in folder. **Datatron, Inc. Test Systems Div.**, Santa Ana, Calif.  
Circle 305 on Inquiry Card

## Acoustic Couplers/Modems/OEM Boards

Catalog provides table of specs and general descriptions which explain applications in time-sharing and message communications environments. **Omnitec Corp.**, Phoenix, Ariz.  
Circle 306 on Inquiry Card

## Communications Network Processor

Aimed at data communications management, publication supplies information, drawings, and tables on family of devices to aid in network design. **Codex Corp.**, Newton, Mass.  
Circle 307 on Inquiry Card

## Illuminated Switches

Specs, application data, and mounting information for the 554 series of computer-grade modular switches are offered in illustrated catalog. **Dialight, a North American Philips Co.**, Brooklyn, NY.  
Circle 308 on Inquiry Card

## Flat Cable

Design guide provides basic data on applications and advantages of systems, as well as information on types of cables and terminations. **Institute of Printed Circuits**, Evanston, Ill.  
Circle 309 on Inquiry Card

## OEM Minicomputer Equipment

Designed as an overview for future buyers, brochure has sections devoted to product descriptions, support, service planning, and purchase agreements. **Hewlett-Packard Co.**, Palo Alto, Calif.  
Circle 310 on Inquiry Card

## Programmable Controllers

Features of the 184 and 384 controllers are furnished in illustrated brochure which explains programming, applications, and electrical and mechanical specs. **Modicon Corp.**, Andover, Mass.  
Circle 311 on Inquiry Card

## RF Capacitors

Complete with tables, diagrams, and graphs, 256-page handbook covers basic circuit design considerations, aids, test data, and applications for capacitors. **American Technical Ceramics**, Huntington Station, NY.  
Circle 312 on Inquiry Card

## Microcomputer System

Specs, selection information for memory and interface boards, and descriptions of software and documentation are furnished in illustrated catalog on the 8080 system. Send \$1 to **IMS Associates, Inc.**, 14860 Wicks Blvd., San Leandro, CA 94577.

## Power Supplies

Brochure points out std features, characteristics, specs, and options of family of brownout-proof switching supplies designed for OEM digital applications. **Pioneer Magnetics, Inc.**, Santa Monica, Calif.  
Circle 313 on Inquiry Card

## Remote Intelligent Multiplexer System

Software, communications facilities and protocols, and interfacing capabilities are detailed in data sheet describing the RIM system. **General Automation, Inc.**, Anaheim, Calif.  
Circle 314 on Inquiry Card

## Terminal Clustering Unit

Describing the CLU-8, its operation, and technical specs, literature includes diagrams illustrating typ system applications in multiple-terminal data communications networks. **Syntech Corp.**, Rockville, Md.  
Circle 315 on Inquiry Card

## LSI Test Systems

Illustrated with photos, tables, and a system block diagram, brochure pinpoints application areas and gives features and specs of MD-501 and MD-501MS multi-user, multi-usage systems. **Macrodata Corp.**, Woodland Hills, Calif.  
Circle 316 on Inquiry Card

## Remote Communications Controller

Functional descriptions, specs, options, and typ applications for the Procom I microprocessor-based controller are specified in technical bulletin. **Computer Products, Inc.**, Fort Lauderdale, Fla.  
Circle 317 on Inquiry Card

## Integrated Circuits

Pamphlet on Monochip custom ICs offers detailed description of components, a pull-out section featuring questions and answers, and 20 design examples. **Interdesign, Inc.**, Sunnyvale, Calif.  
Circle 318 on Inquiry Card

## D-A Converters

Product data sheet presents tables of specs, block diagram, and drawings which illustrate features of series 2470 high speed DACs. **Dynamic Measurements Corp.**, Winchester, Mass.  
Circle 319 on Inquiry Card

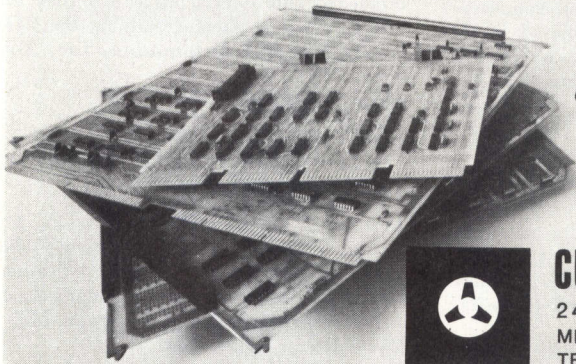


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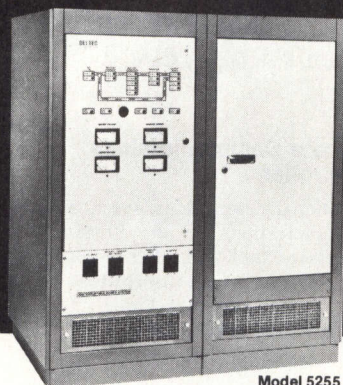
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## LITERATURE

### Data Line Extender

Complete with photo and diagram, bulletin contains general information, technical summary, and ordering information for the 25B/108 data set. **GTE Lenkurt Inc**, San Carlos, Calif.

Circle 320 on Inquiry Card

### Modular Micro Printer System

Brochure on the Mark II system gives descriptions of features, parts interchangeability, and application flexibility, and shows complete selection matrix. **Sheldon Printer Corp**, Anaheim, Calif.

Circle 321 on Inquiry Card

### Coaxial Connectors

Specs of std line of connectors, Golden Crimp series, and Lepra/Con ultraminiature connectors are outlined in revised catalog. **Malco, a Microdot Co**, Montgomeryville, Pa.

Circle 322 on Inquiry Card

### Electrostatic Plotters

Brochure covers applications, general specs and descriptions, detailed plotting specs, model selection, and options of series of 10 plotters. **Versatec, a Xerox Co**, Santa Clara, Calif.

Circle 323 on Inquiry Card

### Memory Systems

Specs and features of the models 696 and 698 core memory systems, 16K words x 18 bits and 32K words x 18 bits respectively, are discussed in brochure. **Fabritek Inc**, Minneapolis, Minn.

Circle 324 on Inquiry Card

### A-D Converters

"Minibrochure" describing the 6100 series of microprocessor-compatible integrating ADCs features specs, outline dimensions, pin connections, and applications. **SGR Corp**, Canton, Mass.

Circle 325 on Inquiry Card

### Stepping Motors and Digital Controls

Brochure includes descriptions, applications, general specs, and dimensions for 4- and 8-phase fine angle motors, as well as for logic drive systems. **USM Corp**, Woburn, Mass.

Circle 326 on Inquiry Card



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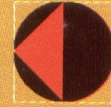


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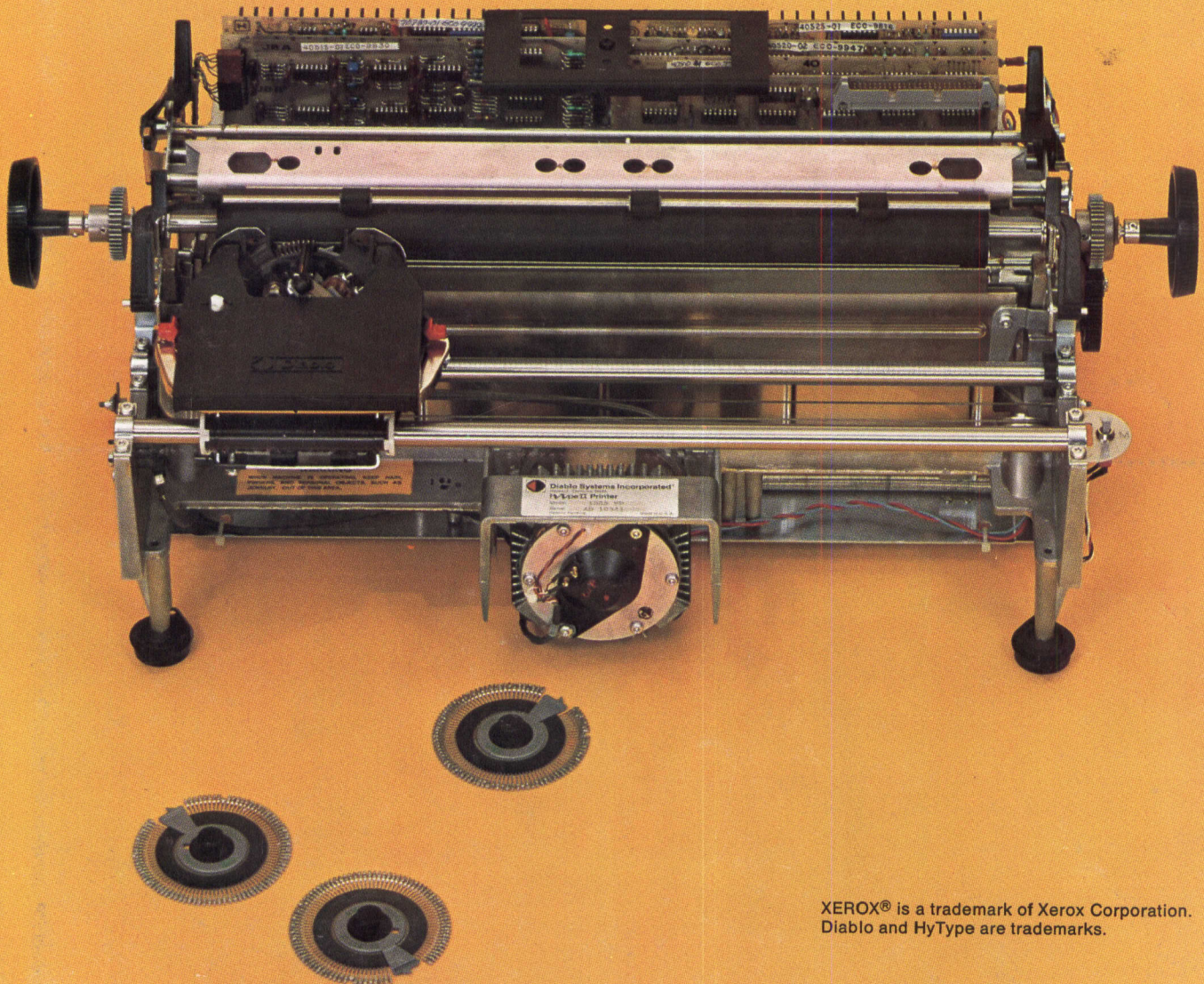
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