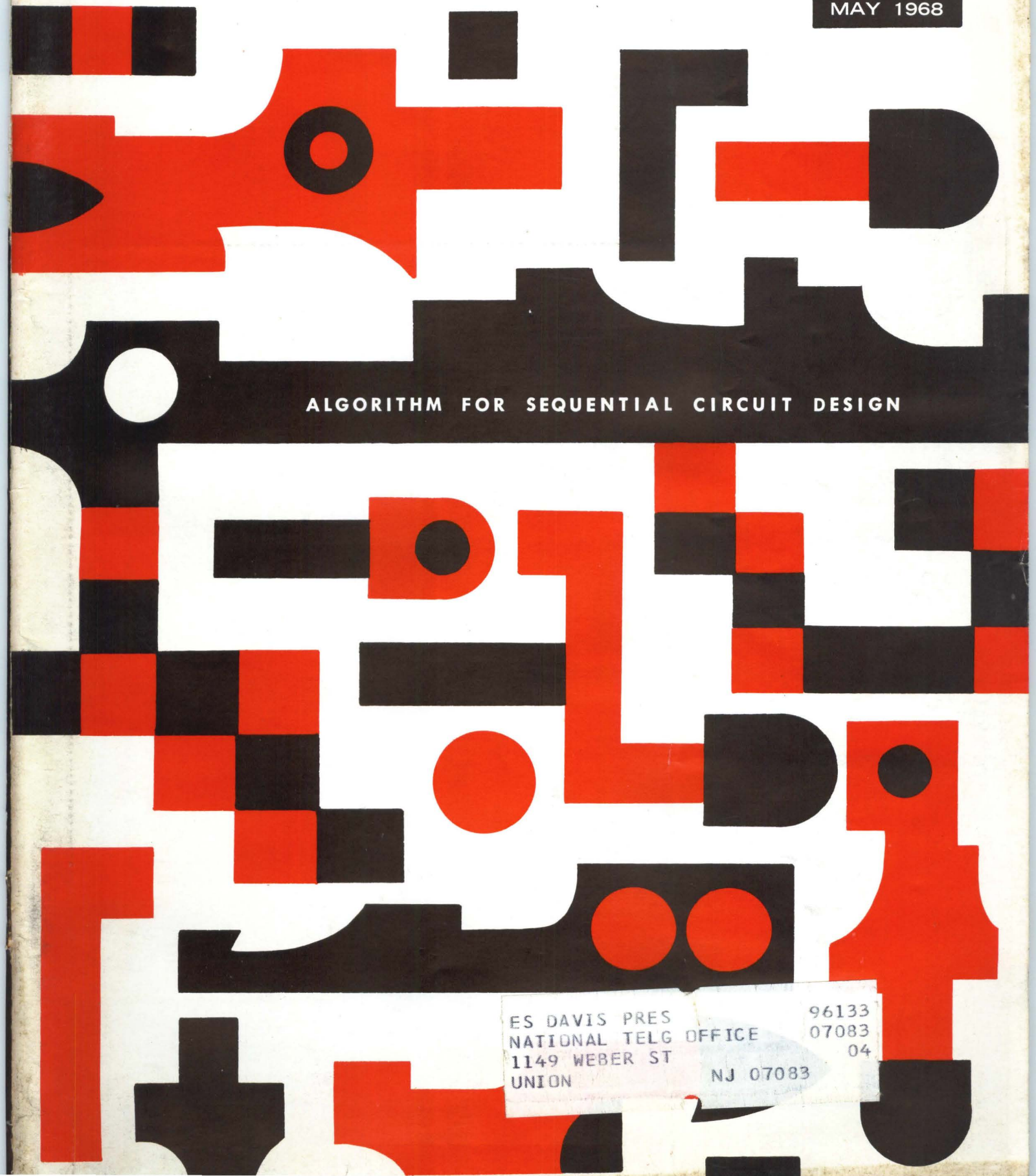
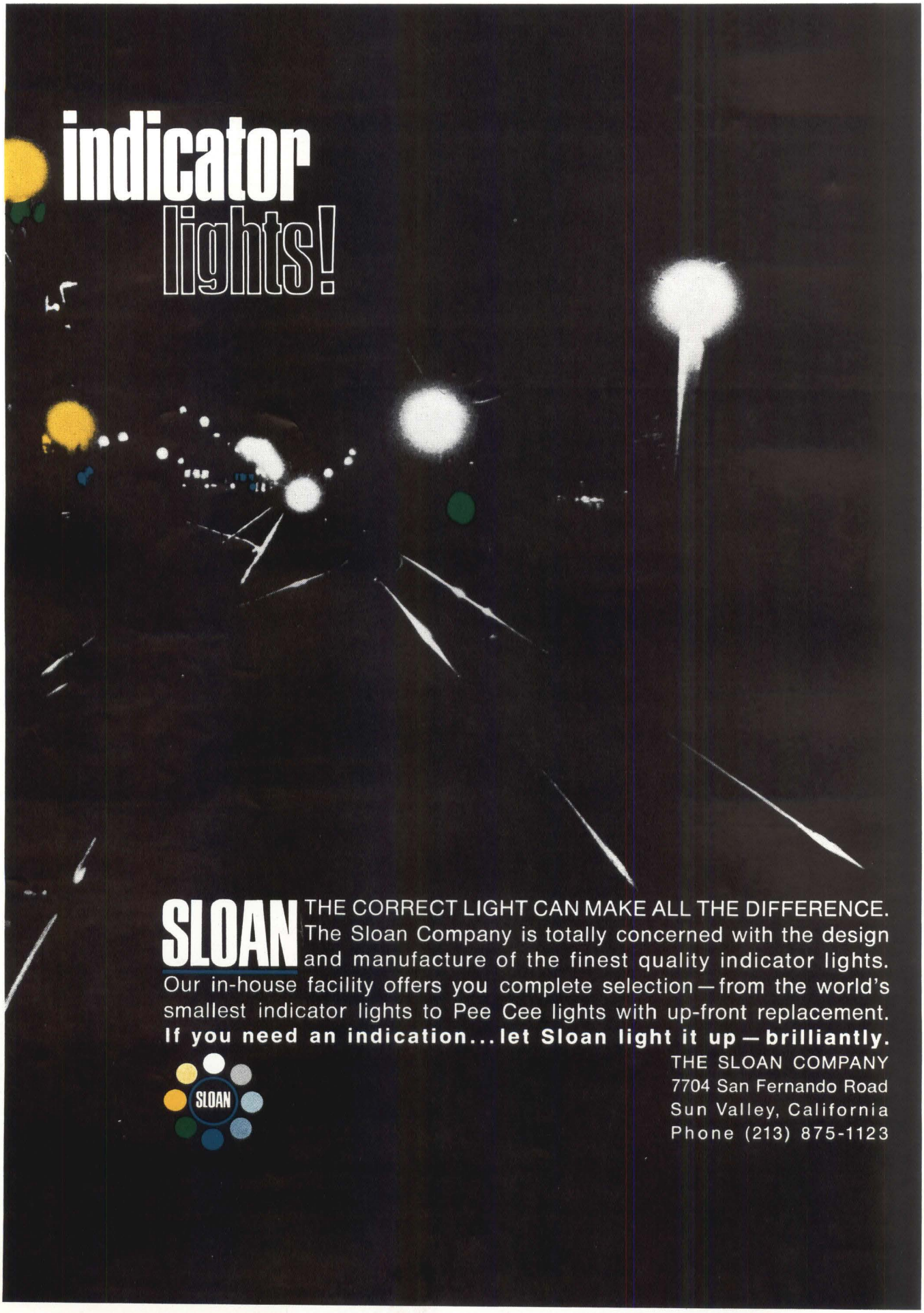
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

MAY 1968



ALGORITHM FOR SEQUENTIAL CIRCUIT DESIGN



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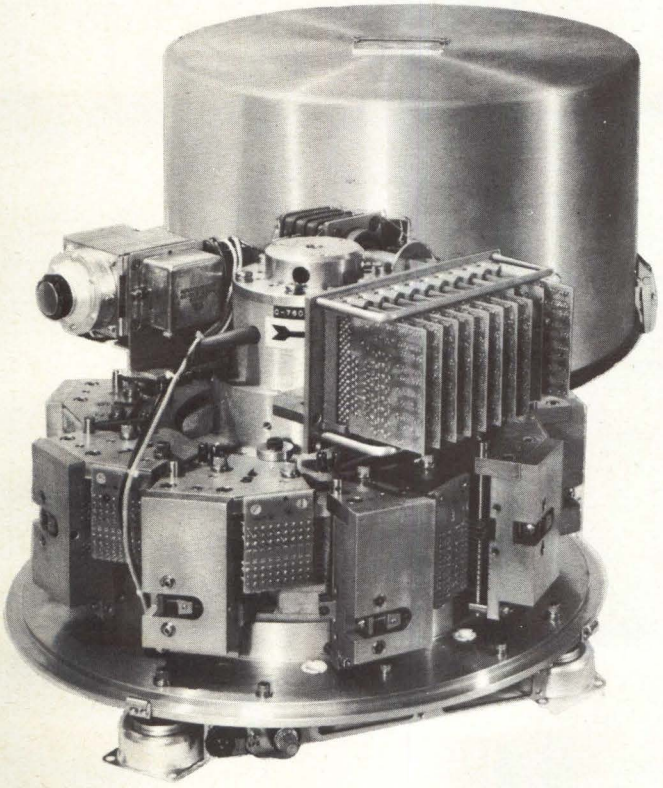

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

Editorial & Executive Offices
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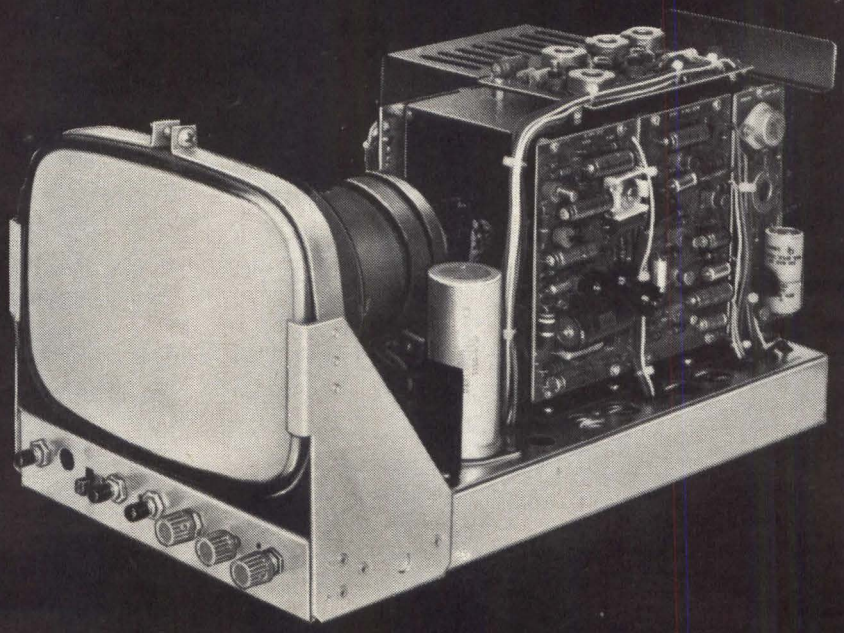
FEATURES

DEPARTMENTS

BBRC/Miratel's *TU Monitor*

SOLID-STATE–AND PROVEN



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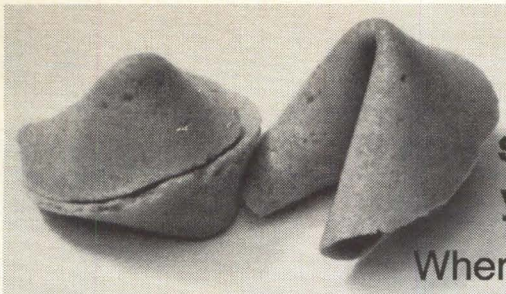

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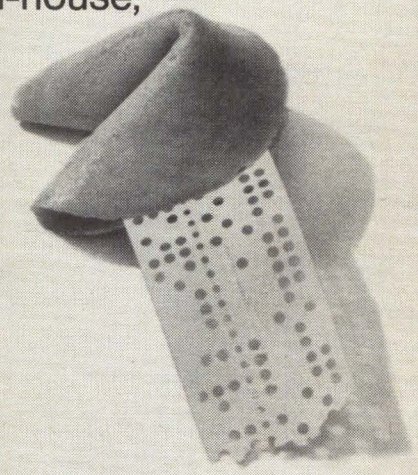

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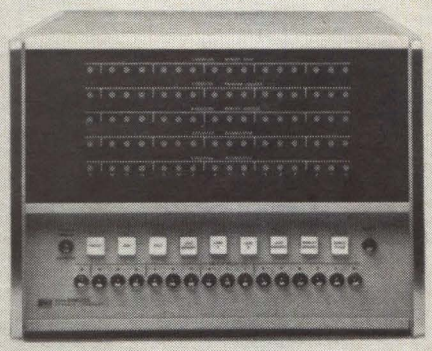

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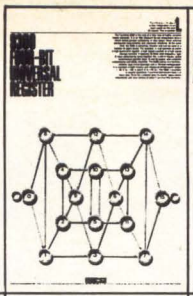
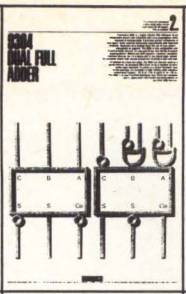
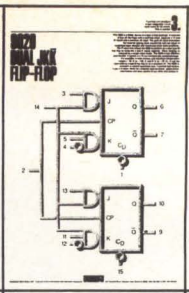
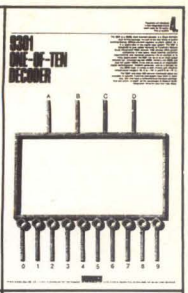
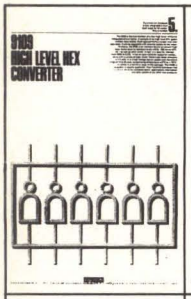
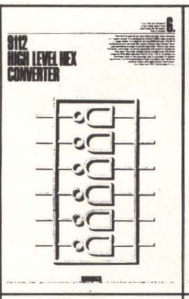
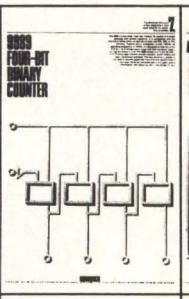
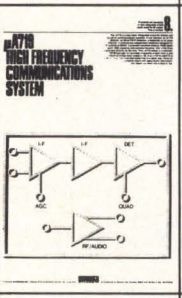
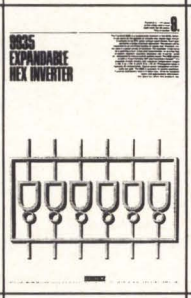
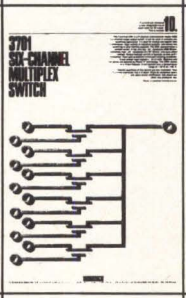
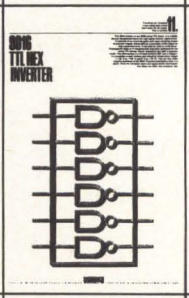
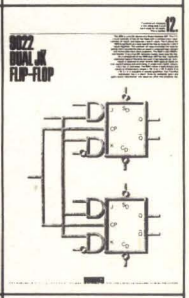
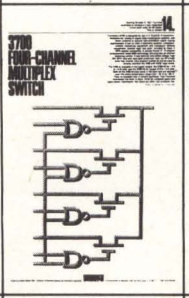
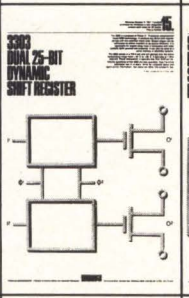
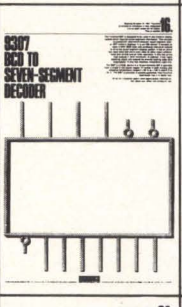
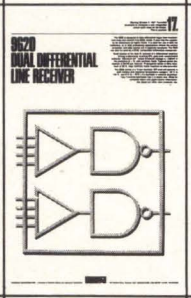
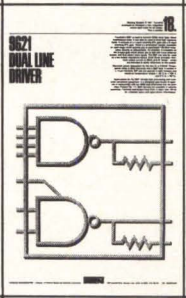
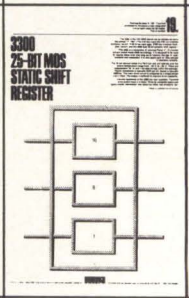
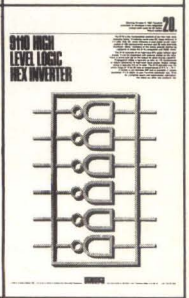
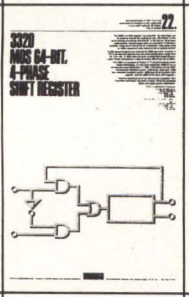
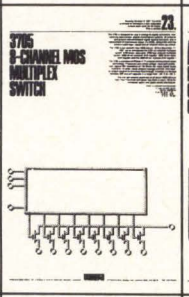
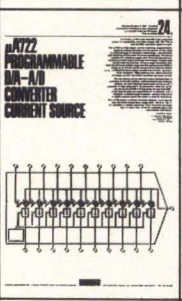
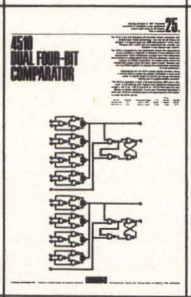
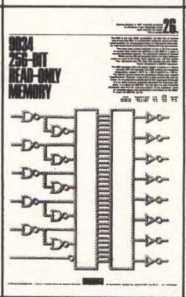
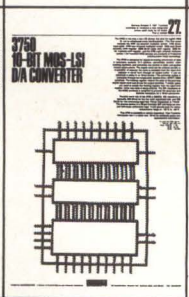
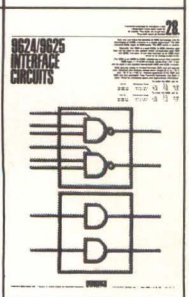
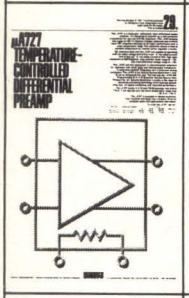
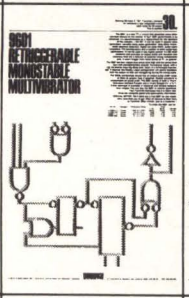
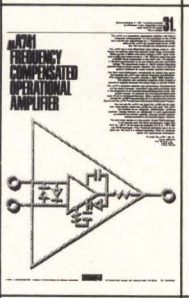
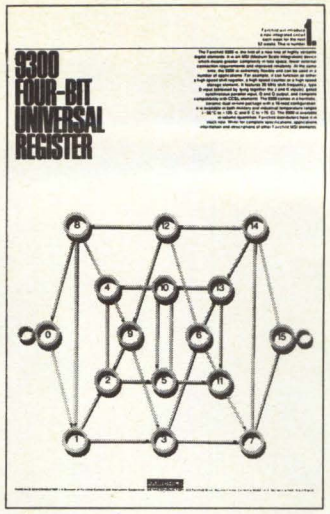
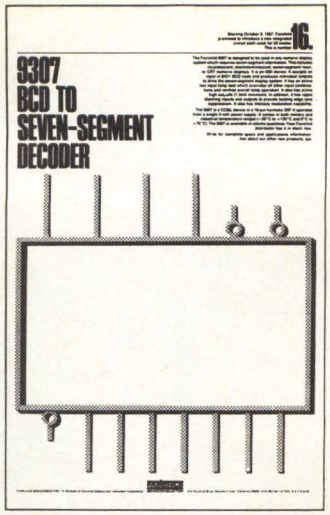
 1. 9300 FOUR-BIT UNIVERSAL SHIFT REGISTER	 2. 9304 DUAL FULL ADDER	 3. 9020 DUAL J-K FLIP-FLOP	 4. 9301 ONE-OF-TEN DECODER				
 5. 9309 HIGH LEVEL HEX CONVERTER	 6. 9312 HIGH LEVEL HEX CONVERTER	 7. 9099 FOUR-BIT BINARY COUNTER	 8. μA719 VHF/UHF FREQUENCY COMMUNICATIONS SYSTEM	 9. 9035 EXPANDABLE HEX INVERTER	 10. 3701 SIX-CHANNEL MULTIPLEX SWITCH	 11. 9016 TTL HEX INVERTER	 12. 9022 DUAL J-K FLIP-FLOP
 13. 3102 MOS THREE-INPUT GATE	 14. 3708 FOUR-CHANNEL MULTIPLEX SWITCH	 15. 3305 DUAL 25-BIT DYNAMIC SHIFT REGISTER	 16. 9307 BCD TO SEVEN-SEGMENT DECODER	 17. 9620 DUAL DIFFERENTIAL LINE RECEIVER	 18. 9621 DUAL LINE DRIVER	 19. 3300 25-BIT MOS STATIC SHIFT REGISTER	 20. 9100 HIGH LEVEL LOGIC HEX INVERTER
 21. 4500 BIPOLAR MICROMATRIX® ARRAY	 22. 3220 MOS 64-BIT, 4-PHASE SHIFT REGISTER	 23. 3705 8-CHANNEL MOS MULTIPLEX SWITCH	 24. μA722 PROGRAMMABLE D/A-A/D CONVERTER CURRENT SOURCE	 25. 4510 DUAL FOUR-BIT COMPARATOR	 26. 9034 256-BIT, READ-ONLY MEMORY	 27. 3758 10-BIT MOS-LSI D/A CONVERTER	 28. 9624/9625 INTERFACE CIRCUITS
 29. μA727 TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMP	 30. 9601 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR	 31. μA761 FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER	May 13, 1968	May 20, 1968	May 27, 1968	June 3, 1968	June 10, 1968
June 17, 1968	June 24, 1968	July 1, 1968	July 8, 1968	July 15, 1968	July 22, 1968	July 29, 1968	August 5, 1968
August 12, 1968	August 19, 1968	August 26, 1968	September 2, 1968	September 9, 1968	September 16, 1968	September 23, 1968	September 30, 1968

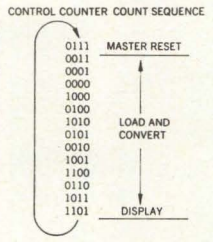
More about:





BINARY TO DECIMAL 7-SEGMENT DISPLAY CONVERTER.

Put new products #1 and #16 together, and you've got the basis of a whole new subsystem. Using five 9300s and four 9307s, combined with a variety of four other Fairchild components (19 packages in all), you can build a subsystem that would normally require 60 discrete integrated circuit packages. (Each 9300 replaces six IC packages and each 9307 replaces five IC packages.)

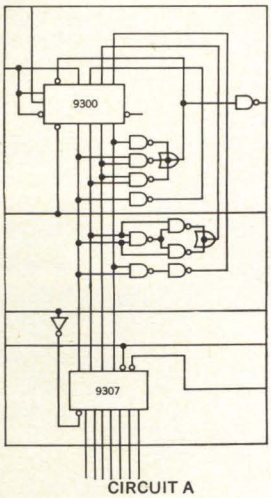


This application demonstrates the excellent interfacing compatibility of CCSL circuitry. It allows you to combine the best features of each circuit family: MSI for complexity and economy, DTμL for wire-OR and lower power applications, and TTμL for speed and line driving.

The 9300 and 9307 are MSI. Like the rest of the family, they're designed to work as basic building blocks in any digital logic system. They work together with a minimum of interface circuitry.

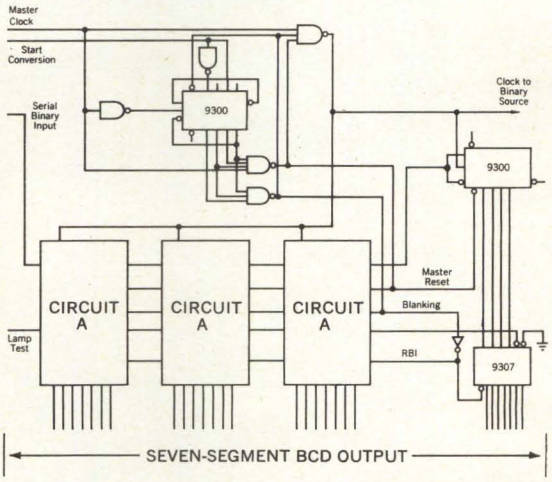
The new subsystem converts a 12-bit binary number (in serial form) to the individual outputs required to drive four 7-segment numeric displays. These could include incandescent, electroluminescent, 7-segment neons or CRT numeric displays.

The conversion takes place in two steps: (1) conversion of the 12-bit binary number to parallel BCD code and (2) conversion of the BCD to outputs necessary to drive the 7-segment displays.



CIRCUIT A

The logic diagram and control counter count sequence illustrates how the conversion takes place. When the START conversion goes high, the 9300 control counter transfers from the 1101 state to the 0111 state (the display outputs, that is, the 9307 decoders, are enabled only in the 1101 state, thus they become disabled and remain so during the entire conversion process). In the 0111 state, the four 9300 shift registers containing the results of the last conversion are cleared to zeros. After the 0111 state is reached, the clock signal is enabled both to the binary source and to the conversion registers until twelve clock pulses have occurred. After twelve clock pulses, the 1101 state is again entered, at which time the display decoders are enabled to display the results of the conversion, and the clock pulse to the conversion logic and binary source is disabled. The 9300 control counter shifts to the parallel enable mode when the 1101 state is reached, and will remain there until the START conversion goes high again.



PARTS LIST
3 . . . . . 9936 DTμL Hex Inverters
5 . . . . . 9946 DTμL Quad Two-Input Nands
1 . . . . . 9009 TTμL Power Driver
1 . . . . . 9003 TTμL Triple Three-Input Gate
5 . . . . . 9300 MSI Universal Shift Registers
4 . . . . . 9307 MSI Seven-Segment Decoders

Conversion from the serial binary input to parallel 8421-BCD occurs in the following way: After each bit is shifted into the conversion register (most significant bit first), the numeric contents of every 4-bit register (except the last) are examined. If a register contains a value of 5 or greater, the mode of the register is converted to parallel enable. On the next clock, 3 is added to the present contents of the register and the results are shifted one place.

For complete specs and other application information, circle Reader Service Numbers 101 and 116. If you have an immediate application requirement, call your local Fairchild distributor now.

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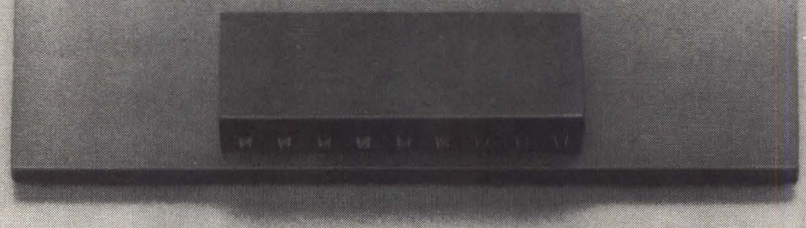
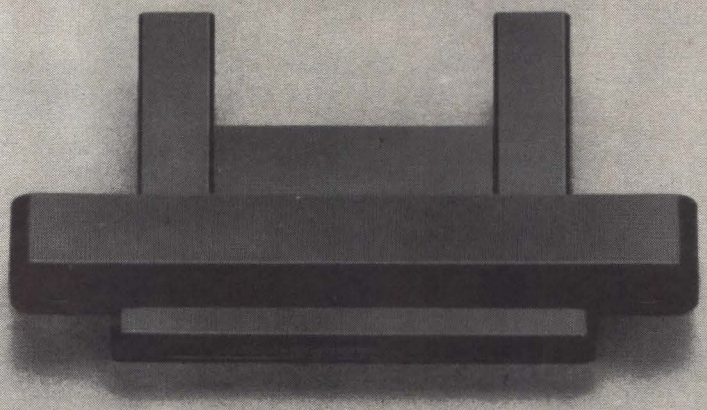
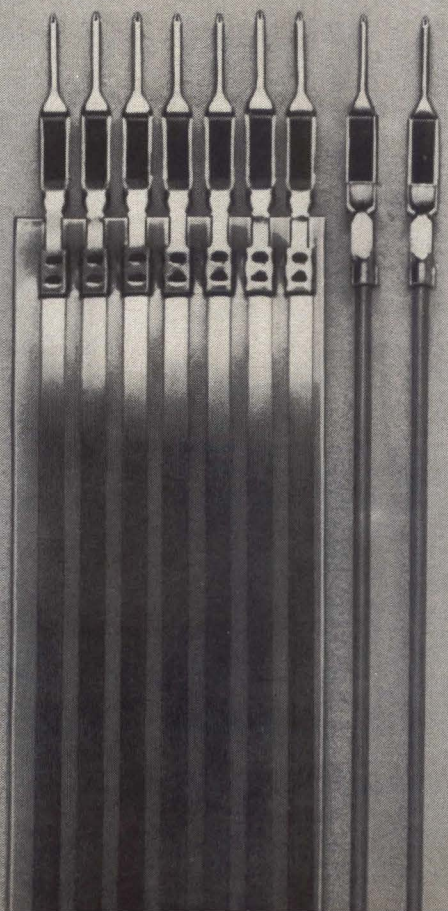
Put an end to flat cable. Just crimp.







No stripping
or plating.
No welding
or soldering.
Just crimp and snap in.
Cable to cable,
cable to board,
cable to wire.
Mix flat cable
and round wire.
Practical, low cost, easy.
Maintainable. Reliable.
Available now.
For information
on our flat cable
connector, write

AMP Incorporated,
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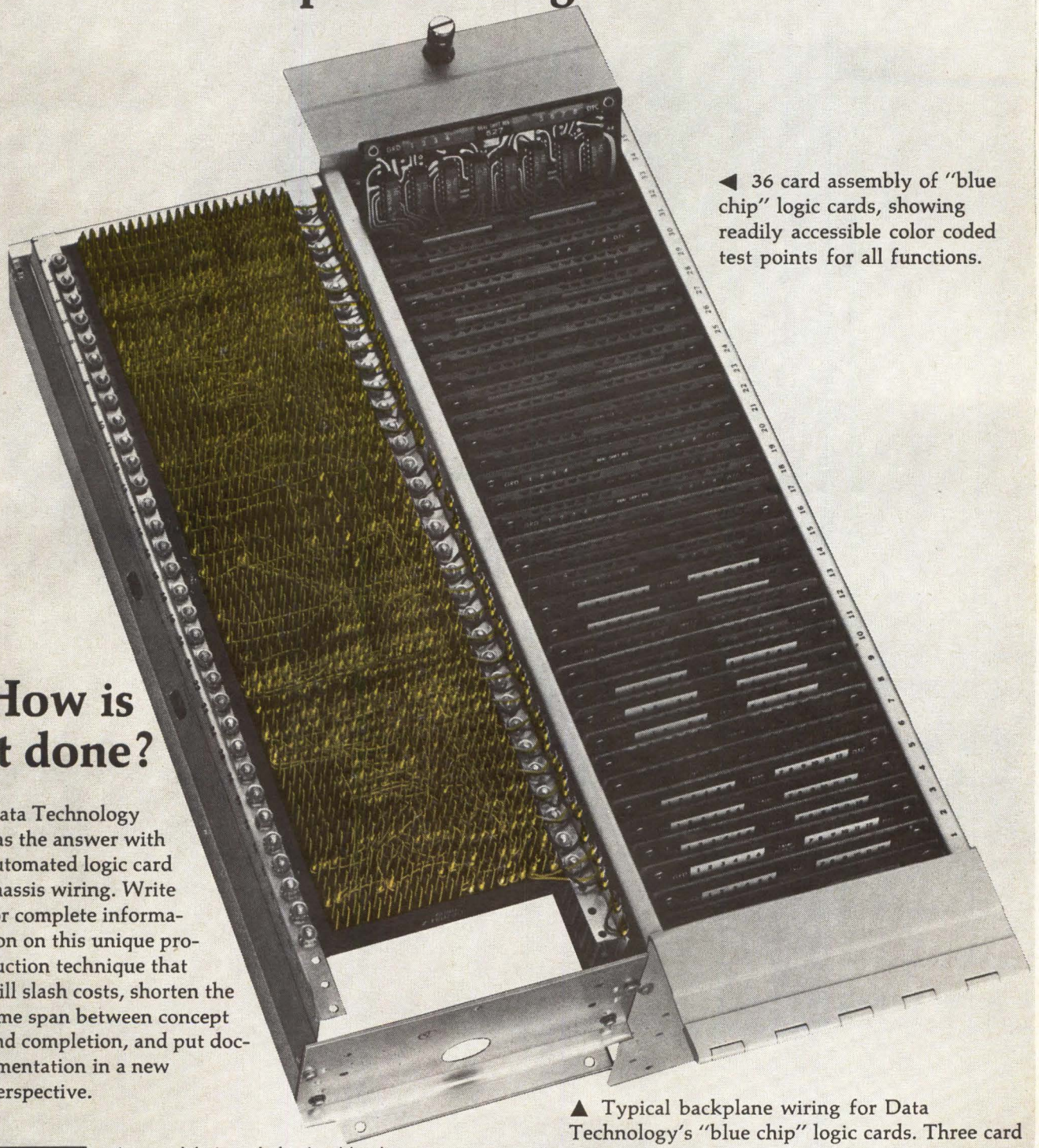
From idea to hardware in 50% less time, at 30% less cost, and with the highest degree of accuracy in the industry!

Completely eliminates heating problems associated with backplane wiring.



◀ 36 card assembly of "blue chip" logic cards, showing readily accessible color coded test points for all functions.

How is it done?

Data Technology has the answer with automated logic card chassis wiring. Write for complete information on this unique production technique that will slash costs, shorten the time span between concept and completion, and put documentation in a new perspective.

▲ Typical backplane wiring for Data Technology's "blue chip" logic cards. Three card cages with up to 2,000 logic functions can be wired in one operation.

Automated logic card chassis wiring is another example of the total service package provided by Data Technology.

Data Technology Corporation, 2370 Charleston Road, Mountain View, California 94040. Phone (415) 964-2600, TWX (910) 379-6476.

CIRCLE NO. 7 ON INQUIRY CARD

← CIRCLE NO. 6 ON INQUIRY CARD

Complex-function integrated circuits give you a new look in system package count ... system costs, too! (MECL II MAKES IT POSSIBLE!)

– where the priceless ingredient is care!

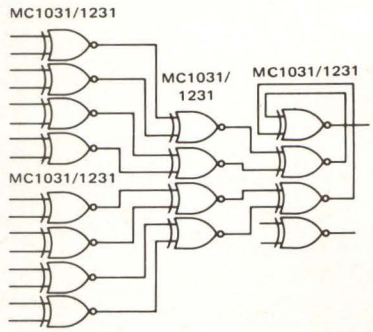
30% SYSTEM COST REDUCTIONS POSSIBLE!

Since we don't know your exact system requirements, we can't predict precisely how much MECL II can reduce your costs. But, our engineers figure that 30% is a *conservative* estimate for most systems! Why? There are three reasons: First, there's the recent reduction in piece-part prices — as much as 65% on some types. Then, we've now introduced several new complex-function types (and, more on the way) to further reduce "can-count." And, of course, there's the complementary output feature of all MECL circuits — to provide superior design flexibility as well as reduced package-count.

It's a great combination!

Further, even the new complex-function circuits are lower in price than other comparable types. For example, the cost-per-gate-element of the MC1030/MC1031 is less than 33 cents! Yet, these Quad 2-Input Exclusive OR and NOR gates will replace up to 12 standard gates and make it possible for you to build a 25 ns, 16-Bit Parity Checker, as shown

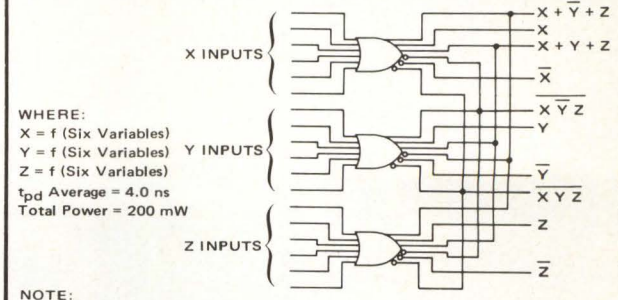
25 ns 16-BIT PARITY CHECKER (Even Parity)



COMPLEMENTARY OUTPUTS REDUCE PACKAGE COUNT

The six-input OR/NOR gates in the MECL II series are extremely useful in generating multiple wired-OR logic functions since six independent outputs are provided, as shown. In addition to lowering system costs by reducing package count, this unique feature reduces delay time and design headaches; plus, it provides almost unlimited flexibility of logic design.

MECL II "WIRED OR" FEATURE



NOTE:
All Outputs That Are Used Require An Internal or External Pulldown Resistor.

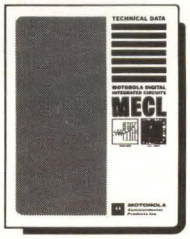
NOW - UP TO 65% LOWER PRICES ON SOME MECL II TYPES!

TYPE NO.	FUNCTION	PRICE 1000-UP	TYPE NO.	FUNCTION	PRICE 1000-UP
MC1001P	Single 6-Input Gate	$1.25	MC1017P	Translator (Sat. Logic to MECL)	$2.75
MC1002P	Single 6-Input Gate	1.25	MC1018P	Translator (MECL to Sat. Logic)	2.75
MC1003P	Single 6-Input Gate	1.25	MC1019P	Full Adder	3.50
MC1004P	Dual 4-Input Gate	1.30			
MC1005P	Dual 4-Input Gate	1.30	MC1020P	Quad Line Receiver	1.25
MC1006P	Dual 4-Input Gate	1.30	MC1021P	Full Subtractor	3.50
MC1007P	Triple 3-Input Gate	1.35	MC1022P	Type D Flip-Flop	3.70
MC1008P	Triple 3-Input Gate	1.35			
MC1009P	Triple 3-Input Gate	1.35	MC1023P	Dual 4-Input Clock Driver (2ns t_{pd})	5.80
MC1010P	Quad 2-Input Gate	1.40	MC1024P	Dual 2-Input Expandable Gate	1.35
MC1011P	Quad 2-Input Gate	1.40	MC1025P	Dual 4- and 5-Input Expander	1.30
MC1012P	Quad 2-Input Gate	1.40	MC1027P	120 MHz AC Coupled J-K FlipFlop	5.80
MC1013P	85 MHz AC Coupled J-K Flip-Flop	2.40	MC1029P	Data Distributor	2.60
MC1014P	Dual R-S Flip-Flop (Pos. Clock)	2.60	MC1030P	Quad 2-Input Exclusive OR Gate	3.95
MC1015P	Dual R-S Flip-Flop (Neg. Clock)	2.60	MC1031P	Quad 2-Input Exclusive NOR Gate	3.95
MC1016P	Dual R-S Flip-Flop (Single Rail)	2.60	MC1033P	Dual R-S Flip-Flop (Neg. Clock)	2.60

OTHER COMPLEX FUNCTIONS TO BE ANNOUNCED SOON:

16-Bit Coincident Memory
100 MHz Decade Counter
180 MHz Type "D" Flip-Flop
Transmission Line Driver
Dual Schmitt Trigger

New MECL Data Brochure provides "how-to-use" information plus complete specifications, for the World's Fastest, Most Advanced I/C Logic Line . . . 80-pages of pertinent applications information, complete data for 58 MECL II devices (30 circuits) and a general information section that includes a full explanation of the emitter coupled logic design approach. It's yours for the asking! Simply write on your company letterhead to: P.O. Box 955, Phoenix, Arizona 85001.



Most MECL II circuits also available in ceramic flat pack (TO-86) for −55° to +125°C operation.

MOTOROLA *Semiconductor Products Inc.*

CIRCLE NO. 8 ON INQUIRY CARD

regnecentralen

knows that missed bits can mean missed Kröner.

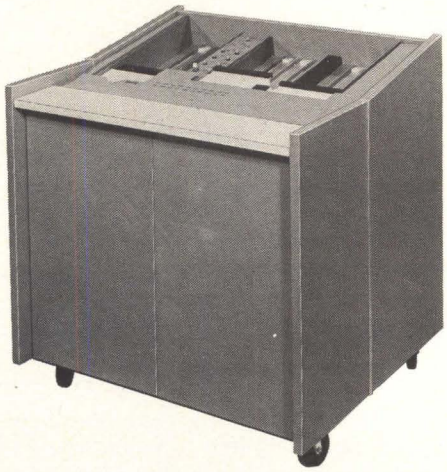
The data products MSR-1500 makes sure they won't miss!

When the Danish Telephone System needed a fast, dependable way to tally telephone tolls, Regnecentralen, our customer in Copenhagen, installed a computer system incorporating our new MSR-1500 Card Reader.

The MSR-1500, a complete Speedreader-1500 **with mark-sense reading capability,** can read both mark-sense **and** punch cards, at 1500 cards per minute. The MSR-1500 can also read punches and marks from the same card.

Accurate data transfer is assured by the electronic checking of reading, timing and card travel on every card cycle. Solid-state electronics, plug-in modules, operational flexibility, low cost and ease of interface helped an OEManufacturer solve a problem in Denmark. How (or where) in the world can we help you?

For detailed literature write
data products/uptime,
8535 Warner Drive,
Culver City, Calif. 90230

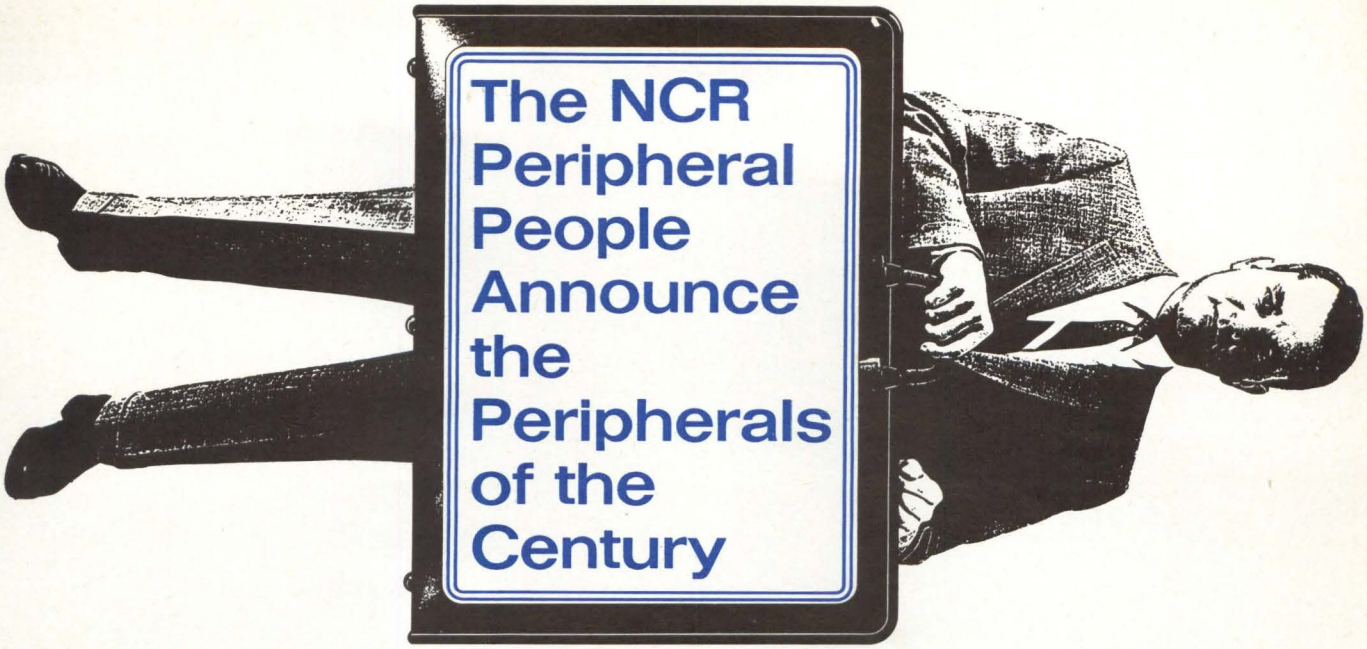


data products | uptime

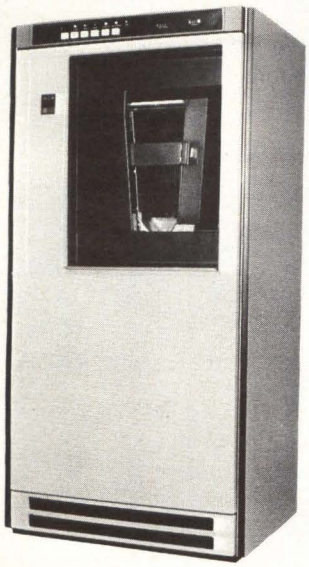
"the peripheralists"

data products manufactures
LINE/PRINTER®, DISCFILE™, Core Memories, Tape Cleaners, Off-Line Printer Systems, Card Readers & Punches

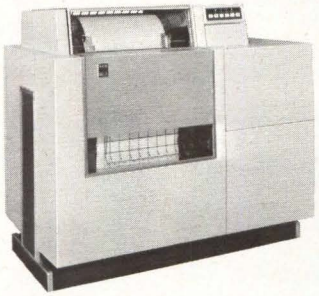
CIRCLE ON. 9 ON INQUIRY CARD



The NCR Peripheral People Announce the Peripherals of the Century



EM-H6 CRAM (Card Random Access Memory)
Super CRAM! The billion bit (125 million byte) 4th Generation Peripheral reads and writes faster at random than many sequential units. Average access time is 115 ms. One controller can handle 8 CRAM-6 on one imput line. Automatic read after write.



EM-C5 High Speed Printer
Prints up to 3000 lpm. "Swing-away" typedrum, interchangeable tool steel drums. Excellent operator access to exchange drum, ribbon, paper and code discs. Magnetic particle clutch for years of maintenance-free operation. Incomparable!

EM-C3 Low Cost Printer
NCR built everything except blinding speed into this unit. It's reliable, offers flexibility, operator access never before possible. Prints 450 lpm using 48 of the 64 character set or 900 lpm using double numeric typedrum.

EM-J1 Dual Disc Unit
Fastest access time of any comparable disc drive—48 ms avg. With 12 read/write heads per disc surface you can access up to half a million bytes without head positioning. Each unit contains two disc packs (six surfaces, 72 read-write heads each) for a total capacity of 11.6 million eight bit bytes. It's "big system" hardware at an amazingly low price.

NCR knows electro-mechanics. For more information about these and other NCR Peripherals, call or write the Peripheral People today.

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CIRCLE NO. 10 ON INQUIRY CARD

Stop worrying about your IC digital system and let Raytheon Computer ask one question.

How do you want it?

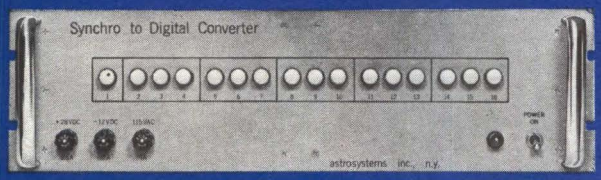
Ask for a MINIVERTER™, not just a converter. Start with a 16-channel multiplexer, sample-and-hold amplifier and 10 or 12-bit binary or 13-bit BCD A/D converter—wired, tested and mounted on a connector block you can hold in your hand or install in your own drawer. Or order it in a 40-module drawer with indicator lights, panel controls and other options, or in a 120-module case with even more options (like up to 256 channels). All our analog instruments offer the same flexibility whether you want a MINIVERTER, the A/D converter only, or just a sample-and-hold or multiplexer.

Analog and Digital IC Modules. There's a complete range of analog and digital functions. To make systems design and assembly easy, mounting hardware and accessories have analog and digital power and ground distribution built in. You can even send us your wire list and we'll send you an automatically wire-wrapped and assembled system within weeks—faster and cheaper than you can do it yourself. All modules and instruments are compatible with our $15,000 703 IC Systems Computer.

We've done most of the work, so for the first time digital systems engineering can be fun. Call or write today and ask for Data File C-152. Raytheon Computer, 2700 South Fairview St., Santa Ana, Calif. 92704 Phone (714) 546-7160.

Raytheon Computer... the company that gives you a break.

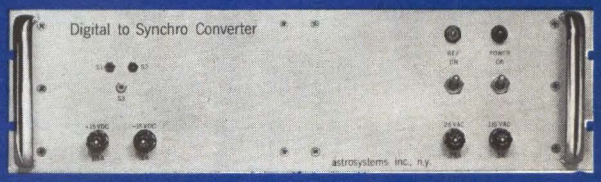
Synchro to Digital



Synchro and/or Resolver to Digital
MODEL NO. A-602-16
OUTPUT: Parallel Binary
RESOLUTION: 1 part in 2^{16}
ACCURACY: ±9 seconds

(Options available to suit any requirement)

Digital to Synchro



Digital to Synchro and/or Resolver
MODEL NO. A-702-16
INPUT: 16 Bit Binary, Parallel Entry
OUTPUT: 3 or 4 Wire AC
(Synchro or Resolver 11.8 to 90V)
ACCURACY: ±9 seconds
(Options available to suit any requirement)

If you need converters, come to the people who perfected them.

We build the very best in:

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Digital to Synchro Converters
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CIRCLE NO. 12 ON INQUIRY CARD

NEW NEW NEW

Incremental tape recorder

FACIT 4210

- IBM-compatible
- low price
- control unit available
- extremely compact

FACIT

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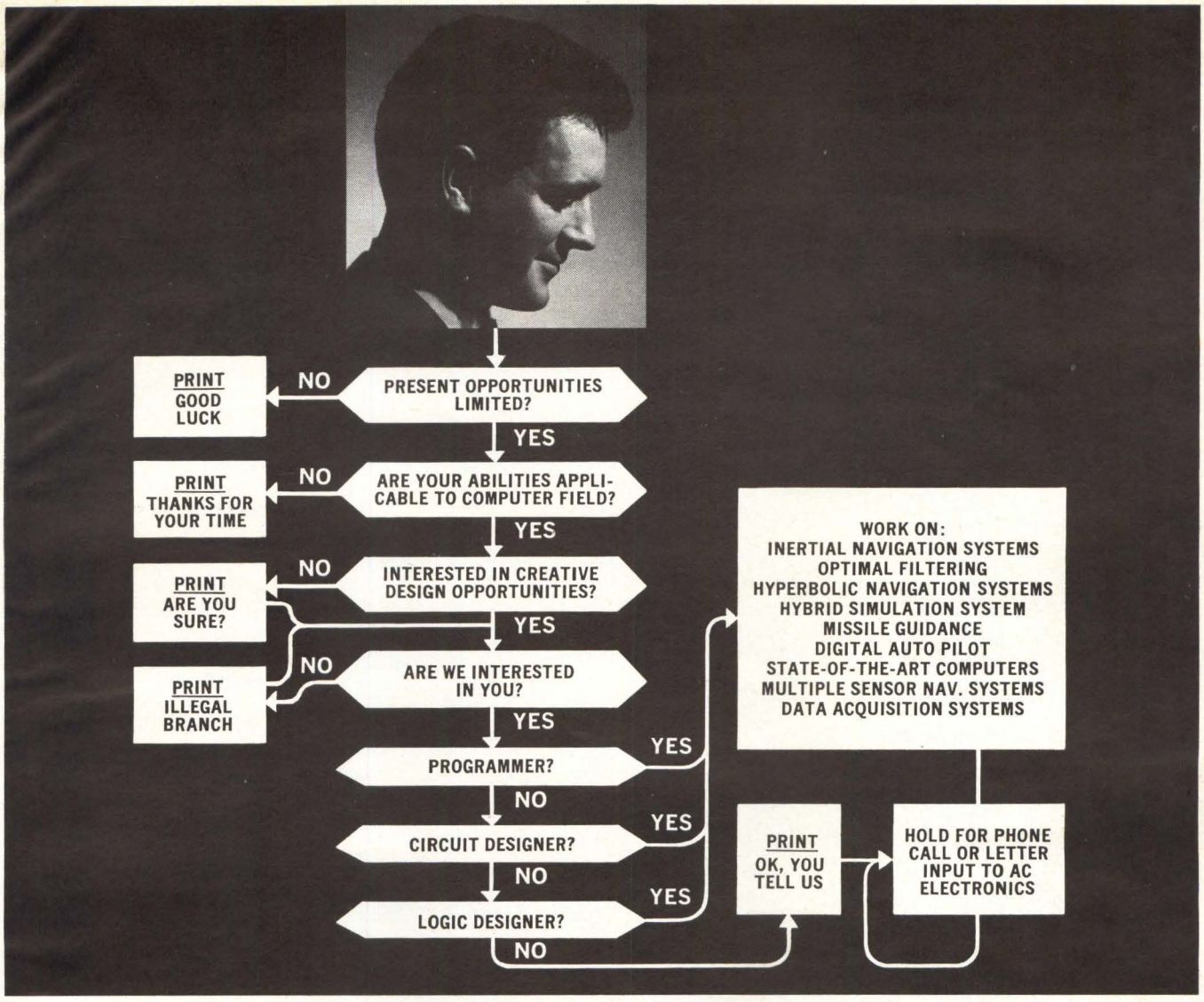
CIRCLE NO. 31 ON INQUIRY CARD



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Design, check-out, and evaluation of advanced circuits utilized in special-purpose digital and hybrid airborne computers. Will utilize recent advances in integrated circuit development.

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Perform detailed mechanization of memory devices used in AC-developed MAGIC series computers.

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Perform logic and circuit design, development and check-out of airborne and ground instrumentations systems.

Computer Logic Designers —
Develop and optimize advanced logic input-output design for use in real time computer application.

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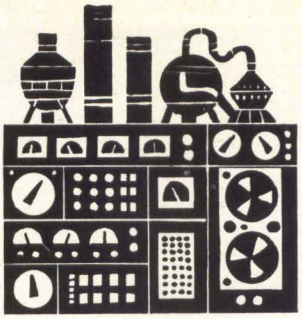
CIRCLE NO. 900 ON INQUIRY CARD



INDUSTRY NEWS

NEW FERRITE COMPOSITION DEVELOPED — A National Aeronautics and Space Administration physicist has announced the development of a new ferrite composition which should lead to less expensive temperature-stable memory cores.

Howard Lessoff, in a technical paper presented before the annual meeting of the American Ceramic Society last month, reported the composition was developed in the Materials Branch of the Component Technology Laboratory at NASA Electronics Research Center, Cambridge, Mass.

The new composition is obtained by a partial substitution (order of a few atomic percent) of calcium for iron in lithium ferrite. "The calcium has beneficial effects on the conditions of the sintering process by which memory cores are made," Mr. Lessoff said. "Sintering temperatures are decreased, secondary recrystallization is inhibited, grain size and porosity are reduced, and the size distribution is made more uniform."

The composition has potential application in the fabrication of memory cores for space-borne computer memory systems. Compared to the presently-used lithium ferrite, the new composition offers greater uniformity and reproducibility of properties, and substantial reduction of operational power requirements.

AIRBORNE DIGITAL COMPUTERS — Each giant U. S. Air Force-Lockheed C-5 cargo transport will carry as standard equipment three airborne digital computers built by the Nortronics Division of Northrop Corporation, in Hawthorne, Calif.

Two of the lightweight digital units are a part of the inertial-doppler navigation system built by Northrop for the C-5 Galaxy. (Two computers are used to provide primary and auxiliary systems.) The third computer, similar to the navigation system computers but with a different input/output unit, is used in the airplane's Malfunction Analysis Detection and Recording (MADAR) system, designed by Lockheed.

Both primary and auxiliary digital computers in the navigation system's data processing section are high-speed (parallel arithmetic) general purpose machines with random-access core memories. Combined memory capacity is 20,000 words. Add time is eight microseconds, with a word length of 28 bits.

Either computer can be used to back up the other in case of trouble. In addition, each will be programmed to perform a few separate functions. The two, however, provide computational redundancy in all principal navigation tasks. The MADAR computer has an 8000-word memory, but the same add time and word length as the navigation computers.

The low weight of the computers is achieved through maximum use of film hybrid circuits and microelectronic integrated circuits, plus advanced packaging techniques. These engineering and packaging techniques also allow production of the digital computers at low cost with very high reliability. Although they are extremely compact and lightweight, the airborne units have all the computational capability of large data processing machines. Because of their versatility, the computers are being successfully applied to several other current aircraft and space programs.

UNIQUE SEMICONDUCTOR TEST SERVICE — TI Supply, a distribution subsidiary of Texas Instruments, is inaugurating a complete semiconductor testing service for its customers with the establishment of a testing center in the New York City area at Great Neck. Duplicate facilities already are installed in Houston, where TI Supply began a pilot operation five months ago to evaluate this type of service which is unique among distributors of electronic supplies.

The new VersaSTORE II core memory system can give you all the speed, capacity, and convenience you'll ever need.

It can also save you a few bucks.

1.6 μsec asynchronous speed with 650 nsec access time.

Capacity up to 4096 36-bit words, up to 8192 18-bit words.

Occupies only 5¼" rack space, weighs less than 35 lbs.

VersaSTORE II capacity is expandable via exclusive "Party Line" design.

Plug-in stack permits easy service.

Includes timing and control flags, test points, and optional self-test for easy system checkout.

All-silicon design and modular front-access construction.

Servoed current drive system compensates for ambient temperature changes, insures excellent margins under elevated temperatures.

VersaSTORE II is our improved version of the original VersaSTORE memory with more than two years' success in hundreds of systems.

We'd be happy to give you an unlimited amount of our own personal time, or even send you a copy of our complete new VersaSTORE II brochure. Just call or write.

Let us quote on a VersaSTORE II to meet your requirements. Our low price will surprise you.

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a varian subsidiary
Formerly Decision Control, Inc.
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We need Senior Development Engineers and Programmers. Write to Mr. Bruce Ferris.

Both centers will handle discrete components, circuit cards, integrated circuits, and Large Scale Integration products of any manufacturer.

Everett Hanlon, Test Service manager, Houston, said, "These centers give the small manufacturer access to a sophisticated testing service that only a few major companies could afford outright, without need for capital investment or increased overhead. They also provide fast 'overload' relief for larger manufacturers, meeting requirements for the most complex programs and all government specifications." He added that most moderate production lots could be processed and returned to the customer within 48 hours.

Equipment in the centers includes dynamic test systems for parametric testing, test controllers, testers for d-c and pulse testing of discrete components, and computer controlled systems for functional testing of digital circuits.

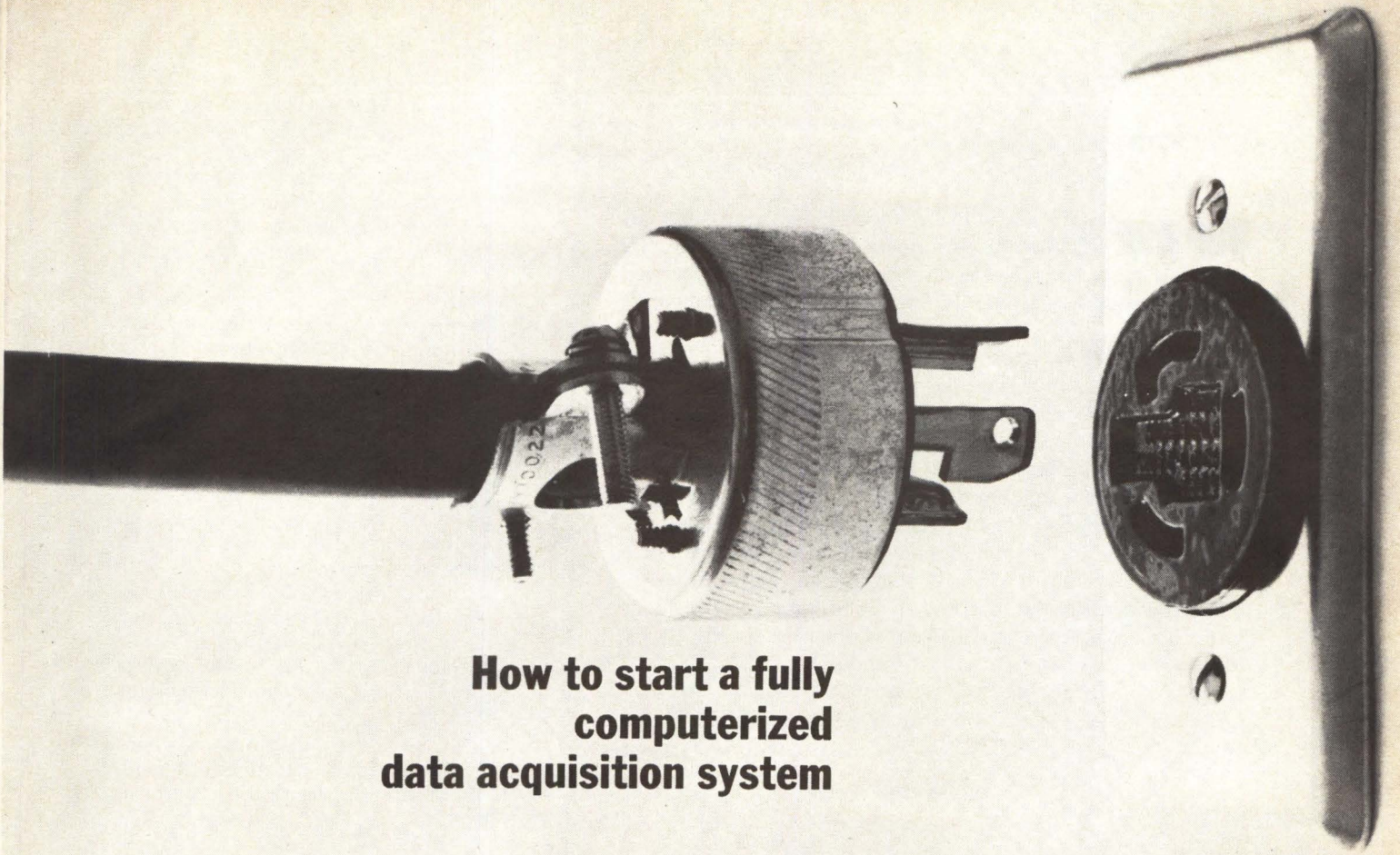
In addition to computerized testing of d-c, linear, and dynamic parameters, the centers provide burn-in and component aging services, and physical and chemical environmental tests.

"Many standard test programs already have been developed by Texas Instruments for use with components made by TI and other companies," Mr. Hanlon said. "These software programs are available to our customers at no additional charge. Such programs also can be modified at minimum charge, or special test programs can be developed as required."

The scope of services of the new centers includes incoming inspection on a statistical sample or 100 per cent test basis; screening for selected characteristics, electrical failure analysis and special studies.

SILVER-PALLADIUM ELECTRODE PASTE LOWERS CIRCUIT MODULE COSTS — A patent has been granted to an International Business Machines Corporation chemist covering a composition and method for silver-palladium electrode pastes that perform better than commercially available pastes costing up to ten times as much.

Lewis F. Miller, of IBM's Components Division development laboratory in East Fishkill, New York, received patent number 3,374,110 for his invention of the new compositions. One of the compositions is now being used in the manufacture of Solid Logic Technology (SLT) circuit modules, the micro-



How to start a fully computerized data acquisition system

DIGITAL makes complete computer based acquisition systems at prices beginning at $20,000. They are complete and ready to start work the day they are delivered. Just plug them in and go.

For collection and analysis of analog and digital inputs. For data logging. For status, log and alarm. For complete closed-loop control.

DIGITAL's data-logging systems collect the data in the form you want, read it out on standard teletype as hard copy, all at computer speeds. The data-collection and analysis systems preprocess the information and provide outputs on industry-compatible magnetic tape for computer analysis. Status log and alarm systems are bigger. Closed-loops are bigger yet. But to you, consider these systems black boxes.

DIGITAL's systems incorporate some of the smallest and least expensive; some of the most sophisticated and powerful computers in the world. They incorporate the converters that feed these computers, the multiplexers, the consoles. Complete computerized systems for data acquisition that can grow as your business does.

Because growth is important. DIGITAL customers appreciate the compatibility of one DIGITAL computer with another, the compatibility of the converters with several computers, the ultimate compatibility of the interfacing that is built from one of the largest module lines in the industry. The modules, in fact, that are used in the computers themselves. Stepping up and growing is built into the DIGITAL systems.

We'll match the size of the system to the size of the problem — a small system that includes the $10,000 PDP-8/S, a more powerful one that incorporates the $35,000 PDP-9, a giant that uses the $500,000 PDP-10, and many stops inbetween. But to you, black boxes all.

And DEC provides easy to use software packages to let you assemble programs tailored to your application.

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COMPUTERS · MODULES

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electronic building blocks in IBM System/360 computers.

The electrode paste consists of approximately 4 parts silver to 1 part palladium, and a vitreous frit, dispersed in an organic vehicle. The paste is applied to the surfaces of ceramic substrates through a silk-screening process to form conductive ciruit patterns or "lands." The paste is then dried, fired, and finally tinned with a layer of solder. In other process steps, resistors are formed and active semiconductor devices (transistors and diodes) joined to the pattern at selected points to complete the SLT hybrid module circuitry.

For the manufacturing process, the conductive lands formed by the paste are usually no more than 5 to 15 thousandths of an inch wide and only a fraction as thick.

In addition to being several times less expensive than similar pastes made from combinations of other precious metals, this formula offers these properties and advantages over previous compositions:

- The silver-palladium lands sinter and fuse exceptionally well, forming a very dense, uniform land — much better than that provided by other metallurgical systems.
- The conductivity is significantly greater than the commonly used gold-platinum pastes.
- The paste has demonstrated excellent compatibility with glazed resistors and other passive components with respect to such properties as scaling, interfacial hot spots, temperature coefficient of resistance, and drift.
- The paste drastically reduces the tendency of pure silver to form extraneous conductive paths under conditions of high humidity and high current levels. Furthermore, it is particularly solderable and not subject to dissolving in molten solders, as normal silver preparations are.
- The formuation is reliable, reproducible, and readily adaptable to mass production techniques.

CERAMIC METAL FIXTURE INCREASES PRINTED CIRCUIT BOARD PRODUCTION — Printed circuit board production at the Univac Division of Sperry Rand Corporation, Utica, New York, has been increased by the use of a newly-designed fixture made from Nucerite, a ceramic-metal compo-

6 new off-beat 2½ D stacks.

1 HEATED STACK — Built for a process control application, this has an extremely large bit length. (16K x 25 bits). Heaters keep the temperature a constant 55°C ±3°C; but the whole stack with heaters and large capacity only takes up 750 cubic inches.

2 FOLDED STACK — We've built hundreds of these for SDS computers over the past year. With a 4K x 9 bit capacity, the stack uses our 20 mil cores, and turns out a cycle time of 830 nanoseconds.

3 HIGH/LOW TEMP STACK — This 8K x 18 bit 2½ D, built for RCA, uses our special lithium cores. They have a low temperature coefficient and excellent stability over a 10°C to 55°C range. The beauty of this is that the customer doesn't have to bother with temperature compensation.

4 COMPACT STACK WITH LARGE CAPACITY — For Honeywell, we put together a 32K x 18 bit prototype stack in a space of 600 cubic inches (10" x 20" x 3"). This stack uses our 20 mil cores and has a cycle time of less than 650 nanoseconds.

5 SPLIT MODULE STACK — This was a tricky one for Raytheon. It was a special 16K x 18 bit stack, and two sets of diode modules in the word direction had to be placed on each side of the stack. (Usually, they're all on one side.) The whole stack was designed, built, and shipped in 8 weeks.

6 NANOSTACK™ — We use this one in our large capacity NANOMEMORY system, but we've also been making a modified version for over a year and a half for Digital Equipment Corp. The stack has an 8K x 18 bit capacity and measures only 10½" x 20½" x 2".

If your 2½ D requirements are off-beat, call us, and we will see what we can do for you. Or write for Litpak 100 describing our stack capability.

EM electronic memories

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site made by The Pfaudler Co., a division of Ritter Pfaudler Corporation, Rochester, New York, and used widely in the chemical process industries.

Prior to using Nucerite fixtures, the Division had a serious adherence problem in its printed circuit board soldering operation. The previously used fixtures, holding the printed circuit boards, were deteriorating and picking up unwanted solder as they passed through the solder bath. As a result, the printed circuit boards were frequently soldered to the fixture and were damaged, sometimes beyond repair when removed.

The solution was a Nucerite ceramic-metal fixture. Clifford Monfils, manufacturing engineer at Univac, said, "It really did the job for us when everything else failed. We since have ordered 40 additional Nucerite fixtures.

"Because of the new fixtures we've increased our production, enhanced product reliability, and saved ourselves a considerable amount of money. In addition, it has made it easier on our employees who work on the soldering line. They no longer have to stop production and remove solder from the fixture, which is a tiring and costly task."

The Nucerite fixtures have been in operation for about three years and are still in good condition. Even when severe mechanical abuse produces some chipping of the fixture, enough of the Nucerite ceramic remains on the metal to prevent adherence of the solder. There is no wear at all in the grooves which grip the printed circuit boards. This area, which accumulates much solder, was a constant source of difficulty with previously used fixtures.

Use of the Nucerite fixtures has also simplified the conveyorized system which is in operation now two eight hour shifts a day, five days a week. No longer is it necessary to slow down the operation due to a lack of needed fixtures, while removing the unwanted solder which has accumulated on the base metal.

The four step soldering procedure is simple, efficient, and reliable. After loading in the fixtures, the printed circuit boards are flux coated in a mildly activated, rosin base mixture. They are then passed over pre-heaters raising the temperature to about 200 degrees Fahrenheit. The fixtures are then passed through the top of a solder wave for 6 to 10 seconds at 500°F.

At the end of the conveyor line,

the printed circuit boards are removed from the fixture and rinsed in Chlorothene at 110 degrees Fahrenheit. They're now ready for minor touch ups prior to being used in Univac computers. The fixtures are then sent back for reloading.

Success of Nucerite in this application is attributed to the combination of unusual physical, chemical, and thermal properties exhibited by the composite, which is made up of a specially formulated ceramic fused to a base metal, in this case stainless steel. Nucerite has high resistance to corrosion, abrasion, impact strength and temperature stability to 1450°F.

AIRBORNE FOLDED ARRAY MEMORY — Engineers at Indiana General Corporation, Electronics Div., Keasbey, N. J., have designed a miniature memory stack utilizing a folded array technique to provide increased reliability. The memory is for use in the tiny D26J-41 Inertial Navigation Computer being built by the Autonetics Div. of North American Rockwell Corp. The computer in conjunction with an N16 Autonavigator form the inertial navigation set for the F-111D and FB-111A aircraft Mark II type Avionics system.

The D26J-41 is a microminiaturized, general purpose, synchronous, parallel mode, internally stored program digital computer. Measuring 19.75 x 6.50 x 8.0 inches, it occupies 0.59 cubic feet and weighs but 26.4 pounds, including the power supply and input/output. The power supply inverts the aircraft's 28 volts d-c at 160 watts to 115-volt 400 Hz. single-phase current to operate the computer.

Memory is random access, destructive readout, protected from power failure and transients. The memory stack is a Microstack® package, with a storage capacity of 4096 words, 12 bits per word. It is strung with 30-mil, 0.645 switching time, wide temperature-range ferrite cores in coincident current fashion, four wires per core.

All 49,152 cores are contained in the one-inch-thick stack which measures 5 11/16 x 5 9/16 inches. They are strung on continuous wires in four mats of 12,288 cores each, which are folded, one upon the other, to form the complete array. According to Indiana General engineers, the folded array technique increases reliability by reducing the number of solder connections by 80 percent compared to conventional frame construction. In the Autonetics stack, compared to a

conventional one - frame - per - mat stack, the number of necessary solder joints was reduced by more than 2500. The entire Microstack, including the decoding diodes which are integral with the printed circuit board cover, weighs 1.25 pounds.

The MIL operating specifications the stack will meet are:

1. Temperature, −55°C to plus 80°C and MIL E-5400 H
2. Shock, 20 g's for 11 milliseconds duration and MIL Standard 810A
3. Vibration, 80 mil double amplitude between 15 and 50 cycles, 60 mil double amplitude between 50 and 100 cycles, and 10 g's between 100 and 500 cycles.

The stack can cycle in 2.5 miroseconds. Based on a one megahertz clock, the arithmetic speeds are: Add —8 microseconds; multiply —18 microseconds; and divide —18 microseconds. The twelve-bit word length includes sign/single precision, but becomes 23 bits including sign/double precision. Instructions are 36 plus input/output and modified instructions.

The navigation computer is constructed with monolithic integrated circuits mounted on multilayer modules. In addition to the MIL-E-5400 temperature and vibration specs, the computer is designed to meet the MIL-I-6181 specs for RFI and EMI. Cooling is by conduction to the chassis and external forced air. The unit features built-in test capability (BITE), one interrupt and power control.

FIRST IMPLEMENTATION OF NEW COMPUTER LANGUAGE — Dr. Ralph T. Dames, President, announced that Spectrodata is implementing a new digital computer language designated Continuous System Simulation Language (CSSL). Basic CSSL Specifications were originally developed for industry by a committee of Simulation Councils, Inc.

CSSL is designed to facilitate the simulation of continuous dynamic systems on a variety of digital computers. CSSL can be used as a simple programming tool for the scientific user while still providing the sophisticated programmer the power and flexibility needed for a major programming task. Although the initial application for CSSL is in the field of digital and hybrid simulation, Dr. Dames expects broad interest in many real time areas, including bio-medical and the process control industry.

Lockheed stacks stack up.

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Core after core, plane after plane ...the only difference between Lockheed stacks is the serial numbers. This precision means memory systems using Lockheed stacks are more reliable.

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Testing is another way Lockheed assures reliability. An average plane in a stack must pass 260,000 performance tests (based on an average of 16K words per plane) before the stack can be shipped.

Lockheed also knows your business. We make memory systems, too. So our stack designs are systems-oriented... and perform that way. Plus, Lockheed offers you a large library of standard stack designs covering the entire range of memory systems technology.

■ For stacks of additional technical material, promptly mailed, write to: Memory Products, Lockheed Electronics Company, 6201 E. Randolph Street, Los Angeles, Calif. 90022. Or save a stamp and call (213) 722-6810.

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KING-SIZED MODEL SOLVES SMALL DESIGN PROBLEM — Two IBM engineers seeking to reduce transmission noise in an experimental computer device found the answers they needed by creating an electro-dynamic model of the transmission lines nearly 20 times their actual size.

Results of the study were described last month at the International Conference on Magnetics by Erich Valstyn, with the Systems Development Division of International Business Machines Corporation at San Jose, California. Co-designer on the project is Timothy Moth, with the IBM development laboratory at Hursley, England.

The noise problem faced by the engineers arises only in very fast systems where a ground plate is used for current return. Under these conditions, diffusion of current into the ground plate results in a slowly decaying noise voltage. To solve the problem, they decided to investigate three design alternatives: stratifying the ground plate, keeping the plate at a low temperature, and terminating the line with a small resistor-capacitor network.

Initial attempts to work with the transmission line in miniaturized form quickly met with obstacles. Accurate measurements were prohibitively time-consuming and uncertain, and changes required expensive fabrication techniques such as vacuum deposition and electroplating.

The designers turned to the task of constructing a scaled-up model that would exactly duplicate the electrical properties of the actual device. They achieved this by mathematically increasing the time scale and the resistivity of the materials by the same factor as they applied to the physical dimensions. A common metal alloy (Cu Ni Zn) was used to simulate copper in the transmission lines and ground plate of the scale model.

Advantages of the scaled-up values were immediately apparent. Physical dimensions as small as three microns in the miniaturized device now became accessible to accurate measurement with an ordinary micrometer. And line responses, previously vulnerable to distortion even from test instruments, were no longer significantly disturbed by drivers, terminations and measuring equipment.

By using the scale model as a design tool, the engineers were able to establish that all three design methods were capable of considerably reducing the noise problem.

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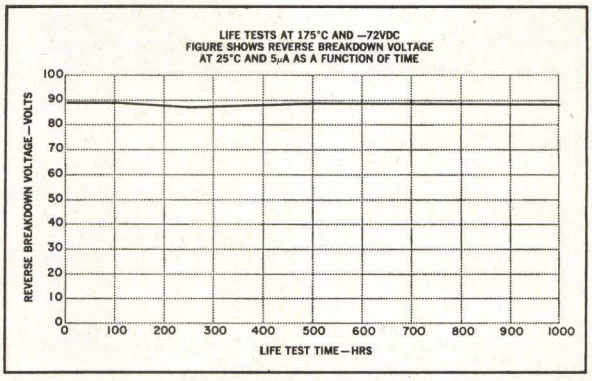

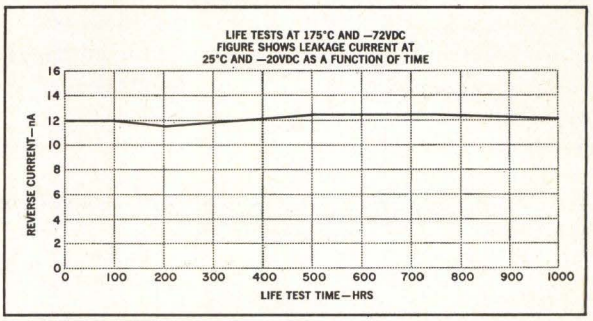

The figures above show the extreme stability of NITRODES under high temperature DC blocking test conditions.

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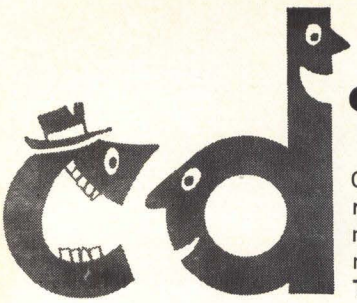

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

INTEGRATED CIRCUIT FABRICATION: Where Can Costs Be Sliced?

by

D. E. MARSHALL, JR.

In the past three years, drastic reductions in the price of integrated circuits have resulted from rapid advances in high-yield/high-volume fabrication processes, but this is just the beginning. The numerous estimates predicting future purchase costs cannot be ignored by the system designer. Let us investigate how IC fabrication expenses can be cut to help these predicted costs.

First, consider the cost associated with the various steps in IC production. The production cycle has been simplified into six steps:

1. **Slice Fabrication and Preparation** — including silicon bar fabrication, slicing, slice lapping and surface preparation
2. **Slice Processing** — including the numerous steps involved in diffusing the electronic devices into the silicon slice and interconnecting them
3. **Probe Testing** — the dc testing conducted on the circuits prior to assembly and the separation of the slice into individual circuit chips
4. **Package Fabrication** — preassembly of the chip package
5. **Assembly** — scribing, chip to package attachment, chip to lead wire bonding, and lidding
6. **Final Test** — electrical, hermetic, and environmental tests.

Consider an "off the shelf" commercial integrated dual or quad digital logic gate in a 14-lead flat pack. Silicon chip size would be about 40 mils square with 500 circuits fabricated on a one-inch diameter slice.

Mr. D. E. Marshall, Jr., the author of this month's CD Commentary, is Manager of the Microelectronics Circuit Development Department at Honeywell's Computer Control Division. He has circuit design responsibility in converting the circuit needs of the division's computer and modular product lines into integrated circuitry purchased from major IC manufacturers.

TABLE I. IC FABRICATION COSTS

Function	Labor and Material Cost	Yield
Slice Fabrication and Preparation	$1.00/slice, 0.2¢/circuit	
Slice Processing	$5.00/slice, 1.0¢/circuit	
Probe Testing	$2.00/slice 0.4¢/circuit	60%
Slice Total	1.6¢/circuit	
Slice Total/good circuit	2.7¢/circuit	
Package Fabrication	25¢/package	
Assembly	20¢	
Final Test	5¢	70%
Total	52.7¢	
Total Cost per circuit	73.5¢	

Table I shows approximate costs for the six fabrication steps described above. The figures do not represent any specific process, but are average numbers showing the relative contributions of the various steps to the total circuit cost. Actual sell price would be derived by applying an appropriate markup factor to cover G & A, profit, etc.

There are a number of places in the fabrication cycle, particularly during slice processing, at which rejects may be eliminated through visual or electrical tests. However, Probe and Final Test are the two places where comprehensive electrical testing is per-

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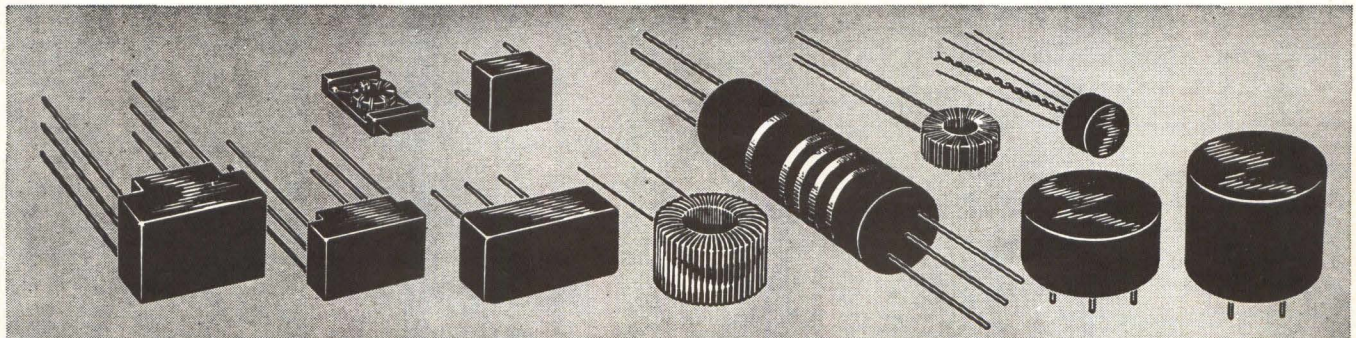

Here are commonly used packages for which tooling is available. Other configurations are always possible.

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formed and most rejects are caught. For simplicity, the table shows inclusive yields up to these two points.

High Package and Assembly Costs

The most striking fact to be seen from this table is the relatively low cost of the completed slice compared to the total circuit cost, or conversely, the high package and assembly costs. This factor is responsible for many of the developments being undertaken in integrated circuits today.

The epoxy package is a good example. Instead of mounting the circuit chip in a separately fabricated kovar or ceramic package, a number of chips are mounted directly on a multicircuit lead frame and simultaneously compression molded. This approach reduces package material costs, eliminates package preassembly, simplifies wire bonding from the chip to the package leads, and allows the circuits to be handled more easily in larger batches during assembly. Result: a package and assembly cost of about 19¢ for a total good circuit of about 41¢. There are other approaches being developed which compete with the plastic package in reducing complexity and cost.

The high packaging and assembly cost has also intensified the search for low-cost labor in this country and abroad. Nearly all the assembly cost is labor, mostly incurred during wire bonding.

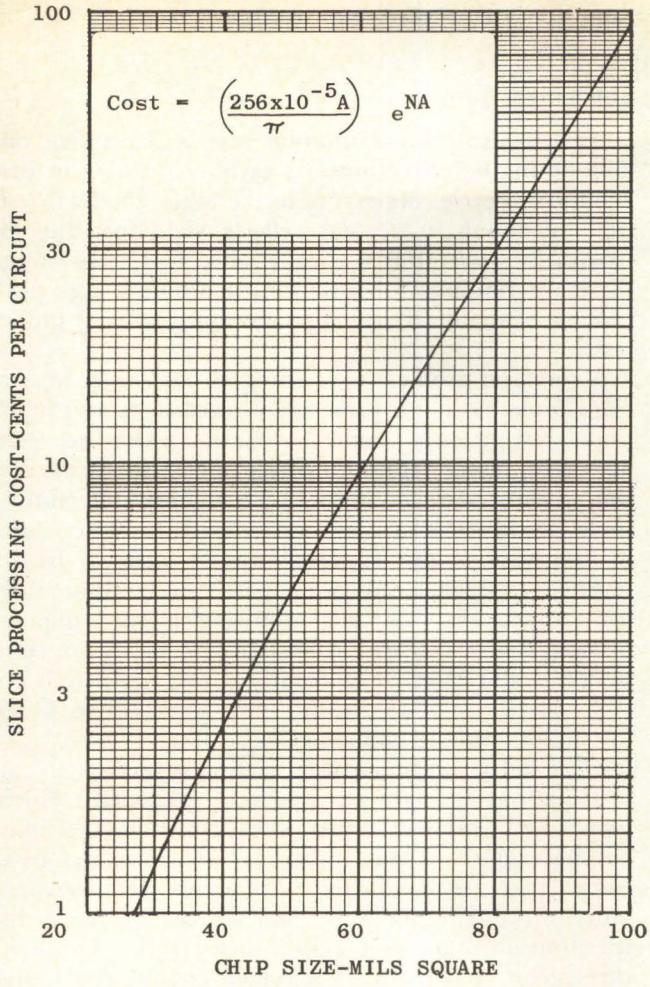
Other notable developments being pursued to reduce wire bonding costs are the flip-chip technique and the beam lead technique. Both of these approaches attempt to replace 14 separate wire bond operations (for a 14-lead package) with a single simultaneous bonding operation. The assembly cost reduction potential is about 8¢ to 10¢ a circuit before yield is considered.

Ultimately, the presently conceived package may disappear entirely with the development of a well passivated silicon surface and a selfsupporting, mechanically reliable lead technique. The economic advantages of this approach are evident from the table.

Where to Chop a Chip

Even considering the continuing cost reductions which are occurring in IC packages, for the example given, the processed slice cost is still only about ten percent of the total. It would seem likely that more performance per dollar would be obtained by adding more gates to the chip and making use of the added logic capability. This, of course, is what is happening in the new product releases in functional circuits. If yield and probe test costs were unchanged, a 60 mil square chip with the functional equivalent of 16 gates costs 6.1 cents through probe test since the number of circuits per slice is reduced from 500 to 220.

There are basic limits on how far chip area can be increased without affecting slice yield and test costs. First of all, slice yield can be attributed to two general types of defects: gross defects in which large areas of the slice are affected, and point defects in which areas much smaller than the chip are affected. Slice yield is independent of chip size for the first type of defect until very large areas are reached. However there is a much stronger relationship between chip



area and yield for point defects. A good approximation is:

$$Y = 0.8e^{-NA}$$

where Y is slice yield, A is chip area in square mils, and N is about 2 x 10^{-4}. For the 40 square mil chip previously discussed, the contribution to slice yield loss is about equal for gross and point defects. Above 60 square mils, point defects predominate and severly reduce yield and increase slice cost.

At 120 mils square (about 70 gates), slice processing yield is so small that the cost-performance ratio becomes unfavorable with present fabrication techniques. If present trends continue, the constant N will be pushed out at a rate of about 10 to 20 percent per year.

Bigger Circuit smaller Market

Secondly, more logic per circuit means a direct reduction in circuits per system, a smaller market, and resultant higher sell price. An additional market reduction occurs because the logic must be more committed and therefore is useful in a smaller number of applications. A higher logic complexity also means increased test time at both Probe and Final Test. The simple circuit first described may require 20 dc tests at probe and the test time is essentially all in sequencing from circuit to circuit on the slice.

For committed logic the number of functional tests required increases at a greater rate than the number of gates, and may approach a 2^k rate of increase, where k is the number of functionally related inputs. The

same considerations apply to Final Electrical Test.

Catch them Early

Success in achieving minimum cost is dependent on eliminating defective units as early as possible in the production cycle. Referring to the table, the final test field of about 70 percent reflects yield loss due to fabrication operations after Probe Test. However, there are a number of situations in which a high percentage of the defective chips are not caught at probe test.

A common problem is catching ac parameter rejects since probe testing is presently limited to dc and functional testing only. Some correlation exists between dc performance and ac performance in relatively simple integrated circuits. In the majority of off-the-shelf circuits, the ac specifications are broad enough so that most of the ac rejects can be detected by dc testing. In high-speed gates, particularly those that utilize saturated switches requiring a gold doping process, this is not true, and final test yields are considerably less than 70 percent. If this yield falls to 50%, total circuit fabrication cost increases to $1.05 for the example in the table.

Since it is rarely possible to test as accurately at probe test as at final test, any circuit parameter which is specified close to the process distribution peak may not be caught at probe test. To minimize test cost, probe tests are conducted at ambient temperatures only, introducing an additional source of error if the specification includes a significant operating temperature range. For a tightly specified circuit, test limits at probe are a compromise between guard banding to reject as many valid rejects as possible and widening limits to avoid rejecting good units due to measurement errors. The classic "out" of the above problem is the double or triple selection level at final test into "Military", "Industrial", and sometimes "Limited Temperature Range" versions.

Since only the area of the chip which has a device on it is susceptible to the point defects previously discussed, reducing component size will improve slice yield. Bipolar components are likely to see a four-to-one reduction in size over the next several years. The MOS transistor has a much smaller area in addition to a simpler process (about one-third the slice processing steps). For well organized functions requiring low interconnection area, the smaller MOS device area is taken advantage of in an order-of-magnitude increased functional complexity compared to bipolar circuits.

Summary

IC production technology has reached the point where the cost of the basic electronic device is small compared to the interconnection and packaging media for high volume standard circuitry. The result has been a two fold effort to reduce lead and package cost through new developments and cheaper labor; and to provide more performance per dollar using larger, more costly chips with greater logic power. Since slice processing yields will continue to improve, these trends will continue through the foreseeable future.

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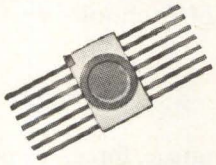

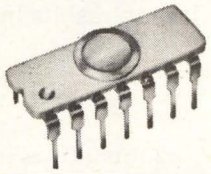

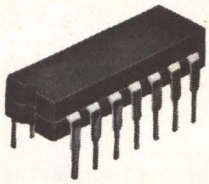

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Expandable Input (6KΩ)	CD2312	$2.90	CD2312D	$2.90	CD2312E	$1.45
Expandable Input (2KΩ)	CD2313	$2.90	CD2313D	$2.90	CD2313E	$1.45
Flip-Flops						
Clocked RS with JK Capability (6KΩ)	CD2304/945	$3.00	CD2304D/945	$3.00	CD2304E/845	$1.90
Clocked RS with JK Capability (2KΩ)	CD2305/948	$3.00	CD2305D/948	$3.00	CD2305E/848	$1.90
Input Expander						
Dual 4-Diode	CD2314/933	$2.25	CD2314D/933	$2.25	CD2314E/833	$ .90

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RCA
Integrated Circuits

A low-cost remote terminal to provide switch-form output from a time shared computer is described. The terminal consists of a modified model 35KSR teletype and a local memory unit. The unit is independent of any particular computer, and is easy to test and maintain. The states of the memory control and memory words are observable directly by indicator lights. An application of the memory to automatic set-up and control of an analog computer is included.

A LOW-COST OUTPUT TERMINAL FOR TIME-SHARED COMPUTORS

RONALD C. ROSENBERG
DANIEL W. KENNEDY
ROGER A. HUMPHREY

Project MAC
Massachusetts Institute of Technology

The problem of retrieving information from a time-shared digital computer is typically met in several ways; e.g., printers, punched cards, and magnetic tape. For many applications it is desirable to have access to digital information in the form of switch settings (or states). This permits local decisions to be made regarding the use of such information. For example, a terminal which has a keyboard and a bank of switches under digital computer program control, permits symbolic manipulation and control of local hardware, as well as computer analysis of experimental data in the laboratory. It is the purpose of the equipment described in this article to provide such a terminal at low cost. The terminal itself is ultimately connected to an on-line time-shared digital computer.

As an example of the use of such a memory, we briefly describe the ENPORT program,[1] and its associated output. The ENPORT program is designed to simulate the time behavior of certain classes of multiport engineering systems, such as hydraulic, mechanical, and electrical circuits, and systems involving measurement and control. Description of a particular problem requires relatively little information (e.g., the system structure, parameters, initial conditions). The available output includes time histories of powers, energies, and signal quantities such as voltage, force, and velocity. An analog computer is masterful at displaying such information, once it has been set up. Setting up involves wiring, setting coefficients, and scaling, none of which tells the engineer what he wants to know. However, using ENPORT to set up a local analog computer automatically permits the engineer to describe his problem in physical terms, and quickly scan the full variety of output data.

TERMINAL DESIGN CONSTRAINTS

Several restrictions were placed on the nature of the terminal, primarily to ensure easy access to components for maintenance, and partly to minimize cost. Among the restrictions were that:

1. The terminal equipment must be entirely local, communicating with the digital computer only by a single telephone line;
2. The memory unit must be compatible with a standard model 35 KSR teletype unit, which provides the keyboard and printer functions, as well as modulating and demodulating equipment for transmission and reception. In particular, this implies that the memory unit must operate at teletype-compatible speeds (as a

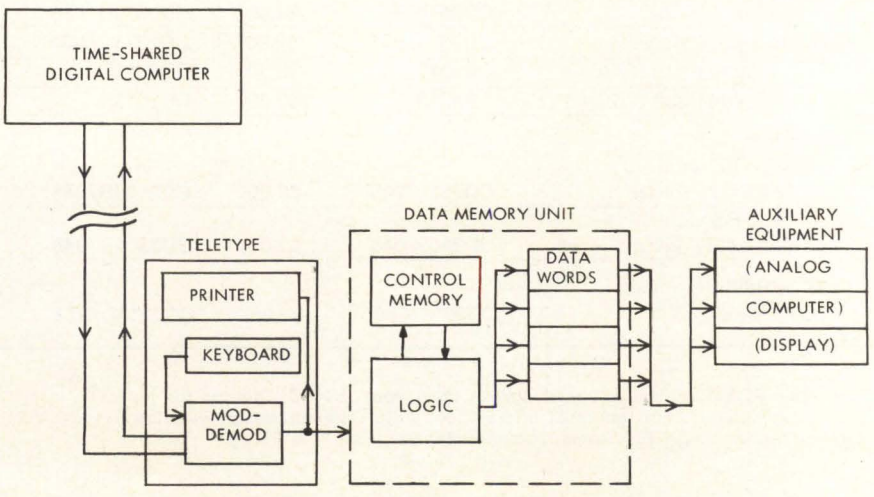


Figure 1. Major terminal components, showing information flow.

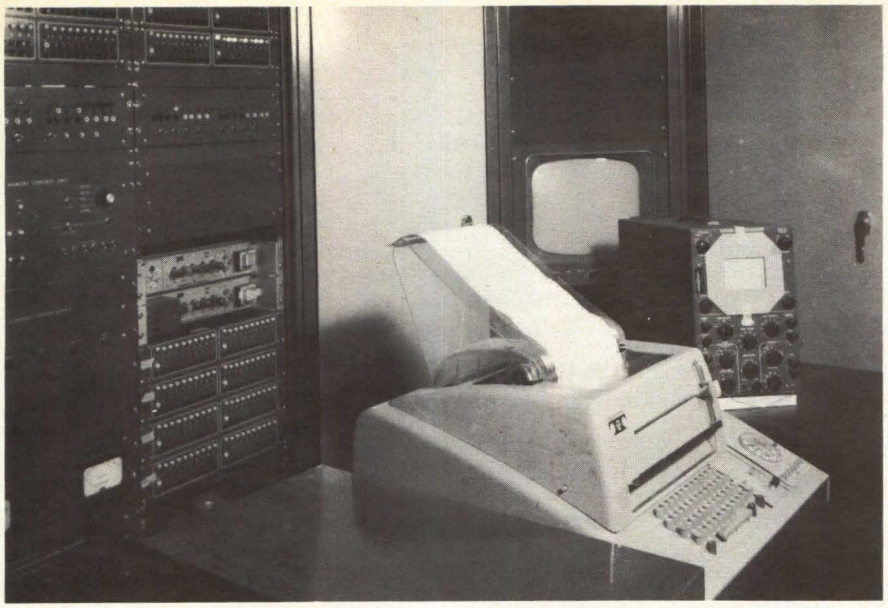


Figure 2. A remote terminal set-up.

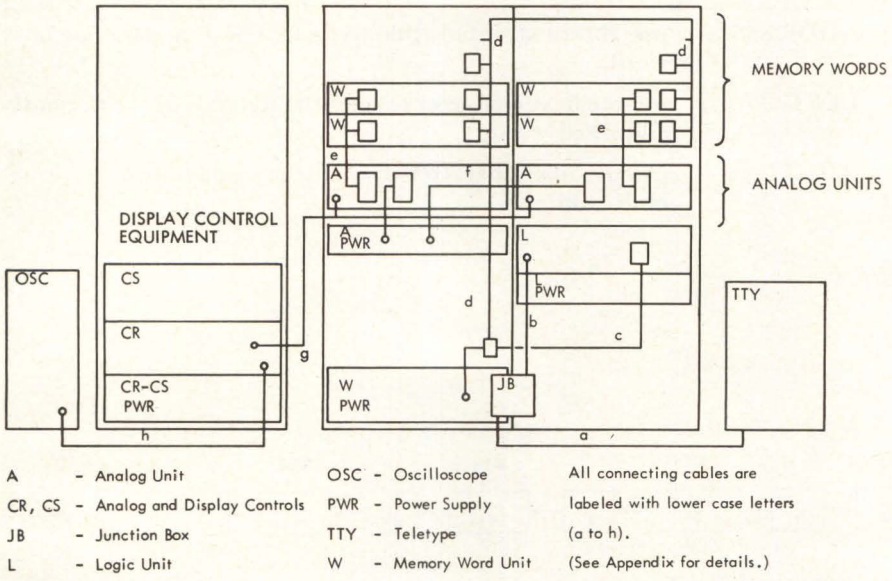


Figure 3. Diagram of terminal equipment, showing functional units and connections.

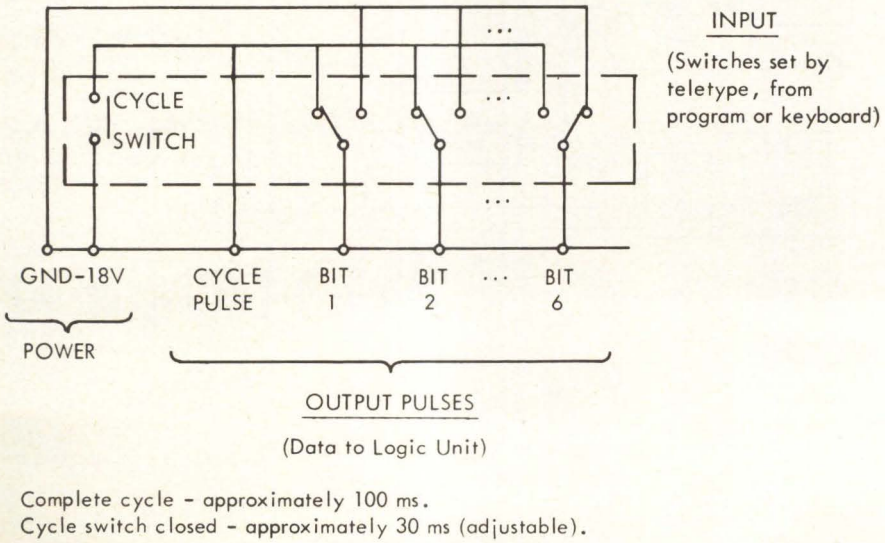


Figure 4. Input circuit from teletype to logic unit.

minimum), and from standard teletype code.

The device which meets the above restrictions is a local, low-speed memory unit that is independent of the type of computer. Teletypes are relatively inexpensive devices that are fairly well-suited to computer keyboard communication. Some indication of the cost of nonstandard parts for the memory is presented in Appendix A.

TERMINAL SYSTEM

The major components of the terminal system are shown in Figure 1 in terms of the information flow. Between the teletype and the digital computer there is a bilateral channel. The logic unit monitors all teletype communications, either received from the computer or generated by the keyboard, and responds to certain control characters. When the logic unit accepts data, they are used to fill the data memory. The memory contents may be used as required to control auxiliary equipment.

A picture of the terminal is shown in Figure 2. Figure 3 depicts the functional units and their connections. Also shown are components of an analog computer which is described in Section III. Appendix B describes the cable functions, and explains the addressing system built into cable "d".

Teletype Unit

The teletype is a modified Model 35 Keyboard-Send-and-Receive (KSR) with a set of read-out switches to make available eight bits of coded information per teletype character. Of the eight available bits, the logic and data memory use a subset of six bits, for which a full count (0 to 63 in binary form) exists. The maximum transmission rate for teletype characters is about ten per second.

The input circuit to the logic unit from the teletype is shown in Figure 4. This connection is cable "a" of Figure 3. Detailed information on standard teletype codes and cycle operation is available elsewhere[2]. It is possible to inhibit or enable the printing of information intended for the memory by use of the printer control characters of the

teletype. The memory may be loaded directly from the keyboard, which is useful for testing and manipulation purposes (e.g., even if the computer is not operating it is possible to load the memory).

Logic Unit

The logic unit receives its information from the teletype. Use of the information depends upon the logic unit state and the reception of several special-purpose machine commands listed in Table I.

The three machine command characters for the logic unit set the states START and STOP, and reset the cycle counter to ADDRESS. The cycle counter automatically advances the internal state from ADDRESS to LEFT to RIGHT (and so on), one step per set of input data. Figure 5 shows a schematic of the logic unit.

In addition to the teletype (external) input which is normally used, the unit is equipped with a set of toggle and control switches to permit the manual input of data. This feature has proven useful for test and debugging purposes. The front panel also has a set of lights which show the state of the logic unit, and the value of the current data word.

TABLE I

Machine Command	Function
START	enables the logic unit to process all subsequent input characters (stable until changed);
ADDRESS	sets the internal counter to interpret the following input character as an address;
STOP	ignores all subsequent input characters except START command (stable until changed).

After a START command has been received, the following internal machine states may exist:

Machine State	Description
ADDRESS	use the next input character to select a data memory word;
LEFT	use the next character to load the left half of the presently addressed word;
RIGHT	use the next character to load the right half of the presently addressed word.

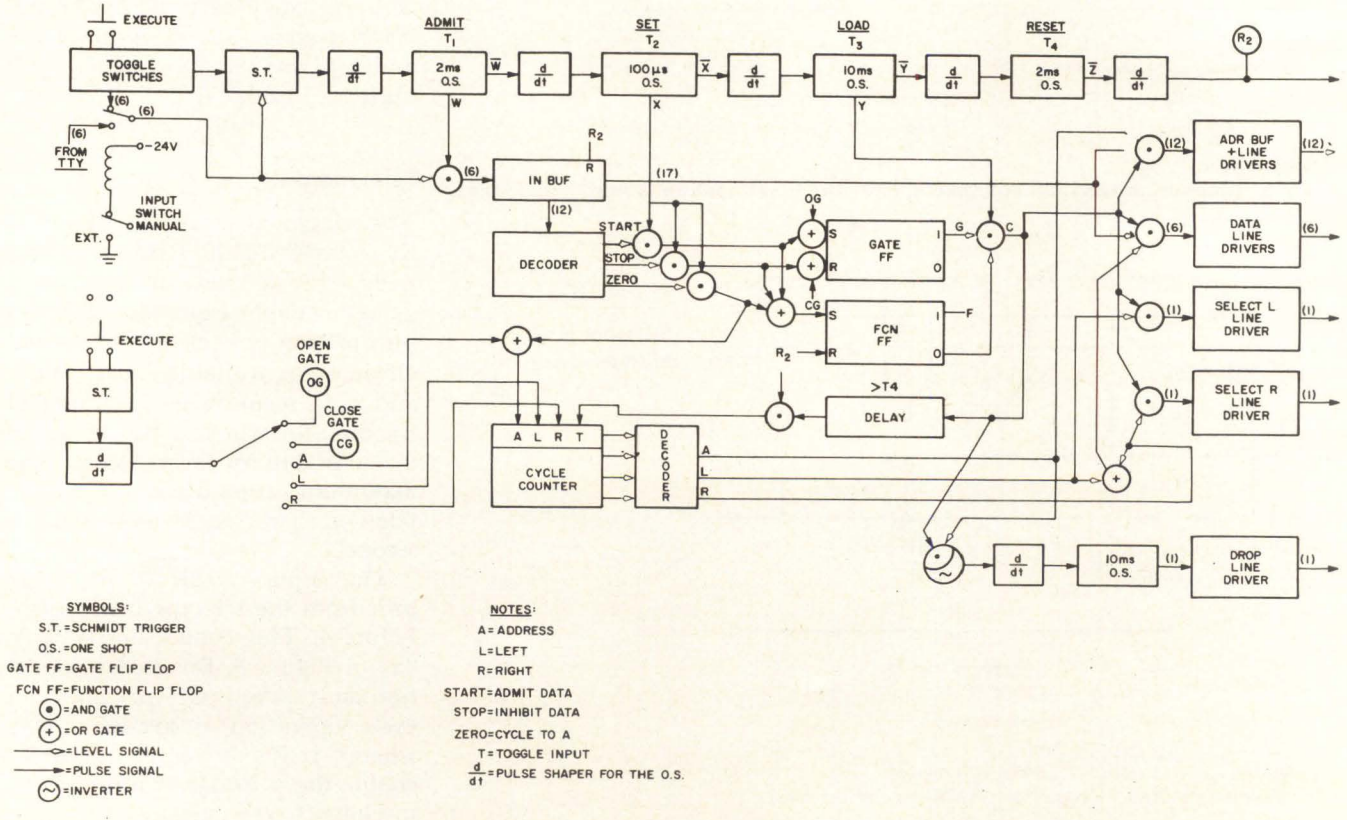


Figure 5. Logic unit schematic.

Data Memory

Each data memory word consists of ten bits — nine single-pole and one double-pole (or sign) bit. All bits are self-latching, as may be seen from Figure 6, which is a circuit diagram of a word of memory. When a word is addressed, its present contents are erased or dropped (i.e., the drop line is activated) in preparation for loading the left half (bits S, 1 to 4), and then the right half (bits 5 to 9).

Each memory chassis contains two words, whose addresses differ only in the final bit. All the memory word chassis are interchangeable, because the addressing is done by the wiring in cable "d" (see Figure 3). Although only thirty-two addressable words have been built, the system is designed to allow sixty-one or sixty-four words if the logic control characters are modified suitably. Figure 7 is a photograph of a memory chassis, indicating the common input block for the pair of words. The components are mounted on printed circuit boards.

Output from each word is available at the front panel as sets of terminal pairs, and in the back on a 24-pin connector. The state of each bit is shown by a light. A program written for the Project MAC IBM 7094 computer allows testing of the memory by an easily used set of commands. The author is Stephen Braunstein, an M.I.T. undergraduate student. Instructions for the use of the program are shown on the opposite page as part of an on-line interactive exchange between program and user. Because the basic program was written to operate on the M.I.T. time-sharing system, where certain modifications have been made to the teletype code and FORTRAN Monitor Systems (FMS), listings are not included here.

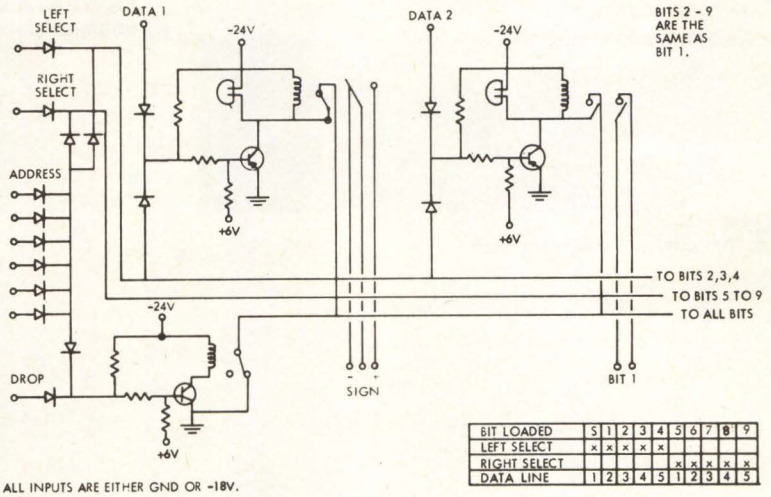
```
LOADGO MTEST TBIT
W 1008.5
 NEED BR      CLOCK
R 10.033+.833

USE BRCLOK
W 1008.9
EXECUTION.

'MEMORY' WILL LOAD, CLEAR, AND THEN LOAD MEMORY.
'CLEAR' WILL CLEAR MEMORY.
'RAMP12' WILL GENERATE RAMPS WITH INTEGRATORS 1 AND 2.
'RAMP34' WILL GENERATE RAMPS WITH INTEGRATORS 3 AND 4.
'SELF' WILL SET UP A FIRST ORDER SYSTEM FOR EACH INTEGRATOR.
'OSC12' WILL SET UP AN OSCILLATING SYSTEM WITH INTEGRATORS 1 AND 2.
'OSC34' WILL SET UP AN OSCILLATING SYSTEM WITH INTEGRATORS 3 AND 4.
'MEMO', WHERE '0' IS AN INTEGER 1-6, WILL PERFORM THE MEMORY TEST
    ON ONE OF THE SIX VERTICAL WORD BLOCKS.
'CLEARO', WHERE '0' IS AN INTEGER 1-6, WILL CLEAR ONE OF THE
    SIX VERTICAL WORD BLOCKS.


INITIAL CONDITIONS OF INTEGRATORS--
   INTEGRATOR      I.C
        1           +30
        2           +10          (This is reference information
        3           -10          for signals on the analog display.)
        4           -30


GO AHEAD..
```



BIT LOADED	S	1	2	3	4	5	6	7	8	9
LEFT SELECT	x	x	x	x	x					
RIGHT SELECT						x	x	x	x	x
DATA LINE	1	2	3	4	5	1	2	3	4	5

Figure 6. Schematic of a memory word part.

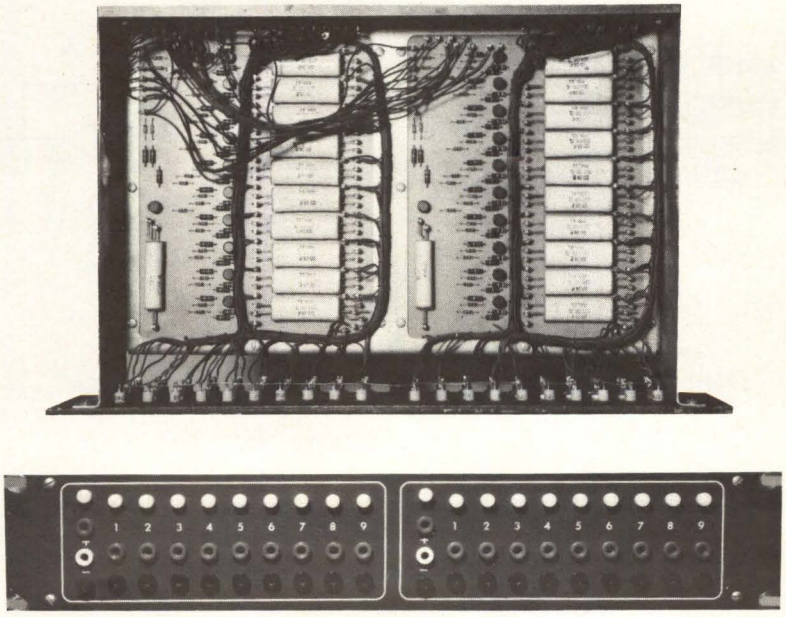
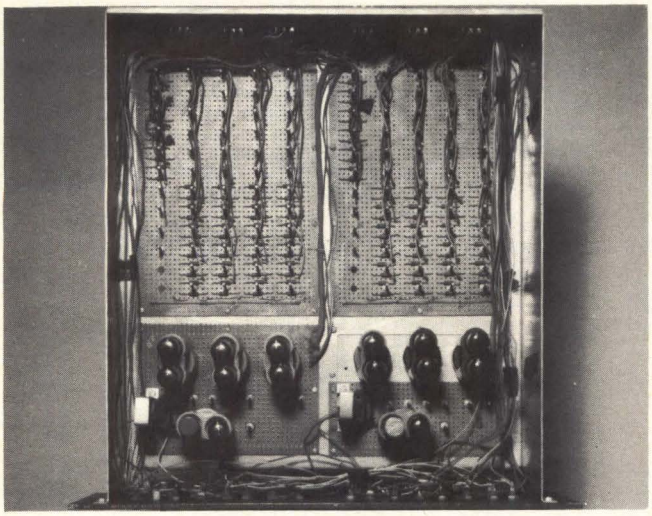


Figure 7. A local memory unit.

AN APPLICATION — AUTOMATED ANALOG COMPUTATION

This section describes using part of the memory to set up (program) an analog computer by means of a digital computer. As anyone who has worked with analog computers knows, the problems of set-up (e.g., wiring) and scaling (e.g., adjusting coefficients and integration rates)



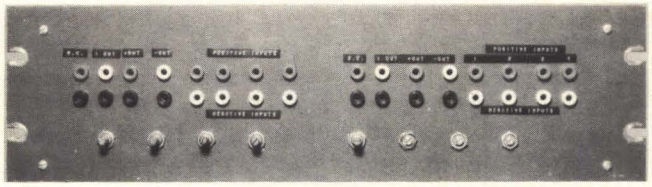


Figure 8. An analog integrator unit.

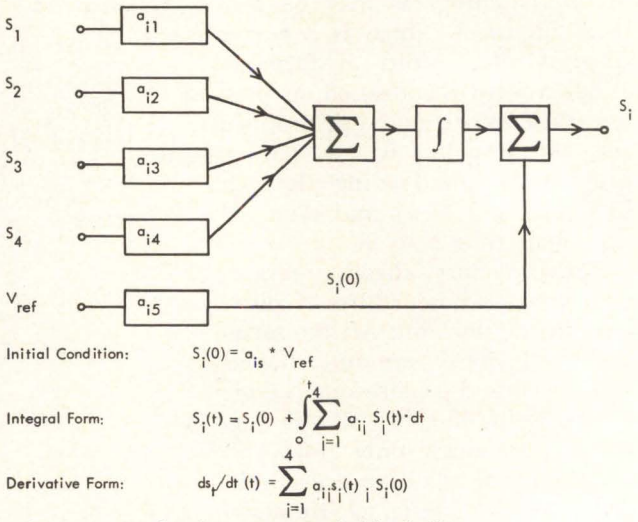
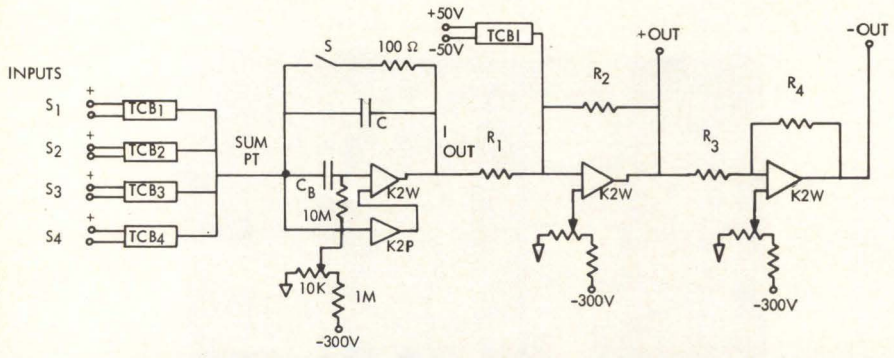


Figure 9. Analog integrator unit block diagram, and associated system equations.



C - integrating capacitor
C_B - blocking capacitor
R_1 to R_4 - inverter and adder resistors
TCB - transconductor block
TCBI - transconductor block for initial condition
S - the cycle switch (closed is reset to zero)

Amplifier functions:
First stage - integrator (K2P stabilized)
Second stage - adds the initial condition
Third stage - inverts the positive signal

Figure 10. Schematic of an integrator unit.

are not trivial; even when the problem is linear.

Purpose Of Analog Computer

The particular analog computer described in this article was used to simulate simple linear dynamic systems. The principal purpose was to display on a screen the wave forms of key variables in a rapid fashion. The remote terminal, equipped with such an automatic display facility, was used in an automated teaching experiment concerned with dynamic system behavior[6].

Analog Computer

The analog computer design was strongly influenced by the organization of the Philbrick K5-U Universal Linear Operator[4]. A fourth-order, completely coupled linear system can be simulated, by the use of four identical summing integrator units, whose coefficients and initial conditions are set by the (digital) program. The analog and display units are shown as terminal system components in Figure 3. In particular, cable "e" provides control data from the memory for the analog units, and cable "g" presents the variables to the display unit.

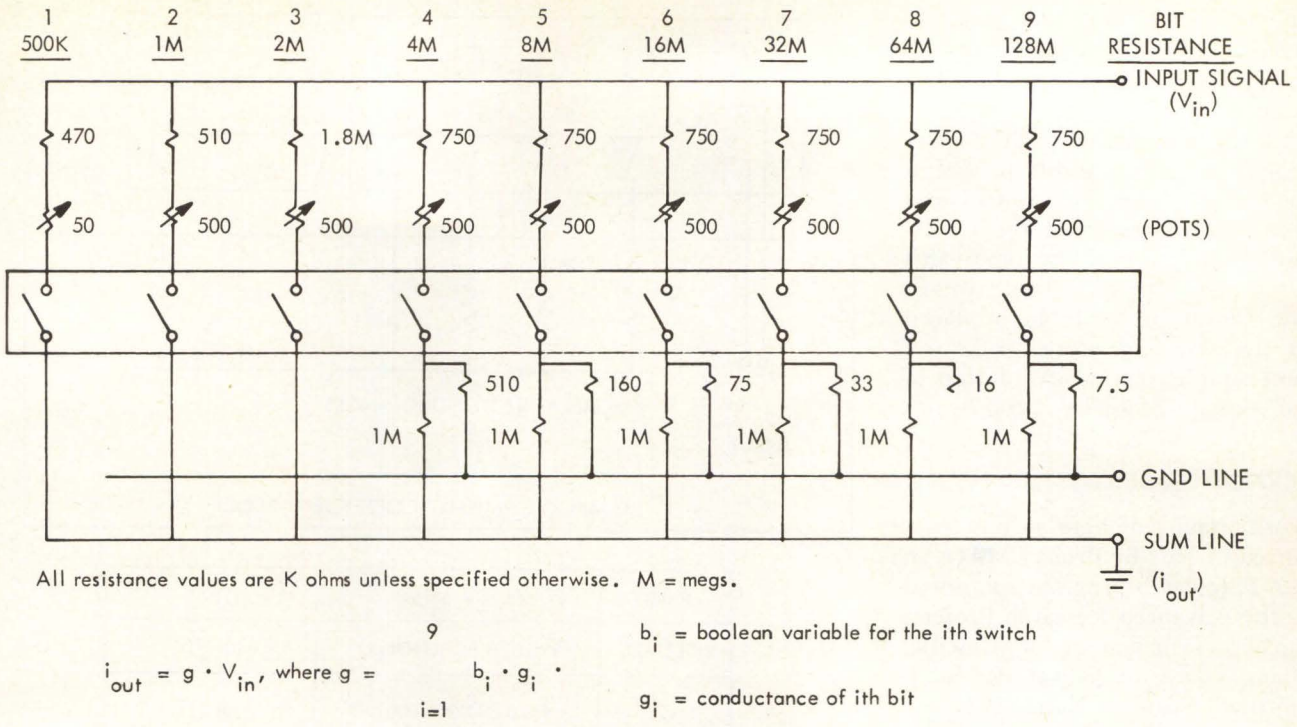


Figure 11. Schematic of a transconductor.

Figure 8 shows an analog integrator unit. Figure 9 shows a block diagram for an integrator unit, and indicates the form of system equations. Figure 10 is the integrator unit schematic, and Figure 11 gives details of a transconductor block, which is the memory-controlled coefficient.

The repetition rate was fixed at twenty cycles per second due to match the display equipment. However this rate may also be brought under program control by providing a switch-controlled set of integrating capacitors; an easy matter with the present equipment. This would extend the dynamic range of systems which could be simulated.

For the particular application described here, the memory words were connected to the analog units in a pattern which allowed direct observation of the analog computer set-up from the memory front panel lights. Each column of memory words contains the four input coefficients and, at the bottom, the weighting factor for an initial condition. A five-by-four block of memory words was wired as shown in Table II.

TABLE II

Variable	S_1	S_2	S_3	S_4
	A_{11}	A_{21}	A_{31}	A_{41}
	A_{12}	A_{22}	A_{32}	A_{42}
	A_{13}	A_{23}	A_{33}	A_{43}
	A_{14}	A_{24}	A_{34}	A_{44}
Initial Conditions	A_{15}	A_{25}	A_{35}	A_{45}

These coefficients refer to the equation in Figure 9.

The information transmitted by the digital program for display generation was near a minimum, since only structural and parametric data (plus initial conditions) had to be sent. A second-order system might require six data words plus a few control characters, and the computed time response could be displayed in less than four seconds real-time. A closely coupled third-order system might require about seven seconds to set up.

In the present version of the analog unit the memory output is wired directly into the transconductor units, as shown in Figure 12. This introduces wires of some two to three feet in length into the integration circuit. The distributed resistance and capacitance of these conductors is not negligible, and degrades accuracy considerably. Some tests which used the memory to set closely coupled transconductor relays (i.e., relays mounted right in the analog units) have indicated that excellent accuracy can be obtained by this modification.

Display Generation

The equipment used to multiplex the four analog signals for display is a standard Philbrick CR and CS display package[4]. This equipment superimposes the four input signals

on a time-voltage grid, generates synchronized computing control signals, and displays the results on an ordinary single-beam oscilloscope.

In the absence of such display equipment it is possible to design one's own computing control and display unit, and feed the results into a standard oscilloscope. In this latter case, the time and voltage line would probably be replaced by the standard scope grid, and some simple manual calibration of the display would be necessary.

ACKNOWLEDGMENTS

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The support of Philbrick Researchers, Inc., is also gratefully acknowledged.

REFERENCES

1. Karnopp, D. C. and R. C. Rosenberg, "Analysis and Simulation of Multiport Systems," *The M.I.T. Press,* Cambridge, Mass. 1968, Chapter 7.

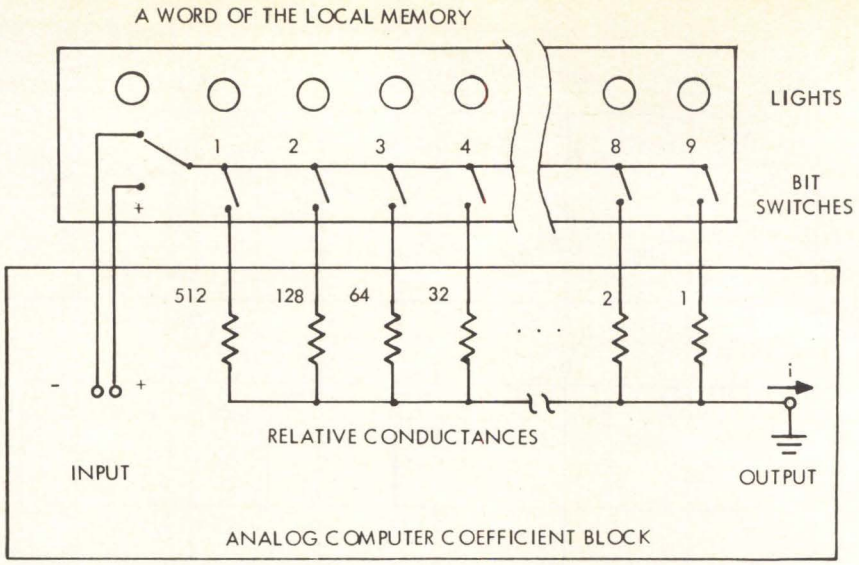
2. Technical Manual, Model 35 Keyboard Send-Receive (KSR) Teletypewriter Set, Bulletin 281B, Vol. 1, Teletype Corp., Skokie, Illinois, 1963.

3. Instruction Manual for 200-KC- S-PAC Digital Modules, Computer Control Company, Inc., Framingham, Mass., August 1963.

4. Philbrick Analog Applications Sheets-K5-U, KS-M, RC, CR, CS, R-500, G. A. Philbrick Researches, Inc., Dedham, Mass.

5. Paynter, H. M. and J. Suez, "Automatic Digital Setup and Scaling of Analog Computers," *ISA Transactions,* January 1964, pp. 55-64.

6. Rosenberg, R. C., "Computer-Aided Teaching of Dynamic System Behavior," PhD. Thesis, M.I.T. Mechanical Engineering Department, September 1965.



INPUT	DATA BITS	OUTPUT
VOLTAGE	SWITCH POSITIONS	CURRENT, i
s	0 000 000 000	0 s
s	1 000 000 001	-1 s
s	0 000 000 011	3 s
s	1 110 000 000	-768 s

Figure 12. Technique used to set analog coefficients.

Appendix A — Cost Information For Non-Standard Equipment

Memory Words — 34 units

Reed switches and coils	$813.00	
Lights and clips	264.50	
Circuit components	473.20	
Connectors	266.00	
Fabrication of chasses	271.50	
Printed circuit boards (drilled)	217.30	
Miscellaneous hardware	102.50	
TOTAL		$2,407.50*
Approximate cost per bit (34 at 10 = 340 bits)	$ 7.06	

Logic Unit

Standard CCC components and mounting racks	$1,300.75*
Power Supplies (2)	$ 235.04*
TOTAL	$3,943.29*

* Exclusive of labor for assembly of components.

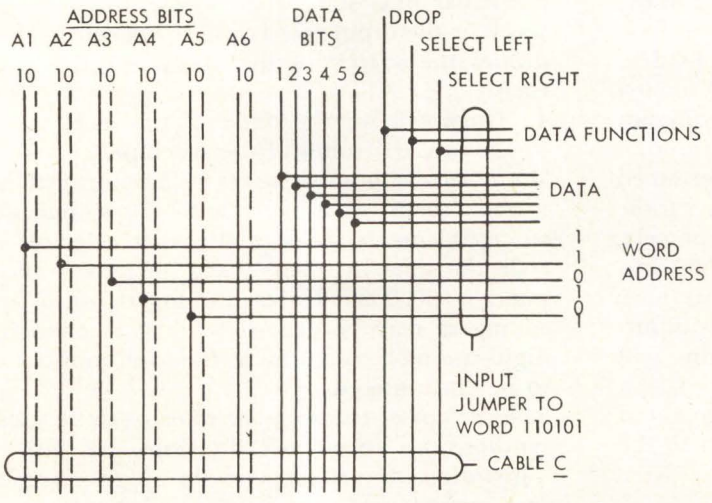
Continued

Appendix B — List Of Cable Functions

CABLE FUNCTION SUMMARY LIST

Cable	No. Lines	Signal Information
A	8	Six input character bits, cycle switch
B	8	Continuation of cable A
C	21	Six address bits; six address complements; six data bits; drop, select left, select right
D	21 + 3	Same signals as C, plus +6V, −18V gnd
E	12	Common pole connection; + and − sign bits; nine data bits
F	7	Analog unit power (± 30V, ±300V, 6.3 VAC, gnd)
G	5	Four analog output signals; relay control
H	4	Horizontal and vertical sweeps; flyback suppress; ground

DETAIL OF MEMORY CABLE C



* See Figure 3 for reference.

END

The method presented in this article will always yield a design solution to "any" sequential machine. When intuition in the design fails the designer will find this method to be an invaluable tool.

AN ALGORITHM FOR SEQ

This article aims to provide the engineer with a simple step by step procedure for the design of various digital subsystems. Subsequent to the statement of the design algorithm, two examples are given: a Modulo-7 counter using T flip flops as storage elements and a digit sequence detector using TTL logic blocks and SR flip flops.

An important feature of the algorithm is that the solution obtained for a problem is in no way dependent upon the "type" of logic utilized in the design. The solution obtained from the algorithm is in general form, and therefore whether the sequential circuit is configured using AND/OR, NAND or NOR logic incorporating discrete logic elements, RTL, DTL or TTL, etc. is left solely to the discretion of the circuit designer.

The term sequential machine is normally used to describe the class of networks whose output, at any instant of time, is determined not only by the present input to the machine, but also by the present internal states. The present state of the machine is determined by the "condition" of the memory elements of the machine, i.e. relays, flip flops, magnetic cores; namely, whether they are on or off, store a "1" or a "0", etc. It is to be noted that these memory elements have been placed into their present state by previous inputs and conversely the present input to the machine will determine the next state they will be in.

In general the synthesis (or design) of a sequential circuit consists of the following steps, as shown in the flow diagram of Figure 1.

Sequential Machine Synthesis Algorithm

1. Translation of the verbal problem into a *state diagram.*

A pictorial presentation is prepared which contains a number of circles, each of which indicates a state the machine may be in. These circles are numbered from 1 to n, where n indicates the number of possible conditions that may be encountered.

2. Reduction of the number of states and construction of a *reduced state diagram.*

Since the initial state diagram is merely a translation of the verbal statement of the problem, it does not necessarily yield an economical minimum state representation. A reduced state diagram is obtained by examining whether several states are equivalent to each other and may thus be merged into a single state.

3. Construction of the *reduced state table* from the reduced state diagram.

Since from this point on it is more convenient to work with tabular representations of the state diagram, a table is constructed which consists of one row per state, indicates the present state number in the first column, the "next state" number in the second or third column (depending whether one arrived in that particular next state when the input to the machine was 0 or the input was 1) and a last column which indicates the output of the machine corresponding to each state.

4. *Assignment of* the *states* of the memory elements to the internal states of the machine.

We normally number states in a manner that is convenient to us, such as 1, 2, 3 . . . n, but since our storage elements are normally binary devices we must code the state in binary form, such as 1 may correspond to 000, 2 may correspond to 001, etc. or any other coding as may be desired as long as enough binary digits are used to represent the total number of states to be encountered.

5. *Selection of* the *memory element* to be used in the synthesis, i.e. relays, S-R flip flops, J-K flip flop, etc. This selection will depend on speed considerations, cost, or apparent functional suitability.

6. Generation of the *excitation table* for the particular problem.

Subsequent to the state assignment it is known how many memory elements are required but it is not known how they are to be interconnected or "excited" to take on the various states in the proper sequence as required by the original statement of the problem. Entries are placed into the excitation table in accordance with the requirements of the "present state to next state transition" input requirements of the particular memory element selected.

UENTIAL CIRCUIT DESIGN

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G. W. JACOB

Sperry Gyroscope Division
Sperry Rand Corporation
Great Neck, N.Y. 11020

7. Generation of the memory element input or *excitation equations.*
The excitation table contains the information which is required to obtain a Karnough Map (or equivalent) logic minimization thus obtaining the excitation equation for each logic element.
8. Generation of *output equations.*
Since outputs are to be obtained only in particular states a similar process as in 7 is used to obtain the output equation.
9. Drawing of *circuit* configuration.

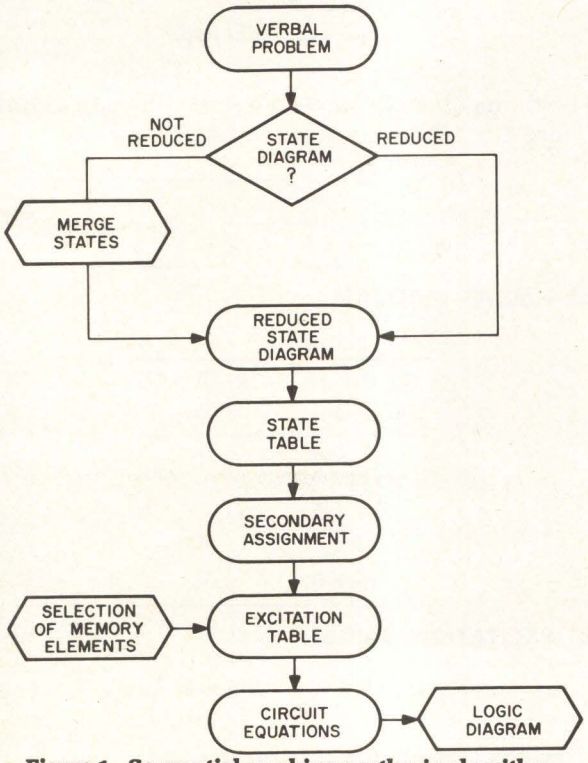


Figure 1. Sequential machine synthesis algorithm.

Example 1 — Modulo-7 Counter

The design of a digital counter is quite simple when the desired count is binary, i.e. 2,4,8. . .2^n. However when the count is not binary, the problem becomes much more involved due to the feedback requirements. Let us design a counter which gives a 1 output for every seven input pulses. This circuit is commonly referred to as a Modulo-7 counter. The block diagram and timing waveforms are shown in Figure 2.

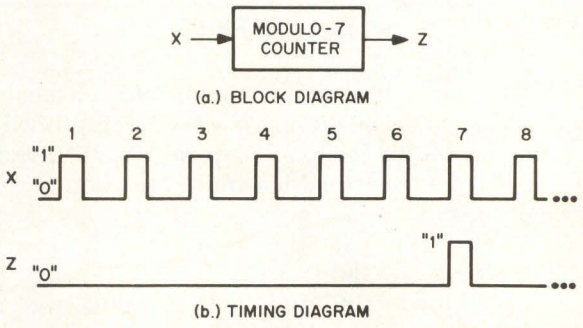


Figure 2. Modulo-7 counter.

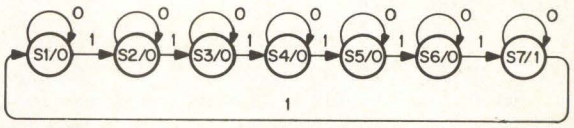


Figure 3. State diagram.

1. The symbology used in the state diagram is self-evident (see Figure 3). It is assumed that the machine is initially reset; that is, the machine is initialized to state S_1 on turn on. State S_1 is referred to as the present state for time t_0 and denoted P.S. The output associated with state S_1 is Z = 0 and denoted $S_{1/0}$. If the input, denoted X, is 0 the machine stays in state S_1 and its output denoted by Z is 0. However, an input X = 1 causes the machine to go to state S_2 again with an output of 0. The remainder of the states follow in this manner until state S_7 to which we associate an output of 1. Note that this machine is commonly referred to as a Moore machine.[2]
2. Reduction of states of state diagram. Two states Si and Sj are equivalent and could therefore be reduced to one equivalent state if and only if BOTH states Si and Sj will go to the next state Sm for input X = 0

and state Sn for input X = 1 and the outputs associated with these states are unchanged. In this case, however, no further reductions exist.

In general, the reduces state diagram is immediately obtainable by careful construction of the diagram. It is important to realize that minimizing the number of states of a sequential machine, in general reduces the number of memory elements required in the synthesis; i.e. a nine state machine requires four memory elements while an eight state machine requires three memory elements.

3. Construction of state table follows directly from the reduced state diagram. We therefore obtain the state table shown in Figure 4.

Present State	Next State X = 0	Next State X = 1	Output Z
1	1	2	0
2	2	3	0
3	3	4	0
4	4	5	0
5	5	6	0
6	6	7	0
7	7	1	1

Figure 4. State table.

4. Assignment of the states of the memory elements to the internal states of the machine is accomplished by use of Figure 4. In general, independently distinguishing S state of a sequential machine requires n memory elements where

(1) $S = 2^n$ or,
$n = [\log_2 S]$, and [ ] is used to indicate the largest integer greater than or equal to $\log_2 S$.

In our example, we get:

(2) $n = [\log_2 7]$ or
but $\log_2 7 = 2.84$
$\therefore n = 3$

The three (3) memory elements required for the realization constitute eight (2^3) independent states. The secondary assignment table is shown in Figure 5. Each of the seven (7) present states were coded as shown. Where these states appear in the N.S. column, the corresponding coded state was written.

This secondary assignment was made in an arbitrary manner. There are many other possible assignments, and in fact for this problem there exists 8! ($\approx 4 \times 10^4$) such assignments. The method of assigning the binary variable codes to the internal states of the machine has been one of the major analysis problems in the design of sequential machines. The selection of the codes, in general, result in the varying complexity of the circuits required for realization.

It has been shown by Hartmanis and Stearns[3,4] that the theory of partitions is of great significance in the selection of the secondary assignment; although the realization may not yield the minimum realization. For the purpose of this article, however, only arbitrary assignments are considered.

Present State P.S.	Next State N.S. X = 0	Next State N.S. X = 1	Output Z
1 → 000	000	001	0
2 → 001	001	010	0
3 → 010	010	011	0
4 → 011	011	100	0
5 → 100	100	101	0
6 → 101	101	110	0
7 → 110	110	000	1

Figure 5. Secondary assignment.

5. Selection of the memory elements to be used in the synthesis is now of importance. Whether a relay or some special type of flip flop be used is usually predicated by speed of the circuit or some other physical constraint. The different types of memory elements most commonly used are discussed below.

a) Toggle or Trigger Flip Flop

The toggle flip flop is shown pictorially in Figure 6. The T flip flop, as it is commonly referred to, has one input and two outputs. Its operation is that of a binary counter; that is, it changes state (or toggles) for each successive "1" input.

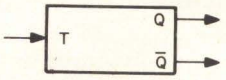
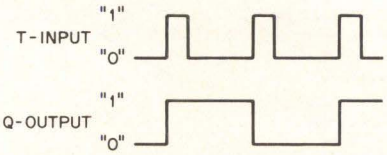


Figure 6. T flip flop.

The timing diagram and excitation table are shown in Figure 7.



(a) TIMING DIAGRAM

TO CHANGE Qn → Qn + 1	REQUIRED INPUT T
0 → 0	0
0 → 1	1
1 → 1	0
1 → 0	1

(b) EXCITATION TABLE

Figure 7. T flip flop.

From the above table we find that

(4) $Qn+1 = T\,\overline{Q}n + \overline{T}\,Qn$ which represents the excitation equation of the T Flip Flop

b) Set Reset Flip Flop

The S-R flip flop, as it is commonly referred to, has two inputs and two outputs as shown in Figure 8. The

S-R flip flop is a basic multivibrator; a "1" input on the S input causes the output Q to "set to" a "1", while a "1" input on the R input causes the Q output to "reset to" a "0". The timing diagram and truth table is shown in Figure 9 while the excitation table is shown in Figure 10.

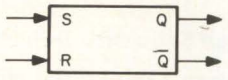
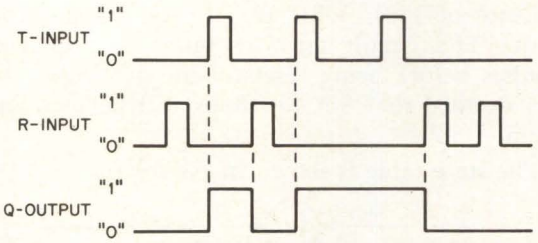


Figure 8. S-R flip flop.



(a) TIMING DIAGRAM

S	R	Qn	Qn + 1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	?
1	1	1	?

(b) TRUTH TABLE

Figure 9. S-R flip flop.

From the truth table we note that

(5) $Qn+1 = \overline{S}\,\overline{R}\,Qn + S\,\overline{R}\,QN + S\,\overline{R}\,\overline{Q}n$

or (6) $Qn+1 = \overline{R}\,Qn + S\,\overline{R} = \overline{R}\,(Qn + S)$

and that a S=R=1 condition is prohibited; that is, the state of the flip flop for this condition is undermined. The excitation function is now determined.

TO CHANGE Qn → Qn + 1	REQUIRES INPUTS S	R
0 → 0	0	ø*
0 → 1	1	0
1 → 1	ø	0
1 → 0	0	1

*INDICATES DONT CARE STATE

Figure 10. S-R flip flop excitation table.

c) J-K Flip Flop

The J-K flip flop shown pictorially in Figure 11 has essentially the same characteristics as that of the S-R flip flop with the exception of the J=K=1 case. The truth table and excitation table is shown in Figure 12.

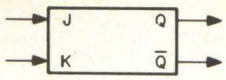


Figure 11. J-K flip flop.

J	K	Qn	Qn+1	
0	0	0	0	INHIBIT
0	0	1	1	
0	1	0	0	STEER
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	1	TOGGLE
1	1	1	0	

(a) TRUTH TABLE

TO CHANGE Qn	Qn+1	REQUIRED INPUT J	K
0	0	0	ø
0	1	1	ø
1	1	ø	0
1	0	ø	1

(b) EXCITATION TABLE

Figure 12. J-K flip flop.

For our example let us choose the T Flip Flop since these are the simplest and lowest cost counter elements available and are very suitable for the simple modulo 7 counter.

6. Generation of the excitation table for this particular problem is obtained by utilizing the excitation table for the T Flip Flop, Figure 7(b), in conjunction with the secondary assignment table, Figure 5. The excitation table for this problem is shown in Figure 13.

Present State			Next State X = 0(X)			X = 1(X)			Output
Q_1	Q_2	Q_3	T_1	T_2	T_3	T_1	T_2	T_3	Z
0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	1	1*	0
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	1	1	0
1	1	0	0	0	0	1	1	0	1
1	1	1	ø	ø	ø	ø	ø	ø	ø

Figure 13. Excitation table.

* For example, this term is obtained by considering that in the table of Figure 5

P.S. $Q_1\ Q_2\ Q_3$ = 0 0 1 goes to N.S. $Q_1\ Q_2\ Q_3$ = 0 1 0 for an input of X = 1.

For this to happen then:

Q_1 goes from 0 to 0; requires $T_1 = 0$

Q_2 goes from 0 to 1; requires $T_2 = 1$

Q_3 goes from 1 to 0; requires $T_3 = 1$

Therefore $T_1\ T_2\ T_3$ is written under the X column

0 1 1

7. Generation of the memory element input equations is obtained by generating the three Karnaugh maps "contained" in Figure 14(a), (b), (c). The maps and

their equations are now obtained.

8. Generation of the output equation is obtained by generating the Karnaugh map as shown in Figure 14(d).

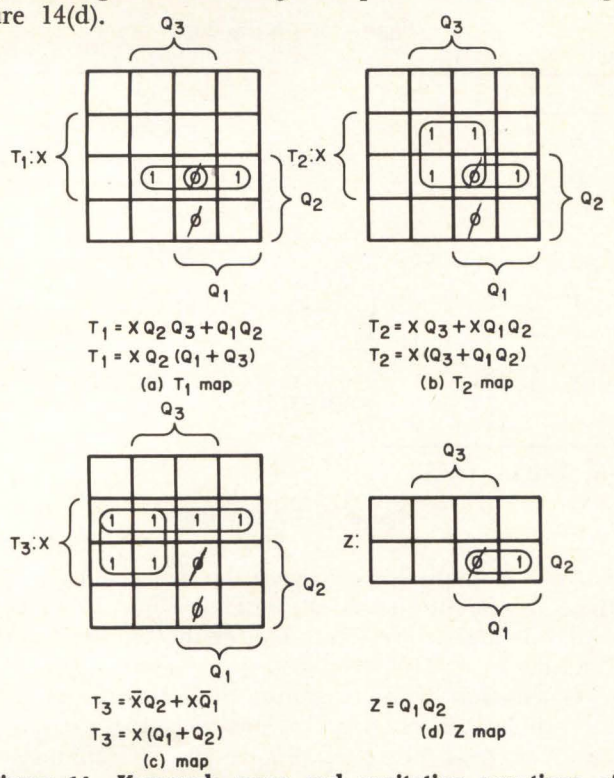


Figure 14. Karnaugh maps and excitation equations of example.

9. The circuit may then be drawn from the equations previously developed. For this problem, the circuit is:

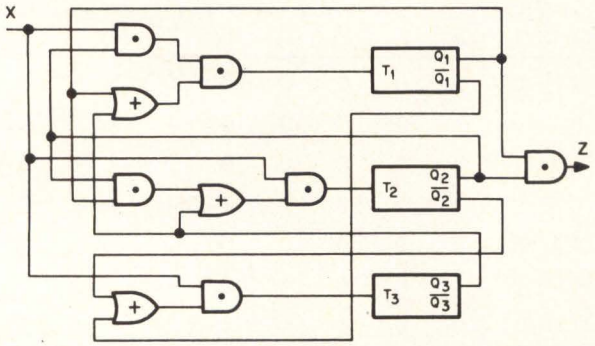


Figure 15. Logic diagram of modulo-7 counter utilizing DTL micrologic.

Notice that the circuit of Figure 15 is configured in general form, i.e. AND/OR logic with no specific logic type indicated. The circuit could be configured utilizing NAND or NOR logic with either discrete, RTL, DTL or TTL micrologic by making the appropriate circuit equation transformations. An example of this is covered in Example 2.

Furthermore, the circuit shown in Figure 15 can be considered as an *asynchronous pulsed sequential circuit*. In an asynchronous pulsed sequential circuit only the presence of an input pulse, X = 1, causes the circuit to change state. Therefore the presence of an input pulse is recognized by the circuit, while the absence of the input pulse is not. With no input pulse present, the circuit must remain in its present state.

Another type of sequential circuit commonly designed is the *synchronous sequential circuit*. In a synchronous sequential circuit it is necessary to be able to determine at specified instants of time (at those instances in which clock pulse occurs) whether the input(s) is a one or a zero. An example of a different sequential circuit, which in this case happens to be synchronous, is shown in Example 2.

Example 2 — Digit Sequence Detector

It is desired to design a sequential circuit in accordance with the following specifications:

An output of "1" is to be generated whenever the sequence of 1101, 1001, 1011 or 1111 appear at the input. The circuit must examine all sequences of 4 pulses before being reset on the 5th pulse. It has been decided that S-R flip flops will be used in this design.

1. The state table is shown in Figure 16.

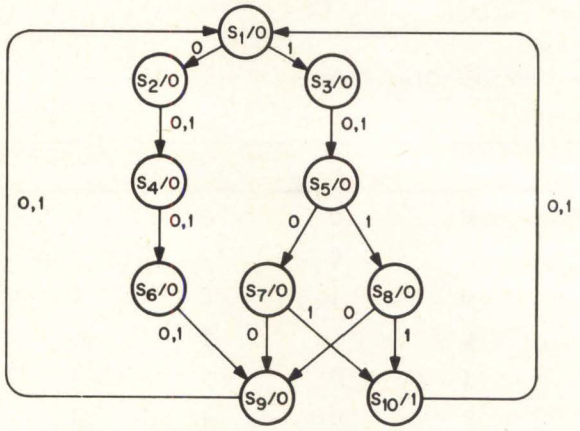


Figure 16. State diagram.

2. The above state diagram is not in reduced form. We note that states S_7 and S_8 are equivalent and as per the Algorithm are merged into a single state. The reduced state diagram is shown in Figure 17.

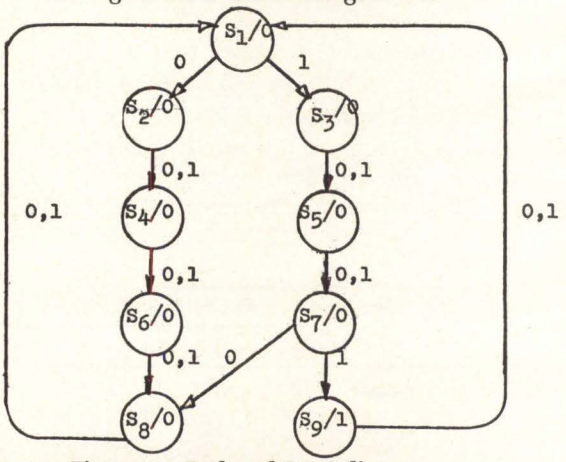


Figure 17. Reduced State diagram.

3. The reduced state table is now developed and shown in Figure 18.

4. The secondary assignment table is shown in Figure 19.

5. The problem set forth specified the use of S-R flip flops.

6. The excitation table shown in Figure 20 is derived by utilizing Figures 10 and 19.

7. The excitation equations are developed from Fig-

Present State				Next State																
				X = 0								X = 1								
Q_1	Q_2	Q_3	Q_4	S_1	R_1	S_2	R_2	S_3	R_3	S_4	R_4	S_1	R_1	S_2	R_2	S_3	R_3	S_4	R_4	Z
0	0	0	0	0	ø	0	ø	0	ø	1	0	0	ø	0	ø	1	0	0	ø	0
0	0	0	1	0	ø	0	ø	1	0	ø	0	0	ø	0	ø	1	0	ø	0	0
0	0	1	0	0	ø	1	0	0	1	0	ø	0	ø	1	0	0	1	0	ø	0
0	0	1	1	0	ø	1	0	0	1	ø	0	0	ø	1	0	0	1	ø	0	0
0	1	0	0	0	ø	ø	0	1	0	0	ø	0	ø	ø	0	1	0	0	ø	0
0	1	0	1	0	ø	ø	0	1	0	ø	0	0	ø	ø	0	1	0	ø	0	0
0	1	1	0	0	ø	ø	0	ø	0	1	0	1	0	0	1	0	1	0	ø	0
0	1	1	1	0	ø	0	1	0	1	0	1	0	ø	0	1	0	1	0	1	0
1	0	0	0	0	1	0	ø	0	ø	0	ø	0	1	0	ø	0	ø	0	ø	1
1	0	0	1	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	0	1	0	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	0	1	1	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	1	0	0	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	1	0	1	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	1	1	0	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø
1	1	1	1	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø

Figure 20. Excitation table.

Present State	Next State		Z
	0	1	
1	2	3	0
2	4	4	0
3	5	5	0
4	6	6	0
5	7	7	0
6	8	8	0
7	8	9	0
8	1	1	0
9	1	1	1

Figure 18. State table.

Present State	Next State		Z
	0	1	
1 → 0000	0001	0010	0
2 → 0001	0011	0011	0
3 → 0010	0100	0100	0
4 → 0011	0101	0101	0
5 → 0100	0110	0110	0
6 → 0101	0111	0111	0
7 → 0110	0111	1000	0
8 → 0111	0000	0000	0
9 → 1000	0000	0000	1

Figure 19. Secondary assignment table.

ure 20. Note that the equations may be derived by performing Karnaugh map combinations directly from the table.

The equations are:

$S_1 = X\,Q_2\,Q_3\,\overline{Q}_4$

$R_1 = Q_1$

$S_2 = \overline{Q}_2\,Q_3$

$R_2 = X\,Q_2\,Q_3 + Q_2\,Q_3\,Q_4 = Q_2\,Q_3\,(X + Q_4)$

$S_3 = \overline{Q}_2\,\overline{Q}_3\,Q_4 + X\,\overline{Q}_1\,\overline{Q}_2\,\overline{Q}_3 + Q_2\,\overline{Q}_3$

$R_3 = \overline{Q}_2\,Q_3 + X\,Q_3 + \overline{X}\,Q_3\,Q_4$

$S_4 = \overline{X}\,\overline{Q}_1\,\overline{Q}_2\,\overline{Q}_3 + X\,Q_2\,Q_3\,\overline{Q}_4$

$R_4 = Q_2\,Q_3\,Q_4$

8. The output equation is likewise derived by performing the Karnaugh map combinations directly from the table of Figure 20. The equation is

$Z = Q_1$

The transformation of these equations to ones which lend themselves to a NAND synthesis is quite simple. For example, consider the following equation in the sum of products form

(1) $R_2 = X\,Q_2\,Q_3 + Q_2\,Q_3\,Q_4$

By DeMorgan's theorem

(2) $\overline{S}_1 = \overline{X\,Q_2\,Q_3 + Q_2\,Q_3\,Q_4}$

$= (\overline{X\,Q_2\,Q_3})\,(\overline{Q_2\,Q_3\,Q_4})$

$= (\overline{X} + \overline{Q}_2 + \overline{Q}_3)\,(\overline{Q}_2 + \overline{Q}_3 + \overline{Q}_4)$

Then (3) $R_2 = \overline{(\overline{X} + \overline{Q}_2 + \overline{Q}_3)\,(\overline{Q}_2 + \overline{Q}_3 + \overline{Q}_4)}$

Utilizing the Sheffer stroke notation for NAND logic we know in general that

(4) a) $A/B/C = \overline{A \cdot B \cdot C}$

where / indicates the NAND function

b) $A/B/C = \overline{A} + \overline{B} + \overline{C}$

Incorporating the identity of 4a into (3) yields

(5) $R_2 = (\overline{X} + \overline{Q}_2 + \overline{Q}_3)\,(\overline{Q}_2 + Q_3 + \overline{Q}_4)$.

Now incorporating 4b into equation 5 yields

(6) $R_2 = (X/Q_2/Q_3)\,(Q_2/Q_3/Q_4)$

Therefore, upon comparing Equations (1) and (6) it is quite evident that the transformation of an equation in the sum of products form to a NAND equation merely involves the replacing of both the AND and OR function with the NAND function, while all the literals remain *unchanged.* A generalized transformation equation may be written as follows:

(7) f_{SUM} (X1,X2 . . . Xn,+,·) => f_{NAND} (X1,X2, . . . Xn,/,/) or f1 = X11,X12 . . . X1n + X21,X22 . . . X2n + . . . + Xm1,Xm2 . . . Xmn

is transformed to

f1 = (X11/X12/ . . . /X1n)/(X21/X22/ . . . /X2n)/ . . . (Xm1/Xm2/ . . . Xmn)

The logic diagram for the above transformation is shown in Figure 21.

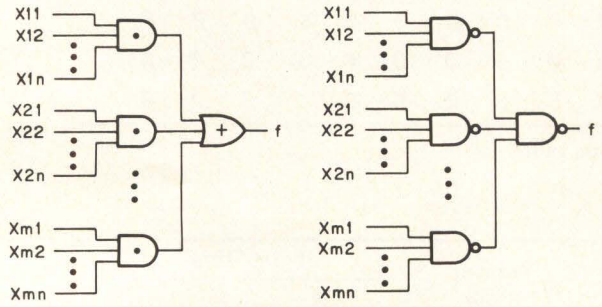


Figure 21. NAND transformation.

In a similar manner, it could be shown that there is a similar transformation between a product of sum form of an equation, and a NOR equation. The generalized transformation equation is

(8) f_{PROD} (X1,X2, . . . ,Xn,·,+) => f_{NOR} (X1,X2, . . . ,Xn,↓,↓)

where ↓ indicates the NOR function, or

f1 = (X11 + X12 + . . . + X1n) (X21,X22, . . . X2n) . . . (Xm1,Xm2 . . . Xmn)

is transformed to

f1 = (X11 ↓ X12 ↓ . . . X1n) ↓ (X21 ↓ X22 ↓ . . . ↓ X2n) ↓ . . . ↓ (Xm1 ↓ Xm2 . . . Xmn)

The logic diagram for this transformation is shown in Figure 22.

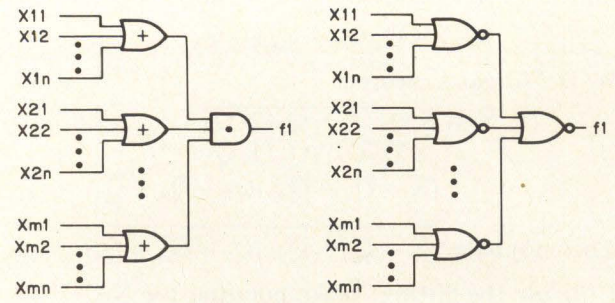
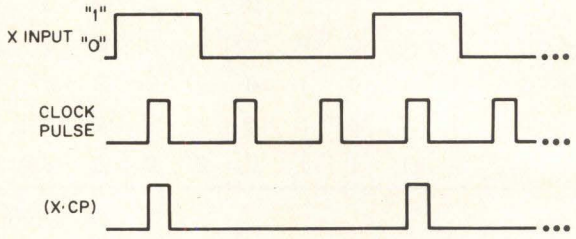


Figure 22. NOR transformation.

9. Utilizing the equations of parts 7 and 8 and the transformation property to NAND logic we can design the logic network to this example. The logic circuit is shown in Figure 23. A typical microcircuit card which contains the number of microcircuits required for this application is shown in Figure 24. For this example Texas Instrument Series 54 TTL microcircuits were used. The sequential circuit design is shown in Figure 23.

It should be observed that a clock pulse (C.P.) input has been added to some of the gates in the logic realization of this example as shown in Figure 23. In the design of *synchronous sequential circuits,* the clock pulses provide the tool for determining the state of the input for every instant of time, i.e. whether the input is a zero or a one. The clock pulse thereby allows the circuit to recognize the difference between a zero input and no input by its coincidence with the clock pulse.

If, for example, the input X is to represent the sequence 10011 . . . as shown below,



then clearly the (X·CP) waveform eliminates the error of recognizing the no data time as a zero or rather the input sequence to be X = 10101. . . .

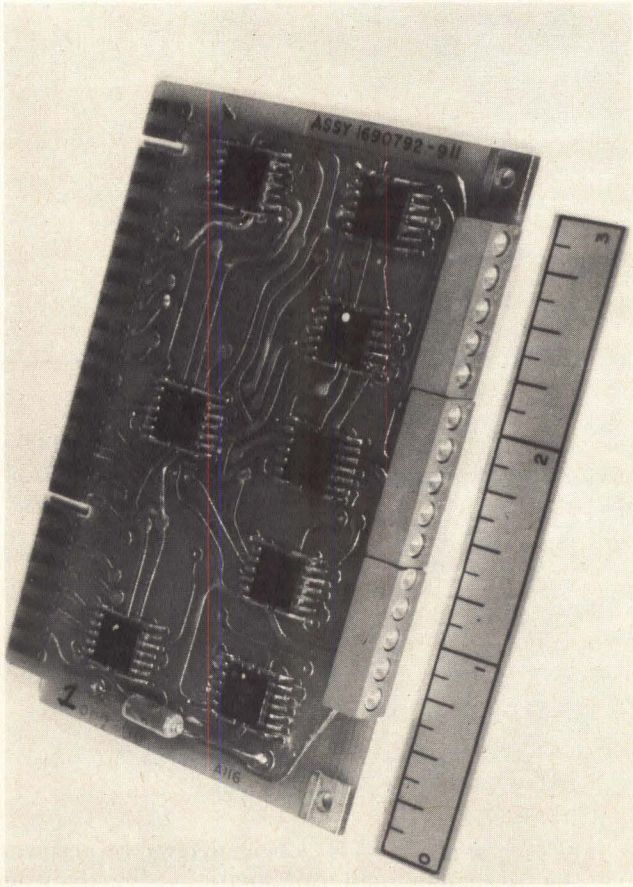


Figure 24. Typical microcircuit card.

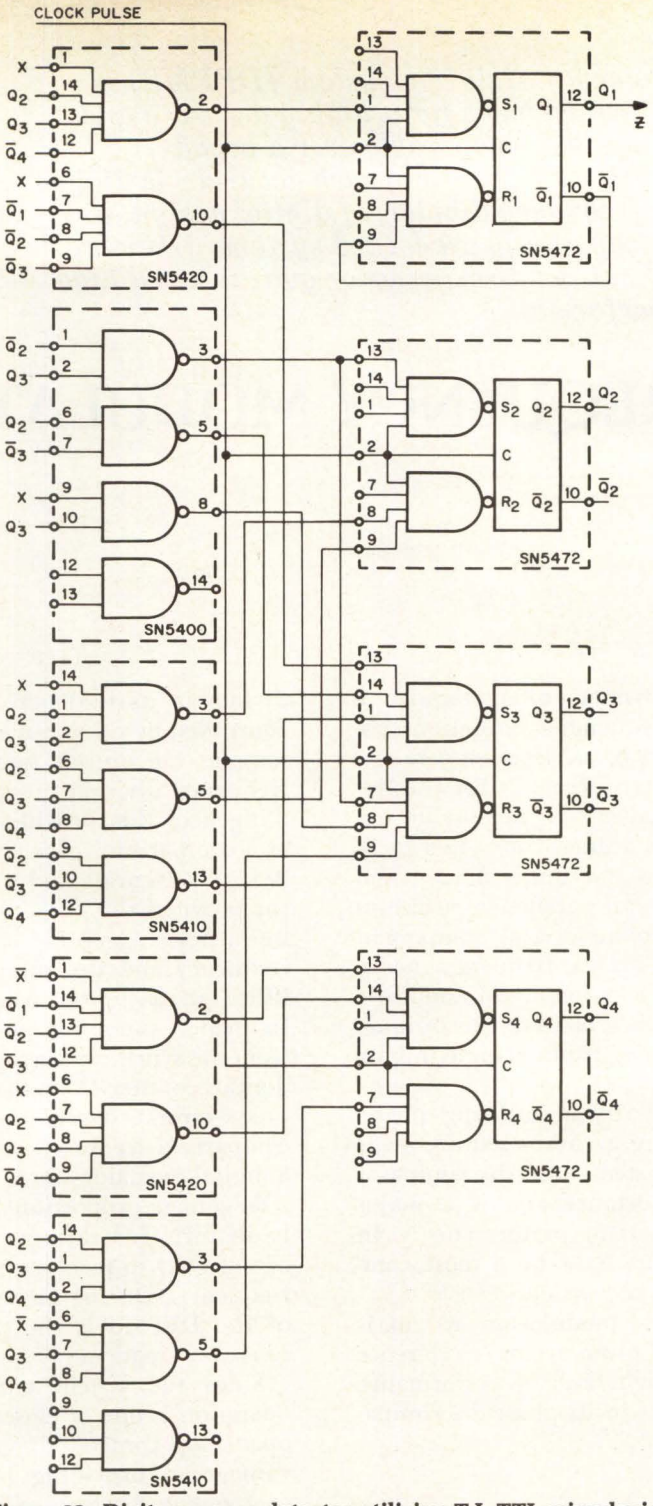


Figure 23. Digit sequence detector utilizing T.I. TTL micrologic.

Notes: All unused inputs are tied to +V, all pin 4's to +V, all pin 11's to GND

Conclusions

The solution to these examples are not unique and by no means do the authors claim them to be optimum. Reiterating, the selection of the secondary assignment will largely determine the complexity of the logic circuit. In addition, the choice of secondary elements (T flip flop vs J-K flip flop, etc.) will predicate the circuits complexity, too.

The method presented in this paper, however, will always yield to design solution for "any" sequential machine. And, when intuition in the design fails, the designer of sequential logic networks will find this method an invaluable tool.

REFERENCES

1. Jacob, G. W. and Ettinger, M. A., *Switching Theory and Logic Design,* a text based on lecture notes prepared by the authors which includes both basic theory and state-of-the-art miscrocircuit logic design techniques of combinational and sequential switching circuits — to be published.

2. Moore, E. F., *Gedanken-Experiment on Sequential Machines,* Automatic Studies, Annals of Mathematics Studies No. 34 pp 129-153, Princeton University Press, N. J., 1956.

3. Hartmanis, J., *On the State Assignment Problem for Sequential Machines I, IRE Transactions on Electronic* Computers, Vol. EC-10, No. 2 pp 157-165, June 1961.

4. Hartmanis, J. and Stearns, R. E., *Algebraic Structure Theory of Sequential Machines,* Prentice-Hall, Inc., 1966.

A digital feedback frequency modulation system (DFFMS) is presented to satisfy the requirement for a highly accurate and stable FM subsystem that must be operable over a broad frequency range. The method of attaining such accuracy is unique in that a programmable frequency divider, of digital design, is utilized in the feedback loop of a phase-locked system. Utilizing digital circuitry throughout the discriminator guarantees a high level of overall system performance.

A FREQUENCY MODULATION SYSTEM

Modern signal processing systems often require a highly accurate and stable frequency modulation subsystem that is operable over a broad frequency range. If the accuracy and stability requirements for the frequency modulator are not severe, an acceptable approach would be to employ a voltage-controlled oscillator (VCO) designed to be sufficiently linear and sufficiently independent of circuit parameter variations caused by changes in environment and component aging. If these requirements for the frequency modulator are severe, however, it becomes economically advisable to employ phase-locked oscillator techniques to derive the required frequency from a single, highly accurate and stable source.[1]

In recent years, the popularity of utilizing phase-locked systems to satisfy severe accuracy requirements has increased.[2,3,4] In such systems, the discriminator operation is of utmost importance and is a major contributor to the overall system performance.[5] In the past, analog discriminators have been most commonly employed in phase-locked systems.[6,7,8]

In this article, a frequency modulation system is discussed that is phase-locked to an accurate reference and achieves an extremely high level of performance by utilizing digital techniques in its phase-discriminator design.

SYSTEM CONCEPT

The digital feedback frequency modulation system (DFFMS), is an original method of attaining extremely high accuracy in frequency modulation systems. The proposed system is composed of a conventional VCO and a feedback loop containing a programmable digital phase discriminator. The programmable digital feedback is the unique feature of this design and is the mechanism that permits the high accuracy frequency modulation to be realized.

A functional block diagram of the DFFMS is shown in Figure 1. It varies from the basic automatic frequency control (AFC) system[9] in that a programmable frequency divider in the feedback loop serves as the signal input; i.e., the basic AFC system employs unity feedback whereas the DFFMS employs a frequency divider in its feedback loop, the divisor of which is controlled by the input signal. Essentially, the divider samples the output frequency and, through varying frequency division, precisely removes the desired intelligence; this provides a correction signal for use as a comparison frequency in the phase discriminator. A highly accurate and stable crystal-controlled oscillator provides the phase discriminator with a reference frequency. Algebraic combination of the reference frequency and the comparison frequency is accomplished in a digital synchronizer, which serves as a frequency summing point. Phase error increments from the synchronizer are integrated in a bidirectional digital counter. As the digital counter tracks the phase error between the reference frequency and the comparison frequency, the counter stage is sensed by a digital-to-analog (D/A) converter, thereby generating a dc voltage proportional to phase error. This voltage is, in turn, fed through a filter to the control input of the VCO to produce a change in the system output frequency. During phase-locked operation, the output of the DFFMS is the programmed multiple of the reference frequency.

Since the system employs feedback control, the operation is one of closed loop control, in contrast to open loop control; therefore, this system has the advantage of providing less dependence upon system component characteristics and less sensitivity to load disturbances. Those components that exhibit major influence on the overall system performance have been designed for high accuracy and reliability; i.e., the components comprising the phase discriminator utilize state-of-the-art integrated circuits and employ digital techniques in their design. Since the operation of the various digital portions of the system is significant, a detailed discussion of these components follows.

THEORY OF OPERATION

Programmable Frequency Divider

The logic circuit diagram of an n-bit programmable frequency divider is shown in Figure 2. In operation, an input frequency may be divided by any integer

UTILIZING A DIGITAL CONTROL LOOP

RAYMOND B. SEPE

Submarine Signal Division
Raytheon Company
Portsmouth, Rhode Island

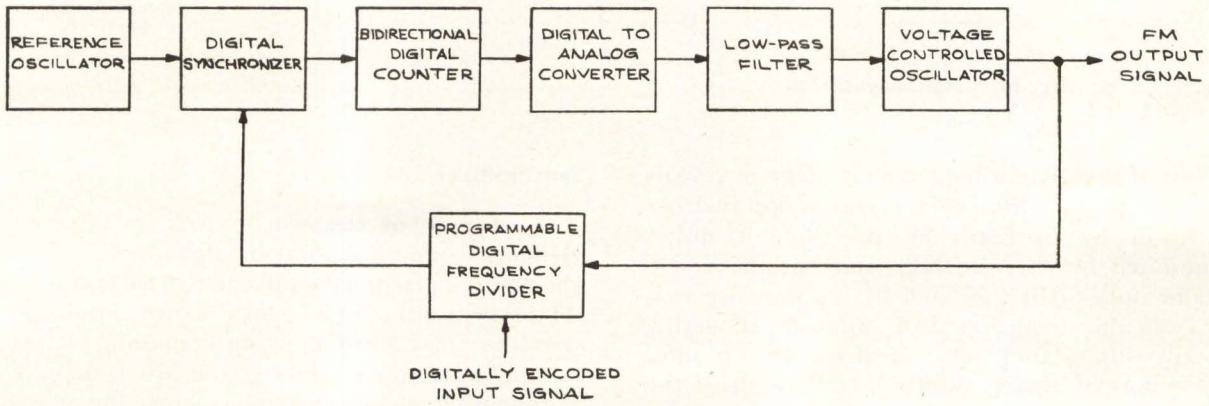


Figure 1. Functional block diagram of the DFFMS.

ranging from 1 through 2^n, where n is the number of flip flops cascaded in the divider. Divider control orders, digitally encoded, provide remote control of the divisor. The divider utilizes integrated circuits in a simultaneous carry division scheme. The design is repetitive in two-bit groups and is therefore especially well suited to modular construction on printed circuit cards. As many two-bit groups as desired may be cascaded to provide as large a division range as required for a particular application. Only two types of components are used throughout the design: NOR gates and J-K flip flops.

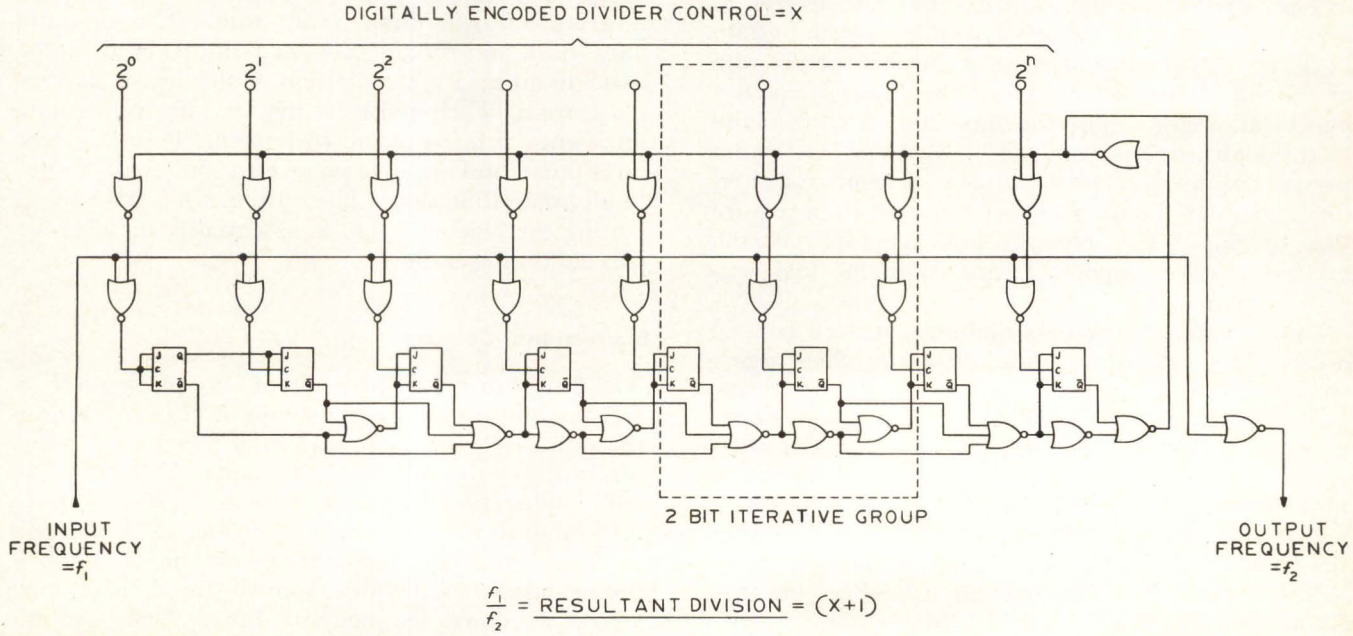


Figure 2. Logic circuit diagram of n-bit programmable divider.

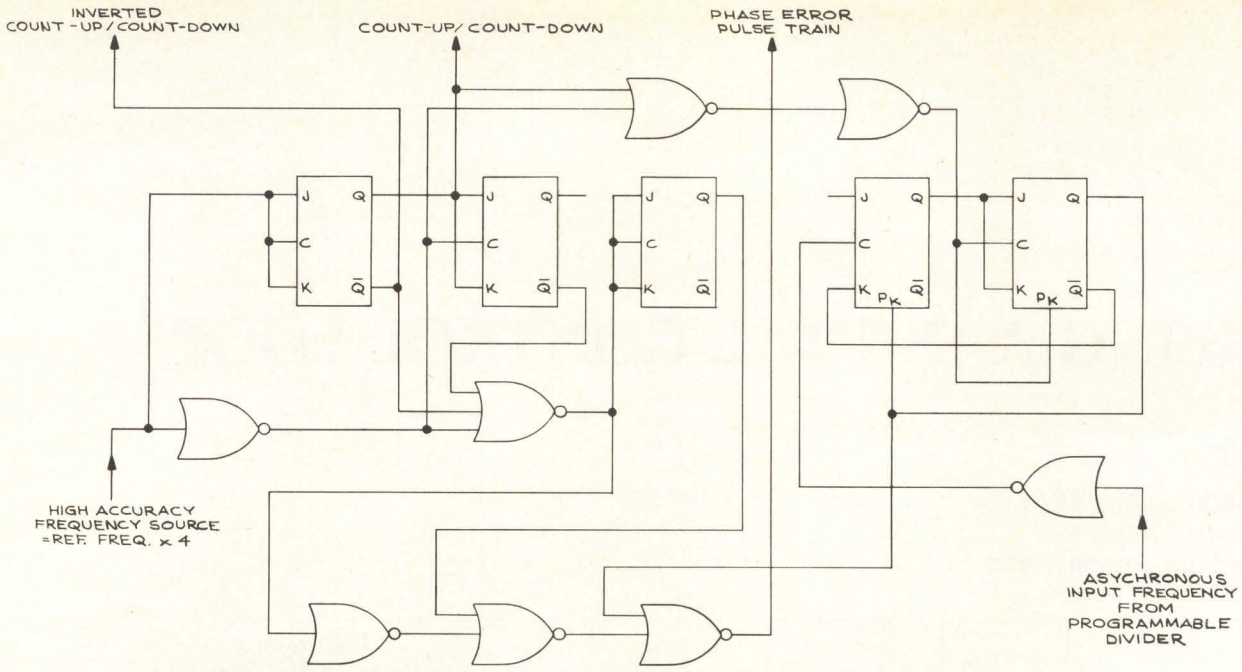


Figure 3. Logic circuitry for a digital synchronizer.

Analysis of the divider logic circuit diagram reveals that the input frequency toggles each flip flop that has all ONES in the flip flop chain preceding it, unless it is inhibited by the all-ONES state of the entire counter or unless it is inhibited by the presence of a ZERO from the divider control input. Such gating allows the input frequency to drive the counter through a normal binary counting sequence up to the all-ONES state and then to recycle the counter in the highest x + 1 states, where x is the number encoded on the divider control inputs. One output pulse is emitted synchronously with the input frequency each time the counter recycles through the all-ONES state. As x varies from 0 to $2^n - 1$, the ratio of divider output frequency to divider input frequency varies from 1 to $1/2^n$.

The division scheme utilized in this divider is unique in that the counter is driven from state to state in its entire sequence of states uniformly, at the rate of the input frequency. Thus, the input frequency may be allowed to attain the maximum rated response of the logic circuits employed. "Between-clock-pulse preset" schemes and "unstable state" schemes for altering the normal binary counting sequence often require that the input frequency be less than one-half the maximum rated response frequency of the logic circuits employed.

Since the divider accepts digitally encoded control orders, the required sequence of divisors which represent the modulating signal may be generated by various means, e.g., a memory unit, a cycling binary counter, an A/D converter, or even push button switches. In all cases, the sequence of divisors serve to program the frequency divider for precise removal of the desired intelligence from the feedback sample of the DFFMS output. The correction signal, appearing at the frequency divider output, is fed to the synchronizer for comparison with a highly accurate and stable reference frequency.

Synchronizer

The purpose of the synchronizer is to serve as a frequency summing point by algebraically combining the reference frequency and the comparison frequency. The synchronizer must generate two outputs to support the phase error tracking operation taking place in the bidirectional counter: the first is a pulse train representing phase error increments; the second is a pulse train representing the algebraic sign associated with the coincident-occurring phase error increment pulse. The logic circuitry required to accomplish this is shown in Figure 3. The synchronizer utilizes integrated circuits to generate an up-count pulse train by subdivision of the output of the high accuracy crystal oscillator. Asynchronous output pulses from the programmable frequency divider are aligned to generate a down-count pulse train. The up-count pulse train and the down-count pulse train are interlaced to form a time division multiplexed tracking pulse train. Each pulse in the tracking pulse train represents a phase error increment. Positive phase error pulses and negative phase error pulses are located in alternate time slots. The output pulse train representing the algebraic sign is, essentially, the demultiplexing timing train.

Bidirectional Counter

The bidirectional counter accepts the phase error increment pulse train as a clocking input, and accepts the demultiplexing timing train as a count-up/count-down control input. The logic circuit diagram of an m-bit bidirectional counter is shown in Figure 4. In operation, input pulses applied to the clock line will sequence the counter up through its binary states if the count-up/count-down control input is a logic ONE, or down through its binary states if the count-up/count-down control input is a logic ZERO.

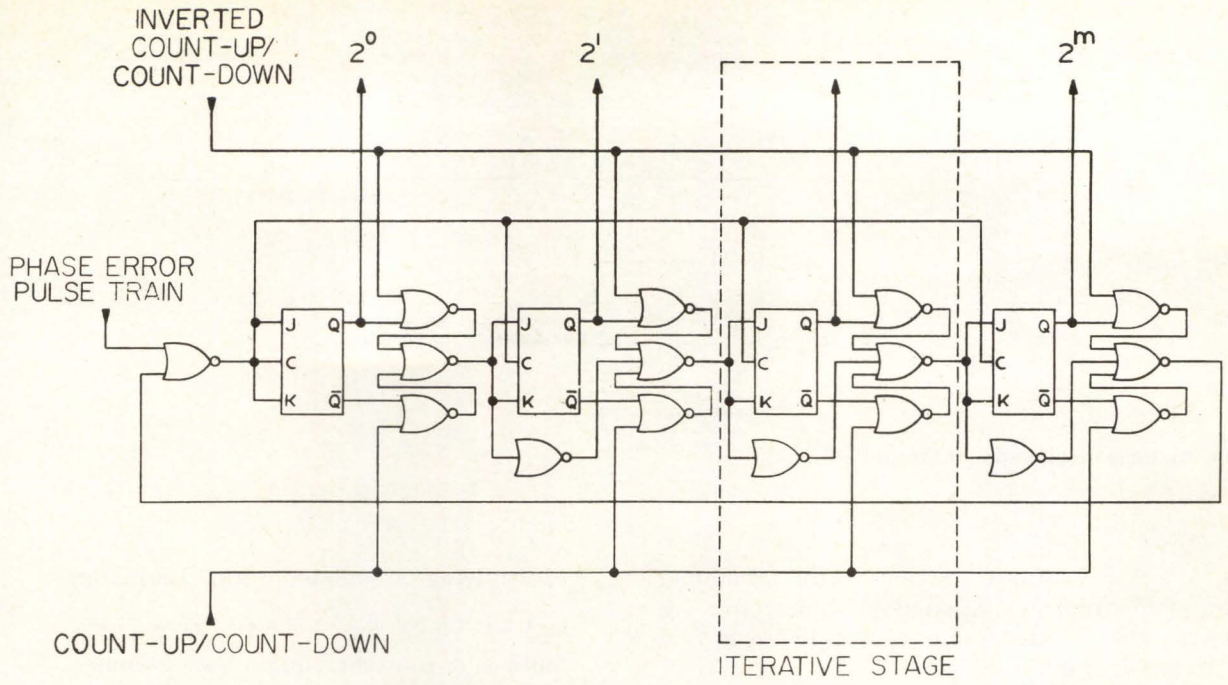


Figure 4. Logic circuit diagram of m-bit bidirectional counter.

The counter is gated such that saturation of the counter in either direction will not cause recycling, i.e., up-counting in excess of the counter's maximum count capacity (2^m) will not cause overflow and subsequent recycling to minimum count, and down-counting in excess of the counter's minimum count capacity (0) will not cause underflow and subsequent recycling to maximum count. In a given application of the DFFMS, the bit capacity of the bidirectional counter would be such that saturation would not occur over the entire range of phase-locked operation.

The bidirectional counter utilizes integrated circuits in a simultaneous carry counting scheme. The design is a result of sequential logic circuit synthesis techniques[10] that yielded logic recursion formulas indicating bit-wise iterative networks as indicated in Figure 4. In general, the j^{th} bit of an m-bit bidirectional counter is toggled by the logic:

$$T_j = U \prod_{k=j+1}^{m} yk + D \prod_{k=j+1}^{m} \bar{y}k \qquad (1)$$

where

$T_j = j^{th}$ toggle logic
U = up-count/down-count control: ONE
D = up-count/down-count control: ZERO
$yk = $ state of K^{th} flip flop
$\bar{y}k = $ inverse state of K^{th} flip flop

and the m^{th} bit is the least significant bit.

As the counter performs an integration of phase error increments between the reference frequency and the feedback comparison frequency, the counter state is sampled by the D/A converter, thereby generating a dc voltage proportional to error.

D/A Converter Operation

The function of a D/A converter is to accept a digitally encoded signal and convert it to analog form. The digitally encoded signal changes in discrete steps; the smallest amplitude change is dependent on the number of signal quantization levels. The conversion of each discrete step on the digital inputs to an accurate corresponding change at the analog voltage output requires a settling time. The output will have high frequency transients before it begins to settle. If the output is going to a low frequency device, the transients can be ignored.

Filter Operation

In the DFFMS, the output of the D/A converter is fed through a low pass filter to the VCO. The low pass filter provides smoothing of the transition between states as well as filtering of the high frequency transients. Considerations for idealizing the filter are included in the literature[2] and shall not be pursued here in detail.

VCO Operation

The purpose of the VCO is to accept the filtered output of the D/A converter and provide a corresponding voltage-to-frequency conversion. The VCO must have the flexibility to generate the entire range of required output frequencies as the filtered D/A converter output traverses its entire voltage range. The linearity requirement of the voltage-to-frequency conversion is not severe since the feedback through the phase discriminator provides a linearizing compensation on the control voltage, during phase-locked operation.

ANALYSIS

The development of a suitable mathematical model to facilitate analysis of the DFFMS is accomplished by developing an equivalent analog model for the digital

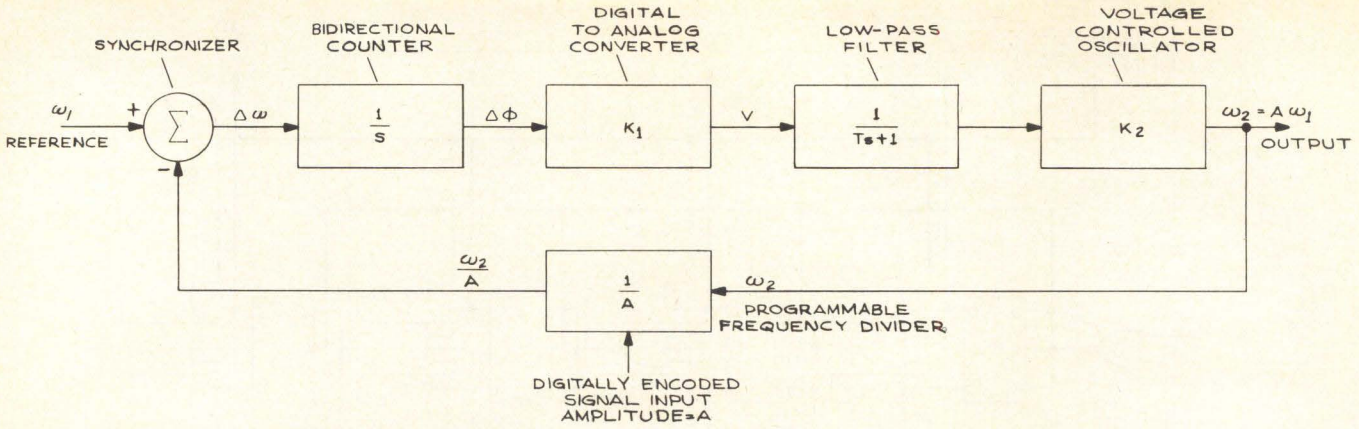


Figure 5. Mathematical model of the DFFMS.

system. When the various functions in the functional diagram of Figure 1 are replaced by their respective transfer functions, the result is the mathematical model shown in Figure 5.

The programmable divider used in the feedback loop converts output frequency to a submultiple of output frequency and therefore is represented by 1/A, where A is the instantaneous amplitude of the digitally encoded input signal. The summation point represents the algebraic combination of the feedback comparison frequency and the reference. The integration of phase-error increments accomplished in the bidirectional counter is represented by the 1/S term, and the gain of the D/A converter is represented by the constant K_1. F (s) is the transfer function of the low pass filter which for analysis is assumed to be

$$F(s) = \frac{1}{Ts + 1}$$

The VCO merely accomplishes a voltage-to-frequency conversion and its analog representation is a constant K_2.

The resulting mathematical model describes the DFFMS as a second-order nonlinear system similar to basic AFC systems, except for the complications of a variable ratio feedback. The full implication of a variable ratio feedback is revealed in the detailed analysis of the system phase-plane portrait.

Writing the system equation:

$$\frac{\omega_2}{\omega_1} = \frac{K}{S(1 + Ts) + K/A} \tag{2}$$

where

$$K = K_1 K_2$$

Writing the equation for system error:

$$\varepsilon = \omega_1 - \frac{\omega_2}{A} \tag{3}$$

Rearranging the right side of equation (3)

$$\varepsilon = \omega_1 - \left(\frac{\omega_2}{\omega_1}\right)\frac{\omega_1}{A} \tag{4}$$

Substituting equation (2) into equation (4)

$$\varepsilon = \omega_1 - \frac{K\omega_1/A}{s(1 + Ts) + K/A} \tag{5}$$

Multiplying through to clear denominators:

$$T\varepsilon s^2 + \varepsilon s + K/A\,\varepsilon = \omega_1 Ts^2 + \omega_1 s \tag{6}$$

Since ω_1 = constant, equation (6) becomes:

$$\varepsilon s^2 + \frac{1}{T}\varepsilon s + \frac{K}{TA}\varepsilon = 0 \tag{7}$$

Transferring to the time domain, the homogeneous differential equation for error is:

$$\frac{d^2\varepsilon}{dt^2} + \frac{1}{T}\frac{d\varepsilon}{dt} + \frac{K}{AT}\varepsilon = 0 \tag{8}$$

And the natural frequency is given by:

$$\omega_0 = \sqrt{\frac{K}{AT}} \tag{9}$$

And the damping ratio is given by:

$$\zeta = \frac{1}{2T\sqrt{\frac{K}{AT}}} = \sqrt{\frac{A}{4KT}} \tag{10}$$

Normalizing time:
Let

$$\tau = \omega_0 t,\ d\tau = \omega_0 dt \tag{11}$$

Substituting equations (9), (10) and (11) into equation (8):

$$\frac{d^2\varepsilon}{d\tau^2} + 2\zeta\frac{d\varepsilon}{d\tau} + \varepsilon = 0 \tag{12}$$

Define the new variables:

$$x1 \equiv \varepsilon$$
$$x2 \equiv \frac{d\varepsilon}{d\tau} \tag{13}$$

Substituting equation (13) into equation (12):

$$\frac{dx2}{d\tau} + 2\zeta x2 + x1 = 0 \tag{14}$$

For a given value of ζ, the system phase-plane portrait may be plotted.

In the DFFMS, the value of ζ changes with signal input to the programmable frequency divider. In a typical system, the divisor amplitude A may vary

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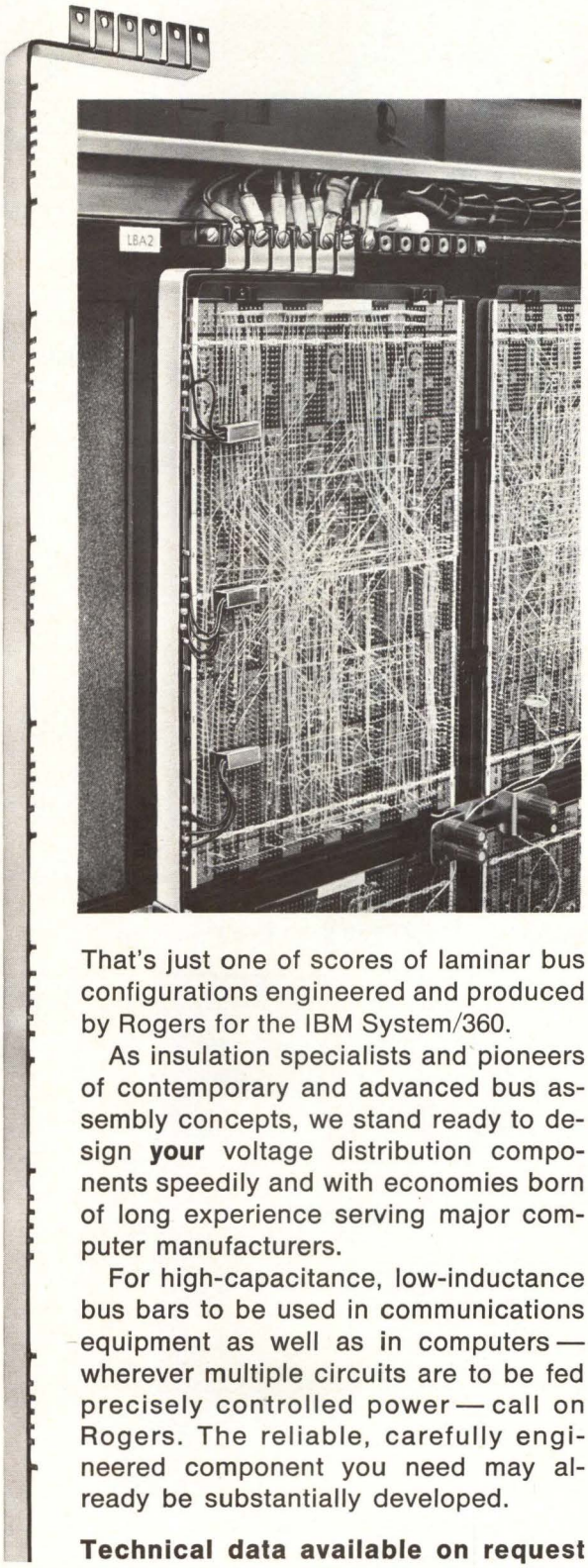

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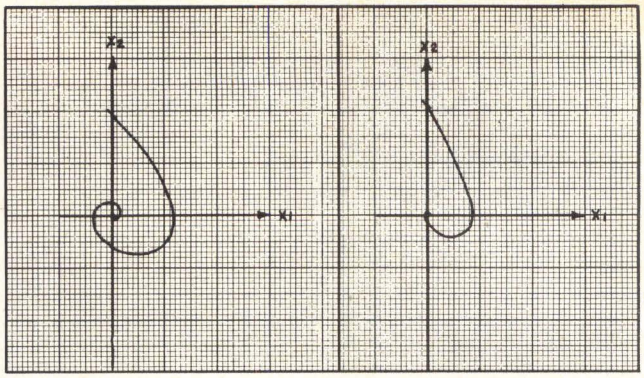

Figure 6. Phase-plane portrait damping ratio 0.40.

Figure 7. Phase-plane portrait damping ratio 0.98.

through the integers from 1 to 16. A typical total gain constant is

$$K = K_1 K_2 = 10^3 \tag{15}$$

And a typical filter corner frequency is:

$$\frac{1}{T} = \frac{1}{RC} = 2\pi \times 10^2 \text{ rad per sec} \tag{16}$$

To yield:

$$\zeta = .4\sqrt{A} \tag{17}$$

$$\omega_0 = 792 \frac{1}{\sqrt{A}} \tag{18}$$

The resulting values of the damping ratio ζ, tabulated in Table I, correspond to a typical range of values for the divisor amplitude A.

TABLE I

Damping Ratios Corresponding to Division Amplitudes 1 through 16

A	$\zeta = .4\sqrt{A}$
1	0.40
2	0.57
3	0.69
4	0.80
5	0.89
6	0.98
7	1.06
8	1.13
9	1.20
10	1.26
11	1.33
12	1.38
13	1.44
14	1.50
15	1.55
16	1.60

The significance of equation (17) is that the system damping ratio changes as the signal input changes. Thus, the analysis is somewhat complicated by the

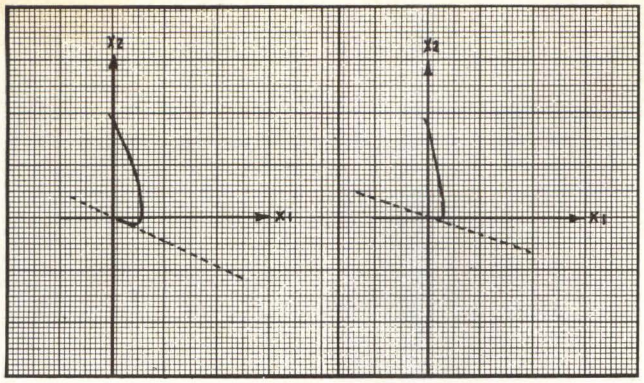

Figure 8. Phase-plane portrait damping ratio 1.33.

Figure 9. Phase-plane portrait damping ratio 1.60.

presence of a varying feedback ratio, as was predicted earlier. Since the signal input is digital, however, the amplitude variations occur as a sequence of discrete changes. The system performance may be adequately predicted by analyzing the phase-plane portrait corresponding to each of the values of damping ratio that are listed in Table I. By establishing that the system is stable in each of its discrete states, its stability is esablished as it operates sequentially switched throughout its entire range of states.

The phase-plane portraits corresponding to some of the values of the damping ratio listed in Table I are shown in Figures 6 through 9. They illustrate that for any given initial conditions, the phase trajectory of the system spirals into the origin. Since the loop transient response decays for any given initial conditions, the system is stable. Interpretation of the phase-plane plots is well documented in the literature[11], and will not be discussed in great detail here. It should be mentioned, however, that the patterns exhibited by Figures 6 through 9 fall into two characteristic patterns of stable system behavior. Figures 6 and 7 describe a system trajectory that spirals in toward the singular point, which is a stable focus. Such is the result when the damping ratio is in the range:

$$0 < \zeta < 1 \qquad (19)$$

Figures 8 and 9 describe a system trajectory that moves directly into the singular point, a stable node, without encircling it. Such is the result when the damping ratio is in the range:

$$\zeta > 1 \qquad (20)$$

Since the DFFMS never exhibits a damping ratio that is either equal to zero or less than zero, the system trajectory will never describe a circle, ellipse, or a diverging spiral. A circular or an ellipsoidal trajectory indicates undamped oscillation. A diverging spiral trajectory indicates an unstable focus. In general, it can be stated that the system will be stable since the damping ratio is always greater than zero; however, as the divisor amplitude is increased or the filter corner frequency is increased, the damping ratio is increased, and the phase-plane trajectory tightens to minimize the number and size of overshoots.

Richman[12] states that the time required for the system to lock, in response to a step input, depends

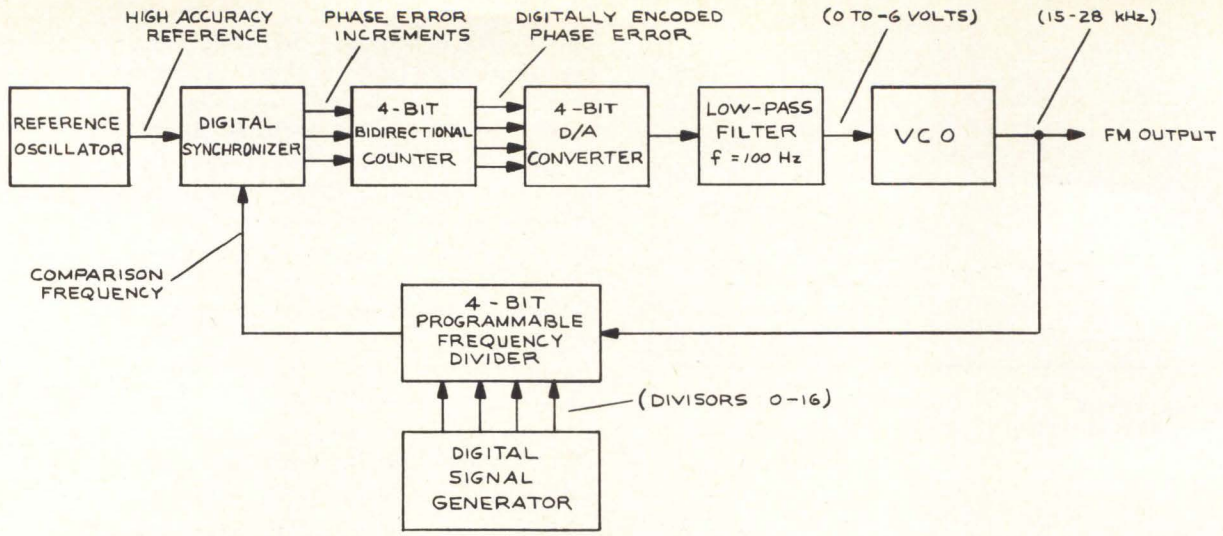

Figure 10. Experimental model of DFFMS.

on the initial frequency offset Δf and the system bandwidth F_n as follows:

$$t \cong 4 \frac{\Delta f^2}{F_n^3} \text{ seconds} \tag{21}$$

The noise bandwidth of the system expressed in terms of its damping ratio ζ, natural frequency ω_0, and total gain constant K is stated by Gruen[9] to be:

$$F_n = \frac{\pi\omega_0}{4\zeta}\left[1 + \left(2\zeta - \frac{\omega_0}{K}\right)^2\right] \text{radians/second} \tag{22}$$

Substituting equations (15), (17) and (18) into equation (22) yields an expression for noise bandwidth in terms of the signal amplitude A as follows:

$$F_n = 1240 - \frac{930}{A} + \frac{1240}{A^2} \text{ radians/second} \tag{23}$$

Substituting equation (23) into equation (21) yields an expression for pull-in, in terms of the signal amplitude A as follows:

$$t = 4 \frac{\Delta f^2}{\left(1240 - \frac{930}{A} + \frac{1240}{A^2}\right)^3} \text{ seconds} \tag{24}$$

In a typical system, as the signal amplitude varies from 1 through 16, the pull-in time will vary from 3120 microseconds to 40 microseconds. Thus, the input signal bandwidth for a typical system is considered to be 320 cycles per second for linear operation.

EXPERIMENTAL RESULTS

The results of the foregoing analysis are incorporated in the design of the experimental model of the DFFMS shown in Figure 10. Since the overall performance of the system is heavily dependent upon the accuracy of the phase discriminator, digital techniques are utilized in the design and implementation of the programmable divider, the synchronizer, and the bidirectional counter.

Practical limitations are placed on the capacity of the various digitally implemented functional blocks, but they do not detract from the usefulness of the experimental model. As an example, the programmable divider is limited to four bits, thereby limiting the system input signal to sixteen quantized levels of amplitude. This limitation, subsequently, limits the system output to sixteen quantized frequencies, provided that the VCO is capable of operating over that range.

The synchronizer is also designed with a practical limitation that is quite tolerable. The maximum frequency of the tracking pulse train is limited by the time division multiplex frequency. As a result of limiting the tracking frequency, the bidirectional counter tracks at a speed nearly proportional to error for small error magnitudes, and at the multiplex frequency for large error magnitudes.

The bidirectional counter is limited to four bits, thereby limiting the D/A converter to sixteen quantization levels. For a given voltage range, a larger number of quantization levels would reduce the size of the discrete voltage steps at the output of the D/A converter with an attendant reduction in the requirements on the smoothing action of the low-pass filter preceding the VCO. In the experimental model, a simple low-pass filter with a corner frequency at 100 Hz was used.

The D/A converter is limited to four bits to match the bidirectional counter capacity. The output voltage swing is approximately six volts, zero to negative, to be compatible with the VCO. Thus, the D/A converter limitations are dictated by its interfacing components.

The VCO employed has an output frequency range from 15 kHz to 28 kHz corresponding to an input voltage swing of five volts. The resulting gain of the VCO is approximately 2.6 volts per kilohertz. Proper selection of reference frequency and system input signal will allow the system to be tested within the VCO range.

The product of the reference frequency and the control signal must be in the range of the VCO for phase-locked operation. Experimental results of system operation as a function of reference frequency versus system output frequency are shown in Figure 11. Acceptable input signal amplitudes are indicated as superimposed rays on the same plot. Clearly, for a given carrier frequency, an increase in the VCO output frequency range would result in an increase in the number of acceptable input signal quantization levels.

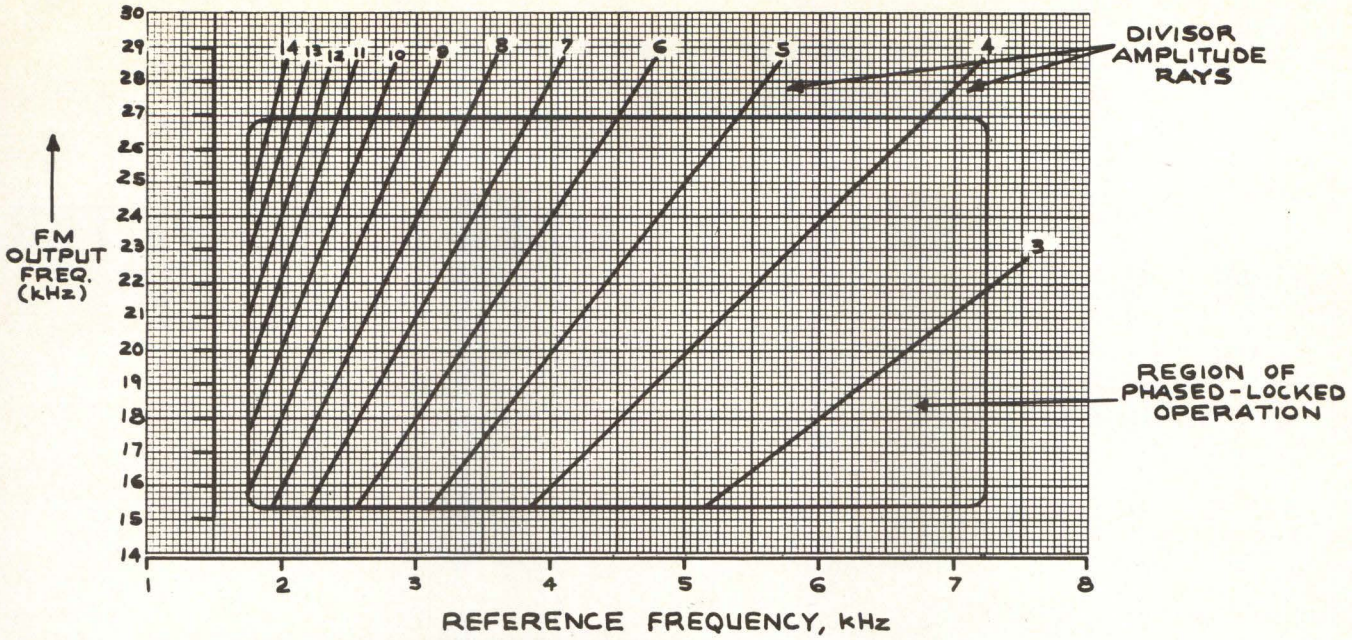

Figure 11. Experimental results of system operation.

Also, for a given VCO frequency range, the number of acceptable input signal quantization levels will increase as the reference frequency is decreased.

Although the experimental model is sufficiently complete to demonstrate typical DFFMS performance, the limitations imposed during the design were somewhat arbitrary. In a specific application, however, significant parameters will be defined by a system specification. For example, the number of discrete frequency levels required at the system output will be defined by the specification. This constraint will dictate the minimum capacity of the programmable divider. The specified separation between the discrete frequency levels will dictate the reference frequency. The product of the number of frequency levels N and the reference frequency f_r will dictate the VCO output frequency range:

$$\text{VCO Range} = N f_r \tag{25}$$

It should be noted, however, that the VCO linearity requirements will not be severe since the control loop provides linearizing compensation during phase-locked operation.

CONCLUSIONS

Signal processing systems often require a frequency modulation subsystem that is highly accurate and stable over a broad frequency range. The DFFMS is a phase-locked system that attains high accuracy and stability in its operation by deriving its output frequency from a single high accuracy reference. It utilizes a digital phase discriminator to detect output error and to generate a compensating error signal. The system output is simply and accurately controlled by a digitally encoded input signal.

Analysis of the system phase-plane portraits indicates that the phase trajectory spirals into a stable node or a focal point, whose pull-in time depends on the signal amplitude and the time constant of the low-pass filter. The sensitivity of the phase discriminator is dependent on the signal amplitude, also. In a series of tests performed on an experimental model of the DFFMS, the system performed exactly as predicted.

Extended applications of the DFFMS are expected to be numerous, and are based largely on the ingenuity of the system designer. Several examples of its potential use may be to generate broad band FM sweep waveforms, generate comb filter mixer frequencies, or to operate as a laboratory frequency synthesizer locked to a standard reference. Complex FM waveforms such as Gaussian FM, sinusoidal FM, or others may be generated by programming the DFMS from a memory system. In all cases, the performance will be highly predictable due to the advantages inherent in systems employing phase-locked and digital techniques.

REFERENCES

1. J. G. Shields, D. C. Weller, and W. R. Wysock, "A Phase-Locked Primary Frequency Supply," *Bell Laboratories Record,* XLIV, No. 7 (July-August, 1966), 236-238.
2. R. W. Sanneman and S. C. Gupta, "Optimum Strategies for Minimum Time Frequency Transitions in Phase-Locked Loops," *IEEE Transactions on Aerospace and Electronic Systems,* AES2, No. 5 (September, 1966), 570-581.
3. H. T. McAleer, "A New Look at the Phase-Locked Oscillator," *Proceedings of IRE,* XLVII (June, 1959), 1137-1143.
4. J. C. Otto, "Feedback Phase Modulator," *NEREM Record,* VII (1965), 90-91.
5. R. F. Shea, *Amplifier Handbook* (McGraw-Hill, New York, 1966).
6. E. E. Suckling, "A Stabilized Narrow-Band Frequency Modulation System for Duplex Working," *Proceedings of IRE,* XXXIII (January, 1945), 33-35.
7. G. L. Beers, "A Frequency-Dividing Locked-In Oscillator Frequency Modulation Receiver," *Proceedings of IRE,* XXXII (December, 1944), 730-737.
8. P. A. Borden, *Telemetering Systems* (Reinhold, New York, 1959).
9. W. J. Gruen, "Theory of AFC Synchronization," *Proceedings of IRE, XLI* (August, 1953), 1043-1049.
10. S. H. Caldwell, *Switching Circuits and Logical Design* (Wiley, New York, 1958).
11. J. E. Gibson, *Non-linear Automatic Control* (McGraw-Hill, New York, 1963).
12. D. Richman, "Color-Carrier Reference Phase Synchronization Accuracy in NTSC Color Television," *Proceedings of IRE,* XLII (January, 1954), 106 and 288.

This software system utilizes a family of computer programs developed for use as a design tool for logic and circuit designers and design draftsmen. The system has the capability to detect common errors and reject complete processing if errors are sensed.

ACCLAIM—A COMPUTER

ACCLAIM — Automated Circuit Card Layout and Implementation — is a family of computer programs, written in FORTRAN IV, which reduces Boolean equations to logical elements, translates the logical elements to physically realizable gates, synthesizes the gates into a switching network, and topologically configures a printed circuit card. It then determines the connection signal paths and produces artwork which is photographically processed into an etching template.

ACCLAIM consists of ten links operating under the IBSYS monitor system. The source decks contain more than 10,000 source statements. At the General Electric Aerospace Electronics Department (AED), these programs are running on an IBM 7040 computer with ten tape drives and a Univac 1004 off-line peripheral processor. A CALCOMP plotter is employed for graphical output.

The ACCLAIM system means different things to people from different disciplines. The logical designer envisions ACCLAIM as a design tool. He views the ACCLAIM programs as implementers of his design conceptions. The circuit designer conceives of ACCLAIM as a packaging manipulator. His utilization is to package a set of logic elements according to his predefined selections. The design draftsman heralds ACCLAIM as a tool to eliminate the long queues and delays often created in the layout and drafting cycle. The team that was assembled to develop this software system represented programmers from the applications and systems areas and engineers from both the hardware and logic design areas.

DESIGN PHILOSOPHY

The programming ground rules were simple and unequivocal: All coding was to be done in FORTRAN IV. Efficiency was to be sacrificed for simplicity and compatibility of experience. Generalized subroutines were to be developed when it had been resolved that the mathematical techniques to be programmed had been rigorously evaluated. Special-purpose subroutines were to be developed in those areas that employed heuristic techniques. Answers were to speak louder than hypotheses.

NETWORK MODELING

A presentation of the major functions of the ACCLAIM system first requires a discussion of input modeling. Networks are expressed in the AND-OR Boolean notation reflecting both combinatorial and sequential models. The network can be either synchronous or asynchronous. The equations are flip-flops or terminal connector pin input equations, or define subnetworks nested in the model.

The ACCLAIM system mechanizes multilevel (factored) input equations. Names of all variables are limited to six characters, with flip-flops designated by the leading character F. The terminal pins are designated by T; clock pulses, which require special consideration, are identified by CP. Any variables having other leading character designations are either input signal variables or dependent variables for a nested equation. Since we do not have a satisfactory partitioning algorithm, each switching network model cannot exceed the limits of a single predefined circuit card. The circuit card presently employed has a limitation of 104 gates.

CIRCUIT CARD PACKAGING

The most popular packaging configuration at AED is the stick module assembly. Twelve stick modules are mounted on a multilayer mother board (Figure 1). The stick module is a parallelepiped, 5 in. x ½ x ½ in., which has a maximum of 26 mounted flat packs (Figure 2). Two faces of the parallelepiped are used for signal routing, and the flat packs are juxtaposed on the two remaining faces. The environment of this hardware demands special thermal control; the core of the stick module constitutes a heat sink. The top and bottom faces have 200 flat pack pin feed-thrus and 96 mother board connector pins (Figure 3). The mother board connector pins can be used either as a signal connector to the mother board or as access to any of the four surfaces on the top and bottom faces.

The original intent of the ACCLAIM program was to specifically mechanize the Fairchild DTL (Diode Transistor Logic) logic module flat packs. In addition,

AIDED DESIGN SYSTEM

MILES D. AAKHUS
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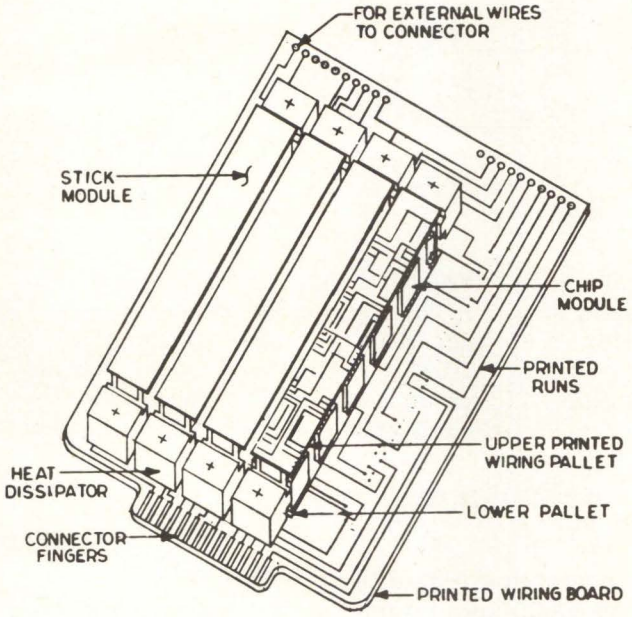


Figure 1. Stick module and mother board assembly.

other DTL lines and the Texas Instruments TTL (Transistor Transistor Logic) line have been mechanized. A partial set of the Suhl II TTL module repertoire has been configured. In all of these cases, the flat pack module has been employed.

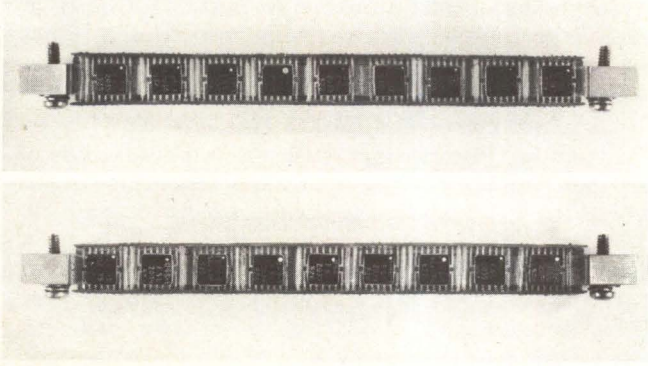


Figure 2. Two views of stick module.

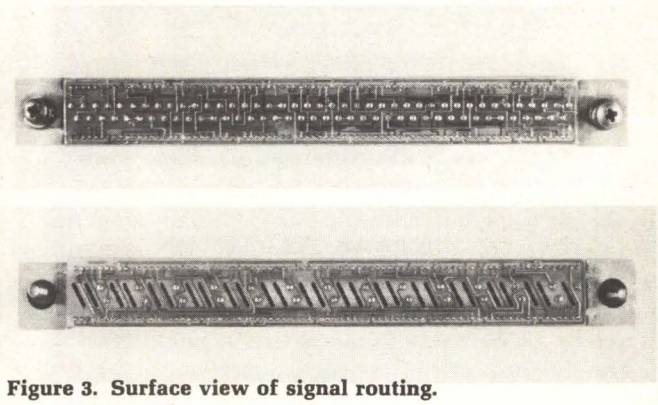


Figure 3. Surface view of signal routing.

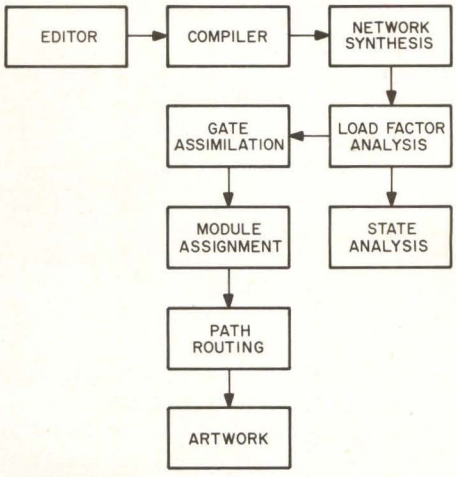


Figure 4. ACCLAIM System of programs.

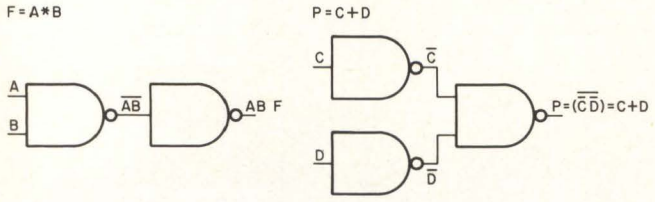
FUNCTIONAL DESCRIPTION

The ten links which make up the ACCLAIM system are illustrated in Figure 4. The EDITOR program checks the grammar of the Boolean equations used to input the switching network model. Conditions validated are the use of operators, the relationship of

left to right parentheses, and the synchronous versus asynchronous utilization of flip-flops. By utilizing a dictionary, all alpha-numeric symbology is converted to computerized digital notation. Finally, continuation cards are examined for order and structure.

The COMPILER translates the Boolean equations to computer-manageable (compiled text) lists. The multilevel equations are stripped of parentheses, and hierarchy of precedence is determined. Push down — pull up stacking methods are employed during the compiler processing.

The sequential function next performed by the ACCLAIM system is NETWORK SYNTHESIS. This program converts the compiled text, which is the AND/OR diode logic to a NAND transistor logic. The conversion is achieved by inverting the output of a NAND gate to realize a logical AND; inverting the inputs to a NAND gate delivers the OR function.



The NETWORK SYNTHESIS program assigns the logic elements into five categories after applying the transistor logic substitution. Gates are collected into three categories, based on the number of input signals. Flip-flops and terminal signals comprise the remaining categories. The gates, flip-flops and terminal connector pins are cross-referenced with interconnecting signals.

The network synthesis mechanization can be illustrated by describing the array used to create a physical realization. The α array is n x 7, where n is the number of logical elements used for the network formulation.

	1	2	3	4	5	6	7
1							
2							
3							
$\alpha =$ 4							
•							
•							
•							
n							

The rows of the array describe the individual logic elements required for the network synthesis. Each row will eventually be mechanized as an element or component of the stick module assembly. The logical elements employed in ACCLAIM are flip-flops, 2-legged gates, 4-legged gates, 4-legged expanders, terminal connectors, 4-legged lamp drivers and mono flip-flops.

The seven columns identify specific characteristics of the logic element. Column 1 identifies the number of input signals to be connected to the logic element. Column 2 describes the function the element is to perform. Column 3 is an interconnection identifier. It is this column which records the interconnection of the network. Columns 4 through 7 contain the identity of the input signals for the logic element.

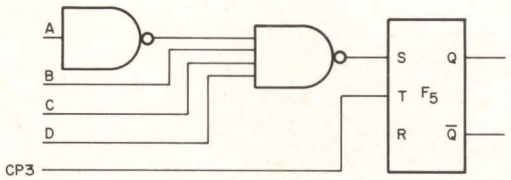
Let us examine the mechanization of an equation to illustrate the key to the ACCLAIM data base.

The equation: $F_5 = (A + \overline{B} + \overline{C} + \overline{D})\ CP_3$

The i^{th} row of the α array is an inverter (column 2 = I) used to invert signal A (column 4 = A) and the output ($\overline{A}$) is referred to as T_1 (column 3 = T_1). The j^{th} row is a 4-legged gate performing the OR (column 2) function. The k^{th} row is a flip-flop.

	1	2	3	4	5	6	7
i	1	I	T_1	A			
•							
•							
•							
j	4	OR	T_2	T_1	B	C	D
•							
•							
•							
k	2	FF	F_5	CP_3	T_2		

The α array creates and interconnects the elements illustrated in the following diagram.

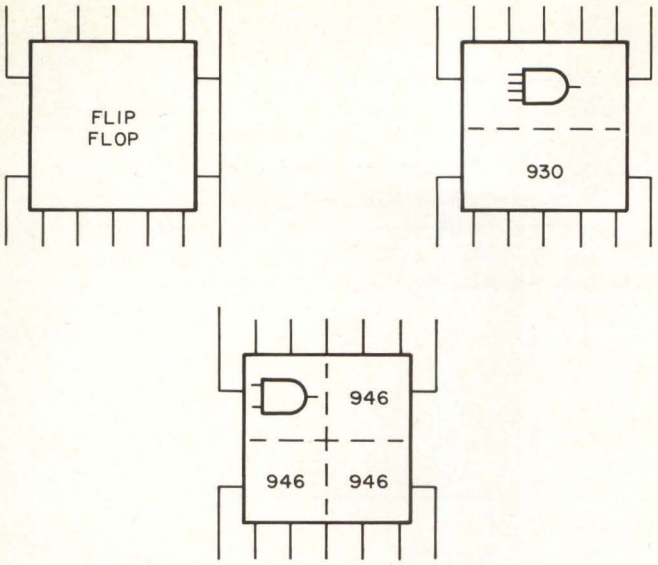


The LOAD FACTOR ANALYSIS program next insures the circuit loading integrity of the synthesized gating. Each logic element (gate or flip-flop) is analyzed for compatibility of fan-in and fan-out. Should a loading discrepancy occur, such as the fan-out of a flip-flop exceeding its drive capacity, additional gating is employed. Line driving amplifiers are added, and if complexity exceeds a combination of line driving amplifiers and flip-flops, the program requests engineering intervention.

Upon completion of the Load Factor Analysis program, an option is available. The State Analysis program, which simulates the logic of the network, may be selected or the primary function of ACCLAIM may be pursued: the creation of a printed circuit board. The State Analysis program will be discussed later.

PLACEMENT PROCEDURE

Placement of the elements of a logical network on a given physical configuration may be thought of as an application of two closely related procedures. Since the network is in general a composite of unlike logic elements (flip-flops, NAND-NOR gates, buffers, etc.), the first procedure, ASSIMILATION (commonly referred to as Gate Assignment), is the organization of the logic into physically equivalent sets (flat packs) where the flat packs each occupy identical space on the configuration. For example, a flip-flop is in itself a flat pack; however, in the case of DTL 930's (4-input NAND gate), DTL 932's (4-input NAND buffer), or DTL 933's (4-input diode expander), two such elements comprise a flat pack, and as many as four DTL 946's (2-input NAND gate) make up a flat pack.



The second procedure of Placement is the actual placing of flat packs relative to one another on the stick module. Consequently, Placement will herein be referred to as "Assimilation and Placement" or "A & P".

The A & P technique has as its underlying principle the conception of what the authors term an "m x n" Signal-Logic Matrix, $\Delta = \delta_{ij}$. The rows of Δ correspond to the m distinct signals, the columns to the n logic elements of the network. The matrix entries are binary and an entry δ_{ij} equals 1 only if the i^{th} signal is associated with the j^{th} logic element. The initial ordering of the elements in the network, and hence the columns of Δ, is not random, but on the contrary has a precise formulation. In order to describe this formulation, it is well first to consider the requirements and constraints of the stick module.

A CRITERION FOR PLACEMENT

As described earlier, a stick module is a parallelepiped, with flat packs embedded on each of two opposite faces and routing made from pin to pin (each flat pack has 14 pins — 7 pins on top and 7 pins on bottom) on the two enclosed "pallets" or faces. Occasionally the flat pack pins on one pallet must be connected to pins on the opposite pallet. This is accomplished via feed-thru holes between surfaces. However, because of the physical characteristics of the stick module, only a limited number of feed-thru holes are available in the routing. The Assimilation portion of A & P then must to some extent minimize the number of such holes required (Figure 5).

THE ASSIMILATION ALGORITHM

Consider the Signal-Logic matrix again in view of minimizing feed-thru holes. A flip-flop may be considered as composed of two disjoint sets, namely, the pins on the top and bottom of the flat pack, respectively. On the bottom, for example, are pins for clock pulse, set functions, set-direct and ground. In constructing the Signal-Logic matrix, the top and bottom portions of a flip-flop are selected, each as separate columns. Then, δ_{ij}, the entry corresponding to row i and column j, for the i^{th} signal in the network (ordering of signals is completely arbitrary) is non-zero only if the signal is a clock pulse, set function, set-direct or ground of the flip-flop in question.

The precise structuring of Δ is now readily evident. Columns are separated into two sets: set 1 represents all logic constituting the top portion of the stick module, set 2 the bottom. Arbitrarily we select half of the 930's, 932's, etc. for set 1; the remainder of logic is placed in set 2, thus completing the initial construction of the matrix.

	LOGIC OF SET 1			LOGIC OF SET 2		
	L_1	L_2	L_i	L_{i+1}	L_{n-1}	L_n
S_1	δ_{11}	δ_{12}	δ_{1i}	δ_{1i+1}	δ_{1n-1}	δ_{1n}
S_2	δ_{21}	δ_{22}	δ_{2i}	δ_{2i+1}	δ_{2n-1}	δ_{2n}
•	•	•				
•	•	•				
•	•	•				
S_m	δ_{m1}	δ_{m2}	δ_{mi}	δ_{mi+1}	δ_{mn-1}	δ_{mn}

SIGNAL-LOGIC MATRIX

Assume there are i_1 flip-flops, then logic elements $b_1, b_2, \ldots, b_n$ and $L_{n-i_1+1}, L_{n-i_1+2}, \ldots, L_n$ are selected to represent the top and bottom halves, respectively. Similarly, if there are i_2 930's, then $L_{i_1+1}, L_{i_1+2}, \ldots, L_{i_1+(i_2/2)}$ are initially the columns of set 1 associated with the first $i_2/2$ elements and $L_{n-[(i_2/2)+i_1]+1}, L_{n-(i_2+i_1)+2}, \ldots, L_{n-i_1}$ are the 930's of set 2 (if i_2 is odd, the extra element may be placed in either set 1 or set 2). The same applies for the remaining 932, 933 and 946 logic.

Feed-thru signals are easily recognized in the Signal-Logic matrix: if row k of Δ contains non-zero entries in both sets 1 and 2, then a feed-thru hole would be necessary in implementing a Placement. This suggests that feed-thrus can be minimized by interchanging a logic element in set 1 with a like element in set 2 if, by so doing, a feed-thru can be eliminated. To this end a routine, DIVIDE, was designed which considers all such juxtapositions or like logic.

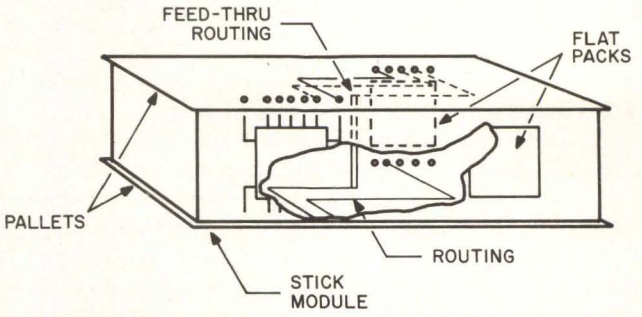


Figure 5. Feed-thru routing.

The second consideration of Assimilation is the combination of 946's in pairs so that the columns of Δ each reflect the logic comprising the entire top or bottom of a flat pack. A special-purpose subroutine, MAXMAL, was written to make this pairing. Essentially MAXMAL adds two likely columns, well orders the result and compares it with all other contingent pairs. Physically, the interpretation of this is simple: two gates having a common signal make a better pair than two that do not. If two prospective

pairs have an identical number of common signals, then that pair is selected which has the greatest activity (most signals) in the network. The motivation behind all this is simple: the length of subsequent routing can be more optimally minimized by the proximity, obtained in Placement, of "most active" flat packs. It is important here to note that upon selecting a pair of gates, their respective columns are replaced by the OR'ed sum. This preserves the essential binary integrity of the Signal-Logic matrix, which in turn allows subsequent columnar comparison requisite to A & P performance.

At this point, Δ is a matrix whose columns represent complete "half" flat packs, either half flip-flops, gates, or combinations of gates (946 pairs). A routine completely analogous to MAXMAL pairs off the upper and lower stick-module gates, and the Assimilation portion of A & P is complete. Upon ANDing the flip-flop portions, Δ becomes a Signal flat pack matrix.

To the authors' minds, Assimilation is the key to A & P. Excellent Placement is only possible as a natural consequence of sound Assimilation. As for the Placement of flat packs on the stick module, several alternatives presented themselves, the best of which (we might add) utilize the concept of a Signal-Logic matrix. For brevity, only one will be mentioned here.

THE PLACEMENT ALGORITHM

In the stick-module configuration, there are essentially but two directions pin-to-pin routing can take (feed-thru routing has been minimized): parallel routing, and vertical or cross routing (Figure 6).

Cross pallet routing in general is more objectionable than parallel routing (there are numerically less ways of circumventing a vertical run). Hence, the first step in "placing" flat packs is to use the previously mentioned DIVIDE routine to minimize cross runs on the module, by allowing the initially arbitrarily placed flat packs to be interchanged with brethren on the opposite side. The next step is a MAXMAL mating of flat packs on each side of the module (Figure 7a) followed by the analogous pairing of the mates on one side with those on the other (Figure 7b).

We are left with disjoint sets, four flat packs per set. Let us term these sets "super chips." The super chips must be placed relative to one another on the module and this is accomplished by DIVIDE. The super chips are labelled A, B, C, D, . . . in Figure 8. D_1, D_2, D_3, . . . are dividing lines employed to define successive sets in continuous application of DIVIDE. To illustrate this, super chip A is placed alone in set 1 with D_1 as dividing line. A call to DIVIDE then substitutes for A the most independent super chip on the module. Then, using D_2 as dividing line, the second most independent super chip, or the super chip most closely related to A's replacement, is substituted for B. This process is continued through D_3, D_4, etc.

Exhaustive flat pack placement is not yet accomplished. Super chips only (sets of four flat packs) are positioned on the module. In each super chip are two pairs of flat packs, a pair on either side of the stick module. The flat pack components of each pair were arrived at through MAXMAL, but the ordering of the components relative to the module is purely arbitrary.

Consequently DIVIDE is employed to consider an iterative interchanging of component flat packs within each pair (see Figure 9). For example, F_1 and F_2 are

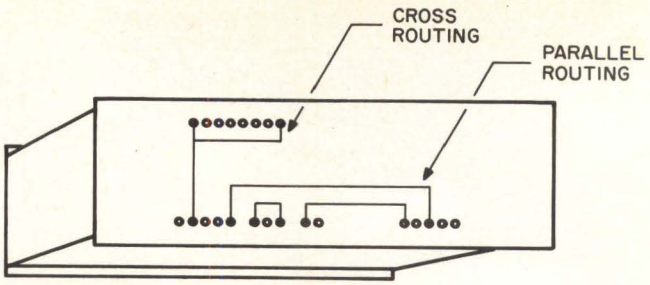


Figure 6. Stick routing and types of routing.

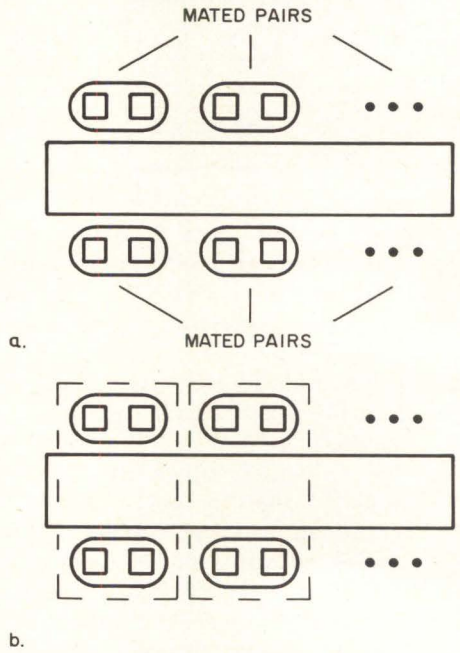


Figure 7. MAXMAL Pairs and pairing to form super chips.

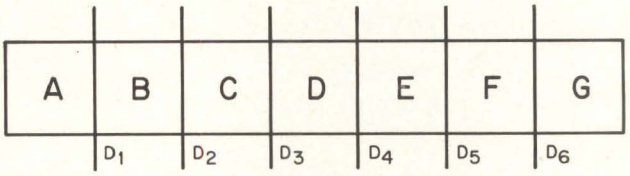


Figure 8. DIVIDE method of super chip selection.

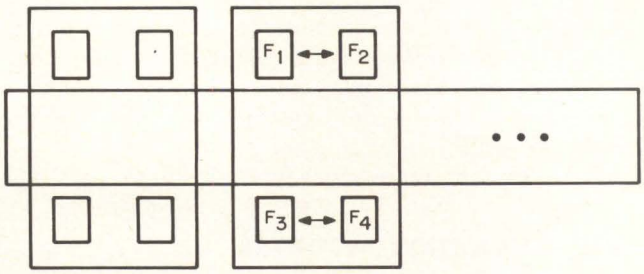


Figure 9. Interchangeability of flat packs within super chips. Arrows denote permissible interchanges within each super chip.

allowed to be interchanged relative to the entire module followed by a similarly considered interchange of F_3 and F_4. Then the process is iterated, since, if F_3 and F_4 were switched, the situation of F_1 and F_2 may be affected. The process is carried out similarly for each super chip on the module (Figure 10).

The purpose of the next process, PATH ROUTING, is to determine three-dimensional pin-to-pin signal paths. In addition, the path routing program massages the pin connection requirements, orders the signal lists, and recognizes special packaging constraints. The algorithm for routing is the industry standard: Lee's Algorithm.

The techniques of path routing have been extensively reported in the literature; however, one special technique employed by the ACCLAIM path routing may be of interest. A subnetwork consists of an input signal(s) entering a network, fanning out, combining with other signals, fanning in and exiting from the network. Processing of a subnetwork consists of routing individual line segments one at a time. As the home target list is processed, various pins (home or target) will have been previously connected (history) as an element of a path (line segment). In order to avoid redundancy of paths, it is desirable (and electrically equivalent) to allow the new path and the constructed path to intersect. An obvious example of this condition occurs during the fan-out of a signal.

A procedure is offered to extend Lee's fan-out algorithm to determine the shortest path between a point and a line (previously constructed path). This capability is desirable in order to obtain the minimum aggregate length of signal path routing. It can be shown that by using Lee's algorithm a shortest path can be found from point A (home) to point B (target). The reverse is also true; therefore, the home and target references are interchangeable. We call this technique "stubbing".

Let

H_i = a home
T_i = a target
P_i = a completed path
$\bullet\!\!-\!\!\!-\!\!\bullet$ = is connected to
$---$ = to be connected

Let α be the set of points which have been connected

$$\{\alpha\} = \{H_i \cup T_j \bigcup_{n=1}^{m} P_n\} \qquad H_i \bullet\!\!-\!\!\!-\!\!\bullet T_j \text{ by } P_n$$

Let β be the set of points which define a path to be constructed

$$\{\beta\} = \{H_k \cup T_1\} \qquad H_k ---T_1$$

Determine whether H_k or T_1 exists in α.

1) If $H_k \cap \{\alpha\} \neq \phi$

then

$$\{\beta\} = \{H_1, T_k \bigcup_{n=1}^{m} P_n\}$$

2) If $T_1 \cap \{\alpha\} \neq \phi$

then

$$\{\beta\} = \{H_k, T_1 \bigcup_{n=1}^{m} P_n\}.$$

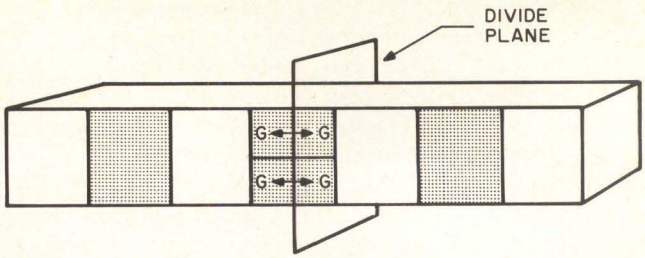


Figure 10. Three-dimensional conception of interchanges within super chips. Arrows denote permissible interchanges.

In (1) the home and target designations are interchanged. In (2) any point on the path (line segment) which includes T_1 is an alternate target (whichever comes first)

Let us examine the advantage of this technique. Given:

$$H_1 \bullet\!\!-\!\!-\!\!\bullet T_1 \text{ by } P_1 = \alpha$$

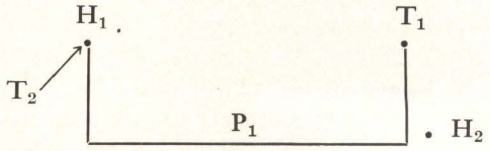
and the next set of points to be processed is

$$H_2 \!-\!\!-\! T_2 = \beta \text{ where } H_1 \equiv T_2$$

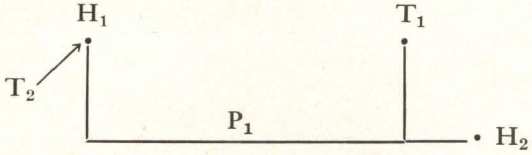
From (2)

$$\beta = H_2 \!-\!\!-\! T_2 \cup P_1$$

All the points of path P_1 are candidate alternate targets.



Lee's fan-out will connect H_2 to P_1, hence:

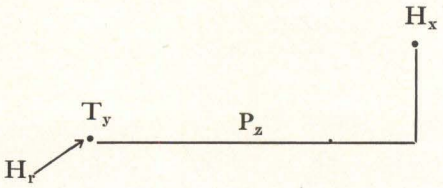


Given:

$$\alpha = \{H_x \cup T_y \bigcup_{n=1}^{m} P_{zm}\} \qquad H_x \bullet\!\!-\!\!\bullet T_y \text{ by } P_z$$

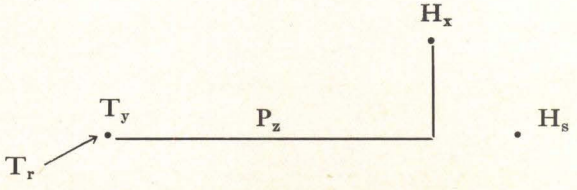
$$\beta = \{H_r \cup T_s\} \qquad H_r \!-\!\!-\! T_s$$

where $H_r \equiv T_y$



From (1)

$$\beta = \{H_s, T_r \bigcup_{n=1}^{m} P_{zm}\} \qquad H_s \!-\!\!-\! T_r \cup P_z$$



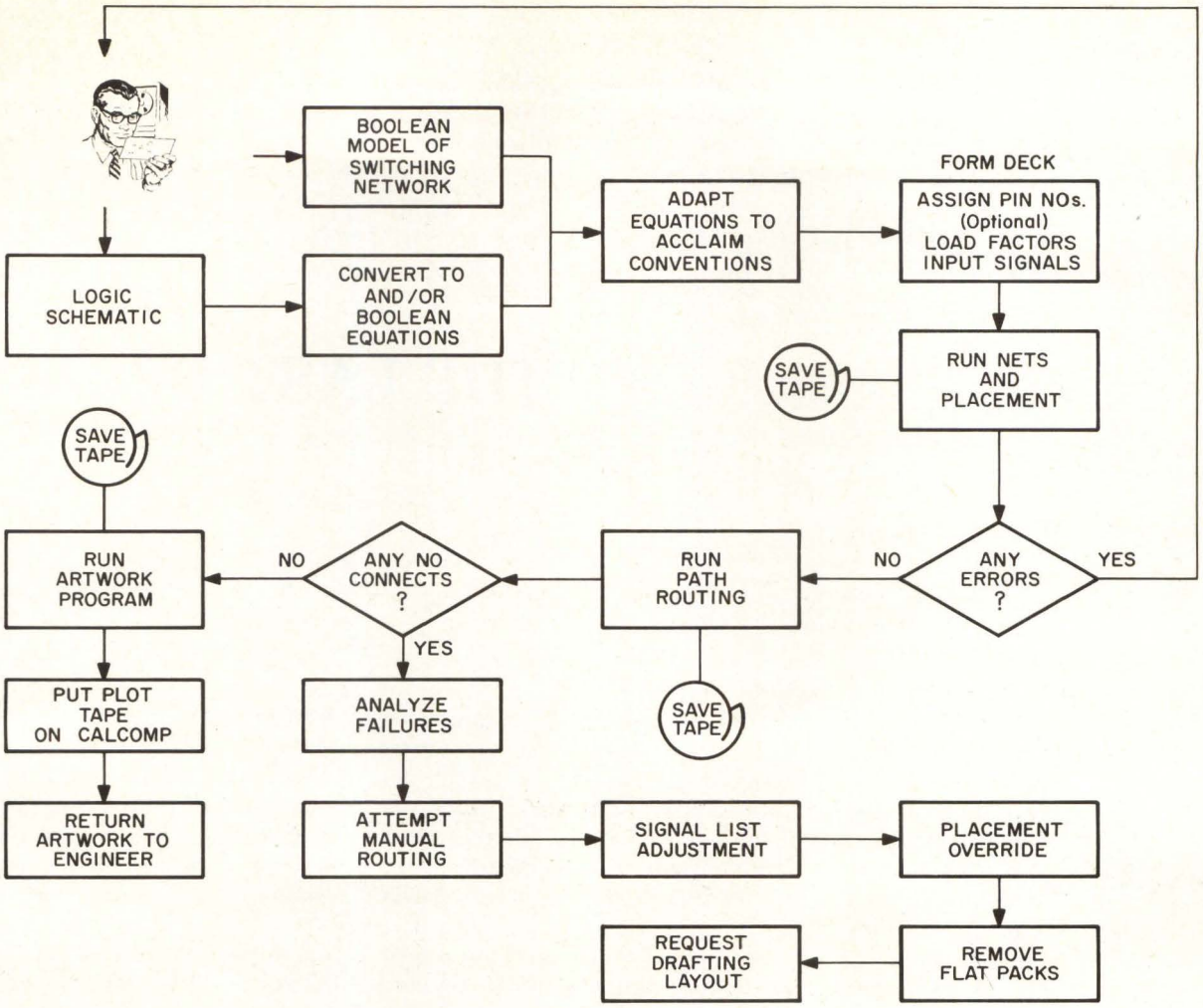
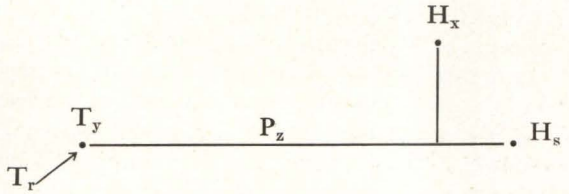


Figure 11. Processing of an ACCLAIM job.

Lee's algorithm will connect

$H_s \bullet\!\!-\!\!-\!\!\bullet P_z$

Hence:



The final program, ARTWORK, provides graphic output. Upon completion of each layer (surface), the path routing program eliminates all the ancillary data from the routing array, transmitting only signal path data to the Artwork program, selecting the critical points which are used as arguments for the general-purpose plotting routines supplied by CALCOMP. The critical points are the initial, terminal and change of direction points of the line segments joining the pins.

Adapting to manufacturing procedures ACCLAIM prepares two layers (surfaces) per drawing. Mylar is taped to the drum of the CALCOMP plotter and four time scale drawings of the stick module surfaces are generated. The performance (accuracy and repeatability) of the CALCOMP serves well for the stick module application.

STATE ANALYSIS

The STATE ANALYSIS program has been called by many different aliases, e.g., digital network simulator, logical verification, logical simulator, timing analysis, etc. The purpose of this program is to determine the states of the logical elements as a function of a predefined string of input stimuli. The program uses the compiled text of ACCLAIM after the network synthesis program has applied the substitution rules of NAND logic. The input stimuli are entered at time zero to create a predefined condition for the quiescent state of the network. Input stimuli may be introduced for any time interval, and those inputs will prevail. It is this option that allows a fault analysis to be performed in conjunction with the state analysis program. Sequential networks and combinatorial networks may be simulated, and the use of synchronous and/or asynchronous memory elements is allowed. A truth table output is provided via the off-line printer, and timing diagrams are plotted by a CALCOMP plotter.

Figure 11 illustrates how a job is processed through the ACCLAIM system of programs. The diagnostics of ACCLAIM detect common errors and reject complete processing if errors are sensed. If no errors occur, the processing continues to the completion of a job, culminating in a CALCOMP plot tape.

In the last ten years, the computer industry has witnessed two generations of computers. Initiated by the development of transistors and improvements in memories, computers became faster and more powerful. Developments in machine organization, the use of time sharing, and the introduction of microprogramming served to reinforce these hardware developments. With large-scale integration now becoming a reality, large (capacity) computers using monolithic integrated circuit arrays of hundreds of logic gates will provide the next generation.

THE LAST DECADE OF

This survey covers the period from about 1957 to the present; an excellent survey of the period up to that time is contained in Bauer.[1] The paper by Bauer is a reasonably thorough discussion of the development and state of the computer art up to the introduction of the first transistorized computers and represents an accurate view of the computer world as it appeared to a knowledgeable observer in 1957. However, since Bauer addresses himself to large-scale systems, he neglects to mention such important (historically) machines as the IBM-650[2], the first real production-type model of a full-sized computer. It was introduced in 1954, and at its peak, there were well over 2,000 installations.

HARDWARE DEVELOPMENTS

Transistors

The first major change in hardware in the period since Bauer's report was the introduction of the transistor. It was a great boon to the computing field for three main reasons:

1) It required much less power than the vacuum-tube.
2) It was physically much smaller in size.
3) It was a considerably longer-life device.

These factors, combined in various proportion, made possible the design of far more powerful computers (many more logic elements) than was possible with vacuum-tube technology. There was, of course, progress in transistors as circuits were made faster, but during the period in which the discrete transistor circuit was the mainstay of the computer logic (1960 to 1966) most improvements in computer performance were due to improved memory designs, the magnetic core memory in particular.

Memory Devices

Core memories became larger (10^6-bit memories were standard for any moderately large computer installation and some of the larger installations included 10^7 bits). Speeds increased to where cycle times approaching 1 μs were common, and through the use of interleaving of independent banks of memory, effective cycle times measured in hundreds of nanoseconds were realized. The core memory has proved a remarkably durable device. It was first introduced into the computer in the early to mid 1950's and has remained the major memory device up to the present time. Only in the current generation of machines (and only in a small number of machines) is there any suggestion of a replacement for the core.

Univac, in its 9000 series machines[3] is including a plated wire memory that operates in the nondestructive read mode at 600-ns cycle time, Burroughs has a 500-ns flat-film memory for its super-large 8500 system, and IBM has orders for the 360/95[5] — a super high speed computer with a magnetic-film main memory operating at 125-ns cycle time. At present, core memories operating at 750 to 850-ns are common and CDC has demonstrated full-scale core memories operating at 250-ns. It appears, however, that the discrete core memory has seen its peak as a main memory device.

Logic Elements

In third generation computers, integrated circuits have become the standard logic device (monolithic circuits for most manufacturers — hybrid circuits for IBM) and logical speeds have started to increase markedly: circuits with pair delays of under 5-ns are commonly available from semiconductor manufacturers and are beginning to appear in machines. Within the next few years, large-scale integrated gate arrays (100 to 300 on a single wafer) will become commonplace, and for the same reasons, the integrated array will be as much an improvement over the discrete transistor as the transistor was over the vacuum-tube.

RCA is building a general purpose computer, LIMAC[6], using arrays of bipolar logic and complementary symmetry MOS memory; Texas Instruments[7] is building a terrain-following-radar computer using bipolar logic and memory;

:OMPUTER DEVELOPMENT

SAUL LEVY

Data Processing Research
RCA Laboratories
Princeton, New Jersey

and Philco[7] is building a small guidance computer using P-MOS arrays for both memory and logic. These three computers scheduled for delivery to the Air Force at the end of this year and the beginning of next year will be the first computers constructed utilizing the new LSI technology.

Scratchpad Memories

In the 1960's the scratchpad memory, a small auxiliary memory operating about an order of magnitude faster than main memory speed, became quite common. At first, these were small core memories which could be made very fast because of their size — they have been replaced by small flat-film memories in some machines and by arrays of transistor registers in others. The scratchpad seems an ideal place to introduce LSI; in the SDS Σ-7 machine the memory is built from integrated arrays containing eight bits of transistor flip-flop storage,[8] and the IBM 360/85 has a buffer memory constructed from 64-bit arrays. Since this is an obvious area to apply large arrays, fully integrated solid-state scratchpad memories will probably appear before 1970 and will be a standard feature of the next generation of computer.

Another argument for using solid-state devices rather than magnetics for scratchpad memories stems from the requirements for a disproportionately large quantity of electronics just to make the magnetic memory electrically compatible with the logic (e.g. line drivers, sense amplifiers, level shifters, etc.). The semiconductor memory can be made compatible with the logic devices without the aid of additional interface electronics.

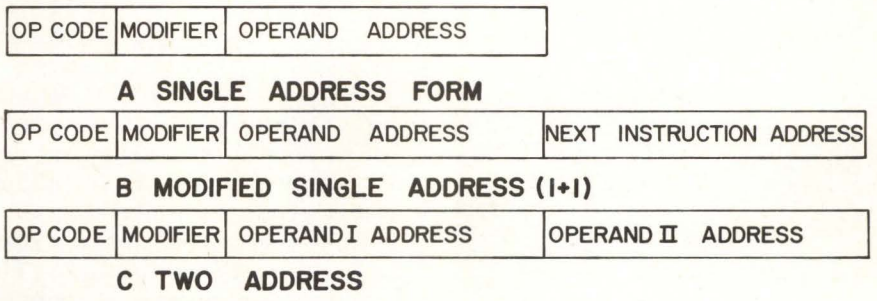
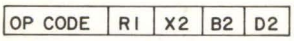


Figure 1. Instruction words.

MACHINE ORGANIZATION

Instruction Words

In the earliest machines (such as SEAC), the storage size, and consequently the address size, were small. This made it convenient for a single instruction word to contain several addresses. In the early drum machines, the modified single address or (1 + 1 address) structure was quite common. In this form, an instruction word contains an op-code and an op-address as in a single address instruction, but it also contains the address of the next instruction to be executed (Fig. 1). Thus, instructions could be distributed around the drum to minimize expected waiting times between instructions. With the advent of randomly accessible main memory this is no longer necessary and successive instructions are normally considered to lie in successive memory locations. As the size of memories increased, longer addresses were required to access a piece of data and this tended to make it difficult to fit several addresses into a single instruction word. Most current machines have either



R1 names fast access register which contains first operand

B2 is the name of the base register used in forming the address of operand two

X2 names the index register used in computing the address of operand two

D2 is the displacement used in computing the address of operand two

OPERAND 1 is in the register R1

OPERAND 2 is in the address computed by adding the contents of base register B2, and the contents of index register X2, and D2

Figure 2. Third generation computer instruction (RX format).

a double address (two operands specified) or a single address (one operand and the accumulator) with one noteable exception, the CDC 6600[9]. Addressing for large data bases is generally broken into two components: a base value stored in a full-length register which generally is set and holds a single value over a portion of computation, and a displacement value (typically 12 to 16 bits) which is shorter in length than the base and is the portion of the address carried along in the instruction (Fig. 2). An instruction which needs to access main memory specifies the base address register (one of 8 or maybe 16) and a displacement, and the address in memory is computed by adding the displacement to the contents of the base address register (plus whatever address modifiers are specified).

GENERAL COMMENTS

Progress in the early 60's was very much evolutionary. Main memories became faster and larger, electromagnetic devices made billions of bits of storage available in millisecond access times, and the basic logic gates became faster. The small machine became very popular spearheaded by the unbelievable success of the IBM 1400 series: nearly 15,000 of these were sold either as small stand-alone units or as peripheral processors for the larger 7000 series.

The upper-middle-size machine was dominated substantially by the IBM 709 — 7094-7094II. However the most interesting progress occurred in the development of large-size machines. STRETCH[1] was a failure both technically and financially: it neither met its design goals nor produced for anywhere near its selling price (although IBM claims that much of its loss was in effect recovered by incorporating much of the STRETCH design — hardware mostly — into the 7090 series). However, only the CDC 6600 shows serious potential for becoming a financially successful large computer. The basic organization of this machine represents a departure from conventional machines. There is a single central processor which has ten functioning instruction units (i.e. multiplier, divider, shifter, etc.) capable of parallel operation. The central processor operating on 60-bit words is a very high speed unit with typical arithmetic operation times running from a 300-ns floating add to a 3 μs floating divide. "Surrounding" the central processor are ten small complete computers each with its own 4096-word memory (12-bit words). These peripheral processors control I/O and handle the general functions of data preparation for the central machine (which stores 131,000 60-bit words).

The machine, first delivered in 1964, has the major bugs worked out of it and now seems on its way to general acceptance as the big machine. The memory which has a cycle time of 1 μs (fast for 1964) is overlapped 32 ways, although the machine cycle is such that only 10 memory accesses may be made in 1 μs. The basic memory module is 4096 words by 12 bits. These are stacked 5 high and arranged in 32 banks to make the main memory, and are used individually as peripheral processor memories.

The central processor has a set of eight 60-bit high-speed registers, X_0, X_1, . . . , X_7 used for holding operands and results. Associated with these registers are eight 18-bit address registers A_0, A_1, . . . , A_7. A change in the contents of any one of registers A_1 through A_5 results in new data being fetched from the main memory location (as specified by the contents of that register) and placed in the corresponding X register. In a similar manner, changes in A_6 or A_7 result in the contents of the corresponding X register being stored. (There are also eight 18-bit registers (B_0, . . . , B_7) used to hold modifiers and tallies. These are used in the conventional way.) Most central processor instructions are three address instructions specifying two operand registers and a result. There is an elaborate look-ahead mechanism including an instruction stack holding up to 32 instructions used to keep the appropriate operands in the high speed registers when they are needed. The ten peripheral processors are used mainly for general overhead and I/O processing.

Much attention to machine organization has been focussed on array or cellular computers. These computers are composed of a mat-

continued on page 76

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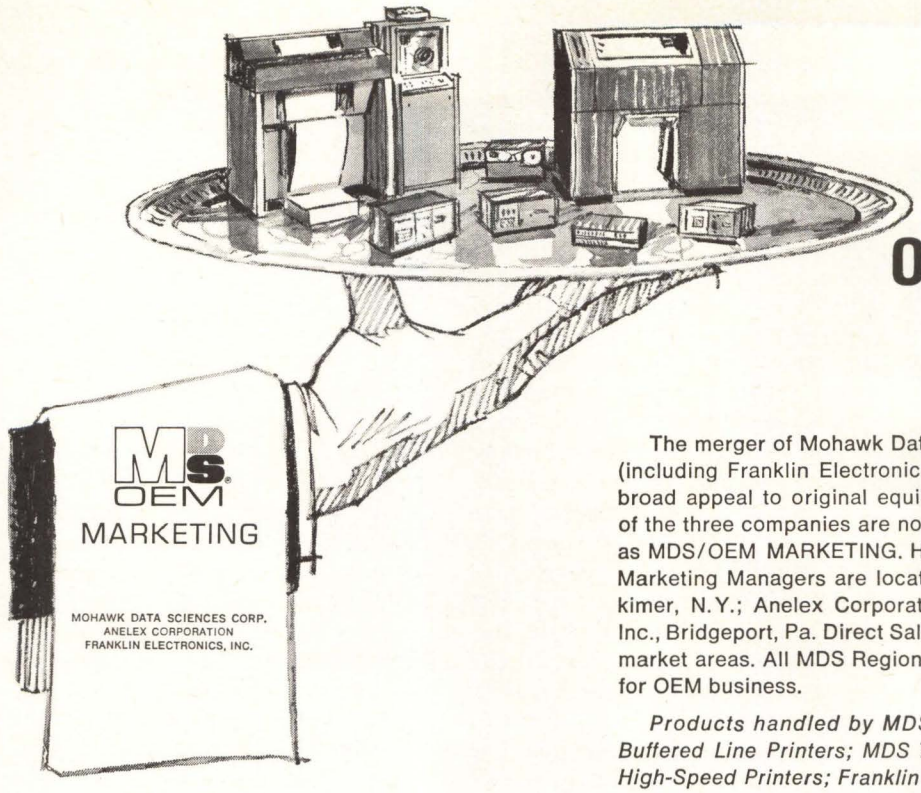
rix of small individual computers, each communicating with some restricted set of "neighbors" and each doing its own processing. Examples are 1) the Holland[10] machine where each processor worked independently of the others with no central control and 2) the Solomon[11] where the processors worked in parallel but under the control of a single central processor. Of the two types, the difficulties of programming the Holland machine were never overcome and the machine was never built. An early scaled-down version of Solomon was built for RADC, but severe restrictions in connectivity, difficulty of programming, etc. resulted in its being set aside. A strong argument against the approaches taken in the array machines described above is stated in "Grosch's Law". Grosch's Law[12] is an element of the folklore of computers which has been verified empirically and states roughly that *computing power increases as the square of cost.* This holds within the bounds of the current technology. But this says, in effect, that putting together multiple simple computers to do a larger job is not as economical as building a more complex single processor. The current effort to build a Solomon[13] is more reasonable in that each of the basic processors, instead of being a simple device, is a computer which is at the edge of the technology. It is being built by Burroughs for the University of Illinois and funded by ARPA. The memory is to be 250-ns thin films and the logic, to be built by Texas Instruments, Inc., will approach large scale integration. In general, the array machine appears to be effective for the type of problem which can keep many processors busy. This is a restricted, but apparently large, class of problems; it now remains to be seen how effectively the machine can be used.

Another approach to the supercomputer is a multi-computer system where the computers, instead of being identical, are specialized to the task. An example is the CDC 6600 mentioned above and the more recent IBM 360/90[5] machines. The 360/90 contains special I/O processors, a special fixed-point processor, a special floating-point arithmetic unit, and a special pro-

continued on page 78



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cessor whose main job is to look ahead in the program and schedule the execution of instructions to keep the floating-point-arithmetic unit busy. There is a great deal invested in the floating point unit; in fact, it alone is bigger (more gates) than most large computers.[14] Similar to the 6600, it has autonomous computation units, but they are of a type known as pipeline units. In the multiplier for example (an almost combinational 64-bit floating point — about 20,000 gates) the time for a multiplication is about 180-ns, but it is operated in three cycles about 60-ns each. A new multiply can be entered each 60-ns. so at any given instant three multiplications at different stages of activity can be in process in the single multiplier. The floating-point unit contains its own set of hardware registers, and the main task of the special processor is to see that all the operands required in the floating-point instructions are available in the registers at the time they are needed to ensure the floating-point unit is not kept waiting for a piece of data to arrive from main memory. The machine is programmed in the conventional way (in fact it is compatible with the rest of the 360 line) and any alterations in sequencing, etc. are handled in the special processor.

TIME SHARING

The biggest stir in the computer field has been caused by time sharing. The first major endeavor in this field was in MIT's Project MAC[15] using an IBM 7094 specially adapted to work with an extra-large core memory. The system was virtually all in software with the exception of additional I/O buffers and, of course, the terminals. Since the initial Project MAC experience, all the major manufacturers are constructing computers with special hardware to facilitate time sharing: the GE 645 came first and is replacing computers at Project MAC and Bell Labs New Jersey locations, among others. The SDS Σ-7 a smaller machine has won acceptance at several smaller users. IBM announced a machine, the 360/67 intended for time sharing which immediately swept the large time-sharing market selling to MIT Lincoln Labs (not Project MAC), Bell Labs midwest, and almost everyone else interested in large machines. There are also other machines like the Honeywell 8200, the CDC 6500, and the Univac 1108 multiprocessor system.

RCA is making a moderate-scale time-sharing system, the 70/46, to compete with the SDS machine and others of that size. Though there are many time-sharing systems now in operation from the very modest GE 265 (GE 235 and model-30 buffer) up to the DEC PDP 6 at Applied Logic or the SDS 940 (with 11 languages) at Berkeley, and of course, Project MAC; all of these are essentially software systems — with little or no special hardware to assist in such difficult tasks as management of a storage hierarchy; consequently there is inefficiency introduced when they are operated in a time shared environment. The 'typical' on-line user expects rapid (at most a few seconds) response from the computer. Then, the only way for the machine to satisfy many users is to alternate in some reasonable order among them with a very short cycle time. If the main memory of the machine was infinite, each user could fit his whole program in memory; in each time slot, the machine would execute a piece of the stored program for the appropriate user. But memories are not infinite, and in general, the sum of the memory requirements exceeds the capacity of the main memory. This must be hidden from the user — he should not have to worry about limiting his program size in accordance with the needs of other users. Something must be done to make the main memory appear "as big as it must."

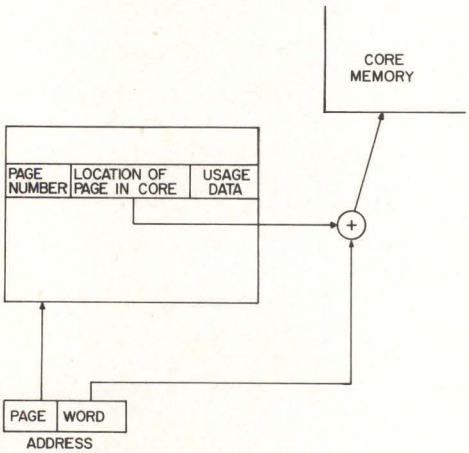


Figure 3. Page addressing scheme.

PAGING

This is a general description of paging (Fig. 3): most manufacturers have adopted some variation. About 1960, the computer group at the University of Manchester[16] was faced with the problem of building a high-speed computer with only a small core memory and a reasonably-sized drum memory for back-up. They attempted to build a system where the entire memory (core and drum) was addressed as if it were in core. The technique worked essentially as follows (the numbers are approximate): memory was divided into 512 word units called pages, the core memory held 32 pages. The drum storage was 96K words. There was a special set of 32 page registers which held the addresses of the 32 pages contained in the core memory in addition to some simple housekeeping information (e.g. when a particular page was last addressed). A memory address could be thought of as consisting of two components:

1) A 9-bit page name specifying in which page the address was located; and
2) A 9-bit address specifying which of the 512 words in that page was specified.

When a reference to memory was requested, the page portion of the address was checked against the table; if the page was shown to be in memory, the reference continued; if not, it had to be brought in from the drum. If there was no vacant page on the drum, this would have to wait until a page was dumped from core onto the drum. One of the jobs of the system was to see there was always an empty page in core when it was needed. To assist in this process, the page table stored special usage information (for example, has this page been written into?) as well as the location of pages in core.

In time-shared computers, paging is used to make large core memories appear enormous. Certain variations on the paging scheme are quite common; the most significant of these is segmentation, roughly an extra level of paging. The pages are arranged in segments in much the same way as words are arranged in pages and the address

is thought of as containing three components: the segment number, the page number, and the word number. Essentially the technique is the same as paging.

MICROPROGRAMMING

In 1951, Wilks first suggested the control sequence for a computer might be put into a read-only memory — associating with each of the lines in the processor to be controlled, a bit or set of bits stored in words in the read-only memory.[17] A sequence of words would be associated with each command. Thus, a certain flexibility is introduced into the control of the computer not present when the control sequence is generated by wired-in gates. To build a microprogram control the memory used must be 1) low cost and 2) very fast. The current generation of machines — at least the IBM system 360 and the RCA Spectra 70 — have microprogram controls for the lower-speed members of the family. Both manufacturers (RCA in the 70/55 and IBM in the 360/75 and above) find to get the speed required for fast machines at an economical price, wired logic is necessary. RCA's read-only memory is in two overlapped memory banks each with a 960-ns cycle time giving an effective read time of 480-ns/step. IBM has read-only memory in the 360/65 operating as fast as 125-ns. The microprogram control also enables both manufacturers to provide emulators with their computers. An emulator is essentially an additional read-only memory which enables the computer to interpret and execute an additional set of instructions, typically for a second generation computer. In this way, a user can run without any rewriting or preparation a program written for his old machine and much faster than he could have run it with a software simulator. Emulators are available to run IBM 1401, RCA 301, and RCA 501 programs on the Spectra 70/45 and 70/35; IBM has emulators enabling to run 1401 and 7000 series programs on the appropriate 360 machines. Read-only memories are generally only mechanically alterable although the Honeywell 8200[18] will have a read-only memory which will be electrically alterable by the manufacturer.

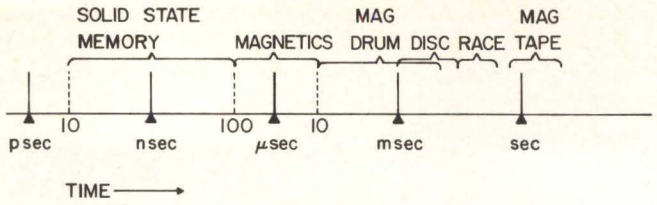


Figure 4. Spectrum of memory devices.

INPUT-OUTPUT EQUIPMENT

Surprisingly enough, the progress in I/O equipment has been very slow compared to the electronics. High-speed line-at-a-time printers operating at 1000 to 1200 lines/min. were common in 1960 and are still at the upper limit for mechanical printers. Console typewriters which punch and type at a maximum speed of about characters/sec. are also the rule now as they were in 1960 (or even earlier). Punched-paper-tape readers similarly have remained at virtually the same performance level since 1960 (about 1000 characters/sec. — read, about 100 characters/sec. — punch). Card readers have almost doubled in speed; but if one considers that computer speeds have increased by 1 to 2 orders of magnitude, then it is not very significant. However, there have been major improvements in magnetic recording techniques resulting in very high bit densities on magnetic media. This results in high speed magnetic tapes (120 to 240 kilobytes/second for high-speed units) and high-speed high-density magnetic drums (1 μs read or write times with capacities of 10^7 bits and access times of 10 to 20 ms).

New random-access storage devices with capacities far exceeding drums and access times measured in milliseconds have appeared. The primary device of this type is the magnetic disc memory which stores data on a stack of magnetic discs. A typical disc memory stores about 7,000,000 bytes which may be accessed in about 100 ms and then read at a 150-kilobyte rate. It is not uncommon for a computer to obtain as many as eight of these devices. Another class of random-access device involves data stored on magnetic cards which must be selected from a file and brought under the read/write heads. These include the RCA Race, the NCR Cram, and the IBM Data Cell. Access times average about 200 to 250 ms and data is then read at 70 kilobyte rates. The attractive feature of this device is that its capacity is large — almost 600 million bytes/unit with each RCA or IBM machine having a capacity to handle up to eight units with a single controller. Because of the relatively long times taken to access the first piece of information (Fig. 4) these devices find their primary application as block storage devices; one does not normally go to them to acquire a single piece of information, but rather to acquire a relatively large sequence of adjacent pieces of data. There are several new special devices for handling communications between computer and the outside, including such special-purpose devices as those which assemble voice messages. Communications buffers and data gathering devices are standard in every product line.

A device which has become more common in present generation machines, to a large extent as a result of time sharing, is the graphic console. This enables the user to communicate with the computer in a picture language much as he would use in order to solve problems with pencil and paper.

SOFTWARE

At the time that Bauer's report was written (1957) IBM introduced the first FORTRAN compiler. There had been other user-oriented languages (even compilers) before but FORTRAN was the first designed to produce "good" code comparable in quality to that hand produced by a "good" programmer. FORTRAN became the first widely accepted programming language to be adopted for use on the machines of several manufacturers. At present, better than 100 processors have been prepared for the FORTRAN language and it is available for nearly every computer intended for scientific use in this country. After

FORTRAN, COBOL (a Business-oriented counterpart) was introduced; then another scientific language ALGOL in several versions became very popular in Europe and at certain universities. Most recently, IBM has announced PL/I a kind of super-set of all the others. These languages all fit in the category of problem-oriented languages (their instruction repertoire is closer to the needs of the problems to be handled than the languages of the machines on which they are to be implemented). These languages have been joined lately by a host of special purpose languages such as COGO[19] suited to the problems of civil engineers, SKETCHPAD[20] a pictorial language for use with graphical I/O devices, etc. But FORTRAN remains the most widely used of all computer languages.

At present, the machine-oriented language is used primarily by two classes of user: 1) systems programmers and 2) others for whom there is no problem-oriented language suitable for their particular class of problem.

As the number and variety of problem-oriented languages increase, the fraction of computer users for the machine language will continue to decline. The use of problem-oriented languages carries with it a compatibility not carried by the machine language.

Compatibility at the machine language level is an important feature of third generation computers. IBM, RCA, Univac, and Burroughs have introduced compatible families of machines where machine-language programs written on one member of a machine family can be run on other members of the same family (with some restrictions on system configuration). RCA has designed its Spectra 70 to be language compatible, generally, with the IBM 360-series; Univac has apparently done the same with its 9000-series. But the most significant compatibility lies in the common user-oriented languages.

PREDICTIONS FOR THE NEAR FUTURE

The next generation of computers will be constructed with monolithic integrated circuits, although the number of gates on a single circuit will probably range from 4 to 300. The largest arrays to appear will most probably be in scratchpad memory. Monolithic memories, probably magnetic, will overtake the core memory as the main computer memory. However, as the batch fabrication technology improves, solid-state scratchpad memories on the order of a few thousands of words at very high speeds should become common, and what is now the main memory will become less significant in the scheme of computer operation.

The current generation of computers is better oriented to multiprocessor operation than preceding generations and this trend will undoubtedly continue. There are provisions for sharing memory banks as well as I/O channels; in fact, several systems such as the time sharing machines are designed and sold as multi-processors. (These include GE 645, IBM 360/67, CDC 6500, Honeywell 8200, and Burroughs B8500.)

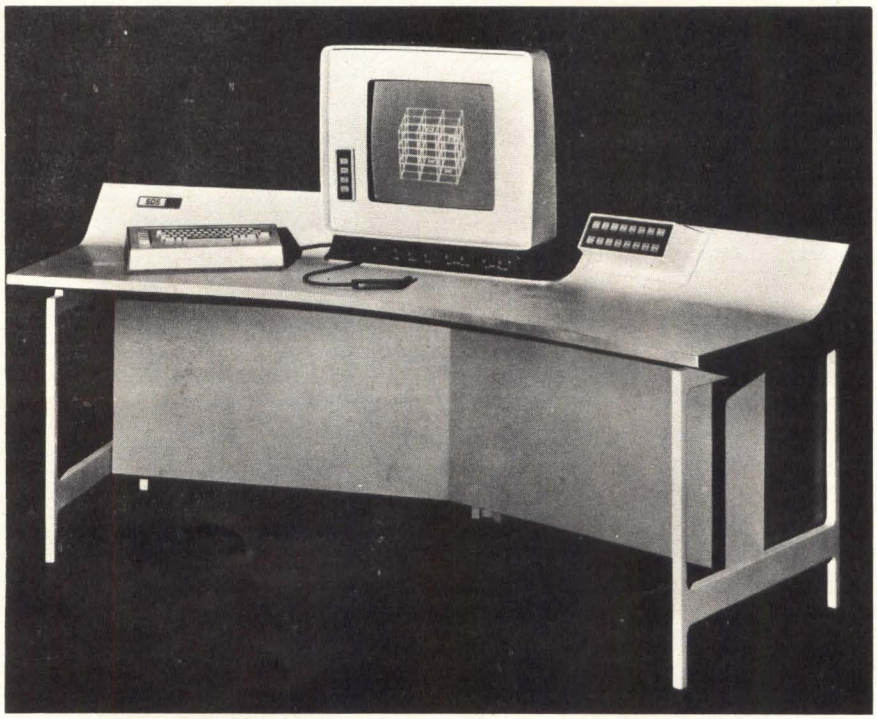
The pipeline-type processor described briefly above in connection with the IBM 360/90 will achieve more general acceptance. Time sharing will have a great impact on the fourth generation of machines. The market for small consoles (like the teletype and the graphic consoles) will increase by orders of magnitude. Two main types of machines for time sharing will be marketed. The first (like the PDP 10, the RCA 70/46, and the SDS Σ-7) will serve those users who envision running many small-to-medium size problems in a generally restricted environment — requiring fewer than, say, a dozen languages (e.g. FORTRAN, SNOBOL, COBOL, and a debugging language).

The large machines (the GE 645 or the Project MAC system) would be used in what is commonly called the "computer utility" mode. This would involve the maintenance of large special files for many of the users as well as a capacity for each user to contribute to the system work he has invested in the machine. Then a new language or set of routines developed by one user for the system can be immediately made available to the other users. (Naturally, if desired, privacy could be maintained.) There is a current market for both types of systems, and this market should continue.

REFERENCES

1. W. F. Bauer, "Modern Large Scale Computer Design," *Computers and Automation,* 1957.
2. F. E. Hamilton and E. C. Kubie, "The IBM Magnetic Drum Calculator Type 650," *JACM,* Vol. 1, PB (Jan. 1954).
3. "The Univac 9200 and 9300," *Datamation* (July 1966).
4. "The Burroughs B8500," *Datamation* (Aug. 1965).
5. Talk delivered at Princeton University EE Department by a representative of IBM. Details of the 360/91 a version of the same machine equipped with a conventional core memory may be found in the *IBM Journal of Research and Development,* Vol. 11, No. 1 (Jan. 1967).
6. H. R. Beelitz, S. Y. Levy, R. J. Linhardt, H. S. Miller, "System Architecture for Large Scale Integration," *Proceedings FJCC 1967.*
7. "Special Report on Large Scale Integration," *Aerospace Technology,* Vol. 21, No. 16 (Jan. 29, 1968), pps. 24-46.
8. "The Sigma 7 from SDS," *Datamation* (Mar. 1966).
9. J. Thornton, "Parallel Operation in the Control Data 6600," *Proceedings FJCC,* Vol. II (1964).
10. J. Holland, "A Universal Computer Capable of Executing an Arbitrary Number of Subprograms Simultaneously," *Proceedings of the EJCC,* Winter 1959.
11. D. L. Slotnick, W. C. Bosch, and R. C. McReynolds, "The Solomon Computer," *Proc. FJCC* (1962), pp. 97-107.
12. D. Slotnick, "Unconventional Systems," *Proc. SJCC* (1967).
13. K. E. Knight, "Changes in Computer Performance," Datamation (Sep. 1966).
14. John Earle, Panel Discussion on Logic Partioning in LSI, *ISSCC* (Feb. 1967).
15. F. J. Corbato, M. Merwin-Daggett and R. C. Daley — "An Experimental Time-Sharing System," *Proc. SJCC* (1962), p. 335, "The compatible Time-Sharing System Programmer's Guide," *MIT Press* (1963).
16. T. D. Kilburn, B. G. Edwards, M. J. Lanigan, and F. H. Summer, "One Level Storage System," *IRE Transactions on Electronic Computers,* Vol. EC-11, No. 2 (Apr. 1962).
17. M. V. Wilkes, "The Best Way to Design in Automatic Calculating Machine," Manchester University Inaugural Conference, Manchester (Jul. 1951), pp. 16-18.
18. "The Honeywell 8200," *Datamation* (Jul. 1965).
19. D. Holstein, "Are You Ready for Computer-Aided Design," *Product Engineering* (Nov. 23, 1964).
20. I. E. Sutherland, "SKETCHPAD: A Man-Machine Graphical Communications System," *Proc. SJCC,* Vol. 23 (May 1963). T. E. Johnson, "SKETCHPAD III Three Dimensional Graphical Communication with a Digital Computer," Ibid.
21. N. Nisenoff, "Hardware for Information Processing Systems: Today and in the Future," *Proceedings of the IEEE,* Vol. 54, No. 12, (Dec. 1966).
22. T. H. Bonn, "Mass Storage: A Broad Review," *Proceedings of the IEEE,* Vol. 54, No. 12 (Dec. 1966).

NEW PRODUCTS



GRAPHIC DISPLAY UNIT

A high-performance graphic display unit designed for use with SDS Sigma 5 and Sigma 7 computers; Model 7580 can be used to display data from on-going experiments, operate upon static displays to study the effects of design- or test-parameter changes, or visualize data or programs stored in memory to facilitate the development of new programs.

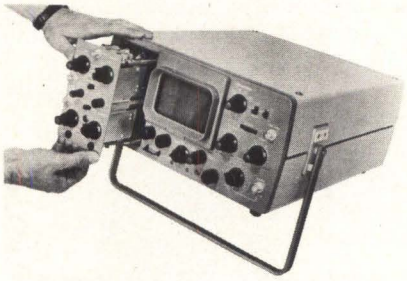
The flexible unit features a 21-inch cathode ray tube, four display generators, a 64-character alphanumeric keyboard, a 16-character function keyboard, four action switches, light pen, and associated electronics. Solid-state deflection and control circuitry are used in the CRT for accuracy, stability, and speed. Nominal display area is 100 square inches, accommodating 1024 divisions along both the X and Y axes. Within the 10-inch working area, resolution of a point is 0.01 inch and plotting rates exceed 140,000 points per second. Four display generators permit the unit to draw alphanumeric characters and special symbols, points, rasters, and vectors. Keyboard and action switches permit both the display unit and its associated computer to be programmed quickly and accurately for a variety of calculations and displays. Information displayed on the CRT can be sensed and manipulated by a light pen. The pen can be used to record the location of data, erase portions of a display, construct new displays and modify mathematical models. Scientific Data Systems, Santa Monica, Calif.

Circle No. 202 on Inquiry Card

MINIATURE SWITCH

The 11SM701 SPDT low operating force miniature switch requires only 56 grams (2 ounces) of force for actuation and has an electrical rating of 4 amps at 125/250 Vac. It is furnished with a number of material variations for environmental use options. The switch has a mechanical life rating of 95 per cent survival after 10 million operations. Integral lever versions offering an operating force as low as 6 grams are available. The switch will function within a temperature range of —85°F to +250°F. It weighs .096 ounces, maximum. Manufactured under space-age clean-room conditions, the 11SM701-T is UL approved (L119). MICRO SWITCH, a division of Honeywell, Freeport, Ill.

Circle No. 204 on Inquiry Card



PORTABLE OSCILLOSCOPE

A true dual-beam portable, solid-state oscilloscope, model S1302A, is operable on either internal battery or line voltage and features a choice of two plug-in Y amplifiers, (either 15MHz or 30MHz), and 21 ranges of calibrated sweep speeds from 100 nsec/cm to 0.5 sec/cm. Signal delay is approximately 190 nsecs. Time base variable delay is selected by switch and variable by potentiometer to cover a range from 0.1 mS to 100 mS.

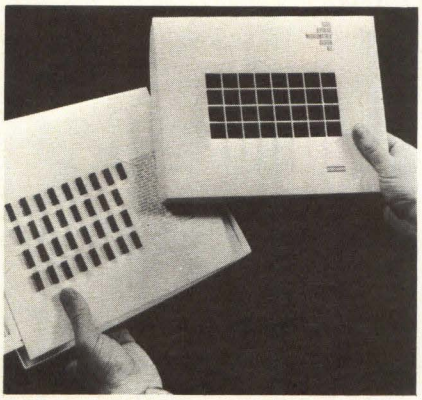
The voltage calibrator has square wave outputs of 5 mV and 50 mV and a rise time of less than 1 μsec. at a frequency of 1000 Hz ± 1 per cent. The differential input allows Y1 + Y2 signals to be coupled and displayed differentially on Y1 channel. The 6 cm × 10 cm display area has an illuminated internal graticule. The scope's size, 7″ high, 14″ wide and 18″ deep, and weight, 20 lb. make it ideal for field use. Motorola Communications & Electronics, Inc., Chicago, Ill.

Circle No. 229 on Inquiry Card

IC DECODER/DRIVER

The 8T01 integrated circuit decoder-driver can drive Nixie™ tubes directly and will interface with all popular DTL and TTL circuits. The circuit has a guaranteed 68-volt breakdown (with typical capability in excess of 100 volts) which insures Nixie tube operation without excessive background glow. No external discrete components are required for interfacing. Two other elements will soon be available, the 8T02 with built-in output transistors for driving incandescent lamp displays and the 8T03, a similar unit designed for use with external lamp drivers. Signetics Corporation, Sunnyvale, Calif.

Circle No. 224 on Inquiry Card

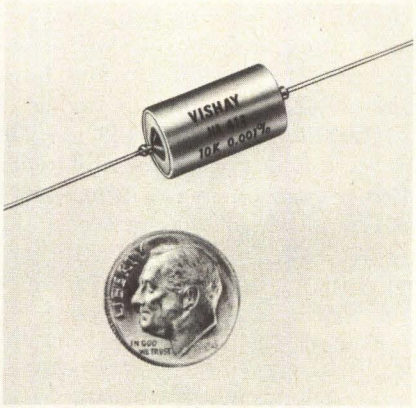


LSI DESIGN KIT

Systems manufacturers and circuit designers can now design their own custom LSI circuits, using a 4500 Bipolar Micromatrix™ Design Kit. The building blocks of the kit are a collection of CCSL (Compatible Current Sinking Logic) quarter cells in Dual In-Line packages, which can be assembled for an equivalent 4500 Micromatrix array. Designated as 4501 devices, the quarter cells such comprise a 4-input DTμL NAND gate offering logic options for input AND expansion, internal OR expansion or output open-collector. The 4501's are monolithic elements and components of the 32-gate 4500 Micromatrix array, are constructed with the aid of computer design incorporating two-layer metalization.

Purchase of the design kit entitles the buyer to a copy of Fairchild's 4500 Micromatrix Design Handbook, a 40-page guide that presents a comprehensive body of design suggestions keyed to the Micromatrix concept. The multi-color handbook represents a basic introduction to Micromatrix and features sections on cell assignments, interconnections, applications and testing. Many schematic diagrams and illustrative photos are included. When the 4500 breadboard design is complete, the user can then submit his logic block diagram and master layout sheet to Fairchild for customization of the metal interconnects and testing of the final array. This Micromatrix procedure results in fast delivery time and substantially lower engineering costs. Price is $99.00. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 200 on Inquiry Card



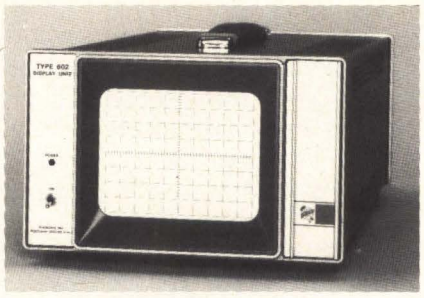
VERSATILE RESISTOR'S

HA Series resistors are usable at virtually any frequency (dc to 100 MHz. and above) with absolute tolerances to 0.001%, shelf stability of ±5ppm/yr. (guaranteed), standard TC's — for all resistance values — of 0±1ppm/°C. (absolute), 0.5ppm/°C. (tracking) and 0.25 ppm/°C. (matching) reported to be the most perfect resistor ever developed (with no trade-offs), the units are small enough for production use.

Depending on resistance value desired (30 ohms to 200 K ohms), the HA Series units are available in two basic diameters (3/8" and 1/2"), and lengths from 5/16" to 1 1/4". Maximum power, without derating, ranges from 1/2 watt to 1.25 watts. Available absolute tolerances (from 0.001% to 1%) are maintained under normal storage conditions within 5ppm/yr (0.0005%) by the hermetic sealing and oil-filling of the elastically mounted resistance elements within a shell. Vishay Resistor Products, Malvern, Pa.

Circle No. 201 on Inquiry Card

NEW PRODUCTS

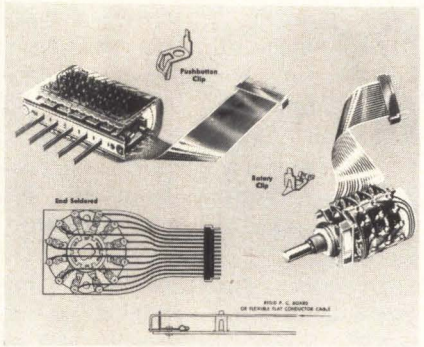


DISPLAY UNIT

The Type 602 Display Unit, is designed for viewing graphic and alphanumeric information from computers. Vertical (Y) and horizontal (X) amplifiers provide 1 MHz bandwidth and 100 mV/cm deflection factor. Phase difference between amplifiers is within 1° to 1 MHz. A linear DC coupled Z amplifier with 1 MHz bandwidth permits analog intensity modulation of the writing beam.

Dimensions are: height — 6 in; width — 8½ in; and depth — 17⅜ in. Weight is 17¼ lb. Also available in rack mounting configuration. Tektronix, Inc., Beaverton, Ore.

Circle No. 206 on Inquiry Card

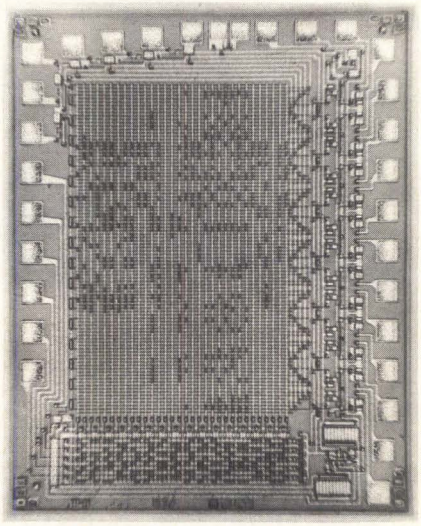


PRINTED CIRCUIT CLIPS

A series of space-saving printed circuit clips for rotary and push-button switch applications allows direct connections to virtually all types of PC boards and cabling. Engineers can now make easy, fast terminations to the new flexible flat conductor cables as well as to rigid PC boards simply by specifying the new clips on many Oak switches. The new clips with flexible circuitry also drastically reduce overall wiring errors.

The multi-purpose clips can be used for wrap-around or end connection of flexible flat cable or conventional PC board and are available for the Oak Types F, J and N as well as Type 130 and 131 push-button switches. Additional advantages include plug-in capability; positive-circuit assurance; complete elimination of harnessing; ability to make connections by pot-dip or hand soldering methods; and use of copper-clad material on either or both sides of the printed circuit. An extensive variety of clip finishes are offered: silver-plated brass; silver alloy; hard-gold alloy on special spring-base material; silver alloy, hard-gold plated; silver alloy with rolled-on hard-gold alloy. Oak Manufacturing Co., Crystal Lake, Illinois.

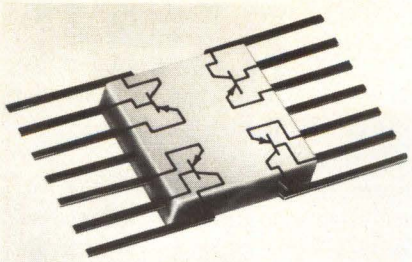
Circle No. 203 on Inquiry Card



READ-ONLY MEMORY DEVICE

A totally new Character Generator (Read-Only Memory device) with a fixed stored program, known as the MEM 5042, defines 32 different alpha numeric characters in a 5 by 13 character matrix. It has 13 unique outputs which are multiplexed out by five separate timing signals. The device utilizes four phase techniques throughout in order to minimize size and power dissipation and also features: 2-phase clock supply, medium speed operations, no dc power, all inputs zener network protected, stores 160, 13-bit words or 2,080-bits, and non-return to zero D.C. restored outputs. General Instrument Corp., Hicksville, L.I., N.Y

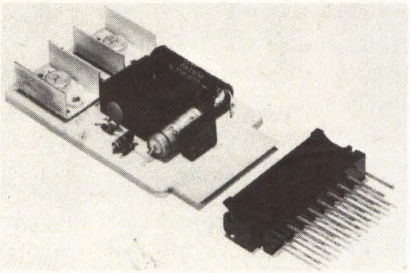
Circle No. 207 on Inquiry Card



QUAD TRANSISTOR

The first EIA registered quad transistor designated 2N5146, is designed for medium-current, high-speed switching and driver applications where space limitation or minimum lead inductance are imoperation, no dc power, all inputs of four individual PNP silicon Annular ™ transistors packaged in a 14 pin to -86 ceramic flat pack. Exclusive of leads, the package measures 0.25 by 0.25 inch and is 0.07 inch high. Typical characteristics for each of the four transistors are: $h_{FE} = 40$ @ $I_C =$ Adc, $V_{CE(sat)} =$ 0.7 Vdc @ $I_C = 1$ Adc, $C_{cb} = 11$ pF @ $V_{CB} = 10$ Vdc, $f_T = 250$ MHz @ $I_C = 50$ mAdc, and $t_s = 30$ ns @ $I_C = 1$ Adc. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 208 on Inquiry Card



REGULATED 12Vdc POWER SUPPLY

Model 1010 was designed to power integrated circuit modules. A transformer is supplied and is mounted separately. Input is 105-125V, 60Hz and the output is ±12VDC @ 300 ma. Either plus or minus may be grounded. Regulation is .01% line and load. Ripple is 500uV RMS. Recovery time is less than 50usec. P.C. card measures 500μV RMS. Recovery time is less than 50μsec. P.C. card measures 4.5″ x 2.6″ with components extending .593″ above the board. Circuitry is all silicon and operates up to 85°C. Output is short circuit proof and has current limiting. Fairlane Electronics, Long Valley, New Jersey.

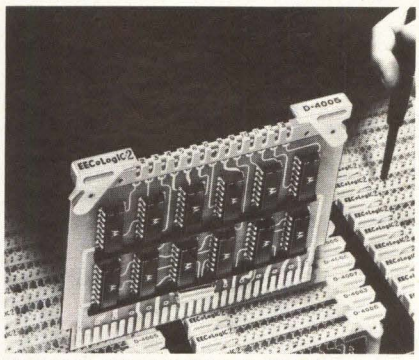
Circle No. 216 on Inquiry Card

HIGH CURRENT DIODE ARRAY

The RDA-10 single-chip diode array for core driver applications, shrugs off surge currents to 1,000 mA with a steady state forward current of 200 mA.

The dielectrically isolated device features a working inverse voltage of 30 volts, and provides a maximum reverse recovery time of 20 nsec, at extreme switching conditions of 450 mA forward to 45 mA reverse. Rated power dissipation is 400 mW. Ambient temperature range is −55°C to +125°C. The units are packaged in hermetically sealed TO-84 flat packs. Radiation Inc., Microelectronics Div., Melbourne, Fla.

Circle No. 209 on Inquiry Card

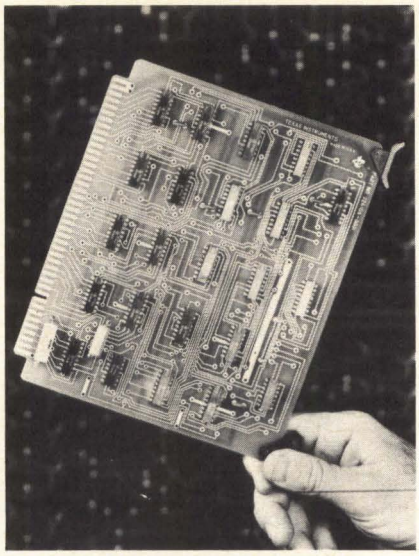


IC DIGITAL LOGIC CARDS

A line of DTL integrated circuit digital logic cards, called EECo-LogIC•2•, is designed to cut digital system costs. Prices per logic function have been reduced about 10%. More of any system fits in a standard 19″ drawer, four cards across and ½″ between cards (up to 6240 pin connections/drawer). The number of drawers can be halved and wiring costs are minimized since fewer drawers mean less interface wiring and cabling. Other features include: Wire Wrap and Termi-Point wiring capability using manual or automatic machines, as well as soldering. 13 Test Points located atop each card accept probes, clips or hooks and make system checkout fast. Integral Locking Extractor Handles hold each card securely in the card frame, identify the circuit and make card removal easy. Laminated Power Busses on each card and in the power wiring of each drawer reduce high frequency noise. Electronic Engineering Co. of Calif., Santa Ana, Calif.

Circle No. 225 on Inquiry Card

NEW PRODUCTS

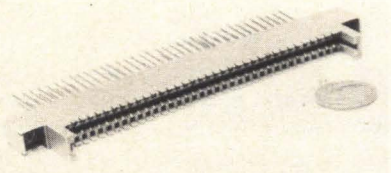


BCD-TO-BINARY CONVERTER

A compact modular converter, capable of accepting 6 BCD digits on 24 lines and converting them to 20-bit natural binary output, offers exceptional capability on a printed circuit card only six and one-quarter by seven and three-quarters inches.

It facilitates decimal to binary conversion in such areas as programming switches, computer input typewriters, and BCD outputs from digital voltmeters to a computer. By using TTL integrated circuit logic and simplified circuitry, the conversions take place at a much higher speed than is possible with older multi-step processing techniques. The converter uses a 5 volt dc supply and no external controls are required. Texas Instruments Inc., Apparatus Div., Houston, Texas.

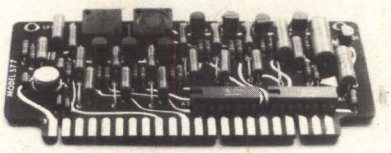
Circle No. 210 on Inquiry Card



CARD-EDGE CONNECTORS

Designed for high packaging density (mounting on .300-in. centers) in programmed wire wrap applications, Series 6309 connectors are suitable for mounting on chassis, p.c. boards and metal plate assemblies. Contacts are .025 inch square wire wrap posts, spaced on .100-in. square grid, and accommodate 1/16-in. p.c. cards. Compact, glass-filled nylon insulators feature extended card guides for easy card insertion and incorporate X and Y axis datum holes facilitating programmed wire wrapping and inspection. Contacts are preloaded in the insulator to maintain optimum contact force on the p.c. card; the cantilevered design affords maximum flexibility for resistance to set and for tolerance of card thickness variations. Elco Corp., Willow Grove, Pennsylvania.

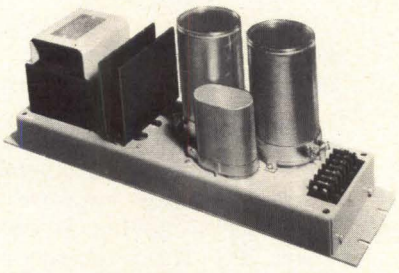
Circle No. 217 on Inquiry Card



DIGITAL TO ANALOG CONVERTER

Model 577 is a highly compact and versatile 8 bit digital-to-analog converter mounted on a standard "Blue Chip" logic card. A significant feature of the device is an integral input storage register that requires only positive inputs. Accuracy is better than 0.25%, output is 10 volts, and conversion rate is 100 kHz Data Technology Corp., Mountain View, Calif.

Circle No. 215 on Inquiry Card



REGULATED POWER SUPPLIES

An expanded line of regulated dc power supplies includes a total of thirty 50 and 60-hertz models with output voltages ranging from 10 to 200 volts dc. Featuring static-magnetic circuitry for reliability and

long life, they provide precise output voltage, close regulation and high efficiency. Output voltage will not vary more than ± 1% for a change in input voltage over the rated range of 97 to 130 volts ac. A change of 1% in frequency will only change the output voltage level approximately 1½%. Full-load efficiency ranges from 70 to 85% for normal output voltage levels.

These power supplies are designed to operate in ambient temperatures from —10° to 40°C. For every 40°C change in ambient temperature, the output voltage will change only about 1%. They can be installed with either polarity. Output voltage ripple level is 1% or less (RMS). All units provide electrical isolation between the power source and the d-c load. As an additional safety feature, short circuit current is limited to approximately 200 percent of rated value. General Electric Co., Schenectady, N.Y.

Circle No. 221 on Inquiry Card

DISPLAY UNIT

The PD-3 program-display accessory for use with Clary's Model DE-600 digital computer, displays complete information on each programmed step as it is being executed by the DE-600.

The PD-3 displays the same algebraic symbols and decimal numbers used in operating and programming the DE-600. Thus, there is no need to translate from machine language when using the PD-3 to debug programs. The display shows the program step number; the operation being performed; and the memory locations and registers involved. On program steps which include input-output and shifting, the PD-3 displays word-length and decimal-point control data.

In many applications, Clary's extensive library of programs obviates the need for program development by the user. However, many users are developing their own programs for the DE-600, and the PD-3 will aid them in program checkout. Clary Datacomp Systems, Inc., San Gabriel, Calif.

Circle No. 220 on Inquiry Card

PLUG-IN INTERFACE

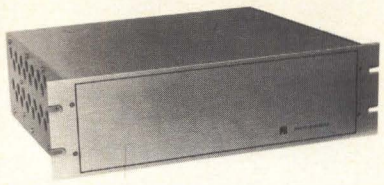
A plug-in interface, called Logic-Pak, interfaces the IBM model 735 Selectric typewriter to the DEC PDP-8, 8/S and 8/I computers. By converting IBM code to teletype code and vice versa, the setup does away with teletype and becomes the standard means of input and output for DEC computers.

The unit allows a user to enjoy many advantages of the Selectric model 735, which is the heavy-duty typewriter used with the IBM 360 systems. These advantages are: more accurate input and output; over 150 words per minute; upper and lower case; two-color ribbon shift; automatic tab control; and changeable type balls which may include mathematical and foreign language symbols. It produces quality presentation copy with easy handling of multi-part forms, and accepts rolls or sheets up to 15½ inches wide. It is a familiar terminal with a sculptured-touch keyboard. Error parity checking, and reverse and half-line indexing are available options.

Logic-Pak includes documentation and code conversion tapes to convert IBM code to ASCII and vice versa. Software also provides overlay program tapes for operating DDT and other DEC routines. Hardware includes a pushbutton keyset which will generate the 12 additional codes found on the teletype (alt mode, rubout, CTRL/ form, etc.), decoder and encoder cards which recognize and produce functional codes such as tab, space, carriage return, back space, index, ribbon shift and upper and lower case, and the logic and circuitry necessary to properly gate and condition selection magnets. It is a cabinet unit with an integral power supply, plus all the necessary cables and plugs for installation. Logic, Inc., Detroit, Mich.

Circle No. 222 on Inquiry Card

NEW PRODUCTS



CORE MEMORY SYSTEM

An economical, compact, modular, Random Access Core Memory System Model 470, offers storage capacity up to 4,096 words per module, 6 to 26 bits, with word expandability to 32,768 by adding on additional modules. The memory will operate at speeds of 1.75 μs Full Cycle and 1.0 μs Half Cycle; Access Time is 750 ns. A special "Memory Select" control input, in conjunction with unique expansion techniques, allows for easy decoding of memory blocks.

The Model 470 can be supplied with or without Power Supply, and requires no external cooling to operate over the temperature range of 0°C. to 50°C.

Physical dimensions, are: Height — 5.25 inches; Width — 19.0 inches, relay rack mounting; Depth — 19.0 inches, includes mating interface connectors. Weight is 35 pounds. Fabri-Tek Incorporated, Edina, Minn.

Circle No. 228 on Inquiry Card

IC DRIVER/DECODERS

An IC driver/decoder for driving incandescent lamps in IEE rear-projection readouts, utilizes integrated circuits for gating and coding resulting in a smaller, more reliable instrument. Other advantages include internal data storage for pulsed operations or single line for strobe and re-set, low power consumption (typically 500 mW), same logic voltage as used with IC's and high noise immunity (1.0 V.) which prevents false decimal indication.

All models incorporate forbidden code rejection eliminating ambiguous displays. Standard 8-4-2-1 BCD code accepted; equivalent decimal output provided. Industrial Electronic Engineers, Inc., Van Nuys, Calif.

Circle No. 218 on Inquiry Card

QUAD 2-INPUT NOR GATE

A digital IC quadruple two-input NOR gate, with "Phantom-OR" capability, offers the convenience and economy of four extremely high speed gates in one package. It features a typical propagation delay of 3.6ns; provides a typical noise margin of 40 per cent of the logic swing; and exhibits excellent temperature tracking through the use of an internal reference voltage source. The CD2153 comprises four gates each having two-inputs and one NOR output in a 14-lead hermetically sealed ceramic flat pack. In addition to its inherent high speed, and excellent noise immunity, the new quad two-input gate can drive a 100-ohm transmission line and is logic-level compatible with all the other circuits in the CD2150 family. RCA/Electronic Components, Harrison, N.J.

Circle No. 205 on Inquiry Card

LITERATURE

Solid State Sensors

A 24-page booklet on solid-state-controlled sensors and protective devices includes complete descriptions of functions, applications, and graphic representations for 3-phase average voltage sensors, over voltage sensors, under voltage sensors, adjustable differential voltage sensors, frequency sensors and 3-phase rotation sensors. Guardian Electric Mfg. Co. of Calif., Inc. Culver City, Calif.

Circle No. 301 on Inquiry Card.

Computer Talk

A series of quarterly bulletins, covering problems unique to computer users, called "Computer Talk", deals with a variety of subjects pertaining to the electronic data processing field. The initial issue covers the handling and storage of computer tape. 3M Company, Magnetic Products Division, St. Paul, Minn.

Circle No. 305 on Inquiry Card.

Data Set

A 12-page brochure describing the 26C Duobinary-Datatel (TM) System includes an equipment description, photographs and performance information. Lenkurt Electric Co., Inc. San Carlos, Calif.

Circle No. 310 on Inquiry Card.

Terminal Blocks

Completely new line of terminal blocks and accessories, is described in this 8 page illustrated bulletin 500.2. Each terminal block is presented pictorally in both color and black and white illustrations, and is fully described as to installation procedures. Catalog specifications are also given. Also included are illustrations of the various accessories, and catalog information. A temperature rating graph is shown and instructions for finding current rating are given. The Thomas & Betts Co., Elizabeth, N. J.

Circle No. 307 on Inquiry Card.

Sub-Miniature Lamps

A 28-page color catalog on high reliability illumination with miniature and ultra-miniature lamps, lists complete characteristics for 144 separate lamps. Included are many Military Standard and U. S. A. Standards Institute items. Also featured is an 8 page section with facts on illumination, lamp design and specialized lighting techniques, plus an improved light chromaticity diagram. Los Angeles Miniature Products, Inc., Gardena, Calif.

Circle No. 304 on Inquiry Card.

Functional Semiconductor Assemblies

A 12-page brochure presents in basic terms the advantage of using solid-state assemblies in all types of consumer, industrial and military systems plus gives insight into what to look for in your equipment that could benefit from cost and time-saving advantages. "One-purpose, one-purchase, one-time" advantage is stressed with special emphasis on specific, illustrative examples — including circuits — of a variety of functions that have been engineered and designed to fit a wide spectrum of customer-specified electrical and mechanical criteria. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 303 on Inquiry Card.

Dry-Type Transformers

A veritable encyclopedia of dry-type transformers, this 72-page catalog, lists full engineering information, including specifications and performance curves and similar charts. Also featured in a new line of oil- and Askarel-filled power transformers and a unique SBW line of control transformers. In addition, other specialty products such as saturable reactors, power supplies, voltage regulators and accessories are listed. Hevi-Duty Electric, Division of Sola Basic Industries, Goldsboro, N.C.

Circle No. 306 on Inquiry Card.

LITERATURE

Systems Computer Manual

A 400 page manual for use with the DATA 620/i systems computer, contains major sections on the features and operation of the 620/i; a system reference; a programming reference; FORTRAN reference and operating instructions; subrouting descriptions; and interface reference. The DATA 620/i is a system-oriented digital computer, designed to fill the gap between special purpose digital hardware and general purpose computers. Variam Data Machines, Newport Beach, Calif.

Circle No. 311 on Inquiry Card.

D-To-A Conversion System

"Y" Series Digital-to-Analog Conversion Systems; are emphasized in a brochure which illustrates elimination of problems of logic level compatibility, analog-digital isolation, and data input coding. System structure and operation are discussed, including features such as the flexible addressing capability and the availability of two Data Distributors to provide different degrees of sophistication in system control. A functional block diagram, timing diagram, photographs and system specifications are included. Adage, Inc., Boston, Mass.

Circle No. 319 on Inquiry Card.

Epoxy Resins

Bulletin No. 28 describes method of applying epoxy systems and the required hardeners to obtain improved product performance, and increased productivity. Complete discussion is given on applications, especially for requirements in electronic cooling equipment, utilizing epoxies for bonding parts, for dielectric coatings, and in casting or potting of components. Specific examples are discussed along with procedures for use of epoxies with aluminum, copper, steel and silver. Wakefield Engineering Inc., Wakefield, Mass.

Circle No. 302 on Inquiry Card.

Test Equipment

Insulation test equipment, electronic test and measuring instruments, high-voltage power supplies, and automatic component testers are comprehensively covered in 40-page catalog 31. The section on insulation test equipment provides complete technical data and specifications. A special section is also devoted to automatic component testers. Beckman Instruments, Inc., Cedar Grove, N. J.

Circle No. 309 on Inquiry Card.

Printed Circuit Connectors

A family of low cost, commercial edge card printed circuit connectors is detailed in a four page brochure. Test performance data is listed in table form so that a performance/cost comparison can readily be made with your current requirements. Viking Industries, Inc. Chatsworth, Calif.

Circle No. 308 on Inquiry Card.

Systems Hardware

A 36-page catalog, "System Mounting Hardware, Cabling and Power Supplies," describes a recently introduced line of interlocking systems hardware that reduces the mechanical and electrical problems of constructing a digital system. Through exploded views, dimension drawings, and photos, the catalog shows how various pieces can be integrated into a system. Complete specifications and loading rules are given for individual items. Scientific Data Systems, Santa Monica, Calif.

Circle No. 312 on Inquiry Card.

Signal/Power Transistors

A line of silicon and germanium small signal and power transistors for military, industrial and commercial applications, is presented in a 40-page, 3-color catalog. Each family of transistors is presented in a separate section and includes typical h_{FE}, $V_{BE}(sat)$ and $V_{CE}(sat)$ curves, along with specification charts, outline dimension drawings and actual size photos of the standard cases. Brief suggested applications are included. Solitron Devices, Inc., Riviera Beach, Fla.

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LITERATURE

Indicator Lamps

Condensed catalog CMD-2, contains information relating to standard industrial lamps, CM8 miniature, thin line and line filament lamps, neon glow lamps, and telephone slide lamps. All lamps are listed in numerical order to facilitate locating a specific lamp type. Each listing indicates design voltage and current, mean spherical candle power, base type, bulb type, filament type, average life, maximum diameter and length. Chicago Miniature Lamp Works, Chicago, Ill.

Circle No. 300 on Inquiry Card.

Encoder Applications

An 8-page monthly engineering publication called Application Topics, describes the use of shaft encoders for readout and control of diffractometers, spectro-photometers, goniometers, ellipsometers, film readers, and plotters. Actual applications are given in a case history format. Free subscriptions as well as back issues are available. Theta Instrument Corp., Fairfield, N. J.

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Potentiometers/Resistors

Potentiometers, field-assembled controls, power rheostats and resistors are described in this 32-page illustrated catalog. Included are photographs, engineering drawings, complete technical specifications and dimensional information. A special section describing military-qualified potentiometers is also provided. Clarostat Mfg. Co., Inc., Dover, N. H.

Circle No. 320 on Inquiry Card.

Precision Switches

Four page 2-color condensed catalog contains 28 illustrations and technical descriptions of tab type thumbwheel switches, panel sealed pushbutton switches, rotary selector switches and custom assemblies. Chicago Dynamic Industries, Inc., Precision Products Division, Chicago, Ill.

Circle No. 315 on Inquiry Card.

ADVERTISERS' INDEX

4 breakthroughs: new NIXIE® tube

size

.530″ dia. x 1.5″ for IC compatibility — largest numeral height provides best readability.

anode strobing

new design permits all like-numerals to be driven in parallel for time sharing operation with improved brightness.

pin spacer

simplifies both PC board layout and tube insertion.

price

in quantities of 1,000 — only **$3.95** each.

ACTUAL SIZE

This new tube, type B-5750, has been engineered to achieve all these outstanding breakthroughs in a single design. The new slim-line tube not only has two internal decimal points but also has an "in-line" lead arrangement which is compatible with dual in-line IC's. In addition, the numeral aspect ratio has been designed to provide the optimum in readability and viewing distance.

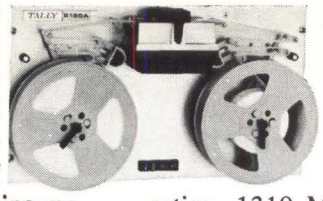
The movable pin spacer – standoff, which is used to align the tube pins for ease of PC layout and insertion, is part of the tube assembly.
The anode strobing/time sharing operation permits substantial reduction in driver costs for many multi-digit display applications. For more information on these and other features contact your nearest Burroughs representative or sales engineer, or write: *Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Department N6, Plainfield, New Jersey 07061 TEL: (201) 757-5000.*

Burroughs

CIRCLE NO. 54 ON INQUIRY CARD

New Tally HR 150 perforated tape readers run for reliability. With zero preventive maintenance, the reader is designed for a minimum life of 10,000 hours. In typical reader applications, minor failures would be experienced less than once a year. Day after day, month in, month out, these new readers will give you "full bore" performance without costly downtime.

These remarkable "state of the art" readers operate asynchronously and bidirectionally at 150 characters per second and feature a compact, self-contained design, low noise level and essentially zero preventative maintenance. Heart of the new reader is a new stepping motor technique which permits true pulse by pulse operation and avoids the wear and tear caused by continuously moving parts.



Tape loading is easy and fast. Reeling tension arms can be locked upright for convenient tape threading. Rewind is bidirectional at 40 inches per second.

For full price, delivery, and technical information, please write Tom Tracy, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) MA 4-0760. In Europe and the U.K., address Tally, Ltd., 6a George Street, Croydon, Surrey, England. Phone: MUN 6838.