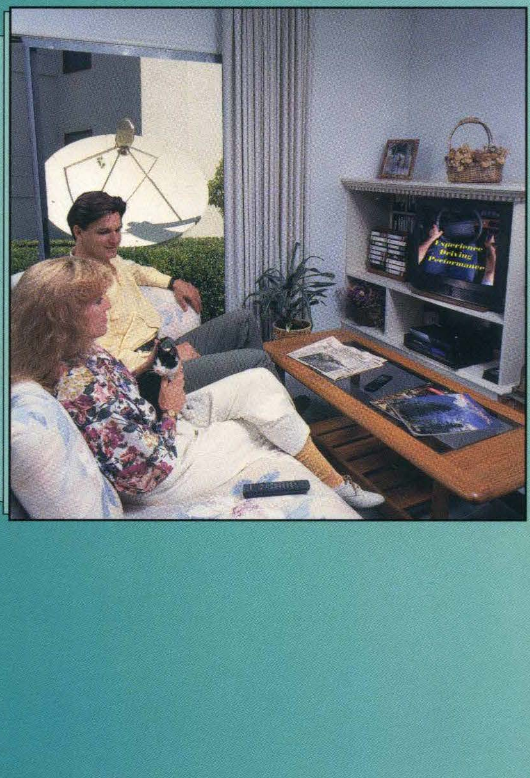
ZiLOG

Z8® Microcontrollers

For Computer Peripheral and Consumer Electronics Applications



Includes Specifications and Application Notes for the following parts:

Z86C07
Z86C08
Z86E08
Z86C11
Z86C12
Z86C21
Z86E21
Z86C61/62/96
Z86C63/64
Z86C91
Z86C93

Product Specifications Databook

ZiLOG Z8® Microcontrollers Databook

ZILOG

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For Peripherals and Consumer Electronic Products

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- Z86C93

Databook

DC 8305-01

Z8® Microcontroller Databook

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INTRODUCTION

Zilog's Focus on Application Specific Products Helps You Maintain Your Technological Edge

I

Zilog's Consumer products are suitable for a broad range of applications, from general-purpose uses to application specific markets such as IR remote control, security systems, cable TV receivers, and TV satellite systems. Whichever device you choose, you'll find a comprehensive feature set, easy-to-use development tools and, application specific expertise to help speed your design into production. Once designed in, the product family allows easy migration of your application using the same hardware and software.

Z86C07 CMOS Z8® 8-Bit Microcontroller
The Z86C07 is a member of the Z8® single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. This device is housed in 18-pin DIP and 18-pin SOIC packages and is manufactured in CMOS technology. The Z86C07 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, and industrial applications.

Z86C08 CMOS Z8® 8-Bit Microcontroller
The Z86C08 is a member of the Z8® single-chip microcontroller family with 2 KBytes of ROM and 124 bytes of general-purpose RAM. As in the Z86C07, this device is housed in 18-pin DIP and 18-pin SOIC packages and is manufactured in CMOS technology. The Z86C08 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

Z86E08 CMOS Z8® 8-Bit Microcontroller
Zilog's Z86E08 is the OTP version of the Z86C08 with 2 Kbytes of OTP. The device is housed in an 18-pin DIP, and is manufactured in CMOS technology. The device allows for easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

Z86C11 CMOS Z8® 8-Bit Microcontroller
The Z86C11 features 4 Kbytes of ROM and 256 bytes of RAM. The MCU is housed in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP package. The ROMless pin option is available on the 44-pin versions only. Having the ROM/ROMless selectively, this device offers both external memory and preprogrammed ROM. This enables the Z8 microcontroller to be used in high volume applications, or where code flexibility is required.

Z86C12 CMOS Z8® In-Circuit Emulator Microcontroller
The Z86C12 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, easy hardware/software system expansion, a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

Z86C21 8K ROM CMOS Z8® Microcontroller

Zilog's Z86C21 CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The Z86C21 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many consumer applications.

Z86E21 CMOS Z8® Microcontroller With 8K OTP

The Z86E21 is a pin compatible, OTP version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbytes of ROM on the Z86C21. This MCU is housed in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The Z86E21 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation, easy hardware/software system expansion along with low cost and low power consumption.

Z86C61/62/96 CMOS Z8® Microcontroller

The Z86C61/62/96 is a member of the Z8 single-chip microcontroller family. It is pin compatible with the Z86C21 but has twice the on-board memory with 16 Kbytes of ROM. It offers all the outstanding features of the Z8 family architecture. The device provides up to 16 output address lines permitting an address space of up to 48 Kbytes of external program and data memory each. The 256-byte register file consists of 236 general-purpose registers, four I/O port registers, and 16 status and control registers.

Z86C63/64 32K ROM CMOS Z8® Microcontroller

The Z86C63/64 is a 32K ROM version of the Z8 single-chip microcontroller family. It is pin compatible with the Z86C61/62 but has twice the on-board memory with 32 Kbytes of RAM. Compatibility between the C21, C61 and C63 allows users to build on their existing hardware and software design, providing the flexibility needed to meet the challenge of todays market needs.

Z86C91 CMOS Z8® ROMless Microcontroller

The Z86C91 is a member of the ROMless Z8 single-chip microcontroller family with 236 bytes of RAM. The MCU is packaged in a 40-pin DIP, 44-pin PLCC or a 44-pin QFP. The Z86C91 is a ROMless device that offers the use of external memory which enables this Z8 MCU to be used where code flexibility is required.

Z86C93 CMOS Z8® Multiply/Divide Microcontroller

The Z86C93 is a CMOS ROMless Z8 Microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers. A capture register and a fast decrement mode is also provided. The device is housed in a 40-pin DIP, 44-pin PLCC, 44-pin QFP, or 48-pin VQFP package and is manufactured in CMOS technology. Besides the four additional signals (SCLK, IACK, /SYNC, and /WAIT), the Z86C93 is compatible with the Z86C91, yet is offers a much more powerful mathematical capability,

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Z86C07

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP Package
- Low Cost
- 3.0 to 5.5 Volt Operation Range
- Low Power Consumption; 50 mW (typical)
- Low Voltage Protection
- Fast Instruction Pointer; 1 µs at 12 MHz
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines
- Three Digital Inputs at CMOS Levels
- Eleven Digital Inputs at CMOS Levels; Schmitt-Triggered
- Extended Temperature Operation –40°C to +105°C
- 2 Kbytes of ROM
- 124 Bytes of RAM,
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds 8 and 12 MHz
- On-Board Power-On Reset Circuit
- Permanently Enabled Watchdog Timer
- Two Comparators with Programmable Interrupt Polarity.
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86C07 Microcontroller Unit (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C07 is a member of the Z8 single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is housed in 18-pin DIP, and 18-pin SOIC, and is manufactured in CMOS technology. The Zilog Z86C07 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

The Z86C07 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, and industrial applications.

For applications which demand powerful I/O capabilities, the Z86C07 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with real-time tasks such as counting/timing and I/O data communications, the Z86C07 offers two on-chip counter/timers with a large number of user selectable modes. Also, there are two on-board comparators that can process analog signals with a common reference voltage (Figure 6).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

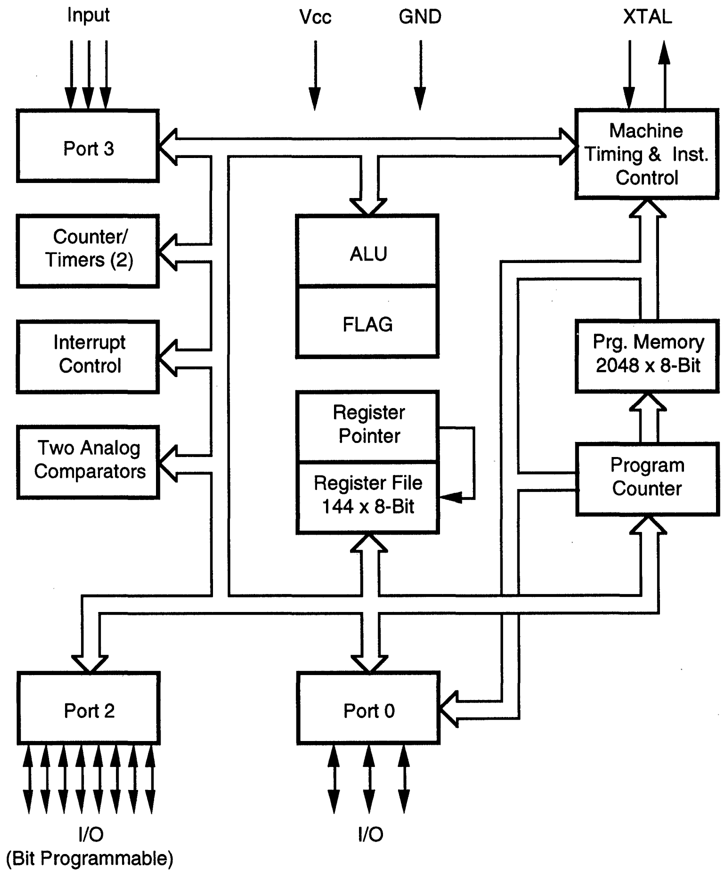


Figure 1. Functional Block Diagram

PIN DESCRIPTION

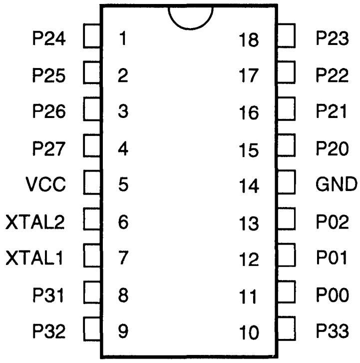


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	Input
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	Input
15-18	P20-P23	Port 2, Pins 0, 1 ,2, 3	In/Output

1

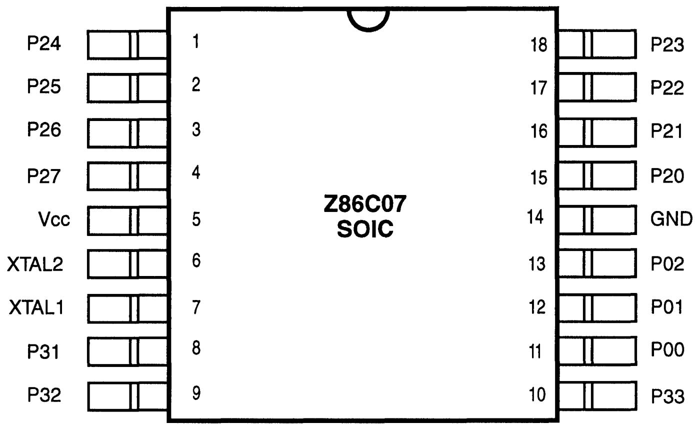


Figure 3. 18-Pin SOIC Pin Configuration

Table 2. 18-Pin SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	Input
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1, 2	In/Output
14	GND	Ground	Input
15-18	P20-P23	Port 2, Pin 0, 1, 2, 3	In/Output

PIN DESCRIPTION (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, nibble programmable, bidirectional, CMOS compatible I/O port. These three I/O lines can be configured under software control to be an input or output (Figure 4).

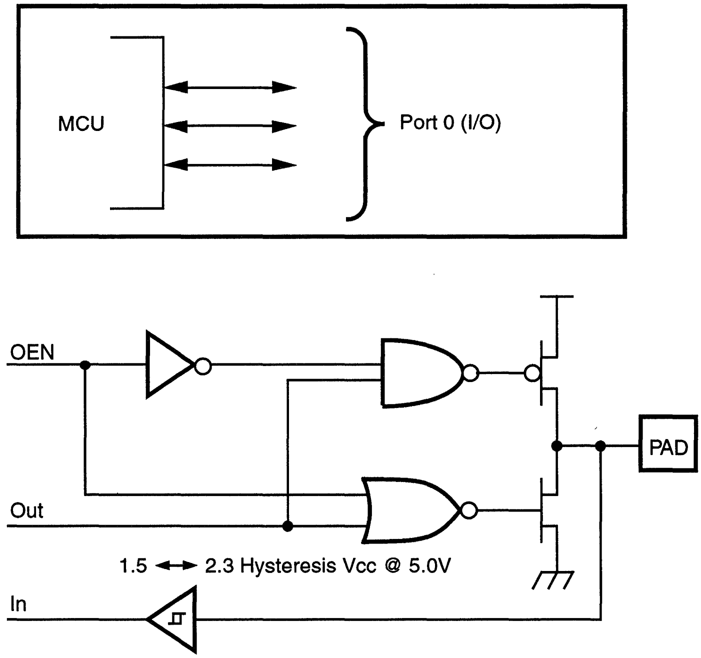


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 5).

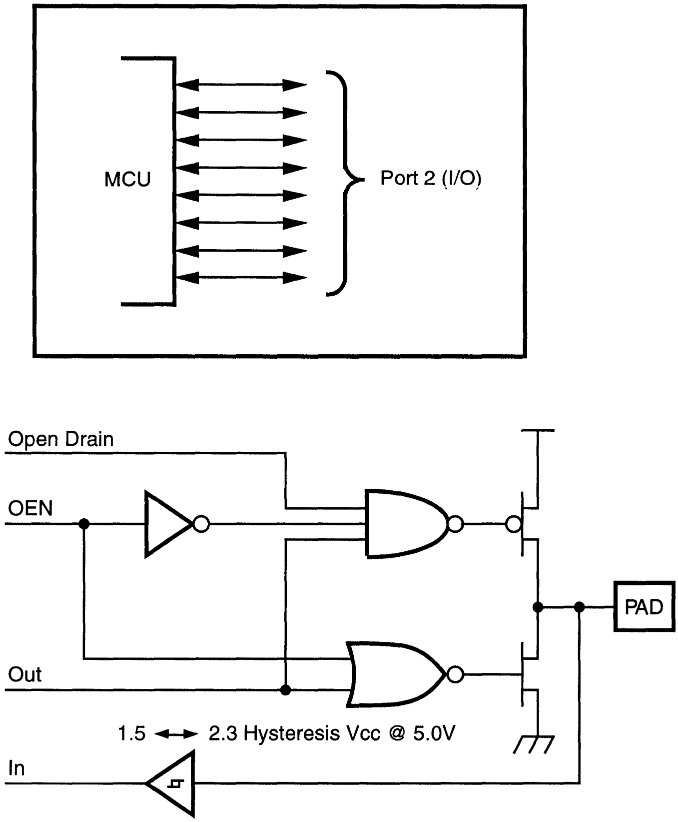
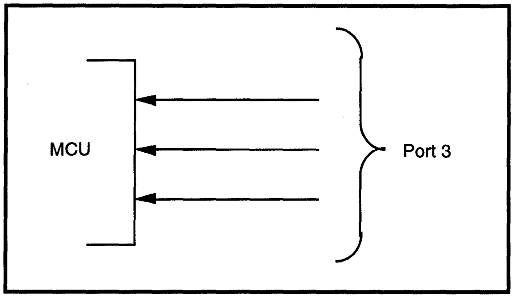


Figure 5. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 6).



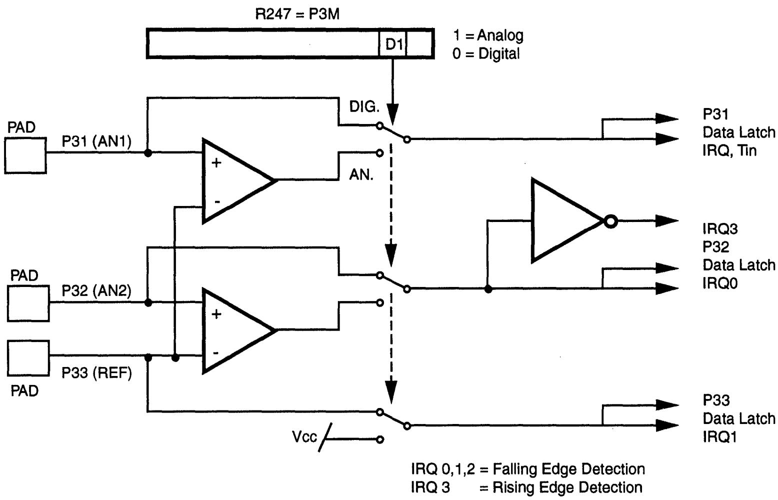


Figure 6. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The Z8 MCU incorporates special functions to enhance the Z8's versatility in consumer, industrial, and advanced technologies applications.

Reset. Upon power-up the Power-On Reset circuit waits for 50 µsec plus 18 crystal clocks and then starts program execution at address %000C (HEX) (Figure 7). Reference the Z86C07 control registers' Reset value (Table 3).

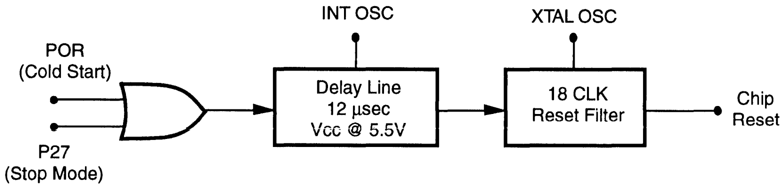


Figure 7. Internal Reset Configuration

Table 3. Z86C07 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FE	SPH	U	U	U	U	U	U	U	U	Not used, stack always internal
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 3 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86C07 can address up to 2 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

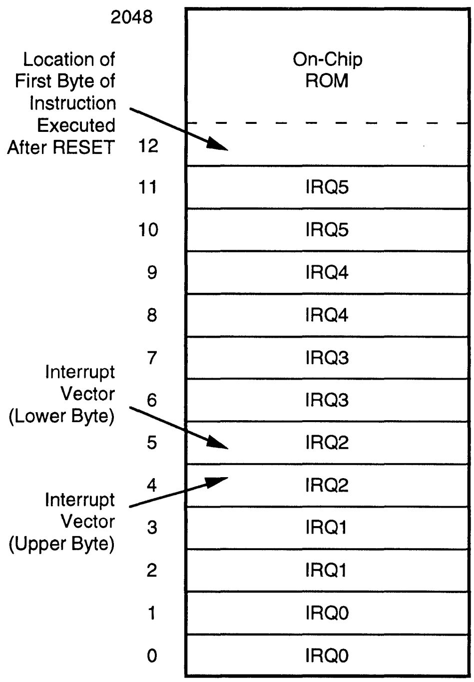


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers (R3-R0, R127-R4 and R255-R241, respectively - Figure 9). The Z86C07 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Reserved	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	To Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240 128	Not Implemented	
127 4	General Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 9. Register File

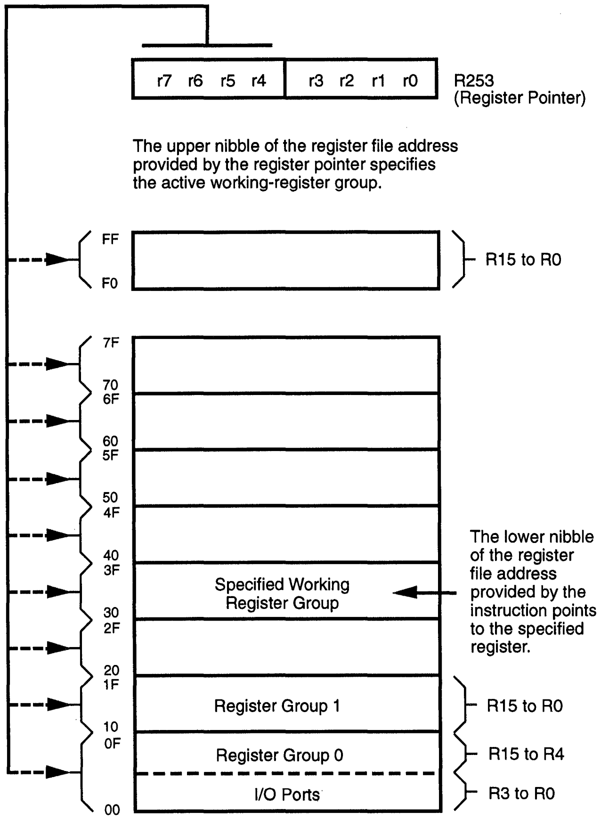


Figure 10. Register Pointer

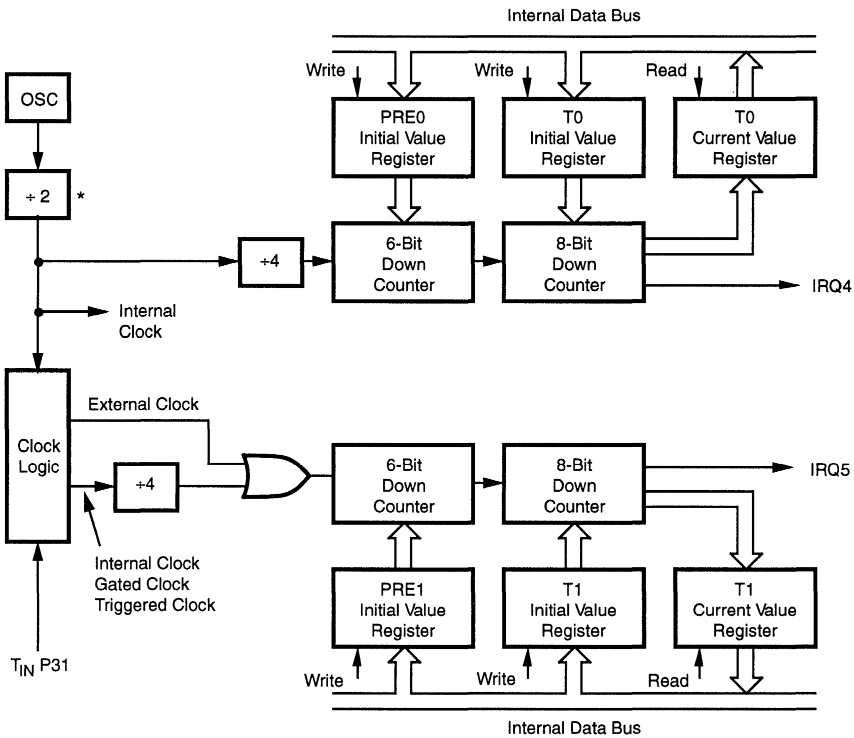
Stack Pointer. The Z86C07 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.



* Note: Divide-by-two is not used in Low EMI Mode.

Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C07 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C07 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

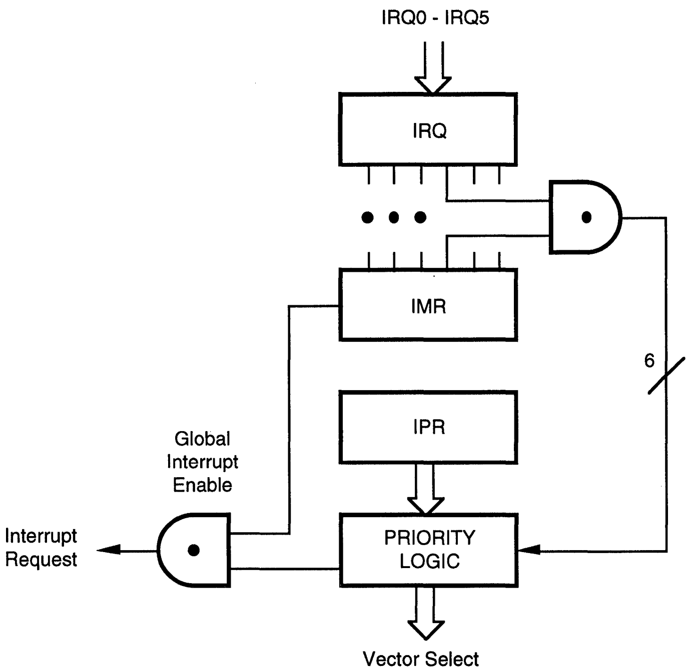


Figure 12. Interrupt Block Diagram

Clock. The Z86C07 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (capacitance is between 10 pF to 250 pF which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device ground pin 14 (Figure 13).

Note that the crystal capacitor loads should be connected to V_{SS}, pin 14 to reduce Ground noise injection.

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location 000C (HEX). An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC}. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP Mode.

Program execution under both conditions begins at location 000C (HEX). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state.

To use the P27 release approach with STOP Mode, use the following instruction:

```
OR      P2M, #80H
NOP
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate SLEEP instruction. i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is permanently enabled. The WDT should be refreshed at least every 10 msec; otherwise, the Z86C07 resets itself.

WDT = 5F (HEX).

Opcode WDT (5FH). Execution of the command clears the WDT counter. This has to be done at least every 15 msec. Otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 µsec +18 XTAL clock cycles. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

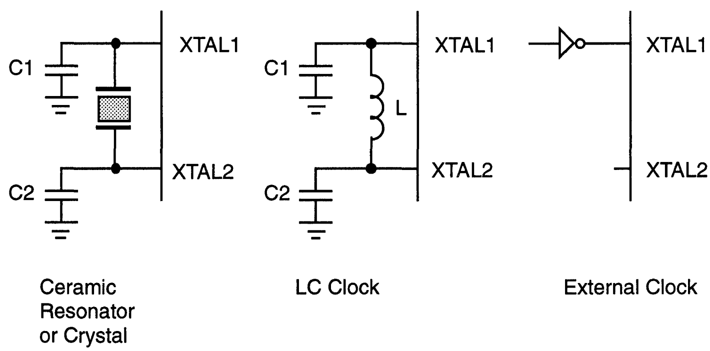


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection (V_{LV}).The Low Voltage trip voltage (V_{LV}) is less than 3 volts and above 1.4 volts under the following conditions:

Maximum (V_{LV}) Conditions:

Case 1 T_A = –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

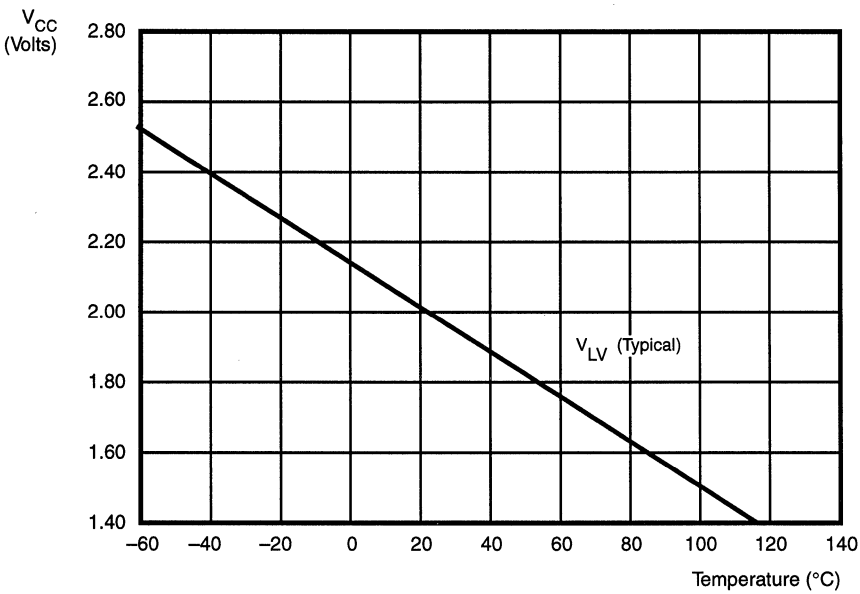
Case 2 T_A = –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	–40°C	0°C	+25°C	+70°C	+105°C
V_{LV}	2.55	2.4	2.1	1.7	1.6



Power-On Reset threshold for V_{CC} and 4 MHz V_{LV} overlap

Figure 14. Typical Z86C07 V_{LV} vs Temperature

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:
*Voltages on all pins with respect to GND
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 15).

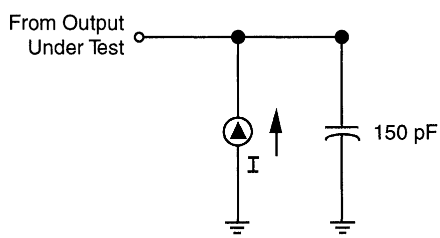


Figure 15. Test Load Diagram

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.0V

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage	3.0V		12		12		V	I_{IN} = 250 µA
		5.5V		12		12		V	I_{IN} = 250 µA
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.75	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V	
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltge	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA [5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA [5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
		5.5V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA [5]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA [5]
		3.0V		0.4		0.4		V	Low Noise @ 0.5 mA
		5.5V		0.4		0.4		V	Low Noise @ 0.5 mA
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max [5]
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max [5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV	
		5.5V		25		25	10	mV	
V_{LV}	V_{CC} Low Voltage			2.7		2.95	2.1	V	@ 1 MHz Max, Int. CLK Freq
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}
V_{ICMR}	Input Common Mode Range		0	V_{CC}–1.0	0	V_{CC}–1.5		V	

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		4.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		1.2		1.2	0.4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6		1.6	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		1.5		1.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9		1.9	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		2.0		2.0	0.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4		2.4	0.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal/Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] For 2.75V operating, the device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.

[4] V_{CC} = 3.0V to 5.5V

[5] Standard Mode (not Low EMI Mode)

DC ELECTRICAL CHARACTERISTICS
Timing Diagrams

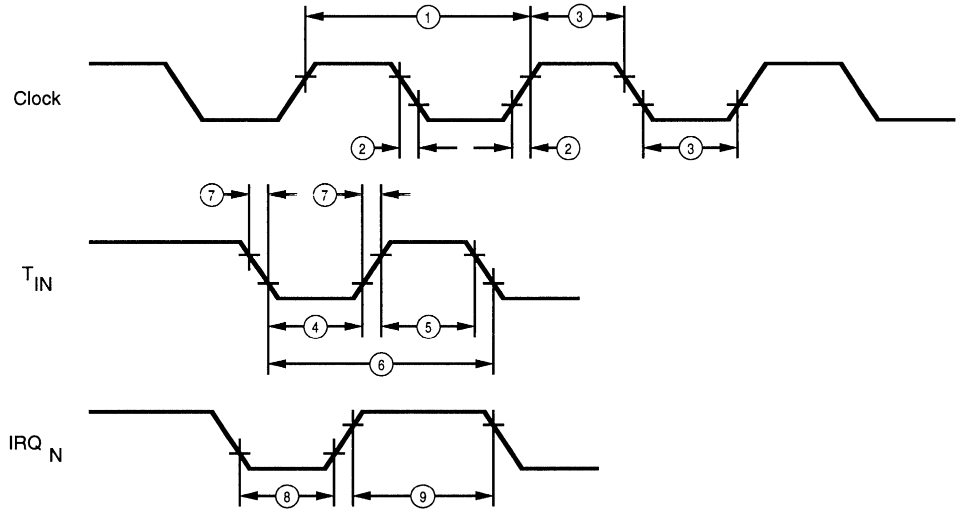


Figure 16. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode)

				T_A = –40°C to +105°C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	100,000	83	100,000	ns	[1]
			5.5V	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise	3.0V		25		15	ns	[1]
		and Fall Times	5.5V		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		ns	[1,2]
		Low Time	5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	5TpC		5TpC			[1]
		High Time	5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V		25		25	ms	[1]
		Delay Time	5.5V		10		10	ms	[1]
11	Tpor		3.0V		24		24	ms	[1]
			5.5V		12		12	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).

Low Noise Version

Low EMI Emission

The Z86C07 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode, –0°C to +70°C.
- All pre-driver slew rates reduced to 10 ns typical.
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z86C07 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements were made while operating the Z86C07 in three states: (1) Idle condition; (2) static output; (3) switched output.

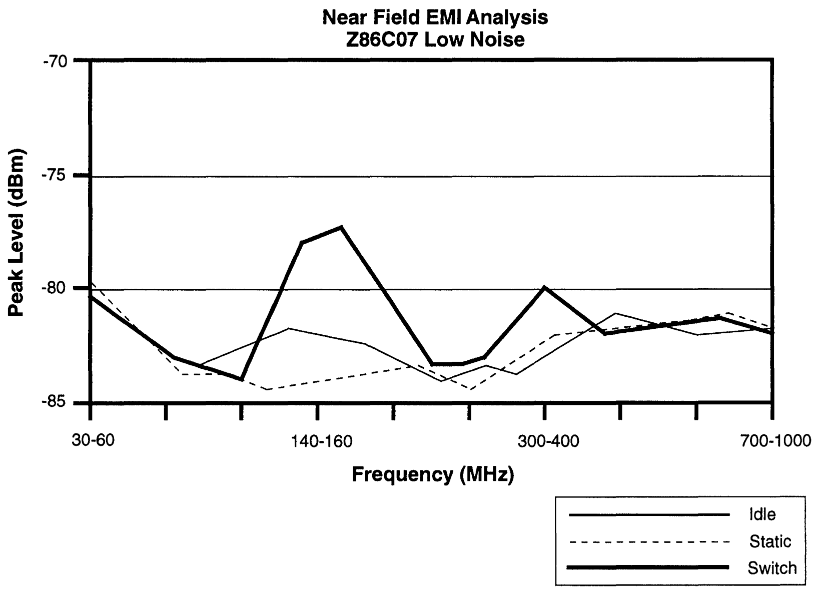


Figure 17. Low Noise Analysis

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V		25		25		25		25	ms	[1]
		Delay Time	5.5V		12		12		10		10	ms	[1]

Notes:
[1] Timing Reference uses 0.8 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).

Z8 CONTROL REGISTER DIAGRAMS

R241 TMR

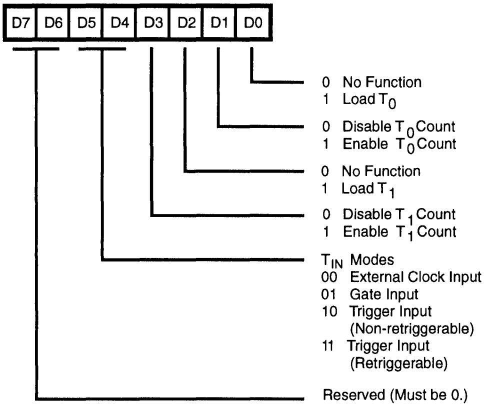


Figure 18. Timer Mode Register ($F1_H$: Read/Write)

R242 T1

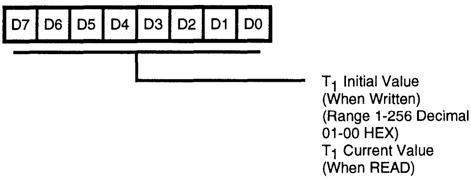


Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

R243 PRE1

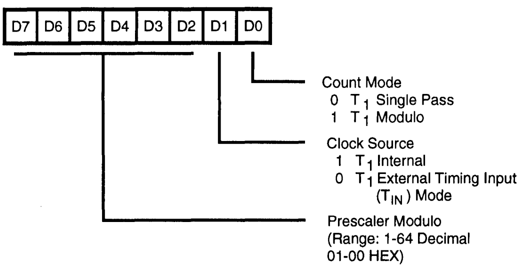


Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

R244 T0

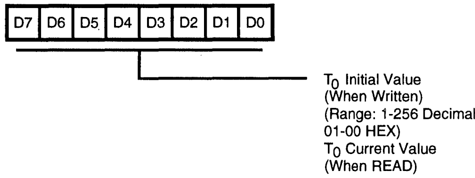


Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

R245 PRE0

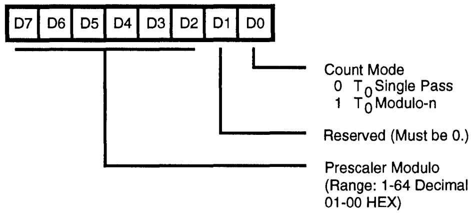


Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

R246 P2M

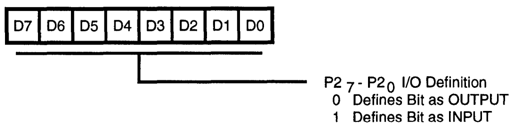


Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

R247 P3M

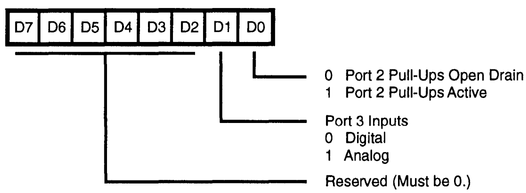


Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

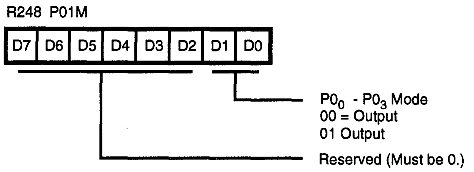


Figure 25. Port 0 and 1 Mode Register ($F8_H$: Write Only)

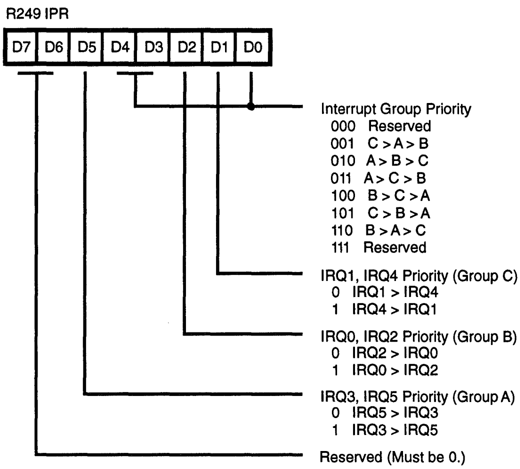


Figure 26. Interrupt Priority Register ($F9_H$: Write Only)

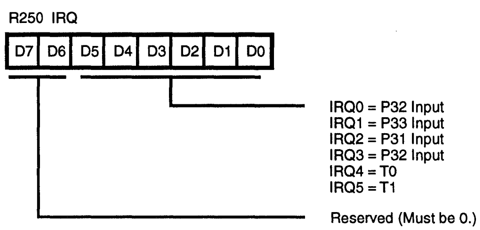


Figure 27. Interrupt Request Register (FA_H: Read/Write)

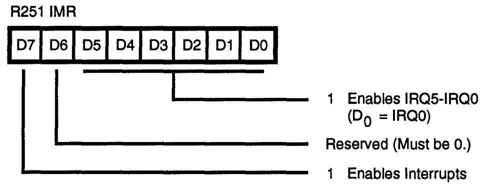


Figure 28. Interrupt Mask Register (FB_H: Read/Write)

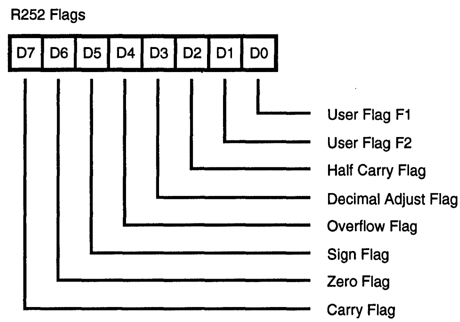


Figure 29. Flag Register (FC_H: Read/Write)

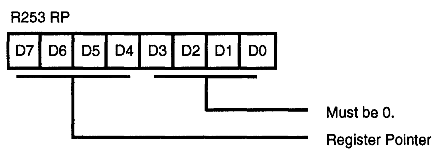


Figure 30. Register Pointer (FD_H: Read/Write)

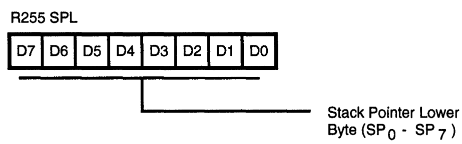


Figure 31. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

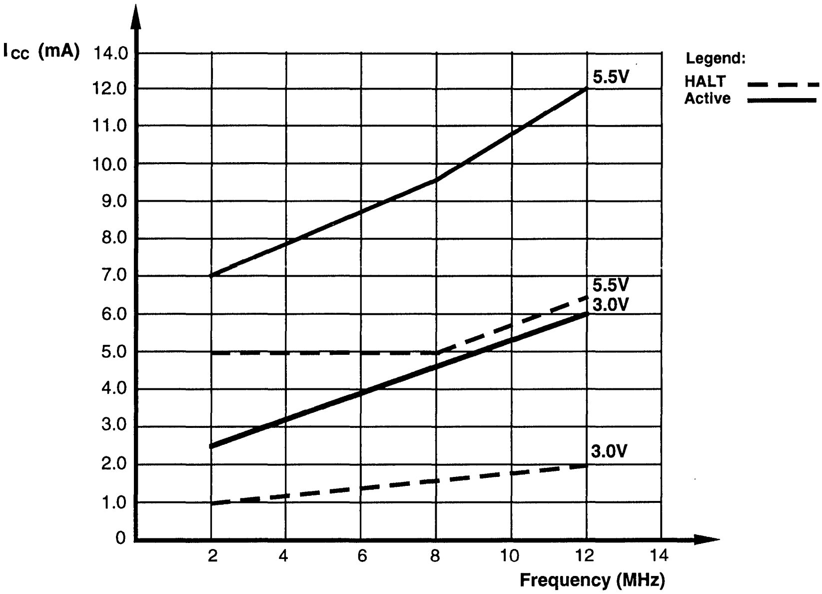


Figure 32. Maximum I_{cc} vs Frequency

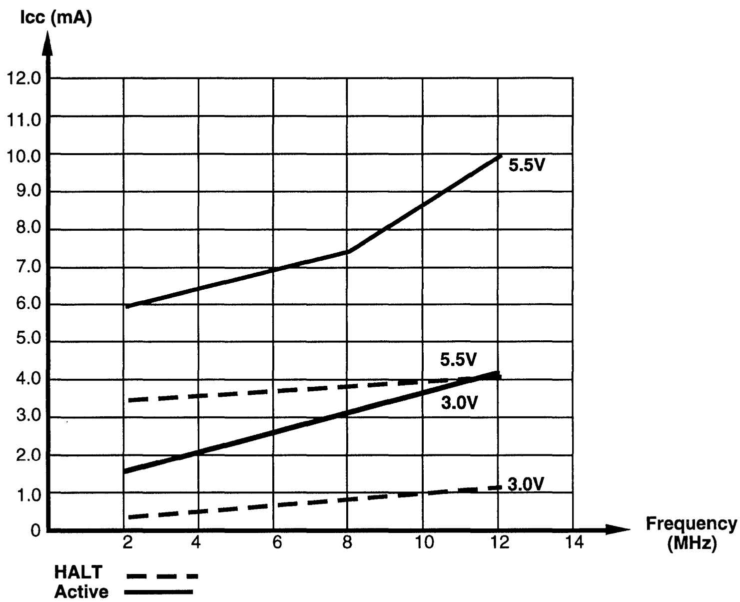


Figure 33. Typical I_{cc} vs Frequency

DEVICE CHARACTERISTICS (Continued)

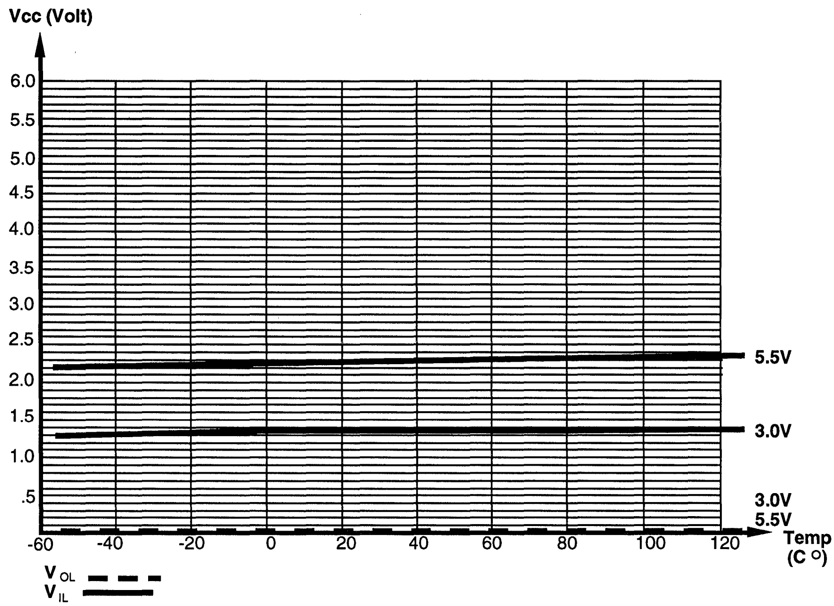


Figure 34. V_{IL}, V_{OL} vs Temperature

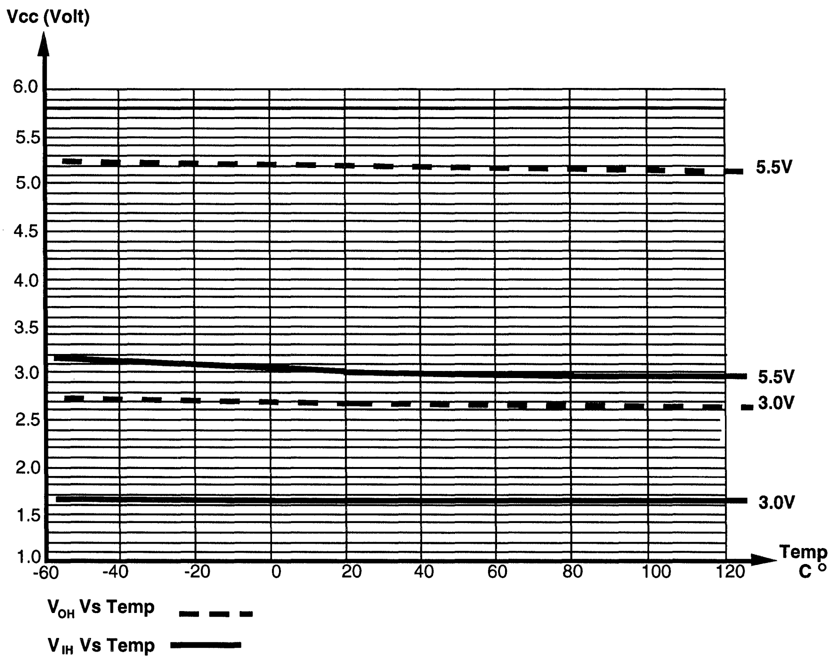


Figure 35. V_{IH}, V_{OH} vs Temperature

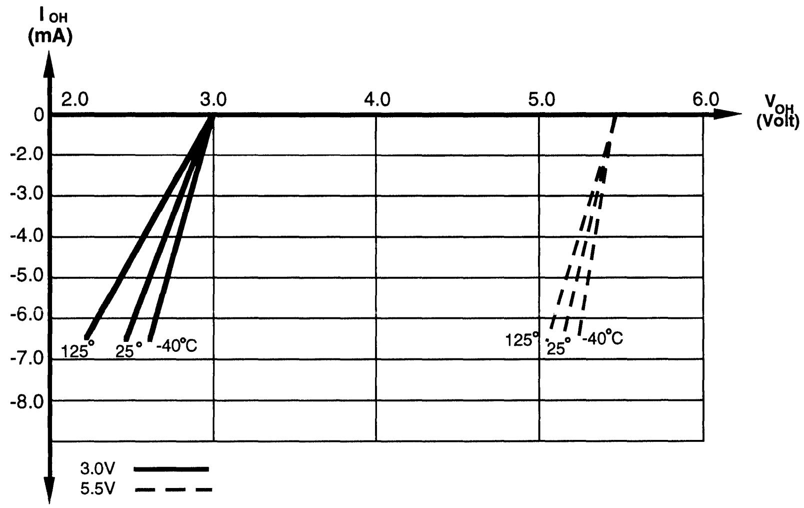


Figure 36. Typical I_{OH} vs V_{OH}

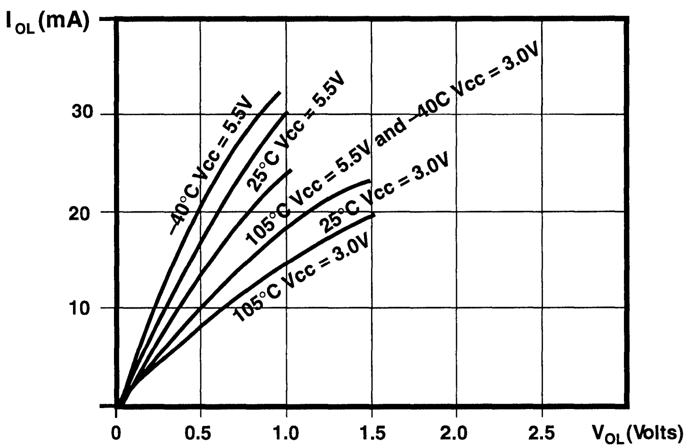


Figure 37. Typical I_{OL} vs V_{OL}

1

DEVICE CHARACTERISTICS (Continued)

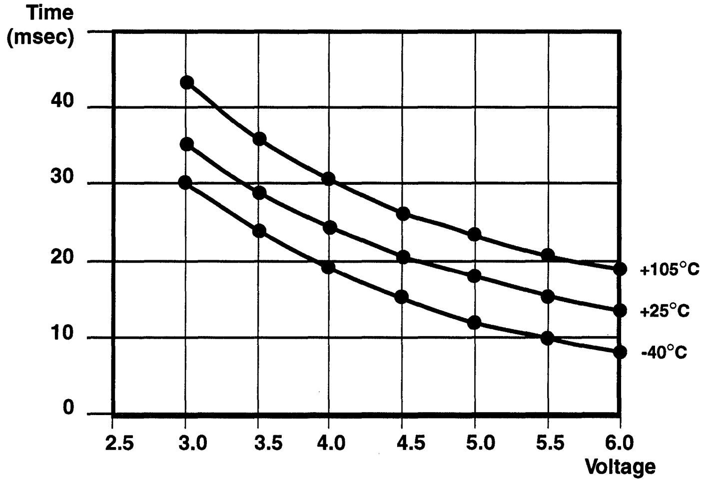


Figure 38. Typical WDT Time Out Period vs V_{CC} Over Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

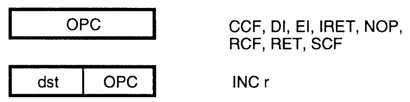
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

1

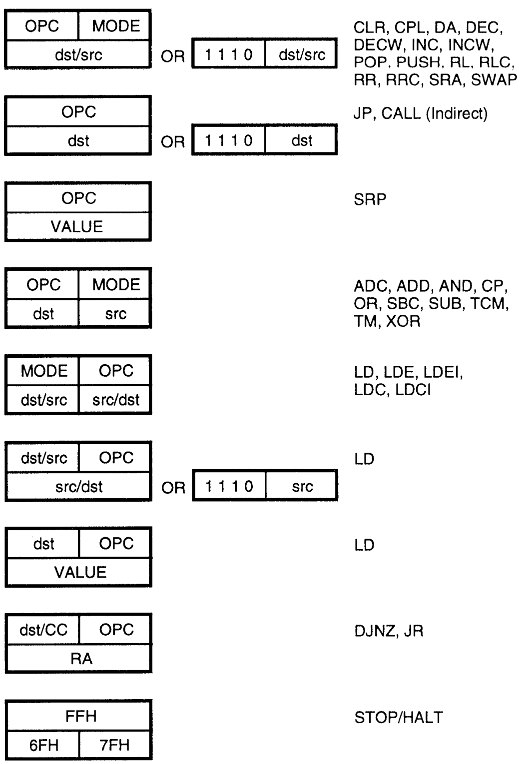
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never True (Always False)	---

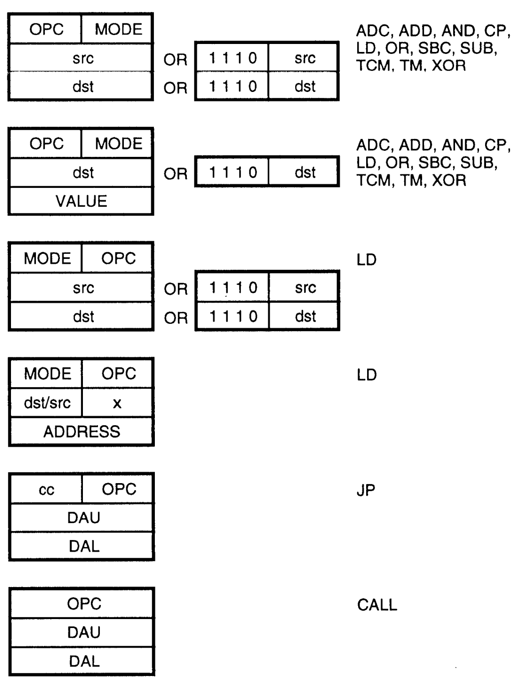
INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

1

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

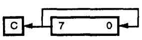
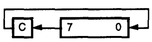
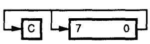
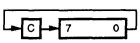
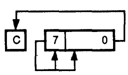
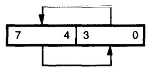
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†	2[ ]	*	*	*	*	1	*
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
WDT		5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

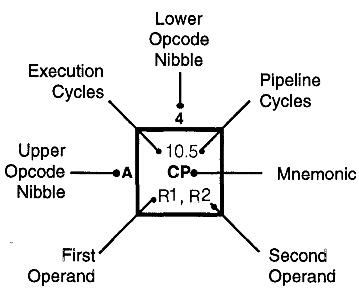
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

1

OPCODE MAP

Lower Nibble (Hex) across the top; **Upper Nibble (Hex)** down the side.

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



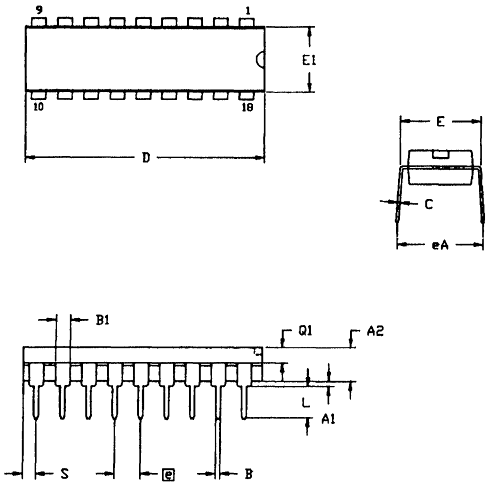
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

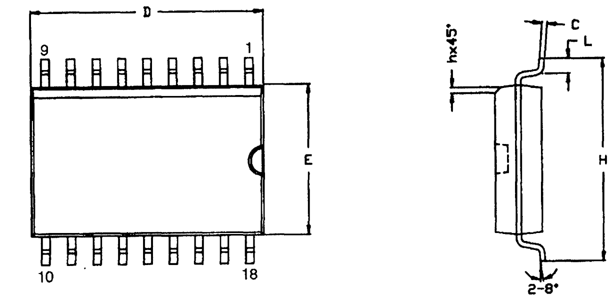
PACKAGE INFORMATION

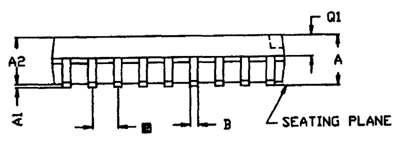


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C07

8 MHz	12 MHz
Z86C0708PSC	Z86C0712PSC
Z86C0708PEC	Z86C0712PEC
Z86C0708SSC	

For fast results, contact your local Zilog sale offices for assistance in ordering the part desired.

Package
P = Plastic DIP
S = SOIC

Temperature
E = -40°C to + 105°C
S = 0°C to 70°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C07 08 P S C is a Z86C07, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86C07 — Product Number
- Z — Zilog Prefix

Introduction I

Z86C07 Z8® CMOS 8-Bit Microcontroller 1

Z86C08 Z8® CMOS 8-Bit Microcontroller 2

Z86E08 Z8® CMOS 8-Bit OTP Microcontroller 3

Z86C11 Z8® CMOS Microcontroller 4

Z86C12 Z8® CMOS In-Circuit Emulator MCU 5

Z86C21 Z8® CMOS 8K ROM Microcontroller 6

Z86C08

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP, and 18-Pin SOIC Package
- Low Cost
- 3.0V to 5.5V Operation Range
- Low Power Consumption; 50 mW (Typical)
- Brown-Out Protection
- Fast Instruction Pointer; 1 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines
- Three Digital Inputs at CMOS Levels
- Eleven Digital Inputs at CMOS Levels; Schmitt-Triggered
- 2 Kbytes of ROM
- 124 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds 8 and 12 MHz
- Watch-Dog/Power-On Reset Timers
- Two Comparators with Programmable Interrupt Polarity.
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

2

GENERAL DESCRIPTION

The Z86C08 Microcontroller Unit (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C08 is a member of the Z8 single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is packaged in 18-pin DIP, and 18-pin SOIC, and is manufactured in CMOS technology. The Zilog Z86C08 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

The Z86C08 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C08 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with real-time tasks such as counting/timing and I/O data communications, the Z86C08 offers two on-chip counter/timers with a large number of user selectable modes. Also, there are two on-board comparators that can process analog signals with a common reference voltage (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

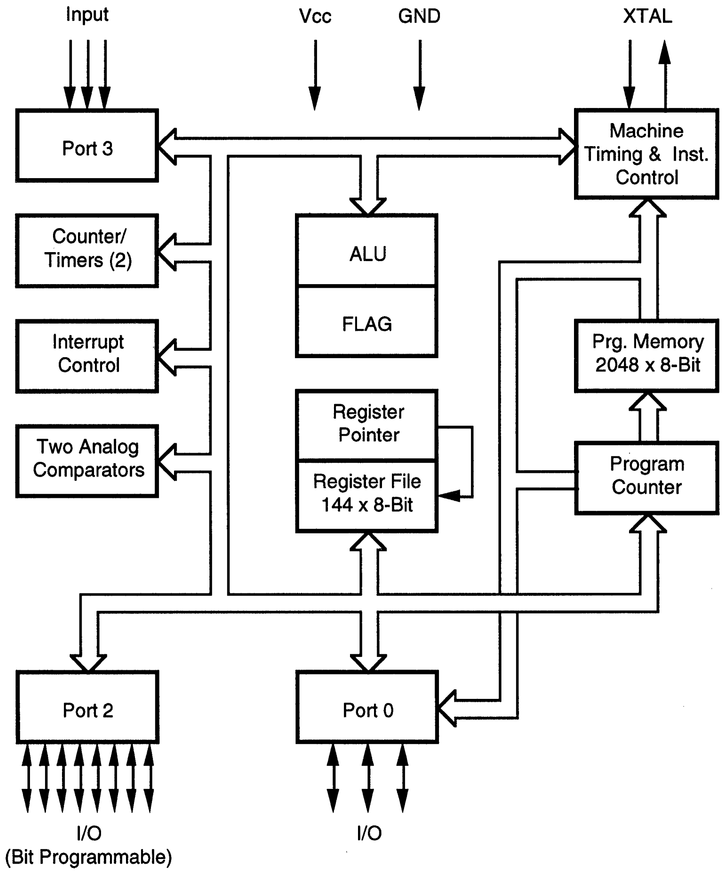


Figure 1. Functional Block Diagram

PIN DESCRIPTIONS

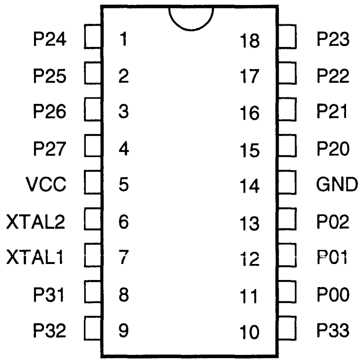


Figure 2. 18-Pin DIP Configuration

Table 1. 18-Pin DIP Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

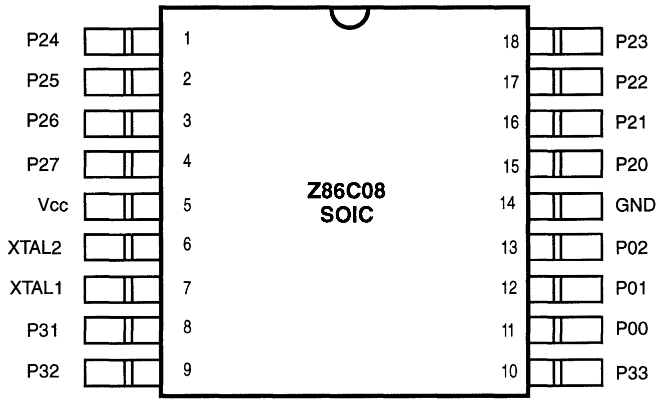


Figure 3. 18-Pin SOIC Pin Configuration

Table 2. 18-Pin SOIC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output	9	P32	Port 3, Pin 2, AN2	Input
5	V_{cc}	Power Supply		10	P33	Port 3, Pin 3, REF	Input
6	XTAL2	Crystal Oscillator Clock	Output	11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
7	XTAL1	Crystal Oscillator Clock	Input	14	GND	Ground	
8	P31	Port 3, Pin 1, AN1	Input	15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

PIN DESCRIPTION (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, nibble programmable, bidirectional, CMOS compatible I/O port. These three I/O lines can be configured under software control to be an input or output (Figure 4).

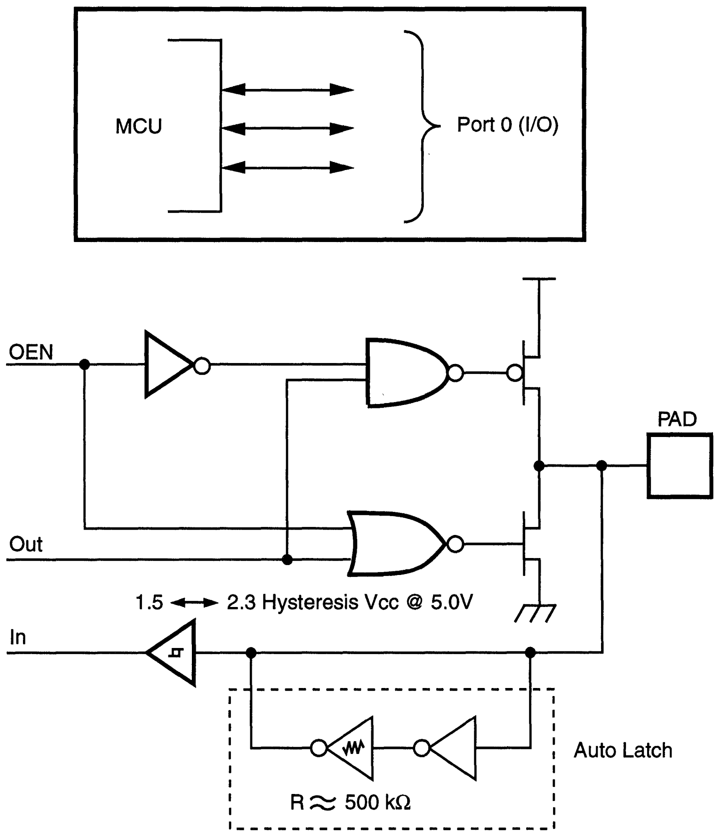


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 5).

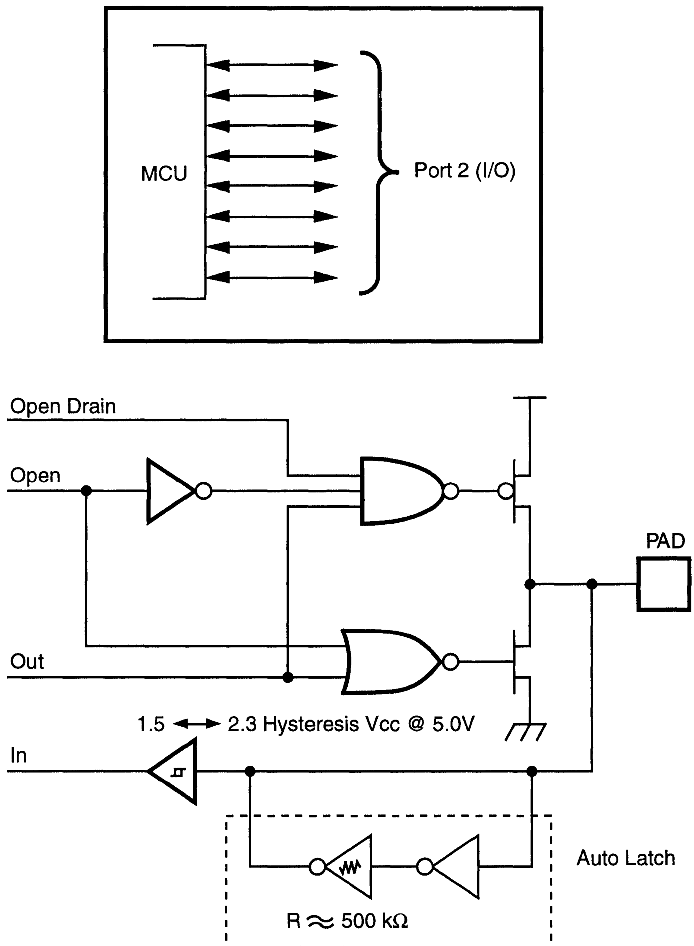
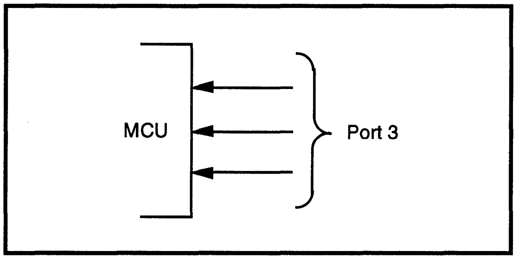


Figure 5. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 6).



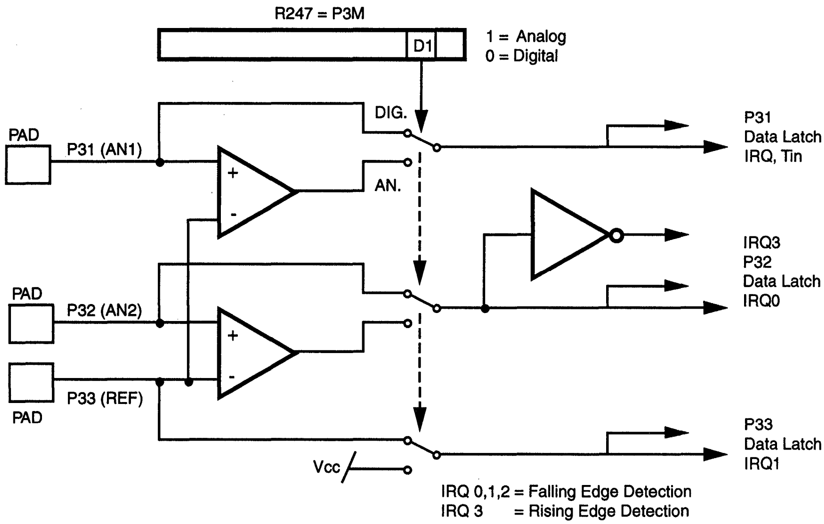


Figure 6. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternately, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific research, auto, and consumer applications.

FUNCTIONAL DESCRIPTION

Reset. Upon power-up the Power-On Reset circuit waits for 30 µsec plus 18 crystal clocks and then starts program execution at address %000C (Hex) (Figure 7). Reference the Z86C08 control registers' Reset value (Table 3).

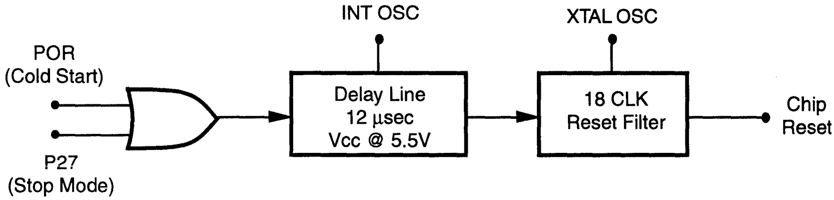


Figure 7. Internal Reset Configuration

Table 3. Z86C08 Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FE	SPH	U	U	U	U	U	U	U	U	Not used, stack always internal
FF	SPL	U	U	U	U	U	U	U	U	
*00	Port 0	U	U	U	U	U	U	U	U	
*02	Port 2	U	U	U	U	U	U	U	U	
03	Port 3	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 3 and the user must avoid Bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86C08 can address up to 2 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

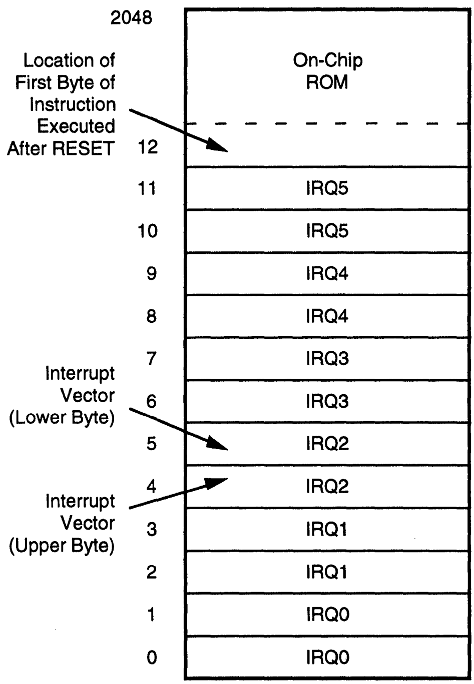


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers (R0, R2-R3, R4-R127, and R241-R253, and R255, respectively - Figure 9). The Z86C08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group. Upon power-up, the general purpose registers are undefined.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Reserved	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	To Prescaler	PRE0
244	Timer/Counter0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter1	T1
241	Timer Mode	TMR
240 128	Not Implemented	
127 4	General Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 9. Register File

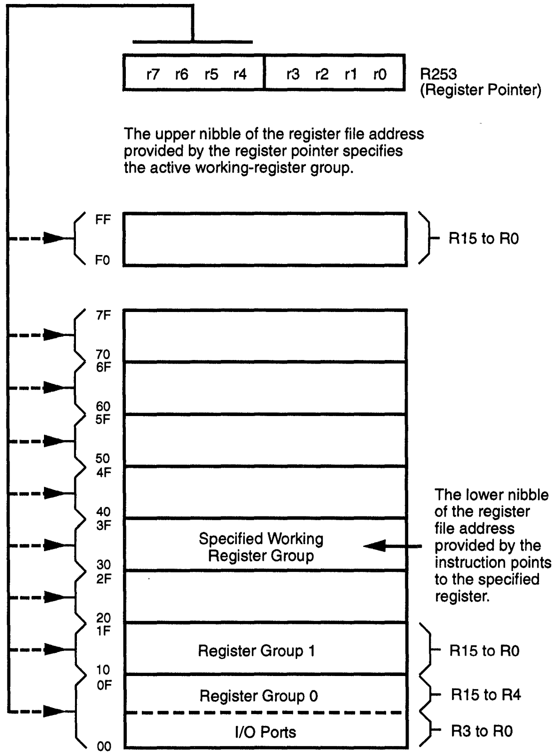


Figure 10. Register Pointer

Stack Pointer. The Z86C08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

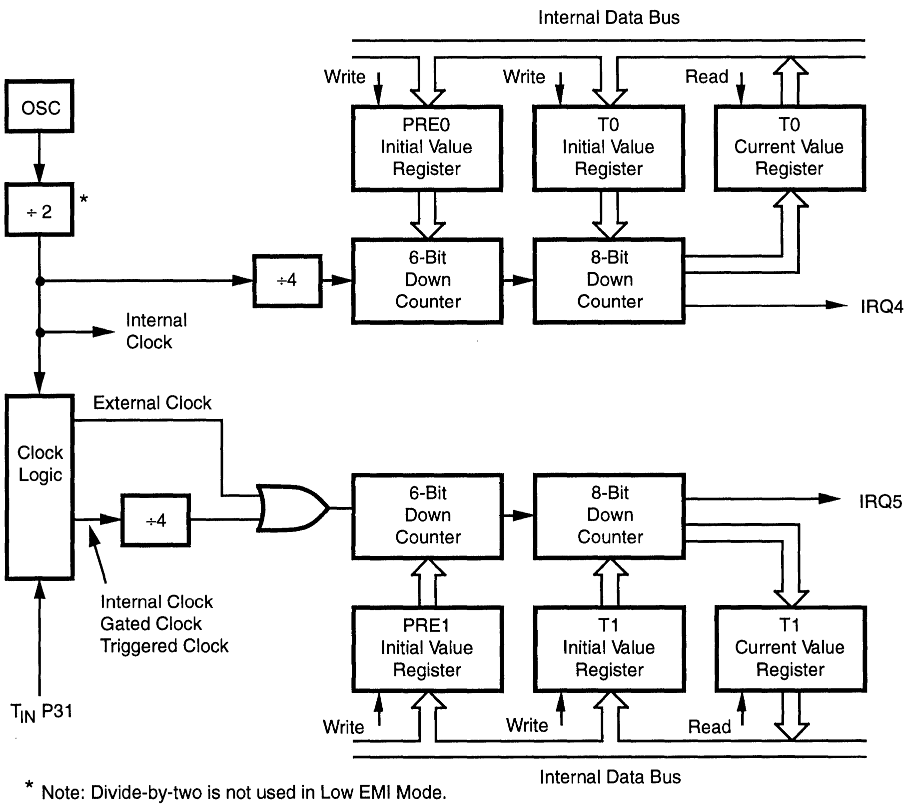


Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C08 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

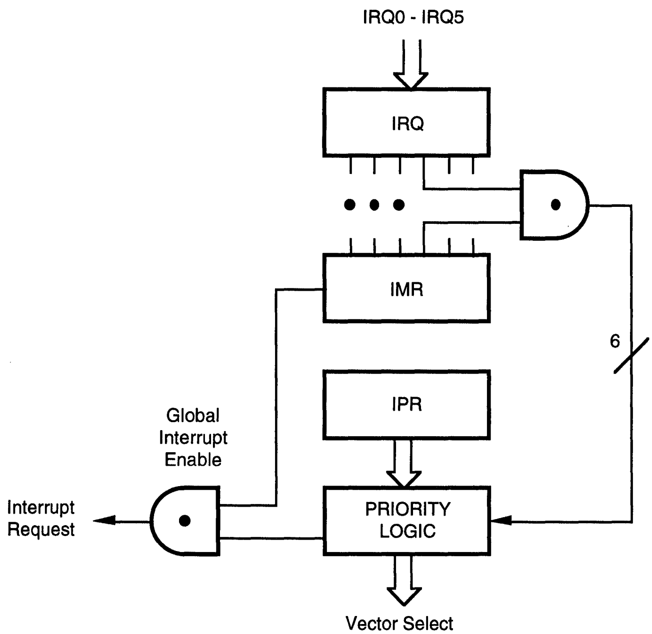


Figure 12. Interrupt Block Diagram

Clock. The Z86C08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (capacitance is between 10 pF to 250 pF which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device Ground pin 14 (Figure 13).

Note that the crystal capacitor loads should be connected to V_{SS}, pin 14 to reduce Ground noise injection.

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location 000C (HEX). An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC}. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP Mode.

Program execution under both conditions begins at location 000C (Hex). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
OR      P2M, #80H
NOP
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction. i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every 10 µsec; otherwise, the Z86C08 resets itself. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

WDT = 5F (Hex).

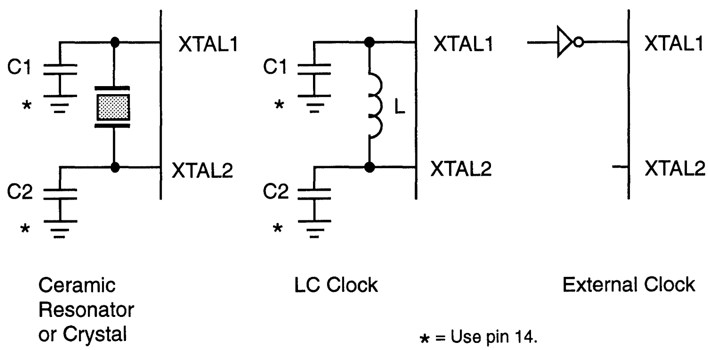


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done at least every 10 µsec. Otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} µsec +18 XTAL clock cycles. The WDT does not work in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT function running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Brown-Out Protection (V_{BO}). Maximum (V_{BO}) Conditions:

Case 1 T_A= –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

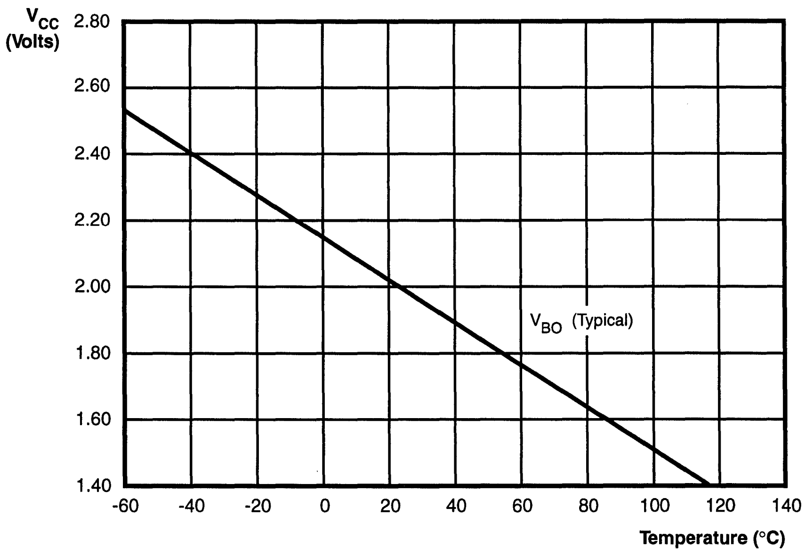
Case 2 T_A= –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Brown-Out Protection trip point (V_{BO}) is reached. The device is guaranteed to function normally at supply voltages above the brown-out trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual brown-out trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	–40°C	0°C	+25°C	+70°C	+105°C
V_{BO}	2.55	2.4	2.1	1.7	1.6



* Power-On Reset threshold for V_{BO} and 1 MHz internal clock frequency V_{BO} overlap.

Figure 14. Typical Z86C08 V_{BO} vs Temperature

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:
*Voltages on all pins with respect to GND
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 15).

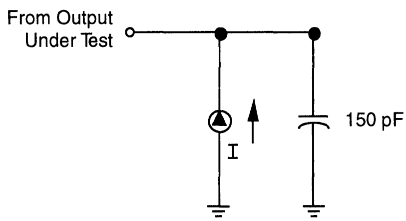


Figure 15. Test Load Diagram

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.0V		12		12		V	I_{IN} = 250 µA	
		5.5V		12		12		V	I_{IN} = 250 µA	
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	[5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA	
		5.5V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	[5]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[5]
		3.0V		0.4		0.4		V	Low Noise @ 0.5 mA	
		5.5V		0.4		0.4		V	Low Noise @ 0.5 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max	[5]
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{BO}	V_{CC} Brown Out Voltage			2.7		2.95	2.1	V	@ 1 MHz Max, Int. CLK Freq	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{REF}			0	V_{CC}–1.0	0	V_{CC}–1.5		V		

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	[5]
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	[5]
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	[5]
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	[5]
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	[5]
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	[5]
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	[5]
		5.5V		4.0		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	[5]
		3.0V		4.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[5]
		5.5V		5.0		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[5]
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[5]
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[5]
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 4 MHz	
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz	

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		1.2		1.2	0.4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6		1.6	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		1.5		1.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9		1.9	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		2.0		2.0	0.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4		2.4	0.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	3.0V		6.0		8.0	3.0	µA	0V < V_{IN} < V_{CC}
		5.5V		22		30	16	µA	0V < V_{IN} < V_{CC}
I_{ALH}	Auto Latch High Current	3.0V		–4.0		-5.0	-1.5	µA	0V < V_{IN} < V_{CC}
		5.5V		–12.0		-20	-8.0	µA	0V < V_{IN} < V_{CC}

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal/Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] For 2.75V operating, the device operates down to V_{BO}. The minimum operational V_{CC} is determined on the value of the voltage V_{BO} at the ambient temperature. The V_{BO} increases as the temperature decreases.

[4] V_{CC} = 3.0V to 5.5V

[5] Standard Mode (not Low EMI mode)

AC ELECTRICAL CHARACTERISTICS

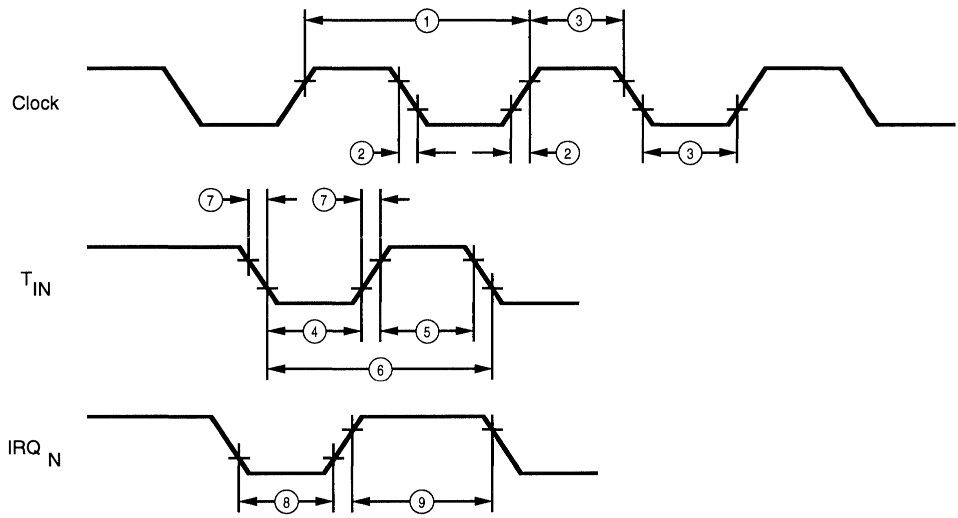


Figure 16. AC Electrical Timing Diagram

2

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode)

				T_A = 0°C to +70°C				T_A = –40°C to +105°C					
				8 MHz		12 MHz		8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	100,000	83	100,000	125	100,000	83	100,000	ns	[1]
			5.5V	125	100,000	83	100,000	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	[1]
			5.5V		25		15		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			62		41		[1]
			5.5V	62		41			62		41	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	[1]
			5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	3.0V		25		25		25		25	ms	[1]
			5.5V		12		12		10		10	ms	[1]
11	Tpor		3.0V		24		24		24		24	ms	[1]
			5.5V		12		12		12		12	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P31-P33).

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C				T_A = −40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watchdog Timer	3.0V		25		25		25		25	ms	[1]
		Delay Time	5.5V		12		12		10		10	ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P31-P33)

LOW NOISE VERSION

Low EMI Emission

The Z86C08 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode, –0°C to +70°C.
- All pre-driver slew rates reduced to 10 ns typical.
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z86C08 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements were made while operating the Z86C08 in three states: (1) Idle condition; (2) static output; (3) switched output.

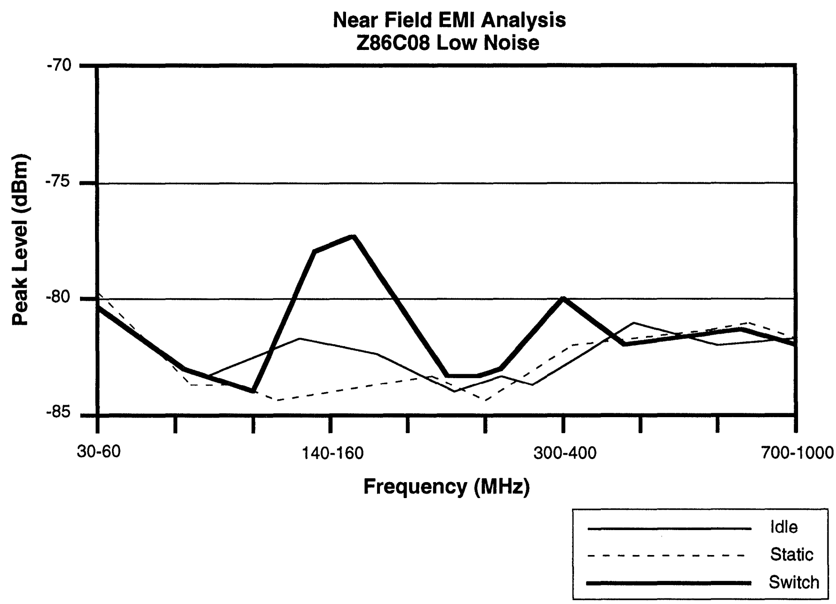


Figure 17. Low Noise Analysis

Z8 CONTROL REGISTER DIAGRAMS

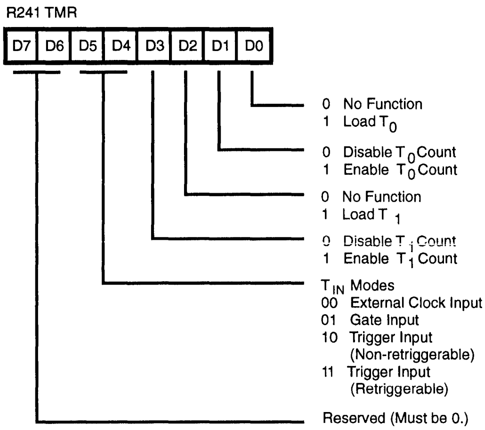


Figure 18. Timer Mode Register ($F1_H$: Read/Write)

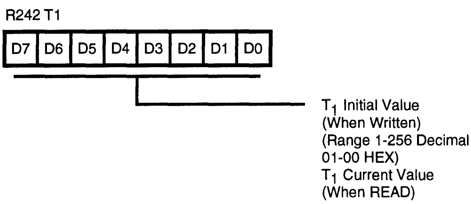


Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

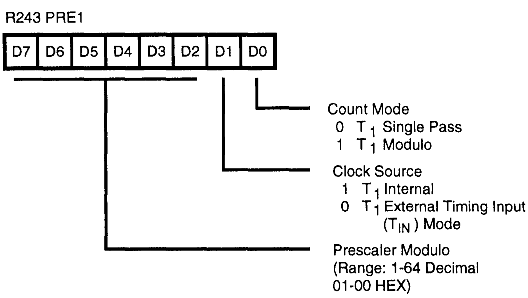


Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

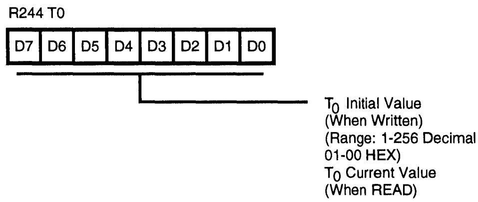


Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

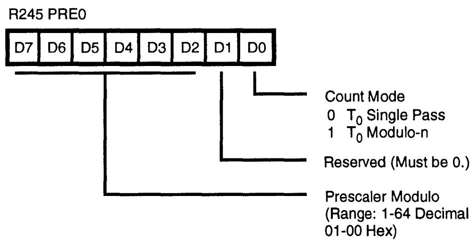


Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

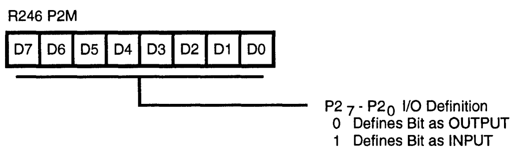


Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

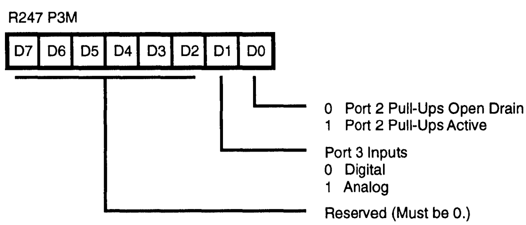


Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

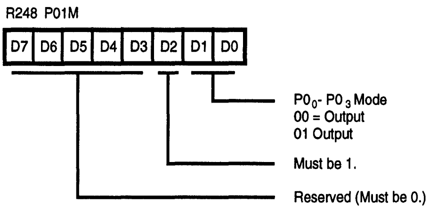


Figure 25. Port 0 and 1 Mode Register ($F8_H$: Write Only)

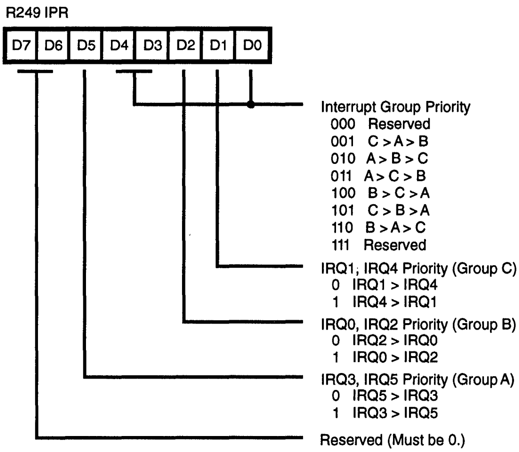


Figure 26. Interrupt Priority Register ($F9_H$: Write Only)

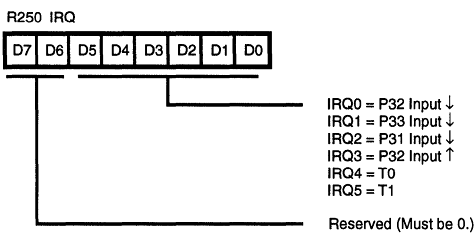


Figure 27. Interrupt Request Register (FA_H: Read/Write)

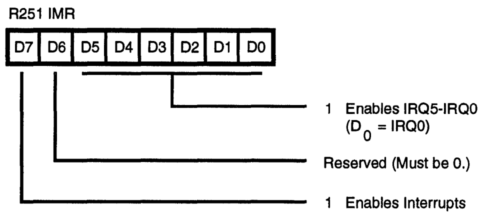


Figure 28. Interrupt Mask Register (FB_H: Read/Write)

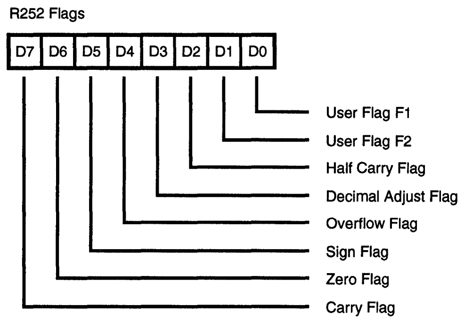


Figure 29. Flag Register (FC_H: Read/Write)

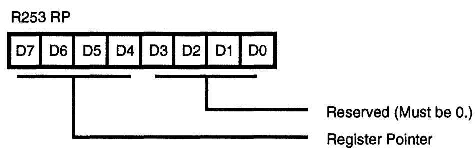


Figure 30. Register Pointer (FD_H: Read/Write)

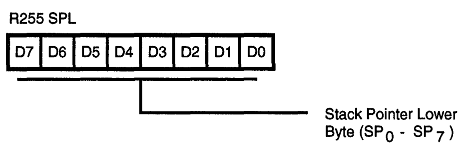


Figure 31. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS
Standard Mode

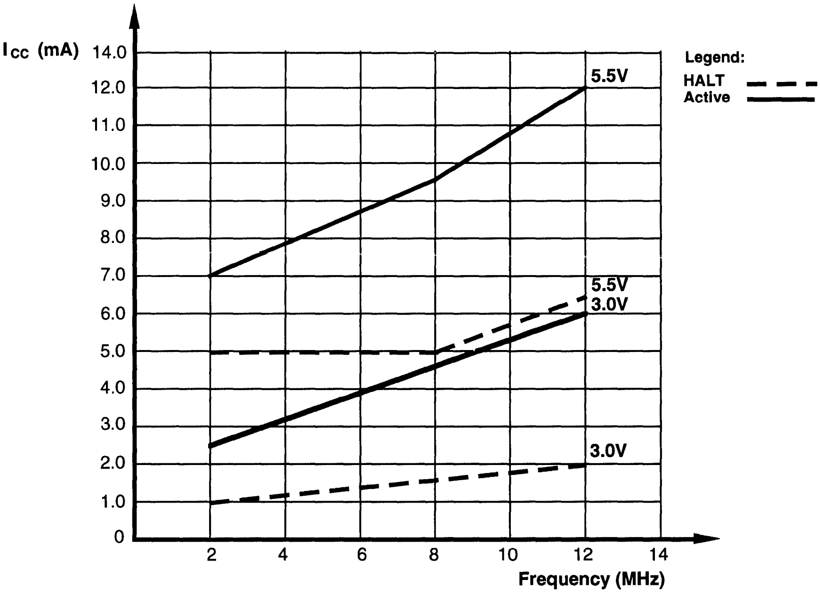


Figure 32. Maximum I_{cc} vs Frequency

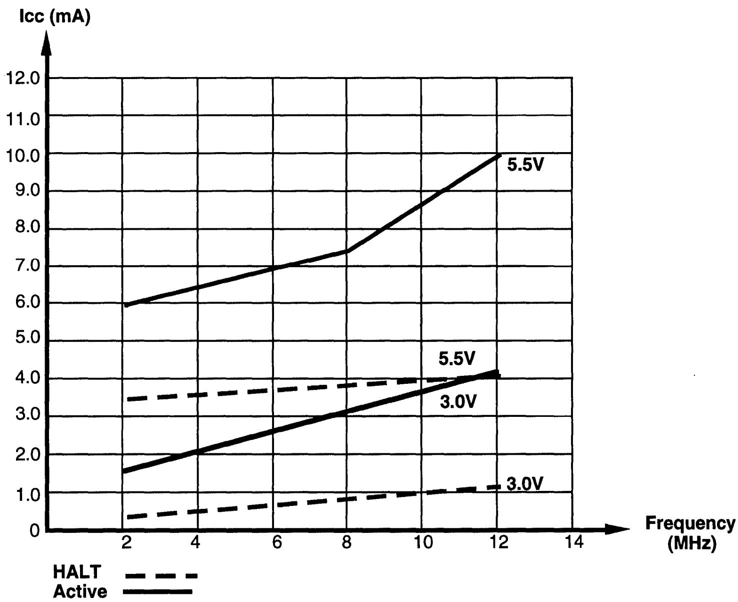


Figure 33. Typical I_{cc} vs Frequency

DEVICE CHARACTERISTICS (Continued)

Standard Mode

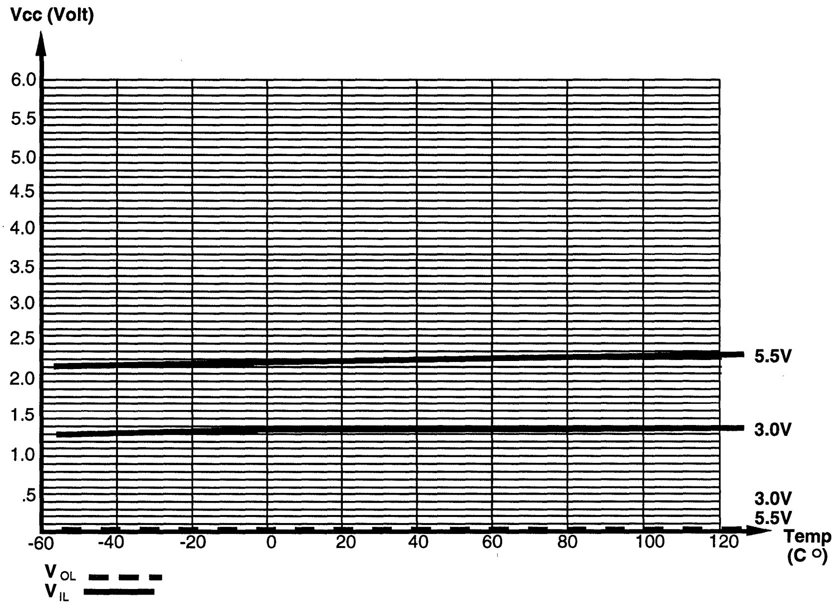


Figure 34. V_{IL}, V_{OL} vs Temperature

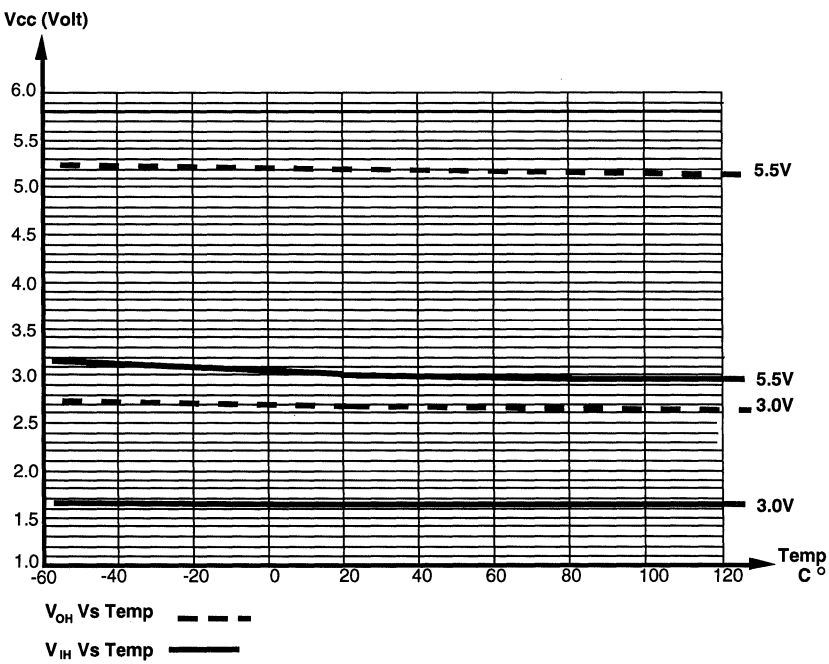


Figure 35. V_{IH}, V_{OH} vs Temperature

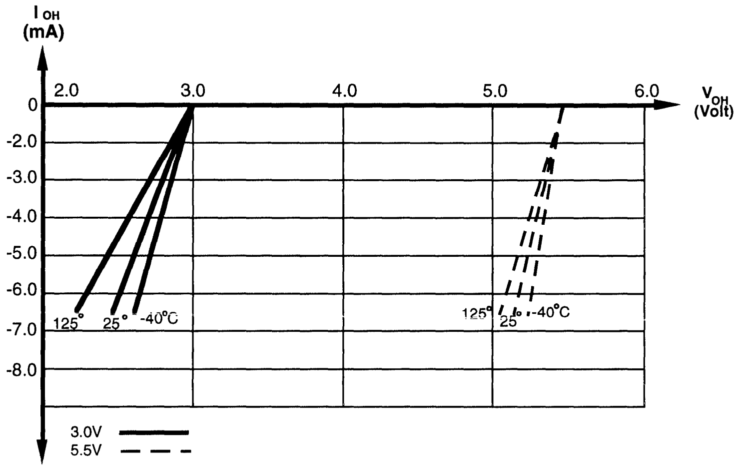


Figure 36. Typical I_{OH} vs V_{OH}

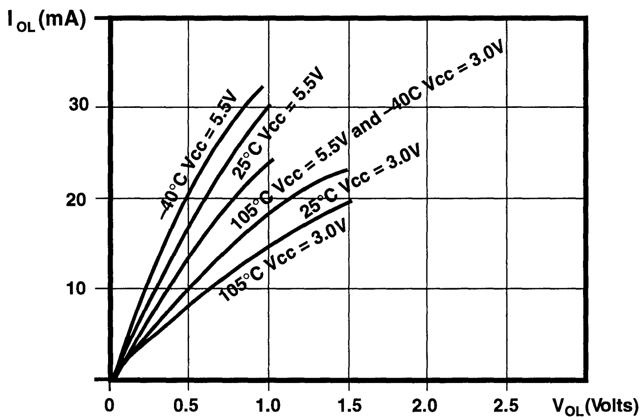


Figure 37. Typical I_{OL} vs V_{OL}

DEVICE CHARACTERISTICS (Continued)
Standard Mode

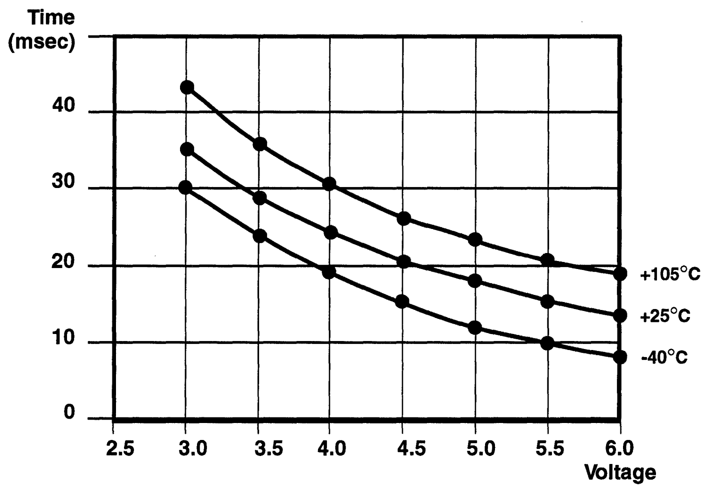


Figure 38. Typical WDT Time Out Period vs V_{CC} Over Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

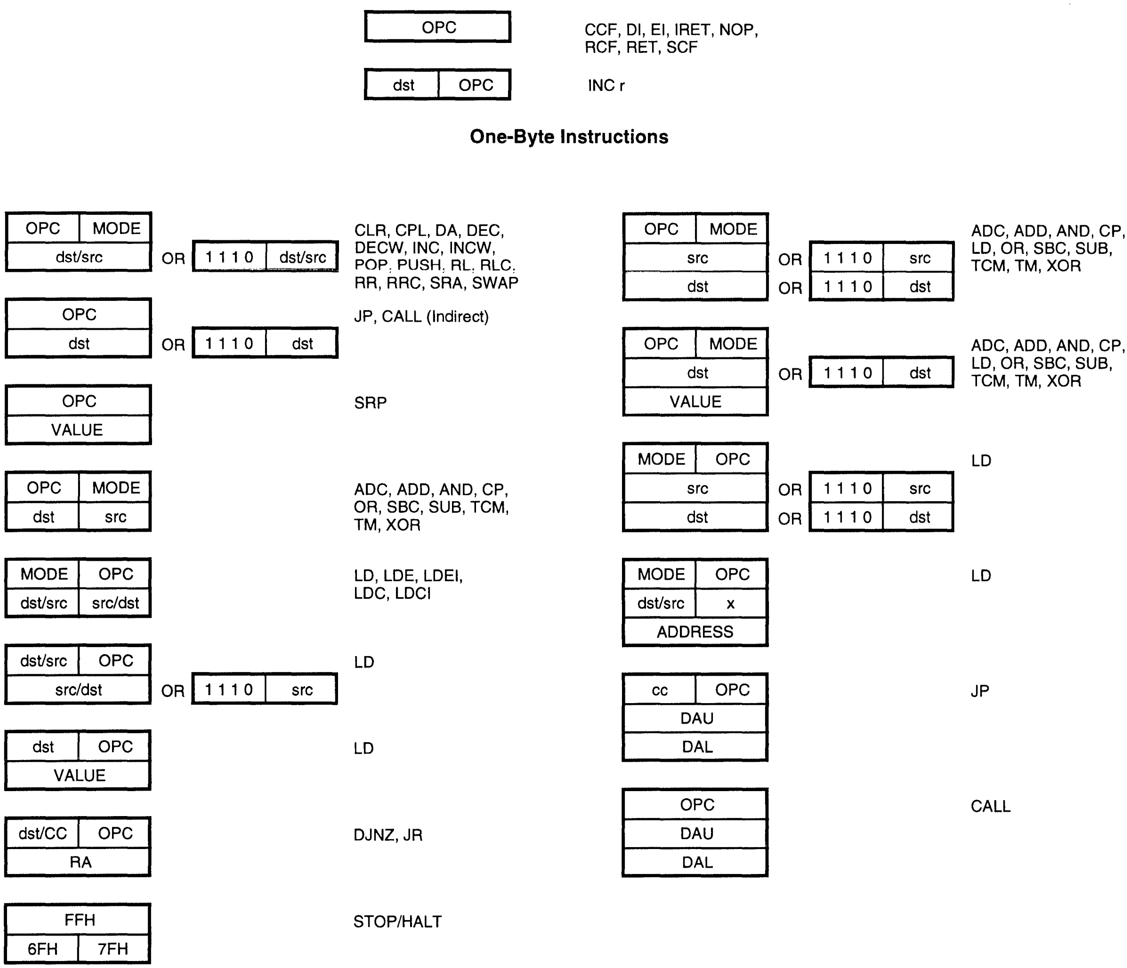
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

2

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never true (always false)	---

INSTRUCTION FORMATS



One-Byte Instructions

Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

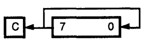
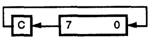
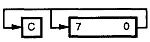
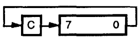
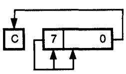
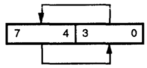
dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - -
CCF C←NOT C			EF	* - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst – src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst – 1	R IR		00 01	- * * * - -
DECW dst dst←dst – 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - -
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	- - - - - -
EI IMR(7)←1			9F	- - - - - -
HALT			7F	- - - - - -

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	- - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - -
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	- - - - - -
NOP			FF	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†	2[ ]	*	*	*	*	1	*
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
WDH		4F	-	-	-	-	-	-
WDT		5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

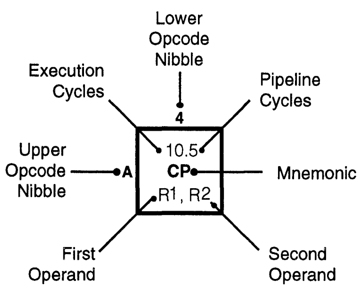
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



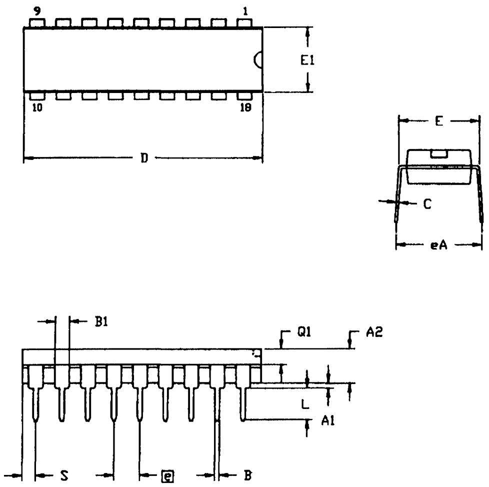
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

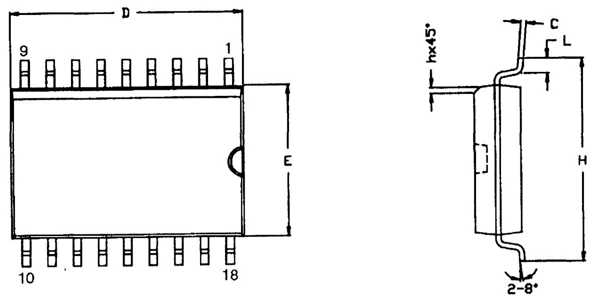
PACKAGE INFORMATION

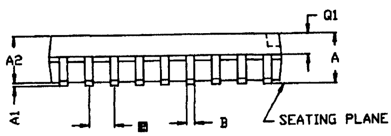


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C08

8 MHz	12 MHz
Z86C0808PSC	Z86C0812PSC
Z86C0808PEC	Z86C0812PEC
Z86C0808SEC	Z86C0812SEC
Z86C0808SSC	Z86C0812SSC

For fast results, contact your local Zilog sale offices for assistance in ordering the part desired.

Package
P = Plastic DIP
S = SOIC

Temperature
E = -40°C to + 105°C
S = 0°C to 70°C

Speed
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:
Z 86C08 08 P S C is a Z86C08, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86C08 — Product Number
- Z — Zilog Prefix

Introduction I

Z86C07 Z8® CMOS 8-Bit Microcontroller 1

Z86C08 Z8® CMOS 8-Bit Microcontroller 2

Z86E08 Z8® CMOS 8-Bit OTP Microcontroller 3

Z86C11 Z8® CMOS Microcontroller 4

Z86C12 Z8® CMOS In-Circuit Emulator MCU 5

Z86C21 Z8® CMOS 8K ROM Microcontroller 6

Z86E08

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP Package
- Low Cost
- Low Noise Programmable
- ROM Protect Programmable
- 4.0V to 5.5V Operating Range
- Low Power Consumption - 50 mW (Typical)
- Fast Instruction Pointer - 1 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines
- All Digital Inputs, CMOS Levels, Schmitt-Triggered.
- 2 Kbytes of One Time PROM
- 144 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Five Different Sources.
- Clock Speeds - 8 and 12 MHz
- Watch-Dog Timer
- Power-On Reset
- Two On-Board Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86E08 Microcontroller (MCU) introduces a new level of sophistication to single-chip architecture. The Z86E08 is a member of the Z8 single-chip microcontroller family with 2 Kbytes of one-time PROM. The device is housed in an 18-pin DIP, and is manufactured in CMOS technology. The device allows easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

The Z86E08 has a flexible I/O scheme, an efficient register and address space structure. Also, it has a number of ancillary features that are useful in many consumer, industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86E08 provides 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations; program memory and 124 bytes of general-purpose registers.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with real-time tasks such as counting/timing and I/O data communications, the Z86E08 offers two on-chip counter/timers with a large number of user selectable modes. Included, are two on-board comparators that process analog signals with a common reference voltage (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

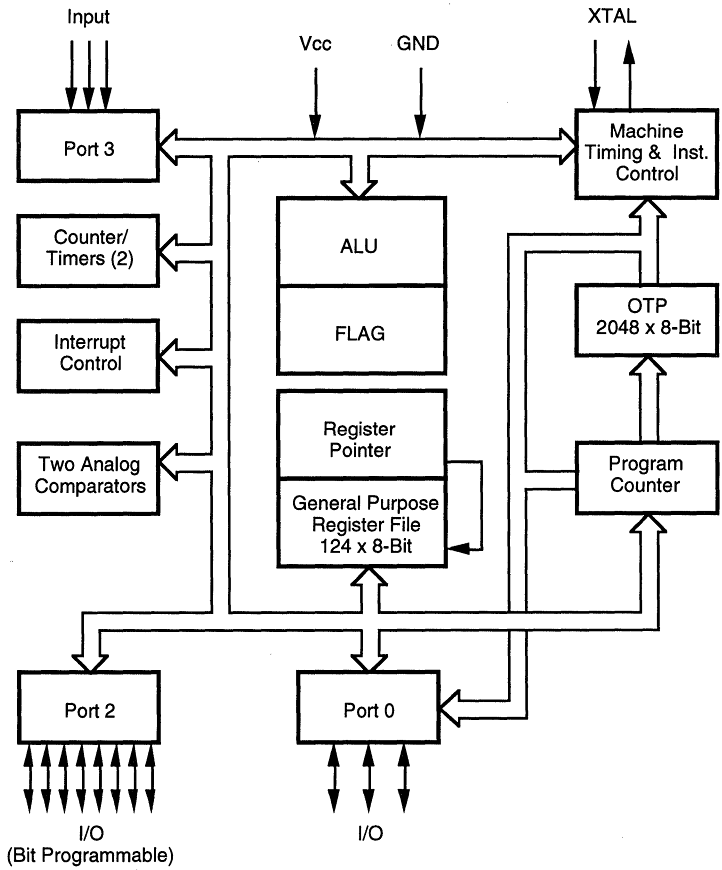


Figure 1. Functional Block Diagram

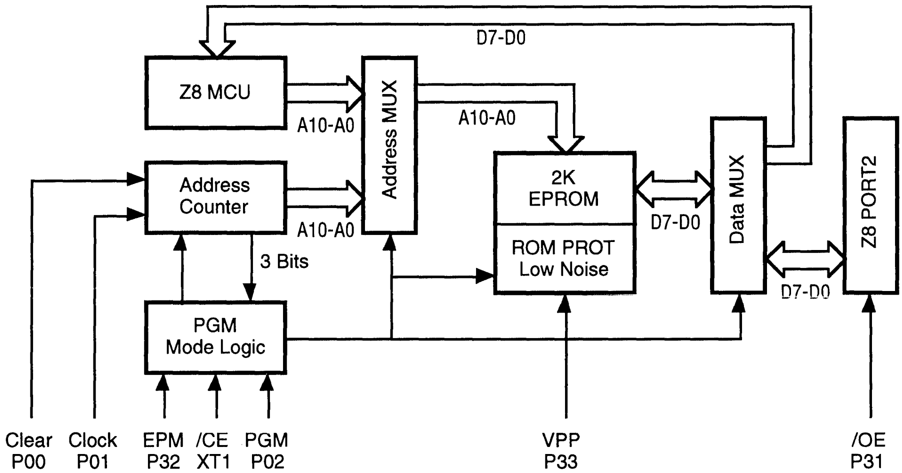


Figure 2. EPROM Mode Block Diagram

PIN DESCRIPTION

Table 1. EPROM Mode Pin Identification

Z86E08 EPROM Mode Pin #	Symbol	Function	Direction
1-4	D7-D4	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	Input
6	N/C	No Connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Prog Mode	Input
14	GND	Ground	Input
15-18	D3-D0	Data 0,1, 2, 3	In/Output

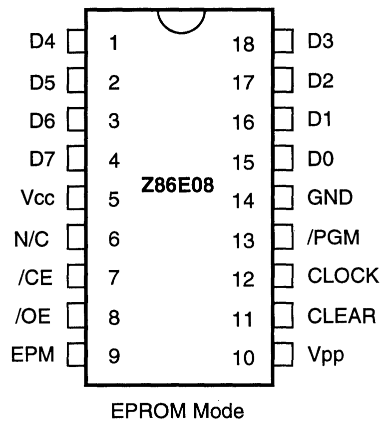
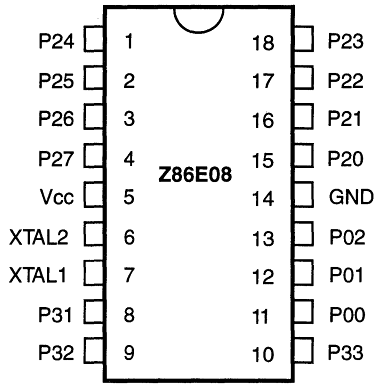


Figure 3. EPROM Mode Pin Configuration

PIN DESCRIPTION

Table 2. Standard Mode Pin Identification

Z86E08 Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1-4	P27-P24	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	Input
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1	Input
9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3	Input
11-13	P02-P00	Port 0, Pins 0, 1, 2	Input/Output
14	GND	Ground	Input
15-18	P23-P20	Port 2, Pins 0, 1, 2, 3	In/Output



Standard Mode

Figure 4. Standard Mode Pin Configuration

PIN FUNCTIONS

OTP Programming Mode

D7-D0 *Data Bus.* The data can be read from, or written to the EPROM through this data bus.

V_{CC} *Power Supply.* It is 5V during the EPROM Read mode and 6V during the other mode.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

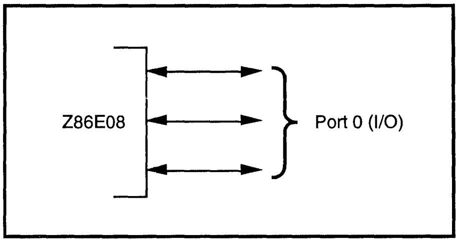
Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock signal.

/PGM *Program Mode* (active Low). Low Level at this pin programs the data to the EPROM through the Data Bus.

Z86E08 Standard Mode

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bi-directional, CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be an input or output (Figure 5).



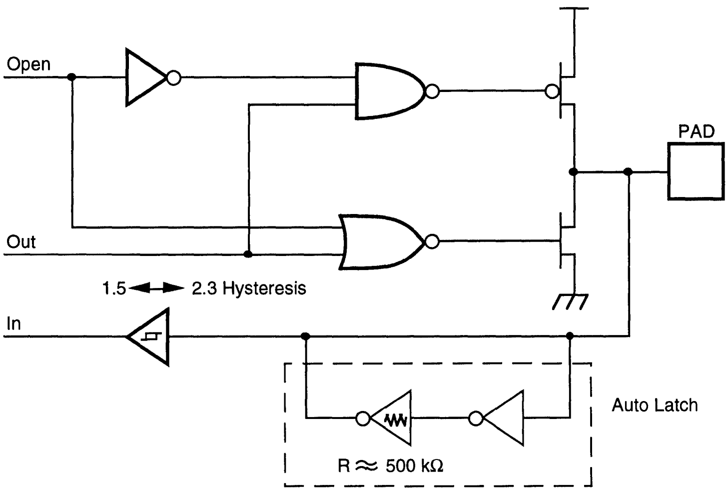


Figure 5. Port 0 Configuration

Z86E08 Standard Mode (Continued)

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 6).

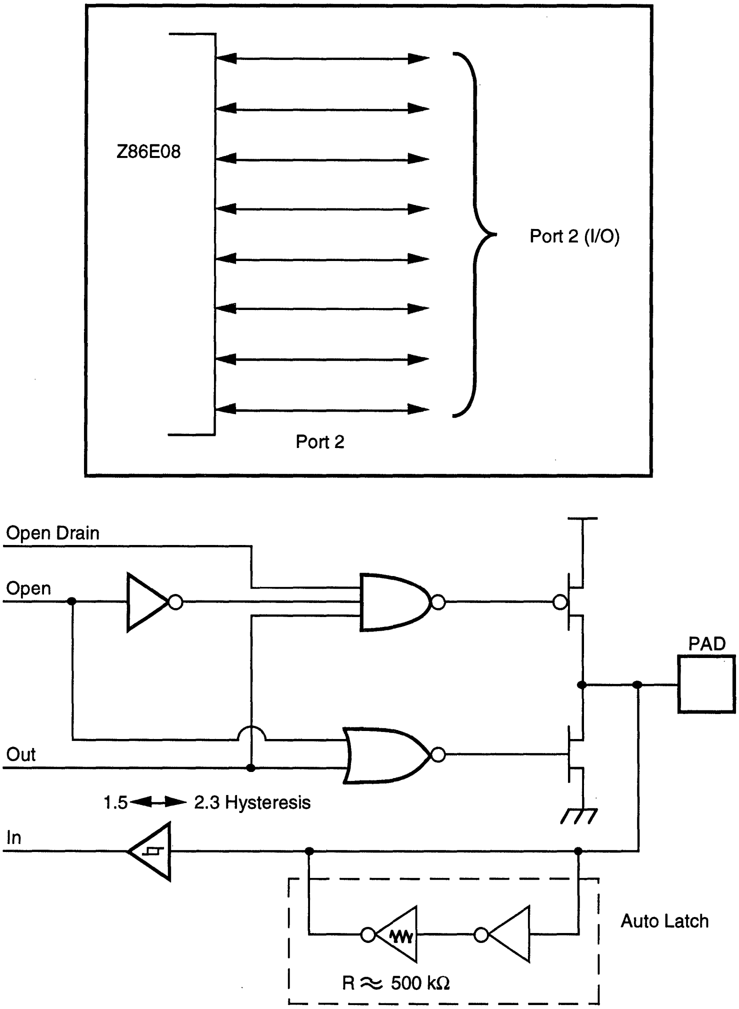
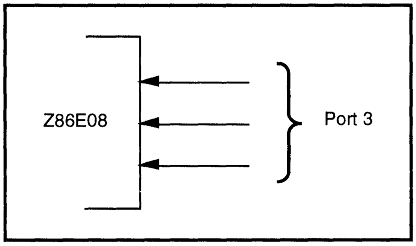
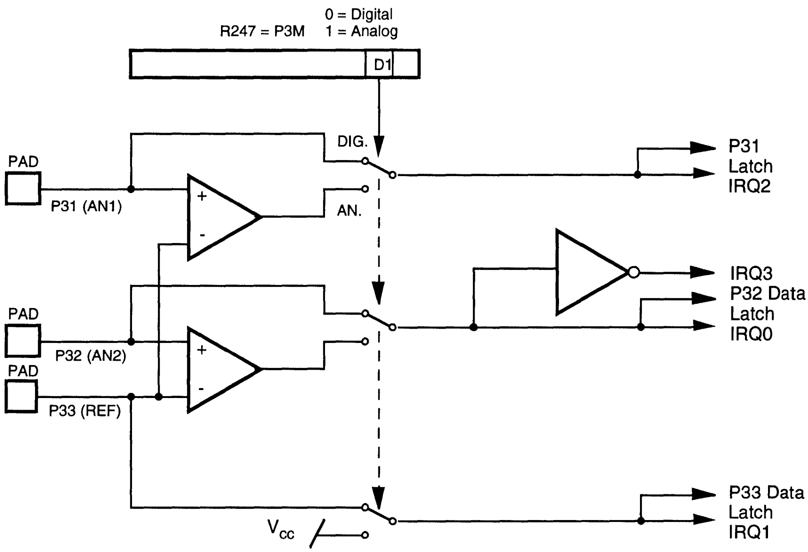


Figure 6. Port 2 Configuration

Port 3, P31-P33. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P32-P30) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN} - Figure 7).





IRQ 0,1,2 = Falling Edge Detection
IRQ3 = Rising Edge Detection

Figure 7. Port 3 Configuration

3

Z86E08 Standard Mode (Continued)

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P3REF is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90dB and 60dB, respectively.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

SPECIAL FUNCTIONS

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific and advanced technologies applications.

RESET is accomplished through Power-On or a Watch-Dog Timer Reset. Upon power-up, the power-on reset circuit waits for 50 µsec plus 18 crystal clocks and then starts program execution at address 000C (Hex). Reference Table 3 for the Z86E08 control registers' reset values (Figure 8).

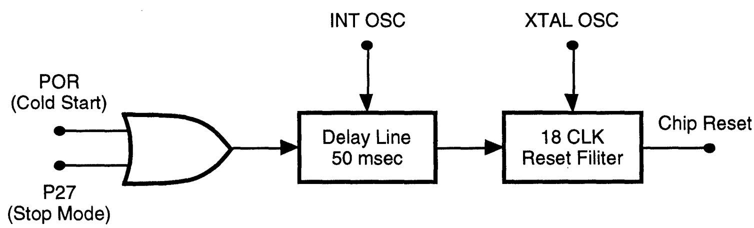


Figure 8. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time out
- WDH time out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Table 3. Z86E08 Control Registers

Addr.	Reg.	D7	D6	D5	D4	D3	D2	D1	D0	Comments
				Reset Condition						
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset.
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection.
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Not reset after a Low on P27 to get out of STOP Mode

Program Memory. The Z86E08 addresses up to 2 Kbytes of internal program memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip one-time programmable ROM.

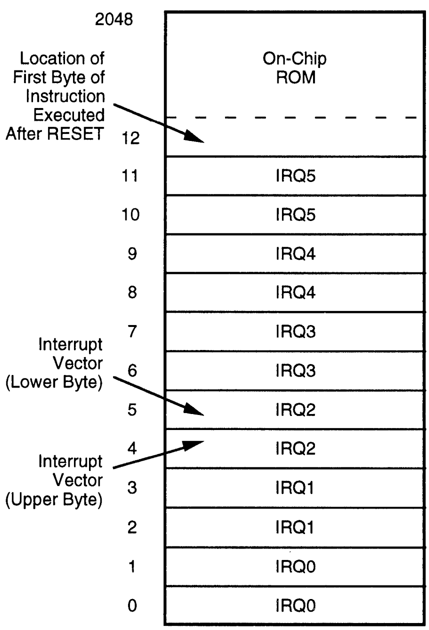


Figure 9. Program Memory Map

SPECIAL FUNCTIONS (Continued)

Register File. The Register File consists of three I/O port registers, 124 general purpose registers, and 14 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 10). General purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The Mode and Configuration Registers are the same as the Z86C08. The Z86E08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 11) addresses the starting location of the active working-register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General Purpose Register	GPR
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	HMH
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
127	Not Implemented	
	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 10. Register File

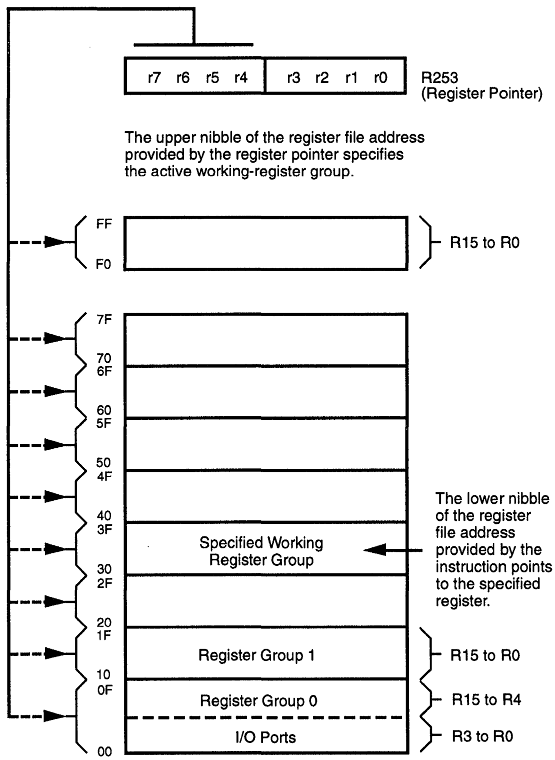


Figure 11. Register Pointer

Stack Pointer. The Z86E08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

GPR *(R254).* This register is a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 12).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or used as a gate input for the internal clock.

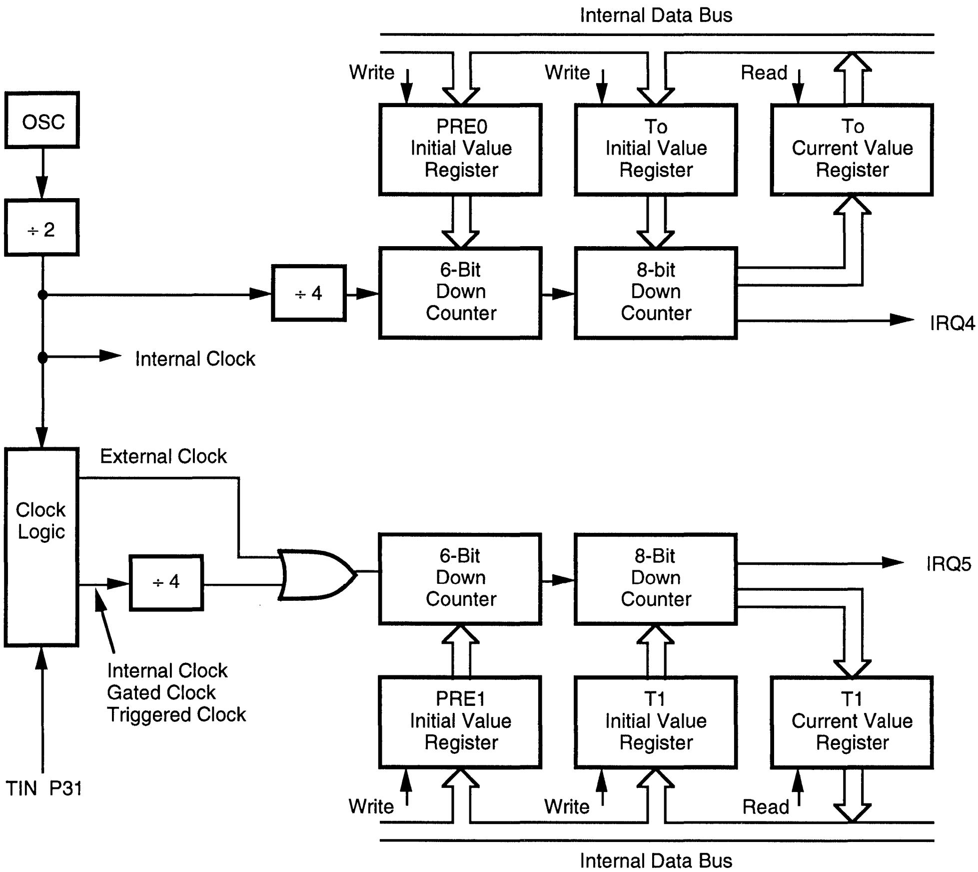


Figure 12. Counter/Timers Block Diagram

3

SPECIAL FUNCTIONS (Continued)

Interrupts. The Z86E08 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 13). The five sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86E08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

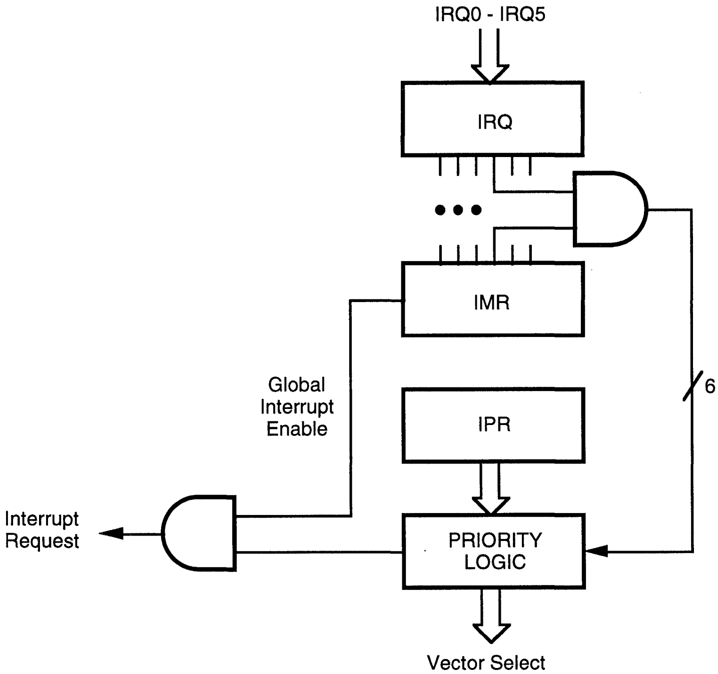


Figure 13. Interrupt Block Diagram

Clock. The Z86E08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source. The crystal should be AT cut, 12 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors (capacitance is between 10 pF to 250 pF depending upon the crystal manufacturer, ceramic resonator and PCB layout) from each pin to device ground pin (Figure 14).

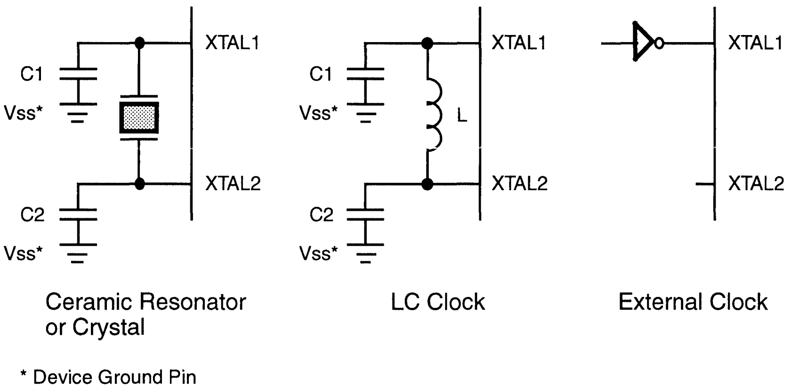


Figure 14. Oscillator Configuration

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. The I_{CC} in HALT state is I_{CC} (run mode) divided-by-ten. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). Program execution begins at location 000C (Hex). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
OR    P2M, #80H
NOP
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF   NOP;    clear the pipeline
6F   STOP;   enter STOP mode
             or
FF   NOP;    clear the pipeline
7F   HALT;   enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 15 µsec; otherwise, the Z86E08 resets itself.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This has to be done at least every 15 µsec. Otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of 50 µsec +18 XTAL clock cycles.

SPECIAL FUNCTIONS (Continued)

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Auto Reset Voltage (V_{RST}). The Z86E08 has an auto-reset built-in. The auto-reset circuit resets the Z86E08 when it detects the V_{CC} below V_{RST}. Figure 15 shows the Auto Reset Voltage vs temperature.

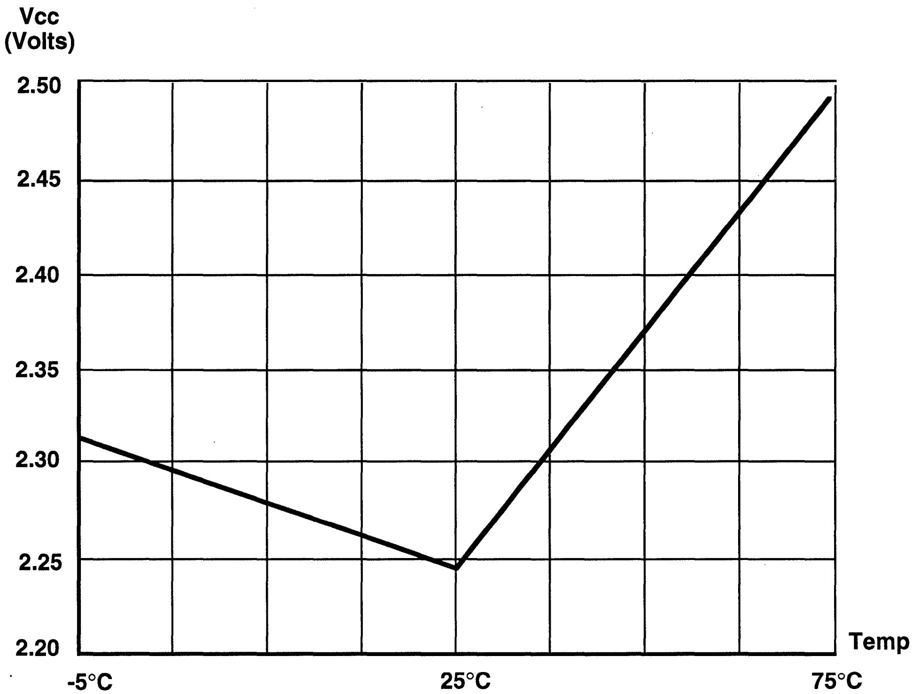


Figure 15. Typical Auto Reset Voltage (V_{RST}) vs Temperature

Low EMI Emission

The Z86E08 can be programmed to operate in a low EMI emission mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Z86E08 offers programmable ROM Protect and programmable Low Noise features. When the device is programmed for ROM Protect, the Low Noise feature will automatically be enabled. When programmed for Low Noise, the ROM Protect feature is optional.

Besides V_{DD} and GND (V_{SS}), the Z86E08 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as /PGM.

ROM Protect. ROM Protect fully protects the Z86E08 ROM code from being read externally. When ROM Protect is selected, the Z86E08 will disable the instructions LDC and LDCI (Z86E08 and Z86C08 do not support the instructions of LDE and LDEI).

User Modes. Table 5 shows the programming voltage of each mode of Z86E08.

Table 5. OTP Programming Table

Programming Modes	Device	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	All	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	All	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	All	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
LOW NOISE SELECT	E08	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

SPECIAL FUNCTIONS (Continued)

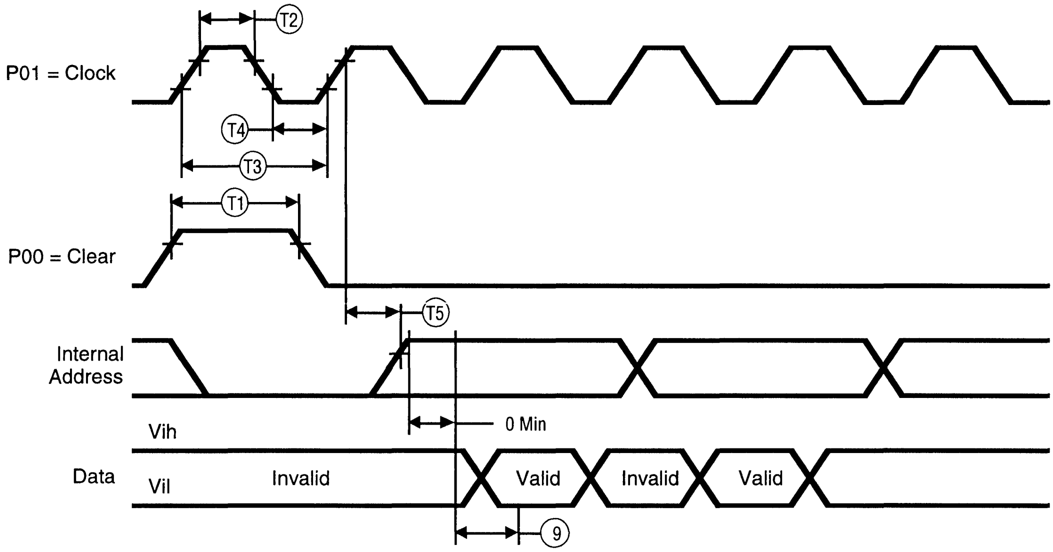
Internal Address Counter. The address of Z86E08 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the set-up time of the serial address input.

Programming Waveform. Figures 17, 18 and 19 show the programming waveforms of each mode. Table 6 shows the timing of programming waveforms.

Programming Algorithm. Figure 20 shows the flow chart of the Z86E08 programming algorithm.

Table 6. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 16. Z86E08 Address Counter Waveform

Low EMI Emission (Continued)

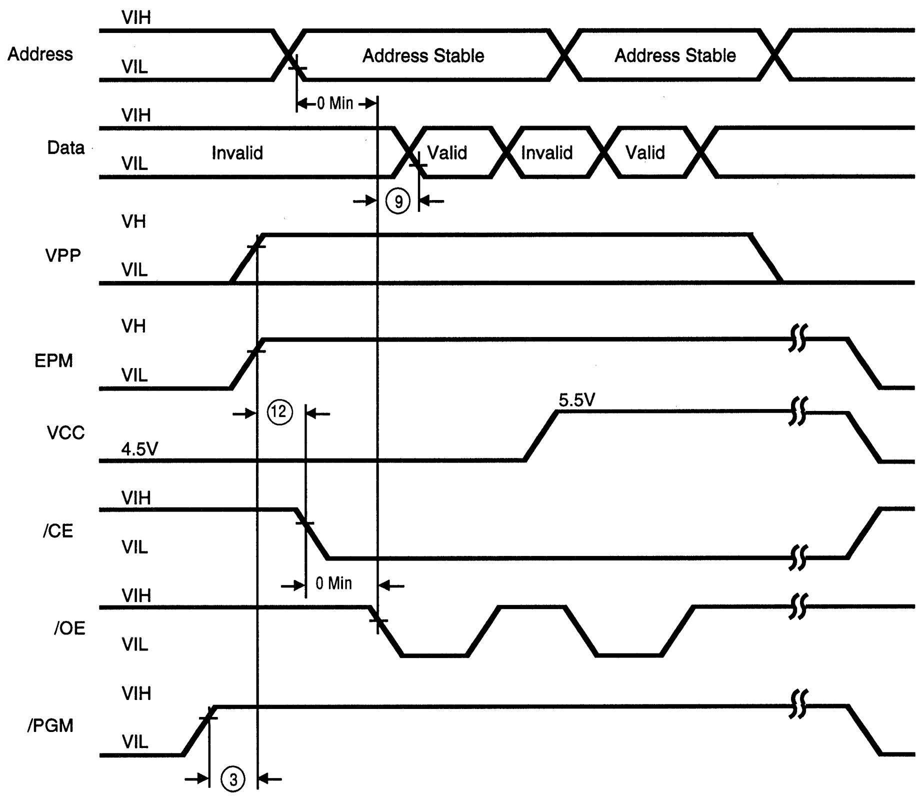


Figure 17. Z86E08 Programming Waveform (EPROM Read)

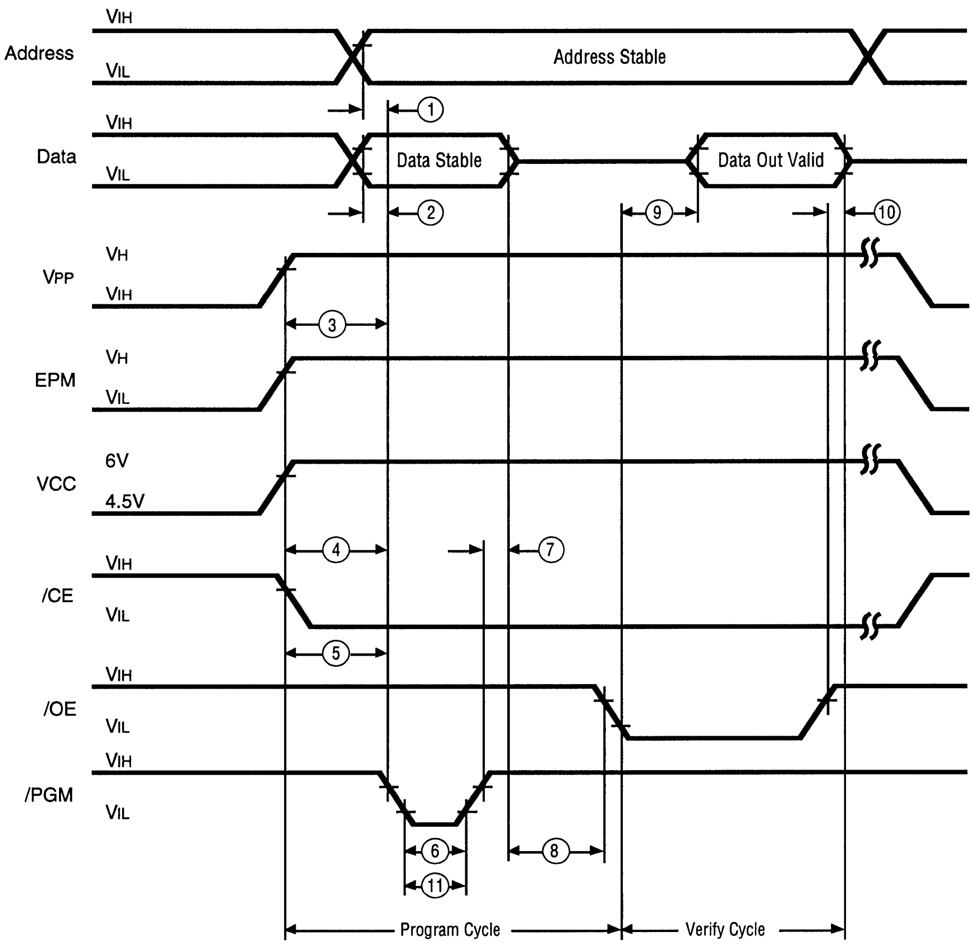


Figure 18. Z86E08 Programming Waveform (Program and Verify)

Low EMI Emission (Continued)

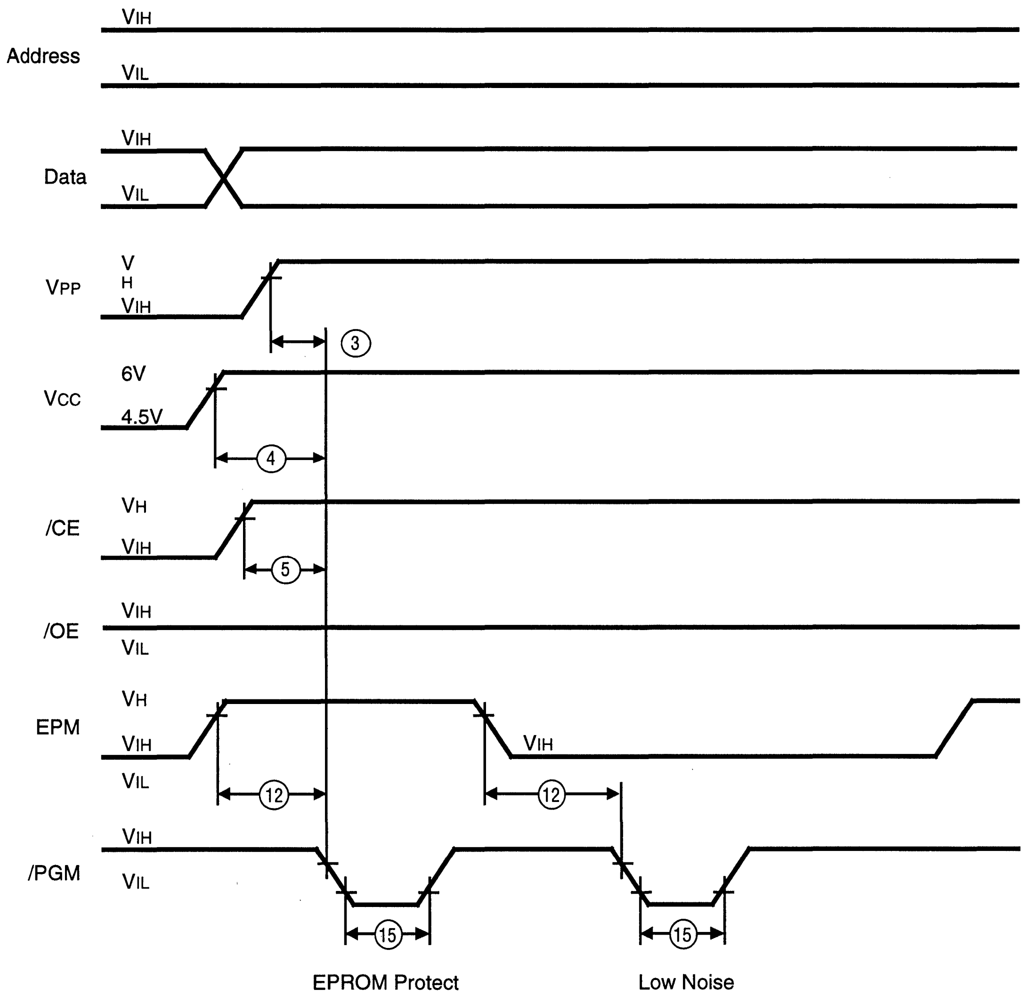


Figure 19. Z86E08 Programming Waveform (EPROM Protect and Low EMI Program)

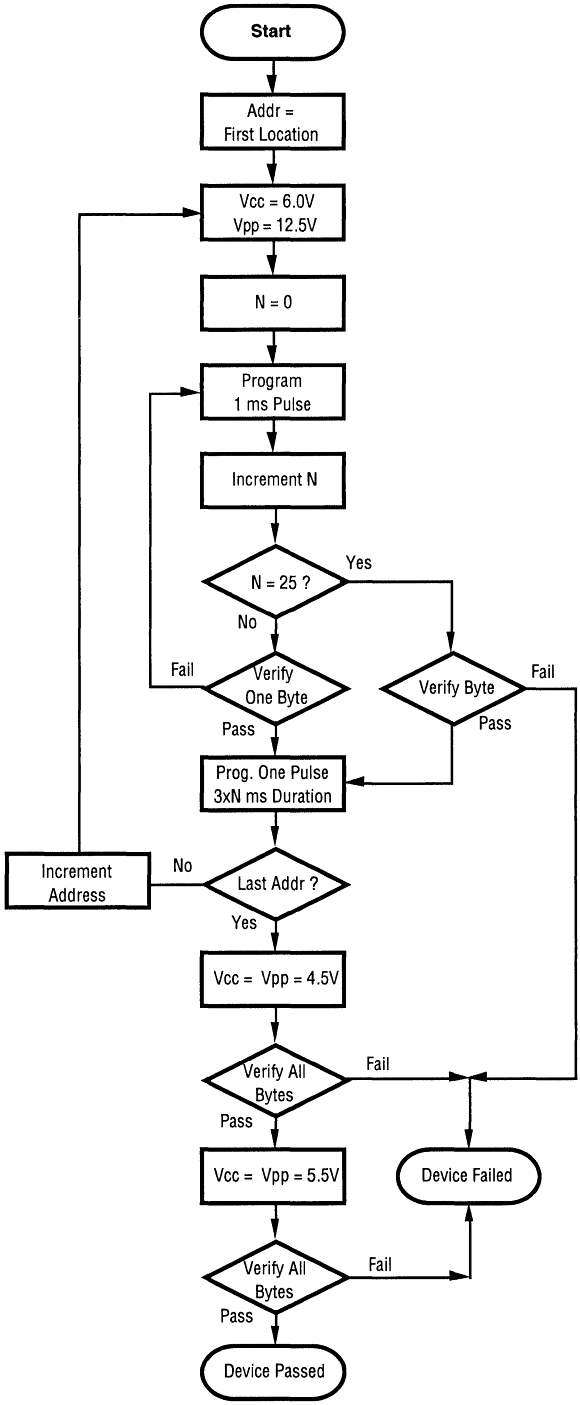


Figure 20. Z86E08 Programming Algorithm

3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 19).

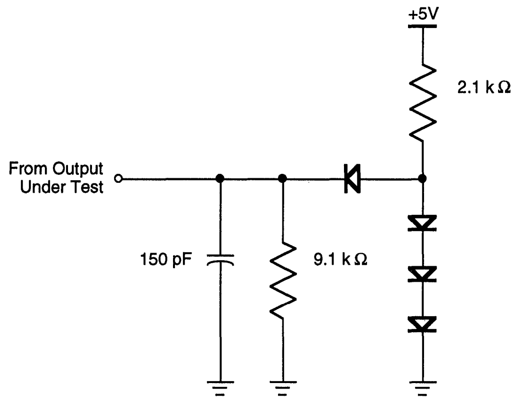


Figure 21. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f =1.0 MHz, unmeasured pins to GND.

Parameter	Max
Input Capacitance	10 pF
Output Capacitance	20 pF
I/O Capacitance	25 pF

V_{CC} SPECIFICATION

4.5V to 5.0V ± 0.5V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage	4.5V		12		V	V_{IN} = 250 µA
		5.5V		12		V	V_{IN} = 250 µA
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.6		Driven by External Clock Generator
		5.5V	V_{SS}–0.3	0.2 V_{CC}	2.3	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.1	V	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.7	V	
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.2	V	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		3.9	V	I_{OH} = –2.0 mA
		5.5V	V_{CC}–0.4		5.4	V	I_{OH} = –2.0 mA
V_{OL1}	Output Low Voltage	4.5V		0.8	0.2	V	I_{OL} = +4.0 mA
		5.5V		0.4	0.2	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	4.5V		TBD	0.7	V	I_{OL} = +12 mA, 3 Pin Max
		5.5V		0.8	0.5	V	I_{OL} = +12 mA, 3 Pin Max
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		10	6	mV	
		5.5V		25	7	mV	
V_{RST}	Auto Reset Voltage		1.55	2.7	2.4	V	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	4.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	1.0	µA	V_{IN} = 0V, V_{CC}

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current (Standard Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0	5.0	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		9.0	4.5	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0	8.3	mA	All Output and I/O Pins Floating @ 8 MHz
		4.5V		10	6.1	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15	10.8	mA	All Output and I/O Pins Floating @ 12 MHz
I_{CC1}	Standby Current (Standard Mode)	4.5V		2.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		4.5V		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		4.5V		5.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
		5.5V		7.0	2.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
I_{CC}	Supply Current (Low Noise Mode)	4.5V		4.0	2.2	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0	4.2	mA	All Output and I/O Pins Floating @ 1 MHz
		4.5V		6.0	2.9	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0	5.5	mA	All Output and I/O Pins Floating @ 2 MHz
		4.5V		8.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0	7.9	mA	All Output and I/O Pins Floating @ 4 MHz

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		1.2	0.4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		4.5V		1.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		4.5V		2.0	0.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	4.5V		10	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	4.5V		–7.0	–3.3	µA	0V < V_{IN} < V_{CC}
		5.5V		–7.0	–6.5	µA	0V < V_{IN} < V_{CC}
I_{ALH}	Auto Latch High Current	4.5V		10	–6.0	µA	0V < V_{IN} < V_{CC}
		5.5V		15	11.5	µA	0V < V_{IN} < V_{CC}

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on Crystal	3.0	5.0	mA	8 MHz
or XTAL Resonator	0.3	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

3

AC ELECTRICAL CHARACTERISTICS

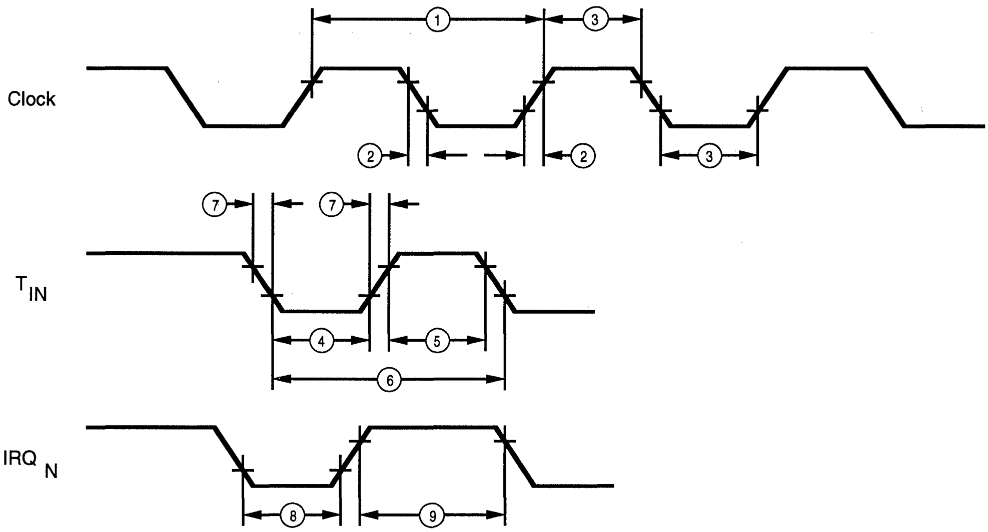


Figure 22. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	1000		250	100,000	ns	[1]
			5.5V	1000		250	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	4.5V	450		100		ns	[1]
			5.5V	450		100		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	1.5TpC		1.5TpC			[1]
			5.5V	1.5TpC		1.5TpC			[1]
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	1.5TpC		1.5TpC			[1]
			5.5V	1.5TpC		1.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		20		20	ms	[1]
			5.5V		15		15	ms	[1]
11	TPOR	Power-On Reset Time	4.5V		100		100	ms	[1]
			5.5V		90		90	ms	[1]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

3

AC ELECTRICAL CHARACTERISTICS
Standard Mode, Standard Temperature

				T_A = 0°C to +70°C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	TpC	Input Clock Period	4.5V	125	100,000	83	100,000	ns	[1]
			5.5V	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	4.5V	37		26		ns	[1]
			5.5V	37		26		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	3TpC		3TpC			[1]
			5.5V	3TpC		3TpC			[1]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	4.5V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	4.5V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	4.5V	3TpC		3TpC			[1]
			5.5V	3TpC		3TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	4.5V		50		50	ms	[1]
			5.5V		45		45	ms	[1]
11	TPOR	Power-On Reset Timer	4.5V		100		100	ms	[1]
			5.5V		90		90	ms	[1]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

Z8 CONTROL REGISTERS

R241 TMR

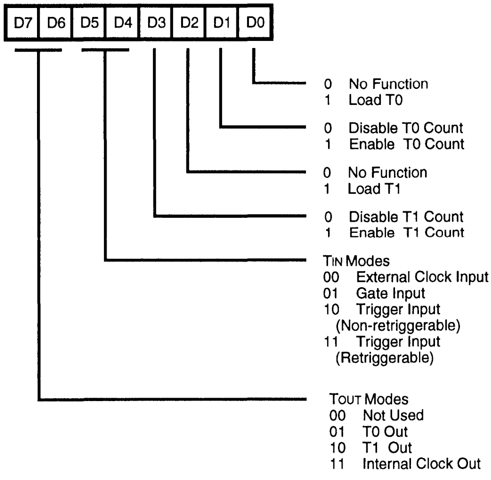


Figure 23. Timer Mode Register (F1H: Read/Write)

R242 T1

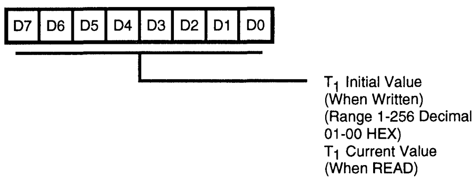


Figure 24. Counter Timer 1 Register (F2H: Read/Write)

R243 PRE1

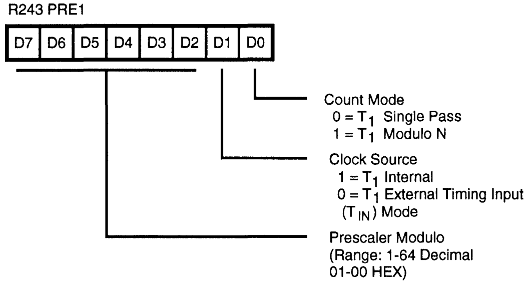


Figure 25. Prescaler 1 Register (F3H: Write Only)

R244 T0

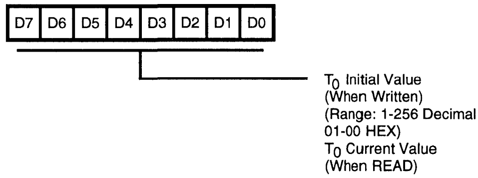


Figure 26. Counter/Timer 0 Register (F4H: Read/Write)

R245 PRE0

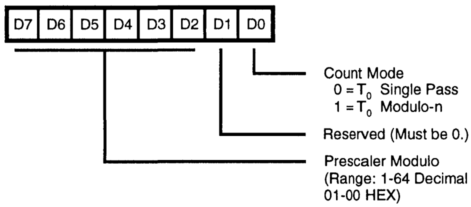


Figure 27. Prescaler 0 Register (F5H: Write Only)

R246 P2M

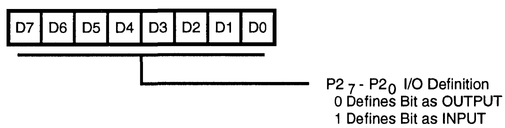


Figure 28. Port 2 Mode Register (F6H: Write Only)

R247 P3M

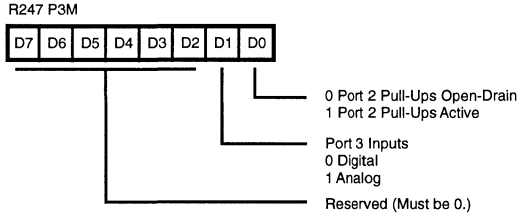


Figure 29. Port 3 Mode Register (F7H: Write Only)

Z8 CONTROL REGISTERS (Continued)

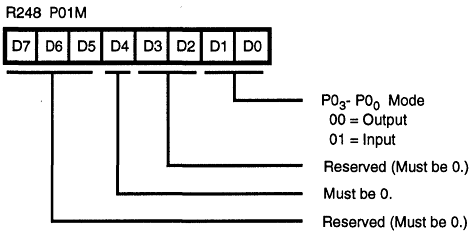


Figure 30. Port 0 and 1 Mode Register (F8H: Write Only)

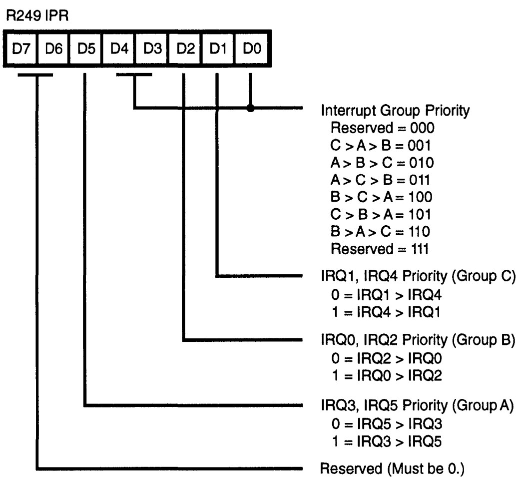


Figure 31. Interrupt Priority Register (F9H: Write Only)

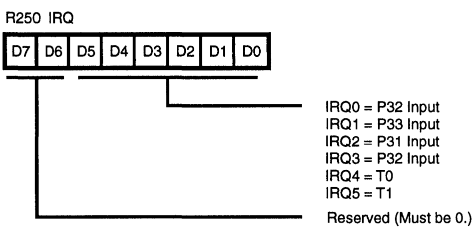


Figure 32. Interrupt Request Register (FAH: Read/Write)

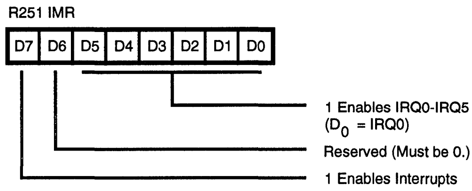


Figure 33. Interrupt Mask Register (FBH: Read/Write)

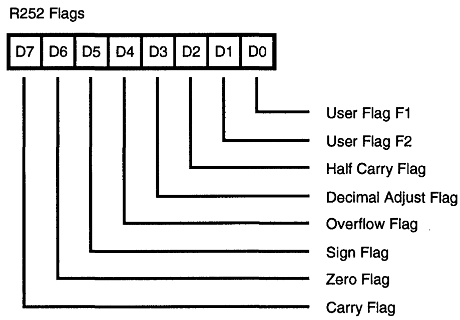


Figure 34. Flag Register (FCH: Read/Write)

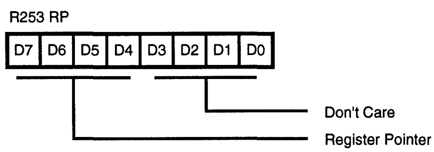


Figure 35. Register Pointer (FDH: Read/Write)

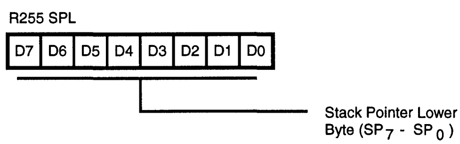


Figure 36. Stack Pointer (FFH: Read/Write)

OPERATING MODES

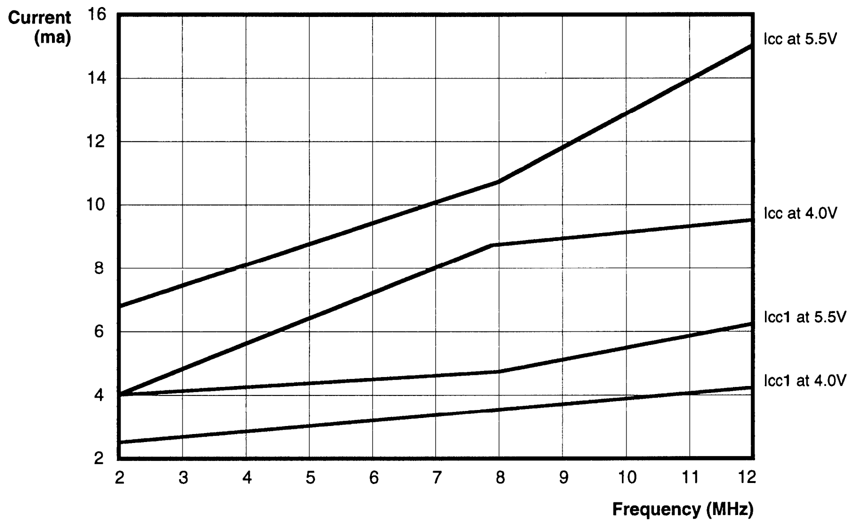


Figure 37. Maximum I_{CC} and I_{CC1} vs Frequency in Standard Mode

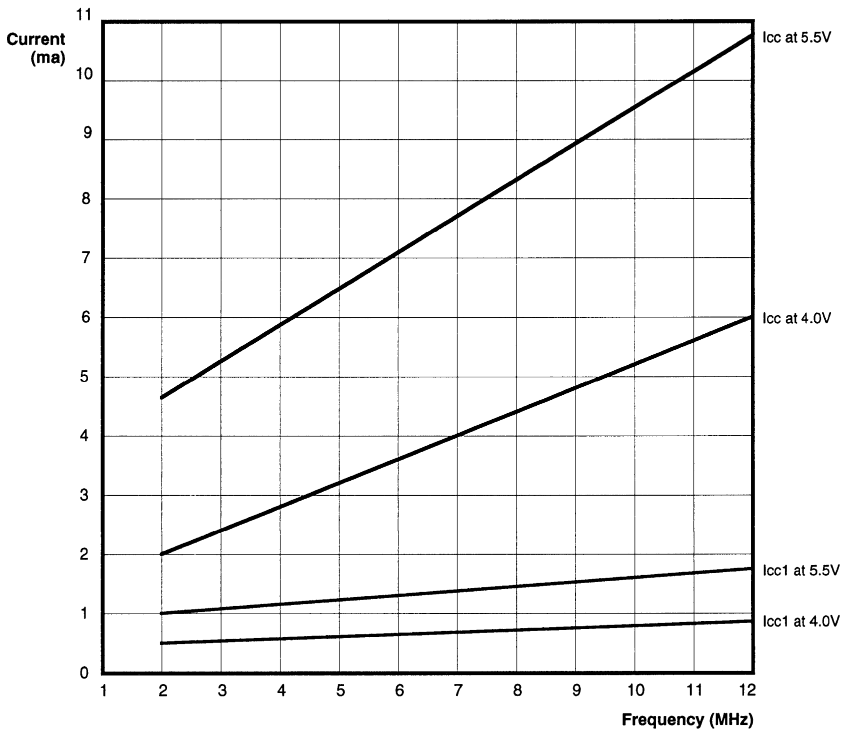


Figure 38. Typical I_{CC} and I_{CC1} vs Frequency in Standard Mode

OPERATING MODES (Continued)

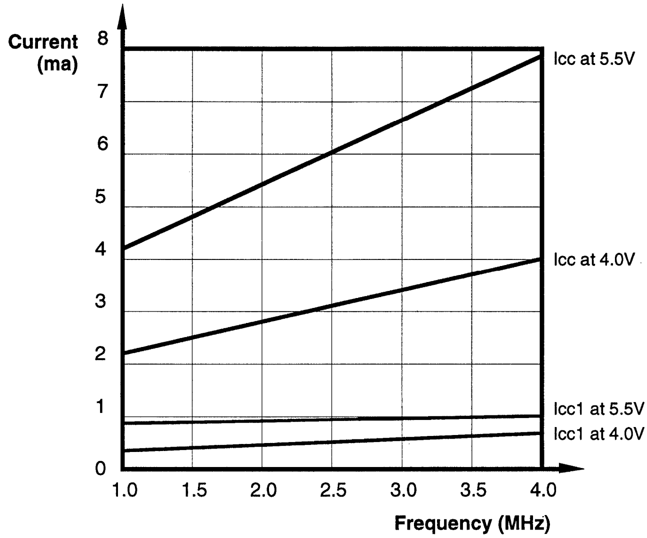
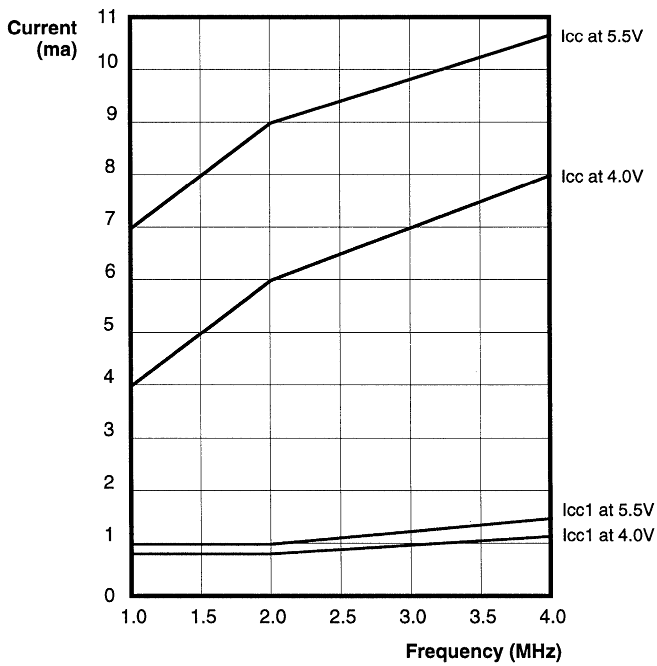


Figure 39. Typical I_{CC} and I_{CC1} vs Frequency in Low EMI Mode



igure 40. Maximum I_{CC} and I_{CC1} vs Frequency in Low EMI Mode

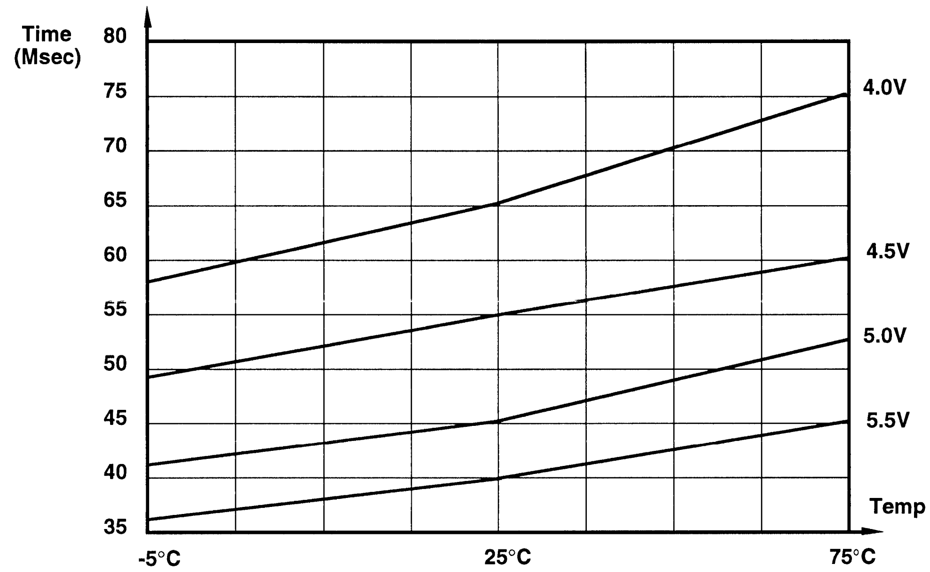


Figure 41. Typical POR Time Out Period vs Temperature

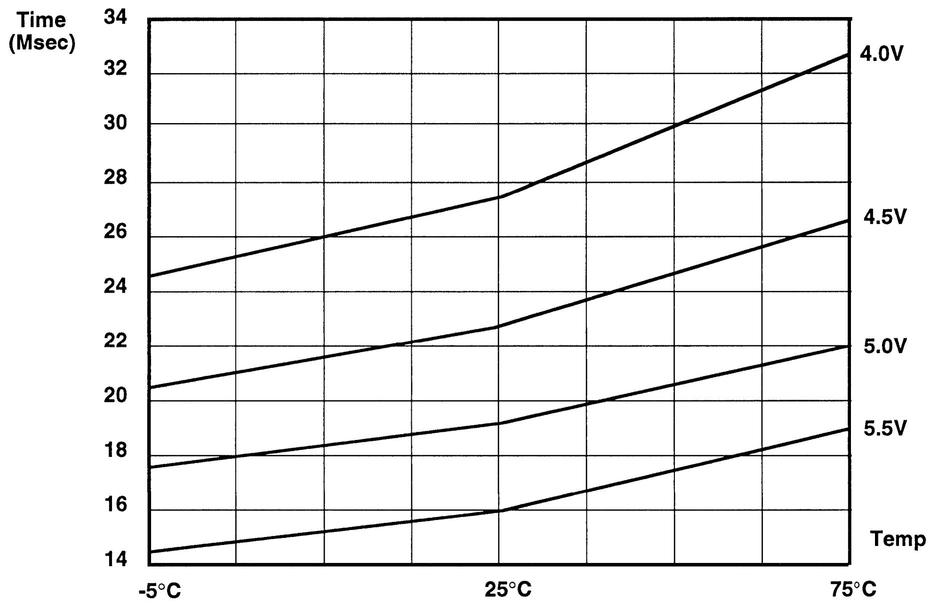


Figure 42. Typical WDT Time Out Period vs Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

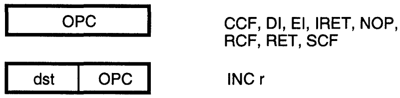
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

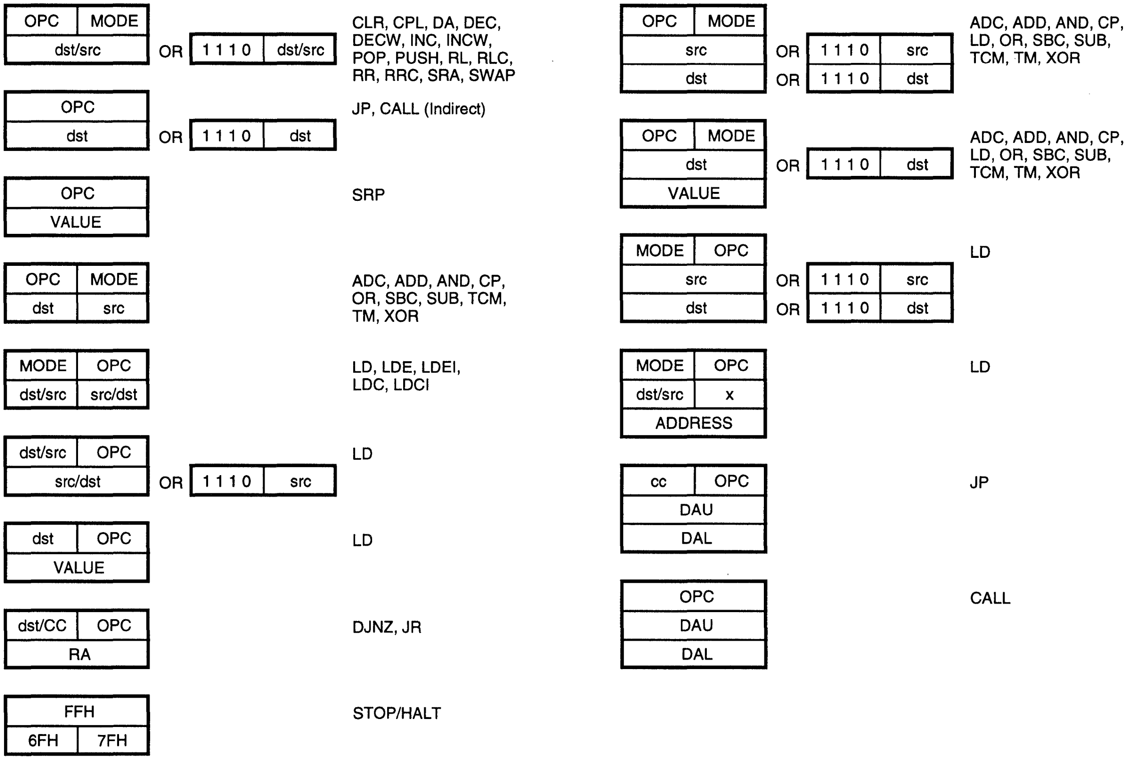
Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	---

3

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions **Three-Byte Instructions**

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

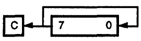
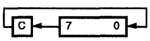
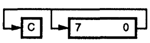
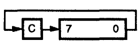
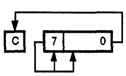
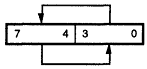
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - -
CCF C←NOT C			EF	* - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst – src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst – 1	R IR		00 01	- * * * - -
DECW dst dst←dst – 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - -
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 - F	- - - - - -
EI IMR(7)←1			9F	- - - - - -
HALT			7F	- - - - - -
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	- - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - -
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	- - - - - -

3

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP		FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†	2[ ]	[	[	[	[	1	[
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
WDH		4F	-	-	-	-	-	-
WDT		5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

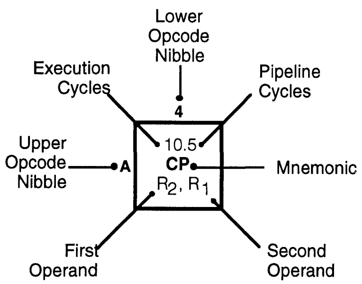
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) (columns) / **Upper Nibble (Hex)** (rows)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1							↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



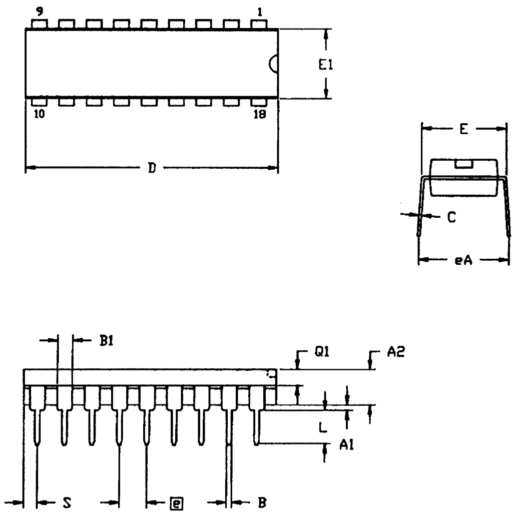
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram

ODERING INFORMATION

Z86E08

8 MHz	12 MHz
Z86E0808PSC	Z86E0812PSC

For fast results, contact your local Zilog sales office or technical center for assistance in ordering the part desired.

Package
P=Plastic DIP

Temperature
S = 0°C to +70°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C= Plastic Standard

Example:

Z 86E08 12 P S C is an Z86E08, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E08 — Product Number
- Z — Zilog Prefix

Introduction | I

Z86C07 Z8® CMOS 8-Bit Microcontroller | 1

Z86C08 Z8® CMOS 8-Bit Microcontroller | 2

Z86E08 Z8® CMOS 8-Bit OTP Microcontroller | 3

Z86C11 Z8® CMOS Microcontroller | 4

Z86C12 Z8® CMOS In-Circuit Emulator MCU | 5

Z86C21 Z8® CMOS 8K ROM Microcontroller | 6

Z86C11

CMOS Z8®
MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC or 44-Pin QFP Package
- 4.5 to 5.5 Voltage Operating Range
- Low Power Consumption - 220 mW (max) @ 16 MHz
- Fast Instruction Pointer - 1.0 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- Low EMI Option
- 4 Kbytes of ROM
- 256 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 12 and 16 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.

GENERAL DESCRIPTION

The Z86C11 is a member of the Z8 single-chip microcontroller family with 4 Kbytes of ROM and 256 bytes of RAM. The MCU is housed in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP, and is manufactured in CMOS technology.

The ROMless pin option is available on the 44-pin versions only. Having the ROM/ROMless selectivity, the MCU offers both external memory and preprogrammed ROM. This enables the Z8 microcontroller to be used in high volume applications, or where code flexibility is required.

Zilog's Z86C11 microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C11 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C11 provides 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight-lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C11 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

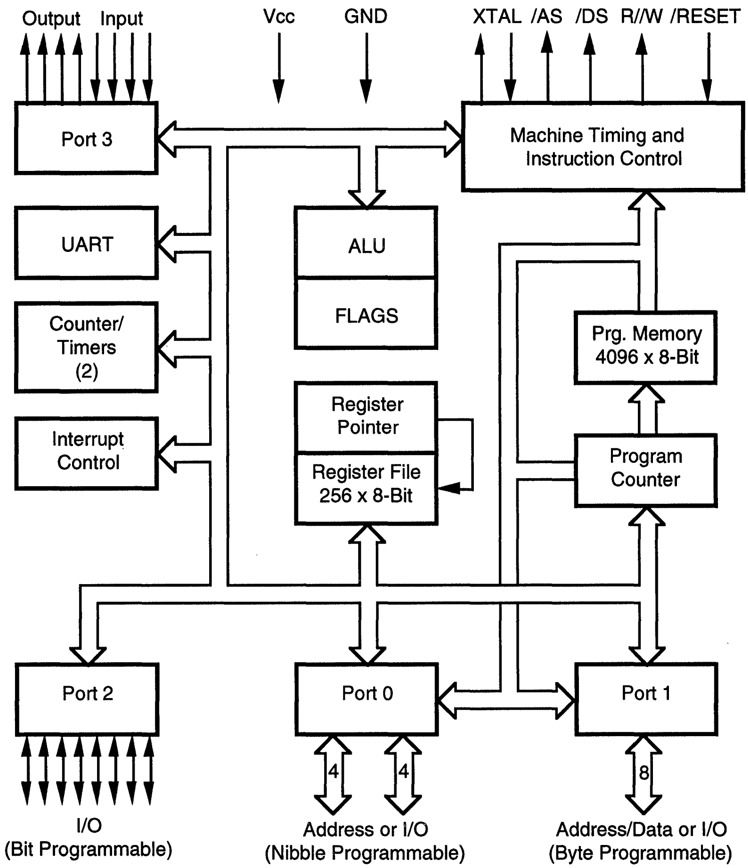


Figure 1. Functional Block Diagram

PIN DESCRIPTION

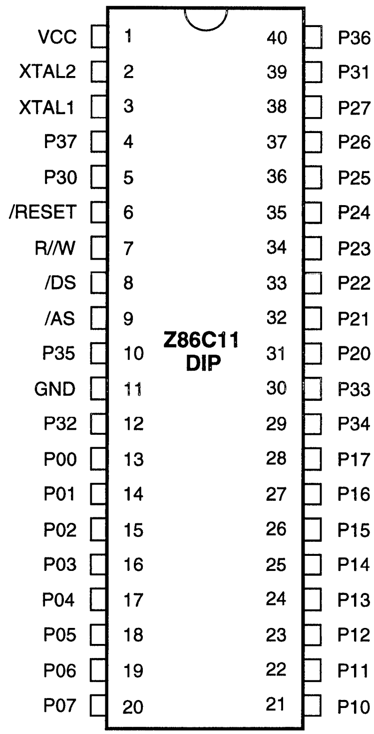


Figure 2. 40-Pin DIP Pin Assignments

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, pin 7	Output
5	P30	Port 3, pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, pin 5	Output
11	GND	Ground	
12	P32	Port 3, pin 2	Input
13-20	P00-P07	Port 0, pins 0 through 7	In/Output
21-28	P10-P17	Port 1, pins 0 through 7	In/Output
29	P34	Port 3, pin 4	Output
30	P33	Port 3, pin 3	Input
31-38	P20-P27	Port 2, pins 0 through 7	In/Output
39	P31	Port 3, pin 1	Input
40	P36	Port 3, pin 6	Output

PIN DESCRIPTION (Continued)

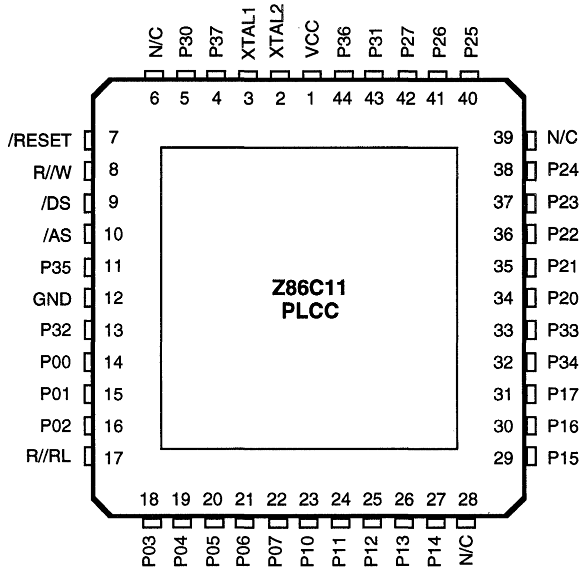


Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0, Pins 0, 1, 2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0, Pins 3, 4, 5, 6, 7	In/Output
4	P37	Port 3, Pin 7	Output	23-27	P10-P14	Port 1, Pins 0, 1, 2, 3, 4	In/Output
5	P30	Port 3, Pin 0	Input	28	N/C	Not Connected	
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1, Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3, Pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3, Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2, Pins 0, 1, 2, 3, 4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	
11	P35	Port 3, Pin 5	Output	40-42	P25-P27	Port 2, Pins 5, 6, 7	In/Output
12	GND	Ground	Input	43	P31	Port 3, Pin 1	Input
13	P32	Port 3, Pin 2	Input	44	P36	Port 3, Pin 6	Output

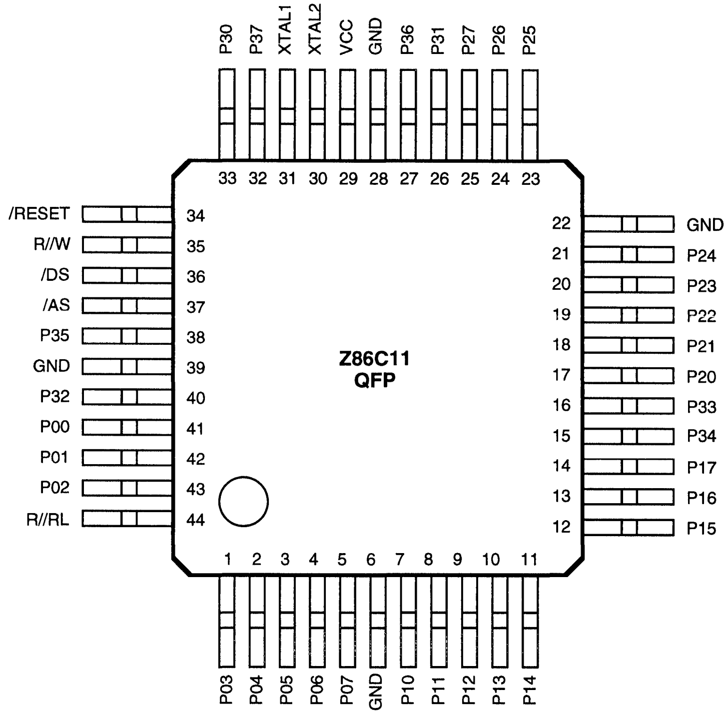


Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Pins 3, 4, 5, 6, 7	In/Output
6	GND	Ground	
7-14	P10-P17	Port 1, Pins 0 through 7	In/Output
15	P34	Port 3, Pin 4	Output
16	P33	Port 3, Pin 3	Input
17-21	P20-P24	Port 2, Pins 0, 1, 2, 3, 4	In/Output
22	GND	Ground	
23-25	P25-P27	Port 2, Pins 5,6,7	In/Output
26	P31	Port 3, Pin 1	Input
27	P36	Port 3, Pin 6	Output
28	GND	Ground	Input
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output

Pin #	Symbol	Function	Direction
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Pin 7	Output
33	P30	Port 3, Pin 0	Input
34	/RESET	Reset	Input
35	R//W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3, Pin 5	Output
39	GND	Ground	
40	P32	Port 3, Pin 2	Input
41-43	P00-P02	Port 0, Pins 0, 1, 2	In/Output
44	R//RL	ROM/ROMless control	Input

4

PIN FUNCTIONS

/ROMless (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the part functions as a normal Z86C11 ROM version). This pin is only available on the 44-pin versions of the Z86C11.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C11 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs. On the 5th clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control. For the ROMless option, Port 0 comes up as A15-A8 Address lines after /RESET.

For external memory references, Port 0 can provide address bit A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 5).

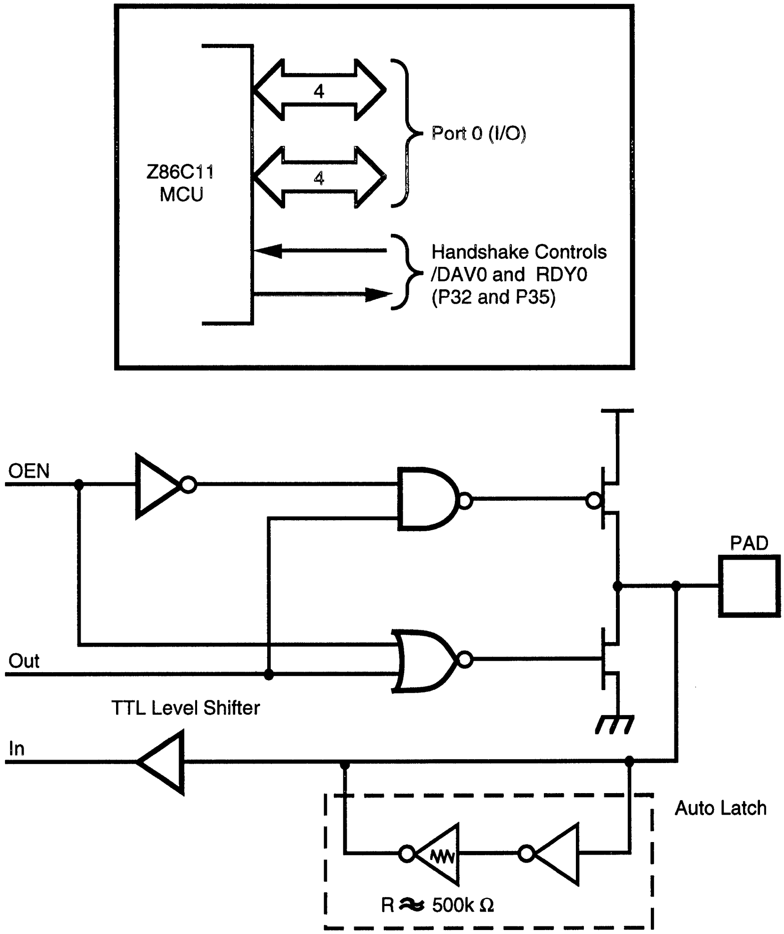


Figure 5. Port 0 Configuration

PIN FUNCTION (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C11, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/ data port for interfacing external memory. When used as an I/O port, Port 1 is placed under handshake control. In this configuration, Port 3 lines P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 4096 are referenced through Port 1. To interface external memory, Port 1 is programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS and R//W, allowing the MCU to share common resource in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 6).

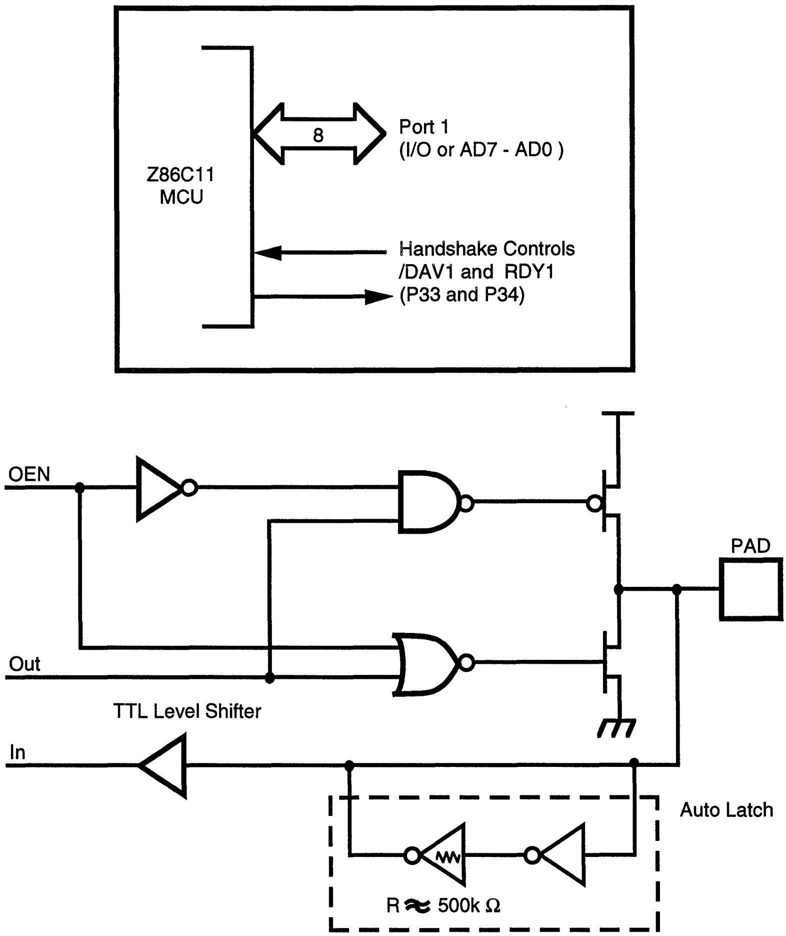


Figure 6. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7).

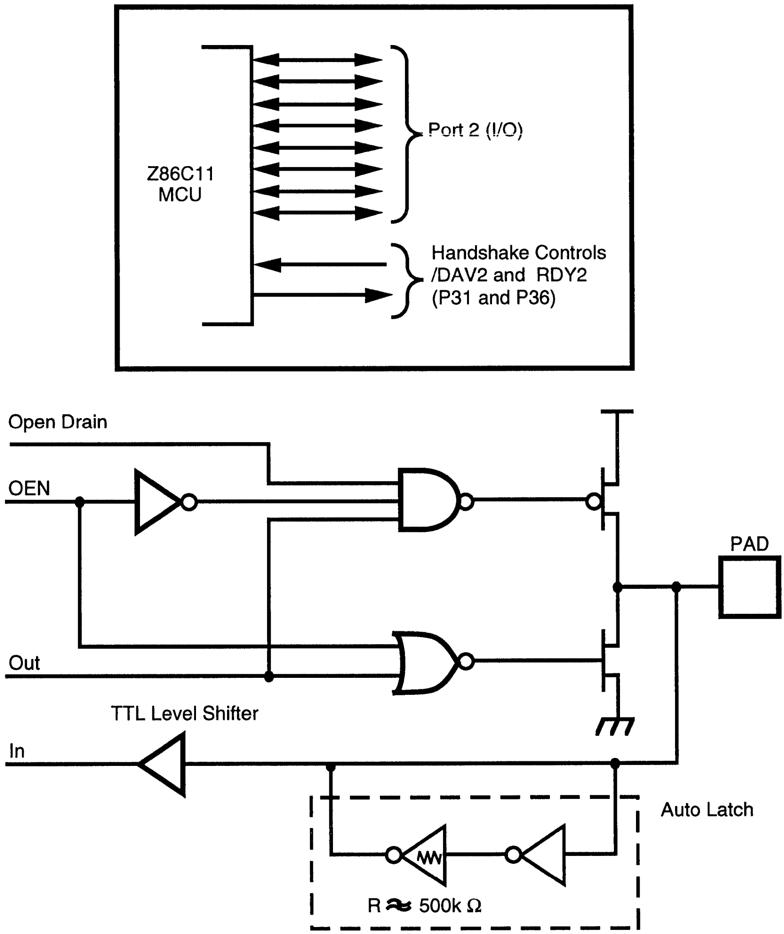


Figure 7. Port 2 Configuration

PIN FUNCTION (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, TTL compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four fixed (P37-P34) output ports. Port 3 pins P30 and P37, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 8).

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0, 1 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

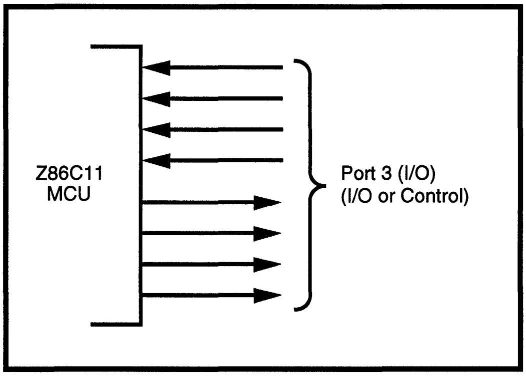


Figure 8. Port 3 Configuration

Table 4. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

UART Operation. Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z86C11 automatically adds a start bit and two stop bits to transmitted data (Figure 9). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

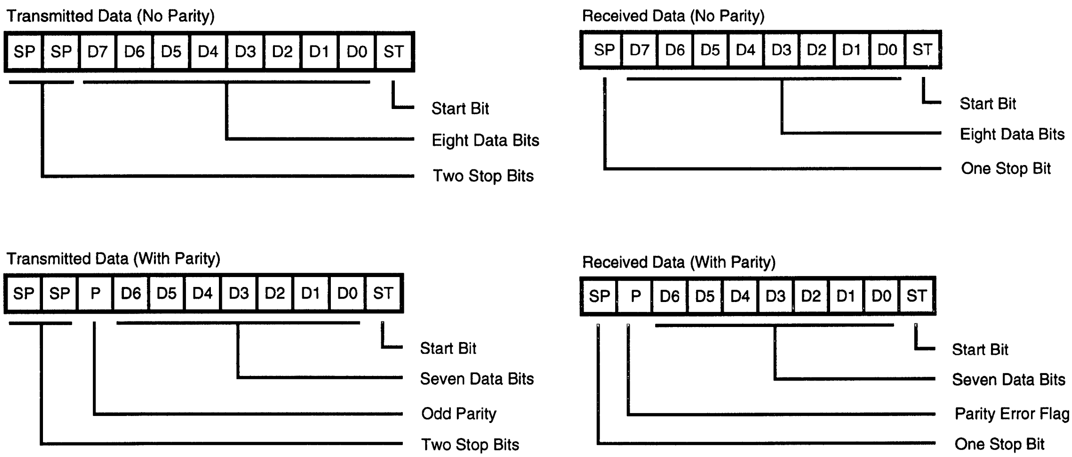


Figure 9. Serial Data Formats

Auto-Latch. The Auto-Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This will reduce excessive supply current flow in the input buffer when it is not been driven by any source.

Low EMI Option. The Z86C11 is available in a low EMI option. This option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted. Use of this feature results in:

- Less than 1 mA current consumptions during HALT mode.
- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 ohms typical.
- Oscillator divide-by-two circuitry is eliminated.
- Internal SCLK/TCLK operation is limited to a maximum of 4 MHz (250 ns cycle time).

4

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C11 can address up to 60 Kbytes of external program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 4095 consists of on-chip ROM. At address 4096 and greater, the Z86C11 executes external program memory fetches. In the ROMless mode, the Z86C11 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000C (HEX) after a reset.

Data Memory (/DM). The ROM version can address up to 60 Kbytes of external data memory space beginning at location 4096. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 11). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

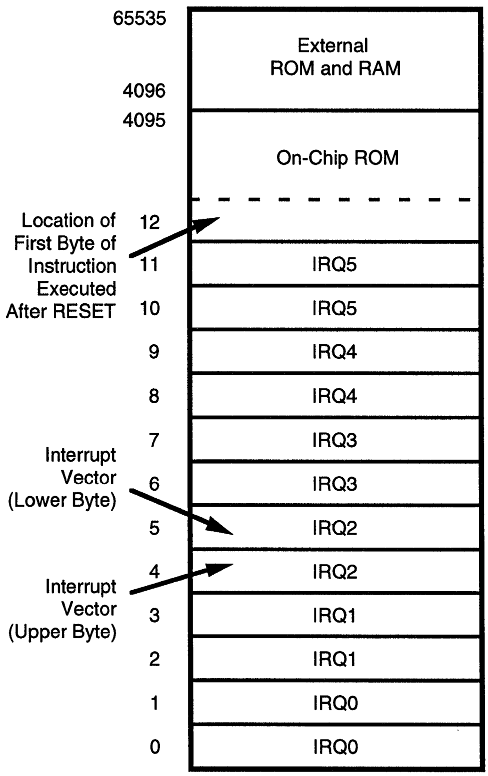


Figure 10. Program Memory Configuration

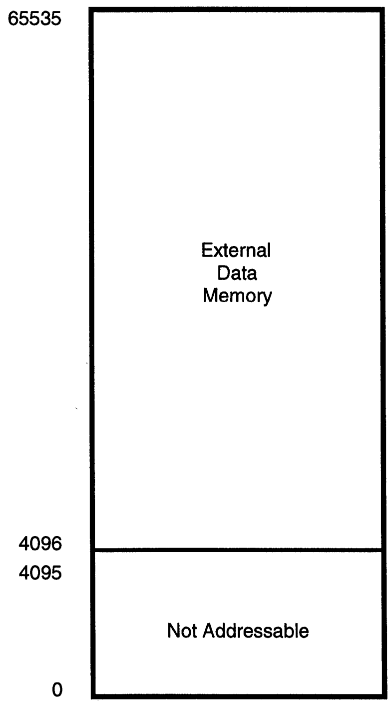


Figure 11. Data Memory Configuration

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 12). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C11 also allows short 4-bit register addressing using the Register Pointer (Figure 13). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

LOCATION		IDENTIFIERS
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
4	General-Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Port1	P1
0	Port 0	P0

Figure 12. Register File

4

FUNCTIONAL DESCRIPTION (Continued)

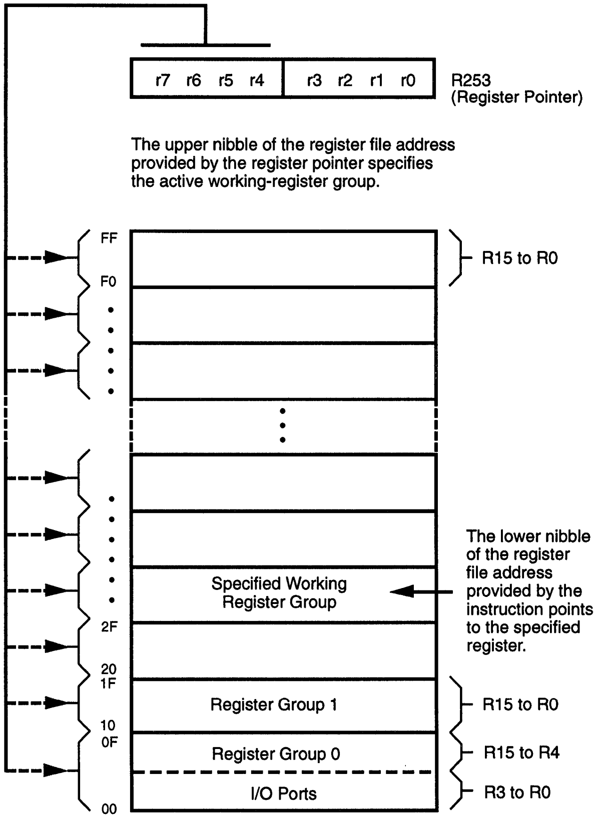


Figure 13. Register Pointer

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 4 Kbytes of program memory is mask programmable. A ROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Note: With ROM Protect enabled, the Z86C11 cannot access the memory space.

Stack. The Z86C11 has a 16-bit Stack Pointer (R254-R255) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 4096 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH-Bit 8-15) is used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 14).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

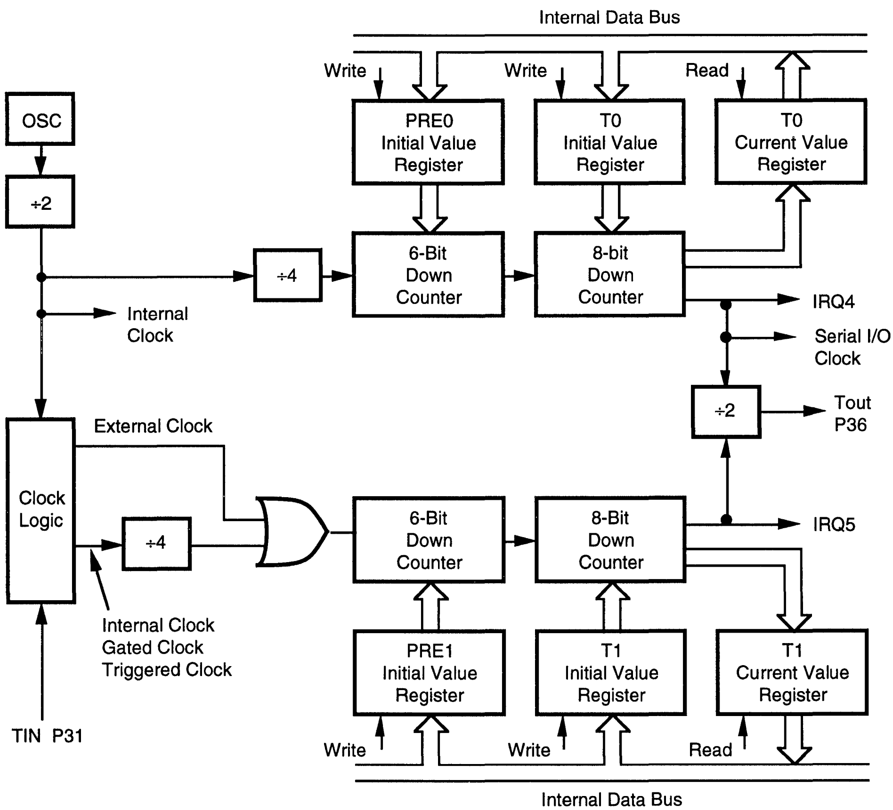


Figure 14. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C11 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 15). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z86C11 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request (IRQ) register.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

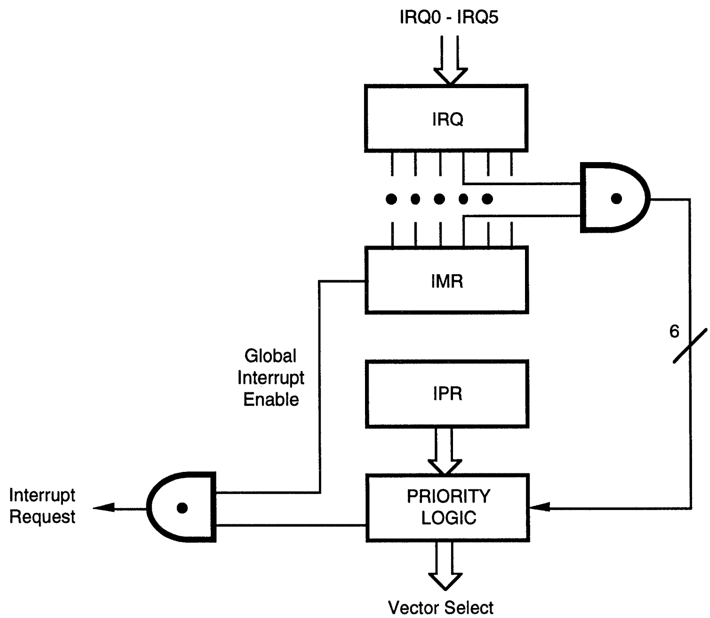


Figure 15. Interrupt Block Diagram

Clock. The Z86C11 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 300 pF) from each pin to ground (Figure 16).

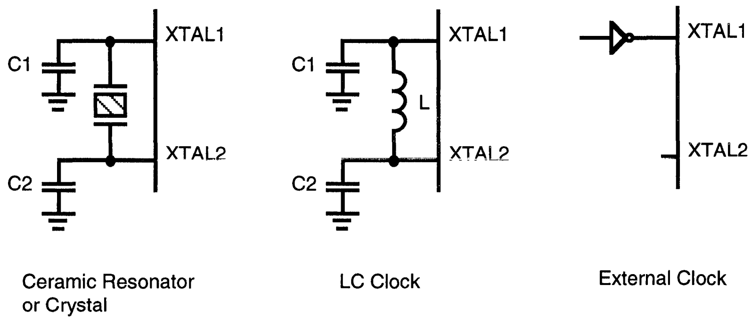


Figure 16. Oscillator Configuration

HALT. Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remains active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical). The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode = OFFH) immediately before the appropriate sleep instruction,. i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

4

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp		†	°C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 17).

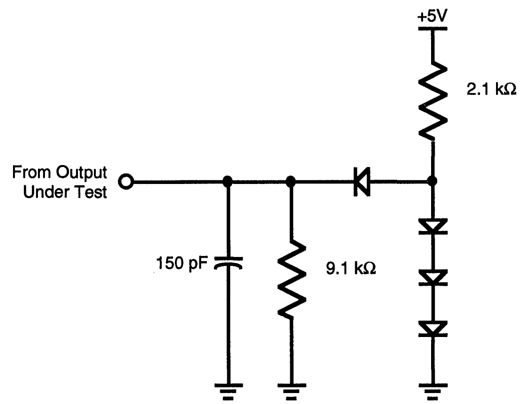


Figure 17. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to 70°C Min	Max	T_A = –40°C to 105°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC}+0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100 mV		V_{CC}–100 mV			V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC}+0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.8	–0.03	0.8		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	V_{RL} = 0V
I_{CC}	Supply Current		30		30	20	mA	[1] @ 12 MHz
			35		35	24	mA	[1] @ 16 MHz
I_{CC1}	Standby Current		6.5		6.5	4	mA	[1] HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			7.0		7.0	4.5	mA	[1] HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1, 2] STOP Mode V_{IN} = 0V, V_{CC}

Notes:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.
[2] I_{CC2} requires loading TMR (F1H) with any value prior to STOP execution.
Use this sequence:

```
LD TMR,#00
NOP
STOP
```

4

AC CHARACTERISTICS
External I/O or Memory Read or Write Timing Diagram

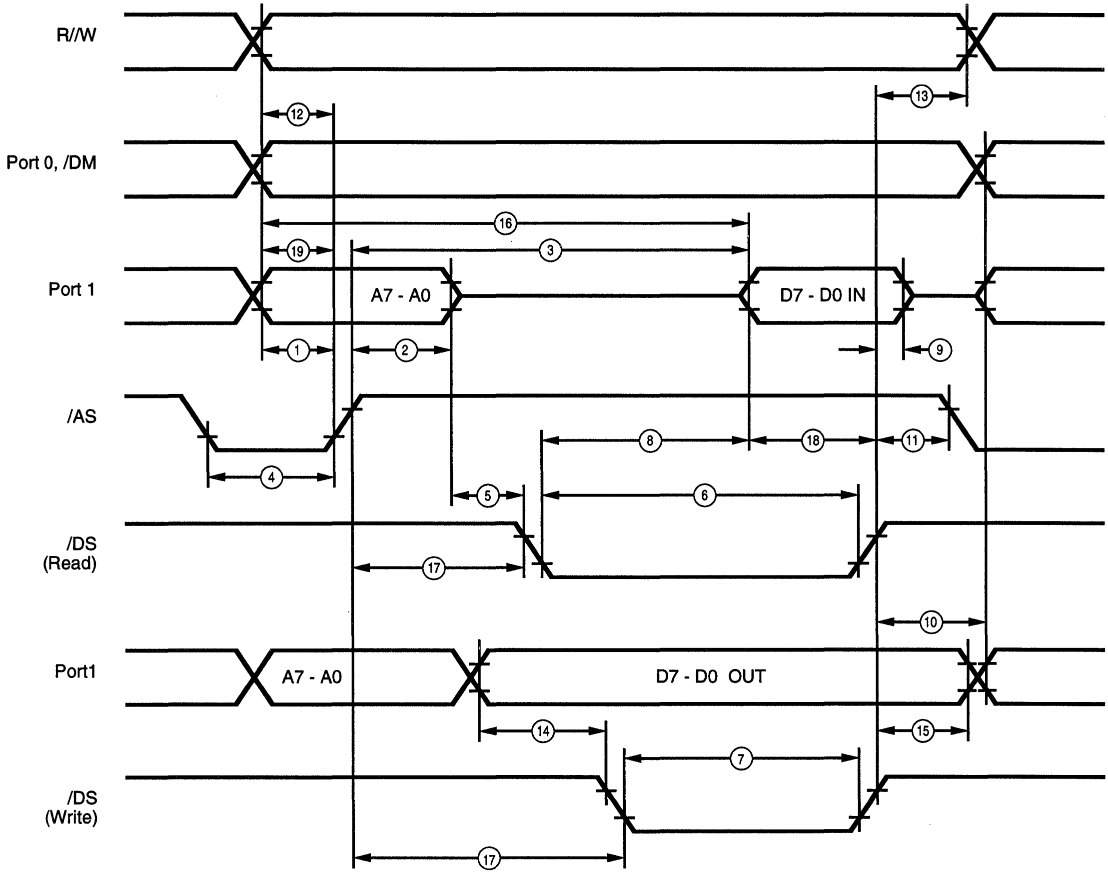


Figure 18. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
External I/O or Memory Read or Write Timing Table

			T_A = 0°C to 70°C				T_A = –40°C to 105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		25		35		25		ns	[2, 3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		35		45		35		ns	[2, 3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		250		180		250		180	ns	[1, 2, 3]
4	TwAS	/AS Low Width	55		40		55		40		ns	[2, 3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1, 2, 3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1, 2, 3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1, 2, 3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2, 3]
10	TdDS(A)	/DS Rise to Address Active Delay	65		50		65		50		ns	[2, 3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	45		35		45		35		ns	[2, 3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2, 3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	50		35		50		35		ns	[2, 3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2, 3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	55		35		55		35		ns	[2, 3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		310		230		310		230	ns	[1, 2, 3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	65		45		65		45		ns	[2, 3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		75		60		ns	[1, 2, 3]
19	TdDM(AS)	/DM Valid to /AS Rise Delay	50		30		50		30		ns	[2, 3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
Standard Test Load
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC – 3.25
3	TdAS(DR)	2.38TpC + 6.14
4	TwAS	0.66TpC – 1.65
6	TwDSR	2.33TpC – 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC – 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC – 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC – 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC – 19
16	TdA(DR)	4TpC – 20
17	TdAS(DS)	0.91TpC – 10.7
18	TsDI(DS)	0.8TpC – 10
19	TdDM(AS)	0.9TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

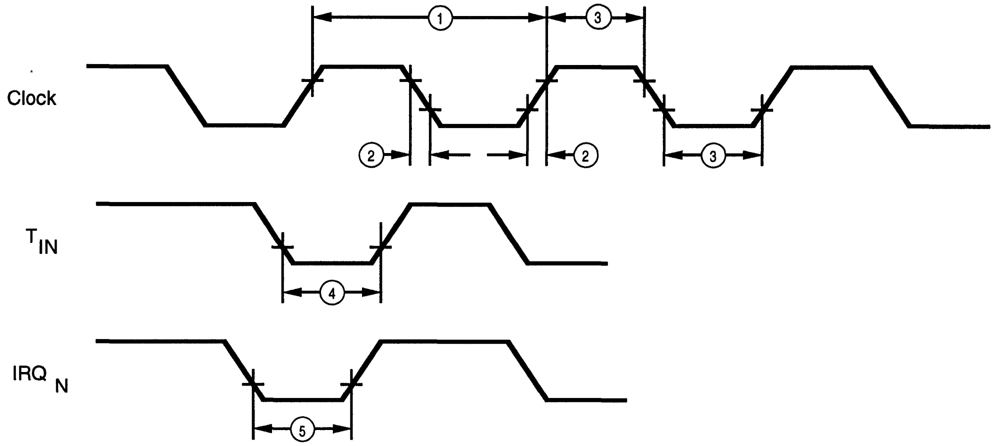


Figure 19. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

			T_A = 0°C to 70°C				T_A = –40°C to 105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	35		25		35		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		50		ns	[2, 4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC		3TpC		3TpC			[2, 5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC		3TpC			[2, 3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31)
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

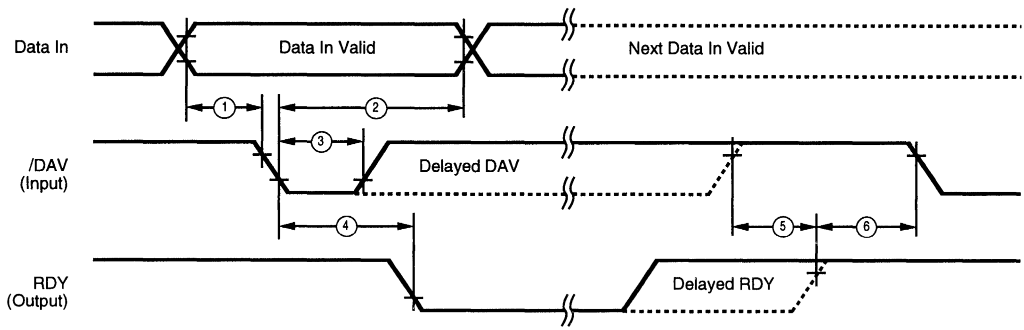


Figure 20. Input Handshake Timing

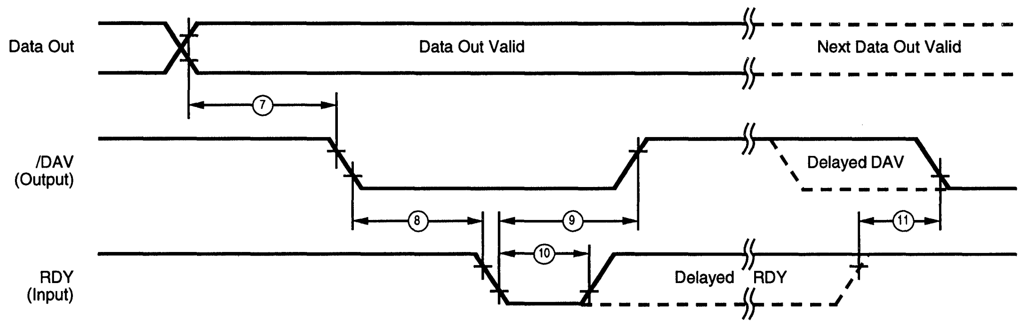


Figure 21. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

			T_A = 0°C to 70°C				T_A = –40°C to 105°C				
			12 MHz		16 MHz		12 MHz		16 MHz		Data
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		In
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		In
3	TwDAV	Data Available Width	110		110		110		110		In
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	In
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	In
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		In
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	Out
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		Out
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	Out
10	TwRDY	RDY Width	110		110		110		110		Out
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	Out

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Z8 CONTROL REGISTER DIAGRAMS

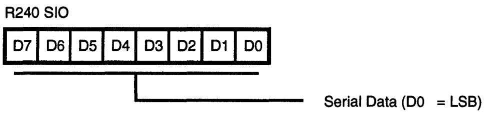

Figure 22. Serial I/O Register (F0H: Read/Write)

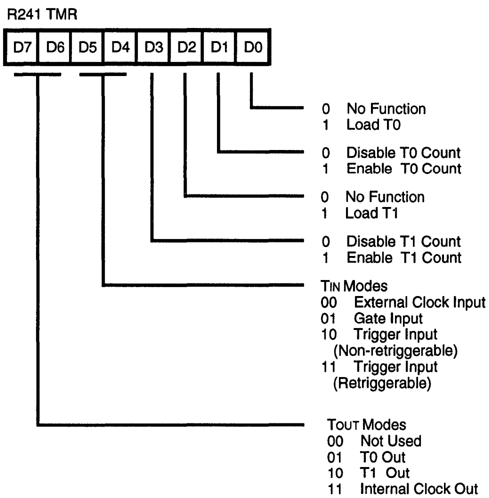

Figure 23. Timer Mode Register (F1H: Read/Write)

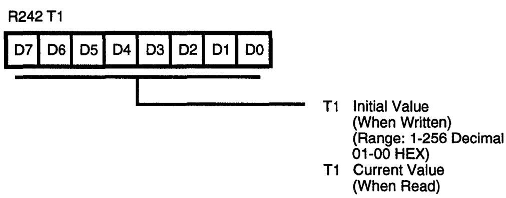

Figure 24. Counter/Timer 1 Register (F2H: Read/Write)

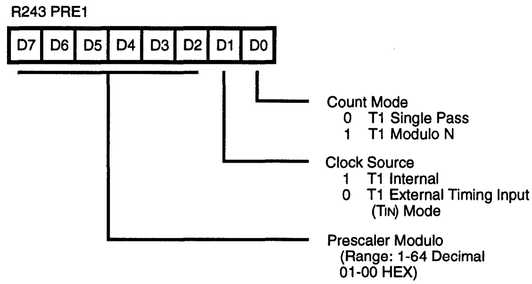

Figure 25. Prescaler 1 Register (F3H: Write Only)

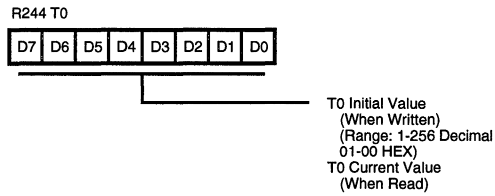

Figure 26. Counter/Timer 0 Register (F4H: Read/Write)

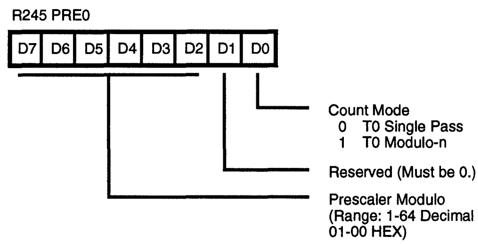

Figure 27. Prescaler 0 Register (F5H: Write Only)

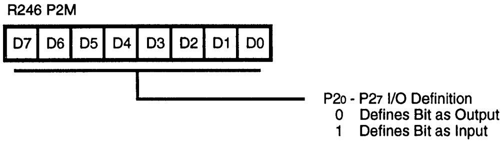

Figure 28. Port 2 Mode Register (F6H: Write Only)

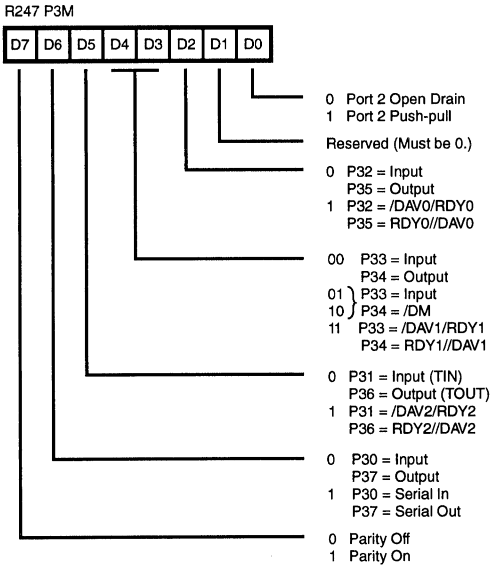

Figure 29. Port 3 Mode Register (F7H: Write Only)

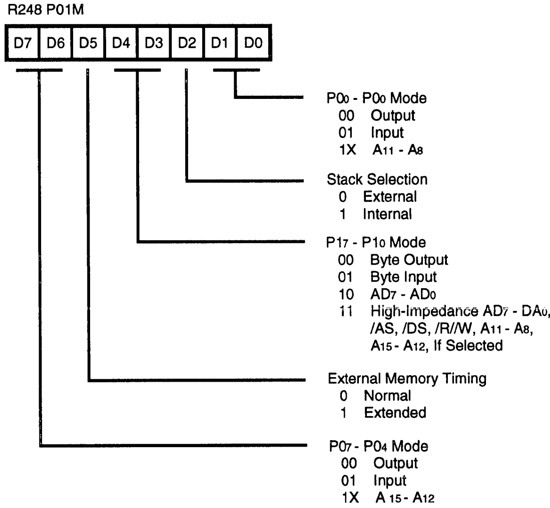

Figure 30. Port 0 and 1 Mode Register (F8H: Write Only)

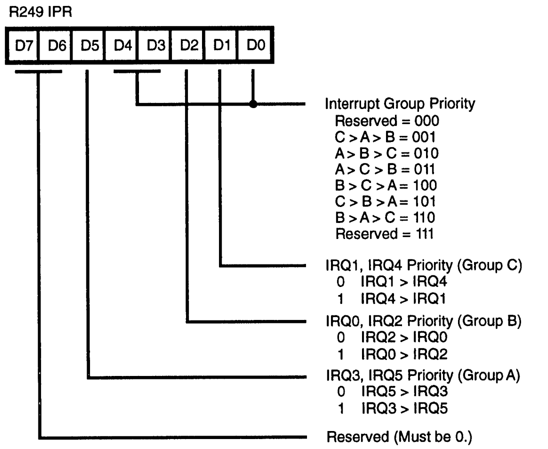

Figure 31. Interrupt Priority Register (F9H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

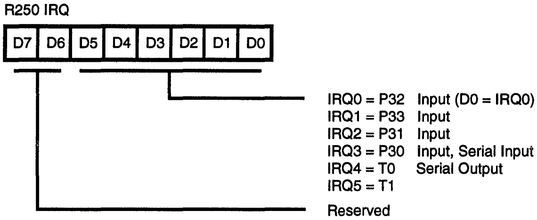

Figure 32. Interrupt Request Register (FAH: Read/Write)

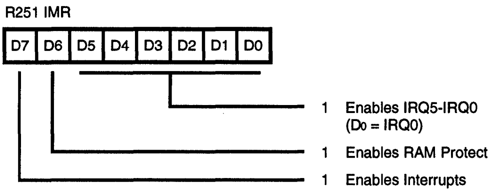

Figure 33. Interrupt Mask Register (FBH: Read/Write)

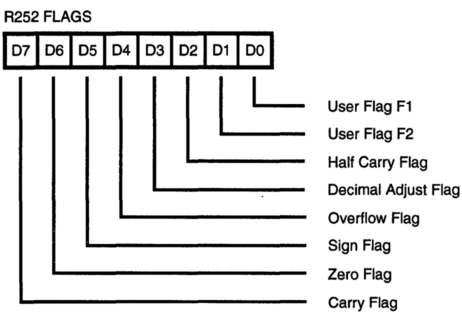

Figure 34. Flag Register (FCH: Read/Write)

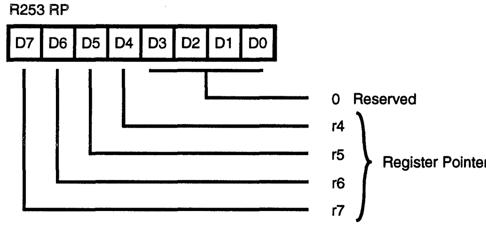

Figure 35. Register Pointer Register (FDH: Read/Write)

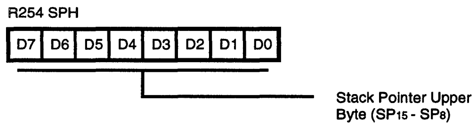

Figure 36. Stack Pointer Register (FEH: Read/Write)

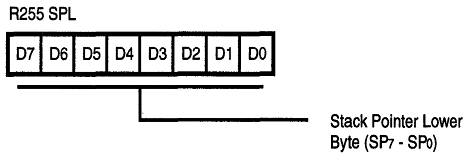

Figure 37. Stack Pointer Register (FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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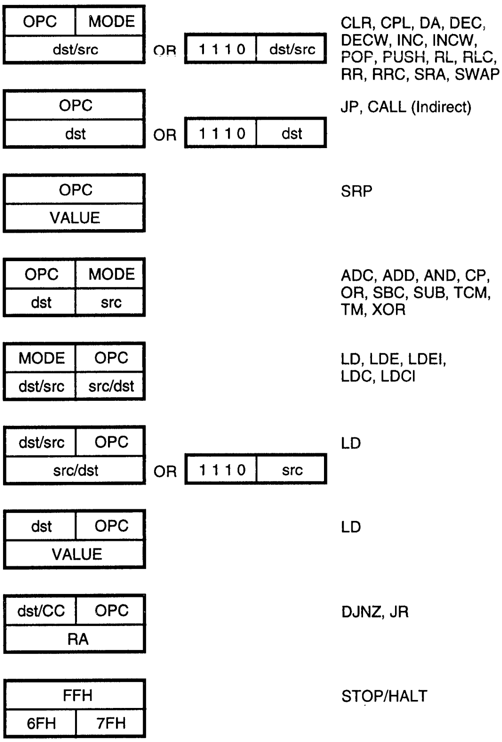
CONDITION CODES

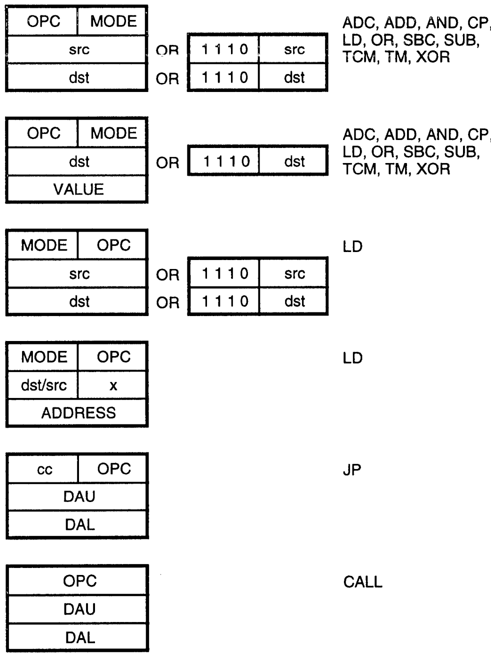
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

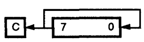
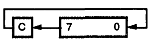
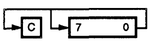
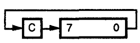
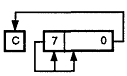
dst (7)

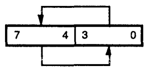
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	1 - - - - -
SUB dst, src dst←dst←src	†	2[ ]	[[[[1 [
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

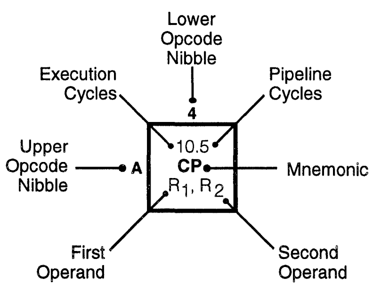
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

4

OPCODE MAP

Lower Nibble (Hex) (columns) / **Upper Nibble (Hex)** (rows)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r2, Irr1	18.0 **LDCI** Ir2, Irr1	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1



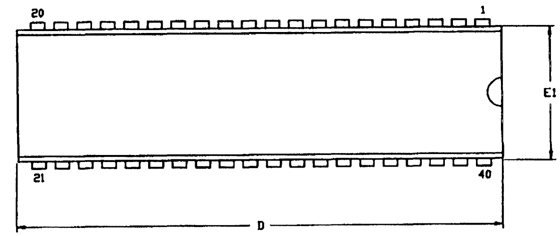
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

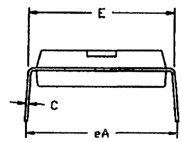
Sequence:
Opcode, First Operand,
Second Operand

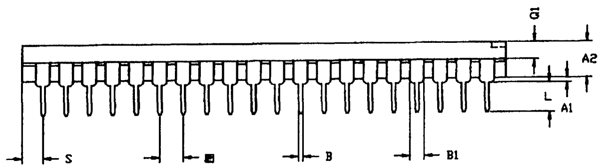
Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGING INFORMATION



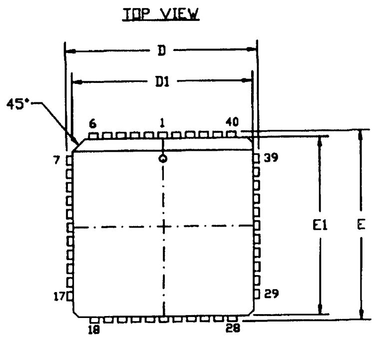


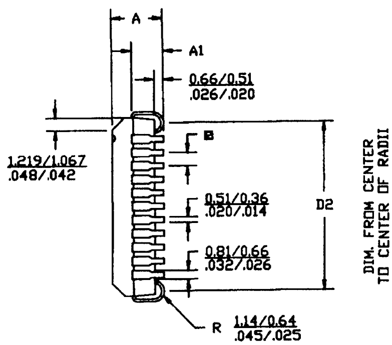


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
▣	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



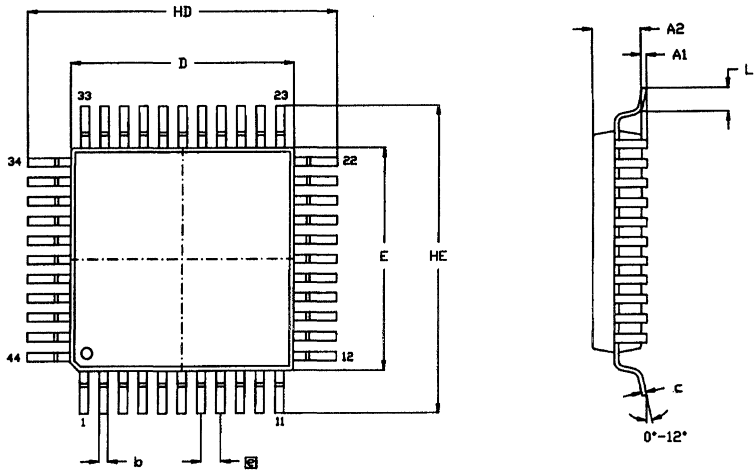


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
▣	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

PACKAGING INFORMATION



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C11

12 MHz

40-pin DIP	44-pin PLCC	44-pin QFP
Z86C1112PSC	Z86C1112VSC	Z86C1112FSC
Z86C1112PEC	Z86C1112VEC	Z86C1112FEC

16 MHz

40-pin DIP	44-pin PLCC	44-pin QFP
Z86C1116PSC	Z86C1116VSC	Z86C1116FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Temperature
S = 0°C to + 70°C
E = -40°C to 105°C

Speed
12 = 12 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:

Z 86C11 12 P S C is a Z86C11, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86C11 — Product Number
- Z — Zilog Prefix

4

Introduction I

Z86C07 Z8® CMOS
8-Bit Microcontroller 1

Z86C08 Z8® CMOS
8-Bit Microcontroller 2

Z86E08 Z8® CMOS 8-Bit
OTP Microcontroller 3

Z86C11 Z8® CMOS
Microcontroller 4

Z86C12 Z8® CMOS
In-Circuit Emulator MCU 5

Z86C21 Z8® CMOS
8K ROM Microcontroller 6

Z86C12

Z8® CMOS IN-CIRCUIT EMULATOR

FEATURES

- 8-bit CMOS Microcontroller Emulator
- 84-Pin PGA Package
- 4.5 to 5.5 Volt Operating Range
- Low Power Consumption - 275 mW (max)
- Average Instruction Execution Time of 1 µs
- Fast Instruction Pointer - 0.6 µs @ 16 MHz
- Two Standby Modes - STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Six Memory Emulation Modes
- 256 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupt from Eight Different Sources
- Clock Speed 16 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.

GENERAL DESCRIPTION

The Z86C12 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, easy hardware/software system expansion, a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C12 provides 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 General Purpose Registers.

To unburden the program from coping with real-time tasks such as counting/timing and serial data communication, the Z86C12 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (Figure 1. Functional Block Diagram).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

5

GENERAL DESCRIPTION (Continued)

The Z86C12 In-Circuit Emulator development device allows users to prototype a system with an actual hardware device and to develop the code. This code is eventually mask-programmed into the on-chip ROM for most of the Z86CXX devices. Development devices are also useful in emulator applications where the final system configuration, memory configuration, I/O, interrupt inputs, etc., are unknown. The Z86C12 development device is identical to its equivalent Z86C21 microcontroller with the following exceptions:

- No internal ROM is provided, so that code is developed in off-chip memory. Five size inputs configure the memory boundaries.
- The normally internal ROM address and data lines are buffered and brought out to external pins to interface with the external memory.
- Control lines (/MAS and /DAS) are added to interface with external program memory.
- The Timing and Control, I/O ports, and clock pins on the Z86C12 are identical in function to those on the Z86C21.

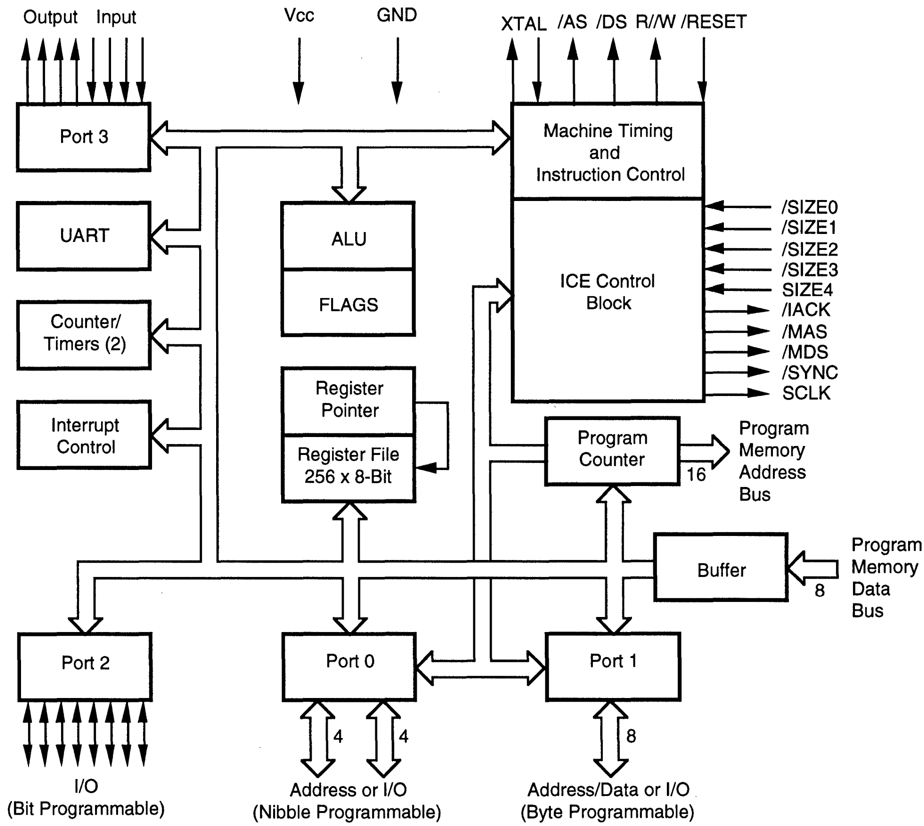


Figure 1. Functional Block Diagram

PIN DESCRIPTION

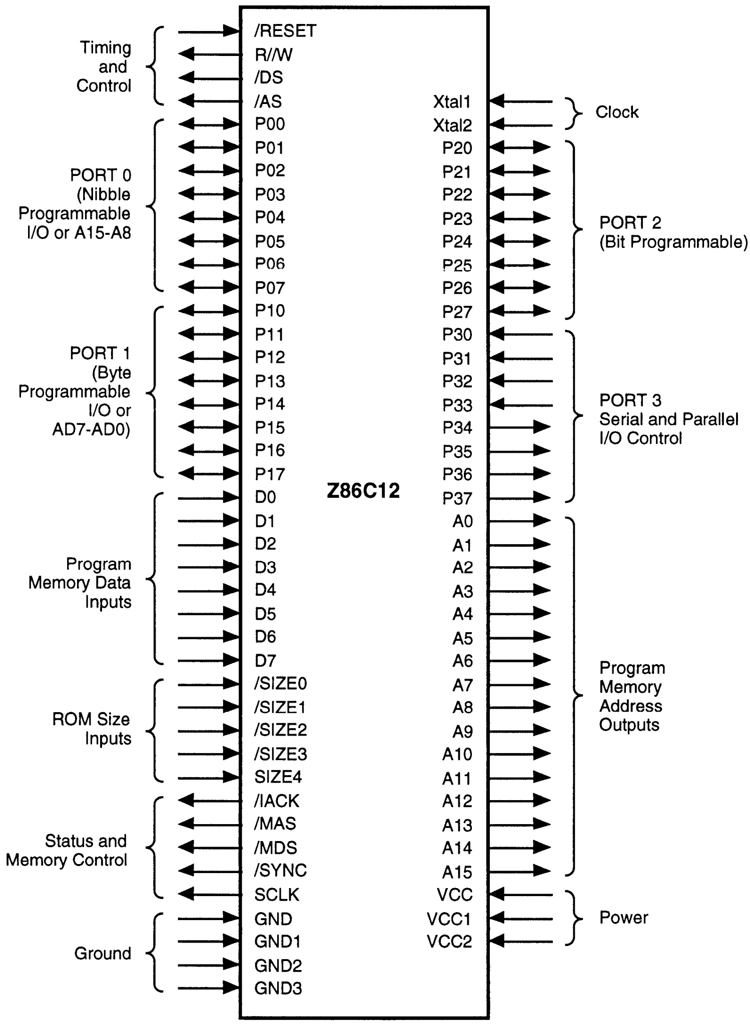


Figure 2. Z86C12 Pin Functions

5

PIN DESCRIPTION (Continued)

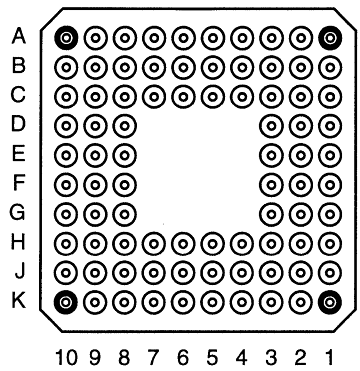


Figure 3. 84-Pin PGA Pin Configuration

Table 1. 84-Pin PGA Pin Assignments

Name	Pin	Name	Pin	Name	Pin	Name	Pin
/AS	B2	A5	K6	P02	D2	P27	C7
/DS	C4	A6	J6	P03	D1	P30	B4
/MAS	E1	A7	K8	P04	E3	P31	B7
/MDS	G3	A8	J5	P05	G1	P32	C2
/RESET	B3	A9	K4	P06	H1	P33	D9
/SIZE0	A3	D0	H3	P07	J1	P34	E10
/SIZE1	C5	D1	K2	P10	G8	P35	B1
/SIZE2	A6	D2	J3	P11	G9	P36	A7
/SIZE3	C6	D3	K3	P12	G10	P37	A5
/SYNC	F1	D4	H8	P13	F8	R//W	A1
A0	J9	D5	J10	P14	D10	SCLK	G2
A1	H7	D6	H9	P15	C10	SIZE4	F10
A10	J4	D7	H10	P16	B10	V_{CC}	A4
A11	H4	/IACK	F2	P17	E9	V_{CC1}	B6
A12	K9	N/C	J2	P20	C9	V_{CC2}	F9
A13	K7	N/C	C3	P21	A10	GND	F3
A14	K5	N/C	D8	P22	B9	GND1	E2
A15	H5	N/C	H2	P23	C8	GND2	H6
A2	K10	N/C	K1	P24	A9	GND3	E8
A3	J8	P00	C1	P25	B8	XTAL1	B5
A4	J7	P01	D3	P26	A8	XTAL2	A2

PIN FUNCTIONS

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external program. Program or data memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, write Low). The Read/Write signal is Low when the Z86C12 is writing to external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C12 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset will occur. On the fifth clock after the /RESET is detected, an internal RESET signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time is held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

D7-D0 *Data Bus* (inputs, TTL compatible). These eight lines provide the input data bus to access external memory, which is emulating the on-chip ROM. During read cycles in the internal memory space the data on these lines is latched in just prior to the rise of the /MDS data strobe.

A15-A0 *Address Bus* (outputs TTL compatible). During T1 these lines output the current memory address. All addresses, whether internal or external, are output.

/MAS *Memory Address Strobe* (output, TTL compatible). This line is active during every T1 cycle. The rising edge of this signal is used to latch the current memory address on the lines A15 - A0. This line is always valid. It is not tri-stated when /AS is tri-stated.

/MDS *Memory Data Strobe* (output, TTL compatible). This is a timing signal used to enable the external memory to emulate the on-chip ROM. It is active only during accesses to the on-chip ROM memory space as selected by the configuration of the SIZEn pins.

/SCLK *System Clock* (output, TTL compatible). This line is the internal system clock.

/SYNC *Sync Signal* (output, TTL compatible). This signal indicates the last clock cycle of the currently executing instruction.

/IACK *Interrupt Acknowledge* (output, TTL compatible). This output, when Low, indicates that the Z86C12 is an interrupt cycle.

/SIZE0, /SIZE1, /SIZE2, /SIZE3, /SIZE4 (Inputs, TTL compatible). The SIZEn lines control the emulation mode of the Z86C12. The functions are defined as shown in Table 2. The Z86C12 need not be RESET when the state of these lines is changed.

Table 2. Memory Size Configuration

/SIZE4	/SIZE3	/SIZE2	/SIZE1	/SIZE0	Memory
0	1	1	1	1	ROMless
0	1	1	1	0	2K ROM
0	1	1	0	1	4K ROM
0	1	0	1	1	8K ROM
0	0	1	1	1	16K ROM
1	1	1	1	1	32K ROM

Note: The SIZE pins can be configured to make the memory control signals (/MAS, /MDS, R/W, /AS, and /DS) look like the Z86C91 ROMless device. However, on power-up or reset, Ports 0 and 1 are configured as inputs, rather than A15-A8 and AD7-AD0, respectively. This means that if ROMless mode is desired, the device is powered up in ROM mode, and executes a few instructions through the Z86C12 address/data ports. These instructions reconfigure the ports as required, and then the SIZE inputs can be set to ROMless mode - but without a RESET.

PIN FUNCTIONS (Continued)

I/O Ports

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control. For the ROMless option, Port 0 appears as A15-A8 Address lines after reset.

For external memory references, Port 0 provides address bit A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O, while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 4).

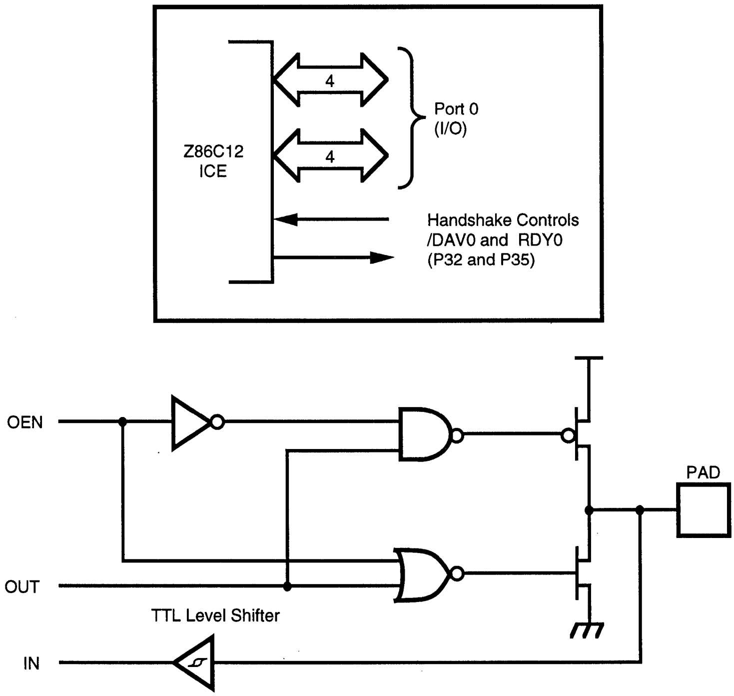


Figure 4. Port 0 Configuration

Port 1 (P10-P17). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For the Z86C12, these eight I/O lines can be programmed as Input or Output lines or the port can be configured, under software control, as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines P33 and P34 are used as the handshake controls RDY1 and /DAV1, respectively.

Memory locations greater than 8192 are referenced through Port 1. To interface external memory, Port 1 is programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS and R//W, allowing the Z86C12 to share common resource in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 5).

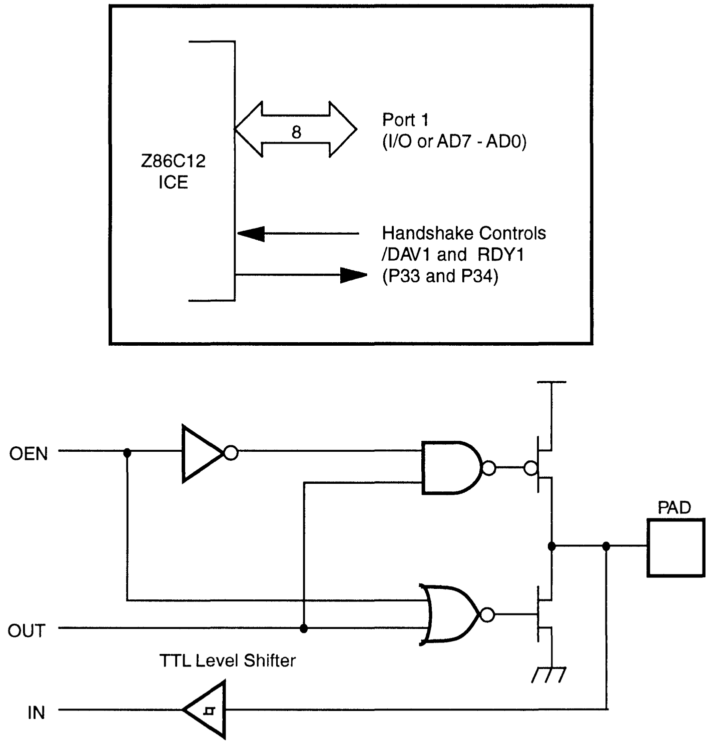


Figure 5. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 6).

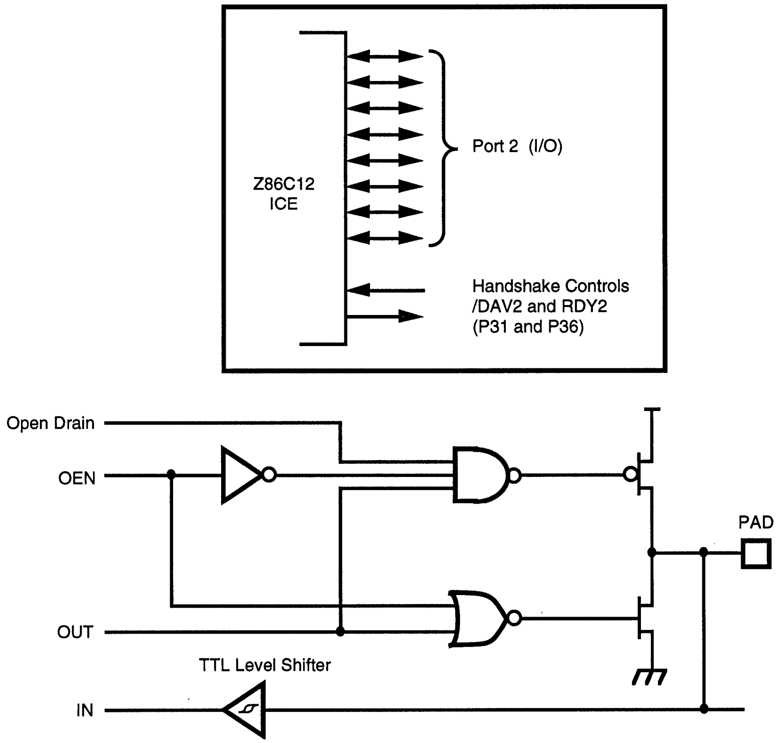


Figure 6. Port 2 Configuration

Port 3 (P30-P37). Port 3 is an 8-bit, CMOS compatible four fixed input and four fixed output port. These eight I/O lines have four-fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 7 and Table 3).

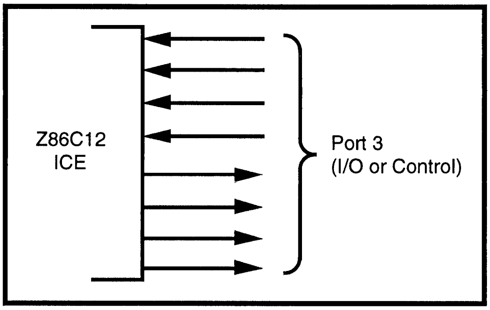


Figure 7. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select (/DM).

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

5

PIN FUNCTIONS (Continued)

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z86C12 automatically adds a start bit and two stop bits to transmitted data (Figure 8). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

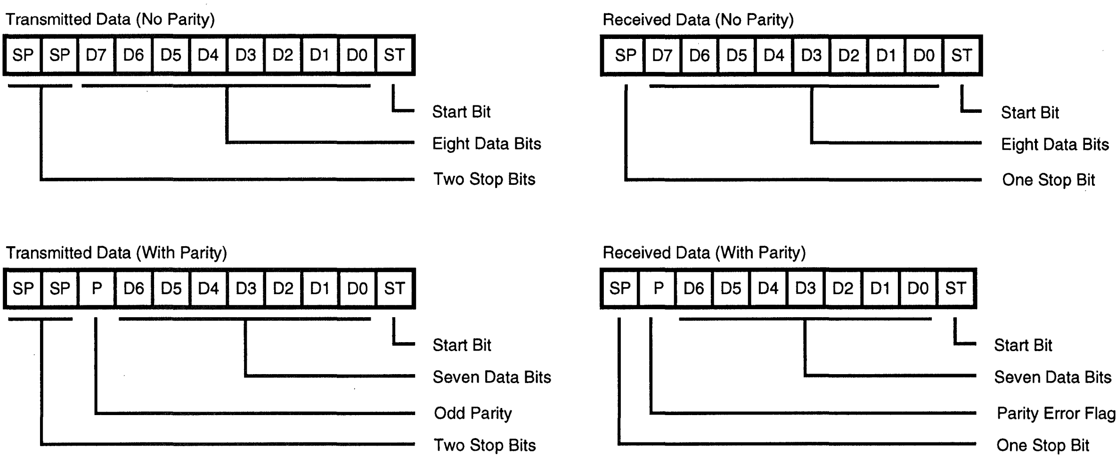


Figure 8. Serial Data Formats

PROGRAMMING

Address Space

Program Memory. The Z86C12 can address up to 64 Kbytes of external program memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. The five SIZEn inputs dictate the amount of ROM being emulated, and for an 8K ROM the input is '01011'. Respectively, 000C to 8191 is the memory map for the emulated ROM, and 8192 to 65535 is the remaining program memory for which the Z86C12 executes external memory fetches.

Data Memory (/DM). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34, is used to distinguish between data and program memory space (Figure 10). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory. The lower unaddressable part of the data memory is in fact addressable with the Z86C12 /MDS line (as /DS is not active for internal ROM reads), but there should be no need for this.

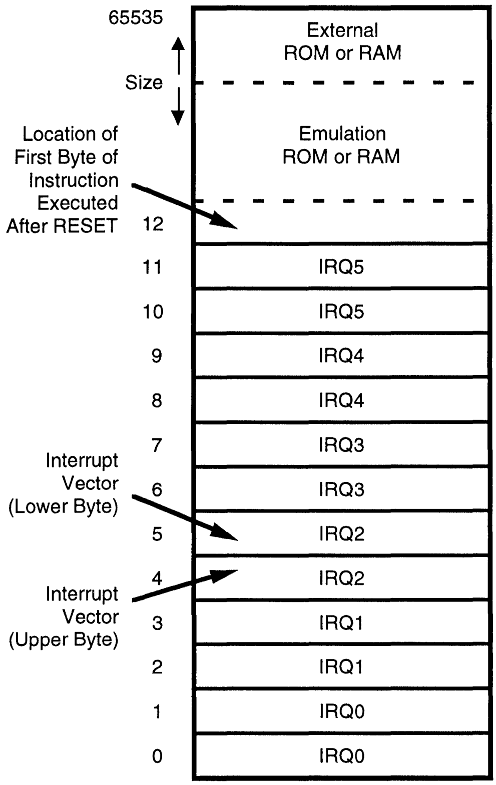


Figure 9. Program Memory Configuration

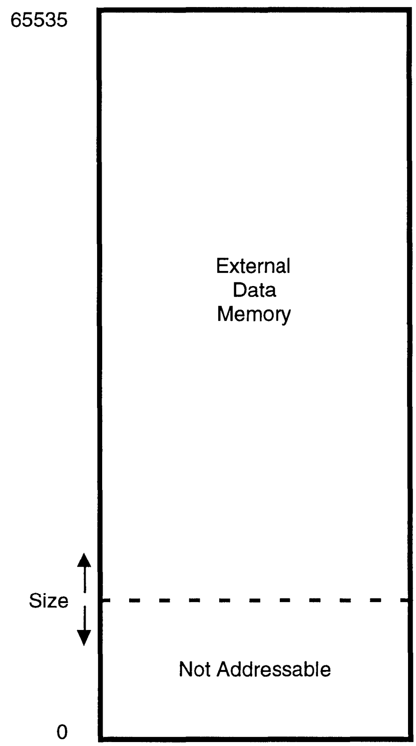


Figure 10. Data Memory Configuration

5

PROGRAMMING (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 11). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C12 also allows short 4-bit register addressing using the Register Pointer (Figure 12). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

LOCATION		IDENTIFIERS
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
	Not Implemented	
239 4	General-Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Port1	P1
0	Port 0	P0

Figure 11. Register File

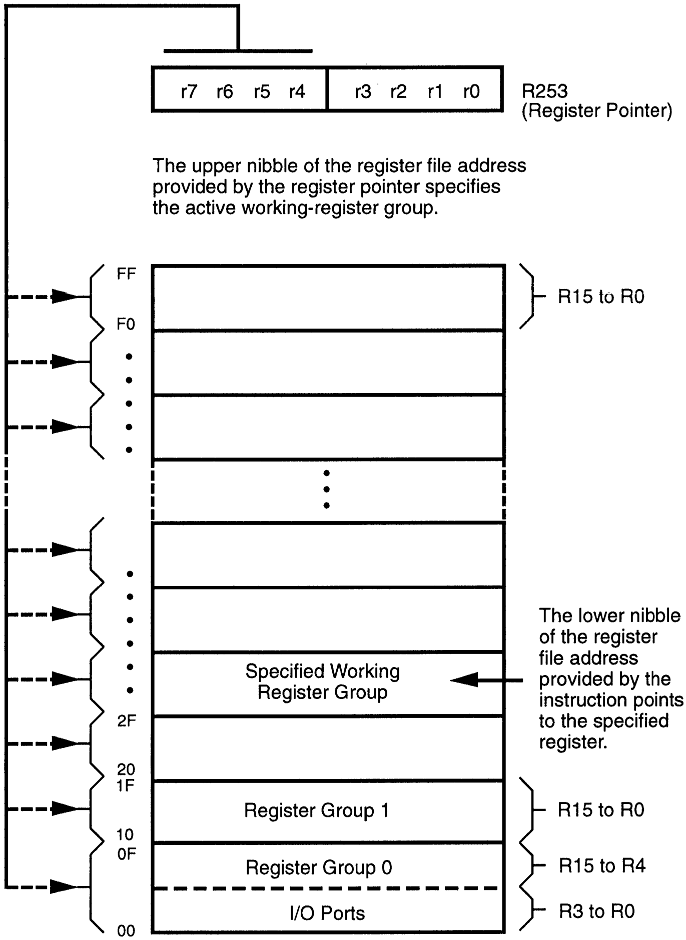


Figure 12. Register Pointer

Stack. The Z86C12 has a 16-bit Stack Pointer (R254-R255) used for an external stack that resides anywhere in the data memory for the ROMless mode, but only from SIZEn to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH-Bit 8-15) can be use as a general purpose register when using internal stack only.

5

FUNCTIONAL DESCRIPTION

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; the T0 prescaler is driven by the internal clock only (Figure 13).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, is read at any time without disturbing its value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock is output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

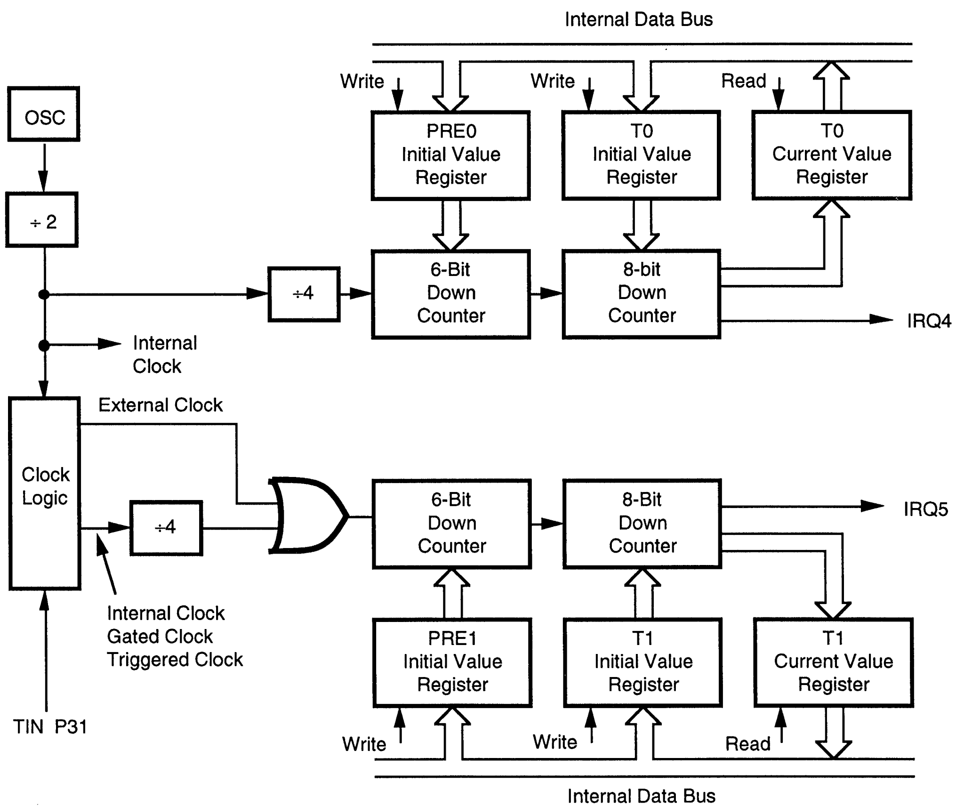


Figure 13. Counter/Timers Block Diagram

Interrupts. The Z86C12 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in serial out, one in serial in, and two in the counter/timers (Figure 14). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C12 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request is valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point. This corresponds to the 63rd TpC cycle following the external interrupt sample point.

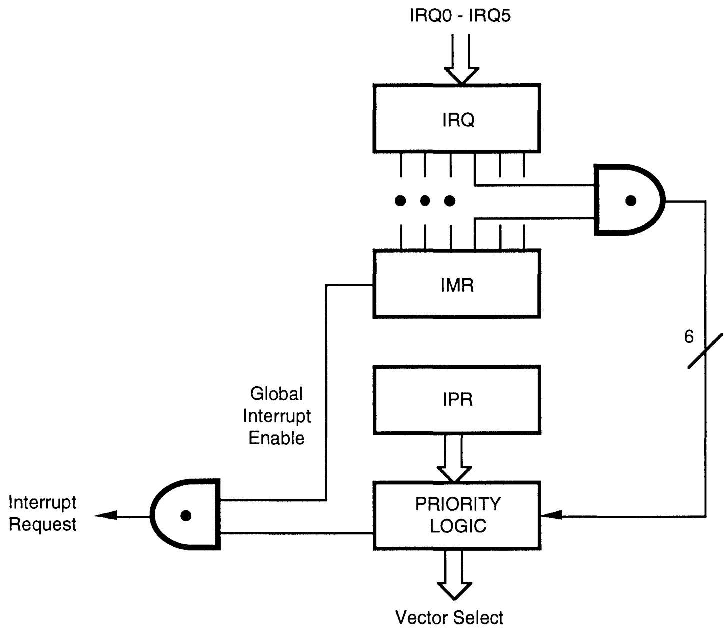


Figure 14. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C12 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground (Figure 15).

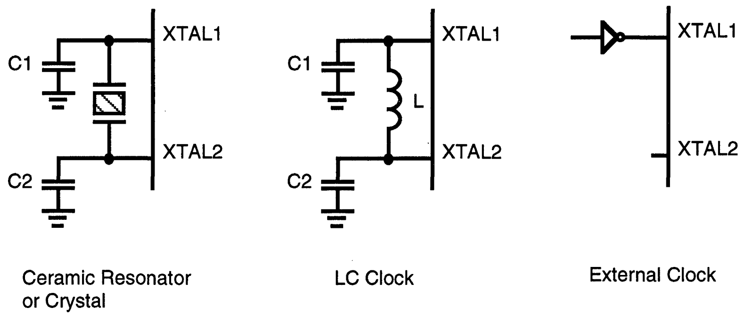


Figure 15. Oscillator Configuration

HALT. This turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less (typical). The STOP Mode is terminated by a reset, which causes the processor to restart the application program at address 000C (Hex).

To enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate sleep instruction. i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

Instruction Cycle Timing

Figures 16 and 17 show instruction cycle timing for instructions fetched from external memory.

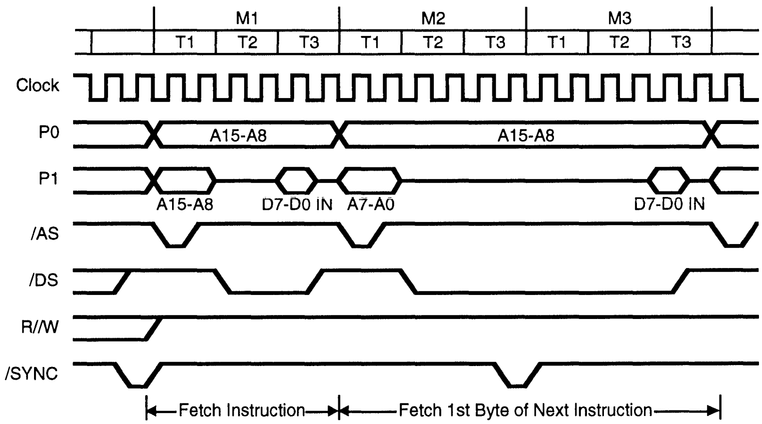


Figure 16. Instruction Cycle Timing (One-Byte Instructions)

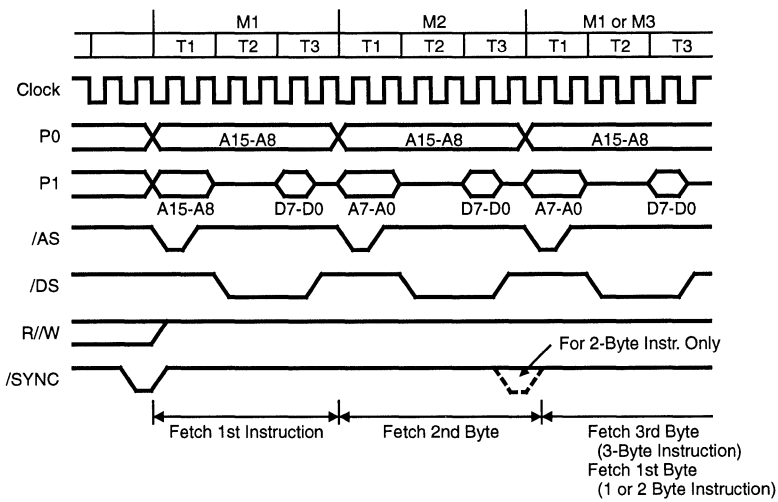


Figure 17. Instruction Cycle Timing (Two- and Three-Byte Instructions)

5

FUNCTIONAL DESCRIPTION (Continued)

The addresses, Address Strobe (/AS) and Read Write (R//W) are output at the beginning of each machine cycle (Mn). The addresses output through Port 0 (if used) remain stable throughout the machine cycle. Addresses output through Port 1 remain valid only during MnT1. The addresses are guaranteed valid at the rising edge of /AS, which is used to latch the Port 1 output. Port 1 is placed in an input mode at the end of MnT1. The Data Strobe is output during MnT2 allowing data to be placed on the Port 1 bus. The Z8 accepts the data during MnT3 and /DS is terminated.

Instruction synchronization pulse /SYNC is output one clock pulse period prior to the beginning of an opcode fetch machine cycle (M1). This output is directly available on the 64-pin versions of our Z8® Family; whereas, on the 40-pin versions, the Data Strobe pin outputs /SYNC only if external memory is not used.

Note that all instruction fetch cycles have the same machine timing regardless of whether the memory is internal or not. If configured for external memory, and internal memory is referenced, the addresses are still output through Ports 0 and 1; /DS and R//W are inactive. If configured for internal memory only, Ports 0 and 1 are used for I/O, /DS outputs, /SYNC; R//W is inactive.

The exception to the instruction fetch timing is during the opcode fetch of an instruction following the fetch of a one-byte instruction. One-byte instructions require two machine cycles to execute. The pipelining causes the following opcode fetch to begin one machine cycle early.

External Memory or I/O Timing

When external memory is addressed, Ports 0 and 1 are configured to output the required number of address bits. Port 1 is used as a multiplexed address/data bus for AD7-AD0 and Port 0 outputs address bits A15-A8. The timing relationships for addressing external memory and I/O are illustrated in Figures 18, 19, 20 and 21. The main difference between these figures is that Figures 20 and 21 contain an added timing cycle (Tx) that extends external memory timing to allow for slower memory.

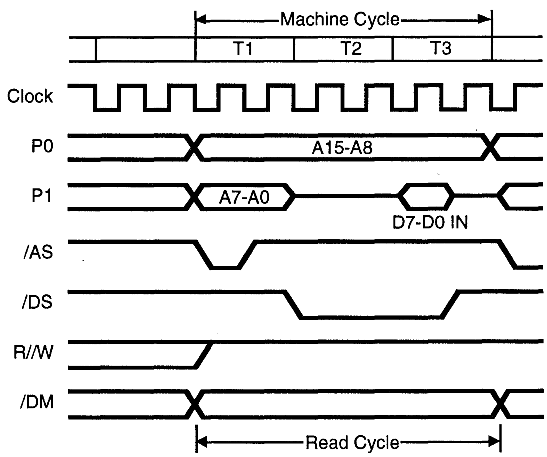


Figure 18. External Instruction Fetch, I/O or Memory Read Cycle

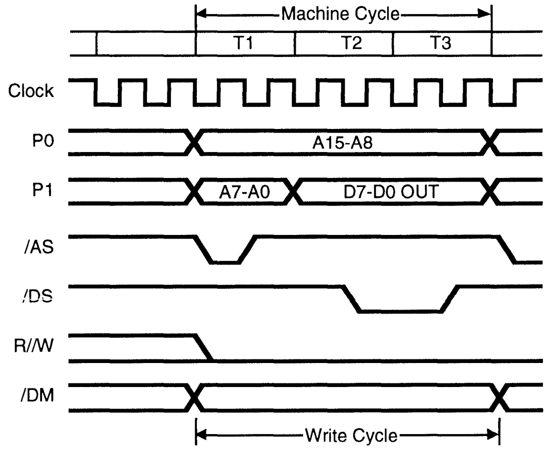


Figure 19. External I/O or Memory Write Cycle

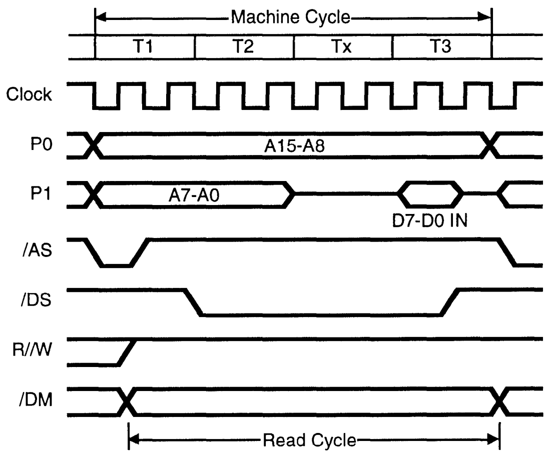


Figure 20. Extended External Instruction Fetch, I/O or Memory Read Cycle

FUNCTIONAL DESCRIPTION (Continued)

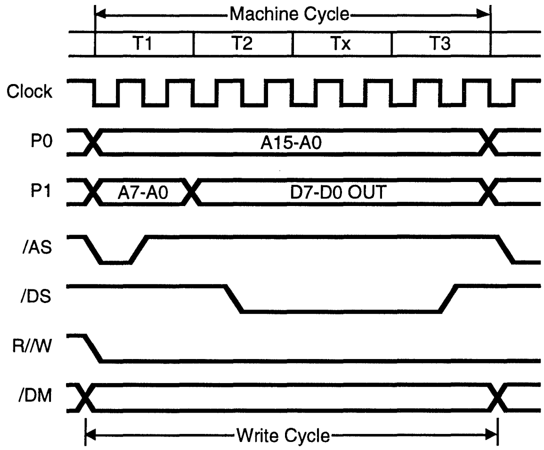


Figure 21. Extended External I/O or Memory Write Cycle

Address bits A15-A0 are valid on Ports 0 and 1 at the trailing edge of /AS for both the read and write memory cycles. Because Port 0 is not multiplexed, address bits A15-A8, if used, are present all through the read/write memory cycle.

During the read cycle, the input data must be valid on Port 1 at the trailing edge of the Data Strobe output (/DS). The Data Memory Select output (/DM) is used to select external data memory or external program memory. If selected, /DM is active during the execution of certain instructions.

During the write cycle, the address outputs follow the same timing relationships as for the read cycle. However, the output data is valid for the entire period /DS is active, and R//W is active (Low) during the entire write cycle.

Interrupt requests are sampled before each instruction fetch cycle (Figure 22). First, external interrupt requests are sampled four clock periods prior to the active /AS pulse that corresponds to an instruction fetch cycle. Then, internal interrupt requests are samples one clock period preceding /AS.

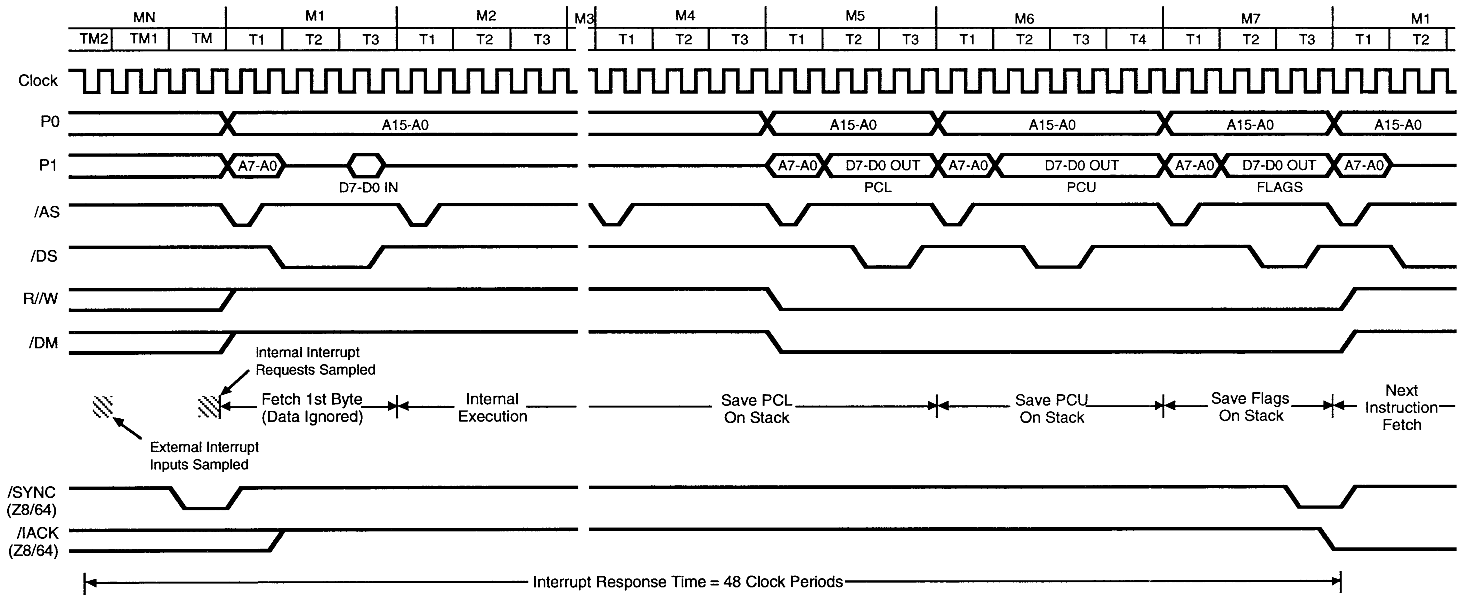


Figure 22. Interrupt Cycle Timing

FUNCTIONAL DESCRIPTION (Continued)

If an interrupt request is set, the Z8 spends seven machine cycles (44 clock periods) resolving interrupt priorities, selecting the proper interrupt vector, and saving the program counter and flags on the stack. Although Figure 13 illustrates the timing for an external stack, the same timing is used for an internal stack. The total interrupt response time (including the external interrupt sample time) for an external interrupt is 48 clock periods. The first instruction of the interrupt service routine is fetched at this time. When an interrupt request is detected in our 64-pin Z8® Family versions, /IACK is activated (Low) and remains active until the first instruction of the interrupt service routine is fetched.

Reset Timing

The internal logic is initialized during reset if the Reset input is held Low for at least 18 clock periods (Figure 23). During the time /RESET is Low, /AS is output at the internal clock rate, /DS is forced Low, R//W is inactive and Ports 0, 1 and 2 are placed in an input mode. /AS and /DS both Low is normally a mutually exclusive condition; therefore, the coincidence of /AS Low and /DS Low can be used as a reset condition for other devices. Zilog Z-Bus® peripherals take advantage of this reset condition.

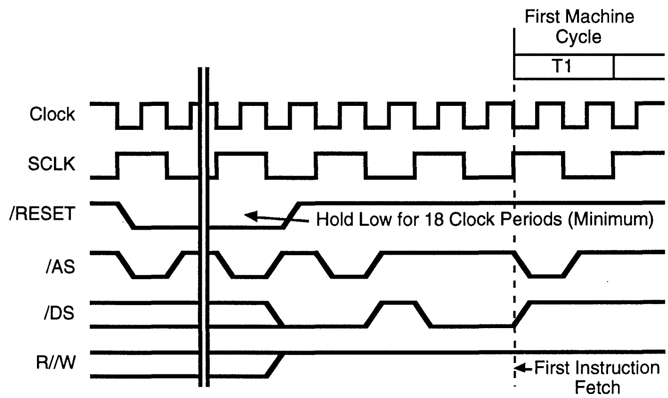


Figure 23. Reset Cycle Timing

Alternative Control Signal Uses

In addition to their uses in memory transfers, the control signals /AS, /DS and R//W can be used in the following interface applications:

/AS can be modified to provide the /RAS (Row Address Strobe) signal for dynamic memory interface. /RAS can be derived from the trailing edge of /DS to the trailing edge of /AS.

/DS has several alternative uses: as a /CAS (Column Address Strobe) for dynamic memory interface; as a Chip Enable for memory and other interface devices; as an Enable input for tri-state bus drivers/receivers for memory and interface devices.

R//W can be used as a Write input to memory interfaces, and as an Early Status output to switch the direction of tri-state bus drivers/receivers.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp**		C	

Notes:
* Voltages on all pins with respect to GND.
** See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 24).

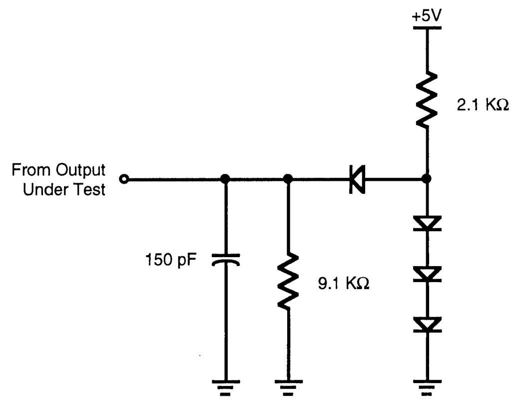


Figure 24. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to 70°C		T_A = –40°C to 105°C		Typical	Units	Conditions
		Min	Max	Min	Max	@ 25°C		
	Max Input Voltage		7		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –250 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.8	–0.03	0.8		V	
I_{IL}	Input Leakage	–1	1	–10	10		µA	0V V_{IN} +5.25V
I_{OL}	Output Leakage	–1	1	–10	10		µA	0V V_{IN} +5.25V
I_{IR}	Reset Input Current		–80		–50		µA	V_{CC} = +5.25V, V_{RL} = 0V
I_{CC}	Supply Current		50		50	25	mA	@ 12 MHz
			60		60	35	mA	@ 16 MHz
I_{CC1}	Standby Current		15		15	5	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 12 MHz
			20		20	10	mA	HALT Mode V_{IN} = 0V, V_{CC}@ 16 MHz
I_{CC2}	Standby Current		10		10	5	µA	STOP Mode V_{IN} = 0V, V_{CC}@ 12 MHz
			10		10	5	µA	STOP Mode V_{IN} = 0V, V_{CC}@ 16 MHz

Notes:
I_{CC2} requires loading TMR (%F1H) with any value prior to STOP execution.
Use this sequence:

```
LD TMR,#00
NOP
STOP
```

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

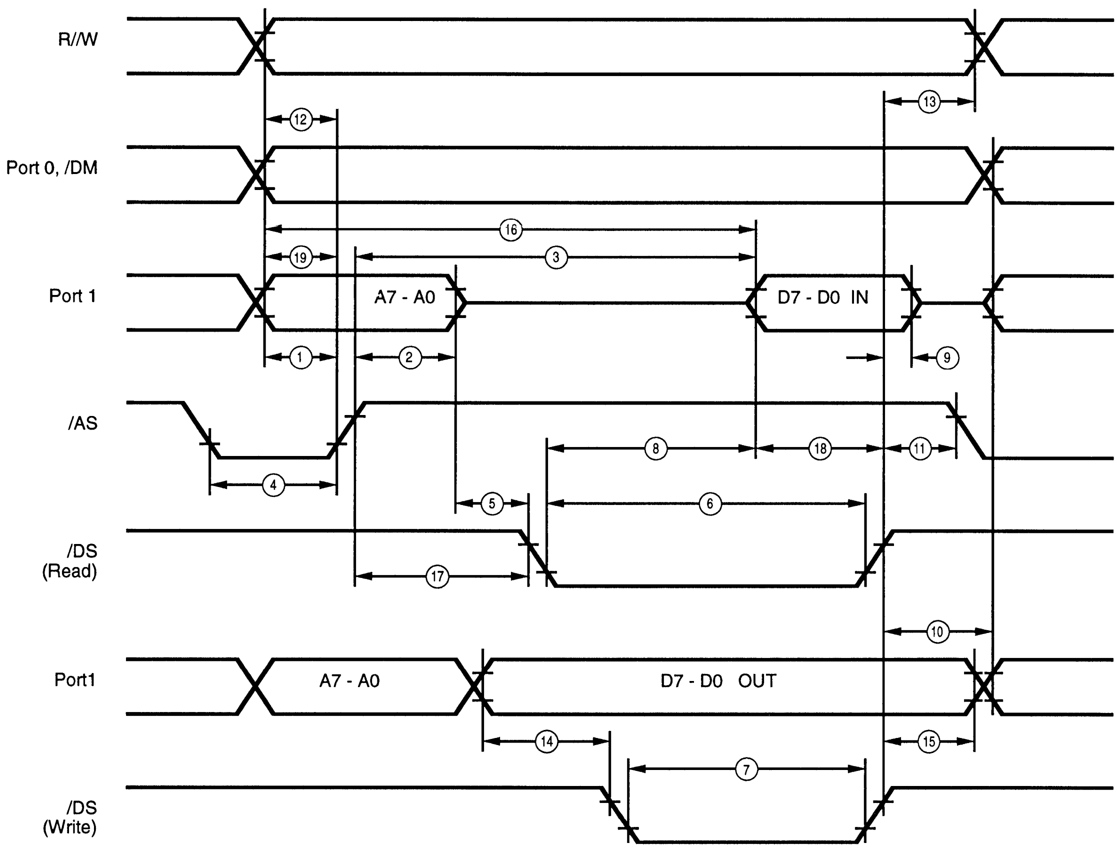


Figure 25. External I/O or Memory Read or Write Timing

AC CHARACTERISTICS
External I/O or Memory Read and Write Timing Table

			T_A = 0°C to 70°C				T_A = –40°C to 105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		45		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	35		30		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		65		45		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		50		30		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
Standard Test Load
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC – 3.25
3	TdAS(DR)	2.83TpC + 6.14
4	TwAS	0.66TpC – 1.65
6	TwDSR	2.33TpC – 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC – 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC – 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC – 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC – 19
16	TdA(DR)	4TpC – 20
17	TdAS(DS)	0.91TpC – 10.7
18	TsDI(DS)	0.8TpC – 10
19	TdDM(AS)	0.9TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

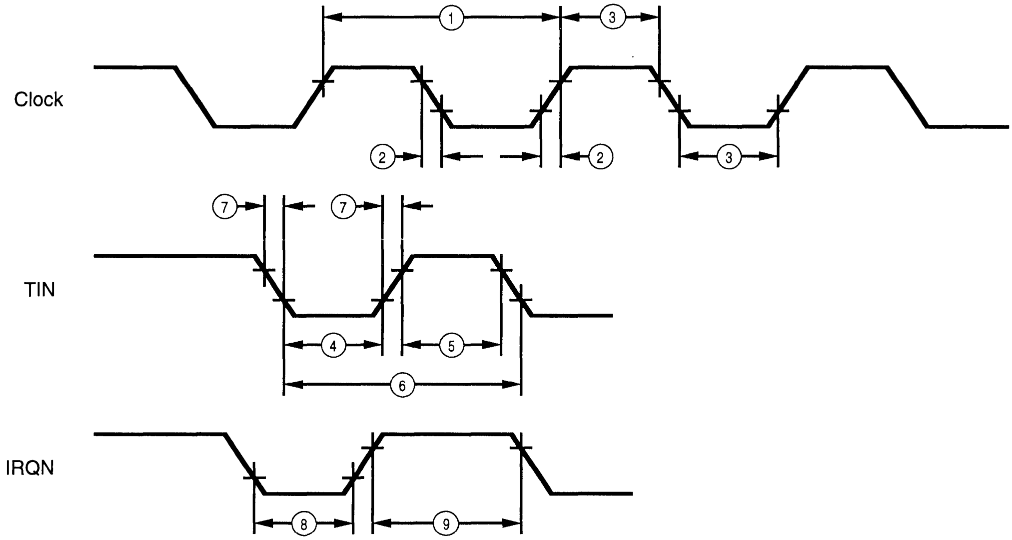


Figure 26. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

			T_A = 0°C to 70°C				T_A = –40°C to 105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	37		21		37		21		ns	[1]
4	TwTinL	Timer Input Low Width	70		50		70		50		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC		3TpC		3TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P31-P33).
[5] Interrupt request through Port 30.

5

AC CHARACTERISTICS
Handshake Timing Diagram

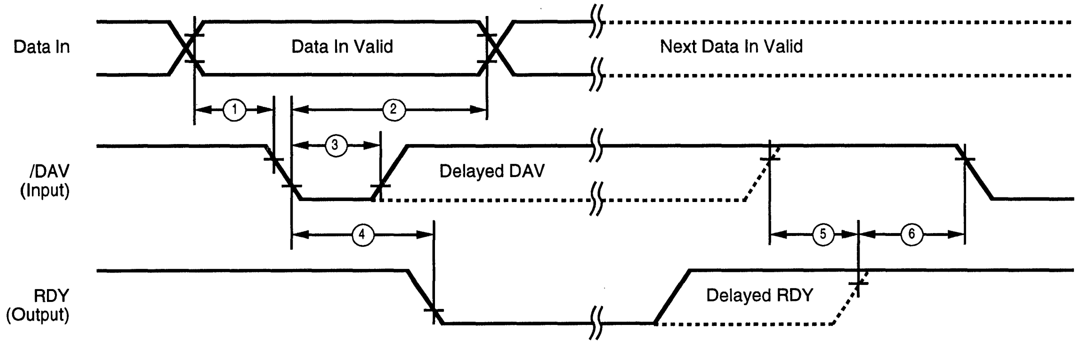


Figure 27. Input Handshake Timing

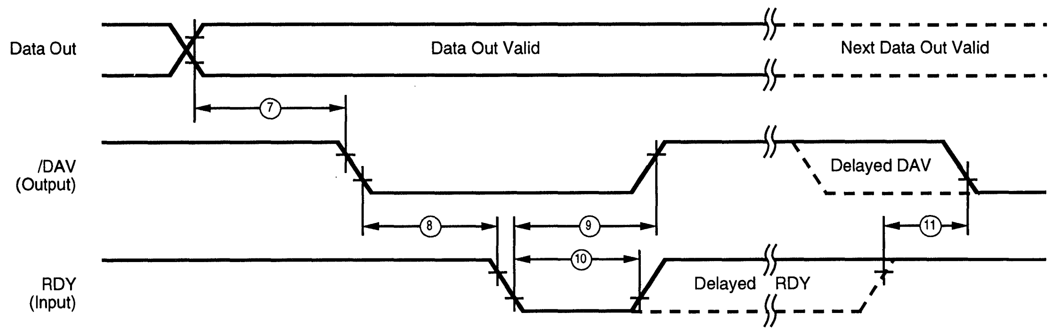


Figure 28. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

			T_A = 0°C to 70°C				T_A = −40°C to 105°C				
			12 MHz		16 MHz		12 MHz		16 MHz		Data
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		IN
3	TwDAV	Data Available Width	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110		110		110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

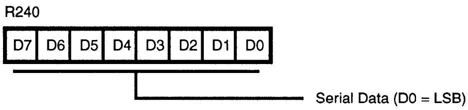


Figure 29. Serial I/O Register (F0H: Read/Write)

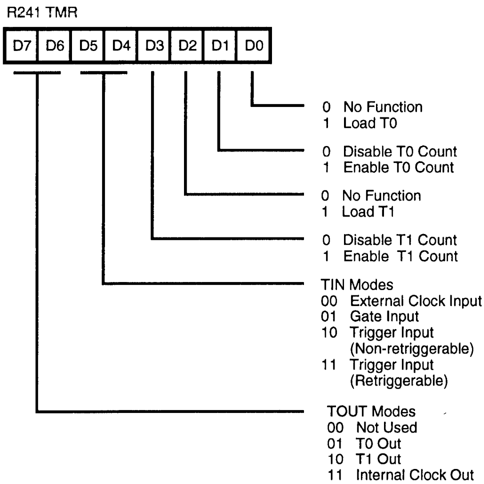


Figure 30. Timer Mode Register (F1H: Read/Write)

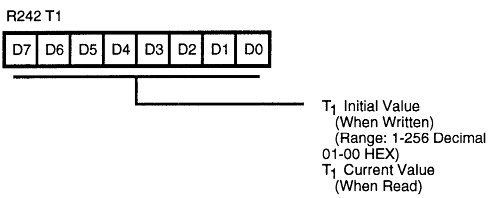


Figure 31. Counter/Timer 1 Register (F2H: Read/Write)

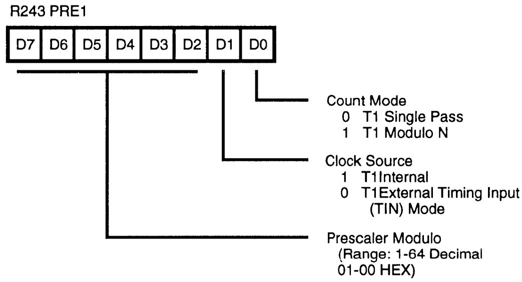


Figure 32. Prescaler 1 Register (F3H: Write Only)

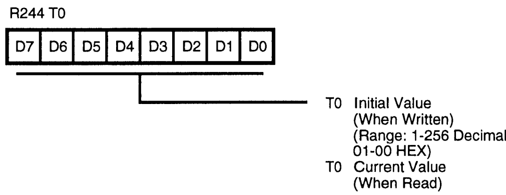


Figure 33. Counter/Timer 0 Register (F4H: Read/Write)

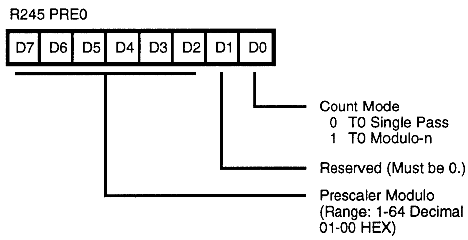


Figure 34. Prescaler 0 Register (F5H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

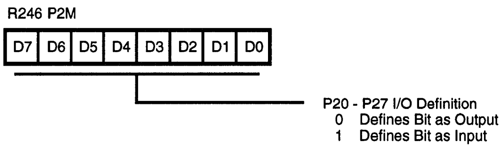


Figure 35. Port 2 Mode Register (F6H: Write Only)

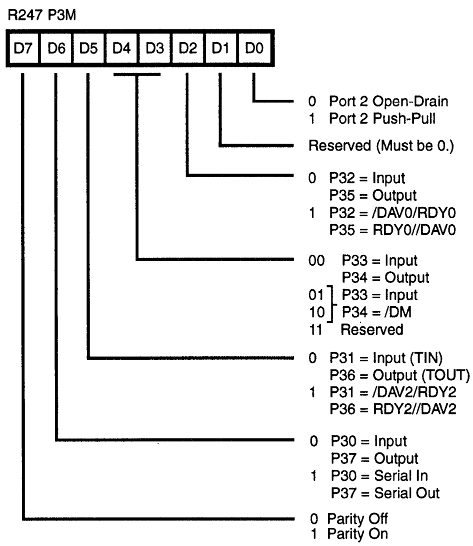


Figure 36. Port 3 Mode Register (F7H: Write Only)

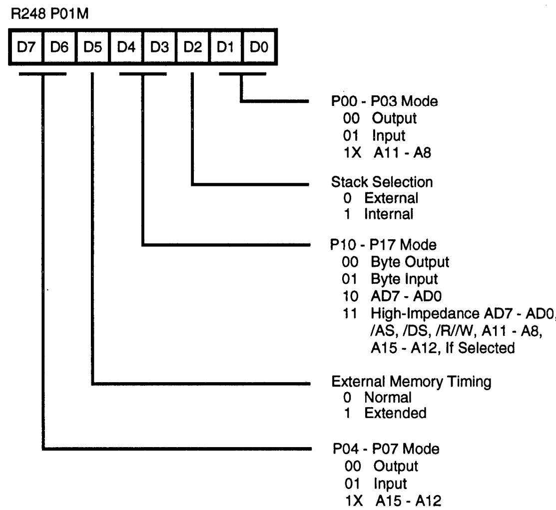


Figure 37. Ports 0 and 1 Mode Register (F8H: Write Only)

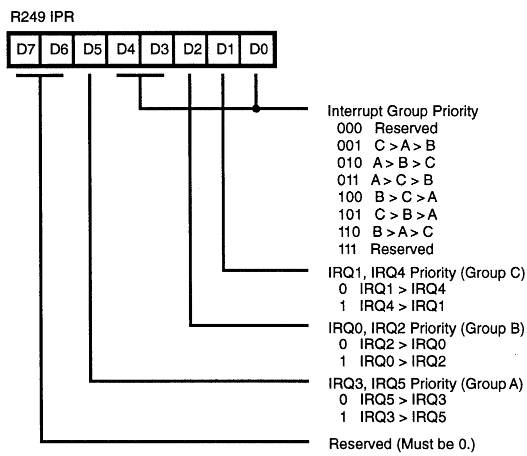


Figure 38. Interrupt Priority Register (F9H: Write Only)

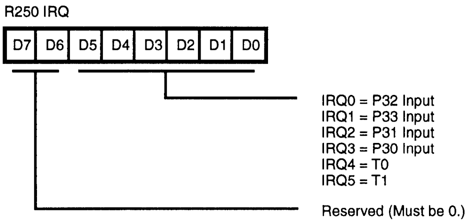


Figure 39. Interrupt Request Register (FAH: Read/Write)

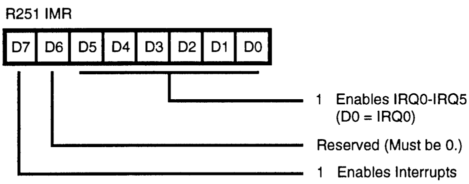


Figure 40. Interrupt Mask Register (FBH: Read/Write)

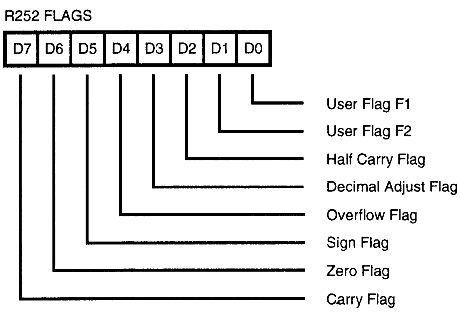


Figure 41. Flag Register (FCH: Read/Write)

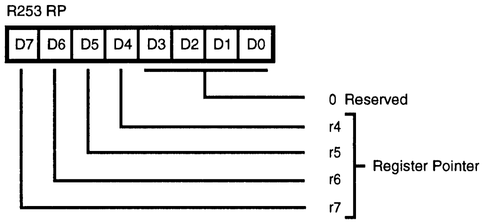


Figure 42. Register Pointer Register (FDH: Read/Write)

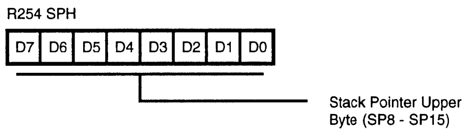


Figure 43. Stack Pointer Register (FEH: Read/Write)

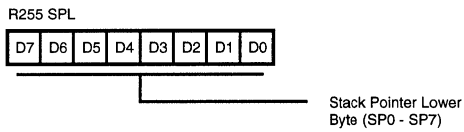


Figure 44. Stack Pointer Register (FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

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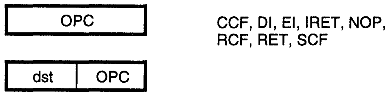
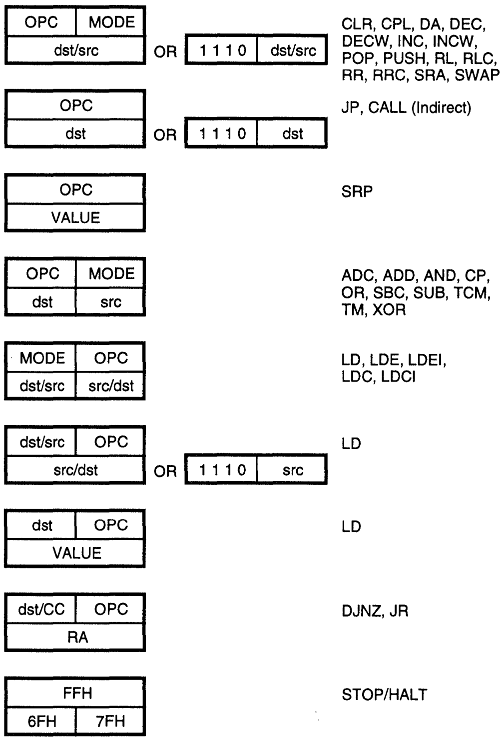
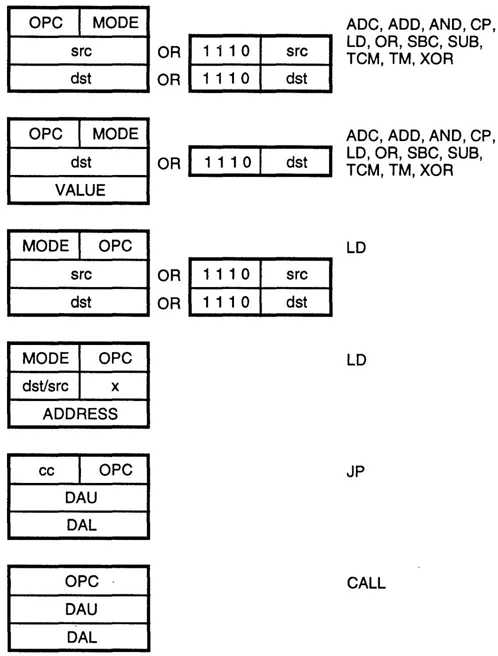
INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

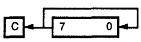
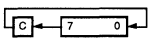
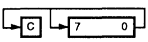
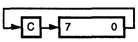
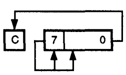
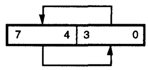
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP − 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - - -
CCF C←NOT C			EF	* - - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst − src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst − 1	R IR		00 01	- * * * - -
DECW dst dst←dst − 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - - -
DJNZr, dst r←r − 1 if r ≠ 0 PC←PC + dst Range: +127, −128	RA		rA r = 0 - F	- - - - - - -
EI IMR(7)←1			9F	- - - - - - -
HALT			7F	- - - - - - -
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	- - - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, −128	RA		cB c = 0 – F	- - - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - - -
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	- - - - - - -

5

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP		FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP − 1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†	2[ ]	[	[	[	[	1	[
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

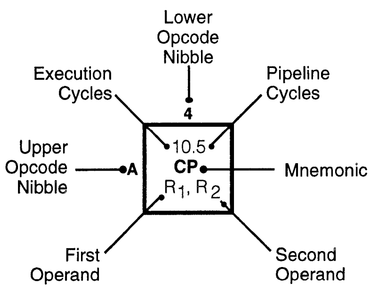
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2		**J85**			↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r2, Irr1	18.0 **LDCI** Ir2, Irr1	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

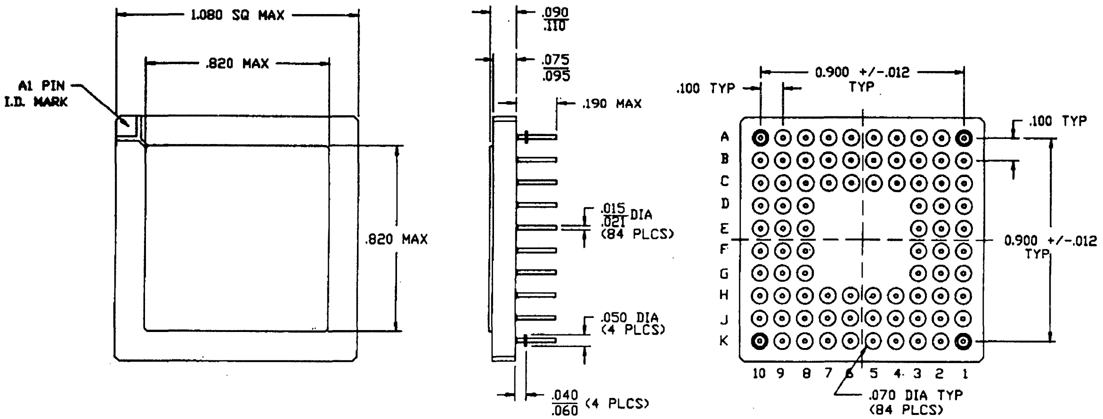
Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are not defined.

* 2-byte instruction appears as a 3-byte instruction

5

PACKAGE INFORMATION



84-Pin PGA Package Diagram

ORDERING INFORMATION

Z86C12

16 MHz
84-Pin PGA
Z86C1216GSE

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
G = Pin Grid Array

Temperature
S = 0°C to +70°C

Speed
16 - 16 MHz

Environmental
E = Hermetic Standard

Example:

Z 86C12 16 G S E is an Z86C12, 16 MHz, PGA, 0°C to +70°C, Hermetic Standard

- E — Environmental Flow
- S — Temperature
- G — Package
- 16 — Speed
- 86C12 — Product Number
- Z — Zilog Prefix

Introduction I

Z86C07 Z8® CMOS
8-Bit Microcontroller 1

Z86C08 Z8® CMOS
8-Bit Microcontroller 2

Z86E08 Z8® CMOS 8-Bit
OTP Microcontroller 3

Z86C11 Z8® CMOS
Microcontroller 4

Z86C12 Z8® CMOS
In-Circuit Emulator MCU 5

Z86C21 Z8® CMOS
8K ROM Microcontroller 6

Z86C21

8K ROM Z8® CMOS MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC or 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low Power Consumption - 220 mW (max) @ 16 MHz
- Fast instruction pointer - 1.0 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- 8 Kbytes of ROM
- 256 Byte Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes Control/Status Registers
  - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 12 and 16 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86C21 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C21 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM.

The MCU is packaged in a 40-pin DIP, 44-pin Plastic Leaded Chip Carrier, or a 44-pin Quad Flat Pack and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. Having the ROM/ROMless selectively, the MCU offers both external memory and preprogrammed ROM which enables this Z8 microcontroller to be used in high-volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C21 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C21 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C21 offers two on-chip counter/timers with a large number of user selectable modes, and a Asynchronous Receiver/Transmitter (UART-Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

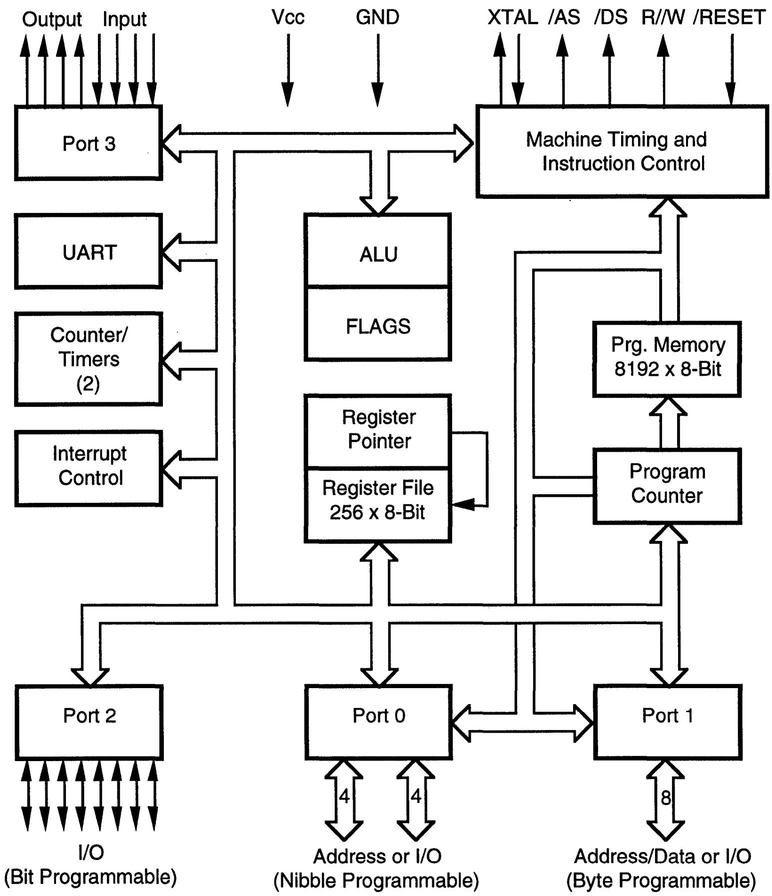


Figure 1. Functional Block Diagram

PIN DESCRIPTION

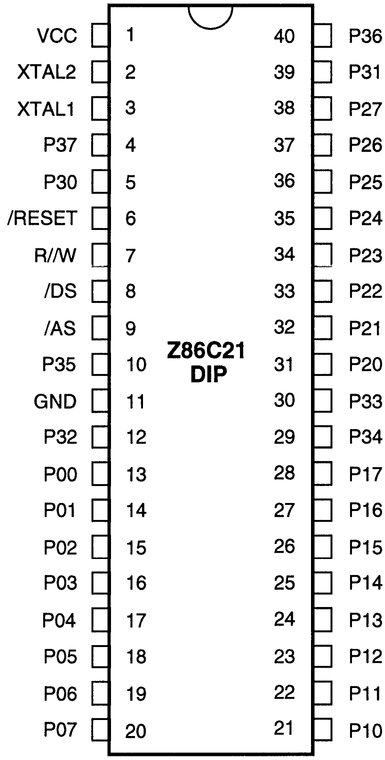


Figure 2. 40-Pin DIP Pin Assignments

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pins 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

6

PIN DESCRIPTION (Continued)

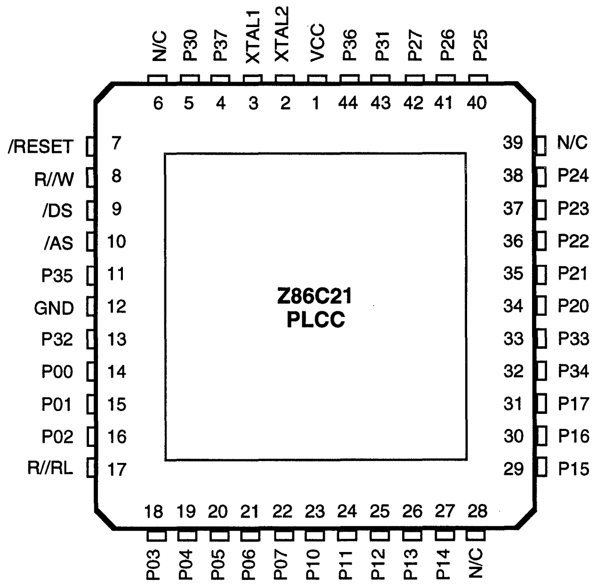


Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0 pin 0,1,2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0 pins 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pins 0,1,2,3,4	In/Output
5	P30	Port 3 pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1 pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3 pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3 pin 5	Output	40-42	P25-P27	Port 2 pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3 pin 1	Input
13	P32	Port 3 pin 2	Input	44	P36	Port 3 pin 6	Output

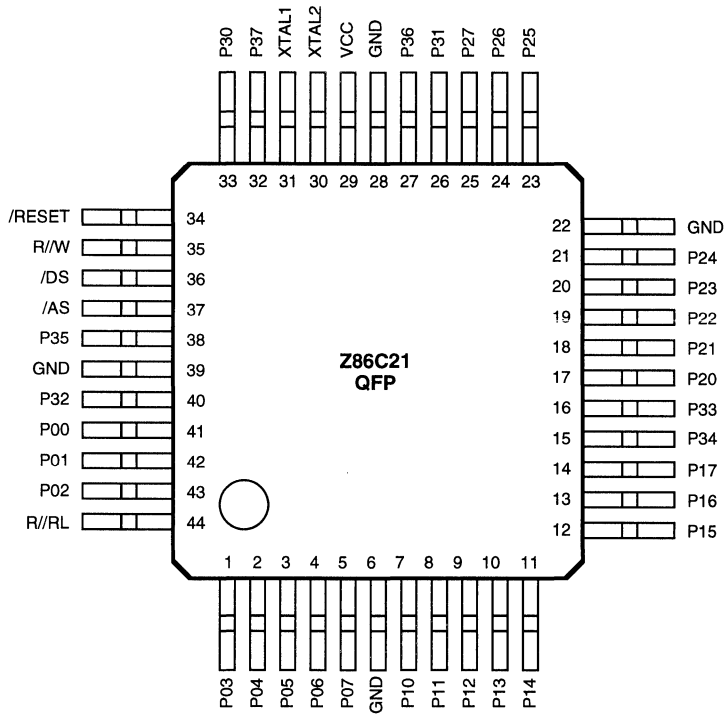


Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 pins 3,4,5,6,7	In/Output
6	GND	Ground	Input
7-14	P10-P17	Port 1 pins 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3 pin 4	Output
16	P33	Port 3 pin 3	Input
17-21	P20-P24	Port 2 pins 0,1,2,3,4	In/Output
22	GND	Ground	Input
23-25	P25-P27	Port 2 pins 5,6,7	In/Output
26	P31	Port 3 pin 1	Input
27	P36	Port 3 pin 6	Output
28	GND	Ground	Input
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output

Pin #	Symbol	Function	Direction
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3 pin 7	Output
33	P30	Port 3 pin 0	Input
34	/RESET	Reset	Input
35	R//W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3 pin 5	Output
39	GND	Ground	Input
40	P32	Port 3 pin 2	Input
41-43	P00-P02	Port 0 pins 0,1,2	In/Output
44	R//RL	ROM/ROMless control	Input

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PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8. For more details on the ROMless version, refer to the Z86C91 product specification. (**Note:** that when left unconnected or pulled high to V_{CC}, the part functions as a normal Z86C21 ROM version). This pin is only available on the 44-pin versions of the Z86C21.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C21 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC2. When /RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 5).

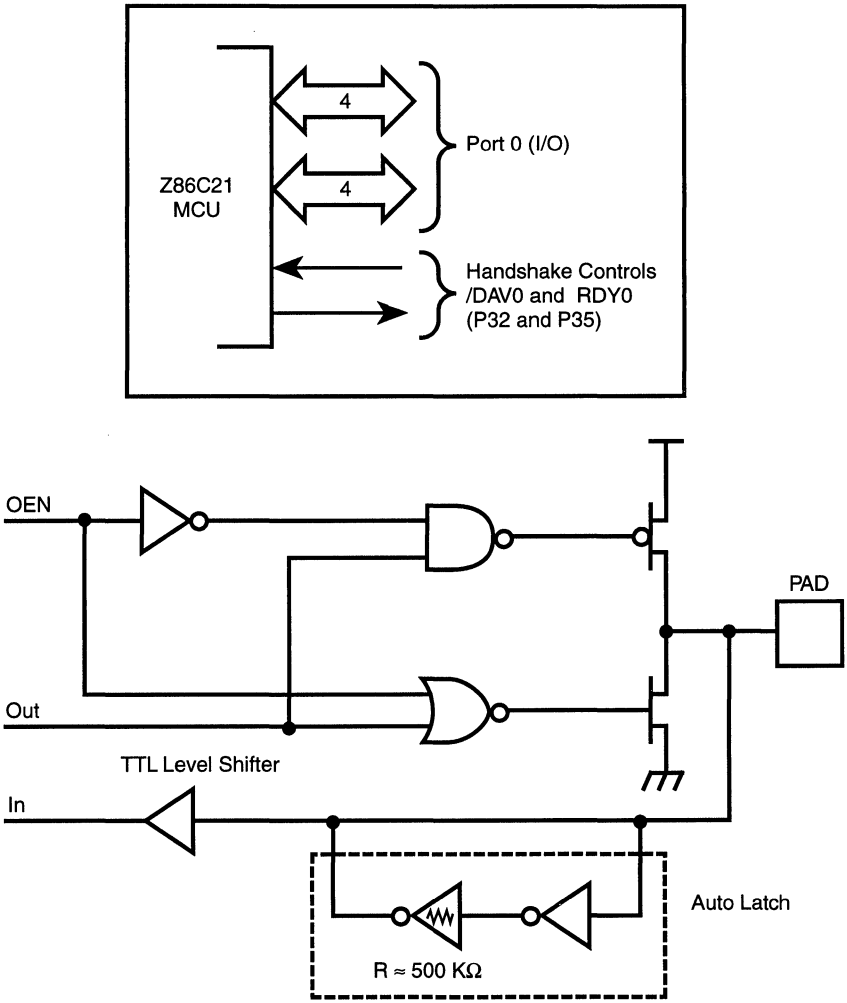


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C21, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 8192 are referenced through Port 1. To interface external memory, Port 1 is programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in a high-impedance state along with Port 0, /AS, /DS and R//W, allowing the MCU to share common resource in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 6).

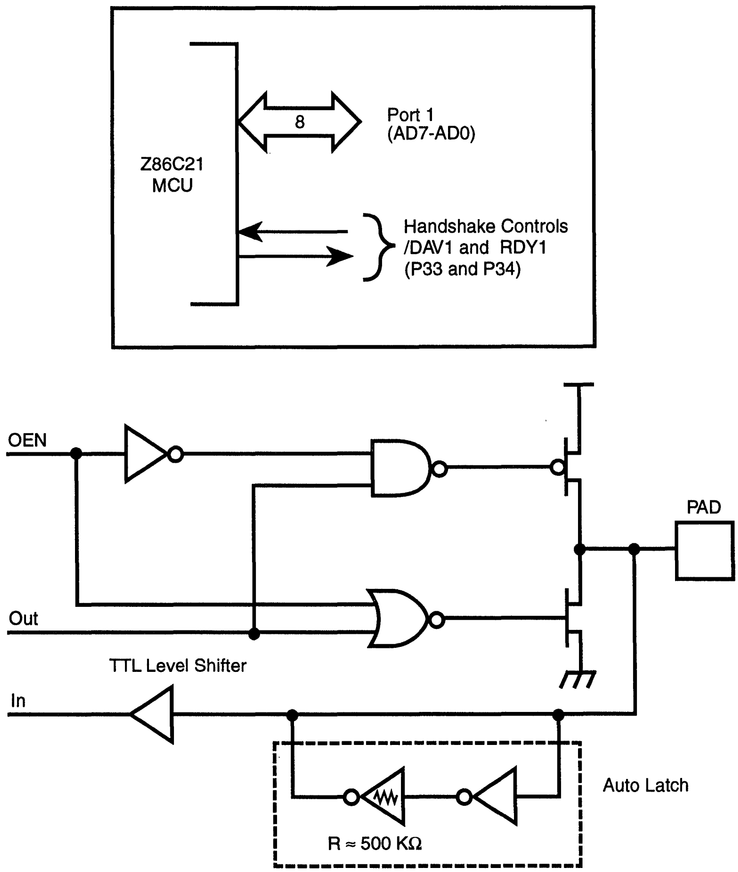


Figure 6. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7).

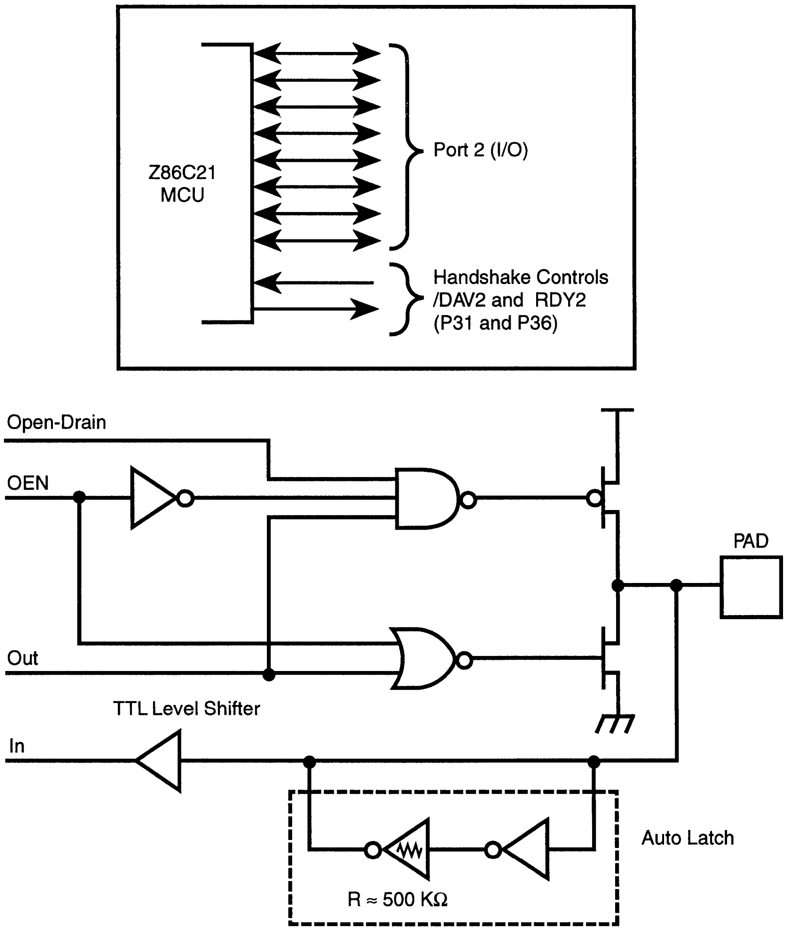


Figure 7. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed-input and four-fixed-output port. These eight I/O lines have four-fixed input (P33-P30) and four fixed output (P37-P34) ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 8 and Table 4) Port 3 pins have Auto Latches only.
Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

UART Operation. Port 3 lines P30 and P37, are be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C21 automatically adds a start bit and two stop bits to transmitted data (Figure 9). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

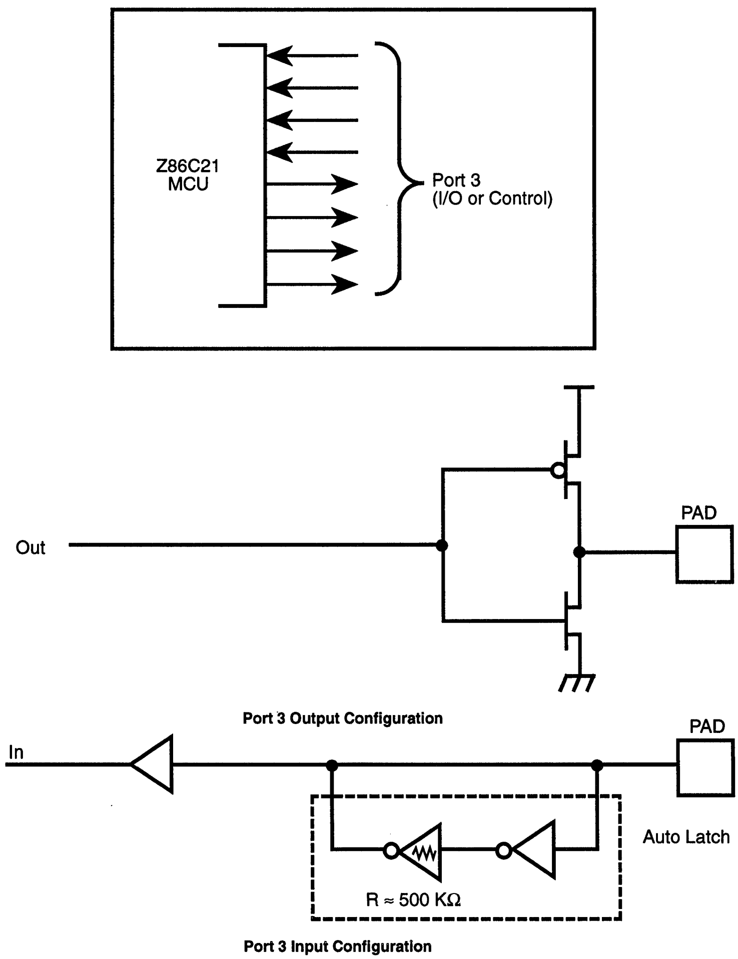


Figure 8. Port 3 Configuration

Table 4. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals; D = Data Available; R = Ready

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not been driven by any source.

Low EMI Option. The Z86C21 is available in a Low EMI option. This option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms typical.
- Oscillator divide-by-two circuitry is eliminated.
- Internal SCLK/TCLK operation is limited to a maximum of 4 MHz (250 ns cycle time)

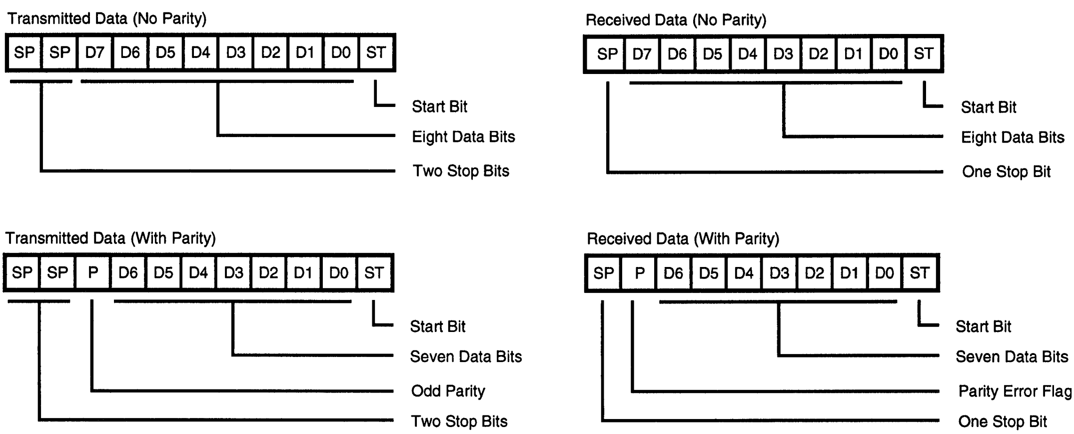


Figure 9. Serial Data Formats

FUNCTIONAL DESCRIPTION
Address Space

Program Memory. The Z86C21 can address up to 56K bytes of external program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 8191 consists of on-chip ROM. At addresses 8192 and greater, the Z86C21 executes external program memory fetches. In the ROMless mode, the Z86C21 can address up to 64K bytes of external program memory. Program execution begins at external location 000C (HEX) after a reset.

Data Memory (/DM). The ROM version can address up to 56K bytes of external data memory space beginning at location 8192. The ROMless version can address up to 64K bytes of external data memory. External data memory can be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34, is used to distinguish between data and program memory space (Figure 11). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

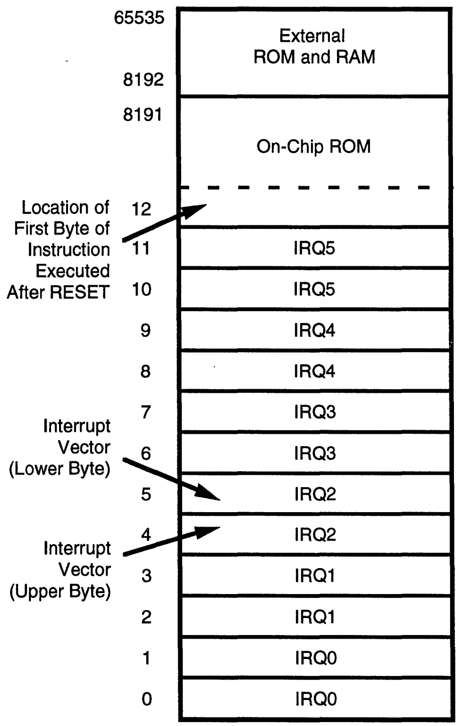


Figure 10. Program Memory Configuration

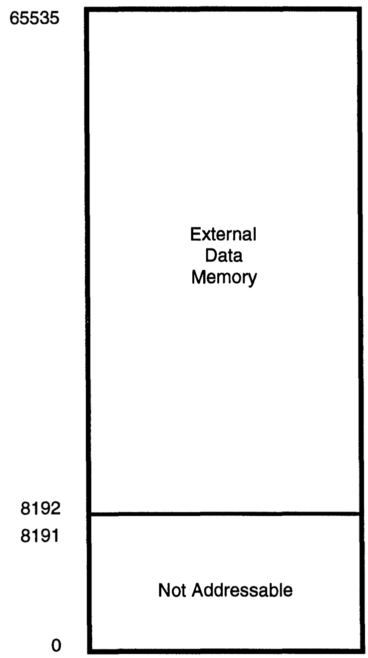


Figure 11. Data Memory Configuration

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 12). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C21 also allows short 4-bit register addressing using the Register Pointer (Figure 13). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group. For the reset and power-up conditions of the Register File, see Figure 14.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239 … R4	General-Purpose Registers	
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 12. Register File

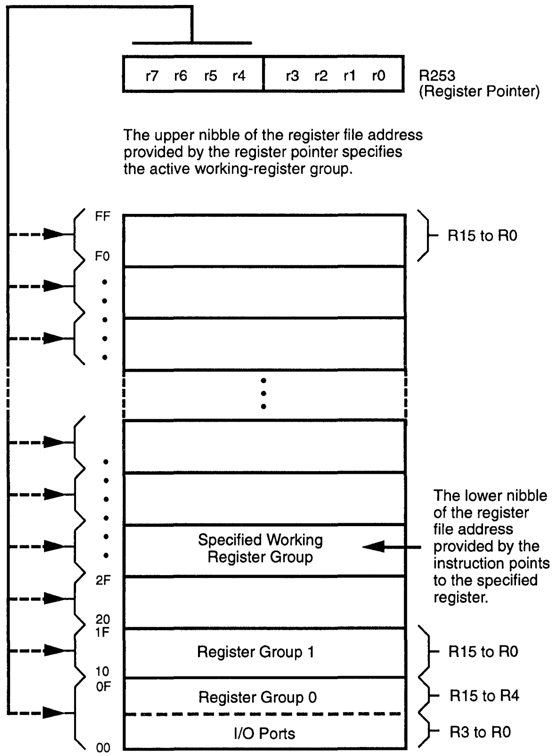
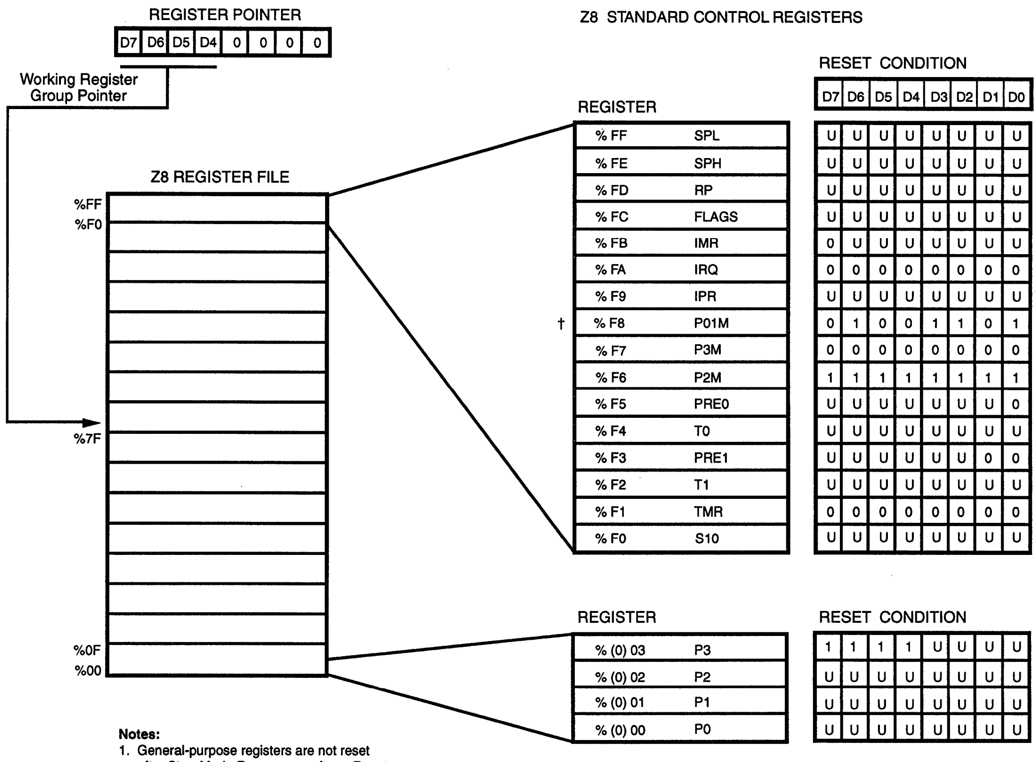


Figure 13. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)



Notes:
1. General-purpose registers are not reset after Stop-Mode Recovery or after a Reset.
2. General-purpose registers are undefined after Power-up.

U = Unknown

† = For ROMless (Z86C91) reset condition = 10110110

Figure 14. RAM Register File Reset Condition

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 8 Kbytes of program memory is mask programmable. A ROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Note: With RAM/ROM protect on even, the Z86C21 cannot access the memory space.

Stack. The Z86C21 has a 16-bit Stack Pointer (R254-R255) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 8192 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH-Bit 8-15) is used as a general-purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers divides the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

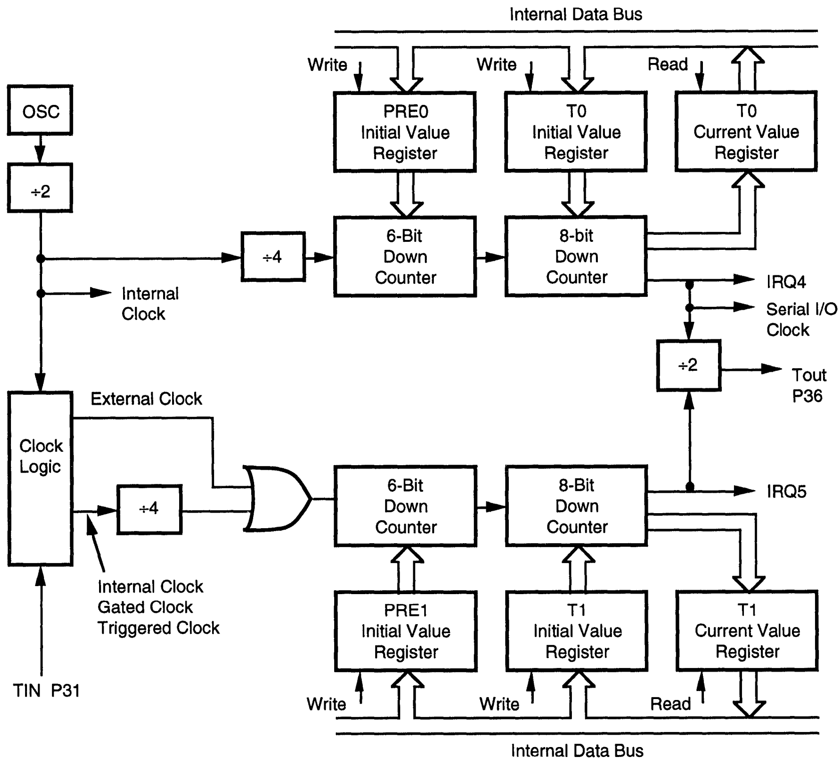


Figure 15. Counter/Timers Block Diagram

6

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C21 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follow: four sources are claimed by Port 3, lines P33-P30; one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. (Refer to Table 4.)

All Z86C21 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

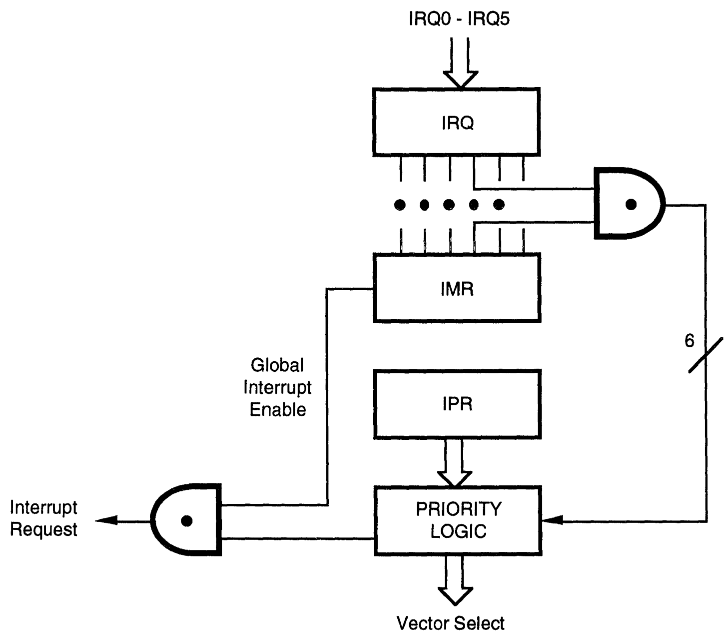


Figure 16. Interrupt Block Diagram

Clock. The Z86C21 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 300 pF) from each pin 11, ground instead of just system ground. This prevents noise injection into the clock input (Figure 17).

Note: Actual capacitor value is specified by the crystal manufacturer.

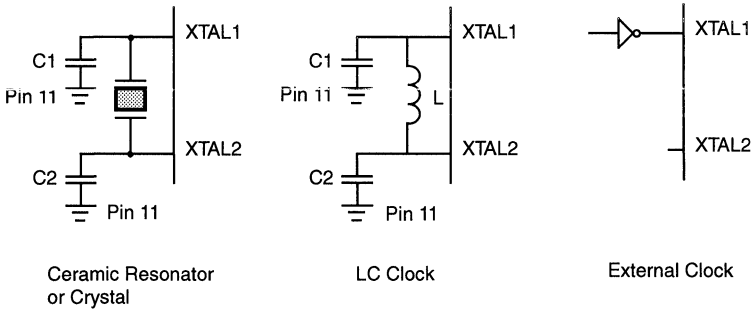


Figure 17. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset which causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction. i.e.,

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp		†	°C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).

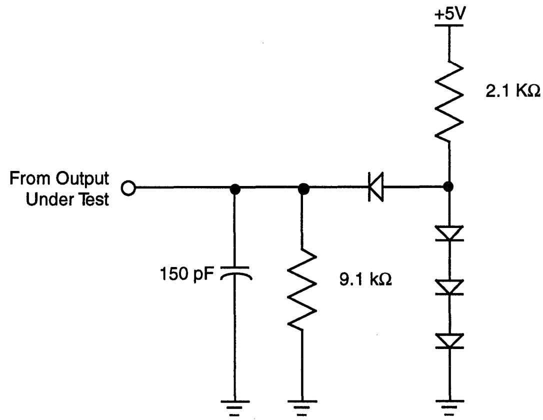


Figure 18. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 μA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC}+0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC}+0.3	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage	V_{CC}–100 mV		V_{CC}–100 mV			V	I_{OH} = –100 μA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC} +0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	–2	2		μA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		μA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		μA	V_{RL} = 0V
I_{CC}	Supply Current		30		30	20	mA	[1] @ 12 MHz
			35		35	24	mA	[1] @ 16 MHz
I_{CC1}	Standby Current		6.5		6.5	4	mA	[1] HALT mode V_{IN} = 0V, V_{CC}@ 12 MHz
			7		7	4.5	mA	[1] HALT mode V_{IN} = 0V, V_{CC}@ 16 MHz
I_{CC2}	Standby Current		10		20	1	μA	[1] STOP mode V_{IN} = 0V, V_{CC}
I_{ALL}	Auto Latch Low Current	–10	10	–14	14	5	μA	

Notes:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.

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AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

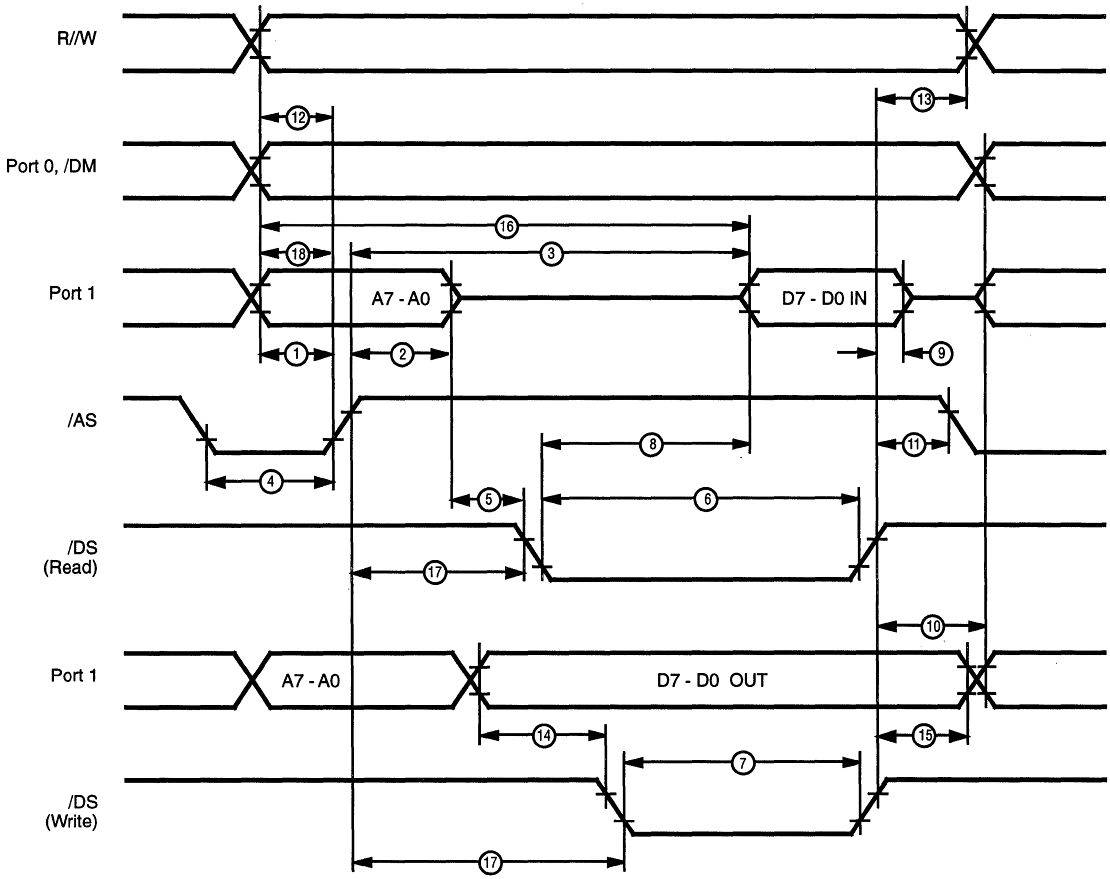

Figure 19. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
External I/O or Memory Read or Write Timing Table

			T_A = 0°C to +70°C				T_A = −40°C to +105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		25		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		35		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		250		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		40		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	65		50		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	45		35		45		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	50		35		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	55		35		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		310		230		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	65		45		65		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Rise Delay	50		30		50		30		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.

Standard Test Load
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC – 3.25
3	TdAS(DR)	2.83TpC + 6.14
4	TwAS	0.66TpC – 1.65
6	TwDSR	2.33TpC – 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC – 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC – 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC – 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC – 19
16	TdA(DR)	4TpC –20
17	TdAS(DS)	0.91TpC –10.7
18	TdDM(AS)	0.9TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

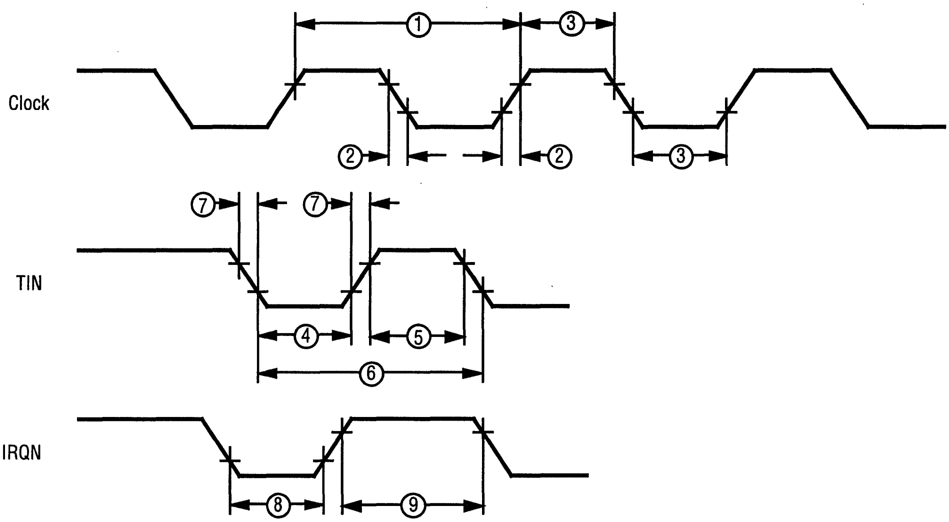

Figure 20. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Sym	Parameter	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A = −40°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	35		25		35		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC		3TpC		3TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

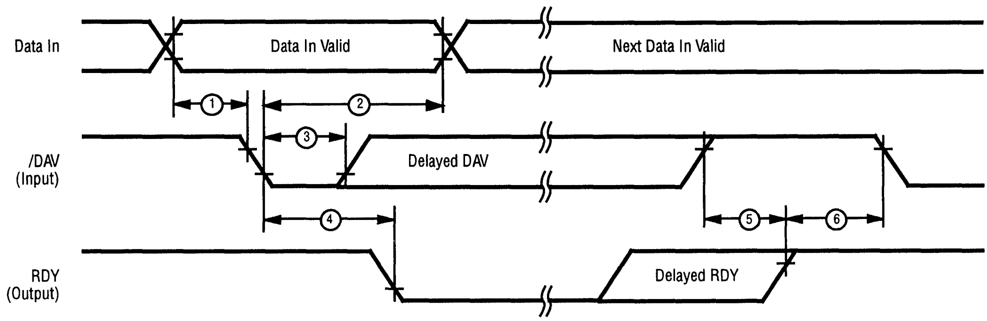

Figure 21. Input Handshake Timing

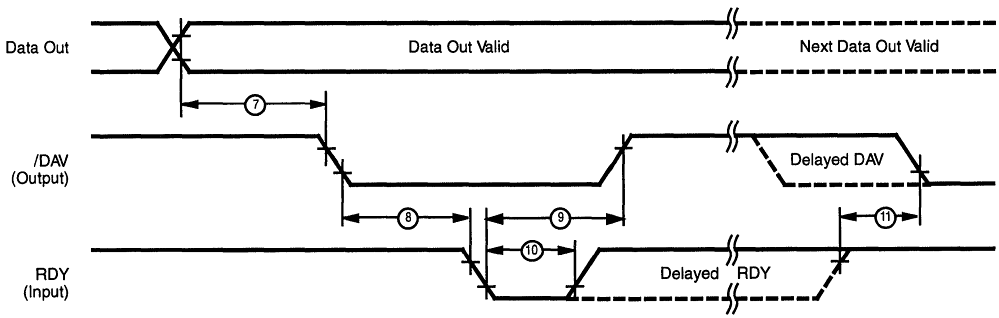

Figure 22. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Sym	Parameter	T_A = 0°C to +70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = −40°C to +105°C 12 MHz Min	Max	16 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		IN
3	TwDAV	Data Available Width	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdRDYO(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		IN
7	TdDO(DAV)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TdDAVO(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		OUT
9	TdRDYO(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110		110		110		110		OUT
11	TdRDYOd(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

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Z8 CONTROL REGISTER DIAGRAMS

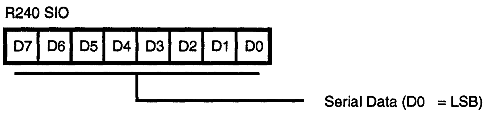

Figure 23. Serial I/O Register (F0H: Read/Write)

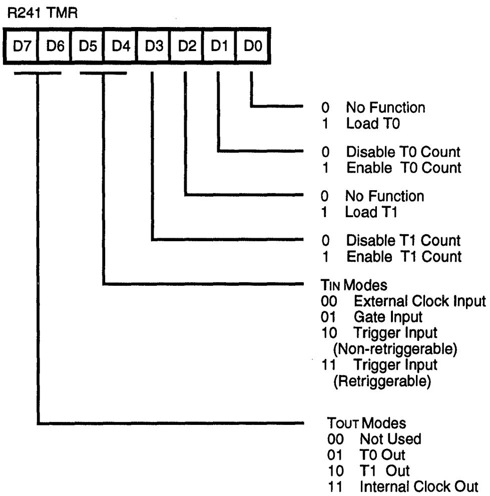

Figure 24. Timer Mode Register (F1H: Read/Write)

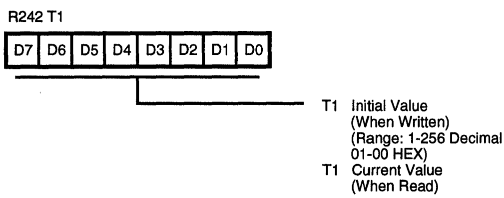

Figure 25. Counter/Timer 1 Register (F2H: Read/Write)

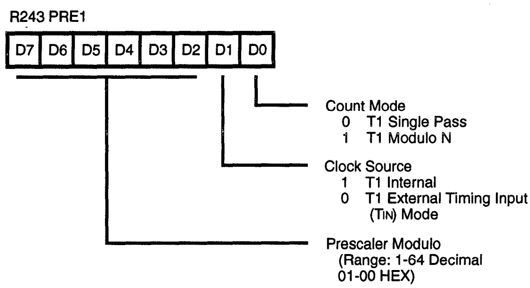

Figure 26. Prescaler 1 Register (F3H: Write Only)

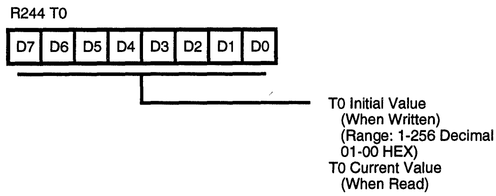

Figure 27. Counter/Timer 0 Register (F4H: Read/Write)

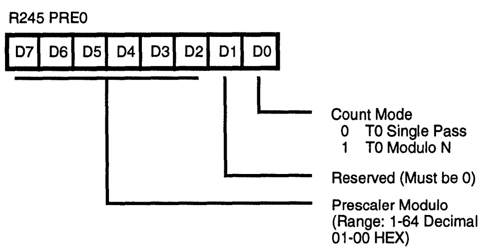

Figure 28. Prescaler 0 Register (F5H: Write Only)

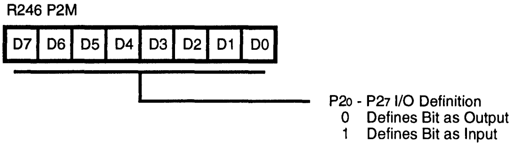

Figure 29. Port 2 Mode Register (F6H: Write Only)

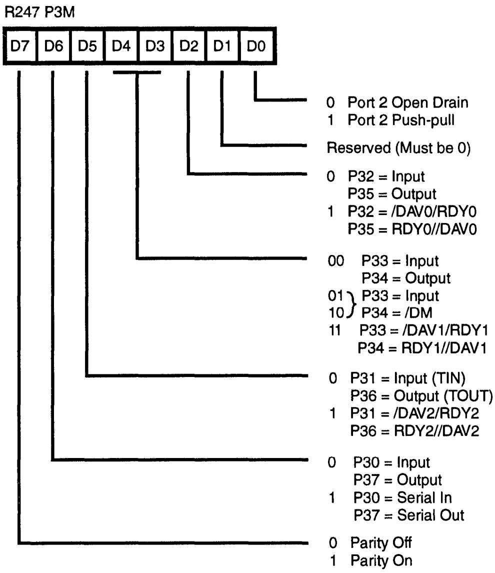

Figure 30. Port 3 Mode Register (F7H: Write Only)

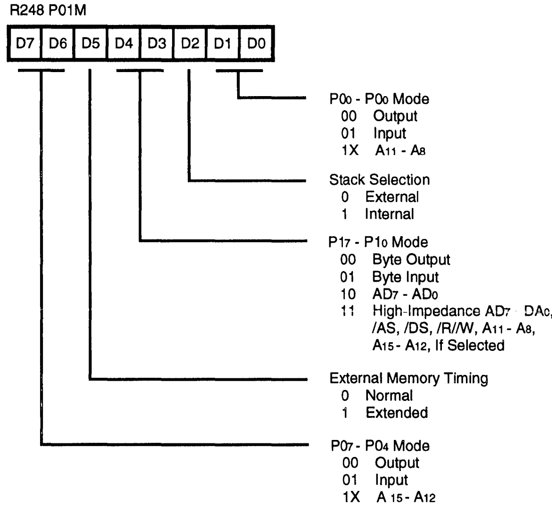

Figure 31. Port 0 and 1 Mode Register (F8H: Write Only)

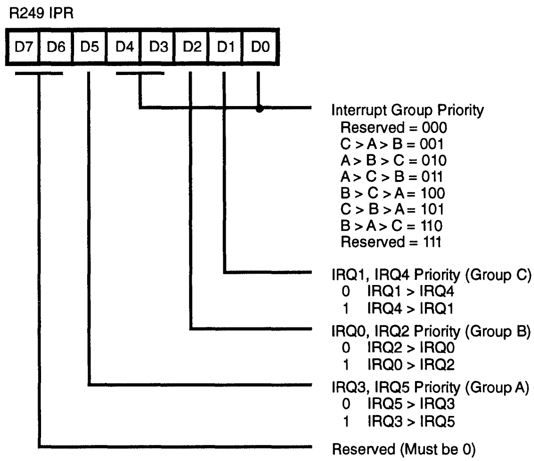

Figure 32. Interrupt Priority Register (F9H: Write Only)

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Z8 CONTROL REGISTER DIAGRAMS (Continued)

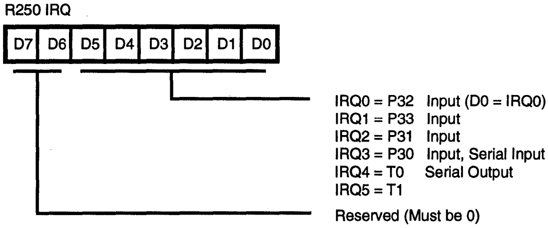


Figure 33. Interrupt Request Register (FAH: Read/Write)

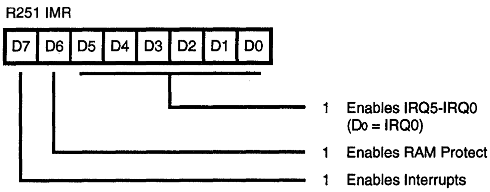


Figure 34. Interrupt Mask Register (FBH: Read/Write)

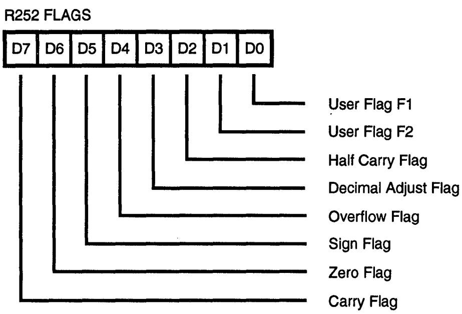


Figure 35. Flag Register (FCH: Read/Write)

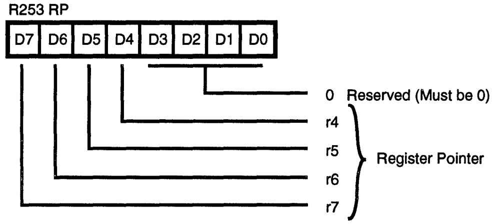


Figure 36. Register Pointer Register (FDH: Read/Write)

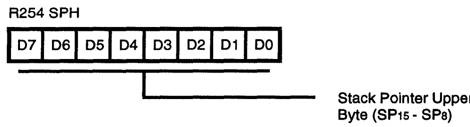


Figure 37. Stack Pointer Register (FEH: Read/Write)

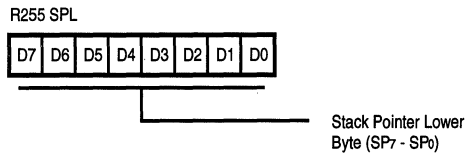


Figure 38. Stack Pointer Register (FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

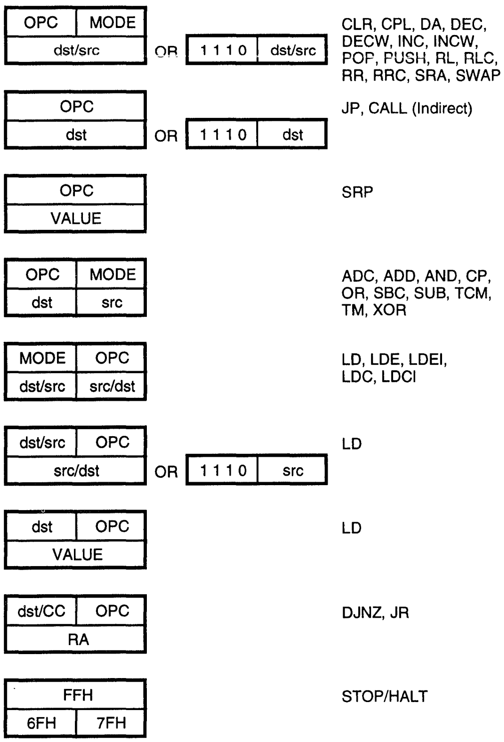
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

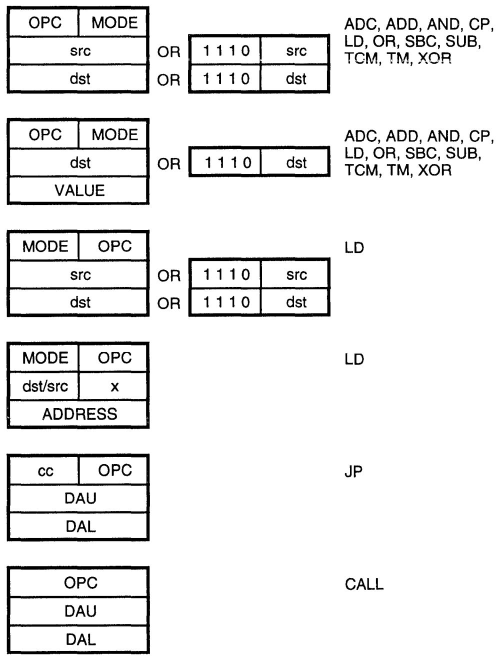
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "$\leftarrow$". For example:

dst $\leftarrow$ dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

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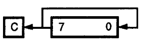
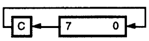
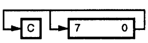
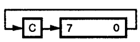
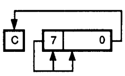
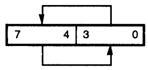
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

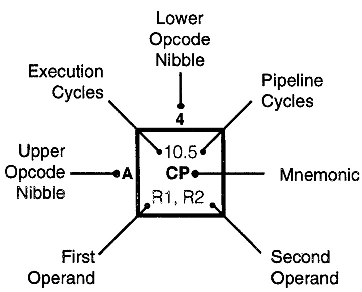
Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

6

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1



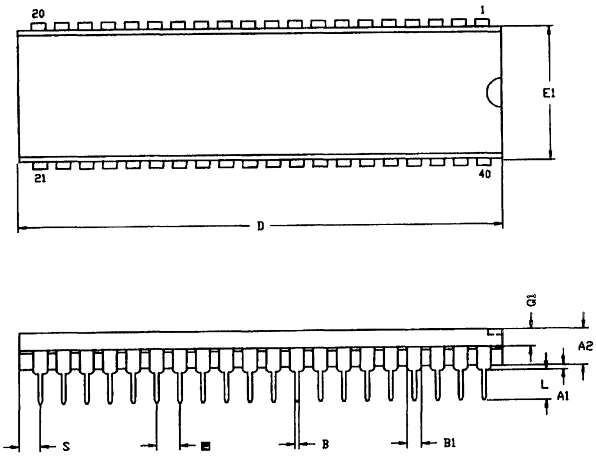
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

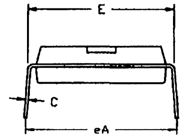
Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

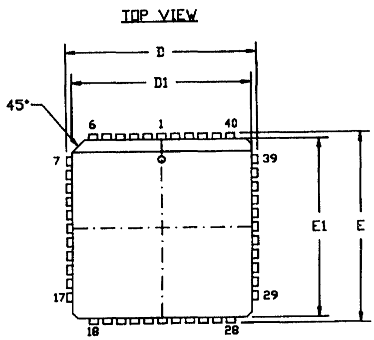


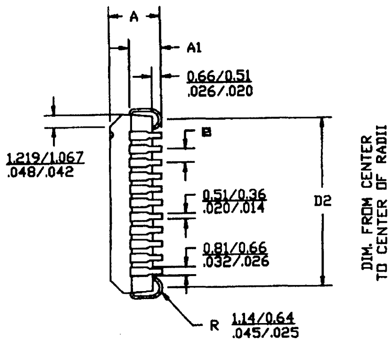


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
■	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin PDIP Package Diagram



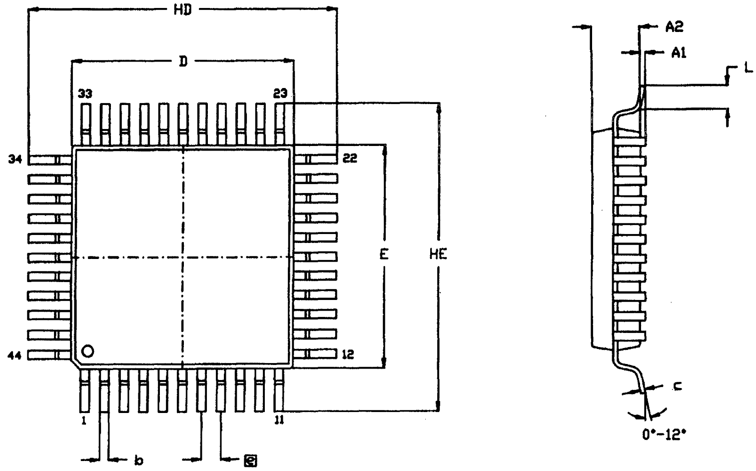


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : $\frac{MM}{INCH}$

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
■	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C21

12 MHz

40-pin DIP	**44-pin PLCC**	**44-pin QFP**
Z86C2112PSC	Z86C2112VSC	Z86C2112FSC
Z86C2112PEC	Z86C2112VEC	Z86C2112FEC

16 MHz

40-pin DIP	**44-pin PLCC**	**44-pin QFP**
Z86C2116PSC	Z86C2116VSC	Z86C2116FSC

For fast results, contact your local Zilog Sales Office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Temperature
S = 0°C to +70°C
E = -40°C to 105°C

Speed
12 = 12 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:

Z 89C21 12 P S C is a Z89C21, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 89C21 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller 7

Z86C61/62/96 CMOS Z8®
Microcontroller 8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
ROMless Microcontroller 10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller 11

Support Products 12

Superintegration™
Products Guide S

Zilog's Literature Guide
Ordering Information L

Z86E21

CMOS Z8® MICROCONTROLLER WITH 8K OTP

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, or 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low Power Consumption - 275 mW (max)
- Fast Instruction Pointer - 1.0 ms @ 12 MHz
- Two Standby Modes - STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- High Voltage Protection on High Voltage Inputs
- RAM and EPROM Protect
- 8 Kbytes of EPROM
- 256 Bytes Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes of Control and Status Registers
  - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 12 and 16 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E21 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E21 is a member of the Z8® single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E21 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbytes of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcontroller to be used in high-volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E21 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

GENERAL DESCRIPTION (Continued)

For applications which demand powerful I/O capabilities, the Z86E21 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E21 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (UART) (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

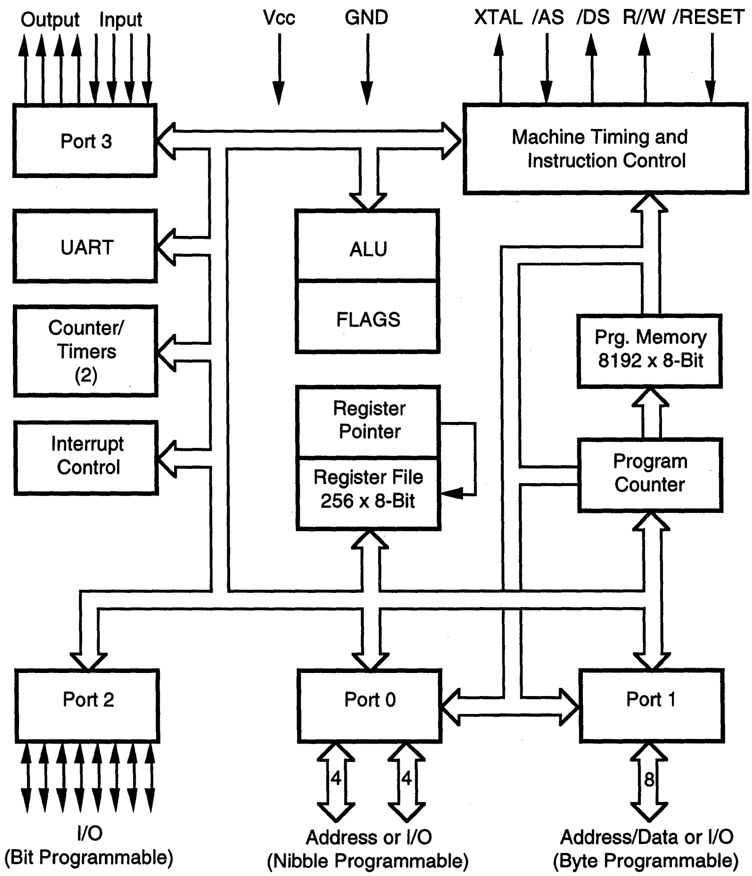


Figure 1. Functional Block Diagram

PIN DESCRIPTION
Standard Mode

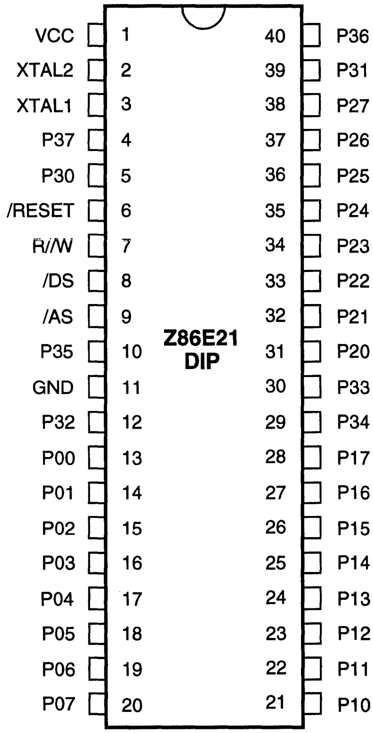


Figure 2. 40-Pin DIP Pin Assignments

Table 1. 40-Pin DIP Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

PIN DESCRIPTION (Continued)
Standard Mode

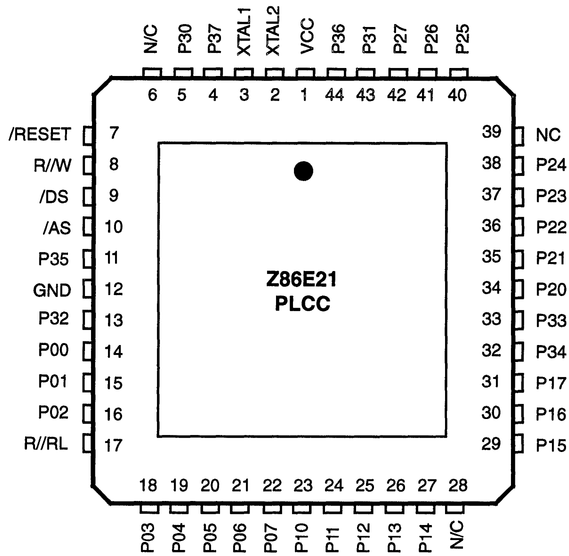


Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
4	P37	Port 3, Pin 7	Output	23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
5	P30	Port 3, Pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3, Pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3, Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3, Pin 5	Output	40-42	P27-P25	Port 2, Pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3, Pin 1	Input
13	P32	Port 3, Pin 2	Input	44	P36	Port 3, Pin 6	Output

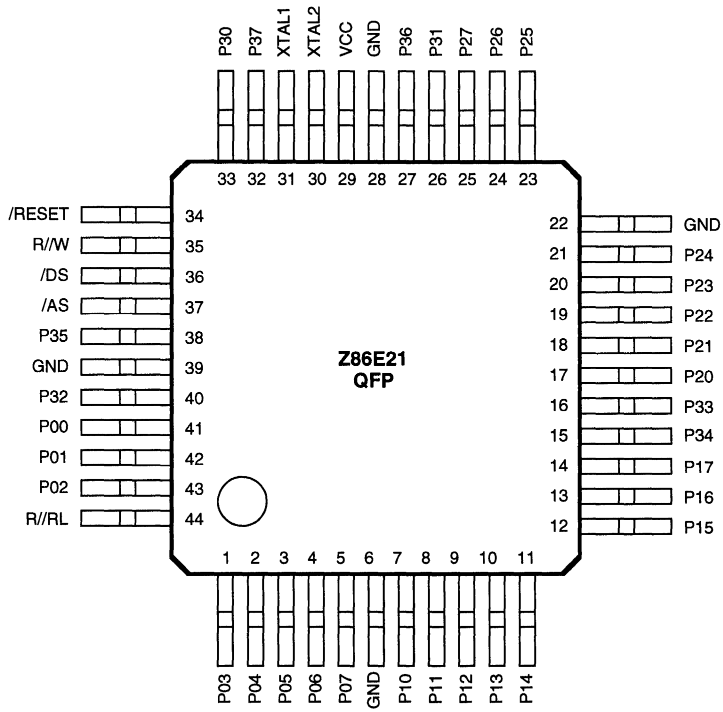


Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction
1-5	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
6	GND	Ground	Input
7-14	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3, Pin 4	Output
16	P33	Port 3, Pin 3	Input
17-21	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
22	GND	Ground	Input
23-25	P27-P25	Port 2, Pins 5,6,7	In/Output
26	P31	Port 3, Pin 1	Input
27	P36	Port 3, Pin 6	Output
28	GND	Ground	Input
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output

Pin #	Symbol	Function	Direction
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3, Pin 7	Output
33	P30	Port 3, Pin 0	Input
34	/RESET	Reset	Input
35	R//W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3, Pin 5	Output
39	GND	Ground	Input
40	P32	Port 3, Pin 2	Input
41-43	P02-P00	Port 0, Pins 0,1,2	In/Output
44	R//RL	ROM/ROMless control	Input

PIN DESCRIPTION (Continued)
EPROM Mode

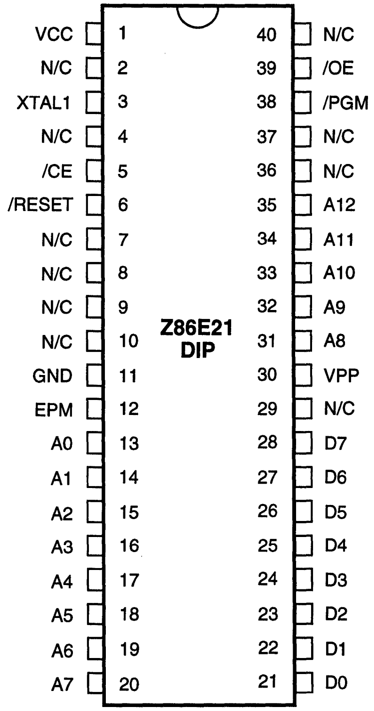


Figure 5. 40-Pin DIP Pin Assignments

Table 4. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	N/C	Not Connected	Input
3	XTAL1	Crystal, Oscillator Clock	Input
4	N/C	Not Connected	Input
5	/CE	Chip Enable	Input
6	/RESET	Reset	Input
7-10	N/C	Not Connected	Input
11	GND	Ground	Input
12	EPM	EPROM Prog Mode	Input
13-20	A7-A0	Address 0,1,2,3,4,5,6,7	Input
21-28	D7-D0	Data 0,1,2,3,4,5,6,7	In/Output
29	N/C	Not Connected	Input
30	V_{PP}	Prog Voltage	Input
31-35	A12-A8	Address 8,9,10,11,12	Input
36-37	N/C	Not Connected	Input
38	/PGM	Prog Mode	Input
39	/OE	Output Enable	Input
40	N/C	Not Connected	Input

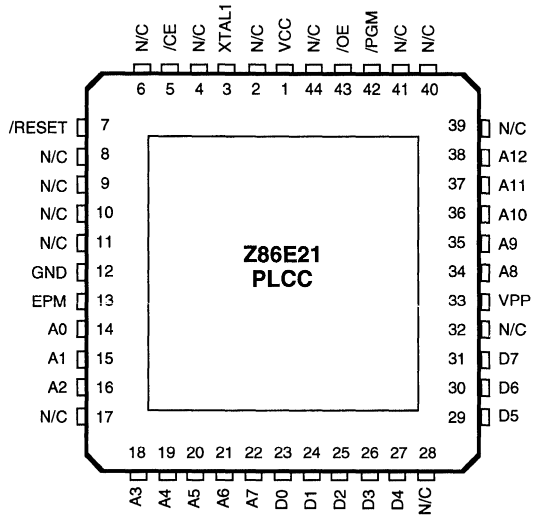


Figure 6. 44-Pin PLCC Pin Assignments

Table 5. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	N/C	Not Connected	Input
3	XTAL1	Crystal, Oscillator Clock	Input
4	N/C	Not Connected	Input
5	/CE	Chip Enable	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8-11	N/C	Not Connected	Input
12	GND	Ground	Input
13	EPM	EPROM Prog Mode	Input
14-16	A0-A2	Address 0,1,2	Input
17	N/C	Not Connected	Input

Pin #	Symbol	Function	Direction
18-22	A7-A3	Address 3,4,5,6,7	Input
23-27	D4-D0	Data 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	D7-D5	Data 5,6,7	In/Output
32	N/C	Not Connected	Input
33	V_{PP}	Prog Voltage	Input
34-38	A12-A8	Address 8,9,10,11,12	Input
39-41	N/C	Not Connected	Input
42	/PGM	Prog Mode	Input
43	/OE	Output Enable	Input
44	N/C	Not Connected	Input

PIN DESCRIPTION (Continued)
EPROM Mode

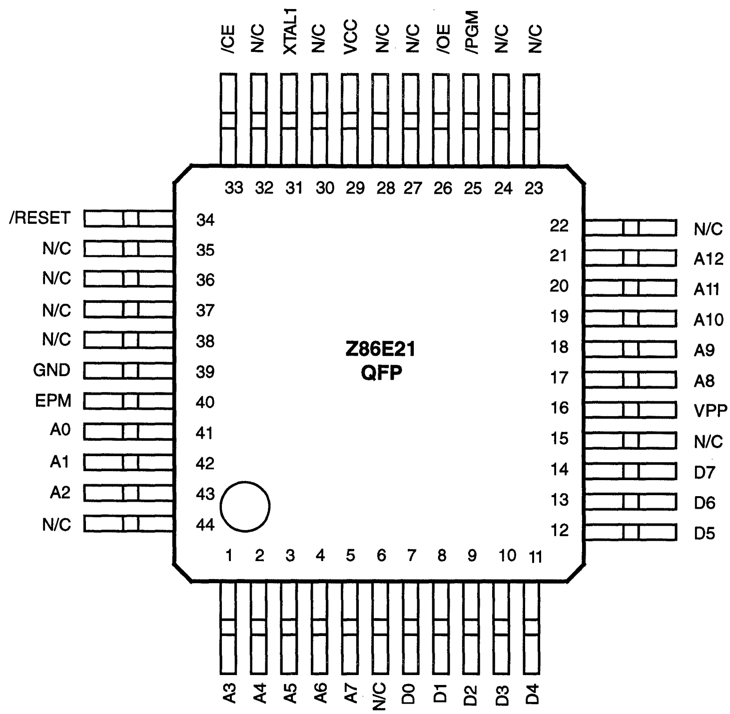


Figure 7. 44-Pin QFP Pin Assignments

Table 6. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-5	A7-A3	Address 3,4,5,6,7	Input	29	V_{CC}	Power Supply	Input
6	N/C	Not Connected	Input	30	N/C	Not Connected	Input
7-11	D4-D0	Data 0,1,2,3,4		31	XTAL1	Crystal, Oscillator Clock	Input
12-14	D7-D5	Data 5,6,7	In/Output	32	N/C	Not Connected	Input
15	N/C	Not Connected	Input	33	/CE	Chip Enable	Input
16	V_{PP}	Prog Voltage	Input	34	/RESET	Reset	Input
17-21	A8-A12	Address 8,9,10,11,12	Input	35-38	N/C	Not Connected	Input
22-24	N/C	Not Connected	Input	39	GND	Ground	Input
25	/PGM	Prog Mode	Input	40	EPM	EPROM Prog Mode	Input
26	/OE	Output Enable	Input	41-43	A2-A0	Address 0,1,2	Input
27	N/C	Not Connected	Input	44	N/C	Not Connected	Input
28	N/C	Not Connected	Input				

PIN FUNCTIONS

ROMless (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8. For more details on the ROMless version, refer to the Z86C91 product specification.

Note: When left unconnected or pulled high to V_{CC}, the part will function as a normal Z86E21 EPROM version. This pin is only available on the 44-pin versions of the Z86E21.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1 *Crystal 2, Crystal 1* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86E21 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 8).

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86E21, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/ data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 8192 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 9).

PIN FUNCTIONS (Continued)

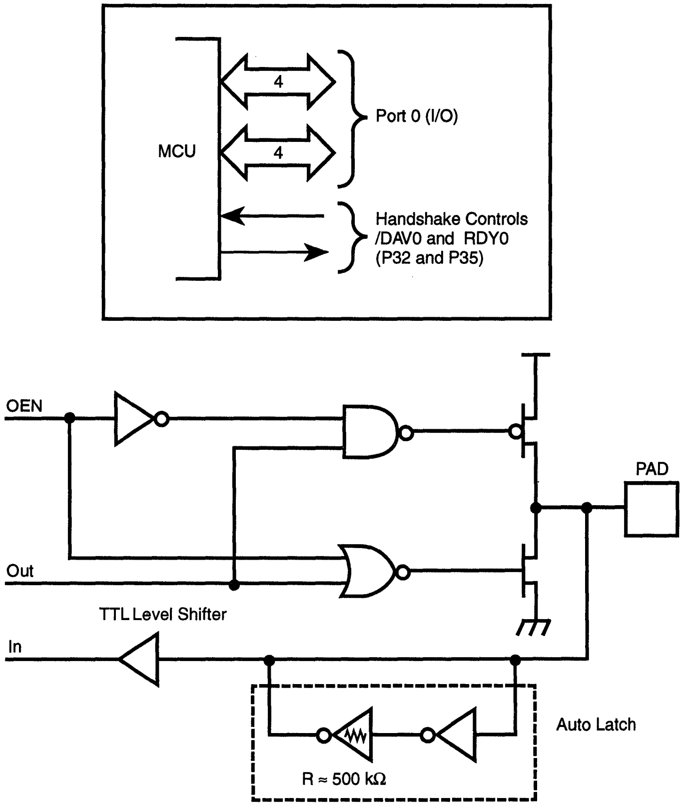


Figure 8. Port 0 Configuration

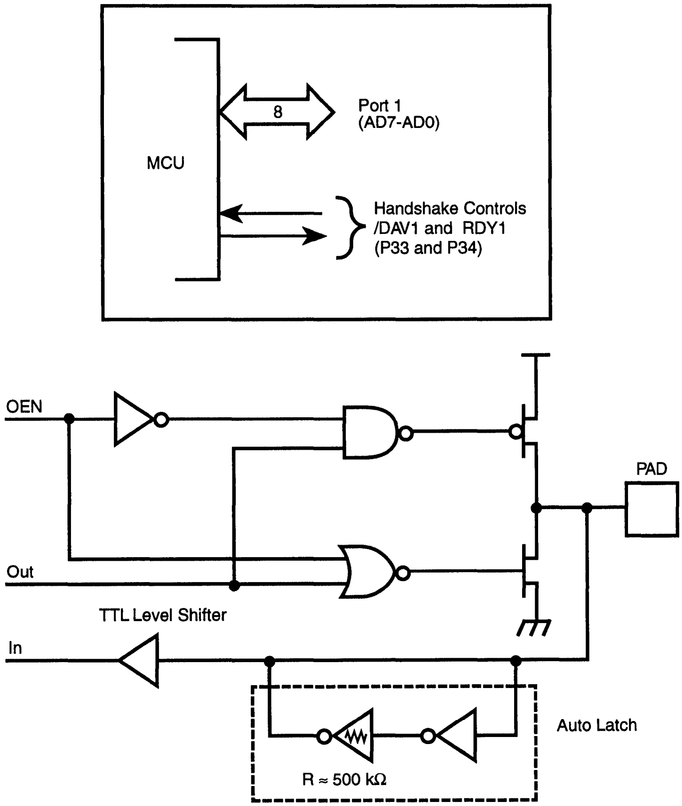


Figure 9. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 10 and Table 7).

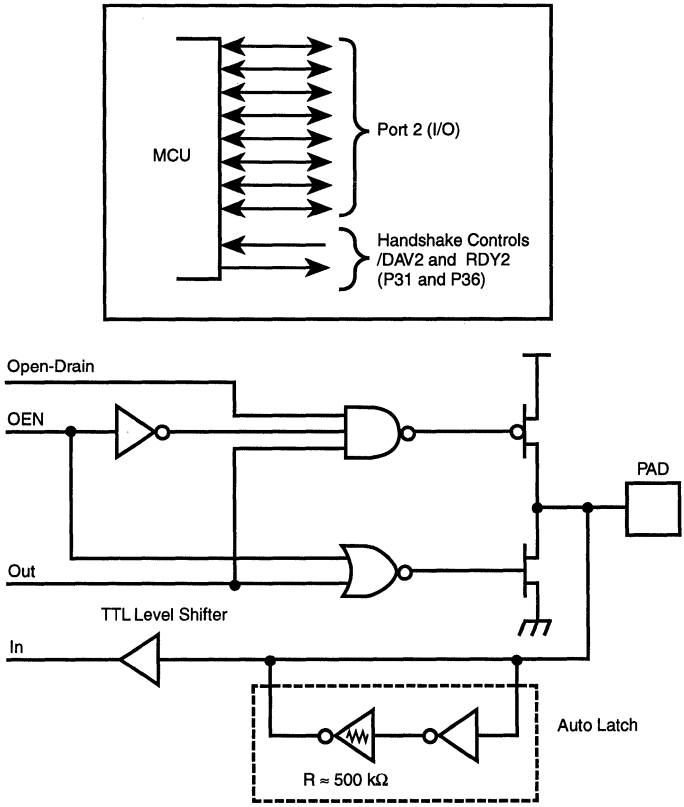


Figure 10. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 11).

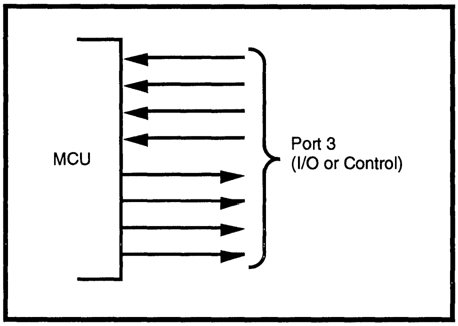


Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), Data Memory Select (/DM) and EPROM control signals (P30 = /CE, P31 = /OE, P32 = EPM and P33 = V_{PP}).

Table 7. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN		IRQ3				Serial In		/CE
P31	IN	T_{IN}	IRQ2			D/R			/OE
P32	IN		IRQ0	D/R					EPM
P33	IN		IRQ1		D/R				V_{PP}
P34	OUT				R/D			DM	
P35	OUT			R/D					
P36	OUT	T_{OUT}				R/D			
P37	OUT						Serial Out		
T0			IRQ4						
T1			IRQ5						

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z86E21 automatically adds a start bit and two stop bits to transmitted data (Figure 12). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

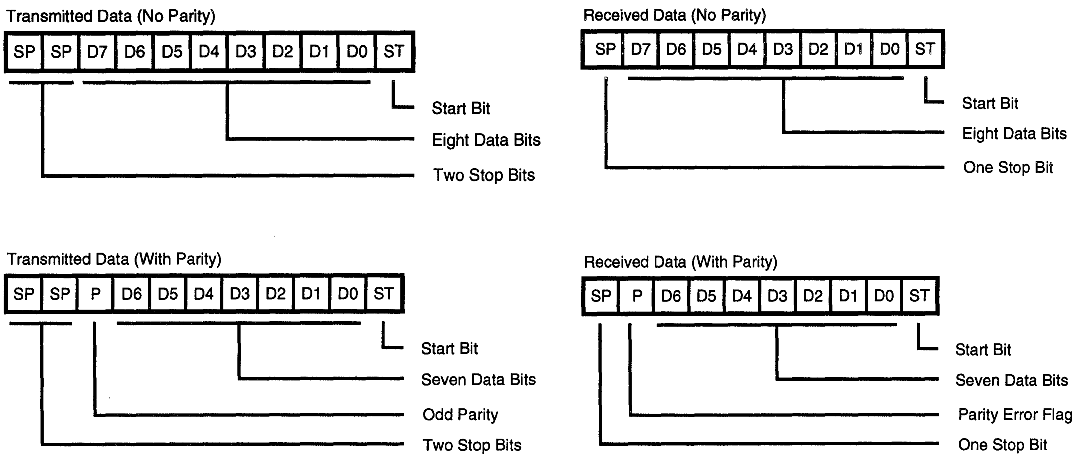


Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33-P30 inputs differ from the Z86C21 because there is no clamping diode to V_{CC} due to the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode

ADDRESS SPACE

Program Memory. The Z86E21 can address 56 Kbytes of external program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 8191 consists of on-chip EPROM. At addresses 8192 and above, the Z86E21 executes external program memory fetches. In ROMless mode, the Z86E21 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

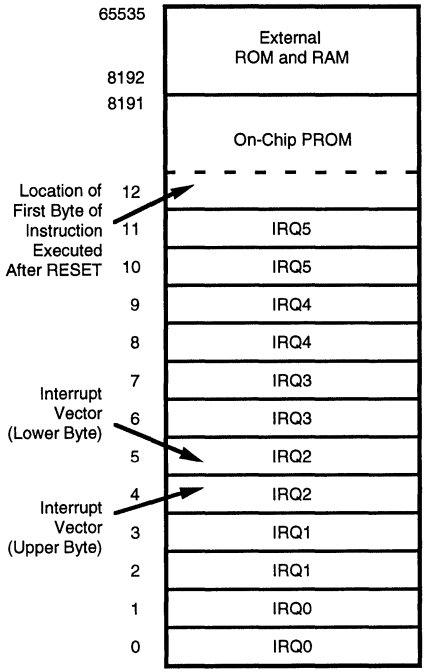


Figure 13. Program Memory Configuration

Data Memory (/DM). The EPROM version can address up to 56 Kbytes of external data memory space beginning at location 8192. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

Register File. The register file consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E21 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Stack. The Z86E21 has a 16-bit Stack Pointer (R255-R254) used for external stacks that reside anywhere in the data memory for the ROMless mode, but only from 8192 to 65535 in the EPROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH Bits 15-8) can be use as a general purpose register when using internal stack only.

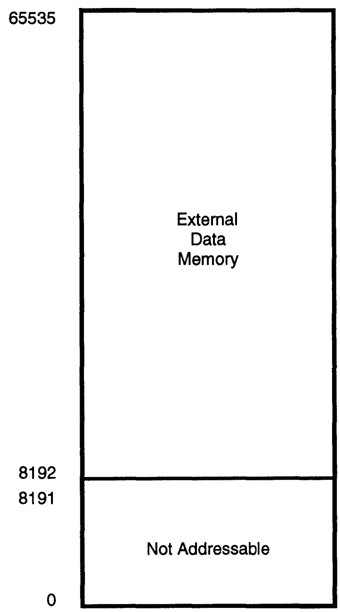


Figure 14. Data Memory Configuration

ADDRESS SPACE (Continued)

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239 … R4	General-Purpose Registers	
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 15. Register File

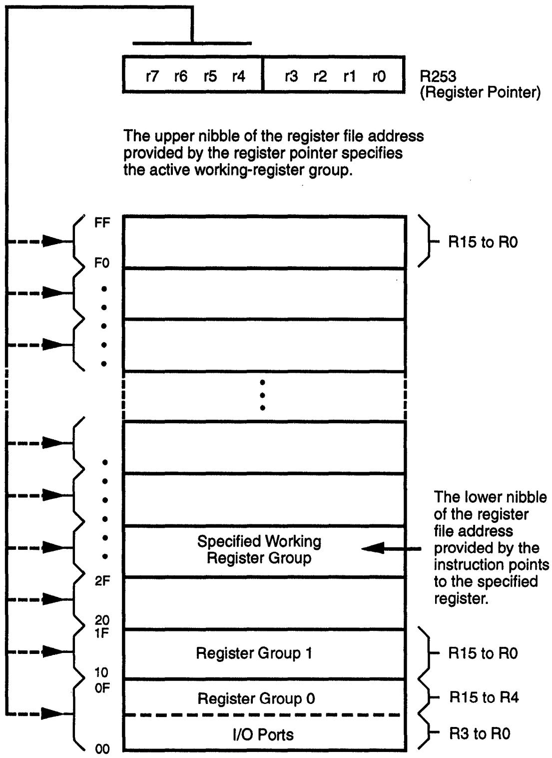


Figure 16. Register Pointer

FUNCTIONAL DESCRIPTION

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

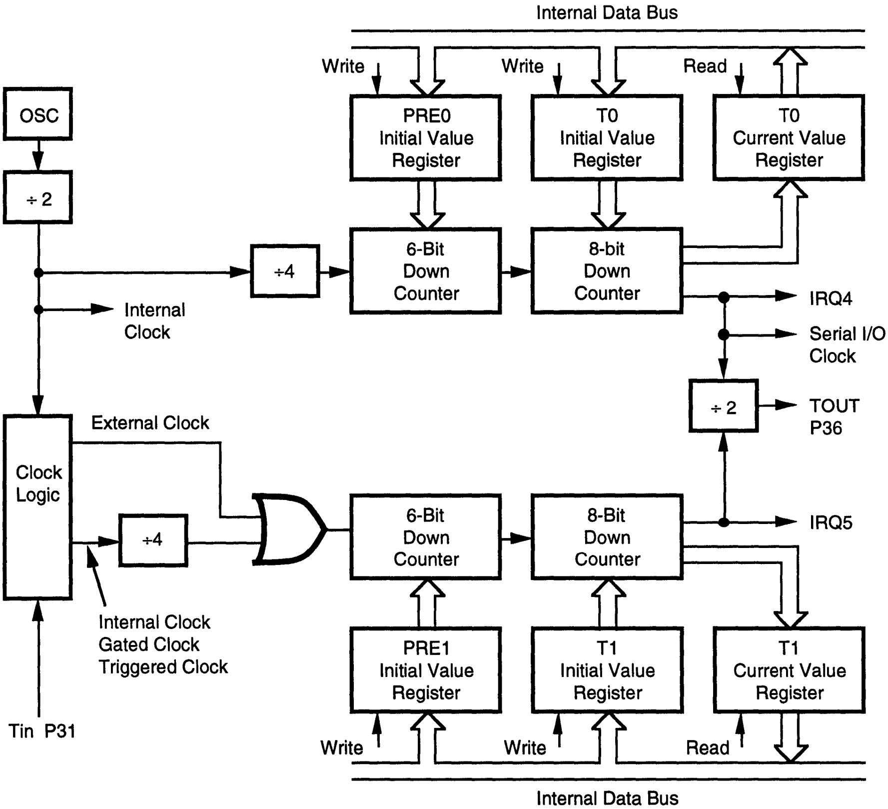


Figure 17. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E21 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 18). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (refer to Table 7).

All Z86E21 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

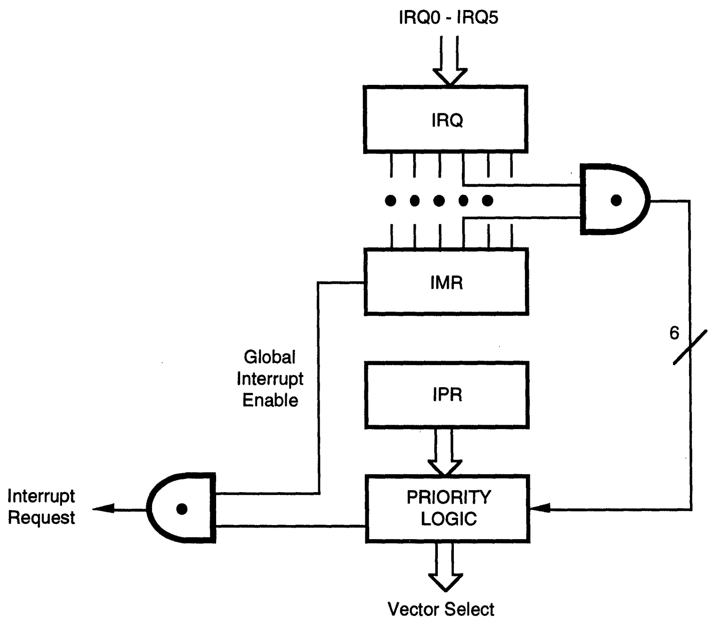


Figure 18. Interrupt Block Diagram

Clock. The Z86E21 on-chip oscillator has a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground (Figure 19). **Note:** Actual capacitor value specified by crystal manufacturer.

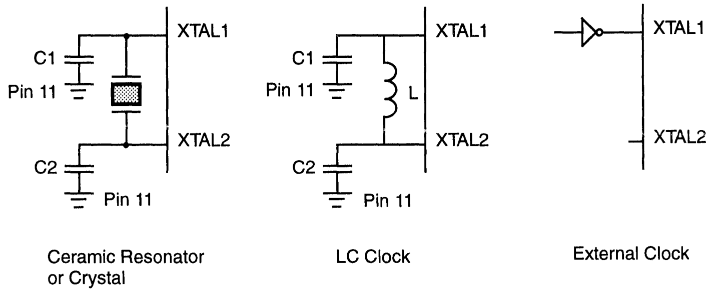


Figure 19. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = OFFH) immediately before the appropriate SLEEP instruction. i.e.,

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
    or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

PROGRAMMING

Z86E21 User Modes

The Z86E21 uses separate AC timing cycles for the different User Modes available. Table 8 shows the Z86E21 User Modes. Table 9 shows the timing of the programming waveforms.

User MODE 1 EPROM Read

The Z86E21 EPROM read cycle is provided so that the user may read the Z86E21 as a standard 2764A EPROM. This is accomplished by driving the /EPM pin (P32) to V_H and activating /CE and /OE. /PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 20.

User MODE 2 EPROM Program

The Z86E21 Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC} at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E21 programming cycle is shown in Figures 20 and 21.

PROGRAMMING (Continued)

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E21. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figure 22.

User Mode 6: 4K/8K Size Selection

The Z86E21 allows the user to select the internal ROM size. This feature is useful in that once programmed, the Z86E21 knows at which address boundary to "go external." The Z8 distinguishes internal and external fetches using the data strobe (/DS). If programmed for 4K ROM, fetch cycles include /DS beginning at location 4096 (indicating an external memory fetch). If programmed for 8K ROM, /DS remains inactive until location 8192 is reached. Once the 4K ROM size option is selected, the upper 4K of address space is unusable in the Z86E21.

The timing of the 4K/8K size selection cycle is similar to the EPROM and RAM protect cycles. Note that the 4K/8K size selection cycle requires that address 03 be indicated on the address bus during execution. Timing is shown in Figure 22.

Table 8. OTP Programming Table

Programming Modes	Device	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	All	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	All	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	All	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	All	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RAM PROTECT	E21, E22, E23	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
4K ROM SELECT	E21, E22	V_H	V_H	V_H	V_H	V_{IL}	03	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

Table 9. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

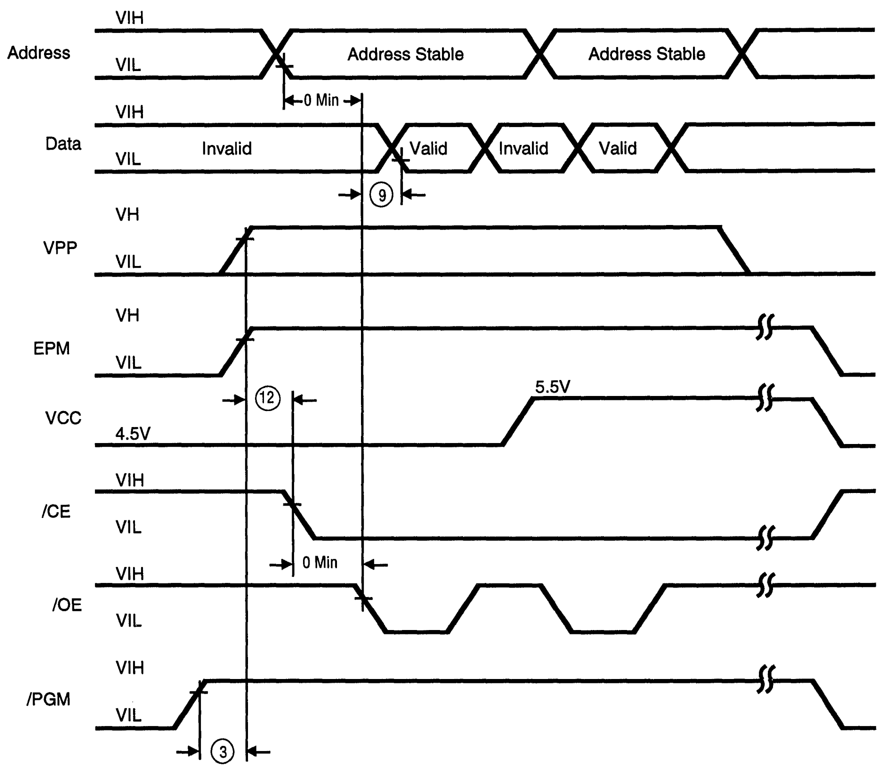


Figure 20. Programming Waveform (User Mode 1)

PROGRAMMING (Continued)

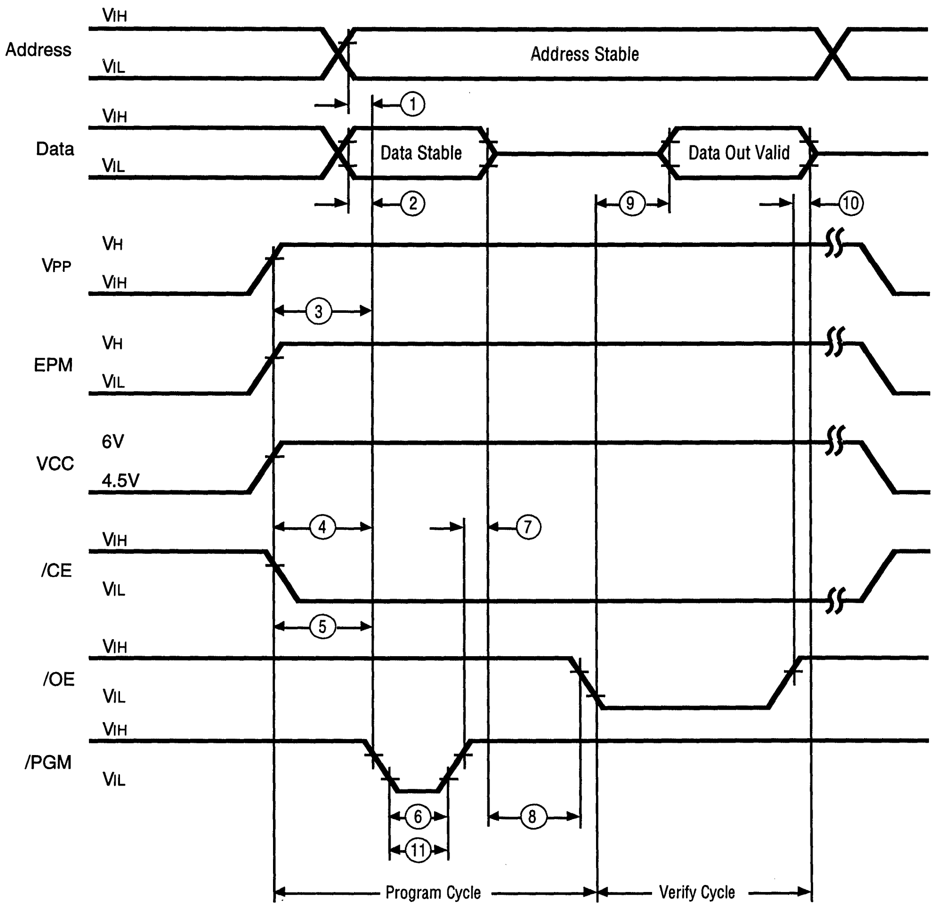


Figure 21. Programming Waveform (User Mode 2, 3)

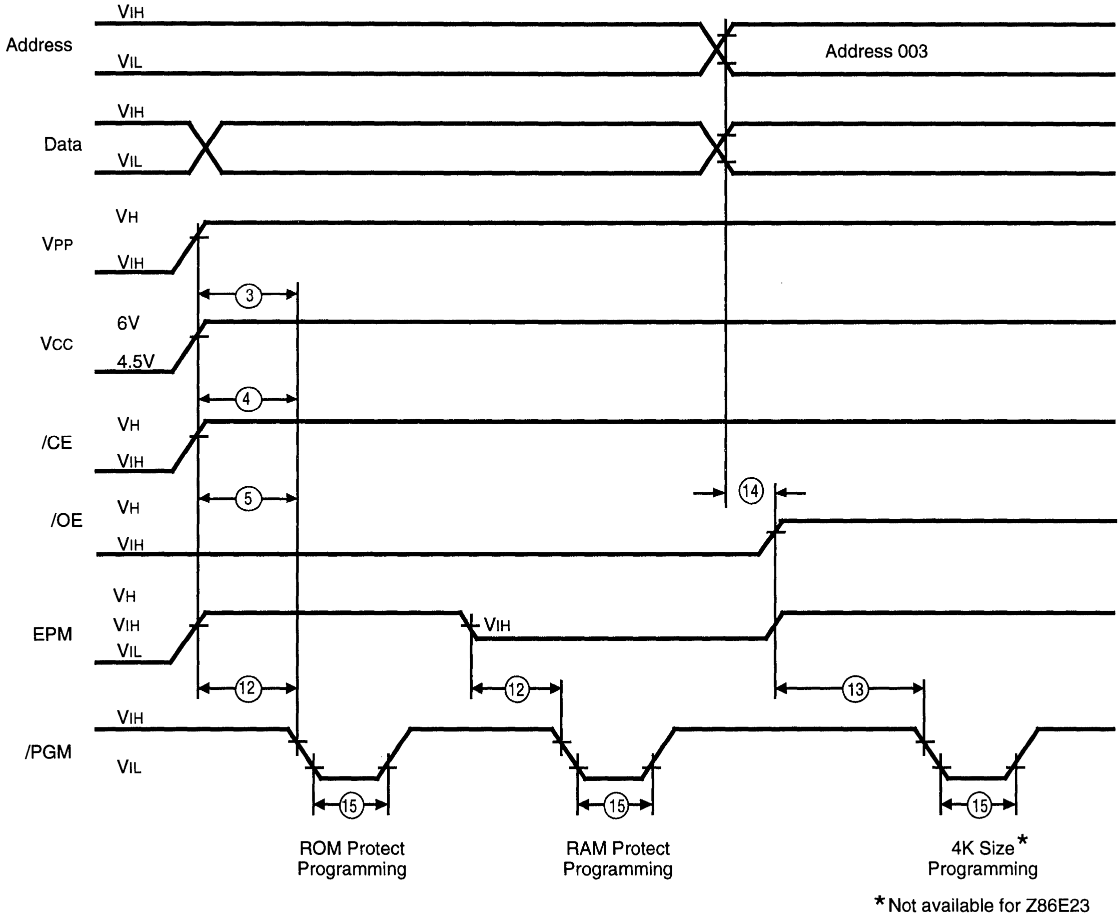


Figure 22. Programming Waveform (User Mode 4, 5, 6)

PROGRAMMING (Continued)

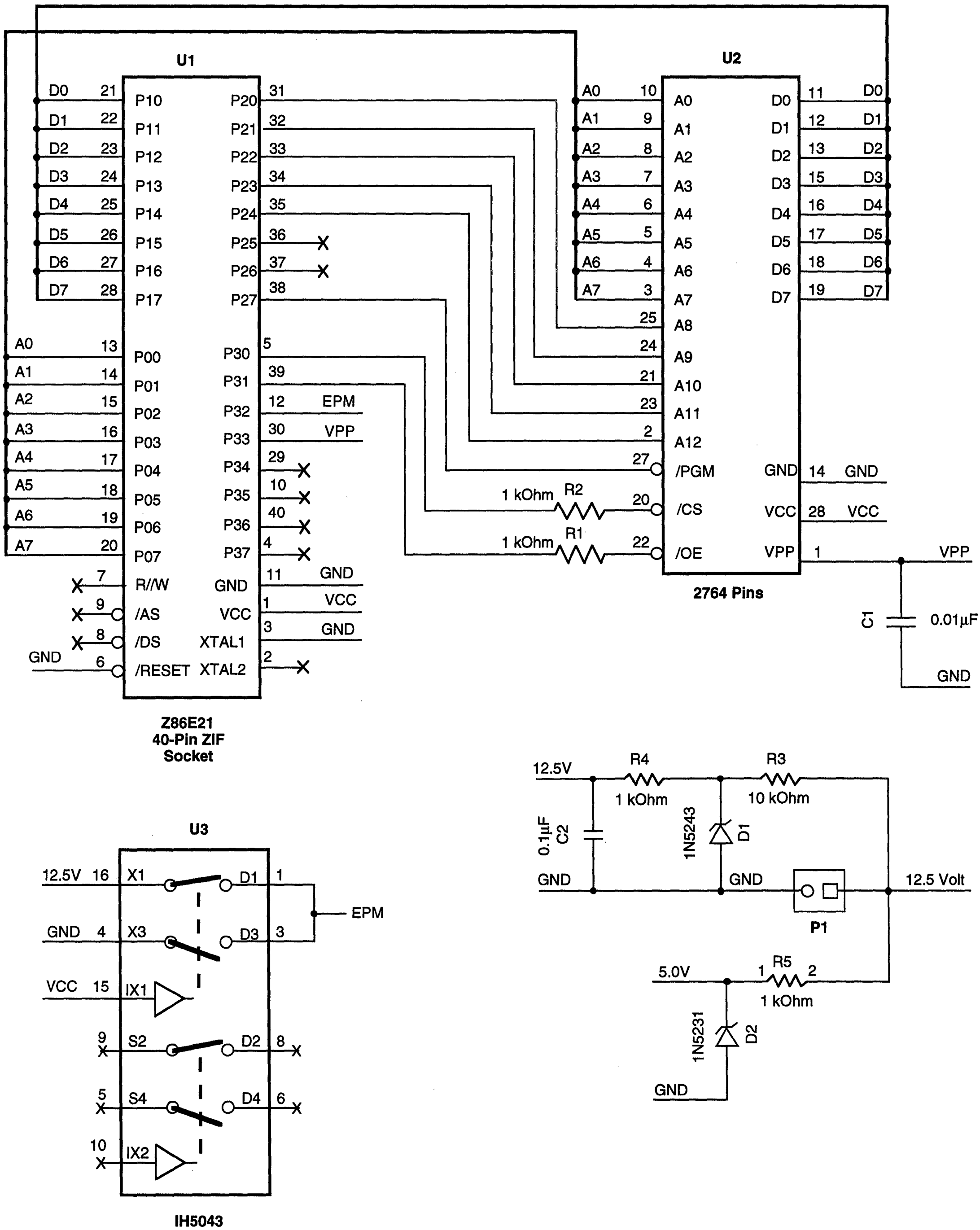


Figure 23. Z86E21 Z8 OTP Programming Adapter

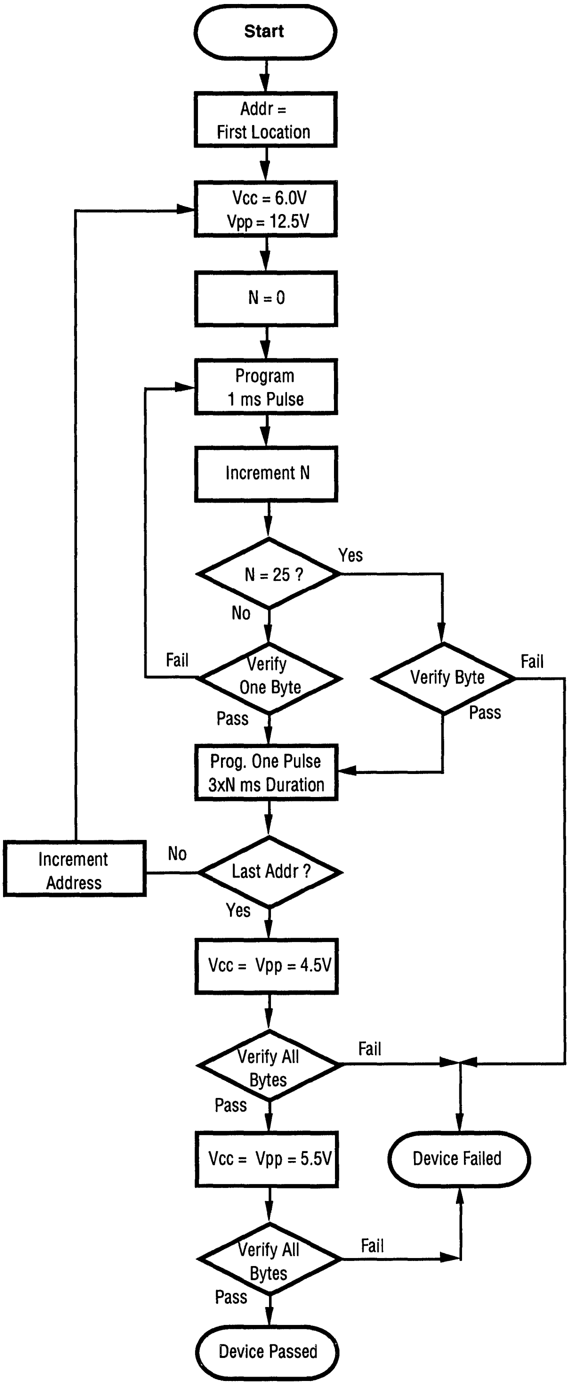


Figure 24. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+ 7.0°	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 25).

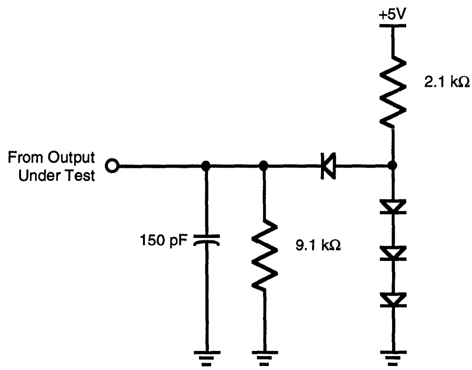


Figure 25. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to +70°C		T_A = −40°C to +105°C		Typical at 25°C	Units	Conditions
		Min	Max	Min	Max			
	Max Input Voltage		7		7		V	I_{IN} 250 µA
	Max Input Voltage		13		13		V	P33-P30 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+ 0.3	3.8	V_{CC}+ 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}+ 0.3	2.0	V_{CC}+ 0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+ 0.3	3.8	V_{CC}+ 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
I_{IL}	Input Leakage	–10	10	–10	10		µA	0V V_{IN} + 5.25V
I_{OL}	Output Leakage	–10	10	–10	10		µA	0V V_{IN} + 5.25V
I_{IR}	Reset Input Current		–50		–50		µA	V_{CC}= + 5.25V, V_{RL} = 0V
I_{CC}	Supply Current		50		50	25	mA	@ 12 MHz
			60		60	35	mA	@ 16 MHz
I_{CC1}	Standby Current		15		15	5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			20		20	10	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		20		20	5	µA	STOP Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			20		20	5	µA	STOP Mode V_{IN} = 0V, V_{CC} @ 16 MHz

Notes:
I_{CC2} requires loading TMR (%F1H) with any value prior to STOP execution.
Use this sequence:

```
LD TMR,#00
NOP
STOP
```

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

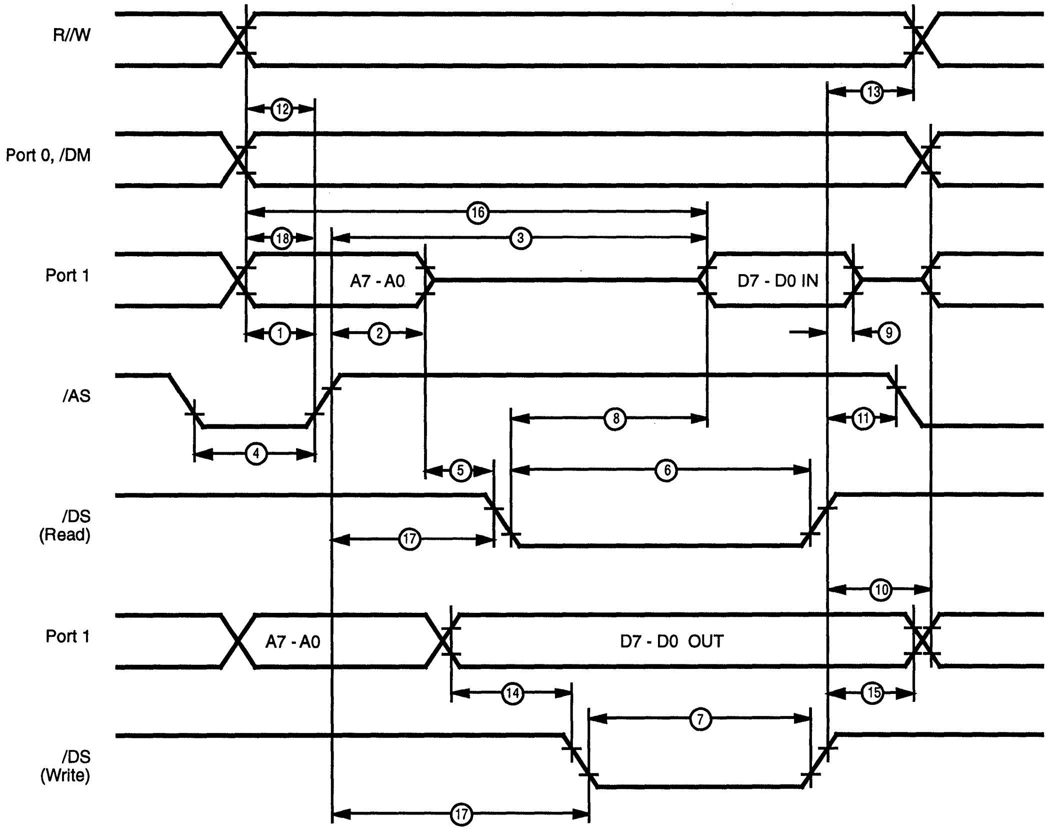


Figure 26. External I/O or Memory Read/Write Timing

7

AC CHARACTERISTICS
External I/O or Memory Read and Write Timing Table

			T_A = 0°C to +70°C				T_A = –40°C to +105°C					
			12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		45		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	35		30		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		65		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		50		30		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

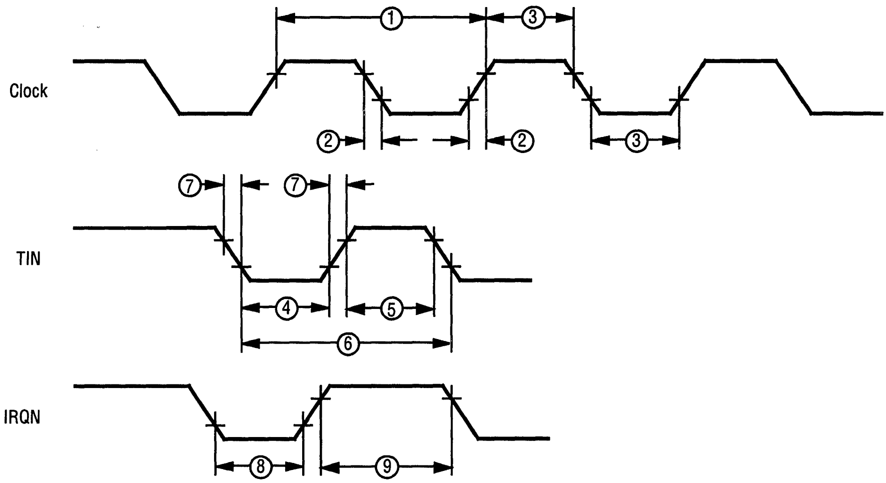


Figure 27. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	T_A = 0°C to +70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = –40°C to +105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	37		21		37		21		ns	[1]
4	TwTinL	Timer Input Low Width	75		50		75		50		ns	[2]
5	TwTinH	Timer Input High Width	5TpC		5TpC		5TpC		5TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC		5TpC		5TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

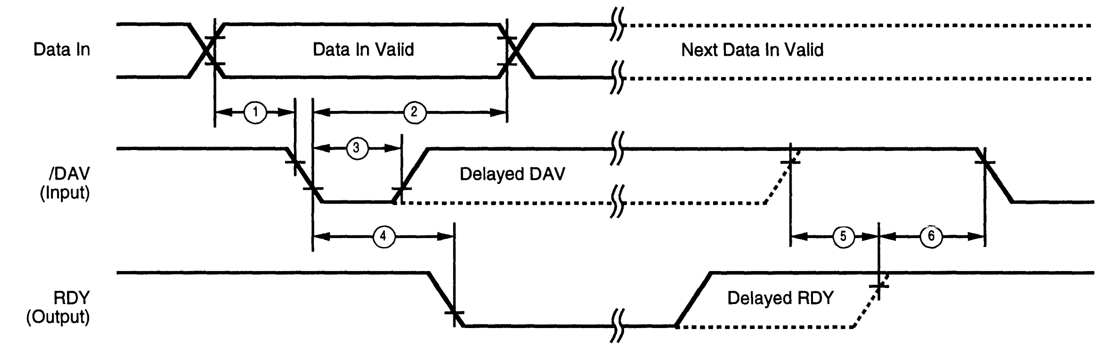


Figure 28. Input Handshake Timing

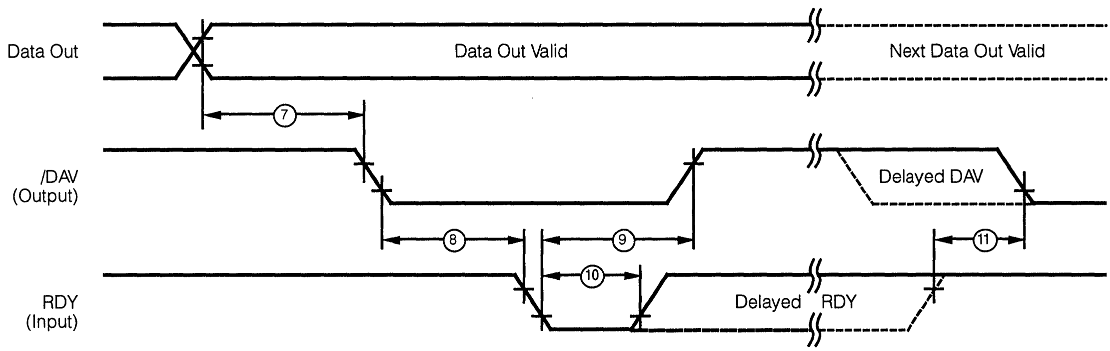


Figure 29. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

			T_A = 0°C to +70°C				T_A = –40°C to +105°C				
			12 MHz		16 MHz		12 MHz		16 MHz		Data
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Direction**
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		IN
3	TwDAV	Data Available Width	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110		110		110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

R240 SIO

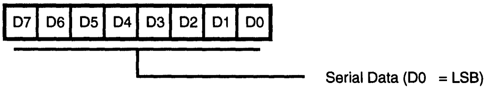


Figure 30. Serial I/O Register (F0H: Read/Write)

R241 TMR

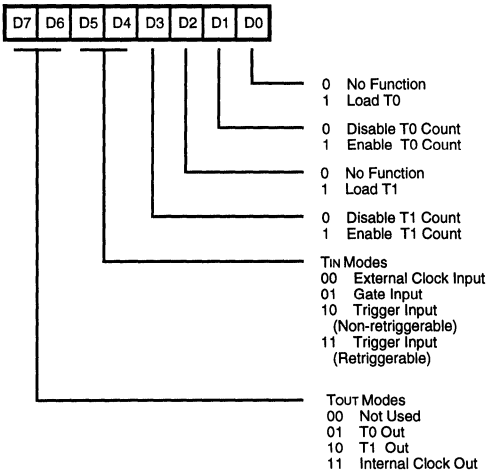


Figure 31. Timer Mode Register (F1H: Read/Write)

R242 T1

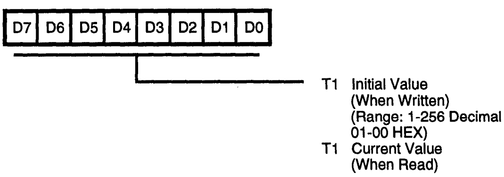


Figure 32. Counter/Timer 1 Register (F2H: Read/Write)

R243 PRE1

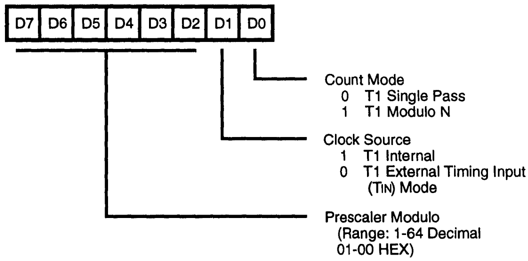


Figure 33. Prescaler 1 Register (F3H: Write Only)

R244 T0

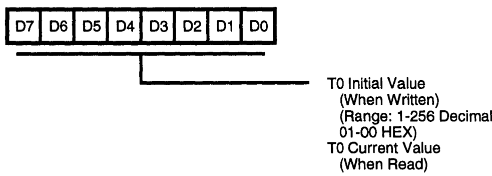


Figure 34. Counter/Timer 0 Register (F4H: Read/Write)

R245 PRE0

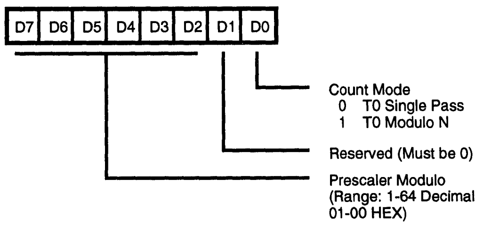


Figure 35. Prescaler 0 Register (F5H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

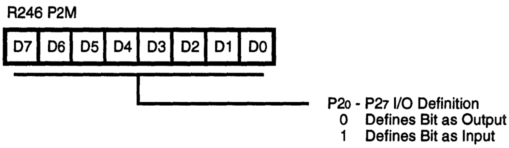


Figure 36. Port 2 Mode Register (F6H: Write Only)

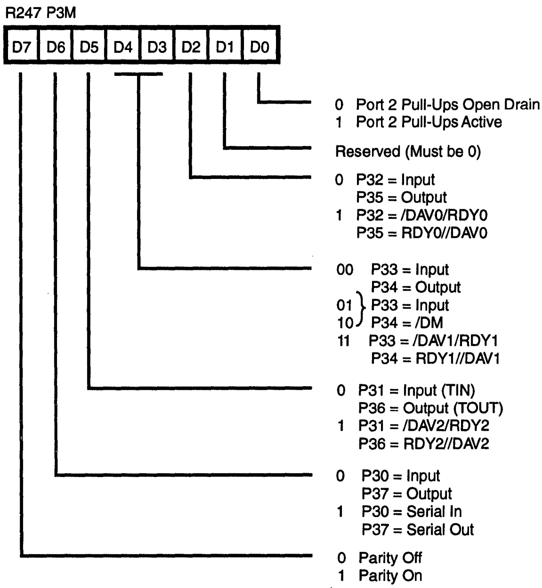


Figure 37. Port 3 Mode Register (F7H: Write Only)

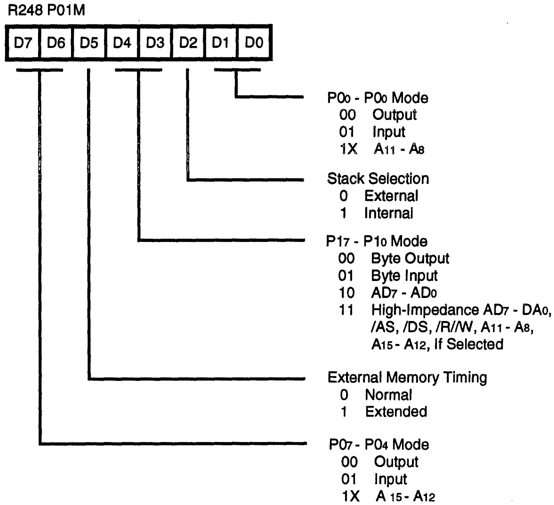


Figure 38. Port 0 and 1 Mode Register (F8H: Write Only)

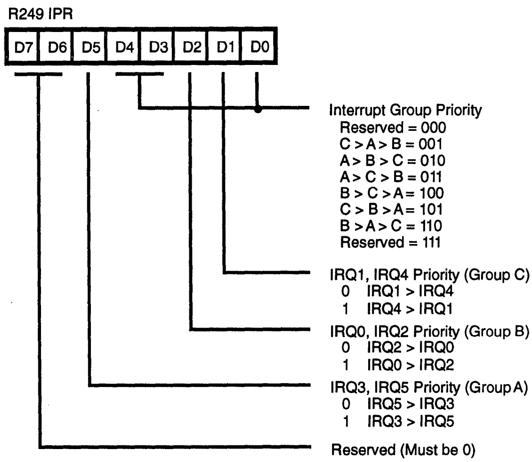


Figure 39. Interrupt Priority Register (F9H: Write Only)

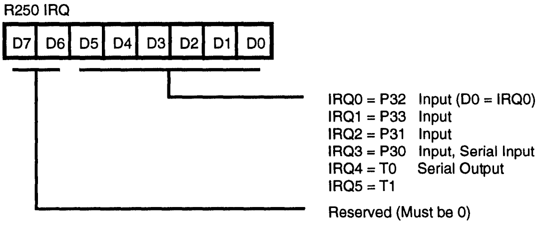


Figure 40. Interrupt Request Register (FAH: Read/Write)

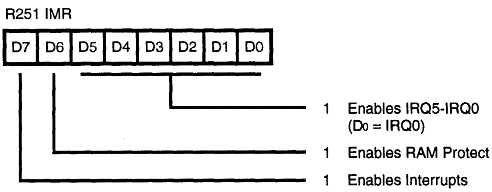


Figure 41. Interrupt Mask Register (FBH: Read/Write)

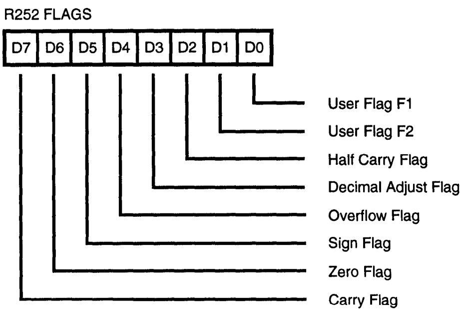


Figure 42. Flag Register (FCH: Read/Write)

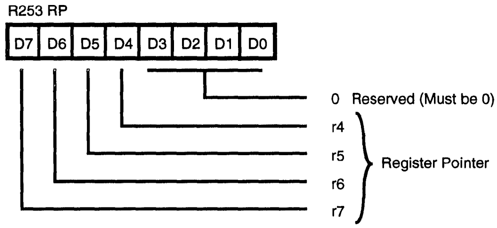


Figure 43. Register Pointer Register (FDH: Read/Write)

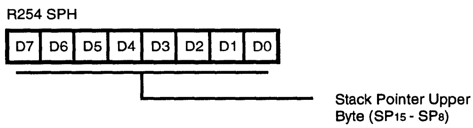


Figure 44. Stack Pointer Register (FEH: Read/Write)

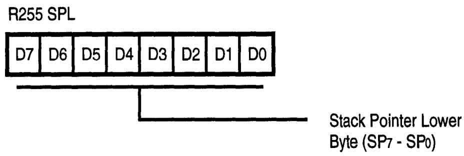


Figure 45. Stack Pointer Register (FFH: Read/Write)

DC CHARACTERISTICS

Supply Current

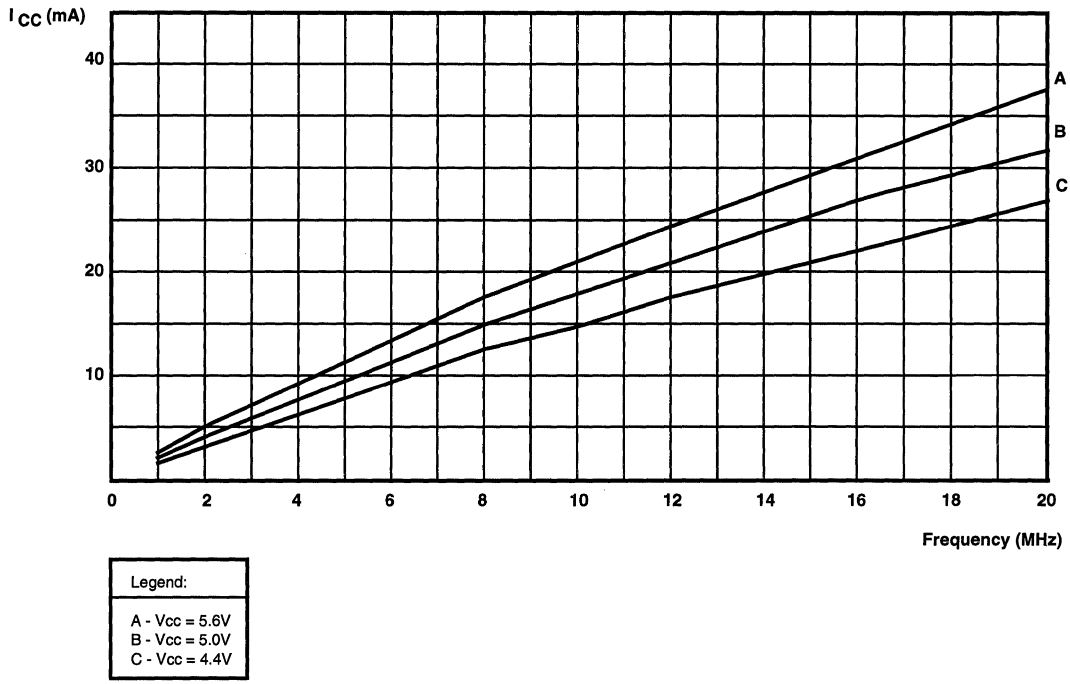


Figure 46. Typical I_{cc} vs Frequency

DC CHARACTERISTICS
Standby Current

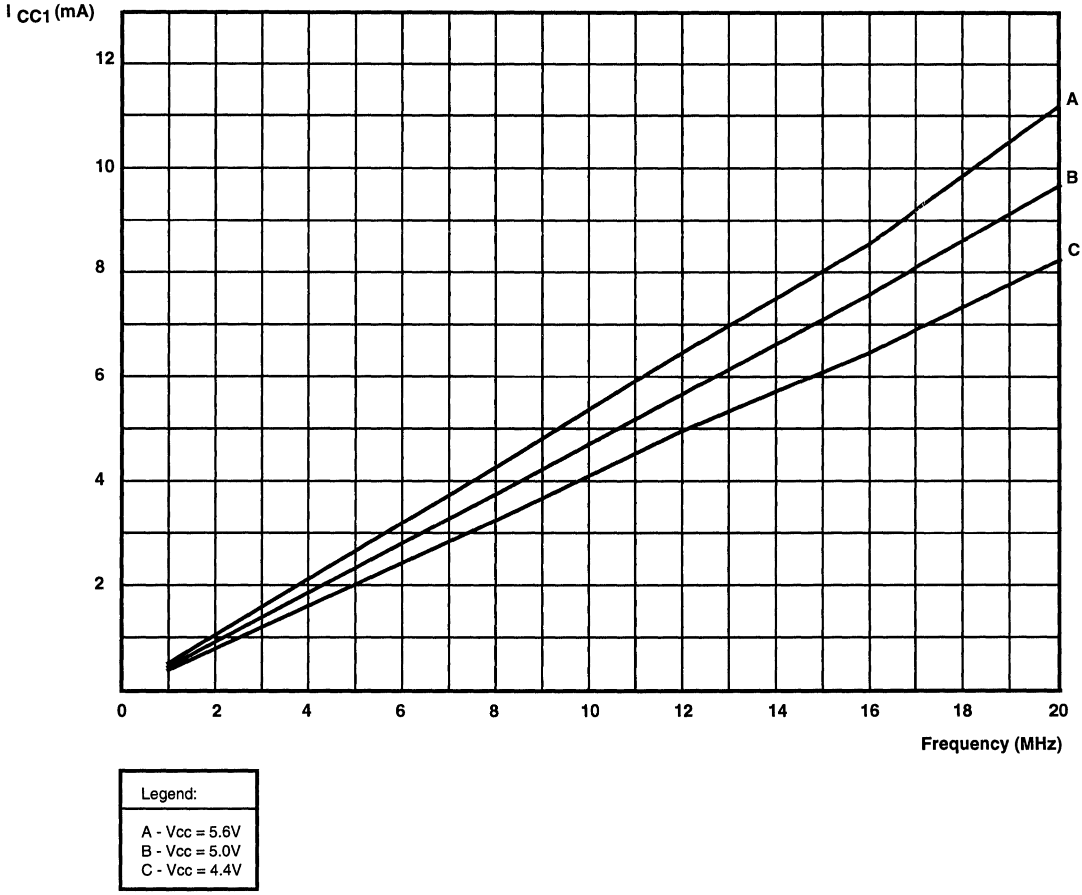


Figure 47. Typical I_{CC1} vs Frequency

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working register pair address
Irr	Indirect working register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working register address
r	Working register address only
IR	Indirect register or indirect working register address
Ir	Indirect working register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition Code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag Register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt Mask Register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

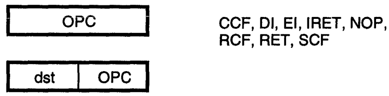
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

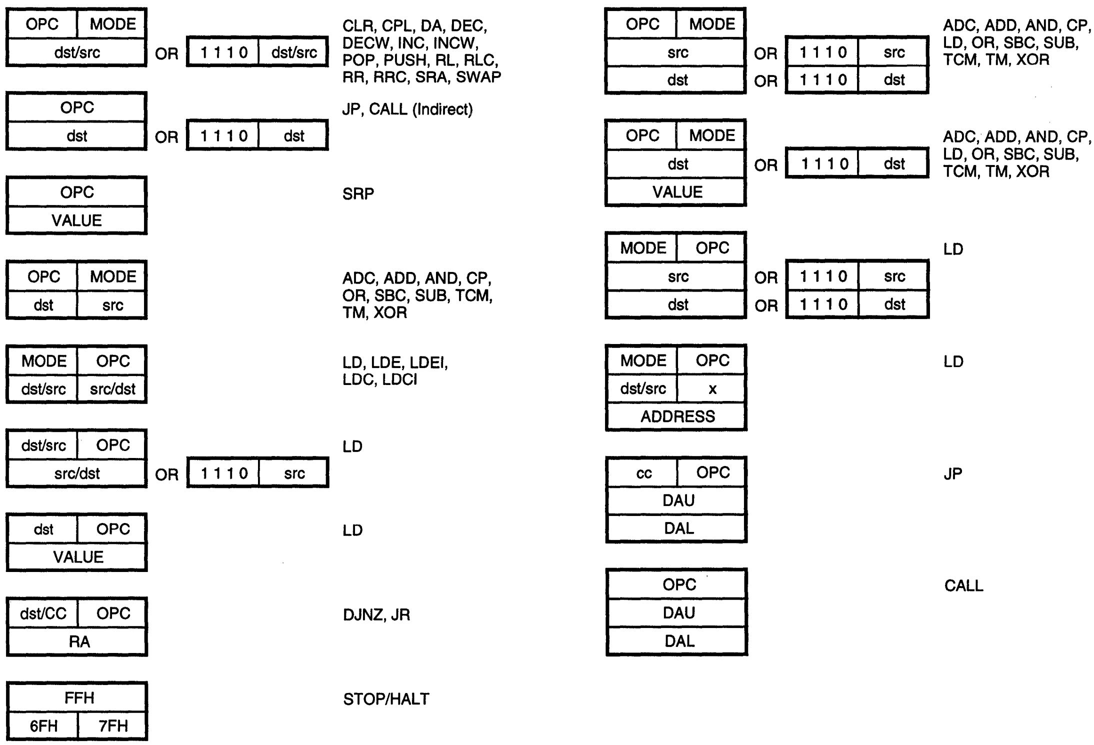
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions **Three-Byte Instructions**

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

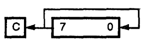
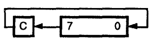
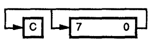
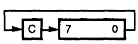
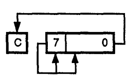
refers to bit 7 of the destination operand.

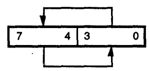
INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP − 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst − src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst − 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst − 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r − 1 if r ≠ 0 PC←PC + dst Range: +127, −128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 − F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR iR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 − F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, −128	RA		cB c = 0 − F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 − F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP		FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†	4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR	50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR	70 71	-	-	-	-	-	-
RCF C←0		CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2		AF	-	-	-	-	-	-
RL dst 	R IR	90 91	*	*	*	*	-	-
RLC dst 	R IR	10 11	*	*	*	*	-	-
RR dst 	R IR	E0 E1	*	*	*	*	-	-
RRC dst 	R IR	C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†	3[ ]	*	*	*	*	1	*
SCF C←1		DF	1	-	-	-	-	-
SRA dst 	R IR	D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	C	Z	S	V	D	H
STOP		6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†	2[ ]	[	[	[	[	1	[
SWAP dst 	R IR	F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†	6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†	7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†	B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

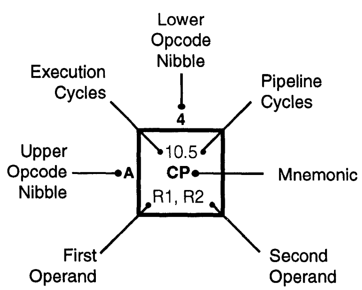
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down.

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1



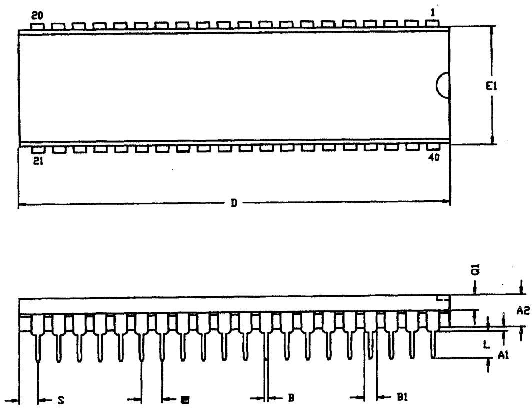
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

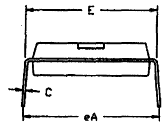
Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

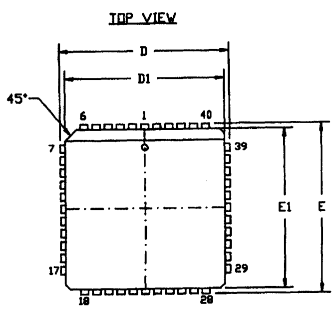


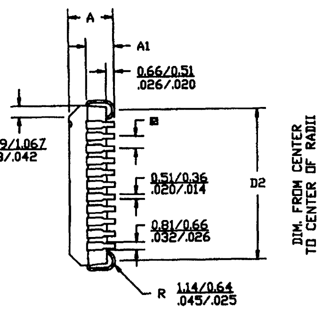


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



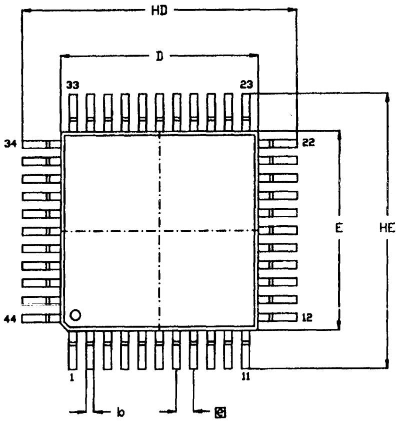


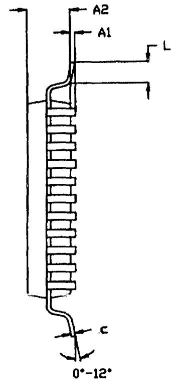
NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram





NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86E21

12 MHz

40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86E2112PSC	Z86E2112VSC	Z86E2112FSC

16 MHz

40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86E2116PSC	Z86E2116VSC	Z86E2116FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Temperature
S = 0°C to +70°C

Speed
12 = 12 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:
Z 86E21 12 P S C is an Z86E21, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E21 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller 7

Z86C61/62/96 CMOS Z8®
Microcontroller 8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
ROMless Microcontroller 10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller 11

Support Products 12

Superintegration™
Products Guide S

Zilog's Literature Guide
Ordering Information L

Z86C61/62/96
CMOS Z8®
MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, 64-Pin DIP, or 68-Pin PLCC Package
- 32 Input/Output Lines (Z86C61 Only)
- 52 Input/Output Lines (Z86C62 and Z86C96)
- 3.0V to 5.5V Operating Range
- Low Power Consumption - 200 mW (max)
- Fast Instruction Pointer - 0.75 µs @ 16 MHz
- Two Standby Modes - STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- 16 Kbytes of ROM
- 256 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 16 and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86C61/62/96 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C61/62 is a member of the Z8 single-chip microcontroller family with 16 Kbytes of ROM and 256 bytes of RAM. The Z86C96 is the ROMless version.

The Z86C61 is housed in a 40-pin DIP, and a 44-pin PLCC package, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin version only. The Z86C62/96 is housed in a 64-pin DIP, and a 68-pin PLCC. Both versions of the Z86C62 have the ROMless pin option, which allows both external memory and preprogrammed ROM, enabling this Z8 microcontroller to be used in high-volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C61/62/96 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C61 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C62/96 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C61/62/96 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (Figures 1, 2, and 3).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

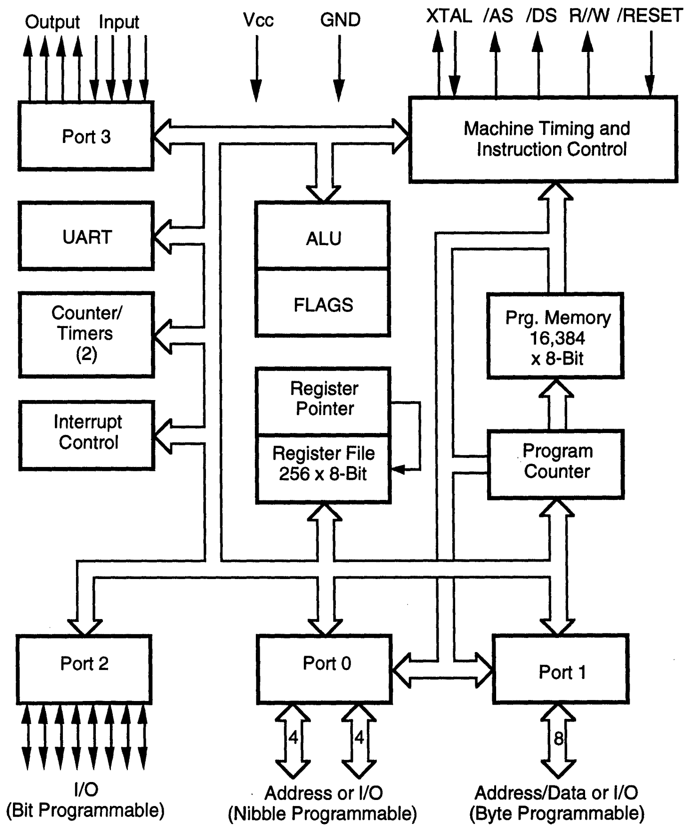


Figure 1. Z86C61 Functional Block Diagram

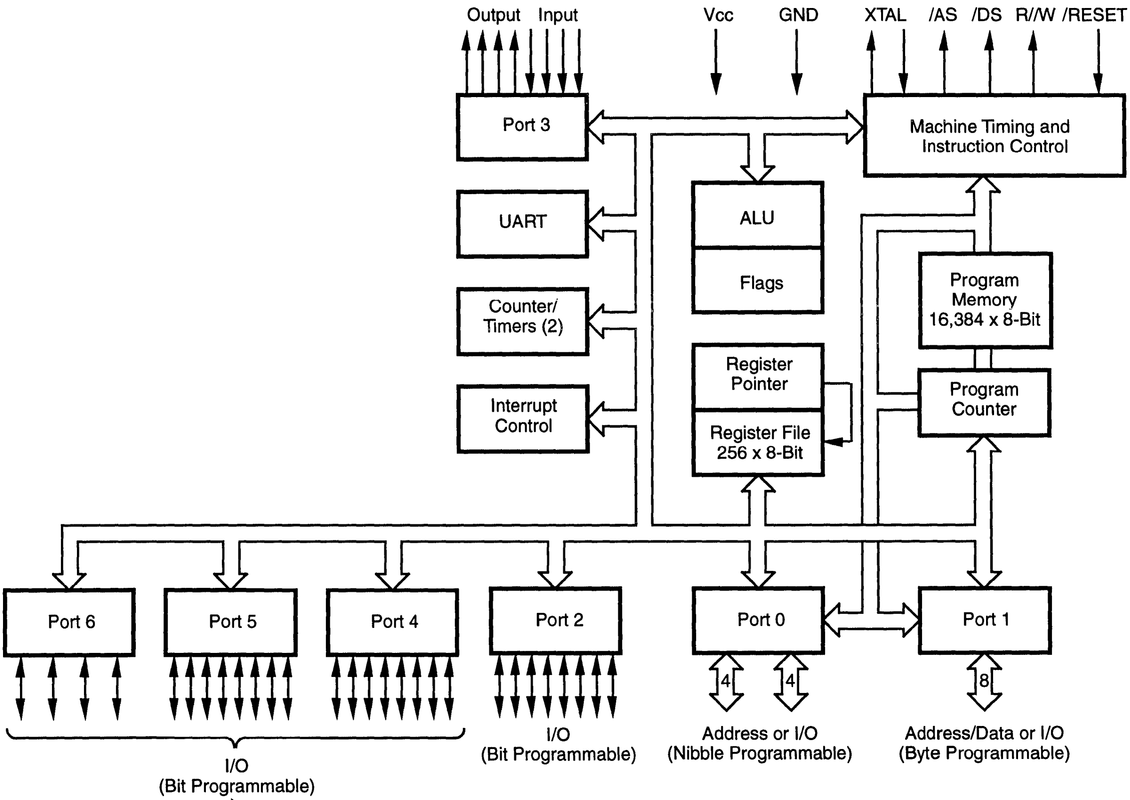


Figure 2. Z86C62 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

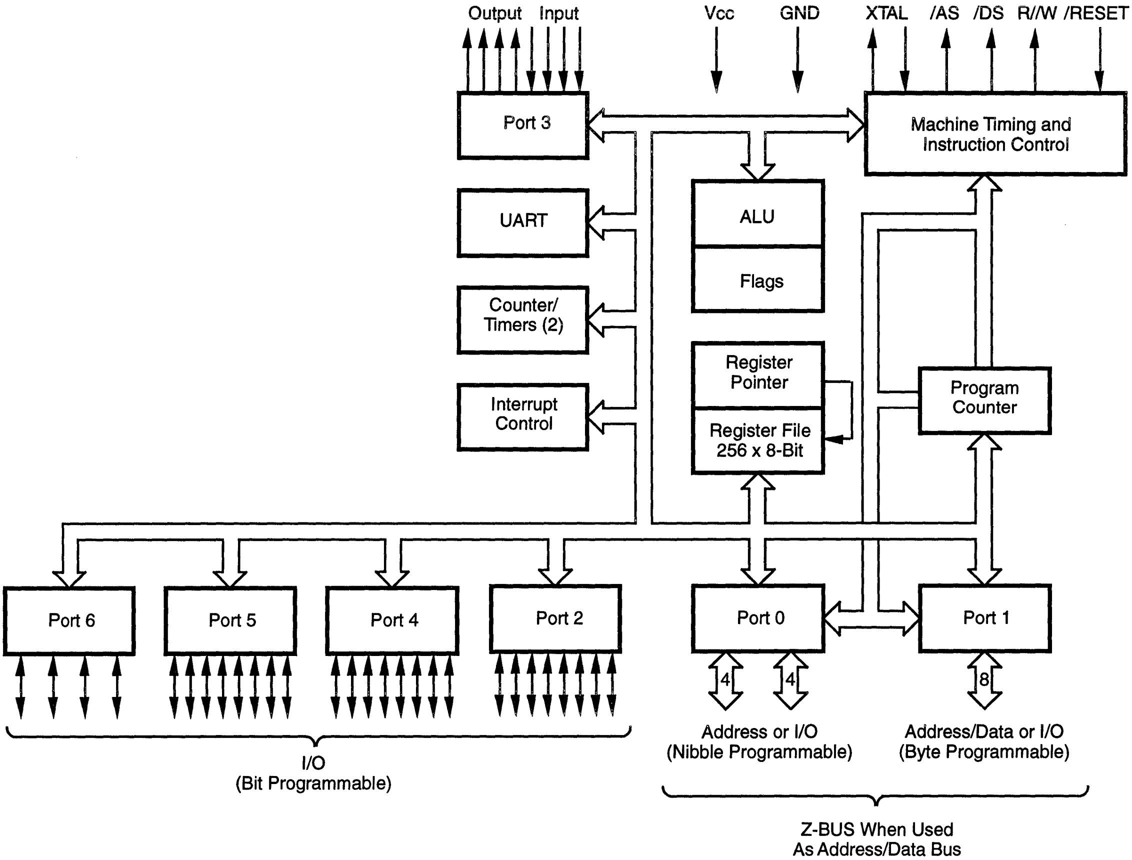


Figure 3. Z86C96 Functional Block Diagram

PIN DESCRIPTION

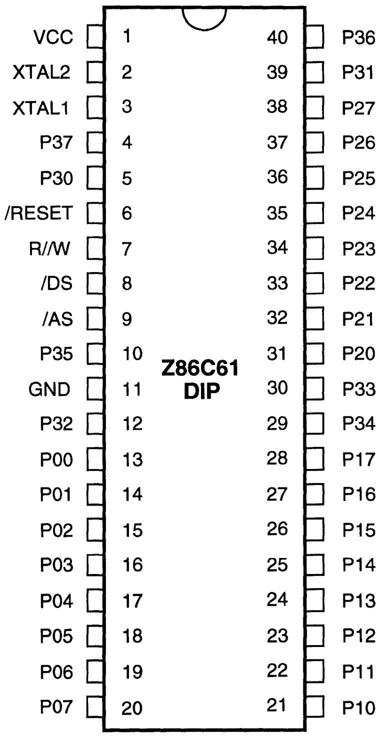


Figure 4. Z86C61 40-Pin DIP Pin Assignments

Table 1. Z86C61 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

PIN DESCRIPTION (Continued)

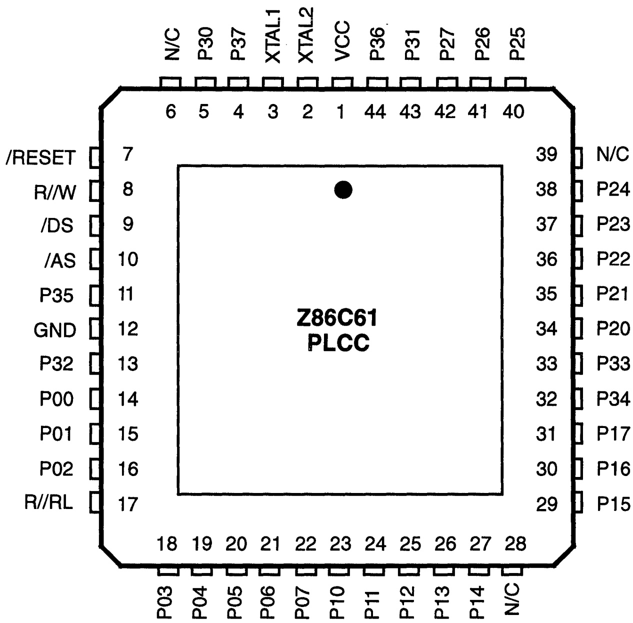


Figure 5. Z86C61 44-Pin PLCC Pin Assignments

Table 2. Z86C61 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
17	R//RL	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
39	N/C	Not Connected	Input
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

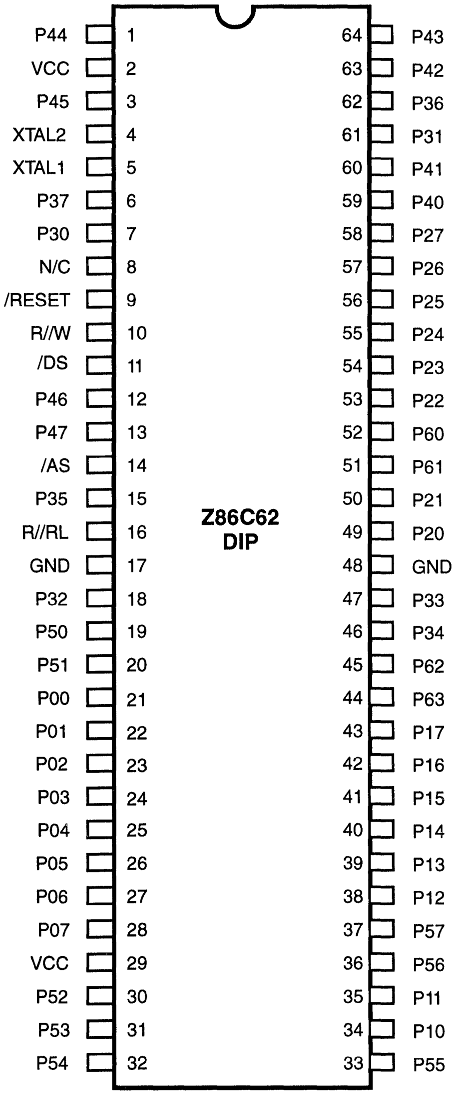


Figure 6. Z86C62 64-Pin DIP Pin Assignments

Table 3. Z86C62 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R//RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

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PIN DESCRIPTION (Continued)

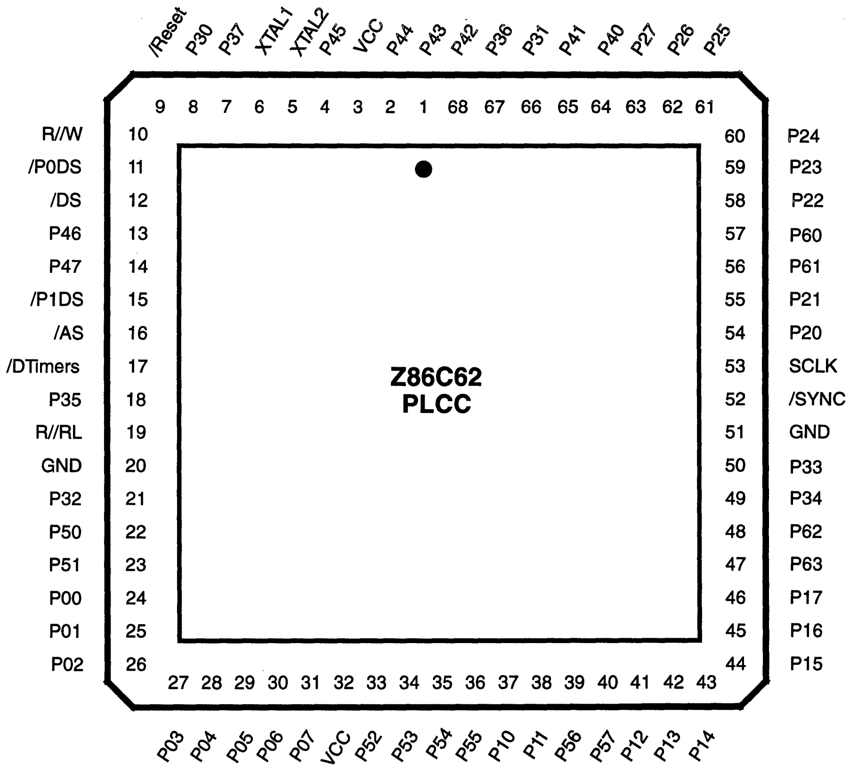

Figure 7. Z86C62 68-Pin PLCC Pin Assignments

Table 4. Z86C62 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	V_{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	R//RL	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
32	V_{CC}	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

PIN DESCRIPTION (Continued)

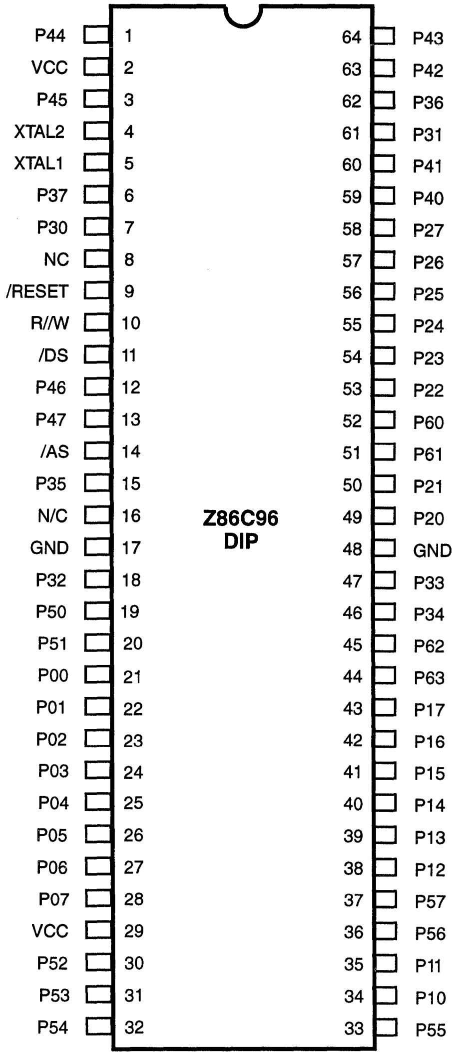

Figure 8. Z86C96 64-Pin DIP Pin Assignments

Table 5. Z86C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pins 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	N/C	Not Connected	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pins 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P55-P52	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P56-P57	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

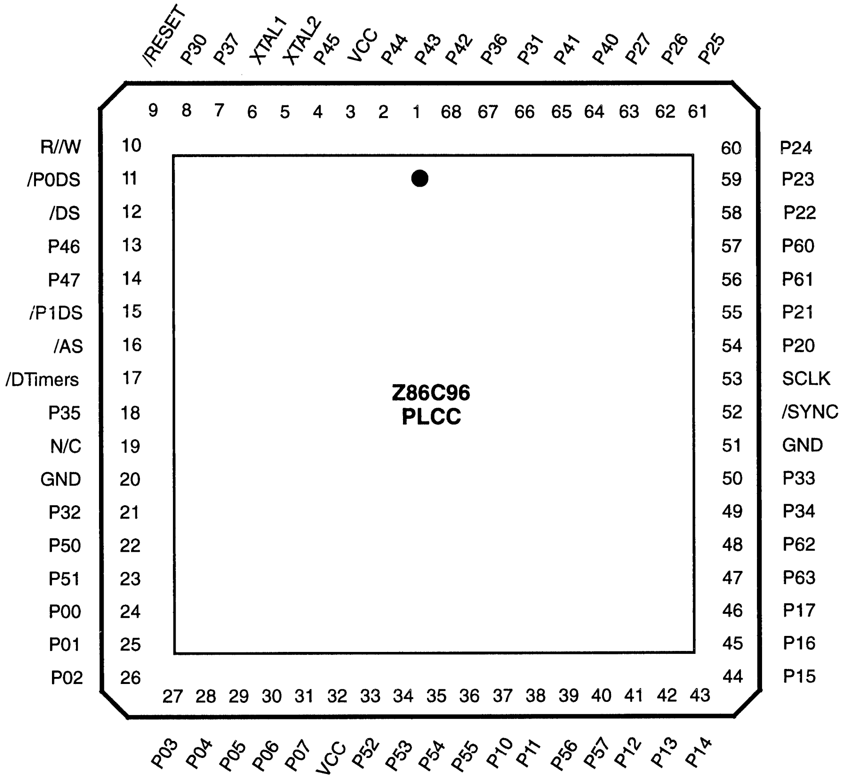

Figure 9. Z86C96 68-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 6. Z86C96 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output	24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
3	V_{CC}	Power Supply	Input	32	V_{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output	33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output	37-38	P11-P10	Port 1, Pins 0,1	In/Output
6	XTAL1	Crystal, Oscillator Clock	Input	39-40	P57-P56	Port 5, Pins 6,7	In/Output
7	P37	Port 3, Pin 7	Output	41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
8	P30	Port 3, Pin 0	Input	47-48	P63-P62	Port 6, Pins 3,2	In/Output
9	/RESET	Reset	Input	49	P34	Port 3, Pin 4	Output
10	R//W	Read/Write	Output	50	P33	Port 3, Pin 3	Input
11	/P0DS	Port 0 Data Strobe	Output	51	GND	Ground	Input
12	/DS	Data Strobe	Output	52	/SYNC	Synchronization	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output	53	SCLK	System Clock	Output
15	/P1DS	Port 1 Data Strobe	Output	54-55	P21-P20	Port 2, Pins 0,1	In/Output
16	/AS	Address Strobe	Output	56-57	P61-P60	Port 6, Pins1,0	In/Output
17	/DTIMER	Disable Timers	Input	58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
18	P35	Port 3, Pin 5	Output	64-65	P41-P40	Port 4, Pins 0,1	In/Output
19	N/C	Not Connected	Input	66	P31	Port 3, Pin 1	Input
20	GND	Ground	Input	67	P36	Port 3, Pin 6	Output
21	P32	Port 3, Pin 2	Input	68	P42	Port 4, Pin 2	In/Output
22-23	P51-P50	Port 5, Pins 0,1	In/Output				

PIN FUNCTIONS

R//RL (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (**Note:** when left unconnected or pulled High to V_{CC} the part functions as a normal Z86C61/62 ROM version.) This pin is only available on the 44-pin version of the Z86C61, and both versions of the Z86C62.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C61/62/96 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

/P0DS *Port 0 Data Strobe* (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

/P1DS *Port 1 Data Strobe* (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

/DTIMERS *Disable Timers* (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

SCLK (output). System clock pin.

/SYNC *Instruction SYNC Signal* (output, active Low). This signal indicates the last clock of the current executing instruction.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 10).

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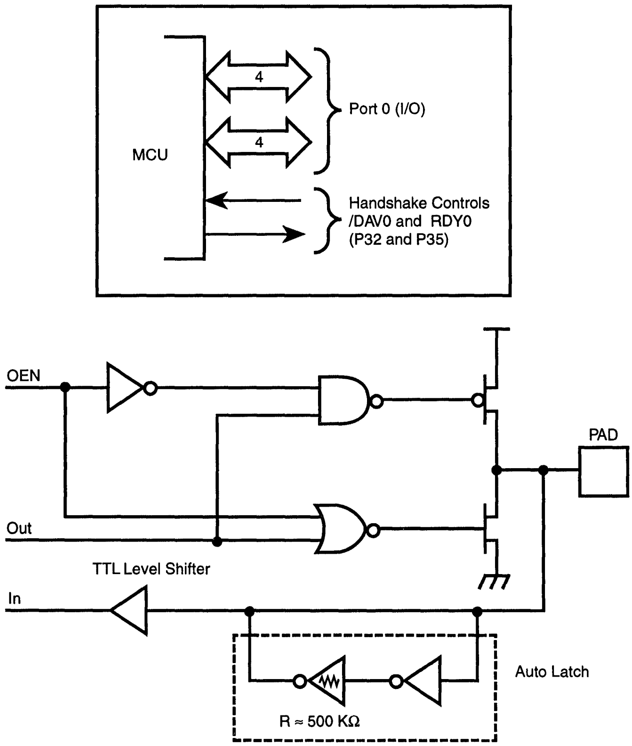

Figure 10. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C61/62/96, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 16,384 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the microcontroller to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 11).

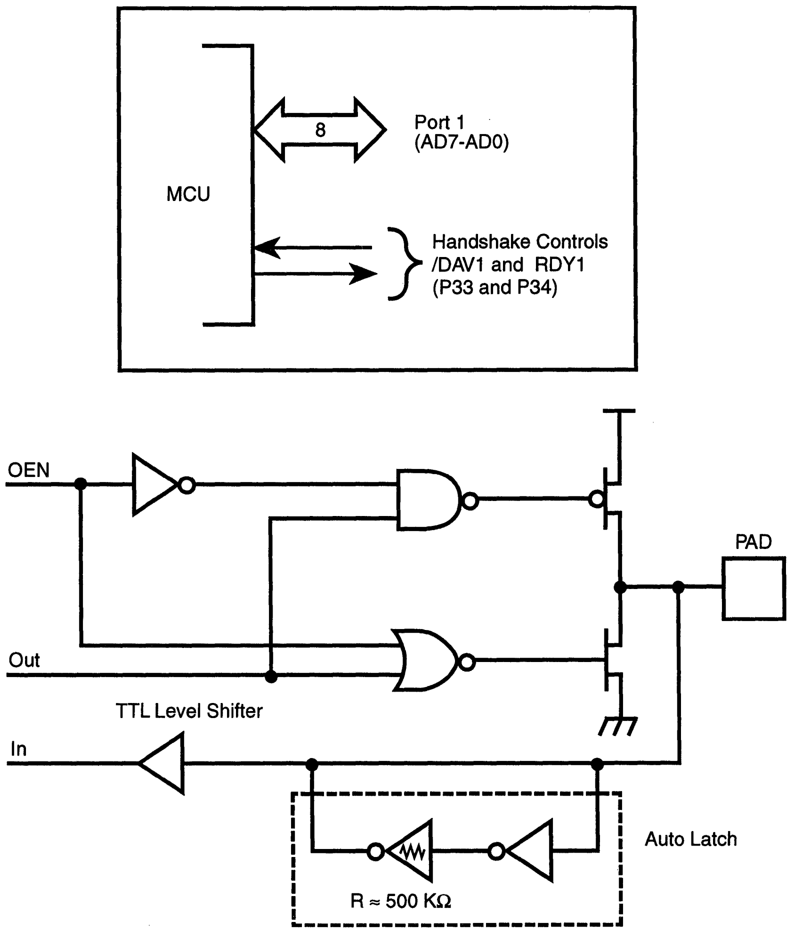

Figure 11. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 12).

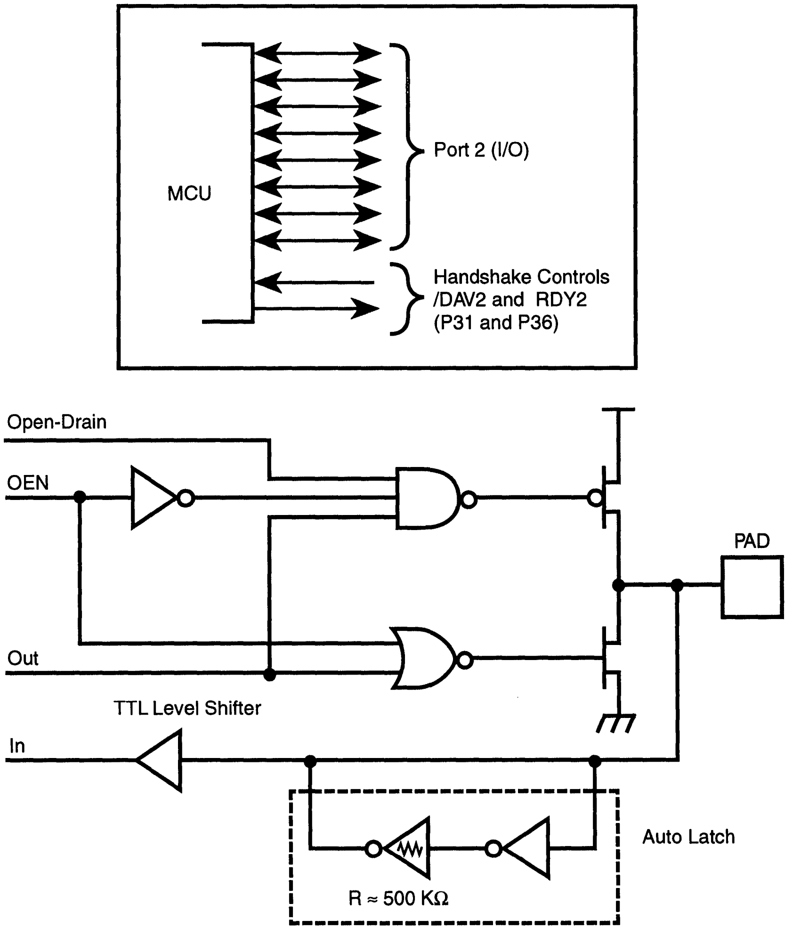

Figure 12. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 13).

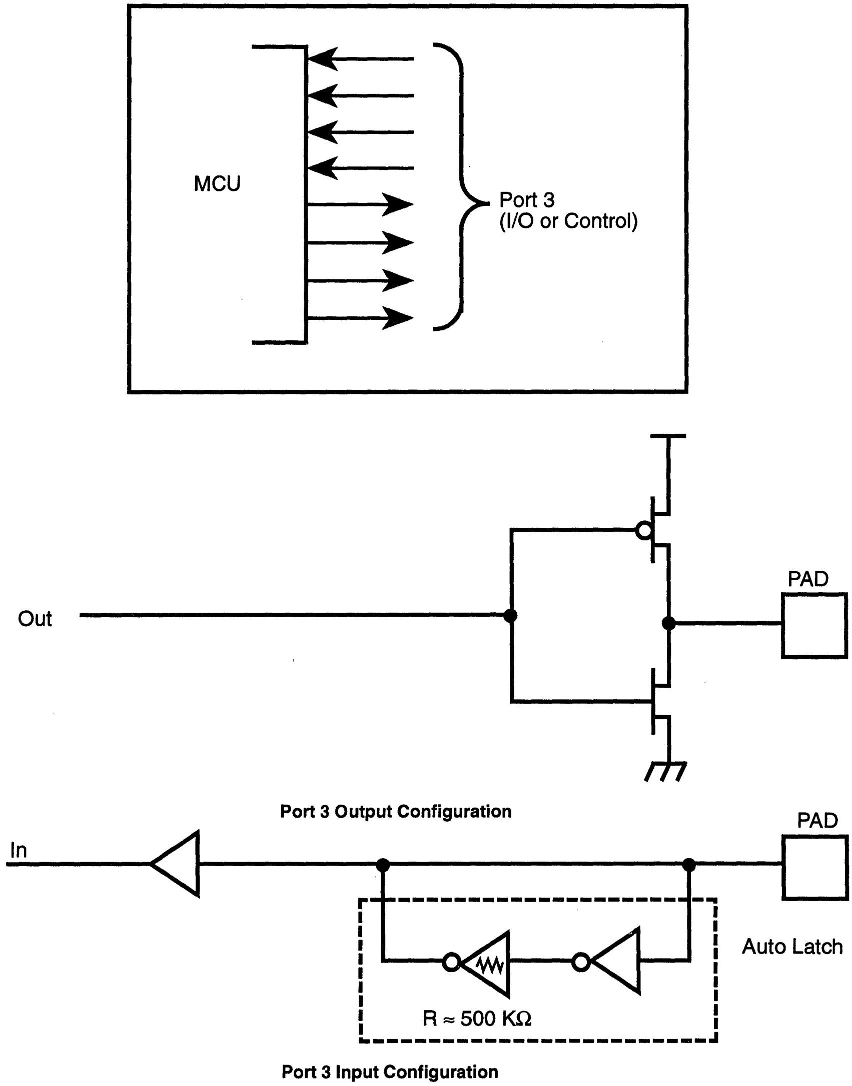

Figure 13. Port 3 Configuration

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Table 7. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

UART OPERATION

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/ transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C61/62/96 automatically adds a start bit and two stop bits to transmitted data (Figure 14). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Note: UART function is only available in stardard timing mode (i.e., P01M D5 = 0).

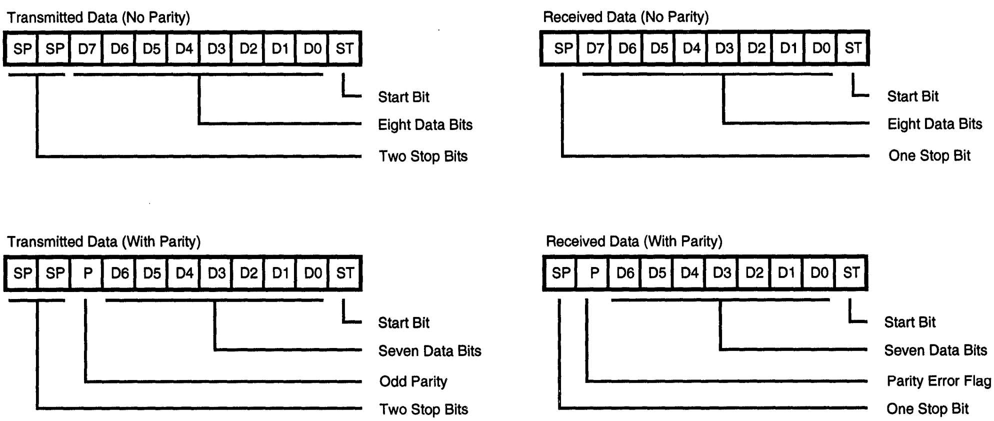

Figure 14. Serial Data Formats

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 15). Port address (F)02.

Port 5 (P57-P50). Same as Port 4. Port address (F)04.

Port 6 (P63-P60). Same as Port 4. (**Note:** this is a 4-bit port, bits D3-D0.) Port address (F)07.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

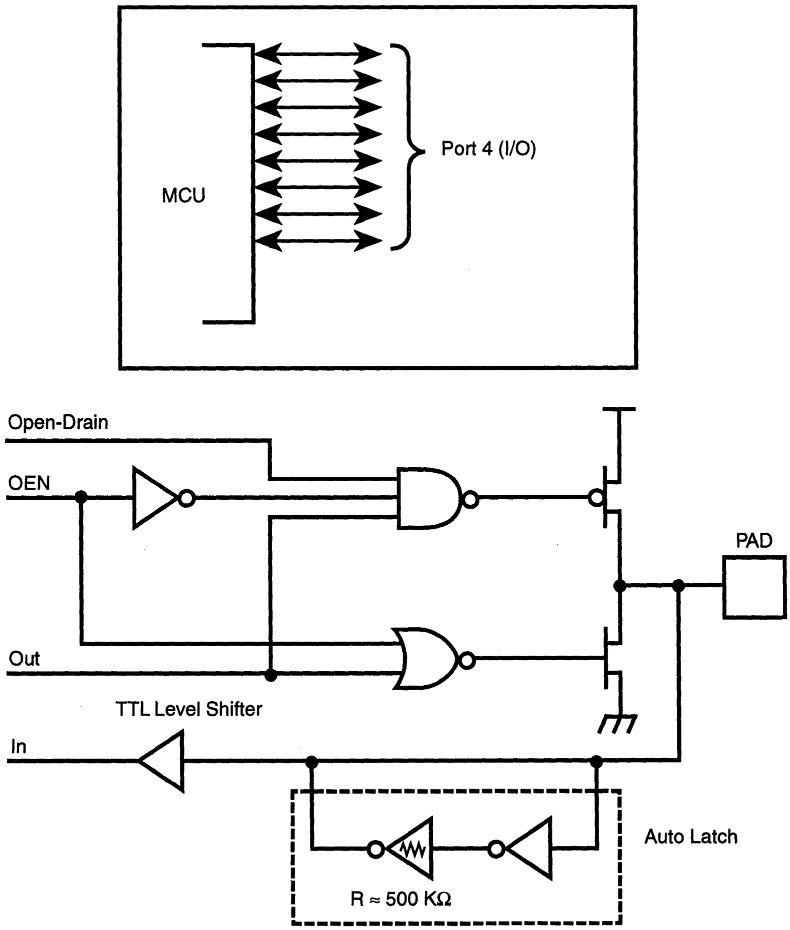

Figure 15. Port 4 Configuration

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C61/62 can address up to 48 Kbytes of external program memory (Figure 16). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 16383 consists of on-chip ROM. At addresses 16384 and greater, the Z86C61/62 executes external program memory fetches. The Z86C96, and the Z86C61/62 in ROMless mode, can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory (/DM). The ROM version can address up to 48 Kbytes of external data memory space beginning at location 16384. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 17). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

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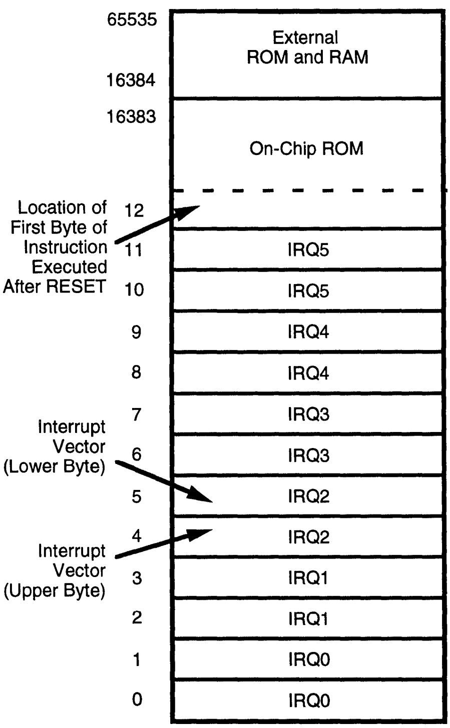


Figure 16. Program Memory Configuration

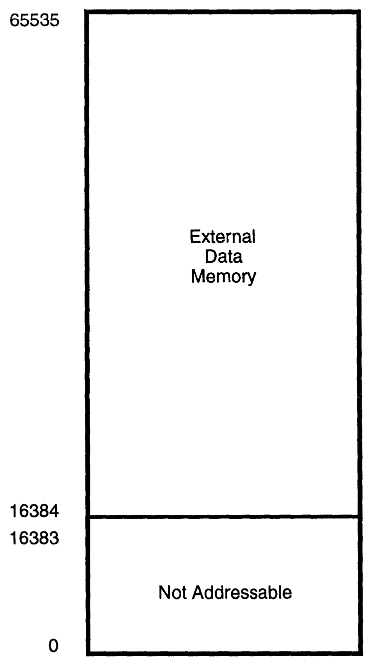


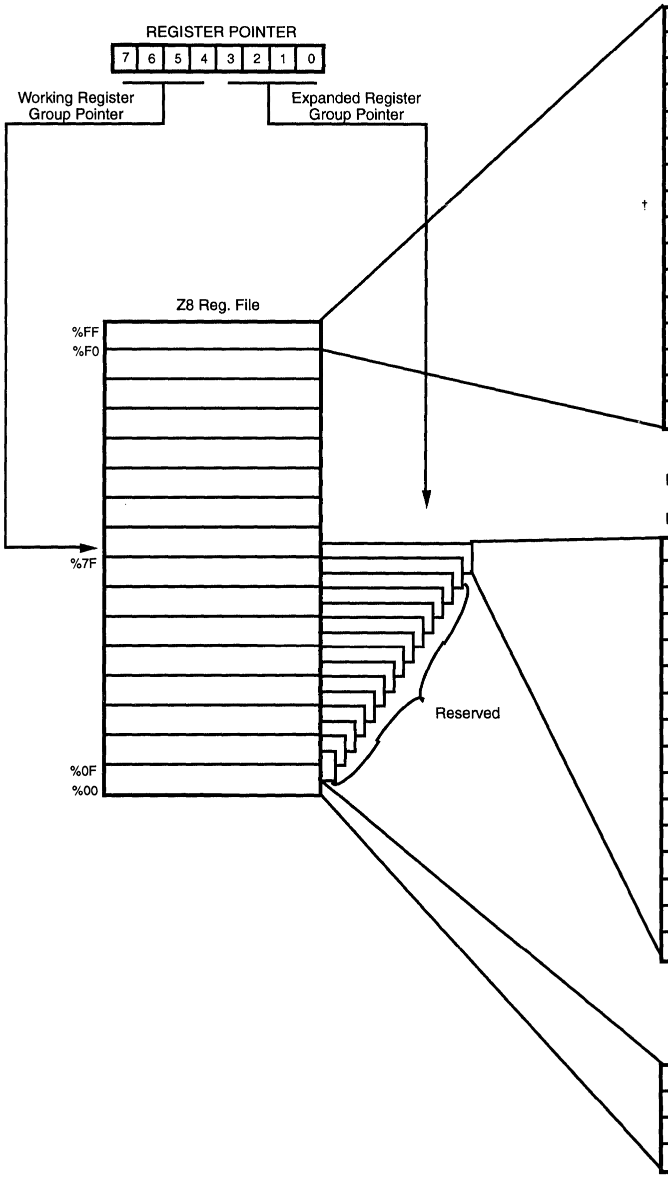
Figure 17. Data Memory Configuration

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 19).

Location		Identifiers
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239 … R4	General-Purpose Registers	
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 18. Register File



Z8 STANDARD CONTROL REGISTERS

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% FF	SPL	U	U	U	U	U	U	U	U
% FE	SPH	U	U	U	U	U	U	U	U
% FD	RP	0	0	0	0	0	0	0	0
% FC	FLAGS	U	U	U	U	U	U	U	U
% FB	IMR	0	U	U	U	U	U	U	U
% FA	IRQ	0	0	0	0	0	0	0	0
% F9	IPR	U	U	U	U	U	U	U	U
† % F8	P01M	0	1	0	0	1	1	0	1
% F7	P3M	0	0	0	0	0	0	0	0
% F6	P2M	1	1	1	1	1	1	1	1
% F5	PRE0	U	U	U	U	U	U	U	0
% F4	T0	U	U	U	U	U	U	U	U
% F3	PRE1	U	U	U	U	U	U	0	0
% F2	T1	U	U	U	U	U	U	U	U
% F1	TMR	0	0	0	0	0	0	0	0
% F0	SIO	U	U	U	U	U	U	U	U

(RESET CONDITION: D7–D0)

EXPANDED REG. GROUP (F)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% (F) 0F	Reserved								
% (F) 0E	Reserved								
% (F) 0D	Reserved								
% (F) 0C	Reserved								
% (F) 0B	Reserved								
% (F) 0A	ICE						0		
% (F) 09	P6M								
% (F) 08	P6D								
% (F) 07	P6					U	U	U	U
% (F) 06	P45M								
% (F) 05	P5D								
% (F) 04	P5	U	U	U	U	U	U	U	U
% (F) 03	P4D								
% (F) 02	P4	U	U	U	U	U	U	U	U
% (F) 01	Reserved								
% (F) 00	Reserved								

(RESET CONDITION)

EXPANDED REG. GROUP (0)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% (0) 03	P3	1	1	1	1	U	U	U	U
% (0) 02	P2	U	U	U	U	U	U	U	U
% (0) 01	P1	U	U	U	U	U	U	U	U
% (0) 00	P0	U	U	U	U	U	U	U	U

(RESET CONDITION)

U = Unknown
† = For Z86C96 (ROMless) Reset condition:"10110110"

Figure 19. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 20). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

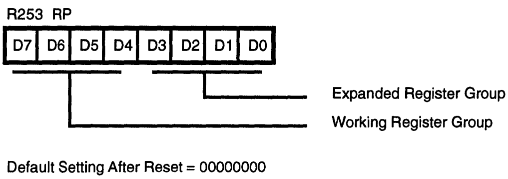


Figure 20. Register Pointer Register

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 21). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 20) selects which group of 16 bytes in the register file, out of the full 256, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C61/62/96, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C61: (See Figures 18 and 19)

R253 RP = 00H	R0 = Port 0	R2 = Port 2
	R1 = Port 1	R3 = Port 3

But If:

R253 RP = 0FH	R0 = Reserved
	R1 = Reserved
	R2 = Port 4
	R3 = Port 4, Direction Register
	R9 = Port 6, Mode Register

Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general purpose register 12H
LD 12H, #11010110	Load value into general purpose register 12H
LD 2, #10010110	Load value into Port 4

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 16 Kbytes of program memory is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

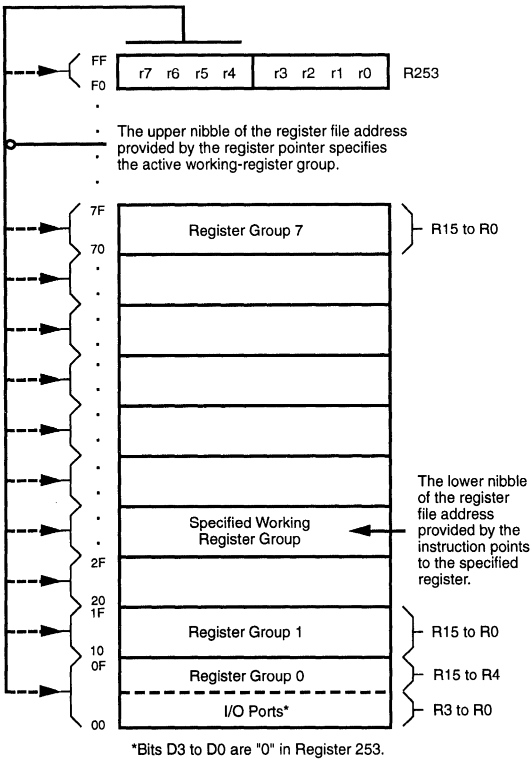


Figure 21. Register Pointer

Stack. The Z86C61/62/96 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 16384 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH-Bit 8-15) can be used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 22).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

FUNCTIONAL DESCRIPTION (Continued)

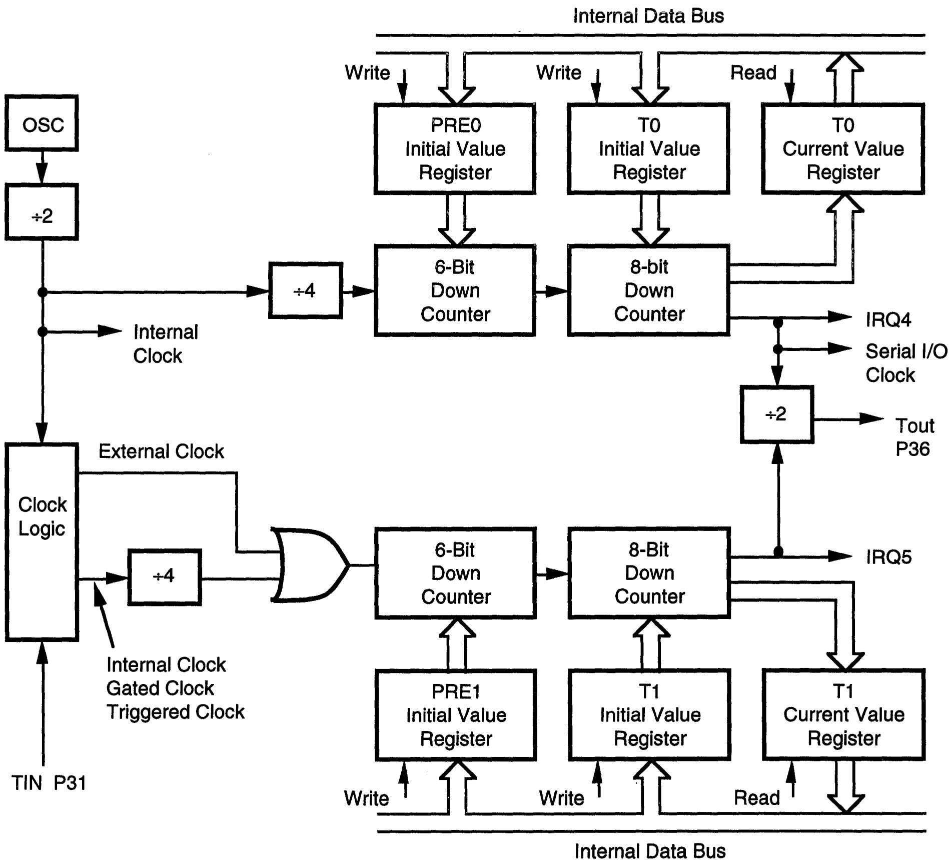


Figure 22. Counter/Timers Block Diagram

Interrupts. The Z86C61/62/96 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 23). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C61/62/96 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

8

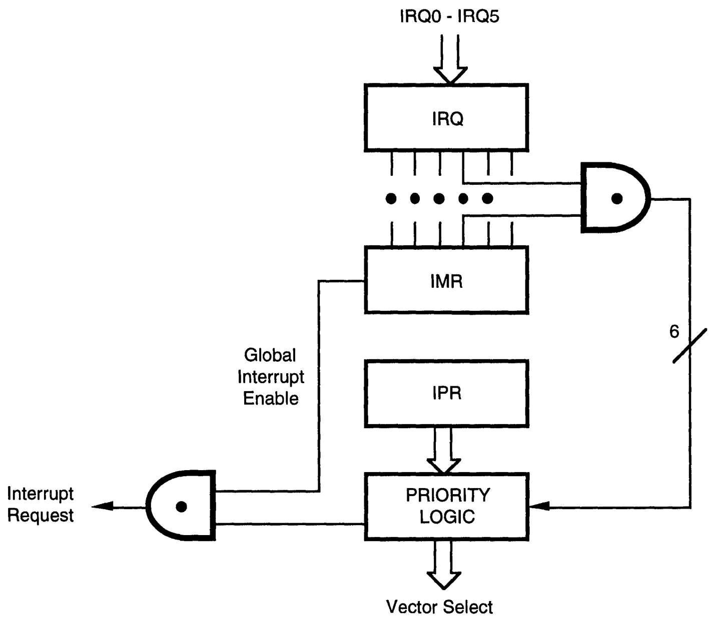


Figure 23. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C61/62/96 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to device ground (Figure 24).

Note: Actual capacitor values specified by the crystal manufacturer.

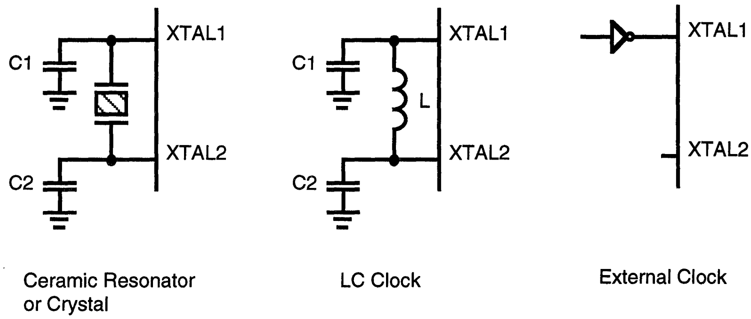


Figure 24. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

8

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 25).

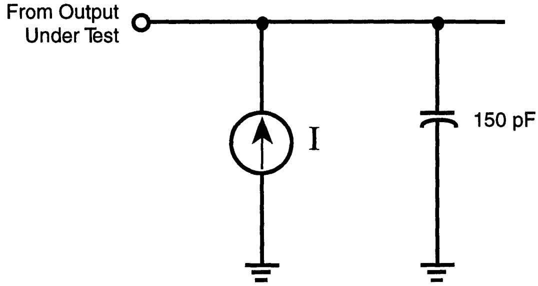


Figure 25. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS
Z86C61/62/96

Sym	Parameter	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC} – 100 mV		V_{CC} – 100 mV		V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	V_{RL} = 0 V
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current		40		40	30	mA	[1] @ 20 MHz
I_{CC1}	Standby Current		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}
I_{ALL}	Auto Latch Low Current	–14	14	–20	20	5	µA	

Notes:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.
[2] V_{CC} = 3.0V to 3.6V
[3] V_{CC} = 4.5V to 5.5V

AC CHARACTERISTICS

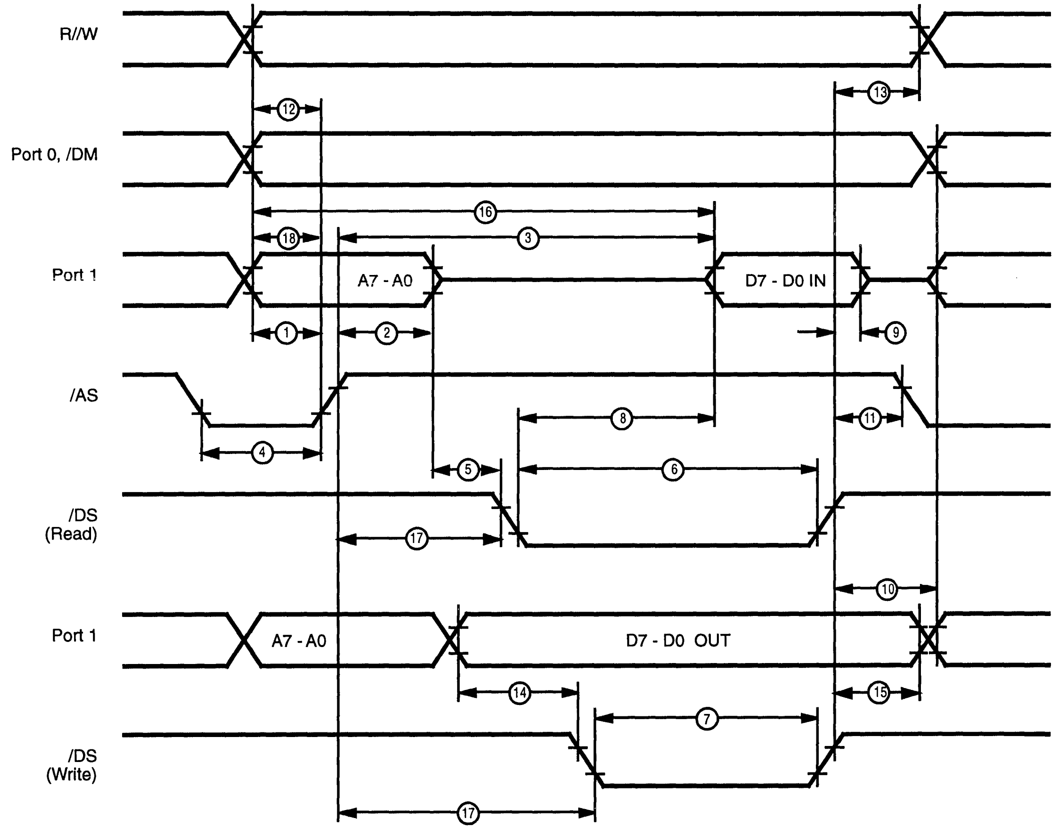


Figure 26. External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Z86C61/62/96 (16 MHz)

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (20 MHz)

No	Symbol	Parameter	T_A = 0°C to +70°C 20 MHz Min	Max	T_A = –40°C to +105°C 20 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	[1,2,3]
4	TwAS	/AS Low Width	30		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	65		65		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.

AC CHARACTERISTICS
Additional Timing Diagram

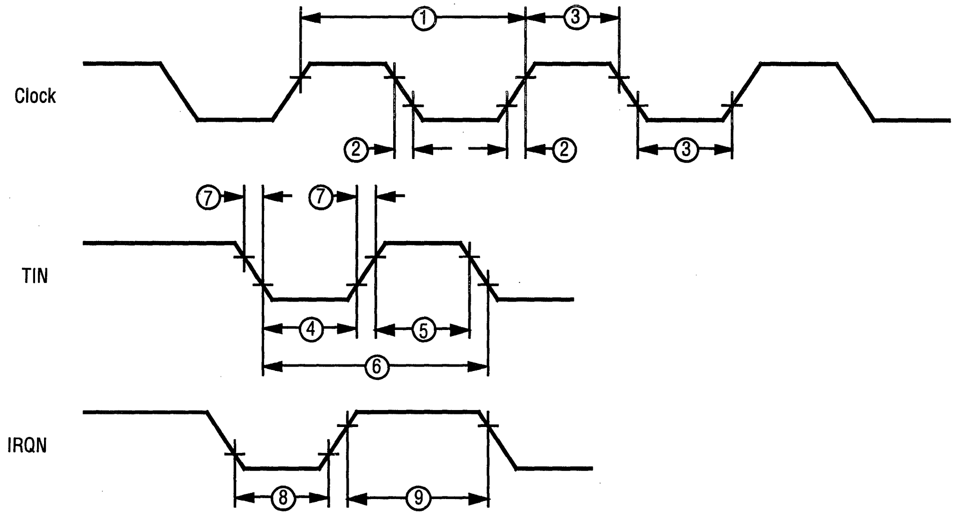


Figure 27. Additional Timing

AC CHARACTERISTICS
Additional Timing Table
Z86C61/62/96

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	[1]
3	TwC	Input Clock Width	25		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:
[1] Clock timing references use $0.8V_{cc}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

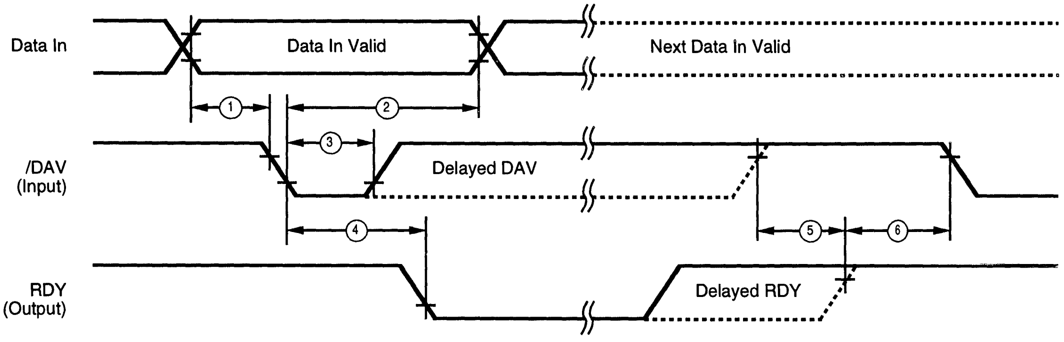


Figure 28. Input Handshake Timing

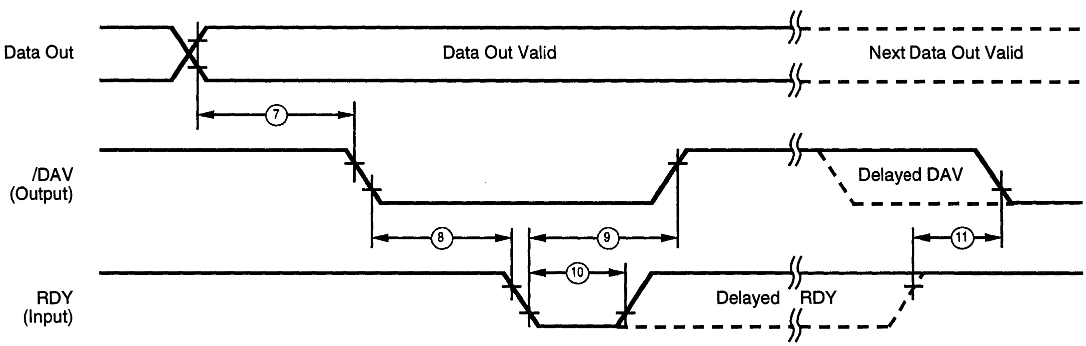


Figure 29. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table
Z86C61/62/96

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY fall to DAV rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY rise to DAV fall Delay	115		115		OUT

Z8 CONTROL REGISTER DIAGRAMS

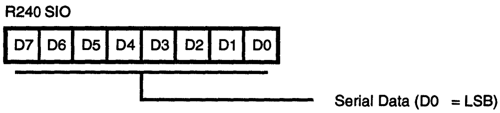


Figure 30. Serial I/O Register (F0H: Read/Write)

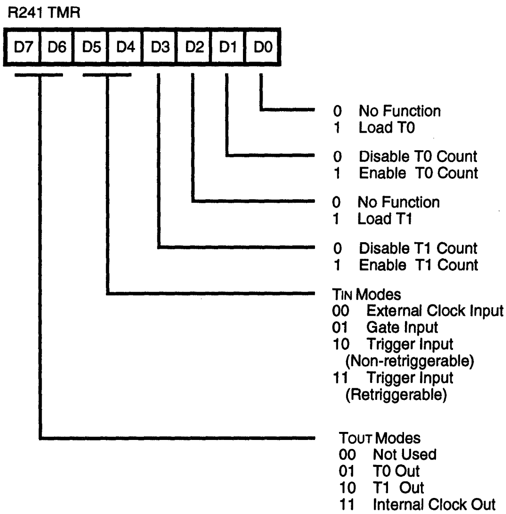


Figure 31. Timer Mode Register (F1H: Read/Write)

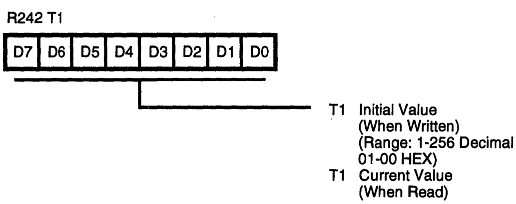


Figure 32. Counter/Timer 1 Register (F2H: Read/Write)

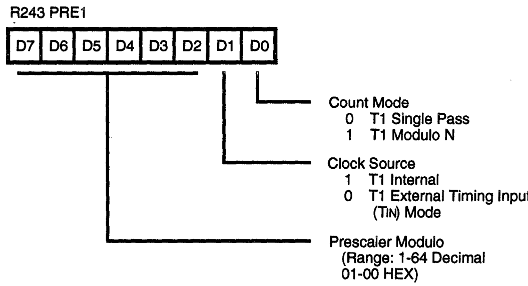


Figure 33. Prescaler 1 Register (F3H: Write Only)

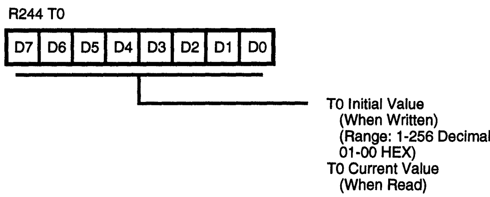


Figure 34. Counter/Timer 0 Register (F4H: Read/Write)

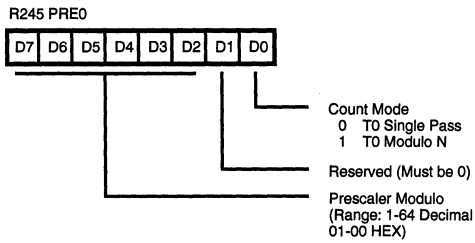


Figure 35. Prescaler 0 Register (F5H: Write Only)

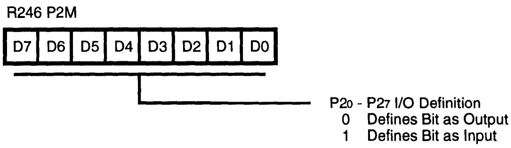


Figure 36. Port 2 Mode Register (F6H: Write Only)

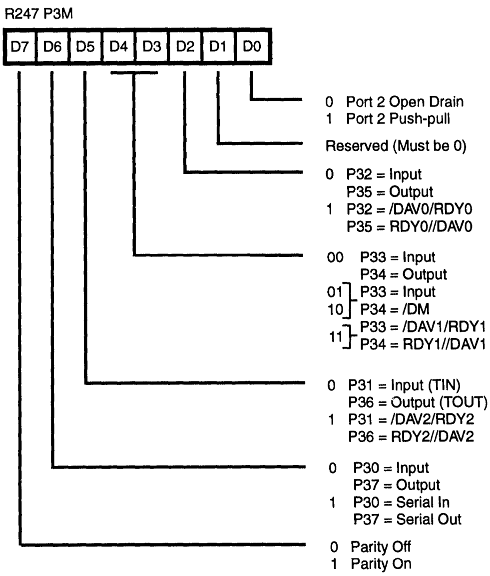


Figure 37. Port 3 Mode Register (F7H: Write Only)

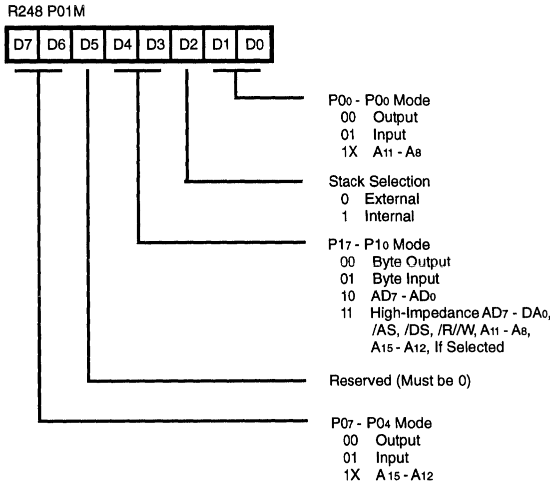


Figure 38. Port 0 and 1 Mode Register (F8H: Write Only)

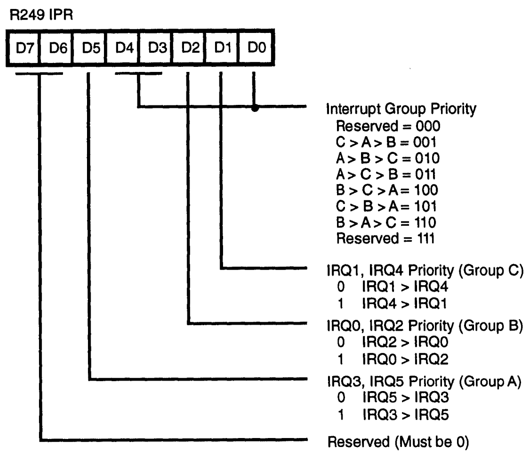


Figure 39. Interrupt Priority Register (F9H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

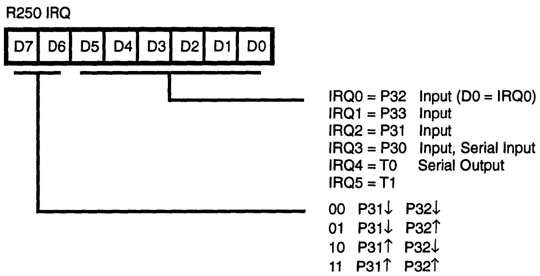


Figure 40. Interrupt Request Register (FAH: Read/Write)

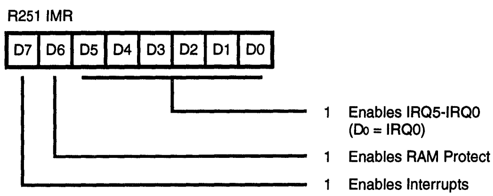


Figure 41. Interrupt Mask Register (FBH: Read/Write)

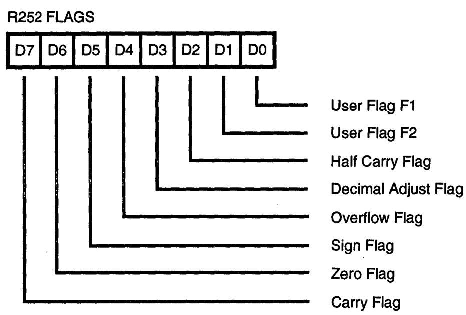


Figure 42. Flag Register (FCH: Read/Write)

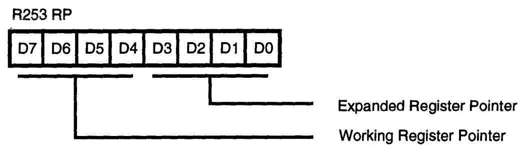


Figure 43. Register Pointer Register (FDH: Read/Write)

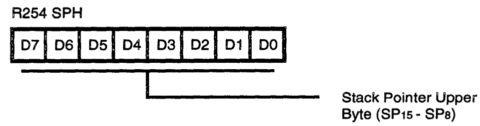


Figure 44. Stack Pointer Register (FEH: Read/Write)

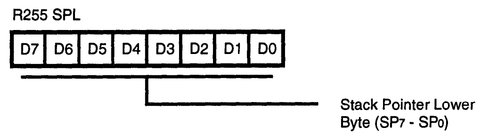


Figure 45. Stack Pointer Register (FFH: Read/Write)

Z8 EXPANDED REGISTER FILE CONTROL REGISTERS

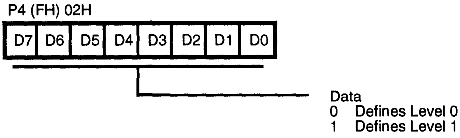


Figure 46. Port 4 Data Register (F)02: (Read/Write)

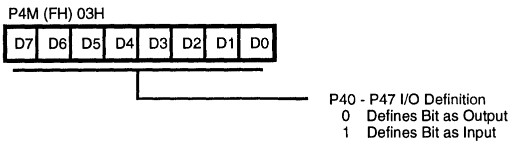


Figure 47. Port 4 Mode Register (F)03: (Write Only)

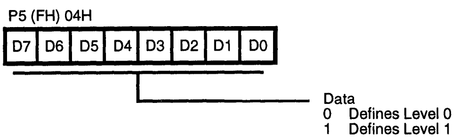


Figure 48. Port 5 Data Register (F)04: (Read/Write)

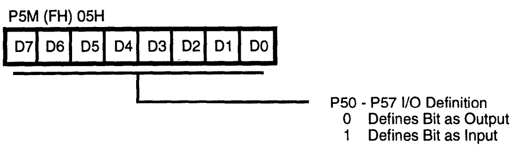


Figure 49. Port 5 Mode Register (F)05: (Write Only)

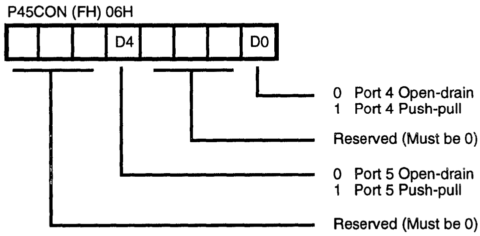


Figure 50. Port 4/5 Configuration Register (F)06: (Write Only)

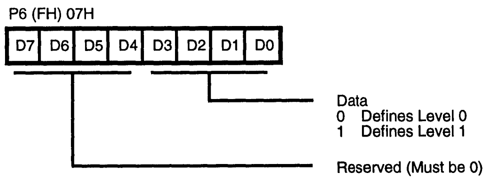


Figure 51. Port 6 Data Register (F)07: (Read/Write)

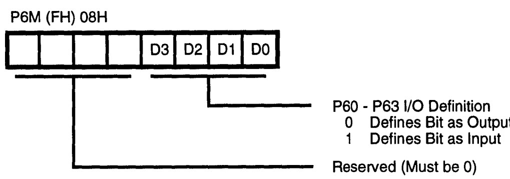


Figure 52. Port 6 Mode Register (F)08: (Write Only)

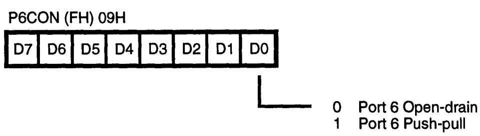


Figure 53. Port 6 Mode Register (F)09: (Write Only)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

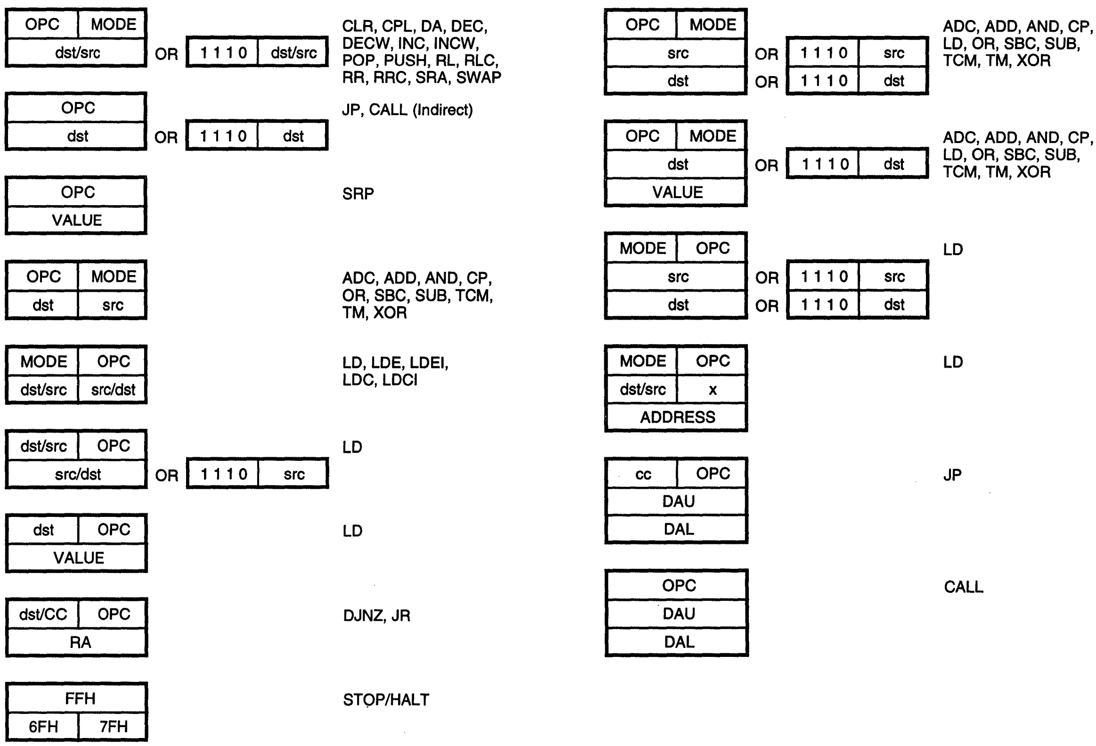
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions **Three-Byte Instructions**

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

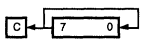
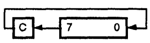
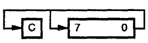
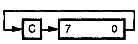
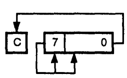
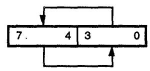
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst +src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst +src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC +dst Range: +127, –128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP +1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC +dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr +1	Ir	Irr	C3	-	-	-	-	-	-

8

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

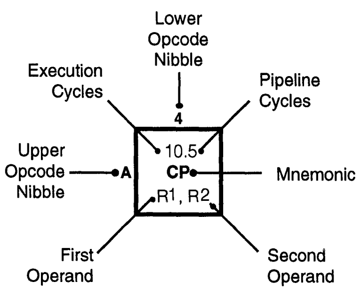
8

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**

Bytes per Instruction: columns 0–3: 2; columns 4–7: 3; columns 8–C: 2; column D: 3; columns E–F: 1



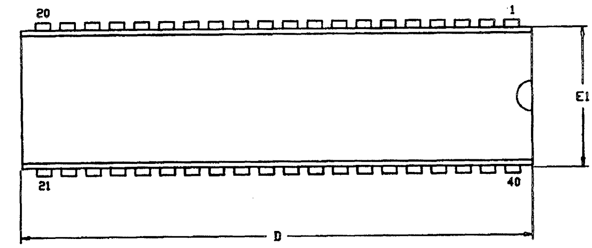
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

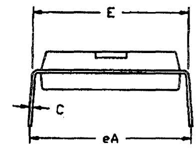
Sequence:
Opcode, First Operand, Second Operand

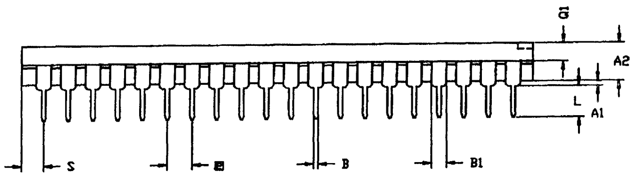
Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



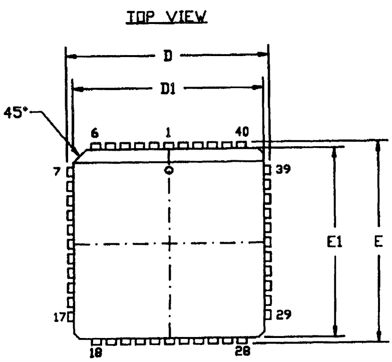


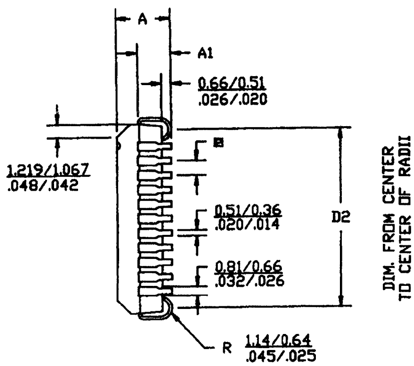


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin Plastic DIP Package



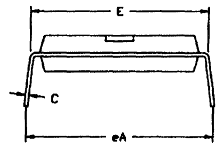


NOTES:

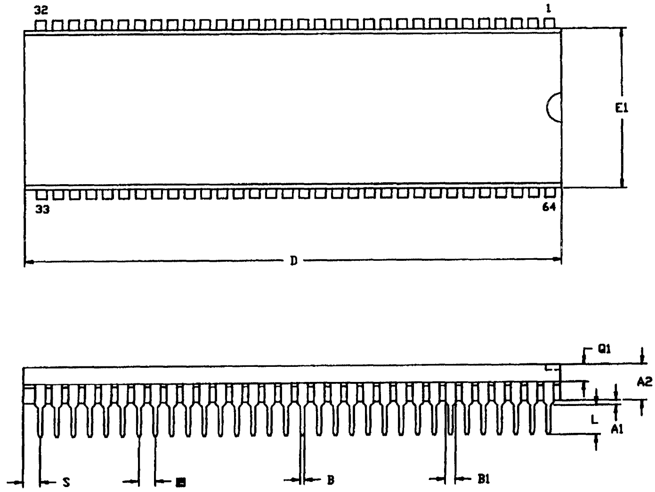
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

44-Pin PLCC Package

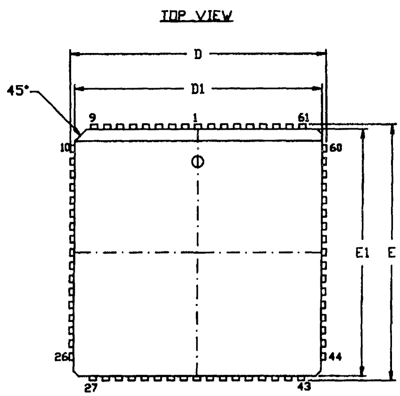


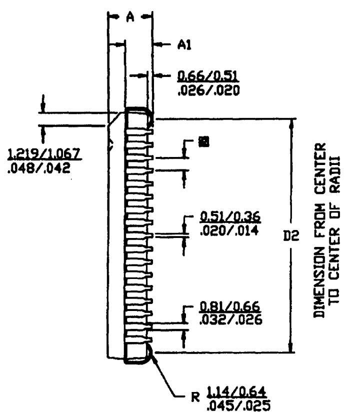
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
■	1.78 TYP		.070 TYP	
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070



CONTROLLING DIMENSIONS : INCH

64-Pin Plastic DIP Package





NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.67	2.92	.105	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
■	1.27 TYP		.050 TYP	

68-Pin PLCC Package

ORDERING INFORMATION

Z86C61/62/96

16 MHz	
40-pin DIP	**44-pin PLCC**
Z86C6116PSC	Z86C6116VSC

16 MHz	
64-pin DIP	**68-pin PLCC**
Z86C6216PSC	Z86C6216VSC

20 MHz	
64-pin DIP	**68-pin PLCC**
Z86C9620PSC	Z86C9620VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
V = Plastic Chip Carrier

Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speed
16 = 16 MHz
20 = 20 MHz

Environmental
C = Plastic Standard

Example:
Z 86C61 16 P S C is an 86C61, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 16 — Speed
- 86C61 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller 7

Z86C61/62/96 CMOS Z8®
Microcontroller 8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
ROMless Microcontroller 10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller 11

Support Products 12

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Products Guide S

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Ordering Information L

Z86C63/64

CMOS Z8®
32K ROM MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, 64-Pin DIP, or 68-Pin PLCC Package
- 32 Input/Output Lines (Z86C63 Only)
- 52 Input/Output Lines (Z86C64)
- 3.0V to 5.5V Operating Range
- Low Power Consumption - 200 mW (max)
- Fast Instruction Pointer - 0.75 µs @ 16 MHz
- Two Standby Modes - STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- 32 Kbytes of ROM
- 256 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 16 and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive
- Low EMI Emission Mode

GENERAL DESCRIPTION

The Z86C63/64 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C63/64 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM.

The Z86C63 is housed in a 40-pin DIP, and a 44-pin PLCC package, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin version only. The Z86C64 is housed in a 64-pin DIP, and a 68-pin PLCC. Both versions of the Z86C64 have the ROMless pin option, which allows both external memory and preprogrammed ROM, enabling this Z8 microcontroller to be used in high-volume applications or where code flexibility is required. The Z86C96 ROMless Z8 will support the Z86C63/64.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C63/64 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C63 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C64 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C63/64 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (UART) (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

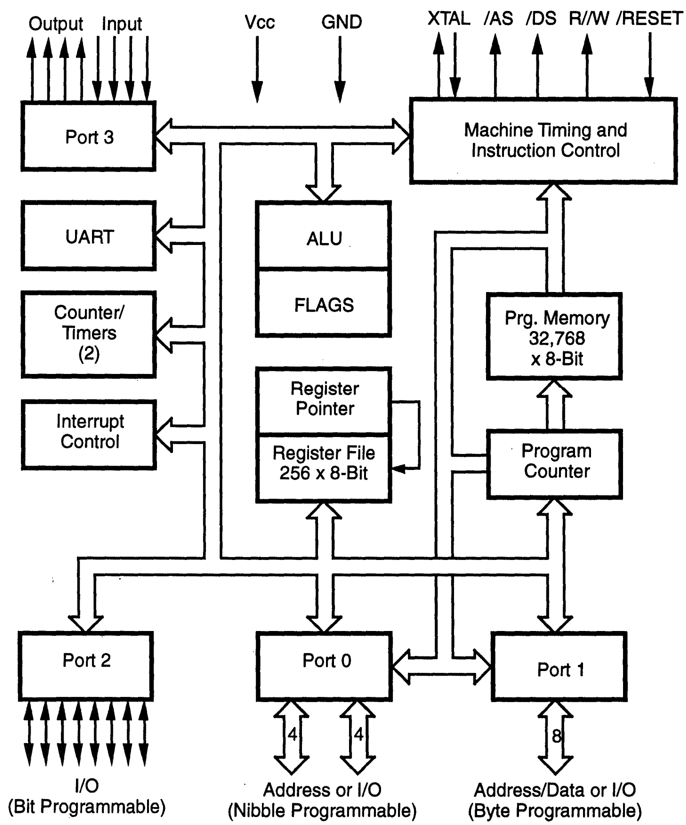


Figure 1. Z86C63 Functional Block Diagram

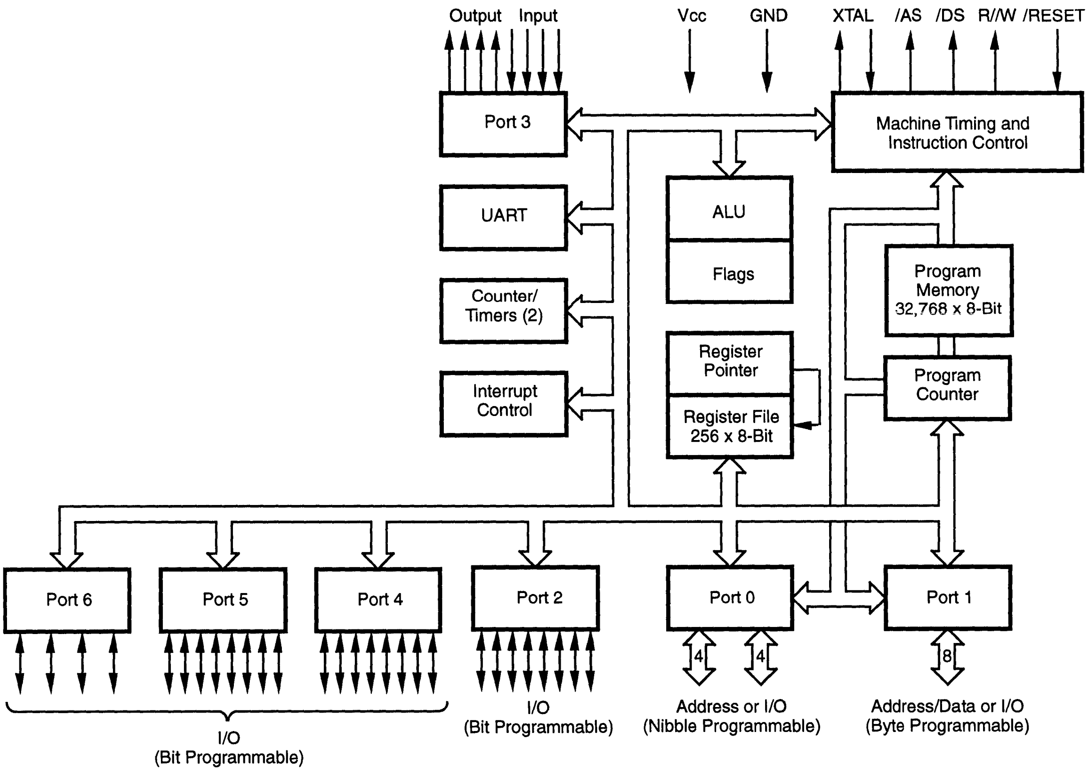


Figure 2. Z86C64 Functional Block Diagram

PIN DESCRIPTION

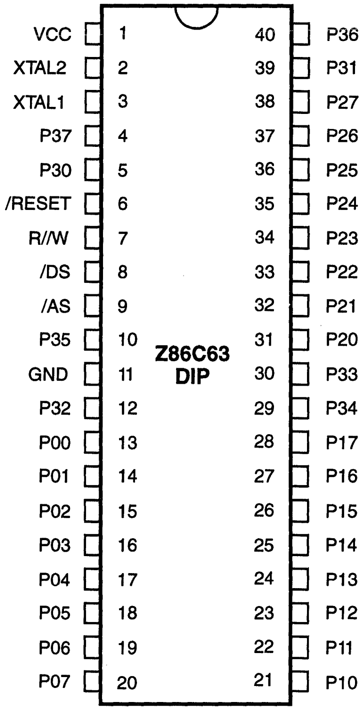


Figure 3. Z86C63 40-Pin DIP Pin Assignments

Table 1. Z86C63 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0 through 7	In/Output
21-28	P17-P10	Port 1, Pins 0 through 7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0 through 7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

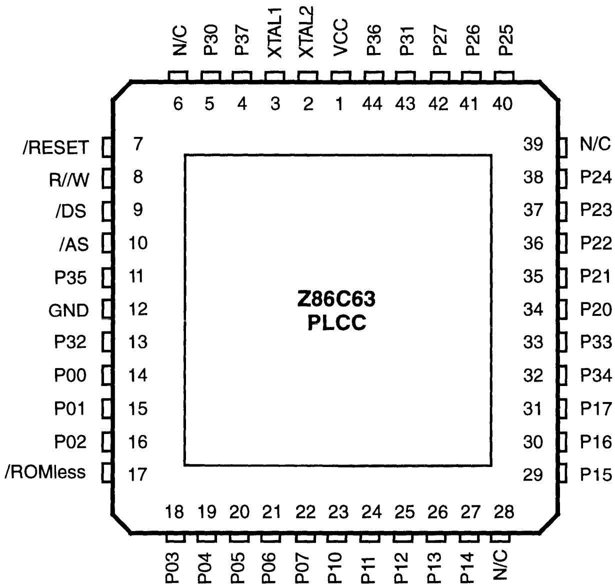


Figure 4. Z86C63 44-Pin PLCC Pin Assignments

Table 2. Z86C63 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output

Pin #	Symbol	Function	Direction
17	/ROMless	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
39	N/C	Not Connected	Input
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

9

PIN DESCRIPTION (Continued)

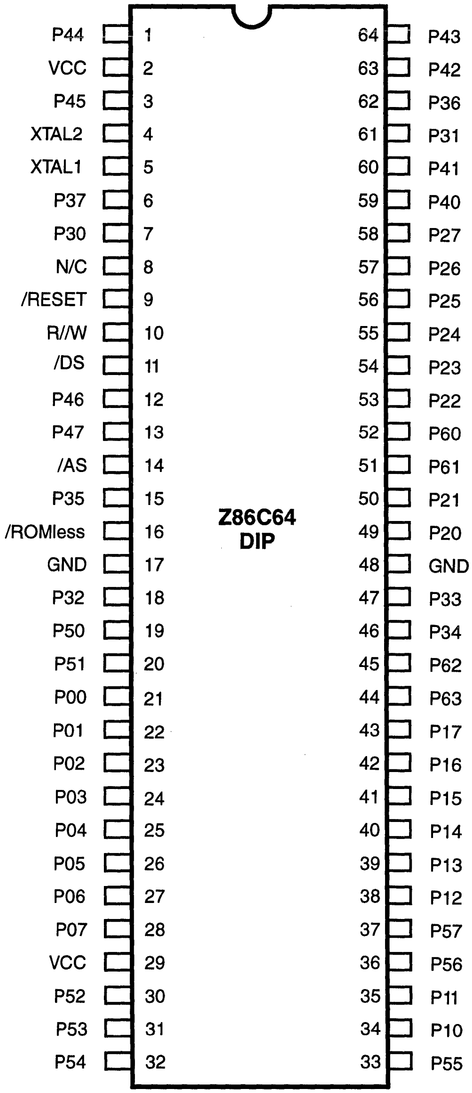


Figure 5. Z86C64 64-Pin DIP Pin Assignments

Table 3. Z86C64 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	/ROMless	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0 through 7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

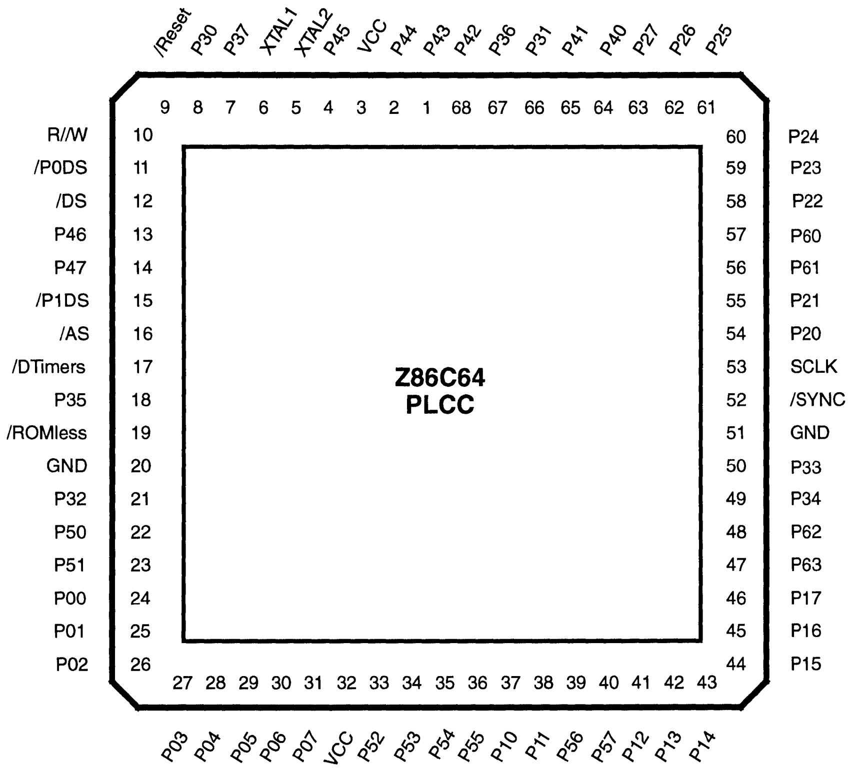


Figure 6. Z86C64 68-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 4. Z86C64 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	V_{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	/ROMless	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0 through 7	In/Output
32	V_{CC}	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (**Note:** When left unconnected or pulled High to V_{CC} the part functions as a normal Z86C63/64 ROM version.) This pin is only available on the 44-pin version of the Z86C63, and both versions of the Z86C64, and has internal pull-up.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C63/64 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Stop-Mode Recovery is accomplished by resetting the device.

/P0DS *Port 0 Data Strobe* (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

/P1DS *Port 1 Data Strobe* (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

/DTIMERS *Disable Timers* (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

SCLK (output). System clock pin.

/SYNC *Instruction SYNC Signal* (output, active Low). This signal indicates the last clock of the current executing instruction.

PIN FUNCTIONS (Continued)

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 7).

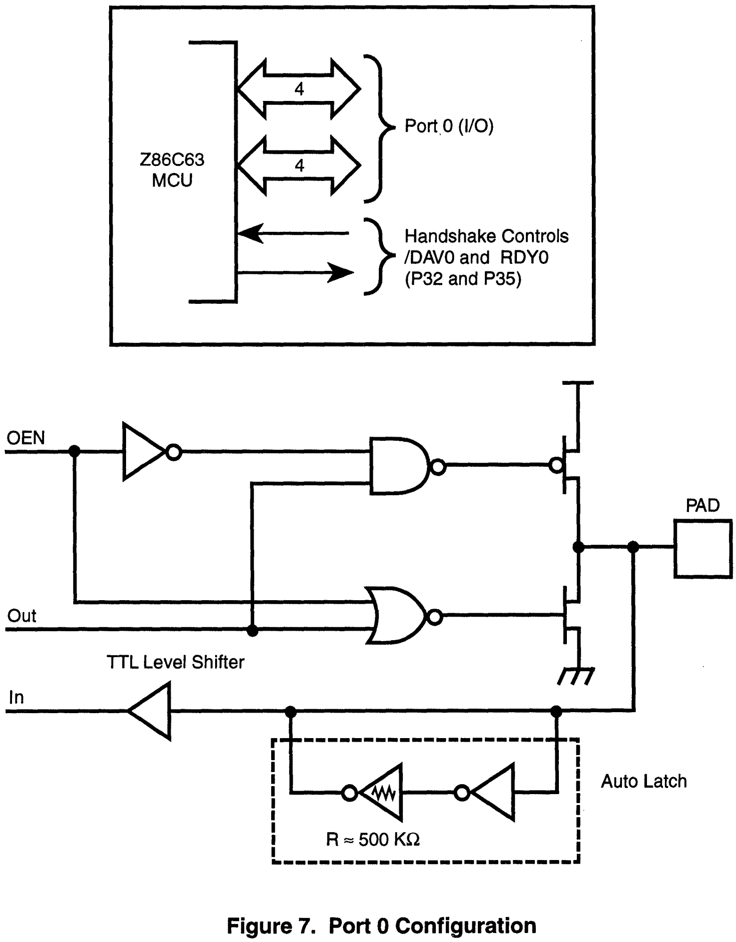


Figure 7. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C63/64, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 32,768 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the microcontroller to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 8).

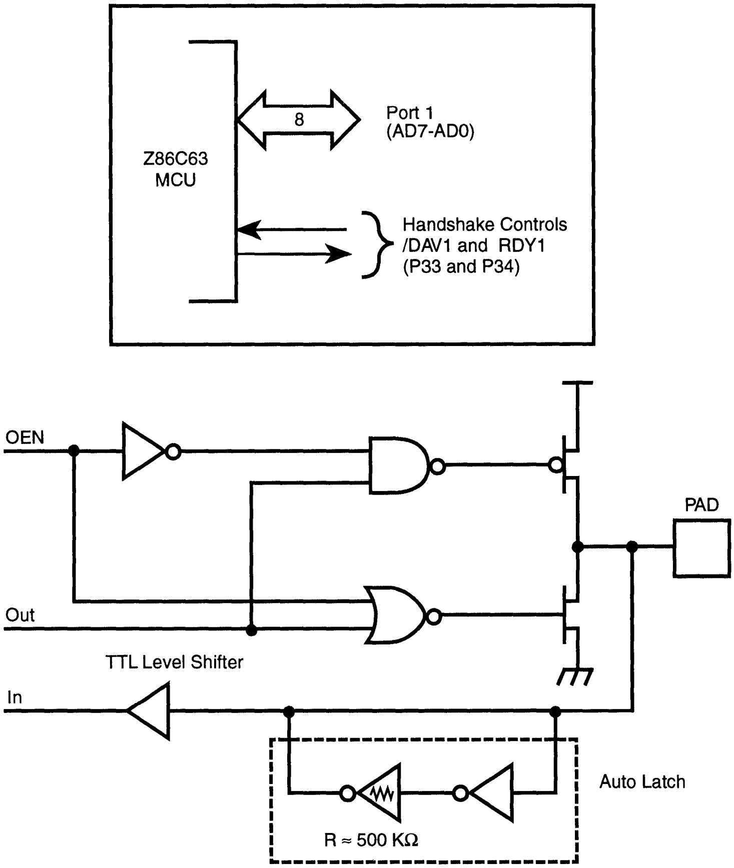


Figure 8. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

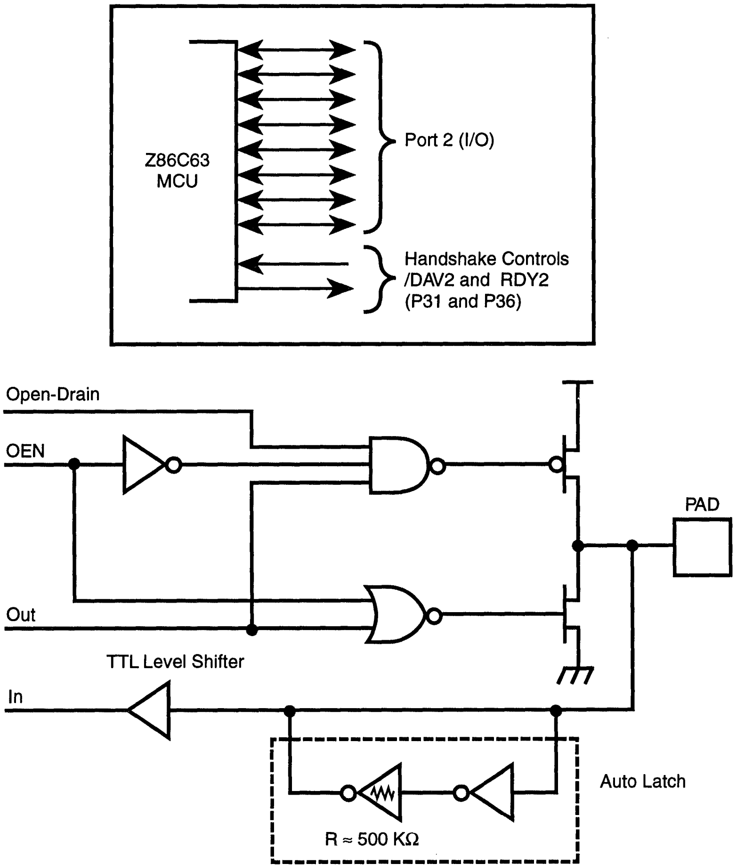


Figure 9. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10). Port 3 inputs have Auto Latches.

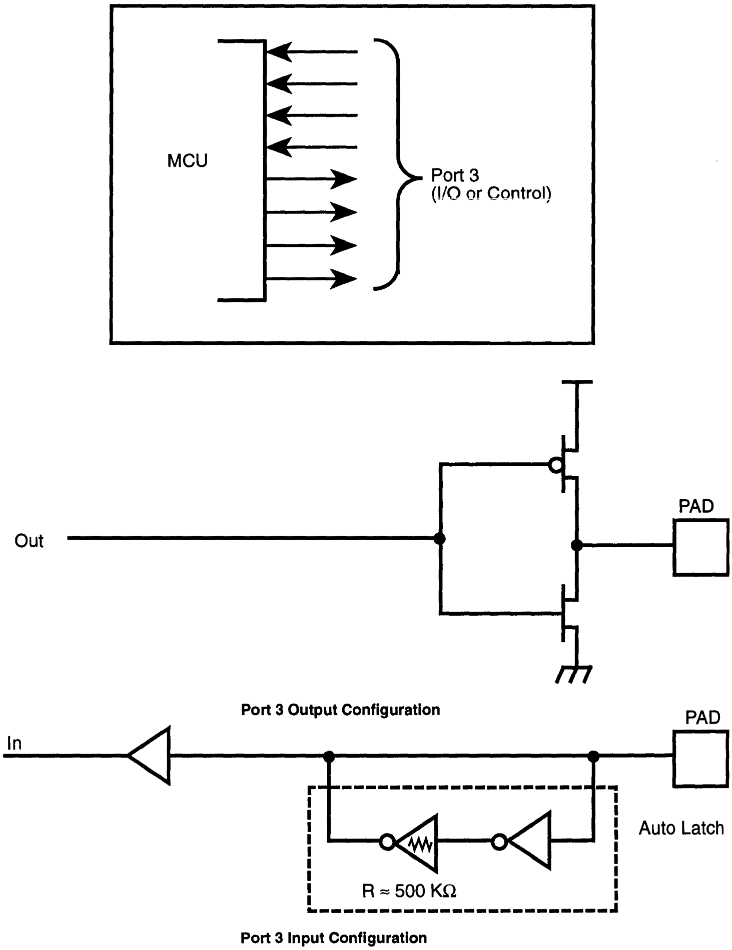


Figure 10. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Table 5. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

UART OPERATION

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C63/64 automatically adds a start bit and two stop bits to transmitted data (Figure 11). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Note: UART function is only available when the Z86C63/64 is in standard timing mode (i.e., P01M D5 = 0).

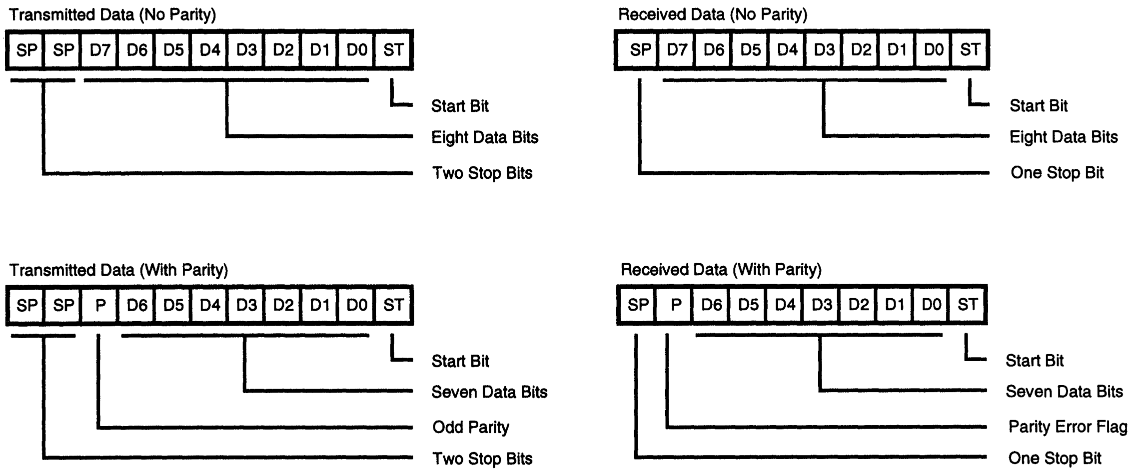


Figure 11. Serial Data Formats

UART OPERATION (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 12). Port address (F)02.

Port 5 (P57-P50). Same as Port 4. Port address (F)04.

Port 6 (P63-P60). Same as Port 4. (**Note:** this is a 4-bit port, Bits D3 to D0.) Port address (F)07.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

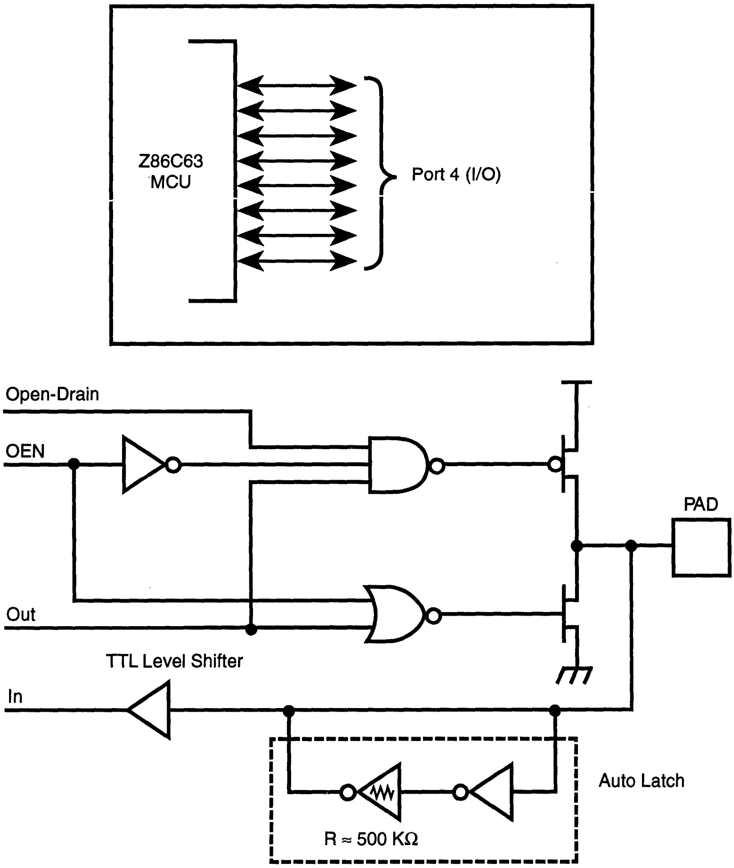


Figure 12. Port 4 Configuration

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C63/64 can address up to 32 Kbytes of external program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 32,768 consists of on-chip ROM. At addresses 32,768 and greater, the Z86C63/64 executes external program memory fetches. The Z86C96, and the Z86C63/64 in ROMless mode, can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory (/DM). The ROM version can address up to 32 Kbytes of external data memory space beginning at location 32,768. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

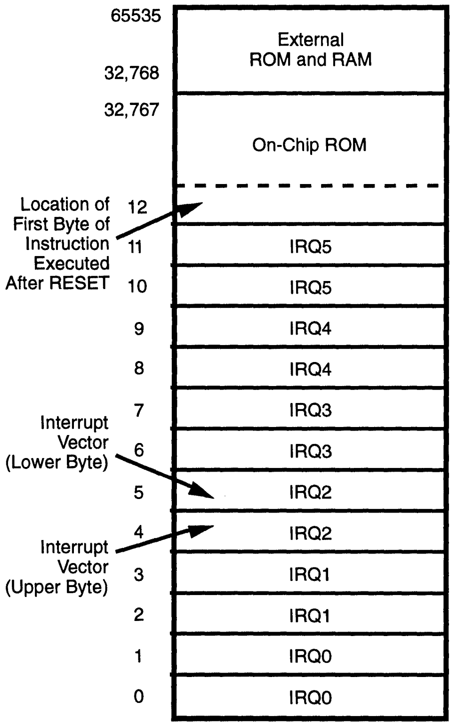


Figure 13. Program Memory Configuration

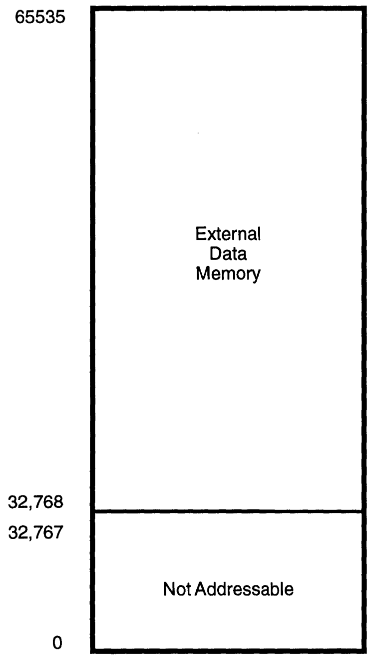


Figure 14. Data Memory Configuration

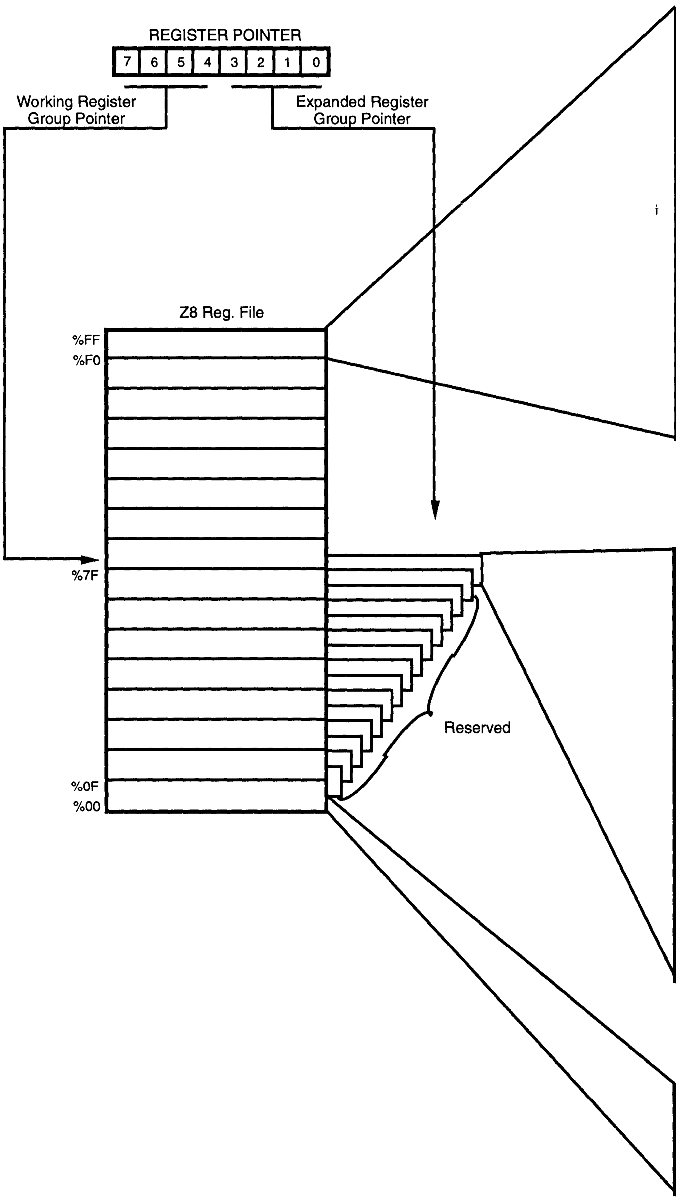
9

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 15). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 16).

Location		Identifiers
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239 … R4	General-Purpose Registers	
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 15. Register File



Z8 STANDARD CONTROL REGISTERS

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% FF	SPL	U	U	U	U	U	U	U	U
% FE	SPH	U	U	U	U	U	U	U	U
% FD	RP	0	0	0	0	0	0	0	0
% FC	FLAGS	U	U	U	U	U	U	U	U
% FB	IMR	0	U	U	U	U	U	U	U
% FA	IRQ	0	0	0	0	0	0	0	0
% F9	IPR	U	U	U	U	U	U	U	U
† % F8	P01M	0	1	0	0	1	1	0	1
% F7	P3M	0	0	0	0	0	0	0	0
% F6	P2M	1	1	1	1	1	1	1	1
% F5	PRE0	U	U	U	U	U	U	U	0
% F4	T0	U	U	U	U	U	U	U	U
% F3	PRE1	U	U	U	U	U	U	0	0
% F2	T1	U	U	U	U	U	U	U	U
% F1	TMR	0	0	0	0	0	0	0	0
% F0	SIO	U	U	U	U	U	U	U	U

EXPANDED REG. GROUP (F)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% (F) 0F	Reserved								
% (F) 0E	Reserved								
% (F) 0D	Reserved								
% (F) 0C	Reserved								
% (F) 0B	Reserved								
% (F) 0A	ICE						0		
% (F) 09	P6M								
% (F) 08	P6D								
% (F) 07	P6					U	U	U	U
% (F) 06	P45M								
% (F) 05	P5D								
% (F) 04	P5	U	U	U	U	U	U	U	U
% (F) 03	P4D								
% (F) 02	P4	U	U	U	U	U	U	U	U
% (F) 01	Reserved								
% (F) 00	Reserved								

EXPANDED REG. GROUP (0)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
% (0) 03	P3	1	1	1	1	U	U	U	U
% (0) 02	P2	U	U	U	U	U	U	U	U
% (0) 01	P1	U	U	U	U	U	U	U	U
% (0) 00	P0	U	U	U	U	U	U	U	U

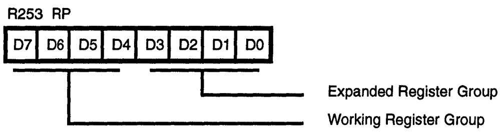
U = Unknown

† = For Z86C96 (ROMless) Reset condition:"10110110"

Figure 16. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C63/64 also allows short 4-bit register addressing using the Register Pointer (Figure 17). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.



Default Setting After Reset = 00000000

Figure 17. Register Pointer Register

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 18). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 17) selects which group of 16 bytes in the register file, out of the full 256, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C63/64, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C63: (See Figures 15 and 16)

R253 RP = 00H	R0 = Port 0 R1 = Port 1	R2 = Port 2 R3 = Port 3

But If:

R253 RP = 0FH	R0 = Reserved R1 = Reserved R2 = Port 4 R3 = Port 4, Direction Register R9 = Port 6, Mode Register

Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general-purpose register 12H
LD 12H, #11010110	Load value into general-purpose register 12H
LD 2, #10010110	Load value into Port 4

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 32 Kbytes of program memory is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

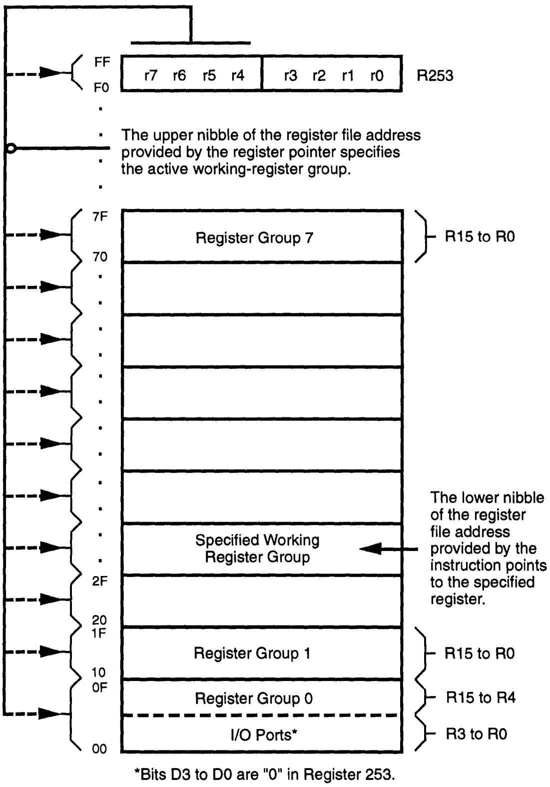


Figure 18. Register Pointer

Stack. The Z86C63/64 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 32,768 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH-Bit 8-15) can be used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Note: When the Z86C63/64 is in extended timing mode (P01M D5 = 1), the system clock output on P36 will stretch by one clock cycle during data strobes.

FUNCTIONAL DESCRIPTION (Continued)

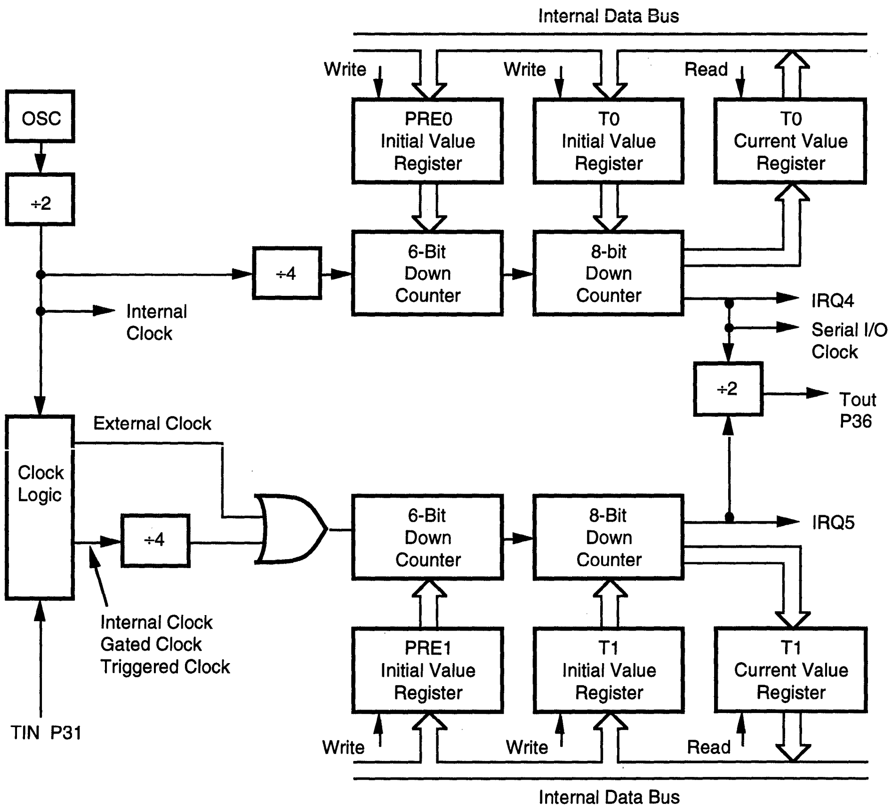


Figure 19. Counter/Timers Block Diagram

Interrupts. The Z86C63/64 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 20). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C63/64 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

9

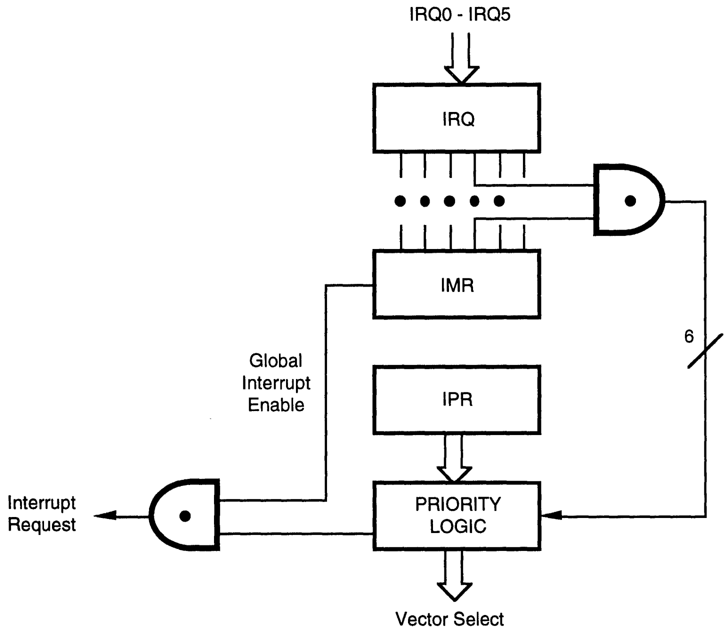


Figure 20. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C63/64 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to device ground (Figure 21).

Note: Actual capacitor values specified by the crystal manufacturer.

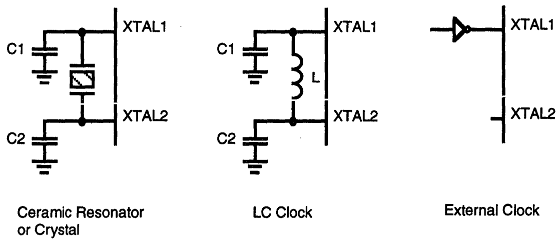


Figure 21. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

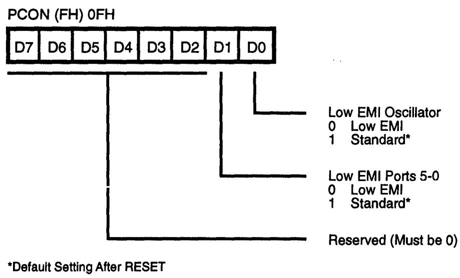


Figure 22. Port Configuration Register (PCON) (Read/Write)

Port Configuration Register (PCON). The PCON register configures the ports; low EMI on Ports 0, 1, 2, 3, 4, and 5, and low EMI oscillator. The PCON register is located in the expanded register file at bank F, location 00 (Figure 22).

Low EMI Ports (D1). Ports can be configured as Low EMI Ports by resetting this bit (D1 = 0) or configured as Standard Ports by setting this bit (D1 = 1). The default value is 1.

Low EMI OSC (D0). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. The low EMI mode will reduce the drive of the oscillator (OSC).

Selecting the Low EMI oscillator changes the internal Z8 system clock from XTAL/2 to XTAL/1. Maximum clock speed is 4 MHz.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).

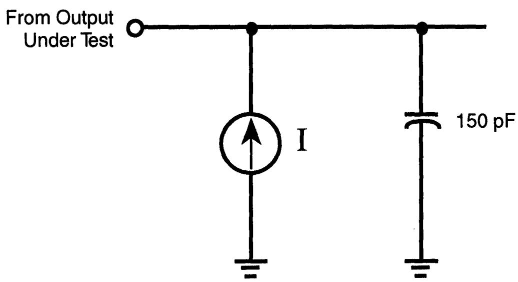


Figure 23. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS
Z86C63

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage	V_{CC} – 100 mV		V_{CC} – 100 mV			V	I_{OH} = –100 µA
V_{OH}	Output High Voltage (Low EMI)	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage (Low EMI)		0.4		0.4		V	I_{OL} = +2.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{OL}	Output Low Voltage (Low EMI)		0.6		0.6		V	I_{OL} = +2.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	V_{RL} = 0 V
I_{CC}	Supply Current (Standard Mode)		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current (Standard Mode)		40		40	30	mA	[1] @ 20 MHz
I_{CC}	Supply Current (Low EMI)		6.0			4.0	mA	@ 4 MHz
I_{CC1}	Standby Current (Standard Mode)		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC1}	Standby Current (Low EMI)		1.6			0.8	mA	@ 4 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}
I_{ALL}	Auto Latch Low Current	–14	14	–20	20	5	µA	

Notes:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.
[2] V_{CC} = 3.0V to 3.6V
[3] V_{CC} = 4.5V to 5.5V

AC CHARACTERISTICS

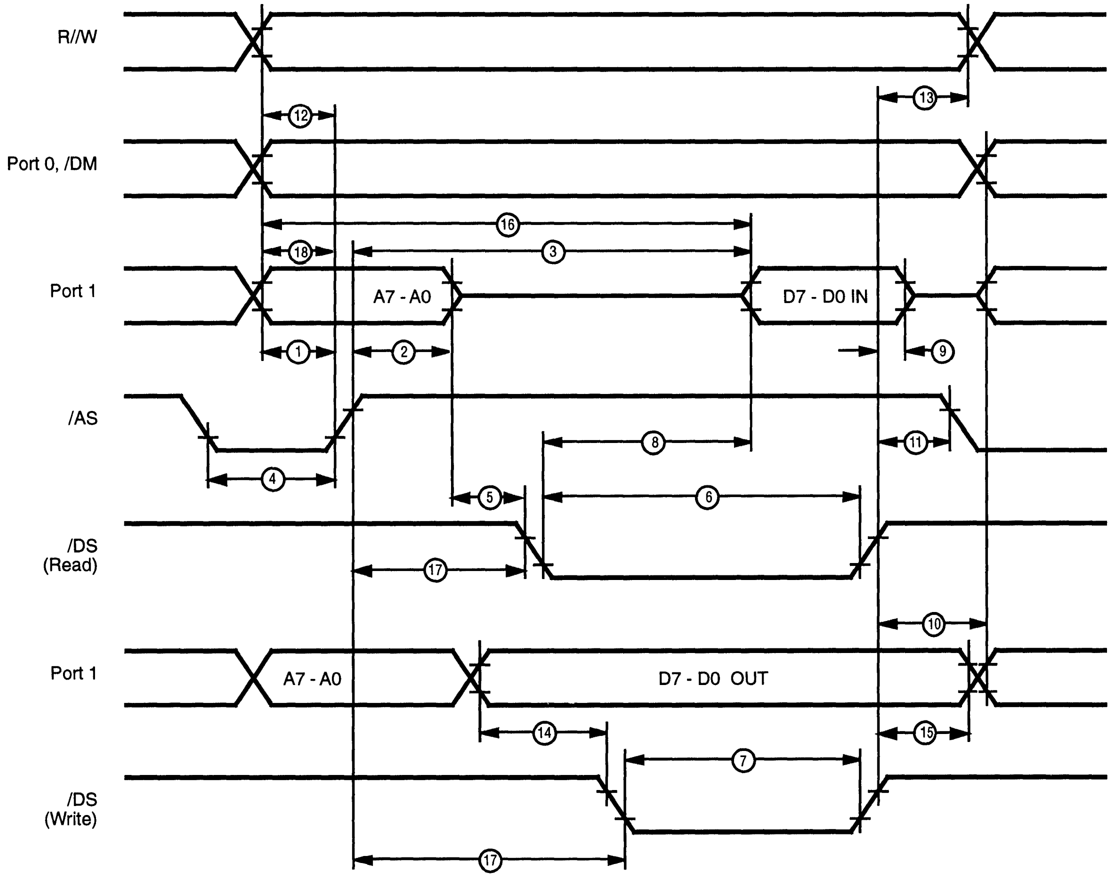


Figure 24. External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C63/64 (16 MHz—Standard Mode Only[4])

			T_A = 0°C to +70°C 16 MHz		T_A = –40°C to +105°C 16 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.
Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C63/64 (20 MHz—Standard Mode Only[4])

			T_A = 0°C to +70°C 20 MHz		T_A = –40°C to +105°C 20 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	[1,2,3]
4	TwAS	/AS Low Width	30		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	65		65		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.
Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

AC CHARACTERISTICS
Additional Timing Diagram

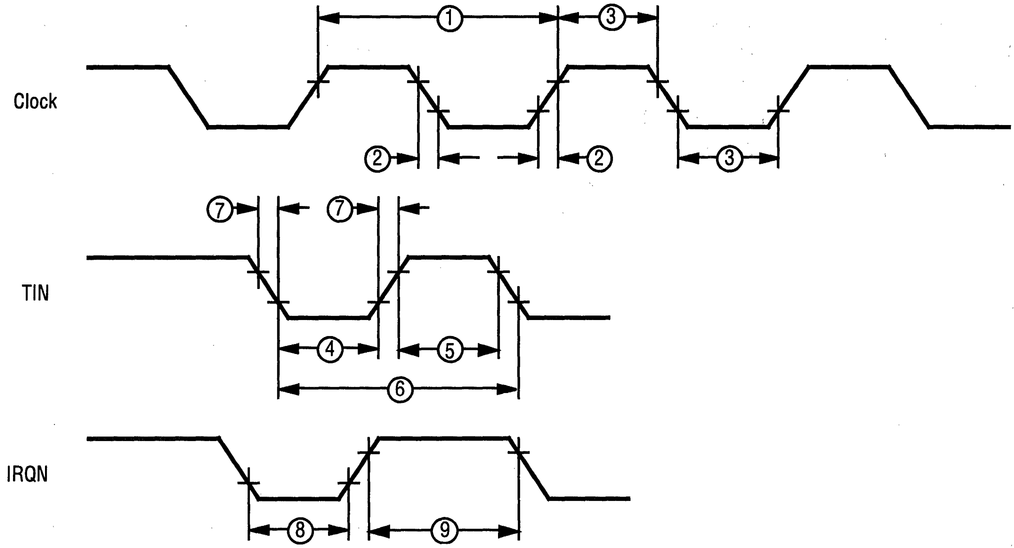


Figure 25. Additional Timing

AC CHARACTERISTICS
Additional Timing Table
Z86C63 (Standard Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	[1]
3	TwC	Input Clock Width	25		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

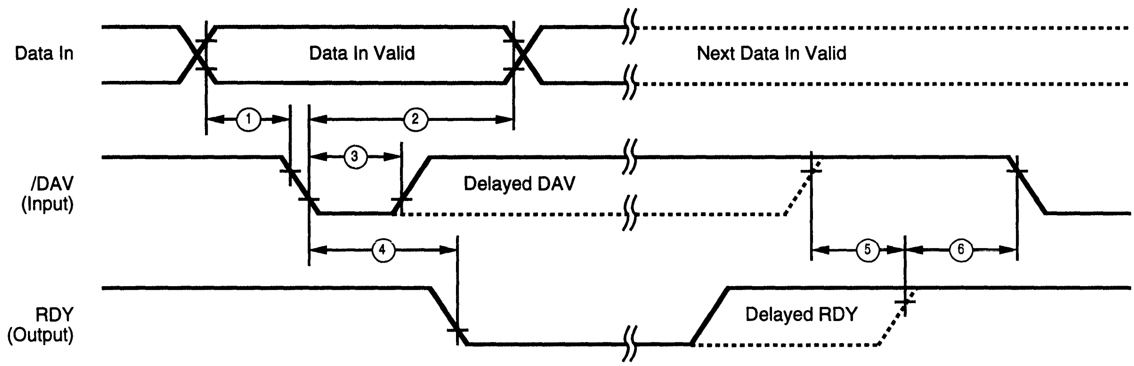


Figure 26. Input Handshake Timing

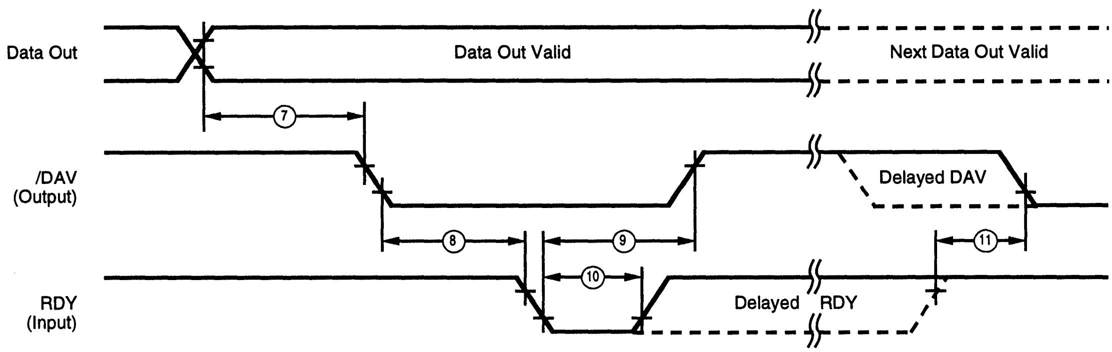


Figure 27. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table
Z86C63

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV Fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	115		115		OUT

Z8 CONTROL REGISTER DIAGRAMS

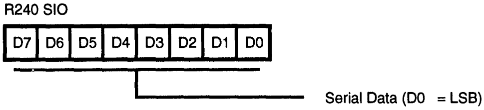


Figure 28. Serial I/O Register (F0H: Read/Write)

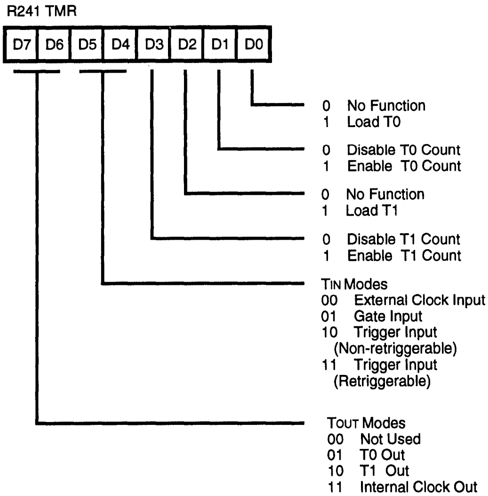


Figure 29. Timer Mode Register (F1H: Read/Write)

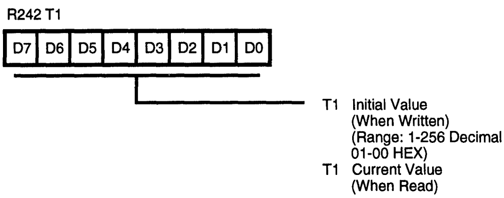


Figure 30. Counter/Timer 1 Register (F2H: Read/Write)

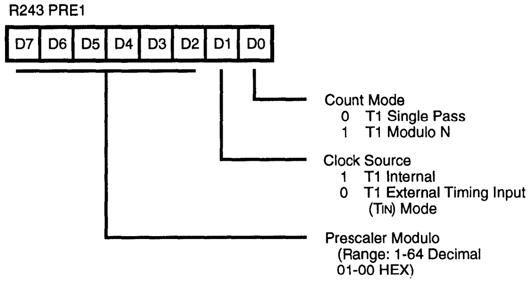


Figure 31. Prescaler 1 Register (F3H: Write Only)

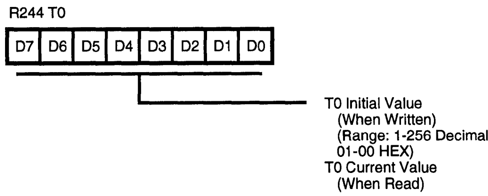


Figure 32. Counter/Timer 0 Register (F4H: Read/Write)

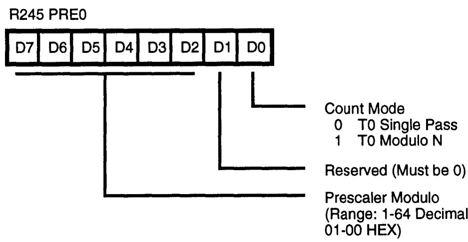


Figure 33. Prescaler 0 Register (F5H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

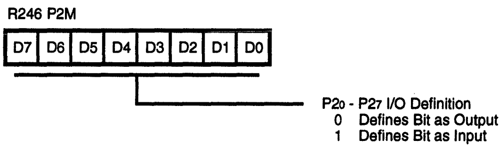


Figure 34. Port 2 Mode Register (F6H: Write Only)

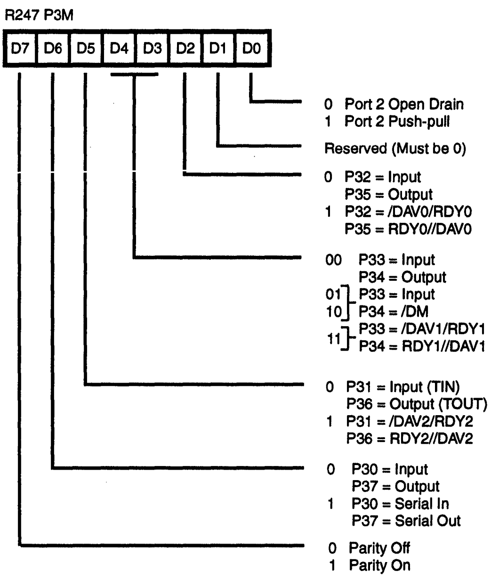


Figure 35. Port 3 Mode Register (F7H: Write Only)

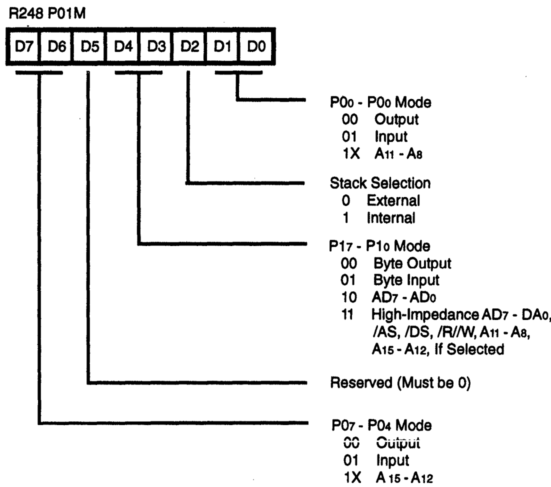


Figure 36. Port 0 and 1 Mode Register (F8H: Write Only)

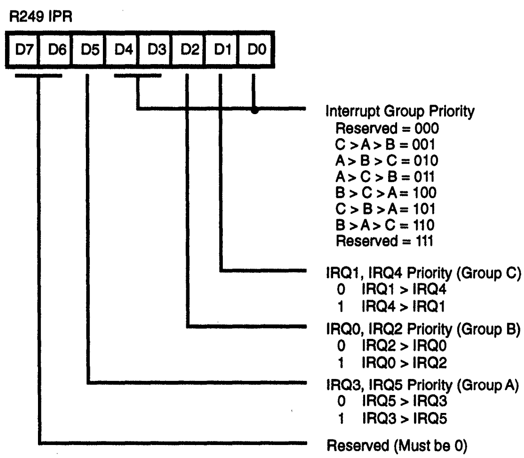


Figure 37. Interrupt Priority Register (F9H: Write Only)

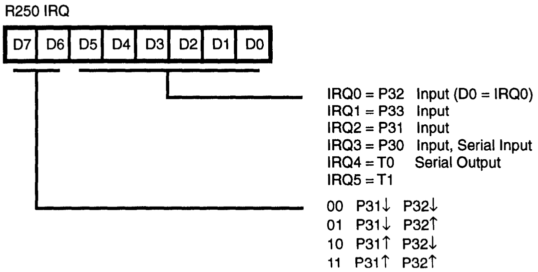


Figure 38. Interrupt Request Register (FAH: Read/Write)

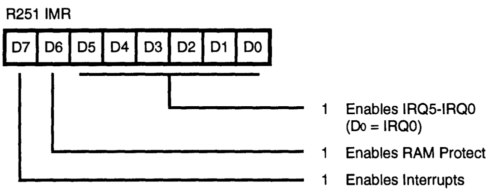


Figure 39. Interrupt Mask Register (FBH: Read/Write)

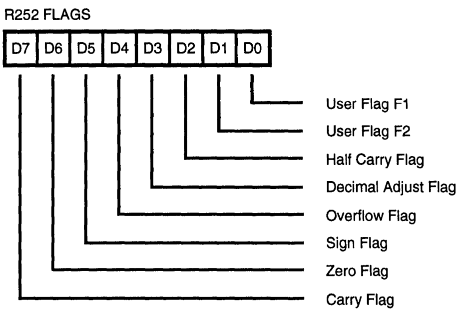


Figure 40. Flag Register (FCH: Read/Write)

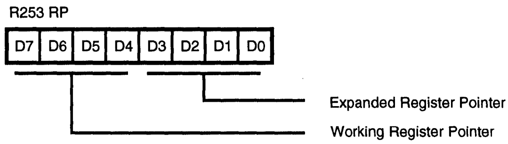


Figure 41. Register Pointer Register (FDH: Read/Write)

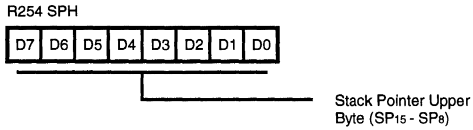


Figure 42. Stack Pointer Register (FEH: Read/Write)

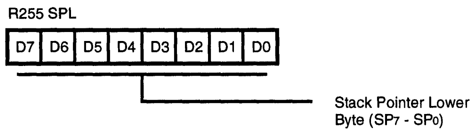


Figure 43. Stack Pointer Register (FFH: Read/Write)

Z8 EXPANDED REGISTER FILE CONTROL REGISTERS

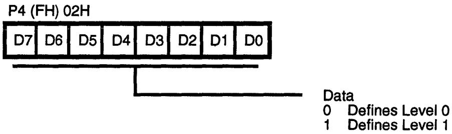


Figure 44. Port 4 Data Register (F)02: (Read/Write)

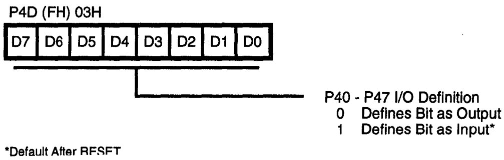


Figure 45. Port 4 Direction Register (F)03: (Write Only)

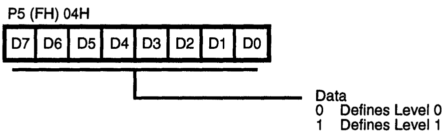


Figure 46. Port 5 Data Register (F)04: (Read/Write)

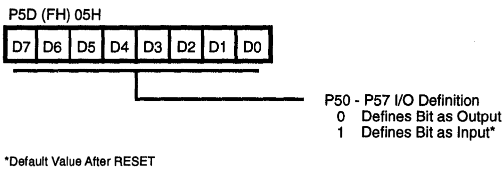


Figure 47. Port 5 Direction Register (F)05: (Write Only)

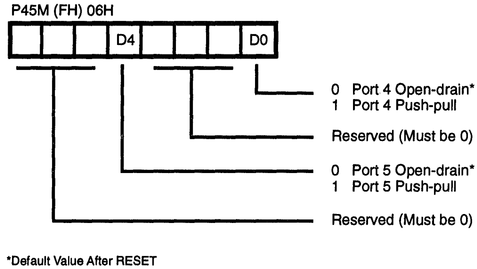


Figure 48. Port 4/5 Mode Register (F)06: (Write Only)

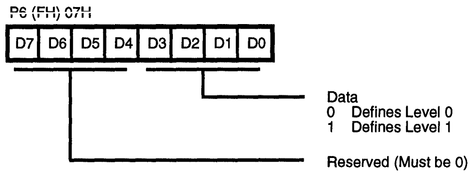


Figure 49. Port 6 Data Register (F)07: (Read/Write)

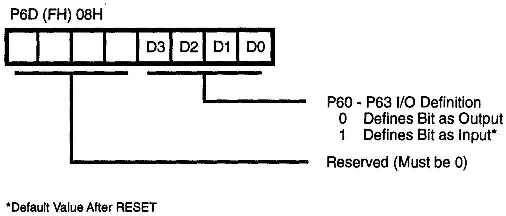


Figure 50. Port 6 Direction Register (F)08: (Read/Write)

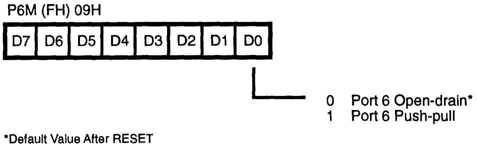


Figure 51. Port 6 Mode Register (F)09: (Write Only)

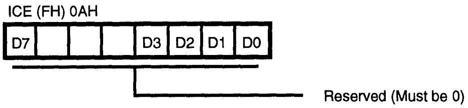


Figure 52. ICE Register (F)0A: (Write Only)

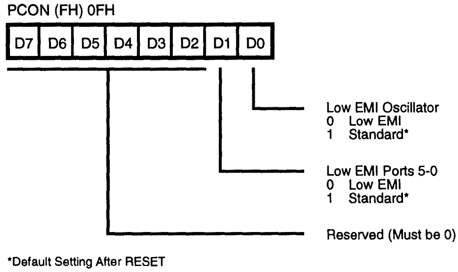


Figure 53. Port Configuration Register (F)0F: (Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

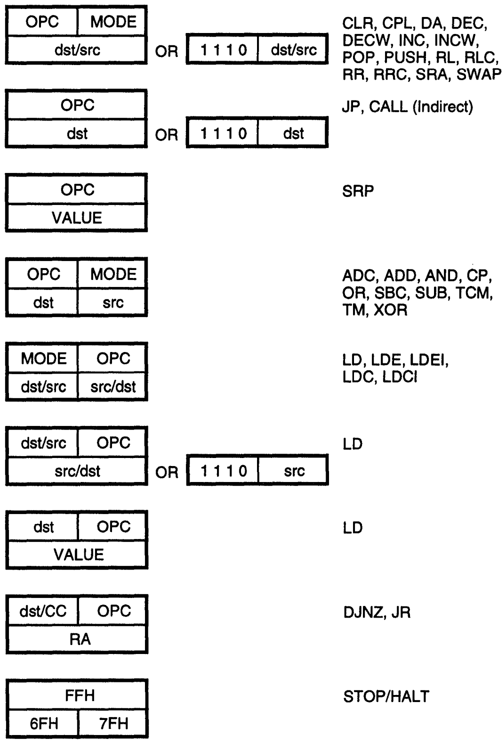
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

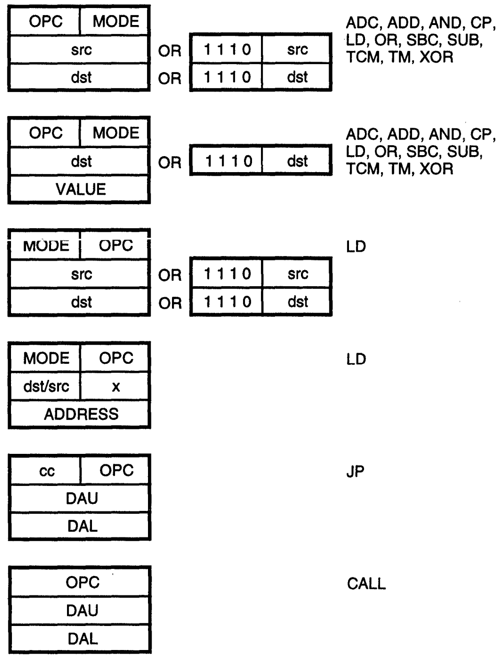
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†	1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†	0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†	5[ ]	- * * 0 - -
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR	D6 D4	- - - - - -
CCF C←NOT C		EF	* - - - - -
CLR dst dst←0	R IR	B0 B1	- - - - - -
COM dst dst←NOT dst	R IR	60 61	- * * 0 - -
CP dst, src dst – src	†	A[ ]	* * * * - -
DA dst dst←DA dst	R IR	40 41	* * * X - -
DEC dst dst←dst – 1	R IR	00 01	- * * * - -
DECW dst dst←dst – 1	RR IR	80 81	- * * * - -
DI IMR(7)←0		8F	- - - - - -
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA	rA r = 0 - F	- - - - - -
EI IMR(7)←1		9F	- - - - - -
HALT		7F	- - - - - -
INC dst dst←dst + 1	r R IR	rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR	A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1		BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR	cD c = 0 – F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA	cB c = 0 – F	- - - - - -
LD dst, src dst←src	r Im r R R r r X X r r Ir Ir r R R R IR R IM IR IM IR R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r Irr	C2	- - - - - -
LDCI dst, src dst←src r←r + 1; rr←rr + 1	Ir Irr	C3	- - - - - -

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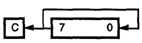
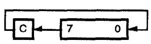
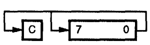
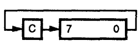
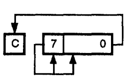
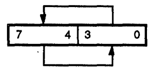
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - - -
STOP		6F	1 - - - - -
SUB dst, src dst←dst←src	†	2[ ]	[[[[1 [
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

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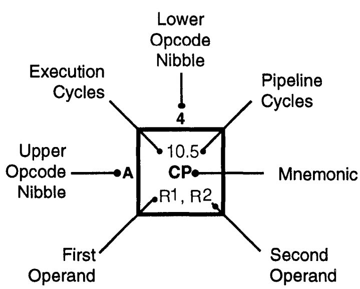
OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM	↓	↓	↓	↓	↓	↓	↓	
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**

Bytes per Instruction	0–3	4–7	8–C	D	E–F
	2	3	2	3	1



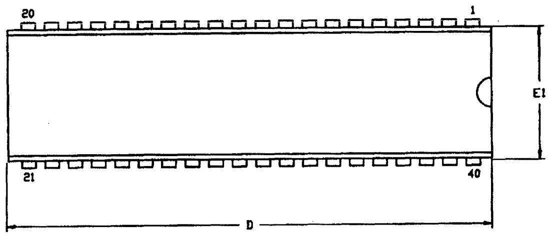
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

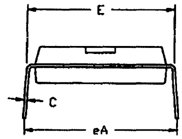
Sequence:
Opcode, First Operand, Second Operand

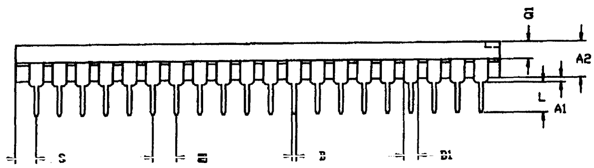
Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



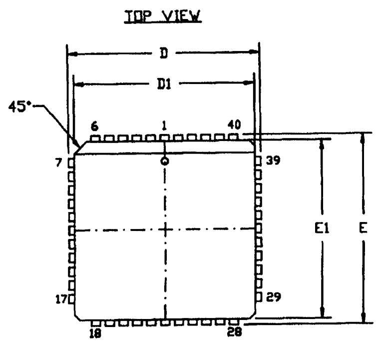


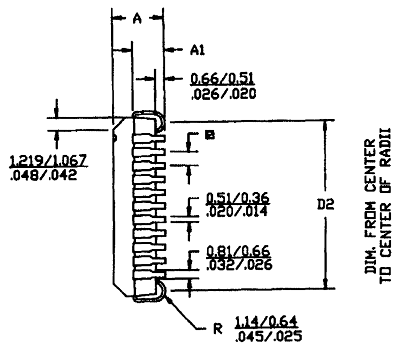


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
▣	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin Plastic DIP Package



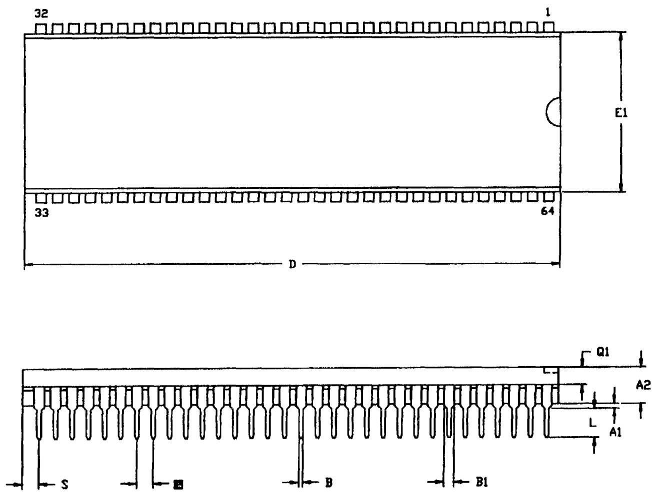


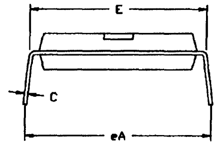
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
▣	1.27 TYP		.050 TYP	

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

44-Pin PLCC Package



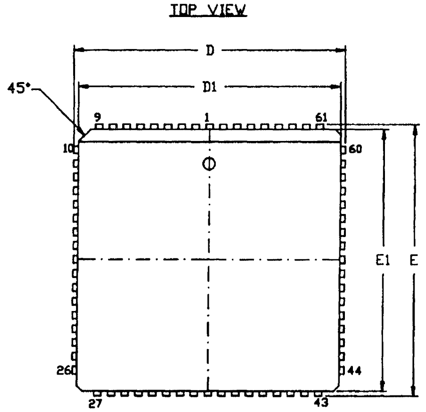


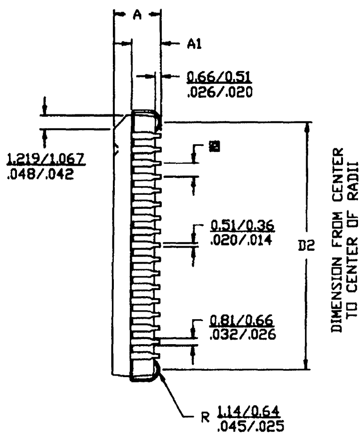
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
■	1.78 TYP		.070 TYP	
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070

CONTROLLING DIMENSIONS : INCH

64-Pin Plastic DIP Package

TOP VIEW





NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.67	2.92	.105	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
■	1.27 TYP		.050 TYP	

68-Pin PLCC Package

ORDERING INFORMATION

Z86C63/64

16 MHz

40-pin DIP	**44-pin PLCC**
Z86C6316PSC	Z86C6316VSC

16 MHz

64-pin DIP	**68-pin PLCC**
Z86C6416PSC	Z86C6416VSC

20 MHz

64-pin DIP	**68-pin PLCC**
Z86C6420PSC	Z86C6420VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
V = Plastic Chip Carrier

Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speed
16 = 16 MHz
20 = 20 MHz

Environmental
C = Plastic Standard

Example:
Z 86C63 16 P S C is an 86C63, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 16 — Speed
- 86C63 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller

7

Z86C61/62/96 CMOS Z8®
Microcontroller

8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller

9

Z86C91 CMOS Z8®
ROMless Microcontroller

10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller

11

Support Products

12

Superintegration™
Products Guide

S

Zilog's Literature Guide
Ordering Information

L

Z86C91

CMOS Z8® ROMLESS MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, or 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low Power Consumption - 275 mW (max) @ 20 MHz
- Fast Instruction Pointer - 1.0 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 24 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- ROMless
- 256 Byte Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes Control and Status Register
  - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds 12, 16, and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86C91 microcontroller (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C91 is a member of the ROMless Z8 single-chip microcontroller family with 236 bytes of RAM.

The MCU is packaged in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP, and is manufactured in CMOS technology. The Z86C91 is a ROMless part and offers the use of external memory which enables this Z8 microcontroller to be used where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C91 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provided timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C91 offers two on-chip counter/timers with a large number of user selectable modes, and a universal asynchronous receiver/transmitter (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

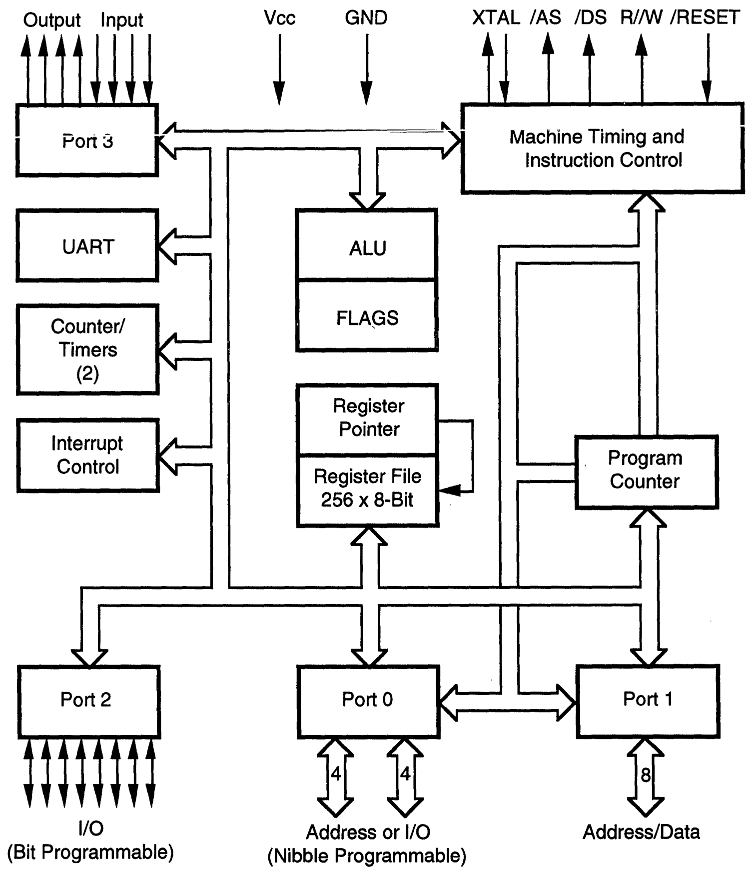


Figure 1. Functional Block Diagram

PIN DESCRIPTION

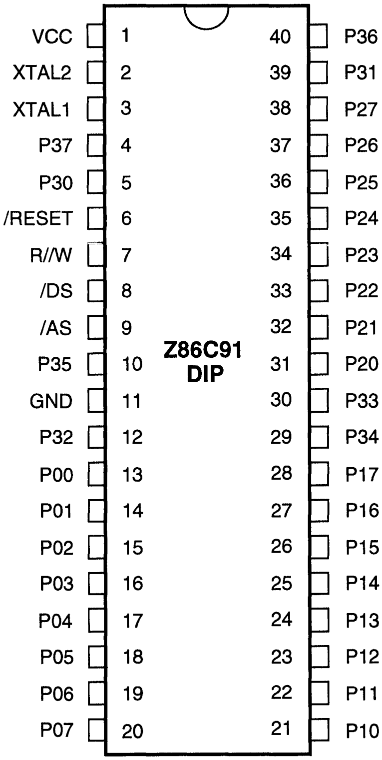


Figure 2. 40-Pin DIP Pin Assignments

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pins 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

10

PIN DESCRIPTION (Continued)

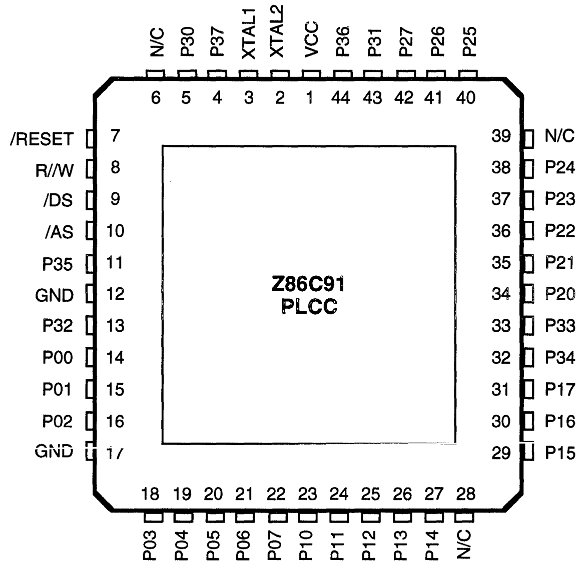


Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0 pins 0,1,2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	GND	Ground	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0 pins 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pins 0,1,2,3,4	In/Output
5	P30	Port 3 pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1 pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3 pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3 pin 5	Output	40-42	P25-P27	Port 2 pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3 pin 1	Input
13	P32	Port 3 pin 2	Input	44	P36	Port 3 pin 6	Output

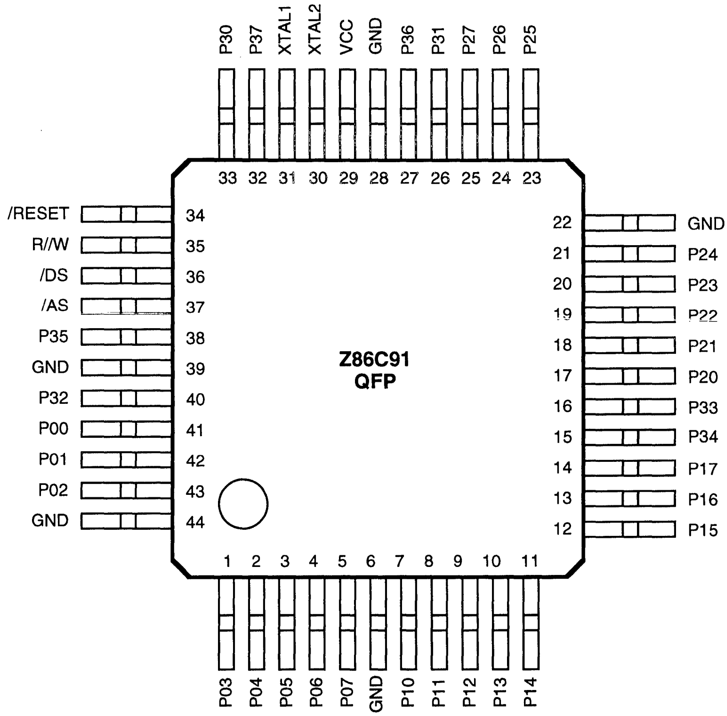


Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 pins 3,4,5,6,7	In/Output	31	XTAL1	Crystal, Oscillator Clock	Input
6	GND	Ground	Input	32	P37	Port 3 pin 7	Output
7-14	P10-P17	Port 1 pins 0,1,2,3,4,5,6,7	In/Output	33	P30	Port 3 pin 0	Input
15	P34	Port 3 pin 4	Output	34	/RESET	Reset	Input
16	P33	Port 3 pin 3	Input	35	R//W	Read/Write	Output
17-21	P20-P24	Port 2 pins 0,1,2,3,4	In/Output	36	/DS	Data Strobe	Output
22	GND	Ground	Input	37	/AS	Address Strobe	Output
23-25	P25-P27	Port 2 pins 5,6,7	In/Output	38	P35	Port 3 pin 5	Output
26	P31	Port 3 pin 1	Input	39	GND	Ground	Input
27	P36	Port 3 pin 6	Output	40	P32	Port 3 pin 2	Input
28	GND	Ground	Input	41-43	P00-P02	Port 0 pins 0,1,2	In/Output
29	V_{CC}	Power Supply	Input	44	GND	Ground	Input
30	XTAL2	Crystal, Oscillator Clock	Output				

PIN FUNCTIONS

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external program. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read//Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C91 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC2. When /RESET is deactivated program, execution begins at location 000C (HEX). Power-up reset time is held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 provides Address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 5).

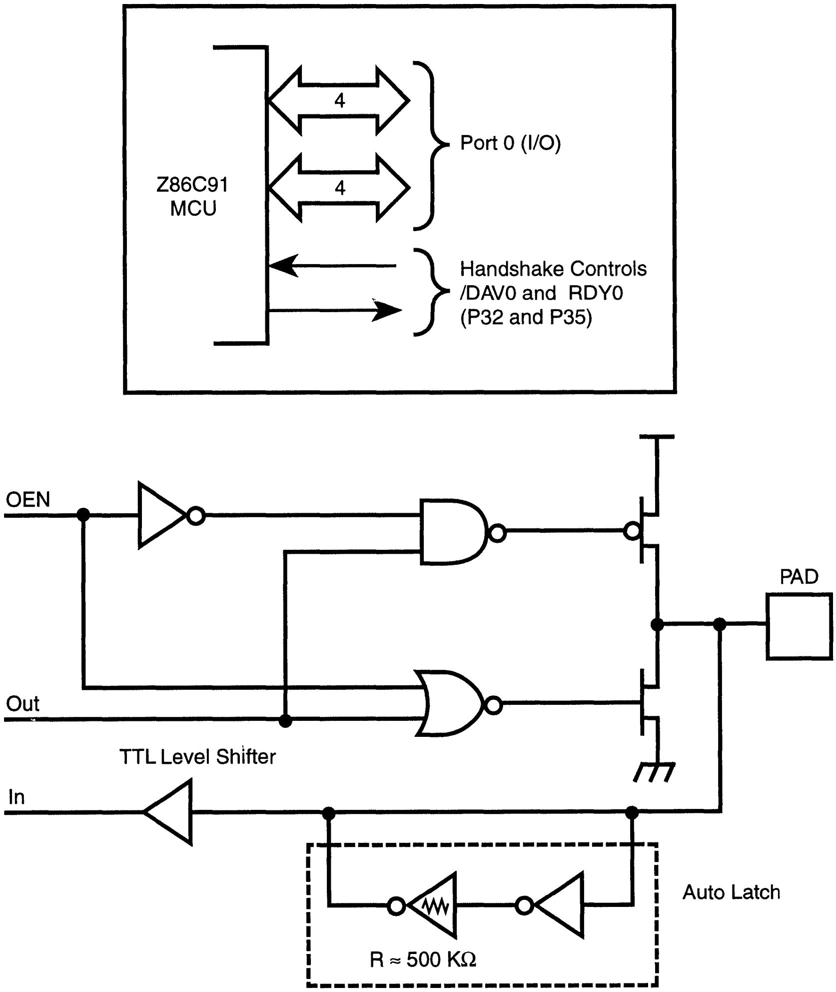


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory.

If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in a high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 6).

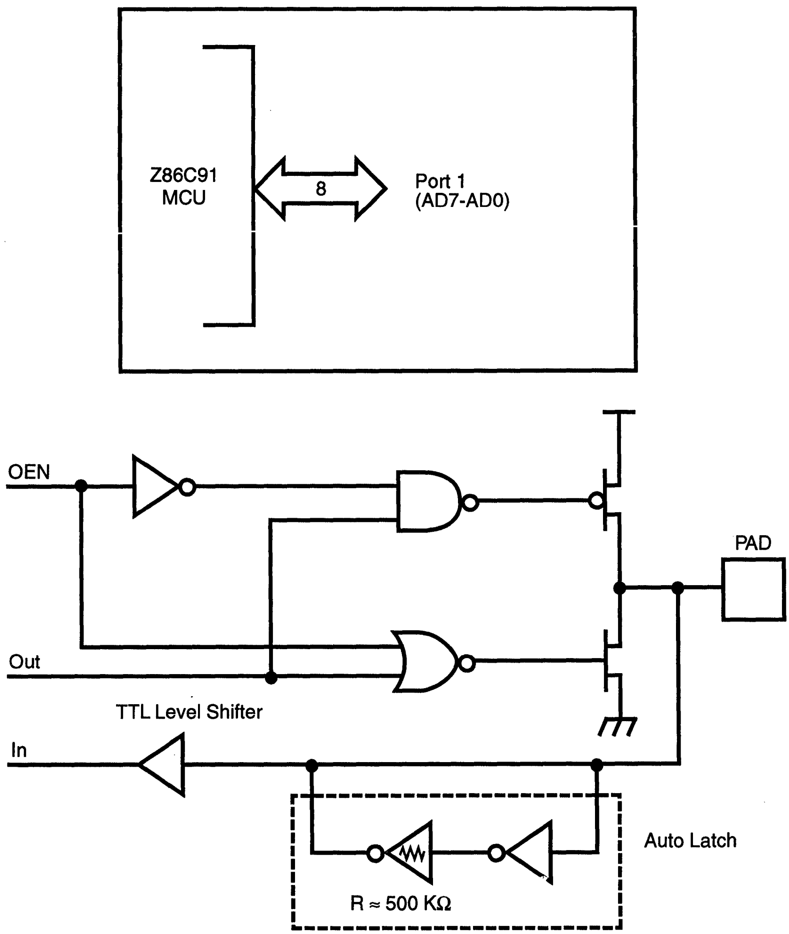


Figure 6. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7).

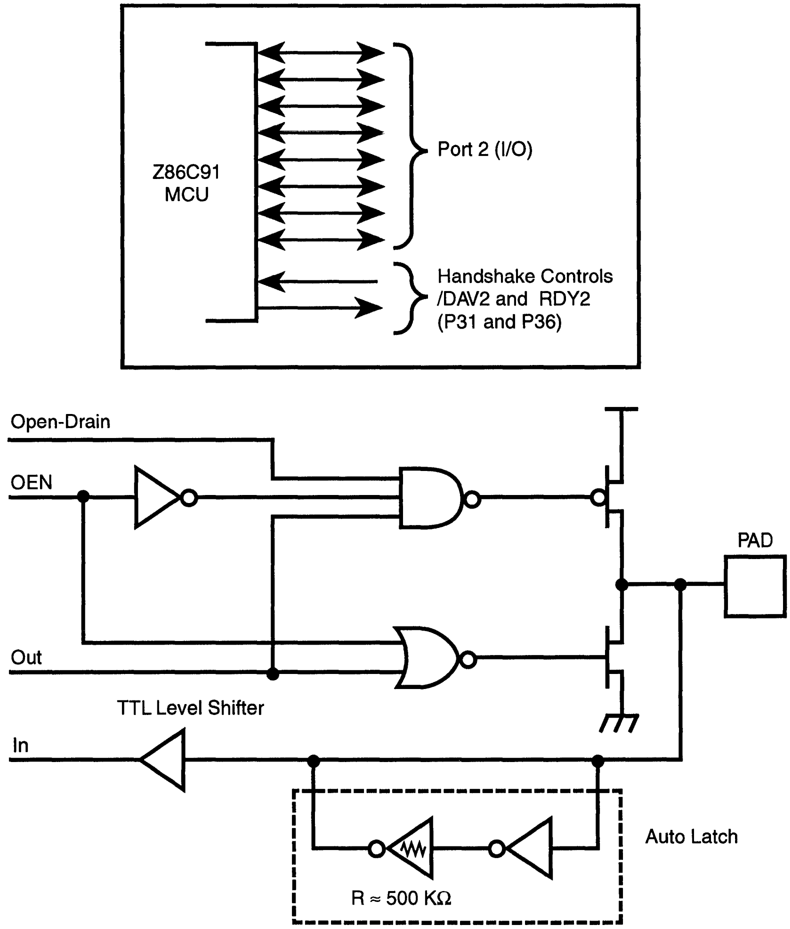


Figure 7. Port 2 Configuration

PIN FUNCTION (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four fixed (P37-P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 8). Port 3 inputs only are designed with Auto Latches.

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM) (Table 4.)

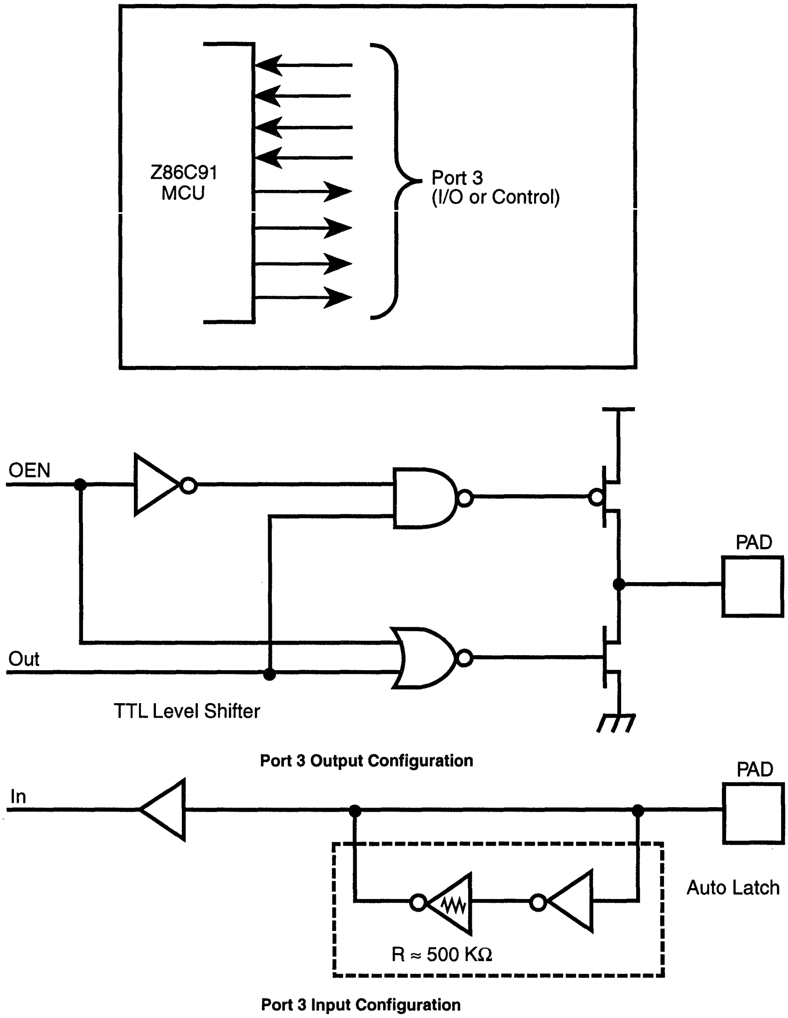


Figure 8. Port 3 Configuration

Table 4. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = HANDSHAKE SIGNALS
D = Data Available
R = Ready

UART OPERATION

Port 3 lines P30 and P37, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C91 automatically adds a start bit and two stop bits to transmitted data (Figure 9). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

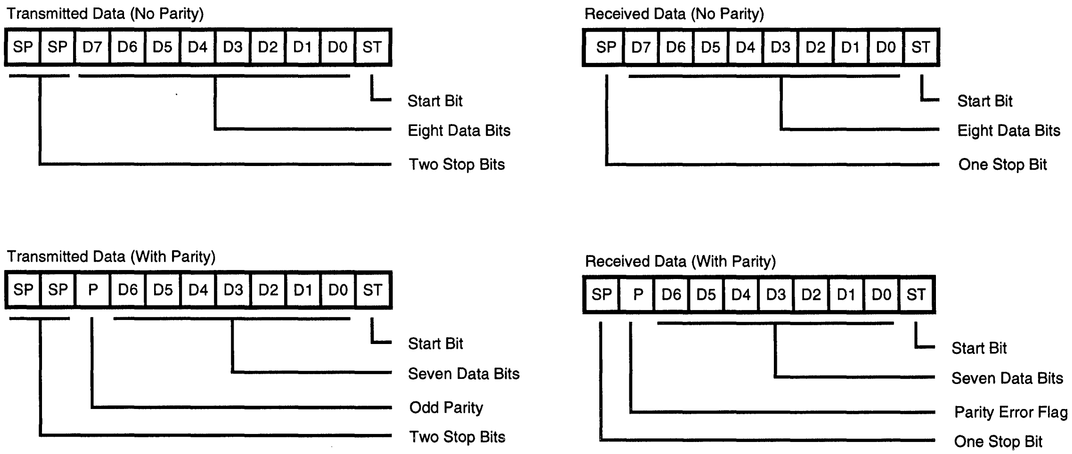


Figure 9. Serial Data Formats

FUNCTIONAL DESCRIPTION
Address Space

Program Memory. The Z86C91 can address up to 64 Kbytes of external program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location 000CH after a reset.

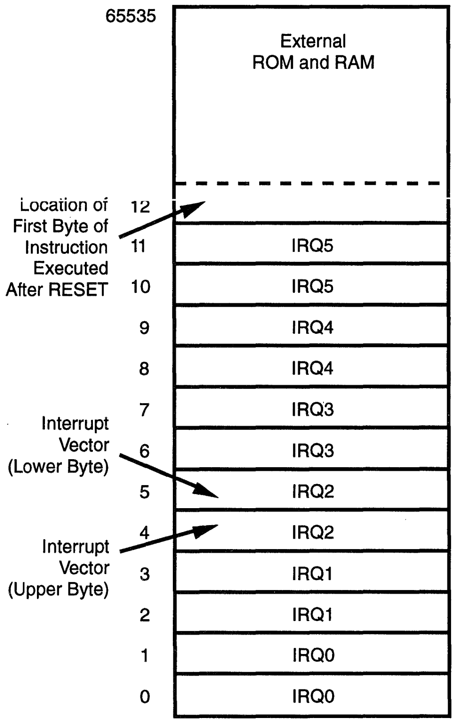


Figure 10. Program Memory Configuration

Data Memory (/DM). The Z86C91 addresses up to 64 Kbytes of external data memory space. External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34, is used to distinguish between data and program memory space (Figure 11). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

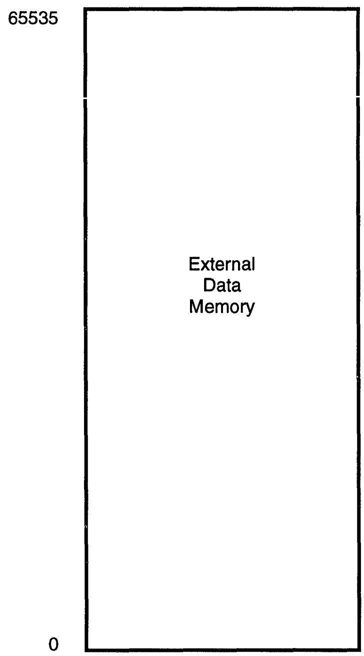


Figure 11. Data Memory Configuration

Register File. The Register File consists of three I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 12). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 13). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group. For the reset and power-up conditions of the Register File see Figure 14.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239 … R4	General-Purpose Registers	
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Figure 12. Register File

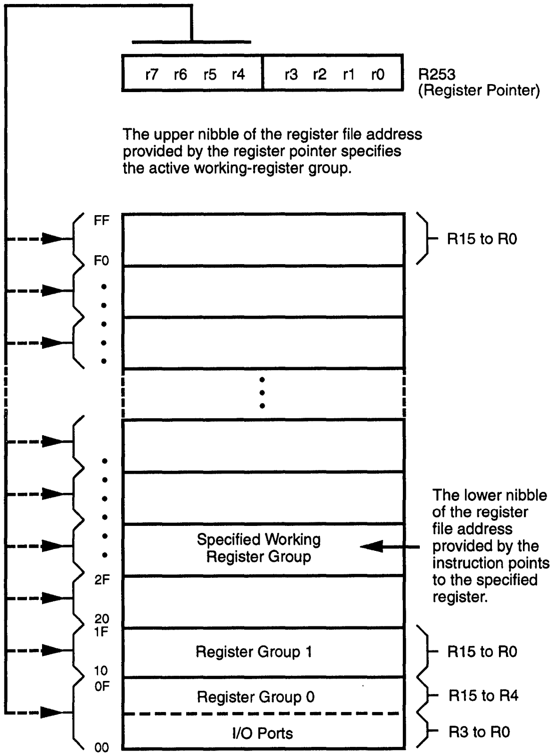
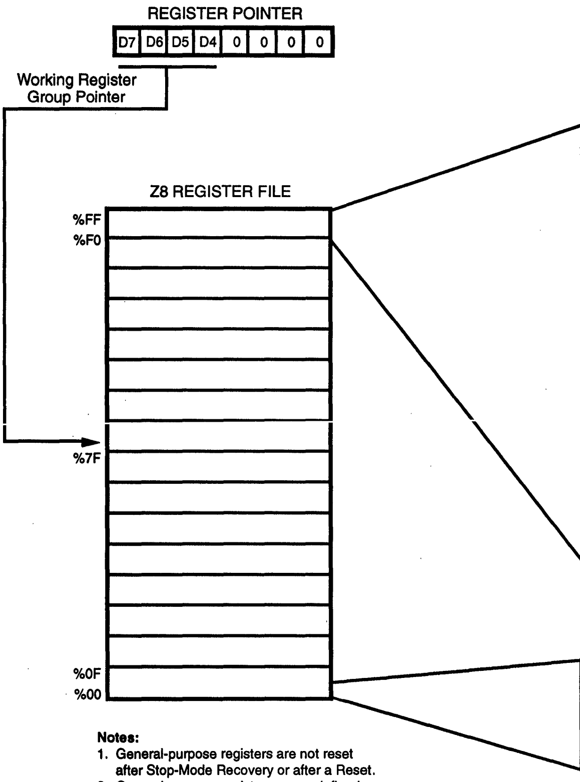


Figure 13. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)



Z8 STANDARD CONTROL REGISTERS

REGISTER		RESET CONDITION D7	D6	D5	D4	D3	D2	D1	D0
% FF	SPL	U	U	U	U	U	U	U	U
% FE	SPH	U	U	U	U	U	U	U	U
% FD	RP	U	U	U	U	U	U	U	U
% FC	FLAGS	U	U	U	U	U	U	U	U
% FB	IMR	0	U	U	U	U	U	U	U
% FA	IRQ	0	0	0	0	0	0	0	0
% F9	IPR	U	U	U	U	U	U	U	U
% F8	P01M	1	0	1	1	0	1	1	0
% F7	P3M	0	0	0	0	0	0	0	0
% F6	P2M	1	1	1	1	1	1	1	1
% F5	PRE0	U	U	U	U	U	U	U	0
% F4	T0	U	U	U	U	U	U	U	U
% F3	PRE1	U	U	U	U	U	U	0	0
% F2	T1	U	U	U	U	U	U	U	U
% F1	TMR	0	0	0	0	0	0	0	0
% F0	S10	U	U	U	U	U	U	U	U

REGISTER		RESET CONDITION							
% (0) 03	P3	1	1	1	1	U	U	U	U
% (0) 02	P2	U	U	U	U	U	U	U	U
% (0) 01	P1	U	U	U	U	U	U	U	U
% (0) 00	P0	U	U	U	U	U	U	U	U

Notes:
1. General-purpose registers are not reset after Stop-Mode Recovery or after a Reset.
2. General-purpose registers are undefined after Power-up.

U = Unknown

Figure 14. RAM Register File Reset Condition

Stack. The Z86C91 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The High byte of the Stack Pointer (SPH-Bit 8-15) is used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1 or sub the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1

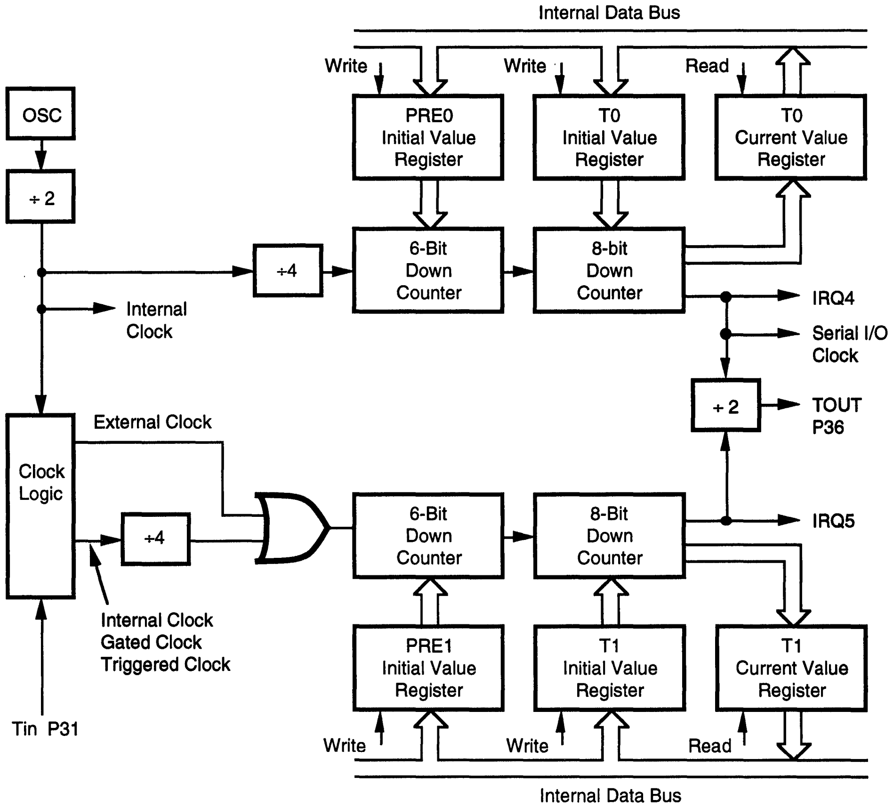


Figure 15. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C91 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follow: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (Refer to Table 4).

All Z86C91 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

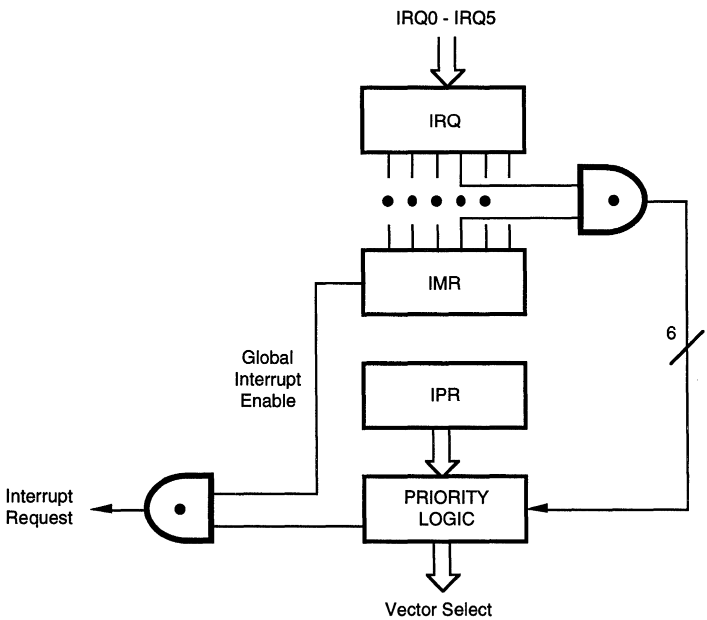


Figure 16. Interrupt Block Diagram

Clock. The Z86C91 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 300 pF) from each pin 11 ground instead of just the system ground. This prevents noise injection into the clock inputs (Figure 17).

Note: Actual capacitor values specified by the crystal manufacturer.

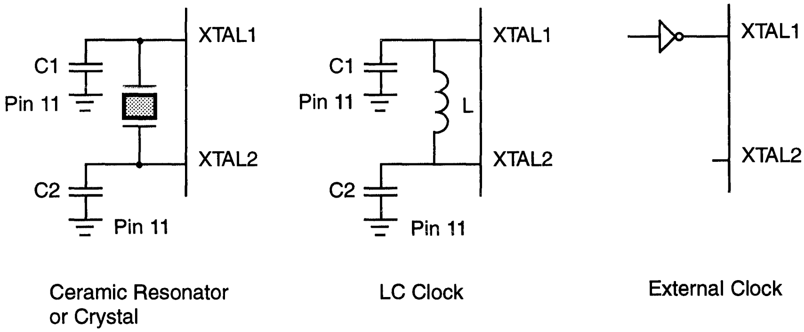


Figure 17. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset, which cause the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = OFFH) immediately before the appropriate sleep instruction, i.e.,

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp		†	°C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).

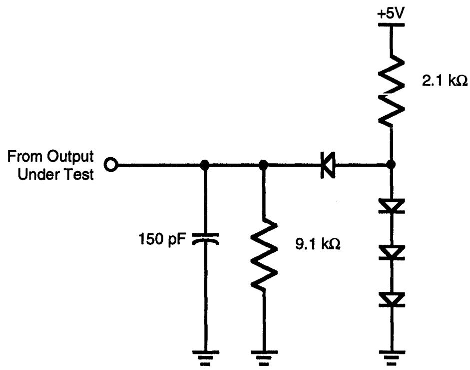


Figure 18. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC}+0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC}+0.3	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = – 2.0 mA
V_{OH}	Output High Voltage	V_{CC} –100 mV		V_{CC} –100 mV			V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3	3.8	V_{CC}+0.3		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	V_{RL} = 0V
I_{CC}	Supply Current		30		30	20	mA	@ 12 MHz [1]
			35		35	24	mA	@ 16 MHz [1]
			50		50		mA	@ 20 MHz [1]
I_{CC1}	Standby Current		6.5		6.5	4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz [1]
			7		7	4.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 16 MHz [1]
			8.5		8.5		mA	HALT mode V_{IN} = 0V, V_{CC} @ 20 MHz [1]
I_{CC2}	Standby Current		10		20	1	µA	STOP mode V_{IN} = 0V, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	–10	10	–14	14	5	µA	

Note:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.

10

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram

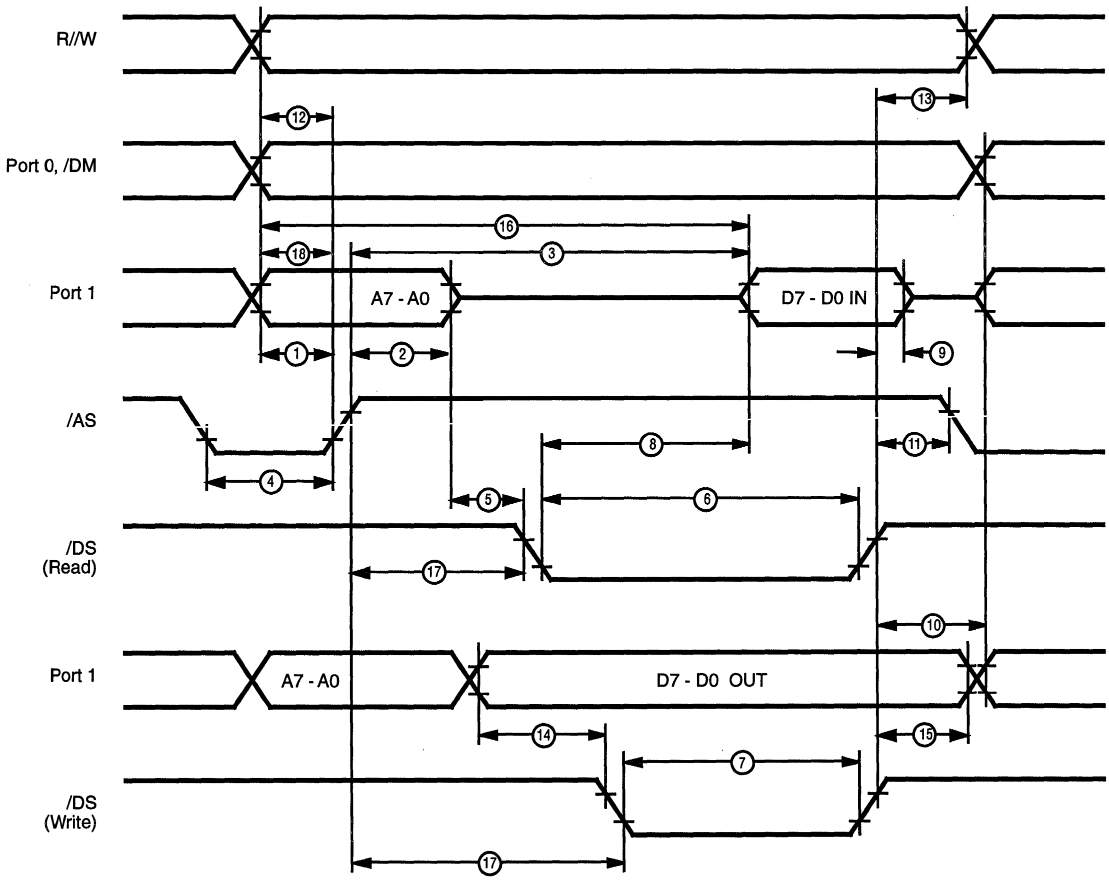


Figure 19. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
External I/O or Memory Read or Write Timing Table

			T_A = 0°C to +70°C						T_A = –40°C to +105°C							
			12 MHz		16 MHz		20 MHz		12 MHz		16 MHz		20 MHz			
No	Sym	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		25		20		35		25		20		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		35		25		45		35		25		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		250		180		150		250		180		150	ns	[1,2,3]
4	TwAS	/AS Low Width	55		40		30		55		40		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		105		185		135		105		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		65		110		80		65		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		55		130		75		55	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	65		50		40		65		50		40		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	45		35		25		45		35		25		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		25		20		33		25		20		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	50		35		25		50		35		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		20		35		25		20		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	55		35		25		55		35		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		310		230		180		310		230		180	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	65		45		35		65		45		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Rise Delay	50		30		20		50		30		20		ns	[2,3]

Notes:
[1] When using extended memory timing add 2TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
Standard Test Load
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC – 3.25
3	TdAS(DR)	2.38TpC + 6.14
4	TwAS	0.66TpC – 1.65
6	TwDSR	2.33TpC – 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC – 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC – 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC – 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC – 19
16	TdA(DR)	4TpC – 20
17	TdAS(DS)	0.91TpC – 10.7
18	TdDM(AS)	0.9TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

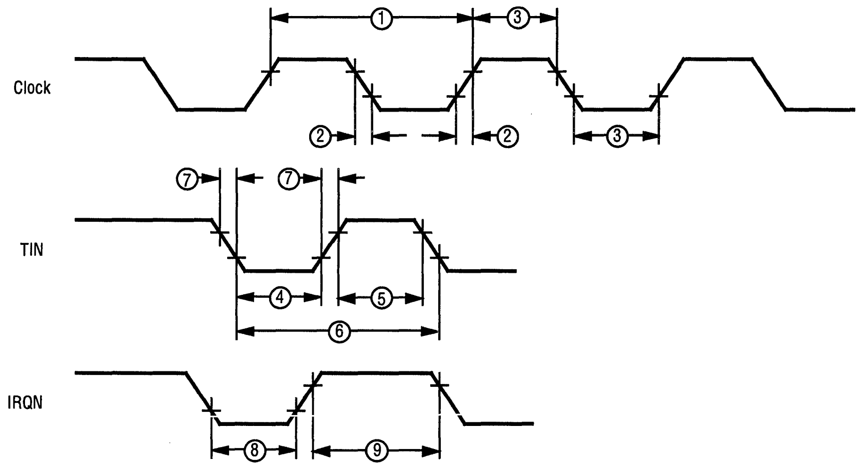


Figure 20. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

			T_A = 0°C to +70°C						T_A = −40°C to +105°C							
			12 MHz		16 MHz		20 MHz		12 MHz		16 MHz		20 MHz			
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	83	1000	62.5	1000	50	1000	83	1000	62.5	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		10		15		10		10	ns	[1]
3	TwC	Input Clock Width	35		25		15		35		25		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	5TpC		5TpC		5TpC		5TpC		5TpC		5TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC		5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC		5TpC		5TpC		5TpC		5TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

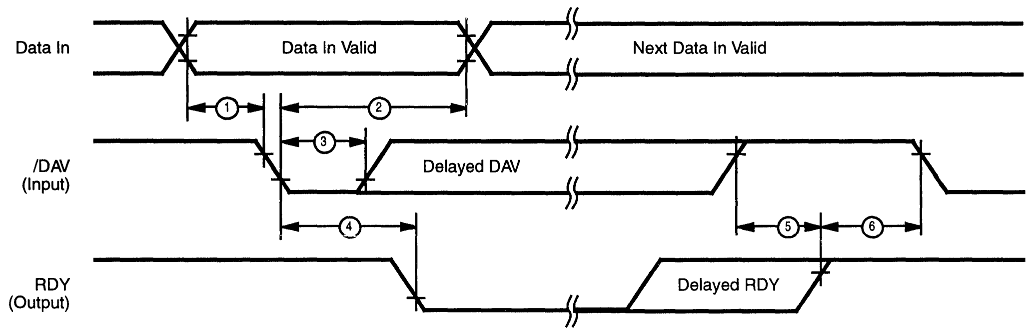


Figure 21. Input Handshake Timing

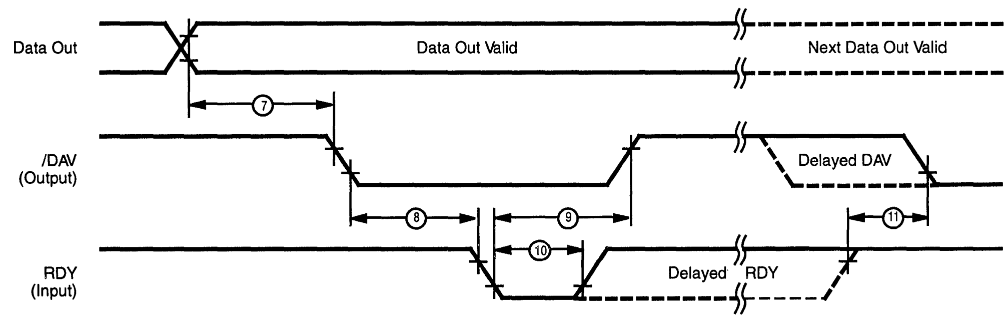


Figure 22. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Sym	Parameter	T_A = 0°C to +70°C 12, 16, and 20 MHz Min	Max	T_A = –40°C to +105°C 12, 16, and 20 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay		115		115	IN
6	TdRDYO(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay		TpC		TpC	OUT
8	TdDAVO(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDYO(DAV)	RDY fall to DAV rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDYOd(DAV)	RDY rise to DAV fall Delay		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

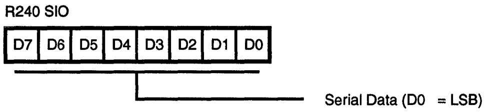


Figure 23. Serial I/O Register (F0H: Read/Write)

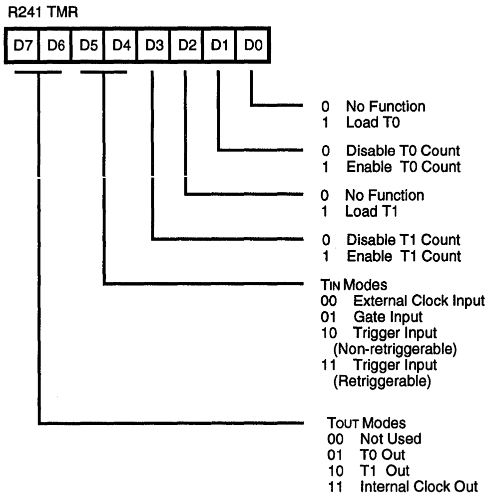


Figure 24. Timer Mode Register (F1H: Read/Write)

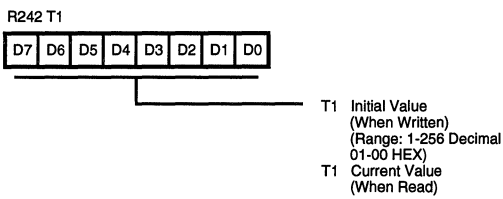


Figure 25. Counter/Timer 1 Register (F2H: Read/Write)

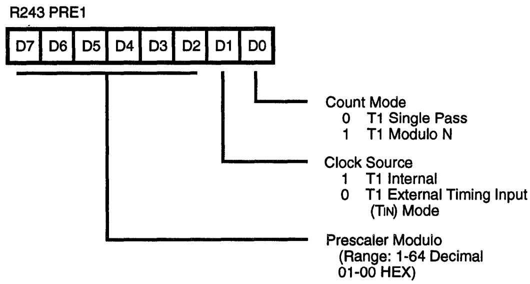


Figure 26. Prescaler 1 Register (F3H: Write Only)

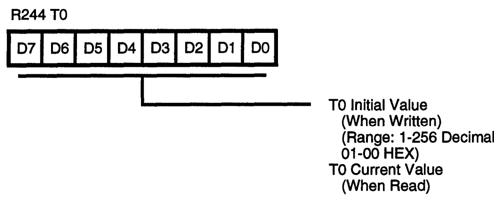


Figure 27. Counter/Timer 0 Register (F4H: Read/Write)

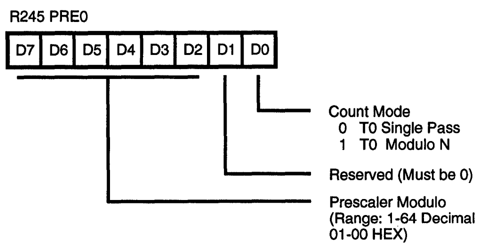


Figure 28. Prescaler 0 Register (F5H: Write Only)

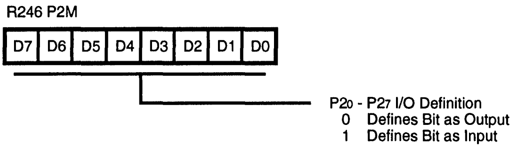


Figure 29. Port 2 Mode Register (F6H: Write Only)

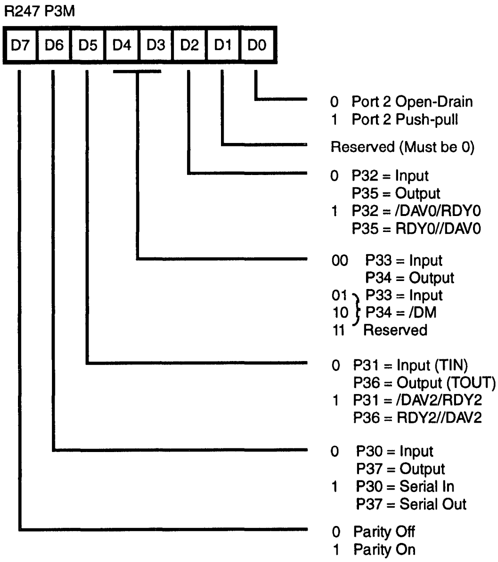


Figure 30. Port 3 Mode Register (F7H: Write Only)

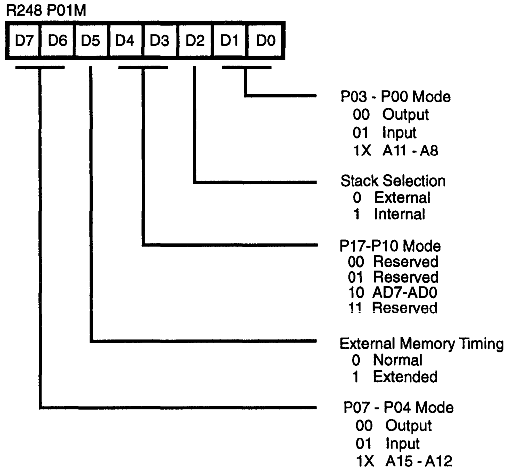


Figure 31. Port 0 and 1 Mode Register (F8H: Write Only)

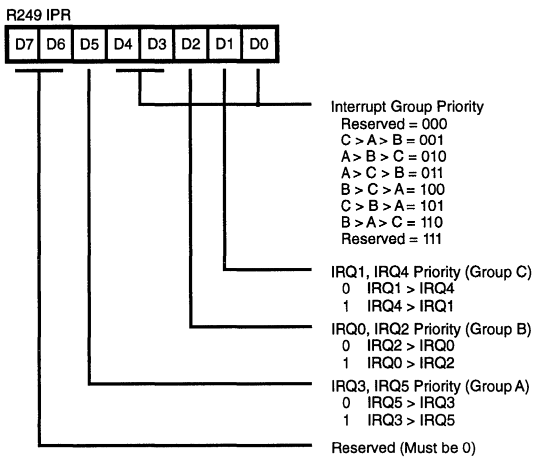


Figure 32. Interrupt Priority Register (F9H: Write Only)

10

Z8 CONTROL REGISTER DIAGRAMS (Continued)

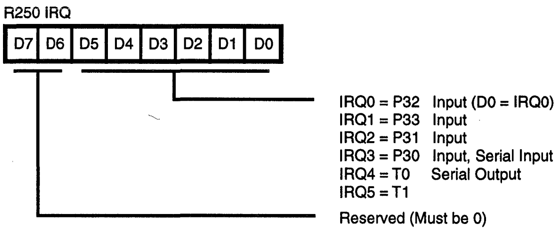


Figure 33. Interrupt Request Register (FAH: Read/Write)

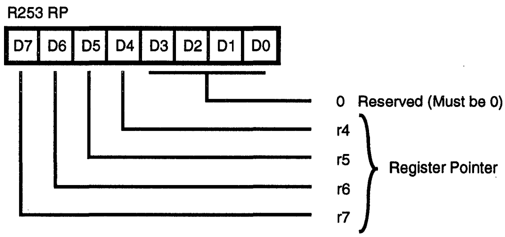


Figure 36. Register Pointer Register (FDH: Read/Write)

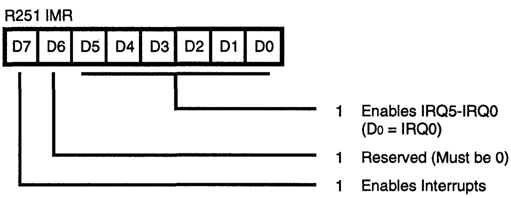


Figure 34. Interrupt Mask Register (FBH: Read/Write)

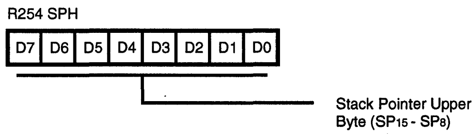


Figure 37. Stack Pointer Register (FEH: Read/Write)

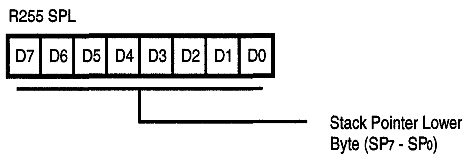


Figure 38. Stack Pointer Register (FFH: Read/Write)

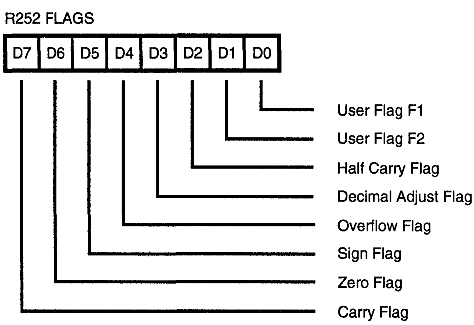


Figure 35. Flag Register (FCH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS

Format	Instructions
OPC	CCF, DI, EI, IRET, NOP, RCF, RET, SCF
dst | OPC	

One-Byte Instructions

Format	OR	Instructions
OPC | MODE dst/src	1 1 1 0 | dst/src	CLR, CPL, DA, DEC, DECW, INC, INCW, POP, PUSH, RL, RLC, RR, RRC, SRA, SWAP
OPC dst	1 1 1 0 | dst	JP, CALL (Indirect)
OPC VALUE		SRP
OPC | MODE dst | src		ADC, ADD, AND, CP, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC dst/src | src/dst		LD, LDE, LDEI, LDC, LDCI
dst/src | OPC src/dst	1 1 1 0 | src	LD
dst | OPC VALUE		LD
dst/CC | OPC RA		DJNZ, JR
FFH 6FH | 7FH		STOP/HALT

Two-Byte Instructions

Format	OR	Instructions
OPC | MODE src dst	 1 1 1 0 | src 1 1 1 0 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
OPC | MODE dst VALUE	 1 1 1 0 | dst	ADC, ADD, AND, CP, LD, OR, SBC, SUB, TCM, TM, XOR
MODE | OPC src dst	 1 1 1 0 | src 1 1 1 0 | dst	LD
MODE | OPC dst/src | x ADDRESS		LD
cc | OPC DAU DAL		JP
OPC DAU DAL		CALL

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

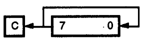
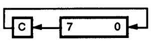
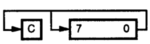
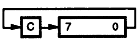
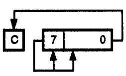
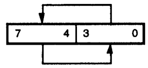
dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

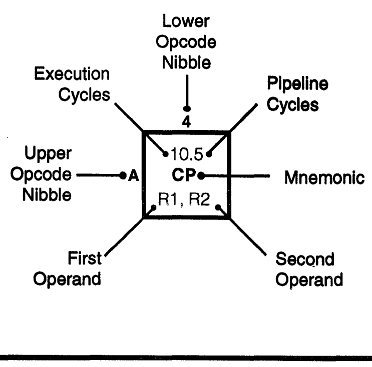
Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) / **Upper Nibble (Hex)**

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**

Bytes per Instruction: 2 (lower nibble 0–3), 3 (lower nibble 4–7), 2 (lower nibble 8–C), 3 (lower nibble D), 1 (lower nibble E–F)



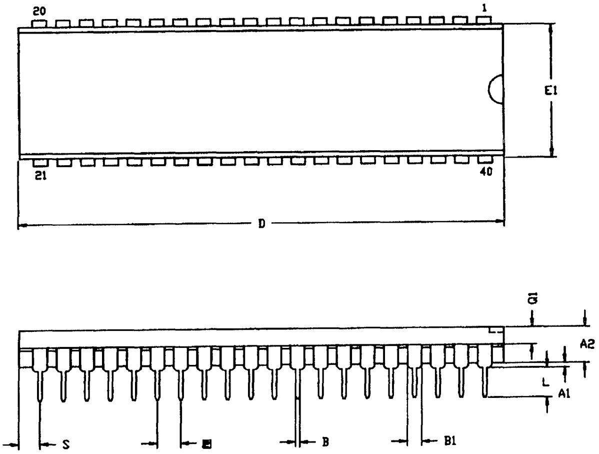
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

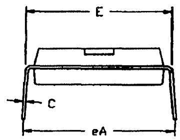
Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

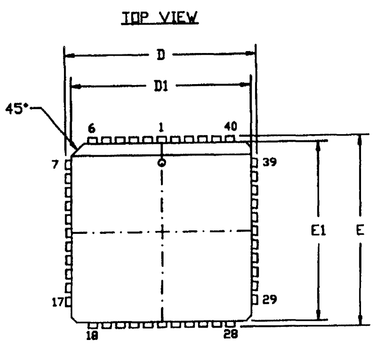


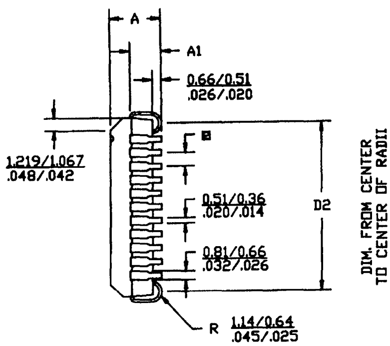


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



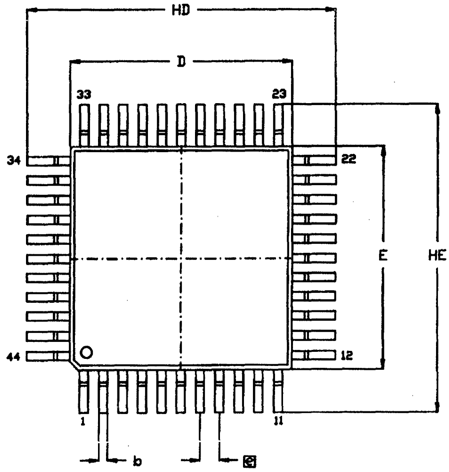


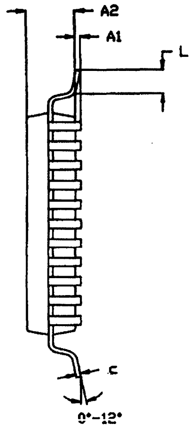
NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)





NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C91

12 MHz

40-pin DIP	**44-pin PLCC**	**44-pin QFP**
Z86C9112PSC	Z86C9112VSC	Z86C9112FSC
Z86C9112PEC	Z86C9112VEC	Z86C9112FEC

16 MHz

40-pin DIP	**44-pin PLCC**	**44-pin QFP**
Z86C9116PSC	Z86C9116VSC	Z86C9116FSC

20 MHz

40-pin DIP	**44-pin PLCC**	**44-pin QFP**
Z86C9120PSC	Z86C9120VSC	Z86C9120FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speed
12 = 12 MHz
16 = 16 MHz
20 = 20 MHz

Environmental
C = Plastic Standard

Example:
Z 86C91 12 P S C is a Z86C91, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86C91 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller
7

Z86C61/62/96 CMOS Z8®
Microcontroller
8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller
9

Z86C91 CMOS Z8®
ROMless Microcontroller
10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller
11

Support Products
12

Superintegration™
Products Guide
S

Zilog's Literature Guide
Ordering Information
L

Z86C93

CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

FEATURES

- Complete Microcontroller, up to 24 I/O lines, and up to 64 Kbytes of Addressable External Space each for Program and Data Memory.
- 16 x 16-Bit Hardwired Multiplier with 32-Bit Product in 17 Clock Cycles.
- 32 x 16-Bit Hardwired Divider with 16-Bit Quotient and 16-Bit Remainder in 20 Clock Cycles.
- 256-Byte Register File, Including 236 General-Purpose Registers, up to Three I/O Port Registers, and 16 Status and Control Registers.
- 17-Byte Expanded Register File, Including Two General-Purpose Registers and 15 Status and Control Registers.
- Two 16-Bit Counter Timers with 6-Bit Prescalers.
- Two Low Power Standby Modes, STOP and HALT
- On-Chip Oscillator that Accepts Crystal or External Clock Drive.
- Vectored, Priority Interrupts for I/O, Counter/Timers and UART.
- Three 16-Bit Counter/Timers with 4-Bit Prescaler, One Capture Register and a Fast Decrement Mode.
- Register Pointer for Short, Fast Instructions that can Access Any One of the 16 Working Register Groups.
- Additional Emulation Signals SCLK, IACK, and /SYNC are Made Available.
- Full-Duplex UART
- 3.3V ±10% Operation at 25 MHz
- 5.0V ±10% Operation at 20, 25, and 33 MHz

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8® microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin DIP, 44-pin PLCC, 44-pin QFP, and 48-pin VQFP (Figures 2, 3, 4, 5, and 6). Besides the four additional signals (SCLK, IACK, /SYNC, and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining eight bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into 16 groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and Counter/Timer blocks.

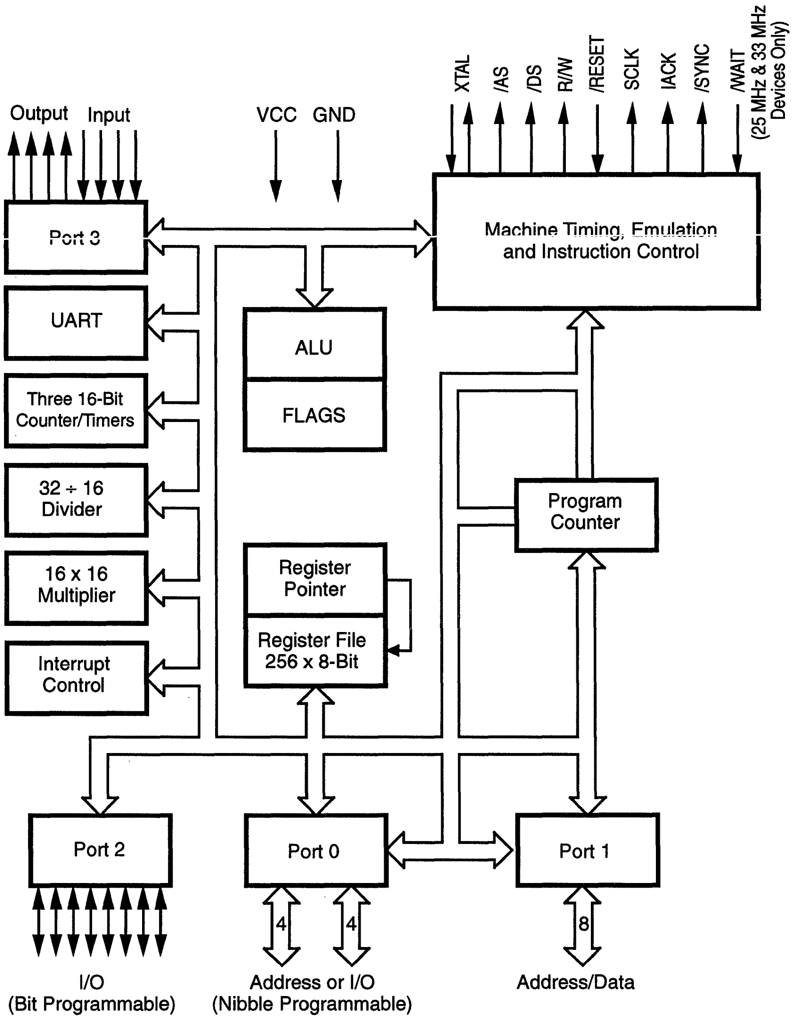


Figure 1. Functional Block Diagram

PIN DESCRIPTION

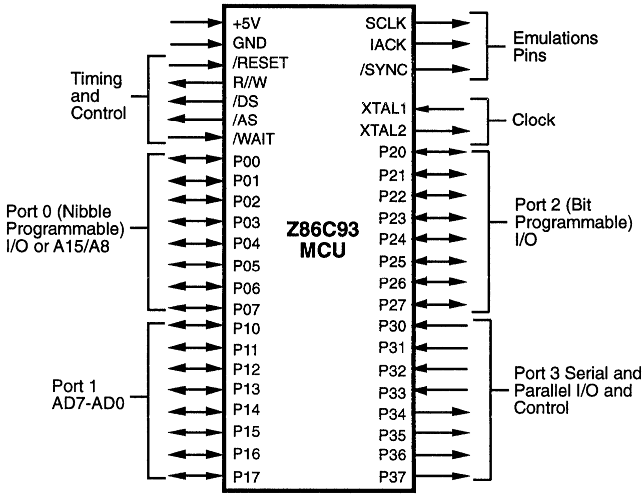


Figure 2. Z86C93 Pin Functions

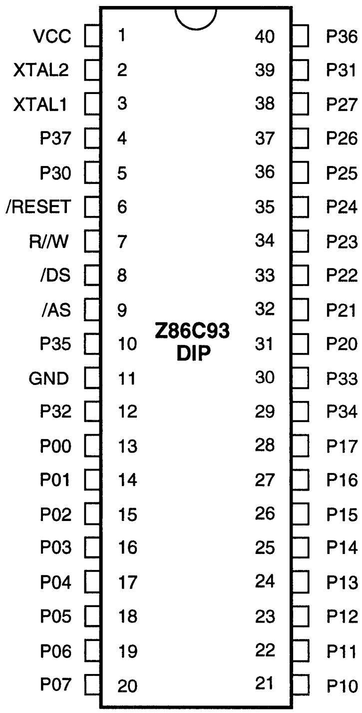


Figure 3. 40-Pin DIP Assignments

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL1	Crystal, Oscillator Clock	Input
3	XTAL2	Crystal, Oscillator Clock	Output
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-P27	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

11

PIN DESCRIPTION (Continued)

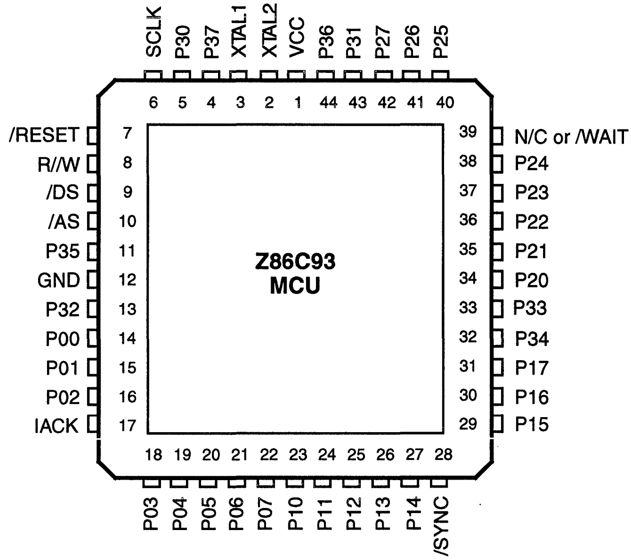


Figure 4. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0, Pins 0,1,2	In/Output
2	XTAL2	Crystal, Osc. Clock	Output	17	IACK	Int. Acknowledge	Output
3	XTAL1	Crystal, Osc. Clock	Input	18-22	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output
4	P37	Port 3, Pin 7	Output	23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
5	P30	Port 3, Pin 0	Input	28	/SYNC	Synchronize Pin	Output
6	SCLK	System Clock	Output	29-31	P15-P17	Port 1 Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3, Pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3, Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 Pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected (20 MHz)	Input
					/WAIT	WAIT (25 or 33 MHz)	Input
11	P35	Port 3, Pin 5	Output	40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3, Pin 1	Input
13	P32	Port 3, Pin 2	Input	44	P36	Port 3, Pin 6	Output

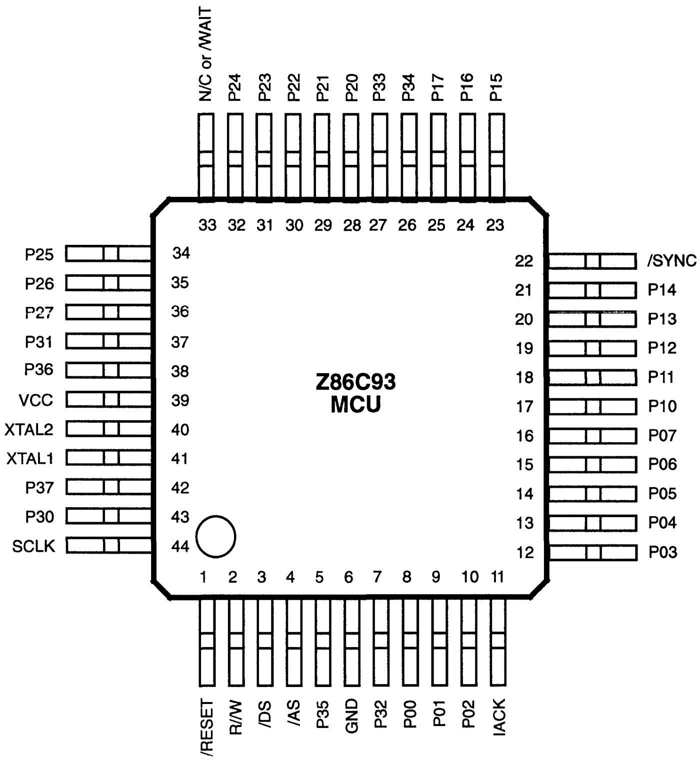


Figure 5. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

No	Symbol	Function	Direction
1	/RESET	Reset	Input
2	R//W	Read/Write	Output
3	/DS	Data Strobe	Output
4	/AS	Address Strobe	Output
5	P35	Port 3, Pin 5	Input
6	GND	Ground	Input
7	P32	Port 3, Pin 2	Input
8-10	P00-P02	Port 0, Pins 0,1,2	In/Output
11	IACK	Int. Acknowledge	Output
12-16	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output
17-21	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
22	/SYNC	Synchronize Pin	Output
23-25	P15-P17	Port 1, Pins 5,6,7	In/Output
26	P34	Port 3, Pin 4	Output
27	P33	Port 3, Pin 3	Input
28-32	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
33	N/C	Not Connected (20 MHz)	Input
	/WAIT	WAIT (25 or 33 MHz)	Input
34-36	P25-P27	Port 2, Pins 5,6,7	In/Output
37	P31	Port 3, Pin 1	Input
38	P36	Port 3, Pin 6	Output
39	V_{CC}	Power Supply	Input
40	XTAL2	Crystal, Osc. Clock	Output
41	XTAL1	Crystal, Osc. Clock	Input
42	P37	Port 3, Pin 7	Output
43	P30	Port 3, Pin 0	Input
44	SCLK	System Clock	Output

11

PIN DESCRIPTION (Continued)

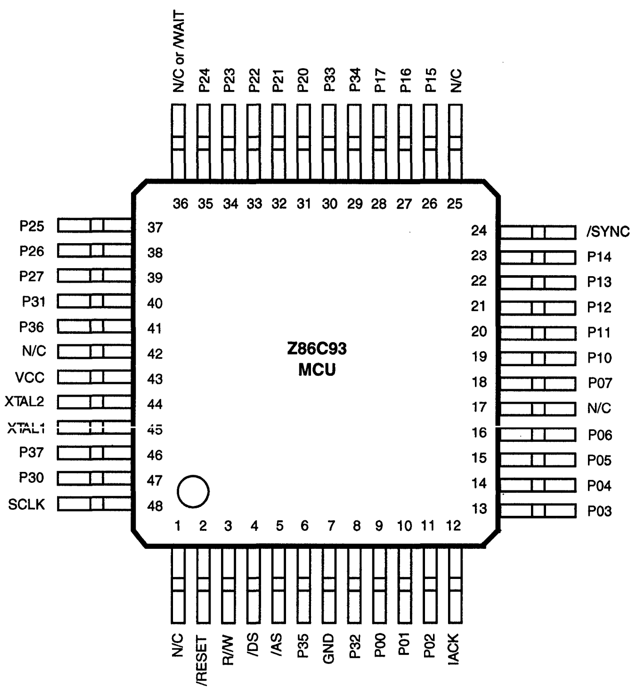


Figure 6. 48-Pin VQFP Pin Assignments

Table 4. 48-Pin VQFP Pin Identification

No	Symbol	Function	Direction
1	N/C	Not Connected	Input
2	/RESET	Reset	Input
3	R/W	Read/Write	Output
4	/DS	Data Strobe	Output
5	/AS	Address Strobe	Output
6	P35	Port 3, Pin 5	Input
7	GND	Ground	Input
8	P32	Port 3, Pin 2	Input
9-11	P00-P02	Port 0, Pins 3,4,5,6	In/Output
12	IACK	Int. Acknowledge	Output
13-16	P03-P06	Port 0, Pins 3,4,5,6	In/Output
17	N/C	Not Connected	Input
18	P07	Port 0, Pin 7	In/Output
19-23	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
24	/SYNC	Synchronize Pin	Output

No	Symbol	Function	Direction
25	N/C	Not Connected	Input
26-28	P15-P17	Port 1, Pins 5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 33	Input
31-35	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
36	N/C	Not Connected (20 MHz)	Input
	/WAIT	WAIT (25 or 33 MHz)	Input
37-39	P25-P27	Port 2, Pins 5,6,7	In/Output
40	P31	Port 3, Pin 1	Input
41	P36	Port 3, Pin 6	Output
42	N/C	Not Connected	Input
43	V_{CC}	Power Supply	Input
44	XTAL2	Crystal, Osc. Clock	Output
45	XTAL1	Crystal, Osc. Clock	Input
46	P37	Port 3, Pin 7	Output
47	P30	Port 3, Pin 0	Input
48	SCLK	System Clock	Output

PIN FUNCTIONS

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. When /RESET is asserted, /AS toggles. Memory address transfers are valid at the trailing edge of /AS.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, read High/write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory. It is High when the MCU is reading from the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C93 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of 2TpC. When /RESET is deactivated, program execution begins at location 000CH. Reset time must be held Low for 50 ms or until V_{CC} is stable, whichever is longer.

SCLK *System Clock* (output). The internal system clock is available at this pin. Available in the PLCC, QFP, and VQFP packages only.

IACK *Interrupt Acknowledge* (output, active High). This output, when High, indicates that the Z86C93 is in an interrupt cycle. Available in the PLCC, QFP, and VQFP packages only.

/SYNC (output, active Low). This signal indicates the last clock cycle of the currently executing instruction. Available in the PLCC, QFP, and VQFP packages only.

/WAIT (input, active Low). Introduces asynchronous wait states into the external memory fetch cycle. When this input goes Low during an external memory access, the Z86C93 freezes the fetch cycle until this pin goes High. This pin is sampled after /DS goes Low; should be pulled up if not used. Available in the 25 MHz and 33 MHz devices only.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 7). The /OEN (Output Enable) signal in Figure 7 is an internal signal.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

PIN FUNCTIONS (Continued)

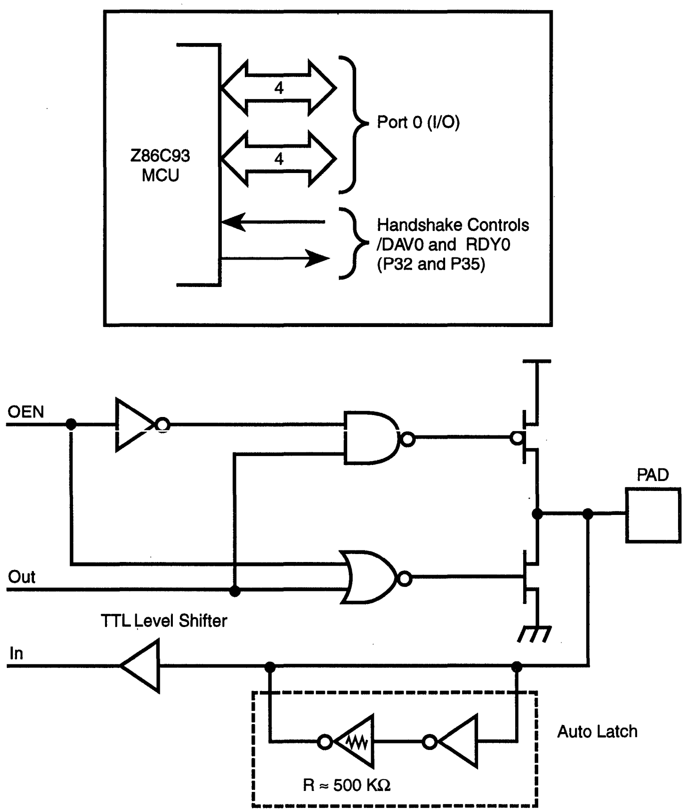
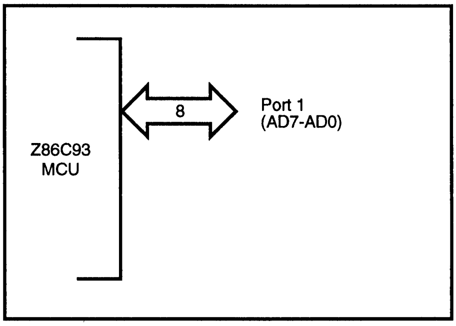


Figure 7. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory (Figure 8).

If more than 256 external locations are required, Port 0 must output the additional lines.



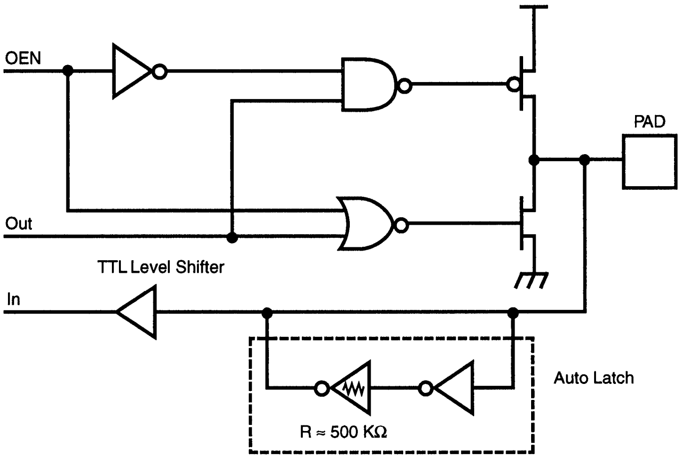


Figure 8. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

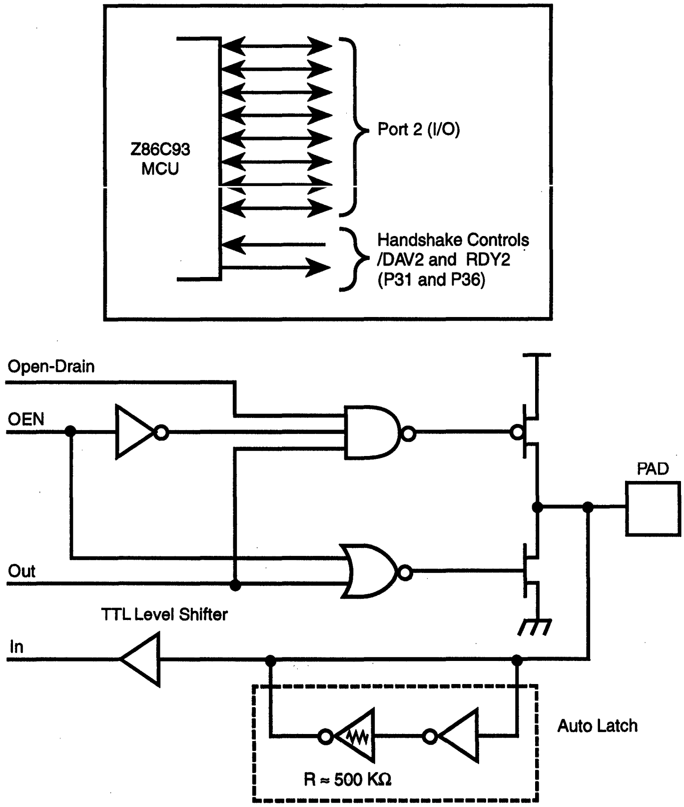


Figure 9. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P33-P30) input and four fixed (P37-P34) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

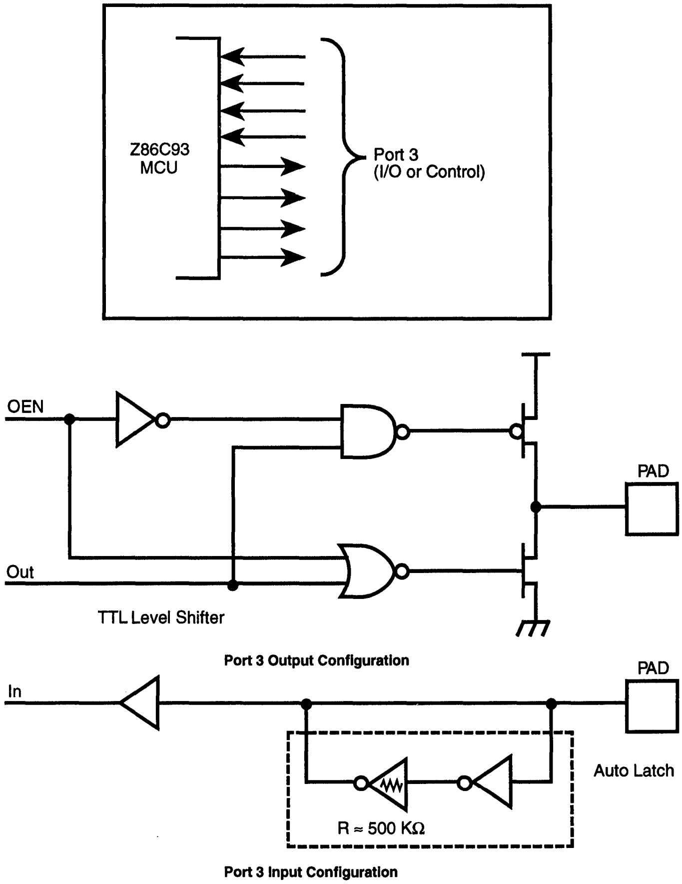


Figure 10. Port 3 Configuration

PIN FUNCTIONS (Continued)

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In		IRQ3			Serial In	
P31	In	T_{IN}	IRQ2		D/R		
P32	In		IRQ0	D/R			
P33	In		IRQ1				
P34	Out						DM
P35	Out			R/D			
P36	Out	T_{OUT}			R/D		
P37	Out					Serial Out	

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/ transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 11). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

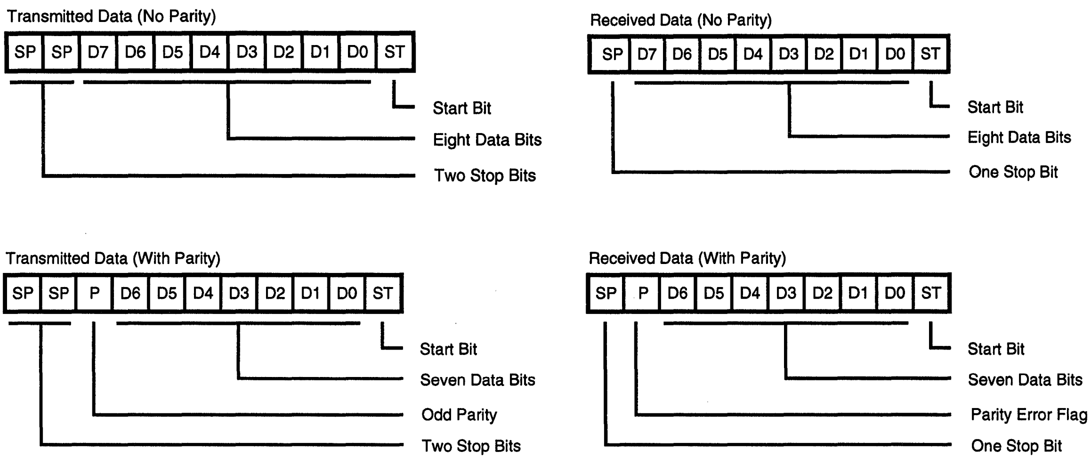


Figure 11. Serial Data Formats

ADDRESS SPACE

Program Memory. The Z86C93 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory. The Z96C93 can address up to 64 Kbytes of external data memory. External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34 is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area (Figure 13). The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14). The registers that are used in the multiply/divide unit reside in the Expanded Register File at Bank E and those for the additional timer control words reside in Bank D. The rest of the Expanded Register is not physically implemented and is open for future expansion.

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers. The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C93 also allows short 4-bit register addressing using the Register Pointer (Figure 15). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Group E0-EF can only be accessed through working registers and indirect addressing modes.

Stack. The Z86C93 has a 16-bit Stack Pointer (R254-R255), used for external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH, Bits 8-15) can be used as a general-purpose register when using internal stack only.

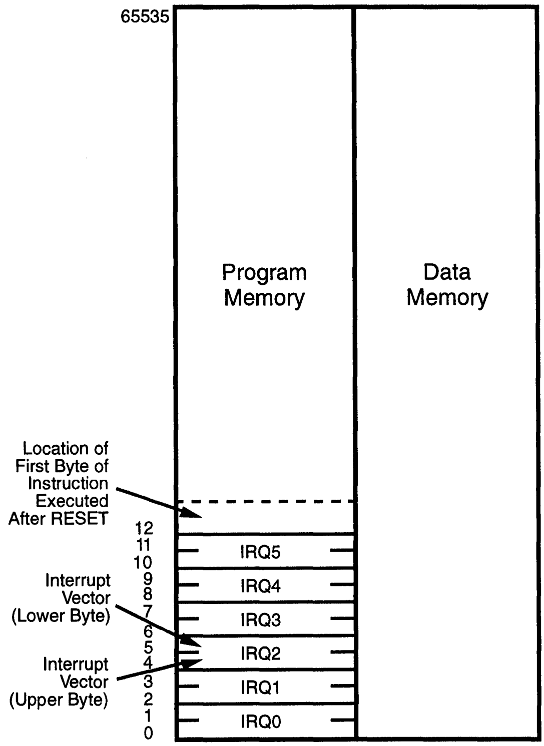
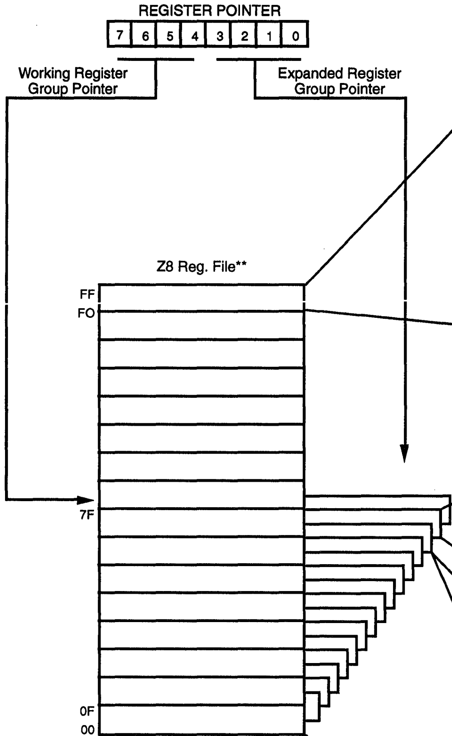


Figure 12. Program and Data Memory Configuration

ADDRESS SPACE (Continued)



Z8 STANDARD CONTROL REGISTERS

	REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	SPH	U	U	U	U	U	U	U	U
	FD	RP	U	U	U	U	U	U	U	U
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	0	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	1	1	1	1	0	1	1	1
	F7	P3M	0	0	0	0	0	0	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
*	F5	PRE0	U	U	U	U	U	U	U	0
	F4	T0	U	U	U	U	U	U	U	U
	F3	PRE1	U	U	U	U	U	U	0	0
	F2	T1	U	U	U	U	U	U	U	U
	F1	TMR	0	0	0	0	0	0	0	0
	F0	SIO	U	U	U	U	U	U	U	U

EXPANDED REG. BANK (E)

REGISTER		RESET CONDITION							
(E) 15	GPR	U	U	U	U	U	U	U	U
(E) 14	GPR	U	U	U	U	U	U	U	U
(E) 13-7	Reserved								
(E) 6	MDCON	1	0	0	U	U	U	0	0
(E) 5	MREG5	U	U	U	U	U	U	U	U
(E) 4	MREG4	U	U	U	U	U	U	U	U
(E) 3	MREG3	U	U	U	U	U	U	U	U
(E) 2	MREG2	U	U	U	U	U	U	U	U
(E) 1	MREG1	U	U	U	U	U	U	U	U
(E) 0	MREG0	U	U	U	U	U	U	U	U

EXPANDED REG. BANK (D)

REGISTER		RESET CONDITION							
(D) 9	T2CAPL	U	U	U	U	U	U	U	U
(D) 8	T2CAPH	U	U	U	U	U	U	U	U
(D) 7	T2L	U	U	U	U	U	U	U	U
(D) 6	T2H	U	U	U	U	U	U	U	U
(D) 5	Reserved								
(D) 4	T0H	U	U	U	U	U	U	U	U
(D) 3	T2PRE	U	U	U	U	0	U	0	0
(D) 2	T1H	U	U	U	U	U	U	U	U
(D) 1	T2TMR	U	0	U	0	0	0	0	0
(D) 0	Reserved								

EXPANDED REG. BANK (0)

REGISTER		RESET CONDITION							
(0) 03	P3	1	1	1	1	U	U	U	U
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved								
(0) 00	P0	U	U	U	U	U	U	U	U

U = Unknown
* = Will not be reset with a STOP Mode Recovery
GPR = General Purpose Register
** = All addresses are in hexadecimal

Figure 13. Register File

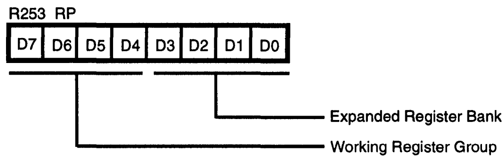


Figure 14. Register Pointer Register

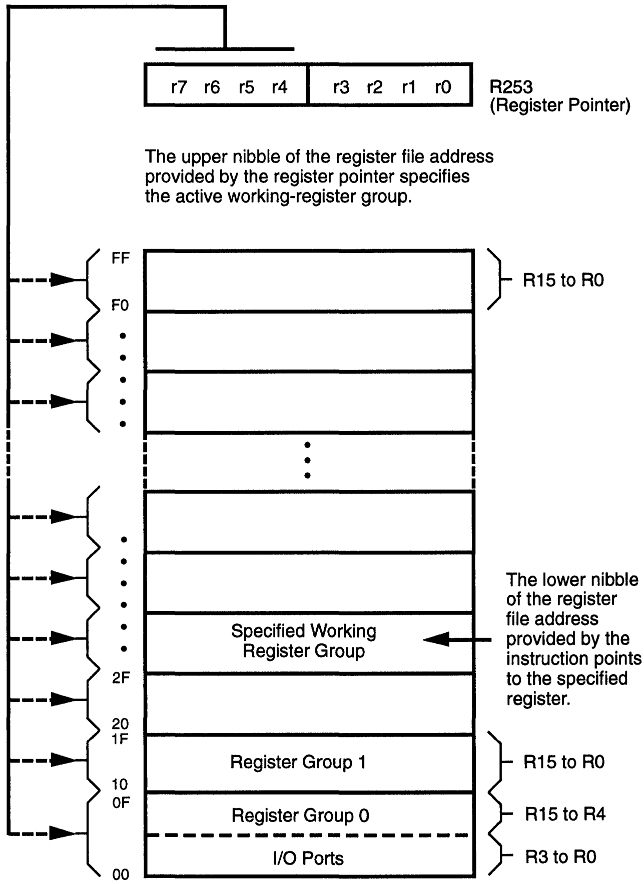


Figure 15. Register Pointer

FUNCTIONAL DESCRIPTION

Multiply/Divide Unit

The Multiply/Divide unit describes the basic features, implementation details of the interface between the Z8 and the multiply/divide unit.

Basic features:

- 16 x 16-bit multiply with 32-bit product
- 32 x 16-bit divide with 16-bit quotient and 16-bit remainder
- Unsigned integer data format
- Simple interface to Z8®

Interface to Z8. The following is a brief description of the register mapping in the multiply/divide unit and its interface to the Z8 (Figure 16).

The multiply/divide unit is interfaced like a peripheral. The only addressing mode available with the peripheral interface is register addressing. In other words, all of the operands are in the respective registers before a multiplication/division can start.

Register Mapping. The registers used in the multiply/divide unit are mapped onto the expanded register file in Bank E. The exact register locations used are shown below.

Register	Address
MREG0	(E) 00
MREG1	(E) 01
MREG2	(E) 02
MREG3	(E) 03
MREG4	(E) 04
MREG5	(E) 05
MDCON	(E) 06
GPR	(E) 14
GPR	(E) 15

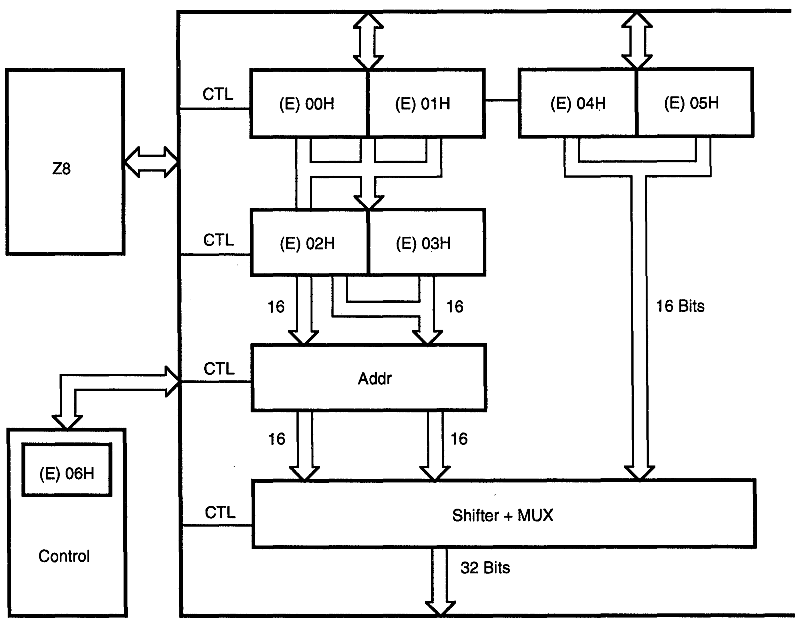


Figure 16. Multiply/Divide Unit Block Diagram

Register Allocation. The following is the register allocation during multiplication.

Register	Allocation
Multiplier high byte	MREG2
Multiplier low byte	MREG3
Multiplicand high byte	MREG4
Multiplicand low byte	MREG5
Result high byte of high word	MREG0
Result low byte of high word	MREG1
Result high byte of low word	MREG2
Result low byte of low word	MREG3
Multiply/Divide Control register	MDCON

The following is the register allocation during division.

Register	Allocation
High byte of high word of dividend	MREG0
Low byte of high word of dividend	MREG1
High byte of low word of dividend	MREG2
Low byte of low word of dividend	MREG3
High byte of divisor	MREG4
Low byte of divisor	MREG5
High byte of remainder	MREG0
Low byte of remainder	MREG1
High byte of quotient	MREG2
Low byte of quotient	MREG3
Multiply/Divide Control register	MDCON

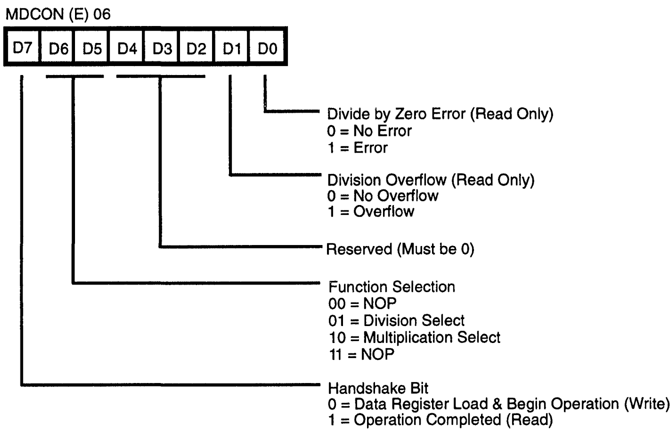


Figure 17. Multiply/Divide Control Register (MDCON)

Control Register. The MDCON (Multiply/Divide Control Register) is used to interface with the multiply/divide unit (Figure 16). Specific functions of various bits in the control register are given below.

DONE Bit (D7). This bit is a handshake bit between the math unit and the external world. On power-up, this bit is set to 1 to indicate that the math unit has completed the previous operation and is ready to perform the next operation.

Before starting a new multiply/divide operation, this bit should be reset to 0 by the processor/programmer. This indicates that all the data registers have been loaded and the math unit can now begin a multiply/divide operation. During the process of multiplication or division, this bit is write-protected. Once the math unit completes its operation it sets this bit to indicate the completion of operation. The processor/programmer can then read the result.

MULSL *Multiply Select* (D6). If this bit is set to 1, it indicates a multiply operation directive. Like the DONE bit, this bit is also write-protected during math unit operation and is reset to 0 by the math unit upon starting of the multiply/divide operation.

DIVSL *Division Select* (D5). Similar to D6, D5 starts a division operation.

D4-D2. Reserved.

FUNCTIONAL DESCRIPTION (Continued)

DIVOVF *Division Overflow* (D1). This bit indicates an overflow during the division process. Division overflow occurs when the high word of the dividend is greater than or equal to the divisor. This bit is read only. When set to 1, it indicates overflow error.

DIVZR *Division by Zero* (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example: Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined
x = Irrelevant
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

Performance of Multiplication. The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided-by-two). This results in an actual multiplication time (16 x 16-bit) of 1.7 µs. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 µs. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

Performance of Division. The actual division needs 20 internal clock cycles. This translates to 2.0 µs for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 µs at 10 MHz.

Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. Either T0 or T1 can be outputted through P36.

The following are the enhancements made to the counter/timer block on the Z86C93 (Figure 18):

- T0 counter length is extended to 16 bits. For example, T0 now has a 6-bit prescaler and 16-bit down counter.
- T1 counter length is extended to 16 bits. For example, T1 now has a 6-bit prescaler and 16-bit down counter.
- A new counter/timer T2 is added. T2 has a 4-bit prescaler and a 16-bit down counter with capture register.

These three counters are cascadable as shown in Table 6. The result is that T2 may be extendable to 32 bits and T1 extendable to 24 bits. Bits 1 and 0 (CAS1 AND CAS0) of the T2 Prescaler Register (PRE2) determine the counter length.

Table 6. Counter Length Configurations

CAS1	CAS0	T0	T1	T2
0	0	8	8	32
0	1	16	16	16
1	0	8	24	16
1	1	8	16	24

The controlling clock input to T2 is programmed to XTAL/2 or XTAL/8 (only when T2 counter length is 16 bits), which results in a resolution of 100 ns at an external XTAL clock speed of 20 MHz.

FUNCTIONAL DESCRIPTION (Continued)

Capture Register. T2 has a 16-bit capture register associated with T2 HIGH BYTE and T2 LOW BYTE registers. The negative going transition on P33 enables the latching of the current T2 value (16 bits) into the capture register. The register mapping of the capture register is in Bank D (Figure 13). Note that the negative transition on P33 is capable of generating an interrupt. Also, the negative transition on P33 always latches the current T2 value into the capture register. There is no need for a control bit to enable/disable the latching; the capture register is read only.

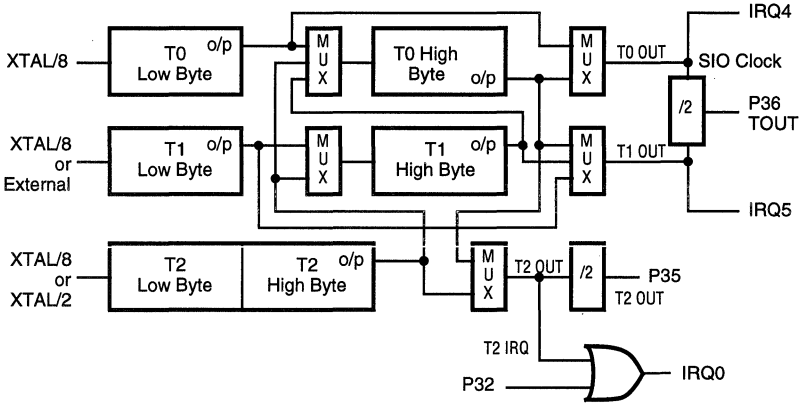


Figure 18. Counter/Timer Block Diagram

Operation

Except for the programmable down counter length and clock input, T2 is identical to T0.

T0 and T1 retain all their features except that now they are extendable interims of the down-counter length.

The output of T2, under program control, goes to an output (P35). Also, the interrupt generated by T2 is ORed with the interrupt request generated by P32. Note that the service routine then has to poll the T2 flag bit and also clear it (bit 7 of T2 Timer Mode Register).

On power-up, T0 and T1 are configured in the 8-bit down counter length mode (to be compatible with Z86C91) and T2 is in the 32-bit mode with its output disabled (no interrupt is generated and T2 output ***does not*** go to port P35).

The UART uses T0 for generating the bit clock. This means, while using UART, T0 should be in 8-bit mode. So, while using the UART there are only two independent timer/counters.

The counters are configured in the following manner:

Timer	Mode	Byte
T0	8-bit	Low Byte (T0)
T0	16-bit	High Byte (T0) + Low Byte (T0)
T1	8-bit	Low Byte (T1)
T1	16-bit	High Byte (T1)+ Low Byte (T1)
T1	24-bit	High Byte (T0) + High Byte (T1) + Low Byte (T1)
T2	16-bit	High Byte (T2) + Low Byte (T2)
T2	24-bit	High Byte (T0) + High Byte (T2) + Low Byte (T2)
T2	32-bit	High Byte (T0) + High Byte (T1) + High Byte (T2) + Low Byte (T2)

Note that the T2 interrupt is logically ORed with P32 to generate IRQ0.

The T2 Timer Mode register is shown in Figure 19. Upon reaching end of count, bit 7 of this register is set to one. This bit ***is not*** reset in hardware and it has to be cleared by the interrupt service routine.

T2 interrogates the state of the Count Mode Bit (D2) once it has counted down to its zero value. T2 then makes the decision to continue counting (Modulo-n Mode) or stop (Single Pass Mode). Monitor this function if attempting to modify the count mode prior to the end of count bit (D7) being set.

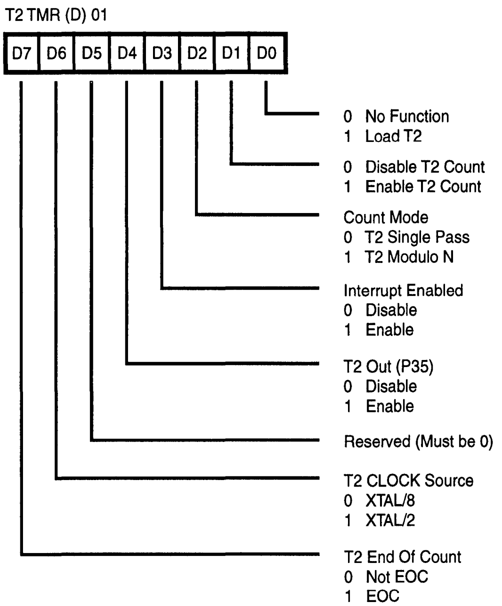


Figure 19. T2 Timer Mode Register (T2)

The register map of the new CTC registers is shown in Figure 13. T0 high byte and T1 high byte are at the same relative locations as their respective low bytes, but in a different register bank.

The T2 Prescaler Register is shown in Figure 20. Bits 1 and 0 of this register control the various cascade modes of the counters.

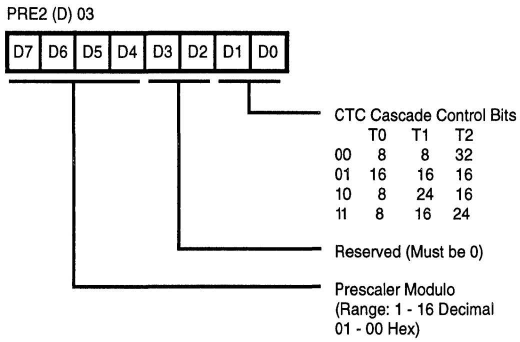


Figure 20. T2 Prescaler Register (PRE2)

FUNCTIONAL DESCRIPTION (Continued)

Interrupts

The Z86C93 has six different interrupts from nine different sources (Figure 21). The interrupts are maskable and prioritized. The nine sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

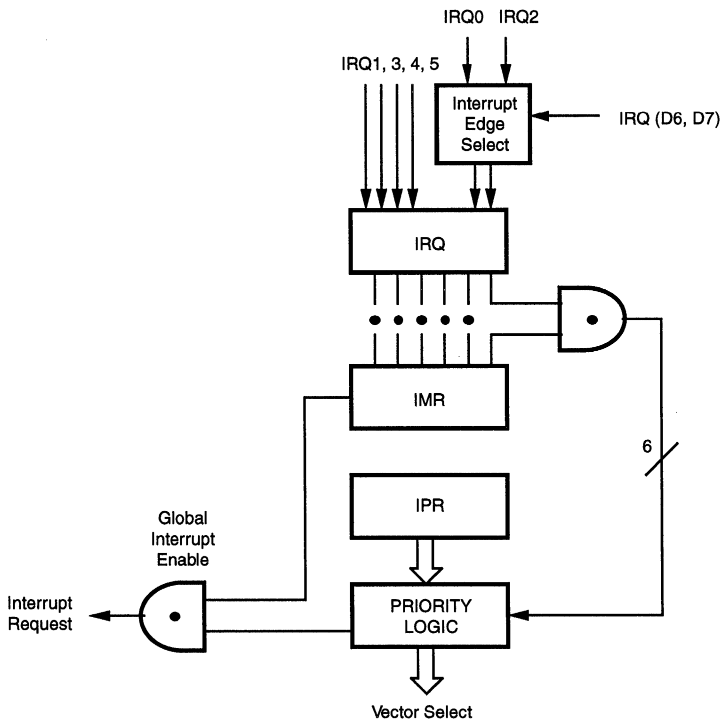


Figure 21. Interrupt Block Diagram

Table 7. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, P32, T2	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ1	P33	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, P31, T_{IN}	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ3	P30, Serial In	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0, Serial Out	8, 9	Internal
IRQ5	T1	10, 11	Internal

Clock

The Z86C93 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The external clock levels are not TTL. The crystal should be AT cut, 1 MHz to 25 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF<CL<100 pF) from each pin to ground (Figure 22).

Note: Actual capacitor values specified by the crystal manufacturer.

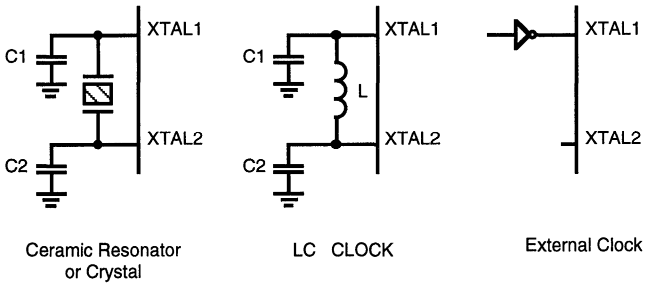


Figure 22. Oscillator Configuration

Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode, After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode = OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

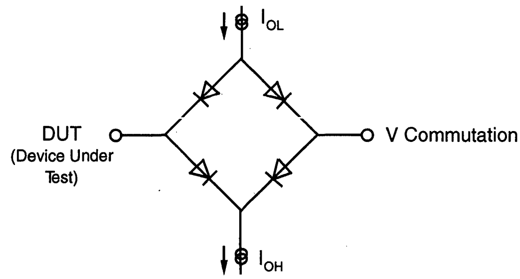


Figure 23. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS
$V_{CC} = 3.3V \pm 10\%$

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
	Max Input Voltage	7			V	$I_{IN} < 250\ \mu A$	
V_{CH}	Clock Input High Voltage	0.8 V_{CC}	V_{CC}		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	–0.3	0.1 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC}		V		
V_{IL}	Input Low Voltage	–0.3	0.1 V_{CC}		V		
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –1.0 mA	
V_{OH}	Output High Voltage	V_{CC} – 100 mV			V	I_{OH} = –100 µA	
V_{OL}	Output Low Voltage	0.4			V	I_{OL} = +1.0 mA	
V_{RH}	Reset Input High Voltage	0.8 V_{CC}	V_{CC}		V		
V_{RI}	Reset Input Low Voltage	–0.3	0.1 V_{CC}		V		
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{IR}	Reset Input Current	–120			µA	V_{RL} = 0V	
I_{CC}	Supply Current		30	20	mA	@ 25 MHz	[1]
I_{CC1}	Stand By Current (HALT mode)		12	8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 25 MHz	[1]
I_{CC2}	Stand By Current (HALT mode)		8	1	µA	STOP mode V_{IN} = 0V, V_{CC}	[1]
I_{ALL}	Auto Latch Low Current	–10	10	5	µA		

Note:
[1] All inputs driven to 0V, V_{CC} and outputs floating.

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
	Max Input Voltage	7			V	I_{IN} < 250 µA	
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0	V_{CC}		V		
V_{IL}	Input Low Voltage	–0.3	0.8		V		
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –2.0 mA	
V_{OH}	Output High Voltage	V_{CC}–100 mV			V	I_{OH} = –100 µA	
V_{OL}	Output Low Voltage	0.4			V	I_{OL} = +5 mA	
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V		
V_{RI}	Reset Input Low Voltage	–0.3	0.8		V		
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{IR}	Reset Input Current	–120			µA	V_{RL} = 0V	
I_{CC}	Supply Current	55		35	mA	@ 33 MHz	[1]
		40		25	mA	@ 25 MHz	[1]
		30		20	mA	@ 20 MHz	[1]
I_{CC1}	Standby Current (HALT mode)	15		9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 25 MHz	[1]
		20		15	mA	HALT mode V_{IN} = 0V, V_{CC} @ 33 MHz	[1]
		12		7	mA	HALT mode V_{IN} = 0V, V_{CC} @ 20 MHz	[1]
I_{CC2}	Standby Current (STOP mode)	10		1	µA	STOP mode V_{IN} = 0V, V_{CC}	[1]
I_{ALL}	Auto Latch Current	–16	16	5	µA		

Note:
[1] All inputs driven to 0V, or V_{cc} and outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram

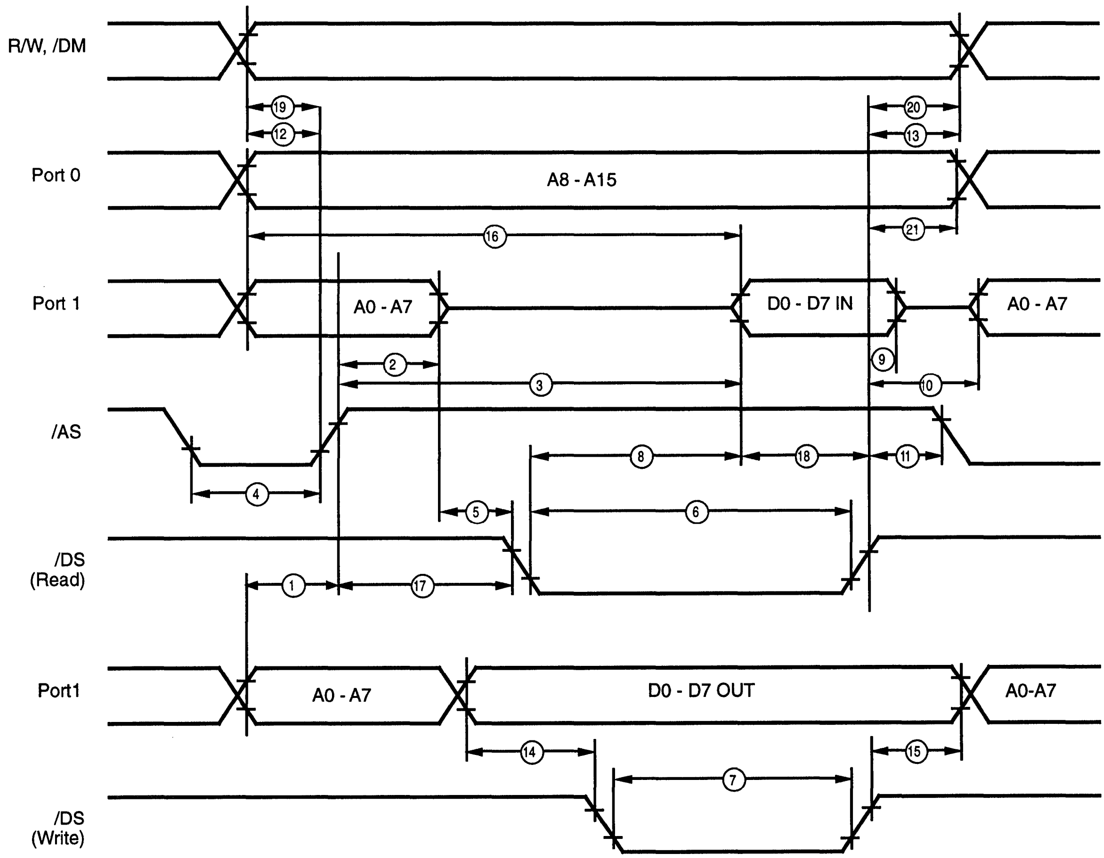

Figure 24. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

			T_A = 0°C to +70°C						Typical	
			33 MHz		25 MHz		20 MHz		V_{CC} = 5.0V	
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	@ 25°C	Units
1	TdA(AS)	Address Valid To /AS Rise Delay	13		22		26			ns
2	TdAS(A)	/AS Rise To Address Hold Time	20		25		28			ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		90		130		160		ns
4	TwAS	/AS Low Width	20		28		36			ns
5	TdAZ(DSR)	Address Float To /DS Fall (Read)	0		0		0			ns
6	TwDSR	/DS (Read) Low Width	65		100		130			ns
7	TwDSW	/DS (Write) Low Width	40		65		75			ns
8	TdDSR(DI)	/DS Fall (Read) To Data in Req'd Valid Delay		30		85		100		ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0			ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		40		48			ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36			ns
12	TdR/W(AS)	R/W Valid To /AS Rise Delay	12		26		32			ns
13	TdDS(R/W)	/DS Rise To R/W Not Valid Delay	12		30		36			ns
14	TdDO(DSW)	Data Out To /DS Fall (Write) Delay	12		34		40			ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40			ns
16	TdA(DI)	Address Valid To Data In Req'd Valid Delay		110		160		200		ns
17	TdAS(DSR)	/AS Rise To /DS Fall (Read) Delay	20		40		48			ns
18	TaDI(DSR)	Data In Set-up Time To /DS Rise Read	16		28		36			ns
19	TdDM(AS)	/DM Valid To /AS Rise Delay	10		22		26			ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay							34*	ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time							34*	ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising							20*	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling							23*	ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling							29*	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising							29*	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling							29*	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising							29*	ns
28	TsW(XT)	Wait Set-up Time							10*	ns
29	ThW(XT)	Wait Hold Time							15*	ns
30	TwW	Wait Width (One Wait Time)							25*	ns

Notes:
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
* Preliminary value to be characterized.

AC CHARACTERISTICS (Continued)

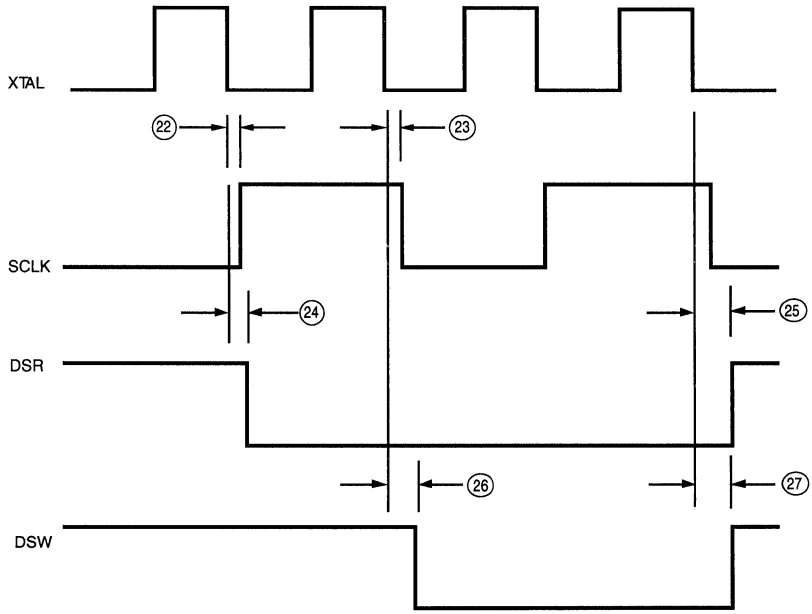

Figure 25. XTAL/SCLK to DSR and DSW Timing

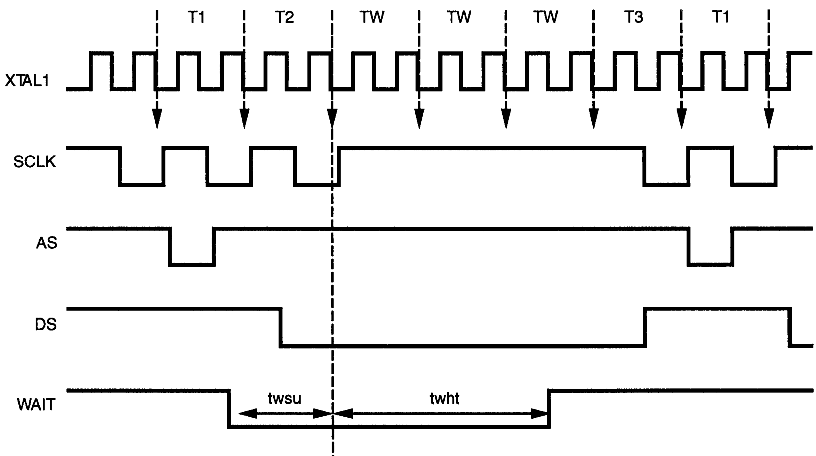

Figure 26. XTAL/SCLK to WAIT Timing
(25 MHz & 33 MHz Device only)

AC CHARACTERISTICS
Additional Timing Diagram

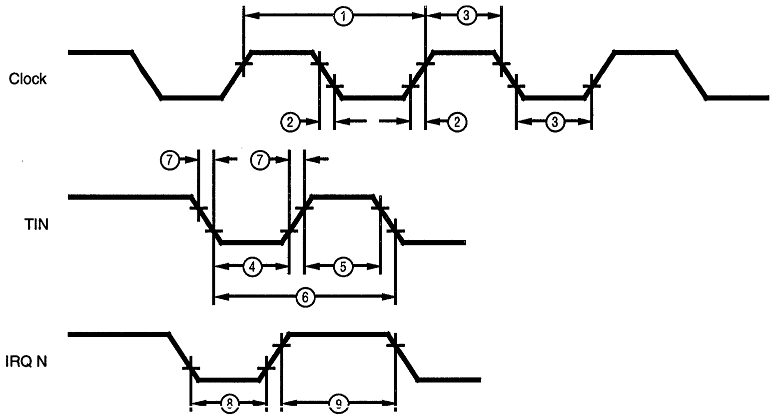

Figure 27. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

			T_A = 0°C to +70° C							
			33 MHz		25 MHz		20 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	30	1000	42	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		5		10		10	ns	[1]
3	TwC	Input Clock Width	10	11		15			ns	[1]
4	TwTinL	Timer Input Low Width	75	75		75			ns	[2]
5	TwTinH	Timer Input High Width	3TpC	3TpC		3TpC				[2]
6	TpTin	Timer Input Period	8TpC	8TpC		8TpC				[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100	100		100			ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70	70		70			ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC	5TpC		5TpC				[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC	3TpC		3TpC				[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

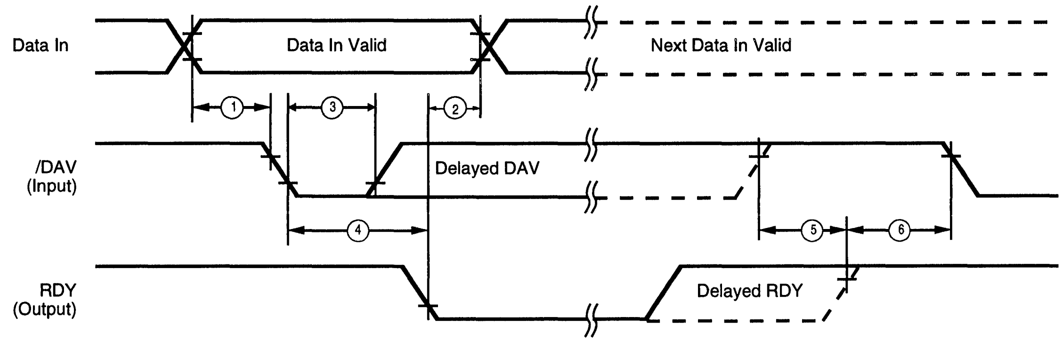

Figure 28. Input Handshake Timing

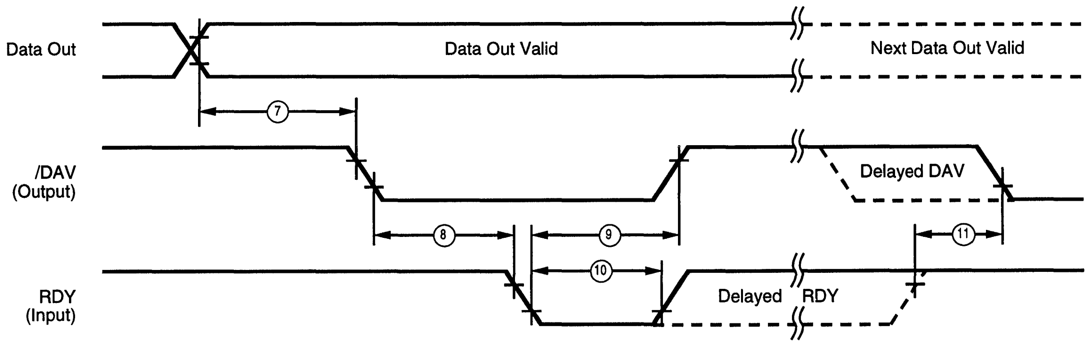

Figure 29. Output Handshake Timing

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AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	T_A = 0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time to /DAV	0		ns	In
2	ThDI(DAV)	RDY to Data In Hold Time	0		ns	In
3	TwDAV	/DAV Width	40		ns	In
4	TdDAVIf(RDYf)	/DAV to RDY Delay		70	ns	In
5	TdDAVIr(RDYr)	DAV Rise to RDY Wait Time		40	ns	In
6	TdRDYOr(DAVIf)	RDY Rise to DAV Delay	0		ns	In
7	TdDO(DAV)	Data Out to DAV Delay		TpC	ns	Out
8	TdDAVOf(RDYIf)	/DAV to RDY Delay	0		ns	Out
9	TdRDYIf(DAVOr)	RDY to /DAV Rise Delay		70	ns	Out
10	TwRDY	RDY Width	40		ns	Out
11	TdRDYIr(DAVOf)	RDY Rise to DAV Wait Time		40	ns	Out

EXPANDED REGISTER FILE CONTROL REGISTERS

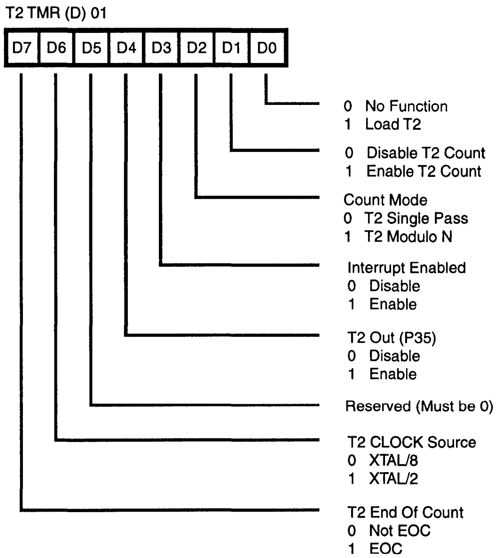


Figure 30. Timer 2 Mode Register (01H: Read/Write)

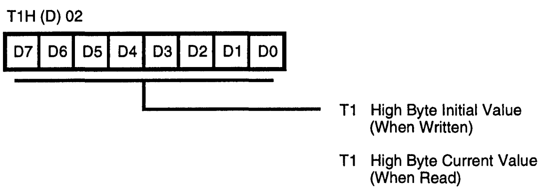


Figure 31. Counter Timer 1 Register High Byte (02H: Read/Write)

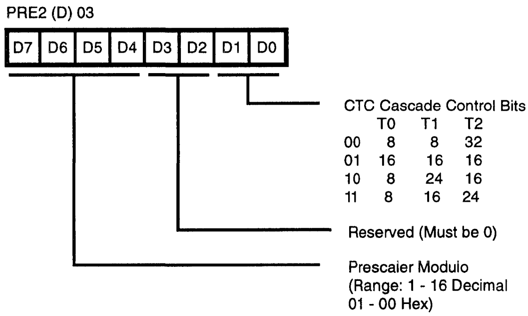


Figure 32. Prescaler 2 Register High Byte (03H: Write Only)

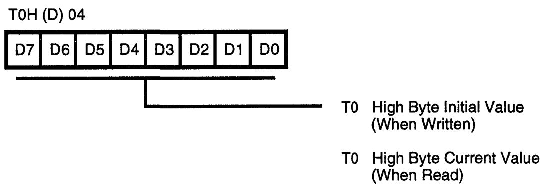


Figure 33. Counter Timer 0 Register High Byte (04H: Read/Write)

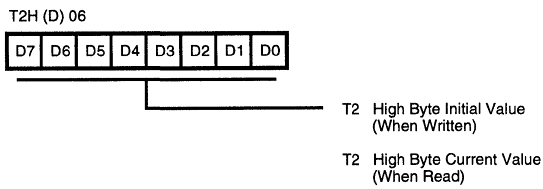


Figure 34. Counter Timer 2 Register High Byte (06H: Read/Write)

Z8 CONTROL REGISTERS

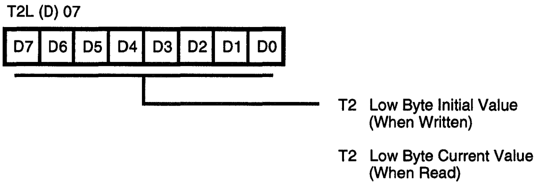


Figure 35. Counter Timer 2 Register Low Byte (07H: Read/Write)

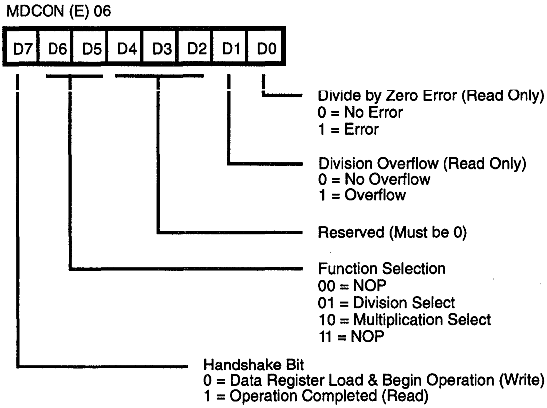


Figure 36. Multiply/Divide Control Register (MDCON)

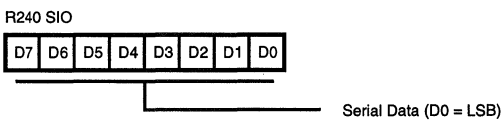


Figure 37. Serial I/O Register (F0H: Read/Write)

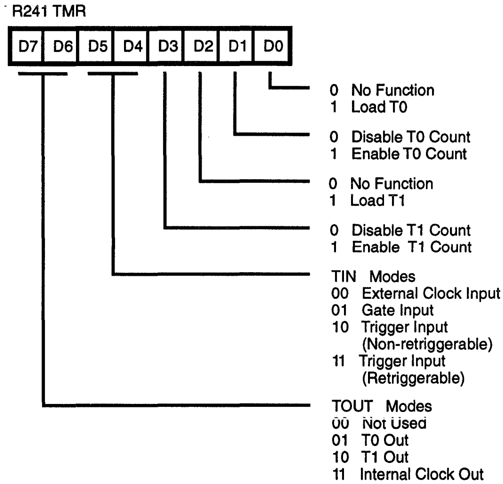


Figure 38. Timer Mode Register (F1H: Read/Write)

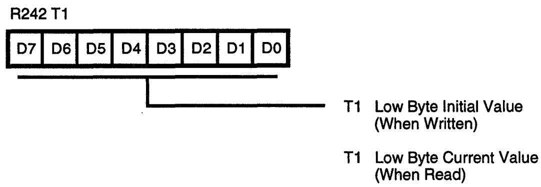


Figure 39. Counter/Timer 1 Register (F2H: Read/Write)

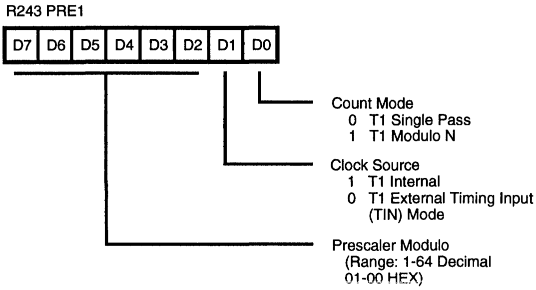


Figure 40. Prescaler 1 Register (F3H: Write Only)

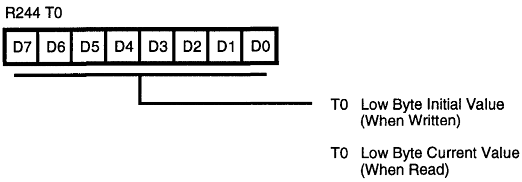


Figure 41. Counter/Timer 0 Register (F4H: Read/Write)

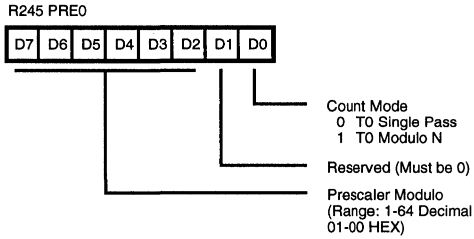


Figure 42. Prescaler 0 Register (F5H: Write Only)

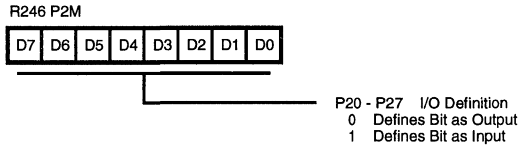


Figure 43. Port 2 Mode Register (F6H: Write Only)

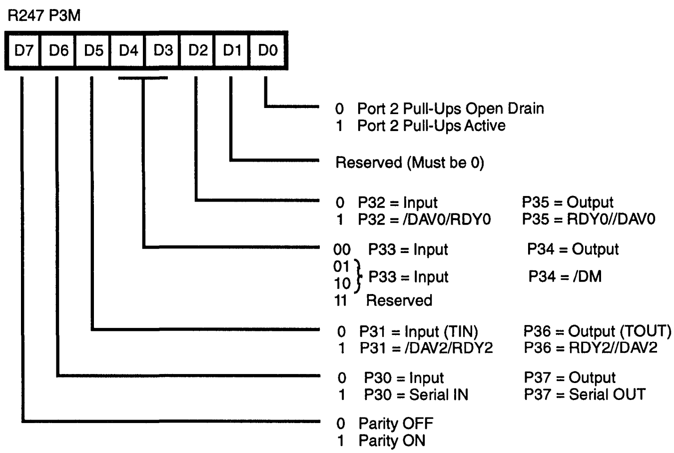


Figure 44. Port 3 Mode Register (F7H: Write Only)

Z8 CONTROL REGISTERS (Continued)

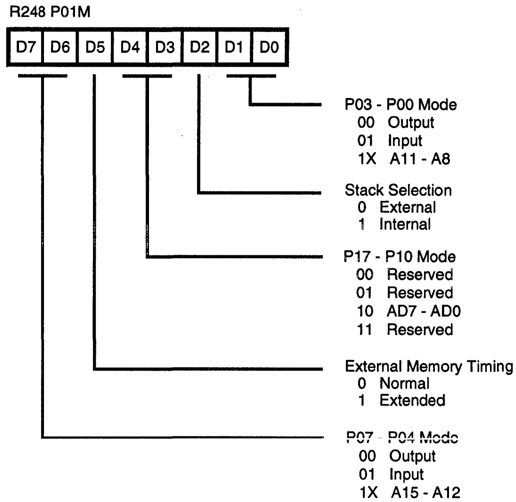


Figure 45. Ports 0 and 1 Mode Registers (F8H: Write Only)

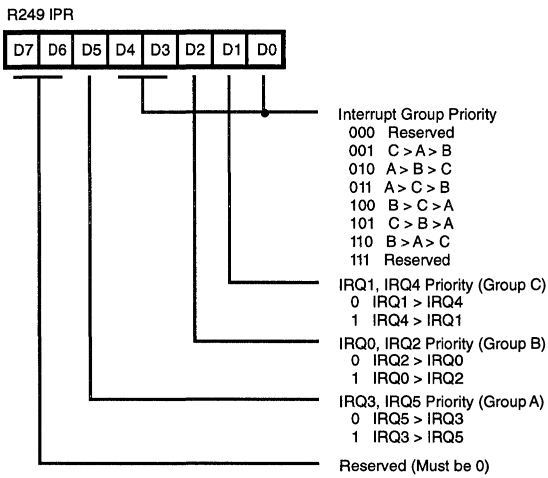


Figure 46. Interrupt Priority Register (F9H: Write Only)

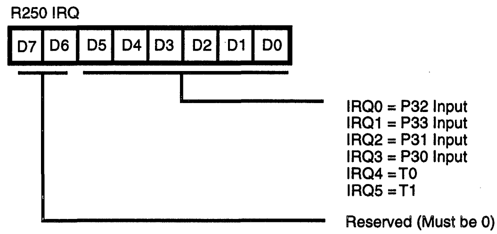


Figure 47. Interrupt Request Register (FAH: Read/Write)

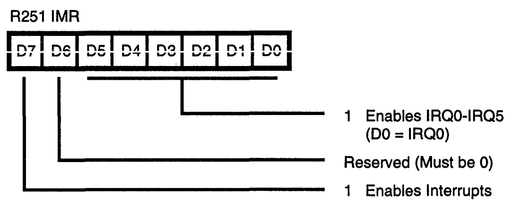


Figure 48. Interrupt Mask Register (FBH: Read/Write)

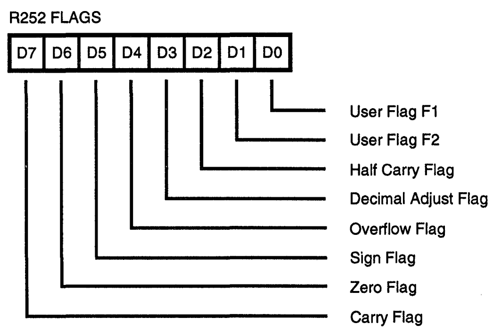


Figure 49. Flag Register (FCH: Read/Write)

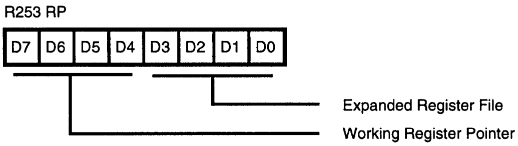


Figure 50. Register Pointer (FDH: Read/Write)

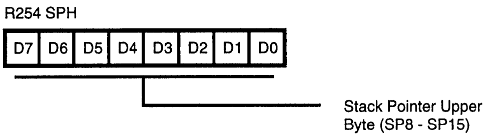


Figure 51. Stack Pointer High (FEH: Read/Write)

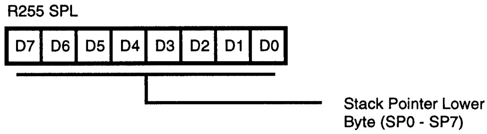


Figure 52. Stack Pointer Low (FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

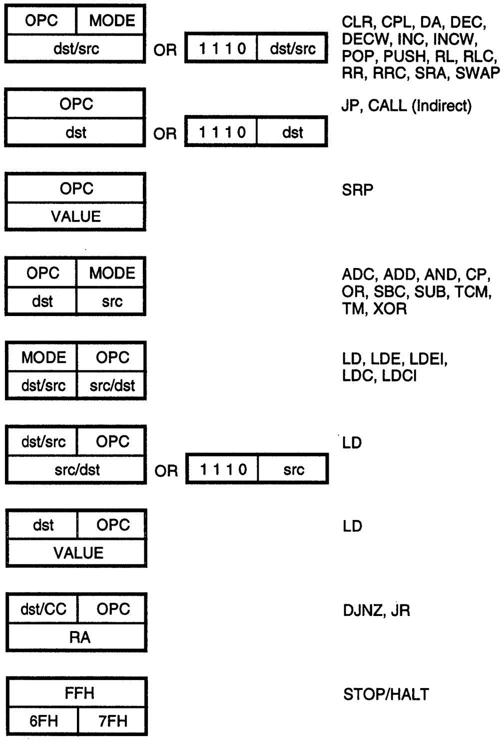
Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

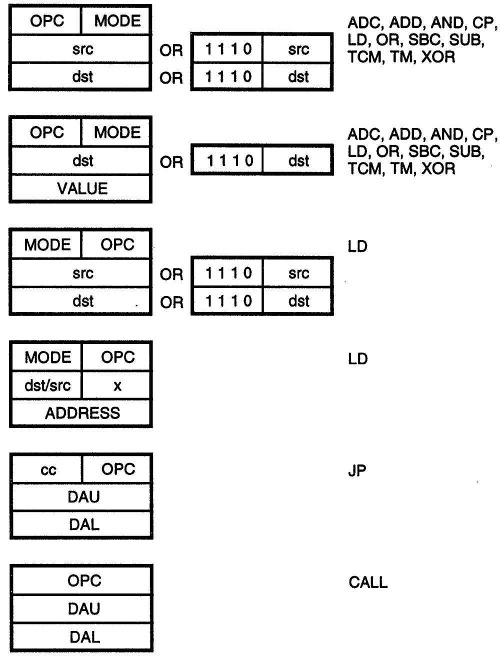
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - -
CCF C←NOT C			EF	* - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst – src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst – 1	R IR		00 01	- * * * - -
DECW dst dst←dst – 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - -
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 - F	- - - - - -
EI IMR(7)←1			9F	- - - - - -
HALT			7F	- - - - - -
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	- - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src dst←src	r	Irr	C2	- - - - - -
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	- - - - - -

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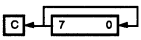
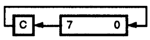
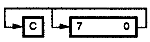
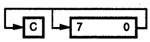
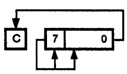
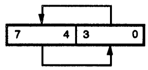
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -
STOP		6F	1 - - - - -
SUB dst, src dst←dst←src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

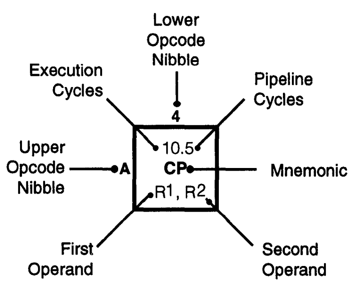
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down.

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2	2	2	2	3	3	3	3	2	2	2	2	2	3	1	1

(Columns 8 through E: the entry in row 0 applies to all rows, indicated by downward arrows.)



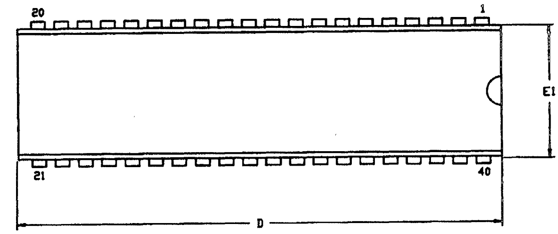
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

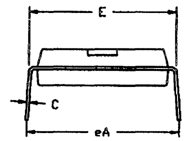
Sequence:
Opcode, First Operand, Second Operand

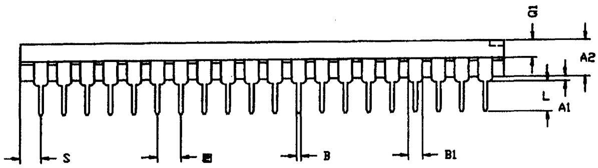
Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



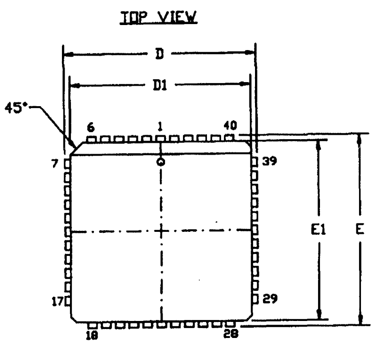


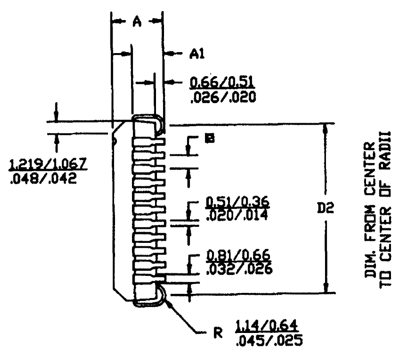


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



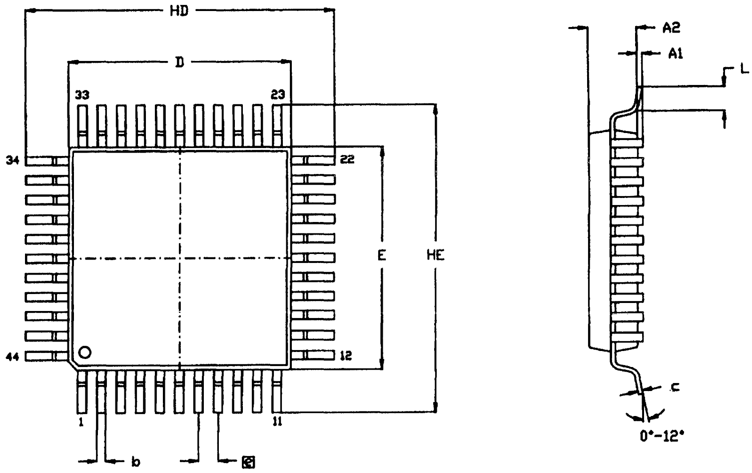


NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

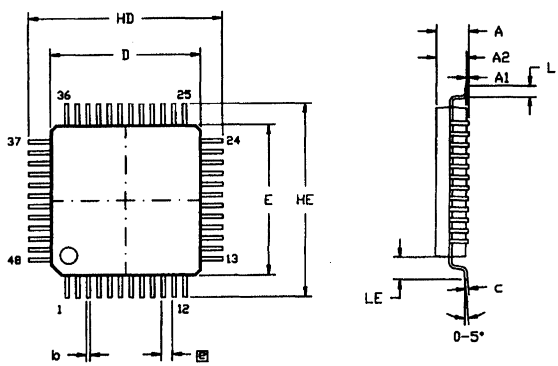
44-Pin PLCC Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.18	.004	.007
HD	8.60	9.40	.339	.370
D	6.90	7.10	.272	.280
HE	8.60	9.40	.339	.370
E	6.90	7.10	.272	.280
e	0.50 TYP		.020 TYP	
L	0.30	0.70	.012	.028
LE	0.90	1.10	.035	.043

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"

48-Pin VQFP Package Diagram

ORDERING INFORMATION

Z86C93

20 MHz

44-pin PLCC	**44-pin QFP**	**40-pin DIP**	**48-pin VQFP**
Z86C9320VSC	Z86C9320FSC	Z86C9320PSC	Z86C9320ASC

25 MHz

44-pin PLCC	**44-pin QFP**	**40-pin DIP**	**48-pin VQFP**
Z86C9325VSC	Z86C9325FSC	Z86C9325PSC	Z86C9325ASC

33 MHz

44-pin PLCC	**44-pin QFP**	**40-pin DIP**	**48-pin VQFP**
Z86C9333VSC	Z86C9333FSC	Z86C9333PSC	Z86C9333ASC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
V = Plastic Leaded Chip Carrier
P = Plastic Dual In Line Package

Longer Lead Time
F = Plastic Quad Flat Pack
A = Very Small Quad Flat Pack

Temperature
S= 0°C to +70°C

Speed
20 = 20 MHz
25 = 25 MHz
33 = 33 MHz

Environmental
C = Standard Flow

Example:

Z 86C93 33 V S C is a Z86C93, 33 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- V — Package
- 33 — Speed
- 86C93 — Product Number
- Z — Zilog Prefix

Z86E21 CMOS Z8®
8K OTP Microcontroller 7

Z86C61/62/96 CMOS Z8®
Microcontroller 8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
ROMless Microcontroller 10

Z86C93 CMOS Z8® Multiply/
Divide Microcontroller 11

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Z0860000ZCO DEVELOPMENT KIT PRODUCT SPECIFICATION

SUPPORTED DEVICES: Z8600, Z8601, Z8611, Z86C21, Z86C61, Z86C91, Z86C93

DESCRIPTION

The Z8® Development Kit can be used for several purposes. As an evaluation tool, one can learn the Z8 instruction set plus the manipulation of the Z8 MCU's interrupt vectors and register set. Secondly, the Z8 Development Kit is designed to aid the user in constructing specific applications using the Z8 microcontroller.

SPECIFICATIONS

Power Requirements

+5 Vdc @ 50 mA

Dimensions

Width: 4.0 in. (10.2 cm)
Length: 8.0 in. (20.3 cm)

Serial Interface

RS-232C @ 9600 baud

KIT CONTENTS

Z8 Development Board
CMOS Z86C91 MPU
12 MHz Crystal
(32K)/8K x 8 EPROM
(32K)/8K x 8 Static RAM
RS-232C PC Interface
Z86C91 Expansion Header

Cables

25-Pin RS-232 Cable

Software (IBM® PC Platform)

Z8/Super8™ Assembler and Utilities
Host Communication Package
Monitor Instructions
Tutorial
Sample Z86C91 Application Software

Documentation

Microcontrollers Data Book
Z8 Development Kit User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION

Part No: Z0860000ZCO

12

Z86C0800ZCO APPLICATIONS BOARD PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86C08

DESCRIPTION

The kit contains an assembled circuit board, software and documentation to help the user become familiar with the features of the Z86C08 microcontroller.

The Z86C0800ZCO Applications Board is used to demonstrate the advantages and versatility of the 18-pin Z8 device. Included is simple hardware and software that demonstrates the implementation of WDT, HALT, and STOP mode, low cost D to A, and A to D conversion techniques.

SPECIFICATIONS

Power Requirements

+5 Vdc @ 50 mA

Dimensions

Width: 4.4 in. (11.2 cm)
Length: 4.8 in. (12.2 cm)

KIT CONTENTS

Z86C08 Application Board

CMOS Z86C08 MPU
4 MHz Crystal
Four 7-segment LED Displays
17-Key Keypad

Software (IBM® PC Platform)

Application Source Code
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation

Microcontrollers Data Book
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Z86C08 Application Kit User Guide

ORDERING INFORMATION

Part No: Z86C0800ZCO

Z86C0800ZDP ADAPTOR BOARD PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86C08

DESCRIPTION

The Z86C08 Adaptor Board converts the Z8® MCU from a 40-pin pin out to an 18-pin pin out. This adaptor board allows a standard Z8 emulation device to emulate the Z86C08. The Z86C08 Adaptor Board is placed between the Z8 emulator and the user's target socket. The board does not emulate the watchdog timer function.

SPECIFICATIONS

Dimensions

Width: 2.5 in. (6.4 cm)
Length: 2.9 in. (7.4 cm)

KIT CONTENTS

Z86C08 Adaptor Board

40-Pin Z8 MPU Socket
18-Pin Z86C08 Socket
12 MHz Crystal

Cables

18-Pin Z86C08 Emulation Cable

Documentation

Z86C08 Adaptor Kit User Guide

ORDERING INFORMATION

Part No: Z86C0800ZDP

12

Z86E2100ZDF ADAPTOR KIT
PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86E21

DESCRIPTION

The Z86E21 QFP OTP Program Adaptor Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS

Power Requirements

+12.5 Vdc @ .5 A

Dimensions

Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS

Z86E21 QFP OTP Program Adaptor Board

44-Pin QFP ZIF Socket
28-Pin Connector

Documentation

OTP Program Adaptor User Guide

ORDERING INFORMATION

Part No: Z86E2100ZDF

Z86E2100ZDP ADAPTOR KIT
PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86E21

DESCRIPTION

The Z86E21 DIP OTP Program Adaptor Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS

Power Requirements

+12.5 Vdc @ .5 A

Dimensions

Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS

Z86E21 OTP Program Adaptor Board

40-Pin DIP ZIF Socket
28-Pin Connector

Documentation

OTP Program Adaptor User Guide

ORDERING INFORMATION

Part No: Z86E2100ZDP

12

Z86E2100ZDV ADAPTOR KIT PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86E21

DESCRIPTION

The Z86E21 PLCC OTP Program Adaptor Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS

Power Requirements

+12.5 Vdc @ .5 A

Dimensions

Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS

Z86E21 PLCC OTP Program Adaptor Board

44-Pin PLCC ZIF Socket
28-Pin Connector

Documentation

OTP Program Adaptor User Guide

ORDERING INFORMATION

Part No: Z86E2100ZDV

Z86E2101ZDF CONVERSION KIT PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86E21

DESCRIPTION

The Z86E21 OTP Program Conversion Kit converts a 44-pin QFP package to a 40-pin DIP package, which allows the C12 ICEBOX™ to program the 44-pin QFP Z86E21 OTP microcontroller.

SPECIFICATIONS

Dimensions

Width: 2.0 in. (5.1 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS

Z86E21 OTP Program Conversion Board

44-Pin QFP ZIF Socket
40-Pin Connector

ORDERING INFORMATION

Part No: Z86E2101ZDF

Z86E2101ZDV CONVERSION KIT
PRODUCT SPECIFICATION

SUPPORTED DEVICE: Z86E21

DESCRIPTION

The Z86E21 OTP Program Conversion Kit converts a 44-pin PLCC package to a 40-pin DIP package, which allows the C12 ICEBOX™ to program the 44-pin PLCC Z86E21 OTP microcontroller.

SPECIFICATIONS

Dimensions

Width: 1.8 in. (4.6 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS

Z86E21 OTP Program Conversion Board

44-Pin PLCC ZIF Socket
40-Pin Connector

ORDERING INFORMATION

Part No: Z86E2101ZDV

Z86C6100TSC Z86C61/63 MCU OTP EMULATION BOARD
PRODUCT SPECIFICATION

SUPPORTED DEVICES: Z86C61, Z86C63

DESCRIPTION
The Z86C6100TSC Emulation Board allows the user to plug a programmed EPROM into the board to verify operation of code before submitting for mask ROM.

The Z86C61 Emulation Board provides emulation for Zilog's 40-pin Z86C61/63 16K/32K MCUs.

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed 16 MHz

Power Requirements
+5 Vdc @ 100 mA from Target Board

Dimensions
Width: 0.9 in. (2.28 cm)
Length: 2.7 in. (6.86 cm)

Operating Voltage Range
4.5 V to 5.5 V

Operating Temperature
0 to 70°C

Operating Humidity
10-90% RH (non-condensing)

KIT CONTENTS
Z86C6100TSC Emulation Board
CMOS Z86C12 ICE
28-Pin 16K X 8 or 32K X 8 EPROM Socket
40-Pin Z86C61/63 Socket Plug

Software (IBM®-PC Platform)
Z8/Z80/Z8000 Cross Assembler
MOBJ Link/Loader

Documentation
Z86C6100TSC Emulation Board User Guide

ORDERING INFORMATION
Part No: Z86C6100TSC

Z86C6200ZEM IN-CIRCUIT EMULATOR PRODUCT SPECIFICATION

SUPPORTED DEVICES: Z86C62, Z86C96

DESCRIPTION

The Z86C6200ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX C62 provides emulation for Zilog's Z86C62 (ROM device) and Z86C96 (ROMless device) micro-controllers. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT, 386, 486 compatible).

SPECIFICATIONS

Emulation Specification

Maximum emulation speed 16 MHz

Power Requirements

+5 Vdc @ .5 A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface

RS-232C @ 19200 baud

KIT CONTENTS

Z86C62 Emulator

- Z8® Emulation Base Board
  - CMOS Z86C9120PSC
  - 8K x 8 EPROM (Programmed with Debug Monitor)
  - 32K x 8 Static RAM
  - 3 64K x 4 Static RAM
  - RS-232C Interface
  - Reset Switch
- Z86C62 Emulation Daughter Board
  - 20 MHz CMOS Z86C9620VSC ICE Chip
  - 5 HP-16500A Logic Analysis System Interface Connectors
  - 80/60 Pin Target Connector

Cables

12", Z86C96 68-Pin PLCC Emulation Pod
12", Z86C62 64-Pin DIP Emulation Pod
48" Power Cable
15" Power Cable with Banana Plugs
60" DB 25 RS-232C Cable

Software (IBM PC Platform)

Z8/Z80®/Z8000® Cross Assembler
Windows Host Interface (GUI)
MOBJ Link/Loader
Host Package

Documentation

ICEBOX™ User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Windows Host Interface User Guide (GUI)
Registration Card

ORDERING INFORMATION

Part No: Z86C6200ZEM

Z86C1200ZEM Z8® IN-CIRCUIT EMULATOR -C12
PRODUCT SPECIFICATION

SUPPORTED DEVICES Z86C08, Z86E08, Z86C00, Z86C10, Z86C11, Z86C20, Z86C21, Z86E21[1], Z86E22[1], Z86E23[2], Z86C91

DESCRIPTION

The Z86C1200ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX -C12 provides emulation and OTP programming support for Zilog's Z8 microcontroller. The Emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The data entering, program debugging, and OTP programming are performed by the monitor ROM and the Host Package which communicates through a RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer through the RS-232C connector. The user code may then be executed using various debugging commands in the monitor. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT Compatible).

SPECIFICATIONS

Emulation Specification

Maximum Emulation Speed 16 MHz

Power Requirements

+5 Vdc @ 1.0 A

Dimensions

Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface

RS-232C @ 19200 baud

Notes:
[1] Does not support 4K/8K option bit.
[2] With Z86E2300ZDP Programming Adaptor, Rev. 1.0

KIT CONTENTS

Z86C12 Emulator

- Z8 Emulation Base Board (Revision B)
  - CMOS Z86C9120PSC
  - 8K X 8 EPROM (Programmed with Debug Monitor)
  - EPM5128 EPLD
  - 32K X 8 STATIC RAM
  - 3 64K X 4 STATIC RAM
  - RS-232C Interface
  - Reset Switch
- Z86C12 Emulation Daughter Board
  - EPM5032 EPLD
  - 16 MHz CMOS Z86C1216GSE ICE Chip
  - 40/18 Pin ZIF OTP Sockets
  - 80/60/40 Pin Target Connectors

Cables

12", 40-Pin DIP Emulation Cable
12", 28-Pin DIP Emulation Cable
12", 18-Pin DIP Emulation Cable
15", Power Cable with Banana Plugs
48", Power Cable
60", DB 25 RS-232C Cable

Software (IBM®-PC Platform)

Z8/Z80/Z8000 Cross Assembler
MOBJ Link/Loader
Host Package (Revision 1.5)
Includes Windows and non-Windows

Documentation

Emulator User Guide
Support Products Catalog
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Registration Card

ORDERING INFORMATION

Part No: Z86C1200ZEM

Z8® S SERIES EMULATORS BASE UNITS AND PODS

DESCRIPTION

The system comprises three base unit options, (64K, 128K, or 256K of emulation program ROM), and four pod options which allow the emulation of various Z8 microcontrollers. Features include real-time transparent emulation up to 20 MHz, in-line symbolic assembler and disassembler, real-time hardware breakpoints, eight channel user logic analyzer, external trigger input and outputs, trace display and memory display/edit during execution, and window or command driven user interface.

SPECIFICATIONS

Microcontrollers Emulated:

Z86C1200ZPD Z86C00, Z86C10, Z86C20, Z86C11, Z86C21, Z86E21, Z86C91, Z86C61
Z86C5000ZPD Z86C09, Z86C19, Z86C30, Z86C40, Z86C90
Z86C9300ZPD Z86C93
Z86C9500ZPD Z86C95

Maximum Emulation Speed:

Up to 30 MHz (microcontroller dependent)

Size:

260 mm wide, 260 mm deep, 64 mm high

Operating Temperature:

0°C to +40°C

Storage Temperature:

–10°C to +65°C

Operating Humidity:

0 to 90%

Maximum Emulation Program Memory:

64 Kbytes with Z86C0000ZUSP064
128 Kbytes with Z86C0000ZUSSP128
256 Kbytes with Z86C0000ZUSP256

Maximum Emulation Data Memory:

64 Kbytes

Program Memory Mapping:

1K blocks

Pass Counters:

Two, 16-bit each

Trace Buffer:

32K - 80 bits

Sequencer:

Hardware, 8 levels

User Probe:

Eight channel logic input
One trigger input
Seven trigger outputs (Events, Pass Counters, Sequencer)

Host Interface:

Asynchronous RS-232C
9600/115 KBaud
XON/XOFF support

File Upward/Downward Format:

Zilog MUFOM (EEE 695-1985)
Intel® HEX
Intel AOMF
2500AD® Software

MINIMUM HOST REQUIREMENTS

- IBM® compatible PC/XT/AT/386 or PS-2
- 640 Kbyte memory
- 20 Mbyte hard disk
- RS-232 serial port (COM 1 or COM 2)
- Mouse (serial or bus)
- MDA, CGA, EGA, or VGA video adaptor

MINIMUM EMULATION SUPPORT

- One base unit
- One emulation pod

ORDERING INFORMATION:

Base Unit	Emulation Pod
Z86C0000ZUSP064	Z86C9300ZPD
Z86C0000ZUSP128	Z86C1200ZPD
Z86C0000ZUSP256	Z86C5000ZPD
Z86C9500ZUSP064	Z86C9500ZPD

Z86E21 CMOS Z8®
8K OTP Microcontroller 7

Z86C61/62/96 CMOS Z8®
Microcontroller 8

Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
ROMless Microcontroller 10

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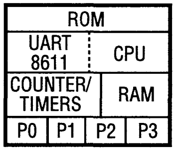
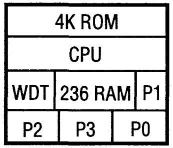
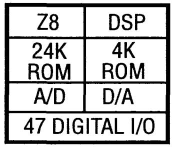
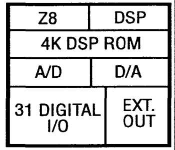
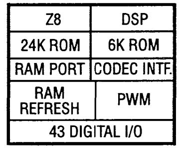
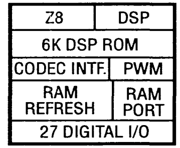
ZiLOG Fax/Modem Superintegration™ Products Guide

	Data Pump	Single Chip		Controllers			
Block Diagram	DSP 512 RAM / 4K ROM 16-BIT MAC DATA I/O / RAM I/O	Z8 / DSP 24K ROM / 4K WORD ROM 256 BYTES RAM / 512 WORD RAM 8-Bit A/D / 10-Bit D/A	Z8 / DSP 4K WORD ROM 256 BYTES RAM / 512 WORD RAM 8-BIT A/D / 10-BIT D/A	PIO / CGC WDT SIO / CTC Z80 CPU	24 I/O ESCC (2 CH) / 16550 MIMIC S180	Z80 CPU / 2 DMA 2 UART 2 C/T C/Ser MMU / OSC	ESCC
Part #	**Z89C00**	**Z89120**	**Z89920**	**Z84C15**	**Z80182**	**Z80180**	**Z85230**
Description	16-Bit Digital Signal Processor	Zilog Modem/Fax Controller (ZMFC)	Zilog Modem/Fax Controller (ZMFC)	IPC/EIPC Controller	Zilog Intelligent Peripheral (ZIP™)	High-performance Z80® CPU with peripherals	Enhanced Serial Com. Controller
Process/Speed	CMOS 10, 15 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 6, 10,16 MHz	CMOS 16, 20 MHz	6, 8, 10, 16*, 20* *Z8S180 only	CMOS 8, 10,16, 20 MHz
Features	16-bit Mac 75 ns 2 data RAMs (256 words each) 4K word ROM 64Kx16 Ext. ROM 16-bit I/O Port 74 instructions Most single cycle Two conditional branch inputs, two user outputs Library of software macros available zero overhead pointers	Z8® controller with 24 Kbyte ROM 16-bit DSP with 4K word ROM 8-bit A/D 10-bit D/A (PWM) Library of software macros available 47 I/O pins Two comparators Independent Z8® and DSP Operations Power-Down Mode	Z8 w/64K external memory DSP w/4K word ROM 8-bit A/D 10-bit D/A Library of macros 47 I/O pins Two comparators Independent Z8® and DSP Operations Power-Down Mode	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1] 3 and 5 Volt Version	Complete Static Version of Z180™ plus ESCC (2 channels of Z85230) 16550 MIMIC 24 Parallel I/O Emulation Modes[1]	Enhanced Z80® CPU MMU 1 Mbyte 2 DMAs 2 UARTs with BRGs C/Serial I/O Port Oscillator Z8S180 includes; Pwr dwn, Prgmble EMI, divide-by-one clock option	Full dual-channel SCC plus deeper FIFOs: 4 bytes on Tx 8 bytes on Rx DPLL counter per channel Software compatible to SCC
Package	68-pin PLCC 60-pin VQFP	68-pin PLCC	68-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP 100-pin VQFP	64-pin DIP 68-pin PLCC 80-pin QFP	40-pin DIP 44-pin PLCC
Other Applications	16-bit General-Purpose DSP TMS 32010/20/25 applications	Multimedia-Audio Voicemail Speech Storage and Transmission Modems FAXes, Sonabouys	Multimedia-Audio Voicemail Speech Storage and Transmission Modems FAXes, Sonabouys	Intelligent peripheral controllers Modems	General-Purpose Embedded Control Modem, Fax, Data Communications	Embedded Control	General-Purpose datacom. High performance SCC software compatible upgrade

ZiLOG Mass Storage Superintegration™ Products Guide

Block Diagram	UART CPU OSC 256 RAM CLOCK P0 P1 P2 P3	8K PROM UART CPU 256 RAM P0 P1 P2 P3	DSP 512 RAM 4K ROM 16-BIT MAC DATA I/O RAM I/O	MULT DIV UART CPU OSC 256 RAM CLOCK P0 P1 P2 P3	MULT DIV UART CPU DSP DAC PWM ADC SPI P2 P3 A15-0	88-BIT R-S ECC SRAM/DRAM CTRL DISK INTER-FACE MCU INTER-FACE AT/DE HOST INTER-FACE
Part #	**Z86C91/Z8691**	**Z86E21**	**Z89C00**	**Z86C93**	**Z86C95**	**Z86018**
Description	ROMless Z8®	Z8® 8K OTP	16-Bit Digital Signal Processor	Enhanced Z8®	Enhanced Z8® with DSP	Zilog Datapath Controller (ZDPC)
Process/Speed	CMOS 16 MHz (C91) NMOS 12 MHz (91)	CMOS 12, 16 MHz	CMOS 10, 15 MHz	CMOS 20, 25 MHz	CMOS 24 MHz	CMOS 40 MHz
Features	Full duplex UART 2 Standby Modes (STOP and HALT) 2x8 bit Counter/Timer	8K OTP ROM 256 Byte RAM Full-duplex UART 2 Standby Modes (STOP and HALT) 2 Counter/Timers ROM Protect option RAM Protect option Low EMI option	16-bit Mac 75 ns 2 data RAMs (256 words each) 4K word ROM 64Kx16 Ext. ROM 16-bit I/O Port 74 instructions Most single cycle Two conditional branch inputs, two user outputs Library of software macros available zero overhead pointers	16x16 Multiply 1.7 µs 32x16 Divide 2.0 µs Full duplex UART 2 Standby Modes (STOP and HALT) 3 16-bit Counter/Timers Pin compatible to Z86C91 (PDIP)	8 channel 8-bit ADC, 8-bit DAC 16-bit Multiply/Divide Full duplex UART SPI (Serial Peripheral Interface) 3 Standby Modes (STOP/HALT/PAUSE) Pulse Width Modulator 3x16-bit timer 16-bit DSP slave processor 83 ns Mult./Accum.	Full track read Automatic data transfer (Point & Go®) 88-bit Reed Solomon ECC "on the fly" Full AT/IDE bus interface 64 KB SRAM buffer 1 MB DRAM buffer Split data field support 100-pin VQFP package JTAG boundary scan option Up to 8 KB buffer RAM reserved for MCU
Package	40-pin DIP 44-pin PLCC 44-pin QFP	40-pin DIP 44-pin PLCC 44-pin QFP	68-pin PLCC 60-pin VQFP	40-pin DIP 44-pin PLCC 44-pin QFP 48-pin VQFP	80-pin QFP 84-pin PLCC 100-pin VQFP	100-pin VQFP 100-pin QFP
Application	Disk Drives Modems Tape Drives	Software Debug Z8® prototyping Z8® production runs Card Reader	Disk Drives Tape Drives Servo Control Motor Control	Disk Drives Tape Drives Modems	Disk Drives Tape Drives Servo Control Motor Control	Hard Disk Drives

Block Diagram						
Part #	**Z08600/Z08611**	**Z86C30/E30 Z86C40/E40**	**Z89C65**	**Z89C66**	**Z89C67**	**Z89C68**
Description	Z8® NMOS (CCP™) 8600 = 2K ROM 8611 = 4K ROM	Z8® Consumer Controller Processor (CCP™) with 4K ROM C30 = 28-pin C40 = 40-pin E30/E40 = OTP version	Telephone Answering Controller with DSP LPC voice synthesis and DTMF detection	Telephone Answering Controller with DSP LPC voice synthesis and DTMF detection and external ROM/RAM interface	Telephone Answering Controller with digital voice encode and decode DTMF detection and full memory control interface	Telephone Answering Controller with digital voice encode and decode DTMF detection and external ROM/RAM interface
Process/Speed	NMOS 8,12 MHz	CMOS 12 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 20 MHz	CMOS 20 MHz
Features	2K/4K ROM 128 Bytes RAM 22/32 I/O lines On-chip oscillator 2 Counter/Timers 6 vectored, priority interrupts UART (Z8611)	4K ROM, 236 RAM 2 Standby Modes 2 Counter/Timers ROM Protect RAM Protect 4 Ports (86C40/E40) 3 Ports (86C30/E30) Brown-Out Protection 2 Analog Comparators Low EMI Watch-Dog Timer Auto Power-On Reset Low Power option	Z8® Controller 24K ROM 16-bit DSP 4K Word ROM 8-bit A/D with AGC DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available 47 I/O Pins	Z8® Controller 16-bit DSP 4K Word ROM 8-bit A/D with AGC DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available External ROM/RAM capability 31 I/O Pins	Z8® Controller 24K ROM 16-bit DSP 6K Word ROM DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available ARAM/DRAM/ROM Controller & Interface Dual Codec Interface 43 I/O	Z8® Controller 64K ROM (external) 16-bit DSP, 6K word ROM DTMF macro available LPC macro available 10-bit PWM D/A Other DSP software options available ARAM/DRAM control/ interface External ROM/RAM Dual Codec Interface 27 I/O
Package	28-pin DIP 40-pin DIP 44-pin PLCC	28-pin DIP 40-pin DIP 44-pin PLCC, QFP	68-pin PLCC	68-pin PLCC	84-pin PLCC	84-pin PLCC
Application	Low cost tape board TAD	Window Control Wiper Control Sunroof Control Security Systems TAD	Fully featured cassette answering machines with voice prompts and DTMF signaling	General-Purpose DSP applications in TAD and other high-performance 1-tape voice processors	Voice Processing, DSP applications in tapeless TAD and other high-performance 1-tape voice processors	Voice Processing, DSP applications in tapeless TAD and other high-performance 1-tape voice processors

ZiLOG Video Products — Superintegration™ Products Guide

	TV Controller			IR Controller		Cable TV	
Block Diagram	8K ROM 4K CHAR ROM Z8 CPU | RAM OSD 13 PWM | TIMER WDT | 5 PORTS	6K ROM 3K CHAR ROM Z8 CPU | RAM OSD 7 PWM | TIMER WDT | 3 PORTS	CHAR ROM COMMAND INTERPRETER ANALOG SYNC/DATA SLICER | OSD CTRL	1K/6K ROM Z8 CPU WDT | 124 RAM P2 | P3	2K/8K/16K ROM Z8 CPU WDT | 128,256, 768 RAM P0 | P1 | P2 | P3	4K ROM CPU WDT | 236 RAM | P1 P2 | P3 | P0	16K ROM | UART CPU | 236 RAM P0 | P1 | P2 P3 | P4 | P5 | P6
Part #	**Z86C27/127/97**	**Z86227**	**Z86128**	**Z86L06/L29**	**Z86L70/71/72** (Q193)	**Z86C40/E40**	**Z86C61/62**
Description	Z8® Digital Television Controller MCU with logic functions needed for Television Controller, VCRs and Cable	Standard DTC features with reduced ROM, RAM, PWM outputs for greater economy	Line 21 Controller (L21C™) for Closed Caption Television	18-pin Z8® Consumer Controller Processor (CCP™) low-voltage and low-current battery operation 1K-6K ROM	Z8® (CCP™) low-voltage parts that have more ROM, RAM and special Counter/Timers for automated output drive capabilities	Z8® Consumer Controller Processor (CCP™) with 4K ROM (C40) E40 = OTP version	Z8® MCU with Expanded I/O's and 16K ROM
Process/Speed	CMOS 4 MHz	CMOS 4 MHz	CMOS 12 MHz	Low Voltage CMOS 8 MHz	Low Voltage CMOS 8 MHz	CMOS 12 MHz	CMOS 16, 20 MHz
Features	Z8/DTC Architecture 8K ROM, 256-byte RAM 160x7-bit video RAM On-Screen Display (OSD) video controller Programmable color, size, position attributes 13 PWMs for D/A conversion 128-character set 4Kx6-bit char. Gen. ROM Watch-Dog Timer (WDT) Brown-Out Protection 5 Ports/36 pins 2 Standby Modes Low EMI Mode	Z8/DTC Architecture 6K ROM, 256-byte RAM 120x7-bit video RAM OSD on board Programmable color, size, position attributes 7 PWMs 96-character set 3Kx6-bit character generator ROM Watch-Dog Timer (WDT) Brown-Out Protection 3 Ports/20 pins 2 Standby Modes Low EMI Mode	Conforms to FCC Line 21 format Parallel or serial modes Stand-alone operation On-board data sync and slicer On-board character generator - Color - Blinking - Italic - Underline	Z8® Architecture 1K ROM & 6K ROM Watch-Dog Timer 2 Analog Comparators with output option 2 Standby Modes 2 Counter/Timers Auto Power-On Reset 2 volt operation RC OSC option Low Noise option Brown-Out Protection High current drivers (2, 4)	Z8® Architecture 2K/8K/16K ROM Watch-Dog Timer 2 Analog Comparators with output option 2 Standby Modes 2 Enhanced Counter/Timers, Auto Pulse Reception/Generation Auto Power-On Reset 2 volt operation RC OSC option Brown-Out Protection High current drivers (4)	4K ROM, 236 RAM 2 Standby Modes 2 Counter/Timers ROM Protect RAM Protect 4 Ports Brown-Out Protection 2 Analog Comparators Low EMI Watch-Dog Timer Auto Power-On Reset Low Power option	16K ROM Full duplex UART 2 Standby Modes (STOP and HALT) 2 Counter/Timers ROM Protect option RAM Protect option Pin compatible to Z86C21 C61 = 4 Ports C62 = 7 Ports
Package	64-pin DIP 52-pin active (127)	40-pin DIP	18-pin DIP	18-pin DIP 18-pin SOIC	20-pin DIP (L71), 18-pin DIP, SOIC (L70) 40,44-pin DIP, PLCC, QFP (L72)	40-pin DIP	40-pin DIP (C61) 44-pin PLCC,QFP (C61) 68-pin PLCC (C62)
Application	Low-end Television Cable/Satellite Receiver	Low-end Television Cable/Satellite Receiver	TVs, VCRs, Decoders	I.R. Controller Portable battery operations	I.R. Controller Portable battery operations	Window Control Wiper Control Sunroof Control Security Systems TAD	Cable Television Remote Control Security

Zilog Datacommunications Superintegration™ Products Guide

Block Diagram	SCC	ESCC	SCC DMA DMA DMA DMA BIU	PIO, CGC WDT SIO, CTC Z80 CPU	CTC, SCC/2 (85C30/2) 16 I/O Z180	24 I/O 85230 ESCC (2 CH), 16550 MIMIC S180	USC	USC/2 TSA	USC/2 DMA DMA
Part #	**Z8030/Z80C30 Z8530/Z85C30**	**Z85230/Z80230 Z85233***	**Z16C35**	**Z84C15**	**Z80181**	**Z80182**	**Z16C30**	**Z16C33**	**Z16C32**
Description	Serial Com. Controller	Enhanced Serial Com. Controller	Integrated Serial Com. Controller	Intelligent Peripheral Controller	Smart Access Controller	Zilog Intelligent Peripheral	Universal Serial Controller	Mono-channel Universal Serial Controller	Integrated Universal Serial Controller
Process/ Speed/ Clock Data Rate	NMOS: 4, 6, 8 MHZ CMOS: 8,10 16 MHz 2, 2.5, 4 Mb/s	CMOS: 10, 16 20 MHz 2.5, 4.0, 5.0 Mb/s	CMOS: 10, 16 MHz 2.5, 4.0 Mb/s	CMOS 6, 10,16 MHz	10, 12.5	CMOS 16, 20 MHz	CMOS: 20 MHz CPU Bus 10 Mb/s 20 Mb/s	CMOS: 10 MHz CPU Bus 10 Mb/s	CMOS:20 MHz CPU Bus 16 Mb/s 20 Mb/s
Features	Two independent full-duplex channels Enhanced DMA support: 10x19 status FIFO 14-bit byte counter NRZ/NRZI/FM	Full dual-channel SCC plus deeper FIFOs: 4 bytes on Tx 8 bytes on Rx DPLL counter per channel Software compatible to SCC *One channel of Z85230	Full dual-channel SCC plus 4 DMA controllers and a bus interface unit	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1] 3 and 5 Volt Version	Complete Z180™ plus SCC/2 CTC 16 I/O lines Emulation Mode[1]	Complete Static version of Z180 plus ESCC (2 channels of 85230) 16550 MIMIC 24 Parallel I/O Emulation Mode[1]	Two dual-channel 32-byte receive & transmit FIFOs 16-bit bus B/W: 18.2 Mb/s 2 BRGs per channel Flexible 8/16-bit bus interface	Single-channel (half of USC™) plus Time Slot Assigner functions for ISDN	Single-channel (half of USC) plus two DMA controllers Array chained and linked-list modes with ring buffer support
Package	40-pin DIP 44-pin CERDIP 44-pin PLCC	40-pin DIP 44-pin PLCC *44-pin QFP (85233)	68-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP	100-pin QFP 100-pin VQFP	68-pin PLCC	68-pin PLCC	68-pin PLCC
Application	General-Purpose datacom.	General-Purpose datacom. High performance SCC software	High performance datacom. SCC upgrades	Intelligent peripheral controllers Modems	Intelligent peripheral controllers Printers, Faxes, Modems, Terminals	General-Purpose Embedded Control Modem, Fax, Data Communications	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay	General-Purpose high-end datacom. Ethernet HDLC X.25 Frame Relay

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ZILOG Z80® Embedded Controllers Superintegration™ Products Guide

Block Diagram	84C01* CPU OSC PWR. DOWN; 2K BYTES SRAM; WSG	SIO; CTC; PIO; PIA; OSC	CTC; CGC; SIO; WDT; Z80 CPU	PIO; CGC; WDT; SIO; CTC; Z80 CPU	40 I/O; CTC; WDT; Z80 CPU	Z80 CPU; 2 DMA; 2 UART; 2 C/T; C/Ser; MMU; OSC	16-BIT Z80 CPU; OSC; 4 DMA; Z80/Z-BUS INTERFACE; UART; MMU; 3 C/T; CACHE; WSG	CTC; 16 I/O; SCC/2 (85C30/2); Z180	24 I/O; 85230 ESCC (2 CH); 16550 MIMIC; S180
Part #	**Z84C50**	**Z84C90**	**Z84013/C13**	**Z84015/C15**	**Z84011/C11**	**Z80180/S180**	**Z80280**	**Z80181**	**Z80182**
Description	Z80/84C01 with 2K SRAM	Killer I/O (3 Z80 peripherals)	Intelligent Peripheral Controller	Intelligent Peripheral Controller	Parallel I/O Controller	High-performance Z80® CPU with peripherals	16-bit Z80® code compatible CPU with peripherals	Smart Access Controller	Zilog Intelligent Peripheral
Speed MHz	10	8, 10, 12.5	6, 10	6, 10, 16	6, 10	6, 8, 10, 16*, 20* *Z8S180 only	10, 12	10, 12.5	16, 20
Features	Z80® CPU 2 Kbytes SRAM WSG Oscillator Pin compatible with Z84C00 DIP & PLCC EV mode[1] *84C01 is available as a separate part	SIO, PIO, CTC plus 8 I/O lines	Z80® CPU, SIO, CTC WDT, CGC, WSG, Power-On Reset 2 chip selects EV mode[1]	Z80® CPU, SIO, CTC WDT, CGC The Z80 Family in one device Power-On Reset Two chip selects 32-bit CRC WSG EV mode[1]	Z80® CPU, CTC, WDT 40 I/O lines bit programmable Power-On Reset EV mode[1]	Enhanced Z80 CPU MMU 1 Mbyte 2 DMAs 2 UARTs with BRGs C/Serial I/O Port Oscillator Z8S180 includes; Pwr dwn, Prgmble EMI, divide-by-one clock option	16-bit code compatible Z80® CPU Three stage pipeline MMU 16 Mbyte CACHE 256 byte Inst. & Data Peripherals 4 DMAs, UART, 3 16-bit C/T, WSG Z80/Z-BUS® interface	Complete Z180 plus SCC/2 CTC 16 I/O lines Emulation Mode[1]	Complete Static Version of Z180™ plus ESCC (2 channels of Z85230) 16550 MIMIC 24 Parallel I/O Emulation Modes[1]
Package	40-pin DIP 44-pin PLCC 44-pin QFP	84-pin PLCC	84-pin PLCC	100-pin QFP 100-pin VQFP	100-pin QFP	64-pin DIP 68-pin PLCC 80-pin QFP	68-pin PLCC	100-pin QFP	100-pin QFP 100-pin VQFP
Application	Embedded Controllers	General-purpose peripheral that can be used with Z80 and other CPU's	Intelligent datacom controllers	Intelligent peripheral controllers Modems	Intelligent parallel-I/O controllers Industrial display terminals	Embedded Control	Embedded Control Terminals Printers	Intelligent peripheral controllers Printers, Faxes, Modems, Terminals	General-Purpose Embedded Control Modem, Fax, Data Communications

[1] Allows use of existing development systems.

Peripherals — Superintegration™ Products Guide

	Z8036 Z8536	Z32H00	Z5380 Z53C80	Z85C80
Description	Counter/Timer & parallel I/O Unit (CIO)	Hyperstone Enhanced Fast Instruction Set Computer (EFISC) Embedded (RISC) Processor	Small Computer System Interface (SCSI)	Serial Communication Controller and Small Computer System Interface
Process/ Speed	NMOS 4,6 MHz	CMOS 25 MHz	CMOS Z5380: 1.5 MB/s Z53C80: 3.0 MB/s	CMOS SCC - 10, 16 MHz SCSI - 3.0 MB/s
Features	Three 16-bit Counter/Timers, Three I/O ports with bit catching, pattern matching interrupts and handshake I/O	32-bit MPU 4 Gbytes address space 19 global and 64 local registers of 32 bits each 128 bytes instruction cache 1.2μ CMOS 42 mm^2 die	ANSI X3.131-1986 Direct SCSI bus interface On-board 48 mA drivers Normal or Block mode DMA transfers Bus interface, target and initiator	Full dual-channel SCC plus SCSI sharing databus and read/write functions
Package	40-pin PDIP 44-pin PLCC	144-pin PGA 132-pin QFP	Z5380: 40-pin DIP 44-pin PLCC Z53C80: 48-pin DIP 44-pin PLCC	68-pin PLCC
Application	General-Purpose Counter/Timers and I/O system designs	Embedded high-performance industrial controller Workstations	Bus host adapters, formatters, host ports	AppleTalk® networking SCSI disk drives

[2] Software and hardware compatible with discrete devices.

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Z86C63/64 32K ROM Z8®
CMOS Microcontroller 9

Z86C91 CMOS Z8®
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LITERATURE GUIDE

Z8®/SUPER8™ MICROCONTROLLER FAMILY

Databooks	Part No	Unit Cost
Z8 Microcontrollers Databook (includes the following documents)	**DC-8275-04**	**5.00**

Z8 CMOS Microcontrollers
Z86C00/C10/C20 MCU OTP Product Specification
Z86C06 Z8 CCP™ Preliminary Product Specification
Z86C08 8-Bit MCU Product Specification
Z86E08 Z8 OTP MCU Product Specification
Z86C09/19 Z8 CCP Product Specification
Z86E19 Z8 OTP MCU Advance Information Specification
Z86C11 Z8 MCU Product Specification
Z86C12 Z8 ICE Product Specification
Z86C21 Z8 MCU Product Specification
Z86E21/Z86E22 OTP Product Specification
Z86C30 Z8 CCP Product Specification
Z86E30 Z8 OTP CCP Product Specification
Z86C40 Z8 CCP Product Specification
Z86E40 Z8 OTP CCP Product Specification
Z86C27/97 Z8 DTC™ Product Specification
Z86127 Low-Cost Digital Television Controller Adv. Info. Spec.
Z86C50 Z8 CCP ICE Advance Information Specification
Z86C61 Z8 MCU Advance Information Specification
Z86C62 Z8 MCU Advance Information Specification
Z86C89/C90 CMOS Z8 CCP Product Specification
Z86C91 Z8 ROMless MCU Product Specification
Z86C93 Z8 ROMless MCU Preliminary Product Specification
Z86C94 Z8 ROMless MCU Product Specification
Z86C96 Z8 ROMless MCU Advance Information Specification
Z88C00 CMOS Super8 MCU Advance Information Specification

Z8 NMOS Microcontrollers
Z8600 Z8 MCU Product Specification
Z8601/03/11/13 Z8 MCU Product Specification
Z8602 8-Bit Keyboard Controller Preliminary Product Spec.
Z8604 8-Bit MCU Product Specification
Z8612 Z8 ICE Product Specification
Z8671 Z8 MCU With BASIC/Debug Interpreter Product Spec.
Z8681/82 Z8 MCU ROMless Product Specification
Z8691 Z8 MCU ROMless Product Specification
Z8800/01/20/22 Super8 ROMless/ROM Product Specification

Peripheral Products
Z86128 Closed-Captioned Controller Adv. Info. Specification
Z765A Floppy Disk Controller Product Specification
Z5380 SCSI Product Specification
Z53C80 SCSI Advance Information Specification

Z8 Application Notes and Technical Articles
Zilog Family On-Chip Oscillator Design
Z86E21 Z8 Low Cost Thermal Printer
Z8 Applications for I/O Port Expansions
Z86C09/19 Low Cost Z8 MCU Emulator
Z8602 Controls A 101/102 PC/Keyboard
The Z8 MCU Dual Analog Comparator
The Z8 MCU In Telephone Answering Systems
Z8 Subroutine Library
A Comparison of MCU Units
Z86xx Interrupt Request Registers
Z8 Family Framing
A Programmer's Guide to the Z8 MCU
Memory Space and Register Organization

Super8 Application Notes and Technical Articles
Getting Started with the Zilog Super8
Polled Async Serial Operations with the Super8
Using the Super8 Interrupt Driven Communications
Using the Super8 Serial Port with DMA
Generating Sine Waves with Super8
Generating DTMF Tones with Super8
A Simple Serial Parallel Converter Using the Super8

Additional Information
Z8 Support Products
Zilog Quality and Reliability Report
Literature List
Package Information
Ordering Information

Z8®/SUPER8™ MICROCONTROLLER FAMILY (Continued)

Databooks	Part No	Unit Cost
Digital Signal Processor Databook (includes the following documents) Z86C95 Z8® Digital Signal Processor Preliminary Product Specification Z89C00 16-Bit Digital Signal Processor Preliminary Product Specification Z89C00 DSP Application Note "Understanding Q15 Two's Complement Fractional Multiplication" Z89120, Z89920 (ROMless) 16-Bit Mixed Signal Processor Preliminary Product Specification Z89121, Z89921 (ROMless) 16-Bit Mixed Signal Processor Preliminary Product Specification Z89320 16-Bit Digital Signal Processor Preliminary Product Specification Z89321 16-Bit Digital Signal Processor Advance Information Specification	DC-8299-02	3.00
Telephone Answering Device Databook (includes the following documents) Z89C65, Z89C66 (ROMless) Dual Processor T.A.M. Controller Preliminary Product Specification Z89C67, Z89C68 (ROMless) Dual Processor Tapeless T.A.M. Controller Preliminary Product Specification	DC-8300-01	3.00
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Technical Articles

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- Serial Communication with the Z80A DART
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- Serial Clock Generation Using the Z8536 CIO
- Timing in an Interrupt-Based System with the Z80® CTC
- A Z80-Based System Using the DMA with the SIO
- Interfacing the Z8500 Peripherals to the 68000
- Z180™ Break Detection
- The Z180™ Interfaced with the SCC at 10 MHz
- Technical Considerations When Implementing LocalTalk Link Access Protocol
- Using the Z84C11/C13/C15 in Place of the Z84011/013/015
- Using SCC with Z8000 in SDLC Protocol
- SCC in Binary Synchronous Communications
- On-Chip Oscillator Design
- Interfacing Z80® CPUs to the Z8500 Peripheral Family
- Boost Your System Performance Using The Zilog ESCC™
- Design a Serial Board to Handle Multiple Protocols
- Using the Z16C30 USC Universal Serial Controller
- Datacommunications IUSC/MUSC Time Slot Assigner
- Integrating Serial Data and SCSI Peripheral Control on One Chip
- A Fast Z80® Embedded Controller
- Using the Zilog Datacom Family with the 80186 CPU

Questions and Answers

- Z80® Questions and Answers
- Z180™ Questions and Answers
- SCC Questions and Answers
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- Classic Family
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Catalogs, Handbooks, Product Flyers and Users Guides	Part No	Unit Cost
Superintegration Shortform Catalog 1992	DC-5472-11	N/C
Superintegration Products Guide	DC-5499-07	N/C
ZIA™ 3.3-5.5V Matched Chip Set for AT Hard Disk Drives Datasheet	DC-5556-01	N/C
ZIA ZIA00ZCO Disk Drive Development Kit Datasheet	DC-5593-01	N/C
Zilog Hard Disk Controllers - Z86C93/C95 Datasheet	DC-5560-01	N/C
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Zilog ASSPs - Partnering With You Product Flyer	DC-5553-01	N/C
Quality and Reliability Report	DC-2475-11	N/C
The Handling and Storage of Surface Mount Devices User's Guide	DC-5500-02	N/C
Universal Object File Utilities User's Guide	DC-8236-04	3.00
Zilog 1991 Annual Report	DC-1991-AR	N/C
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