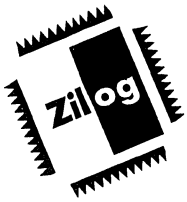
Zilog Wireless Databook

Wireless Databook

Includes Specifications for the following Parts:

Z87000 Z87L00
Z87010 Z87L10
Z87100 Z87200



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Includes Specifications for the following Devices:

- Z87000/Z87L00
- Z87010/Z87L10
- Z87100
- Z87200

Q4/96 DB96WRL0101

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INTRODUCTION

ZILOG'S FOCUS ON APPLICATION-SPECIFIC PRODUCTS HELPS YOU MAINTAIN YOUR TECHNOLOGICAL EDGE

Comprehensive Wireless Solutions

Zilog's Wireless family of products provides comprehensive solutions for a wide range of high-volume wireless systems—from telephony to automated meter reading, and narrowband to spread-spectrum technology. Zilog develops its own application technology in house, so the Zilog Wireless products are individually tailored to their end-product application for high-performance and cost-effective results.

Total Customer Support

Zilog's customer support program dramatically shortens the design-to-production cycle. Our worldwide, dedicated engineering team works with you to develop your solutions using a comprehensive suite of development tools. Every Zilog Wireless controller has an In-Circuit Emulator (ICE-BOX™), application board, and C programming language compiler for complete and individualized product support.

WIRELESS DATABOOK

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Z87000/Z87L00
Spread Spectrum Controllers

Z87000/Z87L00

SPREAD SPECTRUM CONTROLLERS

FEATURES

Device	ROM (KWords)	RAM* (Words)	I/O Lines	Package Information
Z87000	12	512	32	84-Pin PLCC 100-Pin QFP
Z87L00	12	512	32	100-Pin QFP

Note: *General-Purpose

- Transceiver/Controller Chip Optimized for Implementation of 900 MHz Spread Spectrum Cordless Phone
  - Adaptive Frequency Hopping
  - Transmit Power Control
  - Error Control Signaling
  - Handset Power Management
  - Support of 32 kbps ADPCM Speech Coding for High Voice Quality
- DSP Core Acts as Phone Controller
  - Zilog-Provided Embedded Transceiver Software to Control Transceiver Operation and Base Station-Handset Communications Protocol
  - User-Modifiable Software Governs Phone Features
- Transceiver Circuitry Provides Primary Cordless Phone Communications Functions
  - Digital Downconversion with Automatic Frequency Control (AFC) Loop
  - FSK Demodulator
  - FSK Modulator
  - Symbol Synchronizer
  - Time Division Duplex (TDD) Transmit and Receive Buffers
- On-Chip A/D and D/A to Support 10.7 MHz IF Interface
- Bus Interface to Z87010 ADPCM Processor
- Static CMOS for Low Power Consumption
- 3.0V to 3.6V, -20°C to +70°C, Z87L00
4.5V to 5.5V, -20°C to +70°C, Z87000
- 16.384 MHz Base Clock

GENERAL DESCRIPTION

The Z87000/Z87L00 FHSS Cordless Telephone Transceiver/Controllers are expressly designed to implement a 900 MHz frequency hopping spread spectrum cordless telephone compliant with United States FCC regulations for unlicensed operation. The Z87000 and Z87L00 are distinct 5V and 3.3V versions, respectively, of the device. For the sake of brevity, all subsequent references to the Z87000 in this document also apply to the Z87L00, unless specifically noted.

The Z87000 supports a specific cordless phone system design that uses frequency hopping and digital modulation to provide extended range, high voice quality, and low system costs.The Z87000 uses a Zilog 16-bit fixed-point two's complement static CMOS Digital Signal Processor core as the phone and RF section controller. The Z87000's DSP core processor further supports control of the RF section's frequency synthesizer for frequency hopping and the generation of the control messages needed to coordinate incorporation of the phone's handset and base station.

GENERAL DESCRIPTION (Continued)

Additional on-chip transceiver circuitry supports Frequency Shift Keying modulation/demodulation and multiplexing/demultiplexing of the 32 kbps voice data and 4 kbps command data between handset and base station. The Z87000 provides thirty-two I/O pins, including four wake-up inputs and two CPU interrupt inputs. These programmable I/O pins allow a variety of user-determined phone features and board layout configurations. Additionally, the pins may be used so that phone features and interfaces are supported by an optional microcontroller rather than by the Z87000's DSP core.

In combination with an RF section designed according to the system specifications, Zilog's Z87010/Z87L10 ADPCM Processor, a standard 8-bit PCM telephone CODEC and minimal additional phone circuity, the Z87000 and its embedded software provide a total system solution.

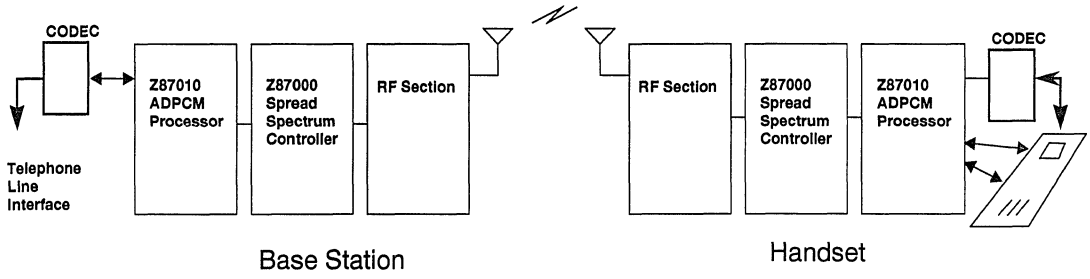

Figure 1. System Block Diagram of a Z87000/Z87010 Based Phone

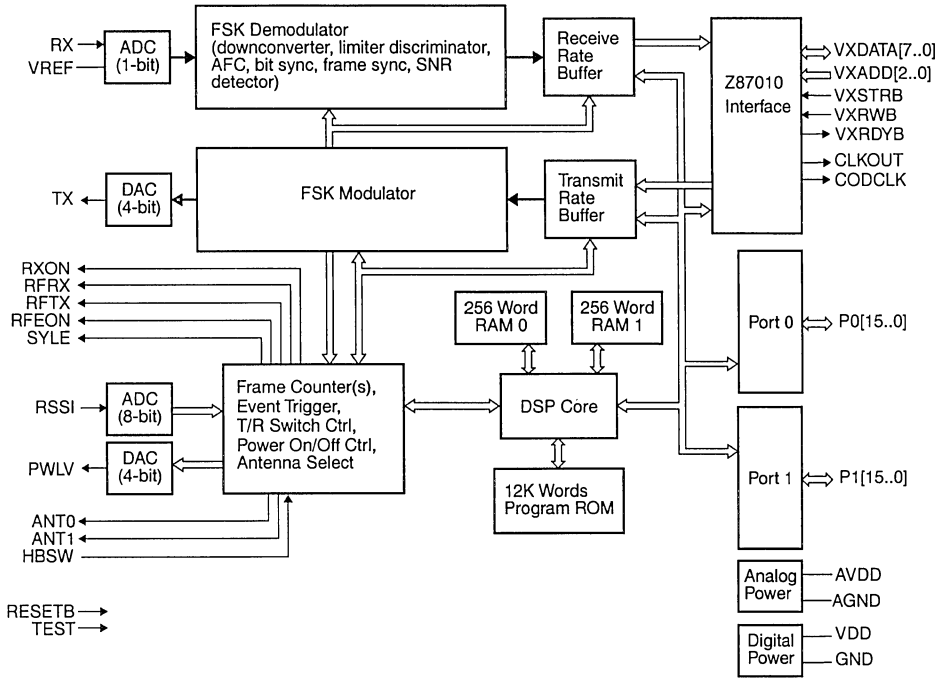

Figure 2. Z87000 Functional Block Diagram

PIN DESCRIPTION

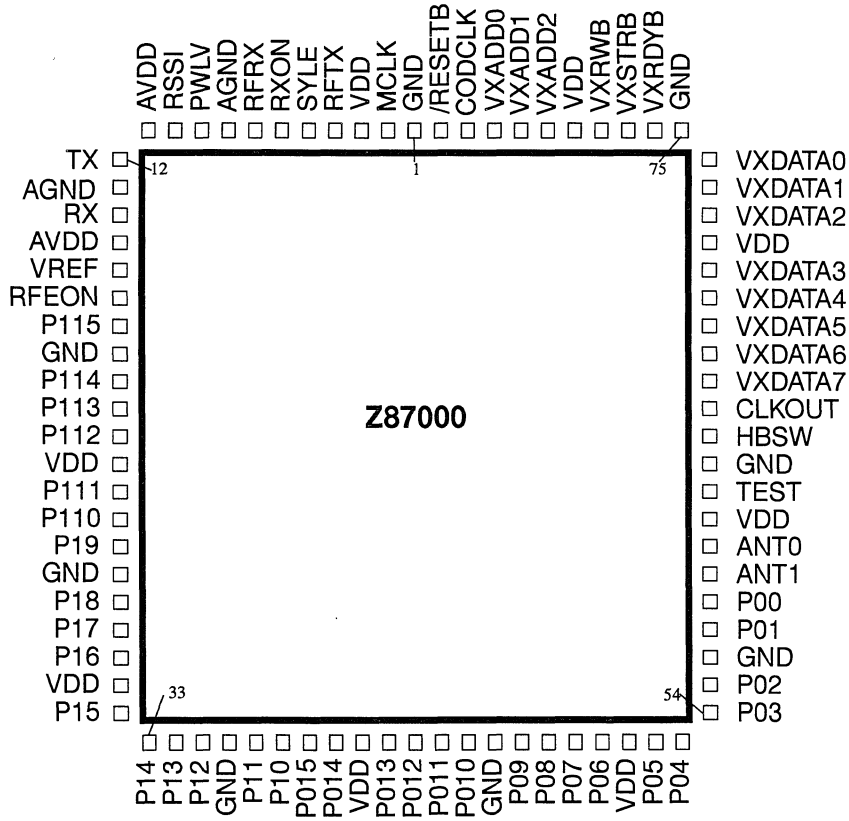

Figure 3. 84-Pin PLCC ROM Pin Configuration (Z87000 only)

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Table 1. 84-Pin PLCC Pin Description Summary

Pin Number	Symbol	Function	Direction
1,19,27,36,46, 56,63,75	GND	Ground	–
2	MCLK	Master clock (16.384 MHz)	Input
3,23,31,41,51, 61,71,79	V_{DD}	Digital	–
4	RFTX	RF transmit switch control	Output
5	SYLE	RF synthesizer load enable	Output
6	RXON	Demodulator "on" indication	Output
7	RFRX	RF receive switch control	Output
8,13	AGND	Analog ground	–
9	PWLV	RF transmit power level	Output
10	RSSI	RF receive signals strength indicator	Input
11,15	AV_{DD}	Analog V_{DD}	–
12	TX	Analog transmit IF signal	Output
14	RX	Analog receive IF signal	Input
16	V_{REF}	Analog reference voltage for RX signal	Output
17	RFEON	RF module on/off control	Output
18,20,21,22,24, 25,26,28,29,30, 32,33,34,35,37,38	P115	General-purpose	Input
59,60	ANT1	RF diversity antenna control	Input/Output
62	TEST	Main test mode control	Input
64	HBSW	Handset/Base Control	–
65	CLKOUT	Clock output to ADPCM Processor	Output
76	VXRDYB	ADPCM processor ready signal	Output
77	VXSTRB	ADPCM processor data strobe	Input
78	VXRWB	ADPCM read/write control	Input
80,81,82	VXADD2	ADPCM processor address bus	Input
83	CODCLK	Clock output to codec	Output
84	/RESETB	Reset signal	Input

PIN DESCRIPTION (Continued)

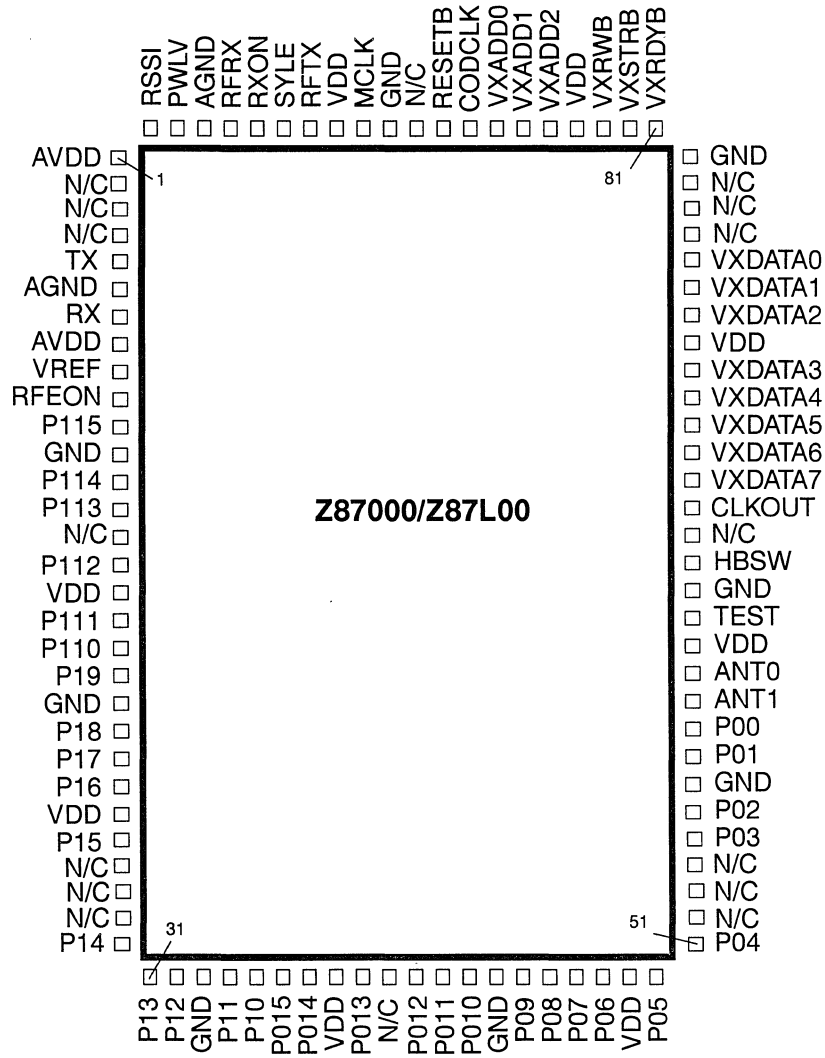

Figure 4. 100-Pin QFP Pin Configuration

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Table 2. 100-Pin QFP Pin Configuration

No	Symbol	Function	Direction
1,8	AV_{DD}	Analog V_{DD}	–
2,3,4,15,27,28, 29,40,52,53,54, 66,77,78,79,90	N/C	No connection	–
5	TX	Analog transmit IF signal	Output
6,98	AGND	Analog ground	–
7	RX	Analog receive IF signal	Input
9	VREF	Analog reference voltage for RX signal	–
10	RFEON	RF module on/off control	Output
11,13,14,16,18, 19,20,22,23,23, 26,30,31,32,34,35	P1[15..0]	General-purpose I/O port 0	Input
17,25,38,49,62, 73,84,93	V_{DD}	Digital	–
36,37,39,41,42, 43,45,46,47,48, 50,51,55,56,58,59	P0[15..0]	General-purpose I/O port 0	Input
60,61	ANT[1..0]	RF diversity antenna control	Input/Output
63	TEST	Main test mode control	Input
65	HBSW	Handset/bast control	Input
67	CLKOUT	Clock output to ADPCM processor	Output
68,69,70,71,72, 74,75,76	VXDATA[7..]	ADPCM processor data bus	Input
81	VXRDYB	ADPCM processor ready signal	Output
82	VXSTRB	ADPCM processor data strobe	Input
83	VXRWB	ADPCM processor read/write control	Input
85,86,87	VXADD[2..0]	ADPCM processor address bus	Input
88	CODCLK	Clock output to codec	Output
89	/RESETB	Reset signal	Input
92	MCLK	Master clock input (16.384 MHz)	Input
94	RFTX	RF transmit switch control	Output
95	SYLE	RF synthesizer load enable	Output
96	RXON	Demodulator "on" indication	Output
97	RFRX	RF receive switch control	Output
99	PWLV	RF transmit power level	Input
100	RSSI	RF receive signal strength indicator	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	DC Supply Voltage(1)	-0.5	7.0	V
V_{IN}	Input Voltage(2)	-0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage(3)	-0.5	V_{DD} + 0.5	V
T_A	Operating Temperature	-20	+70	°C
T_{STG}	Storage Temperature	-65	+150	°C

Notes:
1. Voltage on all pins with respect to GND.
2. Voltage on all inputs WRT VDD
3. Voltage on all outputs WRT VDD

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The electrical characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pins. Standard test conditions are as follows:

- $3.0V < V_{DD} < 3.6V$ (Z87L00)
- $4.5V < V_{DD} < 5.5V$ (Z87000)
- GND = 0V
- T_A = -20 to +70 °C

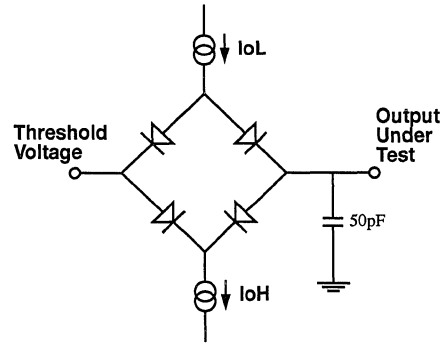

Figure 5. Test Load Diagram

RECOMMENDED OPERATING CONDITIONS

Table 3. 5V ± 0.5V Operation (Z87000)

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.8	V
I_{OH}	Output High Current		-2.0	mA
I_{OL1}	Output Low Current		4.0	mA
I_{OL2}	Output Low Current, Ports (limited usage, 1)		12.0	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]

Table 4. 3.3V ± 0.3V Operation (Z87L00)

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	3.0	3.6	V
V_{IH}	Input High Voltage	0.7 V_{DD}	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.1 V_{DD}	V
I_{OH}	Output High Current		-1.0	mA
I_{OL1}	Output Low Current		2.0	mA
I_{OL2}	Output Low Current, Ports (limited usage, 2)		6.0	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]

DC ELECTRICAL CHARACTERISTICS

Conditions for DC characteristics are corresponding operating conditions, and standard test conditions, unless otherwise specified.

Table 5. 5V ± 0.5V Operation (Z87000)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	2.4		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.6	V
V_{OL2}	Output Low Voltage, Ports (1)	V_{DD} min, I_{OL2} max		1.2	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			80	mA
I_{CC2}	Standby Mode Current (2)			4	mA

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]
2. 2.3 mA typical at 25°C, 5 volts.

Table 6. 3.3V ± 0.3V Operation (Z87L00)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	1.6		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.4	V
V_{OL2}	Output Low Voltage, Ports(1)	V_{DD} min, I_{OL2} max		1.2	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			55	mA
I_{CC2}	Standby Mode Current(2)		1.4		mA

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]
2. 1.6 mA typical at 25°C, 3.3 volts.

ANALOG CHARACTERISTICS

Table 7. 1-Bit ADC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	1	-	bit
Power dissipation	0.54 (70°c)	1.0 (40°c)	2.75 (-20°c)	mW
Power dissipation, Stop mode	0.06 (70°c)	0.2 (40°c)	1.1 (-20°c)	mW
Sample frequency	-	8.192	-	MHz
Sample window(1)	29	31	33	ns
Bandwidth	-	60	-	MHz
Supply Range(=AV_{DD})				
Z87L00	3.0		3.6	V
Z87000	4.5		5.5	V
Acquisition time	2	3	8	ns
Settling time	8	10	18	ns
Conversion time	4	6	18	ns
Aperture delay	2	3	8.5	ns
Aperture uncertainty(2)	-	-	0.5	ns
Input voltage range (p-p)	800	1000	1200	mV
Reference voltage				
Z87L00	1.7 (AV_{DD}= 3V)	1.9 (AV_{DD}= 3.3V)	2.1 (AV_{DD}= 3.6V)	V
Z87000	2.7 (AV_{DD}=4.5V)	3.0 (AV_{DD}= 5V)	3.3 (AV_{DD}= 5.5V)	V
Input resistance	10	18	25	KOhm
Input capacitance	-	10	-	pF

Notes:
Window of time while input signal is applied to sampling capacitor; see next figure.
Uncertainty in sampling time due to random variations such as thermal noise.

ANALOG CHARACTERISTICS (Continued)

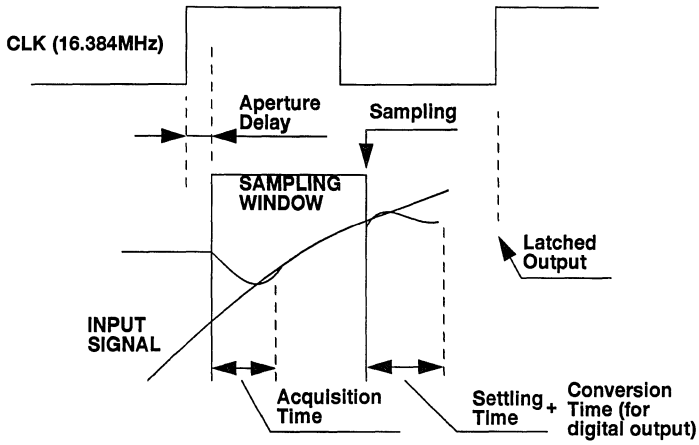

Figure 6. 1-Bit ADC Definition of Terms

Table 8. 8-bit ADC (Temperature -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	6	-	bit
Integral non-linearity	-	0.5	1	LSB
Differential non-linearity	-	-	0.5	LSB
Power Dissipation (peak)		35	70	mW
Sample window	5	-	120	ns
Bandwidth	-	-	2	Msps
Supply Range (=AV_{DD})				
Z87L00	3.0	3.3	3.6	V
Z87000	4.5	5.0	5.5	V
Input voltage range		0-AV_{DD}		V
Conversion time	0.5	-	-	µs
Aperture delay	2	3	8.5	ns
Aperture uncertainty	-	-	1	ns
Input resistance	-	25	-	Kohm
Input capacitance	-	10	-	pF

Notes:
1. 8-bit ADC only tested for 6-bit resolution.

Table 9. 4-bit DAC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	4	-	bit
Integral non-linearity	-	0.25	0.5	LSB
Differential non-linearity	-	0.25	1	LSB
Settling time (1/2 LSB)	-	-	22.5	ns
Zero error at 25°C	-	1	2	mV
Conversion time (input change to output change)	14	19	76	ns
Power dissipation, 25 pF load	1.2 (70°c)	20 (40°c)	24.1 (-20°c)	mW
Power dissipation, 25 pF load, Stop mode	0.18 (70°c)	1.0 (40°c)	1.1 (-20°c)	mW
Conversion time (input change to output change)	14.5	19.1	75.8	ns
Rise time (full swing)	11	15	71	ns
Output slew rate	8	67	96	V/µs
Output voltage range	-	0.2 AV_{DD} to 0.6AV_{DD}	-	V
Supply Range (=AV_{DD})				
Z87L00	3.0	3.3	3.6	V
Z87000	4.5	5.0	5.5	V
Output load resistance		330		Ohm
Output load capacitance	-	25	-	pF

INPUT/OUTPUT PIN CHARACTERISTICS

All digital pins (all pins except V_{DD}, AV_{DD}, GND, AGND, V_{REF}, RX, TX, RSSI and PWLV) have an internal capacitance of 5 pF.

The RX analog input pin has an input capacitance of 10 pF.

The RSSI analog input pin has an input capacitance of 10 pF.

AC ELECTRICAL CHARACTERISTICS

Clocks, Reset and RF Interface

Table 10. Clocks, Reset and RF Interface

No.	Symbol	Parameter	Min	Max	Units
1	TpC	MCLK input clock period (1)	61	61	ns
2	TwC	MCLK input clock pulse width	20	40	ns
3	TrC, TfC	MCLK input clock rise/fall time		15	ns
4	TrCC, TfCC	CLKOUT output clock rise/fall time	2	6	ns
5	TrCO, TfCO	CODCLK output clock rise/fall time	2	6	ns
6	TwR	RESETB input low width	18		TpC
7	TrRF, TfRF	RF output controls rise/fall time (2)	2	6	ns

Notes:
1. MCLK is 16.384 MHz ± 25 ppm
2. RF Controls are RFTX, RFRX, RXON, RFEON, SYLE.

ADPCM Processor Interface

The Z87000 is a peripheral device for the ADPCM Processor. The interface from the Z87000 perspective is composed of an input address bus, a bidirectional data bus, strobe and read/write input control signals and a ready/wait output control signal.

READ CYCLES refer to data transfers from the Z87000 to the ADPCM Processor.

WRITE CYCLES refer to data transfers from the ADPCM Processor to the Z87000.

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Table 11. Read Cycles

Signal Name	Function	Direction
VXADD[2..0]	Address Bus	ADPCM Proc. to Z87000
VXDATA[7..0]	Data Bus	Bidirectional
VXSTRB	Strobe Control Signal	ADPCM Proc. to Z87000
VXRWB	Read/Write Control Signal	ADPCM Proc. to Z87000
VXRDYB	Ready Control Signal	Z87000 to ADPCM Proc.

Table 12. Write Cycles

No.	Symbol	Parameter	Min	Max	Units
8	TsAS	Address, Read/Write setup time before Strobe falls	10		ns
9	ThSA	Address, Read/Write hold time after Strobe rises	3		ns
10	TaDrS	Data read access time after Strobe falls		30 (1)	ns
11	ThDrS	Data read hold time after Strobe rises	8.5	40 (2)	ns
12	TwS	Strobe pulse width	20		
13	TsDwS	Data write setup time before Strobe rises	10		ns
14	ThDwS	Data write hold time after Strobe rises	3		ns
15	TaDrRY	Data read valid before Ready falls	22		ns
16	TdSRY	Strobe high after Ready falls	0		ns

Notes:
1. Requires wait state on ADPCM Processor read cycles
2. Requires no write cycle directly following read cycle on ADPCM Processor

AC TIMING DIAGRAMS

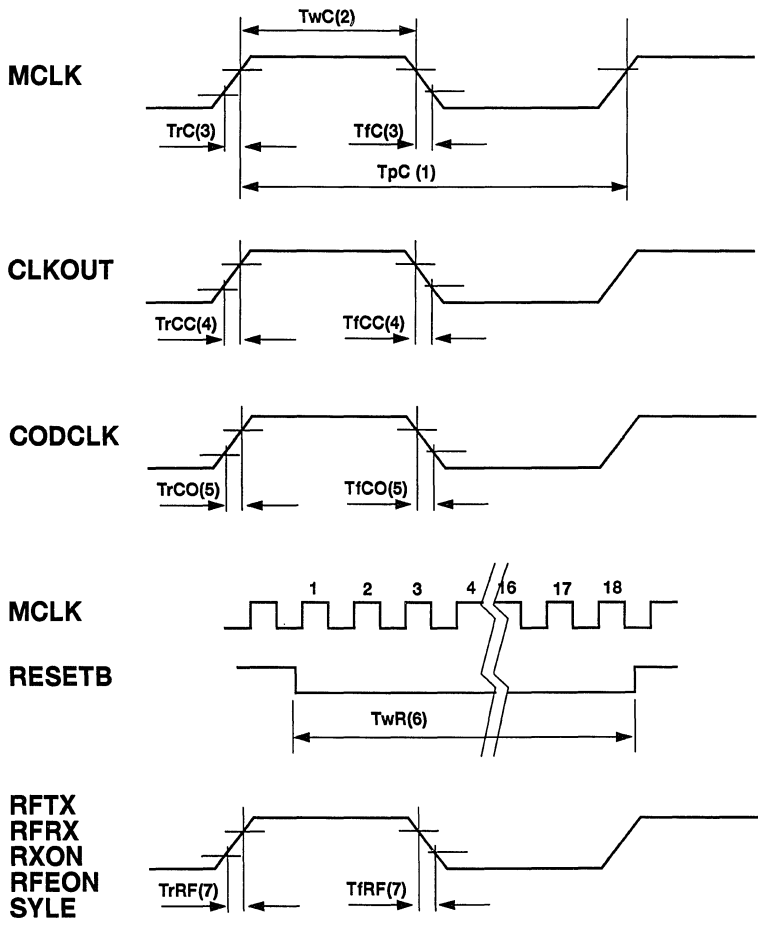
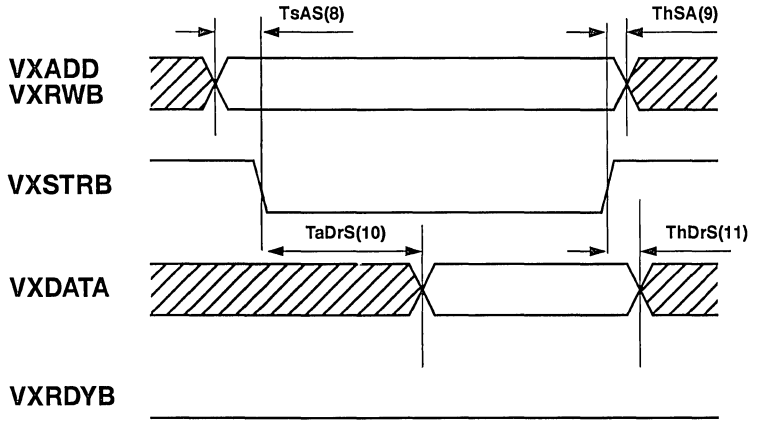
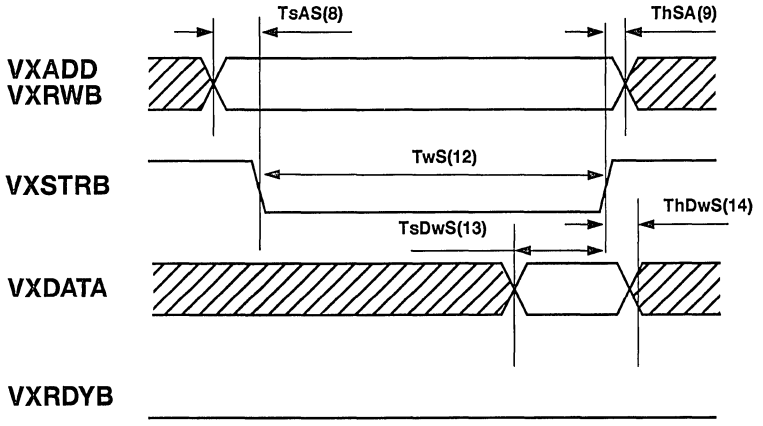


Figure 7. Transceiver Output Signal



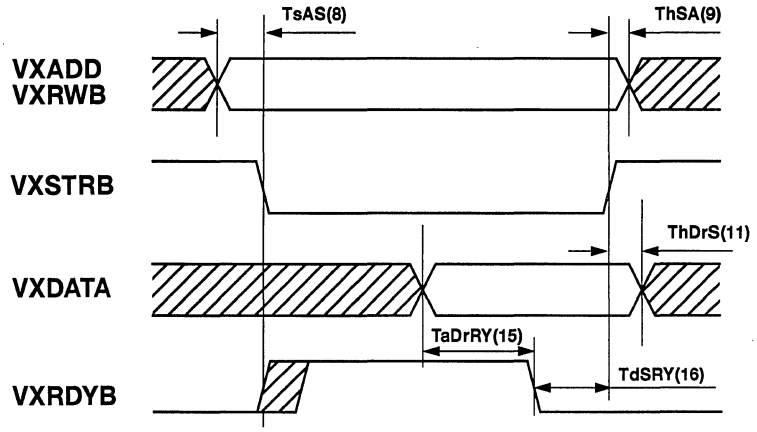
VXDATA Read Cycle



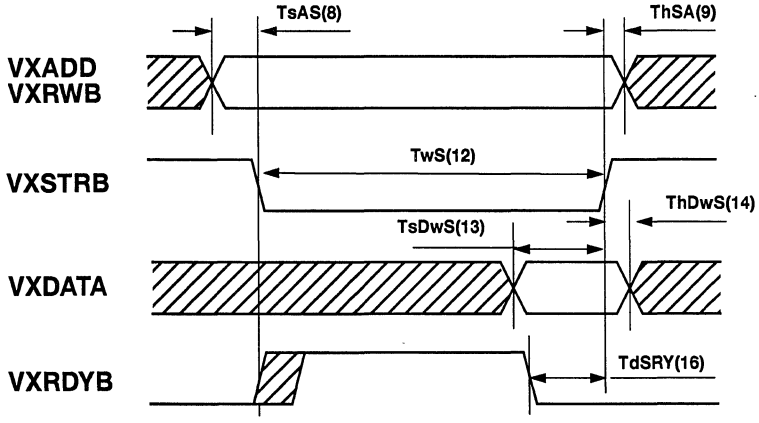
VXDATA Write Cycle

Figure 8. Read/Write Cycle Timings

AC TIMING DIAGRAMS (Continued)



VXDATA Read Cycle with Wait State



VXDATA Write Cycle with Wait State

Figure 9. Read/Write Cycle Timing with Wait State

PIN FUNCTIONS

V_{DD}. Digital power supply.

GND. Digital ground.

AV_{DD}. Analog power supply.

AGND. Analog ground.

V_{REF} (analog reference). This signal is the reference voltage used by the high speed analog comparator to sample the RX input signal.

RX (analog input). This is the RX IF receive signal from the RF module, input to the analog comparator and FSK demodulator. It is internally biased to the V_{REF} DC voltage. The IF signal from the RF module should be AC coupled to the RX pin.

TX (analog output). This is the IF transmit signal to the RF module, output from the FSK modulator and transmit 4-bit D/A converter.

RXON (output; active high or low programmable). This pin reflects the programming of the demodulator turn-on time.

RFRX (output; active high or low programmable). Control for the receive switch on the RF module. Active during receive periods.

RFTX (output; active high or low programmable). Control for the transmit switch on the RF module. Active during transmit periods.

RFEON (output; active high or low programmable). On/off control for the RF module. Active (on) during wake periods. Inactive (off) during sleep periods on the handset.

RSSI (analog input). Receive signal strength indicator from RF module, input to the RSSI 8-bit ADC.

PWLV (analog output). Power level control for RF module, output from the transmit power 4-bit DAC.

SYLE (output). RF synthesizer load enable: latches new frequency hopping control word of external RF synthesizer. Programmable polarity.

ANT[1..0] (output). Control for optional antenna diversity on the RF module.

MCLK (input). Master clock input.

CLKOUT (output). Clock output for external ADPCM processor.

CODCLK (output). Clock output for external voice CODEC.

/RESETB (input, active low). Reset signal.

VXADD[2..0] (input). Address bus controlled by external ADPCM processor. The Z87000 acts as peripheral of the Z87010 ADPCM processor.

VXDATA[7..0](input/output). Read/write data bus controlled by external Z87010 ADPCM processor.

VXSTRB (input). Data strobe signal for the VXDATA bus, controlled by external Z87010.

VXRWB (input). Read/write control for the VXDATA bus, controlled by external Z87010.

VXRDYB (output, active low). Ready control for the VXDATA bus. This signal is driven high (de-asserted) by the Z87000 to insert wait states in the Z87010 ADPCM processor accesses.

TEST (input, active high). Main test mode control. Must be set to GND.

HBSW (input with internal pull-up). Control for handset/base configuration. Must be driven high or not connected for handset, low for base.

P0[15..0] (input/output). General-purpose I/O port. Direction is bit-programmable. Pins P0[3..0],when configured in input mode, can also be individually programmed as wake-up pins for the Z87000 (wake-up active low; signal internally debounced and synchronized to the bit clock).

P0 0	WAKEUP0
P0 1	WAKEUP1
P0 2	WAKEUP2
P0 3	WAKEUP3

P1[15..0] (input/output).General-purpose I/O port. Direction is bit-programmable. Pins P114 and P115, when configured in input mode, also behave as individually maskable interrupt pins for the core processor (positive edge-triggered).

P1 14	INT0
P1 15	INT2

FUNCTIONAL DESCRIPTION

The functional partitioning of the Z87000 is shown in Figure 2. The chip consists of a receiver, a transmitter, and several additional functional blocks.

The receiver consists of the following blocks:

- Receive 1-bit ADC
- Demodulator, including:
  - IF Downconverter
  - AFC (Automatic Frequency Control)
  - Limiter-Discriminator
  - Matched Filter
  - Bit Synchronizer
  - Bit Inversion
  - Frame Synchronizer (unique word detector)
  - SNR Detector
- Receive Frame Timing Counter
- Receive Buffer and Voice Interface

The Transmitter Consists of the Following Blocks:

- Transmit Buffer and Voice Interface
- Transmit Frame Timing Counter (used on base station only)
- Modulator, including:
  - NCO
  - Bit Inversion
- Transmit 4-Bit DAC

In Addition, there are the following Shared Blocks.

- Event Trigger Block, Controlling:
  - Transmit/Receive Switch
  - Power On/Off Switches (Modulator, Demodulator, RF Module)
  - Antenna Switch Control (used on Base Station only for Antenna Diversity)
- 4-Bit DAC for Setting Transmit Power Level
- 8-Bit ADC for Sampling the Received Signal Strength Indicator (RSSI)
- DSP Core Processor
- Two 16-Bit General-Purpose I/O Ports
- Z87010 ADPCM Processor Interface

Basic Operation

The transmitter and receiver operate in time-division duplex (TDD): handset and base station transmit and receive alternately. The TDD duty cycle lasts 4 ms and consists of the following events:

- At the beginning of the cycle, the frequency is changed (hopping)
- The base station transmits a frame of 144 bits while the handset receives
- The handset then transmits a frame of 148 bits while the base receives.

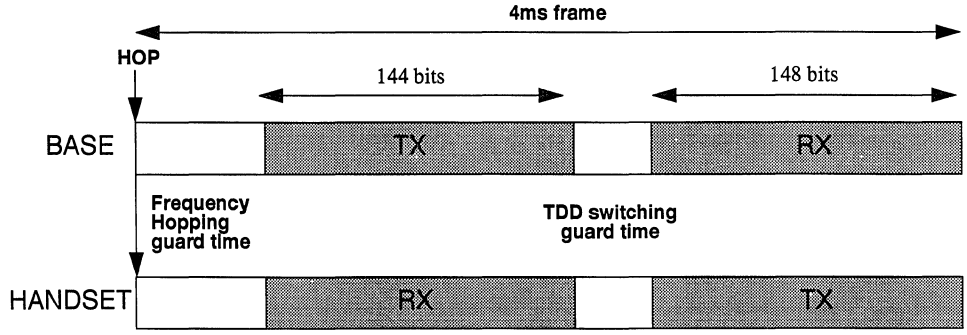


Figure 1. Basic Time Duplex Timing

Receive 1-Bit ADC

The incoming receive signal at the RX analog input pin is sampled by a 1-bit analog-to-digital converter at 8.192 MHz.

The receive signal is FSK-modulated (Frequency Shift Keying) with a carrier frequency of 10.7 MHz (Intermediate Frequency, or IF). The instantaneous frequency varies between 10.7 MHz plus or minus 32.58 kHz. Since the data rate is 93.09 kbps, there are 88 samples per data bit. This oversampled data is further processed by the demodulator to retrieve the baseband information.

The 1-bit converter is implemented with a fast comparator, which determines whether the RX signal is larger or smaller than a reference signal (VREF). The Z87000 internally generates the DC level of both VREF and RX input pins. The received signal at 10.7 MHz should thus be AC coupled to the RX pin via a coupling capacitor. To ensure accurate operation of the converter, the user should also attach to the VREF pin a network whose impedance matches the DC impedance seen by the RX pin.

Demodulator

The demodulator includes a two-stage IF downconverter that brings the sampled receive signal to baseband.

The narrow-band 10.7 MHz receive signal, sampled at 8.192 MHz by the 1-bit ADC, provides a 2.508 MHz useful image. The first local oscillator used to downconvert this IF signal is obtained from a Numerically Controlled Oscillator (NCO) internal to the Z87000, at the nominal frequency of 460 kHz. The resulting signal is thus at 2.048 MHz (= 2.508 MHz - 460 kHz). A second downconversion by a 2.048 MHz signal brings the receive signal to baseband.

The exact frequency of the 460 kHz NCO is slightly adjusted by the Automatic Frequency Control (AFC) loop for exact downconversion of the end signal to the zero frequency. The AFC circuit detects any DC component in the output of the limiter-discriminator (see below) when receiving a known sequence of data (preamble). This DC component is called the "frequency bias". The bias estimate out of the AFC can be read by the DSP processor on every frame and subsequently filtered. The processor then adds or subtract this filtered bias to/from the NCO control word to correct the NCO frequency output.

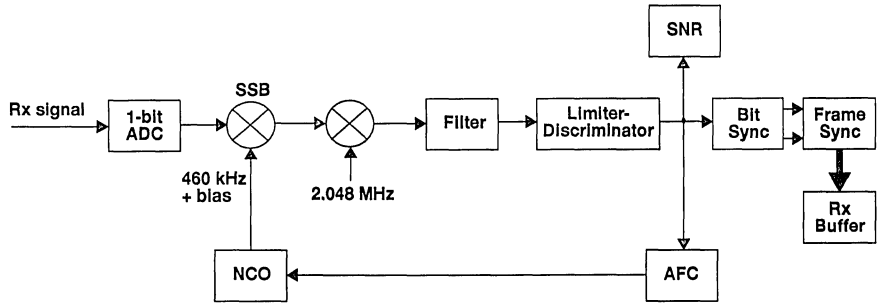


Figure 2. Demodulator Block Diagram

The main element of the demodulator is its limiter-discriminator. The limiter-discriminator detects the frequency variations (ideally up to ± 32.58 kHz) and converts them to "0" or "1" information bits. First, the data is processed through low-pass filters to eliminate high frequency spurious components introduced by the 1-bit ADC. The resulting signal is then differentiated and fed to a matched filter. In the matched filter, an integrate-and-dump operation is performed to extract the digital information from its background noise.

The symbol clock is provided by the bit synchronizer. The bit synchronizer circuit detects 0-to-1 and 1-to-0 transitions in the incoming data stream in order to synchronize a digital phase-lock loop (DPLL). The PLL output is the recovered bit clock, used to time the receiver on the base station, and both receiver and transmitter on the handset.

To ensure enough transitions in the voice data stream, a pseudo-random bit inversion operation is performed on the outgoing voice data. The inversion is then reversed on the demodulated data.

FUNCTIONAL DESCRIPTION (Continued)

Since the data is packed in frames sent alternately from base and handset every 4 ms (TDD), additional synchronization means are necessary. This is realized in a frame synchronizer, based on detection of a "unique word" following the preamble.

The receiver also features a signal-to-noise ratio detector, which allows the DSP software to detect noisy channels and eliminate them from the frequency hopping cycle. The SNR information is also used by the Z87000 software as a measure the current range between handset and base station. This information allows the adaptive power control algorithm to provide sufficient output power to the RF transmitter.

Receive Frame Counter

The receive frame counter is responsible to keep track of time within the frame. It is initialized by the frame synchronizer logic on detection of the unique word. It is then clocked by the recovered bit clock from the bit synchronizer.

On the base station, the receive frame counter is used as time base for the receiver. On the handset, it is used as time base for both receiver and transmitter.

Receive Rate Buffer and Voice Interface

The voice signal is generated at the fixed rate of 32 kips by the Z87010 processor, and transmitted/received in bursts of 93.09 kips across the air. Data buffers in the transmitter and receiver are thus necessary to absorb the rate differences over time. These buffers are called "rate buffers". They can store up to 144 data bits and are organized as an array of 36 4-bit nibbles.

The receive rate buffer stores the received data from the demodulator. Incoming bits are arranged in 4-bit nibbles and transferred to successive locations of the rate buffer. When the last location is reached, transfers resume from the beginning (circular buffer). The system design guarantees that no buffer overrun nor enduring can occur.

The receive rate buffer can be read by the DSP core processor of the Z87000 or by the Z87010 chip. On the Z87000 side, the buffer can be read as a random-access memory: the processor writes the nibble address in an address register and reads the 4-bit data from a data register. On the Z87010 side, a voice processor interface logic handles the addressing to automatically present the successive voice nibbles to the Z87010 in the order they were received.

Transmit Rate Buffer and Voice Interface

The transmit rate buffer stores the data to be modulated. The data is sourced from the Z87010 or the Z87000 core processor. As for the receive rate buffer, the Z87010 sees a unique pipe to write to, while the Z87000 DSP core accesses the rate buffer as random-access memory. The modulator reads from the rate buffer as from a circular buffer.

Transmit Frame Timing Counter

On the handset, transmission does not start until the receiver has synchronized itself to the signal received from the base station. The transmission timing is based on the recovered clock. No additional counter is necessary.

On the base station, the situation is different. Transmission timing is based on a local clock, while the reception's timing is based on the clock recovered from the incoming received signal. Two counters, respectively clocked by local and recovered clocks, are necessary to track the transmit and receive signals.

Note that the receive clock on the base station tracks the handset's transmit clock, which is also the handset's receive clock and tracks the transmit clock of the base station. As a result, receive and transmit clocks of the base station have exactly the same frequency; only their phases differ.

Modulator

The modulator consists of a numerically controlled oscillator (NCO) which generates an FSK (Frequency Shift Keying) signal at the carrier frequency of 2.508 MHz. The carrier frequency is shifted plus or minus 32.58 kHz for a "1" or a "0" data bit. To facilitate conformance to FCC regulations, the transitions from "1" to "0" or vice-versa are smoothed in order to decrease the amplitude of the side lobes of the transmit signal. In practice, the jump from one frequency to the next is performed in several smaller steps.

The carrier frequency is adjustable by the DSP core processor in order to provide additional frequency adjustment between base and handset. This is provided in case of a frequency offset too large for possible correction by the AFC.

The modulator also includes bit inversion logic as discussed in the receiver section.

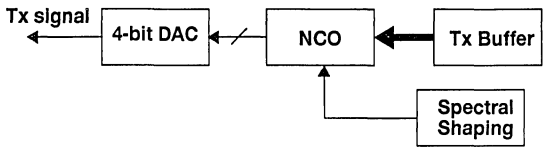


Figure 3. Modulator Block Diagram

Transmit 4-Bit DAC

The transmit DAC clocks one new NCO value out of the Z87000 every 8.192 MHz period. Only the 10.7 MHz alias frequency component of the transmit signal (2.508 + 8.192 MHz image) is filtered, amplified and upconverted to the 900 MHz ISM band by the companion RF module.

Event Trigger Block

The event trigger block is responsible for scheduling the different events happening at the bit and frame levels. The event trigger block receives input from the frame counters as well as the register interface of the DSP core processor.

The event trigger schedules the following events:

- Start of the 4 ms frame: a synthesizer load enable pulse is issued on the SYLE pin
- Power-up of the modulator section and transmission of the frame on handset and base station
- Use of the bit inversion as function of mode
- Power-up of the demodulator section and reception of the frame on handset and base station
- Control of RFTX and RFRX output pins, to be used as TDD control signals switching the antenna as well as transmitter and receiver chains on the RF module
- Control of RFEON pin, to be used as general on/off switch on the RF module
- Control of the Z87000 sleep mode

4-Bit DAC for Setting Transmit Power Level

In order to save battery life, the Z87000 only transmits the amount of RF power needed to reach the remote receiver with a sufficient SNR margin. The on-board transmit power 4-bit DAC provides 4 different voltage levels to the power amplifier in the RF module for that purpose. This DAC is directly controlled by the Z87000 software through an output register.

8-Bit ADC for Sampling the Received Signal Strength Indicator (RSSI)

RSSI information is typically generated from the last stage of the RF receiver. The RSSI is sampled once per frame by the 8-bit ADC and used by the Z87000 software to compute the necessary Transmit Power Level voltages.

DSP Core Processor

A DSP core processor constitutes the heart of the Z87000. The DSP runs the application software which performs the following functions:

- Register initialization
- Implementation of high-level phone features; control of phone user interface (keypad, Led, etc.)
- Control of the Z87010 ADPCM Processor
- Control of the phone line interface
- Ring detection by DSP processing
- Communication protocol between handset and base station supporting voice and signalling channels
- Control of the RF synthesizer and adaptive frequency hopping algorithm
- Control of the RF power and adaptive power algorithm
- Control of the demodulator (bit synchronizer loop filter, AFC bias estimate filtering)
- Control of the modulator (carrier frequency) and adaptive frequency alignment
- Signalling between base and handset to support above features

The DSP core is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction and multiply-accumulate of two 16-bit operands. Most instructions are executed in one clock cycle.

FUNCTIONAL DESCRIPTION (Continued)

The DSP core is operated at the internal speed of 8.192 MHz. It has an internal RAM memory of 512 16-bit words divided in two banks. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six-level stack. One interrupt is used by the transceiver, while the two remaining vectors are mapped into port P1. In the phone system, one of these interrupts is customarily reserved for the Z87010 ADPCM Processor. The other interrupt can be used for custom purposes.

The Z87000 has a (12K+128) x 16-bit internal ROM including 4 words for interrupt and reset vectors. The ROM is mapped at addresses 0000h to 2FFFh, 3F80h to 3FFFh, as shown in Figure 13.

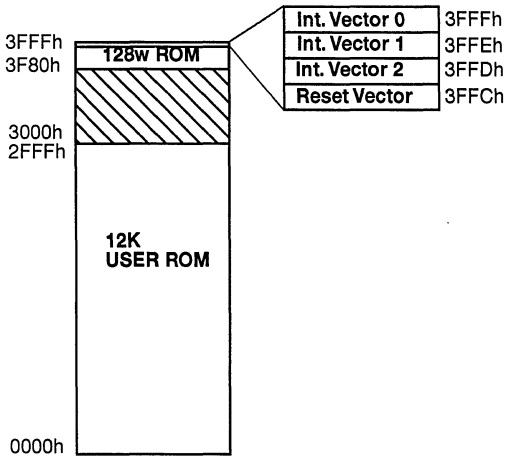


Figure 4. ROM Mapping

Two 16-Bit General-Purpose I/O Ports

Two 16-bit general-purpose I/O ports are directly accessible by the DSP core. These input and output pins are typically used for:

- Implementation of the phone's user interface (keypad, LED, optional display, etc.)
- Control of phone line interface (on/off hook, ring detect)
- Control of battery charging and detection of low battery conditions
- Implementation of additional features for customizing of the phone

Z87010 Interface

In addition to providing clock signals to the Z87010 processor, the Z87000 interfaces to the Z87010 through two different paths:

- A command/status interface
- A data interface

The command/status interface consists of two dual-port registers accessible by both Z87000 and Z87010 DSP core processors. On the Z87000 side, the registers are mapped into the DSP core processor's register interface. To allow access by the Z87010, the internal command/status registers can also be decoded on the pinto of the Z87000. Arbitration logic resolves access contentions.

The data interface allows the Z87010 processor direct access to the Z87000's receive and transmit rate buffers. The rate buffers are decoded on the pin to of the Z87000, and dedicated voice processor interface logic handles the addressing within the rate buffers.

The physical interface between Z87000 and Z87010 consists of an 8-bit data bus, a 3-bit address bus and control signals, as summarized in the following:

VXDATA[7.0]	Data bus
VXADD[2.0]	Address bus
VXSTRB	Data Strobe
VXRWB	Read/Write Control
VXRDYB	Read Control

This bus is controlled by the Z87010. Although in the system the Z87010 is enslaved to the Z87000 master, at the physical level the Z87000 acts as a peripheral of the Z87010.

The mapping of the command status and data interfaces from the Z87010 side is given below.

Interface	Address (VXADD [2.0])	Read /Write	Data (VXDATA[7.0])
Transmit rate buffer	1	W	----3210
Receive rate buffer	1	R	----3210
Command	0	R	76543210
Status	0	W	76543210

OPERATION

Automatic Frequency Control Loop (Receiver) and Modulator

AFC Loop

The AFC loop consists of a bias estimator block, which determines frequency offsets in the incoming signal, an adder, to add this bias to the 460 kHz frequency control word driving the NCO, and various interface points to the DSP core processor. In particular, the DSP can read the bias estimate data and substitute its own calculated bias value to the NCO.

The bias estimator accumulates the discriminator output values (image of instantaneous frequency) that exceed a programmable threshold (BIAS_THRESHOLD). The processor can freeze the bias calculation any time by resetting the BIAS_ENABLE control bit.

The accumulated bias, available in BIAS_ERROR_DATA, can be used directly to correct the NCO frequency. Alternately, the estimated bias can be read by the DSP, further processed, and written to the CORE_BIAS_DATA field. The DSP controls which value is used by setting the USE_CORE_BIAS field. The selected value is added to the 460 kHz signal which downconverts the receive IF signal.

The CORE_BIAS_DATA and BIAS_ERROR_DATA are two's complement numbers in units of 125 Hz.

In addition to correcting the difference in clock frequencies on the receiver using the AFC loop, a Z87000-base system can also modify the frequency of the remote transmit IF signals. The software has access to this frequency through the MOD_FREQ register fields.

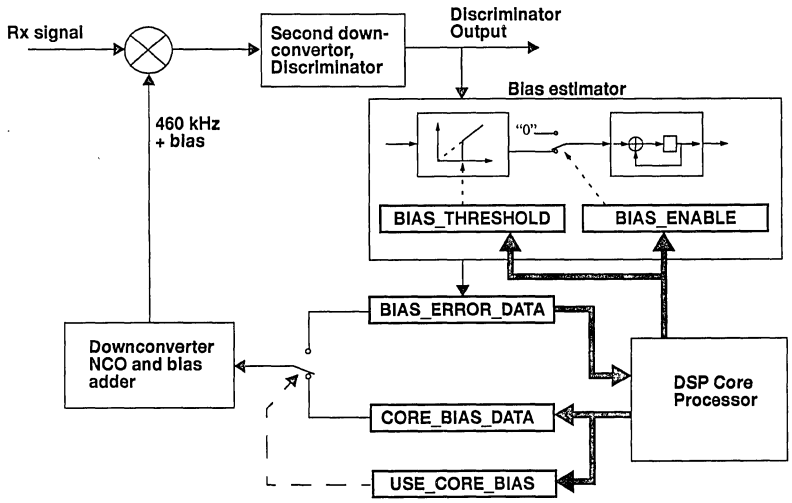


Figure 5. AFC Loop and Processor Control

OPERATION (Continued)

Modulator Control

The MOD_FREQ fields specify the carrier center frequency (should be programmed to 2.508 MHz) and deviation for the FSK signal (should be programmed to ± 32.58 kHz). In addition, wave shaping is performed on bit transitions, in order to satisfy FCC regulations. Up to four different intermediate deviation values are programmable for each of the two FSK states. The MOD_FREQ fields are programmable in units of 62.5 Hz.

Table 1. AFC and Modulator Control Fields

Field	Register	Bank	EXT
BIAS_THRESHOLD	CONFIG1	3	EXT0
BIAS_ENABLE	SSPSTATE	3	EXT2
BIAS_ERROR_DATA	BIAS_ERROR	2	EXT2
CORE_BIAS_DATA	CORE_BIAS	2	EXT4

Bit Synchronizer

The bit synchronizer circuit is an implementation of the Data-Transition-Tracking Loop (DTTL), best described in "Telecommunications Systems Engineering", by W. Lindsey and M. Simon (Dover 1973; oh. 9 p. 442). Its operation is summarized in the following block diagram.

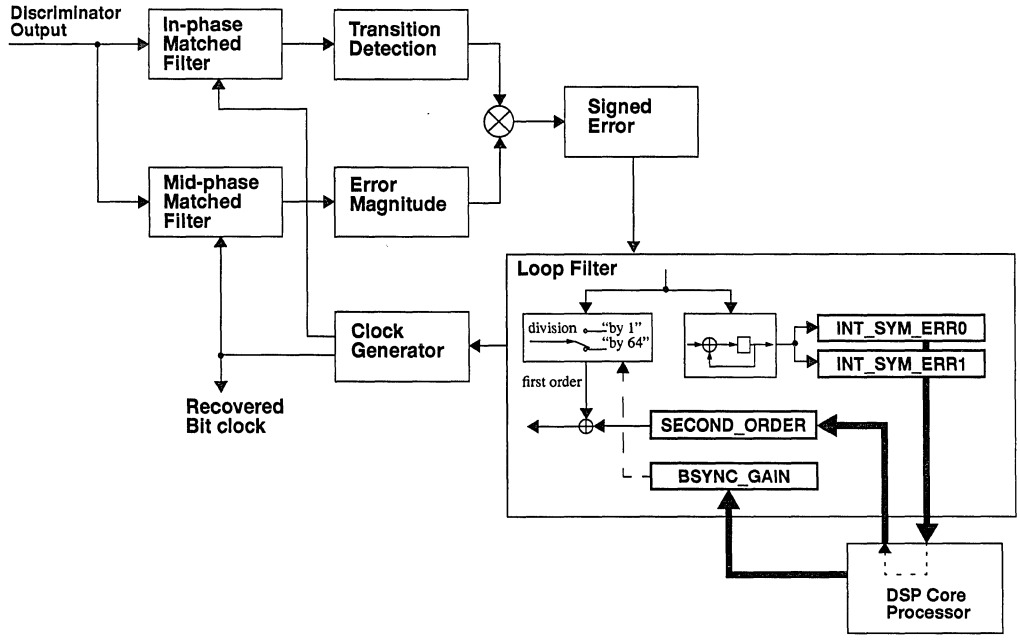


Figure 6. Bit Synchronizer Loop and Processor Control

The loop filter is controlled by the DSP core processor. The DSP core can implement a first order loop by setting the SECOND_ORDER field to zero. Typically, the BSYNC_GAIN would then be set to "divide-by-1" operation to provide a wide closed loop bandwidth and thus a quick acquisition of the bit clock. When the bit clock is in phase with the input data, the loop bandwidth can be narrowed to maintain tracking of the receive clock with minimum impact from signal noise. To reduce the loop bandwidth, the BSYNC_GAIN can be set to "divide-by-64" the first order gain, while the integrated tracking error (available to the DSP in fields INT_SYM_ERR0 and INT_SYM_ERR1) can be used by the DSP software to adjust the SECOND_ORDER term.

The bit synchronizer relies on transitions in the received bit stream to operate. The bit inversion logic guarantees enough transitions for all transferred data.

At the handset, the bit synchronizer must track both frequency and phase of the receive signal's data clock. At the base, only the phase must be tracked. The frequency is inherently correct since the base is the source of the system's data clock.

Table 2. Bit Synchronizer Control Fields

Field	Register	Bank	EXT
BYSNC_GAIN	SSPSTATE	3	EXT2
INT_SYM_ERR1	BIT_SYNC	1	EXT2
INT_SYM_ERR0	INT_SYM-ERR0	0	EXT6
SECOND_ORDER	BIT_SYNC	1	EXT2

Frame Counters

The handset only has one frame counter, which times all receive and transmit events. The base station has distinct transmit and receive frame counters. When used in this document without any explicit reference to either base or handset, the terms "receive frame counter" and "transmit frame counter" refer to both sides. For the handset, both terms refer to the same unique counter.

The frame counters are clocked at the bit rate, or 93.09 kHz (2.048 MHz/22). Each count lasts one bit = 1000/93.09 = 10.74 µs.

Each frame lasts 4 ms, which corresponds to (372 + 8/22) bits; the frame counters count from 0 to 371, with the last count lasting a bad longer than the other ones; at the end of count 371, the counters wrap around to 0.

The "hop" command pulse is asserted to pin SYLE during count "0" of the frame counter (transmit frame counter on the base station).

Frame Synchronizer, Timings and RF Interface

The frame synchronizer tracks the received frames and resets the receive frame counter. The synchronization is performed by recognizing certain data patterns present in the receive bit stream: a comparison is done on the fly between the data pattern and the incoming bit stream; when the data match, the frame counter is reset.

Two possible 16-bit data patterns are pre-programmed in the Z87000. One is named UW (Unique Word) and is used in acquisition mode for first-time synchronization to an incoming signal. UW can also be used to track an acquired signal. The second pattern is named SYNC_D and is used to track the received data frames while voice is being transferred. The transition from tracking UW to tracking SYNC_D is controlled by the DSP processor through the SYNC_SEARCH_WORD field.

UW Synchronization

When the Z87000 matches the UW, the receive frame counter is reset to the value of UW_LOCATION. This value is programmable by the DSP processor. On the handset, where the receive frame counter is used to derive all timings, UW_LOCATION actually defines the guard time between the frequency hop command and the beginning of data reception, which starts at FRAME_COUNTER = (UW_LOCATION - 84) as shown in the next figure.

On the base station, data reception starts when the receive frame counter equals (UW_LOCATION - 84), but this has less significance since the hop pulse is synchronized with the transmit frame counter and there is no fixed relationship between transmit and receive frame counters. On the base station, the UW_LOCATION should be set to 301.

OPERATION (Continued)

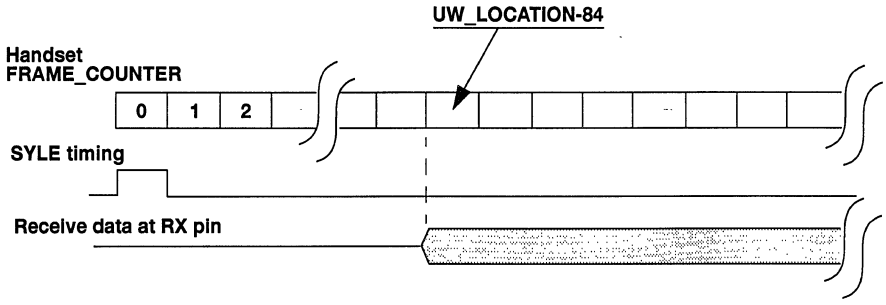


Figure 7. Frame Counter and UW_LOCATION on Handset

Two modes of search are programmable through the SYNC_SEARCH_MODE field: "full search" and "window search". The full search is used by the handset when first acquiring the signal from the base station. In full search, the handset is in receive mode and continuously looks for a match with the UW. When a match is found and the time reference established (UW_LOCATION is set), the DSP processor on the handset detects the synchronization (see below), switches to Time Division Duplex mode (TDD) and starts receiving and transmitting alternately. The search mode should also be switched to "window search" by the DSP software.

The window search mode only searches for a match in a certain time window centered around the expected match time. The window size is programmable by the DSP processor in the WINDOW_SIZE field. If the matching does not occur at the expected time, due to so-called "bit slips", the receive frame counter timing is adjusted. Note: although the bit synchronizer is meant to keep track of time and prevent bit slips when the phone is operating continuously in TDD mode, bit slips are still possible when the handset is in standby mode, and only receives once in a while (see description of sleep mode).

SYNC_D Synchronization

When the DSP processor switches the Z87000 operation to voice mode, the frame synchronization parameters should be modified by the DSP software to:

- SYNC_SEARCH_MODE = window search
- SYNC_SEARCH_WORD = SYNC_D pattern

In this mode, the receiver searches for the SYNC_D pattern in windows of the incoming data stream. The window size is determined by the WINDOW_SIZE field.

The transition to voice mode proceeds in two steps, through an intermediate mode. The mode is set by the DSP processor by programming the MULTIPLEX_SWITCH field. The three modes are:

- **SMUX: initial mode.** This mode allows acquisition, AFC operation, UW synchronization and signalling; ADPCM Processor access disabled; bit inversion disabled.
- **STMUX: intermediate mode.** This mode allows SYNC_D frame synchronization and signalling; ADPCM Processor access disabled; bit inversion enabled.
- **TMUX: voice mode.** This mode allows voice transmission, SYNC_D frame synchronization and signalling; ADPCM Processor access enabled; bit inversion enabled.

In order to detect synchronizations, the software has access to the SYNC_ACQ_IND status field. This field is set by the Z87000 matching hardware every time a match is detected within the right time window. The software must reset the "IND" bit by setting the SYNC_ACQ_CLEAR field.

In addition, the software can track the frame timing by reading the frame counter value, available in the FRAME_COUNTER field. On the base station, where two frame counters are in use, this field returns the value of the transmit frame counter.

Every time the frame counter wraps around to 0, a frame start indicator bit is set (FRAME_START_IND status field). The software must reset this "IND" bit by setting the FRAME_START_CLEAR field. If the FS_INT_ENABLE bit is set, frame starts also trigger interrupts to the DSP processor.

The following table summarizes the fields allowing control of frame synchronization and basic frame timing.

Table 3. Frame Synchronizer Control Fields

Field	Register	Bank	Ext
SYNC_SEARCH-MODE	SSPSTATE	3	EXT2
SYNC_SEARCH_WORD	SSPSTATE	3	EXT2
UW_LOCATION	RX_CONTROL	2	EXT1
WINDOW_SIZE	CONFIG1	3	EXT0
MULTIPLEX_SWITCH	SSPSTATE	3	EXT2
SYNC_ACQ_IND	SSPSTATUS	3	EXT3
SYNC_ACQ_CLEAR	SSPSTATE	3	EXT2
FRAME_COUNTER	SSPSTATUS	3	EXT3
FS_INT_ENABLE	CONTROL	1	EXT6
FRAME_START_IND	SSPSTATUS	3	EXT3
FRAME_START_CLEAR	SSPSTATE	3	EXT2
SYNC_SEARCH-MODE	SSPSTATE	3	EXT2

RF Interface

Several control fields are available in the Z87000 register set to control the timing and polarity of the RF module interface signals.

A first field, RFEON_POLARITY, controls the polarity of the RFEON pin. This pin should be used to control the power of the RF module. It is asserted by the Z87000 when the RF module is in use, and de-asserted in sleep mode. The sleep mode is used by the handset to save battery life when no phone call is in process (See "Sleep mode" on page 21).

The SYLE pin (Synthesizer Load Enable), which carries a "load enable" pulse that tells an external RF synthesizer to generate the next RF channel, is controlled by two fields. The HOP_ENABLE field is a global enable signal for the SYLE signals. The SYLE_POLARITY field defines the polarity of the SYLE pin. The system designer should ensure that the leading edge of the SYLE pulse triggers channel hopping.

In addition to the SYLE signal, the interface to the most RF synthesizers includes two more input lines, "data" and "clock", for serial programming of the data values defining the RF channel. In order to allow interfacing to various popular synthesizers, the Z87000 does not have dedicated clock and data lines with fixed timing. Instead, two general I/O pins from ports P0 and P1 can be controlled in software by the DSP core to realize any particular interface timing. This flexibility is made possible by the high speed, single-cycle architecture of the DSP core.

The transmitter control includes a global enable signal for all transmit functions: TX_ENABLE. The transmission start is controlled by the MOD_PWR_ON field. On the base station, the value programmed in MOD_PWR_ON is referenced to the transmit frame counter.

Two additional fields, RFTX_PWR_ON and RFTX_PWR_OFF, define the duty cycle of the RFTX output pin. On the base station, these fields are referenced to the transmit frame counter. The RFTX_POLARITY bit defines the polarity of the RFTX pin. This pin can be used to control the transmit section and power amplifier of the external RF module.

On the receive side, two fields define the internal timing of the receiver. The start of reception is controlled by the DEMOD_PWR_ON field. Stop of reception (and receiver power down) is controlled by the DEMOD_PWR_OFF field. On the base station, these fields are referenced to the receive frame counter. The RXON output pin follows the timing defined by the DEMOD_PWR_ON and OFF fields.

Two additional fields, RFRX_PWR_ON and RFRX_PWR_OFF, define the duty cycle of the RFRX output pin. On the base station, these fields are referenced to the TRANSMIT (!) frame counter. The RFRX_POLARITY bit defines the polarity of the RFRX and RXON pins. The RFRX pin can be used to control the receive section of the external RF module.

OPERATION (Continued)

The various timing control registers reviewed in this paragraph should be programmed differently for handset and base station. If the same ROM code is used on base and handset, the software can determine which station it runs on by reading the HAND_BASE_SEL bit, which reflects the state of the HBSW pin.

The following figure and table summarize the RF interface control fields.

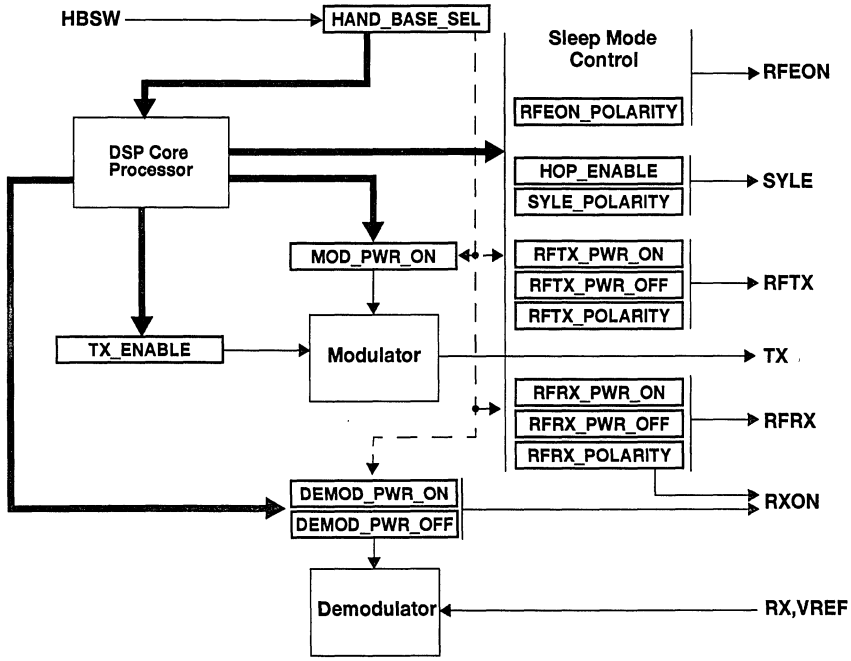


Figure 8. RF interface Control

Table 4. Timing and RF Interface Control Fields

Field	Register	Bank	Ext
RFEON_POLARITY	RX_PWR_CTRL	2	EXT6
HOP_ENABLE	SSPSTATE	3	EXT2
SYLE_POLARITY	CONFIG1	3	EXT0
TX_ENABLE	SSPSTATE	3	EXT2
MOD_PWR_ON	MOD_PWR_CTRL	2	EXT5
RFRX_PWR_ON/OFF	RFRX_PWR_CTRL	0	EXT7
DEMOD_PWR_ON/OFF	DEMOD_PWR_CTRL	2	EXT6
RFRX_POLARITY	RFRX_PWR_CTRL	0	EXT7
RFTX_PWR_ON/OFF	RFTX_PWR_CTRL	2	EXT7
RFTX_POLARITY	RFTX_PWR_CTRL	2	EXT7
HAND_BASE_SEL	SSP_STATUS	3	EXT3

Sleep Mode

To save the phone's battery life on the handset, the Z87000 can be operated in sleep mode while the phone is not in use. The sleep mode is entered by software command. The sleep mode first needs to be enabled by setting the SLEEP_WAKE field. Then a GO_TO_SLEEP command puts the processor to sleep by temporarily stopping its clock. The sleep period can be set to last between 4 ms and 1.02 s by programming the SLEEP_PERIOD field. In sleep mode, the RFEON pin is de-asserted.

The processor comes out of sleep mode in one of two ways. Either the sleep counter counts down to zero, or one of the enabled pins from port P0 is asserted prior to normal expiration of the counter. Four port pins (P0[0..4]) can be individually enabled to provide the wake-up function by setting the appropriate bits in P0_WAKE_ENABLE. Typically, these port pins are connected to the telephone keypad.

When the processor core wakes up, the software needs to know how much time it was actually asleep, in order to restore synchronization to the base station's hopping sequence. For that purpose, the current value of the sleep counter is available to the processor in SLEEP_REMAINING. A value of zero indicates normal expiration of the sleep counter.

In order to guarantee a good operation of the wake-up pins, the wake-up signals are hardware-denounced by the Z87000. Furthermore, these signals are internally synchronized to the bit clock. This ensures that the processor has enough time (one bit time = 10.74 ms) to read a stable value of the remaining sleep time and synchronize correctly to the base station's hopping sequence.

Table 5. Sleep Mode Control Fields

Field	Register	Bank	Ext
SLEEP_EAKE	SSPSTATE	3	EXT2
GO_TO_SLEEP	SSPSTATE	3	EXT2
SLEEP_PERIOD	CONFIG2	3	EXT1
SLEEP_REMAINING	CONFIG2	3	EXT1
P0_WAKEUP_ENABLE	CONTROL	1	EXT6

ADPCM Processor Interface and Rate Buffers

The interface to the ADPCM Processor (Z87010) consists of clock control, command/status interface and data interface. The data interface gives the ADPCM Processor access to the rate buffers.

Clock Interface

The Z87000 generates the Z87010 clock at 16.384 or 8.192 MHz, as set in VP_CLOCK. In addition, the clock can be stopped and restarted with the VP_STOP_CLOCK field in order to reduce power consumption (Note: a software handshaking between Z87000 and Z87010 is necessary before stopping and after restarting the clock).

In addition to providing the Z87010 main clock, the Z87000 generates a CODCLK signal which will be used by the codec and by the Z87010 to synchronize its data transfers with the Z87000. On the base station, the CODCLK is simply obtained by dividing the 16.384 MHz input clock.

On the handset, the CODCLK is synchronized to the base station's CODCLK signal through the receive bit sync logic. This ensures that production and consumption of voice data is happening at identical rates on handset and base, eliminating buffer overrun and underrun situations.

Command/Status Interface

The Z87000 sends commands to the Z87010 through the VP_COMMAND write-only field. It reads the Z87010 status in the VP_STATUS read-only field. Both fields are located at the same address in the Z87000 register interface. A communication protocol should be established in software to ensure correct reception of all commands. Dedicated hardware ensures data integrity when both Z87000 and Z87010 simultaneously access the same register.

Table 6. ADPCM Processor Control Fields

Field	Register	Bank	Ext
VP_CLOCK	CONFIG1	3	EXT0
VP_STOP_CLCOCKS	SSPSTATE	3	EXT2
VP_COMMAND	VP_INOUT	2	EXT0
VP_STATUS	VP_INOUT	2	EXT0

Data Interface and Rate Buffers

The digitized voice data is communicated between the Z87000 and Z87010 through the rate buffers and ADPCM Processor data interface. The transmit and receive rate buffers each contain 36 4-bit nibbles.

To write to the transmit rate buffer, the Z87000 core processor must first set the nibble address in the TX_BUF_ADDR register field, then write the nibble data through TX_BUF_DATA. If the TX_AUTO_INCREMENT bit is set, the address is automatically incriminated (modulo 51 = the number of nibbles in rate buffer + 15 additional data words accessible through TX_BUF_DATA; for more information, see Register Description) after each data write. This allows the DSP core to write successive nibbles without resetting the address each time.

OPERATION (Continued)

The operation of the receive rate buffer is identical. The Z87000 core processor must set the nibble address in RX_BUF_ADDR, then read the nibble from RX_BUF_DATA. If the RX_AUTO_INCREMENT bit is set, the read address is automatically incriminated (modulo 36 = number of nibbles in rate buffer) after each data read. This allows the DSP core to read successive nibbles without resetting the address each time.

Through its register interface, the Z87000 also controls which rate buffer addresses the Z87010 ADPCM Processor can access. The nibble addresses are contained in the TX_BUF_VP_ADDR and RX_BUF_VP_ADDR register fields. After the Z87010 writes or reads a nibble to or from transmit or receive rate buffer, the corresponding "VP_ADDR" is automatically incriminated (modulo 36) to the next accessible address. The locations of accessible addresses are individually controlled by the Z87000 in the three TX_RX_NIBBLE_MARKER register fields. A marker bit equal to "1" enables the Z87010 to access the corresponding address; a bit equal to "0" causes the Z87010's read or write access to skip to the next nibble that has a marker bit equal to "1".

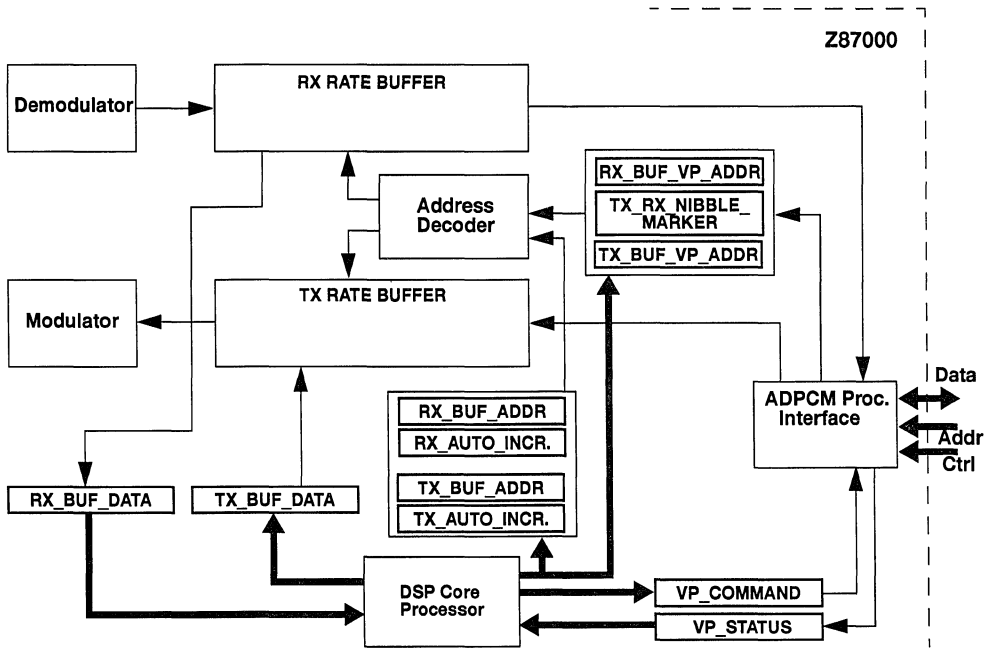


Figure 9. Rate Buffers Access and ADPCM Processor Interface

Table 7. Data and Control Access to Rate Buffers

Field	Register	Bank	Next
RX_AUTO_INCREMENT	RATE_BUF_ADDR	1	EXT0
RX_BUF_ADDR	RATE_BUF_ADDR	1	EXT0
TX_AUTO_INCREMENT	RATE_BUF_ADDR	1	EXT0
TX_BUF_ADDR	RATE_BUF_ADDR	1	EXT0
RX_BUF_DATA	RATE_BUF_DATA	1	EXT0
TX_BUF_DATA	RATE_BUF_ADDR	1	EXT1
TX_BUF_DATA	RATE_BUF_DATA	1	EXT1
RX_BUF_VP_ADDR	RATE_BUF_DATA	1	EXT1
TX_BUF_VP_ADDR	RATE_BUF_DATA	1	EXT1
TX_RX_NIBBLE_MARKER	RATE_BUF_DATA	1	EXT1

Additional Features

Power Control

The Z87000 features several means of measuring and controlling power levels. One input pin (RSSI) connects an external "receive signal strength indicator" to a half flash 8-bit ADC in the Z87000. This ADC is sampled once per frame during the receive portion of the TDD cycle. The RSSI value can be accessed in software in the RSSI_DATA register field. With external multiplexing, the 8-bit ADC can be used for additional purposes.

The RSSI data is used by the software to implement adaptive power control. In order to determine whether the RSSI information is made of signal or noise, the Z87000 includes logic to measure the signal-to-noise ratio (SNR) of the receive signal. This SNR value is available at the end of every frame in the SNR_ESTIMATE register field. It is also used by the adaptive frequency hopping algorithm to determine and avoid the noisy channels.

Finally, a 4-bit DAC (resistive ladder) is provided to control RF power output level. The DAC is under software control through register field TX_PWR_DAC_DATA.

Table 8. Power Control

Field	Register	Bank	Ext
RSSI_DATA	RSSI	2	EXT3
SNR_ESTIMATE	RX_CONTROL	2	EXT1
TX_PWR_DAC_DATA	CONTROL	1	EXT6
RSSI_DATA	RSSI	2	EXT3
SNR_ESTIMATE	RX_CONTROL	2	EXT3

General-Purpose I/O Ports

The Z87000 includes two general-purpose input/output ports, P0 and P1, of 16 bit each. The direction of each bit is independently programmable by setting the register fields DIRECTION0 and DIRECTION1. Then, the software can access the input and output values by accessing DATA0 and DATA1.

Two pins of port P1 (pins 14 and 15), when configured in input mode, also behave as interrupt pins for the core processor. The software can enable or disable each interrupt by setting the INTERRUPT_0_ENABLE and INTERRUPT_2_ENABLE fields. The interrupts are positive edge-triggered.

Pin Number	Interrupt Number	DSP Interrupt Vector
P1 14	INT0	3FFFh
P1 15	INT2	3FFDh

Table 9. General-Purpose I/O Ports

Field	Register	Bank	Ext
DIRECTION0	GPI00DIR	3	EXT4
DATA0	GPI00DATA	3	EXT5
DIRECTION1	GPI0IDIR	3	EXT6
DATA1	GPI0IDATA	3	EXT7
INTERRUPT_0_ENABLE	CONTROL	1	EXT6
INTERRUPT_1_ENABLE	CONTROL	1	EXT6

Four pins of port P0 (pins 0 to 3), when configured in input mode, can also be individually programmed as wake-up pins for the Z87000 (See "Sleep mode" on page 21).

REGISTER DESCRIPTION

The Z87000 DSP core processor has four banks of eight registers mapped in the core processor's "external register" space, as summarized in the following table.

Table 10. Register Summary

BANK	ADDRESS	REGISTER	READ DESCRIPTION	WRITE DESCRIPTION	TABLE #
Bank 3	EXT0	CONFIG1		Clock Dividers, Use Core Bias, SYLE polarity, search window size, Bias Threshold	Table 25
	EXT1	CONFIG2	Remaining Sleep time	ANT0/1 control, Sleep Period	Table 26
	EXT2	SSPSTATE	Stop VP clock, Absent gain, Bias Enable, Tx Enable, Sync Search control, Hop Enable, Frame Start control, Multiplex control, Sleep mode control		Table 27
	EXT3	SSPSTATUS	Frame Counter, Handset/Base, Sync Search control, Frame Start control		Table 28
	EXT4	GPIO0DIR	General-Purpose I/O port 0 direction control		Table 29
	EXT5	GPIO0DATA	General-Purpose I/O port 0 data		Table 30
	EXT6	GPIO1DIR	General-Purpose I/O port 1 direction control		Table 31
	EXT7	GPIO1DATA	General-Purpose I/O port 1 data		Table 32
Bank 2	EXT0	VP_INOUT	ADPCM Processor Status	ADPCM Processor Command	Table 33
	EXT1	RX_CONTROL	SNR estimate	UW location	Table 34
	EXT2	BIAS_ERROR	FCW value		Table 35
	EXT3	RSSI	8-bit ADC data (RSSI)		Table 36
	EXT4	CORE_BIAS		Core Bias data	Table 37
	EXT5	MOD_PWR_CTRL		MOD_PWR control	Table 38
	EXT6	DEMOD_PWR_CTRL		RXON, RFEON pin control	Table 39
	EXT7	RFTX_PWR_CTRL		RFTX pin control	Table 40
Bank 1	EXT0	RATE_BUF_ADDR		Rate Buffer address	Table 41
	EXT1	RATE_BUF_DATA	Re Rate Buffer data	Tx Rate Buffer data, control data	Table 42
	EXT2	BIT_SYNC	Bit Sync monitoring	Bit Sync control	Table 43
	EXT3	RESERVED			Table 44
	EXT4	RESERVED			Table 44
	EXT5	RESERVED			Table 44
	EXT6	CONTROL	INT, WAKEUP pin control, 4-bit DAC data (PWLV)		Table 45
	EXT7	RESERVED			Table 46
Bank 0	EXT0	RESERVED			Table 47
	EXT1	RESERVED			Table 47
	EXT2	RESERVED			Table 47
	EXT3	RESERVED			Table 47
	EXT4	RESERVED			Table 47
	EXT5	RESERVED			Table 47
	EXT6	INT_SYM_ERR0	Bit Sync monitoring		Table 47
	EXT7	RFRX_PWR_CTRL		RFRX, RXON pin control	Table 49

The bank is selectable in software by writing to the core's status register (see Table 24). Once a bank is selected, each of the eight external registers (EXT0 through EXT7) can be accessed by a single-cycle software instruction.

Table 11. Bank Switching

Bank	Status Register	Bank Function
Bank 0	xxxx xxxx x00x xxxx b	Test point access, TDD switching control
Bank 1	xxxx xxxx x01x xxxx b	Rate buffer access, miscellaneous
Bank 2	xxxx xxxx x10x xxxx b	ADPCM processor interface, RF interface, etc.
Bank 3	xxxx xxxx x11x xxxx b	Configuration, status, general-purpose port data and direction

Bank 3 Registers

Table 12. Bank 3 Registers

Config 1 Field	Bank 3 Bit Position	EXT0 R/W	Data	Description
RESERVED	f---------------	R		Returns 0
		W		Must be set to 1
VP_CLOCK	-e--------------			Controls CLKOUT output pin (clock for ADPCM Processor). Returns 0
			0	CLOCKOUT=16.384 MHz
			1	CLOCKOUT = 8.192
USE_CORE_BIAS	--d------------			Controls which bias value is used by the downconverter's NCO as part of the automatic frequency control loop (AFC)
		R		Returns 0
		W	0*	Uses BIAS_ERROR_DATA value from AFC hardware
			1	Uses CORE_BIAS_DATA value from DSP core
SYLE_POLARITY	---c-----------			Controls the polarity of the SYLE output pin (hop pulse)
		R		Returns 0
		W	0	SYLE is a positive pulse
			1	SYLE is a negative pulse
WINDOW_SIZE	----ba98--------			Defines the search window size (in bits) for windowed search mode (for Unique Word or SYNC_D words).
		R		Returns 0
		W	0000	Window size=1
			0001	Window size =3 (1±1)
			•••	
			1111	Window size = 31 (1± 15)
BIAS_THRESHOLD	-------76543210			Bias estimator threshold value
		R		Returns 0
		W	XXh	Sets the bias value

Notes:
1. VP_CLOCK. Internally synchronized to avoid glitches. Changes to this bit take effect immediately.
2. SYLE_POLARITY. Changes to this bit take effect immediately.
3. BIAS_THRESHOLD. The bias threshold must be coded as a negative value (opposite of the threshold value) coded in 2's complement. The nominal value for the threshold is -46 (=D3h). Internally, this value is sign-extended to 13 bits.

REGISTER DESCRIPTION (Continued)

Table 13. Bank 3 Register EXT1

Config 2 Field	Bank 3 Bit Position	EXT1 R/W	Data	Description
ANTENNA_SW_DEFEAT	f---------------			Controls optional antenna switching (ANT0 and ANT1 pins)
		R		Returns 0
		W	0	Enables antenna switching
			1	Disables antenna switching
ANTENNA_SW_OFFSET	-edcba98--------			Controls antenna switching time advancement Returns 0
		R		Offset in number of 2.048 MHz clock cycles
		W	xXh	(<108)
SLEEP_PERIOD	--------76543210	W	00h	Programs sleep duration in sleep mode Illegal
			01h	Sleep period=1 frame (4 ms)
			•••	
			FFh	Sleep period = 255 frames (1.020s)
SLEEP_REMAINING	--------76543210			Returns value of sleep counter when sleep mode is interrupted by a "wake" signal
		R	00h	Normal expiration of sleep counter
			01h	One frame left before normal expiration
			•••	
			FFh	255 frames left before normal expiration

Notes:
1. SLEEP_PERIOD. In sleep mode, the RFEON pin is active. Changes to this bit take effect immediately.
2. SLEEP_REMAINING. A non-zero value indicates that the Z87000 was awakened by a key press activating one of the wake-up pins on port 0. In this case, the processor should immediately reset the SLEEP_WAKE field in SSPSTATE to prevent the process from going back to sleep when the user key press ceases.

Table 14. Bank 3 Register Description

SSPSTATE Field	Bank 3 Bit Position	EXT2 R/W	Data	Description
SW_SYLE	f---------------			Controls accelerated synthesizer programming after sleep
		R/W	0*	Not Active
			1	Active
STOP_CODCLK	-e--------------			Inhibits toggling of codec clock output during sleep
		R/W	0*	CODCLK is free running
			1	CODCLK is frozen high
DBP_STOP_CLOCK	--d-------------			Controls toggling of CLKOUT output pin (clock for ADPCM Processor).
		R/W	0*	CLKOUT is free running
			1	CLKOUT is frozen high
BSYNC_GAIN	---c------------			Selects gain for first order loop of the bit synchronizer
		R/W	0*	Nominal gain
			1	Gain divided by 64
BIAS_ENABLE	----b-----------			Controls closed-loop AFC circuit
		R/W	0*	No new bias estimation is performed (latest estimate used)
			1	Enables BIAS_ERROR_DATA updates
TX_ENABLE	-----a----------			Global enable for all transmit functions
		R/W	0*	Transmitter disabled
			1	Transmitter enabled
SYNC_SEARCH_WORD	------9---------			Controls the word searched for in search mode
		R/W	0*	Search for UW pattern (Unique Word)
			1	Search for SYNC_D pattern
SYNC_SEARCH_MODE	-------87-------			Controls the search mode (and frame synchronization)
		R/W	00*	No search
			01	Window search (<= UW_LOCATION & WINDOW_SIZE)
			10	Full search (during whole frame)
			11	Not used
HOP_ENABLE	---------6------			Enables transmission of the hop pulse on SYLE pin
		R/W	0	Hop pulse disabled
			1	Hop pulse enabled
SYNC_ACQ_CLEAR	----------5-----			Clears the SYNC_ACQ_IND flag.
		R		Returns last value written
		W	1->0	A transition from 1 to 0 clears the flag
FRAME_START_CLEAR	-----------4----			Clears the FRAME_START_IND flag
		R		Returns last value written
		W	1->0	A transition from 1 to 0 clears the flag
SLEEP_WAKE	------------3---			Enable bit for entering sleep mode
		R/W	0	Wake mode only
			1	Sleep mode can be activated by GO_TO_SLEEP command
MULTIPLEX_SWITCH	-------------21-			Controls operation of the transceiver
		R/W	00*	SMUX (bit inversion and ADPCM Processor access
			01	disabled)
			10	STMUX (bit inv. enabled; ADPCM Proc. access disabled)
			11	Reserved
				TMUX (bit inversion and ADPCM Processor access enabled)
GO_TO_SLEEP	--------------0			Command bit to place the Z87000 in sleep mode
		R		Returns last value written
		W	0->1	A transition from 0 to 1 causes Z87000 sleep mode

REGISTER DESCRIPTION (Continued)

Table 14. Bank 3 Register Description

SSPSTATE Field	Bank 3 Bit Position	EXT2 R/W	Data	Description
TX_ENABLE	-----a----------			Global enable for all transmit functions
		R/W	0*	Transmitter disabled
			1	Transmitter enabled
SYNC_SEARCH_WORD	------9---------			Controls the word searched for in search mode
		R/W	0*	Search for UW pattern (Unique Word)
			1	Search for SYNC_D pattern
SYNC_SEARCH_MODE	-------87-------			Controls the search mode (and frame synchronization)
		R/W	00*	No search
			01	Window search (<= UW_LOCATION & WINDOW_SIZE)
			10	Full search (during whole frame)
			11	Not used
HOP_ENABLE	---------6------			Enables transmission of the hop pulse on SYLE pin
		R/W	0	Hop pulse disabled
			1	Hop pulse enabled
SYNC_ACQ_CLEAR	----------5-----			Clears the SYNC_ACQ_IND flag.
		R		Returns last value written
		W	1->0	A transition from 1 to 0 clears the flag
FRAME_START_CLEAR	-----------4----			Clears the FRAME_START_IND flag
		R		Returns last value written
		W	1->0	A transition from 1 to 0 clears the flag
SLEEP_WAKE	------------3---			Enable bit for entering sleep mode
		R/W	0	Wake mode only
			1	Sleep mode can be activated by GO_TO_SLEEP command
MULTIPLEX_SWITCH	-------------21-			Controls operation of the transceiver
		R/W	00*	SMUX (bit inversion and ADPCM Processor access disabled)
			01	STMUX (bit inv. enabled; ADPCM Proc. access disabled)
			10	Reserved
			11	TMUX (bit inversion and ADPCM Processor access enabled)
GO_TO_SLEEP	--------------0			Command bit to place the Z87000 in sleep mode
		R		Returns last value written
		W	0->1	A transition from 0 to 1 causes Z87000 sleep mode

Notes:

1. DBP_STOP_CLOCK. When this bit is set to 1, the ADPCM Processor clock (CLKOUT) is stopped within two clock periods. When this bit is set to 0, the ADPCM Processor clock restarts within two clock periods; in every case, the ADPCM Processor clock minimum specifications for high time and low time are respected.
2. BSYNC_GAIN. Changes to this bit take effect immediately.
   BIAS_ENABLE. This bit is a global enable for the Automatic Frequency Control. When the bit is set, the AFC hardware updates the current BIAS_ERROR_DATA during specific time windows, controlled by the event trigger hardware and suitable for a good operation of the AFC. When the bit is reset, the AFC operation is suspended. However, the current BIAS_ERROR_DATA, resulting from previous bias estimations, can still be used to bias the downconverter NCO. Changes to the BIAS_ENABLE bit take effect at the beginning of the frame following the change.
3. TX_ENABLE. Global control for all system transmit functions, including RFTX pin control (timing set by the RFTX_PWR_ON/OFF register fields) and power to the modulator and NCO (timing set by MOD_PWR_ON and the wake/sleep modes).
4. Changes to this bit take effect immediately.
5. HOP_ENABLE. Changes to this bit take effect immediately.
6. SLEEP_WAKE. This bit must be set to enable the core to put itself to sleep via the GO_TO_SLEEP command. The SLEEP_WAKE bit must be reset to prevent the core to fall back to sleep after it is awaken by one of the Port 0 Wake-up pins when the sleep period has not expired. If the bit is not reset, the core will fall right back to sleep when the wake-up input is de-asserted (note that by design, a wake-up input has a minimum of 10 ms duration, to allow the software enough time to safely reset the SLEEP_WAKE bit).
7. SYNC_AQC_CLEAR. This bit must be set to "1" again after every "clear" operation to allow for the next "clear".
8. FRAME_START_CLEAR. This bit must be set to "1" again after every "clear" operation to allow for the next ?"clear".

Table 15. Bank 3 Register Description

SSPSTATUS Field	Bank 3 Bit Position	EXT3 R/W	Data	Description
FRAME_COUNTER	fedcba987------			Current frame counter value
		R	00h	First value at beginning of frame (0)
			...	
			173h	Last value at end of frame (371)
			...	Illegal values
		W		No effect
RESERVED	---------65----	R		Returns 0
		W		No effect
HAND_BASE_SEL	----------4---			Reflects status of Handset/Base select pin (HBSW)
		R	0	Base (HBSW = 0)
			1	Handset (HBSW = 1)
		W		No effect
SYNC_ACQ_IND	----------3--			Indicates detection of a Sync word (UW or SYNC_D depending on SYNC_SEARCH_WORD search mode)
		R	0	No sync word detected
		W	1	Sync word detected
				No effect
FRAME_START_IND	----------2--			Indicates start of a new frame
		R	0	No start of new frame (1 written to
			1	FRAME_START_CLR)
		W		New frame started
				No effect
RESERVED	----------10	R		Returns 0
		W		No effect

Notes:
FRAME_COUNTER. Read the double-buffered current value of the Frame Counter.
On the handset, a single frame counter is used to clock transmit and receive events.
On the base station, the transmit frame counter value is returned

Table 16. Bank 3 Register Description

GPIO0DIR Field	Bit 3 Bit Position	EXT4 R/W	Data	Description
DIRECTION0	fedcba9876543210			Independent control of Port 0 pin direction
		R/W	..0.	Sets pin in input mode
			..1.	Sets pin in output mode

Table 17. Bank 3 Register Description

GPIO0DATA Field	Bank 3 Bit Position	EXT5 R/W	Data	Description
DATA0	fedcba9876543210			Access to Port 0 data
		R	XXXXh	Reads pin values
		W	XXXXh	Writes output pin values

Notes:
DATA0. The read value returns the actual pin values and does not depend on the pin directions (i.e. for output pins, the output value is returned unless a contention occurs).

REGISTER DESCRIPTION (Continued)

Table 18. Bank 3 Register Description

GPIO1DIR Field	Bank 3 Bit Position	EXT6 R/W	Data	Description
DIRECTION1	fedcba9876543210			Independent control of Port 1 pin direction
		R/W	..0.	Pin in input mode
			..1.	Pin in output mode

Table 19. Bank 3 Register Description

GPIO1DATA Field	Bank 3 Bit Position	EXT7 R/W	Data	Description
DATA1	fedcba9876543210			Access to Port 1 data
		R	XXXXh	Reads pin values
		W	XXXXh	Writes output pin values

Notes:
DATA1. The read value returns the actual pin values and does not depend on the pin directions (i.e. for output pins, the output value is returned unless a contention occurs)

Bank 2 Registers

Table 20. Bank 2 Register Description

VP_INOUT Field	Bank 2 Bit Position	EXT0 R/W	Data	Description
RESERVED	fedcba98--------	R		Returns 0
		W		No effect
VP_STATUS	--------76543210			Access to ADPCM Processor's Command/Status mailbox
		R	XXh	Reads Status byte from ADPCM Processor
VP_COMMAND	--------76543210			Access to ADPCM Processor's Command/Status mailbox
		W	XXh	Writes Command byte to ADPCM Processor

Table 21. Bank 2 Register Description

RX_CONTROL Field	Bank 2 Bit Position	EXT1 R/W	Data	Description
SNR_ESTIMATE	fedcba9876543210			Access to channel measurement (SNR) estimate Returns the SNR value
		R	XXXXh	
UW_LOCATION	-------876543210			Location of the Unique Word
		W	XXXXh	Initializes the value that the receive frame counter is set to on detection of the Unique Word

Notes:
SNR_ESTIMATE. This value is updated every frame. It should be read by the software during the frequency hopping guard time of the next frame.

Table 22. Bank 2 Register Description

BIAS_ERROR Field	Bank 2 Bit Position	EXT2 R/W	Data	Description
BIAS_ERROR_DATA	fedcba9876543210			Access to the bias estimate from the AFC loop.
		R	XXXXh	Current bias estimate value
		W		No effect

Notes:
BIAS_ERROR_DATA. This value is used to bias the downconverter's NCO if the USE_CORE_BIAS register field is reset. It is encoded as a 2's complement number. The unit is 125 Hz

Table 23. Bank 2 Register Description

RSSI Field	Bank 2 Bit Position	EXT3 R/W	Data	Description
RESERVED	fedcba98--------	R		Returns 0
		W		No effect
RSSI_DATA	-------76543210			Access to 8-bit ADC (can be used for RSSI data)
		R	XXh	Returns latest value on 8-bit DAC
		W		No effect

Note:
RSSI_DATA. This value is sampled once per frame (4ms) approximately at bit 72 (middle) of the received data.

Table 24. Bank 2 Register Description

CORE_BIAS Field	Bank 2 Bit Position	EXT4 R/W	Data	Description
RESERVED	fed------------	R		Returns 0
		W		No effect
CORE_BIAS_DATA	---cba9876543210			Stores bias value for correction of downconverter's NCO.
		R		Returns 0
		W	xXXXh	Updates bias value

Notes:
CORE_BIAS_DATA.This value is used if the USE_CORE_BIAS register field is set. It is encoded as a 2's complement number. The unit is 125 Hz.

REGISTER DESCRIPTION (Continued)

Table 25. Bank 2 Register Description

MOD_PWR_CTRL Field	Bank 2 Bit Position	EXT5 R/W	Data	Description
RESERVED	f---------------	R		Returns 0
		W		No effect
MOD_PWR_ON	-edcba98--------			Determines modulator turn-on time referenced to the transmit frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-on time (=(x modulo 128) -1)
RESERVED	--------76543210	R		Returns 0
		W		No effect

Notes:
1. MOD_PWR_ON. Controls the turn-on time for the internal modulator and NCO. Only the 7 LSBits of the 9-bit value necessary to encode an event (from frame counter 0 to 371) are programmable. The two MSBits have fixed values which depend on whether base station or handset is selected: "00" on the base and "01" on the handset. The modulator's turn-off time occurs a fixed time (number of bits) after the turn-on time: 144 bits on the base station, 148 bits on the handset.
2. Changes to this value take effect immediately.
3. To disable the modulator continuously, clear TX_ENABLE

Table 26. Bank 2 Register Description

DEMOD_PWR_CTRL Field	Bank 2 Bit Position	EXT6 R/W	Data	Description
RFEON_POLARITY	f---------------			Controls the polarity of the RFEON output pin
		R		Returns 0
		W	0	Active high
			1	Active Low
DEMOD_PWR_ON	-edcba98--------			Determines internal power up of demodulator and turn on time of RXON pin, referenced to the receive frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-on time (=(x modulo 128) -1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
DEMOD_PWR_OFF	---------6543210			Determine internal power down of demodulator and turn off time of RXON pin, referenced to the receive frame counter
		R		Returns 0
		W	XXh	Bits 6-0 of turn-off time (=(x modulo 128) -1)

Notes:
1. DEMOD_PWR_ON, DEMOD_PWR_OFF. Controls internal receive hardware and the RXON output pin. The turn-on and off times are given in number of received bit periods and are referenced to the Receive Frame Counter. Only the 7 LSBits of the 9-bit value are programmable. The two MSBits have fixed values which depend on whether base station or handset is selected. For DEMOD_PWR_ON, the two bits are "01" on the base and "00" on the handset. For DEMOD_PWR_OFF, the two bits are "10" on the base and "01" on the handset
2. Changes to these values take effect immediately.
3. To enable receive power continuously, clear TX_ENABLE and set SYNC_SEARCH_MODE to FULL_SEARCH (this is the case in acquisition mode).
4. The polarity of the RXON output pin is controlled by the RFRX_POLARITY bit in the RFRX_PWR_CTRL register

Table 27. Bank 2 Register Description

RFTX_PWR_CTRL Field	Bank 2 Bit Position	EXT7 R/W	Data	Description
RFTX_POLARITY	f---------------			Controls the polarity of the RFTX output pin
		R		Returns 0
		W	0	Active high
			1	Active Low
RFTX_PWR_ON	-edcba98--------			Determines RFTX output pin turn-on time referenced to the transmit frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-on time (=(x modulo 128) -1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
RFTX_PWR_OFF	---------6543210			Determine RFTX output pin turn-off time referenced to the transmit frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-off time (=(x modulo 128) -1)

Notes:

1. RFTX_PWR_ON, RFTX_PWR_OFF. Controls the RFTX output pin, and thereby the external RF module's transmitter. The turn-on and off times are given in number of transmitted bit periods and are referenced to the transmit Frame Counter. Only the 7 LSBits of the 9-bit value are programmable. The two MSBits have fixed values which depend on whether base station or handset is selected. For RFTX_PWR_ON, the two bits are "00" on the base and "01" on the handset. For RFTX_PWR_OFF, the two bits are "01" on the base and "10" on the handset.
2. Changes to these values take effect immediately.
3. To disable the transmitter continuously, clear TX_ENABLE in SSP_STATE.

REGISTER DESCRIPTION (Continued)

Bank 1 Registers

Table 28. Bank 1 Register Description

RATE_BUF_ADDR File	Bank 1 Bit Position	EXT0 R/W	Data	Description
RESERVED	f----------	R		Returns 0
		W		No effect
RX_AUTO_INCREMENT	-e----------			Controls the auto-increment feature of the Rx rate
		R		buffer
		W	0	Returns 0
			1	Disables auto-increment
				Enables auto-increment
RX_BUF_ADDR	--dcba98--------			Access to Rx rate buffer address
		R		Returns 0
		W	00h	Address 0
			...	...
			23h	Address 23h = 35
			...	Illegal
RESERVED	--------7-------	R		Returns 0
		W		No effect
TX_AUTO_INCREMENT	---------6------			Controls the auto-increment feature of the Tx rate
		R		buffer
		W	0	Returns 0
			1	Disables auto-increment
				Enables auto-increment
TX_BUF_ADDR	----------543210			Access to Tx rate buffer address
		R		Returns 0
		W	00h	Address 0
			...	...
			23h	Address 23h = 35
			24h	Tx/Rx rate buffer address for ADPCM Processor
			25h	accesses
			26h	Tx/Rx Nibble Marker bits [15..0]
			27h	Tx/Rx Nibble Marker bits [31..16]
			28h	Tx/Rx Nibble Marker bits [35..32]
			29h	MOD_FREQ_DEV 0
			2Ah	MOD_FREQ_DEV 1
			2Bh	MOD_FREQ_DEV 2
			2Ch	MOD_FREQ_DEV 3
			2Dh	MOD_FREQ_DEV 4
			2Eh	MOD_FREQ_DEV 5
			2Fh	MOD_FREQ_DEV 6
			30h	MOD_FREQ_DEV 7
			31h	MOD_FREQ_DEV 8
			32h	MOD_FREQ_DEV 9
			...	MOD_CENTER_FREQ
				Illegal

Table 29. Bank 1 Register Description

RATE_BUF_DATA Field	Bank 1 Bit Position	EXT1 R/W	Data	Description
RX_BUF_DATA	----------3210			Access to the Rx rate buffer data
		R	Xh	Reads value at current RX_BUF_ADDR address (0 to 23h)
TX_BUF_DATA	----------3210			Access to the Tx rate buffer data
		W	XXXXh	Writes value at current TX_BUF_ADDR address (0 to 23h)
TX_BUF_VP_ADDR	--dcba98--------			Sets the initialization value of the Tx rate buffer address used for ADPCM Processor accesses
		W	XXh	Writes initialization value (TX_BUF_ADDR address= 24h)
RX_BUF_VP_ADDR	----------543210			Sets the initialization value of the Rx rate buffer address used for ADPCM Processor accesses
		W	XXh	Writes initialization value (TX_BUF_ADDR address= 24h)
TX_RX_NIBBLE_MARKER	fedcba9876543210			Sets the Nibble Marker register for Tx and Rx rate buffer accesses by ADPCM Processor
		W	XXXXh	Write nibble marker value (TX_BUF_ADDR= 25h to 27h)
MOD_FREQ	fedcba9876543210			Access to modulator settings
		W	XXXXh	Writes modulator setting value (TX_BUF_ADDR=28h to 32h)

Note:
The meaning and address for any RATE_BUF_DATA is set in the RATE_BUF_ADDR register.
MOD_FREQ. The unit for center frequency and frequency deviation words is 62.5 Hz.
These words are encoded as 2's complement numbers.
The meaning and address for any RATE_BUF_DATA is set in the RATE_BUF_ADDR register.
MOD_FREQ. The unit for center frequency and frequency deviation words is 62.5 Hz.
These words are encoded as 2's complement numbers.

Table 30. Bank 1 Register Description

BIT_SYNC Field	Bank 1 Bit Position	EXT2 R/W	Data	Description
INT_SYM_ERR1	fedcba9876543210			Read access to the integrated symbol error from the bit synchronizer's second order loop
		R	XXXXh	Reads error data bits [23..8] (bits [7..0] are in bank 0, EXT6)
SECOND_ORDER	fedcba9876543210			Write access to the bit synchronizer's second-order loop
		W	XXXXh	Writes second order loop's 16-bit value

Table 31. Bank 1 Register Description

RESERVED Field	Bank 1 Bit Position	EXT3 EXT4 EXT5R/W	Data	Description
RESERVED	fedcba9876543210	R		Returns 0
		W	0000h	Must be left alone or written to 0000h (or unpredictable results may occur)

REGISTER DESCRIPTION (Continued)

Table 32. Bank 1 Register Description

CONTROL Field	Bank 1 Bit Position	EXT6 R/W	Data	Description
RESERVED	fedcb----------	R		Returns 0
		W		No effect
FS_INT_ENABLE	-----a----------			Controls frame start interrupt (INT1)
		R/W	0*	Disables frame start interrupt
			1	Enables frame start interrupt
INTERRUPT_0_ENABLE	------9---------			Controls interrupt 0 (INT0 on P114)
		R/W	0*	Disables interrupt 0
			1	Enables interrupt 0
INTERRUPT_2_ENABLE	-------8--------			Controls interrupt 2 (INT2 on P115)
		R/W	0*	Disables interrupt 2
			1	Enables interrupt 2
P0_WAKEUP_ENABLE	--------7654----			Controls wake-up pins (P0[3..0])
		R/W	0000*	Disables all wake-up pins
			1xxx	Enables P03 as wake-up pin (if in input mode)
			x1xx	Enables P02 as wake-up pin (if in input mode)
			xx1x	Enables P01 as wake-up pin (if in input mode)
			xxx1	Enables P00 as wake-up pin (if in input mode)
TX_PWR_DAC_DATA	------------3210			Access to Tx power 4-bit DAC output data
		R/W	Xh	Sets output value

Note:
P0_WAKEUP_ENABLE. When enabled, pins P0[3..0] are active low wake-up pins for the Z87000 sleep mode. The input signal is internally debounced and synchronized to the bit clock. It is internally given a minimum duration of one bit to allow the software to exit sleep mode safely.

Table 33. Bank 1 Register Description

RESERVED Field	Bank 1 Bit Position	EXT7 R/W	Data	Description
RESERVED	fedcba9876543210	R		Returns 0
		W		No effect

Bank 0 Registers

Table 34. Bank 0 Register Description

RESERVED Field	Bank 0 Bit Position	EXT0 EXT1 EXT2 EXT3 EXT4 EXT5 R/W	Data	Description
RESERVED	fedcba9876543210	R		Returns 0
		W		No effect

Table 35. Bank 0 Register Description

INT_SYM_ERR0 Field	Bank 0 Bit Position	EXT6 R/W	Data	Description
RESERVED	fedcba98--------	R		Returns 0
		W		No effect
INT_SYM_ERR0	--------76543210			Read access to the integrated symbol error from the bit synchronizer's second order loop
		R	XXh	Reads error data bits [7..0] (bits [23..8] are in bank1, EXT2)
		W		No effect

Table 36. Bank 0 Register Description

RFRX_PWR_CTRL Field	Bank 0 Bit Position	EXT7 R/W	Data	Description
RFRX_POLARITY	f---------------			Controls the polarity of the RFRX (and RXON) output pins
		R		Returns 0
		W	0	RFRX active Low and RXON active High
			1	RFRX active High and RXON active Low
RFRX_PWR_ON	-edcba98--------			Determines RFRX output pin turn-on time referenced to the transmit frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-on time (=(x modulo 128) -1)
RESERVED	--------7-------	R		Returns 0
		W		No effect
RFRX_PWR_OFF	---------6543210			Determine RFRX output pin turn-off time referenced to the transmit frame counter
		R		Returns 0
		W	xXh	Bits 6-0 of turn-off time (=(x modulo 128) -1)

Notes:

1. RFRX_POLARITY. Caution: notice the inverse polarity of the RFRX pin.
2. RFRX_PWR_ON, RFRX_PWR_OFF. Controls the RFRX output pin. The turn-on and off times are given in number of transmitted bit periods and are referenced to the TRANSMIT (!) Frame Counter. Only the 7 LSBits of the 9-bit value are programmable. The two MSBits have fixed values which depend on whether base station or handset is selected. For RFRX_PWR_ON, the two bits are "00" on the base and "01" on the handset. For RFRX_PWR_OFF, the two bits are "01" on the base and "10" on the handset.
3. Changes to these values take effect immediately.
4. To disable transmit power continuously, clear TX_ENABLE.

INSTRUCTION SET DESCRIPTION

Refer to Zilog's Z89C00 User's Manual, Chapter 5 (Instruction Set Features) and Chapter 6 (Assembly Language Instruction Set), for a complete description of the core processor's instruction set.

Table 37. Instruction Set Summary

Instruction	Description	Opcode	Synopsis	Operands	# Words	# Cycles	Example
ABS	Absolute Value		ABS[<cc>,]<src>				
		1001000		<cc>,A	1	1	ABS NC,A
		1001000		A	1	1	ABS A
ADD	Addition		ADD<dest>,<src>				
		1001001		A,<pregs>	1	1	ADD A,P0:0
		1000001		A,<dregs>	1	1	ADD A,D0:0
		1000100		A,<limm>	2	2	ADD A,#%1234
		1000101		A,<memind>	1	3	ADD A,@@P0:0
		1000011		A,<direct>	1	1	ADD A,%F2
		1000001		A,<regind>	1	1	ADD A, @P1:1
		1000000		A,<hwregs>	1	1	ADD A,X
AND	Bitwise AND		AND<dest>,<src>				
		1011001		A,<pregs>	1	1	AND A,P2:0
		1010001		A,<dregs>	1	1	AND A,D0:1
		1010100		A,<limm>	2	2	AND A,#%1234
		1010101		A,<memind>	1	3	AND A,@@P1:0
		1010001		A,<direct>	1	1	AND A, %2C
		1010001		A,<regind>	1	1	AND A,@P1:2+LOOP
		1010000		A,<hwregs>	1	1	AND A, EXT3
CALL	Subroutine call		CALL				
		0010100	[<cc>,]<address>	<cc>,<direct>	2	2	CALL sub1
		0010100		<direct>	2	2	CALL Z,sub2
CCF	Clear carry flag		CCF				
		1001010		None	1	1	CCF
CIEF	Clear Carry Flag		CIEF				
		1001010		None	1	1	CIEF
COPF	Clear OP flag		COPF				
		1001010		None	1	1	COPF
CP	Comparison		CP<src1>,<src2>				
		0111001		A,<pregs>	1	1	CP A,P0:0
		0110001		A,<dregs>	1	1	CP A,D3:1
		0110101		A,<memind>	1	3	CP A,@@P0:0
		0110011		A,<direct>	1	1	CP A,%FF
		0110001		A,<regind>	1	1	CP A,@P2:1+
		0110000		A,<hwregs>	1	1	CP A,STACK
		0110100		A,<limm>	2	2	CP A,#%FFCF
DEC	Decrement		DEC [<cc>,]<dest>				
		1001000		<cc>A,	1	1	DEC NZ,A
		1001000		A	1	1	DEC A
INC	Increment		INC [<cc>,] <dest>				
		1001000		<cc>,A	1	1	INC PL,A
		1001000		A	1	1	INC A
JP	Jump		JP [<cc>,]<address>				
		0100110		<cc>,<direct>	2	2	JP NIE,Label
		0100110		<direct>	2	2	JP Label

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Table 37. Instruction Set Summary

Instruction	Description	Opcode	Synopsis	Operands	# Words	# Cycles	Example
LD	Load destination with source		LD<dest>,<src>				
		0000000		A,<hwregs>	1	1	LD A,X
		0000001		A,<dregs>	1	1	LD A,D0:0
		0001001		A,<pregs>	1	1	LD A,P0:1
		0000001		A,<regind>	1	1	LD A,@P1:1
		0000101		A,<memind>	1	3	LD A,@D0:0
		0000011		A,<direct>	1	1	LD A, 124
		0000111		<direct>,A	1	1	LD 124, A
		0000100		<dregs>,<hwregs>	1	1	LD DO:0, EXT7
		0001100		<pregs>,<simm>	1	1	LD P1:1,#%FA
		0001010		<pregs>,<hwregs>	1	1	LD P1:1,EXT1
		0000110		<regind>,<limm>	1	1	LD @P1:1,#%1234
		0000010		<regind>,<hwregs>	1	1	LD @P1:1+,X
		0001001		<hwregs>,<pregs>	1	1	LD Y,P0:0
		0000001		<hwregs>,<dregs>	1	1	LD SR,D0:0
		0000100		<hwregs>,<limm>	2	2	LD PC,#%1234
		0100101		<hwregs>,<accind>	1	3	LD X,@A
		0000101		<hwregs>,<memind>	1	3	LD Y,@D0:0
		0000001		<hwregs>,<regind>	1	1	LD A,@P0:0-LOOP
		0000000		<hwregs>,<hwregs>	1	1	LD X, EXT6
MLD	Multiply						
		1010010	MLD<srcl>,<srcl>	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
		1010010	[,<bank switch>]	<hwregs>,<regind>,<ban	1	1	MLD A,@P1:0,OFF
		1011011		k switch>	1	1	MLD @P1:1,@P2:0
		1011011		<regind>,<regind>	1	1	MLD@P0:1,@P1:0,O
				<regind>,<regind>,<bank switch>			N
MPYA	Multiply and add		MPYA <srcl>,<src2>				
		1010010	[,<bank switch>]	<hwregs>,<regind>	1	1	MPYA A@P0:0
		1010010		<hwregs>,<regind>,<ban	1	1	MPYA A,@P1:0,OFF
		1011011		k switch>	1	1	MPYA @P1:1,@P2:0
		1011011		<regind>,<regind>	1	1	MPYA@P0:1,@P1:0,
				<regind>,<regind>,<bank switch>			ON
MPYS	Multiply and subtract		MPYS<src1>,<src2>				
		0010010	[,<bank switch>]	<hwregs>,<regind>	1	1	MPYS A,@P0:0
		0010010		<hwregs>,<regind>,<ban	1	1	MPYS A,@P1:0,OFF
		0011011		k switch>	1	1	MPYS @P1:1,@P2:0
		0011011		<regind>,<regind>	1	1	MPYS@P0:1,@P1:0,
				<regind>,<regind>,<bank switch>			ON
NEG	Negate		NEG <cc>,A				
		1001000		<cc>, A	1	1	NEG NZ,A
		1001000		A	1	1	NEG A
NOP	No operation		NOP				
		0000000		None	1	1	NOP
OR	Bitwise OR		OR <dest>,<src>				
		1101001		A, <pregs>	1	1	OR A, P0:1
		1100001		A, <dregs>	1	1	OR A, D0:1
		1100100		A, <limm>	2	2	OR A,#%202
		1100101		A, <memind>	1	3	OR A,@@P2:1+
		1100011		A, <direct>	1	1	OR A, %2C
		1100001		A, <regind>	1	1	OR A, @P1:0-LOOP
		1100000		A, <hwregs>	1	1	OR A, EXT6

INSTRUCTION SET DESCRIPTION (Continued)

Table 37. Instruction Set Summary

Instruction	Description	Opcode	Synopsis	Operands	# Words	# Cycles	Example
POP	Pop value from stack		POP <dest>				
		0001010		<pregs>	1	1	POP P0:0
		0000100		<regs>	1	1	POP D0:1
		0000010		<regind>	1	1	POP @P0:0
		0000000		<hwregs>	1	1	POP A
PUSH	Push value onto stack		PUSH <src>				
		0001001		<pregs>	1	1	PUSH P0:0
		0000001		<dregs>	1	1	PUSH D0:1
		0000001		<regind>	1	1	PUSH @P0:0
		0000000		<hwregs>	1	1	PUSH BU5
		0000100		<limm>	2	2	PUSH #12345
		0100101		<accind>	1	3	PUSH @A
		0000101		<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine		RET				
		0000000		None	1	2	RET
RL	Rotate Left		RL <cc>,A				
		1001000		<cc>,A	1	1	RL NZ,A
		1001000		A	1	1	RL A
RR	Rotate Right		RR <cc>,A				
		1001000		<cc>,A	1	1	RR C,A
		1001000		A	1	1	RR A
SCF	Set C flag		SCF				
		1001010		None	1	1	SCF
SIEF	Set IE flag		SIEF				
		1001010		None	1	1	SIEF
SLL	Shift left logical		SLL				
		1001000		[<cc>,]A	1	1	SLL NZ,A
		1001000		A	1	1	SLL A
SOPF	Set OP flag		SOPF				
		1001010		None	1	1	SOPF
SRA	Shift right arithmetic		SRA<cc>,A				
		1001000		<cc>,A	1	1	SRA NZ,A
		1001000		A	1	1	SRA A
SUB	Subtract		SUB<dest>,<src>				
		0011001		A,<pregs>	1	1	SUB A,P1:1
		0010011		A,<dregs>	1	1	SUB A,D0:1
		0010100		A,<limm>	2	2	SUB A,#%2C2C
		0010101		A, <memind>	1	3	SUB A,@D0:1
		0010011		A, <direct>	1	1	SUB A,%15
		0010001		A, <regind>	1	1	SUB A, @P2:0-LOOP
		0010000		A, <hwregs>	1	1	SUB A, STACK
XOR	Bitwise exclusive OR		XOR <dest>,<src>				
		1111001		A, <pregs>	1	1	XOR A, P2:0
		1110001		A, <dregs>	1	1	XOR A,D0:1
		1110100		A, <limm>	2	2	XOR A,#13933
		1110001		A, <memind>	1	3	XOR A,@P2:1+
		1110011		A, <direct>	1	1	XOR A, %2F
		1110001		A, <regind>	1	1	XOR A, @P2:0
		1110000		A, <hwregs>	1	1	XOR A, BUS

Z87000/Z87L00
Spread Spectrum Transmitters 1

Z87010/Z87L10
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Z87010/Z87L10
AUDIO ENCODER/DECODERS

FEATURES

Device	ROM (Kbyte)	I/O Lines	Package Information
Z87010	4	16	44-Pin PLCC 44-Pin QFP
Z87L10	4	16	44-Pin QFP

Hardware

- 16-Bit DSP Processor
- 3.0V to 3.6V; -20° to +70°C, Z87L10
  4.5V to 5.5V, -20° to +70°C, Z87010
- Static Architecture
- 512 Word On-Chip RAM
- Modified Harvard Architecture
- Direct Interface to Z87000 Frequency Hopping Spreader/Despreader
- Direct Interface to 8-Bit μ-law Telephone CODEC
- I/O Bus (16-Bit Tristable Data, 3-Bit Address)
- Wait State Generator
- Two External Interrupts
- Four Separate I/O Pins (2 Input, 2 Output)

Software

- Full Duplex 32 Kbps ADPCM Encoding/Decoding
- Single Tone and DTMF Signal Generation
- Sidetone, Volume Control, Mute Functions
- Large Phone Number Memory (21 numbers of 23 digits each)
- Master-Slave Protocol Interface to Z87000 Spreader/-Despreader

GENERAL DESCRIPTION

The Z87010/Z87L10 is a second generation CMOS Digital Signal Processor (DSP) that has been ROM-coded by Zilog to provide full-duplex 32 Kbps, Adaptive Delta Pulse Code Modulation (ADPCM) speech coding/decoding (CODEC), and interface to the Z87000/Z87L00 Spread Spectrum Cordless Telephone Controller. Together the Z87000/Z87L00 and Z87010/Z87L10 devices support the implementation of a 900 MHz frequency-hopping spread spectrum cordless telephone in conformance with United States FCC regulations for unlicensed operation.

The Z87010 and Z87L10 are distinct 5V and 3.3V versions of the ADPCM Audio Encoder/Decoder. For the sake of brevity, all subsequent references to the Z87010 in this document also are applicable to the Z87L10, unless specifically noted.

The Z87010's single cycle instruction execution and Harvard bus structure promote efficient algorithm execution. The processor contains a 4K word program ROM and 512 word data RAM. Six dual operand fetching. Three vectored interrupts are complemented by a six level stack. The CODEC interface enables high-speed transfer rate to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface. An additional 13-bit timer is dedicated for general-purpose use.

The Z87010's circuitry is optimized to accommodate intricate signal processing algorithms and is used here for speech compression/decompression, generation of DTMF tones and other cordless telephone functions. Dedicated hardware allows direct interface to a variety of CODEC

GENERAL DESCRIPTION (Continued)

ICs. As configured by the Zilog-provided embedded software for digital cordless phones, the Z87010 supports a low-cost 8-bit μ-law telephone CODEC. The Z87010 is to be used with the Z87000 and operates at 16.384 MHz, providing 16 MIPS of processing power needed for the cordless telephone application.

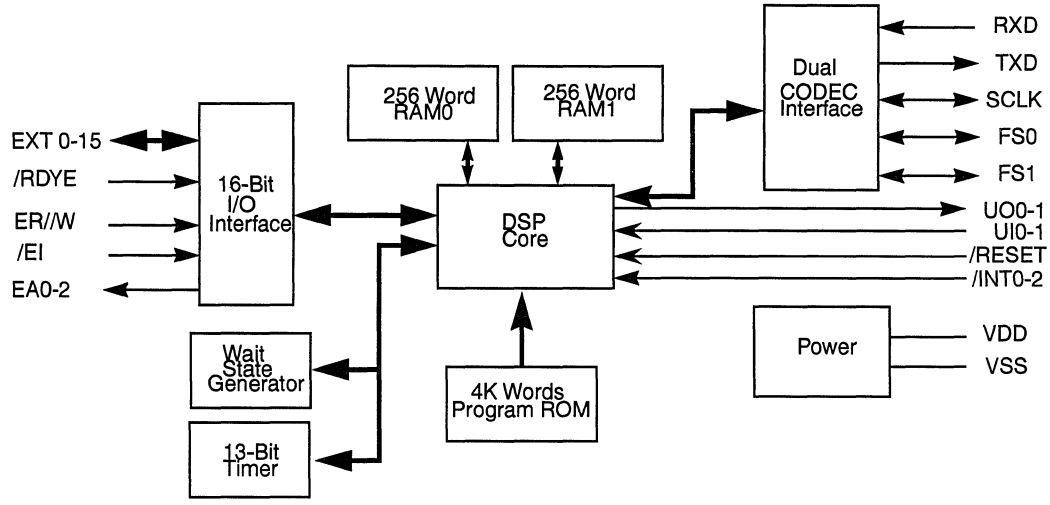

Figure 1. Z87010 Functional Block Diagram

Notes: All signals with a preceding front slash, '/', are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PIN DESCRIPTION

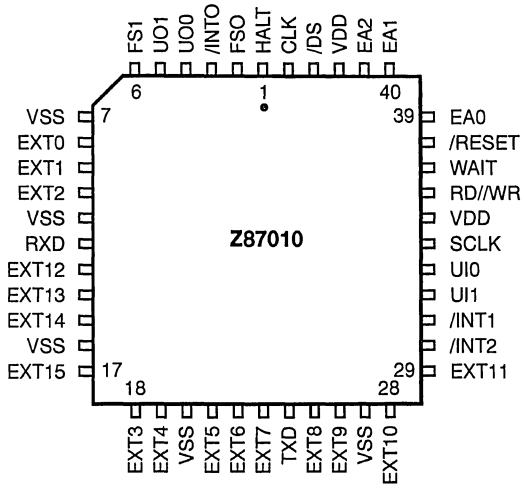

Figure 2. 44-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	CODEC0 frame sync	Input/Output*
3	/INT0	Interrupt	Input
4-5	UO0-UO1	User output	Output
6	FS1	CODEC1 frame sync	Input/Output*
7,11,16,20,27	V_{SS}	Ground	
8-10	EXT0-EXT2	External data bus	Input/Output
12	RXD	Serial input from CODECs	Input
13-15	EXT12-EXT14	External data bus	Input/Output
17	EXT15	External data bus	Input/Output
18-19	EXT3-EXT4	External data bus	Input/Output
21-23	EXT5-EXT7	External data bus	Input/Output
24	TXD	Serial output to CODECs	Output
25-26	EXT8-EXT9	External data bus	Input/Output
28-29	EXT10-EXT11	External data bus	Input/Output
30	/INT2	Interrupt	Input
31	/INT1	Interrupt	Input
32	UI1	User input	Input
33	UI0	User input	Input
34	SCLK	CODEC serial clock	Input/Output*
35,42	V_{DD}	Power supply	Input
36	RD//WR	RD /WR strobe for EXT bus	Output
37	WAIT	WAIT state	Input
38	/RESET	Reset	Input
39-41	EA0-EA2	External address bus	Output
43	/DS	Data strobe for external bus	Output
44	CLK	Clock	Input

Note: *Defined input or output by interface mode selection

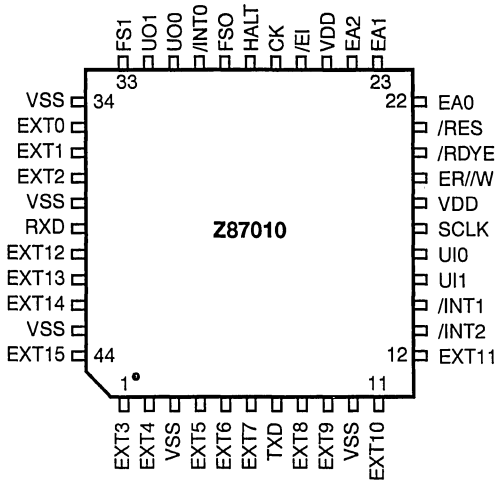

Figure 3. 44-Pin QFP Pin Assignments

PIN DESCRIPTION (Continued)

Table 2. 44-Pin QFP Pin Identification

No.	Symbol	Function	Direction
1-2	EXT3-EXT4	External data bus	Input/Output
3,10	V_{SS}	Ground	–
4-6	EXT5-EXT7	External data bus	Input/Output
7	TXD	Serial output to CODECs	Output
8-9	EXT8-EXT9	External data bus	Input/Output
11-12	EXT10-EXT11	External data bus	Input/Output
13	/INT2	Interrupt	Input
14	/INT1	Interrupt	Input
15	UI1	User input	Input
16	UI0	User input	Input
17	SCLK	CODEC serial clock	Input/Output*
18,25	V_{DD}	Power supply	Input
19	ER//W	R/W for External Bus	Output
20	/RDYE	Data Ready	Input
21	/RES	Reset	Input
22-24	EA0-EA2	External Address Bus	Output
26	/EI	Data Strobe for External Bus	Output
27	CK	Clock	Input
28	HALT	Stop Execution	Input
29	FS0	CODEC0 Frame Sync	Input/Output*
30	/INT0	Interrupt	Input
31-32	U00-U01	User Output	–
33	FS1	CODEC1 Frame Sync	Input/Output*
34	V_{SS}	Ground	Input
35-37	EXT0-EXT2	External data bus	Input/Output
38	V_{SS}	Ground	Input
39	RXD	Serial Input to CODEC	Input
40-42	EXT12-EXT14	External Data Bus	Input/Output
43	V_{SS}	Ground	Input
44	EXT15	External Data Bus	Input/Output

Note: *Input or output is defined by interface mode selection.

ABSOLUTE MAXIMUM RATING

Symbol	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°C	+150°C	C
T_A	Oper. Ambient Temp	-25°	+70°	C

Note: *Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 4).

Standard test conditions are as follows:

$3.0V \leq V_{DD} \leq 3.6V$ (Z87L10)
$4.5V \leq V_{DD} \leq 5.5V$ (Z87010)
$V_{SS} = 0V$
$T_A = -20°$ to $+70°C$

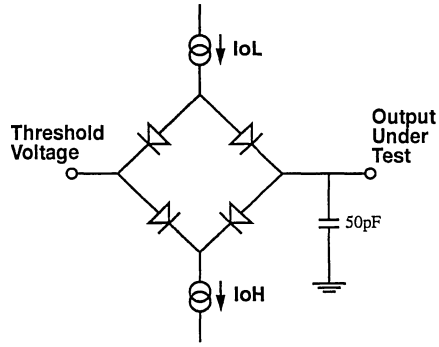

Figure 4. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5V to 5.5V (Z87010)

			T_A=-20°C to +70°C		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Units**
I_{DD}	Supply Current	V_{DD}=5.5V fclock=16.384 MHz		40	mA
I_{DC}	DC Power Consumption	V_{DD}=5.5V		0.2	mA
V_{IH}	Input High Level		2.7		V
V_{IL}	Input Low Level			0.8	V
I_L	Input Leakage			10	µA
V_{OH}	Output High Voltage	I_{OH}=-100µA	V_{DD}-0.2		V
V_{OL}	Output Low Voltage	I_{OL}=2.0 mA		0.5	V (1)
I_{FL}	Output Floating Leakage Current			10	µA

Note:
5. The following specifications are pin specific: EA0-2 has I_{OL} = 5 mA @ 0.5V
6. I_{OH} = 1 mA @ 3.3V

V_{DD} = 3.0V to 3.6V (Z87L10)

			T_A=-20°C to +70°C		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Units**
I_{DD}	Supply Current	V_{DD}=3.6V fclock=16.384 MHz		25	mA
I_{DC}	DC Power Consumption	V_{DD}=3.6V		0.2	mA
V_{IH}	Input High Level		.7V_{DD}	V_{DD}+.3	V
V_{IL}	Input Low Level		Vss-.3	.1V_{DD}	V
I_L	Input Leakage			10	µA
V_{OH}	Output High Voltage	I_{OH}=-50µA	V_{DD}-0.2		V
V_{OL}	Output Low Voltage	I_{OL}=1.0 mA		0.5	V (1)
I_{FL}	Output Floating Leakage Current			10	µA

Note:
7. The following specifications are pin specific: EA0-2 has I_{OL} = 5 mA @ 0.5V
8. I_{OH} = 1 mA @ 3.3V

AC ELECTRICAL CHARACTERISTICS

)

		T_A = -20°C to +70°C	
Symbol	**Parameter**	**Min (ns)**	**Max (ns)**
TCY	Clock Cycle Time	50	–
PWW	Clock Pulse Width	23	–
Tr	Clock Rise Time	–	2
Tf	Clock Fall Time	–	2
TEAD	EA, ER//W Delay from CK	5	28
TXVD	EXT Data Output Valid from CK	5	33
TXWH	EXT Data Output Hold from CK	3	25
TXRS	EXT Data Input Setup Time	10	–
TXRH	EXT Data Input Hold from CK	10	25
TIEDR	/EI Delay Time from CK	3	15
TIEDF		0	15
RDYS	Ready Setup Time	8	–
RDYH	Ready Hold Time	5	–
TINS	Int. Setup Time to CLK Fall	3	–
TINL	Int. Low Pulse Width	10	–
THS	Halt Setup Time to CLK Rise	3	–
THH	Halt Hold Time to CLK Rise	10	–

2

AC TIMING DIAGRAMS

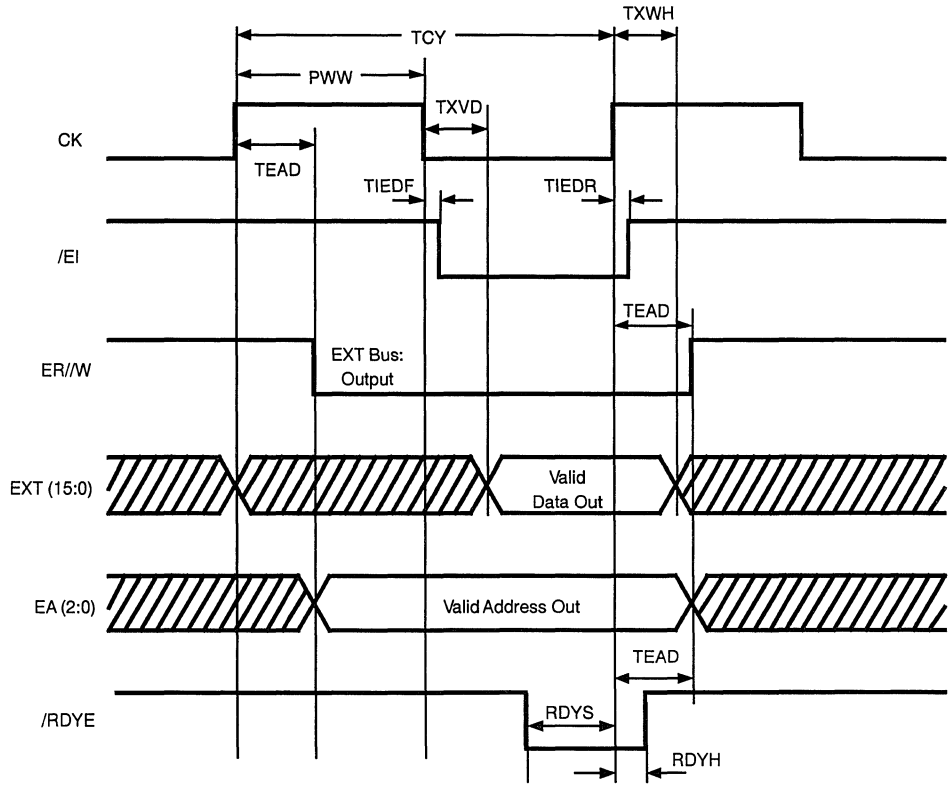

Figure 5. Write to External Device Timing

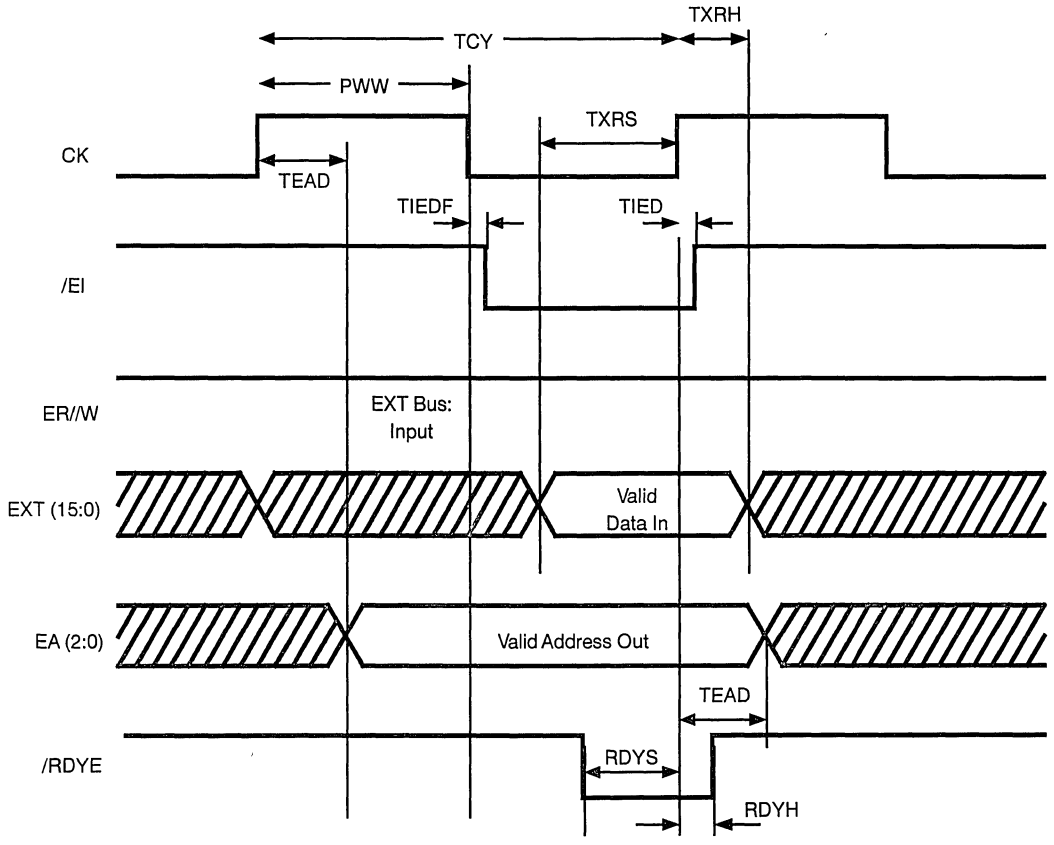

Figure 6. Read From External Device Timing

AC TIMING DIAGRAMS (Continued)

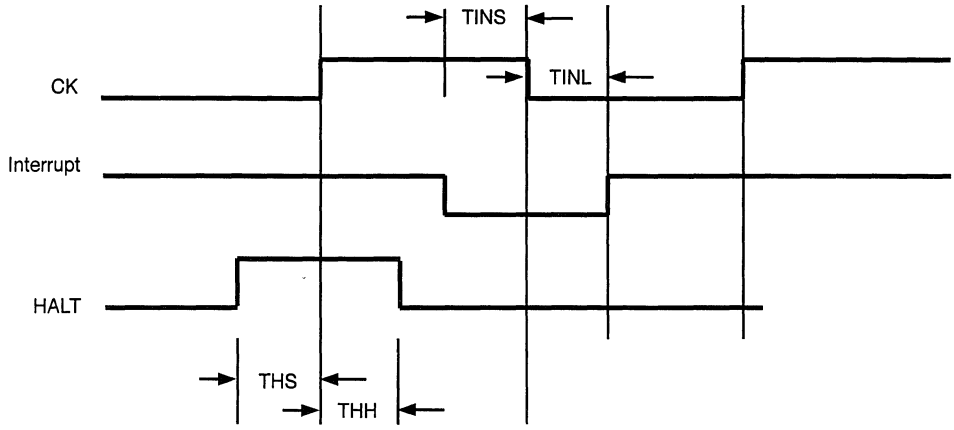

Figure 7. Interrupt/HALT Timing

Table 3. CODEC Interface-AC Timing

Internal SCLK		Min	Max
SDCR	SCLK down from CLK rise	–	15
SUCR	SCLK up from CLK rise	–	15
FDCR	FS0, FS1 down from SCLK rise	–	6
FUCR	FS0, FS1 up from SCLK rise	–	6
TDSR	TXD down from SCLK rise	–	7
TUSR	TXD up from SCLK rise	–	7
RSU	RXD Setup time in respect to SCLK fall	7	
RH	RXD Hold time in respect to SCLK fall	0	
FDCR	FS0,FS1 down from SCLK rise	–	13
FUCR	FS0, FS1 up from SCLK rise	–	13
TDSR	TXD down from SCLK rise	–	12
TUSR	TXD up from SCLK rise	–	12
RSU	RXD setup time in respect to SCLK fall	1	
RH	RXD Hold Time in respect to SCLK fall	6	

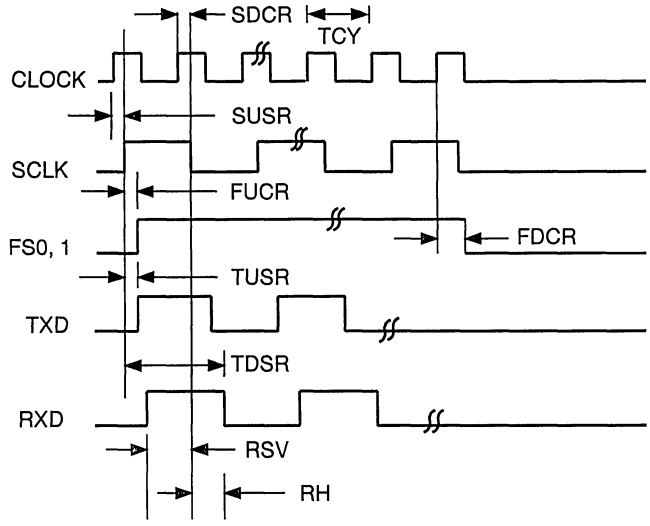

Figure 8. CODEC Interface Timing

PIN FUNCTIONS

CK *Clock (input).* This pin controls the external clock.

EXT15-EXT0 *External Data Bus* (input/output). Data bus for user-defined outside registers. The pins are normally tri-stated, except when the outside registers are specified as destination registers in the instructions. All the control signals exist to allow a read or a write through this bus. The bus is used for Z87000 interface.

ER/W *External Bus Direction* (output). Data direction signal for EXT-Bus. Data is available from the CPU on EXT15-EXT0 when this signal is Low. EXT-Bus is in input mode (high-impedance) when this signal is High.

EA2-EA0 *External Address* (output). User-defined register address output (latched). One of eight user-defined external registers is selected by the processor with these addresses are part of the processor memory map, the processor is simply executing internal reads and writes. External Addresses EXT4-EXT7 are used internally by the processor if the CODEC interface and 13-bit timer are enabled.

/EI *Enable Input* (output). Read/Write timing signal for EXT-Bus. User strobe is for triggering external peripheral. Data is read by the external peripheral on the rising edge of /EI. Data is read by the processor on the rising edge of CK not /EI.

HALT *Halt State* (input). Stop Execution Control. The CPU continuously executes NOPs and the program counter remains at the same value when this pin is held High. This signal must be synchronized with CK. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

/INT2-/INT0 *Three Interrupts* (input, active Low). Interrupt request 2-0. Interrupts are generated on the rising edge of the input signal. Interrupt vectors for the interrupt service routine starting address are stored in the program memory locations 0FFFH for /INT0, 0FFEH for /INT1, and 0FFFDH for /INT2. Priorities are: INT2=Lowest, INT0=highest.

INT1 and INT2 are shared with internal Z87010 peripherals. INT1 is dedicated to the CODEC interface if enabled. INT2 services the 13-bit Timer if enabled. In the Z87010 standard software configuration, INT0 and INT2 are not used; INT1 is used by the CODEC interface.

/RES *Reset* (input, active Low). This pin controls the asynchronous reset signal. The /RESET signal must be kept Low for at least one clock cycle. The CPU pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH after the reset signal is released.

/RDYE *Data Ready* (input). User-supplied Data Ready signal for data to and from external data bus. This pin stretches the /EI and ER/W lines and maintains data on the address bus and data bus. The ready signal is sampled from the rising clock only if ready is active. A single wait-state can be generated internally by setting the appropriate bits in the EXT7-2 register.

UI1-UI0 *Two Input Pins* (input). General-purpose input pins. These input pins are directly tested by the conditional branch instructions: and are reflected in two bits of the status register (S10 and S11). These are asynchronous input signals that have no special clock synchronization requirements.

U01-U00 *Two Output Pins* (push-pull output). General-purpose output pins. These pins reflect the value of two bits in the status register (S5 and S6). UO0 is dedicated to provide an interrupt signal to the Z87000 controller. Note: the user output pin values are the inverse of the status register content.

FUNCTIONAL DESCRIPTION

General functional partitioning of the Z87010 is shown in Figure 1. The chip consists of the Z89S00 static DSP core with 512 words of RAM, 4K words of ROM, a CODEC interface, a general-purpose timer and a wait state generator.

The DSP core is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction and multiply-accumulate of two 16-bit operands. Most instructions are executed in one clock cycle.

The DSP core uses a RAM memory of 512 16-bit words divided in two banks.

Program Memory. The Z87010 has a 4K 16-bit words internal ROM including 4 words for interrupt and reset vectors. The ROM is mapped at address 0000H to 0FFFH. The reset vector is located at address 0FFCH, interrupts INT0 is at 0FFDH, interrupt INT1 is at 0FFEH and interrupt INT2 is at 0FFFH.

Interrupts. The Z87010 has three positive edge-triggered interrupt inputs pins. However, INT1 is dedicated to the CODEC interface and INT2 is dedicated to the 13-bit timer if these peripherals are enabled.

User Inputs. The Z87010 has two inputs, UI0 and UI1, which may be used by Jump and Call instructions. The Jump or Call tests one of these pins and if appropriate, jumps to a new location. Otherwise, the instruction behaves like a NOP. These inputs are also connected to the status register bits S10 and S11, which may be read by the appropriate instruction.

User Outputs. The status register bits S5 and S6 connect directly to UO0 and UO1 pins and may be written to by the appropriate instruction. Note: The user output value is the opposite of the status register content.

I/O Bus. The Z87010 provides a 16-bit, CMOS compatible I/O bus. I/O Control pins provide convenient communication capabilities with external peripherals. Single cycle access is possible. For slower communications, an on-board hardware wait-state generator can be used to accommodate timing conflicts.

These latched output address pins (EA0-2) allow a maximum of eight external peripherals. However up to four of these addresses (EXT4-7) are used by internal peripherals if enabled.

EXT4 13-bit Timer Configuration Register

EXT5 CODEC Interface Channel 0 Data

EXT6 CODEC Interface Channel 1 Data

EXT7 CODEC Interface Configuration Register and Wait State Generator.

CODEC INTERFACE

The CODEC interface provides direct-connect capabilities for standard 8-bit PCM CODECs with hardware μ-law compression. Internal registers EXT5, EXT6 and EXT7 are used to program the CODEC mode. One serial clock and two frame sync control signals are provided, allowing for two bidirectional data channels.

Note: μ-law expansion must be done in software.

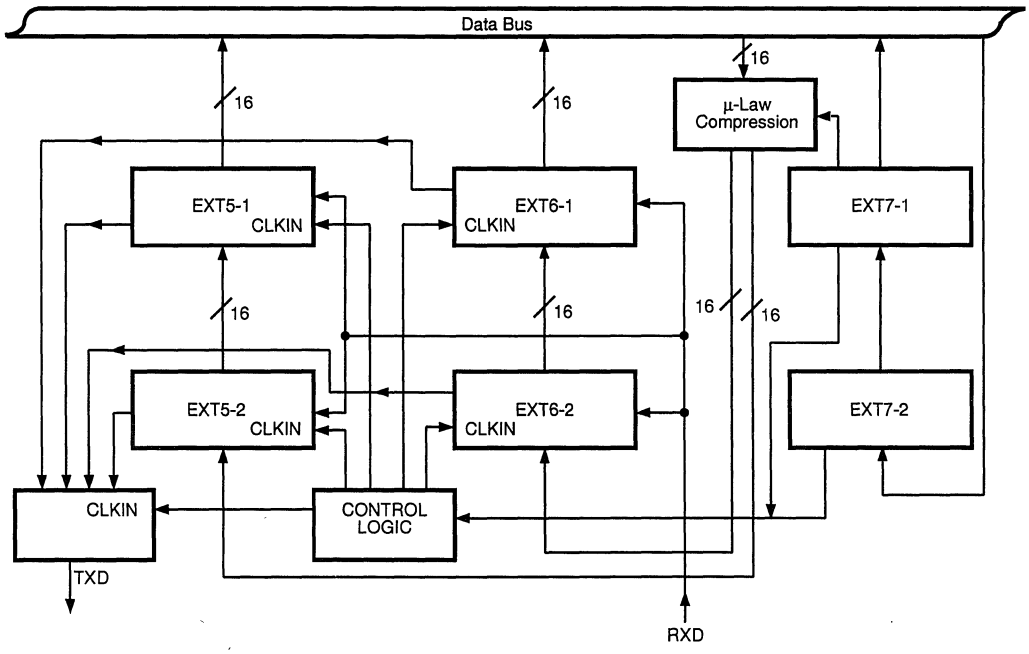

Figure 9. CODEC Interface Block Diagram

CODEC Interface Hardware

The Hardware for the CODEC Interface uses six 16-bit registers, μ-law compression logic and general-purpose logic to control transfers to the appropriate register.

CODEC Interface Control Signals

SCLK (Serial Clock)
The Serial Clock provides a clock signal for operating the external CODEC. A 4-bit prescaler is used to determine the frequency of the output signal.

SCLK = (0.5* CLK)/PS where: CLK = System Clock

PS = 4-bit Prescaler*

Note: An internal divide-by-two is performed before the clock signal is passed to the Serial Clock prescaler.

* The Prescaler is an up-counter.

Assuming an input clock of 16.384 MHz, SCLK is programmed by the Z87010 embedded software for 2.048 MHz.

TXD (Serial Output to CODEC)
The TXD line provides 8-bit data transfers. Each bit is clocked out of the processor by the rising edge of the SCLK, with the MSB transmitted first.

RXD (Serial Input from CODEC)
The RXD line provides 8-bit data transfers. Each bit is clocked into the processor by the falling edge of the SCLK, with the MSB received first.

FS0, FS1 (Frame Sync)
The Frame Sync is used for enabling data transfer/receive. The rising and falling edge of the Frame Sync encloses the serial data transmission. The Z87010 embedded software programs the Frame Sync signal to 8 kHz.

Interrupt
Once the transmission of serial data is completed an internal interrupt signal is initiated. A single-cycle Low pulse provides an interrupt on INT1. When this occurs, the processor will jump to the defined Interrupt 1 vector location.

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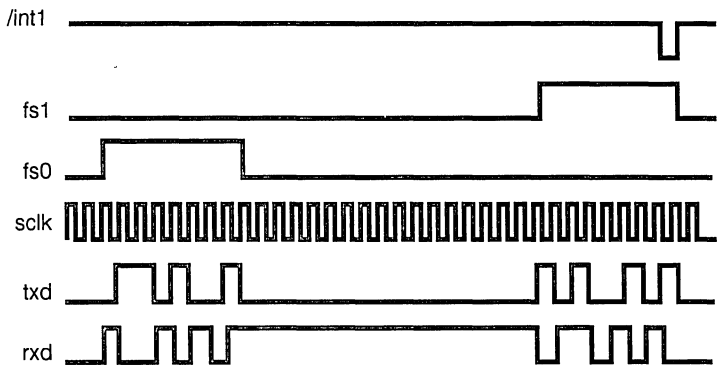


Figure 10. CODEC Interface Timing (8-Bit Mode)

CODEC Interface Timing

Figure 10 depicts a typical 8-bit serial data transfer using both of the CODEC Interface Channels. The transmitting data is clocked out on the rising edge of the SCLK signal. An external CODEC clocks data in on the falling edge of the SCLK signal. Once the serial data is transmitted, an interrupt is given. The CODEC interface signals are not initiated if the CODEC interface is not enabled.

The following modes are available for FSYNC and SCLK signals:

SCLK	FSYNC
Internal	Internal
External	External
External	Internal
Internal	External

CODEC INTERFACE (Continued)

The CODEC interface timing is independent of the processor clock when external mode is chosen. This feature provides the capability for an external device to control the transfer of data to the Z87010. The Frame Sync signal envelopes the transmitted data (Figure 10), therefore care must be taken to ensure proper sync signal timing. In the cordless phone system, the SCLK is externally provided by the Z87000 controller, while FSYNC is internally generated.

The Transmit and Receive lines are used for transfer of serial data to or from the CODEC interface. The CODEC interface performs both data transmit and receive simultaneously.

The FSYNC Signals (FS0, FS1) when programmed for internal mode, are generated by 9-bit counter with SCLK as input clock. Together with the SCLK prescaler, this counter forms a 13-bit counter clocked by the system clock divided by two. The output of this counter can be used to clock the general-purpose 13-bit counter/timer, to form a 26-bit counter.

CODEC Control Registers

The CODEC interface is accessed through addresses EXT5, EXT6 and EXT7. The data accesses are double-buffered registers: two registers (EXT5-1 and EXT5-2) are mapped on address EXT5 and similarly EXT6-1 and EXT6-2 registers are mapped on address EXT6.

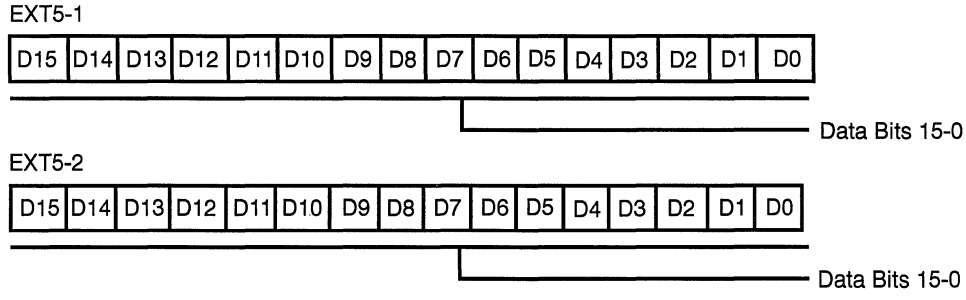


Figure 11. CODEC Interface Data Registers (Channel 0)

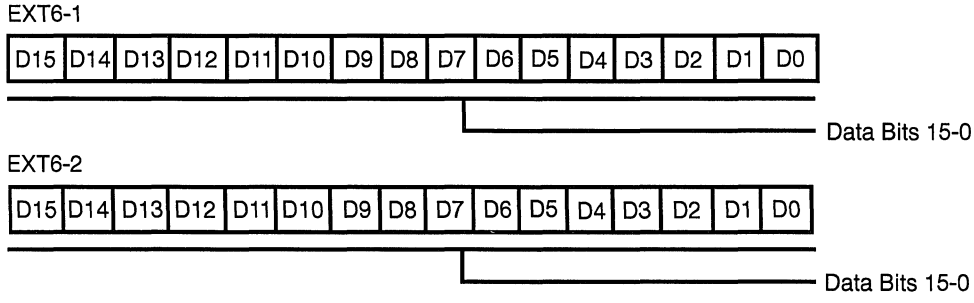


Figure 12. CODEC Interface Data Registers (Channel 1)

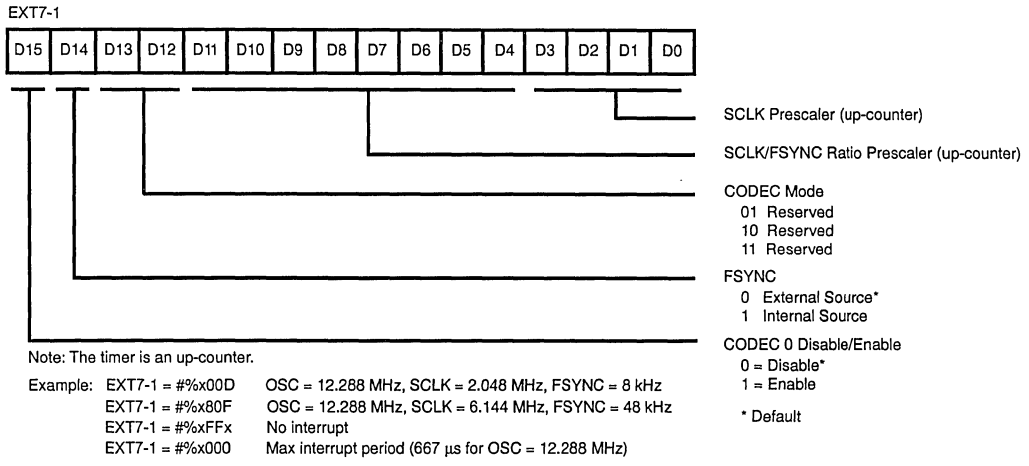


Figure 13. CODEC Interface Control Register

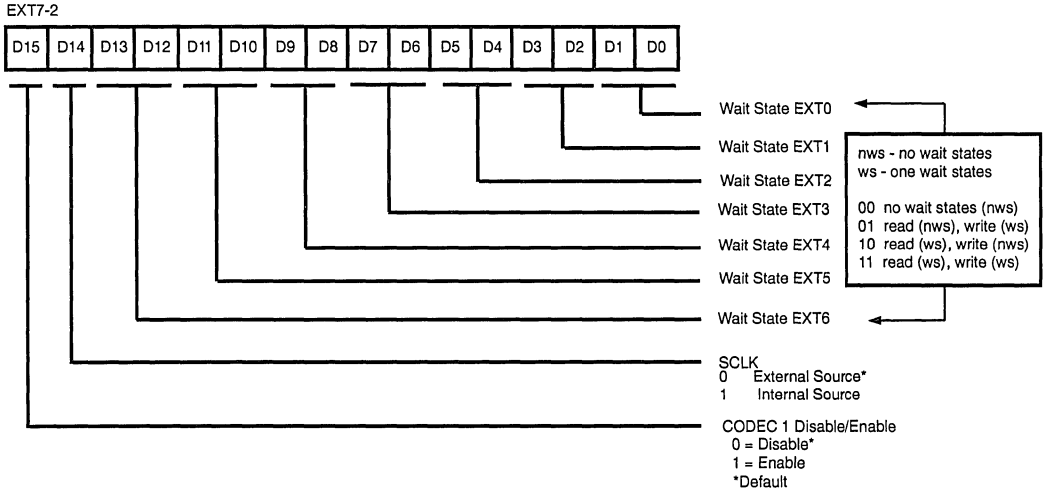


Figure 14. Wait/State/CODEC Interface Control Register

CODEC INTERFACE (Continued)

The CODEC Interface Control Register (EXT7-1) is shown on Figure 13. Setting of the CODEC mode, FSYNC mode and CODEC 0 enable/disable is done through this register. A second control register (EXT7-2) also mapped on address EXT7 control the CODEC 1, SCLK source and wait state generator (see Figure 9). The "operation" section describes how to access the various register.

Wait-State Generator

An internal wait state generator is provided to accommodate slow external peripherals. One wait-state can be automatically inserted by the Z87010 in any EXT bus access. Read and/or write cycles can be independently lengthened for each register, by setting register EXT7-2 accordingly. See Figure 9 for detailed description of EXT7-2.

The Z87010 software uses one wait state on all external register accesses.

For additional wait states, a dedicate pin (/RDYE) can be held high. The /RDYE pin is monitored only during execution of a Read or Write Instruction to external peripherals.

General-Purpose Counter Timer

A 13-bit counter/timer is available for general-purpose use. When the counter counts down to the zero state, an interrupt is received on INT2. If the counter is disabled, EXT4 can be used as a general-purpose address. The counting operation of the counter can be disabled by resetting bit 14. By selecting the clock source to the CODEC counter output (FSYNC), one can extend the counter to a total of 26 bits.

Note: Placing zeroes into the Count Value register does not generate an interrupt. Therefore it is possible to have a single-pass option by loading the counter with zero after the start of count.

The Counter is defaulted to the Enable state. If the system designer does not choose to use the timer, the counter can be disabled. Once disabled, the designer cannot enable the counter unless a reset of the processor is performed.

Example:

```
LD    EXT, #%C0008 1100 0000 0000 1000
                   ; Enable Counter
                   ; Enable Counting
                   ; Clock Source = OSC/2
                   ; Count Value = 1000=8
                   ; Interrupt will occur every 16 clock
                     cycles
```

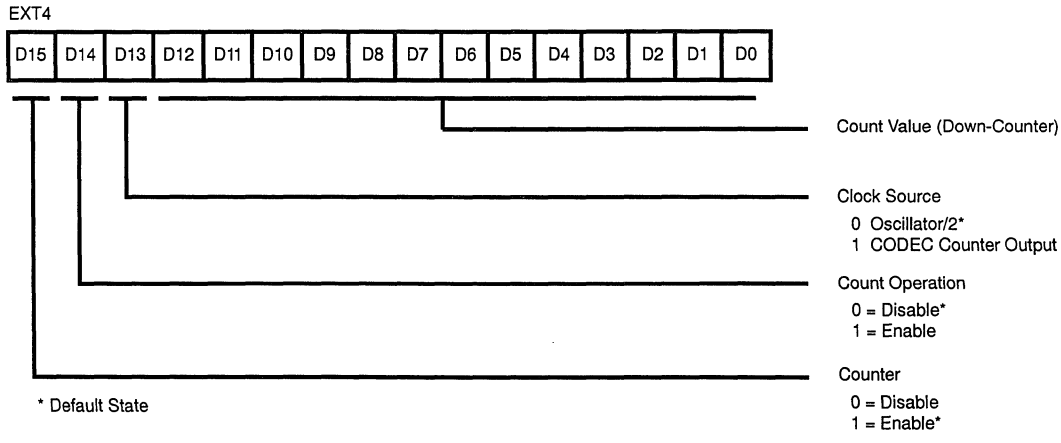


Figure 15. Timer Register

OPERATION

Disabling Peripherals

Disabling a properly (CODEC Interface, Counter) provides a general-purpose use of the EXT address pertaining to the specific peripheral. If the peripheral is not disabled, the EXT control signals and EXT data are still provided but transfer of data on the EXT pins is not available (since internal transfers are being processes on the internal bus). Care must be taken to ensure that control of the EXT bus does not provide bus conflicts.

Accessing the CODEC Interface Registers

EXT5, EXT6 AND EXT7 host double buffered registers. External serial CODEC data is transferred from pin RxD to the Z87010 CODEC interface registers EXT5-2. At the same time, the data present in EXT5-2 is serially transferred to the external CODEC through pin TxD.

Writing a new data word to EXT5 loads that data word to EXT5-2 and transfers the current contents of EXT5-2 to EXT5-1. Reading data from EXT5 reads the contents of EXT5-1. Core must be taken to ensure that EXT5 is not written to while the serial CODEC transfer is taking place. This is achieved by only writing to EXT5 after the CODEC interrupt. This also transfers the CODEC value to EXT5-1 which can be read in software.

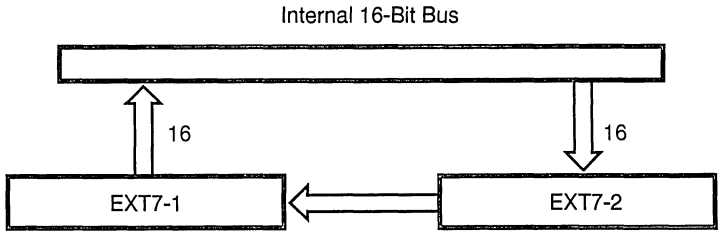
The correct succession of operations is thus

1. Wait for Interrupt
2. Write to EXT5
3. Read from EXT5

The same discussion applies for EXT6.

A similar hardware architecture is used for EXT7. Writing to EXT7 loads the register EXT7-2 and transfers the previous contents of EXT7-2 to EXT7-1. Reading from EXT7 returns the contents of EXT7-1.

In order to load both registers, two successive load operations to EXT7 are required: first with the contents of EXT7-1 then with the contents of EXT7-2. (See Figure 16).



EXT7-1 CODEC Timer Register
EXT7-2 Wait-State Register

Figure 16. EXT7 Register Configuration

1

5

Z87100 PN Modulator Wireless Transmitter 3

4

5

6

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8

9

Z87100

PN MODULATOR WIRELESS TRANSMITTER

FEATURES

Part	ROM (Kbytes)	RAM* (Bytes)	Package Information
Z87100	1	124	18-pin DIP & SOIC

Note: *General-Purpose

- 3.0V to 5.5V Operating Range
- On-Chip PN Modulator for Spread Spectrum Communications
- ROM-Programmable PN Codes, up to 256 Bits ("Chips")
- Fast Instruction Pointer - 1.0 µs @ 12 MHz
- Two Standby Modes - STOP and HALT
- 12 Input/Output Lines (One with Comparator Input)
- Two Programmable 8-Bit Counter/Timers
- 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts (Two External, One Software Generated)
- Maximum Clock Speed of 12 MHz
- Watch-Dog/Power-On Reset Timer
- Analog Comparator with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a RC, or External Clock Drive
- Low EMI Noise Mode
- 0° to +70°C Ultra-Low Power Operation at 10 kHz

GENERAL DESCRIPTION

The Z87100 Wireless Controller is a member of the Z8® single-chip microcontroller family and is manufactured in CMOS technology. Zilog's CMOS Z87100 microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z87100 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The Z87100 offers a flexible I/O scheme and a number of ancillary features that are useful in many consumer, industrial, automotive, and advanced scientific applications.

The Z87100 is designed with specific features for wireless spread spectrum applications using direct sequence pseudo-noise (PN) modulation. With up to 256 bits ("chips") of specially designated "PN ROM", one or more PN code sequences may be stored and used to PN-modulate data generated by the Z87100. PN modulation is synchronous with the data, using an integer number of PN chips per data bit.

The Z87100 features an Internal Time Base Counter which provides a real time clock for Stop-Mode Recovery or interrupt at programmable intervals of 0.25 seconds, one second, one minute and one hour. This requires an external clock oscillator signal at 32.768 kHz.

Special PN modulator control registers allow the user to select the desired PN modulator outputs, to choose the PN clock source and PN sequence start address in PN ROM, to stop/start and enable/disable the PN modulator, and to determine whether a complete PN code sequence is modulated against a single bit or an integer fraction or multiple of a single bit. The PN-modulated data may then be used

GENERAL DESCRIPTION (Continued)

with an external modulator and RF section to form a complete wireless spread spectrum transmitter.

The device's many applications demand powerful I/O capabilities. The Wireless Controller fulfills this with 12 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of General-Purpose Registers, two I/O Port registers and fifteen Control and Status registers. The Expanded Register File consists of two port registers, four control registers and six PN modulator registers.

With powerful peripheral features such as on-board comparators, counter/timers, Watch-Dog Timer, and PN modulator, the Z87100 meets the needs for most sophisticated wireless and low-power controller applications (Figure 1).

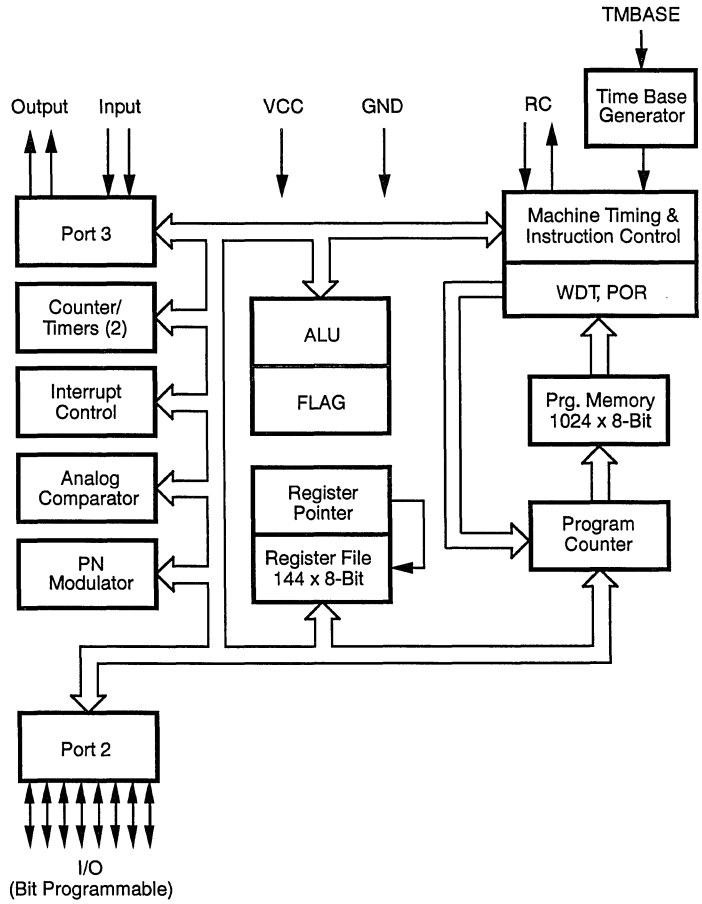


Figure 1. Functional Block Diagram

PIN DESCRIPTION

Table 1. 18-Pin DIP/SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	Input
6	RC2	RC Oscillator Clock	Output
7	RC1	RC Oscillator Clock	Input
8-9	P31, P33	Port 3, Pins 1, 3	Fixed Input
10	TMBASE	Time Base Clock	Input
11	GND	Ground	Input
12-13	P35-36	Port 3, Pins 5, 6	Fixed Output
14	GND	Ground	Input
15-18	P20-23	Port 2, Pins 0, 1, 2, 3	In/Output

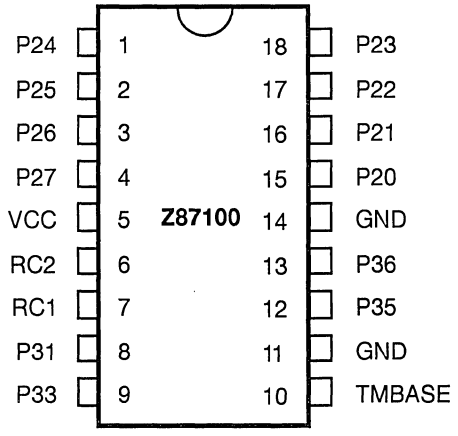


Figure 2. 18-Pin DIP/SOIC Pin Configuration

ABSOLUTE MAXIMUM RATING

Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†		C

Notes:
1. *Voltage on all pins with respect to GND.
2. † See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 3).

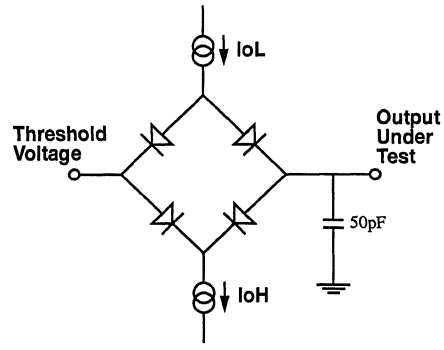


Figure 3. Test Load Configuration

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}	T_A= 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.0V		12		V	$I_{IN} \leq 250\ \mu A$	
		5.5V		12		V	$I_{IN} \leq 250\ \mu A$	
V_{CH}	Clock Input High Voltage	3.0V	0.9 V_{CC}	V_{CC} +0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC} +0.3	3.9	V		
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS} –0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.5V	V_{SS} –0.3	0.2 V_{CC}	2.7	V		
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS} –0.3	0.2 V_{CC}	1.0	V		
		5.5V	V_{SS} –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC} –0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC} –0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I_{OL}=+4.0 mA	
		5.5V		0.4	0.1	V	I_{OL}=+4.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0	0.4	V	I_{OL}= 6 mA, 3 Pin Max	
		5.5V		1.0	0.5	V	I_O = +12 mA, 3 Pin Max	
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	3.0V	–1.0	1.0		µA	V_{IN} = O_V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = O_V, V_{CC}	

3

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}	T_A= 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	$V_{IN} = O_V$, V_{CC}	
		5.5V	–1.0	1.0		µA	$V_{IN} = O_V$, V_{CC}	
I_{CC}	Supply Current	3.0V		8.0	4.5	mA	@ 12 MHz	2,3
		5.5V		15	9.0	mA	@ 12 MHz	2,3
		4.5V		15	10	µA	10 kHz; external RC	2,3
I_{CC1}	Standby Current (HALT mode)	3.0V		4.5	2.0	mA	HALT mode V_{IN}=0_V, V_{CC} @12 MHz	2,3
		5.5V		7.0	4.0	mA		
							HALT mode V_{IN}=0V, V_{CC} @ 12 MHz	2,3
		3.0V		2.0	1.0	mA	Clock Divide-by-16 @12 MHz	2,3
		5.5V		4.5	2.5	mA		
							Clock Divide-by-16 @ 12 MHz	2,3
I_{CC2}	Standby Current (STOP mode)	3.0V		10	1.0	µA	STOP mode $V_{IN} = O_V$, V_{CC} WDT is not Running	4,7
		5.5V		10	3.0	µA		
							STOP mode $V_{IN} = O_V$, V_{CC} WDT is not Running	4,7
		3.0V		TBD	160	µA	STOP mode $V_{IN} = O_V$, V_{CC} WDT is Running	4,7
		5.5V		TBD	200	µA		
							STOP mode $V_{IN} = O_V$, V_{CC} WDT is Running	4,7
		5.5V		12	5	µA	STOP mode; TMBASE=32.768 kHz; WDT is not Running	6,7
T_{POR}	Power-On Reset	3.0V	7	24	13	ms		
		5.5V	3	13	7	ms		
V_{LV}	V_{CC} Low Voltage		1.50	2.65	2.1	V	2 MHz max Ext. CLK Freq.	1

Notes:

1. V_{LV} increases as the temperature decreases.
2. All outputs unloaded, I/O pins floating, inputs at either rail, TMBASE clock input grounded.
3. $C_{L1} = C_{L2} = 100$ pF
4. Same as note 2 except inputs at V_{CC}.
5. Low EMI oscillator selected; SCLK = RC1/2;
   10 kHz external oscillator with the comparator not enabled 10 µA.
   10 kHz external oscillator with the comparator enabled 310 µA
   RC selected for WDT; 10 kHz RC oscillator
   (corresponding to R = 1.2MΩ C~ 68 pF), comparator is off.
6. Z8 in STOP moderate off; Z8 in STOP mode; WDT off.
   TMBASE selected; as Z8 system clock source
   Time base counter enabled; V_{CC} = 5.5V.
7. Analog Comparator disabled

AC ELECTRICAL CHARACTERISTICS

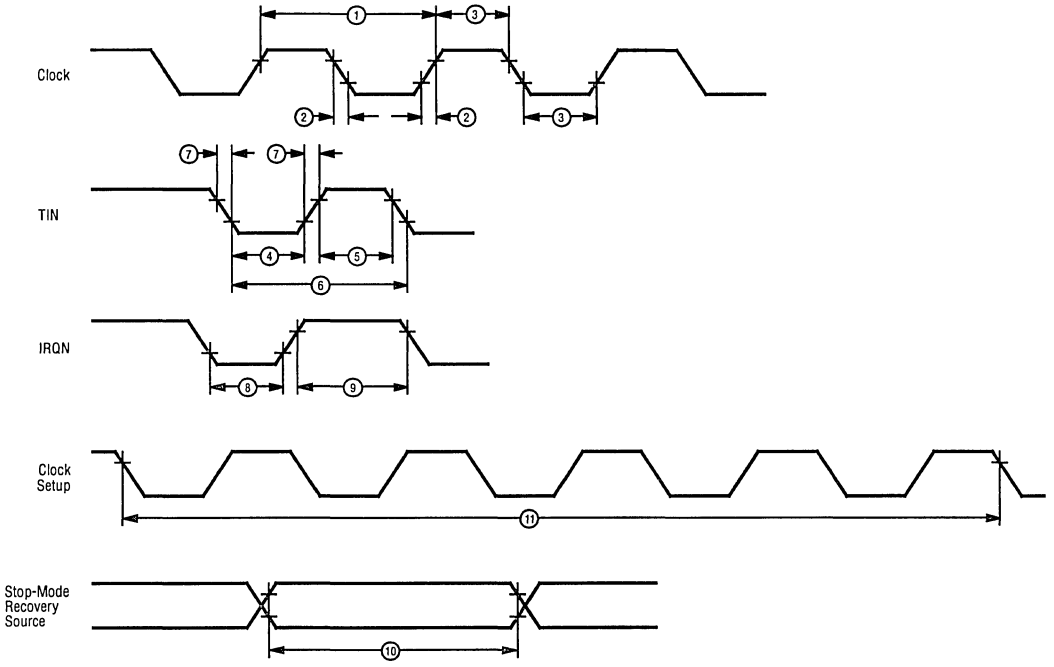


Figure 4. Additional Timing

AC ELECTRICAL CHARACTERISTICS

				T_A=0°C to +70°C 12 MHz			
No	**Sym**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.3V	83	100,000	ns	1
			5.0V	83	100,000	ns	1
2	TrC,TfC	Clock Input Rise	3.3V		15	ns	1
		and Fall Times	5.0V		15	ns	1
3	TwC	Input Clock Width	3.3V	26		ns	1
			5.0V	26		ns	1
4	TwTinL	Timer Input	3.3V	100		ns	1
		Low Width	5.0V	70		ns	1
5	TwTinH	Timer Input	3.3V	3TpC			1
		High Width	5.0V	3TpC			1
6	TpTi	Timer Input Period	3.3V	8TpC			1
			5.0V	8TpC			1
7	TrTin,	Timer Input Rise	3.3V		100	ns	1
	TtTin	and Fall Timer	5.0V		100	ns	1
8	TwIL	Int. Request	3.3V	100		ns	1,2
		Low Time	5.0V	70		ns	1,2
9	TwIH	Int. Request High	3.3V	3TpC			1,2
		Time	5.0V	3TpC			1,2
10	Twsm	Stop-Mode	3.3V	12		ns	
		Recovery	5.0V	12		ns	
		Width Spec					
11	Tost	RC Oscillator	3.3V		5TpC	ms	Reg.4
		Start-up Time	5.0V		5TpC	ms	
	Twdt	Watch-Dog Timer	3.3V	15		ms	D0=0 5
		Refresh Time	5.0V	5		ms	D1=05
			3.3V	30		ms	D0=15
			5.0V	16		ms	D1=05
			3.3V	60		ms	D0=05
			5.0V	25		ms	D1=15
			3.3V	250		ms	D0=15
			5.0V	120		ms	D1=15

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. 5.0V ±0.5V, 3.3V ±0.3V
4. SMR-D5 = 0
5. WDT Oscillator only.

PIN FUNCTIONS

RC1 (RC Oscillator input). This pin connects an external RC network or an external single-phase clock to the on-chip RC oscillator.

RC2 (RC Oscillator output). This pin connects an external RC network to the on-chip RC oscillator.

TMBASE (Time Base Counter Clock Input). This pin connects an external 32 kHz clock signal to the input of an on-chip Time Base Counter.

As a mask option, the Z87100 can be configured to initialize ("cold start") using either RC or TMBASE. Consequently, the Z87100 can be operated with either or both RC and TMBASE clock sources.

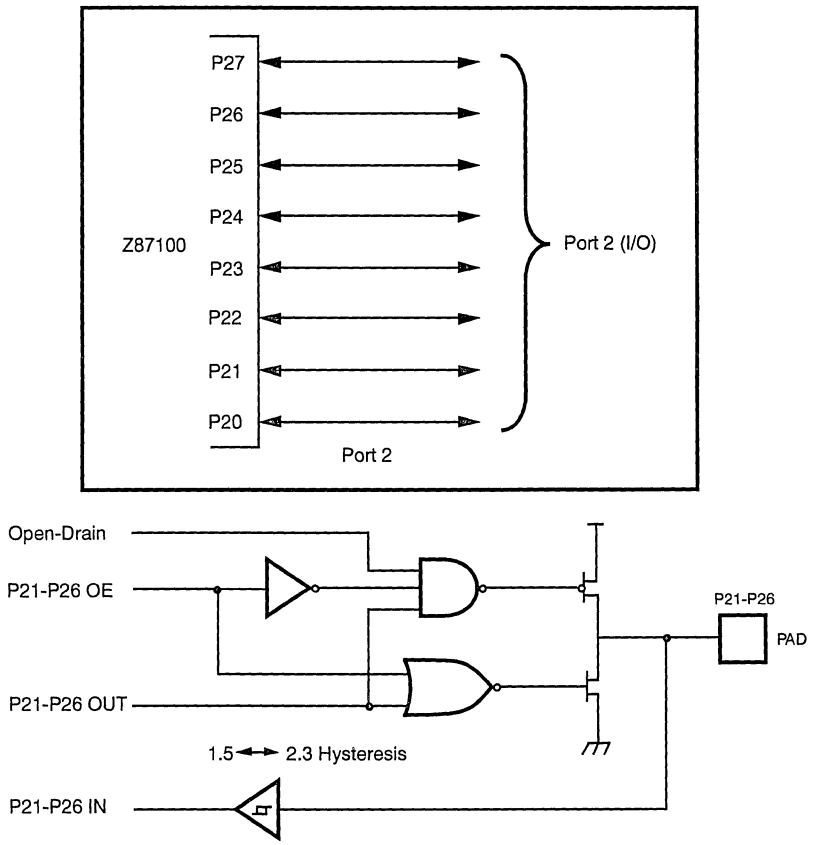


Figure 5. Port 2 Configuration (P21-P26)

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These 8 I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Pins programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 6). In addition, when the PN modulator is enabled, and the appropriate pins are programmed as outputs, P20 may be programmed as the unspread data-out from the PN modulator. To provide a monitor of this unspread data signal, P27 may similarly be programmed as the data clock output.

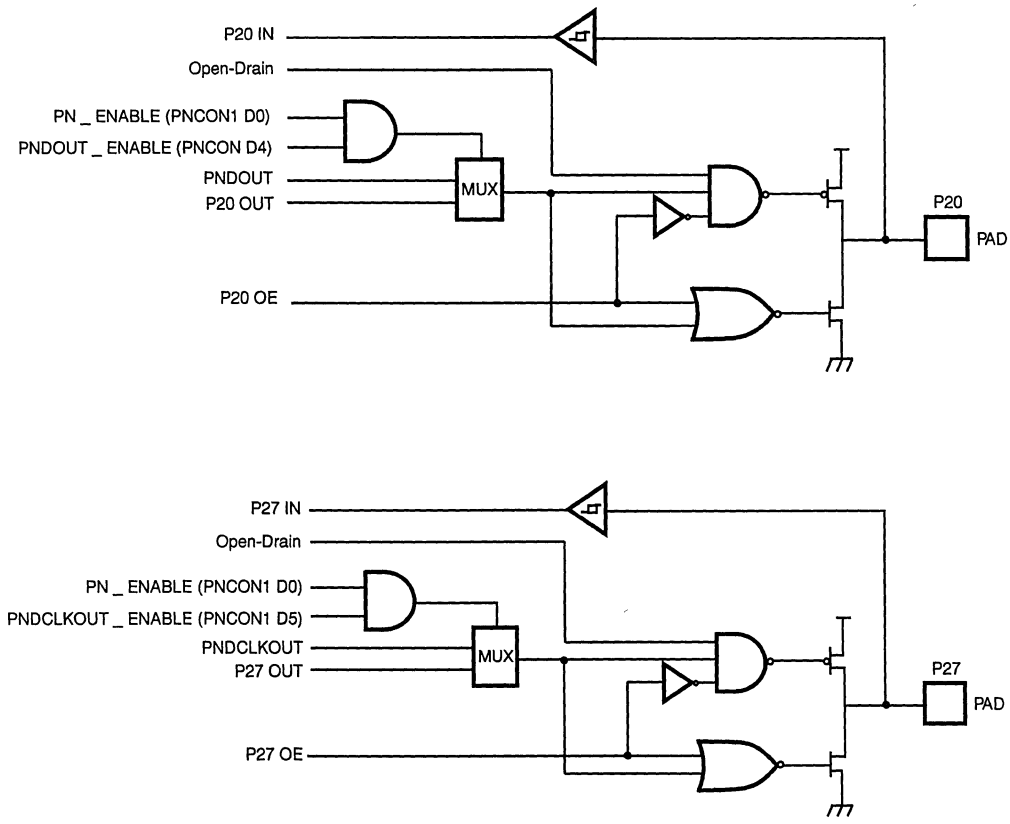


Figure 6. Port 2 Configuration (P20-P27)

Port 3 (P36-P31). Port 3 is a 4-bit, CMOS-compatible port. These four lines consist of two fixed inputs (P31, P33) and two fixed outputs (P36-P35). P31 and P33 are standard CMOS inputs (no auto latch) and P35 and P36 are push-pull outputs. An on-board comparator can process analog signals on P31 with reference to the voltage on P33, where this analog function is enabled by programming Port 3 Mode Register (bit 1). P31 is programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).

When the PN modulator is enabled, P35 is automatically configured as the output for the PN spread data, and, if desired, P36 may be programmed as the PN clock output (Figures 7 and 8).

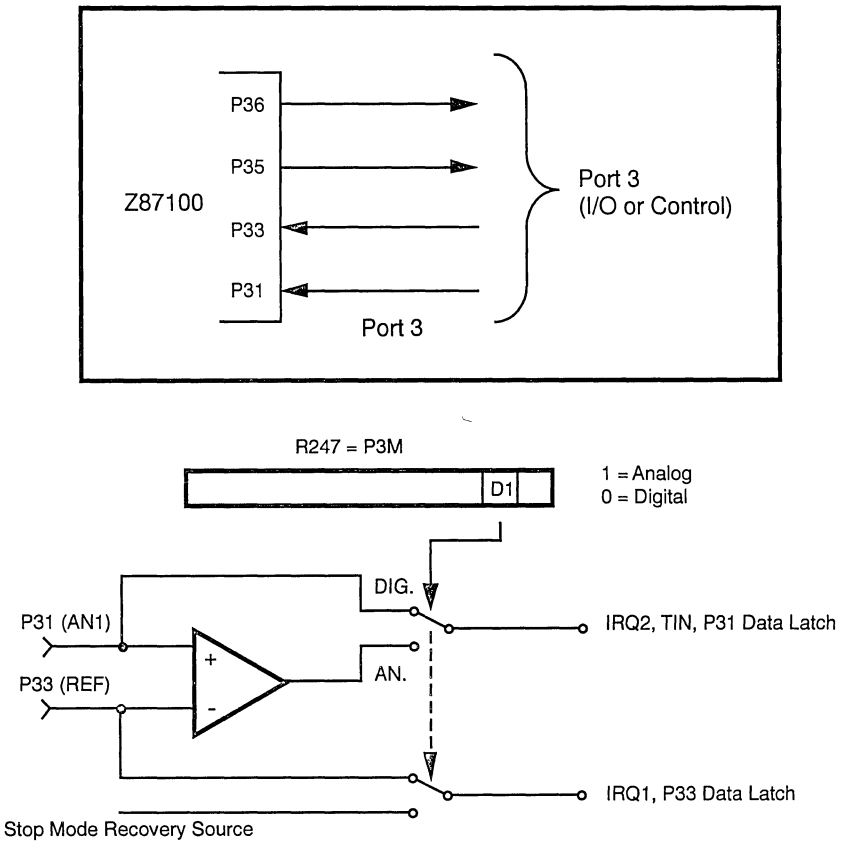


Figure 7. Port 3 Configuration (P31, P33)

PIN FUNCTIONS (Continued)

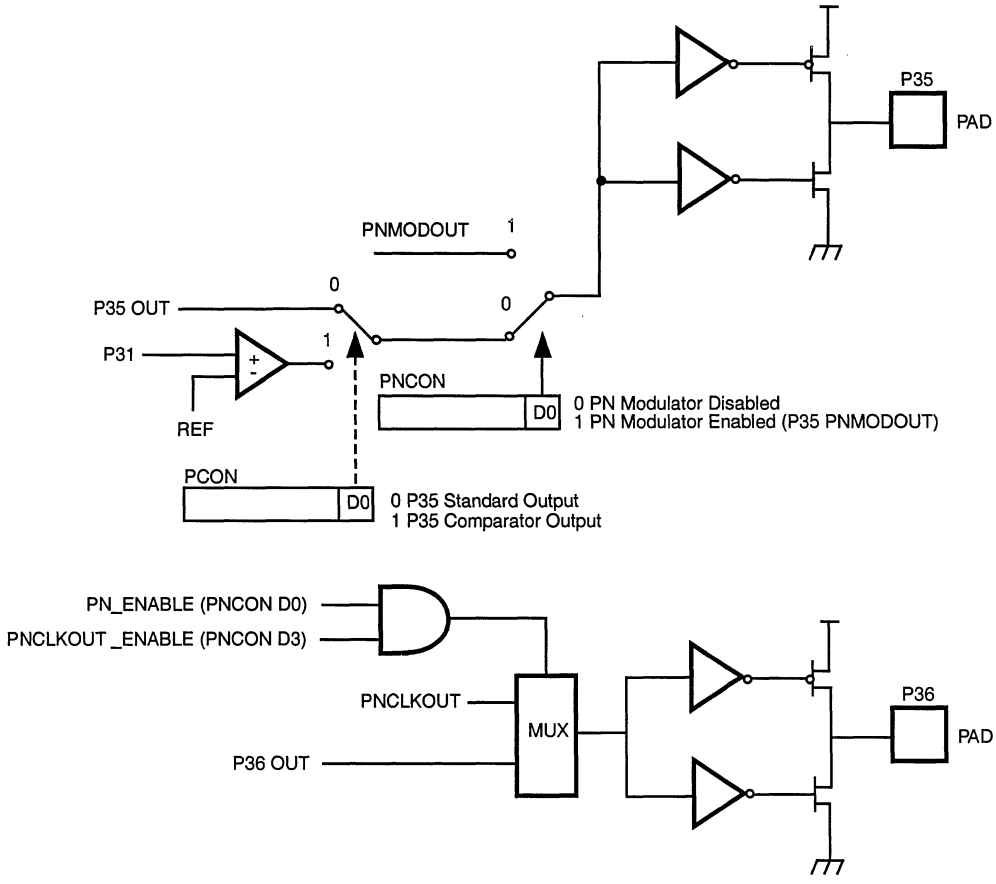


Figure 8. Port 3 Configuration (P35,P36)

PORT Configuration Register (PCON). The PORT Configuration Register (PCON) configures the ports to support comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 7). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator output to P35 (Figure 9), and a 0 releases the port to its standard I/O configuration. Bits 5 and 6 of this register configure ports 2 and 3, respectively, for low EMI operation. A 1 in these locations configures the corresponding port for standard operation, and a 0 configures the port for low EMI operation. Finally, bit 7 of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive.

Low EMI Option. The Z87100 can be programmed to operate in a low EMI emission mode by the PCON register. The RC oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- Less than 1 mA current consumption during the HALT mode.
- The pre-drivers slew rate reduced to10 ns typical.
- Low EMI output drivers have resistance of 200 ohms (typical).
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz (250 ns cycle time).

With bit 7 of the PCON register, the gain of the RC oscillator may be selected: standard gain is intended for high performance, high speed circuits, while the low gain option is intended for low speed, low EMI, and low current consumption applications.

Comparator Inputs. Port 3, P31 has a comparator front end where the comparator reference voltage is provided by P33. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 are connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a P33 register input or IRQ1 source (Figure 9).

When P3M is programmed for analog inputs on port 3 (Bit D1=1) that power to the comparator is on and the current used is 300 µA if V_{REF} is V_{CC}, and , 50 µA if V_{REF} is V_{DD}. When comparator is digital (Bit D1=0) the comparator is off.

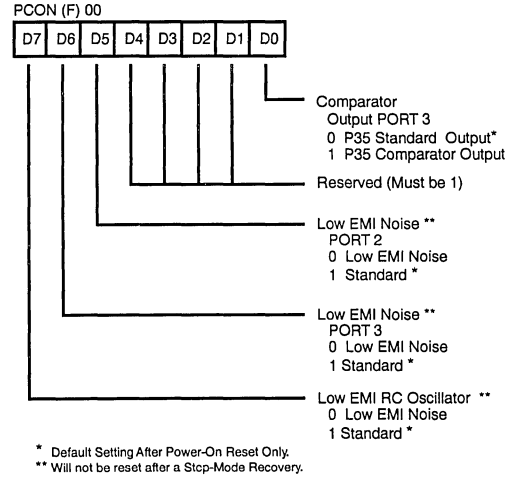


Figure 9. PORT Configuration Register (PCON)

FUNCTIONAL DESCRIPTION

The Z8® Wireless Controller incorporates special functions to enhance the Z8's application in consumer, automotive, industrial, scientific research, and advanced technology applications.

RESET. The device can be reset through one of the following mechanisms:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. The Z87100 can address up to 1 Kbytes of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 1023 consists of on-chip, mask-programmed ROM.

ROM Protect. The 1 Kbytes of Program Memory are mask programmable. A ROM protect feature will prevent "dumping" of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 11). Three system configuration registers reside in the Expanded Register File address space in Bank F, while six PN modulator registers reside in Bank C. The rest of the Expanded Register addressing space is not physically implemented and is open for future expansion. To write to the ERF, the upper nibble of the RP must be zero. To write to the rest of the register file, the lower nibble must be zero.

Antiheroine using Zilog's cross assembler Version 2.1 or earlier, use theLD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

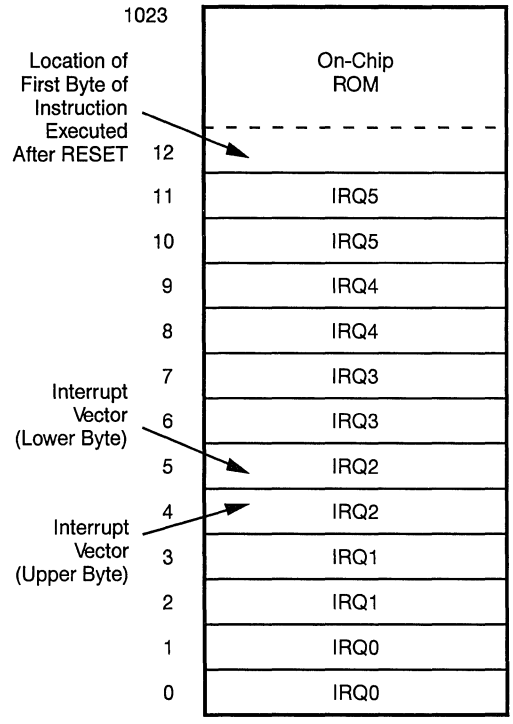


Figure 10. Program Memory Map

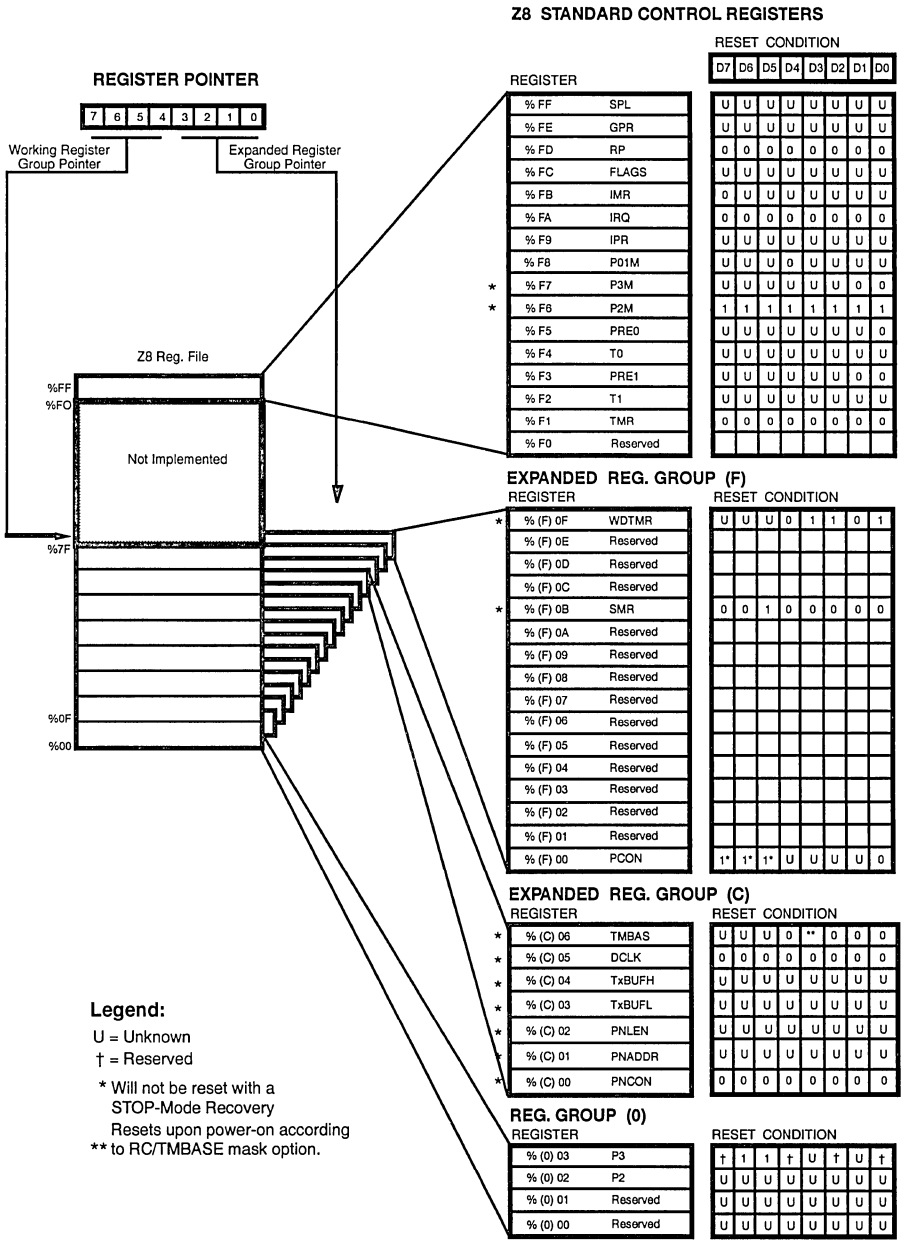


Figure 11. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

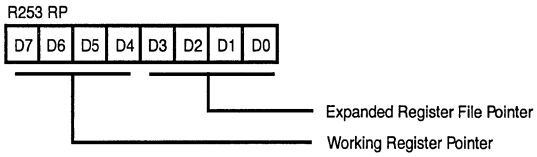


Figure 12. Register Pointer

Register File. The Register File consists of two I/O port registers, 124 general-purpose registers, 15 control and status registers, and ten system configuration registers in the Expanded Register Group, including six registers in support of the PN modulator. The instructions can access registers directly or indirectly through an 8-bit address field, allowing use of a short 4-bit register address with the Register Pointer. In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Caution: D4 of Control Register P01M (R248) must be 0. If the Z87100 is emulated by Z86C90, D4 of P01M has to change to 0 before submission to ROM code.

GPR. The Z87100 has one extra general-purpose register located at %FE(R254).

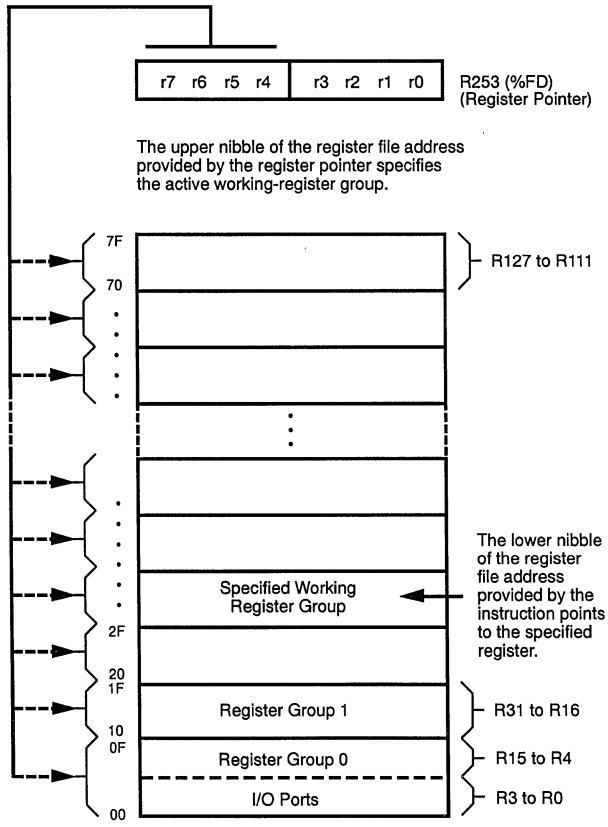


Figure 13. Register Pointer

Stack. The Z87100 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 14).

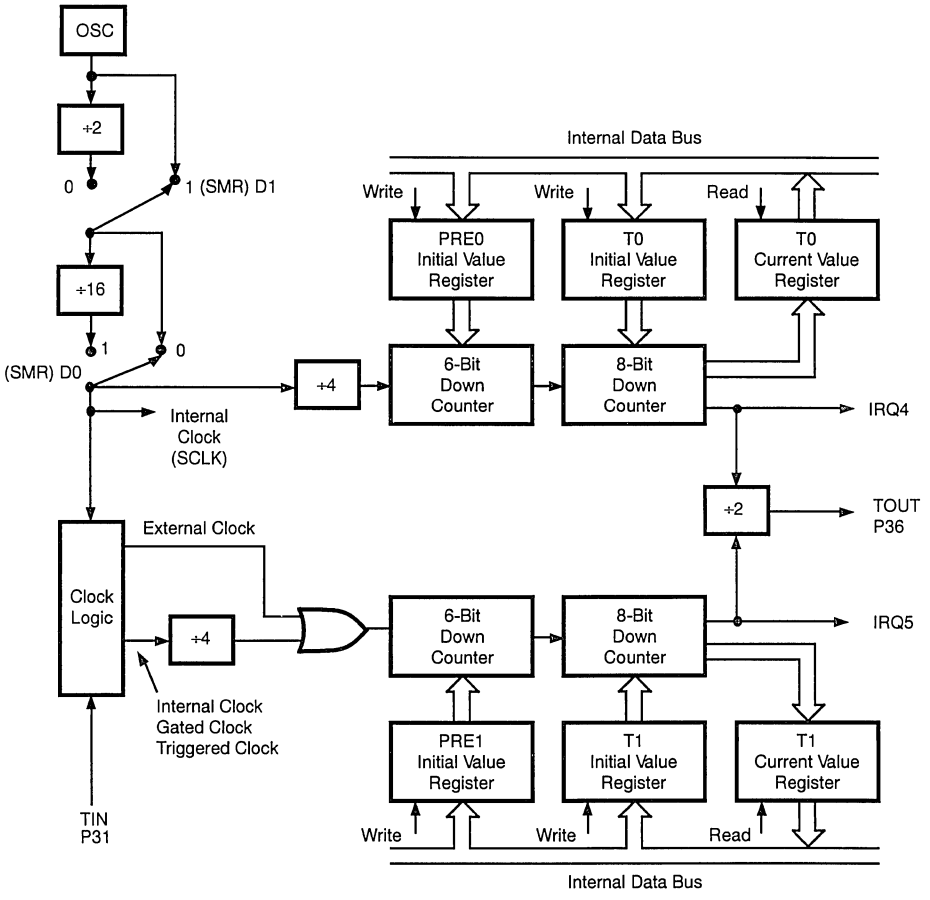


Figure 14. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The 6-bit Prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the Prescaler, may be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z87100 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 15). The six sources are divided as follows; two sources are claimed by Port 3 lines P31 and P33, two sources in the counter/timers, one source for the PN modulator and one source for the time base generator. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

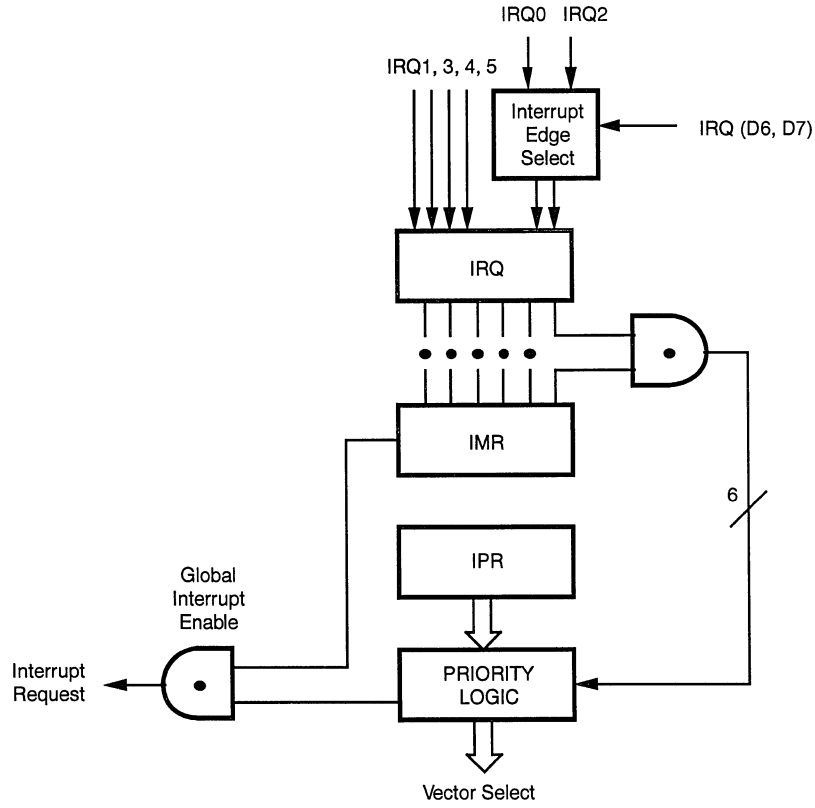


Figure 15. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	Time Base	0, 1	Internal, Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	IRQ2, TIN	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	Software/PN Modulator	6, 7	Software Generated/Internal*
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

Notes:
*When the PN Modulator is enabled, IRQ3 is an internal interrupt.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z87100 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs services. When the PN modulator is disabled, IRQ3 has no hardware source but can be invoked by software by setting bit D3 of the IRQ register to 1. When the PN modulator is enabled, an interrupt will be mapped to IRQ3 after the contents of the PN modulator's data hold register have been loaded into the modulator's data shift register.

An interrupt resulting from AN1 (P31) is mapped into IRQ2, and an interrupt from the time base generator is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both-edge triggered, and are programmable by the user. The software can poll to identify the state of the pin. For IRQ0 and the time base generator, selection of the trigger edge is not critical but should not be changed once selected.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ0 and IRQ2 Interrupt Edge Programming

IRQ Register D7	IRQ Register D6	P31	Interrupt Edge Time Base
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z87100 derives its timing from an on-board RC oscillator referenced as RC or an external clock source applied to the time base counter input referenced as TMBASE. The RC clock source is made of an internal oscillator and an external resistor and an optional external capacitor (See Figure 14).

The 2 terminals that are part of the RC oscillator are referenced as RC1 and RC2. The frequency of the clock signal generated by the RC oscillator cannot exceed 6 MHz. RC1 can also be driven by an external clock source, while RC2 remains unconnected. In this configuration the Z87100 can be clocked up to 12 MHz, when not in Low EMI mode. (4 MHz in Low EMI mode).

Both clock sources, RC and TMBASE, can be selected to drive the internal Z8 system clock, depending on the setting of a mask-programmed option bit.

The TMBASE clock input requires a 32.768 kHz clock signal when the TMBASE is enabled or when the TMBASE is selected to be the default oscillator. As a special feature of the Z87100, ICC current consumption is significantly reduced at a clock frequency of 10 kHz in low EMI noise mode.

FUNCTIONAL DESCRIPTION (Continued)

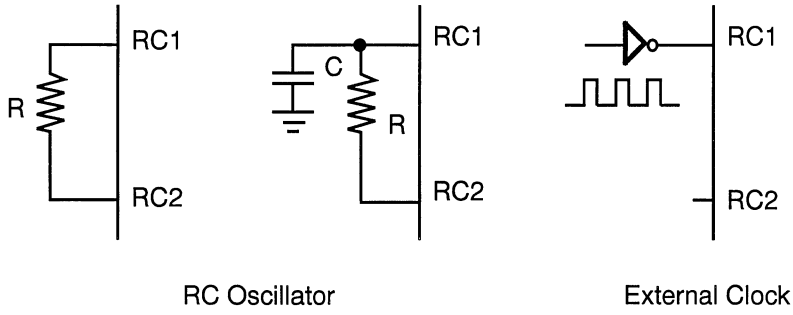


Figure 16. RC Oscillator Configuration

Table 4. Maximum Clock Value in Different Modes

	Standard Mode SCLK=RC1/2	Standard Mode SCLK=RC1	Low EMI SCLK= RC1/2	Low EMI SCLK=RC1
Ext Clock	12 MHz (SCLK=6 MHz)	6 MHz (SCLK = 6 MHz)	4 MHz (SCLK = 2 MHz)	2 MHz (SCLK = 2 MHz)
RC	6 MHz (SCLK = 3 MHz)	3 MHz (SCLK = 3 MHz)	1 MHz (SCLK = 500 kHz)	500 kHz (SCLK = 500 kHz)

Recovery Timer Circuit. A timer circuit clocked by a dedicated on-board WDT oscillator or by the RC oscillator or TMBASE clock oscillator is used as a recovery timer. The timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The recovery timer circuit is a one-shot timer triggered by one of the three conditions:

- Power Fail to Power OK status
- Stop-Mode Recovery (If D5 of SMR=1)
- WDT Time-Out

The recovery time is a nominal 5 ms using the internal WDT oscillator or, if used with the WDT, 256 clock cycles of the selected externally referenced oscillator. Bit 5 of the Stop Mode Register determines whether the recovery timer is bypassed after Stop-Mode Recovery.

HALT. The HALT instruction turns off the internal CPU clock but not the selected RC oscillator or TMBASE clock. The counter/timers and external interrupts IRQ0 and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. After the interrupt, execution proceeds to the next instruction following the HALT instruction.

STOP. This instruction turns off the internal clock and the RC oscillation and reduces the standby current to 10 µA or less. The STOP mode is terminated by either WDT time-out, POR, or SMR recovery. Either of these events causes the processor to restart the application program at address 000C (HEX). Note that the selected clock source, RC oscillator or TMBASE clock, remains active if bits 3 and 4 of the WDTMR are set. In this mode, only the watch-dog timer runs and the time base generator always remain on.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate sleep instruction; i.e.,

```
FF      NOP; clear the pipeline
6F      STOP; enter STOP mode
or
FF      NOP; clear the pipeline
7F      HALT; enter HALT mode
```

PN Modulator. The Z87100 incorporates a PN modulator to allow generation of a direct sequence spread spectrum data stream. Coupled with the appropriate transmitter circuitry, the Z87100 can support wireless and power line spread spectrum transmission.

The PN modulator of the Z87100 is shown in Figure 15. Major elements of the PN modulator include the PN ROM, the PN modulator control logic, the data hold and data shift registers, and the clock select multiplexor and PN and data clock generator.

As part of the PN modulator, a specially designated area of ROM (PN ROM) provides space for 256 bits ("chips") of one or more pseudorandom noise sequences. The PN modulator control logic accesses the PN ROM as a circular buffer and synchronously exclusive-or's (XORs) each chip of the sequence with the data bits loaded in the PN modulator's data shift register, thereby PN modulating the data. The PN code is accessed from the PN ROM beginning at a specified relative address (PNADDR, register %02 in bank C of the Expanded Register Group) until the chip corresponding to the PN code length (PNLEN, register %03 in bank C of the Expanded Register Group) is reached, at which point access continues again from the specified relative address.

The limits of the PN ROM address space are automatically resolved by the control logic so that the PN ROM is effectively a large circular buffer from which smaller circular buffers defined by PNLEN and PNADDR can be accessed. Operation and control of the circular buffer is transparent to the user. As long as the sum of code lengths is less than or equal to 256 chips, more than one PN sequence may be ROM programmed, with the choice of code or even a concatenation of codes to be used for transmission controlled by Z8 software and the values of PNADDR and PNLEN.

Contents of PN ROM are shifted out and XOR'ed with the contents of the data shift register. The rates at which the two streams are shifted are controlled by the PN and data clocks so that one or more PN chips are XOR'ed against a single data bit, where the number of PN chips is determined by the value of PNLEN. The reference clock for the PN modulator may be selected from the internal system clock (SCLK) or either of the two counter/timers (T0 and T1).

In nominal operation, the PN clock is defined by the selected reference clock, and the data clock is then generated as an integer fraction of the PN clock, where the integer is specified by PNLEN. In this way, each data bit can be synchronously modulated by a full PN code sequence as defined by PNLEN, PNADDR, and the contents of PN ROM. As a practical matter, this type of symbol-synchronous PN modulation allows the corresponding spread spectrum receiver to be designed with improved acquisition performance — since the PN and data modulation are synchronously related at the transmitter, PN acquisition at the receiver can simultaneously establish bit synchronization.

FUNCTIONAL DESCRIPTION (Continued)

While nominal operation assumes that a single PN sequence of PNLEN chips corresponds to a single data bit as described above, the PN modulator additionally supports modes which allow 2 or 4 bits per PN sequence or 2 or 4 PN sequences per bit or an arbitrary relationship between the PN and data clocks. The specific relationship between the selected reference clock, the PN clock, and the data clock then depends upon the values of the PNLEN and DCLK registers.

The Z8 loads the data shift register of the PN modulator by writing to the PN modulator's 16-bit data hold register, TxBUFL and TxBUFH. As the last bit of the data shift register is shifted to be XOR'ed, the PN modulator's control logic loads the contents of the data hold register into the data shift register and triggers interrupt IRQ3. Loading of the next byte of data to TxBUFL and TxBUFH can thus be controlled by Z8 software through interrupts or through polling by using IRQ3.

Initiation of PN modulation is controlled by three control bits in the PNCON and TMBASE control registers: PN_ENABLE,PN_MODULATE,and MODULATE_SELECT.

PN _ENABLE (PNCON D0) enables the PN modulator by providing its circuitry with clock signals and configures IRQ3 and P35 of Port 3.

PN_MODULATE (PNCON D6) initializes the PN ROM address counter to the start of the PN sequence, loads the data shift register with the contents of the data hold register, TxBUFH and TxBUFL, and, depending on the value of MODULATE_SELECT, either begins PN modulation of the data or begins transmission of the unmodulated PN sequence.

MODULATE_SELECT (TMBASE D4) controls whether the contents of the data hold register are clocked out to be PN modulated. If MODULATE_SELECT is set to 0, the contents of PN ROM and the data hold register will then be clocked out to be XOR'ed together; otherwise, if MODULATE_SELECT is set to 1, only the contents of PN ROM will be clocked out.

Typically, one would enable the PN modulator with PN_ENABLE, select the desired PN code sequence from PN ROM using PNLEN and PNADDR, configure the desired PN and data clocks using REF_CLOCK_SELECT, DATA_CLOCK_MODE and DCLK, and select the desired outputs using PNCLKOUT_ENABLE, PNDOUT_ENABLE and PNDCLKOUT_ENABLE. With the first data to be transmitted loaded in the data hold register TxBUFL and TXBUFH, transmission of PN modulated data or just the PN code sequence can then begin under control of PN_MODULATE and MODULATE_SELECT.

PN Modulator I/O. The Z87100 PN modulator outputs and inputs are multiplexed with the pins of Ports 2 and 3 according to Table 4. By enabling the PN modulator with PN_ENABLE (D0 of PN Modulator Control Register 1, PNCON1), the PN-modulated data output, PNMODOUT, is automatically multiplexed to P35. Selection of the other PN modulator outputs, however, requires explicit enabling of the associated control bits in PNCON as well as PN_ENABLE. In that way, as few as one or as many as four I/O pins may be used in operation of the PN modulator, depending upon the application's requirements.

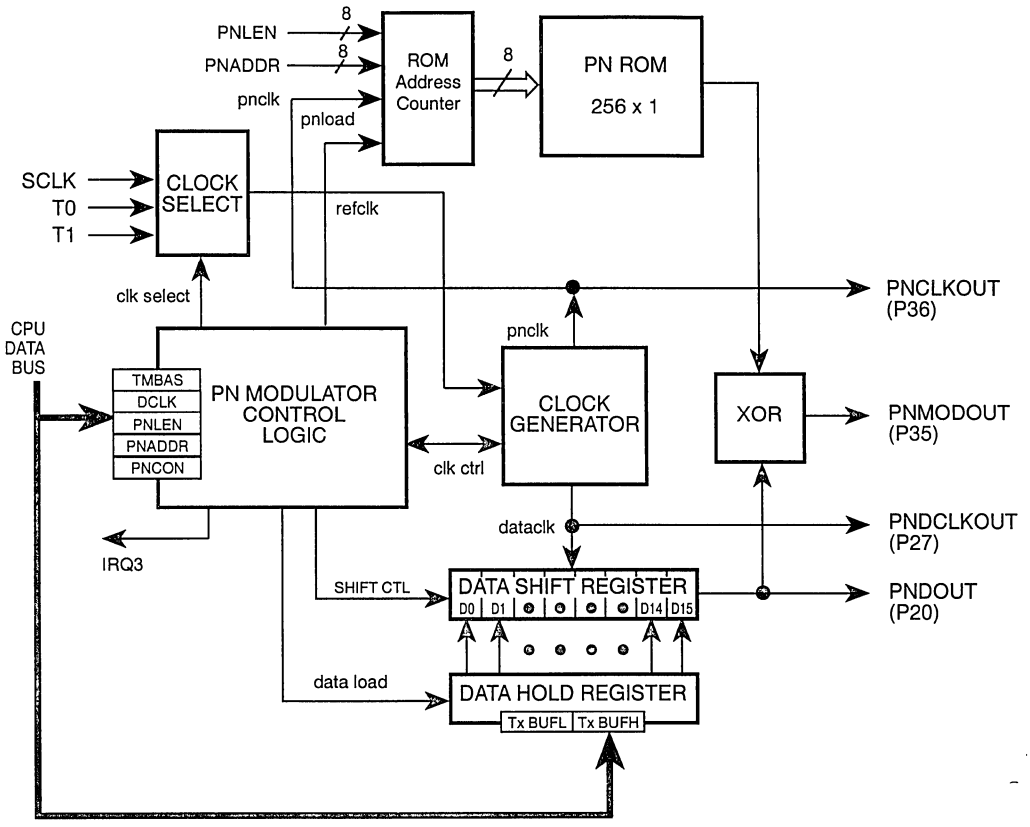


Figure 17. Z87100 PN Modulator Conceptual Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 5. PN Modulator Registers

Pin Name	Location	I/O	Function
PNDOUT	P20	output	unspread data output
PNDCLKOUT	P27	output	data clock output
PNMODOUT	P35	output	PN spread data output
PNCLKOUT	P36	output	PN clock output

PN Modulator Registers

The PN modulator is supported by six read/write registers located in bank (C) of the Expanded Register Group: the PN modulator control register (PNCON) at %(C)00; the PN relative address register (PNADDR) at %(C)01; the PN code length register (PNLEN) at %(C)02; the PN modulator low-byte data hold register (TxBUFL) at %(C)03; the high-byte data hold register (TxBUFH) at %(C)04; and the data clock control register (DCLK) at %(C)05. Internally, the PN modulator also contains the data shift register for the chips and data bits to be XOR'ed.

PNCON

The PN control register, PNCON, shown in Figure 18 and located at %(C)00, controls the operation and configuration of the Z87100's PN modulator. PNCON provides the following control functions:

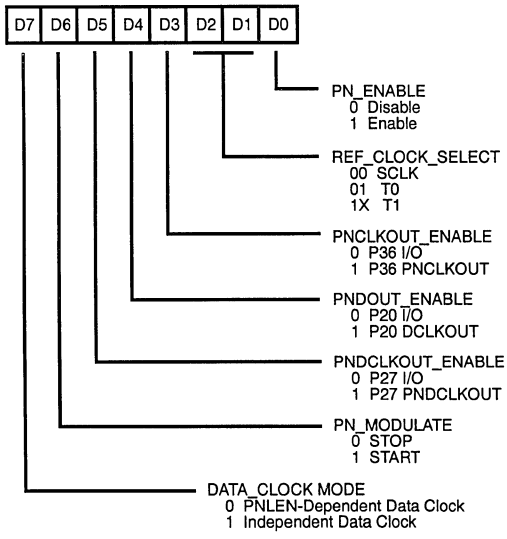


Figure 18. PN Modulator Control Register (PNCON)

PN_ENABLE (PNCON D0) disables or enables the PN modulator. When disabled (PN_ENABLE=0), clock signals to the PN modulator circuitry are discontinued, reducing the overall Z87100 power requirements. When enabled (PN_ENABLE=1), the PN-spread output PNMODOUT is automatically directed to P35 of Port 3 and the pins indicated in Table 4 may, under program control, be selected as indicated.

Enabling the PN modulator further configures interrupt IRQ3 to monitor the status of the PN modulator's data shift register. IRQ3 will initially be cleared (set to 0) but will be set to 1 after the last bit of the data shift register's contents has been PN-modulated and the current contents of TxBUFL and TxBUFH have been automatically transferred to the data shift register. The user then has at most 16 data bit intervals in which to update TxBUFL and TxBUFH.

IRQ3 may be used to control data input to the PN modulator either as an interrupt or as a polled flag, depending on whether the EI instruction has been invoked. As an interrupt, IRQ3 will be automatically cleared as the interrupt is serviced; as a polled flag, IRQ3 must be cleared each time by manually setting bit 3 of the register to 0.

REF_CLOCK_SELECT (PNCON D1:D2) selects which of three sources (SCLK, T0, or T1) is used as the PN clock.

PNCLKOUT_ENABLE (PNCON D3) when enabled (D3=1), selects P36 of Port 3 as the output pin for the PN modulator's PN clock. PN_ENABLE must be set.

PNDOUT_ENABLE (PNCON D4), when enabled (D5=1), selects P20 of Port 2 as the output pin for the unspread data stream. PN_ENABLE must be set, and P20 must be configured as an output pin using P20OE of the P2M Port 2 Mode Register.

PNDCLKOUT_ENABLE (PNCON D5), when enabled (D6=1), selects P27 of Port 2 as the output pin for the unspread data's clock. PN_ENABLE must be set, and P27 must be configured as an output pin using P27OE of the P2M Port 2 Mode Register.

PN_MODULATE (PNCON D6) turns the PN modulation function on and off, starting and stopping its operation once enabled by PN_ENABLE. Setting PN_MODULATE to 1 from 0 loads the data shift register with the current contents of the data hold register, TxBUFL and TxBUFH, and initializes the PN ROM address counter to the start of the PN sequence according to the value set in PNADDR. If MODULATE_SELECT is set to 0, the contents of PN ROM and the data hold register will then be clocked out to be XOR'ed together; otherwise, if MODULATE_SELECT is set to 1, only the contents of PN ROM will be clocked out.

Resetting PN_MODULATE to 0 from 1 stops PN modulation after the current data byte is completely modulated; i.e., after either the high or low byte of the current contents of the 16-bit data shift register is completely modulated. The timing of the command to reset PN_MODULATE must be monitored by the user, based on the number of cycles after IRQ3 was last raised, in order to insure that the desired byte is the last byte transmitted.

When instructed to stop, the contents of TxBUFL and TxBUFH will not be transferred to the data shift register. Setting PN_MODULATE to 1 will then completely reinitiate PN modulation beginning with the PN sequence starting at PNADDR (i.e., the PN sequence will be reset) and with the data word to be modulated as currently stored in the PN modulator's data hold register, TxBUFL and TxBUFH. In effect, the data shift register contents are flushed when PN modulation is stopped.

DATA_CLOCK_MODE (PNCON D7) controls whether the data and PN clocks are integrally related. When DATA_CLOCK_MODE equals 0, the data and PN clocks are integrally related as determined by bits D0, D1, and D2 of register DCLK and the value of PNLEN. When DATA_CLOCK_MODE equals 1, the PN clock is determined by the selected reference clock and PNLEN while the data clock is independently determined by the reference clock and DCLK.

PNADDR

The PN relative address register, PNADDR at %(C)01, indicates the starting address within PN ROM to access the PN sequence to be used in modulation. Addressing is relative, with PNADDR=00H corresponding to the first PN chip contained in PN ROM, PNADDR=FFH corresponding to the last. The value of PNADDR must be set prior to starting operation of the PN modulator; writing to PNADDR while PN modulation is in process will give indeterminate results.

PNLEN

The PN code length register, PNLEN at %(C)02, indicates the number of PN chips to be accessed from PN ROM and modulated against each data bit. If the value of PNLEN plus PNADDR exceeds FFH, the PN modulator's control logic will automatically cycle through PN ROM so that a total of PNLEN chips are utilized. In some modes, the value of PNLEN also determines the data rate, where the PN modulator's data shift register is clocked by an integer multiple or fraction of the selected reference clock divided by PNLEN. The value of PNLEN must be set prior to starting operation of the PN modulator; writing to PNLEN while PN modulation is in process will give indeterminate results.

TxBUFL and TxBUFH

The PN modulator's data hold register, TxBUFL at %(C)03 and TxBUFH at %(C)04, supports the loading of data bytes by the Z8 core for PN modulation. Data loading may be controlled either through software polling or interrupt using IRQ3. The time available to load data depends upon the transmit data rate, itself a function of the speed of the selected reference clock and the value of PNLEN, and, of course, upon the Z87100 clock.

Note that the data shift register is clocked by the dataclk. Data is shifted for PN modulation D15 first, D0 last in terms of the data loaded into TxBUFL and TxBUFH. The data shift register, as opposed to TxBUFL and TxBUFH, is not accessible by the CPU.

DCLK

The data clock control register, DCLK at %(C)05, determines the relationship within the PN modulator among the PN clock controlling the PN shift register (pnclk), the data clock controlling the data shift register (dataclk), and the selected reference clock (SCLK, or one of the two Z8 counter/timers). A conceptual drawing of the PN modulator's timing generator is shown in Figure 17, while Table 5 summarizes the following discussion of the various data clock modes.

When DATA_CLOCK_MODE (PNCON D7) is set to 0, the first three bits of DCLK (D2, D1, D0) establish an integral relationship between the data clock and the PN code sequence.

FUNCTIONAL DESCRIPTION (Continued)

Nominal operation corresponds to DCLK D2=0, D1=0, and D0=0: the PN clock (pnclk) is then equal to the reference clock (refclk), and the data clock is equal to refclk divided by the value of PNLEN. In this way, a complete PN code sequence as defined by PNLEN corresponds to a single data bit. The PN modulator output is thus the PN sequence with its polarity determined by the value of the data bit.

With D2=0, non-zero values of D1 and D0 determine if refclk/PNLEN is further divided by 2D1 D0 to form the data clock. In other words,

pnclk = refclk,

dataclk = pnclk/(PNLEN x 2D1 D0),

As can be seen, a single data bit may correspond to 2, 4,or 8 PN sequences in this mode.

With D2=1, the PN clock is formed by dividing refclk by 4. The values of D1 and D0 then determine the relationship of dataclk to refclk and can allow a single PN sequence to correspond to 2 or 4 data bits:

pnclk = refclk/4,

dataclk = refclk/(PNLEN x 2D1 D0)
or, equivalently,

dataclk = (4/2D1 D0) x pnclk/PNLEN.

When DATA_CLOCK_MODE (PNCON D7) is set to 1, the number of complete PN code sequences per data bit or number of data bits per single PN code sequence is not necessarily an integer. The PN clock is defined by refclk, while the data clock is determined as refclk/DCLK, using all 8 bits of DCLK. Although not likely to be used, DCLK = 00H corresponds to a value of 256. The transition edges of a single chip are still aligned with that of a bit transition, but the PN code cycle is not necessarily synchronous with data transitions.

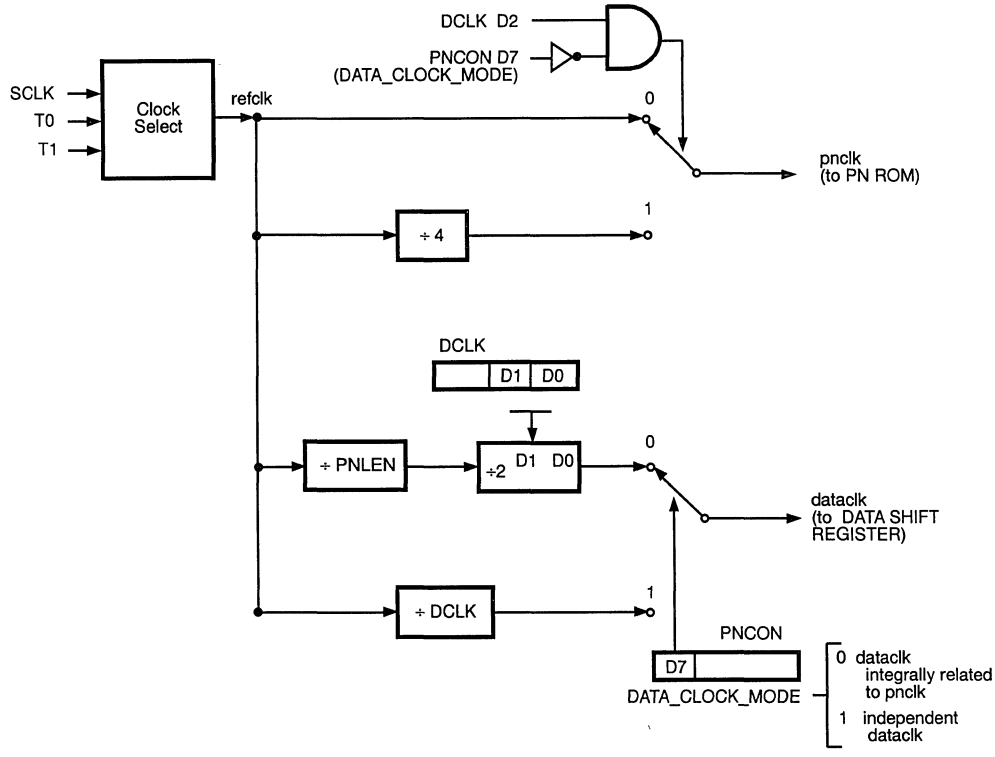


Figure 19. Conceptual Block Diagram of PN Modulator Timing Generator

Table 6. Data and PN Clock Configuration

DATA_CLOCKMODE	DCLK	PNCLK	DATACLK
0	xxxxx000	refclk	pnclk/PNLEN
0	xxxxx001	refclk	pnclk/(PNLENx2)
0	xxxxx010	refclk	pnclk/(PNLENx4)
0	xxxxx011	refclk	pnclk/(PNLENx8)
0	xxxxx100	refclk/4	4xpnclk/PNLEN
0	xxxxx101	refclk/4	2xpnclk/PNLEN
0	xxxxx110	refclk/4	pnclk/PNLEN
0	xxxxx111	refclk/4	pnclk/(PNLENx2)
1	DCLK	refclk	pnclk/DCLK

Time Base Generator. The time base generator can be used while the Z8 is in stop mode to initiate a stop-mode recovery or while the Z8 is operating to generate IRQ0 interrupts as a time-keeping pulse. If used while the Z8 is in stop mode, time-out will trigger a stop-mode recovery ("warm start") and reset the processor to address 000C (hex). Otherwise, time-out of the time base generator will set IRQ0 to 1. This mode can be used while the Z8 continues operation and a regular time base is desired, where IRQ0 can either be polled as a flag and manually cleared by the user or enabled as an interrupt and automatically cleared. The time base generator is programmable and can provide clock signals every .25 seconds, one second, one minute, or one hour, with control of the time base generator provided through the TMBASE register at %(C)06.

TMBASE

The time base generator control register, located at %(C)06 and depicted in Figure 18, allows the time base to be selected and its actions controlled.

TIMEOUT_SELECT. (TMBASE D0-D1) determines the time base. A value of D1=0, D0=0 selects .25 seconds; 01 selects one second; 10 selects one minute; and 11 selects one hour.

If the external time base clock input is not connected to an external clock source, pin 10 should be connected to ground.

TIMEOUT_ENABLE. (TMBASE D2) enables and disables the time base generator. When set to 0, TIMEOUT_ENABLE stops current operation of the time base generator. When set to 1, TIMEOUT_ENABLE resets and starts the time base generator. Reading TIMEOUT_ENABLE provides an indication of the time base generator's status: if set to 0, the time base generator is off; if set to 1, the generator is currently operating.

CLOCK_SELECT. (TMBASE D3) selects either RC or TMBASE as the clock for the Z8. If set to 0, RC will be the clock for the Z87100; if set to 1, TMBASE will be the clock. Determination of which clock is used upon Power-On Reset ("cold start") is mask-programmable, to be selected by the customer at the time ROM code is submitted. Upon a Stop-Mode Recovery warm start, however, the value of this bit (as is true for all the values of this register) is not reset. As a result, a customer could, for example, mask-program the Z87100 to power-up using RC and then, under software control, switch. Depending on the application, operation during the wake cycle could then be conducted using either RC or TMBASE.

FUNCTIONAL DESCRIPTION (Continued)

The time base generator, if mask-optioned, are always on, but RC is off when not selected. When switching from TMBASE to RC, internal circuitry waits for 128 valid clock cycles of TMBASE (4 msec @ 32 kHz) before effecting the switch from TMBASE to RC to insure that RC has stabilized. Internal circuitry also insures that the switch from RC to TMBASE or TMBASE to RC is glitch-free. It is recommended that any command to switch oscillators be followed by a loop that tests the value of CLOCK_SELECT: the value of CLOCK_SELECT will only change when the transition has fully taken place.

MODULATE_SELECT. (TMBASE D4) controls the clocking out of data from the PN modulator's data shift register. If MODULATE_SELECT is set to 0, the contents of PN ROM and the data hold register will be clocked out to be XOR'ed together; otherwise, if MODULATE_SELECT is set to 1, only the contents of PN ROM will be clocked out. Timing of this operation depends on whether the data and PN clocks are integrally related, as determined by DATA_CLOCK_MODE, and whether PN modulation has begun, as determined by PN_MODULATE, as shown in Table 7.

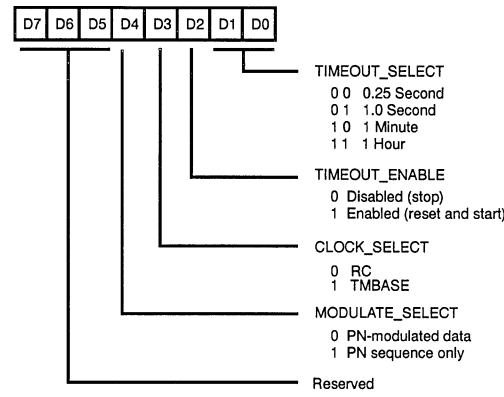


Figure 20. Time Base Generator Control Register

Table 7. PN Modulation Stop/Start Control

PN_MODULATE 0→ 1	
MODULATE_SELECT=0 (PN-Modulated Data)	First data bit and first PN chip of the PN code sequence will be clocked out together at the next edge of the data clock (dclk).
MODULATE_SELECT=1 (PN Sequence Only)	First PN chip of the PN chip sequence will be clocked out at the next edge of the data clock (dclk).
PN_MODULATE=1	
MODULATE_SELECT 1→0 (PN Only → PN + Data)	If DATA_CLOCK_MODE=0 (integer number of PN code sequences per bit), then the first data bit will be clocked out with the next repetition of the first PN chip of the PN code sequence.
	If DATA_CLOCK_MODE=1 (independent PN code sequence length and data bit duration). then the first data bit will be clocked out at the the next edge of the data clock (dclk) together with the ongoing PN sequence.
MODULATE_SELECT 0 →1 (PN + Data → PN Only)	Last data bit will be clocked out with the immediately preceding edge of the data clock (dclk); code sequence output will continue according to the PN clock (pnclk).

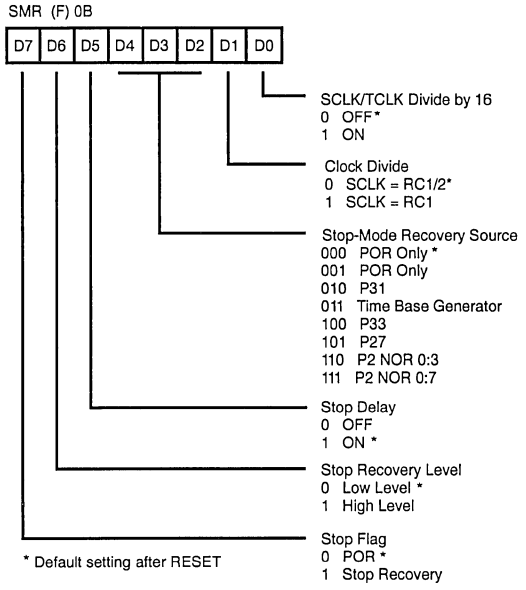


Figure 21. Stop-Mode Register

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 19). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the Stop-Mode Recovery signal. Bit 1 determines whether the selected oscillator, RC or TMBASE, is divided by 1 or 2. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK.

SCLK/TCLK divide-by-16 select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

RC1 Clock divide-by-two (D1). This bit determines whether the RC1 clock is divided by two or one. When this bit is set to 1, the SCLK/TCLK is equal to the RC1 clock. This option can work together with the low EMI options in PCON register to reduce the EMI noise. Maximum clock frequency is 6 MHz when divide-by-one selection is active.

Stop-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 21 and Table 8).

Table 8. Stop-Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only
0	1	0	P31 transition
0	1	1	Time Base Generator
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

P31 and P33 cannot wake up from STOP mode if the input lines are configured as analog inputs.

Stop-Mode Recovery Delay Select (D5). This bit disables the nominal 5 ms RESET delay provided by the recovery timer circuit after Stop-Mode Recovery. The default condition of this bit is 1, enabling the delay. If this bit is 0, the extra delay is disabled, limiting the recovery delay to 18 cycles of RC1.

Stop-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is READ only. When the device enters STOP mode, D7 will be set to 1. D7 will only be reset to 0 to indicate "cold" start if the device is reset by either a Power-On Reset or by a Watch-Dog Timer Reset when the part is in normal operation. Otherwise, if the device is reset by a Watch-Dog Timer Reset when the part is in STOP mode or by any other SMR source, then this bit will continue to be set to 1 to indicate a "warm" start.

Reset Upon Power-On. Upon applying power to the Z87100, an internal reset pulse is generated which triggers the timing recovery circuit illustrated in Figure 22. Power-on reset (POR) behavior is different, however, depending on whether RC or TMBASE has been selected as the clock that drives the Z8®.

When RC is mask-selected to be the Z8 system clock, the recovery counter is clocked by an internal WDT (Watch-Dog Timer) oscillator. The system reset initiated by POR takes 5 ms and guarantees that the RC oscillations are stabilized before the first instruction is executed by the Z8. Subsequently, the recovery counter is used as the Watch-Dog Timer.

When TMBASE is mask-selected to be the default Z8 system clock upon power-on, recovery timing is controlled by the time base generator.

FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and retriggered on subsequent executions of the WDT instruction. The WDT timer circuit is driven by an on-board WDT oscillator or external clock source RC. The WDT does not use TMBASE. The WDT timer clock source is selected with bit 4 of the WDTMR to use either the internal WDT oscillator and a reset delay of 5 ms, or RC1 and a reset delay of 512 RC1 clock cycles. Note that the WDT instruction may affect the zero, sign, and overflow flags.

Bits 0 and 1 control a tap circuit that determines the WDT time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, only the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 23).

The WDTMR register is accessible only during the first 64 processor cycles (128 oscillator clocks) from the execution of the first instruction after Power-On-Reset, Watch Dog Reset or a Stop-Mode Recovery (Figure 22). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH, as shown in Figure 23.

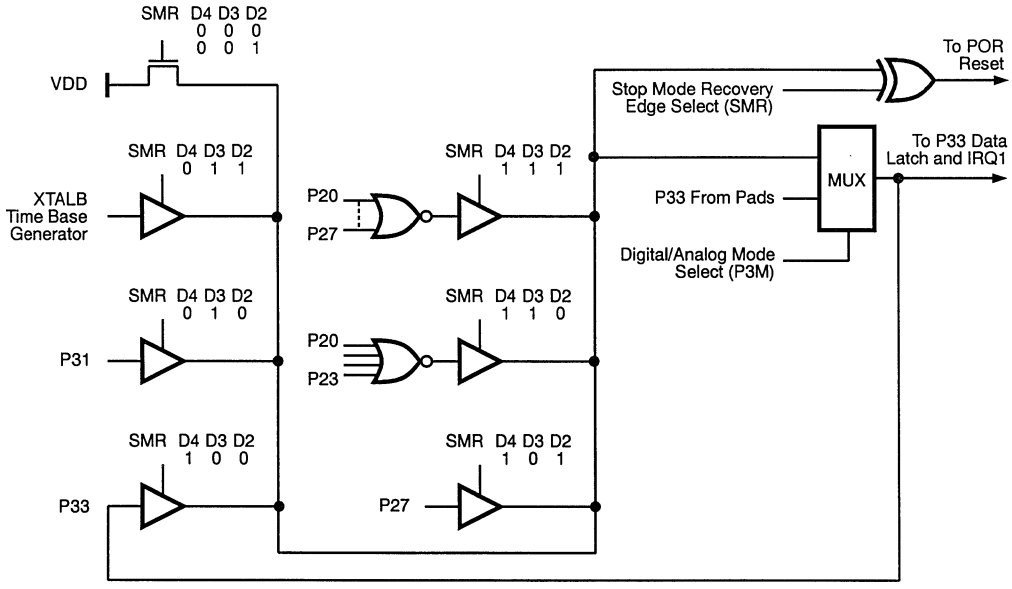


Figure 22. Stop-Mode Recovery Source

Note: The POR, with TMBASE the default Z8 clock source, takes 1.5 seconds the first instruction is executed by the Z8.

WDT Time Select (D1,D0). Selects the WDT time-out period. It is configured as shown in Table 9.

Table 9. WDT Time Select

D1	D0	Time-out of internal WDT OSC	Time-out of RC7 clock
0	0	5 ms min	512TpC
0	1	15 ms min	1024TpC
1	0	25 ms min	2048TpC
1	1	100 ms min	8192TpC

Note: The default on a WDT initiated RESET is 15 ms.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bitdetermines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, then only the WDT is driven by the external clock during STOP mode.

On-Board WDT Oscillator or RC Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal recovery and WDT counter chain. If the bit is a 1, the internal WDT oscillator is bypassed and the recovery and WDT clock source is driven from RC1. The default configuration of this bit is 0, which selects the internal WDT oscillator.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (typically 2.1V).

Low-Voltage Protection (V_{LV}). The low voltage trip voltage (V_{LV}) will be less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{LV}) Conditions:

T_A = 0°, +70°C, Internal Clock Frequency equal or less than 2 MHz

Notes: The internal clock frequency is one half the external clock frequency, unless the device is divide-by-one mode.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low-Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies described above. The device is guaranteed to function normally at supply voltages above the low voltage trip point. The actual low voltage trip point is a function of temperature and process parameters (Figure 23).

ROM Protect. ROM protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. The selection of ROM protect disables the LDC and LDCI instructions.

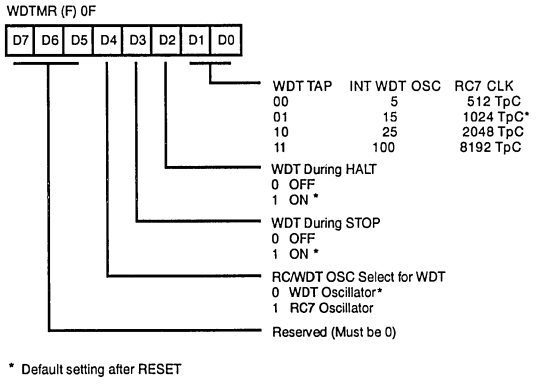


Figure 23. Watch-Dog Timer Mode Register

FUNCTIONAL DESCRIPTION (Continued)

Z87100 Mask Options. The following summarizes the mask options to be selected by the customer at the time of ROM code submittal:

RC/TMBASE

Determine whether "cold start" Initialization: uses RC or TMBASE as base clock.

ROM Protect On/Off: Selects ROM protect.

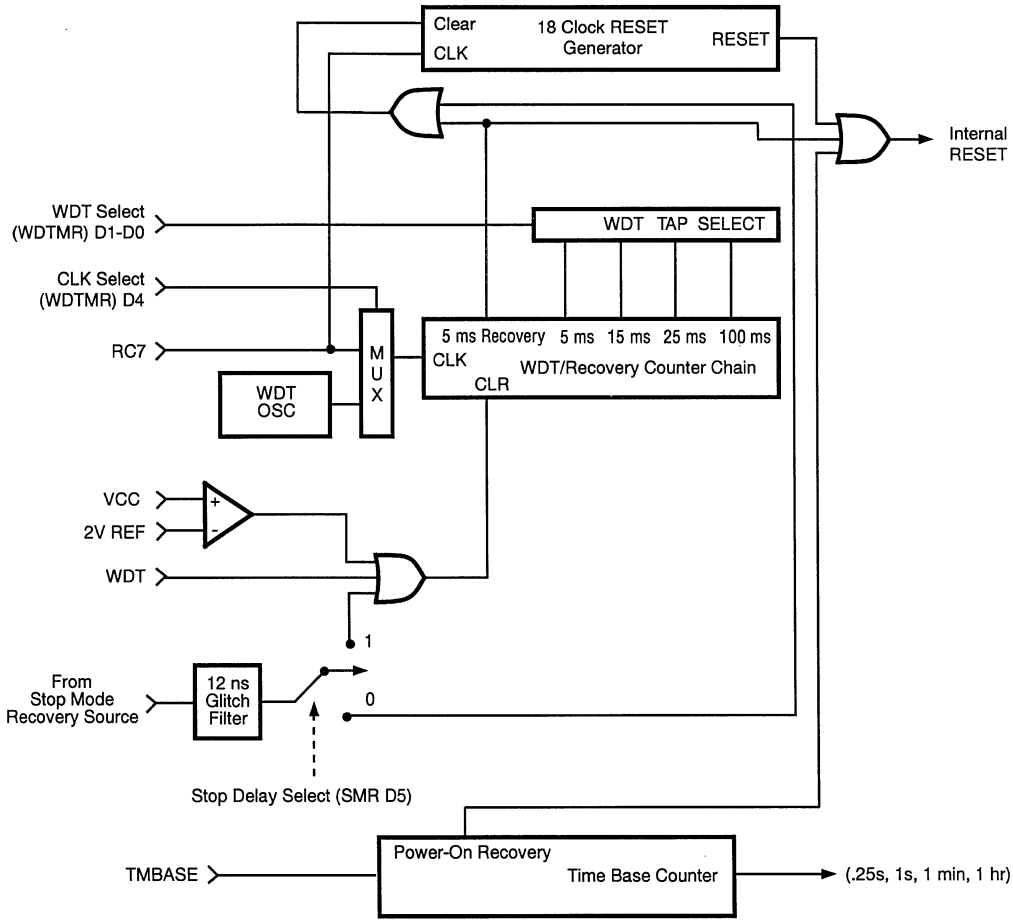


Figure 24. Timing Recovery Circuit (POR, WDT)

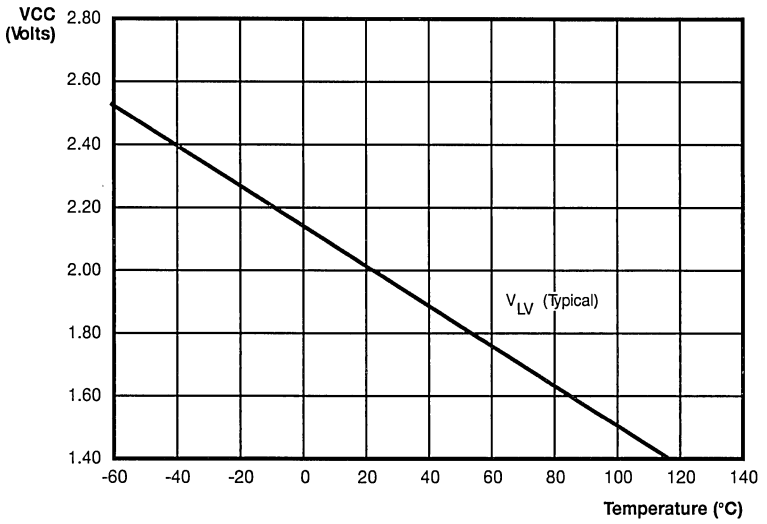


Figure 25. Typical Z87100 V_{LV} Voltage vs Temperature

EXPANDED REGISTER FILE CONTROL REGISTERS

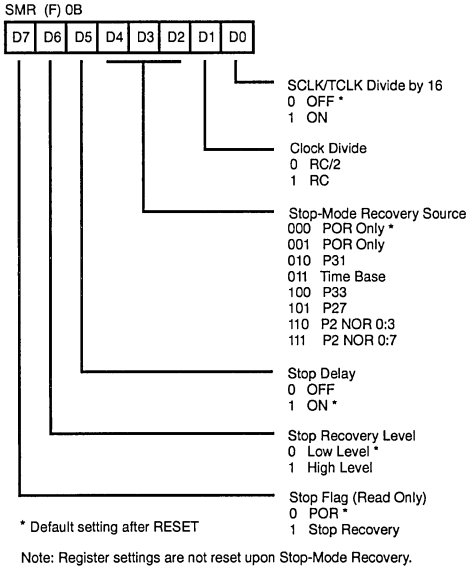


Figure 26. Stop-Mode Recovery Register ((F) 0BH: Write Only)

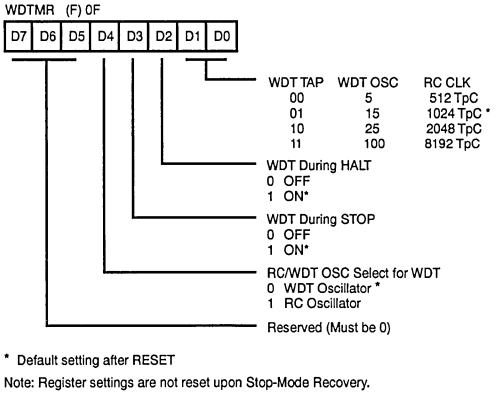


Figure 27. Watch-Dog Timer Mode Register ((F) 0FH: Write Only)

EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)

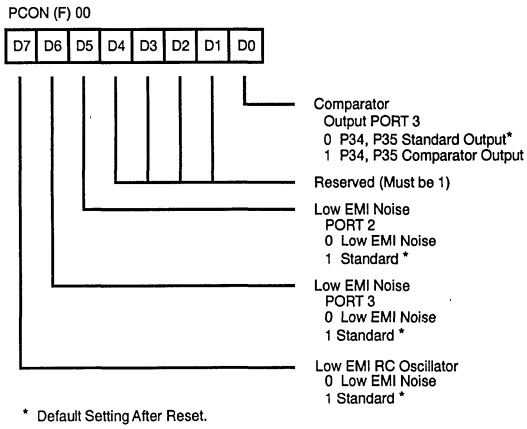


Figure 28. PORT Control Register ((F) 00H: Write Only)

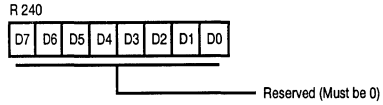


Figure 29. Reserved

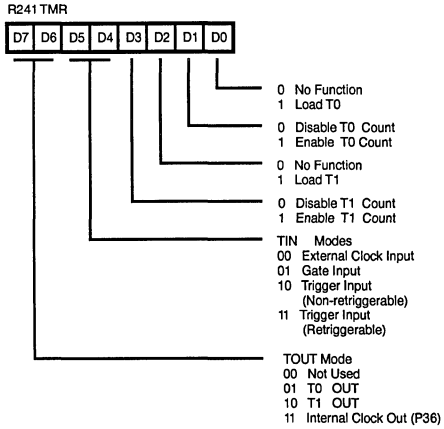


Figure 30. Timer Mode Register (F1H: Read/Write)

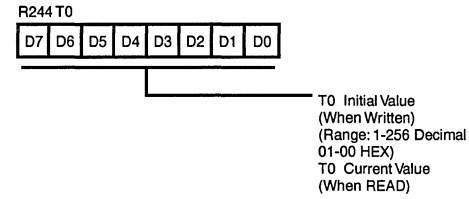


Figure 31. Counter Timer 1 Register (F2H: Read/Write)

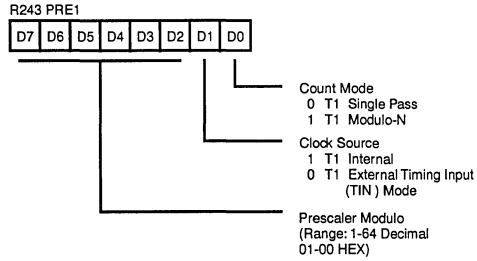


Figure 32. Prescaler 1 Register (F3H: Write Only)

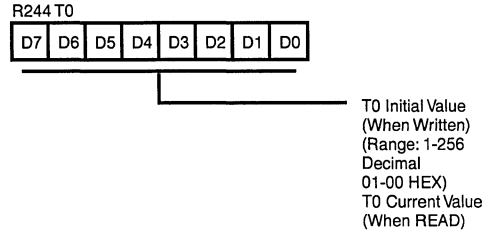


Figure 33. Counter/Timer 0 Register (F4H: Read/Write)

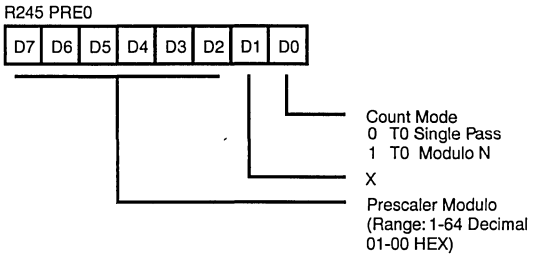
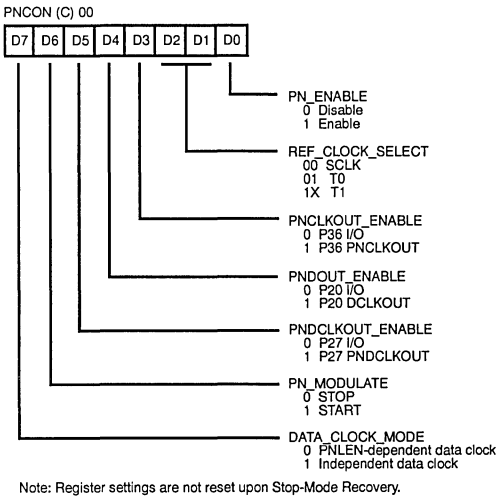
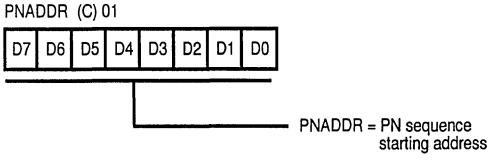


Figure 34. Prescaler 0 Register (F5H: Write Only)



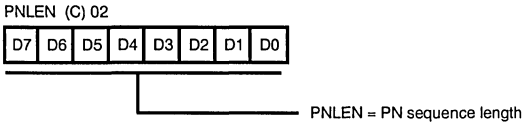
Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 35. PN Modulator Control Register ((C) 00H: Read/Write)



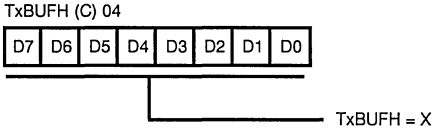
Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 36. PN ROM Relative Address Register ((C) 01H: Read/Write)



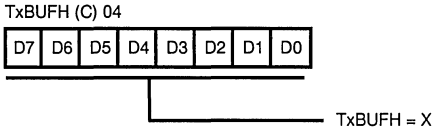
Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 37. PN Code Length Register ((C) 02H: Read/Write)



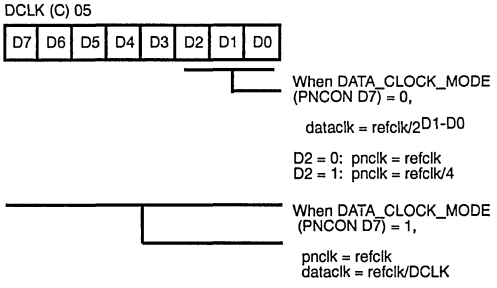
Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 38. PN Modulator Low-Byte Data Hold Register ((C) 03H: Write Only)



Note: Register settings are not reset upon Stop-Mode Recovery.

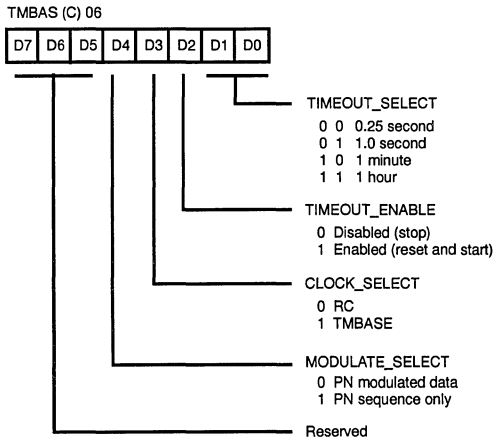
Figure 39. PN Modulator High-Byte Data Hold Register ((C) 04H: Write Only)



Note: Register settings are not reset upon Stop-Mode Recovery.

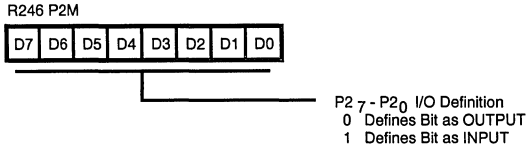
Figure 40. Data Clock Control Register ((C) 05H: Read/Write)

EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)



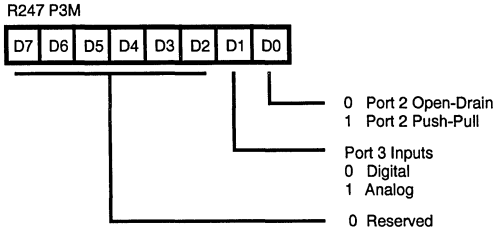
Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 41. Time Base Generator Control Register ((C) 06H: Read/Write)



Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 42. Port 2 Mode Register (F6H; Write Only)



Note: Register settings are not reset upon Stop-Mode Recovery.

Figure 43. Port 3 Mode Register (F7H: Write Only)

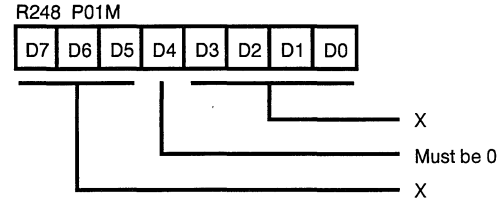


Figure 44. Port 0 and 1 Mode Register (F8H: Write Only)

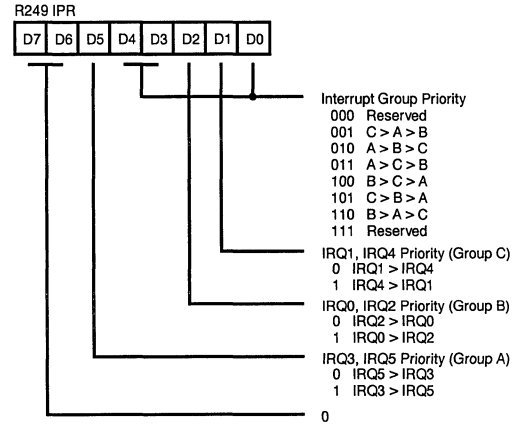


Figure 45. Interrupt Priority Register (F9H: Write Only)

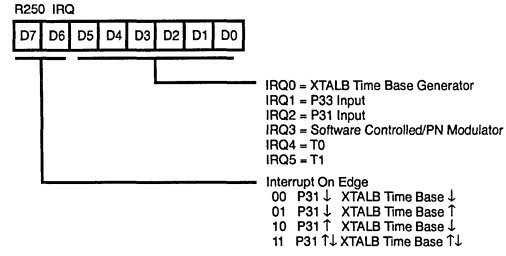


Figure 46. Interrupt Request Register (FAH: Read/Write)

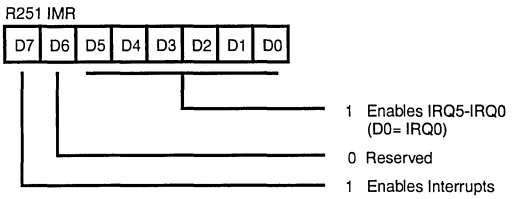


Figure 47. Interrupt Mask Register (FBH: Read/Write)

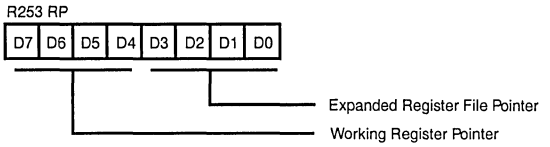


Figure 49. Register Pointer (FDH: Read/Write)

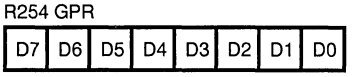


Figure 50. General-Purpose Register (FEH: Read/Write)

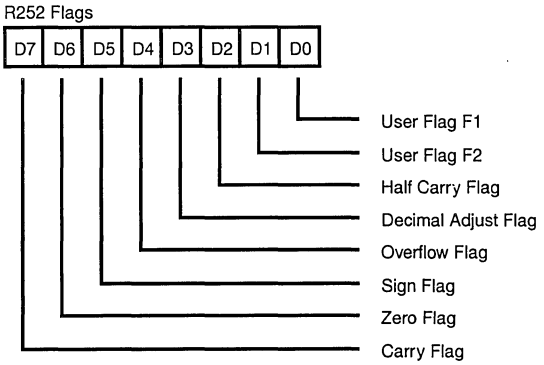


Figure 48. Flag Register (FCH: Read/Write)

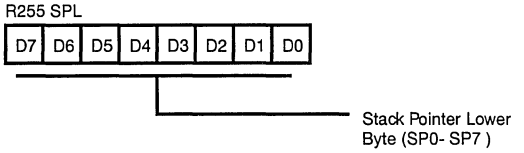


Figure 51. Stack Pointer (FFH: Read/Write)

DEVICE CHARACTERISTICS

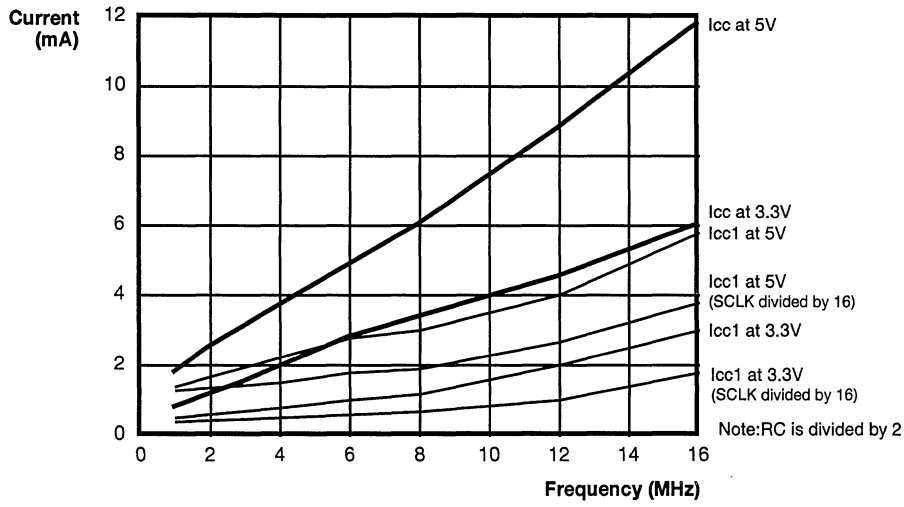


Figure 52. Typical I_{CC} vs Frequency

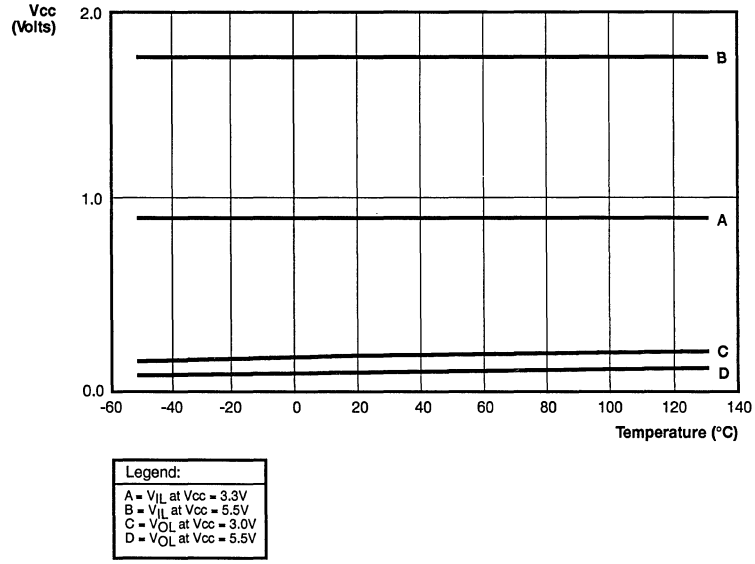


Figure 53. Typical V_{OL}, V_{IL} vs Temperature

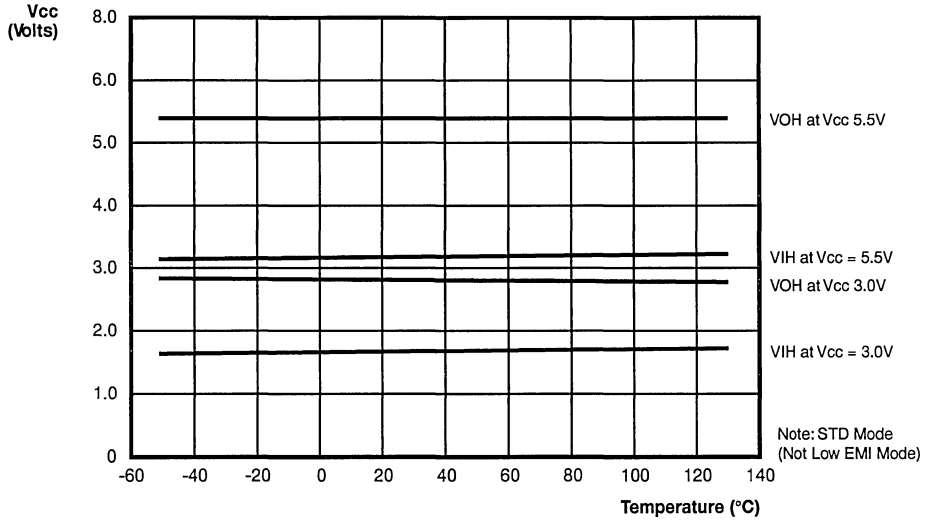


Figure 54. Typical V_{OH}, V_{IH} vs Temperature

DEVICE CHARACTERISTICS (Continued)

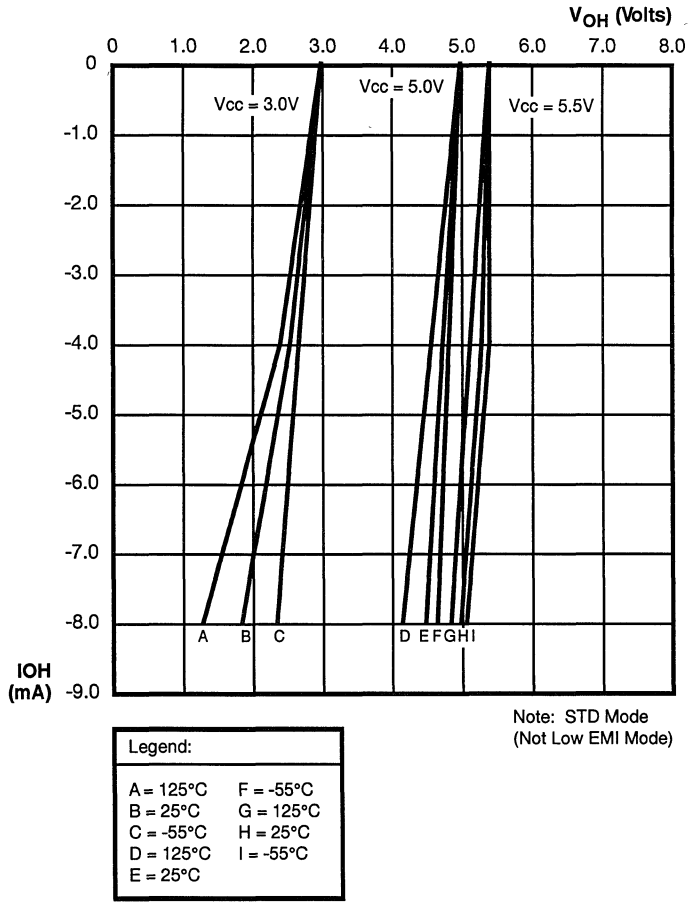


Figure 55. Typical V_{OH} vs I_{OH} Over Temperature

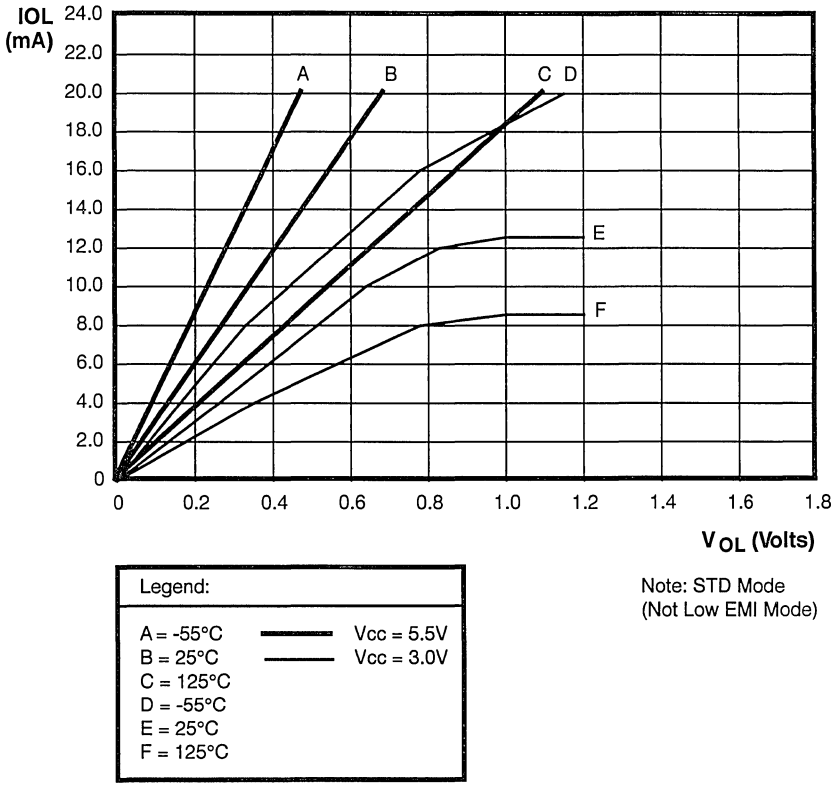


Figure 56. Typical I_{OL} vs V_{OL} Over Temperature

DEVICE CHARACTERISTICS (Continued)

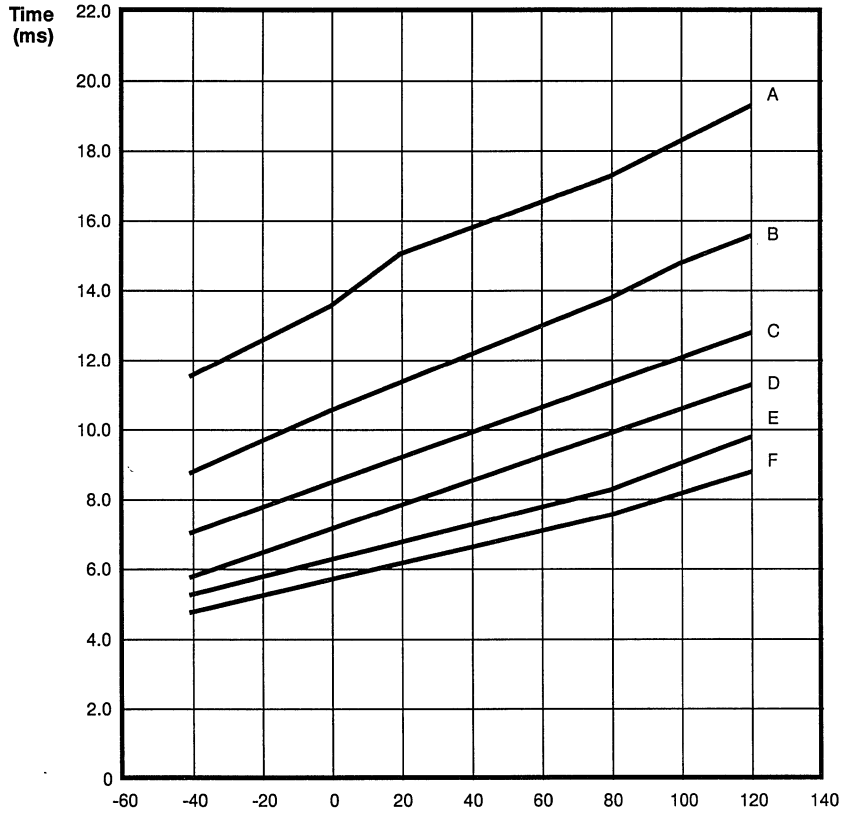


Figure 57. Typical Power-On Reset Time vs Temperature

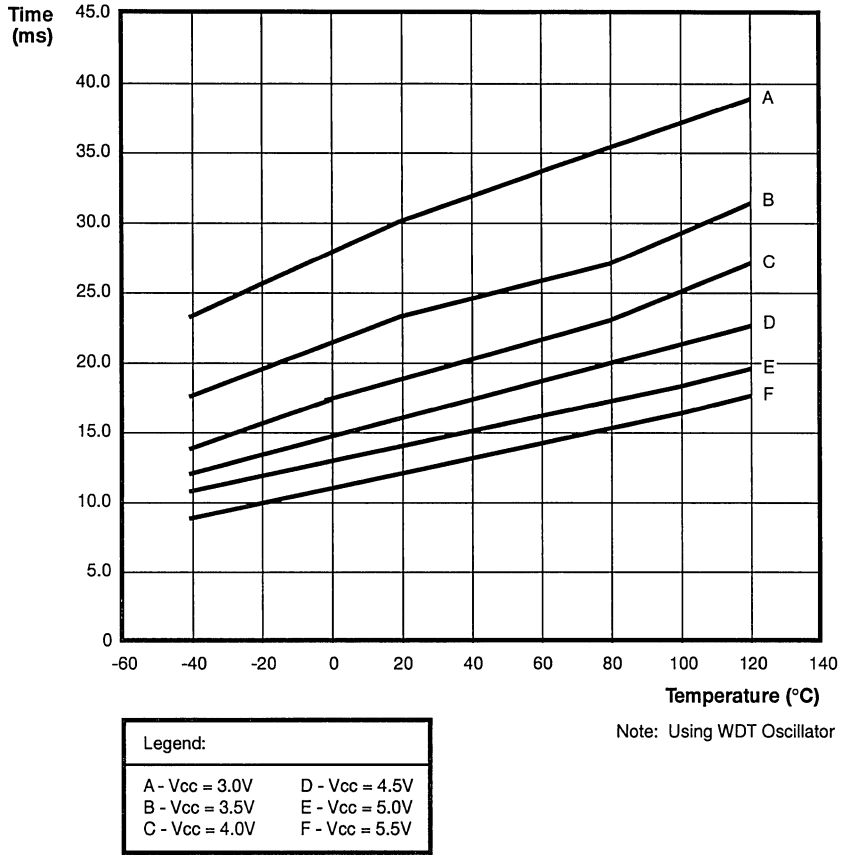


Figure 58. Typical 5 ms WDT Setting vs Temperature

DEVICE CHARACTERISTICS (Continued)

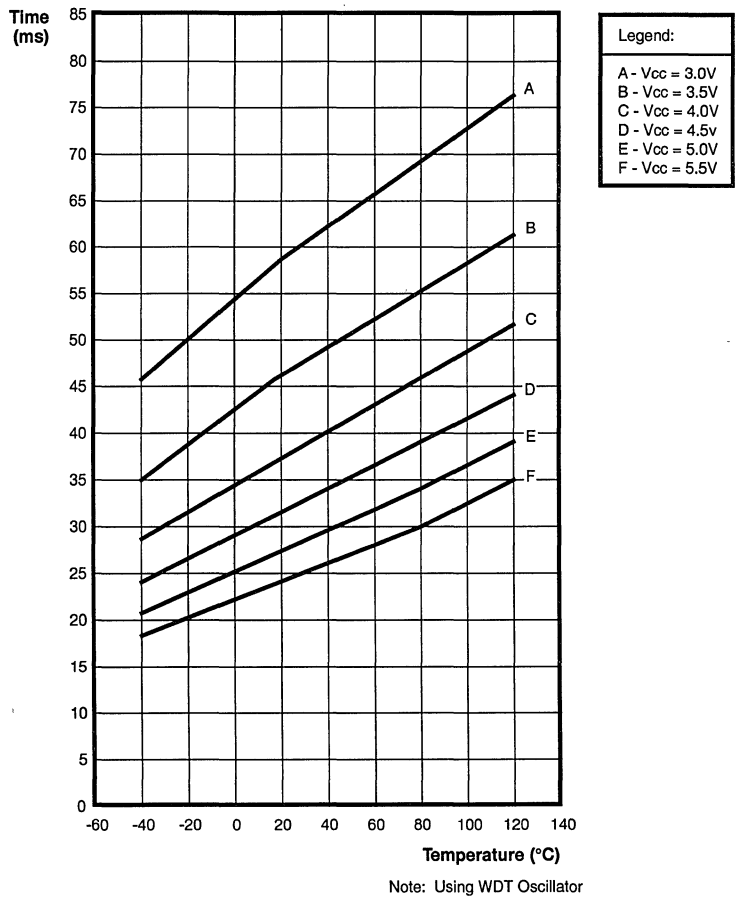


Figure 59. Typical 15 ms WDT Setting vs Temperature

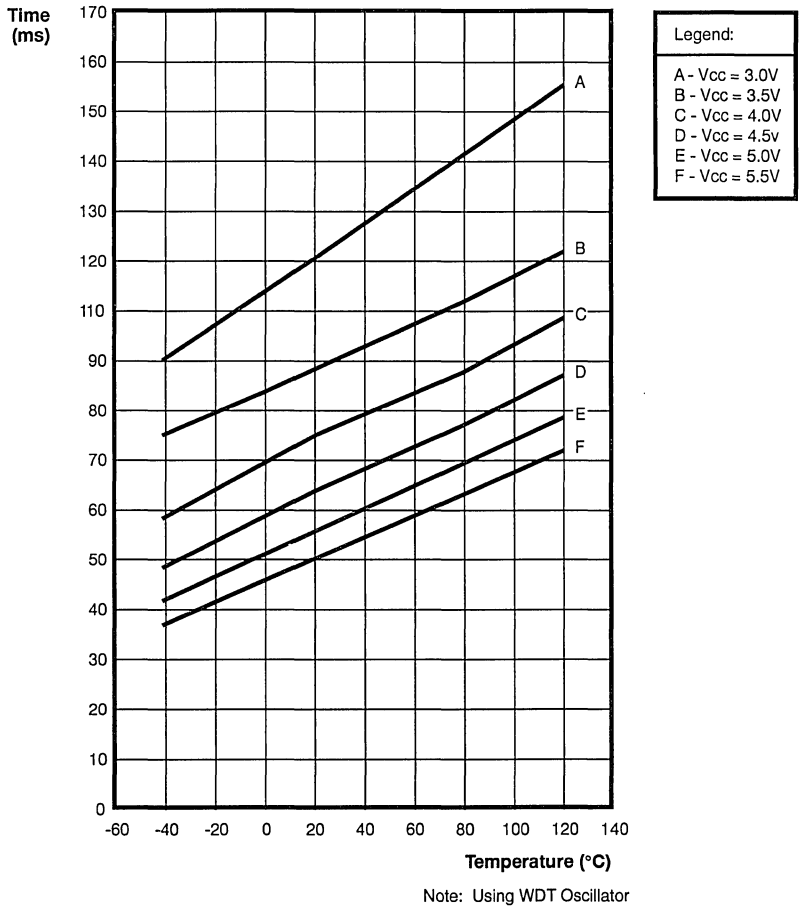


Figure 60. Typical 25 ms WDT Setting vs Temperature

DEVICE CHARACTERISTICS (Continued)

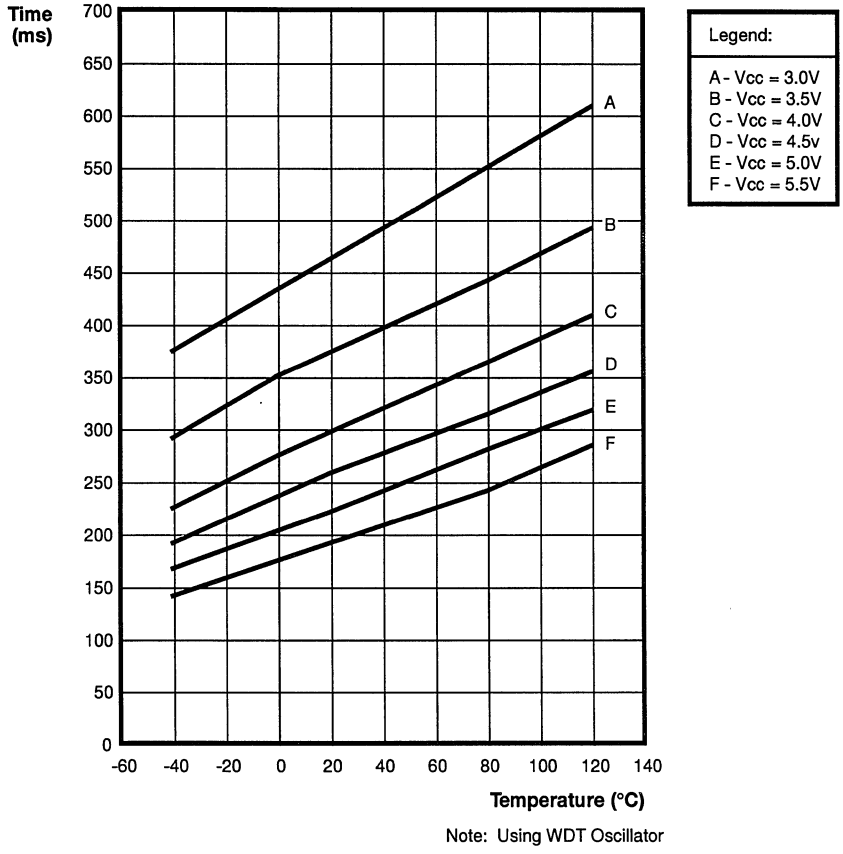
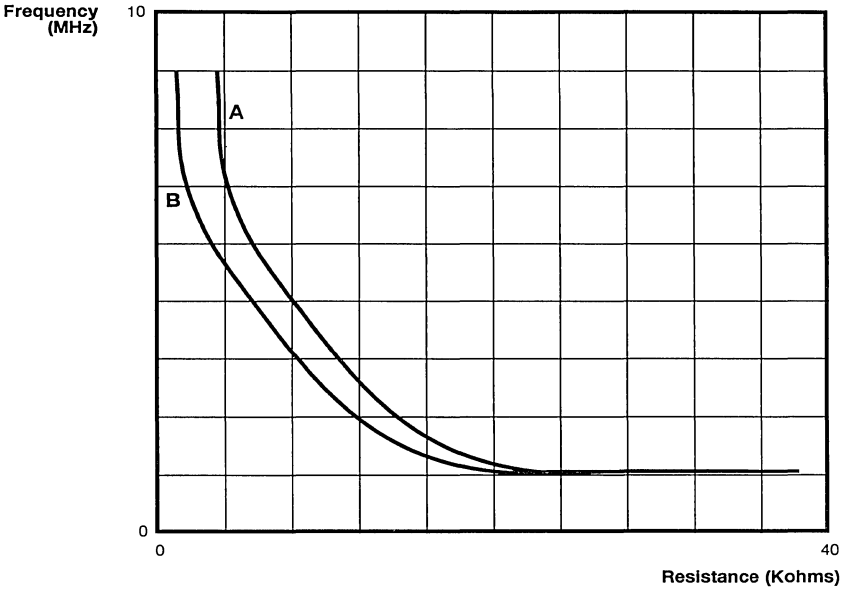


Figure 61. Typical 100 ms WDT Setting vs Temperature



Legend:
A - VCC = 5.0V ±10%; no external capacitor B - VCC = 5.0V ±10%; external capacitor = 22 pF

Figure 62. Typical Frequency vs RC Resistance

Z87200 Spread-Spectrum Transceiver

4

Z87200

SPREAD-SPECTRUM TRANSCEIVER

FEATURES

Device	Min PN Rate* (Mchips)	Max Data Rate* (Mbps)	Speed (MHz)	Package
Z87200	11	2.048	20/45	100-Pin PQFP

Note: *45 MHz only

- Complete Direct Sequence Spread-Spectrum Transceiver in a Single CMOS IC
- Programmable Functionality Supports Many Different Operational Modes
- Acquires Within One Symbol Duration Using Digital PN Matched Filter
- Two Independent PN Sequences, Each up to 64 Chips Long for Distinct Processing of the Acquisition/Preamble Symbol and Subsequent Data Symbols
- Power Management Features
- Optional Spectral Whitening Code Generation
- Full- or Half-Duplex Operation

Benefits

- High Performance and High Reliability for Reduced Manufacturing Costs
- Ideal for a Wide Range of Wireless Applications Including Data Acquisition Systems, Transaction Systems, and Wireless Local Area Networks (WLANs)
- Fast Response and Very Low Overhead when Operating in Burst Modes
- Allows High Processing Gain to Maximize the Acquisition Probability, then Reduced Code Length for Increased Data Rate
- Reduced Power Consumption
- Randomizes Data to Meet Regulatory Requirements
- Permits Dual Frequency (Frequency Division Duplex) or Single Frequency (Time Division Duplex) Operation
- Small Footprint, Surface Mount

GENERAL DESCRIPTION

The Z87200 is a programmable single-chip, spread-spectrum, direct-sequence transceiver. The Z87200 incorporates Stanford Telecom spread-spectrum and wireless technology and is identical to Stanford Telecom's STEL-2000A. By virtue of its fast acquisition capabilities and its ability to support a wide range of data rates and spread-spectrum parameters, the Z87200 spread-spectrum transceiver supports the implementation of a wide range of burst data communications applications.

Available in both 45- and 20-MHz versions, the Z87200 performs all the digital processing required to implement a fast-acquisition direct sequence (such as pseudonoise- or PN-modulated), spread-spectrum full- or half-duplex system. Differentially encoded BPSK and QPSK are fully supported. The receiver section can also handle differentially encoded pi/4 QPSK. A block diagram of the Z87200 is shown in Figure 1; its pin configuration is shown in Z87200 receive functions integrate the capabilities of a digital downconverter, PN matched filter, and DPSK demodulator, where the input signal is an analog-to-digital converted I.F. signal. Z87200 transmit functions include a differential BPSK/QPSK encoder, PN modulator (spreader), and BPSK/QPSK modulator, where the transmitter output is a sampled digitally modulated signal ready for external digi-

GENERAL DESCRIPTION (Continued)

tal-to-analog conversion (or, if preferred, the spread baseband signal may be output to an external modulator).

These transceiver functions have been designed and integrated for the transmission and reception of bursts of spread data. In particular, the PN Matched Filter has two distinct PN coefficient registers (rather than a single one) in order to speed and improve signal acquisition performance by automatically switching from one to the other upon signal acquisition. The Z87200 is thus optimized to provide reliable, high-speed wireless data communications.

Symbol-Synchronous PN Modulation

The Z87200 operates with symbol-synchronous PN modulation in both transmit and receive modes. Symbol-synchronous PN modulation refers to operation where the PN code is aligned with the symbol transitions and repeats once per symbol. By synchronizing a full PN code cycle over a symbol duration, acquisition of the PN code at the receiver simultaneously provides symbol synchronization, thereby significantly improving overall acquisition time.

As a result of the Z87200's symbol-synchronous PN modulation, the data rate is defined by the PN chip rate and length of the PN code; that is, by the number of chips per symbol, where a "chip" is a single "bit" of the PN code. The PN chip rate, R_c chips/second, is programmable to as much as 1/4 the rate of RXIFCLK, and the PN code length, N, can be programmed up to a value of 64. When operating with BPSK modulation, the data rate for a PN code of length N and PN chip rate R_C chips/sec is R_C/N bps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N and PN chip rate R_c chips/sec is $2R_c/N$ bps. Conversely, for a given data rate R_b bps, the length N of the PN code defines the PN chip rate R_c as $N \times R_b$ chips/sec for BPSK or as $(N \times R_b)/2$ chips/sec for QPSK.

The data rate R_b and the PN code length N, however, cannot generally be arbitrarily chosen. United States FCC Part 15.247 regulations require a minimum processing gain of 10 dB for unlicensed operation in the Industrial, Scientific, and Medical (ISM) bands, implying that the value of N must be at least 10. To implement such a short code, a Barker code of length 11 would typically be used in order to obtain desirable auto- and cross-correlation properties, although compliance with FCC regulations depends upon the overall system implementation. The Z87200 further includes transmit and receive code overlay generators to insure that signals spread with such a short PN code length possess the spectral properties required by FCC regulations.

The receiver clock rate established by RXIFCLK must be at least four times the receive PN spreading rate and is limited to a maximum speed of 45.056 MHz in the 45 MHz Z87200 and 20.0 MHz in the 20 MHz Z87200. The ensuing discussion is in terms of the 45 MHz Z87200, but the numerical values may be scaled proportionately for the 20 MHz version. As a result of the maximum 45.056 MHz RXIFCLK, the maximum supported PN chip rate is 11.264 Mchips/second. When operating with BPSK modulation, the maximum data rate for a PN code of length N is 11.264/N Mbps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N is 22.528/N Mbps. Conversely, for a given data rate R_b, the length N of the PN code employed must be such that the product of $N \times R_b$ is less than 11.264 Mchips/sec (for BPSK) or 22.528 Mchips/sec (for QPSK). For the 45 MHz Z87200, then, a PN code length of 11 implies that the maximum data rate that can be supported in compliance with the processing gain requirements of FCC regulations is 2.048 Mbps using differential QPSK. Note again, however, that FCC compliance using the Z87200 with a PN code of length 11 depends upon the overall system implementation.

Z87200 I.F. Interface

The Z87200 receiver circuitry employs an NCO and complex multiplier referenced to RXIFCLK to perform frequency downconversion, where the input I.F. sampling rate and the clock rate of RXIFCLK must be identical. In "complex input" or Quadrature Sampling Mode, external dual analog-to-digital converters (ADCs) sample quadrature I.F. signals so that the Z87200 can perform true full single sideband downconversion directly from I.F. to baseband. At PN chip rates less than one-eighth the value of RXIFCLK, downconversion may also be effected using a single ADC in "real input" or Direct I.F. Sampling Mode.

The input I.F. frequency is not limited by the capabilities of the Z87200. The highest frequency to which the NCO can be programmed is 50% of the I.F. sampling rate (the frequency of RXIFCLK); moreover, the signal bandwidth, NCO frequency, and I.F. sampling rate are all interrelated, as discussed in Higher I.F. frequencies, however, can be supported by using one of the aliases of the NCO frequency generated by the sampling process. For example, a spread signal presented to the Z87200's receiver ADCs at an I.F. frequency of $f_{I.F.}$, where $f_{RXIFCLK} < f_{I.F.} < 2 \times f_{RXIFCLK}$, can generally, as allowed by the signal's bandwidth, be supported by programming the Z87200's NCO to a frequency of ($f_{I.F.} - f_{RXIFCLK}$), as discussed in Appendix A of this product specification. The maximum I.F. frequency is then limited by the track-and-hold capabilities of the ADC(s) selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost as well as the performance can typically be improved by using an I.F. frequency of 30 MHz or lower. Downconversion to baseband is then accomplished digitally by the Z87200, with a programmable loop filter provided to establish a frequency tracking loop.

Burst and Continuous Data Modes

The Z87200 is designed to operate in either burst or continuous mode: in burst mode, built-in symbol counters allow bursts of up to 65,533 symbols to be automatically transmitted or received; in continuous mode, the data is simply treated as a burst of infinite length. The Z87200's use of a digital PN Matched Filter for code detection and despreading permits signal and symbol timing acquisition in just one symbol. The fast acquisition properties of this design are exploited by preceding each data burst with a single Acquisition/Preamble symbol, allowing different PN codes (at the same PN chip rate) to independently spread the Acquisition/Preamble and data symbols. In this way, a long PN code with high processing gain can be used for the Acquisition/Preamble symbol to maximize the probability of burst detection, and a shorter PN code can be used thereafter to permit a higher data rate.

To improve performance in the presence of high noise and interference levels, the Z87200 receiver's symbol timing recovery circuit incorporates a "flywheel circuit" to maximize the probability of correct symbol timing. This circuit will insert a symbol clock pulse if the correlation peak obtained by the PN Matched Filter fails to exceed the programmed detect threshold at the expected time during a given symbol. During each burst, a missed detect counter tallies each such event to monitor performance and allow a burst to be aborted in the presence of abnormally high interference. A timing gate circuit further minimizes the probability of false correlation peak detection and consequent false symbol clock generation due to noise or interference.

To minimize power consumption, individual sections of the device can be turned off when not in use. For example, the receiver circuitry can be turned off during transmission and, conversely, the transmitter circuitry can be turned off during reception when the Z87200 is operating in a half-duplex/time division duplex (TDD) system. If the NCO is not being used as the BPSK/QPSK modulator (that is, if an external modulator is being used), the NCO can also be turned off during transmission to conserve still more power.

4

Conclusion

The fast acquisition characteristics of the Z87200 make it ideal for use in applications where bursts are transmitted relatively infrequently. In such cases, the device can be controlled so that it is in full "sleep" mode with all receiver, transmitter, and NCO functions turned off over the majority of the burst cycle, thereby significantly reducing the aggregate power consumption. Since the multiply operations of the PN Matched Filter consume a major part of the overall power required during receiver operation, two independent power-saving techniques are also built into the PN Matched Filter to reduce consumption during operation by a significant factor for both short and long PN spreading codes.

The above features make the Z87200 an extremely versatile and useful device for spread-spectrum data communications. Operating at its highest rates, the Z87200 is suitable for use in wireless Local Area Network implementations, while its programmability allows it to be used in a variety of data acquisition, telemetry, and transaction system applications.

GENERAL DESCRIPTION (Continued)

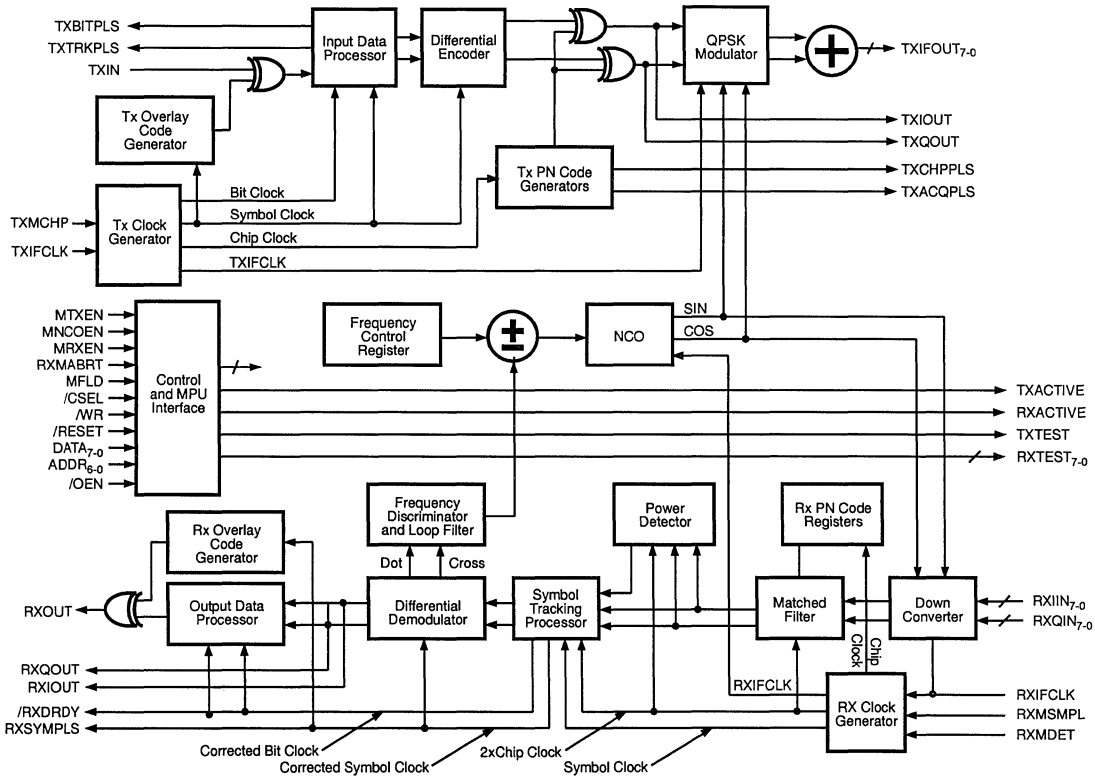


Figure 1. Z87200 Block Diagram

PIN DESCRIPTION

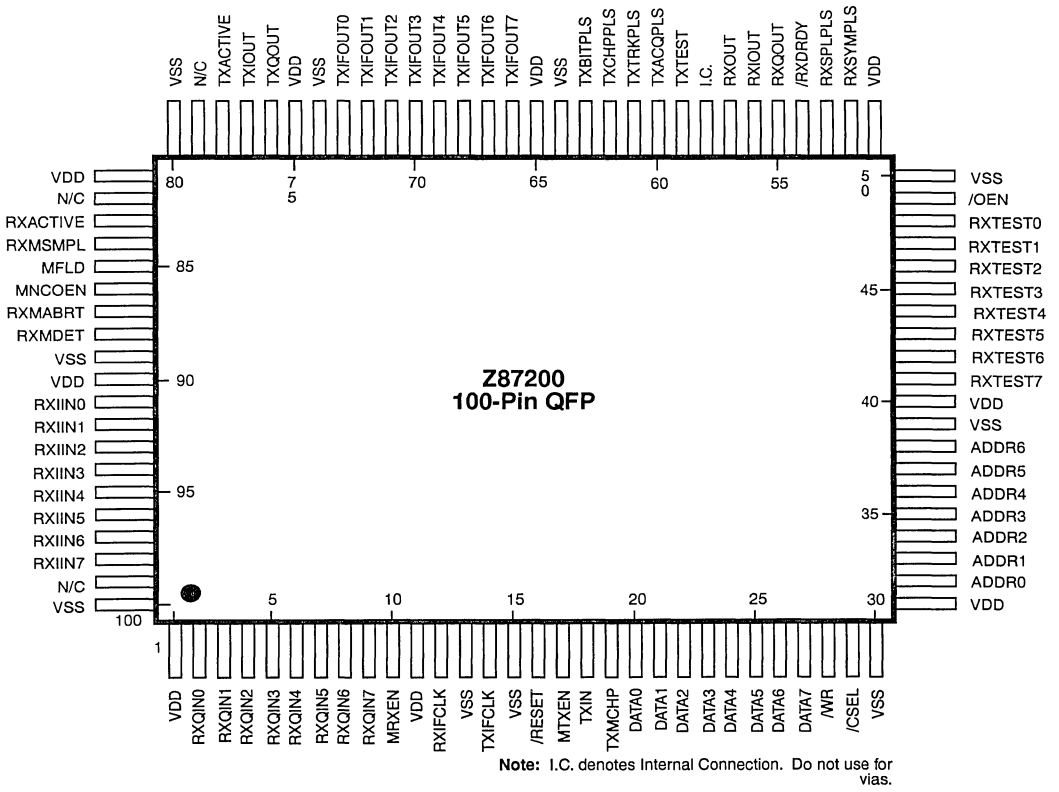


Figure 2. Z87200 100-Pin PQFP Pin Description

PIN DESCRIPTION (Continued)

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
1,11,31,40,51,65,75,81,90	V_{DD}	Power Supply
2	RXQIN0	Rx Q-Channel Input (Bit 0; LSB)
3	RXQIN1	Rx Q-Channel Input (Bit 1)
4	RXQIN2	Rx Q-Channel Input (Bit 2)
5	RXQIN3	Rx Q-Channel Input (Bit 3)
6	RXQIN4	Rx Q-Channel Input (Bit 4)
7	RXQIN5	Rx Q-Channel Input (Bit 5)
8	RXQIN6	Rx Q-Channel Input (Bit 6)
9	RXQIN7	Rx Q-Channel Input (Bit 7; MSB)
10	RXXE	Manual Receiver Enable
12	RXIFCLK	Receiver I.F. Clock
13,15,30,39,50,64,74,80,89	V_{SS}	Ground
14	TXIFCLK	Transmitter I.F. Clock
16	/RESET	/Reset
17	MTXE	Manual Transmitter Enable
18	TXIN	Transmitter Input
19	TXMCHP	Transmitter Manual Chip Pulse
20	DATA0	Data Bus (Bit 0; LSB)
21	DATA1	Data Bus (Bit 1)
22	DATA2	Data Bus (Bit 2)
23	DATA3	Data Bus (Bit 3)
24	DATA4	Data Bus (Bit 4)
25	DATA5	Data Bus (Bit 5)
26	DATA6	Data Bus (Bit 6)
27	DATA7	Data Bus (Bit 7; MSB)
28	/WR	Write Bar
29	/CSEL	Chip Select Bar
32	ADDR0	Address Bus (Bit 0; LSB)
33	ADDR1	Address Bus (Bit 1)
34	ADDR2	Address Bus (Bit 2)
35	ADDR3	Address Bus (Bit 3)
36	ADDR4	Address Bus (Bit 4)
37	ADDR5	Address Bus (Bit 5)
38	ADDR6	Address Bus (Bit 6; MSB)
41	RXTEST7	Receiver Test Output (Bit 7)
42	RXTEST6	Receiver Test Output (Bit 6)
43	RXTEST5	Receiver Test Output (Bit 5)
44	RXTEST4	Receiver Test Output (Bit 4)
45	RXTEST3	Receiver Test Output (Bit 3)
46	RXTEST2	Receiver Test Output (Bit 2)
47	RXTEST1	Receiver Test Output (Bit 1)
48	RXTEST0	Receiver Test Output (Bit 0)
49	/OEN	Output Enable Bar
52	RXSYMPLS	Receiver Symbol Pulse
53	RXSPLPLS	Receiver Sample Pulse

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
54	/RXDRDY	Receiver Data Ready Bar
55	RXQOUT	Receiver Q Channel Output
56	RXIOUT	Receiver I Channel Output
57	RXOUT	Receiver Output
58	I.C.	[Note]
59	TXTEST	Transmitter Test Output
60	TXACQPLS	Transmitter Acquisition Pulse
61	TXTRKPLS	Transmitter Data Track Pulse
62	TXCHPPLS	Transmitter Chip Pulse
63	TXBITPLS	Transmitter Bit Pulse
66	TXIFOUT7	Tx I.F. Output (Bit 7, MSB)
67	TXIFOUT6	Tx I.F. Output (Bit 6)
68	TXIFOUT5	Tx I.F. Output (Bit 5)
69	TXIFOUT4	Tx I.F. Output (Bit 4)
70	TXIFOUT3	Tx I.F. Output (Bit 3)
71	TXIFOUT2	Tx I.F. Output (Bit 2)
72	TXIFOUT1	Tx I.F. Output (Bit 1)
73	TXIFOUT0	Tx I.F. Output (Bit 0, LSB)
76	TXQOUT	Tx Q-Channel Output
77	TXIOUT	Tx I-Channel Output
78	TXACTIVE	Transmitter Active
79,82	N.C.	No Connection
83	RXACTIVE	Receiver Active
84	RXMSMPL	Receiver Manual Sample Clock
85	MFLD	Manual Frequency Load
86	MNCOEN	Manual NCO Enable
87	RXMABRT	Receiver Manual Abort
88	RXMDET	Receiver Manual Detect
91	RXIIN0	Rx I-Channel Input (Bit 0; LSB)
92	RXIIN1	Rx I-Channel Input (Bit 1)
93	RXIIN2	Rx I-Channel Input (Bit 2)
94	RXIIN3	Rx I-Channel Input (Bit 3)
95	RXIIN4	Rx I-Channel Input (Bit 4)
96	RXIIN5	Rx I-Channel Input (Bit 5)
97	RXIIN6	Rx I-Channel Input (Bit 6)
98	RXIIN7	Rx I-Channel Input (Bit 7; MSB)
99	N.C.	No Connection
100	V_{SS}	Ground

Note: I.C. denotes Internal Connection. Do not use for vias.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Range	Units
T_{STG}	Storage Temperature	–55 to +150	°C
V_{DD} (max)	Supply Voltage on V_{DD}	–0.3 to + 7	Volts
V_I(max)	Input Voltage	–0.3 to V_{DD}+0.3	Volts
I_I	DC Input Current	±10	mA
T_A	Operating Temperature (Ambient)	0 to +70	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		Typ		
Symbol	Parameter	Min	Max	@ 25°C	Units	Conditions
I_{DDQ}	Supply Current, Quiescent		1.0		mA	Static, no clock
I_{DD}	Supply Current, Operational		380 170	[Note]	mA mA	$f_{RXIFCLK}$ = 45.056 MHz $f_{RXIFCLK}$ = 20 MHz
V_{IH} (min)	High Level Input Voltage	0.7V_{DD}	V_{DD}+.3	2.6	Volts	Logic '1'
V_{IL}(min)	Low Level Input Voltage	V_{SS}–.3	0.2V_{DD}	1.5	Volts	Logic '0'
I_{IH} (min)	High Level Input Current		10		µA	All inputs, V_{IN} = V_{DD}
I_{IL} (max)	Low Level Input Current		–10		µA	TXIFCLK, RXIFCLK, /RESET only, V_{IN} = V_{SS}
I_{IL}(max)	Low Level Input Current	–130	–15	–45	µA	All other inputs, V_{IN} = V_{SS}
V_{OH}(min)	High Level Output Voltage	V_{DD}–0.4			Volts	I_O = –2.0 mA, all outputs
V_{OL}(max)	Low Level Output Voltage		0.4	0.1	Volts	I_O = +2.0 mA, all outputs
I_{OS}	Output Short Circuit Current	20	130	65	mA	V_{OUT} = V_{DD}, V_{DD} = max
C	Input Capacitance	2			pF	All inputs
C_{OUT}	Output Capacitance			4	pF	All outputs

Notes:
1. The operational supply current depends on how the Z87200 is configured. Typical current consumption can be approximated as follows:
2. I_{DD}=5x$f_{RXIFCLK}$ +13 x f_{CHIP} mA,
3. where $f_{RXIFCLK}$ is the frequency of RXIFCLK and f_{CHIP} is the PN chip rate, both in MHz.

4

A.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
t_{SU}	/CSEL, ADDR, DBUS to WRITE Setup	5		ns	
t_{HD}	WRITE to CSEL, ADDR, DBUS Hold	5		ns	
t_W	WRITE Pulse Width	5		ns	

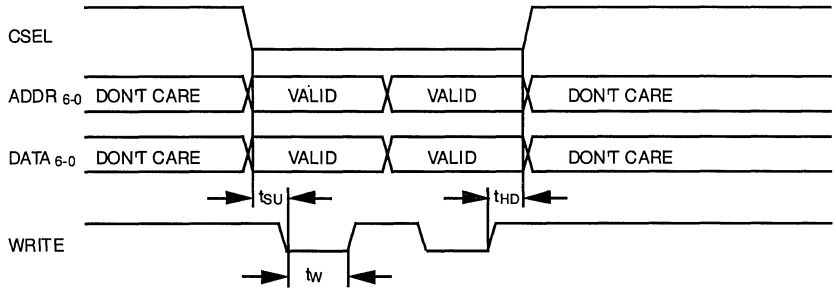


Figure 3. Microprocessor Interface Timing

A.C. CHARACTERISTICS - TRANSMITTER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A 0°C to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
$f_{TXIFCLK}$	TXIFCLK Frequency		45.056 20.0	MHz MHz	Z0200045FSC Z0200020FSC or if TXIFOUT is used
t_{CH}	TXIFCLK Pulse width, High	10		ns	
t_{CL}	TXIFCLK Pulse width, Low	10		ns	
t_{SU}	TXIN to TXIFCLK setup	3		ns	
t_{HD}	TXIN to TXIFCLK hold	5		ns	
t_{CT}	TXIFCLK to TXBITPLS, TXTRKPLS, XACQPLS, TXIOUT or TXQOUT delay		35	ns	

Notes:

1. The number of TXIFCLK cycles per cycle of TXCHPPLS is determined by the data stored in bits 5-0 of address 41_H. It is shown as 2 in Figure 8 but can be set from 2 to 64.
2. The width of the TXBITPLS, TXTRKPLS and TXACQPLS signal pulses is equal to the period of TXCHPPLS; that is, equal to the PN chip period.
3. In QPSK mode, the TXBITPLS signal pulses high twice during each symbol period, once during the center chip and once during the last chip. If the number of chips per symbol is even, the number of chip periods between the TXBITPLS pulse at the end of the previous symbol and the one in the center of the symbol will be one more than the number of chip periods between the TXBITPLS pulse in the center of the symbol and the one at the end. The falling edge of the second pulse corresponds to the end of the symbol period.
4. The TXTRKPLS signal pulses high once each symbol period, during the last chip period of that symbol. The falling edge corresponds to the end of the symbol period.
5. The TXACQPLS signal pulses high once each burst, transmission, during the last chip of the Acquisition/Preamble symbol. The falling edge corresponds to the end of this symbol period.

4

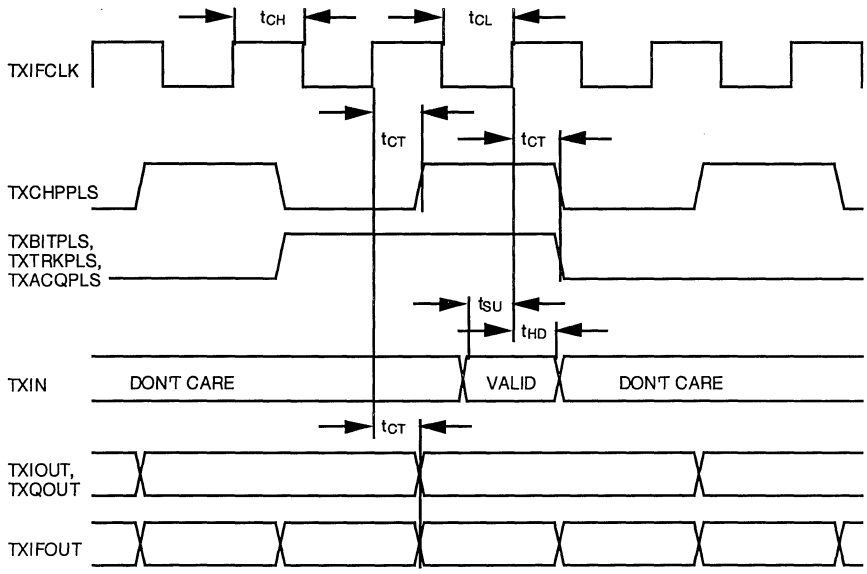


Figure 4. Transmitter Input/Output Timing

A.C. CHARACTERISTICS - RECEIVER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max.**	**Units**	**Conditions**
$f_{RXIFCLK}$	RXIFCLK Frequency		45.056 20.0	MHz MHz	Z8720045FSC Z8720020FSC
t_{CH}	RXIFCLK Pulse width, High	10		ns	
t_{CL}	RXIFCLK Pulse width, Low	10		ns	
t_{SU}	RXIIN or RXQIN to RXIFCLK setup	3		ns	
t_{HD}	RXIIN or RXQIN to RXIFCLK hold	7		ns	
t_{CR}	RXIFCLK to RXSPLPLS, RXSYMPLS, or /RXDRDY delay		35	ns	
t_{CD}	RXIFCLK to RXOUT, RXIOUT, or RXQOUT delay		35	ns	

Notes:

1. The number of RXIFCLK cycles per cycle of RXSPLPLS is determined by the data stored in bits 5-0 of address 02_H. It is shown as 2 in Figure 9, but can be set from 2 to 64.
2. The rising edge of /RXDRDY should be used to clock out the data (RXOUT, RXIOUT, or RXQOUT).

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A.C. CHARACTERISTICS

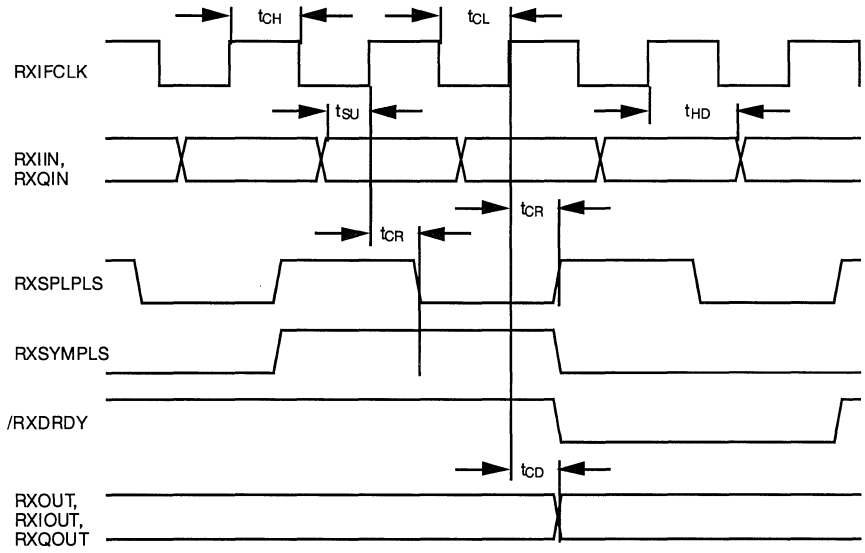

Figure 5. Receiver Input/Output

AC CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		
Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{D1}	/OEN low to RXTEST $_{7-0}$ active	11		ns
t_{D2}	/OEN high to RXTEST $_{7-0}$ tri-state	7		ns

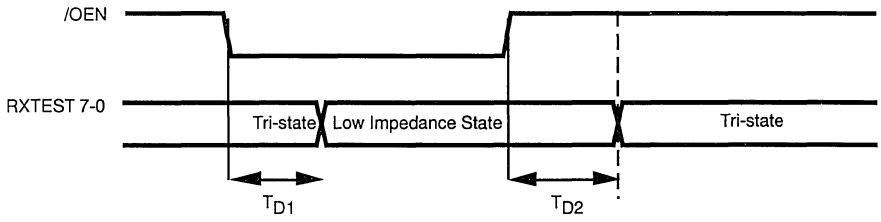

Figure 6. /OEN to RXTEST 7-0 Timing

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FUNCTIONAL BLOCKS

Transmit and Receive Clock Generators

Timing in the transmitter and receiver sections of the Z87200 is controlled by the Transmit and Receive Clock Generator Blocks. These blocks are programmable dividers providing signals at the chip and symbol rates (as well as at multiples and sub-multiples of these frequencies) as programmed through the Z87200's control registers. If desired, the complete independence of the transmitter and receiver sections allows the transmit and receive clocks to be mutually asynchronous. Additionally, the Z87200 allows external signals to be provided as references for the transmit (TXMCHP) and receive (RXMSMPL) chip rates. Given the transmit PN chip rate, the PN-synchronous transmit symbol rate is then derived from the programmed number of PN chips per transmit symbol. At the receiver, symbol synchronization and the receive symbol rate are determined from processing of the PN matched filter output, or, if desired, can be provided from the programmed number of PN chips per receive symbol or an external symbol synch symbol, RXMDET. Burst control is achieved by means of the transmit and receive Symbols per Burst counters. These programmable 16-bit counters allow the Z87200 to operate automatically in burst mode, stopping at the end of each burst without the need of any external counters.

Input and Output Processors

When the transmitter and receiver are operating in QPSK mode, the data to be transmitted and the received data are processed in pairs of bits (dibits), one bit for the in-phase (I) channel and one for the quadrature (Q) channel. Dibits are transmitted and received as single differentially encoded QPSK symbols. Single-bit I/O data is converted to and from this format by the Input and Output Processors, accepting TXIN as the serial data to be transmitted and producing RXOUT as the serial data output. If desired, the received data is also available at the RXIOUT and RXQOUT pins in (I and Q) dibit format prior to dibit-to-serial conversion. While receive timing is derived by the Z87200 Symbol Tracking Processor, transmit timing is provided by the Input Processor. In BPSK mode, the Input Processor will generate the TXBITPLS signal once per symbol to request each bit of data, while in QPSK mode it will generate the TXBITPLS signal twice per symbol to request the two bits of data corresponding to each QPSK symbol.

Differential Encoder

Data to be transmitted is differentially encoded before being spread by the transmit PN code. Differential encoding of the signal is fundamental to operation of the Z87200's receiver: the Z87200's DPSK Demodulator computes "Dot" and "Cross" product functions of the current and previous symbols' downconverted I and Q signal components in order to perform differential decoding as an intrinsic part of DPSK demodulation.

The differential encoding scheme depends on whether the modulation format is to be BPSK or QPSK. For DBPSK, the encoding algorithm is straightforward: output bit(k) equals input bit(k) ⊕ output bit(k–1), where ⊕ represents the logical XOR function. For DQPSK, however, the differential encoding algorithm, as shown in Table 2, is more complex since there are now sixteen possible new states depending on the four possible previous output states and four possible new input states.

Table 2. QPSK Differential Encoder Sequence

New Input		Previously Encoded $OUT(I,Q)_{K-1}$							
$IN(I,Q)_K$		**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**
0	0	0	0	0	1	1	1	1	0
0	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	1
Newly Encoded OUT (I,Q)K									

Transmitter PN Code Generation

When the Z87200 is used for burst signal operation, each burst is preceded by an Acquisition/Preamble symbol to facilitate acquisition. This Acquisition/Preamble symbol is automatically generated by the Z87200's transmitter before information data symbols are accepted for transmission. Two separate and independent PN codes may be employed: one for spreading the Acquisition/Preamble symbol, and one for the subsequent information data symbols. As a result, a much higher processing gain may be used for signal acquisition than for signal tracking in order to improve burst acquisition performance.

The Transmitter Acquisition/Preamble and Transmitter Data Symbol PN code lengths are completely independent of each other and can be up to 64 chips long. Transmit PN codes are programmed in the Z87200 as binary code values. The number of Transmitter Chips per Acquisition/Preamble Symbol is set by the value stored in bits 5-0 of address 43_H, and the Transmitter Acquisition/Preamble Symbol Code coefficient values are stored in addresses 44_H to $4B_H$. The number of Transmitter Chips per Data Symbol is set by the data stored in address 42_H, and the Transmitter Data Symbol Code coefficient values are stored in addresses $4C_H$ to 53_H.

A rising edge of the MTXEN input or of bit 1 of address 37_H causes the Z87200 to begin the transmit sequence by transmitting a single symbol using the Acquisition/Preamble PN code. The completion of transmission of the Acquisition/Preamble symbol is indicated with TXACQPLS, while the ongoing transmission of data symbols is signaled with TXTRKPLS. Data bits to be transmitted after the Acquisition/Preamble symbol are requested with TXBITPLS, where a single pulse requests data in BPSK mode and two pulses request data in QPSK mode. The user data symbols are then PN modulated using the Transmitter Data Symbol PN code.

The PN spreading codes are XORed with the data bits (in BPSK mode) or bit pairs (in QPSK mode) to transmit one complete code sequence for every Acquisition/Preamble and data symbol at all times. The resulting spread I and Q channel signals are brought out as the TXIOUT and TXQOUT signals for use by an external modulator and are also fed into the Z87200's internal on-chip modulator. In BPSK mode, only TXIOUT is used by the Z87200's modulator. If an external QPSK modulator is used, the carrier should be modulated as shown in Table 3 to be compatible with the Z87200 receiver.

Table 3. DQPSK Differential Encoder Sequence

I, Q Bits		Signal Quadrant	Quadrant Diagram	
0	0	First	2nd	1st
1	0	Second	3rd	4th
1	1	Third		
0	1	Fourth		

BPSK/QPSK Modulator

The Z87200 incorporates an on-chip BPSK/QPSK modulator which modulates the encoded and spread transmit signal with the sine and cosine outputs of the Z87200's NCO to generate a digitized I.F. output signal, $TXIFOUT_{7-0}$. Since the NCO operates at a rate defined by RXIFCLK, the BPSK/QPSK modulator output is also generated at this sampling rate, and, consequently, TXIFCLK must be held common with RXIFCLK to operate the Z87200's BPSK/QPSK Modulator. The digital modulator output signal can then be fed into an external 8-bit DAC (operating at RXIFCLK) to generate an analog I.F. transmit signal, where the chosen I.F. is the Z87200's programmed NCO frequency or one of its aliases with respect to the output sampling rate, RXIFCLK. Please note that operation of the BPSK/QPSK modulator is only specified to 20 MHz; that is, if RXIFCLK/TXIFCLK is greater than 20 MHz in the system design, it is recommended that the baseband transmit outputs of the Z87200 be used with an external BPSK/QPSK modulator.

When the Z87200 is set to transmit in BPSK mode (by setting bit 0 of address 40_H high), identical signals are applied to both the I and Q channels of the modulator so that the modulated output signal occupies only the first and third quadrants of the signal space defined in Note that the modulator itself cannot generate $\pi/4$ QPSK signals, but the Z87200 can receive such signals and can be used with an external modulator for their transmission.

4

FUNCTIONAL BLOCKS (Continued)

Frequency Control Register and NCO

The Z87200 incorporates a Numerically Controlled Oscillator (NCO) to synthesize a local oscillator signal for both the transmitter's modulator and receiver's downconverter. The NCO is clocked by the master receiver clock signal, RXIFCLK, and generates quadrature outputs with 32-bit frequency resolution. The NCO frequency is controlled by the value stored in the 32-bit Frequency Control Register, occupying 4 bytes at addresses 03_H to 06_H. To avoid destructive in-band aliasing, the NCO should not be programmed to be greater than 50% of RXIFCLK. As desired by the user, the output of the Z87200 receiver's Loop Filter can then be added or subtracted to adjust the NCO's frequency control word and create a closed-loop frequency tracking loop. If the receiver is disabled, either manually or automatically at the end of a burst, the Loop Filter output correcting the NCO's Frequency Control Word is disabled. When simultaneously operating both the transmitter and receiver, however, the receiver's frequency tracking loop affects the NCO signals to both the receive and transmit sides, a feature which can either be used to advantage in the overall system design or must be compensated in the programming of the Z87200 or in the system design.

Downconverter

The Z87200 incorporates a Quadrature (Single Sideband) Downconverter which digitally downconverts the sampled and digitized receive I.F. signal to baseband. Use of the Loop Filter and the NCO's built-in frequency tracking loop permits the received signal to be accurately downconverted to baseband.

The Downconverter includes a complex multiplier in which the 8-bit receiver input signal is multiplied by the sine and cosine signals generated by the NCO. In Quadrature Sampling Mode, two ADCs provide quadrature (complex) inputs I_{IN} and Q_{IN}, while, in Direct I.F. Sampling Mode, a single ADC provides I_{IN} as a real input. The input signals can be accepted in either two's complement or offset binary formats according to the setting of bit 3 of address 01_H. In Direct I.F. Sampling Mode, the unused RXQIN Q channel input (Q_{IN}) should be held to "zero" according to the ADC input format selected. The outputs of the Downconverter's complex multiplier are then:

$$I_{OUT} = I_{IN} \cdot \cos(\omega t) - Q_{IN} \cdot \sin(\omega t)$$

$$Q_{OUT} = I_{IN} \cdot \sin(\omega t) + Q_{IN} \cdot \cos(\omega t)$$

$$\text{where } \omega = 2\pi f_{nco}$$

These outputs are fed into the I and Q channel Integrate and Dump Filters. The Integrate and Dump Filters allow the samples from the complex multiplier (at the I.F. sampling rate, the frequency of RXIFCLK) to be integrated over a number of sample periods. The dump rate of these filters (the baseband sampling rate) can be controlled either by an internally generated dump clock or by an external input signal (RXMSMPL) according to the setting of bit 0 of address 01_H. Note that, while the receiver will extract exact PN and symbol timing information from the received signal, the baseband sampling rate must be twice the nominal PN chip rate for proper receiver operation and less than or equal to one-half the frequency of RXIFCLK. If twice the PN chip rate is a convenient integer sub-multiple of RXIFCLK, then an internal clock can be derived by frequency dividing RXIFCLK according to the divisor stored in bits 5-0 of address 02_H; otherwise, an external baseband sampling clock provided by RXMSMPL must be used.

The I.F. sampling rate, the baseband sampling rate, and the input signal levels determine the magnitudes of the Integrate and Dump Filters' accumulator outputs, and a programmable viewport is provided at the outputs of the Integrate and Dump Filters to select the appropriate output bits as the 3-bit inputs to the PN Matched Filter. The viewport circuitry here and elsewhere within the Z87200's receiver is designed with saturation protection so that extreme values above or below the selected range are limited to the correct maximum or minimum value for the selected viewport range. Both viewports for the I and Q channels of the Integrate and Dump Filters are controlled by the values stored in bits 7-4 of address 01_H.

Receiver PN Code Register and PN Matched Filter

As discussed for the Z87200 transmitter, the Z87200 receiver is designed for burst signal operation in which each burst begins with a single Acquisition/Preamble symbol and is then followed by data symbols for information transmittal. Complementing operation of the Z87200's transmitter, two separate and independent PN codes may be employed in the receiver's PN Matched Filter, one for despreading the Acquisition/Preamble symbol, and one for the information data symbols. The code lengths are completely independent of each other and can be each up to 64 chips long. A block diagram of the PN Matched Filter is shown in Figure 3.

The Z87200 contains a fully programmable 64-tap complex (dual I and Q channel) PN Matched Filter with coefficients which can be set to ±1 or zero according to the contents of either the Acquisition/Preamble or Data Symbol Code Coefficient Registers. By setting the coefficients of the end taps of the filter to zero, the effective length of the filter can be reduced for use with PN codes shorter than 64 bits. Power consumption may also be reduced by turning off those blocks of 7 taps for which all the coefficients are zero, using bits 6-0 of address 39H. Each ternary coefficient is stored as a 2-bit number so that a PN code of length N is stored as N 2-bit non-zero PN coefficients. Note that, as a convention, throughout this document the first PN Matched Filter tap encountered by the signal as it enters the I and Q channel tapped delay lines is referred to as "Tap 0." Tap 63 is then the last tap of the PN Matched Filter.

The start of each burst is expected to be a single symbol PN-spread by the Acquisition/Preamble code. The receiver section of the Z87200 is automatically configured into acquisition mode so that the Matched Filter Acquisition/Preamble Coefficients stored in addresses 07_H to 16_H are used to despread the received signal. Provided that this symbol is successfully detected, the receiver will automatically switch from acquisition mode, and the Matched Filter Data Symbol Coefficients stored in addresses 17_H to 26_H will then be used to despread subsequent symbols.

To allow the system to sample the incoming signal asynchronously (at the I.F. sampling rate) with respect to the PN spreading rate, the PN Matched Filter is designed to operate with two signal samples (at the baseband sampling rate) per chip. A front end processor (FEP) operating on both the I and Q channels averages the incoming data over each chip period by adding each incoming baseband sample to the previous one:

$$FEP_{OUT} = FEP_{IN} (1 + z^{-1})$$

After the addition, the output of the FEP is rounded to a 3-bit offset 2's complement word with an effective range of ±3.5 such that the rounding process does not introduce any bias to the data. The FEP can be disabled by setting bit 0 of address 27_H to 1, but for normal operation the FEP should be enabled.

The PN Matched Filter computes the cross-correlation between the I and Q channel signals and the locally stored PN code coefficients at the baseband sampling rate, which is twice per chip. The 3-bit signals from each tap in the PN Matched Filter are multiplied by the corresponding coefficient in two parallel tapped delay lines. Each delay line consists of 64 multipliers which multiply the delayed 3-bit signals by zero or ±1 according to the value of the tap coefficient. The products from the I and Q tapped delay lines are added together in the I and Q Adders to form the sums of the products, representing the complex cross-correlation factor. The correlation I and Q outputs are thus:

$$Output_{(I, Q)} = \sum_{n=0}^{n=63} Data_{n(I, Q)} * Coefficient_{n(I, Q)}$$

These I and Q channel PN Matched Filter outputs are 10-bit signals, with I and Q channel programmable viewports provided to select the appropriate output bits as the 8-bit inputs to the Power Detector and DPSK Demodulator blocks. Both I and Q channel viewports are jointly controlled by the data stored in bits 1-0 of address 28_H and are saturation protected.

Two power saving methods are used in the PN Matched Filter of the Z87200. As discussed previously, the first method allows power to be shut off in the unused taps of the PN Matched Filter when the filter length is configured to be less than 64 taps. The second method is a proprietary technique that (transparently to the user) shuts down the entire PN Matched Filter during portions of each symbol period.

FUNCTIONAL BLOCKS (Continued)

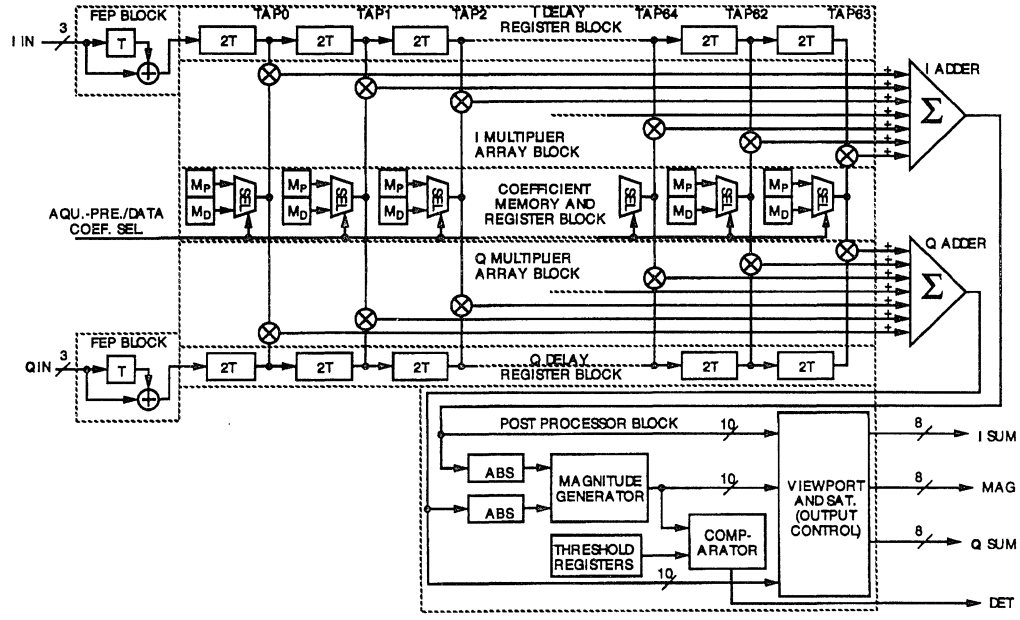

Figure 7. PN Matched Filter

Power Detector

The complex output of the PN Matched Filter is fed into a Power Detector which, for every cycle of the internal baseband sampling clock, computes the magnitude of the vector of the I and Q channel correlation sums,

$$\sqrt{}$$

$I^2(K)+Q^2(k)$, where the magnitude is approximated as

$$\text{Max}\{\text{Abs}(I),\text{Abs}(Q)\} + 1/2\ \text{Min}\{\text{Abs}(I), \text{Abs}(Q)\}.$$

This 10-bit value represents the power level of the correlated signal during each chip period and is used in the Symbol Tracking Processor.

Symbol Tracking Processor

The output of the Power Detector Block represents the signal power during each chip period. Ideally, this output will have a high peak value once per symbol (that is, once per PN code cycle) when the code sequence of the received signal in the PN Matched Filter is the same as (and is aligned in time with) the reference PN code used in the PN Matched Filter. At that instant, the I and Q channel outputs of the PN Matched Filter are, theoretically, the optimally despread I and Q symbols.

To detect this maximum correlation in each symbol period, the signal power value is compared against a 10-bit user-programmable threshold value. A symbol clock pulse is generated each time the power value exceeds the threshold value to indicate a symbol detect. Since the Acquisition/Preamble symbol and subsequent data symbols can have different PN codes with different peak correlation values (which depend on the PN code length and code properties), the Z87200 is equipped with two separate threshold registers to store the Acquisition/Preamble Threshold value (stored in addresses 29_H and $2A_H$) and the Data Symbol Threshold value (stored in addresses $2B_H$ and $2C_H$). The device will automatically use the appropriate value depending on whether it is in acquisition mode or not.

Since spread-spectrum receivers are frequently designed to operate under extremely adverse signal-to-noise ratio conditions, the Z87200 is equipped with a "flywheel circuit" to enhance the operation of the symbol tracking function by introducing memory to the PN Matched Filter operation. This circuit is designed to ignore false detects at inappropriate times in each symbol period and to insert a symbol clock pulse at the appropriate time if the symbol detection is missed. The flywheel circuit operates by its *a priori* knowledge of when the next detect pulse is expected. *A priori*, the expected pulse will occur one symbol period after the last correctly detected one, and a window of ±1 baseband sample time is therefore used to gate the detect pulse. Any detects generated outside this time window are ignored, while a symbol detect pulse will be inserted into the symbol clock stream if the power level does not exceed the threshold within the window, corresponding to a missed detect. An inserted symbol detect signal will be generated precisely one symbol after the last valid detect, the nominal symbol length being determined by the value of Rx Chips Per Data Symbol stored in address $2D_H$.

The cross-correlation characteristics of a noisy received signal with the noise-free local PN code used in the Z87200's PN Matched Filter may result in "smearing" of the peak power value over adjacent chip periods. Such smearing can result in two or three consecutive power values (typically, the on-time and one-sample early and late values) exceeding the threshold. A maximum power selector circuit is incorporated in the Z87200 to choose the highest of any three consecutive power levels each time this occurs, thereby enhancing the probability that the optimum symbol timing will be chosen in such cases. If desired, this function can be disabled by setting bit 3 of address 30_H high.

The Z87200 also includes a circuit to keep track of missed detects; that is, those cases where no peak power level exceeds the set threshold. An excessively high rate of missed detects is an indication of poor signal quality and can be used to abort the reception of a burst of data. The number of symbols expected in each receive burst, up to a maximum of 65,533, is stored in addresses $2E_H$ and 30_H. A counter is used to count the number of missed detects in each burst, and the system can be configured to automatically abort a burst and return to acquisition mode if this number exceeds the Missed Detects per Burst Threshold value stored in address $2F_H$. Under normal operating conditions, the Z87200 will automatically return to acquisition mode when the number of symbols processed in the burst is equal to the value of the data stored in address $2E_H$ and 30_H. To permit the processing of longer bursts or continuous data, this function can be disabled by setting bit 6 of address 30_H high.

Differential Demodulator

Both DPSK demodulation and carrier discrimination are supported in the Z87200 receiver by the calculation of "Dot" and "Cross" products using the despread I and Q channel information generated by the PN Matched Filter for the current and previous symbols. A block diagram of the DPSK Demodulator's I and Q channel processing is shown in Let I_k and Q_k represent the I and Q channel outputs, respectively, for the k^{th} symbol. The Dot and Cross products can then be defined as:

$$\text{Dot}(k) = I_k I_{k-1} + Q_k Q_{k-1}; \text{ and,}$$

$$\text{Cross}(k) = Q_k I_{k-1} - I_k Q_{k-1}.$$

Examination of these products in the complex plane reveals that the Dot and Cross products are the real and imaginary results, respectively, of complex multiplication of the current and previous symbols. The Dot product alone thus allows determination of the phase shift between successive BPSK symbols, while the Dot and Cross products together allow determination of the integer number of $\pi/2$ phase shifts between successive QPSK symbols. Differential encoding of the source data implies that an absolute phase reference is not required, and thus knowledge of the phase shift between successive symbols derived from the Dot and Cross products unambiguously permits correct demodulation.

Implementation of this approach is simplified if the polarities (the signs) alone of the Dot and Cross products provide the information required to make the correct symbol decision. For BPSK and $\pi/4$ QPSK signals, no modifications are needed: in BPSK, the sign of the Dot product fully captures the signal constellation, while, in $\pi/4$ QPSK, the signal constellation intrinsically includes the phase rotation needed to align the decision boundaries with the four possible combinations of the Dot and Cross product polarities. For QPSK signals, a fixed phase rotation of $\pi/4$ (45°) is introduced in the DPSK Demodulator to the previous symbol to simplify the decision algorithm. Rotation of the previous symbol is controlled by the settings of bits 0 and 1 of address 33_H, allowing the previous symbol to be rotated by 0° or ±45°. As noted, for BPSK or $\pi/4$ QPSK signals, a rotation of 0° should be programmed, but, for QPSK signals,

FUNCTIONAL BLOCKS (Continued)

a –45° signal rotation must be programmed to optimize the constellation boundaries in the comparison process between successive symbols. Note also that introduction of a ±45° rotation introduces a scaling factor of $1/\sqrt{2}$ to the signal level in the system as discussed in Theory of Operation, where this factor should be taken into account when calculating optimum signal levels and viewport settings after the DPSK Demodulator

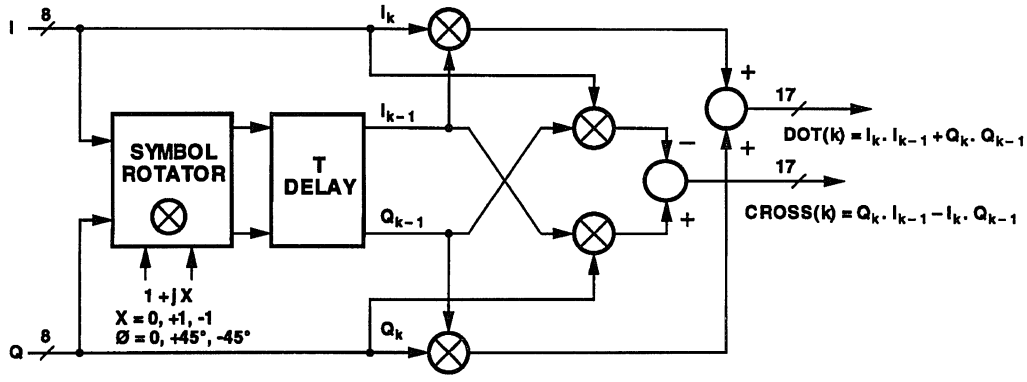

Figure 8. DPSK Demodulator I and Q Channel Processing

Frequency Discriminator and Loop Filter

The Frequency Discriminator uses the Dot and Cross products discussed above to generate the AFC signal for the frequency acquisition and tracking loop, as illustrated in The specific algorithm used depends on the signal modulation type and is controlled by the setting of bit 2 of address 33_H. When bit 2 is set low, the Frequency Discriminator circuit is in BPSK mode and the following algorithm is used to compute the Frequency Discriminator (FD) function:

$$FD = Cross \times Sign[Dot],$$

where Sign[.] represents the polarity of the argument. When bit 2 is set high, the discriminator circuitry is in QPSK mode and the carrier discriminator function is instead calculated as:

$$FD = (Cross \times Sign[Dot]) - (Dot \times Sign[Cross]).$$

In both cases, the Frequency Discriminator function provides an error signal that reflects the change in phase between successive symbols. With the symbol period known, the error signal can equivalently be seen as a frequency error signal. As a practical matter, the computation of the Frequency Discriminator function results in a 17-bit signal, and a programmable saturation protected viewport is provided to select the desired output bits as the 8-bit input to the Loop Filter Block. The viewport is controlled by the value stored in bits 7-4 of address 33_H.

The Loop Filter is implemented with a direct gain (K1) path and an integrated or accumulated (K2) path to filter the Frequency Discriminator error signal and correct the frequency tracking of the Downconverter. The order of the Loop Filter transfer function can be set by enabling or disabling the K1 and K2 paths, and the coefficient values can be adjusted in powers of 2 from 2^0 to 2^{21}. The Loop Filter transfer function is:

$$\text{Transfer Fn.} = K1 + 1/4\ K2$$

The factor of 1/4 results from truncation of the 2 LSBs of the signal in the integrator path of the loop so that, when added to the signal in the direct path, the LSBs of the signals are aligned. The coefficients K1 and K2 are defined by the data stored in bits 4-0 of addresses 35_H and 34_H, respectively. In addition, bit 5 of addresses 35_H and 34_H control whether the K1 and K2 paths, respectively, are enabled. These parameters thus give the user full control of the Loop Filter characteristics.

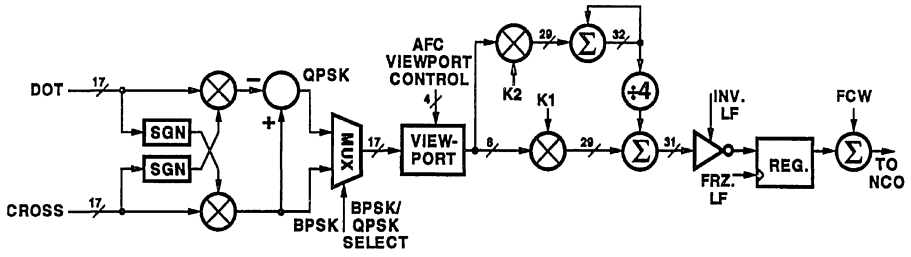

Figure 9. Frequency Discriminator and Loop Filter Detail

4

$RXIIN_{7-0}$ (Pins 91-98)

Receiver In-Phase Input. RXIIN is an 8-bit input port for in-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. The sampling rate of the RXIIN signals (the I.F. sampling rate of the A/Ds) may be independent of the baseband sampling rate (the Down-converter integrate and dump rate) and the PN chip rate, but must be equal to RXIFCLK and at least two times greater than the baseband sampling rate. Since the baseband sampling rate must be set at twice the PN chip rate, the I.F. sampling rate must thus be at least four times the PN chip rate. Data on the pins is latched and processed by RXIFCLK.

$RXQIN_{7-0}$ (Pins 2-9)

Receiver Quadrature-Phase Input. RXQIN is an 8-bit input port for quadrature-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. As with RXIIN, the sampling rate of the RXQIN signals may be independent of the baseband sampling and PN chip rates in the receiver, but must be at least two times greater than the baseband sample rate (or, equivalently, at least four times greater than the PN chip rate). Data on the pins is latched and processed by RXIFCLK.

FUNCTIONAL BLOCKS (Continued)

Note that if the Z87200 is to be used in Direct I.F. Sampling Mode, then the I.F. signal should be input to the RXIIN input port only. RXQIN must then be held to arithmetic zero according to the chosen ADC format as selected by bit 3 of address 01_H. In other words, to support Direct I.F. Sampling, RXQIN must be tied to a value of 127 or 128 if offset binary input format has been selected or to a value of 0 if two's complement input format has been selected.

RXMSMPL (Pin 84)
Receiver Manual Sample Clock. RXMSMPL enables the user to externally generate (independent of the I.F. sampling clock, RXIFCLK) the baseband sampling clock used for all processing after the digital downconverter, including the dump rate of the Integrate and Dump filters. This feature is useful in cases where a specific baseband sample rate is required that may not be derived by the internal sample rate timing generator which generates clock signals at integer sub-multiples of RXIFCLK. The signal is internally synchronized to RXIFCLK to avoid intrinsic race or hazard timing conditions. There must be at least two cycles of RXIFCLK to every cycle of RXMSMPL, and RXMSMPL should be set to twice the nominal receive PN chip rate.

When bit 0 of address 01_H is set high, a rising edge on RXMSMPL will initiate a baseband sampling clock pulse to the Integrate and Dump filters and subsequent circuitry (e.g., PN Matched Filter, DPSK Demodulator, Power Estimator, etc.). The rising edge of RXMSMPL is synchronized internally so that, on the second rising edge of RXIFCLK that follows the rising edge of RXMSMPL, a pulse is internally generated that clocks the circuitry that follows. On the third rising RXIFCLK edge, the contents of the Integrate and Dump Filters of the Downconverter are transferred to the PN Matched Filter. The extra one RXIFCLK delay before transfer of the contents of the filters enables the internally generated baseband sampling clock to be free of race conditions at the interface between the Downconverter and PN Matched Filter.

RXMDET (Pin 88)
Receiver Manual Detect. RXMDET enables the user to externally generate symbol timing, bypassing and overriding the internal symbol power estimation and tracking circuitry. This function may be useful when the dynamic characteristics of the transmission environment require unusual adjustments to the symbol timing.

When bit 0 of address 30_H is set high (Manual Detect Enable) and when bit 0 of address 31_H is set low, a rising edge of RXMDET will generate a symbol correlation detect pulse. The function can also be performed by means of bit 0 of address 31_H. The RXMDET input and bit 0 of address 31_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the manual detect function. The rising edge of RXMDET is synchronized internally so that, on the second rising edge of the baseband sampling clock that follows the rising edge of RXMDET, the correlated outputs of the PN Matched Filter I and Q channels will be transferred to the DPSK demodulator.

RXMABRT (Pin 87)
Receiver Manual Abort. RXMABRT enables the user to manually force the Z87200 to cease reception of the current burst of data symbols and prepare for acquisition of a new burst. This function can be used to reset the receiver and prepare to receive a priority transmission signal under precise timing control, giving the user the ability to control the current status of the receiver for reasons of priority, signal integrity, etc.

When bit 0 of address 32_H is set low, a rising edge on RXMABRT will execute the abort function. The function can also be performed under microprocessor control by means of bit 0 of address 32_H. The RXMABRT input and bit 0 of address 32_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the abort function. The second rising edge of the baseband sampling clock that follows a rising edge of RXMABRT will execute the abort and also clear the symbols-per-burst, samples-per-symbol, and missed-detects-per-burst counters. The counters will be reactivated on the detection of the next burst preamble or by a manual detect signal.

RXIFCLK (Pin 12)
Receiver I.F. Clock. RXIFCLK is the master clock of the NCO and all the receiver blocks. All clocks in the receiver section and the NCO, internal or external, are generated or synchronized internally to the rising edge of RXIFCLK. The frequency of RXIFCLK must be at least four times the PN chip rate of the received signal. When bit 0 of address 01_H is set low, the baseband sampling clock, required to be at twice the nominal PN chip rate, will be derived from RXIFCLK according to the setting of bits 5-0 of address 02_H.

MNCOEN (Pin 86)
Manual NCO Enable. MNCOEN allows the power consumed by the operation of the NCO circuitry to be minimized when the Z87200 is not receiving and not transmitting data. The NCO can also be disabled while the Z87200 is transmitting as long as the Z87200's on-chip BPSK/QPSK modulator is not being used. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MNCOEN low holds the NCO in a reset state; setting MNCOEN high then reactivates the NCO, where it is necessary to then reload the frequency control word into the

NCO. Note that MNCOEN operates independently of MTXEN and MRXEN, where those pins have similar control over the transmit and receive circuitry, respectively.

MNCOEN performs the same function as bit 0 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 0 of address 37_H is set low, MNCOEN controls the activity of the NCO circuitry; when MNCOEN is set low, bit 0 of address 37_H controls the activity of the NCO circuitry. When either bit 0 or MNCOEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following RXIFCLK cycle to effectively disable all of the NCO circuitry, although the user programmable control registers are not affected by this power down sequence.

Upon reactivation (when either MNCOEN or bit 0 of address 37_H return high), the NCO must be reloaded with frequency control information either by means of the MFLD input or by writing 01_H into address 00_H.

MTXEN (Pin 17)

Manual Transmitter Enable. A rising edge on MTXEN causes the transmit sequence to begin, where the Z87200 first transmits a single Acquisition/Preamble symbol followed by data symbols. MTXEN should be set low after the last symbol has been transmitted. When MTXEN is set low, power consumption of the transmitter circuit is minimized. MTXEN operates independently of MRXEN and MNCOEN, where these signals have similar control over the receive and NCO circuitry, respectively.

MTXEN performs the same function as bit 1 of address 37_H. and these two signals are logically ORed together to form the overall control function. When bit 1 of address 37_H is set low, MTXEN controls the activity of the transmitter circuitry, and, when MTXEN is set low, bit 1 of address 37H controls the activity of the transmitter circuitry. A rising edge on either MTXEN or bit 1 (whichever is in control, as defined above) initiates a transmit sequence. A falling edge initiates a reset sequence on the following TXIFCLK cycle to disable all of the transmitter data path, although the user programmable control registers are not affected by the power down sequence.

MRXEN (Pin 10)

Manual Receiver Enable. MRXEN allows power consumption of the Z87200 receiver circuitry to be minimized when the device is not receiving. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MRXEN low reduces the power consumption substantially. When MRXEN is set high, the receiver will automatically power up in acquisition mode regardless of its prior state when it was powered down. MRXEN operates independently of MTXEN and MNCOEN, where these signals have similar control over the transmit and NCO circuitry, respectively.

MRXEN performs the same function as bit 2 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 2 of address 37_H is set low, MRXEN controls the activity of the receiver circuitry and, when MRXEN is set low, bit 2 of address 37_H controls the activity of the receiver circuitry. When either MRXEN or bit 2 (whichever is in control, as defined above) goes low, a reset sequence begins on the following RXIFCLK cycle and continues through a total of six RXIFCLK cycles to virtually disable all of the receiver data paths. The user-programmable control registers are not affected by the power-down sequence, with the exception of $RXTEST_{7-0}$ Function Select (address 38_H), which is reset to 0. If the $RXTEST_{7-0}$ bus is being used to read any function other than the PN Matched Filter I and Q inputs, the value required must be rewritten after re-enabling the receiver.

TXIN (Pin 18)

Transmit Input. TXIN supports input of the information data to be transmitted by the Z87200. In BPSK mode, the transmitter requires one bit per symbol period; in QPSK mode, two bits are required per symbol period.

To initiate and enable transmission of the data, the user must raise MTXEN high. Data for transmission is requested with TXBITPLS, where one or two pulses per symbol are generated depending on whether the device is in BPSK or QPSK mode as set by bit 0 of address 40_H. To allow monitoring of the state of the transmitter, the Z87200 will pulse TXACQPLS after the initial Acquisition/Preamble symbol is transmitted; the transmission of each subsequent symbol is indicated by pulses of TXTRKPLS.

If programmed for BPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where TKBITPLS is generated once per symbol, one chip period before the end of the current symbol. At the end of the symbol duration, the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value, and is generated repeatedly at the symbol rate as long as the input signal MTXEN remains high.

In QPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where this signal is generated twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle before latching the TXIN data into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value.

FUNCTIONAL BLOCKS (Continued)

TXMCHP (Pin 19)
Transmit Manual Chip Pulse. TXMCHP enables the user to provide the PN chip rate clock pulses from an external source. This feature is useful in cases where a specific chip rate is required that cannot be derived by the internal clock generator which generates clocks of integer submultiples of TXIFCLK. The signal is internally synchronized to TXIFCLK to avoid intrinsic race or hazard timing conditions.

When bit 2 of address 40_H is set high, a rising edge on TXMCHP will generate the chip clock to the differential encoder and the following circuitry (Acquisition/Preamble and Data Symbol PN spreaders, etc.). The rising edge of TXMCHP is synchronized internally so that, on the third rising edge of TXIFCLK following the rising edge of TXMCHP, the PN code combined with the differentially encoded signal will change, generating the next chip.

TXIFCLK (Pin 14)
Transmitter I.F. Clock. TXIFCLK is the master clock of the transmitter. All transmitter clocks, internal or external, are generated or synchronized internally to the rising edge of TXIFCLK. The rate of TXIFCLK must be at least twice the transmit PN chip rate. It may be convenient to use the same external signal for both TXIFCLK and RXIFCLK, in which case the frequency of TXIFCLK will be at least four times the PN chip rate as required for RXIFCLK. Moreover, if the Z87200's on-chip BPSK/QPSK Modulator is to be used, TXIFCLK and RXIFCLK must be identical and should not exceed 20 MHz.

MFLD (Pin 85)
Manual Frequency Load. MFLD is used to load a frequency control value into the NCO. The NCO may be loaded in various ways, but MFLD provides a synchronized external method of updating the NCO, while the other methods involve setting bit 0 of address 00H or using the programmable loop filter timing circuitry. MFLD is internally synchronized to RXIFCLK to avoid internal race or hazard timing conditions.

The MFLD input and bit 0 of address 00H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the frequency load function manually. The rising edge of MFLD is synchronized internally so that, on the sixth following rising edge of RXIFCLK, the frequency control word is completely registered into the NCO accumulator. The frequency load command must not be repeated until the six RXIFCLK cycle delay is completed.

/WR (Pin 28)
Write Bar. /WR is used to latch user-configurable information into the control registers. It is important to note that the control registers are transparent latches while /WR is set low. The information will be latched when /WR returns high. $DATA_{7-0}$ and $ADDR_{6-0}$ should be stable while /WR is set low in order to avoid undesirable effects.

$DATA_{7-0}$ (Pins 20-27)
Data Bus. $DATA_{7-0}$ is an 8-bit microprocessor interface bus that provides access to all internal control register inputs for programming. $DATA_{7-0}$ is used in conjunction with the $ADDR_{6-0}$ and /WR signals to set the values of the control registers.

$ADDR_{6-0}$ (Pins 32-38)
Address Bus. $ADDR_{6-0}$ is a 7-bit address bus that selects the control register location into which the information provided on the $DATA_{7-0}$ bus will be written. $ADDR_{6-0}$ is used in conjunction with /WR and $DATA_{7-0}$ to write the information into the registers.

/CSEL (Pin 29)
Chip Select Bar. /CSEL is provided to enable or disable the microprocessor operation of the Z87200. When /CSEL is set high, the $ADDR_{6-0}$ and /WR become disabled and have no effect on the device. When /CSEL is set low, the device is in its normal mode of operation and $ADDR_{6-0}$ and /WR are active.

/OEN (Pin 49)
Output Enable Bar. /OEN is provided to enable or disable the $RXTEST_{7-0}$ output bus. When /OEN is set high, the $RXTEST_{7-0}$ bus will have a high impedance, allowing it to be connected to other busses, such as $DATA_{7-0}$. When /OEN is set low, the $RXTEST_{7-0}$ bus will be active, allowing the RXTEST function selected to be accessed.

/RESET (Pin 16)
Reset Bar. /RESET is the master reset of the Z87200, clearing the control registers as well as the contents within the receiver, transmitter, and NCO data paths when it is set low. Setting /RESET high enables operation of the circuitry.

OUTPUT SIGNALS

TXIOUT (Pin 77)
Transmitter In-Phase Output. TXIOUT is the in-phase output transmission signal that has been differentially encoded and PN spread. TXIOUT changes on the rising edge of TXIFCLK following the falling edge of TXCHPPLS.

TXQOUT (Pin 76)
Transmitter Quadrature-Phase Output. TXQOUT is the quadrature-phase output transmission signal that has been differentially encoded and PN spread. TXQOUT changes on the rising edge of TXIFCLK following the falling edge of TXCHPPLS.

$TXIFOUT_{7-0}$ (Pins 66-73)
Transmitter I.F. Output. $TXIFOUT_{7-0}$ is the modulated transmit output signal from the on-chip BPSK/QPSK modulator. The signal is composed of the sum of the modulated TXIOUT and TXQOUT signals, modulated by the NCO cosine and sine outputs, respectively. Since the modulator is driven by the Z87200's NCO, $TXIFOUT_{7-0}$ changes on the rising edges of RXIFCLK, and operation of the BPSK/QPSK modulator requires that RXIFCLK and TXIFCLK be identical and their common frequency not exceed 20 MHz. $TXIFOUT_{7-0}$ may be in either two's complement or offset binary format according to the setting of bit 1 of address 40_H.

TXACQPLS (Pin 60)
Transmitter Acquisition Pulse. TXACQPLS is an output signal generated at the final chip of the Acquisition/Preamble symbol. The Acquisition/Preamble symbol is generated automatically by the Z87200 upon user command (either via bit 1 of address 37_H or MTXEN input) and immediately precedes transmission of user data. TXACQPLS is then provided to the user to indicate when the final chip of the Acquisition/Preamble symbol is being transmitted.

TXBITPLS (Pin 63)
Transmitter Bit Pulse. TXBITPLS is an output signal used to support transmission timing of user data for either BPSK or QPSK modes, as programmed by bit 0 of 40_H.

In BPSK mode, user-provided data is requested by the Z87200 by a rising edge of TXBITPLS once per symbol. TXBITPLS requests the data one chip period before the TXIN data is latched into the device, and TXBITPLS falls low immediately following the rising edge of TXIFCLK, where TXIFCLK latches the TXIN value.

In QPSK mode, user-provided data is requested by the Z87200 by a rising edge of output signal TXBITPLS which occurs twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle period before the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, where TXIFCLK latches the TXIN value.

In both BPSK and QPSK modes, the data must be valid on the second rising edge of TXIFCLK after the rising edge of TXBITPLS.

TXCHPPLS (Pin 62)
Transmitter Chip Pulse. TXCHPPLS is an output signal used to support transmission timing for the device. TXCHPPLS pulses high for one TXIFCLK cycle at the PN chip rate defined by the user. The chip rate is set either by programming a value in bits 5-0 of address 41_H or through use of the external TXMCHP signal.

TXTRKPLS (Pin 61)
Transmitter Data Track Pulse. TXTRKPLS is an output signal that allows monitoring of data symbol transmissions. A rising edge of output signal TXTRKPLS occurs one chip period before the end of the current data symbol transmission. TXTRKPLS then falls low immediately following the rising edge of TXIFCLK.

TXACTIVE (Pin 78)
Transmitter Active. A high level on TXACTIVE indicates that the transmitter is sending data symbols. This signal will be set high at the end of the Acquisition/Preamble symbol, indicating the start of the first chip of the first data symbol at the TXIOUT and TXQOUT pins. It will be set low at the end of the last chip period of the last data symbol of the burst at the TXIOUT and TXQOUT pins.

RXOUT (Pin 57)
Receiver Output. RXOUT is the output data of the receiver following downconversion, despreading and demodulation. In BPSK mode, one data bit is provided per symbol; in QPSK mode, two data bits are provided per symbol with a half-symbol separation between the bits. Note that, when the Z87200 is operated in burst mode, the data will be invalid during the first symbol of each burst; that is, in BPSK mode the first bit will be invalid, and in QPSK mode the first two bits will be invalid.

RXIOUT (Pin 56)
Receiver I Channel Output. RXIOUT is the I channel output data before dibit-to-serial conversion. RXIOUT can be used in conjunction with the RXQOUT signal in applications where the QPSK output data is required as parallel bit pairs. Note that, when the Z87200 is operated in burst mode, the first bit of RXIOUT in each burst will be invalid RXQOUT (Pin 55).

Receiver Q Channel Output. RXQOUT is the Q channel output data before dibit-to-serial conversion. RXQOUT can be used in conjunction with the RXIOUT signal in applications where the QPSK data is required as parallel bit

OUTPUT SIGNALS (Continued)

pairs. Note that, when the Z87200 is operated in burst mode, the first bit of RXQOUT in each burst will be invalid.

/RXDRDY (Pin 54)
Receiver Data Ready Bar. /RXDRDY is provided as a receiver timing signal. /RXDRDY is normally set high and pulses low during the baseband sampling clock cycle when a new RXOUT signal is generated.

RXSPLPLS (Pin 53)
Receiver Sample Pulse. RXSPLPLS is an output timing signal that provides internal timing information to the user. RXSPLPLS is the internally generated baseband sampling clock, referenced either externally or internally according to the setting of bit 0 of address 01_H. All receiver functions, excluding those in the Downconverter, trigger internally on the rising edge of RXSPLPLS.

RXSYMPLS (Pin 52)
Receiver Symbol Pulse. RXSYMPLS is an output signal that provides the user internal timing information relative to the detection/correlation of symbols. Symbol information from the PN Matched Filter, DPSK Demodulator, and Output Processor is transferred on the rising edge of RXSPLPLS preceding the falling edge of RXSYMPLS.

RXACTIVE (Pin 83)
Receiver Active. A high level on RXACTIVE indicates that the receiver has detected an Acquisition/Preamble symbol and is currently receiving data symbols. RXACTIVE will be set high one bit period before the first rising edge of /RXDRDY, indicating that the first data bit is about to appear at the RXOUT, RXIOUT, and RXQOUT pins. RXACTIVE will be set low immediately following the last rising edge of /RXDRDY, indicating that the last data bit of the burst has been output at the RXOUT, RXIOUT, and RXQOUT pins. $RXTEST_{7-0}$ (Pins 41-48)

These pins provide access to 16 test points within the receiver as shown in The pin outputs are selected according to the value in bits 3-0 of address 38_H and the assignments shown in When one of these 4-bit values is written into address 38_H, the corresponding function becomes available at the $RXTEST_{7-0}$ outputs. The $RXTEST_{7-0}$ bus is a tri-state bus and is controlled by the OEN input. Note that the validity of the $RXTEST_{7-0}$ outputs at RXIFCLK speeds greater than 20 MHz is dependent on the output selected: outputs that change more rapidly than once per symbol may be indeterminate.

Table 4. Receiver Test Functions

	$RXTEST_{7-0}$ Output							
Bits 3-0 of 38_H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0_H			MFQIN 2-0 Matched Filter Q Input			MFIN2-0 Matched Filter I Input		
1_H	$Pk\text{-}Power_{9-2}$ MF Peak Magnitude Output (Changes Once Per Symbol)							
2_H	COS_{7-0} Cosine Output of NCO (Changes Every Cycle of RXIFCLK)							
3_H	SIN_{7-0} Sine Output of NCO (Changes Every Cycle of RXIFCLK)							
4_H	$DCIOUT_{16-9}$ Downconverter I Channel Output (Changes at RXIFCLK Rate)							
5_H	$DCQOUT_{16-9}$ Downcounter Q Output (Changes at RXIFCLK Rate)							
6_H	$ISUM_{9-2}$ Matched Filter I Output (Changes Twice Per Chip)							
7_H	$QSUM_{9-2}$ Matched Filter Q Output (Changes Twice Per Chip)							
8_H	$POWER_{9-2}$ MF Magnitude Output (Changes Twice Per Chip)							
9_H	$ISUM_{7-0}$ MF Viewpoint I Output (Changes Twice Per Chip)							
A_H	$QSUM_{7-0}$ MF Viewpoint Q Output (Changes Twice Per Chip)							
B_H	$Pk\text{-}ISUM_{7-0}$ MF Peak I Channel Output (Changes Once Per Symbol)							
C_H	$Pk\text{-}QSUM_{7-0}$ MF Peak Q Channel Output (Changes Once Per Symbol)							
D_H	DOT_{16-9} Dot Product (Changes Once Per Symbol)							
E_H	$CROSS_{16-9}$ Cross Product (Changes Once Per Symbol)							
F_H	$TXFBK_{7-0}$ Loopback Test Output							

All signals available at this port, with one exception, are expressed as two's complement values, ranging from –128 to +127 (80_H to $7F_H$). The PN Matched Filter power output values, available when the value in bits 3-0 of address 38_H is set to either 1_H or 8_H, is an unsigned binary number, ranging from 0 to 255 (0_H to FF_H).

The reset sequence that occurs when the receiver is disabled will also reset the contents of address 38_H to a value of 0. If the $RXTEST_{7-0}$ bus is to be used to observe any function other than the PN Matched Filter I and Q inputs, then the appropriate value must be rewritten.

TXTEST (Pin 59)

Transmitter Test Output. TXTEST provides access to 3 test points within the transmitter as shown in The pin output is selected according to the state of the two least significant bits of the address line, $ADDR_{1-0}$ and the assignments shown in Table 5. Note that this method of accessing the transmitter test points is completely different than the method by which the receiver test points are accessed. The state of the other address lines does not affect this function, and this function is always enabled. The availability of TXTEST output signals is only supported for TXIFCLK speeds less than 20 MHz; output with clock speeds greater than 20 MHz will be indeterminate.

Table 5. Transmitter Test Functions

$ADDR_{1-0}$	TXTEST	Description
0_H	ISM	Unspread I Symbol
1_H	QSYM	Unspread Q Symbol
2_H	SCODE	Spreading Code

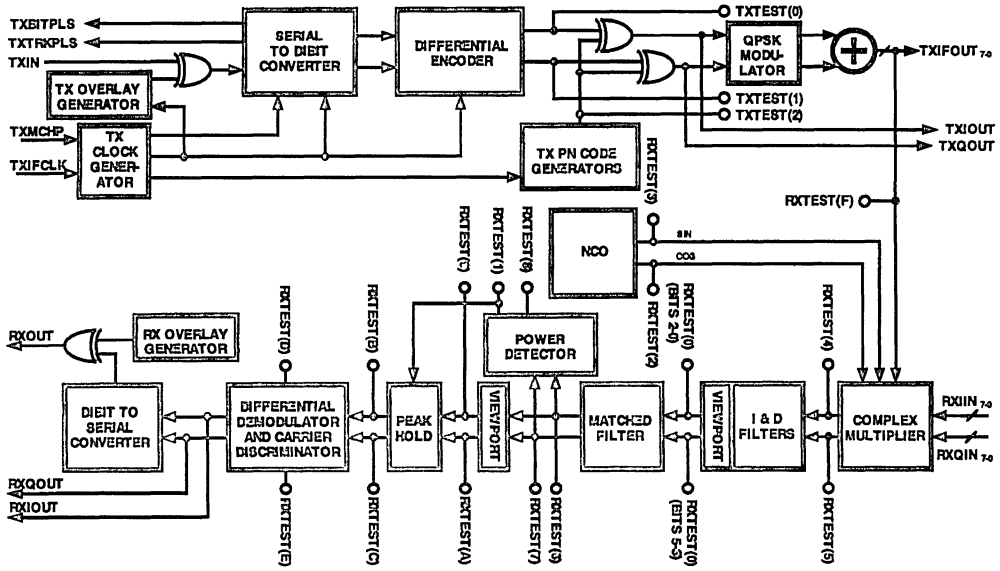

Figure 10. Transmitter and Receiver Test Points

CONTROL REGISTERS

Setting the Control Registers

The majority of the Z87200 control registers are completely independent and can be set or modified in any order. Two exceptions, however, exist:

- First, any time that the NCO is disabled, either through use of pin MNCOEN or bit 0 of address 37_H, the frequency control word must be reloaded, either through use of pin MFLD or bit 0 of address 00_H, once the NCO is re-enabled.
- Second, setting bit 2 of address 37_H to zero to disable the receiver will also cause the data in address 38_H to be set to zero, thereby possibly changing the receiver test point(s) that will be observed on the RXTEST pins. Address 38_H must be loaded with its desired value after bit 2 of address 37_H is again set to 1.

Downconverter Registers

Address 00_H:

Bit 0 — Frequency Control Word Load

This bit is used to load a frequency control value into the NCO, thereby changing its output frequency. The signal is internally synchronized to RXIFCLK to avoid intrinsic race or hazard timing conditions.

The loading of the NCO may be performed by various means. Setting this bit provides a synchronized internal means to control update of the NCO. Alternatively, the MFLD pin or the Z87200's programmable loop filter timing circuitry may be used.

The MFLD input and bit 0 of address 00_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the frequency load function manually. The rising edge of this bit is synchronized internally so that, on the following sixth rising edge of RXIFCLK, the frequency control word is completely registered into the NCO accumulator. The frequency load command must not be repeated until after a delay of six RXIFCLK cycles.

Address 01_H:

Bit 0 — Manual Sample Clock Enable

This bit selects the source of the internal baseband sampling clock, which should be at twice the nominal PN chip rate. The clock reference may be either supplied externally by RXMSMPL or generated internally from RXIFCLK.

When this bit is set high, the baseband sampling rate of the receiver is controlled by the external RXMSMPL signal. When it is set low, the sampling clock is generated internally (at a rate determined by the Sample Rate Control counter and set by bits 5-0 of address 02_H) and the RXMSMPL input is ignored.

Bit 1 — Invert Loop Filter Value

This bit allows the sign of the output signal from the loop filter to be inverted, thereby negating the value of the signal. The capability to invert the loop filter value permits the carrier frequency error component generated in the demodulator to be either added to or subtracted from the Frequency Control Word of the NCO. The correct setting will depend on several factors, including whether high-side or low-side downconversion is used.

When this bit is set low, the loop filter output is negated before being summed with the Frequency Control Word of the NCO and is thus subtracted from the FCW; when this bit is set high, the loop filter output is not negated and is added to the FCW.

Bit 2 — NCO Accumulator Carry In

This bit is primarily used as an internal test function and should be set low for normal operation. When this bit is set high, 1 LSB is added to the NCO accumulator each clock cycle. When it is set low, the NCO accumulator is not affected.

Bit 3 — Two's Complement Input

The $RXIIN_{7-0}$ and $RXQIN_{7-0}$ input signals can be in either two's complement or offset binary formats. Since all internal processing in the device operates with two's complement format signals, it is necessary to convert the $RXIIN_{7-0}$ and $RXQIN_{7-0}$ inputs in offset binary format to two's complement format by inverting the MSBs.

When this bit is set high, the device expects two's complement format inputs on $RXIIN_{7-0}$ and $RXQIN_{7-0}$. When it is set low, the device expects offset binary format on $RXIIN_{7-0}$ and $RXQIN_{7-0}$. In two's complement format, the 8-bit input values range from –128 to +127 (80_H to $7F_H$); in offset binary format, the values range from 0 to +255 (00_H to FF_H).

Bits 7-4 — Integrate and Dump Filter Viewport Control
The Z87200 incorporates viewport (data selector) circuitry to select any three consecutive bits from the 14-bit output of the Integrate and Dump (I & D) Filters in the Downconverter block as the 3-bit inputs to the dual-channel PN Matched Filter. The signal levels of the Integrate and Dump Filter I and Q outputs reflect the input signal levels and the number of samples integrated before the filter contents are "dumped," where the number of samples is determined by the baseband sampling rate (nominally, twice the PN chip rate) and the I.F. sampling rate (RXIFCLK). Setting the viewport thus effectively normalizes the I & D Filter outputs before further processing. The unsigned value, n, of bits 7-4 of address 01_H determines the 3-bit inputs to the PN Matched Filter as the14-bit I & D Filter outputs divided by 2^n. Equivalently, bits 7-4 control the viewport of the Integrate and Dump Filter outputs as shown in Note that viewport control affects both I and Q channels of the Integrate and Dump Filters.

Table 6. Integrate & Dump Filter Viewport Control

Bits 7-4	I & D Bits Output to Matched Filter
0_H	2-0
1_H	3-1
2_H	4-2
3_H	5-3
• • •	• • •
• • •	• • •
A_H	12-10
B_H	13-11

Saturation protection is implemented for those cases when the Integrate and Dump Filter output signal level overflows the scaled range selected for the PN Matched Filter. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Address 02_H:
Bits 5-0 — Receiver Baseband Sampling (Dump) Rate Control
The baseband sampling rate should be set to twice the nominal PN chip rate of the received signal and must be less than or equal to half the rate of RXIFCLK. When bit 0 of address 01_H is set low, the baseband sampling clock for the Integrate and Dump Filter and all subsequent receiver circuitry is referenced to RXIFCLK and generated internally. The receiver baseband sampling rate is then set to the frequency of RXIFCLK/(n+1), where n is the value stored in bits 5-0 and must range from 1 to 63. This feature is useful in cases where a specific sample rate is required that is an integer sub-multiple of $f_{RXIFCLK}$. In cases where a sample rate is required that is not an integer sub-multiple of $f_{RXIFCLK}$, an external baseband sampling rate can be provided by the RXMSMPL input.

Addresses 03_H through 06_H:
NCO Frequency Control Word
The Z87200's internal NCO is driven by a frequency control word that is the sum of the frequency discriminator error value (generated in the demodulator) and the 32-bit frequency control word (FCW) stored in this location. The four 8-bit registers at addresses 03_H to 06_H are used to store the 32-bit frequency control word as shown in The LSB of each byte is stored in bit 0 of each register.

Table 7. Integrate & Dump Filter Viewport Control

ADDR06H	ADDR 05H	ADDR04H	ADDR03H
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

The NCO frequency is then set by the FCW according to the following formula:

$$f_{NCO} = \frac{f_{RXIFCLK} \times FCW}{2^{32}}$$

In order to avoid in-band aliasing, f_{NCO} must not exceed 50% of $f_{RXIFCLK}$; normally, the FCW should be set so that f_{NCO} does not exceed ~35% of $f_{RXIFCLK}$. While this limitation may seem to restrict use of the NCO, higher I.F. transmit or receive frequencies can generally be achieved by using aliases resulting from digital sampling. The signal bandwidth with respect to $f_{RXIFCLK}$, the modulation type, and the use of Direct I.F. or Quadrature Sampling Mode also restrict the choice of NCO frequency, Theory of Operation.

PN Matched Filter Registers

Despreading of the received signal is accomplished in the Z87200 with a dual (I and Q channel) PN Matched Filter. Furthermore, the Z87200 is designed for burst signal operation, where each data burst begins with an Acquisition/Preamble symbol and is then followed by the actual information data symbols. Two separate and independent PN codes can be employed, one for the Acquisition/Preamble symbol, the other for the information symbols. Accordingly, the PN Matched Filter is supported by two PN code registers to independently allow the programming of two distinct codes up to 64 chips in length. The PN codes are represented as a sequence of ternary-valued tap coef-

CONTROL REGISTERS (Continued)

ficients, each requiring 2 bits of storage according to the mapping shown in Table 8.

Table 8. PN Matched Filter Tap Values

Tap Bits 1,0		Tap Coeff
X	0	0
0	1	+1
1	1	-1

As a convention, Tap 0 is the first tap as the received signal enters the PN Matched Filter, and Tap 63 is the last. All active taps of the PN Matched Filter, from Tap 0 up to Tap (N-1), where N is the length of the PN code, should be programmed with tap coefficient values of +1 or -1 according to the PN code sequence. Setting the end coefficients of the PN Matched Filter registers to zero values permits the effective length of the filter to be made shorter than 64 taps.

Addresses 07_H through 16_H:
Matched Filter Acquisition/Preamble Symbol Coefficients
Addresses 07_H to 16_H contain the 64 2-bit Acquisition/Preamble PN code coefficient values. The 128 bits of information are stored in 16 8-bit registers at addresses 07_H to 16_H as shown in Table 8.

Table 9. Acquisition/Preamble Coefficient Storage

Address 16_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 63	Coeff. 62	Coeff. 61	Coeff. 60
Address 15_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 59	Coeff. 58	Coeff. 57	Coeff. 56
---	---	---	---
---	---	---	---
Address 08_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 7	Coeff. 6	Coeff. 5	Coeff. 4
Address 07_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 3	Coeff. 2	Coeff. 1	Coeff. 0

Addresses 17_H through 26_H:
Matched Filter Data Symbol Coefficients
Addresses 17_H to 26_H contain the 64 2-bit Data Symbol PN code coefficient values. The 128 bits of information are stored in 16 8-bit registers at addresses 17_H to 26_H as shown in The contents of addresses 17_H to 26_H are independent of and not affected by the contents of addresses 07_H to 16_H.

Table 10. Data Symbol Coefficient Storage

Address 26_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 63	Coeff. 62	Coeff. 61	Coeff. 60
Address 25_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 59	Coeff. 58	Coeff. 57	Coeff. 56
---	---	---	---
---	---	---	---
Address 18_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 7	Coeff. 6	Coeff. 5	Coeff. 4
Address 17_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 3	Coeff. 2	Coeff. 1	Coeff. 0

Address 27_H:
Bit 0 — Front End Processor Disable
The Front End Processor (FEP) averages the two baseband samples per chip by adding consecutive pairs of samples. The function may be disabled for test purposes by using this bit: when set low, the FEP is enabled and in its normal mode of operation; when set high, the FEP is disabled.

Power Estimator Registers

Address 28_H:
Bits 1-0 — Matched Filter Viewport Control
The Z87200 incorporates viewport (data selector) circuitry to select any eight consecutive bits from the 10-bit outputs of the PN Matched Filter as the 8-bit inputs to the Power Estimator and DPSK Demodulator blocks. The Symbol Tracking Processor, however, operates on the full 10-bit PN Matched Filter outputs before the viewport is applied. The signal levels of the PN Matched Filter output reflect the number of chips per symbol and the signal-to-noise ratio of the signal. Setting the viewport thus effectively normalizes the PN Matched Filter outputs prior to further processing. The unsigned value, n, of bits 1-0 of address 28_H determines the 8-bit input to the Power Estimator and DPSK Demodulator blocks as the 10-bit PN Matched Filter output divided by 2^n. Equivalently, bits 1-0 control the viewport of the PN Matched Filter output as shown in Note

that viewport control affects both I and Q channels of the PN Matched Filter output.

Table 11. Matched Filter Viewport Control

Bits 1-0		ISUM, QSUM
0	0	Bits 7-0
0	1	Bits 8-1
1	X	Bits 9-2

Saturation protection is implemented for those cases when the PN Matched Filter output signal level overflows the scaled range selected for the Power Estimator and DPSK Demodulator. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Acquisition and Tracking Processor Registers

The Acquisition and Tracking Processor Registers allow the user to configure how the PN Matched Filter outputs for the Acquisition/Preamble symbol and the data symbols that follow thereafter are treated in the Symbol Tracking Processor. Since operation of the Z87200 receiver presumes symbol-synchronous PN modulation, processing of the PN Matched Filter outputs can be used for symbol synchronization prior to DPSK demodulation. The Acquisition/Preamble symbol and the data symbols may have different PN spreading codes, however, and so the PN Matched Filter outputs may exhibit different signal levels due to the different code lengths and auto-correlation properties. The control registers in this block allow such differences to be treated, as well as permitting specification of the number of receive data symbols per burst and other parameters associated with burst data communications.

The I and Q channel outputs of the PN Matched Filter are processed to estimate the correlation signal power at each baseband sampling instant. This estimated signal power is compared with the contents of the Acquisition/Preamble and Data Symbol Threshold registers, as appropriate, to determine whether "successful" correlation has been detected. Successful detection in acquisition mode immediately switches the receiver to despread and track the expected subsequent data symbols, while successful detection thereafter yields symbol synchronization. The threshold register values must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread signal is correlated against a local version of the PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold register value, a successful correlation is assumed to have been detected. Further operations in the Symbol Tracking Processor then handle the possibility of multiple detects per symbol, missed detects, etc.

The choice of the threshold values will be determined by several factors. Arithmetically, the digital baseband samples of the received signal are multiplied by the PN Matched Filter tap coefficients each baseband sample clock cycle and the results are summed to provide a correlation value. The I and Q PN Matched Filter correlated output values are then used to estimate the signal power according to the following approximation:

$$\text{Max}\{\text{Abs}(I),\text{Abs}(Q)\}+1/2\ \text{Min}\{\text{Abs}(I),\ \text{Abs}(Q)\}.$$

The magnitude of the estimated power thus depends on several variables, including the setting of the Integrate and Dump Filter viewport, the PN code length and autocorrelation properties, and the magnitudes of the incoming $RXIIN_{7-0}$ and $RXQIN_{7-0}$ signals. The actual threshold values that should be programmed will therefore vary from application to application.

Addresses 29_H and $2A_H$: Acquisition/Preamble Threshold

Addresses 29_H and $2A_H$ contain the unsigned Acquisition/Preamble Threshold value, as shown in This value is used for comparison with the estimated signal power from the PN Matched Filter to determine whether a successful correlation has been detected in acquisition mode. The Acquisition/Preamble Threshold value must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread Acquisition/Preamble is correlated against a local version of the Acquisition/Preamble PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold value, a successful correlation is assumed to have been detected. Note that the Symbol Tracking Processor does not insert missed detect pulses when the device is in acquisition mode.

Table 12. Acquisition/Preamble Threshold Storage

ADDR $2A_H$	ADDR 29_H
Bits 1-0	Bits 7-0
Acq. Thresh. Bits 9-8	Acq. Thresh. Bits 7-0

Addresses $2B_H$ and $2C_H$: Data Symbol Threshold

Addresses $2B_H$ and $2C_H$ contain the Data Symbol Threshold value, as shown in This value is used for comparison with the estimated signal power from the PN Matched Filter to determine whether a successful correlation has been detected for each data symbol. The Data Symbol Threshold value must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread data symbol is correlated against a local version of the data symbol PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold value, a successful correlation is assumed to have been detected. If bit 2 of address 30_H is set low, then the Symbol Acquisi-

CONTROL REGISTERS (Continued)

tion Processor will insert a detect pulse at the appropriate time if a successful correlation is not detected as expected *a priori.*

Table 13. Data Symbol Threshold Storage

ADDR $2C_H$	ADDR $2B_H$
Bits 1-0	Bits 7-0
Data Thresh. Bits 9-8	Data Thresh. Bid 7-0

Address $2D_H$:

Bits 5-0 — Rx Chips per Data Symbol

The number of PN chips per data symbol in the receiver is controlled by address $2D_H$. The unsigned value must range from 1 to 63 (01_H to $3F_H$), where the number of chips per data symbol will be this value plus 1. The *a priori* number of PN chips per data symbol, where this value must be equal to the number of non-zero coefficients stored in the Data Symbol Coefficient Registers (addresses 17_H to 26_H) for the PN Matched Filter, is used to help control symbol timing in the receiver. Since acquisition is purely based on correlation of a single received Acquisition/Preamble symbol, the corresponding number of chips per Acquisition/Preamble symbol is not required and no similar register is provided for such use.

Address $2E_H$:

Receiver Data Symbols per Burst (bits 7-0)

The data stored as two bytes in addresses $2E_H$ (LS Byte) and $3A_H$ (MS Byte) define the number of data symbols per burst. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2, giving a range of 1 to 65,533. Note that the range is slightly different from that supported by the Z87200's transmitter. Once the number of received data symbols processed exceeds this number, the burst is assumed to have ended and the receiver immediately returns to acquisition mode, ready for the next burst.

Address $2F_H$:

Missed Detects per Burst Threshold

To monitor the reception quality of the received burst data symbols, the Z87200 incorporates a feature within its tracking algorithm that tallies the number of received data symbols whose PN Matched Filter correlation output did not exceed the Data Symbol Threshold value.

Whenever a "missed detect" occurs, the tracking algorithm will generate and insert a detect signal at the sample clock cycle corresponding to the expected correlation peak in order to maintain a continuous train of data symbols and symbol clocks. Simultaneously, a "missed detect" pulse will be generated internally and tallied for the current burst. When the accumulated number of missed detects is greater than the value stored in address $2F_H$, the device will terminate reception of the current burst and return to acquisition mode to await the next burst.

The unsigned value in address $2F_H$ must range from 1 to 255 (01_H to FF_H), where this value is the maximum number of missed detects per burst allowed before the burst terminates. This function can be disabled by setting bit 5 of address 30_H high.

Address 30_H:

Bit 0 — Manual Detect Enable

While the receiver is in acquisition mode, valid bursts may be ignored by setting this bit high. When it is set low (normal operation), the detection of a burst's Acquisition/Preamble symbol is enabled. Setting this bit high allows the user to force the device to ignore Acquisition/Preamble symbols that would normally be successfully acquired. This feature could be used, for example, in a system employing multiple receivers with identical PN codes in a Time Division Multiple Access scheme where time-synchronized device management could be supported through dynamic setting of this bit.

Acquisition and Tracking Processor Registers

Bit 1 — Manual Punctual

This bit enables the user to completely disable the internal tracking circuitry and force symbol information to be transferred to the demodulator punctually at the symbol rate determined by the number of chips per data symbol information programmed into address $2D_H$. This function overrides the symbol tracking algorithm, although the absence of a successful correlation will continue to be tallied as a missed detect and compared against the value stored in address $2F_H$ to monitor signal quality unless disabled by bit 5 of address 30_H. When bit 1 is set low, the Z87200 will operate in its normal mode with symbol timing derived from the symbol tracking processor; when set high, symbol timing is derived from the *a priori* number of chips per data symbol stored in bits 5-0 of address $2D_H$.

Bit 2 — Force Continuous Acquisition

This bit enables the user to force the receiver to remain in acquisition mode even after successful detection of the Acquisition/Preamble symbol. When so commanded, the receiver will continuously process only Acquisition/Preamble symbols and will not switch from acquisition mode. This function may be used under manual control to receive a series of repeated Acquisition/Preamble symbols in order to increase the confidence level of burst detection before beginning demodulation of the data symbol information.

When this bit is set high, the device will be locked in acquisition mode and the Symbol Tracking Processor will not in-

sert missed detect pulses; when set low, normal operation will be enabled whereby data symbols are automatically processed immediately following detection of an Acquisition/Preamble symbol.

Bit 3 — Bypass Max. Power Selector
The Z87200's receiver acquisition and tracking circuitry includes a function that continuously selects the highest estimated power level out of the three most recent consecutive estimated power levels from the PN Matched Filter. As the contents of the sliding 3-sample window change each cycle of the baseband sampling clock, a new determination of the highest power level is made from the current set of the three most recent power level values. The correlated I and Q channel values within the 3-sample window corresponding in time to the highest observed power level are then available to be processed in the demodulator.

This function assures that, within any 3-sample period, the I and Q channel values corresponding to the highest estimated power level will be selected over the two other pairs of correlated values even if the estimated power levels of the other pairs exceed the programmed threshold. The Maximum Power Selector is used in normal operation of the Z87200 so that the tracking algorithm discriminates by estimated power levels rather than exact timing intervals, thereby allowing the receiver to adjust to dynamic changes of the symbol phase. In cases where specific correlation values are desired regardless of their associated power level, bit 3 of address 30_H enables the 3-sample power discriminator to be bypassed, thereby making the outputs of the PN Matched Filter available directly to the demodulator.

When this bit is set high, the Maximum Power Selector is bypassed; when it is set low, the Selector is enabled, where this is the normal operating mode.

Bit 4 — Half Symbol Pulse Off
The Z87200 generates two bit clock pulses per symbol when operating in QPSK mode, one at the mid-point of each symbol and one at the end of each symbol. These clocks are used by the Output Processor to manage data flow.

When this bit is set high, the mid-point pulse is suppressed; when it is set low, the device operates in its normal mode. This function is primarily used for test purposes and should not normally be used.

Bit 5 — Missed Detects Per Burst Off
To monitor the quality of the received burst data symbols, the Symbol Tracking Processor keeps track of the cumulative number of received data symbols per burst whose estimated correlation power level did not exceed the specified Data Symbol Threshold value. When the accumulated number of missed detects equals the Missed Detects per Burst Threshold value stored in address $2F_H$, the device will terminate the reception of the current burst with the next missed detect and return to acquisition mode to await the next burst.

When bit 5 is set low, the "missed detect" function operates normally; when set high, this function is disabled, allowing the device to be operated until the end of the specified data burst even when the number of "missed detects" exceeds the Missed Detects per Burst Threshold.

Bit 6 — Receiver Symbols Per Burst Off
The data stored in addresses $2E_H$ and $3A_H$ defines the number of data symbols per burst that will be processed by the receiver. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2. Once the number of data symbols processed by the receiver exceeds this number, the burst is assumed to have ended and the receiver will immediately return to acquisition mode.

When bit 6 is set high, the function is disabled, providing an option to track data symbols under external control for bursts of more than 65,533 data symbols or indefinitely for continuous transmission; when set low, the function will operate normally as defined by the value stored in addresses $2E_H$ and $3A_H$.

Address 31_H:
Bit 0 — Manual Detect Pulse
This bit provides the user a means to externally generate symbol timing, bypassing and overriding the internal symbol power estimation and tracking circuitry. This function may be useful in applications where the dynamic characteristics of the transmission environment require unusual adjustments to the symbol timing.

When bit 0 of address 30_H is set high (Manual Detect Enable) and when RXMDET is low, a rising edge on this bit will generate a detect pulse. The function can also be performed by means of the RXMDET input signal. Bit 0 of address 31_H and the RXMDET input are logically ORed together so that, when either one is held low, a rising edge on the other triggers the manual detect function. The rising edge of this bit is synchronized internally so that on the second rising edge of the baseband sampling clock that follows, the rising edge of bit 0 will transfer the I and Q channel correlated output values of the PN Matched Filter to the DPSK Demodulator.

Address 32_H:
Bit 0 — Receiver Manual Abort
This bit enables the user to manually force the Z87200 to cease reception of the present burst of data symbols and prepare for acquisition of a new burst. This function can be used to reset the receiver and prepare to receive a priority transmission signal under precise timing control, giving the user the ability to control the current state of the receiver as needed.

CONTROL REGISTERS (Continued)

When RXMABRT is set low, a rising edge on bit 0 of address 32_H will execute the abort function. The function can also be performed by means of the RXMABRT input. The RXMABRT input and bit 0 of address 32_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the abort function. The second rising edge of the internal baseband sampling clock that follows a rising edge of this bit will execute the abort and also clear the symbols-per-burst, samples-per-symbol, and missed-detects-per-burst counters. The counters will be reactivated on the detection of the next Acquisition/Preamble symbol or by a manual detect signal.

Demodulator Registers

Address 33_H:

Bits 1-0 — Signal Rotation Control

These bits control the function of the Signal Rotation Block used in demodulation of the differentially encoded BPSK, QPSK, or $\pi/4$ QPSK signals. The previous symbol will be rotated in phase with respect to the current symbol as shown in Table 14, where I_{OUT} and Q_{OUT} are the I and Q channel outputs of the Signal Rotation Block and I_{IN} and Q_{IN} are the inputs. The normal settings are 0 X (no rotation) for BPSK and $\pi/4$ QPSK signals and 1 1 (–45° rotation) for conventional QPSK signals.

Table 14. Signal Rotation Control

Bits 1,0	I_{OUT}	Q_{OUT}	Resulting Rotation
0, X	I_{IN}	Q_{IN}	No rotation
1,0	I_{IN}-Q_{IN}	Q_{IN}+I_{IN}	+45° rotation
1,1	I_{IN} + Q_{IN}	Q_{IN}-I_{IN}	-45° rotation

Bit 2 — Not Used

Bit 2 of address 33_H is not used and must always be set low (0).

Bit 3 — Loop Clear Disable

The setting of this bit determines whether the Loop Filter's K2 accumulator is reset or not when the Z87200 receiver function is turned off when the input signal MRXEN is set low.

When bit 3 is set low, the Loop Filter's K2 accumulator will be reset to zero whenever MRXEN is set low to disable the receiver function. When bit 3 is set high, this function is disabled and the contents of the accumulator are not affected when MRXEN transitions from high to low. The optimum setting of this bit will depend on the stability of the oscillators used for carrier generation and frequency translation in the system and the length of the period between bursts. If the oscillators are stable and the period between bursts is not very long, the optimum setting of this bit will be low so that at the start of each burst the tracking loop will resume from its state at the end of the previous burst. If the oscillators are not stable or if the period between bursts is long with respect to the oscillators' stability, then the optimum setting may be high so that the tracking loop will restart from its initial state at the start of each burst.

Bits 7-4 — AFC Viewport Control

The Z87200 incorporates viewport (data selector) circuitry to select any eight consecutive bits from the 17-bit output of the Frequency Discriminator as the 8-bit input to the Loop Filter block to implement the Z87200's AFC function. The unsigned value, n, of bits 7-4 of address 33_H determines the 8-bit input to the Loop Filter as the 17-bit Frequency Discriminator output divided by 2^n. Equivalently, bits 7-4 control the viewport of the Frequency Discriminator output as shown in Table 14.

Table 15. AFC Viewport Control

Bits 7-4	Discrim. bits output to Loop Filter
0_H	7-0
1_H	8-1
2_H	9-2
3_H	10-3
• • •	• • •
• • •	• • •
8_H	15-8
9_H	16-9
A_H-F_H	Not used

Saturation protection is implemented for those cases when the Frequency Discriminator output signal level overflows the scaled range selected for the Loop Filter. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Address 34_H:

Bits 4-0 — K2 Gain Value

Bits 4-0 control the gain factor K2 within the Loop Filter. The gain factor multiplies the signal before the K2 accumulator by a value of 2^n, where n is the 5-bit K2 Gain Value. The value must range from 0 to 21 (15_H) as shown in Table 15.

Table 16. K2 Gain Values

Bits 4-0	Gain in K2 Path
00_H	2^0
01_H	2^1
• • •	• • •
• • •	• • •
14_H	2^{20}
15_H	2^{21}

Bit 5 — K2 On

This bit enables or disables the K2 path of the Loop Filter. Setting this bit low resets the K2 accumulator and keeps it reset; setting this bit high enables the path and turns on K2.

Bit 6 — Carry In One Half

When this bit is set high, the value of 1/2 of an LSB is added to the accumulator of the K2 path of the Loop Filter each symbol period. This function can be useful in cases where the scale and gain functions that precede the accumulator produce quantized values with significant error. In such cases, the processing of two's complement numbers by the accumulator will compound the error over time. Since truncation of two's complement numbers leads to a negative bias of 1/2 of an LSB when the error is random, adding 1/2 of an LSB per symbol can compensate by averaging the error to zero.

When bit 6 of address 34_H is set high, a value of 1/2 will be added to the accumulator input each symbol cycle; when it is low, a zero will be added.

Address 35_H:

Bits 4-0 — K1 Gain Value

Bits 4-0 control the gain factor K1 within the Loop Filter. The gain factor multiplies the signal by a value of 2^n, where n is the 5-bit K1 Gain Value. The value must range from 0 to 21 (15_H), as shown in Table 16.

Table 17. K1 Gain Values

Bits 4-0	Gain in K1 Path
00_H	20
01_H	21
•••••	•••••
•••••	•••••
14_H	2^{20}
15_H	2^{21}

Bit 5 — K1 On

This bit enables or disables the K1 path of the Loop Filter. Setting this bit low disables the K1 path; setting this bit high enables the path and turns on K1.

Bit 6 — Freeze Loop

This bit enables the Loop Filter to be held constant during symbol cycles, thereby fixing the output frequency of the NCO at the value established by the Loop Filter when bit 6 was set high. This function can be useful in cases where a carrier offset has been tracked by the Loop Filter and additional Doppler offsets are to be ignored.

When this bit is set high, it freezes the output of the Loop Filter; when it is set low, the Loop Filter is enabled and processes the frequency error information in the usual way.

CONTROL REGISTERS (Continued)

Output Processor Control Registers

Address 36_H:

Bit 0 — Reverse I and Q

In QPSK mode, the order in which the received I and Q bit information is output may be reversed by setting this bit high. This function has the effect of interchanging I and Q channels. Normally, when this bit is set low, the I-channel bit will precede the Q-channel bit in each symbol period. When bit 0 is set high, the Q-channel bit will precede the I-channel bit each symbol period.

Bit 1 — BPSK Enable

This bit configures the Output Processor to output either one bit per symbol (BPSK mode) or two bits per symbol (QPSK mode). In addition, it enables the user to output the I-channel information only or the Q-channel information only, depending on the value of bit 0. Table 18 shows the configuration of the output processor for all combinations of the values of bits 0 and 1.

Table 18. Output Processor Modes

Bit 1	Bit 0	Output Processor Mode
0	0	QPSK mode with I-Channel Bit Preceding Q-Channel Bit
0	1	QPSK mode with Q-Channel Bit Preceding I-Channel Bit
1	0	BPSK mode with I-Channel Information Output
1	1	BPSK mode with Q-Channel Information Output

Bit 1 also sets the Frequency Discriminator into either BPSK or QPSK mode. The Z87200 receiver uses Dot and Cross product results generated within the DPSK Demodulator to develop the error signal used to form a closed-loop AFC for carrier frequency acquisition and tracking.

When bit 1 is set high, the discriminator circuitry is in BPSK mode and the Frequency Discriminator function is calculated as:

$$Cross_{16\text{-}0} \times Dot_{MSB}.$$

When bit 1 is set low, the discriminator circuitry is in QPSK mode and the Frequency Discriminator function is calculated as:

$$(Cross_{16\text{-}0} \times Dot_{MSB}) - (Dot_{16\text{-}0} \times Cross_{MSB}).$$

Bit 2 – Invert Output

This bit inverts the output bits of both the I and Q Channels. The inversion will occur at the output pins RXOUT, RXIOUT, and RXQOUT.

When this bit is set low, the outputs are not inverted; when it is set high, the outputs are inverted.

Output Processor Control Registers

Address 37_H:

Bit 0 — NCO Enable

The function of this bit is to allow the power consumed by the operation of the NCO circuitry to be minimized when the Z87200 is not receiving. The NCO can also be disabled while the Z87200 is transmitting provided that the Z87200's on-chip BPSK/QPSK modulator is not being used. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting bit 0 low holds the NCO in a reset state; setting bit 0 high then reactivates the NCO, where it is necessary to reload the frequency control word into the NCO. Note that this bit operates independently of bits 1 (Transmitter Enable) and 2 (Receiver Enable), where those bits have similar control over the transmit and receive circuitry, respectively.

Bit 0 of address 37_H performs the same function as MNCOEN, and these two signals are logically ORed together to form the overall control function. When bit 0 is set low, MNCOEN controls the activity of the NCO circuitry and, when MNCOEN is set low, bit 0 controls the activity of the NCO circuitry. When either bit 0 or MNCOEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following RXIFCLK cycle to virtually disable all of the NCO circuitry, although the user programmable control registers are not affected by the power down sequence. Upon reactivation (when either MNCOEN or bit 0 of address 37_H return high), the NCO must be reloaded with frequency control information either by means of the MFLD input or by writing 01_H into address 00_H.

Bit 1 — Transmitter Enable

A rising edge on this bit causes the transmit sequence to begin so that the Z87200 first transmits a single Acquisition/Preamble symbol followed by data symbols. Bit 1 of address 37_H should be set low after the last symbol has been transmitted to minimize power consumption of the transmitter circuit. Bit 1 of address 37_H operates independently of bits 2 and 0, where those bits have similar control over the receive and NCO circuitry, respectively.

When input signal MTXEN is set low, bit 1 of address 37_H controls the activity of the transmit circuitry and, when MTXEN is set low, bit 1 controls this function. When either bit 1 or MTXEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following TXIFCLK cycle to virtually disable all of the transmitter data path, although the user programmable control registers are not affected by the power down sequence.

Bit 2 — Receiver Enable

The function of this bit is to allow power consumed by the operation of the receiver circuitry to be minimized when the device is not receiving. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting bit 2 low reduces the power consumption substantially. When bit 2 is set high, the receiver will automatically power up in acquisition mode regardless of its prior state when it was powered down. Bit 2 of address 37_H operates independently of bits 1 and 0 of address 37_H, where these signals have similar control over the transmit and NCO circuitry, respectively.

Bit 2 of address 37_H performs the same function as MRXEN, and these two signals are logically ORed together to form the overall control function. When bit 2 of address 37_H is set low, MRXEN controls the activity of the receiver circuitry and, when MRXEN is set low, bit 2 of address 37_H controls the activity of the receiver circuitry. When either bit 2 or MRXEN (whichever is in control, as defined above) goes low, a reset sequence begins on the following RXIFCLK cycle and continues through a total of six RXIFCLK cycles to virtually disable all of the receiver data paths. The user- programmable control registers are not affected by the power down sequence, with the exception of $RXTEST_{7-0}$ (address 38_H), which is reset to 0. If the $RXTEST_{7-0}$ bus is being used to read any function other than the PN Matched Filter I and Q inputs, the value must be rewritten.

Address 38_H:

Bits 3-0 — $RXTEST_{7-0}$ Function Select

The data stored in bits 3-0 of address 38_H selects the signal available at the $RXTEST_{7-0}$ bus (pins 41-48). These pins provide access to 16 test points within the receiver according to the data stored in bits 3-0 of address 38_H and the assignments shown in The validity of the $RXTEST_{7-0}$ outputs at RXIFCLK speeds greater than 20 MHz is dependent on the output selected: outputs that change more rapidly than once per symbol may be indeterminate.

Note that the reset sequence that occurs when the receiver is disabled will also reset the contents of address 38_H to a value of 0. If the RXTEST7-0 bus is to be used to observe any function other than the PN Matched Filter I and Q inputs, then the appropriate value must be rewritten.

Address 39_H:

Bits 6-0 — Matched Filter Power Saver

The data stored in bits 6-0 of address 39_H allows the unused sections of the PN Matched Filter to be turned off when the PN Matched Filter is configured to be less than 64 taps long for data symbols. All taps are always fully powered when the device is in acquisition mode.

The PN Matched Filter is split into seven 9-tap sections, and the power to each section is controlled by the settings of bits 6-0 of address 39_H, as shown in Table 19.

Table 19. Matched Filter Tap Power Control

Bit in Addr. 39_H	MF Taps Controlled
0	1-9
1	10-18
2	19-27
3	28-36
4	37-45
5	46-54
6	55-64

Power control is not provided for Tap 0, the first tap of the PN Matched Filter, since Tap 0 is always used no matter what the PN code length. Setting a bit high in bits 6-0 of address 39_H turns off the power to the corresponding block of taps of the PN Matched Filter. The power should only be turned off to those blocks of taps for which all the tap coefficients in that block have been set to zero

Address $3A_H$:

Receiver Data Symbols per Burst (bits 15-8)

The data stored as two bytes in addresses $2E_H$ (LS byte) and $3A_H$ (MS byte) defines the number of data symbols per burst. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2, giving a range of 1 to 65,533. Note that the range is slightly different from that in the transmitter. Once the number of received data symbols processed exceeds this number, the burst is assumed to have ended and the Z87200 immediately returns to acquisition mode to await the next burst.

CONTROL REGISTERS (Continued)

Address $3B_H$:

Bit 0 — Matched Filter Loopback Enable

The Z87200 incorporates a loopback capability that feeds the encoded and spread transmit signals TXIOUT and TXQOUT directly into the PN Matched Filter inputs. This test mode allows the baseband portion of the system to be tested independently of the BPSK/QPSK Modulator and Downconverter.

Setting bit 0 of address $3B_H$ high enables this loopback path; setting it low puts the device into its normal operating mode.

Bit 1 — I.F. Loopback Enable

The Z87200 incorporates a loopback capability that feeds the encoded, spread and modulated transmit signal $TXIFOUT_{7-0}$ directly into the receiver $RXIIN_{7-0}$ input. This test mode allows the entire digital portion of the system to be tested. Since only the I channel is provided as an input, I.F. loopback requires that the PN chip rate and RXIFCLK rate be consistent with Direct I.F. Sampling Mode.

Setting bit 1 of address $3B_H$ high enables this loopback path; setting it low puts the device into its normal operating mode.

Bits 3-2 — Receiver Overlay Select

The Z87200 incorporates programmable overlay code generators in both the transmitter and receiver. When enabled, the selected receiver overlay code is subtracted from the data symbols, one overlay bit per symbol in both BPSK and QPSK modes. No synchronization beyond the burst acquisition synchronization that is intrinsic to operation of the Z87200 is required since the overlay code generators in both the transmitter and the receiver are automatically reset at the start of each burst. The addition of the overlay code randomizes the transmitted data sequence to guarantee that the spectrum of the transmitted signal will be adequately whitened and will not contain a small number of spectral lines even when the data itself is not random.

Three transmit and receive overlay codes can be selected, where they are each maximal length sequences with lengths of 63, 511 and 1023 symbols. The receiver overlay codes are enabled and selected by the settings of bits 3-2 of address $3B_H$, as shown in Table 19.

Table 20. Receiver Overlay Code Select

Bits 3-2 in Addr. $3B_H$	Overlay Code Length and Polynomial
0	Overlay Code Disabled
1	63: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-6}$
2	511: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-9}$
3	1023: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-10}$

Addresses $3C_H$ through $3F_H$: Unused

Transmit Control Registers

Address 40_H:

Bit 0 — Transmit BPSK

This bit configures the transmitter for either BPSK or QPSK mode transmission. and differential encoding.

If programmed for BPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where TKBITPLS is generated once per symbol, one chip period before the end of the current symbol. At the end of the symbol duration, the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value, and is generated repeatedly at the symbol rate as long as the input signal MTXEN remains high.

In QPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where this signal is generated in this mode twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle before latching the TXIN data into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value.

When bit 0 of address 40_H is set low, the transmitter is configured in QPSK mode; when it is set high, the transmitter is configured in BPSK mode.

Bit 1 — Offset Binary Output
The $TXIFOUT_{7-0}$ output signals can be in either two's complement or offset binary formats. Since all internal processing in the device uses two's complement format signals, the MSB of the two's complement modulated transmitter output must be inverted if the output is to be in offset binary format.

When this bit is set high, the $TXIFOUT_{7-0}$ output will be in offset binary format and, when it is set low, the signal will be in two's complement format. In two's complement format, the 8-bit output values range from –128 to +127 (80_H to $7F_H$); in offset binary format, the values range from 0 to +255 (00_H to FF_H).

Bit 2 — Manual Chip Clock Enable
This bit enables the PN chip rate to be controlled by either the internal chip rate clock generator or by the external input signal TXMCHP. The TXMCHP input allows the user to manually insert a single PN chip clock pulse or continuous stream of pulses. This feature is useful in cases where a specific chip rate is required that cannot be derived by the internal clock generator which generates clocks of integer sub-multiples of the frequency of TXIFCLK. The signal is internally synchronized to TXIFCLK to avoid race or hazard timing conditions.

When this bit is set high, TXMCHP will provide the PN chip rate clock; when it is set low, the clock will be provided by the internal chip rate clock generator controlled by bits 5-0 of address 41_H.

Bit 3 — Invert Symbol
This bit allows the user to invert the I and Q channel bits following differential encoding and before being spread by the PN code. This function has the same effect as inverting the PN code, which may be useful in some cases.

When this bit is set high, the encoded I and Q channel bits will be inverted; when it is set low, the I and Q channel bits will not be inverted.

Address 41_H:
Bits 5-0 — TXIFCLK Cycles per Chip
Bits 5-0 set the transmitter baseband PN chip rate to the frequency of TXIFCLK/(n+1), where n is the value stored in bits 5-0. The value of the data stored in bits 5-0 must range from 1 to 63 (01_H to $3F_H$). This feature is useful when the PN chip rate required is an integer sub-multiple of the frequency of TXIFCLK. In cases where a chip rate is required that is not an integer sub-multiple of the frequency of TXIFCLK, the rate may be controlled externally using TXMCHP.

Address 42_H:
Bits 5-0 — Tx Chips per Data Symbol
The number of chips per data symbol in the transmitter is stored in bits 5-0 of address 42_H. The unsigned value must range from 1 to 63 (01_H to $3F_H$), and the number of chips per data symbol will be this value plus 1. This value controls data symbol timing in the transmitter.

Address 43_H:
Bits 5-0 — Tx Chips per Acquisition/Preamble Symbol
The number of chips per Acquisition/Preamble symbol in the transmitter is stored in bits 5-0 of address 43_H. The unsigned value must range from 1 to 63 (01_H to $3F_H$), and the number of chips per data symbol will be this value plus 1. This value controls the Acquisition/Preamble symbol timing in the transmitter.

Addresses 44_H through $4B_H$:
Transmitter Acquisition/Preamble Symbol Code
Each Z87200 burst transmission begins with an Acquisition/Preamble symbol and is then followed by the actual information data symbols. Two separate and independent PN codes can be employed, one for the Acquisition/Preamble symbol, the other for the information symbols. Accordingly, the Z87200 Transmit PN Code Generators, like the receiver's PN Matched Filter, support independent PN codes up to 64 chips in length for the two modes. Addresses 44_H to $4B_H$ contain the binary Transmitter Acquisition/Preamble Symbol PN code chip values, where the configuration of the stored bits is as shown in Table 20.

Table 21. Acquisition/Preamble Symbol Codes

Addr $4B_H$, Bits 7-0 Code Bits 63-56
•••••••• ••••••••
Addr 45_H, Bits 7-0 Code Bits 15-8
Addr 44_H, Bits 7-0 Code Bits 7-0

The length, N, of the Acquisition/Preamble symbol code is set by the value of (N-1) stored in bits 5-0 of address 43_H. An internal counter begins the transmission with the PN code chip corresponding to that value. The last chip transmitted per symbol is then code chip 0. Note that this convention agrees with that used for the Z87200's PN Matched Filter: for a code of length N, code chip (N-1) will be the first chip transmitted and will first be processed by Tap 0 of the PN Matched Filter; the last chip per symbol to be transmitted, however, will be chip 0, and at that time chip (N-1) will be processed by Tap (N-1) and chip 0 by Tap 0 to achieve peak correlation. Operation with the subsequent data symbols is analogous.

CONTROL REGISTERS (Continued)

Address $4C_H$ through 53_H:

Data Symbol Code

Addresses $4C_H$ to 53_H contain the binary Data Symbol PN code sequence values. The storage capacity, assignments, and operation are similar to that of the Acquisition/Preamble PN code sequence values. The configuration of the bits stored is as shown in Table 22.

Table 22. Data Symbol Codes

Addr 53_H, Bits 7-0 Code Bits 63-56
....
Addr $4D_H$, Bits 7-0 Code Bits 15-8
Addr $4C_H$, Bits 7-0 Code Bits 7-0

Transmit Control Registers

Address 54_H:

Bits 1-0 — Transmitter Overlay Select

The Z87200 incorporates programmable overlay code generators in both the transmitter and receiver. When enabled, the selected transmitter overlay code is subtracted from the data symbols, one overlay bit per symbol in both BPSK and QPSK modes. No synchronization is required since the codes in both the transmitter and the receiver are automatically synchronized by resetting the code generators at the start of each burst. The addition of the overlay codes randomizes the transmitted data sequence to guarantee that the spectrum of the transmitted signal will be adequately whitened and will not contain a small number of spectral lines even when the data itself is not random. Three transmit and receive overlay codes can be selected, where they are each maximal length sequences with lengths of 63, 511 and 1023 symbols. The transmitter overlay codes are enabled and selected by the settings of bits 1-0 of address 54_H, as shown in Table 23.

Table 23. Transmitter Overlay Code Select

Bits 1-0 in Addr. 54_H	Overlay Code Length and Polynomial
0	Overlay Code Disabled
1	63: $1+x^{-2}+x^{-3}+x^{-5}+x^{-6}$
2	511: $1+x^{-2}+x^{-3}+x^{-5}+x^{-9}$
3	1023: $1+x^{-2}+x^{-3}+x^{-5}+x^{-10}$

Bit 2 —Transmitter Symbols Per Burst Off

Bit 2 of address 54_H is not used and must always be set low (0).

Address 55_H through 56_H:

Transmitter Data Symbols per Burst (bits 15-0)

The data stored as two bytes in addresses 55_H (LS byte) and 56_H (MS byte) defines the number of data symbols per burst for the transmitter. This unsigned value must range from 1 to 65,535 (0001_H to $FFFF_H$), and the number of data symbols per burst will be this value plus 1. Note that the range is slightly different from that in the receiver. Once the number of transmitted data symbols exceeds this number, the burst is assumed to have ended and the transmitter is immediately turned off. If the data value is set to 0000_H, then the symbols per burst counter is disabled, permitting the Z87200 to be used for continuous transmission of data.

REGISTER SUMMARY

Table 24. Register Summary

	Contents							
Address	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00_H								NCO Load
01_H	Integrate and Dump Filter Viewport Control				2's C. Input	NCO C'In	Inv. LF	RXMSMPL
02_H			Receiver Baseboard Sampling Rate Control					
$03\text{-}06_H$	NCO Frequency Control Word (32 bits)							
$07\text{-}16_H$	Matched Filter Acquisition/Preamble Symbol Coefficients							
27_H								FEP Disable
28_H							MF Viewport Control	
$29\text{-}2A_H$	Acquisition/Preamble Symbol Threshold, Bits 9-0							
$2B\text{-}2C_H$	Data Symbol Threshold, Bits 9-0							
$2D_H$			Receiver Chips Per Data Symbol					
$2E_H$	Receiver Data Symbols per Burst, Bits 7-0							
$2F_H$	Missed Detects Per Burst Threshold							
30_H		Rx Symb/ Burst Off	Missed Det. Per Bst. Off	Half Symb Pulse Off	Bypass Max Power Sel.	Force Cont. Acquis.	Manual Punctual	Man. Det. Enable
31_H								Man. Det.
32_H								Man. Abort
33_H	AFC Viewport Control				LF Clr. Dis.	Unused (0)	Signal Rotation Control	
34_H		Carry In 1/2	K2 On	K2 Gain Value				
35_H		L2 Freeze	K1 On	K2 Gain Value				
36_H						Inv. O/p	BPSK En.	Rev. I & Q
37_H						Rx. En.	Tx. En.	NCO En.
38_H					RXTEST7-0 Function Select			
39_H	Matched Filter Power Saver							
$3A_H$	Receiver Data Symbols per Burst, Bits 15-8							
$3B_H$					Receiver Overlay Sel		IF Lpbk En	MF Lpbk En
$3C\text{-}3F_H$								
40_H					Inv. Symb.	TXMXHP	O'Bin. O/p	TX BPSK
41_H			TXIFCLK Cycles per Chip					
42_H			Tx Chips per Data Symbol					
43_H			Tx Chips per Acquisition/Preamble Symbol					
$44\text{-}4B_H$	Transmitter Acquisition/Preamble Code (64 bits)							
$4C\text{-}53_H$	TransmitterData Symbol Code (64 bits)							
54_H							Unused (0)	Transmitter Overlay Select

4

THEORY OF OPERATION

The Z87200 receiver's downconverter circuitry allows use of two distinct modes, where the mode chosen will depend upon the application. In applications where the received PN chip rate is less than approximately 1/8 of the I.F. sample clock (RXIFCLK) rate, the Z87200 can be used with a single A/D converter (ADC) and operate in Direct I.F. Sampling Mode. For higher chip rate applications, it is necessary to use the Z87200 in the full Quadrature Sampling Mode; that is, using a quadrature signal source, two ADCs, and the on-chip NCO in its quadrature mode.

Using the Z87200 with a Single ADC in Direct I.F. Sample Mode

Direct I.F. Sampling Mode allows one rather than two ADCs to be used, as will be explained below. If appropriate for the application, use of Direct I.F. Sampling Mode can reduce the system cost since quadrature downconversion with its associated 90° signal separation and the second ADC used in Quadrature Sampling Mode are not required. The trade-off, however, is in the lower maximum PN chip rate that can be supported by the Z87200 in Direct I.F. Sampling Mode as compared to the maximum rate that can be supported by Quadrature Sampling Mode.

In Direct I.F. Sampling Mode, the sampled signal is presented as input to the receiver's I channel input (RXIIN) and the Q channel input (RXQIN) is held to zero (where "zero" is defined by the ADC input format). As a result, only two of the four multipliers in the Downconverter's complex multiplier are used and the device does not make a true single-sideband downconversion from I.F. to baseband. In Quadrature Sampling Mode, by contrast, quadrature inputs to two ADCs provide I and Q inputs to the Z87200 and the full complex multiplier is used. An illustration of the operation of Direct I.F. Sampling Mode is shown in the frequency domain in Figure 11, where the spectra have been drawn asymmetrically so that spectral inversions can be readily identified.

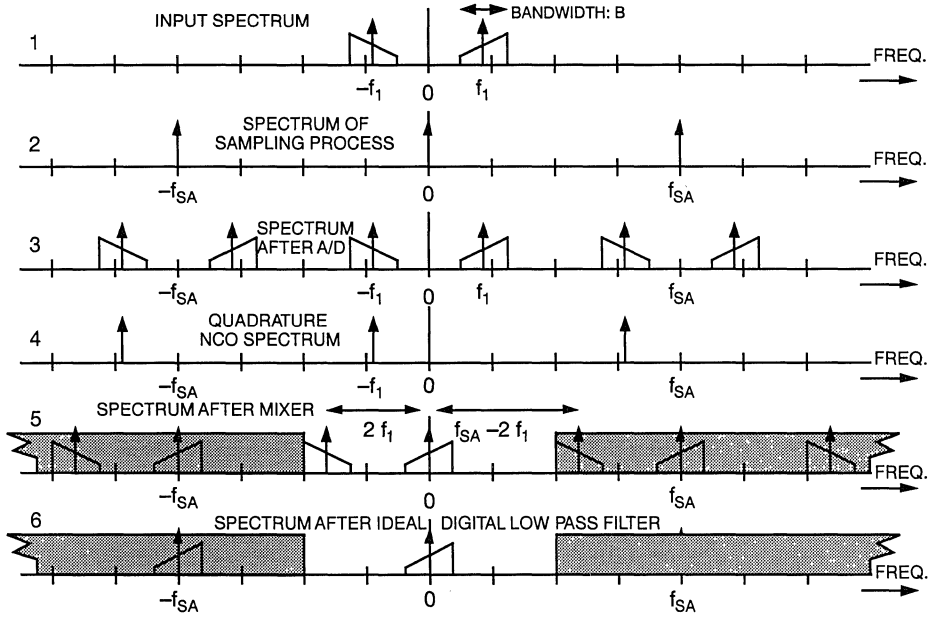

Figure 11. Spectra of Signals in Direct I.F. Sampling Mode

The spectrum of a real input signal with center (I.F.) frequency of f1 and signal bandwidth B is shown in line 1 of Figure 13. The bandwidth B is the two-sided bandwidth, corresponding to a PN chip rate of 1/2 B Mcps. Note that throughout this discussion it is assumed that the signal bandwidth does not exceed $1/2f_{SA}$; that is, $B < 1/2f_{SA}$. Otherwise, the mixing and sampling processes to be described will result in destructive in-band aliasing. Also, clearly, the I.F. frequency must be able to support the signal bandwidth; that is, $1/2B<f1$.

The input signal is sampled at the frequency f_{SA}, where the sampling spectrum is shown in line 2 and the resulting spectrum is shown in line 3. As can be seen, the fundamental and harmonics of the sampling frequency result in images of the input signal spectrum at other frequencies, where here the images are centered about multiples of the sampling frequency. In other words, the spectrum of the sampled signal shown in line 3 contains aliases of the input signal at frequencies $f1 \pm n\ f_{SA}$, where n can assume both positive and negative integer values. Since the sampling process is linear, no spectral inversion occurs; that is, the original spectrum is translated along the frequency axis with no mirror reflections of the input spectrum created.

The Z87200's NCO provides a quadrature (sine and cosine) output that defines a complex signal. Line 4 shows its spectrum as an impulse at frequency -f1, where the minus sign reflects the signal's use in downconversion and the absence of a positive impulse at frequency +f1 results because the NCO output is truly complex. Aliases of this impulse are shown offset by integer multiples of f_{SA} to reflect the sampled nature of the NCO output. When the input sampled signal of line 3 is then modulated with the complex signal of the Z87200's quadrature NCO of line 4, the signal spectrum after mixing is as shown in line 5. The sections shown inside the shaded areas are the aliases of the baseband signal beyond the Nyquist frequency and are not of concern. The signals inside the primary baseband Nyquist region ($|f| < 1/2\ f_{SA}$) consist of the desired signal and a spectrally reversed or inverted image signal with center frequency separated from that of the desired signal by 2 f1, twice the I.F. frequency before sampling. This image signal can be removed by a subsequent ideal lowpass filter as shown in line 6.

In Figure 13, the input signal is shown at a low I.F. frequency such that $f1 < 1/2\ f_{SA}$; that is, the signal is only defined inside the primary Nyquist region. Provided, however, that $B < 1/2\ f_{SA}$, that condition need not be true as long as the input spectrum is only defined for frequencies within a non-primary Nyquist region; that is, defined only over frequencies f such that

$$(n-1/2)f_{SA}<|f|<(n+1/2)f_{SA}$$

for positive integer n.

Direct I.F. Sampling Mode with this type of signal is shown in Figure 14, where it can be seen that in line 3 the diagram's high frequency input has the same spectrum after sampling as does the low frequency input in Figure 11; consequently, all subsequent operations are identical to those in Figure 13.

This result stems from the periodic nature of sampling: sampling an input frequency f1 is theoretically indistinguishable from sampling an input frequency $(n\ f_{SA} + f1)$ for positive integer n and positive $f1 < 1/2\ f_{SA}$. A slightly different result obtains, however, when sampling an input frequency $(n\ f_{SA} - f1)$, again for positive integer n and positive $f1 < 1/2\ f_{SA}$. In this case, the positions of the spectrally inverted and spectrally correct aliases will be interchanged when compared with an input frequency of $(n\ f_{SA} + f1)$. As a consequence, the desired baseband signal after downconversion and filtering will also be spectrally inverted. This phenomenon is equivalent to high-side conversion; that is, downconversion of a signal by means of a local oscillator at a frequency higher than the carrier frequency. If the modulation type is QPSK, demodulation of a spectrally inverted signal will result in the inversion of the Q channel data (which can be readily corrected); if the modulation type is BPSK, there is no effect on the demodulated data.

4

THEORY OF OPERATION (Continued)

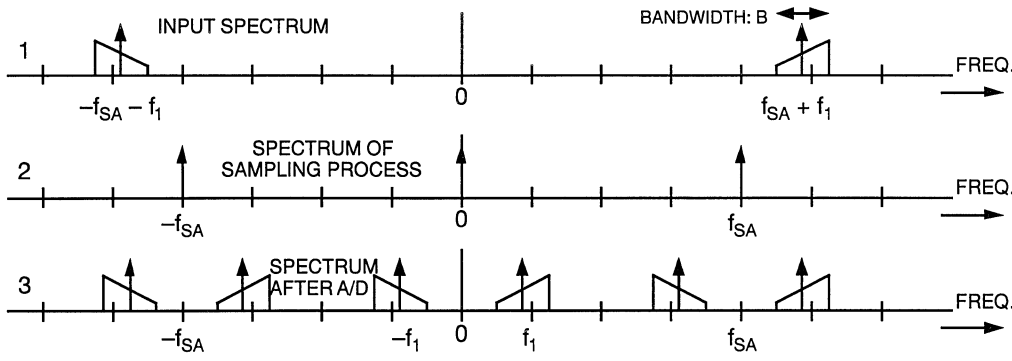

Figure 12. Direct I.F. Sampling Mode with I.F. Frequency ($f_{SA}+f_1$) > Sampling Frequency f_{SA}

The above discussion has assumed ideal low-pass filtering to recover the desired signal at baseband, but, in the Z87200's Downconverter, an ideal low-pass filter is not available. The quadrature Integrate and Dump filter of the Downconverter serves this purpose instead. The Downconverter's Integrate and Dump filter is a decimation filter, integrating input samples over a programmable number of sample periods, N, so that the output sampling rate is (1/N)th of the input sampling rate and the I.F. sampling rate fSA is decimated to the baseband sampling rate. Since the Z87200's PN Matched Filter requires two samples per chip, the baseband sampling rate must be at twice the PN chip rate and N must equal f_{SA}/B. When the sampling rate is much greater than the signal bandwidth (or, equivalently, the chip rate), the Integrate and Dump filter is most effective in attenuating the unwanted aliased image. This performance can be seen from the transfer function G(w) of a decimation filter, where:

$$G(w) = \sin(w')/w' \text{ and } w' = (2\pi Nf)/f_{SA}.$$

Figure 13 shows a plot of the gain of this transfer function as a function of the normalized frequency ($N\ f/F_{SA}$). To effect the desired low-pass filter and eliminate the aliased image in the baseband Nyquist region appearing in line 5 of Figure 11, the attenuation must be suitably high for frequencies greater than, in the worst case, 1/2 B. Given a defined signal bandwidth B, however, judicious choice of f1 and f_{SA} allows a higher break frequency to be chosen, as will be discussed.

As an extreme worst case, if $f1 = 1/4f_{SA}$ and $B=1/2f_{SA}$, corresponding to the highest chip rate that can be handled for a given value of f_{SA}, then the break frequency must be 1/2B (equal to $1/4f_{SA}$). In this example, then, $N = f_{SA}/B=2$ and the attenuation provided by the Integrate and Dump filter is given by the curve of Figure 13 for values of ($N\ f/f_{SA}$) greater than 1/2. As can be seen, the attenuation will be at least equal to the peak of the corresponding lobe or at least ~13 dB. This sidelobe peak is a worst case, and much of the alias energy outside the desired band will be attenuated by more than 13 dB. Nonetheless, the presence of unattenuated energy from the unwanted alias degrades performance. It is for this reason that Direct I.F. Sampling Mode is only recommended for received PN chip rates less than $1/8\ f_{SA}$; in other words, for $B<1/4\ f_{SA}$. The attenuation realized by the Integrate and Dump filter is then further determined by the choice of the I.F. frequency f_1 and the I.F. sampling rate f_{SA}.

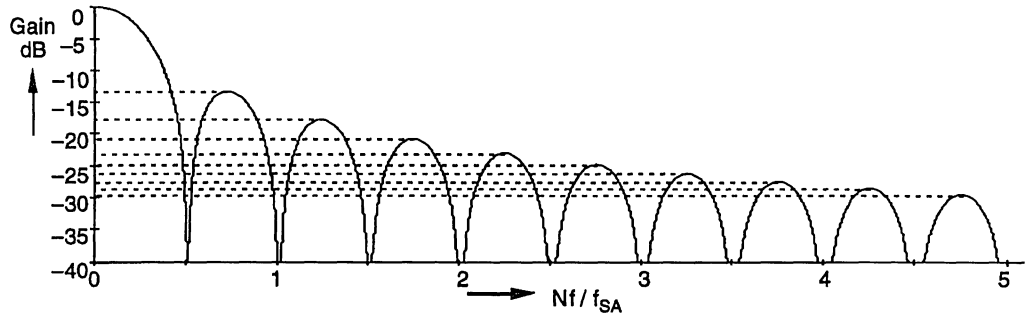

Figure 13. G(ω) = dom (ω')/ω', where ω' = (2πNf)/f_{SA}

The choice of the I.F. frequency and sampling rate is crucial so that the unwanted alias of the signal in the baseband Nyquist region lies as far as possible from the desired signal to permit maximum attenuation. The optimum separation of the desired signal and the unwanted alias occurs when the alias is centered at the bounds of the baseband Nyquist region, $|f| = 1/2\ f_{SA}$ as shown in Figure 14. In this case, the desired signal is equally spaced from the unwanted aliases in both the positive and negative frequency domains and $f1 = 1/4\ f_{SA}$. Consider, then, the worst case appropriate for Direct I.F. Sampling Mode. If $B<1/4\ f_{SA}$ as has been said to be appropriate for Direct I.F. Sampling Mode, then $N=f_{SA}/B=4$, the break frequency is $3/8\ f_{SA}$ or greater, and the attenuation provided by the Integrate and Dump filter is given by the curve of Figure 13 for values of $(N\ f/f_{SA})$ greater than 3/2. Here, the attenuation is at least ~21 dB, offering much better attenuation of the unwanted alias than in the previous worst case example. Further analysis shows that if the input SNR is 15 dB, then the alias attenuated by 21 dB will reduce the SNR by approximately 1 dB.

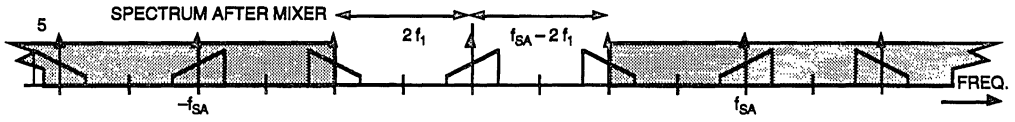

Figure 14. Optimum Condition for Bandpass Sampling

THEORY OF OPERATION (Continued)

The optimum choice of I.F. frequency discussed above can be extended beyond the primary Nyquist region. Since an I.F frequency of $n f_{SA} + f1$ produces exactly the same result for any value of n, the general condition for optimum separation of the desired signal and the unwanted alias is:

$$f1 = n f_{SA} + 1/4 f_{SA} \text{ and } B < 1/2 f_{SA}$$

for positive integer n and positive B and f_1.

And, if care is taken to handle the effect of high side conversion, the following I.F. frequencies also fulfill the optimum condition:

$$f1 = n f_{SA} 1/4 f_{SA} \text{ and } B < 1/2 f_{SA}$$

for positive integer n and positive B and f_1.

Using the Z87200 with Two ADCs in Quadrature Sampling Mode

Quadrature Sampling Mode requires that quadrature I and Q channel I.F. inputs are sampled by two ADCs and input to the Z87200's Downconverter. All four multipliers of the Downconverter's complex multiplier are then used to perform true single sideband downconversion to baseband. Quadrature inputs imply that the input signal is complex, and the input signal spectrum shown in line 1 of Figure 15 is thus only single-sided with no mirror image spectral component. As a result, the image alias within the primary Nyquist region associated with Direct I.F. Sampling Mode does not appear and does not have to be attenuated by the Integrate and Dump filter. As in the prior discussion, this analysis holds as long as $B < 1/2 f_{SA}$, $1/2 B < f1$, and the input spectrum is only defined for frequencies within a single Nyquist region; that is, non-zero over frequencies f such that:

$$(n-1/2)f_{SA} < |f| < (n+1/2)f_{SA}$$

for positive integer n.

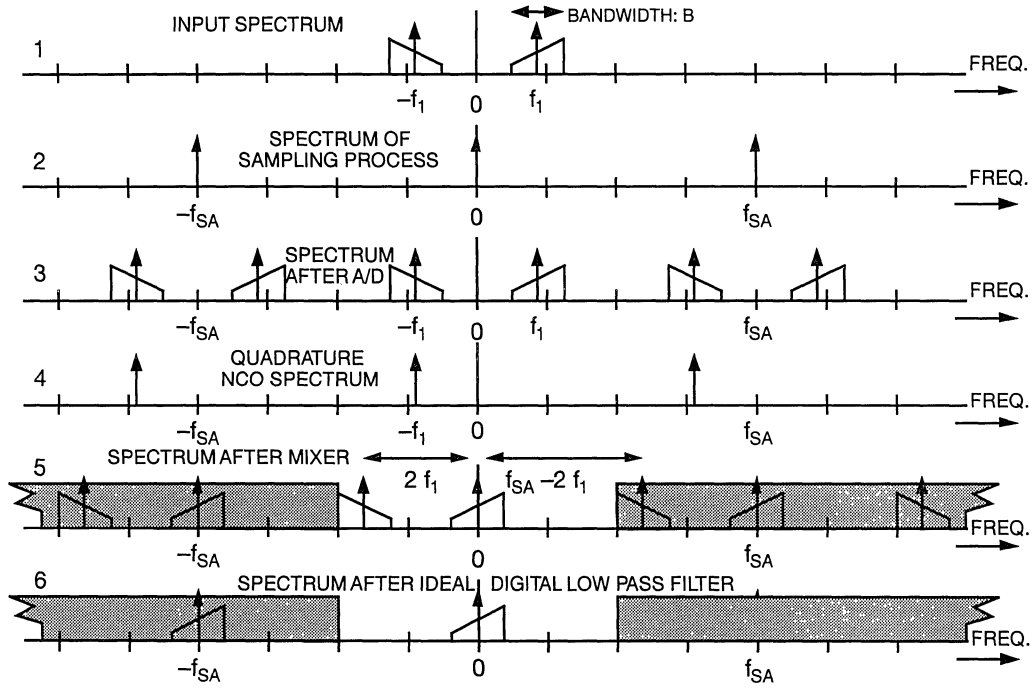

Figure 15. Spectra of Signals in Quadrature Sampling Mode

Differential Demodulation

As noted in the preceding text, computation of the "Dot" and "Cross" products is fundamental to operation of the DPSK Demodulator and Frequency Discriminator. Let I_k and Q_k represent the I and Q channel inputs, respectively, for the k^{th} symbol after downconversion and despreading. The Dot and Cross products can then be defined as:

$$Dot(k) = I_k I_{k-1} + Q_k Q_{k-1}; \text{ and,}$$

$$Cross(k) = Q_k I_{k-1} - I_k Q_{k-1}$$

In the complex domain, these products can be seen to have been defined to form the complex conjugate product between two input samples, one symbol apart. Let the k_{th} input sample, sin(k), be defined as:

$$s_{in}(k) = I(k) + j\,Q(k),$$

where I(k) and Q(k) are the 8-bit peak power PN Matched Filter I and Q channel outputs directed to the DPSK Demodulator. In polar form, $s_{in}(k)$ may be conveniently defined as:

$$s_{in}(k) = A(k)e^{j\emptyset(k)}$$

with

$$A(k)$$

$$\emptyset(k) = \arctan$$

Simple substitution then shows that the complex conjugate product between consecutive symbols (with an arbitrary phase shift introduced to the previous symbol value) may be expressed as:

$$s_{out}(k) = s_{in}(k)\,[s_{in}(k-1) \cdot \omega_{fixed}]^*$$

$$= Dot(k) + j\,Cross(k)$$

where

ω_{fixed} = arbitrary fixed phase rotation;

$Dot(k) = Re[s_{out}(k)]$; and,

$Cross(k) = Im[s_{out}(k)]^*$

The fixed phase rotation ω_{fixed} has been introduced to later simplify the decision criteria. The ability to express real and imaginary parts of the complex conjugate product between consecutive symbols with the Dot and Cross products is the key to their use in DPSK demodulation.

DBPSK Demodulation

In DPSK, the phase difference between successive samples is due to the data modulation phase differences, $\Delta\emptyset$mod, plus any induced phase rotation between symbols, $\Delta\emptyset$rot, resulting from, for example, a frequency offset between the received signal's I.F. and that provided by the Downconverter. For DBPSK, the data modulation differences $\Delta\emptyset$mod can take only the values of 0° or 180°. Expressing the complex phase difference $[\emptyset(k)-\emptyset(k-1)]$ in terms of these components, the decision can be seen to be based on:

$$Sout^{(k)} = A(k)\,A(k-1)\,e^{j\emptyset(k)^*}e^{-j\emptyset(k-1)}$$

$$= A(k)\cdot A(k1)\cdot e^{j[\Delta\emptyset_{mod}(k)+\Delta\emptyset_{rot}(k)]}$$

For DBPSK, only the real part of sout(k), Dot(k), is needed to determine the modulated phase transition:

$$Dot(k) = A(k)\cdot A(k-1)\cdot\cos(\Delta\emptyset_{mod}(k)+\Delta\emptyset rot(k))$$

$$= \pm A(k)\cdot A(k-1)\cdot\cos(\Delta\emptyset_{rot}(k))$$

where the sign is determined by the transmitted data since $\cos[\Delta\emptyset_{mod}(k)] = \pm 1$. As a result,

$$Dot(k) \approx \pm A^2(k)$$

if the amplitude of the signal is constant for consecutive symbols and if the phase rotation $\Delta\emptyset_{rot}(k)$ between symbols is small. The Z87200 DPSK Demodulator can thus use the sign of the Dot product in order to make DBPSK symbol decisions without the introduction of any fixed phase rotation.

THEORY OF OPERATION (Continued)

DQPSK Demodulation

For DQPSK modulation, the possible phase shifts between successive symbols due to the modulation are 0°, 90°, 180°, and 270°. Here, introduction of a phase shift (ω_{fixed}) of ±45° to the previous symbol in the calculation of the Dot and Cross products is desired in order shift the possible phase differences to 45°, 135°, 225°, or 315° so that the DQPSK decision boundaries coincide with the signs of the Dot and Cross products. In the Z87200 DPSK demodulator, phase rotation is accomplished in the signal rotation block by the following transformation of the I and Q channel values:

$$I_{rot}(k)=[\ I(k) - Q(k)]/2 \quad \text{for } 45° \text{ rotation}$$

$$I_{rot}(k)=[\ I(k) + Q(k)]/2 \quad \text{for } -45° \text{ rotation}$$

$$Q_{rot}(k)=[\ I(k) + Q(k)]/2 \quad \text{for } 45° \text{ rotation}$$

$$Q_{rot}(k)=-[\ I(k) + Q(k)]/2 \quad \text{for } -45° \text{ rotation}$$

The divide-by-2 is part of the signal rotation function. This transformation is equivalent to multiplying by $(1 \pm j)/2$ or $(1/\sqrt{2})e^{j\varnothing(fixed)}$ where $\varnothing_{fixed}$ is ±45°. In this case, $s_{out}(k)$ becomes:

$$s_{out}(k)=A(k).A(k-1)^*e^{j\varnothing(k)^*}e^{-j\varnothing(k-1)^*}[\omega_{fixed}]^*$$

$$=A(k).A(k-1)^*e^{j[\Delta\varnothing_{mod}(k)+\Delta\varnothing_{rot}(k)]^*}\ (1/\sqrt{2})e^{j\varnothing(fixed)}$$

$$\sqrt{I^2(K)+Q^2(k)}$$

$$\left(\frac{Q(k)}{I(k)}\right).$$

so that

$$Dot(k)\approx(1/\sqrt{2})A(k)^*A(k-1)^*\cos(\Delta\varnothing_{mod}(k) - \varnothing_{fixed})$$

$$Cross(k)\approx(1/\sqrt{2})A(k)^*A(k-1)^*\sin(\Delta\varnothing_{mod}(k) - \varnothing_{fixed})$$

where the phase rotation $\Delta\varnothing_{rot}(k)$ due to the frequency offset between symbols has been assumed negligible.

A summary of the Dot(k) and Cross(k) products for the possible values of $\Delta\varnothing_{mod}(k)$ and $\varnothing_{fixed}$ is shown below, illustrating how the sign of the Dot and Cross products allow the symbol decision to be made:

	$\varnothing_{fixed}$ = -45°		$\varnothing_{fixed}$ = +45°		
$\Delta\varnothing_{mod}(k)$	Dot(k)	Cross (k)	$\Delta\varnothing_{mod}$ (k)	Dot(k)	Cross (k)
0°	$+A^2$	$+A^2$	0°	$+A^2$	$-A^2$
90°	$-A^2$	$+A^2$	90°	$+A^2$	$+A^2$
180°	$-A^2$	$-A^2$	180°	$-A^2$	$+A^2$
270°	$+A^2$	$-A^2$	270°	$-A^2$	$-A^2$

π/4 QPSK Demodulation

The Z87200 DPSK Demodulator decision logic is designed so that correct DQPSK decisions are made with a signal rotation of $\varnothing_{fixed}$= −45°. For π/4 QPSK modulation, however, the modulator itself inserts 45° between consecutive symbols, and the possible phase shifts between successive symbols due to modulation are 45°, 135°, 225°, and 315°. As a result, the DPSK Demodulator should be configured for π/4 QPSK with $\varnothing_{fixed}$=0°.

DQPSK Phasing and I/Q Channel Reversal

The Z87200 uses Differential BPSK and QPSK modulation and demodulation, meaning that the data is modulated on the carrier as phase changes. At the demodulator, the data is recovered by monitoring the phase change over a symbol period.

The Z87200 provides configuration control to specifically address DPSK phasing and I/Q channel reversal: the Signal Rotation control register, bits 0 and 1 of address 33_H, and the Reverse I and Q control register, bit 0 of address 36_H. The first register causes an insertion of ±45° in phase between consecutive symbols at the receiver, while the second register switches the I and Q channels presented to the DPSK demodulator. As discussed in the Z87200 appendix, the introduction of a phase shift between consecutive symbols changes the mapping of the input data with respect to the decision boundaries defined by the "Cross" and "Dot" product axes.

Assuming that the transmitted DQPSK modulation phasing is differentially encoded as defined in Table 3, the phase shift between consecutive symbols should always be set to –45°; that is, bits 1 and 0 of address 33_H should be set to 11. Similarly, when the transmission path from modulator to demodulator does not introduce a frequency (or phase direction) reversal, the "reverse I and Q" control function should be disabled; that is, bit 0 of address 36H should be set to 0. Note that, in the case of DBPSK, the phase increments are either 0 or 180° and frequency reversal has no impact.

If frequency reversal does take place, however, correct DQPSK demodulation can be achieved by enabling I and Q reversal; that is, the entry into bit 0 of address 36_H should be set to 1. Frequency reversal may occur in the up or down conversion process, depending on which mixing product is selected for further processing. No reversal occurs when the following conditions exist: when the mixing at the transmitter is performed by processing the sum frequency of the local oscillator and the modulator; when the mixing at the receiver is performed by subtracting the local oscillator from the incoming signal; and when the in-phase and quadrature inputs into the I and Q analog-to-digital converters are correctly connected such that the in-phase component leads the quadrature component by 90°. Under these conditions, bit 0 of address 36_H should be set to 0; otherwise, the I and Q channels may need to be reversed at the DPSK demodulator (by setting bit 0 of address 36_H to 1) in order to achieve proper demodulation.

Frequency Error Signal Generation

The frequency discriminator function or error signal is generated based on the Dot and Cross products. The objective is an error signal that is proportional to the sine of the phase difference between the present and prior symbol after correcting for the estimated phase increments due to data modulation. In the Z87200 Frequency Discriminator, the frequency error is calculated through a decision-directed cross-product algorithm and is then used with the Loop Filter to correct the NCO frequency. Assuming an input sin(k), where:

$$s_{in}(k) = I(k) + j\,Q(k),$$

the algorithm calculates the frequency discriminator function for DBPSK, $s_{AFC/BPSK}(k)$, as:

$S_{AFC/BPSK}(k)$=SIGN[Dot(k)]*Cross(k)

=SIGN[Dot(k)]*A(k)*A(k-1)*sin(Ø(k)-Ø(k-1))

=SIGN[Dot(k)]*A(k)*A(k-1)*sin(ΔØmod(k) + ΔØrot(k))

≈SIGN[Dot(k)]*A2(k)*cos[ΔØmod(k)]*sin[ΔØrot(k)]

≈A2(k)*sin[ΔØrot(k)]*

The final result assumes that the amplitude of the signal is constant over consecutive symbols and shows that the discriminator function is directly related to the change in phase between successive symbols. Since the interval between successive symbols is fixed, the discriminator function can be interpreted as a frequency error signal.

For DQPSK signals, the Z87200 computes the discriminator function $S_{AFC/QPSK}(k)$ as:

$S_{AFC/QPSK}(k)$=SIGN[Dot(k)] Cross(k) - SIGN[Cross(k)] Dot(k),

where the above expression can be reduced to the same as for DBPSK,

$S_{AFC/QPSK}(k)$≈A2(k)*sin(ΔØrot(k)).

BPSK/QPSK Modulation

The Z87200 incorporates a Direct Digital Synthesizer (DDS) to implement its on-chip BPSK/QPSK modulator. In the Z87200 design, the NCO and thus the sampling clock for the modulator is driven by fRXIFCLK; for this reason, both TXIFCLK and RXIFCLK must be common if the on-chip BPSK/QPSK modulator is to be used. The BPSK/QPSK modulator can then be used to generate the transmit output signal at a programmable IF frequency, thereby eliminating the need for an external modulator. Because it is a sampled data system like the Downconverter of the Z87200, however, care must be taken to ensure that the results of aliasing do not adversely affect the output transmit signal.

4

THEORY OF OPERATION (Continued)

In general, when a DDS is used to generate an unmodulated signal, the stepped sine wave generated by the DDS has spectral components at integer multiples of the DDS sampling clock. In other words, the Z87200's BPSK/QPSK modulator, when programmed to generate a signal at I.F. frequency f_{OUT}, will produce spectral components at $\pm f_{OUT}$ as well as at ($n_{RXIFCLK} \pm f_{OUT}$), where n is a positive or negative integer. Because of these aliases, one generally cannot program the NCO to provide an output frequency f_{OUT} greater than the Nyquist frequency $f_{RXIFCLK/2}$. When the I.F. frequency f_{OUT} is modulated, however, degradations to the output signal due to aliasing can result even when f_{OUT} is less than $f_{RXIFCLK/2}$.

In particular, the Z87200's PN modulation results in a transmit signal that has a power spectral density characterizable as a sinc function (sin(x)/x) centered about the I.F. frequency f_{OUT}. Nulls of the sinc function occur at integer multiples of the PN chip rate, and the null-to-null signal bandwidth of the Z87200's transmit signal about f_{OUT} is twice the transmit chip rate. The presence of modulation sidelobes and their interaction with aliases due to sampling, however, will result in distortion of the mainlobe of the baseband component centered at f_{OUT} unless attention is paid to the interaction of the chip rate, the I.F. frequency f_{OUT}, and the sampling rate fRXIFCLK.

In the example of Figure 18, the spectrum drawn in bold represents a signal where f_{OUT} has been programmed to be (0.4 x $f_{RXIFCLK}$) and has been PN-modulated at a chip rate of (0.1 x $f_{RXIFCLK}$). The first alias of the negative frequency version of this signal appears centered about (0.6 x $f_{RXIFCLK}$) and is shown as the lighter curve. As can be seen, energy of the second and third modulation sidelobes of the first alias is present within the mainlobe of the baseband component, resulting in distortion. One would typically filter the digital-to-analog converted output of the Z87200's BPSK/QPSK modulator to remove the energy outside the modulation mainlobe, but such filtering will not affect any aliasing distortion within the mainlobe as described here. Note that the nulls of the modulated signal aliases in this example coincide here only due to the choice of values for the I.F. frequency, sampling rate, and PN chip rate; in general, the nulls will not coincide. Note also that the filtering effect of sampling has been neglected in this discussion — in general, the aliases will be suppressed by a second sinc function, sin(f')/(f'), where f' = $\pi f/f_{RXIFCLK}$, but this effect is not very significant for the baseband component and first alias.

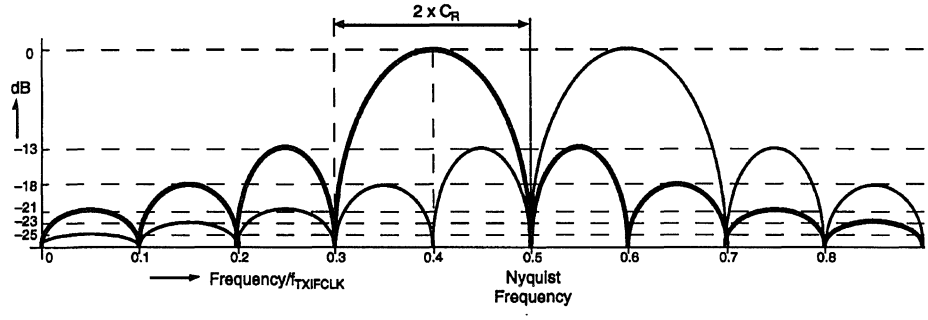

Figure 16. Spectrum of DDS modulated at 0.1 x $f_{RXIFCLK}$ when carrier frequency is set to 0.4 x $f_{RXIFCLK}$

The example of Figure 18 demonstrates that aliasing distortion of the BPSK/QPSK modulator output will result if significant energy of the baseband component's spectrum falls beyond the Nyquist frequency of $f_{RXIFCLK/2}$. The first alias will then shift that energy into the region below the Nyquist frequency and potentially interfere with the desired signal. In Figure 19 the second and third sidelobes of the first alias fall within the mainlobe of the baseband component, where the magnitude of this corrupting signal is approximately –13 dBc.

In Figure 20, by contrast, the level of distortion is considerably reduced by programming an I.F. frequency that increases the separation of the baseband mainlobe from the alias mainlobe. Here, the carrier frequency has been reduced to 0.25 x $f_{RXIFCLK}$, and now the fourth and fifth sidelobes of the first alias lie in the same part of the spectrum as the baseband mainlobe, reducing the distorting energy to approximately –23 dBc at the peak of the fourth sidelobe.

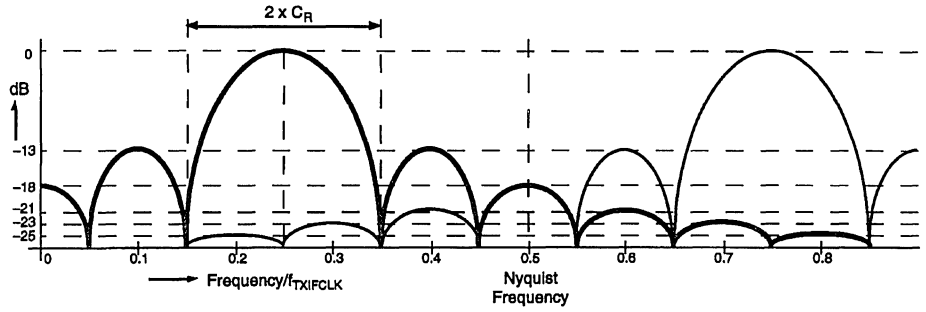

Figure 17. Spectrum of DDS modulated at 0.1 x $f_{RXIFCLK}$ when carrier frequency is set to 0.25 x $f_{RXIFCLK}$

THEORY OF OPERATION (Continued)

In both of the cases shown above, and especially the second, the level of the distortion is low enough so that the performance penalty would not be very great. And, of course, in a spread-spectrum system the effective distortion is reduced by the processing gain realized in despreading the signal at the receiver. In both of these examples, however, the PN chip rate is a very modest 10% of the frequency of the system clock; if the chip rate is increased to 40% of $f_{RXIFCLK}$, then the situation is very different, as shown in Figure 20.

In Figure 20, both the chip rate and the carrier frequency have been set at 40% of the clock frequency. As a result, the baseband mainlobe straddles the Nyquist frequency, and the first alias of the mainlobe overlaps the spectrum of the baseband mainlobe, thereby creating very significant aliasing distortion which cannot be eliminated by filtering. This level of distortion would severely affect the performance of the system and, in general, would be completely unacceptable.

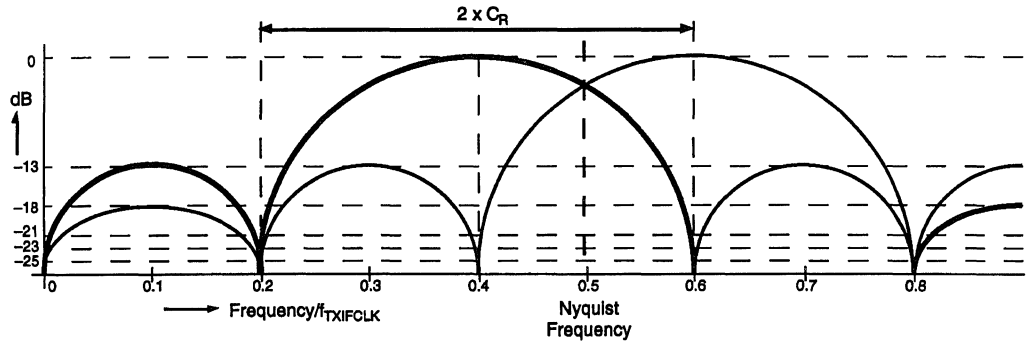

Figure 18. Spectrum of DDS Modulated at 0.4 x $f_{RXIFCLK}$ When Carrier Frequency is set to 0.4 x $f_{RXIFCLK}$

Reducing the carrier frequency to 25% of the clock frequency can reduce the distortion level, as shown in Figure 21. Although the distortion is still fairly severe, adequate performance may be obtainable as a result of the system's processing gain, but the performance would be many dB off the theoretical limit. As the PN chip rate of the system increases, then so, too, does the effect of aliasing distortion in the modulator, resulting in performance degradation. As a rule-of-thumb, one may restrict the I.F. frequency to 25% of the clock frequency, but, in general, each application and combination of PN chip rate, I.F. frequency, and TXIFCLK/RXIFCLK frequency is unique and should be evaluated before deciding whether to use the Z87200's internal BPSK/QPSK modulator.

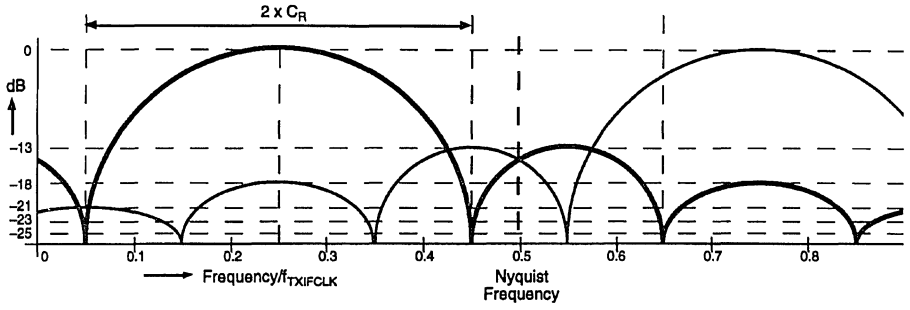

Figure 19. Spectrum of DDS Modulated at 0.4 x $f_{RXIFCLK}$ When Carrier Frequency is set to 0.25 x $f_{RXIFCLK}$

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3
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5 Wireless Technical Article "Superior Cordless Telephony"
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7
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DIGITAL CHIP SET BRINGS SUPERIOR RANGE, VOICE CLARITY, AND NOISE IMMUNITY TO CORDLESS TELEPHONY

BY VINCE HU, LINCOM CORP. AND DIMITRI DESMONS, ZILOG, INC.

INTRODUCTION

A new digital chip set developed jointly by Zilog Incorporated in Campbell, California and LinCom Corporation in Los Angeles, California promises to usher in a new generation of cordless telephones which offer vastly improved performance over existing cordless phones.

The availability of frequency spectrum in the 902 to 928 MHz band, also known as the ISM band, for unlicensed operation has spurred the development of a new generation of wireless products for applications ranging from wireless local area networks, point of sale terminals, to point-to-point radios in addition to digital cordless telephones.

The Z87000 and the Z87010 represent a two chip solution which provides mixed mode digital/analog circuitry to perform the majority of the signal processing functions between IF and baseband frequencies which are required for cordless telephone operation. The two chip set is bundled into a package providing a complete reference solution for OEM vendors which includes the man machine interface and telco support software, RF circuit schematics, and product development platforms.

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CORDLESS TELEPHONY

Cordless telephones were originally introduced to the mass consumer market in the 1980's. These first generation phones transmit and receive in the 46 and 49 MHz bands in the United States. Employing principally analog technology, they use FM modulation to relay full duplex voice between the handset and basestation. The low cost and complexity of these phones has enabled affordability and in turn resulted in widespread consumer acceptance. Nevertheless, phone performance is highly susceptible to background noise and other types of man-made interference. Furthermore, range is extremely limited due to multipath fading and other signal attenuation caused by interior walls and structures typical to household environments. In addition, co-existence between multiple cordless phones in close proximity is severely restricted due to co-channel interference. Indeed, many consumers frequently complain about hearing their neighbor's phone conversations or being altogether unable to place or receive calls. These analog phones have been refined in recent years to include the use of multiple frequency channels in order to avoid interference. Current phones provide 10-channel capability, some with automatic channel selection. The FCC recently approved 25 channel phone operation. However, such improvements only marginally address the major performance impediments such as multipath and co-channel interference which usually limits phone operating range and can especially degrade analog voice quality.

In 1985, however, the U.S. Federal Communications Commission drafted the Part 15.247 regulations permitting unlicensed use of three frequency bands for Industrial, Scientific, and Medical applications (denoted as the ISM bands). The three bands include spectrum between 902 to 928 MHz, 2400 to 2483.5 MHz, and 5725 to 5850 MHz. The FCC regulations allow considerable design flexibility to address a wide array of voice and data communication applications. The use of the 900 MHz ISM band for cordless telephony inherently provides the possibility of improved range because of the better propagation characteristics compared to 46/49 MHz. In addition, the FCC regulations allow up to 1 Watt of transmit power which will further increase range and improve communications performance. The availability of great bandwidth at 900 MHz than at 46/49 MHz makes the use of digital transmission and reception more easily implementable.

CORDLESS TELEPHONY (CONTINUED)

Although this band is not exclusively set aside for spread spectrum operation, applications employing spread spectrum techniques will enjoy improved interference immunity, increased range, inherent privacy and security, and greatly enhanced voice quality.

Currently between 18 to 20 million cordless phones are sold annually in the United States (according to the EIA). Almost 52% of all US households possess a cordless telephone which represents a significant penetration of the US population. The overwhelming majority of these are analog phones operating at 46/49 MHz. However, it is estimated that by the end of 1995, almost 5 to 10% of all cordless phones sold will be 900 MHz phones. The market share is expected to increase as enabling technology is developed to reduce the retail price point to well below $200.00. Over the last two years, a number of new cordless phone products have been introduced using the 900 MHz ISM band. These employ either completely analog transmission or digital transmission. However, until now, product offerings employing digital spread spectrum transmission have been somewhat limited and have fallen short of the expectations of the technology.

The key challenges to designing cordless telephones operating at 900 MHz have been reaching a reasonable cost and battery life comparable to the 46/49 MHz phones. In meeting these challenges, Zilog has developed its ZPhone cordless phone system design upon the Z87000 spread spectrum controller and Z87010 ADPCM processor. While other chip sets developed for use in spread spectrum cordless telephones are available, Zilog's Z87000/Z87010 chip set combination is the only complete design solution available. As part of its effort to support cordless phone manufacturers in developing 900 MHz cordless telephones, Zilog not only provides the IC's which perform all of the IF to baseband signal processing, but it also provides source code and object libraries for software residing on an integrated processor which performs the complete communications protocol and supports all man machine interface and telco functions, complete circuit schematics including a reference RF section design, a comprehensive bill of materials, full documentation and technical support.

ZPHONE SYSTEM OVERVIEW

Zilog's Z87000 Cordless Phone Transceiver/Controller and Z87010 ADPCM Processor together allow implementation of a 900 MHz spread spectrum phone that is in compliance with the United States Federal Communications Commission regulations for operation in the ISM band. These chips are designed to support a specific phone system design—the "ZPhone"—which uses frequency hopping and digital frequency shift keying (FSK) modulation to permit high power transmission and extended range, 32 kbps ADPCM speech coding to achieve high voice quality, adaptive frequency hopping to reduce the effects of in-band interferers, adaptive transmit power control to extend battery life, and an overall system approach that minimizes system costs.

The spread spectrum technique employed is frequency hopping. The hop dwell time is 4 milliseconds. Data is communicated between the handset and basestation via time division duplex (TDD) operation. Each frequency dwell time defines a single TDD frame slot. These TDD frame slots are in turn divided into a time slot during which the basestation transmits a data packed to the handset and a time slot during which the handset transmits a data packet to the basestation. These transmits slots are separated by two distinct guard time slots. Figure 1 depicts the TDD frame structure. The guard times between signal transmission and reception and between frequency hops are provided to allow time for hardware switching and settling. Frame timing is generated via frame counters at the handset and basestation. The basestation establishes the time reference for the overall ZPhone system. The handset tracks the basestation frame timing. The difference in values between the basestation and handset frame counters thus reflect the propagation delay between the basestation and the handset.

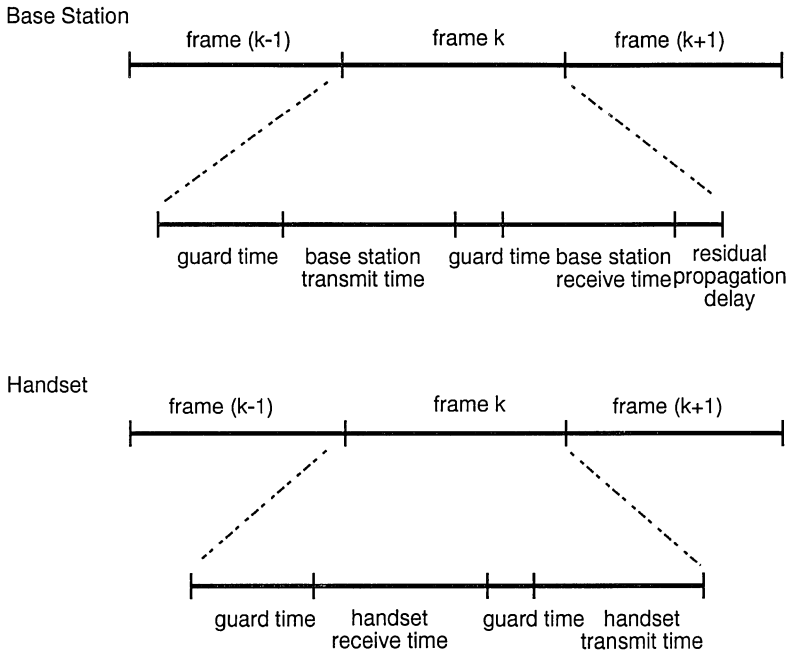

Figure 1. TDD Frame Structure

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ZPHONE SYSTEM OVERVIEW (Continued)

The burst transmission rate is 93 kbps. The 3 dB transmission bandwidth for each hop channel is 180 kHz. With a channel separation of 182 kHz, a total of 142 possible hop frequencies are available between 902 MHz and 928 MHz. At any given time, only 64 of these channels are actively used. The ZPhone system is designed to adaptively avoid those channels with severe interference. This is accomplished by replacing active frequencies which possess poor SNR conditions with hop frequencies from the pool of remaining inactive frequencies. The hopping sequence, i.e. the order in which the active frequencies are hopped to, is generated according to the state of a pseudo-noise sequence generator.

Table 1. Signaling-Multiplex (S-MUX) Format

64 bits	16 bits	8 bits	24 bits	16 bits	16 bits	4 bits
preamble	unique word	code seed	ID security code	control	signaling	antenna switching (handset only)

Table 2. Talk Multiplex (T-Mux) Format

128 bits	16 bits	4 bits
voice	signaling (handset only)	antenna switching

Data is packetized and transmitted in burst during each TDD frame in either Signaling Multiplex (S-Mux) or Talk Multiplex (T-Mux) frame formats. At the basestation, the transmit packets are 144 bits; at the handset the transmit packet is 148 bits. The S-Mux format is used to establish two-way link communication between the handset and basestation. It is optimized for fast acquisition and synchronization. The T-Mux format is used during voice communications between the handset and basestation. Tables 1 and 2 depict the S-Mux and T-Mux frame formats. The S-Mux frame consists of a 64-bit alternating 1 and 0 preamble. This preamble is followed by a 16-bit unique word sequence. After the unique word is an 8-bit field which is updated each frame to represent the state of the pseudo-noise generator register which is used to determine the hopping sequence. The code seed field is followed by a 24-bit ID security code field. This ID code is used to prevent unauthorized access to the cordless phone system. The initial value of the ID security code is set to a default value upon power up but is randomized as time progresses so that a handset can only access its own designated basestation and vice versa. The ID security code is followed by a 16-bit control field. This control field is used to transfer basic alert and link setup information. Finally the last 16-bits are reserved for the transfer of signaling information. For the handset, the transmit packed is 4 bits longer because of the addition of a fixed known pattern used in the antenna diversity switching algorithm.

The basestation hardware can be configured to operate with dual antenna ports to provide antenna diversity. At the end of the reception of a frame from the handset, the basestation performs an energy measurement at each antenna port during the last four bits which are always known. On the basis of these measurements, the antenna switching is toggled to gate the antenna port with the largest energy measurement from the previous frame during the next frame.

The T-Mux format consists of 128 bits of voice data corresponding to 32 4-bit voice sample nibbles. The T-Mux frame also has 16-bit field dedicated for signaling and, for the handset, contains an additional four bits of a fixed pattern to be used for antenna diversity. In order to ensure sufficient data transitions to support accurate symbol timing synchronization, the polarity of several of the bits in the voice field is reversed.

At the handset there are four operating modes: Acquisition Mode, Wake/Sleep Mode, Talk Mode, and Cradle Mode. At the basestation, there are three operating modes: Idle Mode, Talk Mode and Cradle Mode. Figures 2 and 3 illustrate these modes. Transitions between the modes at the handset are coordinated with the transitions at the basestation and vice versa. The basestation' s Idle Mode corresponds to either the Acquisition Mode or the Wake/Sleep Mode of the handset; the basestation's Talk mode corresponds to the handset's Talk Mode; and the basestation's Cradle Mode corresponds to the handset's Cradle Mode.

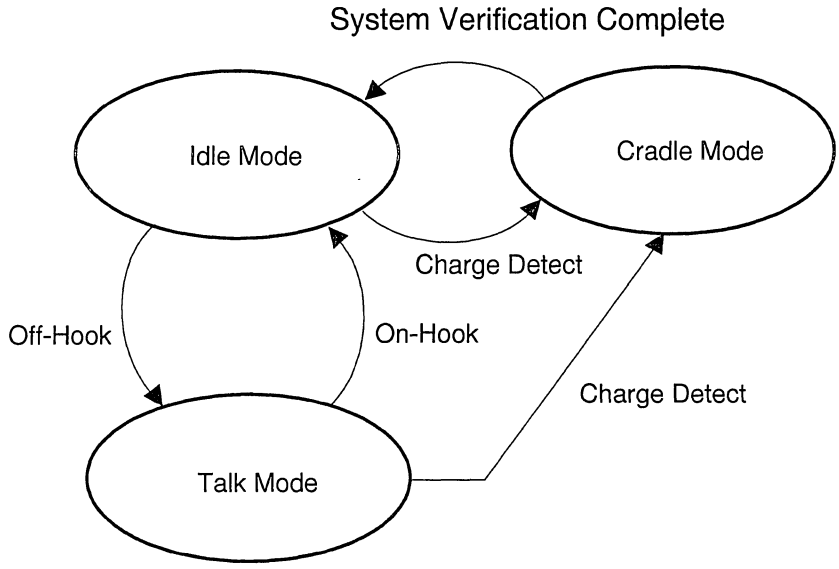

Figure 2. Basestation Operating Modes

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ZPHONE SYSTEM OVERVIEW (Continued)

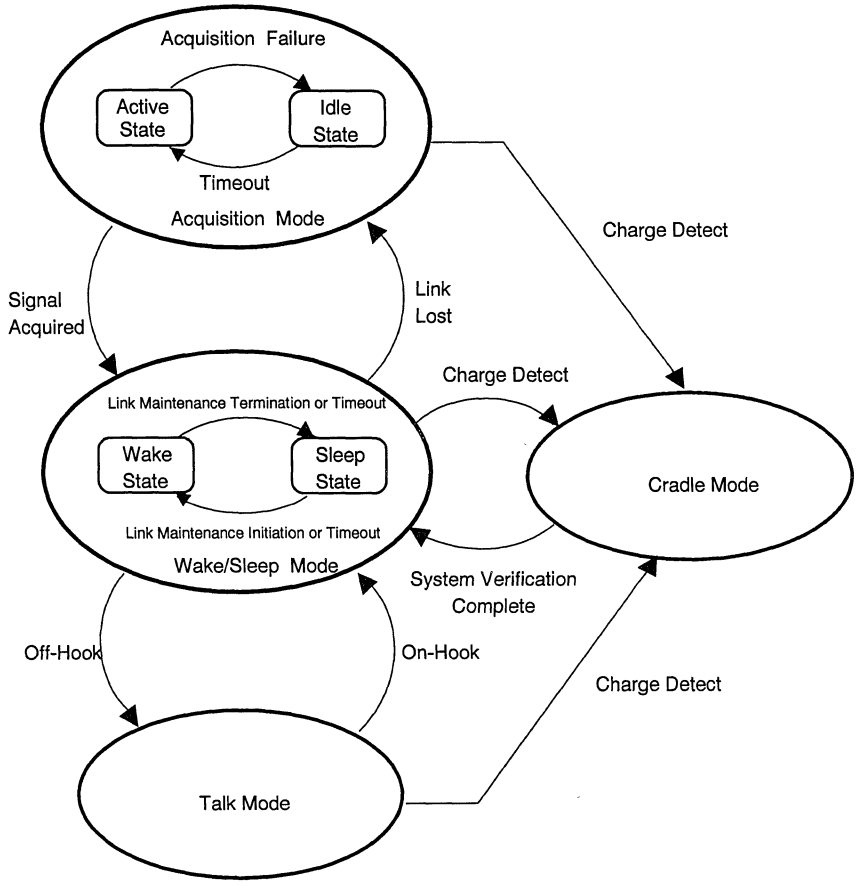


Figure 3. Handset Operating Modes

In Idle Mode, the basestation transmits S-Mux frames for the purpose of handset acquisition when required. The handset remains in a listen only state in Acquisition Mode while attempting to acquire and synchronize its local frame timing to the received S-Mux frames. After synchronizing to the basestation. the handset reverts to Wake/Sleep Mode in which it turns off all power to conserve standby battery life and periodically power on only to ensure that it is still synchronized to the basestation. When a two-way link is required for voice communication, both the handset and basestation activate their Talk modes. The Cradle Mode is activated when the handset is placed in the basestation charger. During this mode the handset and basestation exchange information to verify ID security codes and check for consistency between their frequency hopping tables.

ZPHONE SYSTEM COMPONENTS

Figure 4 depicts the major system components and the signal flow for the ZPhone system. The basestation and handsets are similar in that they both consist of frequency agile RF sections, a Z87000 spread spectrum transceiver controller, a Z87010 ADPCM speech processor, and a PCM Codec interface. The basestation and handset differ primarily in that at the handset the PCM codec interfaces directly to speaker/microphone pair whereas in the basestation, the PCM codec connects to a telephone line interface. Other miscellaneous functions such as the keypad, LED's ringer, et cetera comprise the man-machine interface functions.

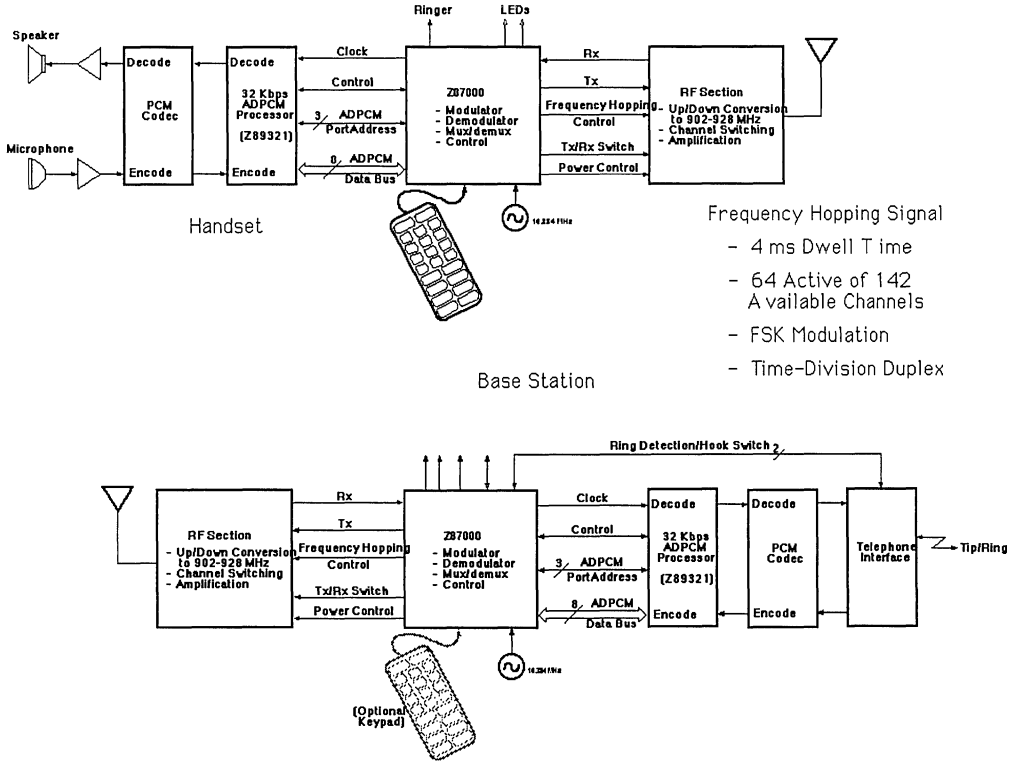


Figure 4. Z87000 Cordless Phone Transceiver/Controller

ZPHONE SYSTEM COMPONENTS (Continued)

The RF sections perform amplification, channel switching, upconversion and downconversion to/from 902-928 MHz. Note that the chip set solution is essentially independent of the actual transmitted frequency. Hence, with the appropriate RF design and supporting software, the chip set can be used to implement a cordless telephone operating at the 2.4 or 5.7 GHz ISM bands or any other band, hopping or not hopping. The RF receive and transmit signals interface directly to the Z87000 spread spectrum transceiver controller at an IF frequency of 10.7 MHz.

Figure 5 depicts the Z87000 functional block diagram. For both transmit and receive, the interface signals at the IF are FSK modulated. The chip contains a 1-bit analog to digital converter with oversampling to digitize and process the received IF signal at 10.7 MHz. On-chip digital circuitry performs downconversion, frequency tracking, limiter-discriminator detection, bit synchronization, frame synchronization, and channel signal to noise ratio estimation. The received serial data stream is collected into 4-bit nibbles at a receiver rate buffer. These nibbles are then transferred via an 8-bit bidirectional interface to the voice processor. On the transmit side, a rate buffer collects 4-bit nibble samples from the same 8-bit bidirectional interface. These samples are then converted to serial format processed by digital circuitry which performs FSK modulation and upconversion to an IF of 10.7 MHz. An on-chip 4-bit digital to analog converter converts the samples from the modulator to provide analog samples for transmission at the RF interface. A separate block contains frame counters and event triggered circuitry to maintain frame timing and generate critical internal and external timing signals. This block also possesses an 8-bit analog to digital converter to sample the analog received signal strength indicator from the RF section and a 4-bit digital to analog converter to provide 16 level control of the transmitted power output.

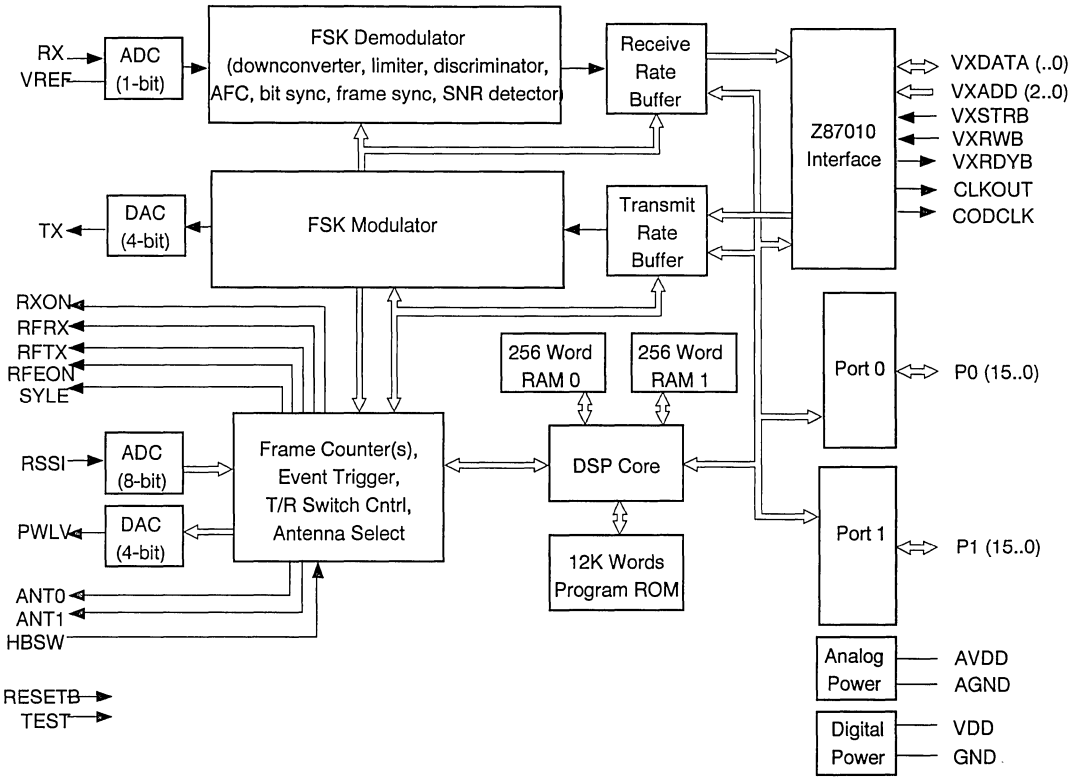


Figure 5. Z87000 Functional Block Diagram

The Z87000 contains a 16-bit fixed point digital signal processing core. The core controls 32 bits of general purpose I/O which can be individually programmed for input or output to support man-machine interface and other telco support functions.

The Z87010 implements the voice compression and decompression algorithms using the CCITT defined G.721 standard for adaptive delta pulse coded modulation. The Z87010 employs essentially the same 16-bit fixed point digital signal processing core as does the Z87000.

ZPHONE LAYERED COMMUNICATION PROTOCOL

Communication between the handset and basestation is performed via a software protocol consisting of three network layers as depicted in Figure 6. Each network layer establishes essentially seamless communication between the handset and basestations. Messages generated at one layer of the basestation or handset are communicated to the corresponding layer at the handset or basestation by first passing through any lower layers and then through the physical radio transmission channel, with the exchange of messages governed by the rules and procedures of that layer's protocol. The network architecture is broadly based on the layered philosophy of the ISO Open Systems Interconnection Reference Manual.

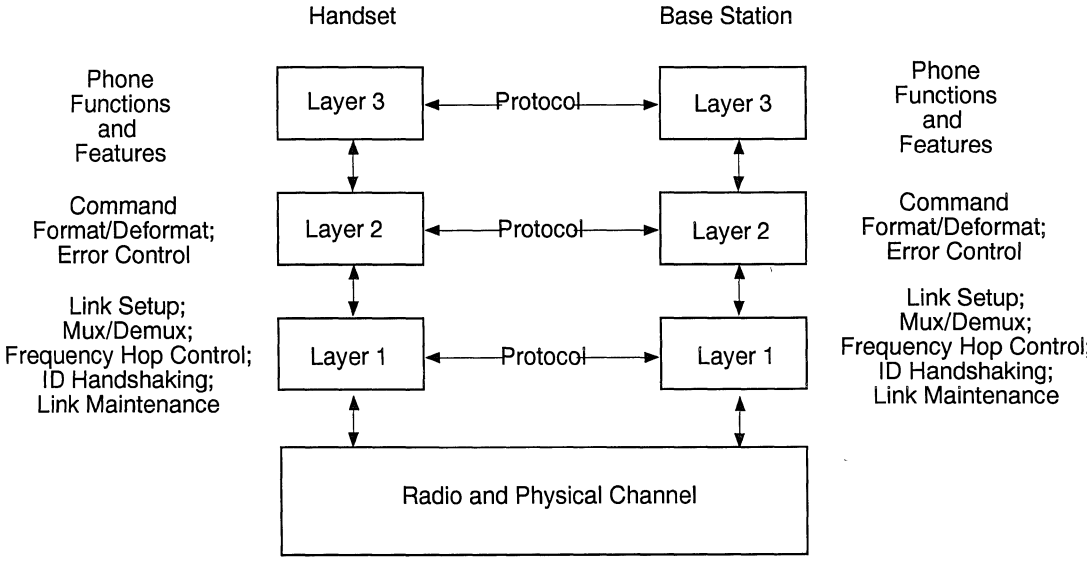


Figure 6. Signaling Architecture

The layer 1 protocol is responsible for operational control of the ZPhone communications circuitry, including support and control of the time division duplexing, signal acquisition, frequency hopping and wake/sleep cycles. Layer 1 also performs multiplexing/demultiplexing of signaling data, ID security code hand-shaking, two-way link communication setup and control, and various link maintenance functions. Link maintenance includes adaptive hop channel frequency assignment, transmit power control, and frequency uncertainty compensation.

The layer 2 protocol is responsible for message formatting of the signaling data, performing acknowledged and unacknowledged signaling data transfer, and signaling data error detection and correction through re-transmission. These layer 2 functions are employed by both the layer 1 and layer 3 protocols to support operation of the Zphone. Information is shuffled between the handset and basestation using variable length Information Elements. These information elements are broken down and formatted into 64-bit message code words. Message codewords include a control octet indicating the message type and sequence number as well as 2 cyclic redundancy code (CRC) octets for error detection.

The layer 3 protocol uses the facilities provided by layers 1 and 2 to offer support of the man machine interface, support of the interface to the public switched telephone network (PSTN), and support of the interface between the Z87000 itself and the Z87010 voice processor. A layer 3 message is defined in terms of information elements which are delivered by layer 2 to or from the remote end. This "application" layer is typically where user specific functions such as memory dialing, LCD support, et cetera are imple-

mented. The layer 3 software is written entirely in C code for easy maintenance and modification. As part of its reference design solution, Zilog provides fully functional layer 3 software to OEM developers which implement advanced phone features taking advantage of most of the Zphone's system capabilities. However, the source code for this software is provided as well as a firmware development platform which permits manufacturers the ability to customize their own man machine interface.

THE ZPHONE DEVELOPMENT KIT

For faster easier development, Zilog offers reference design development kits. The development kit contains a pair of ZPhone Handset/Basestation Evaluation Boards, ZPhone Software, Z87000 In-Circuit Emulators, Z87000 Protopacks, and the Z87000 Software Development Toolset including a C Compiler and Assembler.

The ZPhone Handset/Basestation Evaluation Board can be configured as either a handset or basestation. It consists of an assembled circuit board, the Z87000 spread spectrum controller with telephone software, and the Z87010 speech encoder/decoder. Also included are a telephone line interface, handset speaker, microphone, and an AC adapter. Two such boards can be connected to RF modules and form a complete, full featured cordless telephone with intercom capabilities. The boards may also be connected through an IF link only and used with the Z87000 In-Circuit Emulator to develop custom application software.

The entire ZPhone software suite is mapped to 12K Words of ROM and provided as part of the reference design development kit. The lower 8K Words make up the lower level software functions which control basic transceiver operation. The upper 4K Words implement application level software including the implementation of special features. The software currently provides the following features:

- Tone/Pulse Dialing
- 20 Number Memory
- Redial/Pause
- Flash
- Hold
- Mute
- Page/Intercom
- Handset Volume Control
- Ringer Volume Control
- Talk, Low Battery, Mute, Charge Indicators

The Z87000 In-Circuit Emulator allows ZPhone OEMs to customize the phone application software to their own specific needs. With the Z87000 ICEBOX, the software can be downloaded from a PC and debuffed in a real time development platform. With this tool, the execution of the code can easily be traced.

The Z87000 Protopack is a simple emulation module which allows the application software to be loaded on EPROM and tested in an application system.

The Z87000 Software Development Toolset consists of an assembler and compiler packages written to assist rapid application code development and debug.

Production samples are currently available. For pricing and delivery information or to obtain sample devices and reference design development kits.

Z87C00/Z87L00
Spread Spectrum Controllers 1

Z87C13/Z87L13
Audio Encoder/Decoders 2

Z87100 FM Modulator
Wireless Transmitter 3

Z87200 Spread-Spectrum
Transceiver 4

Wireless Technical Article
"Superior Cordless Telephony" 5

Packaging & Ordering Information **6**

Wireless Family
Support Products 7

Zilog Sales Offices,
Representatives & Distributors Z

Zilog's Literature Guide
Ordering Information L

WIRELESS PRODUCT FAMILY
PACKAGING AND ORDERING INFORMATION

For ordering assistance on these or any Zilog product, please contact your local Zilog sales office.

Z87000/Z87L00

16.384 MHz	**16.384 MHz**
84-Pin PLCC	100-Pin QFP
Z8700016VSC	Z8700016FSC

Z87010/Z87L10

16.384 MHz	**16.384 MHz**
44-Pin PLCC	44-Pin QFP
Z8701016VSC	Z8701010FSC

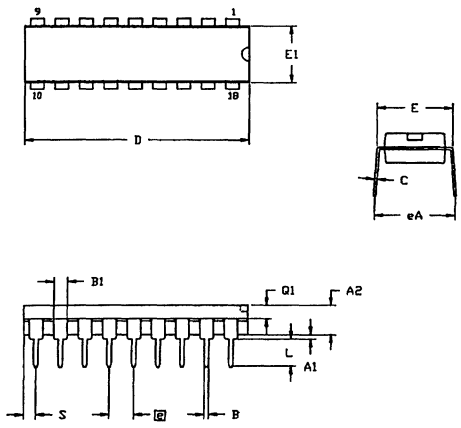
Z87100

12 MHz	**12 MHz**
18-Pin DIP	18-Pin SOIC
Z8710012PSC	Z8710012SSC

Z87200

20 MHz	**45 MHz**
100-Pin QFP	100-Pin QFP
Z8720020FSC	Z8720045FSC

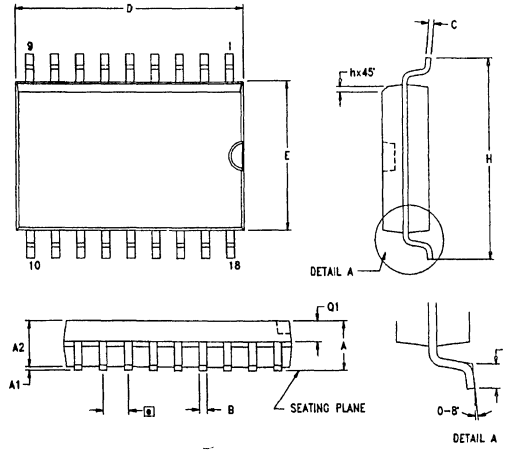
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

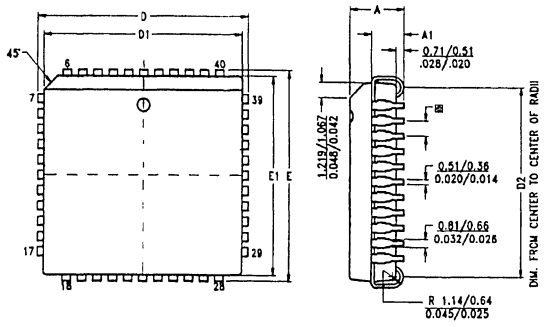
Figure 1. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

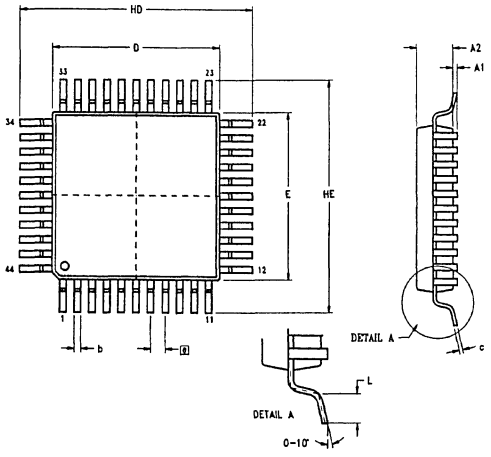
Figure 2. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 3. 44-Pin Lead PLCC Package Diagram

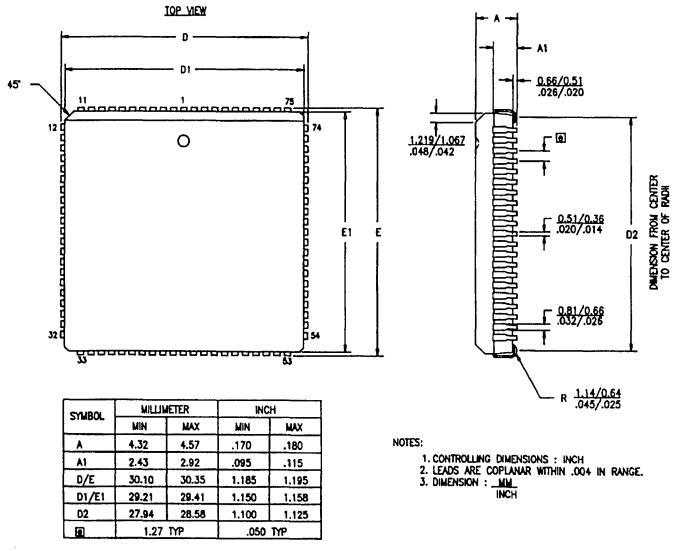


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 4. 44-Pin QFP Package Diagram

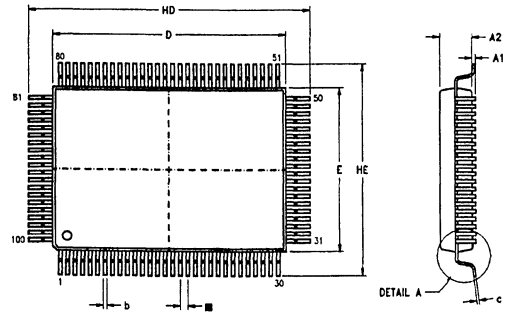
PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	30.10	30.35	1.185	1.195
D1/E1	29.21	29.41	1.150	1.158
D2	27.94	28.58	1.100	1.125
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

Figure 5. 84-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

Figure 6. 100-Pin PQFP Package Diagram

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7 Wireless Family Support Products
8
9

Z8700000TSC

EMULATION MODULE

FEATURES

The Z870000TSC Emulation Module allows the user to plug programmed EPROMs into the board to verify operation of code before submitting for mask ROM.

The Z870000TSC Emulation Module provides emulation for 16.384 MHz operation for the Z87000.

Supported Devices

Z8700016VSC

Specifications

Emulation Specification
Maximum Emulation Speed: 16.384 MHz

Power Requirements
+5 Vdc @ 100 mA from Target Board

Target Clock or Crystal Frequency
16.384 MHz

Operating Voltage Range
4.0V to 5.5V

Operating Temperature
-40°C to +85°C

Operating Humidity
10-90% RH (Non-Condensing)

KIT CONTENTS

Z8700000TSC Emulation Module

CMOS Z87001 Cordless Phone Transceiver/Controller ICE Chip
Two 28-Pin 16K x 8 EPROM Socket
84-Pin PLCC Socket Plug

Documentation

Z8700000TSC Emulation Board User Guide

Ordering Information

Part Number: Z8700000TSC

7

Z8700000ZEM

IN-CIRCUIT EMULATOR

HARDWARE FEATURES

- Supported Products

Packages	Emulation	Programming
84-pin PLCC 100-pin QFP	Z87000	N/A

- Real-Time Emulation
- DSP GUI Emulator Software
- Windows-Based User Interface
- RS-232 Connector
- ICE Pod Connector for Emulation

GENERAL DESCRIPTION

The Z8700000EM is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for the above listed DSP microcontroller devices.

Zilog's in-circuit emulators are interactive, Window-oriented development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z8700000ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C ±10°C
Supply Voltage +5.0 VDC , ±5%
Maximum Emulation Speed: 16.384 MHz

Power Requirements

+5.0 VDC @ 0.5A Minimum

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface

RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB or RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z87000 Emulator

- Emulation Base Board includes:
  CMOS Z86C9320VSC
  8K x 8 EPROM (Programmed with Debug Monitor)
  32K x 8 Static RAM
  RS-232C Interface
  Reset Switch
- Z87000 Emulation Daughterboard
  16 MHz CMOS Z86C1216GSE ICE Chip
  64K x 4 Static RAM
  Two 32K x 4 Static RAM for Breakpoints
  Two 80-pin Target Connectors
  Mini-Coax with SMA Connectors

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
84-Pin PLCC Emulation Pod Cable
Mini-Coax with SMA Connectors

Host Software

DSP GUI Emulator Software

Note: Cross-Assembler and C Compiler are sold separately from Zilog or Production Languages, Tel: (817) 599-8363

Documentation

Emulator User's Manual
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.
2. The GUI does not recognize the PUSH and POP instructions when entered from In-Line Assembler. Use "LD STACK, xxx' for PUSH and "LD xxx, STACK" for POP instead.
3. The initial blue Zilog screen will be distored by other active windows. This only affects the appearance, not functionality, of the GUI.
4. Switching ICEBOXes without quitting the GUI is not supported.
5. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).
6. Download File Name is not shown except at Time of Download. The emulator only shows the name of the file during the download process. To check the name of the file currently downloaded, select "File" and then "Download DSP Memory." The File Name box in the "Down to DSP Code Memory" window will reflect the file that is selected for download. Unlike other emulators, the Debug window or Memory window does not show the name of the currently downloaded file.
7. The ICEBOX breakpoint hardware does not distinguish between instruciton and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

Example:

```
000C    SRP   #%0
000E    LD    R4, #%0016
0010    LD    R5, @R4
0012    NOP
0013    JP    %000C
0016    NOP
```

Setting the breakpoint at %0016 and click GO.

Result: The code will break and stop at %0012.

Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

PRECAUTIONS

1. Breakpoint Overshoot. The Disassembly window shows the processor halting at one or two instructions past the instruciton where the breakpoint was set.
2. Executing GUI. The GUI will occasionally continue to indicate executiong after it has been told to halt. Pushing the GO button will then result in executing. (Executing showing at the top of the screen).
3. The emulator cannot be operated while performing ESD/EMI testing on the target board.
4. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.
5. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.
6. The PLC Z89C00 Assembler RESET symbol in symbol table is fixed at 1000 when the assembly code contains "VECTOR RESET=" statement.

Z8700001ZCO
DEVELOPMENT KIT

FEATURES

- Supported Devices

Packages	Evaluation	Programming/ Emulation
100-Pin QFP	Z8700016FSC	N/A
84-Pin PLCC	Z8700016VSC	N/A
44-Pin QFP	Z8701016FSC	N/S
44-Pin PLCC	Z870106VSC	N/A

- Two Jumper Configurable Circuit Boards
- Supports Real-Time Code Trace
- Direct Connect Logic Analyzer Probe Points
- Hosts Z87000 Emulation Tools
- Voice Processing Capability
- Z87010 ADPCM Encoder/Decoder

GENERAL DESCRIPTION

Zilog's Z87000 Development Kit is a member of the support tool family providing demonstrations and evaluation of spread-spectrum cordless phone transceiver/controllers.

Z8700001ZCO kit includes two identical circuit boards and the hardware required to operate as a cordless telephone handset or base. Each circuit board contains a Z87000 spread-spectrum transceiver/controller and a Z87010 ADPCM encoder/decoder.

The kit enables jumper connection of the cordless phone handset and base at intermediate frequency (IF). This configuration demonstrates the voice processing quality of the Z87000 system.

The kit circuit boards are socketed for easy replacement of the Z87000 spread-spectrum transceiver/controller with either the Zilog Z8700000ZEM ICEBOX™ in-circuit emulator or Z870000TSC emulation module as a platform for software development.

SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5 VDC
Evaluation Speed: 16.384 MHz

Power Requirements

+5 VDC @ 1.5A

Dimensions

Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Telephone Interface

RJ11 Plug

KIT CONTENTS

Two Z87000 Evaluation Boards

Evaluation Base Board:
CMOS Z8700016VSC

CMOS Z870106VSC or Z89371116VSC
(Programmable OTP for the Z87010)

Telephone Hybrid

Telephone Keypad

RJ14 Telephone Handset Interface

RJ11 Telephone Line Interface

Two (32K X 8) Static RAM

(32K x 4) Static RAM for Breakpoints

2 x 80-pin Target Connectors

Two 100-Pin HP-16500A Logic Analyzer
Interface Connector

Cables

Two IF Interface Cables
Two Telephone Handsets with Cords
One Telephone Line with RJ11 Plugs

Documentation

Zilog Z87000 Z-Phone Development User's Manual
Registration Card
Product Information Sheet

PRECAUTIONS

1. The Z87000 R2017, when configured as the handset unit, will sometimes reset itself due to stack overflow. A possible workaround is to reset the base.

2. Pulse dialing does not work due to incorrect software polarity control.

Note: The problems listed in Precautions Number 1 and Number 2 do not occur when using the Z87000 Emulation Module (Proto-Pack, Zilog part number: Z870000TSC), or the Z87000 ICEBOX Emulator (Zilog part number: Z870000ZEM), instead of the Z87000 R2017 device. Contact The Wireless Group at Zilog for the latest software updates to use with the Proto-Pack and emulator. (Zilog address information follows.)

DOCUMENTATION ERRATA

Refer to the Z87000 ZPhone™ Development Kit User's Manual, Chapter 1, "Introduction." The Z8937116VSC is shipped instead of the Z87010. The Z8937116VSC is the one-time programmable device versions of the Z87010 that is programmed with the latest Z87010 ROM code.

Z8710000ZEM

IN-CIRCUIT EMULATOR

FEATURES

- Supported Devices:

Package	Evaluation	Programming/Emulation	Notes
18-Pin DIP	Z87100	N/A	
18-Pin SOIC	Z87100*	N/A*	[1]*

Notes:
1. With optional, separately purchased adapter available from:

Emulation Technology, Inc.
Telephone (408) 982-0660
FAX (408) 982-0664
Part # AS-DIP. 3-020-S003-1

- Real-Time Emulation
- ICEBOX Emulator Provides In-Circuit Program Debug Emulation
- Z8 Graphical User Interface (GUI) Emulator Software
- Windows-Based User Interface
- RS-232C Connector
- ICE Pod Connector for Emulation
- HP-16500 Logic Analysis System Interface Connector

GENERAL DESCRIPTION

The Z87100 Emulator (Z8710000ZEM) is a member of Zilog's ICEBOX product family of in-circuit emulators providing support for those Z8 microcontroller devices listed in the above section.

Zilog's in-circuit emulators are interactive, Windows-based development tools, providing a real-time environment for emulation and debugging.

The emulator provides essential timing and I/O circuitry to simplify user emulation of the prototype hardware and software product.

Data entering and program debugging are performed by the monitor ROM and the host package, which communicates through RS-232C serial interface. The user program can be downloaded directly from the host computer through the RS-232C connector. User code may be executed through debugging commands in the monitor.

The Z8710000ZEM emulator can be connected to a serial port (COM1, COM2, COM3, and COM4) of the host computer and uses Graphical User Interface (GUI) software.

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SPECIFICATIONS

Operating Conditions

Operating Temperature: 20°C, ±10°C
Supply Voltage: +5.0 VDC, ± 5%
Minimum Emulation Speed: 200 kHz
Maximum Emulation Speed: 12 MHz

Power Requirements
+5.0 VDC @ 1.0A

Dimensions
Width: 6.25 in. (15.8 cm)
Length: 9.5 in. (24.1 cm)
Height: 2.5 in. (6.35 cm)

Serial Interface
RS-232C @ 9600, 19200 (default), 28800, or 57600 Baud

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine
33 MHz
4 MB RAM
VGA Video Adapter
Hard Disk Drive (1 MB free space)
3.5-inch, High-Density (HD) Floppy Disk Drive
RS-232C COM port
Mouse or Pointing Device
Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance:

486- or Pentium-based machine
66 MHz (or faster)
8 MB of RAM (or more)
SVGA Video Adapter
Color Monitor
Printer

KIT CONTENTS

Z87100 Emulator

- Emulation Base Board includes:
  CMOS
  8K x 8 EPROM (Programmed with Debug Monitor)
  32K x 8 Static RAM
  Three 64K x 4 Static RAM
  RS-232C Interface
  Reset Switch
- Z87100 Emulation Daughterboard
  20 MHz CMOS Z86C5020GSE ICE Chip
  28-Pin DIP Zero Insertion Force (ZIF)
  PN Data EPROM Socket
  40-Pin Target Connector
  100-Pin HP-16500 Logic Analyzer Interface Connector
  Reset Switch

Cables/Pods

Power Cable with Banana Plugs
DB25 RS-232C Cable
18-Pin DIP Target Pod

Host Software

Z8® GUI Emulator Software
ZASM Cross-Assembler/MOBJ Object File Utilties

Documentation

Z87100 ICEBOX User's Manual
Z8 Cross-Assembler User's Guide
Universal Object File Utilities (MOBJ) User's Guide
Registration Card
Product Information

LIMITATIONS

1. Changing drives in file download and load symbol dialog boxes is not anticipated by the GUI. Typing in the filename in a directory other than shown in "Path:" will result in "File not found". Changing the drive using the mouse is the workaround.

2. The initial blue Zilog screen will be distorted by other active windows. This only affects the appearance, not functionality, of the GUI.

3. Switching ICEBOXs without quitting the GUI is not supported.

4. The maximum symbols that can be loaded is 32768, provided that there is enough system resource (memory).

5. The ICEBOX breakpoint hardware does not distinguish between instruction and data fetches. When a breakpoint in the GUI is set, the breakpoint hardware triggers when the addresses match for either code or data fetches.

Example:

```
000C    SRP     #%0
000E    LD      R4 #%0016
0010    LD      R5, @R4
0012    NOP
0013    JP      %000C
0016    NOP
```

Setting the breakpoint at %0016 and click GO.

Result: The code will break and stop at %0012.

Note: This will not happen when Animate Mode is on because the GUI is not using the hardware breakpoints when in Animate Mode.

6. If the emulator is running a user code at full speed and the port window is opened: Switching to another application or minimizing the GUI (then restoring) will result in the following ICEBOX Communications Error message: "Emulator rejected command: target program is executing." This message may need to be cleared several times (as many as seven) before the GUI returns to normal operation.

Workaround: Always close the port window before leaving the GUI.

7. Clicking on the HALT button does not always halt the ICEBOX execution. If the application goes into Stop Mode or Halt Mode, the only way to halt the emulator execution is by doing a Stop-Mode or Halt-Mode Recovery (as defined by the user program). You may also reset the application using the RESET button; however, this will reset the whole ICEBOX.

8. Single-stepping into the Halt instruction will cause an ICEBOX "Fatal Error" message to be displayed on the screen. The Ice Chip must be reset, either by /Reset Pin on the target board or by resetting the whole ICEBOX by pressing the RESET button at back of emulator.

9. Do not put breakpoint at address after Stop instruction. This will cause program counter to continue at that location after a Stop-Mode Recovery.

10. The Emulator does not operate at 32 kHz frequency. The low-power 32 kHz oscillator cannot be selected in Emulation Mode; however, it can be selected in Stand-Alone Mode.

11. The ICEBOX does not support any OTP programming.

12. RC oscillator emulation is not supported.

13. The emulator uses the C50 ICE Chip; therefore, port 1 cannot be configured to Low EMI mode. (Bit 4 in PCON registers must be set to logic "1")

Note: This condition is not present with the actual emulated device.

PRECAUTION LIST

All Devices

1. The GUI comes up as "C50" in the window caption and uses Z8EM_C50.BSC as the firmware.

2. GUI software versions prior to 3.00 are incompatible with hardware containing BOOTROM 3.00. The GUI software may still boot, but will fail at some later point of the session.

3. When device serialization is enabled in the OTP dialog, the GUI copies the current serial number to code memory immediately before performing a VERIFY operation. If this behavior is undesirable, then device serialization must be disabled prior to invoking the VERIFY operation.

4. The status color bar in OTP dialog box will be cleared in the area where a new window opens on top of it.

5. For 386 PCs, set the baud rate to 19.2K or less because 'Windows' communication driver does not guarantee "reliable" operation at more than 9600 baud. Selection a high baud rate on some slower 386 machines may crash the Windows environment.

6. Do not press hardware reset when the ICEBOX is in OTP programming. If reset is pressed while the GUI is doing OTP programming, close the OTP dialog window and reopen it to reload the information back to the hardware.

Note: Although the Command Status shows "Processing" after the GUI reestablishes the communication link when Retry was selected, the ICEBOX is actually sitting idle.

7. All Z8® control registers are write only unless stated otherwise.

8. Power Supply ramp-up/rise time must be such that when minimum Power-On Reset (POR) time (T_{POR}) expires, then the V_{CC} must be in the supported specified operating range of the device.

9. Check the T_{POR} and T_{WDT} specifications of the device that you wish to emulate. The actual specification may differ from the ICE chip specifications.

10. The PCON Register reserved bits for the Z87100 emulator must be set to "1".

11. The general-purpose registers after POR or at initial emulator use will be different than the actual device. The emulator self test will always leave the same values in the general-purpose registers, while the real device will have a random/undefined value in the general-purpose registers.

12. The register %F8 (P01M register) bits D4 and D3 must be set to state "0" and bit D2 must be set to state "1".

13. Watch-Dog Timer (WDT) running in Stop Mode is not supported.

14. For emulation of the Z87100, select "Z86C06/E06" from the Z8 Microcontroller List Box in the Configuration Dialog Box.

15. The Emulator cannot be operated while performing ESD/EMI testing on the target board.

Z8720000ZCO
EVALUATION KIT

HARDWARE FEATURES

- Supported Devices

Packages	Emulation	Programming
100-pin QFP	Z8720045FSC	N/A
100-pin QFP	Z8018216FSC	N/A

- Fully Programmable Transmitter and Receiver
- Programmable Intermediate Frequency
- Intermediate Frequency and Baseband Inputs/Outputs
- 16550 MIMIC Interface
- IBM PC Plug-In I/O
- Configurable as a Stand-Alone System
- ESCC™ Ports and S180 Microprocessor Core

GENERAL DESCRIPTION

Zilog's Z87200 Evaluation Board is a member of the support tool family providing a development platform to implement data communication applications based onthe Z87200 Spread-Spectrum Burst Processor and the Z80182 Intelligent Modem Controller.

The Z8720000ZCO kit includes an evaluation board operating at baseband, a Z87200 spread-spectrum processor with programmable intermediate frequency, firmware, and host PC software.

Baseband control and interface functions are supported by the Z80182 Enhanced Serial Communications Controller (ESCC™) ports and S180 microprocessor core. The Z87200 spread-spectrum transmitter and receiver are fully programmable and may be monitored through a variety of test points. The board also provides inputs and outputs at both Intermediate Frequency and baseband to allow connection to a user provided RF section or the Zilog loopback board.

SPECIFICATIONS

Power Requirements

+5V, 12V DC

Dimensions (PC AT Board)

Width: 4.3 in
Length: 9.7 in

Serial Interface

26-Pin Header for RS-232-C
(Data Rates up to 115.2 Kbps)
DB25 RS-422 (EIA-530)
(Data Rates up to 4 Mbps)

KIT CONTENTS

Z87200 Evaluation Board
CMOS Z87200 Spread-Spectrum Transceiver
CMOS Z80182 Modem Controller
45.056 MHz Crystal (Z87200)

16.384 MHz Crystal (Z80182)
Comprehensive Test Points
128 KB RAM
64 KB ROM
Reset and NMI Buttons

Documentation

Z87200 Preliminary Product Specification
Z87200 Technical Manual
Z80182 Product Specification
Z80180 Technical Manual
ESCC Technical Manual
Evaluation Board User's Manual
Including Schematics

Z893XXW1ZSW

Z893XX CROSS SOFTWARE FOR OUTSIDE USA AND CANADA (INTERNATIONAL)

FEATURES

- Supported Devices

Z87000	Z89313	Z89331
Z87010	Z89317	Z89332
Z89300	Z89319	Z89371
Z89301	Z89321	Z89373
Z89302	Z89322	Z89391
Z89303	Z89323	Z89393
Z89309	Z89328	Z89C00

- Windows-Based User Interface
- Integrated Development Environment (IDE)
- Macro Assembler with Linker and Librarian
- Source-Level Debugger (SLD)
- Optimizing ANSI C Compiler
- Supported Zilog Emulators*

Z8700000ZEM	Z8932300ZEM	Z89C0000ZEM
Z8930901ZEM	Z8937100ZEM	
Z8931900ZEM	Z8939100ZCO	

* Not supplied; must be purchased separately.

- Instruction Simulator
- Program Visualizer
- Automated Project Maintenance (Make)
- On-line Hypertext HELP System
- On-line Tutorials with Sample Programs
- Drivers for Zilog ICEBOX™ Emulators
- Security Key/Dongle

GENERAL DESCRIPTION

The Z893XX Cross Software (Z893XXW1ZSW) product includes an assembler, linker, librarian, debugger, simulator, emulator driver, and ANSI C compiler for development of source code programs for Zilog DSP microprocessor devices based on the Zilog Z89C00 CPU core. (This product version is for the international market outside the USA and Canada. It comes with a Security Key/Dongle, which must be used to operate the product.)

The product is re-marketed from Production Languages Corporation (PLC) and is limited to producing 8K words of object code. The Z893XX Cross Software can be upgraded via telephone from PLC for larger applications via approved payment, including credit card. Or the user may contact PLC directly to purchase the version appropriate for their budget and application.

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine

33 MHz

8 MB RAM

Hard Disk Drive (15 MB free space)

3.5-inch, High-Density (HD) Floppy Disk Drive

RS-232C COM port (for Zilog Emulators)

Mouse or Pointing Device

Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance and/or for larger application code sizes:

486- or Pentium-based machine

66 MHz (or faster)

16 MB of RAM (or more)

SVGA Video Adapter

Color Monitor

Printer

Windows 95

KIT CONTENTS

PLC Z3XXW-8K-I Software Package:

Host Software

COMPASS/3XX Software on 3.5-inch HD diskettes

Documentation

User's Manual

Registration Card

NOTES

1. To operate properly, this product must be installed on a hard disk drive. (The floppy diskettes are a transport-only medium.)

2. This product is re-marketed from Production Languages Corporation (PLC). The user is advised to consult PLC for specific product details of operation before purchasing to determine the applicability for their end product and development environment.

3. The specifications represented here are true to the best of Zilog's ability to verify at the time of publication and may change without notice by PLC, including support for devices and/or emulators.

4. All technical support is provided by PLC. Extended technical support must be purchased from PLC after initial 90-day free support period. Contact PLC for specific details of rates and coverages.

Address all correspondence to:

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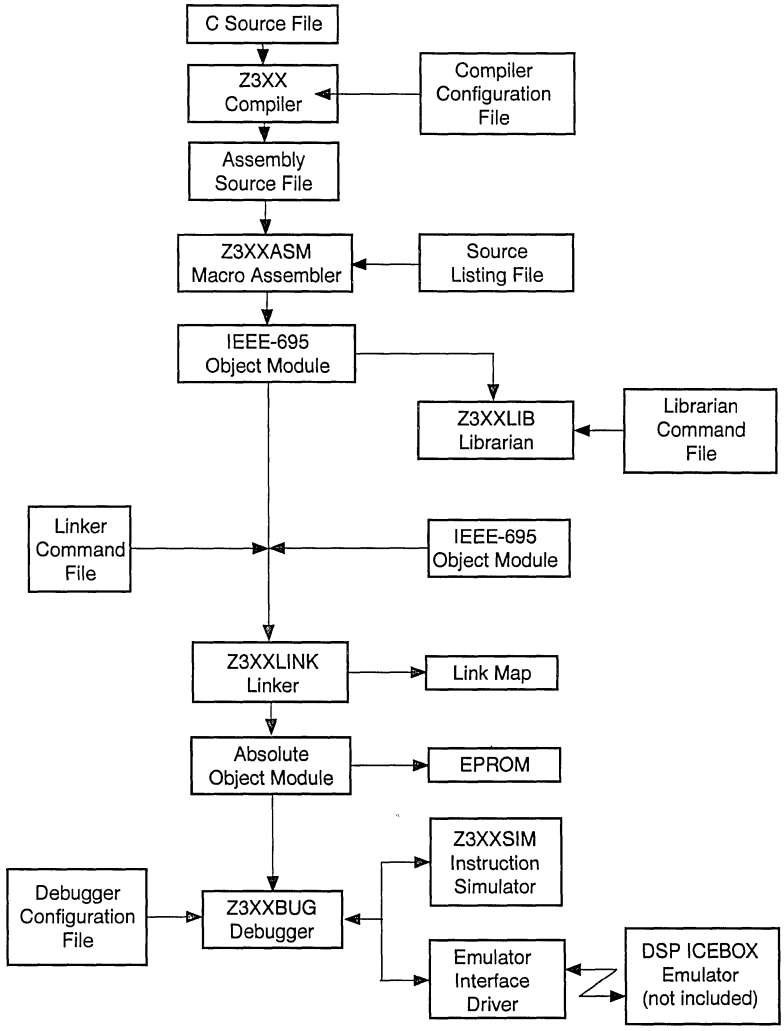

Figure 1. COMPASS/3XX Toolset by Production Languages Corporation

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Z893XXW0ZSW

Z893XX CROSS SOFTWARE FOR USA AND CANADA (DOMESTIC)

FEATURES

- Supported Devices

Z87000	Z89313	Z89331
Z87010	Z89317	Z89332
Z89300	Z89319	Z89371
Z89301	Z89321	Z89373
Z89302	Z89322	Z89391
Z89303	Z89323	Z89393
Z89309	Z89328	Z89C00

- Windows-Based User Interface
- Integrated Development Environment (IDE)
- Macro Assembler with Linker and Librarian
- Source-Level Debugger (SLD)
- Optimizing ANSI C Compiler
- Supported Zilog Emulators*

Z8700000ZEM	Z8932300ZEM	Z89C0000ZEM
Z8930901ZEM	Z8937100ZEM	
Z8931900ZEM	Z8939100ZCO	

* Not supplied; must be purchased separately.

- Instruction Simulator
- Program Visualizer
- Automated Project Maintenance (Make)
- On-line Hypertext HELP System
- On-line Tutorials with Sample Programs
- Drivers for Zilog ICEBOX™ Emulators

GENERAL DESCRIPTION

The Z893XX Cross Software (Z893XXW0ZSW) product includes an assembler, linker, librarian, debugger, simulator, emulator driver, and ANSI C compiler for development of source code programs for Zilog DSP microprocessor devices based on the Zilog Z89C00 CPU core. (This product version is for the domestic market of the USA and Canada only.)

The product is re-marketed from Production Languages Corporation (PLC) and is limited to producing 8K words of object code. The Z893XX Cross Software can be upgraded via telephone from PLC for larger applications via approved payment, including credit card. Or the user may contact PLC directly to purchase the version appropriate for their budget and application.

HOST COMPUTER

Minimum Requirements

IBM PC (or 100-percent compatible) 386-based machine

33 MHz

8 MB RAM

Hard Disk Drive (15 MB free space)

3.5-inch, High-Density (HD) Floppy Disk Drive

RS-232C COM port (for Zilog Emulators)

Mouse or Pointing Device

Microsoft Windows 3.1

The following changes to the Minimum Requirements are recommended for increased performance and/or for larger application code sizes:

486- or Pentium-based machine

66 MHz (or faster)

16 MB of RAM (or more)

SVGA Video Adapter

Color Monitor

Printer

Windows 95

KIT CONTENTS

PLC Z3XXW-8K Software Package:

Host Software

COMPASS/3XX Software on 3.5-inch HD diskettes

Documentation

User's Manual

Registration Card

NOTES

1. To operate properly, this product must be installed on a hard disk drive. (The floppy diskettes are a transport-only medium.)

2. This product is re-marketed from Production Languages Corporation (PLC). The user is advised to consult PLC for specific product details of operation before purchasing to determine the applicability for their end product and development environment.

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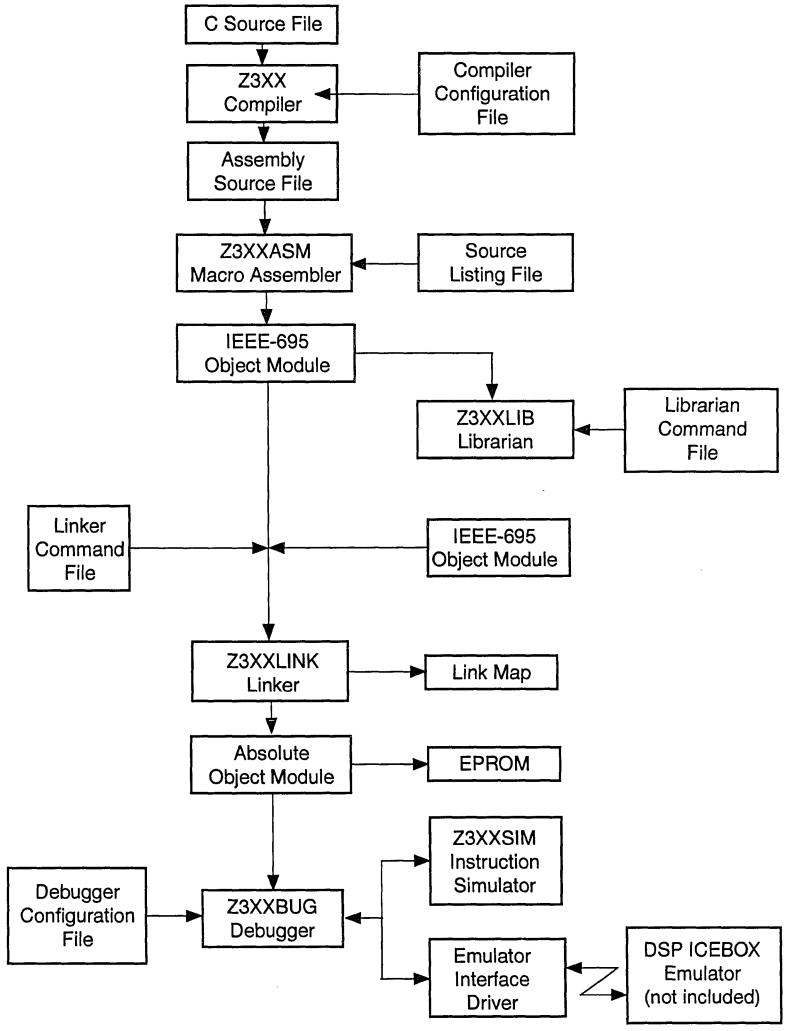

Figure 1. COMPASS/3XX Toolset by Production Languages Corporation

Z89C0000ZHP

ICEBOX™/H-P®

GENERAL DESCRIPTION

The ICEBOX/H-P Logic Analyzer Adapter Board provides the owner of a Hewlett-Packard Logic Analyzer (model #16500A) with real-time trace capabilities for the Zilog ICEBOX Emulator. The adapter board interfaces to the H-P Logic Analyzer probes and ICEBOX interface connector.

At the touch of a button, the captured code can be disassembled, providing a complete listing of program flow in native assembly language on the analyzer screen. This simple and low-cost setup transforms the logic analyzer into a powerful tool for software debugging.

SUPPORTED DEVICES

L7X, C67/121, C65/120, C00

SPECIFICATIONS

Power Requirements
Not Applicable

Dimensions
Width: 4.9 in (12.4 cm)
Length: 5.4 in. (13.7 cm)

KIT CONTENTS

ICEBOX/H-P Logic Analyzer Adapter Board

10 18-Pin DIP RC Network ICs
100-Pin ICEBOX Interface Connector
5 H-P 165XX Logic Analyzer Connectors

Cables
2', 100-Pin Cable

Software (IBM-PC Platform)
Z89C00 Disassembler Software
Z8® Disassembler Software**

Documentation
H-P Adapter Board User Guide

** future support.

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Z8722 Spread-Spectrum
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"Superior Cordless Telephony" 5

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Wireless Family
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Master Selection Guide	MS96COR3200
Superintegration Products Guide	PG96COR2101
Quality and Reliability Report	QR96COR2003
Zilog 1995 Annual Report	AN96COR0100
DSP	
Digital Signal Processor Databook	DB95DSP0105
Z89C00 DSP User's Manual & Algorithms	DC-8294-02
DSP Family Brochure	BR95DSP0100
DSP Mag Strip Flyer	FL95DSP0100
DSP Single-Chip Caller ID Flyer	FL95DSP0200
DSP Application Notes Handbook	DB96DSP0300
New DSP Family Flyer	FL96DSP0300
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Keyboard Databook	DC-8304-01
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PCMCIA Z86017/Z16017 Reference Manual	UM95HDD0101
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