XCELL

Issue 16
First Quarter 1995

THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®

The Programmable Logic Company℠

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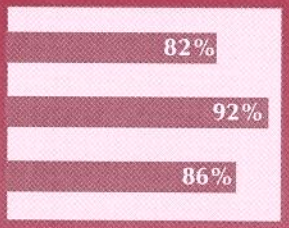
GENERAL FEATURES



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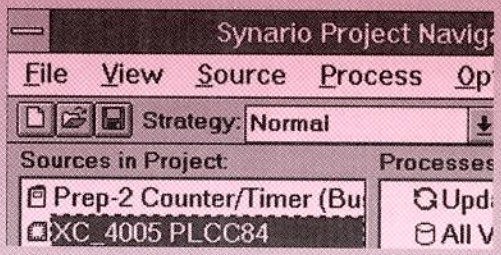

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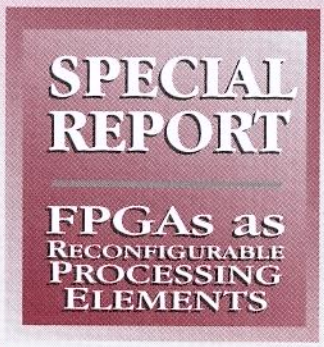

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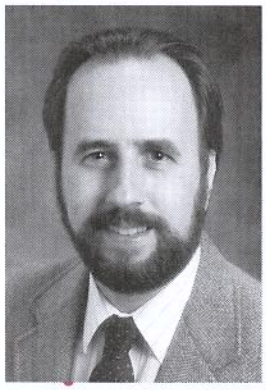
And the Survey Says ...

By BRADLY FAWCETT ◆ Editor

For the third year in a row, Xilinx employed an outside marketing consultant to conduct an extensive survey of our customers last autumn. This is just one of the many ways that we obtain feedback from Xilinx users. Our sincere thanks to the 522 engineers, managers and purchasing agents who took the time to complete and return the survey forms. We thought that you might be interested in a summary of the results.



First, the big picture. We received 331 responses from North America, 83 from Europe and 104 from Japan, a 16 percent response rate overall. 91 percent of the respondents have engineering responsibilities; the remainder work in purchasing. Within the engineering community, 76 percent are using PCs as a design platform and 45 percent are using workstations. (Clearly, some of you are using both.) The number of workstation users is growing, having increased from 36 percent in our 1993 survey.

In terms of overall satisfaction with Xilinx, 82 percent of the respondents were "very satisfied" or "satisfied" and 92 percent indicated that they were likely to recommend Xilinx to their peers. The overall satisfaction rating was higher in Europe and North America than in Japan. Those using the highest volumes of Xilinx components and those who have been using Xilinx products for the longest expressed the highest satisfaction levels.

The survey targeted five different areas: components, development systems, technical support, sales support and communications.

Component products were satisfactory to 86 percent of the respondents. (The consultants who conducted the survey claim that any satisfaction rating over 85 percent represents a company strength.) Not surprisingly, the areas of highest satisfaction were quality, functionality and power consumption, with somewhat lower satisfaction ratings for speed and density. One respondent summed it up nicely with a concise written comment, "Continue to improve speed and lower price."

For development systems, the survey results indicate that you want faster execution times and better third-party interfaces. The written comments also asked for more tutorials and better translation of our manuals into the Japanese language.

> *"We remain firmly committed to meeting our users' needs in every aspect of our business."*

Technical support (via our Field Applications Engineers and technical hotline) received 81 percent satisfaction. Sales support is a Xilinx strength, with 89 percent expressing satisfaction overall (93 percent among North American users). These numbers were consistent for both of our main sales channels: distributors and manufacturers' representatives. Our efforts to communicate with you satisfied 80 percent of respondents overall, with 91 percent in North America and Europe expressing satisfaction.

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Please direct all inquiries, comments and submissions to:

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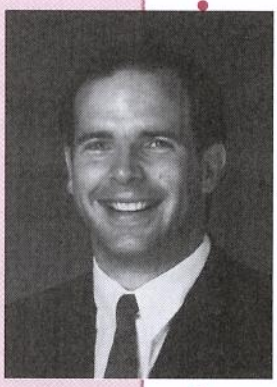
GUEST EDITORIAL

The Predictability Myth

by HANS SCHWARZ ◆ Marketing Director, Development Systems

Some high-density programmable logic vendors try to distinguish themselves from their competitors by claiming that their devices offer "predictable" performance; that is, *the performance of a design is predictable prior to its implementation in the target programmable logic device.* Altera Corp. has been particularly vocal about this *alleged* advantage of the FLEX 8000 architecture, but other vendors make similar claims.



Usually, this claim of "predictability" is based on one feature: the fixed interconnect delays typical of EPLD architectures (and, supposedly, extended to the FLEX 8000 FPGA architecture — yes, Altera has recently decided to call the FLEX devices "Complex PLDs" and not FPGAs, but let's save that topic for another day). Thus, the argument goes, since all the interconnect paths have fixed delays, the performance of the design is completely predictable.

Unfortunately, this view of "predictability" offers little practical use in all but the simplest of designs. While individual net delays are fixed in some of these architectures, net delays are not a measure of the speed of a design. The performance of an application is dependent on the speed of entire paths through the design, not just individual nets. A circuit path through a design typically traverses multiple nets and logic blocks.

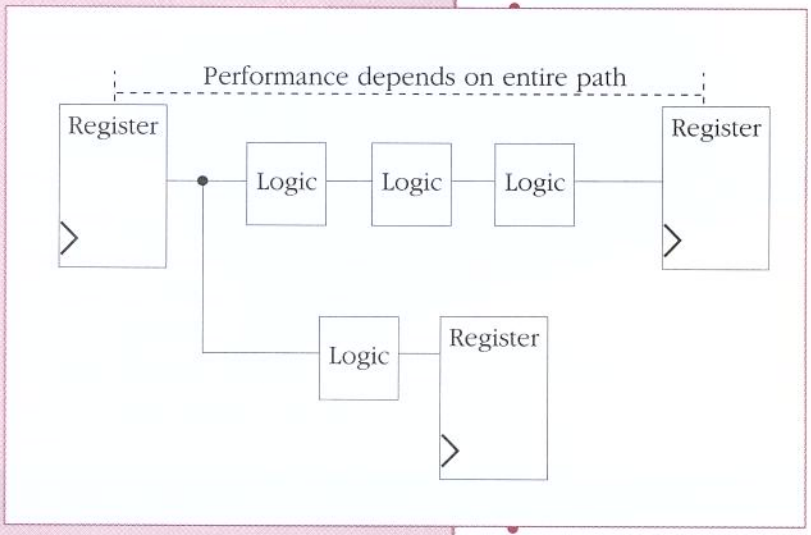


Figure 1: Examples of circuit paths traversing multiple logic blocks and interconnect segments.

For example, in the simple circuit of Figure 1, one of the paths involves two routing segments and an intervening combinatorial logic delay, while the other path includes four routing segments and three logic block delays. In synchronous designs there are four main types of paths: from a clocked register to a clocked register, from a package pin to a package pin with no intervening registers, from a package pin to a register, and from a register to a package pin.

Thus, interconnect delay "predictability" alone is not enough to calculate path delays unless you know which and how many of the different interconnect segments will be used and the number of intervening logic block delays. For a small design in a PAL-like architecture, this may be possible. You must implement the design using your development system's place and route tools to determine path delays in a design of any reasonable complexity in a finer-grained architecture.

Continued on the next page

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GUEST EDITORIAL

Continued from page 3

A more effective approach is first to specify the performance you want to achieve along the critical paths of the design, and then to supply those as targets to timing-driven place and route algorithms. In other words, instead of guessing beforehand how the design will behave, specify how you want it to behave.

This is the approach that Xilinx took with the introduction of the XACT-Performance™ feature of the PPR (Partition, Place, and Route) program nearly two years ago — the industry's first timing-driven place and route tool for FPGAs. Since then, subsequent releases have refined this capability, including the simplification of the user syntax in XACT 5.0. Other FPGA vendors have followed our lead and introduced their own timing-driven implementation programs.

"The best solution is the one that allows you to specify the target performance instead of guessing beforehand."

For the Xilinx EPLD product line, other development system features allow you to specify and control performance, such as the ability to control mapping (including the selection of Fast Function Blocks or High-Density Function Blocks for given portions of the design) and to assign signals to special high-speed clocks and fast output enables. A static timing analyzer and report generator was recently added to the XEPLD toolset to assist in determining the performance of a given implementation.

Some measure of "predictability" is desirable in logic synthesis tools for high-level design. Ideally, the synthesis tools should be able to estimate the performance of a given logic implementation in order to make meaningful performance/area trade-offs during the synthesis process. This can best be accomplished as a statistical exercise using "wire load models" to estimate routing delays between levels of logic on the basis of interconnect loading. In the latest release of the XSI Xilinx-Synopsys interface, these estimates have been refined to the point where they are typically within 10 percent of the actual timing parameters of the implemented design.

So, view claims of performance "predictability" based on fixed interconnect delays with a jaundiced eye. The best solution is the one that allows you to specify the target performance instead of guessing beforehand. ◆

FINANCIAL REPORT

Strong Revenue Growth Continues

Xilinx sales revenues for the third fiscal quarter (ending Dec. 31, 1994) rose to a record $91.3 million, an increase of 14.8 percent from the previous quarter and 37 percent from the same quarter one year ago. For the first nine months of the fiscal year, revenues totaled $245.9 million, an increase of 36 percent over the comparable period last year.

Continued strength in the XC4000 and XC3100 families and significant growth in both the XC3000A/XC3100A and HardWire families contributed to the sales increase. XC4000 family sales rose 23 percent, and combined XC3100/XC3000A/XC3100A sales rose 29 percent compared to the preceding quarter. Sales of the HardWire family reached a record $6 million.

Geographically, revenues from North America remained strong, increasing 19 percent over the previous quarter. International revenues constituted 27 percent of total sales. ◆

XACT 5.0 Enables High-Performance FPGA Design

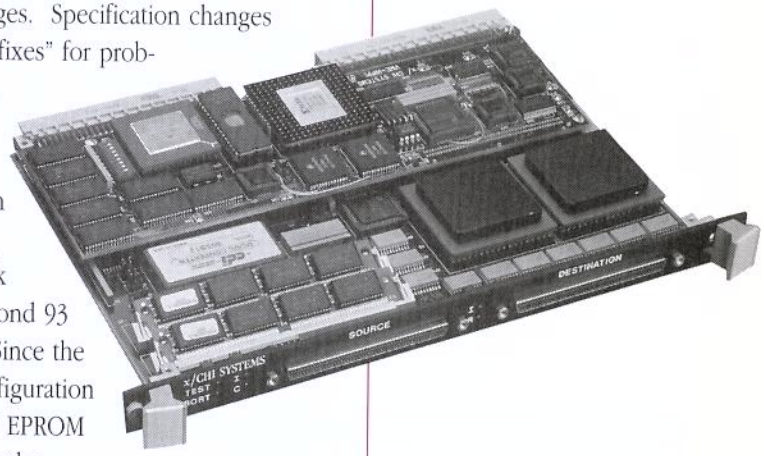
When engineers at Chi Systems (a division of Zitel Inc.) needed to push the limits of FPGA performance in the design of a high-speed interface card, they turned to the XC4010 FPGA and the XACT® 5.0 Development System.

Chi System's Enhanced 6U HiPPI Interface board implements high-speed point-to-point 32-bit data transfers between two standard busses: a High-Performance Parallel Interface (HiPPI) bus and a VME64 bus. Two 32-bit FIFO buffers provide data buffering between the two ports. The board is designed to deliver a sustained transfer rate of over 40 Mbytes per second with a pre-defined block transfer size.

Standard chip sets were selected for implementing each of the bus interfaces. The XC4010 FPGA and a small, high-speed EPLD hold all the control and interface logic linking these interface chip sets, the FIFO buffers, and an on-board Motorola 68EC030 microprocessor. Much like a processor uses a dedicated DMA device, registers in the FPGA that define the parameters of the data transaction (addresses, block sizes, etc.) are loaded by the microprocessor, and logic in the FPGA and EPLD directly controls the actual data transfer operation.

The XC4010 FPGA was designed using Viewlogic and Xilinx XACT 5.0 tools on both PC and workstation platforms. As noted by Larry Henson, Principal Hardware Engineer at Chi Systems, much of the success of the design depended on the advanced features of XACT 5.0. Knowing that speed requirements would be difficult to meet and design changes were inevitable, Chi Systems' engineers used location attributes to floorplan critical portions of the design and carefully applied performance specifications along critical paths using the XACT-Performance™ feature of PPR. "The extra time spent on floorplanning ended up saving us weeks in the debug and system integration phase of the project," stated Henson. "We were able to make design changes in the FPGA without critical paths being disrupted. The use of time spec. attributes and XDelay allowed for a quick review of the timing details of each design iteration. The highlight of the design was the ease at which the XC4010 could absorb design changes."

Initially, about 80 percent of the logic blocks in the XC4010 FPGA were being used, but the designers soon took advantage of the FPGA's ability to absorb design changes. Specification changes and "bug fixes" for problems with the interface chips soon expanded logic block usage beyond 93 percent. Since the FPGA configuration file shared EPROM space with the firmware, changes during beta qualification also were straightforward and accomplished with simple EPROM content changes. In some cases, bugs that would previously have required firmware changes without the flexibility of the FPGA solution were fixed through simple design changes in the FPGA.



"The XC4010 device was able to meet speed and capacity goals well beyond what we considered normal for a large FPGA device," concluded Henson. "Xilinx FPGAs will be considered for all future projects that have similar cost, performance and schedule requirements." ◆

CHI SYSTEMS

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order please contact your local Xilinx sales representative. ◆

For a complete list, please contact your sales representative.

TITLE	DESCRIPTION	PART NUMBER
Corporate		
Xilinx Yellow Pages Directory	*Open-systems directory listing EDA software, synthesis, tester and programmer vendors whose products support Xilinx*	#0010181-01
1995 Training Course Schedule	*Description of the Xilinx training programs and schedule of 1995 classes (worldwide)*	#0010134-04
FPGAs		
XC5000 Family Overview	Features & benefits	#0010235-01

TRAINING COURSE NEWS

New Class Emphasizes HDLs and Logic Synthesis

As FPGA capacity increases and designs become larger and more complex, many designers are considering the use of high-level hardware design languages (HDLs) and logic synthesis tools. The two most common HDLs are VHDL and Verilog-HDL. There are several available synthesis tools optimized for Xilinx device architectures, including FPGA Compiler™ from Synopsys.

Designing with HDLs and synthesis tools can be very different from using schematic entry. As a result, Xilinx now offers a training class that focuses on VHDL and Verilog design entry for Xilinx products. This class differs from the standard course in that HDLs are used instead of schematics in the examples and exercises, and special synthesis topics are discussed.

Initially, the class will be offered at Xilinx Headquarters in San Jose, California, and as a customer-site training option. Later in the year we expect to expand the number of class sites rapidly.

For more information and a class schedule, refer to the 1995 Programmable Logic Training Course brochure. ◆

Price Reductions For On-Site Classes

On-site training is a popular option that brings Xilinx training classes directly to your site. This option is often chosen for its convenience and potential savings (taking travel time and expenses into account). In addition, classes can be customized to suit your particular needs.

Previously, the price of these classes has been as high as $10,000, and required a minimum class size of 10 students. As part of a special promotion, the price has been slashed to $4,500; the minimum class size has been reduced to six students.

To enroll in a class, schedule an on-site class, or get more information about Xilinx classes, contact your local Xilinx sales representative or call the Xilinx training administrator at 408-879-5090. ◆

Xilinx to Host "Programmable Logic Breakthrough '95"

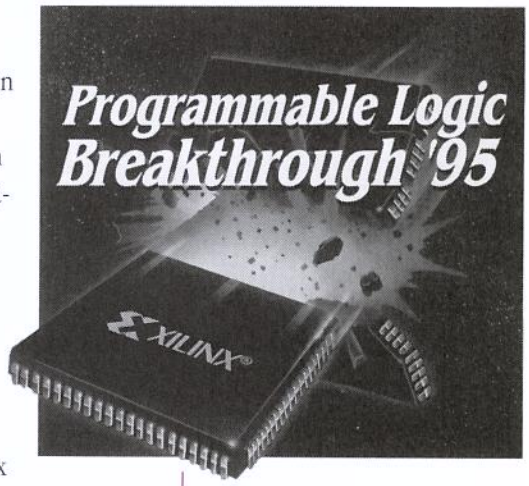
The 1995 Xilinx technical seminar and conference series will be coming to a location near you during the months of May and June. These events give you an opportunity to hear about the programmable logic software and technologies that will carry your designs through the '90s and beyond. The sessions will cover our new Windows-based XACT 6.0 software, three new revolutionary device families and a slew of new product enhancements.

Technical Conference Series

Held exclusively in six U.S. and European locations (Boston, Dallas, Santa Clara, Paris, London and Frankfurt), this full-day program offers four separate technology tracks plus a chance to visit more than 20 of the industry's leading EDA and synthesis tool vendors. Senior members of the Xilinx management and technical staff will be in attendance, as well as your local Xilinx sales representatives and distributors.

Technical Seminar Series

Offered in 65 cities throughout the world, these half-day sessions offer a view of the latest in design methodology alternatives plus an in-depth look at an exciting roster of new technologies from Xilinx. Presented by our applications engineers, these sessions address the architecture and software issues that affect your programmable logic designs.



Watch Your Mailbox for More Information

Invitations for the 1995 Xilinx seminar series will be mailed directly to all users who are currently on the *XCELL* mailing list. You will be able to register for a seminar in the desired city and country by way of telephone, E-mail, fax or reply card.

For additional information on the Xilinx seminar series, contact your local Xilinx sales office or distributor or see the Xilinx home page on the world Wide Web at http://www.xilinx.com. ♦

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. ***For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676).*** ♦

1995 Design SuperCon
Feb. 28 - Mar. 2, 1995
Santa Clara, California

PCI Spring '95 Design Workshop
Mar. 13 - 17, 1995
San Jose, California

PCI '95 - The PCI Bus Industry Conference
Mar. 29 - 31, 1995
Santa Clara, California

IEEE Workshop on FPGAs in Custom Computing Machines (FCCM)
Apr. 11 - 14, 1995
Napa, California

9th International Parallel Processing Symposium
April 24 - 28
Santa Barbara, California

Custom Integrated Circuits Conference (CICC)
May 1 - 4, 1995
Santa Clara, California

5th Annual Advanced PLD & FPGA Day
May 10
London (Heathrow), UK

Silicon Design Show
May 16 - 17
London, UK

DSPx
May 16 - 17
San Jose, California

3rd Canadian Workshop on Field-Programmable Devices (FPD '95)
May 29 - June 1
Montreal, Canada

Design Automation Conference (DAC)
June 12 - 16
San Francisco, California

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - FEBRUARY 1995

Company	Product Name	Version	Function	Design Kit	FPGA Support	EPLD Support	X-BLOX Support
Acugen	Sharpen	2.55	Automatic Test Generation	AALCA interface	✓		
	Sharpeye	2.55	Testability Analysis	AALCA interface	✓		
ALDEC	Susie-Xilinx	2.0	Schematic Entry/Simulation	Xilinx Design Kit	✓	✓	✓
	Active-Xilinx		Schematic Entry/Simulation	Xilinx Design Kit	✓	✓	✓
Altium	P-CAD	6.0	Schematic Entry	PC-Xilinx	2K,3K		
Aptix	System Explorer	2.0	System Emulation	Axess 2.0	✓		
	ASIC Explorer	2.0	ASIC Emulation	Axess 2.0	✓		
Cadence (Valid)	Concept	1.7-P4	Schematic Entry	Xilinx Front End	✓	✓	✓
	Rapidsim	4.2	Simulation	Xilinx Front End	✓	✓	
	Composer	4.3.3	Schematic Entry	Xilinx Front End	✓	✓	✓
	Verilog	2.1.2	Simulation	Xilinx Front End	✓	✓	
	FPGA Designer	3.3	Synthesis	FPGA Synthesis	✓		✓
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XDK-1	✓		
Compass	Asic Navigator		Schematic Entry	Xilinx Design Kit	✓		
	QSim		Simulation		✓		
	X-Syn		Synthesis		✓		✓
CV (Prime)	Design Entry	2.0	Schematic Entry	Xilinx Kit	✓		
Data I/O	ABEL	6.0	Synthesis	Xilinx Fitter	✓	✓	
	Synario	2.0	Schematic Entry, Synthesis and Simulation	Xilinx Fitter	✓	✓	✓
EPS	SIMETRI	2.0	Simulation	XNF2SIM	✓		
Exemplar Logic	CORE	2.2	Synthesis	CORE	✓	✓	✓
	CORE/V-system	2.2	Simulation	CORE/V-system	✓	✓	
Flynn Systems	FS-ATG	2.6	Automatic Test Generation	FS-High Density	✓		
IBM-EDA	Boole-Dozer		Synthesis		✓		
IKOS	2800/2900	5.16	Simulation	Xilinx Tool Kit	✓		
	Voyager	1.41	Simulation	Xilinx Tool Kit	✓		
IK Technology	G-DRAW	5.0	Schematic Entry	GDL2XNF	✓		
	G-LOG	4.03	Simulation	XNF2GDL	✓		
Intergraph	ACE Plus	4.7.5.5	Schematic Entry	Xilinx Design Kit	✓		✓
	AdvanSIM	7.0	Simulation	Xilinx Design Kit	✓		✓
	VeriBest Design System		Schematic Entry/Simulation	VeriBest Design Kit	✓		✓
ISDATA	LOG/iC2	4.1	Hierarchy editor, synthesis, simulation	Xilinx Mapper/ODC	✓	✓	✓
	LOG/iC Classic	4.1	Synthesis, simulation	ODC		✓	
IST (Alpine Design)	ASYL+	3.0	Synthesis	XNF interface	✓		
ITS	XNF2LAS	1a	Lasar model gen.	XNF2LAS	✓		
Logic Modeling (Synopsys Division)	Smart Model		Simulation Models	In Smart Model Library	✓	✓	
	LM1200		Hardware Modeler	Xilinx Logic Module	✓	✓	
Logical Devices	CUPL	4.5	Synthesis	Xilinx Fitter	✓	✓	
Mentor Graphics	QuickSim II	A.1-F (8.4)	Simulation	Call Xilinx	✓	✓	✓
	Design Architect	A.1-F (8.4)	Schematic Entry	Call Xilinx	✓	✓	✓
	Autologic	A.1-F (8.4)	Synthesis	Xilinx Synthesis Library	✓	✓	✓
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2K,3K		
OrCAD	SDT 386+	1.2	Schematic Entry	Call Xilinx	✓	✓	✓
	VST 386+	1.2	Simulation	Call Xilinx	✓	✓	✓
	PLD 386+	2.0	Synthesis	Call OrCAD	✓		
Protel	Advanced Schematic	2.2	Schematic Entry	Xilinx interface	✓	✓	
Quad Design	Motive	4.0	Timing Analysis	XNF2MTV	✓		
Simucad	Silos III	92.115	Simulation	Included	✓		
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓	✓	✓
Synopsys	FPGA Compiler	3.2	Synthesis	Call Xilinx	3K,4K	✓	✓
	Design Compiler	3.2	Synthesis	Call Xilinx	✓	✓	✓
	VSS	3.2	Simulation	Call Xilinx	✓	✓	✓
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓		
Tokyo Electron	ViewCAD	5.0502a	FLDL to XNF	XNFGEN	✓		
Topdown Design	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓		

Continued

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - FEBRUARY 1995 (con't)

Company	Product Name	Version	Function	Design Kit	FPGA Support	EPLD Support	X-BLOX Support
transEDA	TransPRO	1.2	Synthesis	Xilinx LIbrary	✓		
VEDA	Vulcan	4.5	Simulation	Xilinx Tool Kit	✓		
Viewlogic	ProCapture ProSim ProSynthesis	5.0 5.0 5.0	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx Call Xilinx	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓
Viewpoint	VitalBridge VeriLink	1.0 1.0	Vital VHDL Verilog lib. back-annotation	VHDL I/F kit Verilog I/F kit	✓ ✓		
Visual Software Solutions	StateCAD	2.4	State diagram	Xilinx fitter	✓		
Zycad	Paradigm ViP Paradigm XP Paradigm RP		VHDL Simulation Gate-level simulation Rapid prototyping		✓ ✓ ✓		

ALLIANCE PROGRAM - PLATFORMS & CONTACTS

Company	Contact Name	*PLATFORM* PC	Sun	RS6000	HP	Phone Number
Acugen	Peter de Bruyn Kops	✓				603-881-8821
Aldec	David Rinehart	✓				702-293-2271
Altium	Ray Turner	✓	✓			408-534-4148
Aptix Corporation	Wolfgang Hoeflich		✓		✓	408-428-6200
Cadence	Itzhak Shapira Jr.		✓	✓	✓	408-428-5739
Capilano Computing	Chris Dewhurst	✓		Macintosh		604-522-6200
Compass Design	Paul Billig		✓		✓	408-434-7950
Computervision (Prime)	Kevin O'Leary		✓			617-275-1800
Data I/O	Jay Gould	✓	✓			206-881-6444
Evaluations Per Second (EPS)	Michael Massa	✓	✓			617-487-9959
Exemplar Logic	Stan Ng	✓	✓		✓	510-849-0937
Flynn Systems	Mike Jingozian	✓				603-891-1111
IBM-EDA	John Orfitelli			✓		914-433-9073
IKOS	Brad Roberts		✓		✓	408-255-4567
IK Technology	Hiroyuki Kataoka	✓	✓		✓	
Innovative Synth. (IST)	Peter Robinson	✓	✓		✓	510-736-2302
Intergraph Electronics	Lauren Wenzl	✓	✓			303-581-2318
IS DATA	Ralph Remme	✓	✓		✓	+49-721-751087
Logic Modeling	Laura Horsey	✓	✓		✓	503-531-2271
Logical Devices	Joleen Rasmussen	✓				305-974-0967
Mentor Graphics	Steve Eichenlaub		✓	✓	✓	503-685-1559
Minelec		✓				+32-02-4603175
OrCAD	Jim Plymale	✓				503-671-9500
Protel Technology	Matthew Schwaiger	✓	✓			408-243-8143
Quad Design Tech.	Vern Potter		✓		✓	805-988-8250
Simucad	David Smith	✓	✓			510-487-9700
Sophia Systems	Terry Wilfley		✓		✓	408-943-9300
Synopsys	Lynn Fiance		✓	✓	✓	415-694-4102
Teradyne	Phil McAuliffe		✓			617-422-3753
VEDA	Francois Durif		✓		✓	+44-1329-82-2240
ViewLogic	Meredith Luckewicz	✓	✓	✓	✓	508-480-0881

COMPONENT AVAILABILITY CHART - FEBRUARY 1995

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4013D	XC4025	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XC5206	XC5210	XCZ236A	XCZ272A	XCZ318	XCZ336	XCZ354	XCZ372	XCZ3108	XCZ3144
44	PLASTIC LCC	PC44	◆	◆				◆				◆										◆																				◆		◆	◆	◆					
	PLASTIC QFP	PQ44																																											◆	◆						
	CERAMIC LCC	WC44																																											◆		◆	◆				
48	PLASTIC DIP	PD48	◆																																																		
64	PLASTIC VQFP	VQ64		◆	◆	◆						◆					◆					N																															
68	PLASTIC LCC	PC68	◆	◆	◆		◆	◆				◆	◆									◆	◆																							◆		◆	◆				
	CERAMIC LCC	WC68																																											◆		◆	◆				
	CERAMIC PGA	PG68	◆																																																		
84	PLASTIC LCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆			◆	◆	◆	◆			N	N	◆			◆	◆			
	CERAMIC LCC	WC84																																											◆				◆	◆			
	CERAMIC PGA	PG84		◆		◆	◆	◆				◆	◆	◆								◆	◆	◆																						◆								
100	CERAMIC QFP	CQ100				◆		◆																																													
	PLASTIC PQFP	PQ100				◆	◆	◆				◆	◆	◆								◆	◆	◆					◆	N									◆	◆										◆	◆			
	PLASTIC TQFP	TQ100		◆			◆	◆														◆	◆																														
	PLASTIC VQFP	VQ100				◆						◆	◆				◆	◆				◆	◆																	◆	◆													
	TOP BRZ. CQFP	CB100				◆		◆				◆	◆									◆	◆																	◆														
120	CERAMIC PGA	PG120																										◆									◆	◆	◆													
132	PLASTIC PGA	PP132						◆	◆			◆	◆									◆	◆																														
	CERAMIC PGA	PG132						◆	◆			◆	◆									◆	◆																														
144	PLASTIC TQFP	TQ144										◆	◆					◆	◆			◆	◆																			◆	◆										
	CERAMIC PGA	PG144																																																		◆
156	CERAMIC PGA	PG156																										◆	◆													◆											
160	PLASTIC PQFP	PQ160							◆	◆				◆	◆									◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆					◆	◆			N	N							◆	◆
164	CERAMIC QFP	CQ164								◆																																										
	TOP BRZ. CQFP	CB164								◆					◆										◆	◆		◆																									
175	PLASTIC PGA	PP175								◆					◆										◆	◆																											
	CERAMIC PGA	PG175								◆					◆										◆	◆																											
176	PLASTIC TQFP	TQ176													◆						◆				◆																												
184	CERAMIC PGA	PG184																																																		
191	CERAMIC PGA	PG191																														◆	◆								◆		N								
196	TOP BRZ. CQFP	CB196																															◆																		
208	PLASTIC PQFP	PQ208								◆					◆										◆	◆						◆	◆	◆	◆	◆	◆	◆				◆	◆		N	N							
	METAL MQFP	MQ208																														◆	◆	◆	◆															
223	CERAMIC PGA	PG223																								◆									◆		◆					◆			N							
225	PLASTIC BGA	BG225																																◆	◆	◆	◆													◆	◆
	WINDOWED BGA	WB225																																																		N
228	TOP BRZ. CQFP	CB228																																	◆																
240	PLASTIC PQFP	PQ240																																	◆	◆						◆		N							
	METAL MQFP	MQ240																																	◆		◆					◆									
299	CERAMIC PGA	PG299																																		◆															

◆ = Product currently shipping or planned N = New since last XCELL

XILINX RELEASED SOFTWARE STATUS - FEBRUARY 1995

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform				Last Update
					PC1 *6.2*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS									
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	5.02	5.10	5.10	5.10	5.10	01/95
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	5.02	5.10	5.10		5.10	01/95
Mentor[2]	A.1-F	I/F and Libraries	DS-344-xxx	5.02		5.10	1.10	5.10	01/95
OrCAD[2]		I/F and Libraries	DS-35-xxx	5.00	5.10				01/95
Synopsys[2]		I/F and Libraries	DS-401-xxx	3.01B		3.20	3.01B	3.20	01/95
Viewlogic[2]	ProCapture	I/F and Libraries	DS-390-xxx	5.02	5.10				01/95
Viewlogic[2]	ProSim	I/F and Libraries	DS-290-xxx	5.02	5.10				01/95
Viewlogic[2]		I/F and Libraries	DS-391-xxx	5.10	5.11	5.11		5.11	01/95
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	5.00	5.10	5.10			01/95
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	5.00	5.10	5.10		5.10	01/95
XILINX PACKAGES									
Mentor 8	Standard		DS-MN8-STD-xxx	5.02		5.10	1.10	5.10	01/95
OrCAD	Base		DS-OR-BAS-xxx	5.02	5.10				01/95
OrCAD	Standard		DS-OR-STD-xxx	5.02	5.10				01/95
Synopsys	Standard		DS-SY-STD-xxx	2.00		5.10	2.00	5.10	01/95
Viewlogic	Base		DS-VL-BAS-xxx	5.02	5.10				01/95
Viewlogic	Standard		DS-VL-STD-xxx	5.02	5.10	5.10		5.10	01/95
Viewlogic/S	Base		DS-VLS-BAS-xxx	5.02	5.10				01/95
Viewlogic/S	Standard		DS-VLS-STD-xxx	5.02	5.10				01/95
Viewlogic/S	Extended[3]		DS-VLS-EXT-xxx	5.02	5.10				01/95
3rd Party	Standard	FPGA/EPLD CORE	DS-3PA-STD-xxx		5.10	5.10		5.10	
XILINX HARDWARE									
Device Pgmr.	Prom. Pgmr.		HW-112 (XPP)	5.0	5.10	5.10			02/95
Device Pgmr.	EPLD/Prom. Pgmr.		HW-120 (Prolink)	3.14	5.00				06/94
THIRD PARTY PRODUCTION SOFTWARE VERSIONS									
Cadence	Composer	Schematic Entry	N/A	4.3		4.33		4.33	N/A
Cadence	Verilog	Simulation	N/A	2.1		2.1.2		2.1.2	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.7		1.7-P4		1.7-P4	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	4.10		4.2		4.2	N/A
Mentor	NETED	Schematic Entry	N/A				7.XX		N/A
Mentor	QuickSim	Simulation	N/A				7.XX		N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
Mentor	QuickSim II	Simulation	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
OrCAD	SDT 386+	Schematic Entry	N/A	1.10	1.20				N/A
OrCAD	VST 386+	Simulation	N/A	1.10	1.20				N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.01B		3.2A	3.2A	3.2A	N/A
Viewlogic	ProCapture	Schematic Entry	N/A		5.0	5.3		5.3	N/A
Viewlogic	ProSim	Simulation	N/A		5.0	5.3		5.3	N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		6.0	6.0			N/A
Data I/O	Synario	Entry and Simulation	N/A		2.0				N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD [3]Includes ViewSynthesis v2.3.1

Programmer Support for Xilinx XC7200 EPLDs — February 1995

VENDOR	MODEL	7236	7236A	7272	7272A	PC44	PC68	PC84	PG84	Comments
Advin Systems Pilot-U84	Pilot-U40 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E USA-84	USA-84 USA-84	USA-84 USA-84	USA-84 AM-XC84G		
B&C Microsystems, Inc.	Proteus	V3.6j	V3.6j	V3.7h	V3.7h	AMUPLC84	AMUPLC84	AMUPLC84		
BP Microsystems	BP-1200	v2.32	v2.32	v2.34	v2.34	SM44P	SM68P or SM84UP	SM84P or SM84UP	SM84UGA	
DATA I/O	UniSite 2900 3900 AutoSite	v4.3 V3.4* v2.1 V2.4*	v4.6* V3.4* V2.4* V2.4*	v4.5 v2.3 v2.3	v4.5** v2.3** v2.3**	USBASE-PLCC PPI-0243 3900-PLCC PLCC-44-1	USBASE-PLCC PPI-0246 3900-PLCC PLCC-68-1	USBASE-PLCC PPI-0208 3900-PLCC PLCC-84-1		*7236A=PPI-0243 **7272A=PPI-0246 (PC68) **7272A=PPI-0247 (PC84)
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.00	1	2	3		
Elan Digital Systems	6000 APS	K2.04	K2.04	K2.06	K2.06	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi84PGx	
Hi-Lo Systems Research	All-03A All-07	V3.01 V3.01	V3.01 V3.01	V3.00 V3.00	V3.00 V3.00	ADP-XC7236-PL44 PAC-PLCC44	ADP-XC7272-PL68 PAC-PLCC68	ADP-XC7272QPI-84		
ICE Technology Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44	AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68	AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84		
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	2.2 1.35 1.01	BBS BBS 1.01	2.2 1.35 1.01	BBS BBS 1.01	C C MODXP1-44L	C C MODXP1-68L	C C MODXP1-84L	MODXP1-84G	
MQP Electronics	SYSTEM 2000 PINMASTER 48	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 2Q95 P 2Q95	MP1	MP1	MP1		
Stag	Eclipse	P 1Q95	P 1Q95	P 1Q95	P 1Q95	EPU84P+	EPU84P+	EPU84P+		
SMS	Expert Optima Multisyte	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1		
System General	TURPRO-1 TURPRO-1 F\X	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	P44 P44	P68 P68	P84 P84		
Tribal Microsystems	TUP-300 TUP-400 FLEX-700	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	TUP-7236 TUP-7236 TUP-7236	TUP-7272 TUP-7272 PAC-PLCC68			PAC-PLCC 44
Xeltek	SUPERPRO SUPERPRO II	1.7C 1.7C	2.2 2.2	2.1 2.1	2.1 2.1	XXC7236-44PL/40D XXC7236-44PL/40D	XXC7272-68PL/68D XXC7272-68PL/68D	XXC7272-84PL/84D XXC7272-84PL/84D		
Xilinx	HW-120	V3.14	V3.14	V3.14	V3.14	HW-120-PC44	HW-120-PC68	HW-120-PC84	HW-120-PG84	

C = Currently Supported (no version number) P = Planned Release

Programmer Support for Xilinx XC7300 EPLDs — February 1995

VENDOR	MODEL	7318	7336	7354	7372	73108	73144	PC44	PC68	PC84	PQ44	PQ100	PG144	PQ160	PG184	BG225
Advin Systems	PILOT-U40	10.78N	10.78N	10.78N	10.78N	S 2/95	P 1Q95	USA-84	USA-84	USA-84		AM-XC100Q	AM-XC160Q			
	PILOT-U84	10.78B	10.78B	10.78B	10.78B	S 2/95	P 1Q95	USA-84	USA-84	USA-84						
B&C Microsystems, Inc.	Proteus	3.7k	3.7k	3.7k	S 2/95	3.7k	P 1Q95	C	C	C						
BP Microsystems	BP-1200	V3.01	V3.01	V3.01				SM44P	Special Adapter	Special Adapter		Special Adapter			Special Adapter	Special Adapter
DATA I/O	2900	V3.5	V3.5	V3.5				2900-PLCC			0529					
	3900	V2.5	V2.5	V2.5	BBS	BBS	P 1Q95	3900-PLCC	3900-PLCC	3900-PLCC	0529	0557		0558		
	UniSite	V4.7	V4.7	V4.7	BBS	BBS	P 1Q95	USBASE-PLCC	USBASE-PLCC	USBASE-PLCC	0529	0557		0558		
	AutoSite	V2.5	V2.5	V2.5	BBS	BBS	P 1Q95	PLCC-44-1	PLCC-68-1	PLCC-84-1	0529					
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.10	V1.10	P 1Q95	5	6 (13 for 7372)	7				9		
Elan Digital Systems	6000 APS	k2.13	k2.13	k2.13	k2.13	k2.13	P 1Q95	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi044QFx	PDi100QFx		PDi160QFx		PDi225BGx
Hi-Lo Systems Research	All-03A	V3.04	V3.04	V3.04	S 2/95	V3.00	P 1Q95									
	All-07	V3.02	V3.02	V3.02	V3.01	V3.00	P 1Q95	PAC-PLCC44	PAC-PLCC68							
ICE Technology Ltd.	Micromaster 1000/E	VX1.00	VX1.00	VX1.00	VX1.00	VX1.00	P 1Q95	AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44						
	Speedmaster 1000/E	VX1.00	VX1.00	VX1.00	VX1.00	VX1.00	P 1Q95	AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44						
	Micromaster LV	VX1.00	VX1.00	VX1.00	VX1.00	VX1.00	P 1Q95	AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44						
	Speedmaster LV	VX1.00	VX1.00	VX1.00	VX1.00	VX1.00	P 1Q95	AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44						
Logical Devices	ALLPRO-88	BBS	BBS	BBS	BBS	BBS	P 2Q95	C	C	C						
	ALLPRO-88XR	BBS	BBS	BBS	BBS	BBS	P 2Q95	C	C	C						
	XPRO-1	1.01	1.01	1.01	1.01	1.01	P 1Q95	MODXP1-5444L	MODXP1-5468L	MODXP1-108L			MODXP1-160Q	MODXP1-184G	MODXP1-108B	
MQP Electronics	SYSTEM 2000	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95	MP1	MP1	MP1						
	PINMASTER 48	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95									
SMS	EXPERT	C/94	C/94	C/94	S 2/95	P 1/95	P 1Q95	TOP1	TOP1	TOP1						
	OPTIMA	C/94	C/94	C/94	S 2/95	P 1/95	P 1Q95	TOP1	TOP1	TOP1						
Stag	ECLIPSE	V4.10.31	V4.10.31	V4.10.31	V4.10.31	V4.10.31	P 1Q95									
System General	TURPRO-1	V2.2	V2.2	V2.2	V2.2	V2.2	P 1Q95	C								
Tribal Microsystems	ALL-07	V3.02	V3.02	V3.02	V3.01	V3.00	P 1Q95	PAC-PLCC44	PAC-PLCC68							
Xeltek	SUPERPRO	2.1	2.1	2.1	S 2/95	S 2/95	P 1Q95	XXC7354-44PL/40D	XXC7354-68PL/40D							
	SUPERPRO II	2.1	2.1	2.1	S 2/95	S 2/95	P 1Q95	XXC7354-44PL/40D	XXC7354-68PL/40D							
Xilinx	HW-120	V5.00	V5.00	V5.00	V5.00	V5.00	P 1Q95	HW126-PC44	HW126-PC68	HW126-PC84			HW126-PQ160	HW126-PG184	HW126-BG225	

C = Currently Supported (no version number) P = Planned Release

Programmer Support for Xilinx XC1700 Serial Proms — February 1995

VENDOR	MODEL	1736A	1765	17128	17XXD	17XXL	17128D/ 17256D	DIP8	PC20	SO8/VO8
Advantech	PC-UPROG	V1.80	V1.80	V2.1	V2.0			X		
Advin Systems	PILOT-U24	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX-20	SO-8
	PILOT-U28	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U32	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U40	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-U84	10.53	10.53	10.76C	10.71	10.77	10.78B	X	PX20	SO-8
	PILOT-142	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-143	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-144	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
	PILOT-145	10.73	10.73	10.76C	10.73	10.77	10.78B	AM-1736	PX20	SO-8
AVAL	PECKER-50			C	C			X		
	PKW5100			C	C			X		
B&C Microsystems	Proteus-UP40	V3.4E	V3.4E	V3.4E	V3.5F	V3.7F	V3.7L	X	AMUPLC84	
BP Microsystems	CP-1128	C	C	V2.17*	V2.21C*	V2.34*	S 2/95	FH28A	FH28A + 3rd Party	FH28A + 3rd Party
	EP-1140	C	C	V2.17	V2.21C	V2.34	S 2/95	FH40A	FH40A + 3rd Party	FH40A + 3rd Party
	BP-1200	C	C	V2.17	V2.21C	V2.34	S 2/95	SM48D	SM20P or SM84UP	3rd Party
BYTEK	135H-FT/U	V42	V42	V51	V51	V51		TC-824D		
	MTK-1000	V42	V42	V51	V51	V51		TC-824D		
	MTK-2000	V42	V42	V51	V51	V51		TC-824D		
	MTK-4000	V42	V42	V51	V51	V51		TC-824D		
DATA I/O	UniSite/Site 40/48	V3.0	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	UniSite/ChipSite	V3.4	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	UniSite/PinSite	V3.4	V4.0	V4.1	V4.1	V4.6	BBS	X	USBASE-PLCC	USBASE-SOIC
	2900	V1.5	V2.1	V2.2	V2.2	V3.4	BBS	X	2900-PLCC	2900-SOIC
	3900	V1.0	V1.5	V1.6	V1.6	V2.4	BBS	0101	3900-PLCC	3900-SOIC
	AutoSite	V1.1	V1.5	V1.6	V1.6	V2.4	BBS	DIP-300-1	PLCC-20-2	
	UniPak 2B	V23	V24					351B120D		
	ChipLab	V1.1	V1.0	V1.0	V1.0	V1.1	V2.0	X		080801S300
Deus Ex Machina	XPGM			V1.00	V1.00	V1.00	V1.10	0	3rd Party	3rd Party
Elan Digital Systems	3000-145	C	C	C				A116		
	5000-145	C	C	C				A116		
	6000 APS	K2.01	K2.01	K2.02	K2.01	K2.10	K2.14	X	PD184UPLC	PD16USOI
Hi-Lo Systems Research	ALL-03A	V3.30	V3.30	V3.30	V3.30	V3.30	V3.47	X	CNV-PLCC-XC1736	CVN-SOP-NDIP16
	ALL-07	V3.30	V3.30	V3.30	V3.30	V3.30	V3.47	PAC-DIP40	PAC-PLCC44	
ICE Technology, Ltd.	Micromaster 1000/1000E	V1.1	V1.5	V3.00	V3.00		V3.00	X	AD-1736/65-20	
	Speedmaster 1000/1000E	V1.1	V1.5	V3.00	V3.00		V3.00	X	AD-1736/65-20	
	Micromaster LV			V3.00	V3.00	V3.00	V3.00	X		
	LV40 Portable			P 2Q95	P 2Q95	P 2Q95	P 2Q95	X		
	Speedmaster LV			V3.00	V3.00	V3.00	V3.00	X		
Link Computer Graphics	CLK-3100	C	C	V4.1	V4.13			X1736	PLCC-17XX	
Logical Devices	ALLPRO-40	V2.2	V2.2					X	OPTPLC-208	OPTSOI-080
	ALLPRO-88	V2.2	V2.2	V2.3	V2.3			X		OPTSOI-080
	ALLPRO-88XR	V1.1	V1.0	V2.3	V1.3			X		OPTSOI-080
	CHIPMASTER 3000	V2.0	V2.0	V2.1	V2.0	V2.3	V2.3	X	OPTPLC-208	OPTSOI-080
	CHIPMASTER 5000	V1.15	V1.15					X	OPTPLC-208	OPTSOI-080
	XPRO-1	V1.01	V1.01	V1.01	V1.01	V1.01		MODXLN-173	MODXLN-173	MODXLN-173
MQP Electronics	MODEL 200	C	C	6.45	6.45	6.45	6.46	AD13A-16		
	SYSTEM 2600			P 2Q95	P 2Q95	P 2Q95	P 2Q95	MP6		
	PINMASTER 48			P 2Q95	P 2Q95	P 2Q95	P 2Q95	X		
Micro Pross	ROM 5000 B	C	C	V1.70	V1.70			Mu 40		
	ROM 3000 U	C	C	V3.60	V3.60					
Needham's Electronics	EMP20	V1.5	V1.5	V1.5				X		
Red Square	IQ-180	C	C		V8.2					
	IQ-280	C	C		V8.2					
	Uniwriter 40	C	C		V8.2					
	Chipmaster 5000	C	C		V8.2					
Retnel Systems	ZAP-A-PAL	C	C		V3.8J			Module #36		
SMS	Expert	B/93	B/93	A/94	A/94	A1/94	Cx94	TOP40DIP	TOP1PLC or	
	Optima	B/93	B/93	A/94	A/94	A1/94	Cx94	"	TOP3PLC/TOP3PLC	
	Multisyte				A/94			"	"	
	Plus48	B/93	B/93	A/94	A/94	A1/94	Cx94			
	Sprint Plus	B/93	B/93	A/94						
STAG	Eclipse			V4.4	V2.2	V4.3	V4.10.31	EPU48D	EPU84P	
	Quasar	10.76C	10.76C	10.76C	10.76C	10.76C		X	AMPLCC20	
Sunrise	T-10	C	C		V3.13			X		
System General	TURPRO-1	C	C	V2.14	V2.01	V2.12	V2.20G	DIP-Adapter	P20-Adapter	
	Turpro-1 F\X	C	C	V2.14	V2.01	V2.12	V2.20G	DIP-Adapter	P20-Adapter	
	APRO	C	C	V2.14	V2.01	V2.12	S 2/95	X	X	
Tribal Microsystems	TUP-300	C	C	V3.31	V3.31	V3.37C	V3.47	X	CNV-PLCC-XC1736	
	TUP-400	C	C	V3.31	V3.31	V3.37C	V3.47	X	"	
	FLEX-700	C	C	V3.31	V3.31	V3.37C	V3.47	X	"	
Xeltek	SuperPRO	1.5B	1.5B	1.7C	1.7D	1.8	P 1Q95	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
	SuperPRO II	1.5B	1.5B	1.7C	1.7D	1.8	P 1Q95	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
Xilinx	HW112	C	C	V3.11	V3.31	V3.31	V5.0.0	X	HW-112-PC20	HW-112-SO8
	HW120	V5.00	V5.00	V5.00	V5.00	V5.00	P 1Q95	HW-120-PRM	HW-120-PRM	HW-120-PRM

C = Currently Supported, P = Planned, S = Scheduled Release Date, X=Package Supported, CD=Based on customer demand

Continued from page 2

While we do many things well — as evidenced by our financial results in addition to these surveys — there is room for improvement. We remain firmly committed to meeting our users' needs in every aspect of our business. We believe that we are making progress on all these fronts.

Through process technology and architectural improvements, component speeds and densities are constantly increasing. Simultaneously, costs have been decreasing 25-30 percent each year. We are introducing a faster speed grade for the XC3100A family this quarter *(see page 18);* look for a faster version of the XC4000 architecture later this year as well. XC4000 prices decreased again this quarter. And with the recent introduction of the XC5000 family, Xilinx has established a new standard for price/performance in an FPGA.

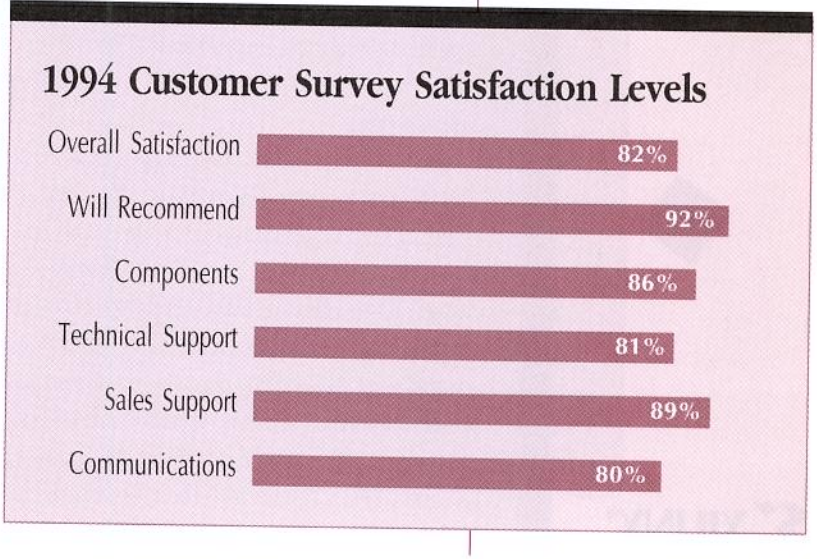
Last year's release of XACT 5.0 was a major stride forward in improving the capabilities of our development system software. Furthermore, we are well on our way in the development of XACT 6.0. The documentation was completely restructured with the 5.0 release to make information easier to find. Each successive release has been more rigorously tested than its predecessor, and has included a larger set of tutorials to help you get started using new features. Our third-party Alliance Program continues to expand, with the intention of facilitating smooth, error-free interfaces to third-party EDA tools.

The training program for our hotline Technical Support Engineers was revamped last year to become more comprehensive than ever. Our staff has expanded, also; we added 12 Field Application Engineers and nine Technical Support Engineers in 1994. We have increased the percentage of calls immediately handled by our Support Engineers from 15 percent two years ago to better than 50 percent today. We have plans to extend the hours during which Technical Support Engineers are available.

The new XDOCs and XFACTs systems are on-line *(see XCELL #15)*, providing you with access to technical support 24-hours-a-day via E-mail or fax. This newsletter was revised six quarters ago as a result of our user surveys, and is indicative of our commitment to improving our communications to our users.

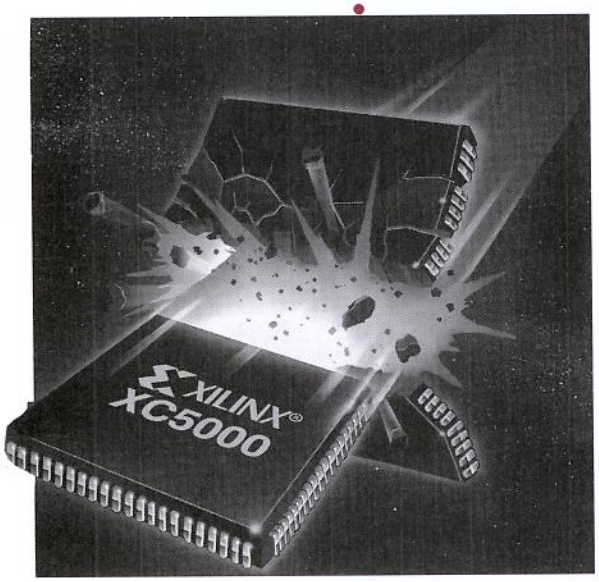
"The survey results indicate that Xilinx products are preceived as technically strong and highly competitive."

In summary, the survey results indicate that Xilinx products are perceived as technically strong and highly competitive. User satisfaction has remained stable, although expectations have increased. Thanks again for your honest feedback. Clearly, we have our work cut out for us, but we think that we are up to the challenge. Keep letting us know how we're doing. ◆



XC5000 Devices Now Available

The first two members of the high-density, low-cost XC5000 FPGA family are now available. The 6,000 gate XC5206 and 10,000 gate XC5210 deliver the lowest cost solutions for system designs ranging in performance up to 40 MHz. Priced at $26.00 and $39.00 (5K units, PC84 package), respectively, these new devices make the benefits of FPGAs affordable for high-volume designs.



The XC5000 is the first FPGA family designed and optimized for 0.6µ three-layer metal (TLM) processes. The combination of a new architecture and advanced process technology has allowed significant breakthroughs in silicon efficiency. With powerful new features like the VersaBlock™ logic module and the VersaRing™ I/O interface, the XC5000 is the optimal solution for high-density designs not requiring the high-performance and on-chip RAM features of the XC4000 family. *(See XCELL #15, page 14.)*

The XC5000 development tools are integrated into the powerful XACT design environment; designing with the XC5000 requires no relearning or additional costs. All in-warranty users will receive XC5000 software as part of our next major release, XACT 6.0 (Windows) and XACT 5.2 (DOS).

Please contact your local Xilinx sales representative for further information regarding software and device availability. ◆

XC4000 Prices Continue to Fall

Effective February, 1995, most XC4000 FPGA device prices have decreased again (as much as 18% in some cases). Prices have gone down more than 50 percent on some devices in the past year.

These price reductions reflect our continuing commitment to relay manufacturing cost improvements to our users. For example, the price of the 10,000-gate XC4010 has fallen to about one-tenth its 1992 release price.

Meanwhile, the number of products in this advanced, high-density FPGA family continues to grow. Recently, the XC4005 was released in a PQ100 package, enabling designers to squeeze 5,000 gates into limited board space. The XC4013D is now available, joining the XC4010D in offering a RAM-less, low-cost product option.

Software enhancements also continue, as evidenced by the release of the new Xilinx-Synopsys Interface and Libraries (XSI). Additional price reductions and the introduction of faster speed grades are planned, further enabling designers to incorporate the advanced XC4000 FPGA family into their system designs. ◆

XILINX®

New Standard Military Drawings (SMDs) for XC4000 Products

As part of our ongoing commitment to the high-reliability defense, aerospace and military markets, Xilinx actively participates in the Standard Military Drawing (SMD) program sponsored by the U.S. Government. By specifying SMDs, users obtain a product intended for high-reliability applications without having to generate their own device specifications. SMD devices are produced as standard products, and are available at lower cost and with shorter lead times than customer-specific versions.

There are now four XC4000 FPGA family members with high-reliability versions in the SMD program. With the recent release of SMDs for the XC4013 (the industry's highest density high-reliability programmable logic device) and the XC4003A, Xilinx now provides the high-reliability designer with advanced XC4000 FPGAs covering a 3,000 to 13,000 gate capacity range. All Xilinx XC4000 products include unique on-chip system features such as built-in JTAG test circuitry and on-chip RAM. Each of these devices is available in various speed grades, and in both through-hole and surface mount packages.

The table below lists the current and new SMD numbers for Xilinx XC4000 family FPGAs. ◆

XC4000 SMD Products

SMD Part Number	Xilinx Equivalent "B" Grade Part Number	Comments
5962-94712	**XC4003A**	
5962-9471201MXC	XC4003A-10PG120B	Pin Grid Array
5962-9471202MXC	XC4003A-6PG120B	Pin Grid Array
5962-9471201MYC	XC4003A-10CB100B	Quad Flat Pack with Base Mark
5962-9471202MYC	XC4003A-6CB100B	Quad Flat Pack with Base Mark
5962-9471201MZC	XC4003A-10CB100B	Quad Flat Pack with Lid Mark
5962-9471202MZC	XC4003A-6CB100B	Quad Flat Pack with Lid Mark
5962-92252	**XC4005**	
5962-9225201MXC	XC4005-10PG156B	Pin Grid Array
5962-9225202MXC	XC4005-6PG156B	Pin Grid Array
5962-9225201MYC	XC4005-10CB164B	Quad Flat Pack with Lid Mark
5962-9225202MYC	XC4005-6CB164B	Quad Flat Pack with Lid Mark
5962-9225201MZC	XC4005-10CB164B	Quad Flat Pack with Base Mark
5962-9225202MZC	XC4005-6CB164B	Quad Flat Pack with Base Mark
5962-92305	**XC4010**	
5962-9230501MXC	XC4010-10PG191B	Pin Grid Array
5962-9230502MXC	XC4010-6PG191B	Pin Grid Array
5962-9230501MYC	XC4010-10CB196B	Quad Flat Pack with Base Mark
5962-9230502MYC	XC4010-6CB196B	Quad Flat Pack with Base Mark
5962-9230501MZC	XC4010-10CB196B	Quad Flat Pack with Lid Mark
5962-9230502MZC	XC4010-6CB196B	Quad Flat Pack with Lid Mark
5962-94730	**XC4013**	
5962-9473001MXC	XC4013-10PG223B	Pin Grid Array
5962-9473002MXC	XC4013-6PG223B	Pin Grid Array
5962-9473001MYC	XC4013-10CB228B	Quad Flat Pack with Base Mark
5962-9473002MYC	XC4013-6CB228B	Quad Flat Pack with Base Mark
5962-9473001MZC	XC4013-10CB228B	Quad Flat Pack with Lid Mark
5962-9473002MZC	XC4013-6CB228B	Quad Flat Pack with Lid Mark

Xilinx Unveils New Speed Grade for High Performance XC3100A

The introduction of the new "-1" speed grade for the XC3100A FPGA family sets a new standard for FPGA performance. The XC3100A-1 offers a 20 percent logic block delay and 15 percent interconnect delay improvement over the XC3100A-2, previously the industry's fastest FPGA. Key performance parameters are listed in the table below.

The new -1 speed grade is yet another example of continual speed improvement through process and manufacturing advances as well as architectural innovation. These increases in FPGA performance continue to expand the range of applications that can be effectively addressed with FPGA technology. The XC3100A FPGA family is an ideal solution to the high-integration, high-performance needs of applications such as PCI interfaces, network controllers, ATM systems, and T3 telecommunications switches.

The XC3100A-1 speeds files are available on the Xilinx Technical Bulletin Board and will be included in the next release of XACT® development system. Samples for the XC3190A-1 are available now in PC84, PP175 and PQ160 packages. Other device/package combinations will soon be available; contact your local Xilinx sales representative for current price and availability information. ◆

XC3100A-1 Performance Parameters (preliminary)

	XC3100A-1	XC3100A-2	Percentage of Improvement
Block Delays (Combinatorial)			
Logic block	1.75 ns	2.2 ns	20%
Input block	1.8 ns	2.0 ns	10%
Output block	2.7 ns	3.0 ns	10%
Block Delays (Registered)			
Setup	1.7 ns	1.8 ns	6%
Clock to out	1.4 ns	1.7 ns	18%

Exemplar CORE 2.2 Adds VHDL Support for XC7300 EPLDs

With the upcoming Exemplar CORE version 2.2, designers can quickly develop efficient, compact, high performance EPLD designs using VHDL or Verilog HDL synthesis. The new CORE synthesis tool provides access to all the advanced features of the Xilinx EPLDs.

Enhancements include:

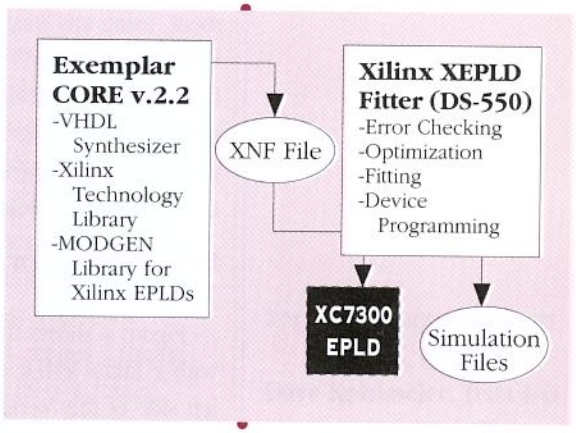
- A MODGEN library containing EPLD-optimized algorithms for creating high-level functions such as incrementers, decrementers, adder/subtracters and comparators. These functions now automatically use the EPLD arithmetic circuitry and fast-carry chain to create designs that are compact and efficient.
- The ability to control EPLD-architecture-specific features such as Fast Clocks, Fast Output Enables, and input pad registers.
- Attributes that allow you to control mapping, optimization and initial register states.
- An enhanced netlist writer capable of expressing all Xilinx XC7000 technology-specific primitives.

As shown in the diagram, Exemplar CORE v 2.2 synthesizes your VHDL or Verilog HDL design using the Xilinx technology and MODGEN libraries, producing an XNF file. The XNF file is then processed by the Xilinx DS-550 fitter to optimize the design for the XC7300 EPLD architecture, create a device programming file and produce reports on resource utilization and static timing analysis. The fitter also produces an XNF file that can be used for timing simulation.

Optimal Solutions with CORE v. 2.2

CORE v. 2.2 synthesizes complex functions by using algorithms optimized for the Xilinx XC7000 family.

For example, if you specify an 18-bit adder (using the "+" operator), the synthesizer uses the adder algorithm to create the function. This same algorithm is used for adders of any size. The MODGEN EPLD algorithms were developed by Xilinx to ensure that the Exemplar synthesizer efficiently uses all of the advanced EPLD features to create compact, high-speed designs automatically.



CORE v. 2.2 also provides attributes that allow users to control how a design is implemented in the target device. Performance and density can be fine-tuned by assigning critical functions to Fast Function Blocks, and by assigning high-speed clocks and fast output enable signals.

What You Need to Get Started

Exemplar CORE v. 2.2 is available from Exemplar Logic. It comes complete with the Xilinx Technology and MODGEN libraries. CORE v 2.2 is compatible with the DS-550 EPLD software (v 5.1 or later) available from Xilinx. No other Xilinx products are needed for EPLD design. Of course, CORE still supports the Xilinx FPGA products, making it a powerful tool for creating high-performance VHDL or Verilog HDL designs for both Xilinx EPLDs and FPGAs.

A VITAL-compliant simulator is now available with CORE. The Xilinx simulation library to support this simulator is under development and will soon be available. ◆

For more information, contact

Exemplar Logic

Phone: 510-849-0937

Fax: 510-849-9935

XILINX®

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

Data I/O Adds VHDL and XAC

Version 2.0 of Data I/O's Synario FPGA software adds two major features for Xilinx users:

- VHDL design entry
- Tight integration with XACT 5.0

With V2.0, users can do efficient Xilinx designs on the PC, in a Windows environment, using any mixture of schematics and VHDL source code. Synario also offers full XACT 5.0 support, including tight integration that allows users to control and run the XACT programs from directly inside Synario's Project Navigator.

Project Navigator Streamlines Xilinx Designs

Figure 1 shows the Project Navigator with a Xilinx VHDL design loaded. The left side of the Navigator shows the design's hierarchy, in this case a mixture with schematics at the top and VHDL below. The right side shows the steps required to implement and simulate the design, including creation of simulation models, generation of XNF files, and the ability to launch XMAKE from the Project Navigator. The Synario user can literally go all the way from design entry to a placed-and-routed FPGA with several mouse clicks.

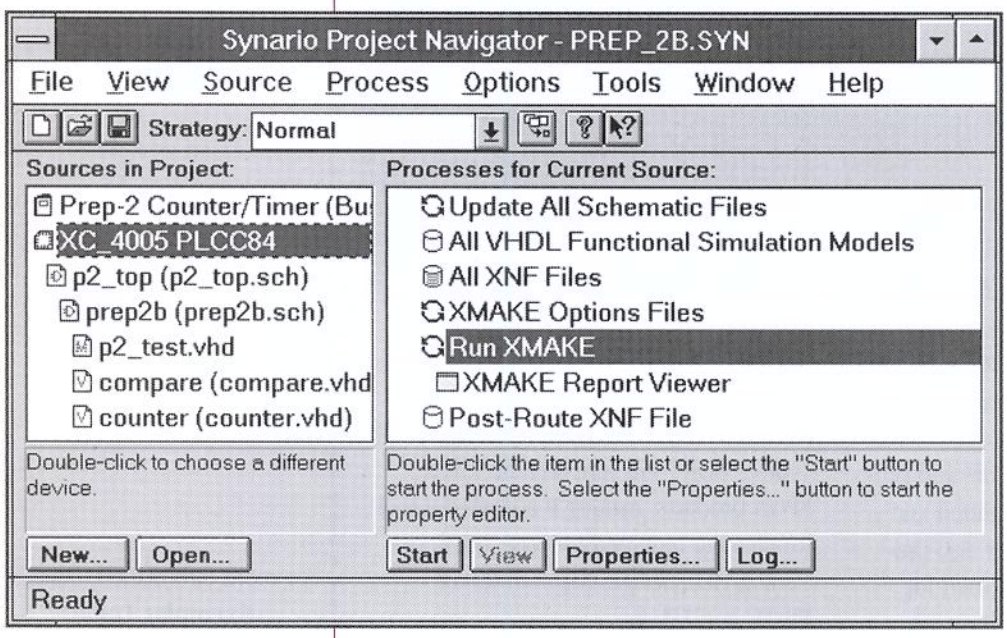


Figure 1: Xilinx VHDL design in Synario's Project Navigator.

Access to the Advanced Options

Synario recognizes that designers pushing the state-of-the-art often need advanced control of the Xilinx design process. Accordingly, the Project Navigator allows the user to set many of the options affecting the XACT programs, again directly from the Windows user interface. Figure 2 shows a portion of the dialog box that gives access to advanced options.

Robust XACT 5.0 Support

Synario V2.0 offers complete XACT 5.0 support, including:

- unified libraries
- X-BLOX
- XACT-Performance
- RPMs
- carry logic
- conversion of .MEM files to Verilog and VHDL
- behavioral instantiation of RPMs and soft macros

Synario's Xilinx Device Kit was substantially re-designed to optimize and improve it for XACT 5.0. The engineering work was done by three ex-hardware engineers with real Xilinx design experience.

Behavioral Entry from A to V

In addition to the SCS schematic environment (notable for its on-line connectivity database), Synario offers a wide range of choices for Xilinx behavioral entry.

Users creating large, multi-chip designs can take advantage of the new VHDL

ntegration to Synario

environment. Synario's VHDL solution offers the benefits of abstraction without sacrificing access to detailed silicon constructs that are often the key to efficient Xilinx implementations. By means of user-defined attributes, virtually any device feature that can be included in a schematic also also can be accessed in VHDL.

Users creating smaller- and medium-sized designs can opt for the ABEL-HDL language. ABEL is an excellent choice for mixed schematic/behavioral circuits with some control or datapath content. ABEL offers very tight control over detailed silicon constructs; again, virtually any Xilinx feature available in a schematic is also available in the language. For Xilinx state machines, ABEL offers automatic one-hot encoding.

Fast, HDL-Based Simulation

Synario V2.0 includes a choice of simulators, depending on the users' needs. The standard simulator is Verilog-based; it can be used transparently as a gate-level simulator, but offers the added advantage of the full Verilog language for stimulus generation.

For the VHDL designer, Synario offers the much-acclaimed Model Technology V-System simulator. Synario's Project Navigator can launch V-System directly and configure it for the Xilinx project. VHDL simulation includes full timing capability, thanks to the VBAK back-annotation software from Topdown Design Solutions, which creates a timing-annotated VHDL model from a routed LCA file. VBAK, too, is completely integrated into the Project Navigator. ◆

For more information about Synario, contact
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e-mail: davek@data-io.com

This article was contributed by Data I/O Corp.

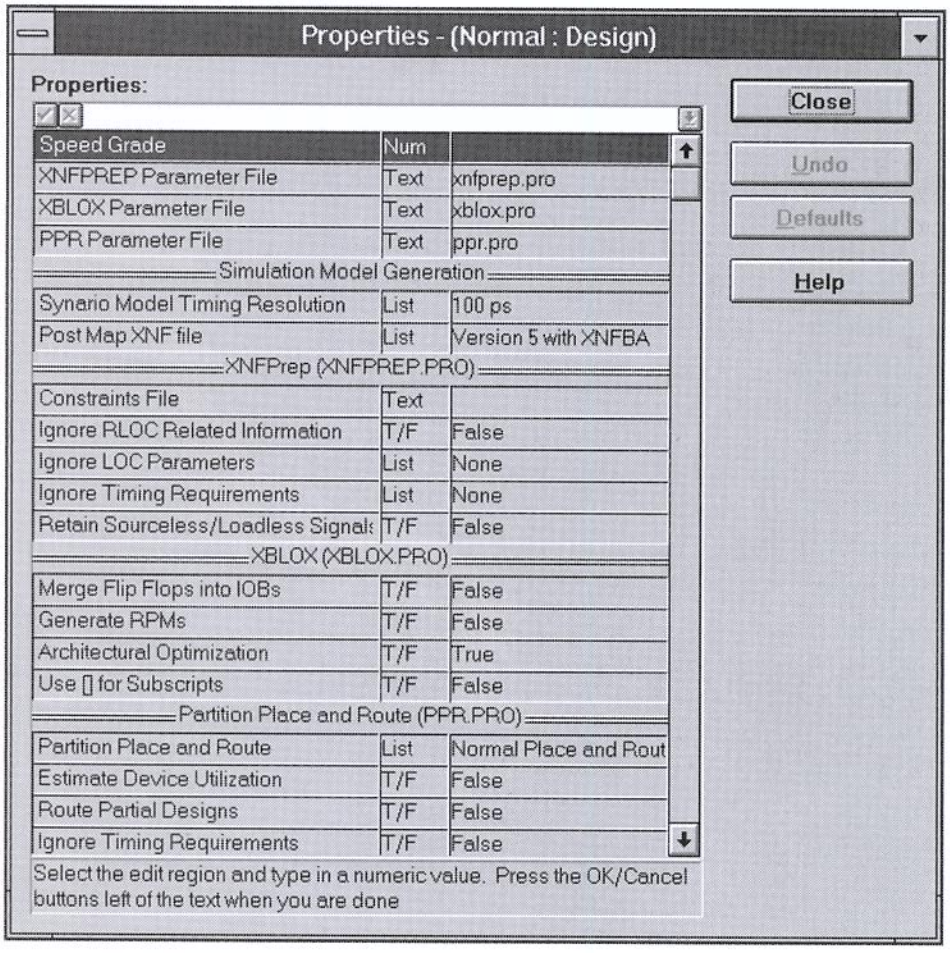


Figure 2: Setting advanced XACT options from inside Synario.

New Mentor Graphics Interface for Version A.1-F

The DS-MN8-STD package for Mentor Graphics A.1-F (formerly known as version 8.4) will begin shipping in March, 1995, as part of the XACT 5.1.1 release. The gen_sch8 and xblxgs programs have been updated, recompiled and relinked to the A.1-F database. RAM components also have been relinked. However, there are no changes to the design flow. The DS-MN8-STD package is available for both Sun Microsystems and HP 700 platforms.

Please refer to the release notes for further information.

Mentor Graphics began shipment of Autologic Unified Libraries for XACT 5 in December, 1994.

This release supports the XC3000, XC4000, and XC7300 families. The libraries are available from Mentor's supportnet under /pub/mentortech/tdd/fpga libraries. The names of the directories where they reside are xc4k_1.0.tar.Z, xc3k_1.0.tar.Z and xc7k_1.0.tar.Z. The ip address of the node is 137.202.128.4. Information on the design flow also is available in the same directory under xilinx_flow.ps (postscript) and xilinx_flow.fmkr (Framemaker). These libraries are developed and supported by Mentor Graphics.

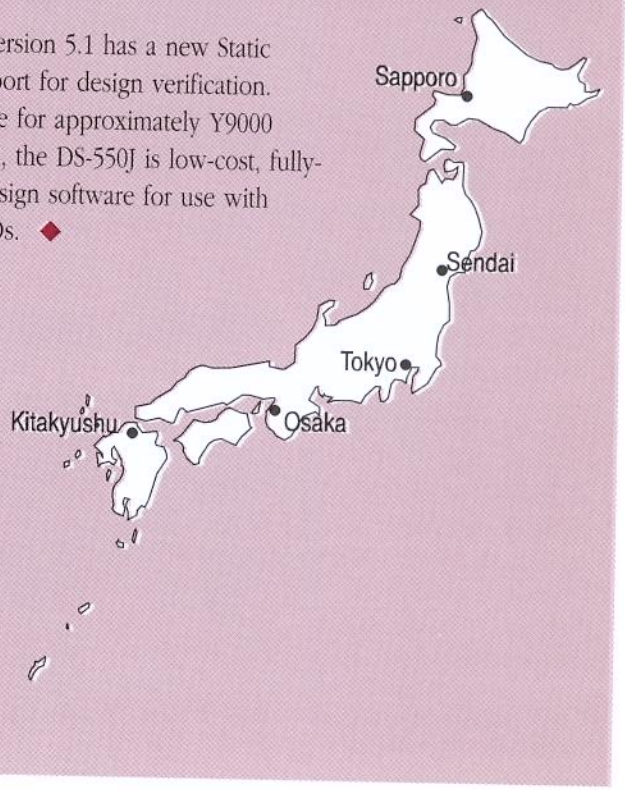
For more information, contact your local Mentor Graphics sales office. ◆

日本のＥＰＬＤユーザのためのソフトウェア (Software for Japanese EPLD Users)

Xilinx continues to meet the specialized needs of its international customer base by offering a localized version of the XEPLD development software for Japan. As with the standard DS-550 software, the DS-550J offers the user full flexibility for the fast, easy development of XC7000 EPLD family designs.

The DS-550J will begin shipping in March, 1995, with the XEPLD version 5.1 software and Japanese-language manuals. Version 5.1 includes support for third-party schematic editors and simulators such as OrCAD, Viewlogic, Mentor and Cadence. The user also has increased behavioral design capabilities; PLD compilers for the ABEL, CUPL, and PALASM design languages also are supported. In addition, version 5.1 has a new Static Timing Report for design verification.

Available for approximately Y9000 ($89.95 US), the DS-550J is low-cost, fully-featured design software for use with Xilinx EPLDs. ◆



SPECIAL REPORT:

FPGAs as Reconfigurable Processing Elements

In most applications, FPGAs are used to implement "glue logic," providing the advantages of high integration levels without the expense and risk of custom ASIC development. However, as SRAM-based FPGA devices have increased in capability, their use as in-system-configurable computing elements is receiving considerable attention. Indeed, reconfigurable FPGA technology holds the potential for reshaping the future of computing by providing the capability to dynamically alter a computer's hardware resources to optimally service the immediate computational needs.

Computing circuits built from SRAM-based FPGAs can meet the true goal of parallel processing — executing algorithms in circuitry with the inherent parallelism of hardware, while avoiding the instruction fetch and load/store bottlenecks of traditional von Neumann architectures. There are many computationally-intensive algorithms that can benefit from being partially or wholly implemented in hardware. Typically, these algorithms are too specialized to justify the expense of manufacturing custom IC devices. Just as often, the "algorithm space" is very large, and it may be impractical to perform enough simulations to find the optimal approach before committing to custom hardware.

"Reconfigurable FPGA technology holds the potential for reshaping the future of computing."

FPGA-based coprocessors address all these issues. With an FPGA-based "configurable coprocessor" the user can design (via FPGA configuration) exactly the special hardware required for a given task without having to construct new hardware for each application. Different tasks can be time-multiplexed into the same silicon. Errors can be corrected and different algorithmic approaches explored, with no further hardware expense.

Several universities and research laboratories have explored the use of SRAM-based FPGAs to implement multi-purpose, high-speed coprocessors for accelerating operations in computer systems. Using these systems, desktop workstations have delivered performance at the level of a supercomputer for specific applications. In particular, two projects have gained considerable notoriety — the PeRLe systems from DEC's Paris Research Lab, and the SPLASH machines from the Supercomputing Research Center (Bowie, Maryland). These systems consist of FPGA-based attached processors in engineering workstations, complete with programming tools and run-time environments, and have been the target for a variety of "real-world" applications.

DEC's Paris Research Lab has designed and implemented four generations of FPGA-based reconfigurable coprocessors called Programmable Active Memories (PAMs). The most-widely used version,

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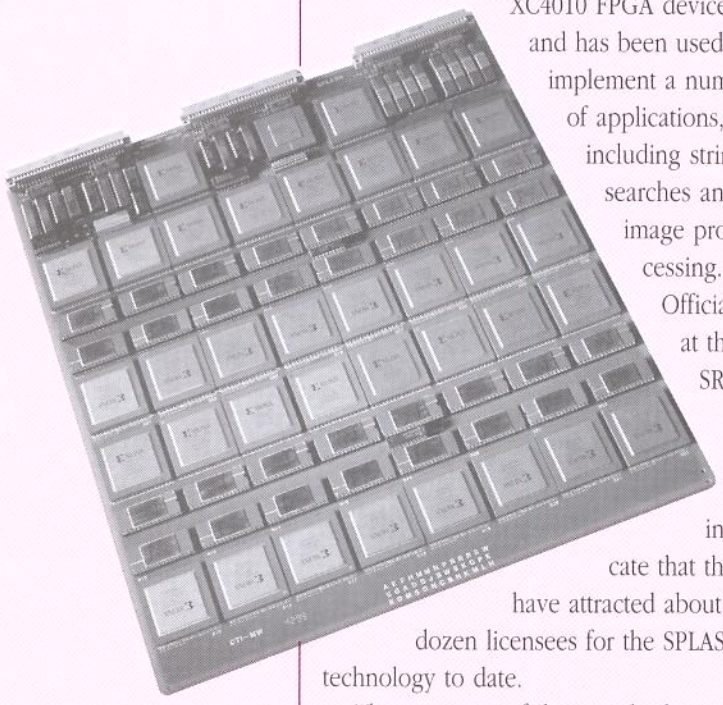
the PeRLe-1, is based on a 5x5 array of XC3090 FPGAs. Developed applications include long multiplication, RSA cryptography, heat and LaPlace equations, a Viterbi decoder, a sound synthesizer and a stereoscopic vision system. The C++ language (coupled with a specialized library) is used for programming the algorithms.

Two generations of the SPLASH processor, based on a linear array of FPGAs, have been designed at the Supercomputing Research Center (SRC). The SPLASH-1 includes a 32-stage linear logic array with a VME interface to a Sun workstation. Each stage consists of an XC3090 FPGA and a 128 Kbyte static memory buffer. SPLASH-1's first application was to implement a systolic algorithm for one-dimensional pattern matching during DNA research, where it outperformed a Cray-2 by a factor of 325 and a custom-built nMOS device by a factor of 45. The SPLASH-2 system is based on XC4010 FPGA devices, and has been used to implement a number of applications, including string searches and image processing. Officials at the SRC indicate that they have attracted about a dozen licensees for the SPLASH technology to date.



The successes of these and other early projects have fueled the interest of the research community. The IEEE now devotes an entire workshop to FPGA-based computing; the third annual IEEE Workshop on FPGAs for Custom Computing Machines (FCCM) will be held in Napa, California, in mid-April. The following is a sampling of some of the research projects discussed at previous FCCM workshops and other technical conferences:

- The GANGLION project at the IBM Almaden Research Center used XC3090 and XC3042 FPGA devices to implement a feed-forward, fully-interconnected neural network on a single VME board. At the time it was the fastest in the world, capable of executing 4.8 billion synaptic connections per second.
- The PRISM-I system from Brown University coupled XC3090 FPGAs with a Motorola M68010 microprocessor. PRISM-II uses XC4010 FPGA devices as coprocessors for an AMD29050 RISC processor. A compiler for functions coded in C also was developed.
- The Laboratoire d'Informatique de Brest (France) designed the ArMen machine, a MIMD ring of Transputers connected to a ring of XC3090 FPGAs, and the ReLaCS systolic programming environment (described as a close cousin to C). This modular, extensible system is implemented on a VME board for a Sun workstation. Developed applications include image processing and lattice gas simulation.
- The University of North Carolina's Anyboard is an ISA-bus coprocessor for PCs based on five XC3042 FPGAs. Designs are entered in a C-like hardware description language.
- The RECON system from the University of Melbourne, a reconfigurable coprocessor for Sun workstations, includes an XC4010 and XC2064 FPGA. C programs are compiled using a standard compiler, and then analyzed to determine which parts are most processor-intensive; these routines are then compiled to the gate level.
- The PAr2 system (Prototyping Array for Parallel Architectures) was designed for the verification of circuit designs gener-

ated by COMPAR, a computed-aided tool for mapping algorithms into parallel architectures (Universität des Saarlandes, Germany). The computational unit is based on a 3x3 array of XC4005 FPGA devices.

Some corporations have built their own FPGA-based reconfigurable processors for inclusion in their products. For example, the Configurable Hardware Algorithm Mappable Preprocessor (CHAMP) was designed by Lockheed Sanders (Nashua, NH) to perform spatial filtering, spectral filtering, and background normalization in an Advanced Missile Warning System. Six processing elements reside on a VME board. Each processing element consists of two XC4013 FPGAs and a 16Kx32 dual-port RAM; the processing elements are connected by a crossbar switch. The Bioccelerator from Compugen Ltd. (Petah-Tikva, Israel) uses 16 processing elements based on XC4000 family FPGAs to accelerate "profile searches" in protein and DNA databases; the system provides two to three orders of magnitude acceleration compared to high-end workstations.

Several emerging companies are bringing general-purpose FPGA-based processors to the commercial marketplace, including Annapolis Micro Systems, Inc. (Annapolis, MD), Giga Operations Corp. (Berkeley, CA), Metalithic Systems, Inc. (Sandy, Utah), and Virtual Computing Corp. (Reseda, CA). The following pages of this report give an overview of these companies and their products, based on material provided by these vendors.

Already, these products have led to some startling successes. Access Data Corp. (Orem, UT), has developed an application that recovers password keys for data decryption. The system uses a "brute force" method, cycling through all possible keys to find the correct one. Access Data recently used their system to assist the San Jose (California) Police Department in decrypting the contents of a disk from a confiscated PC, leading to the arrest of several operators of a child pornography ring.

The Radiation Oncology Department at UCLA is developing a system to accelerate repetitive tasks in the calculation of radiation dosage and dose distribution for treating cancerous tumors, improving the time to perform the calculations from several days (using a Sparc2 workstation) to under an hour.

For their part, FPGA manufacturers are actively involved in funding research and promoting the use of FPGA-based processors. Xilinx is distributing Giga Operations' Spectrum system to researchers and universities as part of its University Support Program. Stan Baker Associates (Los Gatos, CA) has established a home page (http://www.reconfig.com), ftp site, and mail server on the Internet to provide a forum for exchanging information about reconfigurable computing.

FPGA-based reconfigurable processors are viable platforms for a broad range of applications, including scientific computing, database manipulation, design automation, cryptography, image processing and real-time digital signal processing. FPGA-based processors can exploit the fact that most of the processing time for compute-intensive tasks is spent in a relatively small portion of the code, and hardware acceleration of that portion can significantly improve overall performance.

In the long term, expected advances in FPGA density, performance and architecture may offer more real advances than single processor solutions can promise. While significant hardware and software challenges remain, it is conceivable that reconfigurable processors constructed from SRAM-based programmable logic eventually will replace today's general-purpose processors, providing the basis for systems that automatically alter their own hardware to best solve the problem at hand. ◆

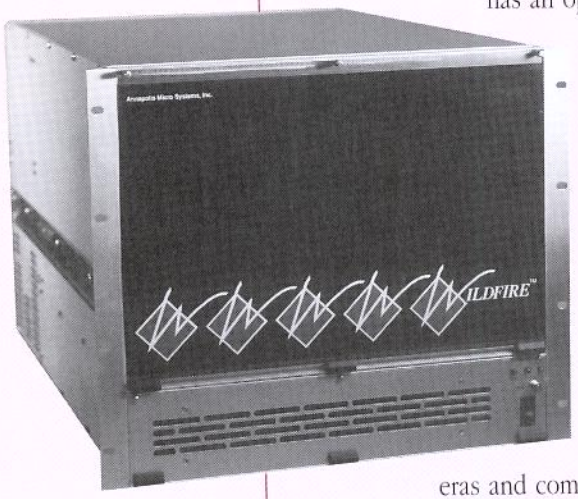
SPECIAL REPORT

FPGAs as RECONFIGURABLE PROCESSING ELEMENTS

Annapolis Micro Systems, Inc.

The WILDFIRE Custom Configurable Computer is based on SPLASH 2 technology transferred from the National Security Agency and the Institute for Defense Analysis' Supercomputing Research Center. Annapolis Micro Systems is the first licensee to offer a commercial product based on the SPLASH technology. A 30-person engineering design company, Annapolis Micro Systems accepted the challenge to bring SPLASH 2 reconfigurable computing out of the prototype/research environment.

Annapolis Micro Systems has enhanced the SPLASH 2 design to increase its commercial appeal and performance by expanding the I/O capabilities and interoperability of the system. The most significant enhancement is the move from a custom Futurebus-like backplane to a VME64 standard backplane. WILDFIRE has an open architecture that allows it to interface with commercial or custom-built VME cards, such as high-speed data acquisition devices (e.g., cameras and communication lines) and standard storage devices (e.g., disks and tapes).



A WILDFIRE computer consists of one to 16 WILDFIRE Array Cards residing in a rack-mountable VME chassis and connected with a Sun SPARC or PCI host processor through a VMEbus to SBus or PCI Bus interface card set. Each WILDFIRE Array Card has an array of 16 programmable Processing Elements (PEs) with crossbar connections to each PE. Each Processing Element consists of an XC4010 FPGA device with 512 Kbytes of high-speed memory. An additional XC4025 device with one megabyte of memory acts as the Control PE. A Motorola 68EC030 microprocessor on each Array Card is used for configuration, readback, diagnostics, and high-level data transfer and control. Three bidirectional 36-bit wide FIFOs provide data buffering — one allocated for SIMD (single instruction, multiple data operations), and one each for the left and right systolic I/O. The reconfigurable 18-port, 36-bit crossbar is built of XC4010 FPGAs. Crossbar connectivity is user-programmable; up to sixteen configurations can be stored, allowing the current configuration to be changed on any clock tick.

Standard WILDFIRE software includes a VHDL model of WILDFIRE, a C Runtime Library, a Host Interface Driver, and a debugger. WILDFIRE supports classic SIMD, MIMD (multiple data, multiple instruction), and systolic processing.

The mission of Annapolis Micro Systems is to provide a fully-supported, commercial product to address the high-speed needs of telecommunications, real-time image processing, encryption, and pattern matching. The company provides full technical support for their products and offers special classes and tutorials as well as application development services.

Established in 1982, Annapolis Micro Systems, Inc. provides custom electronic product design, including expert Xilinx design services, to commercial and government customers. The company has completed over 400 Xilinx FPGA designs. "Our background and expertise with Xilinx and product design place us in a unique position to successfully bring this Xilinx-based computer architecture to market," stated Jane Donaldson, President and founder of Annapolis Micro Systems. ◆

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Giga Operations Corp.

Giga Operations Corp. was founded in 1991 to develop FPGA-based, reconfigurable computing products that deliver supercomputer performance at microcomputer prices. The company is working with OEMs and developers to create a standard reconfigurable computer architecture.

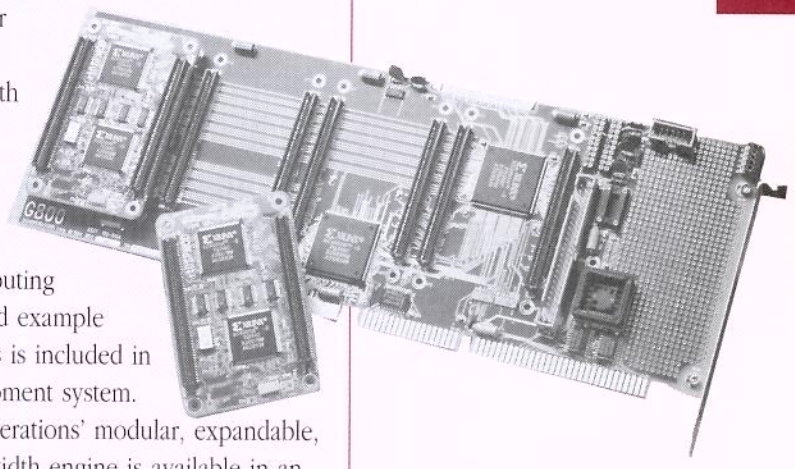
Giga Operations has designed a modular, scalable reconfigurable computing platform and development software that can be applied to many computationally-intensive tasks. The architecture is optimized for processing tileable databases such as video fields or frames. Data flow structures and computing architectures are implemented in FPGAs.

One developed application, the Spectrum™ video computing engine, is intended for applications such as machine vision systems, video editing, image processing, and 3-D volumetric image rendering and visualization. This video processor represents the first use of FPGAs in a reconfigurable computing product developed specifically for general-purpose visual computing applications.

Hardware products are based on plug-and-play XMOD™ computing modules, small boards with FPGAs and memory that can connect to third-party hardware or be embedded in peripheral devices. For example, the X210MOD features two XC4010 FPGAs, 8 Mbytes of DRAM, 256 Kbytes of SRAM and three configurable data bus interfaces on a 2.4" by 3.65" card. The use of isolation buffers between the FPGAs and memories allows local systolic connections to be implemented in local stacks of XMODs. For video processing applications, the VIDMOD/SC module implements S-video and composite video connections for a camera, tuner, television or VCR.

Giga Operations' G800 VESA VL-bus PC board delivers high-bandwidth I/O and is a carrier for XMODs. Four XMODs can be stacked four deep, for a total of 16 per G800 board. Intended for high-bandwidth applications, the G800 includes a 133 MB/s VL-Bus interface to a host PC, a 100 MB/s VMC (VESA Media Channel) bus, and a 100 MB/s interface to an external connector. All busses are programmable and connect to FPGA pins, allowing the development of other bus interfaces. The G800 provides three virtual busses to each XMOD processor: one 64-bit data bus, one 32-bit data bus and one 16-bit data bus.

At the core of Giga Operations' modular and expandable architecture is the XLINK™ operating system, a linker and algorithm packaging program that maps variables and FPGA functions into the user's C program. A compiler allows the use of C syntax to build hardware descriptions output as .XNF files. These enable C programmers to integrate host-based C programs with reconfigurable computers for execution at supercomputer speeds. Giga Operations also provides a Viewlogic interface for designers working with standard Xilinx tools. A library of video computing routines and example applications is included in the development system.



Giga Operations' modular, expandable, high-bandwidth engine is available in an open architecture with C-based software tools and libraries. Giga Operations, OEMs, and third-party developers are developing hardware and software standards for reconfigurable computing. The company and its partners are working to establish the XLINK operating system as the basis for commercial architectures in reconfigurable computing. ◆

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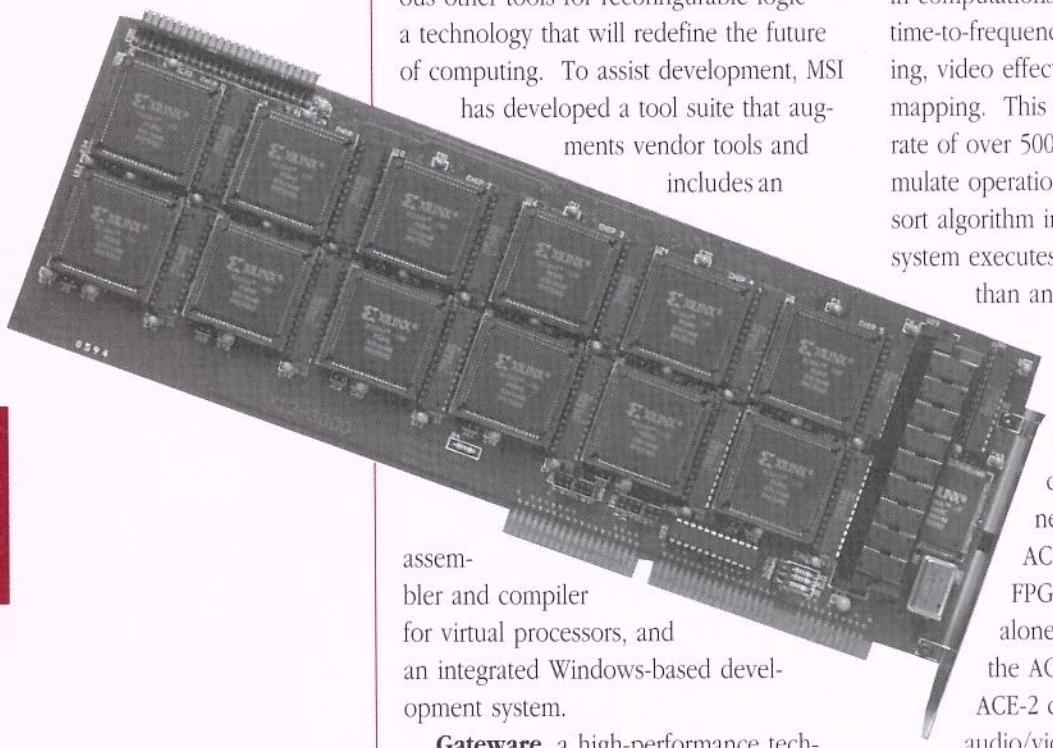
SPECIAL REPORT

FPGAs as Reconfigurable Processing Elements

Metalithic Systems Inc.

Metalithic Systems Inc. (MSI) provides quality computing platforms and tools for the emerging reconfigurable computing market. MSI has established significant expertise in reprogrammable architectures, reconfigurable instruction set processors, computationally-intensive macros, state machine synthesis and various other tools for reconfigurable logic — a technology that will redefine the future of computing. To assist development, MSI has developed a tool suite that augments vendor tools and includes an assembler and compiler for virtual processors, and an integrated Windows-based development system.



Gateware, a high-performance technology developed by MSI President and CEO Kent Gilson, is the foundation for all MSI products. By using FPGA technology, Gateware combines the reprogrammability of conventional microprocessors with the high-speed processing obtained using ASICs to deliver supercomputer-class processing for a fraction of the cost.

MSI's **ACE-12 Reconfigurable Compute Engine** uses 12 FPGAs to perform high-speed processing; the board can be populated with XC3090, XC3195, XC4005 or XC4010 devices. These processing elements are arranged in a parallel fashion, each with its own high-speed SRAM, thereby allowing for the efficient implementation of multiple processors for general-purpose reconfigurable computing. The ACE-12 system includes software and predefined configurations that support the read/write of SRAM, downloading of configurations to any subset of FPGAs, and concurrent configuration and execution.

One application currently running on the ACE-12 is a 3x3 transform engine used in computations such as machine vision, time-to-frequency conversion, video filtering, video effects processing and texture mapping. This engine currently runs at a rate of over 500 million multiply and accumulate operations per second. A swap/sort algorithm implemented on the ACE-12 system executes more than 360 times faster than an Intel 486 processor running at 33 MHz.

For multimedia and general-purpose applications where "moderate" computing power is needed, MSI created the ACE-2 card, based on two FPGA devices. It can stand alone or operate in concert with the ACE-12. Fully configured, the ACE-2 can operate as a personal audio/video/MIDI recording studio, video teleconferencing station, high-speed voice and data modem, video on demand CODEC, or other I/O and computationally-intensive applications.

The SonicACE is a complete recording studio for the PC. The SonicACE system, comprised of an ACE-2 card and SonicACE software, can perform operations normally handled only by similar stand-alone equipment costing as much as 4 to 10 times more. SonicACE allows the user to mix up to 128 digital tracks and includes group mute/solo capabilities, nondestructive pan/fade/echo/EQ, a 24-voice synthesizer, WAV sampling, master/slave MIDI synchronization and simultaneous play and record. ◆

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Virtual Computer Corp.

"We define transformable computing systems as those machines that use the reconfigurable aspects of FPGA technology to implement an algorithm," states Steve Casselman, President and founder of Virtual Computer Corp. "Transformable computers will play a lead role in the evolution of a new generation of programmers, researchers, students and users of computers."

In 1988, Virtual Computer Corp. (VCC) was awarded a grant through the Small Business Innovative Research Program to design a reconfigurable computer for the Naval Surface Weapons Department of the U.S. Navy. The resulting system, the P-Series Virtual Computer, is now available commercially, and provides over 600,000 gates of reconfigurable logic. The system includes 52 XC4010 or XC4013 FPGAs interconnected using 24 I-Cube IQ160 programmable interconnect devices, 8 Mbytes of high-speed SRAM, 256 Kbytes of dual-ported RAM and three 64-bit I/O ports. An SBus interface is available, and interfaces to other busses can be developed with relative ease.

The recently-released EVC-1 system is the first of a series of SBus-based reconfigurable computers from VCC. The EVC-1 board includes the bus interface, a single XC4010, XC4013, or XC4025 FPGA device, and 256K bytes of memory, and is intended for use as a coprocessor in a Sun Sparcstation. The EVC-1 also supports a daughterboard with 96 I/O lines for additional hardware prototyping. The EVC-1 package includes the EVC SBus transformable computer board, schematics, manual, SBus interface driver, source code, and example programs. An optional 2-Mbyte SRAM module currently is available.

The EVC-1 can be used as a logic emulator for rapid product development, as an evaluation platform for new chips and designs, or as an accelerator for computationally-intensive algorithms. Used as a rapid prototyping system, the EVC-1 can accelerate time-to-market at a relatively low cost. To evaluate the use of a new device (such as MPEG, DSP, or ATM chip), the IC can be placed on an add-on module, using the EVC-1 to implement the interface protocols and glue logic; this provides a cost-effective means of testing the functionality of a variety of new chips under consideration for designs. The EVC-1 also can be used to "hardwire" software algorithms, dramatically accelerating slow, repetitive software processes.

VCC's software tools are developed around the concept of "hardware objects" — FPGA-based computing engines that are linked to the application via C subroutine calls. VCC provides pre-developed hardware objects obtained from third-party experts as well as the development software for creating the objects. For example, the Virtual Random Number Generator (VRNG) hardware object is a true, non-deterministic random number generator producing double floating point numbers for use in simulations. The VRNG hardware object performs 15 times faster than running the same algorithm on a SPARC2 workstation.

The EVC-1 transformable computer is being used by more than a dozen universities in Canada, Europe, and the United States, as well as a number of industrial users. *Military and Aerospace* magazine named it the "Editor's Choice" in the October 1994 issue. In December, VCC was selected above 60 other nominees for the first "Small Business Innovative Research Technology of the Year" award at a conference sponsored by NASA and the Technology Utilization Foundation. ◆

SPECIAL REPORT

FPGAs as Reconfigurable Processing Elements

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Building PCI Interfaces With Xilinx FPGAs

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

PCI-compliant, high-density programmable logic devices can be used to create flexible PCI bus interfaces that avoid the costs and risks of custom IC development. Examples of fully compliant programmable logic devices include the XC3100A FPGA and XC7300 EPLD families from Xilinx, Inc. *PCI Compliance Checklist* data has been submitted to the PCI SIG (and is available to interested users) for the -2 speed grade of the XC3100A FPGA family, and -10 and -7 speed grades of the XC7300 EPLD family (as reported in *XCELL #15).*

Some designers are interested in integrating the PCI bus interface, along with their unique control logic for the back-end device being connected to the bus, into the same programmable device. These designers will be attracted to the capacity of the higher-density FPGA devices in the XC3100A and XC4000 families.

The first issue that a designer must face before selecting an FPGA technology is whether full PCI compliance is needed. Full compliance is a requirement for any board intended to be plugged into any PCI system or any system intended to accept any PCI-compatible boards. In other words, full compliance is a must in systems that are to be sold in to the general marketplace and require interoperability among multiple vendors. XC3100A-2 FPGAs are recommended for such systems.

"Full compliance is a must in systems that are to be sold in to the general marketplace and require interoperability among multiple vendors."

However, if the system environment is "closed," in the sense that the PCI bus is being used internally in a system where the equipment designer has control over all devices that interface to that bus (such as an embedded system with no add-in capabilities), then, of course, the designer has freedom to deviate from the specification. This would expand the range of available devices, and the XC4000-4 FPGAs may be preferable.

Several successful PCI designs have been based on the XC3100A FPGA family. In fact, the PCI Special Interest Group (PCI SIG, the industry consortium controlling the PCI standard) chose an XC3100A device for the board developed for use in their BIOS compliance test kit.

While not fully compliant, the XC4000-4 FPGA family also has been used in a number of "embedded system" PCI bus implementations. (The XC4000-4 FPGA devices fall just short of meeting the T_{VAL}, T_{SU}, and T_H timing requirements, but are compliant in all other aspects.) However, XC4400 HardWire™ devices, mask-programmed versions of the XC4000 devices, are compliant, allowing for prototype development with the programmable version, but high-volume manufacturing with the compliant HardWire version. A higher-performance version of the XC4000 FPGA architecture will be available later in 1995, and is expected to be fully compliant. The XC4000 architecture has several features that facilitate PCI bus interface design, including the ability to implement 9-input functions in a single block (easing parity generation and checking), and on-chip RAM capability (facilitating the on-chip implementation of the PCI configuration registers).

Careful design is required to meet the performance and signaling requirements of the PCI specification. The PCI bus protocols encourage burst-oriented data flows between bus agents, facilitating the use of pipelined data flows within PCI bus interface logic; pipelining techniques

often are key to successfully supporting data transfers at the maximum throughput of the bus. Typically, pipelining also is required in the parity generation and checking logic since 36-bit wide parity circuits will traverse multiple levels of logic blocks. The register-rich XC3100A and XC4000 FPGA architectures lend themselves to pipelining techniques.

Typically, the signals involved in bus transactions and the operation of data flow pipelines are controlled by state machines in the bus interface logic; example state machines for controlling bus signaling are provided in Appendix B of the PCI Specification. In some cases, bus control signals must be responded to on the first clock edge after their activation. Thus, high-performance state machines are required. For FPGAs, one-hot-encoded (OHE) state machines are recommended (that is, state machines with one register per state and minimal decoding logic). These are well-suited for register-rich FPGA architectures.

The use of the XACT-Performance™ feature of the PPR place and route program greatly eases the design process by allowing the specification of target performance requirements for entire paths through the design, a key factor in high-performance designs such as PCI interfaces. PPR's guide option, wherein the placement and routing of a previous version of a design can guide the implementation of a new version with minimal changes, also can significantly shorten design cycles.

These and other issues are discussed in a new application note from Xilinx, "A Fully-Compliant PCI Interface in an XC3164A-2 FPGA," which describes a target interface design that links the PCI bus to a slave processor through a dual-port RAM, using an XC3164A-2 device in a 160-pin PQFP package. The design was coded in Verilog HDL, synthesized using Exemplar Logic's CORE™ tools, and verified on a PC using Simucad's Silos/Verilog simulator. It uses only 40 percent of the logic blocks available in the XC3164A FPGA. Verilog-HDL and Viewlogic schematic design files also are available.

While careful design is required, PCI-compatible FPGA devices bring the system-integration, flexibility and time-to-market benefits of high-density programmable logic to the PCI design community. These devices can provide the performance, density, and routability to handle complex structures such as pipelined data paths, 32-bit parity generation, and PCI bus control.

For more information on PCI bus design using Xilinx products or to obtain a copy of the PCI Information Packet, contact your local sales representative, or send electronic mail to pci@xilinx.com. ◆

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

Xilinx Macro for PCMCIA Flash Cards

Mobile Media Research has introduced XFlash, a flash memory controller macro for building PCMCIA cards. The macro is designed for 160-pin XC3064A and larger XC3000A/XC3100A family devices. The XFlash macro and Intel 28F008SA 8-Mbit (or compatible) flash memory devices can be used to design an Intel Series II compatible PCMCIA flash card. The macro implements the same card interface and register set as the Series II flash card, and, therefore, works with the installed base of drivers written for the Intel Series II cards. Of course, the FPGA implementation provides designers with flexibility for customizing the application.

Mobile Media Research (San Jose, CA) manufactures and markets PCMCIA development tools and multimedia development tools and algorithms. *For further information, contact:*

Mobile Media Research
Phone: 408-428-0310
Fax: 408-428-0379 ◆

Achieving Optimal Results With PPR 5.1.0

Previous issues of *XCELL (#11, #13, #14)* have discussed different PPR options for routing tough designs, increasing performance and reducing execution times. Enhancements made to PPR 5.1.0 have made some options obsolete; these options should no longer be used. Please refer to the release notes, and remember to remove the obsolete options from your XACTINIT.DAT files.

There are cost values assigned to the routing resources of an FPGA device. PPR uses these cost values when determining which resources should be used for a given signal. Empirical evidence suggests that some of the default values assigned to the routing resources may be too low in the XC3000A/XC3100A and XC4000A devices. This means that PPR may use these resources more frivolously than it should, and, therefore, the routing is not as efficient as possible. The following options can be added to an XACTINIT.DAT file to adjust the default costs:

For XC3000A/XC3100A parts:

```
def_cost_long = 60
```

For XC4000A parts:

```
def_cost_long = 40
def_cost_double = 20
```

Some options allow you to reduce PPR run times. If your design does not have strict performance and routablility requirements, you can dramatically reduce runtime with the following command-line options:

```
PPR <design_name>
  placer_effort=1
  router_effort=1
```

If you feel that your design should route easily, use the "router_effort = 2" command line option. If your design is marginally routable, use "router_effort = 3". A design that is marginally routable is one that routes to about 95 percent or more fairly quickly, but doesn't route completely with router_effort = 2. If the design routes to less than 90 percent and stays there for an extended period of time with little improvement, try increasing the placer_effort and/or floorplan the design in order to achieve a better placement.

To cut down the run time of the placer when using the "placer_effort=4" command line option, you can also use the "place_with_timing=false" option.

Avoid the "timing=when_routable" or the "timing=false" PPR command line options. ♦

OrCAD Library Compatibility with XACT 5.0

Designers employing OrCAD schematic entry and simulation tools for Xilinx designs need to ensure that their tools are compatible with XACT 5.0 and their OrCAD software.

In order to be compatible with XACT 5.0, the design must be up to Version 4 compatibility. The following is a list of various versions of DS-35 interfaces, and the library files associated with each:

DS-35	Library Filenames
v2.40	x2000.lib, x3000.lib
v4.xx	x2k.lib, x3k.lib, x4k.lib
CVT *	x2-cvt.lib, x3-cvt.lib
v5.00	xc2000.lib, xc3000.lib, xc4000.lib

** CVT was not a release of DS-35. It was a set of intermediate files to allow designs captured in DS-35 v2.40 to be updated to DS-35 v4.xx (XACT 4) compatibility.*

If a design uses libraries from either DS-35 v4.xx, or DS-35 v4.xx and CVT, no modifications are required. The design is already up to XACT 4 compatibility and is suitable for compilation with the XACT 5.(tools. Designs that use the libraries from the DS-35 v2.40 interface are not compatible and must be updated. To update the design, the user must obtain a copy of the CVT files from the Xilinx Bulletin Board

Board-Level Simulation Using Viewlogic Tools and XACT 5.0

To better manage increasing design complexity, a growing number of designers employ board-level simulation involving multiple devices, as well as simulating each FPGA on its own. Board-level simulation increases the designer's ability to integrate today's complex devices into a single board-level design by providing a means to test the interface between devices as well as the functionality of each device.

The Viewlogic simulation tools can be used for board-level simulation of designs using Xilinx devices. First, a board-level schematic is created in a project directory separate from the Xilinx designs. In this board-level project directory, all board-level schematics and symbols representing the Xilinx devices are created. The schematics for the various individual Xilinx devices do NOT reside in this board-level project.

As each Xilinx device, created in its own separate project directory, is routed and then back-annotated, a simulation model, or WIR file, is created. When all the simulation files for the Xilinx devices have been created, they are copied to the board-level simulation directory's WIR subdirectory. The final step is to create a board-level simulation network VSM file.

The steps needed to prepare timing simulation models for board-level simulations with Xilinx devices are described below. The simulation model created can be used with any of the ViewLogic simulation tools. This example assumes the FPGA design is named "design1" and has its own project directory.

1. Run XSimMake (functional) on design1 with the command:
   ```
   xsimmake -fvff design1
   ```
2. Run XMake on design1 with the command:
   ```
   xmake design1
   ```
3. Run XSimMake (timing) on design1 with the command:
   ```
   xsimmake -fvft design1
   ```
4. Run XNF2WIR on the resulting xnfba.xnf file with the command:
   ```
   xnf2wir xnfba.xnf
     wir\sdesign1.1
   ```

In step 3, XSimMake places the timing information in a WIR file called xnfba.1. To create a WIR file with the same name as the symbol used in the board-level schematic, xnf2wir must be run on the

Continued on the next page

n (ORCADCVT.ZIP if using OrCAD
DR386CVT.ZIP if using OrCAD 386+
. The design must be compiled
the CVT files in conjunction with the
v4.xx libraries.
far as compatibility with OrCAD is
ned, the libraries shipped with DS-
00 are in the OrCAD 386+ v1.10
. These libraries are not compatible
ie older OrCAD 4.20 tools. Additionally, the simulation model files are not compatible with the new OrCAD VST 1.20 simulator. Designers who wish to use a version of OrCAD other than OrCAD 386+ v1.10 must obtain a copy of the library source files and recompile them. The source files are available from the Xilinx BBS as:

ORCSRC.ZIP	DS-35 v5.00 library source files
ORLIBSRC.ZIP	DS-35 v4.xx and CVT library source files

◆

Board Level Simulation

Continued from previous page

xnfba.xnf file explicitly, so that the output name can be specified to match the board-level symbol name. Name association is used to pull in the WIR file when the simulation network is created.

5. Run VSM -w on sdesign1 with the command:
   ```
   vsm -w sdesign1
   ```

   VSM will find the sdesign1.1 file in the WIR directory and will use it to create another sdesign1.1 WIR file in the current directory. This step will flatten the design. This means that there will only be built-in components in the resulting WIR file. This must be done because there are no aliases in the WIR file from xnf2wir. Without aliases, VSM will pull in the wrong components if families are mixed (i.e. XC3000 and XC4000 devices on the same board) or multiple designs use X-BLOX.

6. Edit the sdesign1.1 WIR file in the current directory, replacing all the BUILTIN aliases to XBUILTIN. Basically, do a replace string:
   ```
   "XBUILTIN:" for "BUILTIN:".
   ```

   This will create a WIR file in the current directory that contains only Xilinx builtin components with the alias of XBUILTIN, allowing the mixing of Xilinx components with other vendors' libraries. Skip this step if only Xilinx devices are to be simulated. Copy the edited sdesign1.1 file from the current directory to the board-level simulation's WIR directory.

7. If Step 6 was performed, create a viewdraw.ini in the board-level simulation directory with the following directory scan listing at the end:
   ```
   DIR [M] c:\workview\
     unified\builtin (xbuiltin)
   ```

   If Step 6 was NOT performed, create a viewdraw.ini in the board-level simulation directory with the following directory scan listing at the end:
   ```
   DIR [M] c:\workview\
     unified\builtin (builtin)
   ```

8. Add any other libraries needed to simulate any other vendors' components. (e.g., ViewLogic's full blown built-in with the alias "(builtin)").

9. In the board-level simulation directory, create a symbol with the same name as the WIR file that was copied (i.e. sdesign1) and use it in the board schematic.
10. Run VSM on the board-level schematic with the command:
    ```
    vsm toplevel
    ```

    Make sure that the only schematics in the board-level directory are for the board-level design itself. NONE of the sdesign1 schematic files can be present when VSM is run. If these files are found by VSM, VSM will re-create the WIR file by running the ViewLogic check program. This will overwrite the WIR file that was created by the Xilinx tools and copied to the WIR directory. Because the schematic is not found by VSM, VSM will "blindly" pull in the WIR file created by the Xilinx tools and use it to create the simulation .vsm network.

11. Simulate the board-level schematic. ♦

XACT 5.0 Libraries Guide Errata

Chapter 2 - Selection Guide

p. 2-47, 2-48, 2-54, 2-55: The M4_1, M8_1, and M16_1 macros have been obsoleted, yet are incorrectly shown as Exact or Closest Unified Replacements. The Closest Unified Replacements are the M4_1E, M8_1E, and the M16_1E macros, respectively.

p. 2-52: The Exact Unified Replacement for the CUP8H macro should be the CC8CLE macro, not the CB8CLE macro.

p. 2-52: The Exact Unified Replacement for the CUP16H macro should be the CC16CLE macro, not the CB16CLE macro.

Chapter 3 - Design Elements

p. 3-32, 3-301: The text descriptions for the ACLK and GCLK macros are incorrect. You cannot connect ACLK or GCLK to a PAD element. You should connect these elements to an IPAD or to an IBUF if a direct pad connection is not desired.

p. 3-57: The equation to generate an unsigned binary "overflow" that is always active High should read:

```
unsigned overflow =
   C0 XNOR ADD
```

p. 3-97: The third sentence of the first paragraph should read, "When CLR is High, all other inputs are ignored and data (Q1-Q0) and terminal count (TC) go to logic level zero."

p. 3-203, 3-205: The O1 input on the XC3000 CLB symbol should be DI.

p. 3-345: The first sentence should read, "The MD1 output pad is....".

p. 3-387: When the OSC is used with the XC2000 family, the crystal oscillator is enabled automatically. However, when the OSC is used with the XC3000, you must specify the MakeBits -s option. See P. 2-245 of the *XACT Reference Guide, Volume II*, for more information.

p. 3-407, 3-412: The symbol output label should be O(7-0), not Q(7-0).

p. 3-426: The third sentence of the first paragraph should read, "When L is High and CLR is Low, data on the D7-D0 inputs is loaded into the corresponding Q7-Q0 bits of the register during the Low-to-High clock (C) transition."

p. 3-442: The DONEIN pin is incorrectly shown as an output on the STARTUP symbol. It should be an input.

Chapter 4 - Attributes, Constraints, and Carry Logic

p. 4-8: Please note that the correct tag order to specify an inverted clock is "CLK:K:NOT". Specifying "CLK:NOT:K" is invalid.

p. 4-33: Under the description of the C flag, please note that for an XC4000 design, the critical attribute only applies if the PPR path_timing option is set to false, which is not the default.

p. 4-40, 4-41, 4-72, 4-80: References to BUFT support for RLOCS are erroneous. BUFTs do not accept RLOCs.

p. 4-98: Figure 4-18 incorrectly shows the F3 input to the F Carry Logic block being sourced by the F4 input. It should be sourced by the F3 input. Also, for an additional, perhaps clearer, diagram of the carry logic, see P. 8-106 of the *1994 Programmable Logic Data Book*.

p. 4-99, 4-100: Table 4-16 entries should be corrected as follows:

ADD-G-F3- cy4_05
ADDSUB-G-F3-cy4_16
FORCE-F3- cy4_41
SUB-G-F3- cy4_11

Also, included in the XC4000 library you can find a symbol called "CY4MODE". This symbol is a chart of all 42 recognized carry logic modes along with the names of their associated symbols. You may wish to temporarily instantiate this symbol onto your schematic as a quick reference. *(See* XCELL #15, *Technical Q&A).* ◆

Configuration Control Pin Connections in

The following recommendations guarantee a well-defined beginning for any FPGA configuration or reconfiguration process — after the initialization and clearing of the configuration memory in all FPGAs has been completed, and the address counter in the serial PROM(s) has been reset. Previous versions of the Xilinx Data Book have shown different solutions, but the connections described below guarantee reliable operation even under adverse operating conditions such as V_{CC} glitches.

The lead device can use any configuration mode available. In master modes and Asynchronous Peripheral mode, its CCLK pin is the output that clocks all other devices.

Obviously, all CCLK and XC17000 CLK pins must be interconnected, the DATA outputs from multiple XC17000 serial PROMs must be interconnected and connected to the DIN input of the lead device. The daisy-chain must be established by connecting each DOUT output to the downstream DIN input.

The following recommendations assume that there are no XC2000 devices in the daisy chain (they lack the $\overline{\text{INIT}}$ pin) and that, if Serial mode is chosen for the lead device, the XC17000 device(s) store **only one** configuration for the whole daisy chain. The serial PROM(s) must, therefore, be reset before the daisy chain is to be (re)programmed.

There are three possible types of daisy chains using XC3000 and XC4000 devices. Here are the recommended connections for the configuration control pins.

Configuration control pins are:

- **XC3000, XC3000A, XC3100, XC3100A**
  DONE/$\overline{\text{PROGRAM}}$ (open-drain output/input)
  $\overline{\text{RESET}}$ (input)
  $\overline{\text{INIT}}$ (open-drain output)
- **XC4000, XC4000A, XC4000D, XC4000H**
  DONE (open-drain output/input)
  $\overline{\text{PROGRAM}}$ (input)
  $\overline{\text{INIT}}$ (open-drain output/input)
- **XC17000**
  RESET (input with programmable polarity)

Case 1

Daisy chain consists of nothing but XC3000-type devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all slave $\overline{\text{INIT}}$s and connect them to the lead $\overline{\text{RESET}}$ input.
- Interconnect all DONE pins.
- Interconnect all slave $\overline{\text{RESET}}$ inputs
- Instigate **Reprogram** by pulling the slave $\overline{\text{RESET}}$ net Low for at least 6µs while all DONE pins are Low. (DONE can be permanently wired Low, but that sacrifices the use of $\overline{\text{RESET}}$ as a global reset of the user logic. If DONE is not wired Low, reprogram must pull DONE Low with an open-collector or open-drain driver).

Continued on next page

PGA Daisy Chains

Case 2

Lead device is XC4000-type, driving any mixture of XC3000 and XC4000 devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all $\overline{\text{INIT}}$ pins.
- Interconnect all DONE pins.
- Interconnect all XC4000 $\overline{\text{PROGRAM}}$ inputs.
- Interconnect all XC3000 $\overline{\text{RESET}}$ inputs.
- Combine these two nets into one $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ net
- Instigate **Reprogram** by pulling the combined $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ Low.

Case 3

Daisy chain consists of nothing but XC4000-type devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all $\overline{\text{INIT}}$ pins.
- Interconnect all DONE pins (only required for UCLK-SYNC option).
- Interconnect all XC4000 $\overline{\text{PROGRAM}}$ inputs.
- Instigate **Reprogram** by pulling $\overline{\text{PROGRAM}}$ Low. ◆

Beware of a Slow-Rising XC3000 RESET Input

It is a wide-spread habit to drive asynchronous $\overline{\text{RESET}}$ inputs with a resistor-capacitor network to lengthen the reset time after power-on. This also can be done with Xilinx FPGAs, but the user should question the need, and should beware of certain avoidable problems.

Xilinx FPGAs contain an internal voltage-monitoring circuit, and start their internal housekeeping operation only after V_{CC} has reached ~3.5 V. The internal housekeeping and configuration memory clearing operation then takes between 10 and 100 ms, depending on configuration mode and process variations. Any RC delay shorter than 40 ms for a device in master configuration mode, or shorter than 10 ms for a device in slave configuration mode, is clearly useless.

A significantly longer RC delay can be used to hold off configuration, as shown in the flow-diagrams on pages 2-27 and 2-119 of the *1994 Xilinx Data Book*. Without the use of an external Schmitt trigger circuit, the rise time on the $\overline{\text{RESET}}$ input will be very slow, and is likely to cross the threshold of ~1.4 V several times, due to external or internal noise. This can cause the FPGA to start configuration, immediately abort it, then start it again, after having automatically cleared the configuration memory once more.

This is no problem for the FPGA, but it requires that the source of configuration data, especially an XC17000 serial PROM, be reset accordingly. This is another reason for using the $\overline{\text{INIT}}$ output of the lead FPGA, instead of $\overline{\text{LDC}}$, to drive the $\overline{\text{RESET}}$ input of the XC17000 PROMs. ◆

General

Q: Will the XACT 5.x software run under Windows NT?

A: Windows NT controls the PC's parallel port. The XACT 5.x software does not have direct access to the parallel port, and, therefore, cannot recognize the key. The Xilinx programmable key manufacturer, Rainbow Technologies, has developed a work-around for our users. The file RAINPORT.EXE is in the SWHELP area on the Xilinx Bulletin Board Service. This self-extracting archive contains the necessary drivers and instructions for running XACT 5.x software under Windows NT. ◆

XABEL

Q: While running AHDL2X v5.0 on a Pentium 90 MHz PC, I receive a message indicating that my key is not authorized to run XABEL. What could be the cause of this problem?

A: This problem is fixed in the XACT v5.1 update. This update has been shipped to all of our registered Base Package customers. However, if you have not received the update, you may either download PPR_EMUL.ZIP (for 386s without co-processors) or PPR_MATH.ZIP (for 386s with co-processors or 486s) from the Bulletin Board Service, or contact Technical Support to get the update.

Viewlogic Helpful Hint:

For XACT 5.1, a new Xilinx specific built-in library has been added to our Viewlogic interface to support board-level simulation. The following line must be added after the current built-in library. This also has been documented in the XACT 5.1 release notes.

For PCs:

```
DIR [m]
   \workview\unified\xbuiltin
   (xbuiltin)
```

For Workstations:

```
DIR [m]  /workview/unified/
   xbuiltin   (xbuiltin)
```
◆

E-Mail Addresses for Applications Information

Xilinx users with access to the Internet can use the following E-mail addresses for requesting information or asking questions involving the listed application areas. Please be sure your message includes your E-mail address, shipping address, telephone number and fax number so that you may receive a reply. ◆

Application	E-Mail Address
Peripheral Component Interconnect Bus (PCI)	pci@xilinx.com
Asynchronous Transfer Mode Communications (ATM)	atm@xilinx.com
Plug and Play	pnp@xilinx.com
PCMCIA	pcmcia@xilinx.com
Digital Signal Processing (DSP)	dsp@xilinx.com

EPLD

Q: Please outline any architectural differences between members of the XC7300 family of EPLDs.

A: Users of the XC7300 family of EPLDs should be aware of the differences between family members outlined in the table at right.

Also note that, because the XC7318 and XC7336 contain only Fast Function Blocks, all flip-flop clock signals must be on the FCLK nets, and all output enable signals must be on the global FOE nets.

Fast Function Block Differences

XC7318/36/144	XC7354/72/108
Output polarity control	Fixed output polarity
Direct support for D- or T-flip-flop	D-flip-flop only
Flip-flop async. set or reset	Flip-flop asynchronous set only

I/O Block Differences

XC7318/36	XC7354/72/108/144
Direct input only	Direct, latched, or registered input
No input polarity control	Input polarity control

Q: Can I power down the XC7300 but still have the pins active, in order to save power? What if I power down only V_{CCINT} and leave V_{CCIO} powered?

A: No, neither is recommended. Both cases can cause a latchup condition. This is because the pin protection circuitry is connected to V_{CCINT}, and the device inputs cannot be driven above V_{CCINT} + 2V (which would be 2V if V_{CCINT} = 0V). If device pins are driven above V_{CCINT} + 2V, excess current will be drawn through the pins, potentially causing latchup.

Q: Can the XC7300 device pins be individually configured for 3.3V or 5V I/O operation?

A: No. All of the device pins are powered by a common set of V_{CCIO} pins. Therefore, all of the I/O pins are configured for either 3.3V or 5V operation.

Q: When V_{CCIO} is connected to a 3.3V supply, can the XC7300 devices drive/be driven by 5V logic?

A: Yes. The 3.3V I/O output levels are compatible with 5V TTL input levels. The XC7300 also can drive 5V CMOS inputs if pull-up resistors are used. The inputs can be driven by 5V TTL and CMOS logic, even when V_{CCIO} is powered by a 3.3V supply.

Q: Do the XC7300 devices require a special power-up sequence in a mixed voltage system?

A: No. Power can be applied to, and removed from, the V_{CCINT} and V_{CCIO} pins in any sequence. However, the voltage applied to the I/O pins of the device should not exceed V_{CCINT} + 0.5V at any time. ◆

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