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EPLD Application Guide
with XC7000 Data Sheets

April 1995

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Applications

Direct PAL Conversion Using Xilinx EPLDs

January 1995

Application Note

Introduction

In order to remain competitive in the marketplace, compa-nies are being driven to reduce product manufacturing costs while adding more features and improving reliability. Users of low density discrete PALs are turning to higher density erasable programmable logic devices (EPLDs) to meet these goals.

PALs are easy devices to use. Device timing is fixed, routing issues are nonexistent and the device architec-tures are simple and understandable. Many EPLDs how-ever, exhibit timing unpredictability, routing limitations, and limited functionality that can trap the unwary first-time EPLD user. Couple that with the task of learning how to use new design-entry software, and what appeared to be a simple task can turn into a nightmare.

This application note shows how Xilinx EPLDs can be used to simplify the task of reducing the number of discrete low density PALs on a board. This direct PAL conversion is made possible by a unique combination of :

- Architectural features
- Software methodology
- Broad product family

Xilinx EPLD Architecture

In order to support direct PAL conversion, Xilinx XC7000 EPLDs have a PAL-like architecture. Each device consists of several PAL-like logic blocks, called Function Blocks (FBs), on a single IC, all interconnected by a fully popu-lated switch matrix. Each FB can be thought of as a 21V9 PAL, with 21 complementary inputs and an AND-OR array with 57 product terms feeding 9 outputs.

The Xilinx EPLD Function Block is highly flexible superset of the low density PAL. The product term intensive FB has five individual product terms per output. In addition, there are 12 product terms that are shared between all 9 outputs. Each output can be configured as either registered or combinatorial. Each register has individual set, reset and output enable control and can be clocked either individu-ally or by global clocks. In addition, each output has an available XOR gate that can be used for XOR functions or toggle flip flop emulation.

Although product-term-intensive, the timing is fixed. No matter whether the output is performing a single product-term function or a 17 product-term function with the XOR gate, the timing doesn't change.

All of the Function Blocks on a Xilinx EPLD are intercon-nected by a fully populated Universal Interconnect Matrix (UIM™).

Unlike other vendor's sparsely populated matrices that create routing problems and have fanout-dependent tim-ing, the UIM is a fully populated, non-blocking switch matrix that features a constant delay, independent of fanout. Every Function Block output and every signal from every input and I/O pin all feed into the UIM. The UIM in turn drives every input of every FB. This means that each Function Block input can be driven by any input pin, any I/O pin and any Function Block output – just like connecting PALs on a board, but better.

In addition to serving as an interconnect, the UIM may also function as very wide input AND array. This allows the EPLD to generate product terms in the UIM similar to a low density PAL AND array. The propagation delay is fixed regardless of the number of signals used to generate the product term, or the source and destination of those signals.
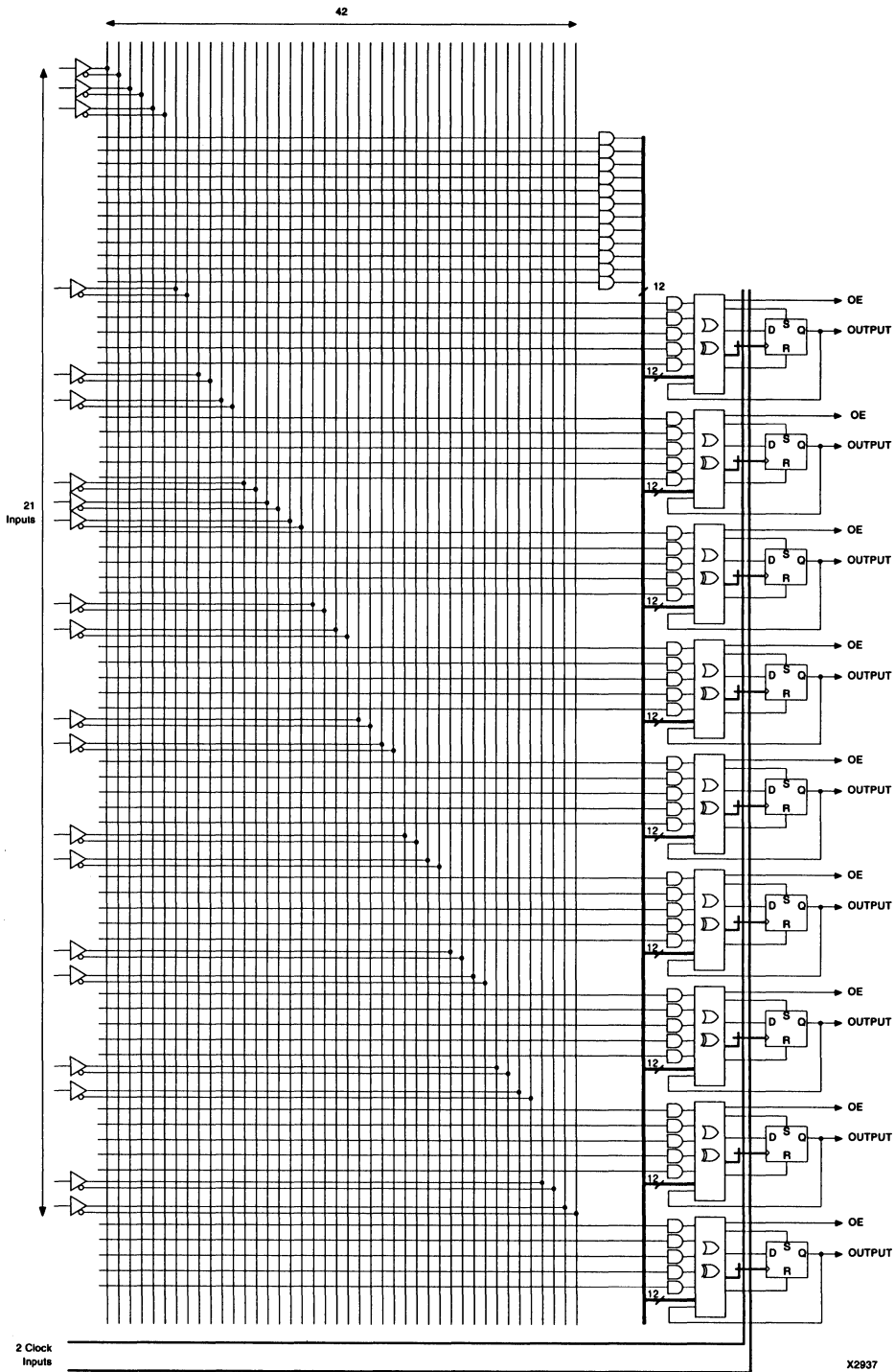
Figure 1. Xilinx EPLD PAL-Like Function Block
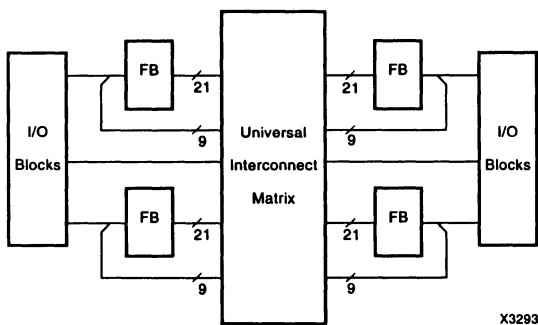
Figure 2. Universal Interconnect Matrix

Figure 4. I/O Block

The EPLD has programmable I/O blocks for driving the device pins. The I/O blocks can be used to decouple the Function Block's outputs from the device pins so the Function Block outputs may be buried while still retaining the use of the pin as a device input. The I/O blocks also provide output inversion control and the ability to latch and register input signals.

Xilinx EPLD Software

When it comes to programmable logic, silicon is only part of the solution. Software is required to translate ideas into reality. The Xilinx EPLD Translator (XEPLD™) works with industry standard PAL logic compilers and languages such as ABEL, CUPL and PALASM. One can directly import JEDEC files from old, proven designs using 22V10s and 20V8s.

The XEPLD system allows design entry with familiar front end tools. Once the design is entered, XEPLD simply acts as a fitter, taking the design description and mapping it into the chosen Xilinx EPLD.

In addition to being easy to use, XEPLD is very powerful. One of the most important functions of a fitter for high density programmable logic is Automatic Partitioning. The design can be entered without having to first partition it into Function Block-size pieces. This lets the designer concen-

trate on the functionality of the design, not its physical implementation.

The PAL Conversion Process

The PAL conversion process is begun by identifying which group of PALs are to be converted to a single EPLD. Then choose the appropriate Xilinx EPLD, based on the I/O and logic requirements. Xilinx makes this process easier by offering each device in a variety of footprint-compatible packages. This flexibility allows the designer to upgrade to a higher density device without having to change the board layout, should the logic requirements change.

Since the timing of the Xilinx EPLD is absolutely predictable, it is an easy matter to verify that the design will meet all critical timing requirements. By eliminating delays getting on and off chip, even 5 ns PALs can be converted to a single Xilinx EPLD.

The choice of whether to do equation-based design entry or schematic-based design entry is based primarily on the user's preference. Equation-based entry allows the user to concatenate PALASM equations from multiple PAL files without any restrictions on the PAL type.

On the other hand, schematic-based design entry may be easier to conceptualize, and it allows the user to directly

Figure 3. The 100% Interconnect
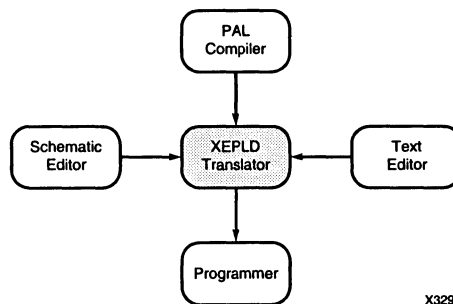
Figure 5. Development System Overview

```
DesignEntry Translate Fitter Verify Utilities Profile Quit

        FITEQM    (Integrate EPLD Behavioral Design)
        FITNET    (Integrate EPLD Schamatic Design)
        PALCONVT      (Convert PAL-based Design)

                  ΣΣ XILINX®
                     XACT®
                 Design Manager
                   Version: 5.0.0.
            Copyright 1989-1994 Xilinx Inc.
   386:DOS-Extender 4.1 – Copyright (C) 1986–1993 Phar Lap Software, Inc.

                   Press F1 for Help

    Family:    XC7300
    Directory:  C:\DESIGNS
    Part:      7354-10PC68
    Mouse:     MS Mouse

Cmd: _
```

X5613

Figure 6. Automatic PALCONVT Ulility Runs Under the Xilinx Design Manager
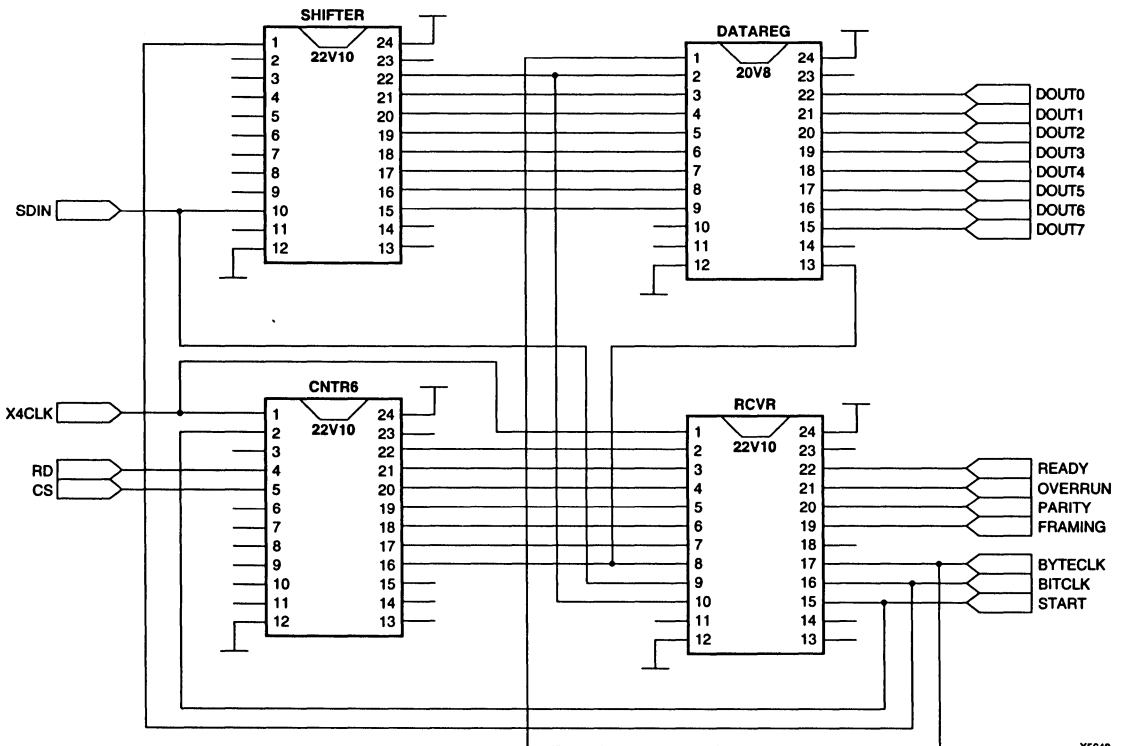
Figure 7. Original UART Design

X5648

PATTERN uartdemo.pld – file made by PALCNVT command

; Behavioral design example for XC7354-xxPC68
; Demo usage: fiteqn -e uartdemo -p 7354

CHIP uartdemo XEPLD

INCLUDE_EQN 'shifter.pld'
INCLUDE_EQN 'rcvr.pld'
INCLUDE_EQN 'datareg.pld'
INCLUDE_EQN 'cntr6.pld'

INPUTPIN SDIN X4CLK RD CS
OUTPUTPIN DOUT7 DOUT6 DOUT5 DOUT4 DOUT3 DOUT2 DOUT1 DOUT0

NODE D7 D6 D5 D4 D3 D2 D1 D0 C0 C1 C2 C3 C4 C5 PAR READ

; declarations added after palconvt:

outputpin start byteclk bitclk framing parity overun ready

EQUATIONS
; equations added after palconvt:

```
START.PRLD       = GND;
BITCLK.PRLD      = GND;
READY.PRLD       = GND;
BYTECLK.PRLD     = GND;
OVERUN.PRLD      = GND;
PAR.PRLD         = GND;
PARITY.PRLD      = GND;
FRAMING.PRLD     = GND;
```

Figure 8. Design File UARTDEMO.PLD

import JEDEC files for 22V10 and 20V8 PALs (PALASM equations may be used for other PAL types).

The following examples show how to use XEPLD to directly convert a multiple-PAL design to a single Xilinx EPLD. The examples show the use of both equation and schematic-based design entry methods. The design, shown in Figure 7, implements a UART originally implemented with three 22V10s and a single 20V8.

Equation-Based Design Entry
Direct PAL conversion is easily accomplished with a modular design approach. Each PAL in the design can be treated as an individual module. A Top-Level design file, created by the XEPLD PALCONVT utility simply links all of the modules together.

The design file UARTDEMO.PLD, shown in Figure 8, was created with PALCONVT. This file is written in PLUSASM, the XEPLD native syntax, and should look very familiar to those familiar with PALASM. The CHIP statement contains the filename of the Top-Level file and targets a Xilinx EPLD. INCLUDE_EQN keywords instruct XEPLD to concatenate the PALASM equations contained in each of the included files that were generated by the PAL compiler. INPUTPIN, OUTPUTPIN and NODE keywords then follow to define device inputs, outputs and nodes.

The EQUATIONS keyword indicates where the equations section of the design file begins. After reading this keyword, XEPLD reads all of the equations in the included files, automatically partitions the equations and converts the multiple-PAL design into a single chip solution. This design flow is illustrated in Figure 9.

For each PAL in the design, generate a PALASM2 Boolean equation file from the original PAL source code. This is easily done with the XEPLD utility PLA2EQNX (for ABEL) or the CUPL -c compiler option. At this time, verify that the signal names in each PAL pinlist establishes the proper signal connectivity for the design.

After generating the Boolean equation files, invoke XEPLD and do the following:

• Select the target device

    Open up the FAMILY menu and select the XC7300 device family. Then open up the PART menu and select the target Xilinx EPLD.

• Create the Top-Level file

    Use the FITTER -> PALCONVT command to create the Top-Level File, selecting the PAL equation files (.PLD or .PDS) that you want to link together with the Create new
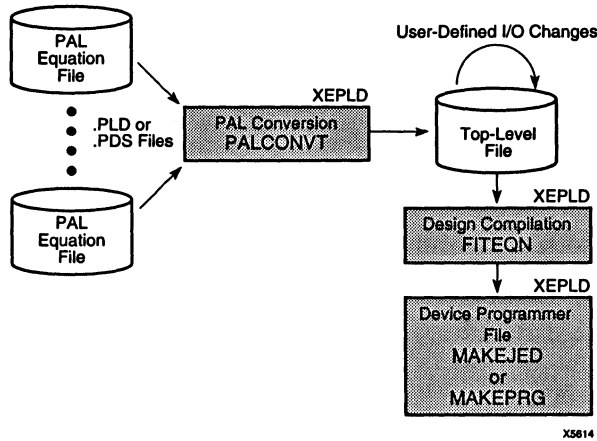
Figure 9. PAL File Conversion Diagram
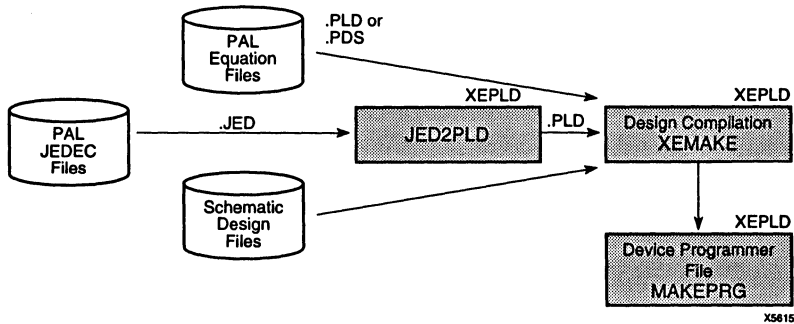
Figure 10. Schematic-Based Design Flow

PLD and PAL Interconnect option. Edit the pin declaration statements in the file to suit the design's I/O requirements.

- Fit the design

  Run FITTER -> FITEQN to implement the design in the target device.

- Generate the programming file

  Run VERIFY -> MAKEPRG to generate the Hex format programming file.

The device can now be programmed and the correct operation verified.

Schematic - Based Design Entry
The schematic design entry flow is also simple and straightforward. The XC7000 component library contains 22V10 and 20V8 PALs to simplify the PAL conversion process. It is a simple matter to connect the PALs exactly as in the original design and import JEDEC files that describe their functionality. For other PAL types, PLUS-ASM compatible PALASM2 Boolean equation files can be targeted at generic 20 and 24-pin PAL symbols in the XC7000 library. Instructions showing how to use ABEL, CUPL and PALASM to generate the required equation files appear in the Xilinx EPLD Handbook. XEPLD then processes the netlist and PAL files to convert the design to a single-chip solution. The design flow is illustrated in Figure 10.

After generating the proper files with a PAL compiler, use a schematic editor to capture the design. Assign the PLD=<file_name> attribute to each PAL in the schematic, linking it to an intermediate file describing its function. Save the design and process it as shown:

- **Import 22V10/20V8 JEDEC Files**
  Run TRANLATE -> JED2PLD for each JEDEC file in the design selecting the JEDEC file to import and the PAL type (22V10 or 20V8).

- **Compile the Design**

  Run TRANSLATE -> XEMAKE -> DONE. Select the name of the schematic with the Make Intelhex Bitmap option and assign an identifying signature, design.a.

XEPLD automatically processes the entire design, optimizing, partitioning, and mapping the logic into the target device, then generating a programming file with a unique identifying signature. The device can now be programmed, installed on the board and correct system operation verified.

Conclusion

This application note demonstrates how easy it is to directly convert PAL based designs to a single Xilinx XC7000 EPLD without any redesign. This direct PAL conversion process is only possible when the target device logic blocks have a PAL-like architecture, the interconnect matrix is fully populated, and chip timing is deterministic. All of these features are incorporated in the XC7000 EPLDs. The EPLD Translator software simplifies this task by interfacing directly to the most popular third party design tools.
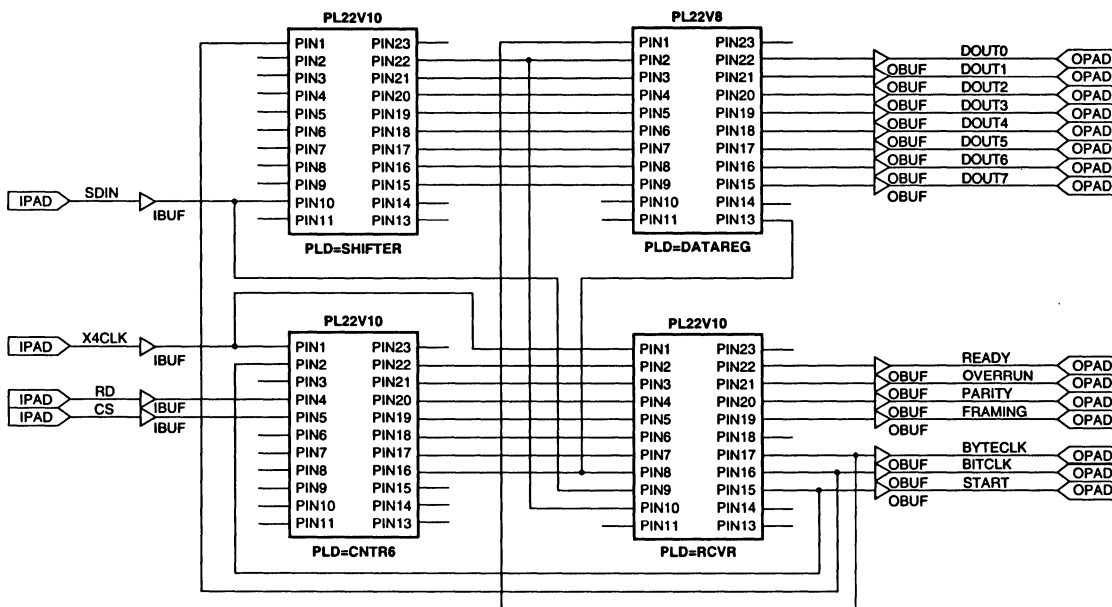
X5655

Figure 11. PAL_UART Schematic

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A Zero Wait State Synchronous DRAM Controller for the Pentium Microprocessor

March 1995   Application Note

Introduction

This application note presents a main memory subsystem solution for any speed grade Pentium microprocessor with a 66 MHz bus clock and is capable of supporting zero wait-state transfers. This is achieved without relying on a second level cache to improve system performance. Instead, this memory subsystem takes advantage of the Pentium's pipelined access mode and memory interleaving to achieve zero wait-state accesses.

The control logic required to implement the DRAM controller needs to be fast enough to run at the processor bus clock frequency and wide enough to decode signals from the both CPU and the two memory controller state machines (one for each bank of memory). The control logic must also have 3.3 V I/O capability to interface directly to the DRAM without additional buffers. In addition, to minimize the microprocessor's output signal loading, especially on the /ADS strobe, chip count needs to be minimized.

A 44-pin Xilinx XC7354-10 EPLD integrates the DRAM control functions into a single chip. This device has an internal cycle time of 77 MHz and features register delays compatible with both the Pentium microprocessor and synchronous DRAM. It's 3.3 V I/O can drive the synchronous DRAM directly, avoiding the delays introduced by external level-shifting buffers.

The DRAM address multiplexing and pipelining is handled by a 44-pin XC7318-7 EPLD. It's 3.3 V I/O and 24 mA drive make it well suited for driving the DRAM array address bus.

Before proceeding with the memory system description, a quick review of the Pentium and synchronous DRAM operation may be helpful to those readers not familiar with these devices.

Pentium Bus Operation

The Pentium processor is connected to the system through a synchronous bus that operates at up to 66 MHz. A bus cycle begins with the Pentium driving an address and asserting bus cycle definition pins with a valid address strobe and ends when the last burst ready signal is returned to indicate that the bus cycle is complete. A single read or write transfer takes two clock cycles to complete without any wait states. When performing cache fill or write back cycles the processor uses a burst transfer mechanism instead. The opening access of the burst transfer still takes two clock cycles, but the second, third and forth data transfer only take one clock each.

When accessing memory, the processor requires the memory controller to determine if the access will result in a burst transfer. If a burst transfer is performed, the memory controller is required to generate the burst addresses since the processor only provides the address for the opening access of the burst.

The Pentium also has the capability of pipelining accesses to improve memory system performance. Pipelining allows the memory subsystem to begin a new memory access while the previous memory access is still in progress. This feature reduces the latency required to perform the opening accesses of burst transfers.

In this design, the Pentium is connected to the EPLD through the address bus and cycle definition signals. The Pentium cycle definition signals used in this design are address strobe (/ADS), write/read (WRITE) and cacheability (/CACHE). The address bus and byte enables (BE[0:7]), are decoded to generate the correct DRAM access signals. The EPLD generates burst ready (/BRDY) to terminate the access and next address (/NA) to indicate that it is ready to begin a pipelined memory access.

Synchronous DRAM Operation

Synchronous DRAMs are designed for use in high-bandwidth main memory subsystems. They derive their high performance through the use of internal address pipelining, and are able to provide valid data on every rising clock edge after the clock latency period has elapsed. Unlike a standard DRAM however, an internal mode register must be initialized to control how the device operates before any memory accesses take place. In addition, these 3.3 V memories can't be directly driven by programmable logic with standard TTL and CMOS output levels. Their low voltage TTL inputs must be driven by logic that has LVTTL compatible I/O such as the Xilinx XC7000 devices.

These devices have a synchronous interface to the system with level sensitive strobes and address inputs that are sampled on rising clock edges. Data is also clocked into and out of the DRAM on rising clock edges. The address bus is multiplexed as on a standard DRAM but the addresses are clocked into the chip when the address strobes are sampled active. This means that the designer does not need to be concerned about maintain-

ing precise control of the timing relationships between the address strobes and address inputs or the write strobe and data. The designer need only ensure that the inputs meet the synchronous DRAM input setup and hold requirement.

The EPLD issues commands to the DRAM through four control inputs; row address strobe (/RAS), column address strobe (/CAS), write (/WE) and chip select (/CS). Although these signals have the same names as a conventional DRAM, they need only be sampled active for one clock cycle when commands are issued. The data mask inputs (DQM) control the output buffers during read cycles and data masks during write cycles. The clock enable (CKE) is not used in this design.

Memory Subsystem Performance

Simulation studies by Intel show that Pentium performance during cache fills is more sensitive to wait states incurred during burst read transfers than to wait states incurred during the opening transfer of the burst. This is because every wait state incurred while bursting affects three transfers and has a larger impact on bus utilization than the wait states that occur once during the opening transfer.

Compared to read cycles, the Pentium's in-system performance was observed to be much less sensitive to wait states during write cycles. However, if a DMA controller is present in the system, wait states during each transfer of a block write operation could have a significant impact on system performance.

Therefore, this memory subsystem was designed to perform zero wait accesses for both read and write burst transfers. The latencies incurred during the opening access of each burst cycle could be partially, and in some cases completely, hidden by taking advantage of the processor's pipelined access capability. Thus, pipelined burst reads by the CPU and pipelined DMA burst reads and writes can be completed in as little as five clock cycles as shown in Table 1.

Table 1. Memory System Performance

Cycle Type	Clocks
Burst Read Cycle	9-1-1-1
Pipelined Burst Read (Alternate Bank)	2-1-1-1
Burst Write	4-1-1-1
Pipelined Burst Write (Alternating Bank)	2-1-1-1

Memory Subsystem Overview

A block diagram of the memory subsystem is shown in Figure 1. The 16 MByte DRAM memory array consists of eight byte wide synchronous DRAM. These 16MBit devices are organized internally as two 1Mx8 banks. Since each bank can be accessed independently through common address and data pins, external address latches and data path multiplexors are not required when implementing a two-bank interleaved system.

The registered DRAM address multiplexor logic multiplexes and pipelines the DRAM row and column addresses during normal accesses as well as generating the proper DRAM addresses during the DRAM mode register write cycle. This is a good example of the I/O intensive high performance applications that the 44-pin XC7318 was designed for.

The DRAM controller was implemented in a single 44-pin XC7354. The DRAM controller logic contains two independent DRAM control state machines; one state machine for each memory bank. These state machines share common CPU inputs and control the DRAM through shared output control signals, however they allow each bank of DRAM to be accessed independently of the other. One of the state machines also is responsible for performing the DRAM mode register write cycle after system reset. In addition to controlling the DRAM, this logic also generates the CPU Next Address signal to support address pipelining and consolidates the system's /BRDY inputs for the CPU.

Registered '646 type transceivers were used to pipeline data between the DRAM array and the CPU. Although this introduces one additional period of clock latency, this permits the data path logic to complete each data transfer in one clock while bursting.

DRAM Controller Overview

The DRAM controller consists of two independent state machines, a set of internal flags and a registered output decoder, and as shown in Figure 2. The two state machines share control of a single set of registered outputs that decode each machine's state bits, cycle termination signals and data masks. The nine flags control inter-state-machine communication and latch memory access requests, refresh cycle requests, and CPU cycle definition signals as shown in Table 2.

The ABEL-HDL code in Appendix A contains comments that completely describe the internal operation of the DRAM controller. The design files, compressed into XAPP049A.ZIP are also available on the Xilinx BBS.

Memory Access Descriptions

Several types of memory accesses are illustrated to show how the Pentium, DRAM controller and synchronous memory work together in this memory subsystem. Timing diagrams are used to show waveforms as well as the internal states of the memory controller state machines.
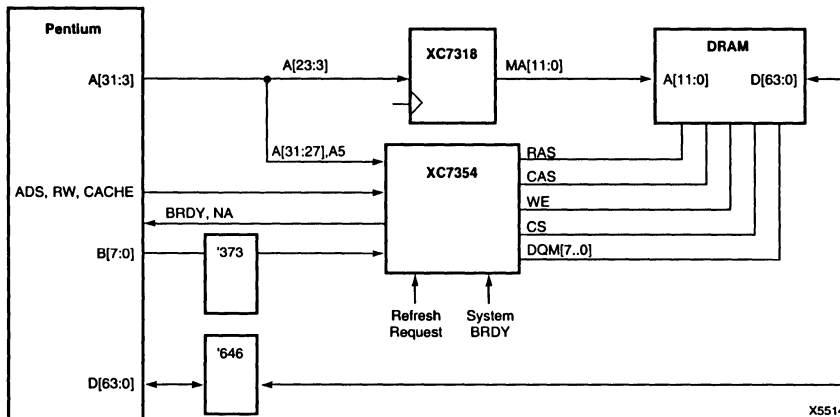
Figure 1. Memory System Block Diagram

Memory Configuration Cycle

Unlike conventional DRAM, an internal mode register must be loaded to configure the DRAM for the desired operating characteristics. The DRAM was configured for a CAS latency of three clock cycles, and an interleaved address wrap and a four transfer burst to conform to the Pentium address wrap sequence and burst length. The mode register contents to be loaded are shown in Figure 3.

Figure 2. DRAM Controller Block Diagram

Figure 3. Mode Register Contents

When the DRAM mode register address space is accessed by the CPU, the DRAM controller precharges both memory banks, then asserts the appropriate control signals to load the mode register as shown in Figure 4. During the memory precharge command, DRAM address bit A10 must be a 1 to precharge both banks of memory, however a 0 must be loaded into A10 of the mode register. The DRAM controller uses the address multiplexor to manipulate this address bit during the memory configuration cycle.

Once the memory configuration cycle is complete, the controller asserts /BRDY to terminate the CPU bus access. The memory controller is now ready to respond to memory access and refresh requests.

Table 2. DRAM Controller Flags

Flag	Definition
Rfrq	Refresh Request
BankA_Pending BankB_Pending	Latched CPU Access Request
BankA_Write, BankA_Cache BankB_Write, BankB_Cache	Identifies Read/Write and Burst Read/Write Access Start
WaitA WaitB	State Machine Wait State Outputs Used to Defer Access Start
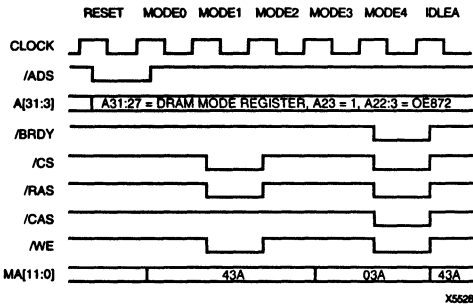
Figure 4. Memory Configuration Cycle

Read Cycles

The Pentium performs a four transfer burst access when filling its on-chip cache as shown in Figure 5. If the memory bank is already precharged the access takes twelve clock cycles. However, the controller is ready to start a pipelined memory access after only five clock cycles have elapsed. By interleaving accesses between memory banks, a pipelined cache fill can be completed without any wait-states as shown in Figure 6.
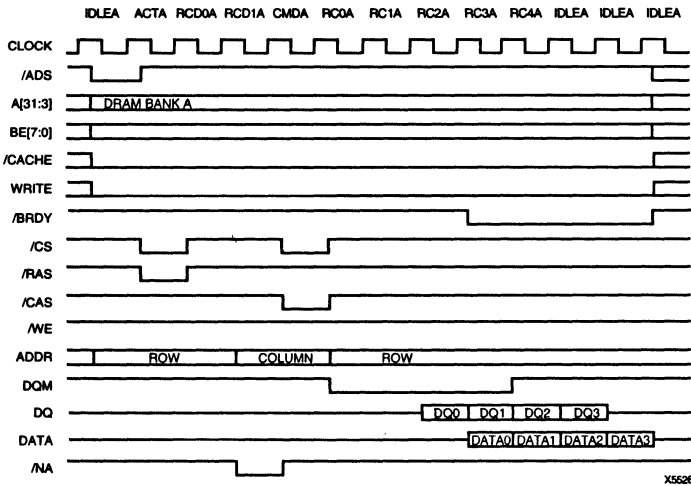
Figure 5. Pentium Burst Read Access
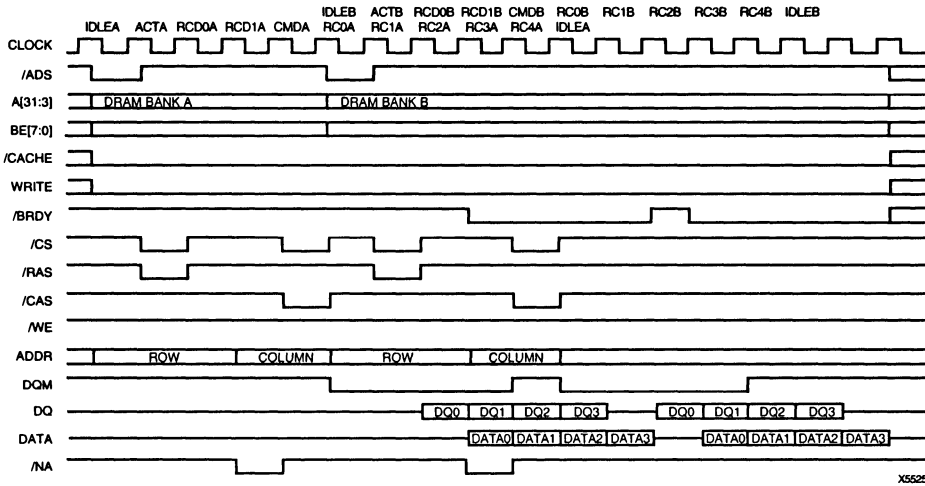
Figure 6. Pentium Pipelined Cache Fill
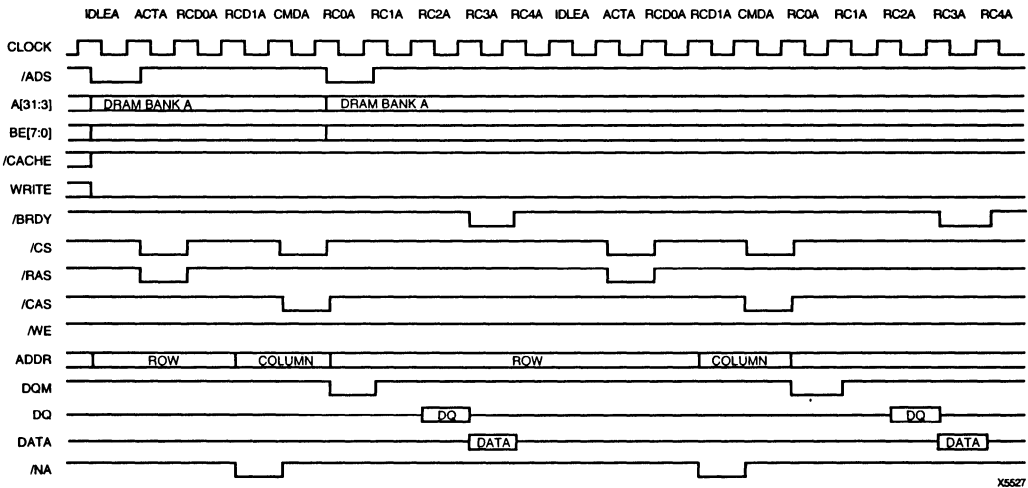
Figure 7. Pentium Single Read/Single Read Access (Same Bank)

With the memory banks divided on 32 byte boundaries to maximize burst transfer performance, pipelined single data reads may have a higher likelihood of hitting the same bank as shown in Figure 7. However, if the alternate bank is hit the access takes only five clock cycles as shown in Figure 8.
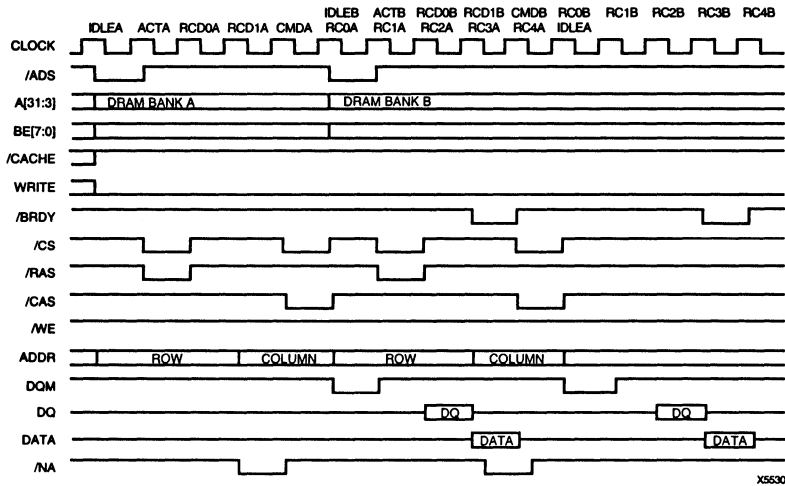
Figure 8. Pentium Single Read/Single Read Access (Alternate Bank)
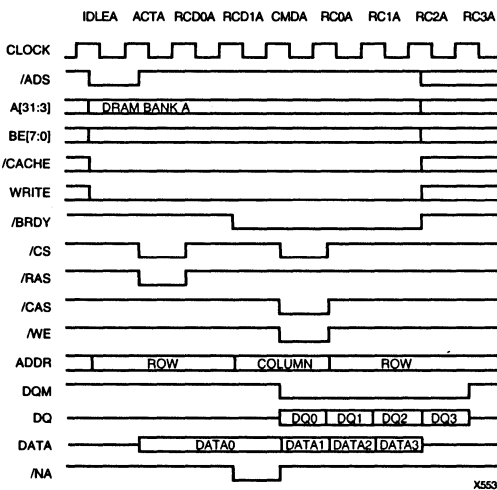
Figure 9. Pentium Burst Write Access

Write Cycles

The Pentium also performs four transfer burst write cycles when writing back the contents of its on-chip cache to the main memory. If the memory bank is already precharged this takes seven clock cycles as shown in Figure 9.

The Pentium processor will not pipeline write cycles into write cycles. However, if the system DMA controller performs pipelined burst write accesses, each access can be completed in as few as five clock cycles as shown in Figure 10.
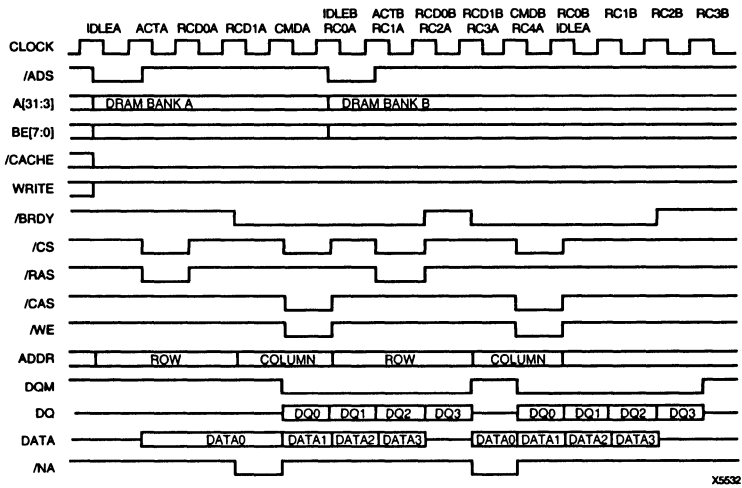
Figure 10. DMA Pipelined Burst Write/Burst Write Access (Alternating Banks)
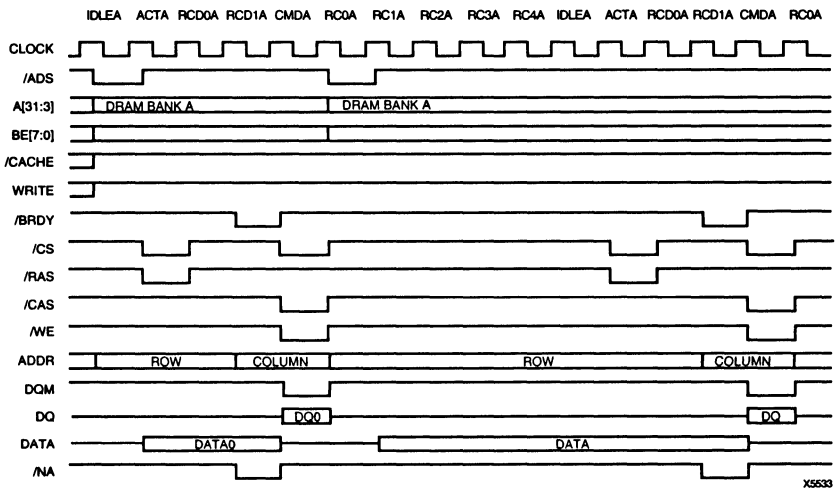
Figure 11. Pentium Single Write/Single Write Access (Same Bank)

With the memory banks divided on 32 byte boundaries to maximize burst transfer performance, pipelined single data writes may have a higher likelihood of hitting the same bank as shown in Figure 11. However, if the alternate bank is hit the access takes only five clock cycles as shown in Figure 12.

Figure 12. Pentium Single Write/Single Write Access (Alternating Bank)

Figure 13. Pentium Burst Read/Single Write Access (Pipelined, Alternating or Same Bank)

Read/Write and Write/Read Cycles

Examples of write cycles that follow read cycles are shown in Figures 13, 14 and 15. Examples of read cycles that follow write cycles are shown in Figures 16, 17, 18 and 19.
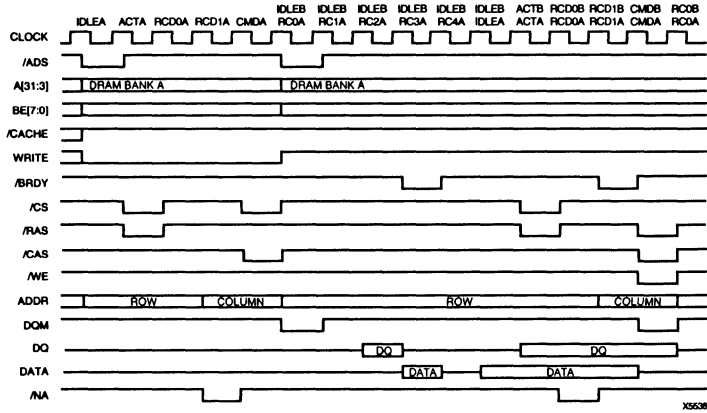
Figure 14. Pentium Single Read/Single Write Access (Pipelined, Same Bank)
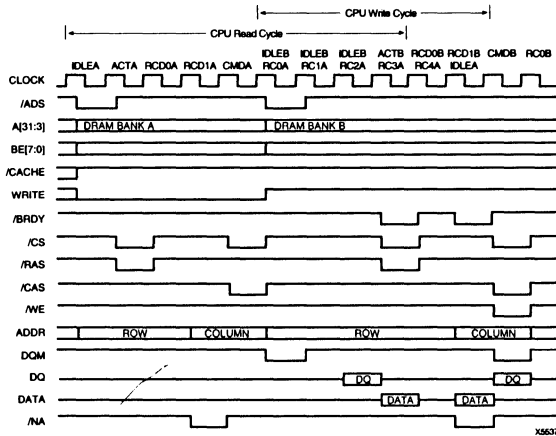
Figure 15. Pentium Single Read/Single Write Access (Pipelined, Alternating Banks)
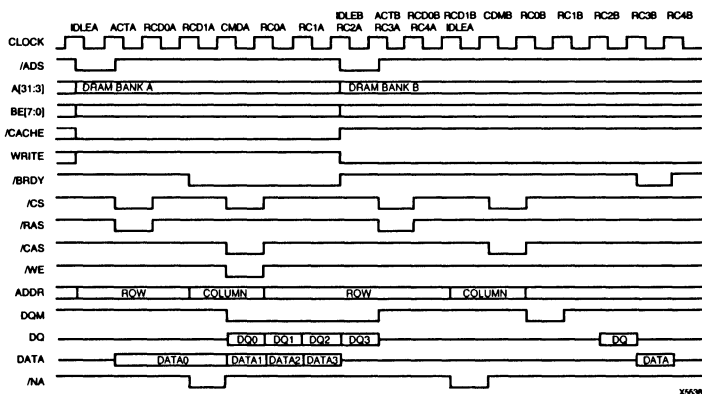
Figure 16. Pentium Burst Write/Single Read Access (Alternating Bank)
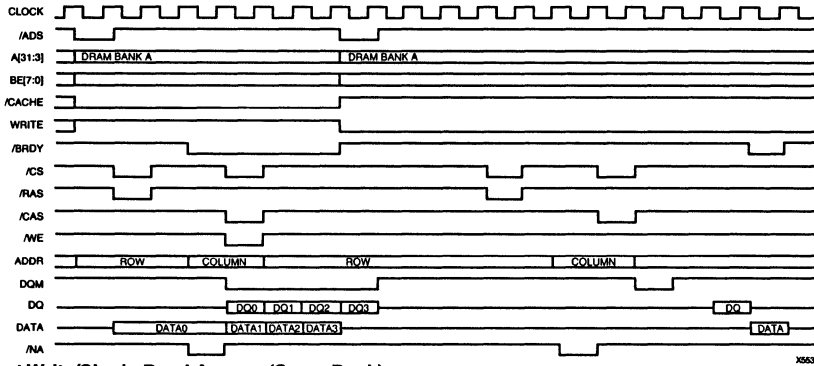
17. Pentium Burst Write/Single Read Access (Same Bank)
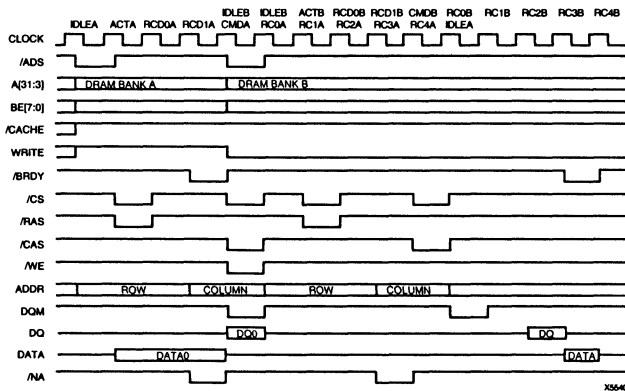
Figure 18. Pentium Single Write/Single Read Access (Alternating Bank)
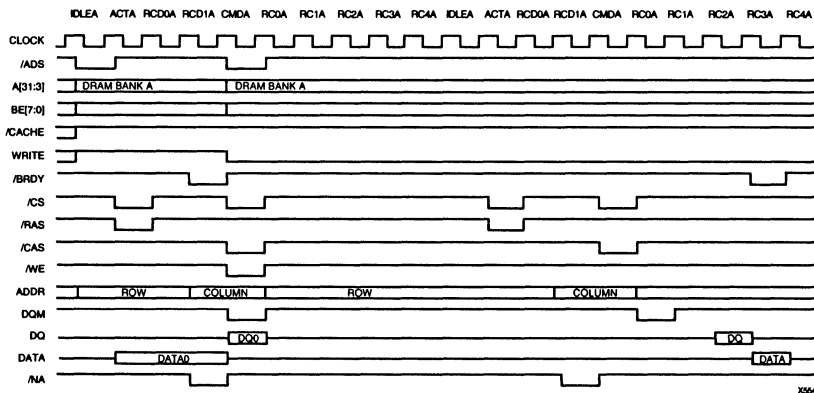
Figure 19. Pentium Single Write/Single Read Access (Same Bank)

Refresh Cycle

The DRAM controller accepts refresh requests from an off-chip refresh timer. The controller latches the external refresh request and synchronizes it before it is sampled by the Bank B state machine. The state machine arbitrates between the refresh and access request, servicing the access request after the refresh cycle has been performed as shown in Figure 20.

IDLEA RFSH0 RFSH1 RFSH2 RFSH3 RFSH4 RFSH5 RFSH6 RFSH7 RFSH8 IDLEA ACTA

CLOCK

/ADS

RFRQ

/CS

/RAS

/CAS

/WE

X5544
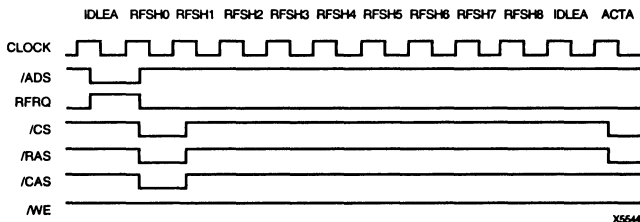
Figure 20. Refresh Cycle

Design Considerations

Xilinx EPLDs are optimized for designs that require very high speed logic paths and complex state machines. To meet the different speed/density requirements of the these functions, the Xilinx XC7354 features two different types of logic blocks on a single IC. This Dual-Block™ architecture combines High Density Function Blocks optimized for density, and simpler Fast Function Blocks (driven directly from Fast Input pins) optimized for speed, on the same device. By featuring multiple types of logic blocks on a single device with a 100% populated switch matrix that guarantees 100% routing with 100% utilization, the Xilinx EPLD avoids the classical trade-offs of speed vs. density vs. routing resources.

This section discusses the design's timing requirements and design considerations. It shows how best to take advantage of the Xilinx XC7000 Dual-Block architecture to meet those requirements. Timing information is based on the worst case AC specifications for the XC7354-10 published in the 1994 Xilinx Programmable Logic Data Book. Timing information for the Pentium is taken from the 1993 Pentium Processor User's Manual.

Table 3. Data Sheet Timing Parameters

Device	t_{SU}	t_{CO}
Pentium-66	5.0	8.0
XC7354-10	5.0	8.0
XC7318-7	4.0	5.5

Critical Timing Parameters

To interface with the Pentium, the register delays of the programmable logic must be Pentium compatible. Since the Pentium address and control signals used in this design become valid 8 ns after the rising edge of clock, the system has only 7 ns to recognize these signals on the next clock edge. The Pentium requires that its /BRDY and /NA inputs be valid 5 ns and 4.5 ns, respectively, before the rising edge of clock leaving the system 10 ns (including board trace delays) to generate these control signals.

Clock

Pentium Address and Control Outputs

|— 15 ns —|
|— 8 ns —|— 7 ns —|
Pentium t_{CO}

Clock

System /BRDY and /NA Outputs

|— 15 ns —|
|—10 ns—|— 5 ns—|
Pentium t_{SU}

X5542
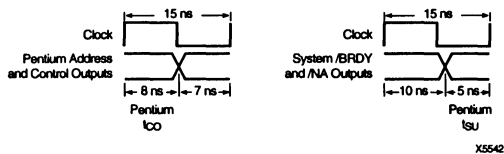
Figure 21. Pentium Requirements for Control Path Timing

Synchronous DRAM features fast setup times for both control and data inputs. The XC7354-10 supplied control signals are available no later than 10 ns after the rising edge of clock. This allows 5 ns for trace delay and DRAM t_{SU} which means the XC7354-10 is compatible with synchronous DRAM timing requirements.

Handling of Critical Signals

In many designs, there are only a limited number of critical input and/or output signals. Critical signals are easily flagged by using property statements in the ABEL-HDL code. The software then automatically assigns critical input signals to the Fast Input pins, and partitions the critical logic functions into the Fast Function Blocks.

The critical DRAM controller input signals in this design are the Pentium address lines, /ADS strobe and WRITE. The DRAM controller needs to decode the Pentium address lines and the /ADS strobe within one clock cycle to detect an access to the DRAM address space. The bank state machines also need to sample the WRITE signal during the first clock cycle to determine if the requested access can potentially conflict with another access that may be in progress.

Clock

System Control Outputs

|— 15 ns —|
|— 10 ns —|— 5 ns|
Trace delay and DRAM t_{SU}

X5543
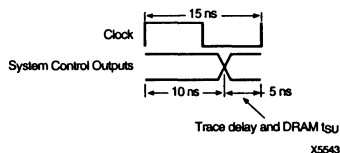
Figure 22. Synchronous DRAM Timing Requirements

To minimize setup to clock for these signals, they are assigned to the Fast Input pins and the state bits and DRAM strobes that sample these signals in the first clock cycle are assigned to the Fast Function Blocks. Fast Input setup to clock on the XC7354-10 is 5 ns, however one additional ns is required in this design because some of the logic functions assigned to the Fast Function Blocks require product terms from adjacent Macrocell. This allows 1ns for chip-to-chip delay.

The critical DRAM controller output signals are the Pentium /BRDY and /NA inputs and the registered multiplexor row/column select line. These functions are assigned to Fast Function Blocks to take advantage of their 8 ns clock to output delay. This allows 2 ns for chip-to-chip delay between the DRAM controller and the Pentium, and 4 ns between the DRAM controller and the multiplexor.

Not all of the state machine bits are critical in this design. States were assigned in a way that only two state bits from each state machine make transitions based on Fast Inputs. This gives the software the freedom to map the other state bits into the more product-term intensive High Density Function Blocks. This state assignment technique takes full advantage of the Dual Block architecture for product term intensive state machines that require fast register setup times.

Likewise, only the DRAM /RAS and /CS strobes need to make transitions based on Fast Inputs. The remaining DRAM control signals can be mapped into the High Den-sity Function Blocks. Their 10 ns clock to output still allows 2.5 ns for chip to chip delays between the DRAM controller and the DRAM.

Conclusion

High performance memory subsystems for the Pentium do not require expensive, power hungry second level caches. Systems based on synchronous DRAM using 3.3 V I/O compatible Xilinx 7000 EPLDs for the control function enable the designer to implement a cost effective, high performance system with a minimum of components.

The Xilinx Dual Block architecture features logic blocks optimized for the critical paths of a Pentium memory subsystem, and logic blocks dense enough to implement two memory controllers, one for each bank of memory, in a single 44-pin device. This control logic supports the high performance access modes of both the Pentium and synchronous DRAM.

References

Intel Corporation, *Pentium™ Processor User's Manual*, 1993

Ghaznavi, Raheel, *An Example Memory Subsystem for the Pentium™ Microprocessor*, Application Note AP-478,1993, Intel Corporation, Santa Clara, CA.

Xilinx, Inc., *The Programmable Logic Data Book*,1994

Appendix A

Module Pentium

"

 title 'Synchronous DRAM Controller for Pentium';

pentium device;

plusasm property 'partition ffb ras cs banka_pending bankb_pending banka0';
plusasm property 'partition ffb banka1 bankb0 bankb4 brdy na';
plusasm property 'inputpin (fi) ads a31 a30 a29 a28 a27 a5 write';

" Inputs

clock	pin; " 66MHz system clock
ads	pin; " Pentium address strobe
a31,a30,a29,a28,a27,a5	pin; " Pentium address signals
be0,be1,be2,be3,be4,be5,be6,be7	pin; " Pentium byte enables
write	pin; " Pentium write signal
cache	pin; " Pentium cache signal
"brdrst	pin; Board reset
refresh	pin; " Refresh timer refresh request
brdy_in	pin; " System burst ready input to controller

" Outputs

ras,cas,we,cs	pin istype 'reg';	" DRAM control signals
dqm0,dqm1,dqm2,dqm3	pin istype 'reg';	" DRAM data mask signals
dqm4,dqm5,dqm6,dqm7	pin istype 'reg';	
mux	pin istype 'reg';	" address mux control
brdy	pin istype 'reg';	" Pentium ready signal
na	pin istype 'reg';	" Pentium next address

" Nodes

banka_pending	node istype 'reg';	" DRAM bank A access request pending flag
bankb_pending	node istype 'reg';	" DRAM bank B access request pending flag
banka_write	node istype 'reg';	" Identify DRAM bank A write cycle
bankb_write	node istype 'reg';	" Identify DRAM bank B write cycle
banka_cache	node istype 'reg';	" Identify DRAM bank A burst cycle
bankb_cache	node istype 'reg';	" Identify DRAM bank B burst cycle
waita	node istype 'reg';	" Wait for bank A
waitb	node istype 'reg';	" Wait for bank B
banka0,banka1,banka2,banka3	node istype 'reg';	" Bank A state bits
bankb0,bankb1,bankb2	node istype 'reg';	" Bank B state bits
bankb3,bankb4	node istype 'reg';	
brdya_extend	node istype 'reg';	" Extend brdy for one " clock during burst " read cycles
brdyb_extend	node istype 'reg';	" Extend brdy for one " clock during burst " read cycles
brdya	node istype 'reg';	" bank A brdy
brdyb	node istype 'reg';	" bank B brdy
dqma,dqmb	node istype 'reg';	" data mask enables
sync_refresh	node istype 'reg';	" Syncs refresh input
rfrq	node istype 'reg';	" Refresh flag

" Variables
" State bit fields, bank addresses and DRAM mode register address

banka_state	= [banka3,banka2,banka1,banka0];
bankb_state	= [bankb4,bankb3,bankb2,bankb1,bankb0];
banka	= a31 & a30 & a29 & !a28 & !a27 & !a5;
bankb	= a31 & a30 & a29 & !a28 & !a27 & a5;
mode	= a31 & a30 & a29 & !a28 & a27 & a5;

"BANK A State Bit Definition

reseta	= [1,1,1,1];
mode0	= [1,0,0,1]; "[1,1,1,0];
mode1	= [1,1,0,0];
mode2	= [1,1,0,1];
mode3	= [1,1,1,0]; "[1,0,0,1];
mode4	= [1,0,1,1];
idlea	= [1,0,1,0];
acta	= [1,0,0,0];
rcd0a	= [0,0,0,0];
rcd1a	= [0,0,0,1];
cmda	= [0,0,1,1];
rc0a	= [0,0,1,0];
rc1a	= [0,1,1,0];
rc2a	= [0,1,0,0];
rc3a	= [0,1,0,1];
rc4a	= [0,1,1,1];

* BANK B State Bit Definition

```
     idleb    = [1,1,1,1,1];
     actb     = [1,1,1,1,0];
     rcd0b    = [1,1,1,0,0];
     rcd1b    = [1,1,1,0,1];
     cmdb     = [1,1,0,0,1];
     rc0b     = [1,1,0,1,1];
     rc1b     = [1,1,0,0,0];
     rc2b     = [1,0,0,0,0];
     rc3b     = [1,0,0,0,1];
     rc4b     = [1,0,0,1,1];
     rfsh0    = [0,1,1,1,0];
     rfsh1    = [0,1,1,0,0];
     rfsh2    = [0,1,1,0,1];
     rfsh3    = [0,1,0,0,1];
     rfsh4    = [0,1,0,1,1];
     rfsh5    = [0,1,0,0,0];
     rfsh6    = [0,0,0,0,0];
     rfsh7    = [0,0,0,0,1];
     rfsh8    = [0,0,0,1,1];
```

* Refresh request clear flag
clr_rfrq   = (bankb_state == rfsh8);   * Clear refresh flag when
                                          * refresh cycle is completed

```
@dcset
state_diagram banka_state;
```

* This state machine controls the DRAM mode load and bank A access cycles.

* The board reset signal puts the state machine in the RESET state. It then
* waits until the Pentium performs an access to the DRAM's mode control
* register. When an access to the register is detected, the state machine
* will precharge both memory banks before asserting the mode load command to
* the DRAM, then cycle through to the IDLE state for normal operation. Once
* the mode load sequence has been run, access requests and refresh requests
* will be honored.

* Accesses start if Pentium requests an access or there is a request pending.
* The access will be deferred if there is a refresh request pending or if
* the reqested access is a write cycle and the other bank is performing one of
* three cycles. If the other bank is performing a burst read, then the access
* will not start until the other bank has entered the IDLE state. If the other
* bank is performing a single read, then the access will not start until the
* other bank has entered state RC2. If the other bank is performing a single
* write, then the access will not start until the other bank has entered state
* RC0. Once the access starts, the state machine will run through
* the access sequence without stopping, then return to the IDLE state.

```
state reseta:
 if !lads & mode then mode0;
 else reseta;

state mode0: goto mode1;
state mode1: goto mode2;
state mode2: goto mode3;
state mode3: goto mode4;
state mode4: goto idlea;

state idlea:
 if (!lads & banka # !banka_pending) & !rfrq & !(!waitb & write)
    then acta;
      else idlea;
```

```
state acta:  goto rcd0a;
state rcd0a: goto rcd1a;
state rcd1a: goto cmda;
state cmda:  goto rc0a;
state rc0a:  goto rc1a;
state rc1a:  goto rc2a;
state rc2a:  goto rc3a;
state rc3a:  goto rc4a;
state rc4a:  goto idlea;

state_diagram bankb_state;

" This state machine controls the DRAM refresh and bank B access cycles.
" The board reset signal puts the state machine in the RESET state.
" It then waits until the bank A state machine has completed it's mode load
" sequence and entered the IDLEA state. Once the bank A state machine has
" entered IDLEA, this state machine can honor any pending refresh requests.
" Accesses start if Pentium requests an access or there is a request pending.
" The access will be deferred if there is a refresh request pending or if
" the reqested access is a write cycle and the other bank is performing one of
" three cycles. If the other bank is performing a burst read, then the access
" will not start until the other bank has entered the IDLE state. If the other
" bank is performing a single read, then the access will not start until the
" other bank has entered state RC2. If the other bank is performing a single
" write, then the access will not start until the other bank has entered state
" RC0. Once the access starts, the state machine will run through
" the access sequence without stopping, then return to the IDLE state.

state idleb:
 if rfrq & (banka_state == idlea) then rfsh0;
else if (!ads & bankb # !bankb_pending) & !rfrq & !(!waita & write)
    then actb;
      else idleb;

state actb:  goto rcd0b;
state rcd0b: goto rcd1b;
state rcd1b: goto cmdb;
state cmdb:  goto rc0b;
state rc0b:  goto rc1b;
state rc1b:  goto rc2b;
state rc2b:  goto rc3b;
state rc3b:  goto rc4b;
state rc4b:  goto idleb;

state rfsh0: goto rfsh1;
state rfsh1: goto rfsh2;
state rfsh2: goto rfsh3;
state rfsh3: goto rfsh4;
state rfsh4: goto rfsh5;
state rfsh5: goto rfsh6;
state rfsh6: goto rfsh7;
state rfsh7: goto rfsh8;
state rfsh8: goto idleb;

equations

" Define Flags and Status Bits

" The refresh request flag is set by external refresh requests. The external
" signal is synchronized with an input pad register by the optimization
" software. The flag is cleared when the refresh cycle is completed.

sync_refresh := refresh;
sync_refresh.ck = clock;

rfrq := sync_refresh
    # rfrq & !clr_rfrq;
rfrq.ck = clock;

" The bank pending bits capture Pentium access request signals. If the
" bank state machine is in the IDLE state, the access will start without
" waiting another clock for the pending bit to go true. But if the state
```

```
* machine is in another state, the pending bit will start another access
* cycle once the state machine returns to the IDLE state.
* The pending bits will be cleared when the access begins.

!banka_pending := !ads & banka
        # !banka_pending & !(banka_state == acta);
 banka_pending.ck = clock;

!bankb_pending := !ads & bankb
        # !bankb_pending & !(bankb_state == actb);
 bankb_pending.ck = clock;
```

```
* There are two status bits required for each bank to identify the type of
* access cycle being run. The access bits are driven by the WRITE and CACHE
* inputs and are used to identify read/write and burst read/write accesses.
* for the cycle in progress.

* The write status bits remain valid through state RC4. They are driven high
* when the IDLE state is entered and remain high until they are updated
* by the bank state machine. When the write status bits are high, the other
* bank is free to start its access.

* The cache status bits remain updated until the next access is started
* because they are used to extend brdy during burst read cycles.

* Since the status bits are not updated until the bank state machines are
* in the ACT state, input setup time to clock is not an issue even if these
* bits are not mapped into FFBs.
```

```
banka_write := (banka_state == rc4a)                    * Cycle done
        # (banka_state == idlea)                        * Keep it high
        # write & (banka_state == acta)                 * Update flag
        # banka_write & ((banka_state == rcd0a)         * and keep it valid
                #(banka_state == rcd1a)                 * until access is
                #(banka_state == cmda)                  * completed
                #(banka_state == rc0a)
                #(banka_state == rc1a)
                #(banka_state == rc2a)
                #(banka_state == rc3a));

banka_write.ck = clock;

banka_cache := cache & (banka_state == acta)            * Update flag
        # banka_cache & ((banka_state == rcd0a)         * and keep it valid
                #(banka_state == rcd1a)                 * until next access
                #(banka_state == cmda)                  * starts
                #(banka_state == rc0a)
                #(banka_state == rc1a)
                #(banka_state == rc2a)
                #(banka_state == rc3a)
                #(banka_state == rc4a)
                #(banka_state == idlea));

banka_cache.ck = clock;

bankb_write := (bankb_state == rc4b)                    * Cycle done
        # (bankb_state == idleb)                        * Keep it high
        # write & (bankb_state == actb)                 * Update flag
        # bankb_write & ((bankb_state == rcd0b)         * and keep it valid
                #(bankb_state == rcd1b)                 * until access is
                #(bankb_state == cmdb)                  * completed
                #(bankb_state == rc0b)
                 #(bankb_state == rc1b)
                #(bankb_state == rc2b)
                #(bankb_state == rc3b));
bankb_write.ck = clock;
```

```
bankb_cache := cache & (bankb_state == actb)                          " Update flag
      # bankb_cache & ((bankb_state == rcd0b)                         " and keep it valid
                  #(bankb_state == rcd1b)                             " until next access
                  #(bankb_state == cmdb)                             " starts
                  #(bankb_state == rc0b)
                  #(bankb_state == rc1b)
                  #(bankb_state == rc2b)
                  #(bankb_state == rc3b)
                  #(bankb_state == rc4b)
                  #(bankb_state == idleb));
bankb_cache.ck = clock;
```

" Define Bank State Machine Wait Signals
" WAITA and WAITB are used by each state machine to control when the other
" state machine is permitted to start its access cycle. If a write access is
" requested, the access will not start until the other bank has reached a
" certain point when performing any one of 3 types of cycles.

" If the other bank is performing a burst read, then the access
" will not start until the other bank has entered the IDLE state. If the other
" bank is performing a single read, then the access will not start until the
" other bank has entered state RC2. If the other bank is performing a single
" write, then the access will not start until the other bank has entered state
" RC0.

```
waita := !banka_write & !banka_cache & ((banka_state == cmda)        " wait for
                  #(banka_state == rc0a)                             " burst read
                  #(banka_state == rc1a)
                  #(banka_state == rc2a)
                  #(banka_state == rc3a))
      # !banka_write & banka_cache & ((banka_state == cmda)          " wait for
                  #(banka_state == rc0a))                            " single read
      # banka_write & banka_cache & (banka_state == rcd1a);          " wait for
                                                                     " single write

waita.ck = clock;

waitb := !bankb_write & !bankb_cache & ((bankb_state == cmdb)        " wait for
                  #(bankb_state == rc0b)                             " burst read
                  #(bankb_state == rc1b)
                  #(bankb_state == rc2b)
                  #(bankb_state == rc3b))
      # !bankb_write & bankb_cache & ((bankb_state == cmdb)          " wait for
                  #(bankb_state == rc0b))                            " single read
      # bankb_write & bankb_cache & (bankb_state == rcd1b);          " wait for
                                                                     " single write

waitb.ck = clock;
```

" Define DRAM Control Signals
" RAS is pulsed low for bank active, refresh and mode load commands
```
!ras := (banka_state == idlea) & (!ads & banka # !banka_pending)     " A access
          & !rfrq & !(!waitb & write)
      # (bankb_state == idleb) & (!ads & bankb # !bankb_pending)     " B access
          & !rfrq & !(!waita & write)
      # rfrq & (banka_state == idlea) & (bankb_state == idleb)       " Refresh
      # (banka_state == mode0)                                       " Precharge
      # (banka_state == mode3);                                      " and Mode
                                                                     " Load


ras.ck = clock;
```

" CS is pulsed low for all DRAM commands
```
!cs := (banka_state == idlea) & (!ads & banka # !banka_pending)      " A access
          & !rfrq & !(!waitb & write)
      # (bankb_state == idleb) & (!ads & bankb # !bankb_pending)     " B access
          & !rfrq & !(!waita & write)
      # (banka_state == mode0)                                       " Precharge &
      # (banka_state == mode3)                                       " Mode Load
      # rfrq & (banka_state == idlea) & (bankb_state == idleb)       " Refresh
      # (banka_state == rcd1a)                                       " Command A
      # (bankb_state == rcd1b);                                      " Command B
```

cs.ck = clock;

* CAS is pulsed low for read/write, refresh and mode load commands
!cas := (banka_state == rcd1a)   * Command A
    # (bankb_state == rcd1b)   * Command B
    # rfrq & (banka_state == idlea) & (bankb_state == idleb)   * Refresh
    # (banka_state == mode3);   * Mode Load
cas.ck = clock;

* WE is pulsed low for write and mode load commands
!we := (banka_state == rcd1a) & write   * Write A
    # (bankb_state == rcd1b) & write   * Write B
    # (banka_state == mode0)   * Precharge &
    # (banka_state == mode3);   * Mode Load
we.ck = clock;

* The DRAM data mask DQM signals are driven low to enable reads and
* writes to each bank. Each bank state machine has individual control of
* the data mask enable signal (dqma and dqmb). These enables go low
* one clock before DQM is required off chip. During read cycles, the
* enables are driven by decoded state bits. During write cycles, they
* always lag each bank's brdy (brdya or brdyb) signal by one clock.

!dqma := (banka_state == rcd1a) & !banka_write   * Read
    # ((banka_state == cmda) # (banka_state == rc0a)
    # (banka_state == rc1a)) & !banka_write & !banka_cache   * Burst Read
    # !brdya & banka_write;   * Write
dqma.ck = clock;

!dqmb := (bankb_state == rcd1b) & !bankb_write   * Read
    # ((bankb_state == cmdb) # (bankb_state == rc0b)
    # (bankb_state == rc1b)) & !bankb_write & !bankb_cache   * Burst Read
    # !brdya & bankb_write;   * Write
dqmb.ck = clock;

* All data masks, dqm[0:7], go low during read cycles when enabled by
* the banka and bankb state machines. During write cycles however, only the
* selected data mask signals, as selected by the latched Pentium byte
* enables, go low.
![dqm0..dqm7] := !dqma & ![be0..be7] & banka_write
    # !dqma & !banka_write
    # !dqmb & ![be0..be7] & bankb_write
    # !dqmb & !bankb_write;
[dqm0..dqm7].ck = clock;

*Define Pentium Burst Ready and Next Address signals

* Each bank state machine controls its own brdy signal. This signal
* goes low one clock cycle before it is required off chip. During
* read cycles it is driven by decoded state bits and latched cache
* and write bits. It is extended one clock during burst reads because
* the state machine has returned to the idle state before the Pentium has
* finished its burst read access.
*
* During write cycles, the write cycle status bits (banka_write and
* bankb_write) are not updated unti RCD0, Therefore, the write signal
* is sampled when the state machine is in state ACT, not the status bit.
* Since the write signal is sampled in ACTA, the setup time is not
* critical for the status bits and brdy signals.
* During mode load, the bank A state machine will drive brdya low
* to terminate the Pentium bus cycle.

!brdya := (banka_state == rc1a) & !banka_write   * Read
    # ((banka_state == rc2a) # (banka_state == rc3a)   * Burst Read
    # brdya_extend) & !banka_cache & !banka_write
    # (banka_state == acta) & write   * Write
    # ((banka_state == rcd0a) # (banka_state == rcd1a)   * Burst Write
    # (banka_state == cmda)) & !banka_cache & banka_write
    # (banka_state == mode3);   * Mode load
brdya.ck = clock;

```
brdya_extend := (banka_state == rc4a);
brdya_extend.ck = clock;

!brdyb := (bankb_state == rc1b) & !bankb_write                      " Read
    # ((bankb_state == rc2b) # (bankb_state == rc3b)               " Burst Read
    # brdyb_extend) & !bankb_cache & !bankb_write
    # (bankb_state == actb) & write                                " Write
    # ((bankb_state == rcd0b) # (bankb_state == rcd1b)             " Burst Write
    # (bankb_state == cmdb)) & !bankb_cache & bankb_write
    # brdy_in;                                                      " System brdy
brdyb.ck = clock;

brdyb_extend := (bankb_state == rc4b);
brdyb_extend.ck = clock;

!brdy := !brdya # !brdyb;
brdy.ck = clock;

"Assert Next Address when either bank is exiting state RCD0

!na := (banka_state == rcd0a)
    # (bankb_state == rcd0b);
na.ck = clock;

" Select column address when MUX is low

!mux := (banka_state == acta)                                      " bank A access
    # (banka_state == rcd0a)
    # (bankb_state == actb)                                        " bank B access
    # (bankb_state == rcd0b)
    # (banka_state == mode1)                                       " Precharge &
    # (banka_state == mode2);                                      " Mode Load
mux.ck = clock;

banka_state.ck = clock;
bankb_state.ck = clock;

end;
```

Module Selector

"

```
title 'Row/Column Address Multiplexor for Synchronous DRAM
    Jeffrey Goldberg
    Xilinx';
selector device;
```

" Inputs

```
clock                                      pin; " 66MHz system clock
mux                                        pin; " Row/Column Select
r0,r1,r2,r3,r4,r5,r6,r7,r8,r9,r10,r11      pin; " Row address inputs
c0,c1,c2,c3,c4,c5,c6,c7,c8                 pin; " Column address inputs
```

```
" MUX, R11 and R[8:0] must be sampled during the first clock
" period of a CPU access, therefore they are declared as fast inputs.
" R9 and R10 drive combinatorial outputs, and can take the UIM path.
" C[8:0] are sampled later in the access, so they are not critical.

plusasm property 'inputpin (fi) r0,r1,r2,r3,r4,r5,r6,r7,r8,r11,mux';
```

" Outputs
```
ma0,ma1,ma2,ma3,ma4,ma5,ma6,ma7,ma8,ma11   pin istype 'reg'; "DRAM address lines
ma9,ma10                                    pin istype 'com';
```

```
" The synchronous DRAM used in this design are organized internally as two
" 1MEGx8 banks. The row address is determined by ma[0:10] and the column
" address by ma[0:8]. MA9 and MA10 are don't cares when the column address is
" being driven during memory accesses but must be driven low when the DRAM
" mode register is being loaded. MA11 is the DRAM bank select input.
```

```
" The CPU address bus should be connected to the multiplexor as shown below.
"          CPU ADDRESS LINE      MULTIPLEXOR INPUT
"                a3                    c0
"                a4                    c1
"                a5                    r11
"                a6                    c2
"                a7                    c3
"                a8                    c4
"                a9                    c5
"                a10                   c6
"                a11                   c7
"                a12                   c8
"                a13                   r0
"                a14                   r1
"                a15                   r2
"                a16                   r3
"                a17                   r4
"                a18                   r5
"                a19                   r6
"                a20                   r7
"                a21                   r8
"                a22                   r9
"                a23                   r10
"
" Row address is selected when mux is high, column address when mux is low.

equations
[ma8..ma0] := [r8..r0] & mux        " These bits are registered because the
# [c8..c0] & !mux;                   " column address must held valid one additional
                                     " clock cycle during a Pentium single write
                                     " access

ma9 = r9;                            " MA9 is a don't care during column access
                                     " so a multiplexor is not needed

ma10 = r10 & mux;                    " MA10 is only used as a row address input
                                     " during memory access cycles. MA10 must be
                                     " high when the precharge command is issued
                                     " by the DRAM controller prior to performing
                                     " a mode load, but must be low when the mode
                                     " load command is issued. Therefore, when the
                                     " preload command is issued, MA10 will follow
                                     " r10, but when the mode load command is issued
                                     " ma10 will be driven low because the DRAM
                                     " controller drives mux low.

ma11 := r11;                         " The bank select bit must be the same for the
                                     " row access and column access commands, so a
                                     " multiplexor is not needed. This bit is
                                     " registered for the same reasons as ma[8:0].

[ma8..ma0].ck = clock;
ma11.ck = clock;
end;
```

∑ XILINX°

Designing Flexible PCI Interfaces With Xilinx EPLDs

January 1995   Application Note – Version 2.0

Abstract

Peripheral Component Interconnect (PCI) is becoming a fundamental building block of today's high-performance PC and workstation peripherals, and developing products that meet the stringent PCI Local Bus Specification (PCI LBS) is the next challenge for system designers.

Xilinx provides a wide range of programmable logic devices that help designers develop PCI-compliant high-performance solutions. The XC7300 Erasable Programmable Logic Devices (EPLDs) offer designers a wide range of programmable logic options that are fully compliant with the PCI LBS.

This application note describes the building blocks of a flexible PCI target interface implemented with XC7300 EPLDs and serves as a guide for designing PCI bus interfaces. To get assistance in evaluating Xilinx EPLDs and FPGAs for your PCI designs, e-mail your design requirements to pci@xilinx.com or call the Xilinx Applications hotline at 1-800-255-7778.

PCI Local Bus Overview

PCI specifies a 32-bit or 64-bit bus with multiplexed address and data lines. It is used as an interconnect between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. Figure 1 shows a typical PCI-based system. The basic system architecture consists of a processor and memory subsystem connected by the processor's local bus. The host bridge connects the local bus and the PCI bus, allowing them to communicate.

High performance peripherals (such as SCSI, LAN, graphics) directly connect to the PCI bus, giving them a high-bandwidth, low latency path to memory. Also shown is a standard bus bridge, that allows low-cost system expansion using a standard bus.

Each agent connected to the PCI bus functions as either a PCI target (slave) or combined PCI initiator/target (master/slave). The initiator function enables an agent to take control of the bus and drive the address, data, and control signals. Target functions cannot initiate bus transfers and rely on initiators to transfer data to them.

PCI Interface Signals

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for an initiator to handle data, address, interface control, arbitration, and system functions. Figure 2 on the next page shows the pins in a initiator/target device, with required pins listed on the left side and optional pins listed on the right side.
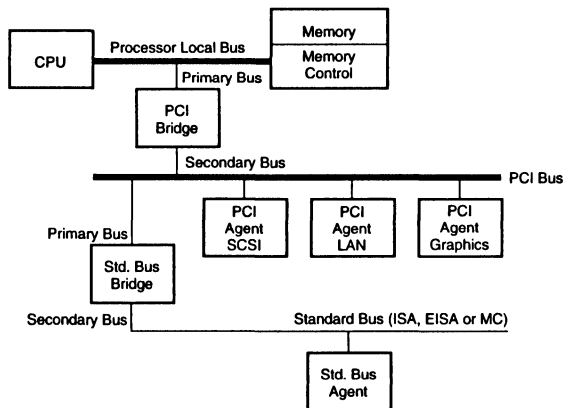
Figure 1. Typical System Architecture
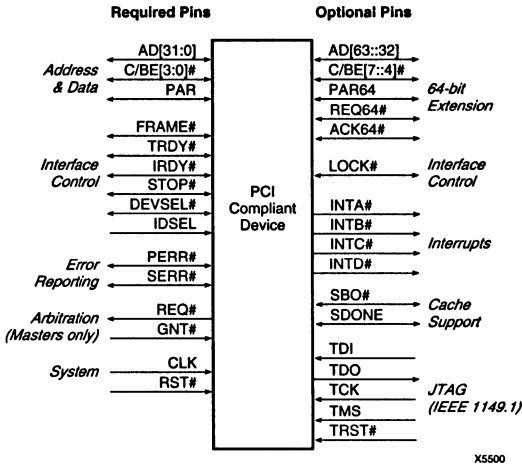
Figure 2. Device Pins

Table 1 lists a summary of the PCI signal pins. A "#" following the signal name indicates the signal is active-low. In this document, PCI signal names appear as **bold**. The signal types are defined as follows:

- **in** — A standard input-only signal.
- **out** — A standard active drive totem pole output.
- **t/s** — A bi-directional, 3-state I/O pin.
- **s/t/s** — A sustained, active-low, 3-state signal; must be high 1 cycle before going low.
- **o/d** — An open drain signal; allows multiple devices to share signals as a wired-OR.

3.3 V and 5 V Signaling Environment Support
The PCI specification defines both 3.3 volt and 5 volt signaling environments and recommends building universal boards with I/O buffers powered by connector-dependent voltage rails as shown in Figure 3.

PCI cards and connectors are keyed to manage both 5 V and 3.3 V environments. In one orientation, the connector is keyed to accept boards using the 5 V system signaling environment. When turned 180°, the key is positioned to accept boards using 3.3 V signaling. Universal boards accept either 3.3 V or 5 V signaling.

The Xilinx XC7300 EPLDs have dual voltage I/O buffers designed to meet these specifications and are ideal for dual voltage operation of the universal board.

Table 1. PCI Signal Summary

Signal	Type	Description
AD[31:0]	t/s	Address and Data Bus.
C/BE[3:0]#	t/s	Bus Command and Byte Enable.
CLK	in	PCI System Clock.
DEVSEL#	s/t/s	Device Select. Signals that the target has decoded its address.
FRAME#	s/t/s	Cycle Frame. Identifies start and length of bus transaction.
GNT#	t/s	Grant. Signals that the master has been granted bus access.
IDSEL	in	Initialization Device Select. Identifies the device selected for configuration.
IRDY#	s/t/s	Initiator Ready. Signals when the master is ready to complete a data transfer.
PAR	t/s	Parity for AD[31:0] and C/BE[3:0].
PERR#	s/t/s	Parity Error.
REQ#	out	Request. Signals a master's request to use the bus.
RST#	in	PCI System Reset.
STOP#	s/t/s	Stop. Signals that the target request to stop the current transaction.
TRDY#	s/t/s	Target Ready. Signals that the target is ready to complete the data transfer.
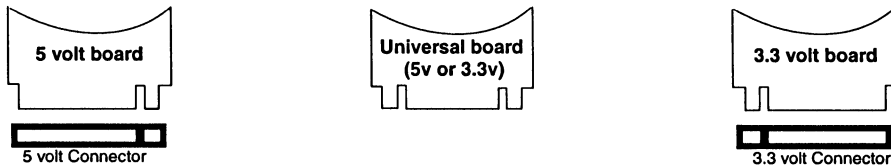
Figure 3. PCI Card Connector Arrangement

PCI Bus Commands

All PCI devices must respond to configuration read/write commands. PCI targets that contain relocatable functions/registers can provide host agents (initiators) the option of mapping those functions into memory space, allowing a device to work where I/O space is not available.

The PCI bus commands, encoded on the **CBE[3:0]#** pins, are summarized in Table 2.

Table 2. PCI Command Summary

C/BE[3:0]#	Command
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

PCI Address Space

PCI defines three address spaces: memory, I/O, and configuration. Memory and I/O spaces are the same as those for Intel microprocessors; configuration space is unique to PCI.

PCI configuration space is divided into a predefined header region (64 bytes) and a device dependent region (192) bytes. A PCI-compliant device is not required to implement all (256 byte) registers. However, all unimplemented registers must return a value of zero when read. The format for the predefined header portion is shown in Table 3; the grey regions indicate the minimum required registers.

The PCI definition also provides for a fully software driven initialization and configuration via a separate configuration address space. One method of implementing this is to pass configuration requests to dedicated memory in the host interface. The designs in Appendices A and B contain configuration cycle decode logic and control signals to support these "pass through" configuration requests to host memory.

The Base Address Register is used by the operating system to determine the Memory or I/O space requirements of a device. In this design, the interface assumes a 16 MB address space (24-bits). The upper 8 bits of the Base Address Register have been implemented with read-write capability and the lower 24 bits always return a read value of zero. To expand or contract the address space allocated, the user simply adjusts the size of the Base Address Register and its associated address comparator.

Table 3. Configuration Space Header

31 16	15 0	
Device ID	Vendor ID	00h
Status	Command	04h
Class Code	Revision ID	08h
BIST / Header Type	Latency Timer / Cache Line Size	0Ch
Base Address Registers		10h - 24h
Reserved		28h
Reserved		2Ch
Expansion ROM Base Address		30h
Reserved		34h
Reserved		38h
Max_Lat / Min_Gnt	Interrupt Pin / Interrupt Line	3Ch
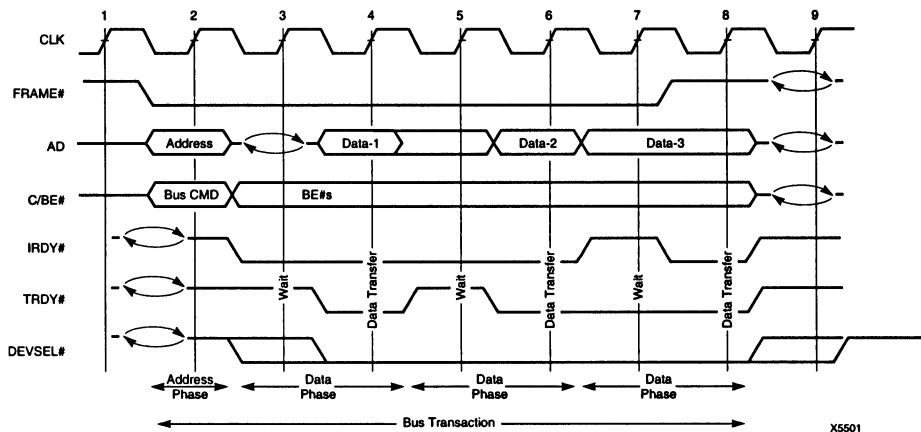
Figure 4. PCI Read Transaction

Data Transfer Timing

The basic PCI bus transfer is a multiple phase protocol which is composed of an address phase and one or more data phases. PCI supports data transfers in both memory and I/O address space. Data transfers are controlled by three signals: **FRAME#**, **IRDY#**, and **TRDY#**. The first clock edge after **FRAME#** is asserted is the address phase; the address value and bus command code are transferred on that clock edge. **FRAME#** remains asserted during each following data phase and de-asserts to indicate the final data phase.

Data is transferred between master and target on each clock edge for which both **IRDY#** (Initiator Ready) and **TRDY#** (Target Ready) are asserted. Wait cycles may be inserted in a data phase by either the master (using **IRDY#**) or by the target (using **TRDY#**). The data source is required to assert its *x*RDY# signal unconditionally when data is valid. The receiving agent may assert its *x*RDY# as it chooses. Once an initiator has asserted **IRDY#**, it cannot change **IRDY#** or **FRAME#** until the current data phase completes, regardless of **TRDY#**. Once a target has asserted **TRDY#** or **STOP#** it cannot change **DEVSEL#**, **TRDY#**, or **STOP#** until the current data phase completes.

The maximum transfer rate of the 32-bit PCI bus is one 32-bit word every 30 ns, or 132 Mbytes/second. Figure 4 shows the read transaction and Figure 5 shows the write transaction.

When the initiator intends to complete one or more data transfers, **FRAME#** is de-asserted and **IRDY#** is asserted indicating the last data phase. After the target indicates the final data transfer (**TRDY#** asserted), the interface returns to the idle state with both **FRAME#** and **IRDY#** de-asserted.
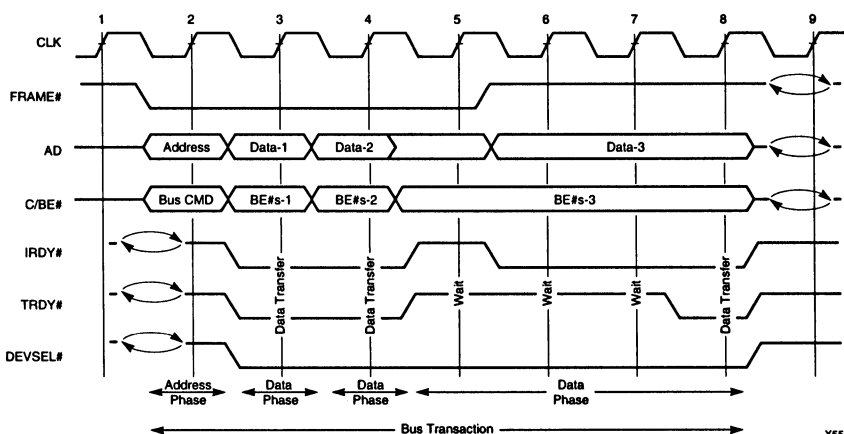
Figure 5. PCI Write Transaction

Target Design Overview

This section discusses various design concepts relating to the architecture of a generic PCI to I/O device target interface for add-in boards.

A PCI add-in board has a PCI bus interface, configuration registers, and optional expansion ROM. It also has implementation specific features such as buffers, FIFOs, device registers, I/O control logic, and the specific back-end functions such as SCSI, IDE, LAN, or graphics.

The PCI interface device (typically connected directly to the PCI bus connector) manages incoming and outgoing data transfer cycles from the PCI bus. During configuration cycles, software device drivers use the information in the configuration registers to identify I/O system requirements and then automatically configure the device for "Plug and Play" operation.

Target Interface Operation

As shown in Figure 6, the PCI I/O interface consists of a PCI Bus Interface, Error Handler, FIFOs, and Memory Controller. This design shows the elements of a generic solution to illustrate the connection of an I/O device to the PCI bus.

A detailed block diagram of the PCI Bus Interface is shown in Figure 7 on the next page. When this Bus Interface detects a bus transaction, it passes address/data

(D[31:0]) to the memory controller (XC3190) and asserts HIT, S[0], and MEM_WR to inform the back-end interface of the bus transaction.

When the I/O device has finished the transaction, it asserts DEV_REQ#. Upon completion of the PCI bus transfer (**IRDY#** and **TRDY#** asserted simultaneously, and **FRAME#** de-asserted), it de-asserts DEV_ACK#. The I/O device asserts DEV_REQ# until it sees DEV_ACK# de-asserted. The I/O device can also signal an error to the PCI bus interface by asserting T_ABORT# or RETRY#. The PCI interface handles these by asserting and de-asserting the appropriate PCI bus signals.

The memory controller state machine in the I/O device is programmed using PCI bus I/O commands. Once the memory controller is properly initiated, the decoded activity is started as a memory operation until a new I/O command is received. The DMA controller handles all FIFO and DMA read/write cycles. Start address and count lengths are in I/O data bits D[23:0]. I/O commands are decoded from data bits D[27:24].

Device specific functions such as buffers, burst address generators and FIFOs vary from one application to the next. For specific information on memory controller designs and FIFO devices, refer to the specific manufacturer's data sheets.
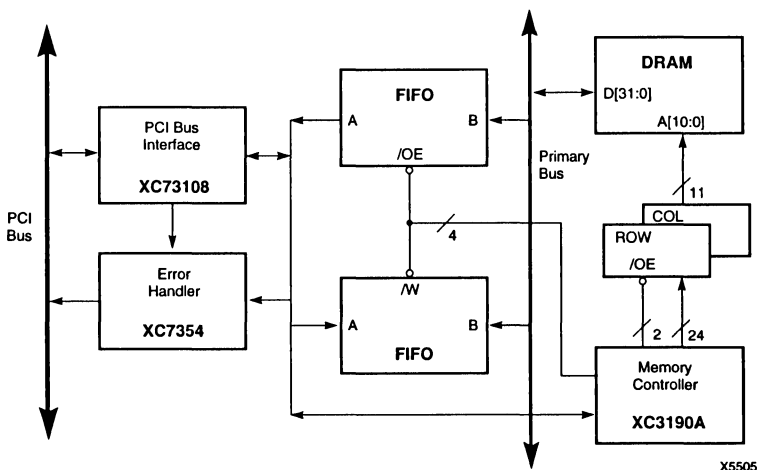
Figure 6. PCI Target Controller Design

Bus Interface Implementation

Many designs use either a target or master bus interface. The target state machine implemented in this design supports the options discussed in the PCI specification with the exception of the target lock operation.

As shown in Figure 7, the Bus Interface consists of four parts: 1) target sequencer which performs the actual bus operation, 2) address decode which identifies valid address cycles, 3) configuration control which handles base address maintenance, and 4) data mux which transfers data between the bus and the I/O controller.

The Target Sequencer

The Target Sequencer Block (TARGET) controls the bus operation and guarantees that the PCI protocol is not violated. The state machine for the target sequencer is shown in Figure 8. This figure is similar to the one found in the PCI Local Bus Specification, but has been modified to support the memory interface described above.

The following paragraphs discuss each state and describe how transitions occur during data transfers.

IDLE is the default state. The bus interface latches signals from the PCI bus to determine the start of a data transfer or configuration access.

When a bus access begins, the address is compared to the base address. If the address matches, HIT is asserted, and the sequencer transitions to the S_DATA state to start a data transfer. Otherwise, it goes to the B_BUSY state.

B_BUSY is the state where the agent waits for the current transaction to complete and the bus to return to idle.

S_DATA is the state where the target transfers data. When the transfer is complete, the sequencer transitions to the TURN_AR state (non-burst transfers) or BACKOFF state (burst transfer attempt).

TURN_AR is the state used to release the PCI bus when the data transfer is complete. It automatically transitions back to the idle state.

BACKOFF is the state where the sequencer goes after it asserts **STOP#** and waits for the master to de-assert **FRAME#**. It then transitions back to the TURN_AR state.
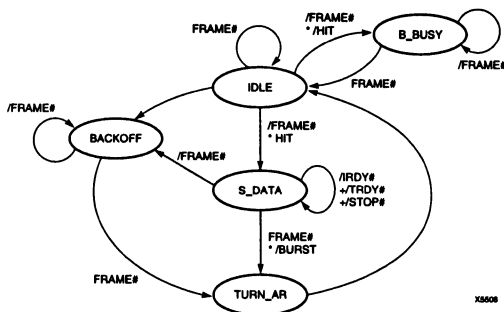
Figure 8. Target Bus Sequencer State Machine
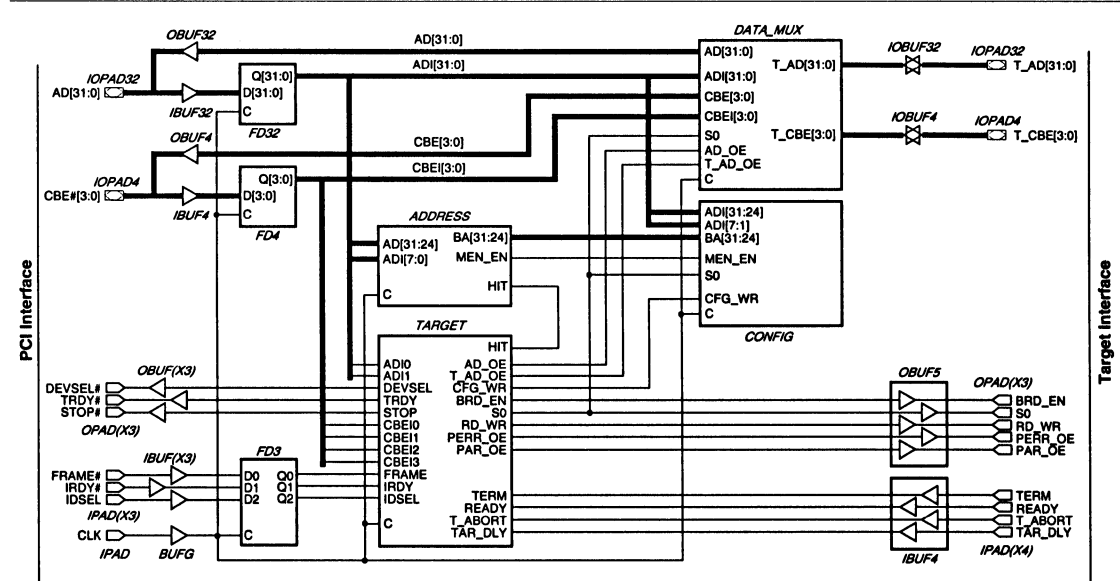
Figure 7. PCI Bus Interface Detailed Block Diagram
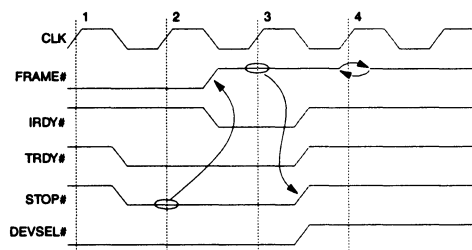
Figure 9. Disconnect Timing
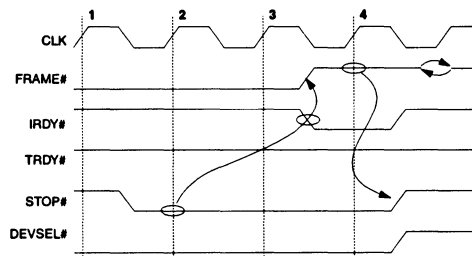
Figure 10. Retry Timing

There are many instances in which targets may wish to terminate the PCI transaction. Target disconnects are identified by the assertion of the signals **STOP#, TRDY#,** and **DEVSEL#** as shown in Figure 9. The initiator responds to the disconnect condition by de-asserting **FRAME#** on the following clock period and does not complete the data transfer until it asserts **IRDY#.** When the PCI interface is accessed and data is unavailable for read transfers or the FIFO is full for write transfers, the PCI interface terminates the cycle and requests a retry. This condition is identified by the assertion of both **STOP#** and **DEVSEL#** while **TRDY#** is de-asserted. Figure 10 shows the behavior of the target Interface when performing a target-initiated retry.

The Address Decoder
The Address Block (ADDRESS) compares the upper 8-bits of the PCI address bus AD[31:24] to the value stored in the Base Address Register (BA[31:24]). The comparison output (MATCH) is gated with memory enable (MEM_EN) to control when the device can detect a valid PCI address cycle (HIT).

The Configuration Registers
I/O devices are required to implement a 256-byte configuration space. Most registers in this configuration space can be built using "reserved" registers where writes to the registers have no effect, and reads must return "0". Guidelines for using several of the registers in I/O controllers are discussed as follows.

The Base Address Registers are used for relocating PCI devices in memory and I/O space. Devices can choose to

map into memory or I/O spaces. However, memory mapped I/O is recommended because performance is generally higher. The initialization software can determine how much address space the device requires by writing ones to the register and then reading the value back. The device returns zeros in all don't-care address bits, effectively specifying the address space required.

The Configuration Block (CONFIG) implements a memory mapped 8-bit Base Address Register located at configuration space header location 10h (CSH_01h). The Base Address Register (BASE_AD_REG) is implemented as a write-only register loaded when PCI address AD[7:2] is 40h. The two least significant address lines. (AD[1:0]) are "00" during the address phase of configuration cycles.

The memory space is easily modified to support more or less memory. Designers should thoroughly evaluate the trade-off between memory space and the size of the Base Address Register. A larger Base Address Register requires a larger comparator which may be difficult to implement in the device.

The configuration block also contains the command register's memory space enable bit (MEM_EN) to provide control over the device's response to memory space address. When a value of "0" is written to this register, the device is locally disconnected from the PCI bus for all addresses except configuration. A value of "1" allows the device to respond to memory space addresses. The MEM_EN signal is used to assert HIT when a valid address is decoded.

The Data Multiplexer

The Data Multiplexer Block (DATA_MUX) controls the movement of data from the PCI bus to the I/O device. During write cycles, PCI data enters the interface and is registered in the I/O pad flip-flops (FD32,FD4) to meet the setup and hold requirements of the PCI bus ($t_{SU} = 7$ nsec, $t_H = 0$ nsec). PCI bus signals pass from the I/O flip-flops to macrocell flip-flops which drive the I/O bus.

During read cycles, data enters the interface through T_AD(31:0) and is registered in macrocell flip-flops which drive the PCI bus. The TARGET block controls the direction of the data path by asserting AD_OE on read cycles and T_AD_OE on write cycles. Figure 11 illustrates how the DATA_MUX block is implemented in the XC73108 device architecture.
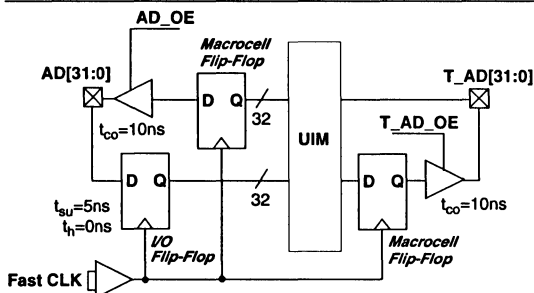
Figure 11. DATA_MUX Architecture

The PCI bus turnaround cycle occurs in different cycles for different signal types (address/data, control, error) resulting in a need for multiple, independent 3-state buffer controls. The XC7300 architecture allows designers two options to meet the clock-to-output enable valid specification ($t_{VAL} = 11$ nsec). Figure 12 illustrates one option using one of the two global Fast Output Enable (FOE) pins in an EPLD Fast Function Block.
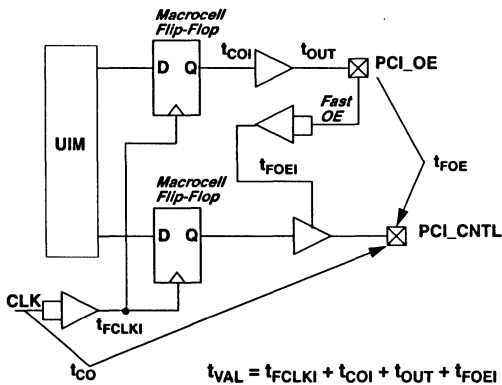
Figure 12. Fast Output Enable Timing Path

Both FOE pins are programmable bi-directional pins which can be driven internally by a macrocell flip-flop or externally by another flip-flop. Using one of the Fast Function Block (FFB) macrocells to drive the FOE pin externally will also meet PCI 3-state enable/disable specifications. FOE is a global 3-state control and should be used to control bussed PCI and back-end signals (address/data and command/byte enable).

For the remaining control signals, PCI clock-to-output valid timing requirements can be met using the High Density Function Block (FB) Fast Input (FI) paths to drive the output enable product term (OE P-TERM). This option is illustrated in Figure 13.
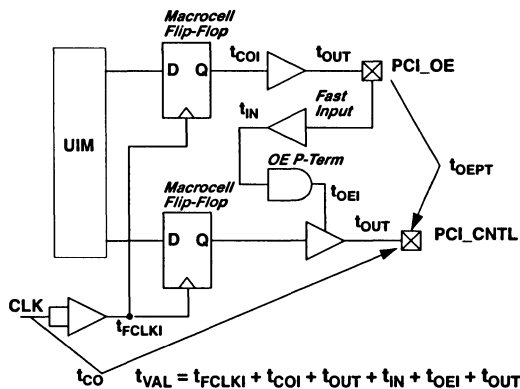
Figure 13. Fast Input Timing Path

Each FB provides three Fast Input (FI) paths driven internally by a dedicated macrocell flip-flop. Like the FOE pin, FI pins are programmable bi-directional pins which can be driven internally by the macrocell flip-flop or externally by another flip-flop. Using one of the Fast Function Block (FFB) macrocells to drive the FI pins externally will also meet PCI 3-state enable/disable specifications.

Figure 12 and Figure 13 incorporate macrocell-to-pad plus pad-to-pad delays to enable the 3-state buffers. Using internal data sheet parameters to calculate t_{VAL} results in values which exceed 11 nsec. Device characterization data however, guarantees that High Density FB macrocells configured as shown in Figures 10 and 11 will meet the 11 nsec specification.

These guaranteed values apply to the -10 and -7 speed grades operating over commercial voltage and temperature ranges. The conservative values, presently published in Xilinx data sheets, unify timing parameters across the XC7300 family and consequently do not reflect the true PCI compliance of the XC7300 family.

Error Handler Implementation

PCI error coverage can range from simple devices, having no interest in errors, to agents that detect, signal, and recover from errors. To allow this flexibility, the generation of parity is required on all transactions by all agents.

Parity on the PCI bus provides a mechanism to determine, transaction by transaction, if the master is successful in addressing the desired target and if data being transferred between them is valid. During address and data phases, parity covers **AD[31:0]** and **C/BE[3:0]** lines. PCI uses even parity; the number of ones on **AD[31:0]**, **C/BE[3:0]**, and **PAR** equals an even number.

On each bus phase, **PAR** is driven by the agent that drives **AD[31:0]** and lags the corresponding address or data by one clock.

PCI defines two signals, **PERR#** and **SERR#**, for detecting and reporting system errors. **PERR#** is used exclusively for reporting data parity errors on all transactions except Special Cycle commands. **SERR#** is used for signaling any other non-parity or system errors. The timing diagram in Figure 14 shows the timing relationships between the signals **AD[31:0]**, **C/BE[3:0]#**, **PAR**, **PERR#**, and **SERR#**.

Xilinx XC7300 devices provide an efficient macrocell structure to easily generate parity. Each High-Density Function Block (FB) macrocell is capable of generating parity across 6-bits. The entire 36-bit parity calculation can be performed within one clock cycle (30 nsec) using a variety of design techniques. In a pipe-lined design, the first stage of the pipe-line generates parity calculations on sub-segments of the 36-inputs (six 6-bit segments). The parity outputs from the first stage are fed into the second pipe-line stage which completes the parity calculation. Figure 15 illustrates how this works.

To maximize the logic capacity of the PCI Interface (XC73108), the parity PAR output has been placed into the XC7354-10. Using this approach, the XC7354 computes parity in parallel with the back-end data ADT[31:0] being read through the PCI Interface. Back-end data is clocked into the PCI Interface and the first stage pipe-line of the parity generator. Following this clock edge, back-end data is placed on the PCI bus and the partial parity is fed to the second pipe-line stage. On the next clock edge, PAR is output onto the PCI bus with one clock cycle delay as specified in the PCI LBS.
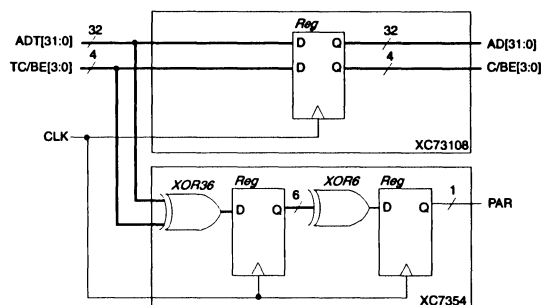
Figure 15. Parity Generation Block Diagram

The parity generation circuit makes use of a registered pipe-lined design approach. Checking of parity on PCI requires replacing the registers in the first stage pipe-line with combinatorial logic paths. Removing the intermediate pipe-line registers converts the parity generator to two-logic levels which can be used to calculate parity in one clock cycle. Appendix B contains the ABEL source code (PARITY.ABL) for the Error Handler Design implemented in the XC7354-10 68-pin PLCC package.

Figure 14. Parity Operation Timing Diagram

Pinout Recommendation

The XC73108 pinout for a PQ160 can been fixed to align with the recommended PCI pinout as shown in Figure 16.

The **IDSEL** input should be placed as close as possible to **AD[31:11]** allowing the option for a non-resistive connection of **IDSEL** to the appropriate address line with only a small additional load. This pin has a maximum capacitive loading specification of 8pf, matching PCI LBS v2.0.

The placement of power and ground pins is package dependent. Connecting the XC7300 V_{CCIO} pins to the PCI signaling rail (+$V_{I/O}$) on the Universal Board (shown in Figure 3) allows the I/O buffers to be powered from these special pins. To ensure adequate capacitance between the I/O buffer power rail and the ground plane, the pins labeled +$V_{I/O}$ should be decoupled to ground with an average of 0.01uF per pin. Additionally, all +3.3 volt pins and any unused +5 volt must have plated card edge fingers and be coupled to the ground plane on the add-in board to control noise immunity and provide efficient AC reference points.

PCI Design Verification

Hardware designs can be verified for full compliance with the PCI standard by using the Xilinx simulation models and the PCI test suite. The PCI test suite consists of 27 test scenarios developed in collaboration with the PCI Special Interest Group to exactly match the SIG's compliance checklist. For more details on Xilinx XC7300 family simulation techniques and the PCI test suit contact your local Xilinx Sales Representative or email Xilinx at **PCI@Xilinx.com**.

Application Summary

This application note discusses the implementation of a Target PCI Bus interface using Xilinx XC73108 and XC7354 EPLDs. This design provides the foundation for PCI systems and allows customization for different design variations and applications. For example, the pinout compatible XC73144 can be used as a drop in replacement to the XC73108 in order to integrate both the XC73108 and XC7354 into a single device. The additional unused logic available in the XC73144 could be used for implementing burst mode counters, latency timers, target locking mechanisms, and other enhancements. Appendix A contains the ABEL source code for the XC73108 bus interface and appendix B contains the ABEL source code for the XC7354 parity generator.

The Xilinx XC7300 family of 100% PCI compliant devices offers a wide range of devices which can be used to implement various PCI solutions such as initiator interfaces, target interfaces, standard peripheral interfaces, and PCI interfaces to standard buses such as ISA, EISA, or VME. Contact your local Xilinx distributor sales office for more information.

The design specifications in this application note are subject to change without notice. Verify with your local Xilinx sales office that you have the latest specifications before finalizing a design.

Figure 16. Recommended Device Pinout

Interfacing with Xilinx XC7300 Devices

This section provides the electrical specifications and operating conditions for both 5 volt and 3.3 volt signaling environments for Xilinx XC7300 devices. This section references the details of the PCI Local Bus Specification Revision 2.0 concerning DC, AC, Clock, and Timing parameters. It is divided into section titles that are identical to the PCI specification for easy reference. These specifications show that the Xilinx XC7300 devices in Table 4 comply with all PCI Local Bus specifications.

Table 4. Xilinx XC7300 PCI Compliant Devices

PCI Compliant XC7300 Devices	
XC7318 -5, -7	PQ44, PC44
XC7336 -5, -7, -10	PQ44, PC44
XC7354 -7, -10	PC44, PC68
XC7372 -7, -10	PC68, PC84, PQ100
XC73108 -7, -10	PQ100, PQ160, BG225
XC73144 -7, -10	PQ160, BG225

Table 5 shows the EPLD macrocell utilization estimates for various functions and PCI interface design configurations. Columns 2 and 3 illustrate the differences between target and initiator only designs. Column 4 shows the effect of handling the data path with PCI compliant registered transceivers. Column 5 shows the single device solution described in this application note.

V/I Curves for 3.3 Volt and 5 Volt Signaling

The PCI bus is unterminated and is based on reflective wave signaling. This means that when the bus drivers transition a signal line from a low to a high, the transition is relatively weak and may only achieve half of the voltage change required to cross the logic threshold. This weak transition wave is propagated along the bus and is seen sequentially by each device connected to the line. When the wave reaches the end of the line, it is reflected back, effectively doubling the voltage and therefore boosting the signal past the logic threshold as it passes each input.

PCI specifies the voltage to current (V/I) requirements for device I/O drivers. Traditionally, a bus specifies I/O sink and source limits at logic 0 and 1, the steady-state conditions. PCI differs in that it also specifies sink and source switching currents across the transition from one logic level to the other. Figure 17 and Figure 18 on the next page show the I_{OH} and I_{OL} limits represented by shaded regions. A device is considered compliant if it's V/I curve does not cut into a shaded region. These curves show that XC7300 EPLDs are fully compliant with both 5 volt and 3.3 volt V/I characteristics.

The V/I curves represent continuous-range, short-circuit conditions where the device I/O must handle over 95mA for very short time periods. PCI devices do not need to handle these levels continuously; steady-state current requirements are only 3-6 mA.

Table 5. XC7300 Macrocell Utilization Estimates

Device	XC73108 + XC7354		XC73108 + PCI Bus Transceiver	XC73144
Interface Type	Target Only	Initator Only	Target/Initiator	Target/Initiator
State Machine	3	4	9	9
Add Decode	1	-	1	1
Base Add Reg	8	-	8	8
Parity Generator	10	10	10	10
PCI Interface	47	49	49	49
I/O Data Path	32	32	-	32
I/O Cntl Logic	17	28	28	28
Total In Design	118	123	105	137
Total In Device	162	162	108	144
Total Available	44	39	3	7

Figure 17. 3.3 Volt V/I Curves

These curves show that both High Density Function Blocks and Fast Function Blocks within Xilinx XC7300 EPLDs are fully compliant with PCI 3.3 volt V/I characteristics.
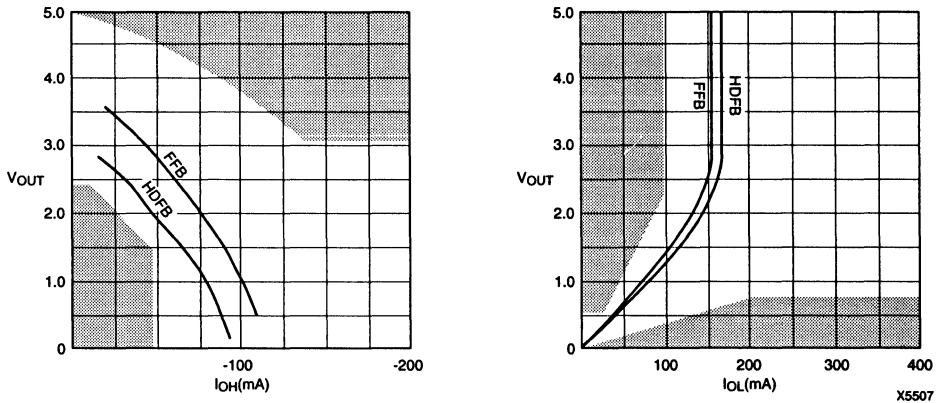
Figure 18. 5 Volt V/I Curves

These curves show that both High Density Function Blocks and Fast Function Blocks within Xilinx XC7300 EPLDs are fully compliant with PCI 5 volt V/I characteristics.

DC Specifications for 3.3 Volt Signaling

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
V_{cc}	Supply Voltage		3.0	3.6	3.0	3.6	V	✔
V_{ih}	Input High Voltage		$0.475\,V_{cc}$	$V_{cc}+0.5$	1.425	$V_{cc}+0.5$	V	✔
V_{il}	Input Low Voltage		-0.5	$0.325V_{cc}$	-0.5	1.17	V	✔
V_{ipu}	Input Pull-up Voltage		$0.7\,V_{cc}$		$0.7\,V_{cc}$		V	✔
I_{il}	Input Low Leakage Current	$0 < V_{in} < V_{cc}$		±10.0		±10.0	μA	✔
V_{oh}	Output High Voltage	I_{out} = -500 μA	$0.9\,V_{cc}$		$0.9\,V_{cc}$		V	✔
V_{ol}	Output Low Voltage	I_{out} = 1500 μA		$0.1V_{cc}$		$0.1\,V_{cc}$	V	✔
C_{in}	Input Pin Capacitance			10.0		8.0	pF	✔
C_{clk}	CLK Pin Capacitance		5.0	12.0	5.0	12.0	pF	✔
C_{IDSEL}	IDSEL Pin Capacitance			8.0		8.0	pF	✔
L_{pin}	Pin Inductance			20.0		10.0	nH	✔

DC Specifications for 5 Volt Signaling

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
V_{cc}	Supply Voltage		4.75	5.25	4.75	5.25	V	✔
V_{ih}	Input High Voltage		2.0	$V_{cc}+0.5$	2.0	$V_{cc}+0.5$	V	✔
V_{il}	Input Low Voltage		-0.5	0.8	-0.5	0.8	V	✔
I_{ih}	Input High Leakage Current	V_{in} = 2.7		70.0		10.0	μA	✔
I_{il}	Input Low Leakage Current	V_{in} = 0.5		-70.0		-10.0	μA	✔
V_{oh}	Output High Voltage	I_{out} = -2 mA	2.4		2.4		V	✔
V_{ol}	Output Low Voltage	I_{out} = 3 mA, 6 mA		0.55		0.5	V	✔
C_{in}	Input Pin Capacitance			10.0		8.0	pF	✔
C_{clk}	CLK Pin Capacitance		5.0	12.0	5.0	12.0	pF	✔
C_{IDSEL}	IDSEL Pin Capacitance			8.0		8.0	pF	✔
L_{pin}	Pin Inductance			20.0		10.0	nH	✔

The PCI specification calls for components to operate within the commercial range of environmental parameters. All of the specifications listed for Xilinx XC7300 devices are for the commercial range of V_{CC} = 5.0 V ± 5% and ambient temperature of 0°C to 70°C.

AC Specifications for 3.3 Volt Signaling (Fast Function Blocks)

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
$I_{oh(AC)}$	Switching Current High	$0 < V_{out} \leq 0.3V_{cc}$	$-12\ V_{cc}$		-50		mA	✔
		$0.3V_{cc} < V_{out} < 0.9V_{cc}$	EqnF	EqnC	Note 3		mA	✔
	(test point)	$V_{out} = 0.7V_{cc}$		$-32\ V_{cc}$		-90	mA	✔
$I_{ol(AC)}$	SwitchingCurrent Low	$V_{cc} > V_{out} \geq 0.6V_{cc}$	$16\ V_{cc}$		70		mA	✔
		$0.6 > V_{out} > 0.1V_{cc}$	$26.7\ V_{out}$	EqnD	Note 4		mA	✔
	(test point)	$V_{out} = 0.18\ V_{cc}$		$38\ V_{cc}$		90	mA	✔
I_{cl}	Low Clamp Current	$V_{in} = -1, -2$	$-25, -91$		$-25, -100$		mA	✔
I_{ch}	High Clamp Current	$V_{in} = V_{cc}+1, V_{cc}+2$	25, 91		25, 100		mA	✔
t_r	Unloaded Output Rise Time	$0.2V_{cc} - 0.6V_{cc}$	1	4	1.1	4	V/ns	✔
t_f	Unloaded Output Fall Time	$0.6V_{cc} - 0.2V_{cc}$	1	4	1.5	4	V/ns	✔

AC Specifications for 3.3 Volt Signaling (High Density Function Blocks)

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
$I_{oh(AC)}$	Switching Current High	$0 < V_{out} \leq 0.3V_{cc}$	$-12\ V_{cc}$		-40		mA	✔
		$0.3V_{cc} < V_{out} < 0.9V_{cc}$	EqnF	EqnC	Note 3		mA	✔
	(test point)	$V_{out} = 0.7V_{cc}$		$-32\ V_{cc}$		-50	mA	✔
$I_{ol(AC)}$	SwitchingCurrent Low	$V_{cc} > V_{out} \geq 0.6V_{cc}$	$16\ V_{cc}$		60		mA	✔
		$0.6 > V_{out} > 0.1V_{cc}$	$26.7\ V_{out}$	EqnD	Note 4		mA	✔
	(test point)	$V_{out} = 0.18\ V_{cc}$		$38\ V_{cc}$		60	mA	✔
I_{cl}	Low Clamp Current	$V_{in} = -1, -2$	$-25, -91$		$-25, -100$		mA	✔
I_{ch}	High Clamp Current	$V_{in} = V_{cc}+1, V_{cc}+2$	25, 91		25, 100		mA	✔
t_r	Unloaded Output Rise Time	$0.2V_{cc} - 0.6V_{cc}$	1	4	1.0	4	V/ns	✔
t_f	Unloaded Output Fall Time	$0.6V_{cc} - 0.2V_{cc}$	1	4	1.5	4	V/ns	✔

Note 3: XC73108-10 I_{oh} switching currents are within the minimum and maximum conditions established by equations F and C.

Note 4: XC73108-10 I_{ol} switching currents are within the minimum and maximum conditions established by 26.7 V_{out} and equation D.

Equation C: $I_{oh} = (98.0/V_{cc})*(V_{out}-V_{cc})*(V_{out}+0.4V_{cc})$ for $V_{cc} > V_{out} > 0.7V_{cc}$

Equation D: $I_{ol} = (256/V_{cc})*(V_{out}*(V_{cc}-V_{out})$ for $0V < V_{out} < 0.18V_{cc}$

Equation F: $I_{oh} = -17.1(V_{cc}-V_{out})$ for $0.3V_{cc} < V_{out} < 0.9V_{cc}$

AC Specifications for 5 Volt Signaling (Fast Function Blocks)

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
$I_{oh(AC)}$	Switching Current High	$0 < V_{out} \leq 1.4$	-44		-60		mA	✔
		$1.4 < V_{out} < 2.4$	EqnE	EqnA	Note 1		mA	✔
	(test point)	$V_{out} = 3.1$		-142		-60	mA	✔
$I_{ol(AC)}$	Switching Current Low	$V_{out} \geq 2.2$	95		110		mA	✔
		$2.2 > V_{out} > 0.55$	$V_{out}/0.023$	EqnB	Note 2		mA	✔
	(test point)	$V_{out} = 0.71$		206		140	mA	✔
I_{cl}	Low Clamp Current	$V_{in} = -1, -2$	-25, -91		-25, -100		mA	✔
t_r	Unloaded Output Rise Time	0.4V to 2.4V	1	5	1.0	5	V/ns	✔
t_f	Unloaded Output Fall Time	2.4V to 0.4V	1	5	1.8	5	V/ns	✔

AC Specifications for 5 Volt Signaling (High Density Function Blocks)

Symbol	Parameter	Condition	PCI Specification		XC7300-10		Units	PCI Compliant
			Min	Max	Min	Max		
$I_{oh(AC)}$	Switching Current High	$0 < V_{out} \leq 1.4$	-44		-45		mA	✔
		$1.4 < V_{out} < 2.4$	EqnE	EqnA	Note 1		mA	✔
	(test point)	$V_{out} = 3.1$		-142		-40	mA	✔
$I_{ol(AC)}$	Switching Current Low	$V_{out} \geq 2.2$	95		95		mA	✔
		$2.2 > V_{out} > 0.55$	$V_{out}/0.023$	EqnB	Note 2		mA	✔
	(test point)	$V_{out} = 0.71$		206		70	mA	✔
I_{cl}	Low Clamp Current	$V_{in} = -1, -2$	-25, -91		-25, -100		mA	✔
t_r	Unloaded Output Rise Time	0.4V to 2.4V	1	5	1.2	5	V/ns	✔
t_f	Unloaded Output Fall Time	2.4V to 0.4V	1	5	1.9	5	V/ns	✔

Note 1: XC73108-10 I_{oh} switching currents are within the minimum and maximum conditions established by equations E and A.

Note 2: XC73108-10 I_{ol} switching currents are within the minimum and maximum conditions established by $V_{out}/0.023$ and equation B

Equation A: $I_{oh} = 11.9*(V_{out}-5.25)*(V_{out}+2.45)$ for $V_{cc} > V_{out} > 3.1V$

Equation B: $I_{ol} = 78.5*(V_{out}*(4.4-V_{out})$ for $0V < V_{out} < 0.71V$

Equation E: $I_{oh} = -44+(V_{out}-1.4)/0.024$ for $1.4 < V_{out} < 2.4$

Timing Specifications

Symbol	Parameter	PCI Specification		XC7300-10		Units	PCI Compliant
		Min	Max	Min	Max		
t_{cyc}	CLK Cycle Time	30.0	∞	16.0	∞	ns	✔
t_{high}	CLK High Time	12.0		5.0		ns	✔
tlow	CLK Low Time	12.0		5.0		ns	✔
-	CLK Slew Rate	1.0	4	1.0	4	V/ns	✔

The PCI specification requires components to support frequencies from 0MHz to 33 MHz.

5 Volt and 3.3 Volt Timing Parameters

Symbol	Parameter	PCI Specification		XC7300-10		Units	PCI Compliant
		Min	Max	Min	Max		
t_{val}	CLK to Signal Valid Delay- bussed signals	2	11	2	10.5	ns	✔
t_{val}(ptp)	CLK to Signal Valid Delay- point to point	2	12	2	10.5	ns	✔
t_{on}	Float to Active Delay	2		2		ns	✔
t_{off}	Active Float Delay		28		28	ns	✔
t_{su}	Input Set up Time to CLK- bussed signals	7		5		ns	✔
t_{su}	Input Set up Time to CLK- bussed signals	7		5		ns	✔
t_{su}(ptp)	Input Set up Time to CLK- point to point	10,12		5		ns	✔
t_h	Input Hold Time from CLK	0		0		ns	✔
t_{rst-on}	Reset Active to Output Float Delay		40		23	ns	✔

In expansion boards, compliance with the clock specification is measured at the expansion board component, not at the connector slot.

Note:

This design has been compiled for Xilinx EPLDs. It has been simulated but not constructed and may require modification to operate in different end applications.

Appendix A
ABEL Source Code
XC73108 PCI Bus Interface

```
module TARGET
title 'PCI Target Interface Design'
TARGET device ;
"PCI Bus Input Signal Declarations
CLK,FRAMEI,IRDYI,IDSELI,CBE3..CBE0        pin;
FRAME,IRDY,IDSEL,CBEI3..CBEI0         node istype 'reg';
"PCI Bus Output and I/O Pad Register Declaration
AD31..AD0,TRDY,STOP,DEVSEL             pin istype 'reg';
ADI31..ADI0                           node istype 'reg';
"Target Bus Input Signal Declarations
TERM,READY,T_ABORT,TAR_DLY,TRDY_FOE       pin;
"TARGET Interface Outputs Node Declarations
T_AD31..T_AD0,TRDY_OE                  pin istype 'reg';
PAR_OE,PERR_OE,AD_OE,T_AD_OE,RD_WR,S0  pin istype 'reg';
TS2..TS0,MEM_EN                       node istype 'reg';
CFG_WR,BA31..BA24,CFGQ7..CFGQ2        node istype 'reg';
HIT,MATCH,BURST,LOAD                  node istype 'com';
NODE_C6..NODE_C3                      node istype 'com';
NODE_CFG_10h,NODE_CFG_04h             node istype 'com';
h,l,x          = 1,0,.X.;
"Signal Bus Declarations for PCI and Target Bus Interfaces
PCI_AD_BUS     = [AD31..AD0];
PCI_AD_REG     = [ADI31..ADI0];
PCI_AD_HI      = [ADI31..ADI24];
CFG_AD_IN      = [ADI7..ADI2];
CFG_AD_CNTR    = [CFGQ7..CFGQ2];
PCI_CBE        = [CBE3..CBE0];
PCI_CBE_REG    = [CBEI3..CBEI0];
T_AD_BUS       = [T_AD31..T_AD0];
BASE_AD_REG    = [BA31..BA24];
"PCI TARGET State Machine Register Assignment
TARGET_SEQ     = [TS2,TS1,TS0];
IDLE_          = [ 0 , 0 , 0 ];
B_BUSY_        = [ 0 , 0 , 1 ];
S_DATA_        = [ 0 , 1 , 1 ];
TURN_AR_       = [ 0 , 1 , 0 ];
BACKOFF_       = [ 1 , 1 , 0 ];
STATEN1_       = [ 1 , 1 , 1 ];
STATEN2_       = [ 1 , 0 , 1 ];
STATEN3_       = [ 1 , 0 , 0 ];
IDLE           = TARGET_SEQ == [0,0,0];
B_BUSY         = TARGET_SEQ == [0,0,1];
S_DATA         = TARGET_SEQ == [0,1,1];
TURN_AR        = TARGET_SEQ == [0,1,0];
BACKOFF        = TARGET_SEQ == [1,1,0];
@ALTERNATE
@DCSET
XEPLD PROPERTY 'PARTITION FFB TS2 TS1 TS0 AD_OE T_AD_OE TRDY STOP DEVSEL FRAME IRDY';
XEPLD PROPERTY 'INPUTPIN (FI) FRAMEI IRDYI';
XEPLD PROPERTY 'LOGIC_OPT OFF NODE_CFG_10h NODE_CFG_04h MEM_EN LOAD BURST';
Equations
" PCI bus to Target interface data path. Target interface passes
" address and data transfers synchronusly through interface

PCI_AD_BUS     := T_AD_BUS.PIN;
PCI_AD_BUS.CLK = CLK;
PCI_AD_BUS.OE  = /AD_OE;
PCI_AD_REG     := PCI_AD_BUS.PIN;
PCI_AD_REG.CLK = CLK;
PCI_CBE_REG    := PCI_CBE.PIN;
PCI_CBE_REG.CLK = CLK;
```

```
FRAME            := FRAMEI;
FRAME.CLK         = CLK;
IRDY             := IRDYI;
IRDY.CLK          = CLK;
IDSEL            := IDSELI;
IDSEL.CLK         = CLK;
T_AD_BUS         := PCI_AD_REG;
T_AD_BUS.OE       = /T_AD_OE;
T_AD_BUS.CLK      = CLK;
BURST             = S_DATA * /IRDY * /TRDY;
LOAD              = (/FRAME * IDSEL * CBEI3 * /CBEI2 * CBEI1);
HIT               =  MATCH * MEM_EN;
MATCH             = (PCI_AD_HI == BASE_AD_REG);
CFG_WR           := IDSEL * CBEI3 * /CBEI2 * CBEI1 * CBEI0 * /ADI1 * /ADI0 * IDLE
                  + CFG_WR * /IDLE;
CFG_WR.CLK        = CLK;
CFGQ2            := LOAD * /BURST * ADI2
                  + /BURST * CFGQ2
                  + BURST * /CFGQ2;
CFGQ3            := LOAD * /BURST * ADI3
                  + /BURST * CFGQ3
                  + BURST * (CFGQ3 :+: CFGQ2);
CFGQ4            := LOAD * /BURST * ADI4
                  + /BURST * CFGQ4
                  + BURST * (CFGQ4 :+: NODE_C3);
CFGQ5            := LOAD * /BURST * ADI5
                  + /BURST * CFGQ5
                  + BURST * (CFGQ5 :+: NODE_C4);
CFGQ6            := LOAD * /BURST * ADI6
                  + /BURST * CFGQ6
                  + BURST * (CFGQ6 :+: NODE_C5);
CFGQ7            := LOAD * /BURST * ADI7
                  + /BURST * CFGQ7
                  + BURST * (CFGQ7 :+: NODE_C6);
CFG_AD_CNTR.CLK = CLK;
NODE_C3           = (CFGQ3 * CFGQ2);
NODE_C4           = (CFGQ4 * CFGQ3 * CFGQ2);
NODE_C5           = (CFGQ5 * CFGQ4 * CFGQ3 * CFGQ2);
NODE_C6           = (CFGQ6 * CFGQ5 * CFGQ4 * CFGQ3 * CFGQ2);
BASE_AD_REG      := (PCI_AD_HI) * CFG_WR * NODE_CFG_10h
                  + (BASE_AD_REG) * /(CFG_WR * NODE_CFG_10h);
BASE_AD_REG.CLK = CLK;
NODE_CFG_10h      = /CFGQ7 * /CFGQ6 * /CFGQ5 * CFGQ4 * /CFGQ3 * /CFGQ2;
MEM_EN           := (ADI1) * CFG_WR * NODE_CFG_04h
                  + (MEM_EN) * /(CFG_WR * NODE_CFG_04h);
MEM_EN.CLK        = CLK;
NODE_CFG_04h      = /CFGQ7 * /CFGQ6 * /CFGQ5 * /CFGQ4 * /CFGQ3 * CFGQ2;
" Target Sequncer State Machine
" DVSEL is asserted from address hit until either TURN_AR or T_ABORT is
" asserted by the Target agent
/DEVSEL          := (IDLE * /FRAME * CBEI3 * /CBEI2 * CBEI1 * /ADI1 * /ADI0 * IDSEL
                  +  IDLE * /FRAME * /CBEI3 * CBEI2 * CBEI1
                  +  IDLE * /FRAME *  CBEI3 * CBEI2 * /CBEI1
                  +  S_DATA * (/IRDY + /TRDY + FRAMEI) * /T_ABORT
                  +  BACKOFF * FRAMEI * DEVSEL);
DEVSEL.OE         = TRDY_FOE;
DEVSEL.CLK        = CLK;
" Target agent ready to complete current data transaction. TRDY is
" asserted while the Target transfers data (S_DATA) and remains
" asserted while READY asserted  and T_ABORT deasserted
/TRDY            := (S_DATA * (/IRDY + /TRDY) * READY * /T_ABORT * TAR_DLY);
TRDY.OE           = TRDY_FOE;
TRDY.CLK          = CLK;
TRDY_OE          := (IDLE * /FRAME * CBEI3 * /CBEI2 * CBEI1 * /ADI1 * /ADI0 * IDSEL
                  +  IDLE * /FRAME * /CBEI3 * CBEI2 * CBEI1
                  +  IDLE * /FRAME *  CBEI3 * CBEI2 * /CBEI1
                  +  BACKOFF + S_DATA + TURN_AR);
```

```
TRDY_OE.CLK      = CLK;
" Target request Master to stop the current transaction. STOP is
" asserted in response to T_ABORT and remains asserted until entering
" TURN_AR
/STOP            := (BACKOFF + S_DATA * (T_ABORT + TERM) * TAR_DLY);
STOP.OE          = TRDY_FOE;
STOP.CLK         = CLK;
/AD_OE           := (IDLE * /FRAME * CBEI3 * /CBEI2 * CBEI1 * /CBEI0 * /ADI1 * /ADI0 * IDSEL
                 +   IDLE * /FRAME * /CBEI3 * CBEI2 * CBEI1 * /CBEI0
                 +   IDLE * /FRAME *  CBEI3 * CBEI2 * /CBEI1 * /CBEI0
                 + S_DATA * TAR_DLY * RD_WR);
AD_OE.CLK        = CLK;
/T_AD_OE         := (IDLE * /FRAME * CBEI3 * /CBEI2 * CBEI1 * CBEI0 * /ADI1 * /ADI0 * IDSEL
                 +   IDLE * /FRAME * /CBEI3 * CBEI2 * CBEI1 * CBEI0
                 + S_DATA * /T_ABORT * /RD_WR);
T_AD_OE.CLK      = CLK;
RD_WR            := /CBE0 * IDLE
                 + RD_WR * /IDLE;
RD_WR.CLK        = CLK;
" Target Adgent control bits S0 0 - Configuration transfer, 1 - Memory transfer
S0               := IDLE * /FRAME * /CBEI3 * CBEI2 * CBEI1 * /CBEI0
                 + IDLE * /FRAME *  CBEI3 * CBEI2 * /CBEI1 * /CBEI0
                 + S0 * /IDLE;
S0.CLK           = CLK;
PAR_OE           := S_DATA * /TRDY * RD_WR;
PAR_OE.CLK       = CLK;
PERR_OE          := /IRDY * /RD_WR;
PERR_OE.CLK      = CLK;


TARGET_SEQ.clk  = CLK;
state_diagram TARGET_SEQ
"IDLE -- Idle condition.
state    IDLE_: if FRAME then IDLE_
                else if     IDSEL * CBEI3 * /CBEI2 * CBEI1 * /ADI1 * /ADI0
                        + /CBEI3 * CBEI2 * CBEI1 * /ADI1 * /ADI0
                        +  CBEI3 * CBEI2 * /CBEI1 * /ADI1 * /ADI0
                        then S_DATA_
                else BACKOFF_;
"B_BUSY -- Agent not involved in current transaction.
state    B_BUSY_: if FRAME then IDLE_
                  else if /IRDY * /HIT then B_BUSY_
                  else if /IRDY * HIT * (/TERM + READY)
                          then S_DATA_
                  else BACKOFF_;
"S_DATA -- Agent has accepted request and will respond.
state    S_DATA_: if FRAME * (/TRDY + /STOP) then TURN_AR_
                  else if /STOP * (TRDY + /IRDY) then BACKOFF_
                  else S_DATA_;

"TURN_AR -- Completed transaction on bus
state    TURN_AR_: if FRAME then IDLE_
                   else if /HIT then B_BUSY_
                   else if /TERM + READY then S_DATA_
                   else BACKOFF_;
"BACKOFF -- Agent busy unable to respond at this time.
state    BACKOFF_: if FRAME then TURN_AR_
                   else BACKOFF_;
"Unassigned States
state    STATEN1_: goto IDLE_;
state    STATEN2_: goto IDLE_;
state    STATEN3_: goto IDLE_;
end;
```

Appendix B
ABEL Source Code
XC7354 Error Handler

```
module PARITY
title 'PCI Parity Generator Block'

parity device ;

"Inputs
        CLK,PAR_OE,T_CBE0..T_CBE3,T_AD0..T_AD31          pin;
"Outputs
        PAR0..PAR5                                node istype 'reg,xor';
        PAR                                       pin istype 'reg,xor';

xepld PROPERTY 'NODE PAR0 PAR1 PAR2 PAR3 PAR4 PAR5';
xepld PROPERTY 'FASTCLOCK CLK';

PAR_NODE              = [PAR0..PAR5];

@ALTERNATE
XOR_FACTORS    PAR0    =  (T_AD3 :+: (T_AD4 :+: T_AD5));
XOR_FACTORS    PAR     =  (PAR4 + PAR5);

Equations

PAR0     := ((T_AD0 :+: T_AD1) :+: T_AD2) :+: (T_AD3 :+: (T_AD4 :+: T_AD5));
PAR1     := ((T_AD6 :+: T_AD7) :+: T_AD8) :+: (T_AD9 :+: (T_AD10 :+: T_AD11));
PAR2     := ((T_AD12 :+: T_AD13) :+: T_AD14) :+: (T_AD15 :+: (T_AD16 :+: T_AD17));
PAR3     := ((T_AD18 :+: T_AD19) :+: T_AD20) :+: (T_AD21 :+: (T_AD22 :+: T_AD23));
PAR4     := ((T_AD24 :+: T_AD25) :+: T_AD26) :+: (T_AD27 :+: (T_AD28 :+: T_AD29));
PAR5     := ((T_AD30 :+: T_AD31) :+: T_CBE0) :+: (T_CBE1 :+: (T_CBE2 :+: T_CBE3));
PAR_NODE.CLK = CLK;

PAR      := ((PAR0 + PAR1) :+: (PAR2 + PAR3)) :+: (PAR4 + PAR5);
PAR.CLK  = CLK;
PAR.OE   = PAR_OE;

end
```

XILINX®

Designing with the XC7336 and XC7318

March 1995

Application Note

Introduction

The Xilinx XC7336 and XC7318 are high speed EPLDs capable of solving a wide range of logic and state machine problems for today's high-performance digital systems. This application note presents an explanation of the parts, a series of useful design examples and practical details for designing successfully with these parts.

XC7336/XC7318 Architecture

The XC7336 includes 36 macrocells arranged in four blocks and supports pin-to-pin speeds as fast as 5 nanoseconds and clock rates up to 167 MHz. I/O signals can interface with 5 V, 3.3 V or both levels. Current software support includes XEPLD, ABEL and CUPL and additional 3rd party schematic and simulation environments.

Figure 1 shows the global architecture of the Xilinx XC7336. Note the regular structure of four similar high speed function blocks, centrally connected by the Universal Interconnect Matrix (UIM™) and surrounded by pins.

Signals enter and exit on the pins, form logic operations within the function blocks and form connections and logic operations within the UIM. Each section will be briefly discussed, to show key functionality.

The Interconnect Structure

There are at least three hierarchical sets of signal paths:

Local - within the function blocks

Global - the UIM

Global - Fast inputs

Interconnect Within Function Blocks

Function blocks have 24 input sites. The blocks receive signals from the UIM, local macrocell feedback, block input pins and 12 global fast input pins. Most signals are multiplexed before block entry. The logic blocks themselves can generate 9 signals per function block from the 9 macrocells within each block. Each macrocell signal can drive its own dedicated I/O pin and/or feedback locally within the function block as well as globally by entering the UIM.
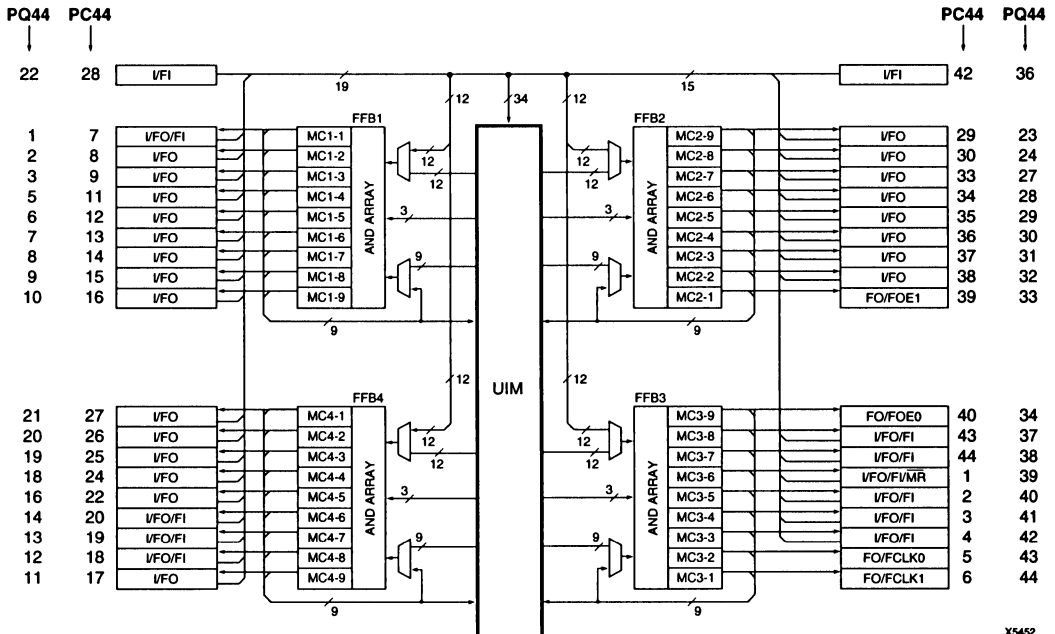
Figure 1. XC7336 Architecture

The UIM

The UIM is a crosspoint switch. Every signal entering it can connect to any line exiting it. The UIM has 24 exit points per function block, giving 96 exit points for the XC7336. Any entering signal can be connected to any of the outgoing lines, giving no connection restrictions within the UIM.

The Fast Inputs

Distributed around the XC7336 is a group of 12 fast input lines. Each line is sourced from a separate pin and directly attached to multiplexers driving into the function blocks. By assigning signals to these input pins, the fastest possible propagation delays occur across the function blocks. Twelve fast input pins covers the largest number of applications requiring fast inputs, and is ideal for fast address decode needs of today's high speed microprocessor systems.

The Logic Block

The function blocks are groups of 9 macrocells. The 9 macrocells share common input points from the UIM, groups of 9 pins and neighboring product term multiplexers. Each macrocell (Figure 2) within the block is assigned 5 product terms that can be used in a number of ways. The macrocell outputs can then drive output pins and/or feedback to both the UIM and the function block in which it resides.

The Macrocell

In the default mode, there are 4 product terms that OR together driving the D input to the macrocell flip flop. This configuration permits the fifth product term to be assigned either to the asynchronous set or reset of the flip flop. This first configuration is the most common one.

Another configuration is to export the 4 product-term cluster to a neighbor, increasing the neighbor's available product terms by 4. Product term exporting is shown in Figure 3. Across the block of 9 macrocells, it is possible to assign all product terms to a single macrocell, taking its total to 36 product terms.

When exporting is used, the remaining product term is reassigned to the D input of the exporting flip flop passing through a series EX-OR gate. By driving one leg of the EX-OR gate with a logical one, the EX-OR inverts making a "NAND" gate at the D input. This remaining logic permits the exporting macrocell to form sums of products when driven from UIM-generated logic.

XC7336 macrocells can also be transformed into T flip flops. The software automatically configures the Q to be

Figure 2. XC7336/XC7318 Macrocell Architecture

X5218
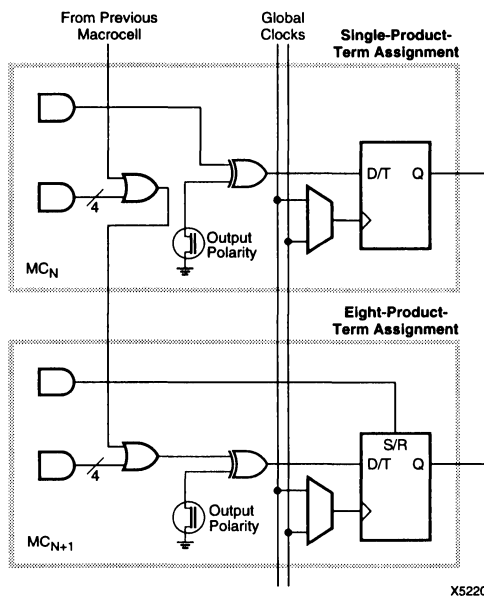
Figure 3. Product Term Exporting

inverted back through a multiplexed EX-OR gate at the D flip flop input. This permits efficient counters to be built using but a few gates to drive the state transitions.

The XC7318 macrocell is identical to the XC7336, but the XC7318 provides half of the number in the same package. Figure 4 shows the XC7318 architecture and Table 1 summarizes key supported features.

Table 1: Key XC7336/XC7318 Features

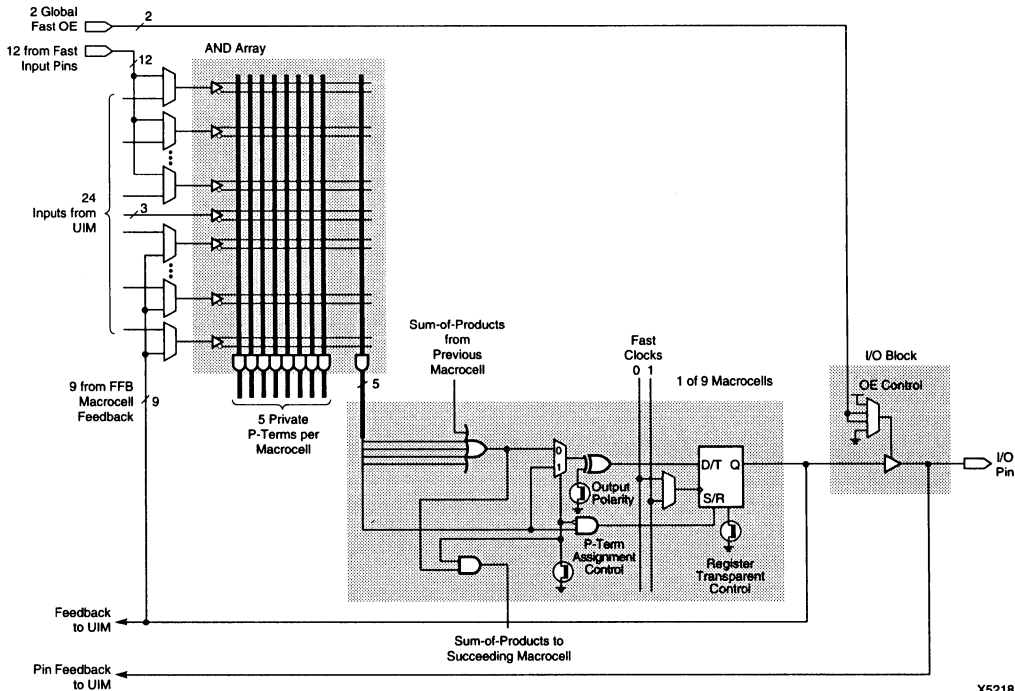| Feature	XC7336	XC7318
Fast Function Blocks	4	2
Fast Inputs	12	12
Fast Clocks	2	2
Fast Output Enables	2	2
3.3 V/5.0 V I/O	Yes	Yes
T_{pd} (Fast In to Fast Out)	5.0/7.5/10/12 ns	5.0/7.5 ns
T_{pd} (I or I/O to Outputs)	8.5 ns	8.5 ns
F_{max}	167 MHz	167 MHz
Number of I/Os	38	38
Current Drive	24 mA	24 mA

Designers needing input registers, additional function block product terms, more macrocells and built in arithmetic operations should try the XC7354. The XC7354 offers more functionality than the XC7336/XC7318 and comes in 44-pin and 68-pin packages.

Table 2 shows the pin functionality of the XC7318, the XC7336 and the XC7354. The righthand column summarizes the common functions of all three chips. By using the recommended pin assignment on the righthand side, for 44-pin designs, an important capability can be had. Specifically, designs can be simply migrated among the 3 parts. For instance, designs wanting minimum density can use the XC7318. Greater density with equivalent speed can be gained by using the XC7336 and still greater density can be had by using the XC7354. Should a design initially target the XC7318, the exact same design can be moved into the other parts, if additional capability is required.

Timing
Figure 5 shows the timing model for the XC7336/XC7318. Multiple paths are represented from input pin to output pin, depending upon whether signals are assigned to pass through the UIM, bypass the D flip flop, incorporate product term exporting and so forth. There are relatively few combinations, but each signal should be tallied separately for its pin to pin time delay, as needed. As an example, tally the time delay of three different signals:

1. Pin-to-pin, fastest path:

$$Tdelay = t_{in} + t_{flogi} + t_{fpdi} + t_{fout}$$

2. Pin-to-Pin delay through the UIM:

$$Tdelay = t_{in} + t_{uim} + t_{flogi} + t_{fpdi} + t_{fout}$$

3. Pin-to-Pin with two levels of p-term exporting:

$$Tdelay = t_{in} + t_{flogi} + 2\, t_{ptxi} + t_{fpdi} + t_{fout}$$

Design Techniques

Automatic Software
The design examples presented are shown using PLUS-ASM which is simple and easy to understand. Typically, designers don't need to designate specific function mapping into the XC7336/XC7318 , but occasionally, designers like to control how a solution is implemented, so these methods may be of interest.

Boolean operators used by PLUSASM are simply /,+ and * for INVERT, OR and AND, respectively. Combinational logic expressions are formed with a simple equal (=) sign, with operands and operators located on the right hand side of the expression. It is possible to use the / operator on the left hand side of an equation, for brevity, when needed.

Flip flop expressions are formed by writing expressions for the specific control pins of the flip flop. The D-input is a special case, where the equal sign is replaced by the compound symbol :=. Clock inputs are determined by the syntax FFname.clkf, and reset inputs are designated by FFname.rstf.

Table 2. Recommended 44-Pin Interchange

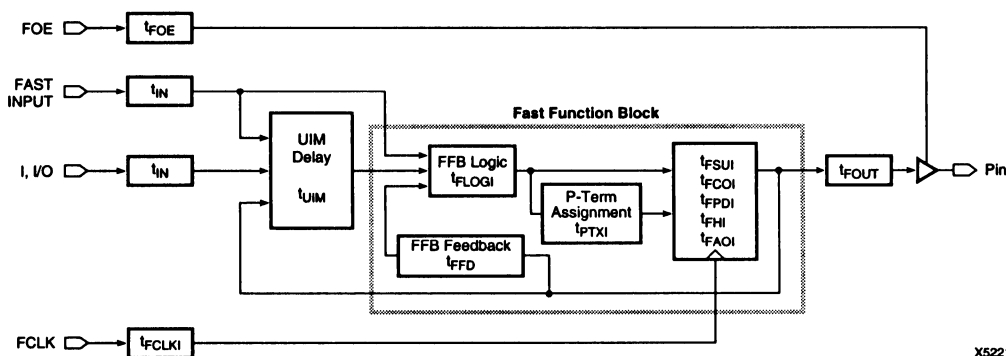| Pin Number	XC7336	XC7318	XC7354	Recommended
1	I/FO/FI/(/MR)	I/FI/(/MR)	I/FI/(/MR)	I/(/MR)
2	I/FO/FI	I/FI	I/FI	I/FI
3	I/FO/FI	I/FI	I/FI	I/FI
4	I/FO/FI	I/FI	I/FI	I/FI
5	FO/FCLK0	FCLK0	O/FCLK0	FCLK
6	FO/FCLK1	FCLK1	O/FCLK1	FCLK
7	I/FO/FI	I/FO/FI	I/FI	I/FI
8	I/FO	I/FO	I/FO	I/FO
9	I/FO	I/FO	I/FO	I/FO
10	GND	GND	GND	GND
11	I/FO	I/FO	I/FO	I/FO
12	I/FO	I/FO	I/FO	I/FO
13	I/FO	I/FO	I/FO	I/FO
14	I/FO	I/FO	I/FO	I/FO
15	I/FO	I/FO	I/FO	I/FO
16	I/FO	I/FO	I/FO	I/FO
17	I/FO	I	I/O/FI	I
18	I/FO/FI	I/FI	I/O/FI	I
19	I/FO/FI	I/FI	I/O/FI	I
20	I/FO/FI	I/FI	I/O/FI	I/O
21	V$_{CCINT}$	V$_{CCINT}$	V$_{CCINT}$	V$_{CCINT}$
22	I/FO	I	I/FI	I/O
23	GND	GND	GND	GND
24	I/FO	I	I/FO	I
25	I/FO	I	I/FO	I
26	I/FO	I	I/FO	I
27	I/FO	I	I/FO	I
28	I/FI	I/FI	I/FI	I/FI
29	I/FO	I/O	I/FO	I/O
30	I/FO	I/O	I/FO	I/O
31	GND	GND	GND	GND
32	V$_{CCCIO}$	V$_{CCCIO}$	V$_{CCCIO}$	V$_{CCCIO}$
33	I/FO	I/O	I/FO	I/O
34	I/FO	I/O	I/FO	I/O
35	I/FO	I/O	I/FO	I/O
36	I/FO	I/O	I/FO	I/O
37	I/FO	I/O	I/FO	I/O
38	I/FO	I/O	I/FO	I/O
39	FO/FOE1	O/FOE1	O/(/CKEN0)	O
40	FO/FOE0	FOE0	O/FOE0	FOE
41	V$_{CCINT}$	V$_{CCINT}$	V$_{CCINT}$/V$_{PP}$	V$_{CCINT}$
42	I/FI	I/FI	I/FI	I/FI
43	I/FO/FI	I/FO/FI	I/FI	I/FI
44	I/FO/FI	I/FO/FI	I/FI	I/FI

Figure 4. XC7318 Block Diagram

Figure 5. XC7336/XC7318 Timing Model

A design file contains a header section including optional documentation sections and mandatory declaration of inputs, outputs, global signals and any user preferred arrangement of functions. The interested reader is referred to the 1994 XEPLD Design Guide for further details.

SMARTswitch™
SMARTswitch is the automatic XEPLD software that places logic into the UIM. As single lines enter the UIM, they are assigned to function block inputs, making connections. However, multiple lines driving a UIM connection form a wired AND function, that is useful for making additional logic. Forming UIM logic will be illustrated in the Counter and Comparator examples shown later.

Gates
The following expressions show the basic logic operations.

$$ABAR = /A;$$
$$AORB = A+B;$$
$$AANDB = A^*B;$$
$$/ANORB = A+B;$$
$$/ANANDB = A^*B;$$
$$AEXORB = /A^*B + A^*/B;$$
$$AEXNORB = A^*B + /A^*/B;$$

Muxes and Decoders
Using the above methods, compound expressions are formed to build up logic functions. Using A0 to A3, B0 to B3 and SEL (select) as inputs, a multiplexer follows:

DAT0 = SEL*A0 + /SEL*B0;
DAT1 = SEL*A1 + /SEL*B1;
DAT2 = SEL*A2 + /SEL*B2;
DAT3 = SEL*A3 + /SEL*B3;

The approach extends to larger multiplexers. The above uses one macrocell per data bit, and leaves behind two unused product terms in each macrocell. To take advantage of four product terms per macrocell, the idea expands as follows:

DAT0 = S1*S0*D0 + S1*/S0*C0 + /S1*S0*B0 + /S1*/S0*A0

DAT1 = S1*S0*D1 + S1*/S0*C1 + /S1*S0*B1 + /S1*/S0*A1

DAT2 = S1*S0*D2 + S1*/S0*C2 + /S1*S0*B2 + /S1*/S0*A2

DAT3 = S1*S0*D3 + S1*/S0*C3 + /S1*S0*B3 + /S1*/S0*A3

Very high speed decoders can be built in the macrocells, to form SRAM select signals, but do not use all of the macrocell product terms or the flip flop in most cases. Decoders are formed as follow:

DEC0 = /A3*/A2*/A1*/A0
DEC1 = /A3*/A2*/A1*A0;
DEC2 = /A3*/A2*A1*/A0;

Using Equation 1 from the Timing section, we can determine the time delay required to generate DEC0,1 or 2 as follows for the XC7318-5:

t_{in} = 1.5 ns
t_{flogi} = 1 ns
t_{fpdi} = 0.5 ns
t_{fout} = 2.0 ns

Tdelay = 1.5 + 1 + 0.5 + 2 = 5 ns

Registers=
Simple registers are formed as follows:

A:= DATAINPUT;
A.CLKF = CLOCK;
A.RSTF = RESET;

This describes a D flip flop with its input tied to something named DATAINPUT, its clock tied to a signal called CLOCK and its reset input tied to a signal called RESET.

Shift Registers

Cascading registers results in a shift register, as follows:

    A:=DATAINPUT;

    B:=A;

    C:=B;

    D:=C;

    A.CLKF = CLOCK;

    B.CLKF = CLOCK;

    C.CLKF = CLOCK;

    D.CLKF = CLOCK;

    A.RSTF = RESET;

    B.RSTF = RESET;

    C.RSTF = RESET;

    D.RSTF = RESET;

This shifter uses four macrocells, and if the signals designated A,B,C,D are declared as outputs, they will appear somewhere at the pins of an XC7336/XC7318. If A,B,C and D are declared as nodes (internal points), the software buries them.

Counters

Counters can be built in a number of different ways. The most efficient is to have the macrocell flip flops configured as T flip flops. The following equations form T flip flops, add logic to load the flip flops, and include a term permitting the counter to be paused (CE = Count Enable):

Q0.T = LOAD */CE*D0*/Q0 +
LOAD*/CE*/D0*Q0 + /LOAD*CE
Q0.CLKF = CLOCK
Q0.RSTF = RESET

Q1.T = LOAD */CE*D1*/Q1 +
LOAD*/CE*/D1*Q1 + /LOAD*CE *Q0
Q1.CLKF = CLOCK
Q1.RSTF = RESET

Q2.T = LOAD */CE*D2*/Q2 +
LOAD*/CE*/D2*Q2 + /LOAD*CE*Q0*Q1
Q2.CLKF = CLOCK
Q2.RSTF = RESET

Q3.T = LOAD */CE*D3*/Q3 +
LOAD*/CE*/D3*Q3 +/LOAD*CE*Q0*Q1*Q2
Q3.CLKF = CLOCK
Q3.RSTF = RESET

Q4.T = LOAD */CE*D4*/Q4 +
LOAD*/CE*/D4*Q4+/LOAD*CE*Q0*Q1*Q2*Q3
Q4.CLKF = CLOCK
Q4.RSTF = RESET

Q5.T = LOAD */CE*D5*/Q5 +
LOAD*/CE*/D5*Q5 + /LOAD*CE*Q0*Q1*Q2*Q*Q4
Q5.CLKF = CLOCK
Q5.RSTF = RESET

Q6.T = LOAD */CE*D6*/Q6 +
LOAD*/CE*/D6*Q6 + /LOAD*CE*Q0*Q1*Q2*Q3*Q4*Q5
Q6.CLKF = CLOCK
Q6.RSTF = RESET

Q7.T = LOAD */CE*D7*/Q7 +
LOAD*/CE*/D7*Q7 + /
LOAD*CE*Q0*Q1*Q2*Q3*Q4*Q5*Q6
Q7.CLKF = CLOCK
Q7.RSTF = RESET

Q8.T = LOAD */CE*D8*/Q8 +
LOAD*/CE*/D8*Q8 + /
LOAD*CE*Q0*Q1*Q2*Q3*Q4*Q5*Q6*Q7
Q8.CLKF = CLOCK
Q8.RSTF = RESET

Count bits Q0 through Q8 fit nicely into a function block. To cascade into the next function block, an additional term is needed, that passes the all one condition of the low order bits. The term is called CO.

Before adding in the CO term, the fastest frequency that a 9 bit counter can achieve will be calculated. This is derived from Figure 5 by tallying the logic time delay (t_{flogi}), with the flip flop required times for setup (t_{su}) , clock to output (tcoi) and the feedback time delay (t_{ffd}). This results in a timing requirement as follows:

$$T_{delay} = t_{flogi} + t_{su} + t_{coi} + t_{ffd}$$

Using timing values for the 7.5 ns version of the XC7318 gives a calculation of the loop time delay as follows:

$t_{flogi} = 1.5$ ns
$t_{su} = 1.5$ ns
$t_{coi} = 1$ ns
$t_{ffd} = 4$ ns
$T_{delay} = 1.5 + 1.5 + 1 + 4 = 8$ ns

The reciprocal of this is the fastest operating frequency the nine bit version of the counter can achieve:

Fmax = 1/(8 ns) = 125 MHz

Adding in the CO term is done by logically ANDing through the UIM.

CO =
Q0*Q1*Q2*Q3*Q4*Q5*Q6*Q7*Q8

Q9.T = LOAD */CE*D9*/Q9 +
LOAD*/CE*/D9*Q9 + /LOAD*CE*CO
Q9.CLKF = CLOCK
Q9.RSTF = RESET

Q10.T = LOAD */CE*D10*/Q10 +
LOAD*/CE*/D10*Q10 + /LOAD*CE*CO*Q9
Q10.CLKF = CLOCK
Q10.RSTF = RESET

In this design, the first 9 bits (Q0 - Q8) reside within an XC7336/XC7318 function block. Each flip flop toggles on the clock when its CE signal is a logic one and all flip flops of lower position are logically one. The condition of all lower bits being logical one is decoded by the AND of the particular bits, that are broadcast among the macrocells within the function block. When nine bits are reached in the counter design, a tenth bit must be conditioned for toggle by sending the term CO from one function block to another. The software automatically forms the AND gate logic for CO in the UIM and passes it as a single signal into the next function block. Figure 6 shows the UIM cascade with CO passed from one function block to another.

Timing for the expanded counter is altered by replacing the local feedback expression t_{FFD} with the time delay of a signal passing through the UIM, t_{UIM}. This value is 4.5 ns, taking the total loop delay to 8.5 ns resulting in a Fmax of 117 MHz.

The above counter design shows the regular pattern needed by an 11 bit up counter. The pattern is easily expanded for up to 36 bits in an XC7336 or 18 bits in an XC7318, and may be converted to a down counter by taking the /Q outputs outside and complementing the data being loaded. Note that two product terms are needed to load the flip flops, because T flip flops require both input data senses to load.

Comparators
Comparators are easily handled by the XC7336/ XC7318 macrocell, but single bit comparators do not use all available macrocell product terms. A more efficient use is to handle four bits at a time to generate multiple compares per macrocell:

COMP = /B1*/B0*/A1*/A0 +
B1*/B0*A1*/A0
/B1*B0*/A1*A0 +
B1*B0*A1*A0

Next, several COMP signals can be gated together to detect equality across larger groups of bits. Each group of four bits uses 4 function block inputs, meaning six four bit compares can occur per function block. Another macrocell or the UIM then forms the composite function of all the bit compares, as needed.
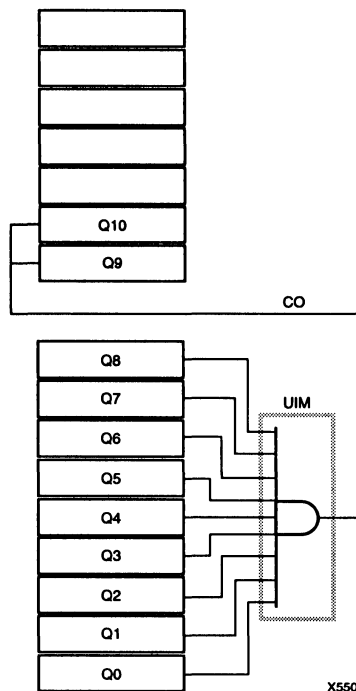
Figure 6. UIM Counter Cascade

An efficient comparator can be built using a slightly different strategy, appropriate for microprocessor address decoding. Assume a 12 bit operand (A0 - A11) resides in other function blocks than the compare function block. This value is registered, and may be compared very quickly to another 12 bit operand (B0 - B11) applied to the fast inputs, forming a low asserted compare signal at the function block output pin. The scheme works using the logical OR of multiple Exclusive OR functions. Each macrocell uses all four product terms, with automatic product term cascading. This approach takes 11 ns on the XC7336-7 part, and the output /COMP signal can be tied directly to chip enables on external memory chips. See Figure 7.

/COMP = A0*/B0 + /A0*B0
+ A1*/B1 + /A1*B1
+ A2*/B2 + /A2*B2
+ A3*/B3 + /A3*B3
+ A4*/B4 + /A4*B4
+ A5*/B5 + /A5*B5
+ A6*/B6 + /A6*B6
+ A7*/B7 + /A7*B7
+ A8*/B8 + /A8*B8
+A9*/B9 + /A9*B9
+ A10*/B10 + /A10*B10
+ A11*/B11 + /A11*B11
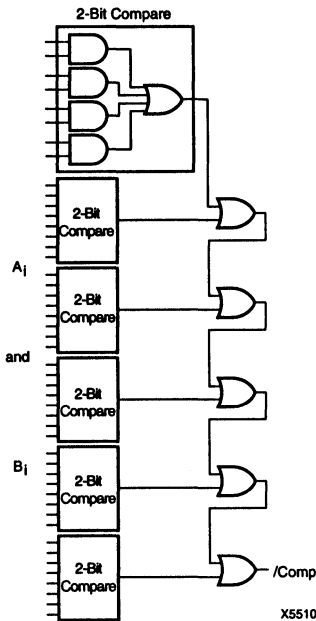
Figure 7. 12-Bit Comparator

Latches

Occasionally, designers need a transparent latch within an XC7336 or XC7318. The latch is formed by feeding the macrocell combinatorial logic back upon itself per the following equation:

$$Q = ENA^*DATA + /ENA^*Q + Q^*DATA$$

Note that the signal Q^*DATA is included to eliminate a hazard, making Q glitch free.

Merged Mux/Latches

Latches often occur when driven from multiplexers. When this happens, the MUX can be embedded right into the latch making a combined function that is faster than the stacked function and more efficient. The following equation merges a 2 to 1 multiplexer into the latch operation.

$$Q = DAT1^*SEL^*ENA + DAT0^*/SEL^*ENA + Q^*/ENA$$

Clock Tricks

Building latches is one way of introducing an additional clock signal, but designers often need to introduce product term clocks. P-term clocks can be formed by simply building a logic expression, which will be formed at a macrocell, and designating that logic expression as another flip flop's clock input. The software will automatically assign the clocking logic to the FCLK0 or FCLK1 pin, where the macrocell output is redirected back into the EPLD and assigned as designated.
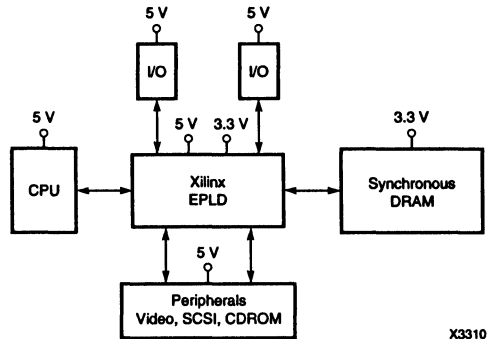
Figure 8. Typical Mixed Voltage System

Practical Considerations for XC7336/XC7318 Designs

The XC7336/XC7318 offer additional capability not highlighted by the previous discussions. Systems using 3.3 volt and 5 volt devices are easily interfaced with the XC7336 / XC7318, by following a few simple rules. Also, very high speed EPLDs behave much better if standard high performance printed circuit board techniques are adhered to, so a small checklist is appropriate for those rules. And finally, best EPLD behavior is obtained by following a few guidelines with respect to the Master Reset (/MR) and power on Master Reset capabilities of the XC7336 and XC7318.

Mixed Voltage Operation

Xilinx EPLDs support mixed voltage systems similar to that shown in Figure 8 combining both 3.3 and 5 Volt components. Xilinx EPLDs combine both logic and level shifting functions in a single programmable device, eliminating the need for discrete level translation buffers. These EPLDs feature split power supply rails. The internal core logic always runs at 5 volts for the fastest possible performance. The output buffers can be powered by either 5 volts or 3.3 volts by connecting the I/O V_{CC} to a 3.3 volt or 5 volt supply. True TTL compatibility allows the EPLDs to drive and be driven by any combination of 3.3 and 5 volt logic without any performance penalty, even when the I/O V_{CC} pins are powered by 3.3 volts.

The Xilinx EPLD I/O structure is shown in Figure 9. Input protection diodes connect to the internal 5 volt power supply rail, not the output buffer supply rail. This allows the input to withstand a maximum voltage of 7 volts, even when the I/O power pins connect to 3.3 volts. Since both output transistors are N-channel devices, there is no parasitic diode to be forward biased if the output is 3-stated and a 5 volt device is driving the EPLD I/O pin.

This enables the EPLD to operate on a bus that includes both 3.3 V and 5 V devices.
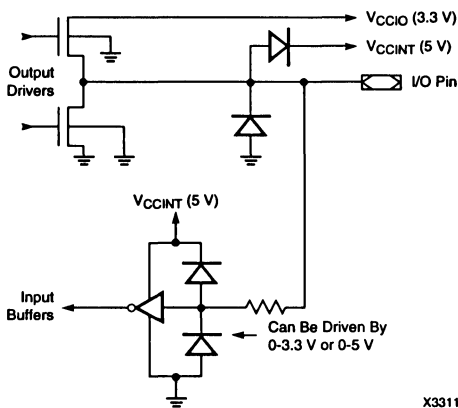
Figure 9. Xilinx EPLD I/O Structure

Mixed voltage power supplies may ramp-up simultaneously, or in either order. In all CMOS devices, current flows through the input pin protection circuitry if pins are driven before V_{CCINT} is applied. In the XC7336/XC7318, no damage will occur if the input current is less than 150 mA/pin. However, the user is advised to power-up all system power supplies simultaneously, thereby minimizing input transient currents.

Xilinx EPLDs are TTL-compatible with 3.3 and 5 volt logic as shown in Figure 10. The 5 volt TTL logic input thresholds are VIH = 2.0 V and VIL = 0.8 V. Xilinx EPLDs drive HIGH greater than 2.4 V and LOW below 0.4 V at rated output drive currents, with at least 400 mV noise margin.

High Speed Design Considerations

The XC7336/XC7318 are offered in both 7.5 and 5 nanosecond versions. These very high speed parts have guaranteed maximum time delays that are 7.5 and 5 nanoseconds, and actual parts may in fact be somewhat faster. Because of this speed, additional care should be taken when using these parts, so that adjoining chips will operate properly.

Many high speed designs also require high current drive outputs for handling capacitive loads. The XC7336/XC7318 provide 24 mA drivers to eliminate the need for additional buffering that would decrease their speed. This results in a need to manage the total current being switched, so a strategy to do that is provided.

As with other high speed logic devices, the XC7336/XC7318 should use low inductance capacitors located as close as possible to the XC7336/XC7318 V_{CC} and GND pins when mounted on a PC board. Care should be taken to mount the devices so that the PC interconnect traces are as close as possible to the target signal destinations.

Layout Checklist:

Complying with the following checklist should assure a successful design with an XC7336 / XC7318:

1. Tie unused inputs (except master reset) to ground. An unused master reset should be tied high. Do not use the -u option in XEPLD.

2. Locate XC7336 / XC7318 parts near chips they drive or are driven from to minimize transmission line effects.

3. Use wide spacing between fast signal lines (particularly clocks) to minimize crosstalk.

4. Power pins (V_{CC} and GND) are recommended to be placed on separate printed circuit board planes. Fast signals should reside on another plane, as well.

5. Decouple the chip V_{CC} with a 0.1 microfarad capacitor directly connecting each physical chip V_{CC} to the nearest ground plane. Low inductance, surface mounted capacitors are recommended.

6. Decouple the printed circuit board power inputs with 0.1 uF ceramic (high frequency) and 100 uF electrolytic (low frequency) filter capacitors.

7. All device ground pins must be connected together.

8. Avoid using sockets to attach XC7318 and XC7336 parts to the PCB. Direct soldered connection minimizes inductance and reduces ground rise.

Managing Ground Rise

Today's high performance designers must also be aware of additional factors that can affect the performance of fast, high current drive systems. As mentioned earlier, possible voltage rise on the ground pins of a device can affect the output levels being driven as well as sensed by the switching EPLD.

Figure 11 shows how ground rise is typically observed with today's high performance EPLDs. In this setup, multiple outputs are switched with a control variable, while one output is constantly being driven low and observed. As the multiple outputs switch, their in rushing current converges at the ground pin(s) of the EPLD. Lead impedance causes the reference ground to develop a voltage higher than before the switching outputs occurred. The result is that the static output being observed also develops an observable voltage swing.

All digital ICs have this property, and it causes no harm to the system unless the voltage swing on the static output is capable of switching another circuit down the line. Problems can occur if the voltage swing is excessive and this effect is particularly significant if the static (quiet) signal is attached to another circuit's clock input.

There are at least two factors that contribute to this ground rise. First, the amount of capacitive load being

Input and Output Breakdown
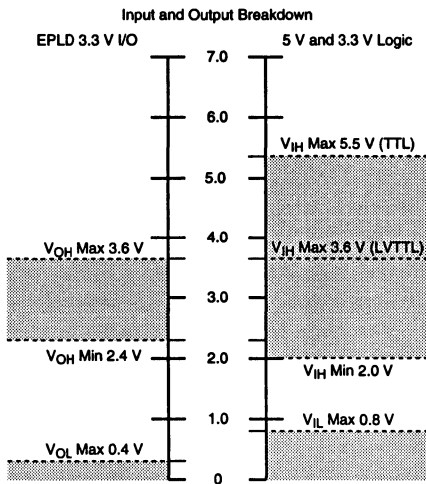
Figure 10. Xilinx EPLD Driving 3.3 V and 5 V Components

driven is important because charge on this capacitance is the source of the in rushing current. Second, the number of simultaneous switching outputs is a factor because each switching output adds to the total capacitance being discharged.

Unlike typical fast PLDs (shown switching in Figures 12 and 13), Xilinx EPLDs are not supplied in DIP packages with only a single ground. Xilinx EPLDs are supplied in symmetric packages that minimize lead inductance and supply multiple ground pins.

The XC7336 and XC7318 each have three grounds. Additional grounds and superior packages permit more outputs to switch simultaneously than other fast PLDs.

Figure 14 a and b show the XC7336-5 switching various numbers of outputs with a statically observed output responding similarly to those shown in Figures 12 and 13. Note that Figure 14 a and b have each output driving an 80 pF load, and that the small ground rise on the "static" output is less than that of Figures 11 and 12 where fewer outputs, driving less load capacitance result in greater ground rise on the static output. In summary, for AMD the ground rise is 1.66 V, for Lattice it is 2.0 V but the XC7336-5 has only 0.72 V.

The following checklist will reduce unnecessary ground rise:

1. Pinout only essential outputs. Intermediate shifter bits, and counter bits that need not drive outputs should remain buried.
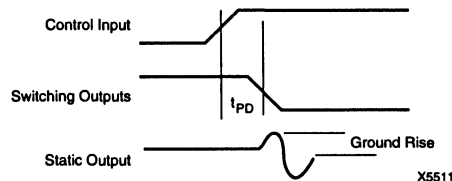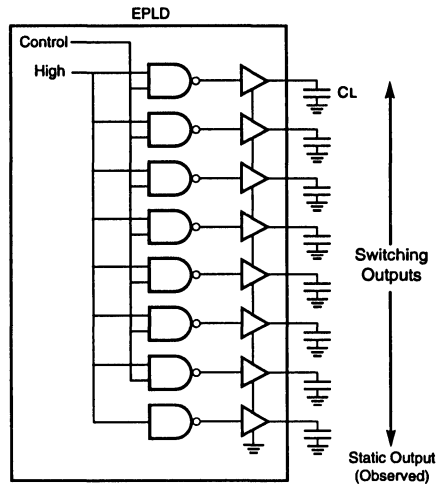
Figure 11. Ground Rise Test

2. Minimize the number of outputs switching simultaneously. This can be accomplished by skewing the output enable signals FOE0 and FOE1. One way to do this is to simply route an enable to FOE0, and pass the same enable signal through a macrocell for delay, to drive FOE1. This is shown in Figure 15 and results in one TPD of time delay.

3. The two fast clock inputs can be managed similar to the two FOE signals, by delaying one of the clocks to gain signal skew.

4. Additional grounding can lower ground rise effects, and may be dealt with simply. Unused outputs can be tied directly to the PCB ground and driven low using internal logic. This splits the current driven into heavily loaded ground pins and lowers the voltage rise.

Master Reset and Power On Master Reset
The XC7336/XC7318 devices undergo a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the /MR pin is tied to V_{CCINT},
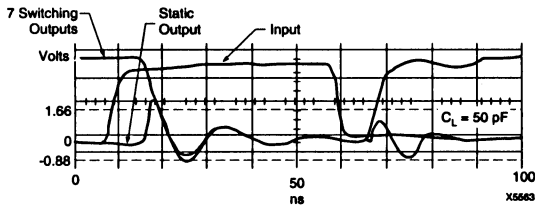
Figure 12. AMD PALCE 16V8H-7

the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If /MR is held low while the device is powering up, the internal initialization sequence begins and the outputs will remain 3-stated until the sequence is complete and /MR is brought HIGH. V_{CC} rise must be monotonic to insure the initialization sequence is performed correctly.
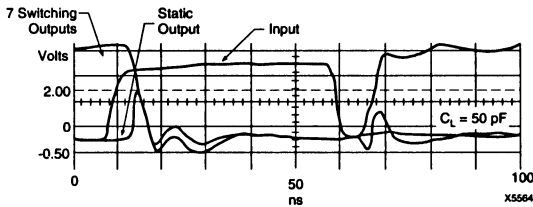
Figure 13. Lattice GAL 16V8-10
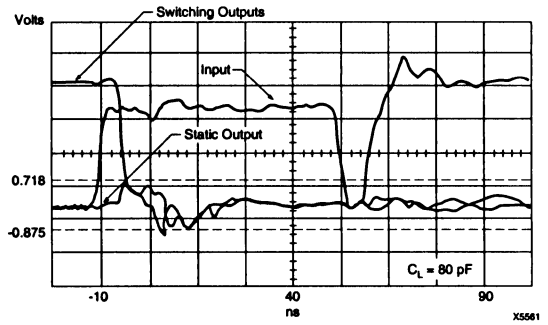
Figure 14a. XC7336-5 (Seven Switched Outputs)
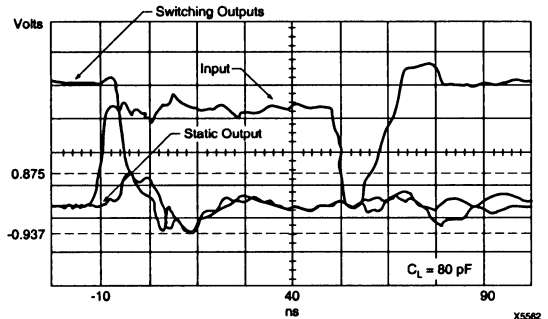
Figure 14b. XC7336-5 (12 Switched Outputs)
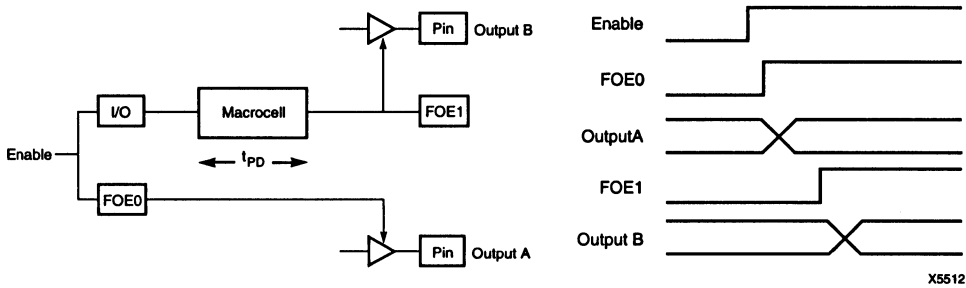
Figure 15. Output Enable Skewing Technique

Figure 16 shows a nonmonotonic rising supply voltage, that can adversely affect an XC7336/XC7318 during its power on initialization sequence.
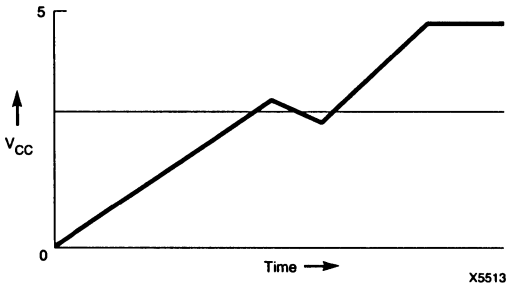
Figure 16. Nonmonotonic V_{CC}

For additional flexibility, the /MR pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of /MR, all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and /MR is brought HIGH. The minimum /MR pulse is t_{WMR}. If /MR is brought high after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}. If /MR is used, it must be driven from a 5 V signal.

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Using Xilinx EPLDs in Mixed Voltage Systems

March 1995　　　　　　　　　　　　　　　　　　Application Note

Introduction

To meet the demand for higher performance, higher integration and reduced power consumption, the semiconductor industry is moving rapidly toward a 3.3 volt nominal voltage standard. This new standard allows for the retention of TTL threshold levels while providing improved performance, noise levels, reliability and power consumption.

While 3.3 volt systems were synonymous with portable and notebook computers in the past, 3.3 volt components are rapidly finding their way into desktop PCs and high performance system applications (e.g. Green PCs and high memory bandwidth systems based on synchronous DRAMs). Even though there are many 3.3 volt components available, systems will still require a mix of 3.3 and 5 volt logic as shown in Figure 1.

Xilinx EPLDs combine both logic and level shifting functions in a single programmable logic device, eliminating the need for performance-robbing discrete level translation buffers. These EPLDs feature split power supply rails. The internal core logic always runs at 5 volts for the fastest possible performance. The output buffers can be powered by either 5 volts or 3.3 volts by connecting the I/O V_{CC} pins to a 3.3 volt or 5 volt supply. True TTL compatibility allows the EPLDs to drive and be driven by any combination of 3.3 and 5 volt logic without any performance penalty, even when the I/O V_{CC} pins are powered by 3.3 volts.

Xilinx EPLD I/O Characteristics

The Xilinx EPLD I/O structure is shown in Figure 2. The input protection diode is connected to the internal core logic 5 volt power supply rail, not the output buffer supply rail. This allows the input to withstand a maximum voltage of 7 volts, even when the I/O power pins are connected to 3.3 volts. Since both output driver transistors are N-channel devices, there is no parasitic diode to be forward biased if the output is 3-stated and a 5 volt device is driving the EPLD I/O pin. Since the input protection circuitry is powered by the 5 volt core logic supply pins, the 5 volt supply must always be powered up at the same time voltage is applied to the I/O pins.

The Xilinx EPLD worst case performance is specified identically for both 3.3 and 5 volt I/O power supplies. The output drive capability exceeds the LVTTL requirements (-2 mA @ V_{OH} min = 2.4 V and 2 mA @ V_{OL} max = 0.4 V) specified in JEDEC standard JESD8-1A. The following curves show typical drive characteristics for the XC7236A.
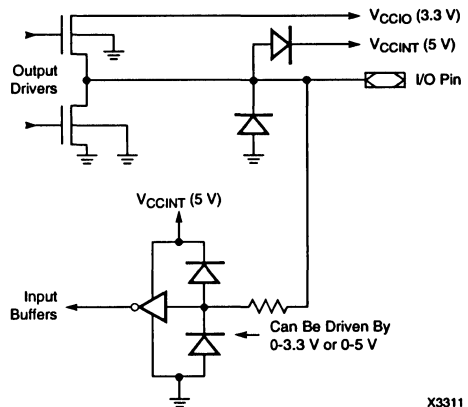
Figure 2. Xilinx EPLD I/O Structure

Figure 1. Typical Mixed Voltage System Using Xilinx EPLDs
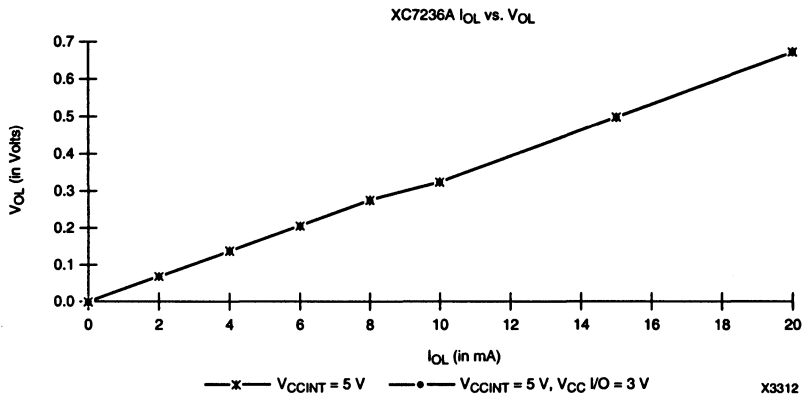
Figure 3. Typical Output Low Characteristics
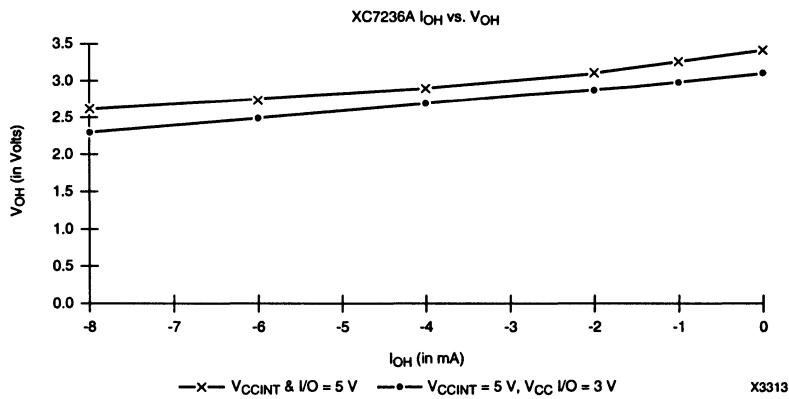
Figure 4. Typical Output High Characteristics
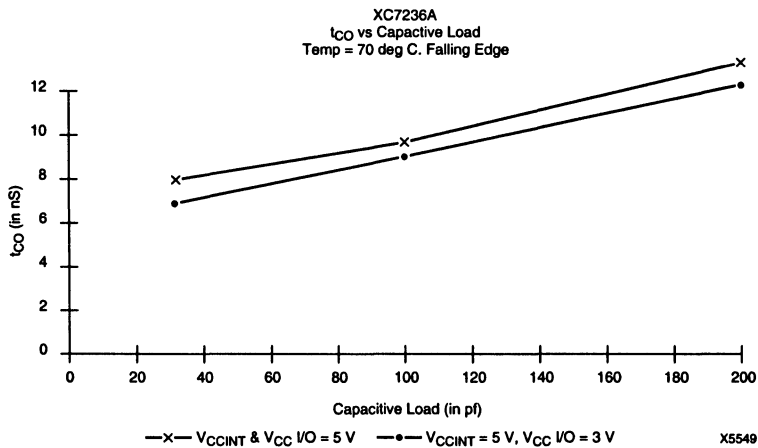
Figure 5. Typical Clock-to-Output (t_{CO}) vs Capacitive Loading (High-to-Low Transition)

XC7236A
t_{CO} vs Capacitive Load
Temp = 70 deg C. Rising Edge

—x— V_{CCINT} & V_{CC} I/O = 5 V   —•— V_{CCINT} = 5 V, V_{CC} I/O = 3 V   X5551
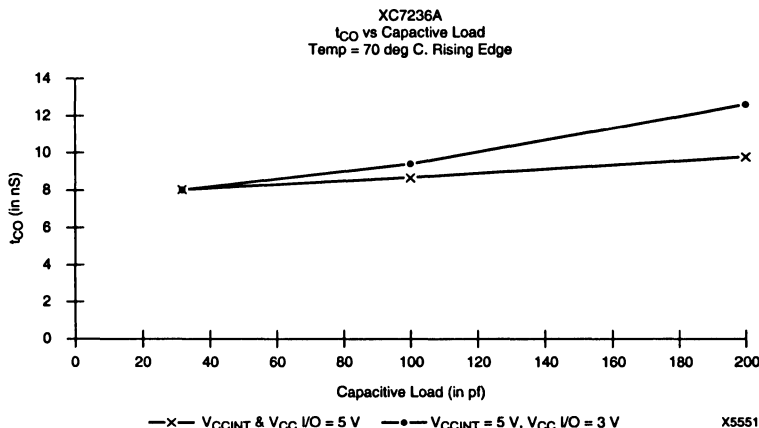
Figure 6. Typical Clock-to-Output (t_{CO}) vs Capacitive Loading (Low-to-High Transition)

Using Xilinx EPLDS in Mixed Voltage Systems

During this transition period to 3.3 volt only systems, there will be a need to use programmable logic to interface 3.3 and 5 volt components together. The Xilinx EPLDs are designed to be TTL-compatible with 3.3 and 5 volt logic as shown in Figure 8. The 5 volt TTL logic input thresholds are V_{IH} = 2.0 V and V_{IL} = 0.8 V. Xilinx EPLDs are guaranteed to drive a HIGH greater than 2.4 V and a LOW below 0.4 V at rated output drive currents. This guarantees at least 400 mV noise margin.

The internal core logic V_{CC} pins are identified as V_{CCINT} in the device data sheets. These pins are always connected to the 5 volt supply. The I/O V_{CC} pins are identified as V_{CCIO}. These pins are connected to the 3.3 volt supply in a mixed voltage system. All off the device GND pins must be connected together. Since the master reset (MR) pin requires a minimum V_{IH} equal to 60% of the core logic V_{CC}, it is not TTL or LVTTL compatible. If an RC circuit is used to hold MR low until V_{CCINT} is stable, the current limiting resistor should be connected to the 5 volt power supply. If a logic device drives MR, a pull up resistor connected to the 5 volt supply must be used unless the device has 5 volt CMOS compatible output levels.

Conclusion

Xilinx EPLDs are designed for the task of interfacing 3.3 volt logic and 5 volt logic together in high performance digital systems. The core logic is always powered at 5 volts for the fastest possible performance. The specified I/O performance is independent of whether the I/O supply is 5 volts or 3.3 volts nominal. Because of the minimal impact of I/O supply voltage on drive capability and propagation delay vs. capacitive loading, Xilinx EPLDs are ideal for high speed bus interfaces and memory subsystems that require the interfacing of 3.3 volt and 5 volt logic.

Figure 7. Test circuit for t_{CO} vs Capacitive Loading Curves
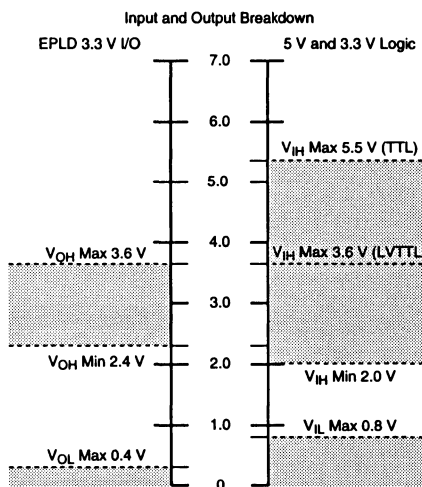
Figure 8. 3.3 V I/O Xilinx EPLD Driving 3.3 V and 5 V Components

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VME Data Acquisition Interface and Control in a Xilinx XC7000†

September 1994

Application Note

Introduction

The VME bus is a widely used and versatile asynchronous bus interface. This application note presents a data acquisition board which interfaces to the VME bus. The board consists of a 12-bit digital to analog converter (DAC), a 12-bit analog to digital converter (A/D), and the logic to control these devices and interface them to the VME bus. The interfacing and control logic are implemented in an XC73108-10PQ160 EPLD. Xilinx EPLDs are an excellent choice for VME bus applications both because of their flexibility and the product line's breadth. The XC7000 family is available in densities ranging from 18 to 144 macrocells, packages from 44 PLCC to 225 BGA, and pin to pin speeds as fast as 5 ns with clock cycles up to 167 MHz. The DualBlock™ architecture is another feature that enhances the XC7000 family's suitability for VME bus interfacing applications. The fast functions blocks can be used for functions which require leading edge pin-to-pin performance such as address decode, while the high density function blocks with integral ALU and carry chain can be used for more complex state machine, counter and compare functions. Because the VME bus is asynchronous, the input registers with clock enables available in the Xilinx EPLDs benefit the designer by allowing the data to be synchronized before it is latched into the device.

VME A/D Board

A block diagram of a basic VME slave to bus interface is shown in figure 1. As can be seen by this block diagram, the VME bus really consists of four buses. All of the signals used in this design interface with the Data Transfer Bus (DTB), with the exception of IACK which is driven to the board from the Priority Interrupt Bus. All the signals used in this design are unidirectional except for the sixteen data lines.

Although the DAC and A/D converter are each 12-bits wide, the design is easily modified for wider or narrower modules due to the flexibility of the Xilinx EPLDs and the DS550 XEPLD compiler software. This design as implemented will run up to 38 MHz. Since the VME system clock driver is specified to run at 16 MHz, the overall system speed in the Xilinx EPLD is more than sufficient. The design has been entered twice, once using Boolean logic equations, and again in schematic capture form. The DS550 XEPLD compiler interfaces with OrCAD386+™, Viewlogic, Mentor and Cadence schematic capture tools. Integral fitters are available for use with DATA I/Os ABEL and Logical Device's CUPL tools. Designs may also be entered using XABEL which is a Xilinx specific version of ABEL.
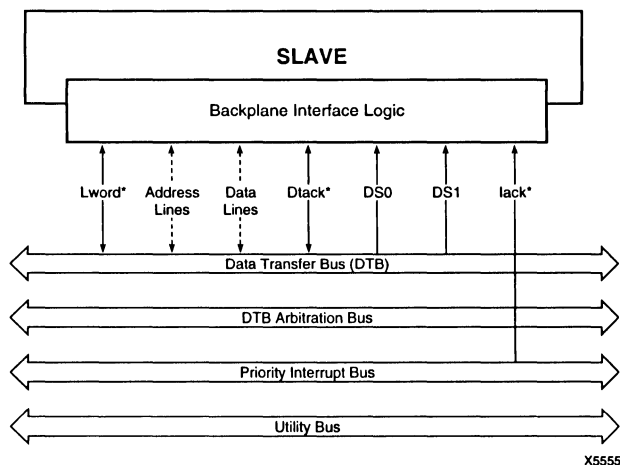
Figure 1. VME Slave Board Block Diagram

†This application note assumes the reader is familiar with the ANS/IEEE VMEbus specification Std 1014-1987. The reader should use this specification to resolve any issues with regards to operation of the VME interface functions described in this application note.

General Operation

The VME bus specification allows for 16, 24, or 32-bit addressing and a data path width of 16 or 32 bits. This design uses 24-bit (or standard), addressing mode and a data path 16 bits wide. A VME system master board drives a 24-bit address along with 6 address modifier bits to the Data Transfer Bus (DTB). The address comparator on the slave board decodes only bits A[24:4]. The lower bits of the address bus are used by the master to indicate what type of operation is required of the slave. The master must also drive the interrupt acknowledge (IACK), LWORD, and the address strobe (AS) low. If bits A[24:4]

and AM[5:0] match the address specified for the Data Acquisition board, then the operation begins when the master drives DS1 or DS0 low and the write (WR) line either high or low depending upon the direction of the data transfer. The assertion of DS1 or DS0 latches the "HIT" signal indicating that the master is addressing this board. The assertion of DS1 or DS0 and the registered version of the "HIT" which is "RHIT", enable the decoder which decodes address bits A2 and A1 to determine what operation the board is to perform. The output of the decoder is further classified by the state of WR. If WR is high, then the board is going to send either the contents

Master	Slave
Address the Slave Present address Present address modifier Drive LWORD* high Drive Iack* high Drive AS* low	
Specify Data Direction Drive WRITE* low **Specify Data Width** Wait until DTACK* high and BERR* high (indicates that previous slave is no longer driving data bus) Place data on D00-D15 Drive DS1* and DS0* low	**Process Adress** Receive address Receive address modifier Receive LWORD* high Receive IACK* high Receive AS* low If address is valid for this slave Then select on-board device
	Store Data Receive WRITE* low Receive DS1* low Receive DS0* low Capture Data from D00-D15 Write data into selected device **Respond to Master** Drive DTACK* low

Terminate Cycle
Receive DTACK* low
If last cycle then
  Release address lines
  Release address modifier lines
  Release data lines
  Release LWORD*
  Release IACK*
Endif
Drive DS0* and DS1* high
Drive AS* high	

End Termination
If last cycle then
  Release DS0* and DS1*
  Release AS* or else go to
  Address the Slave
Endif	

	Acknowledge Termination Receive DS0* and DS1* high Release DTACK*

X5557

Figure 2. Typical Double-byte Write Cycle

of the status register, or the result of the A/D conversion to the data bus; if WR is low then the master is either sending data to the DAC or telling the DAC to start the digital to analog conversion with the data sent on the previous cycle. The assertion of any one of these conditions causes the data acknowledge (DTACK) line to be driven low, indicating the data bus is free. The master then knows that it can then drive more data onto the bus or service an interrupt request from elsewhere in the system. Figure 2 shows a flow diagram from the IEEE/ANSI VME bus specification of an example of a double-byte write cycle.

Address and Address Modifier Module

The address and address modifier module is essentially an equality comparator. The address bits A[24:4] and address modifier bits AM[5:0] are compared with the user defined address and modifier bits B[24:4] and BM[5:0] respectively. The address and modifier bits are clocked into the XC73108's input pad registers (see figure 3), when the master drives the AS line low. The B[24:4] and BM[5:0] signals may be hard encoded at the time the design is compiled (i.e. Bx = GND or Bx = V_{CC}), or brought out to pins and tied to DIP switches so the end user can set the address and modifier code. This design

assumes the DIP switches will be used as this allows for more flexibility as the board is not confined to a particular slot in the system. Therefore bits B[24:4] and BM[5:0] are brought out to external pins. The six address modifier bits are used to determine the number of address bits being used as well as determining the type of transfer in progress. For a slave with sixteen bit I/O capabilities (we are actually using 12 of the data lines and driving the remaining four low), the modifier bits should be set to $2D_H$ this can be accomplished by hard encoding at the time of compilation, or by setting the DIP switches in the appropriate positions. The VME bus specification requires that if IACK is low, a slave must not respond and also that LWORD must be high for a valid double-byte (16-bit) data transfer to occur. When all of the above requirements are satisfied, the "HIT" signal is generated. This is latched into a register called "RHIT". when the master drives either DS0 or DS1 low. The "HIT" signal is registered because the VME bus specification indicates that the address lines can change as soon as the master detects the acknowledge. This register is cleared when both DS0 and DS1 are driven high by the master at the end of the data transfer.
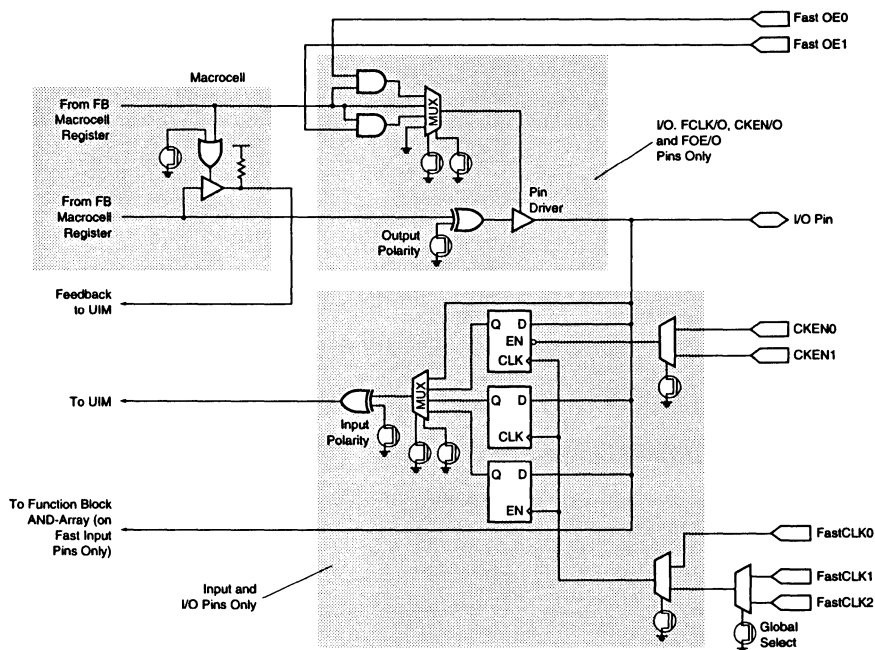
X5463

Figure 3. Xilinx XC7000 I/O Block Diagram

Function Decode

The outputs from the function decoder will be enabled when the address sent by the VME master matches the user defined address and DS0 and DS1 are both asserted. This is where the lower bits of the address bus come into play. Table 1 explains the use of these bits. The WR line determines which of the control function signals is active. If WR is high, then data is directed onto the data bus; conversely if WR is low then the function described in table 1 occurs.

Table 1: Table 1. A2, A1, A0, and WR Decoding

A2 A1 A0	WR	Decoder Function (signal)
0 0 x	0	Write status register
0 0 x	1	Read status register
0 1 x	0	Start A/D conversion
0 1 x	1	Read A/D data
1 0 x	0	Write DAC
1 0 x	1	No Op

When the data transfer is completed, the board drives the data acknowledge signal (DTACK) low. This notifies the system that the bus is free and it can send more data or the next address to the bus.

Analog to Digital Operation

As can be seen in Table 1, page 1 of the schematic diagram, and the PLD listing, when the value of bits A[2:1] is 01 the function decoder asserts the ADS signal which is anded along with the WR signal to generate the ADST (A/D Start) signal. This begins the analog to digital conversion process. When the A/D conversion is complete, the BUSY signal from the A/D converter is driven low which latches the data into ADRDY register. This in turn

enables the AD2BUS signal from the function decoder if the master is driving the WR signal low. WR low allows the data from the A/D converter onto the DTB to be read by the master. This is accomplished by enabling the output drivers on the D[15:0] pins. To enable the outputs, RHIT, DS1, DS0 and A1 must be high, while WR and A2 must be low.

Digital to Analog Conversion

When the proper address is decoded, the HIT signal is latched when the master drives either DS1 or DS0 low. The registered HIT signal, now called RHIT is used with the DS1 and DS0 signals to enable the function decoder. The function decoder decodes the address bits A[2:1] and when this value is 10 it outputs the DAL signal which is anded with WR. If WR is low, the data is read from the bus and the DALD signal is used to latch the data and pass it on to the DAC.

Status register

The status register indicates when data is ready to be read from the A/D converter. This information is passed to the system via the D0 line of the data bus. When WR, DS1 and DS0 are high and bits A2, A1 are low ADRDY is enabled on the bus and the processor can sample D0 to see if there is A/D data to be read.

Modifications

There are many modifications which can easily be made to this design. Additional bits could be added to the status register to send an interrupt to the processor when A/D data is ready instead of having the processor read the status register as is the case in the present design. Another easy modification would be to limit the board to a range of slots in the system. Then some of the user modifiable address bits could be "hard coded" or even eliminated
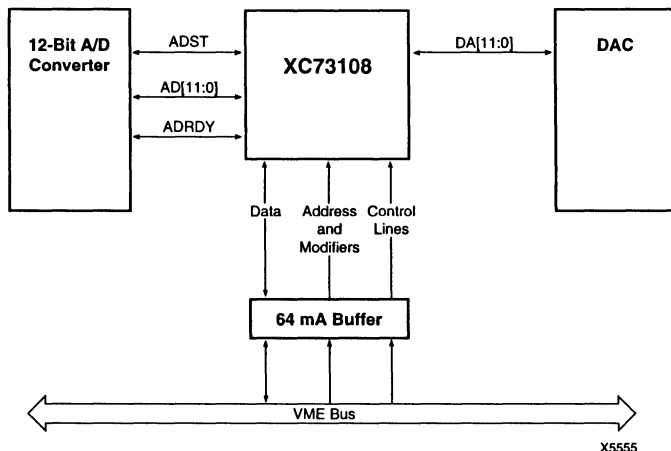
Figure 4. VME Board Block Diagram

thus decreasing the I/O resources needed. This design is also easily modifiable for A/Ds and DACs of differing precision. By using the MSB of the data bus, a 10 or 8-bit A/D and DAC could be easily substituted simply by driving the additional (currently unused), bits of the data bus to ground i.e. for a 10 bit DAC what is now D11 becomes D9 and the D6 and D5 equations are modified so that they are always at ground level.

Summary

This application describes a VME bus interface/data acquisition board controller implemented in a Xilinx XC73108 EPLD. The design is easily modifiable for wider or narrower applications. An electronic version of the design in both Boolean and VIEWlogic schematic format is available on the Xilinx BBS.

Xilinx EPLDs offer a wide variety of devices which can be used to implement various VME bus interface solutions. The Xilinx EPLDs are a superior programmable logic solution for this type of application due to the product line's broad range of devices from 18 to 144 macrocells in speeds up to 5 ns pin-to-pin, the ease of implementation using the Xilinx DS550 XEPLD translator software, and system features such as clock enables for input pad registers which are useful when interfacing to an asynchronous bus such as the VME bus.

Reference:

IEEE Standard for a Versatile Backplane Bus: VMEBus

Published by: The IEEE (1988)

PLD file

The following listing is an annotated version of the PLD file used to implement the data acquisition board in a Xilinx XC73108-10PQ160 EPLD.

```
TITLE    VME Bus interface and data acquisition controller
PATTERN   VMH
REVISION  5.0.0
AUTHOR    Patrick Kane
COMPANY   Xilinx EPLD
DATE     5/3/93
;This file implements a VME interface for a 12 bit DAC and a 12 bit A/D
;converter. The protocol uses 24 bit addressing and double byte
;read/write cycles.
 CHIP DCD_CTRL XEPLD
;Address inputs
INPUTPIN A1 A2 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
        A17 A18 A19 A20 A21 A22 A23 AM5 AM4 AM3 AM2 AM1 AM0
;User input pins for selectable address and modifier code
INPUTPIN B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
        B21 B22 B23 BM5 BM4 BM3 BM2 BM1 BM0
;Input pin from the VME priority interrupt bus
        IACK
;Input pins from the VME Data Transfer Bus (DTB)
        LWORD DS0 DS1 WR
;Inputs from the 12 bit A/D converter
        AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11
;Done signal from 12 bit A/D converter
        BUSY
;System Clock
16MHZ
```

OUTPUTPIN
;Start signal for the DAC
ADST
;Data Acknowledge to the VME DTB
DTACK
;Data for the DAC from the VME DTB bus
DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 DA8 DA9 DA10 DA11

;D0 is output only and is the status register bit
;Data lines D[3..1] are output only and driven to ground because
;we are only using 12 bits. The inputs of D[15..4] are registered in
;the I/O pads

IOPIN D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4
OUTPUTPIN D3 D2 D1 D0

NODE
;Internal nodes for the address and modifier decode
EQ7_0 EQ15_8 EQ23_16 RHIT ANYDS ADRDY HITRST
;CEPIN /AS   ;This is the clock enable for the address latch (in I/O pads)
;FASTCLOCK 16MHz ;system clock

EQUATIONS
;D-type flip-flop configured as a latch in high density function block
 ADRDY := GND
 ADRDY.CLKF = GND
 ADRDY.RSTF = A1 */A2 * DS0 * DS1 */WR * RHIT
 ADRDY.SETF = /BUSY
;These are the comparator equations for the address and address modifier bits
/EQ7_0 =   AM0 */BM0 + /AM0 * BM0 + AM1 */BM1 + /AM1 * BM1 + AM2 */BM2
             + /AM2 * BM2 + AM3 */BM3 + /AM3 * BM3 + AM4 */BM4
             + /AM4 * BM4 + AM5 */BM5 + /AM5 * BM5 + A7 */B7 + /A7 * B7
             + A6 */B6 + /A6 * B6 + A5*/B5 + /A5 * B5 + A4 */B4 + /A4 * B4
/EQ15_8 =   A15 */B15 + /A15 * B15 + A14 */B14 + /A14 * B14 + A13 */B13
             + /A13 * B13 + A12 */B12 + /A12 * B12 + A11 */B11
             + /A11 * B11 + A10 */B10 + /A10 * B10 + A9 */B9
             + /A9 * B9 + A8 */B8 + /A8 * B8
/EQ23_16 = A23 */B23 + /A23 * B23 + A22 */B22 + /A22 * B22
             + A21 */B21 + /A21 * B21 + A20 */B20 + /A20 * B20
             + A19 */B19 + /A19 * B19 + A18 */B18 + /A18 * B18
             + A17 */B17 + /A17 * B17 + A16 */B16 + /A16 * B16
;RHIT is the signal indicating the board is being addressed
RHIT := /LWORD */IACK * EQ7_0 * EQ15_8 * EQ23_16
RHIT.CLKF = ANYDS
RHIT.RSTF = HITRST
HITRST = DS0 + DS1 + /RHIT
ANYDS = /DS0 + /DS1
;ADST strobes analog to digital converter

ADST = A1 */A2 * WR * DS0 * DS1 * RHIT

;DTACK lets the system know that the bus is available

/DTACK := /A1 * A2 * ANYDS * WR * RHIT

            + /A2 * ANYDS */WR * RHIT

            + A1 */A2 * ANYDS * RHIT

DTACK.CLKF = 16MHZ

;these bits come from the DTB and are sent to the DAC

;Dx.PIN is from the input pad

DA11 := GND

DA11.CLKF = GND

DA11.RSTF = /A1 * A2 * DS0 * DS1 * WR */D15.PIN * RHIT

DA11.SETF = /A1 * A2 * DS0 * DS1 * WR * D15.PIN * RHIT

DA10 := GND

DA10.CLKF = GND

DA10.RSTF = /A1 * A2 * WR */D14.PIN * DS0 * DS1 * RHIT

DA10.SETF = /A1 * A2 * WR * D14.PIN * DS0 * DS1 * RHIT

DA9 := GND

DA9.CLKF = GND

DA9.RSTF = /A1 * A2 * DS0 * DS1 * WR */D13.PIN * RHIT

DA9.SETF = /A1 * A2 * DS0 * DS1 * WR * D13.PIN * RHIT

DA8 := GND

DA8.CLKF = GND

DA8.RSTF = /A1 * A2 * DS0 * DS1 * WR */D12.PIN * RHIT

DA8.SETF = /A1 * A2 * DS0 * DS1 * WR * D12.PIN * RHIT

DA7 := GND

DA7.CLKF = GND

DA7.RSTF = /A1 * A2 * DS0 * DS1 * WR */D11.PIN * RHIT

DA7.SETF = /A1 * A2 * DS0 * DS1 * WR * D11.PIN * RHIT

DA6 := GND

DA6.CLKF = GND

DA6.RSTF = /A1 * A2 * DS0 * DS1 * WR */D10.PIN * RHIT

DA6.SETF = /A1 * A2 * DS0 * DS1 * WR * D10.PIN * RHIT

DA5 := GND

DA5.CLKF = GND

DA5.RSTF = /A1 * A2 * DS0 * DS1 * WR */D9.PIN * RHIT

DA5.SETF = /A1 * A2 * DS0 * DS1 * WR * D9.PIN * RHIT

DA4 := GND

DA4.CLKF = GND

DA4.RSTF = /A1 * A2 * DS0 * DS1 * WR */D8.PIN * RHIT

DA4.SETF = /A1 * A2 * DS0 * DS1 * WR * D8.PIN * RHIT

DA3 := GND

DA3.CLKF = GND

DA3.RSTF = /A1 * A2 * WR */D7.PIN * DS0 * DS1 * RHIT

DA3.SETF = /A1 * A2 * WR * D7.PIN * DS0 * DS1 * RHIT

DA2 := GND

DA2.CLKF = GND

DA2.RSTF = /A1 * A2 * WR */D6.PIN * DS0 * DS1 * RHIT

DA2.SETF = /A1 * A2 * WR * D6.PIN * DS0 * DS1 * RHIT

```
DA1 := GND
DA1.CLKF = GND
DA1.RSTF = /A1 * A2 * WR */D5.PIN *  DS0 * DS1 * RHIT
DA1.SETF = /A1 * A2 * WR * D5.PIN *  DS0 * DS1 * RHIT
DA0 := GND
DA0.CLKF = GND
DA0.RSTF = /A1 * A2 * WR */D4.PIN *  DS0 * DS1 * RHIT
DA0.SETF = /A1 * A2 * WR * D4.PIN *  DS0 * DS1 * RHIT
;these are the data outputs
;D0 is from the status register and indicates when data is ready from the A/D converter
;D[1:4] are always driven to ground because the DAC and A/D are only
;12 bits wide
D0 := GND
D0.CLKF = GND
D0.RSTF = /A1 */A2 * DS0 * DS1 */WR * RHIT */ADRDY
D0.SETF = /A1 */A2 * DS0 * DS1 */WR * RHIT * ADRDY
D0.TRST = /A1 */A2 * DS0 * DS1 */WR * RHIT
D1  = GND
D1.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D2  = GND
D2.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D3  = GND
D3.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D4  = AD0
D4.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D5  = AD1
D5.TRST =  A1 */A2 */WR *  DS0 * DS1 * RHIT
D6  = AD2
D6.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D7  = AD3
D7.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D8  = AD4
D8.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D9  = AD5
D9.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D10  = AD6
D10.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D11  = AD7
D11.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D12  = AD8
D12.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D13  = AD9
D13.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
D14  = AD10
D14.TRST =  A1 */A2 */WR *  DS0 * DS1 * RHIT
D15  = AD11
D15.TRST =  A1 */A2 * DS0 * DS1 */WR * RHIT
```

IPAD8 IBUF8 COMP8
I[7:0]
AD[23:16] ADI[23:16]
A[7:0]
EQ

IPAD8 IBUF8
I[7:0]
BD[23:16] BDI[23:16]
B[7:0]

IPAD8 IBUF8 COMP8
I[7:0]
AD[15:8] ADI[15:8]
A[7:0]
EQ

IPAD8 IBUF8
I[7:0]
BD[15:8] BDI[15:8]
B[7:0]

COMP4
IPAD AD7 IBUF ADI7 A0
IPAD AD6 IBUF ADI6 A1
IPAD AD5 IBUF ADI5 A2
IPAD AD4 IBUF ADI4 A3
IPAD BD7 IBUF BDI7 B0
IPAD BD6 IBUF BDI6 B1
IPAD BD5 IBUF BDI5 B2
IPAD BD4 IBUF BDI4 B3
EQ

COMP4
IPAD AM5 IBUF AMI5 A0
IPAD AM4 IBUF AMI4 A1
IPAD AM3 IBUF AMI3 A2
IPAD AM2 IBUF AMI2 A3
IPAD BM5 IBUF BMI5 B0
IPAD BM4 IBUF BMI4 B1
IPAD BM3 IBUF BMI3 B2
IPAD BM2 IBUF BMI2 B3
EQ

COMP2
IPAD AM1 IBUF AMI1 A0
IPAD AM0 IBUF AMI0 A1
IPAD BM1 IBUF BMI1 B0
IPAD BM0 IBUF BMI0 B1
EQ

ILD
IPAD LWORD D Q
16MHZ G
NAND2B2

ILD
IPAD IACK D Q
16MHZ G

IPAD BUFG 16MHZ

IPAD DS0 IBUF DS0I
IPAD DS1 IBUF DS1I
OR2B2 ANYDS
NAND2B2 DS_EN

SCR
NAND2B1 SCR2BUS
ADS
NAND2B1 AD2BUS
DAL
AND2B2 ADST
IPAD WR IBUF
AND2B2 DALD

ADST
DALD NOR2
SCR2BUS
NAND2B2 DTACK
OBUF DTACKO OPAD

NAND6

FDC
HIT D Q
ANYDS C
CLR RHIT

NAND2B1 ANYDS

X74_138
IPAD AD1 IBUF ADI1 A Y0
IPAD AD2 IBUF ADI2 B Y1
IPAD AD3 IBUF ADI3 C Y2
Y3
Y4
DS_EN G2A Y5
G2B Y6
RHIT G1 Y7
GND

FD4
D0 Q0 DAL
D1 Q1 ADS
D2 Q2 SCR
D3 Q2
ANYDS C
OBUF ADOE IOPAD

BUF16

OBUFE8X1

IOPAD8

IPAD ANDIG15 IBUF ADG15
IPAD ANDIG14 IBUF ADG14
IPAD ANDIG13 IBUF ADG13
IPAD ANDIG12 IBUF ADG12
IPAD ANDIG11 IBUF ADG11
IPAD ANDIG10 IBUF ADG10
IPAD ANDIG9 IBUF ADG9
IPAD ANDIG8 IBUF ADG8
IPAD ANDIG7 IBUF ADG7
IPAD ANDIG6 IBUF ADG6
IPAD ANDIG5 IBUF ADG5
IPAD ANDIG4 IBUF ADG4

ADG[15:0] DO[15:0]

DO[15:8] DIO[15:8]

IO[7:0]

ADOE BUFFOE

OBUFE8X1 IOPAD8

DO[7:0] DIO[7:0]

IO[7:0]

ADG3
ADG2
ADG1
ADG0
GND
GND
GND
GND

LD4

DIO7 IBUF DI7 D0 Q0 DA3 OBUF OPAD
DIO6 IBUF DI6 D1 Q1 DA2 OBUF OPAD
DIO5 IBUF DI5 D2 Q2 DA1 OBUF OPAD
DIO4 IBUF DI4 D3 Q3 DA0 OBUF OPAD
DAL G

OFDE

SCR2BUS ADRDY D Q DO OPAD
INV C

LD4

DI[15:8] DA[11:4]

DIO15 IBUF DI15 D[7:0]
DIO14 IBUF DI14 Q[7:0]
DIO13 IBUF DI13
DIO12 IBUF DI12
DIO11 IBUF DI11 DAL G
DIO10 IBUF DI10
DIO9 IBUF DI9
DIO8 IBUF DI8

DA11 OBUF OPAD
DA10 OBUF OPAD
DA9 OBUF OPAD
DA8 OBUF OPAD
DA7 OBUF OPAD
DA6 OBUF OPAD
DA5 OBUF OPAD
DA4 OBUF OPAD

FDRS

IPAD BUSY IBUF
D S Q ADRDY
C
GND R
AD2BUS

XILINX® EPLDs

Title: VME I/F - DATA AQUISITION BOARD	
Comments: A/D AND DAC INTERFACE	
Date: 7/28/94	Ver:1.0
VME.2 Page 2 of 2	Rev:1.0

X5559

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1   **Applications**

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3   **XC7200A EPLD Family**

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XILINX®

XC7300 EPLD Family

XILINX®

XC7300 CMOS EPLD Family

Product Description

Features

- High-performance Erasable Programmable Logic Devices (EPLDs)
  - 5 / 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency

- Advanced Dual-Block architecture
  - Fast Function Blocks
  - High-Density Function Blocks (XC7354, XC7372, XC73108, XC73144)

- 100% interconnect matrix

- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 to 61 MHz 18-bit accumulators

- Multiple independent clocks

- Each input programmable as direct, latched, or registered

- High-drive 24 mA output

- I/O operation at 3.3 V or 5 V

- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V

- Power management options

- Multiple security bits for design protection

- Supported by industry standard design and verification tools

- 100% PCI compliant

Description

The XC7300 family employs a unique Dual-Block architecture, which provides high speed operations via Fast Function Blocks and/or high density capability via High Density Function Blocks.

Fast Function Blocks (FFBs) provide fast, pin-to-pin speed and logic throughput for critical decoding and ultra-fast state machine applications. High-Density Function Blocks (FBs) provide maximum logic density and system-level features to implement complex functions with predictable timing for adders and accumulators, wide functions and state machines requiring large numbers of product terms, and other forms of complex logic.

In addition, the XC7300 architecture employs the Universal Interconnect Matrix (UIM) which guarantees 100% interconnect of all internal functions. This interconnect scheme provides constant, short interconnect delays for all routing paths through the UIM. Constant interconnect delays simplify device timing and guarantee design performance, regardless of logic placement within the chip.

All XC7300 devices are designed in 0.8μ CMOS EPROM technology.

All XC7300 EPLDs include programmable power management features to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to mini-

The XC7300 Family

	XC7318	XC7336	XC7354	XC7372	XC73108	XC73144
Typical 22V10 Equivalent	1.5 – 2	3 – 4	6	8	12	16
Number of Macrocells	18	36	54	72	108	144
Number of Function Blocks	2	4	6	8	12	16
Number of Flip-Flops	18	36	108	126	198	276
Number of Fast Inputs	12	12	12	12	12	12
Number of Signal Pins	38	38	58	84	120	156
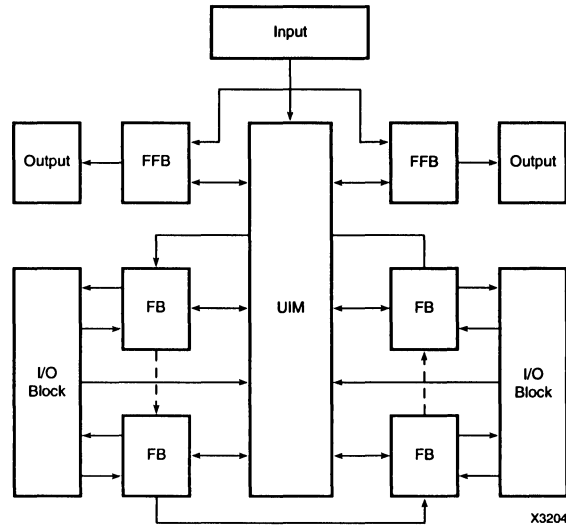
Figure 1. XC7300 Device Block Diagram

mize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software supports XC7300 EPLD design using third-party schematic entry tools, HDL compilers, or direct equation-based text files. Using a PC or a workstation and one of these design capture methods, designs are automatically mapped to an XC7300 EPLD in a matter of minutes.

The XC7300 devices are available in plastic and ceramic leaded chip carriers, pin-grid-array (PGA), ball-grid-array (BGA), and quad flat pack (QFP) packages. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.

Architecture

The XC7300 architecture consists of multiple programmable Function Blocks interconnected by a UIM as shown in Figure 1. The Dual-Block architecture contains two types of function blocks: Fast Function Blocks and High-Density Function Blocks. Both types of function blocks, and the I/O blocks, are interconnected through the UIM.

Fast Function Blocks

The Fast Function Block has 24 inputs which can be individually selected from the UIM, 12 fast input pins, or the nine Macrocell feedbacks from the Fast Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive the nine Macrocells in

each Fast Function Block. Each Macrocell can be configured for registered or combinatorial logic. See Figure 2.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs.

Two fast function block Macrocell differences exist when comparing the XC7336 FFB to the XC7354, XC7372 and XC73108 FFBs.

In the XC7336, five product terms from the programmable AND array are allocated to each Macrocell. Four of these product-terms are OR'd together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product-term drives the asynchronous active High programmable Set or Reset input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs. See Figure 2.

In the XC7354, XC7372 and XC73108, five product terms from the programmable AND array are allocated to each Macrocell. Four of these product-terms are OR'd together, inverted and drive the input of a programmable D-type flip-flop. The fifth product-term drives the asynchronous active High programmable Set input to the Macrocell flip-flop. The flip-flop can be configured as a D-type flip-flop or transparent for combinatorial outputs. See Figure 3.
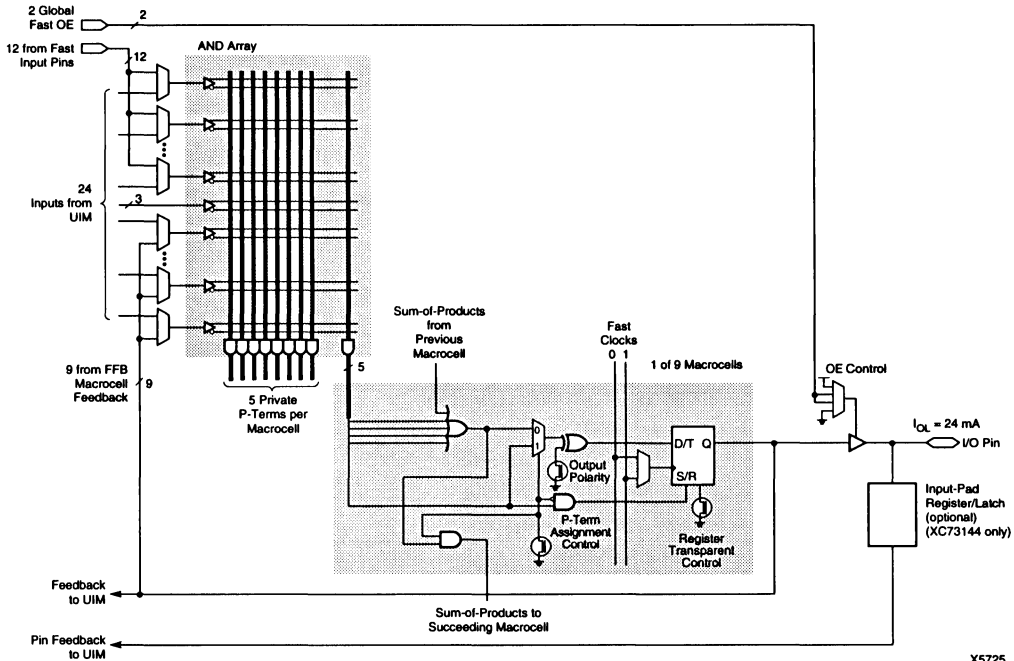
Figure 2. Fast Function Block and Macrocell Schematic for the XC7318, XC7336, and XC73144
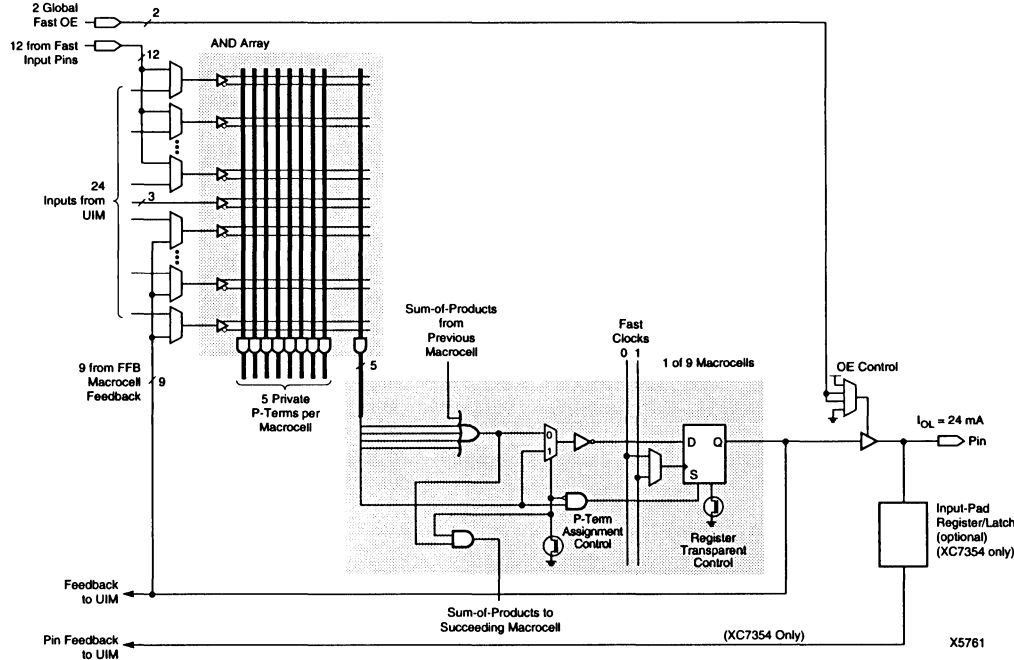
Figure 3. Fast Function Block and Macrocell Schematic for the XC7354, XC7372, and XC73108

The programmable clock source is one of two global Fast-Clock signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated Fast Output Enable inputs or permanently enabled or disabled. The Macrocell output can also be routed back as an input to the Fast Function Block and the UIM.

Each Fast Function Block output is capable of sinking 24 mA when V_{CCIO} = 5 volts. These include all outputs on the XC7318 and XC7336 devices and all Fast Outputs (FOs) on the XC7354, XC7372, XC73108, and XC73144 devices.

Unlike other I/Os, the Fast Function Block inputs do not have an input register.

Product Term Assignment

Each Macrocell sum-of-product OR gates can be expanded using the Fast Function Block product term assignment scheme. Product-term assignment transfers product-terms in increments of four product-terms from one Macrocell to the neighboring Macrocell (Figure 4). Complex logic functions requiring up to 36 product-terms can be implemented using all nine Macrocells within the Fast Function Block. When product-terms are assigned to adjacent Macrocells, the product-term normally dedicated to the Set or Reset function becomes the input to the Macrocell register.
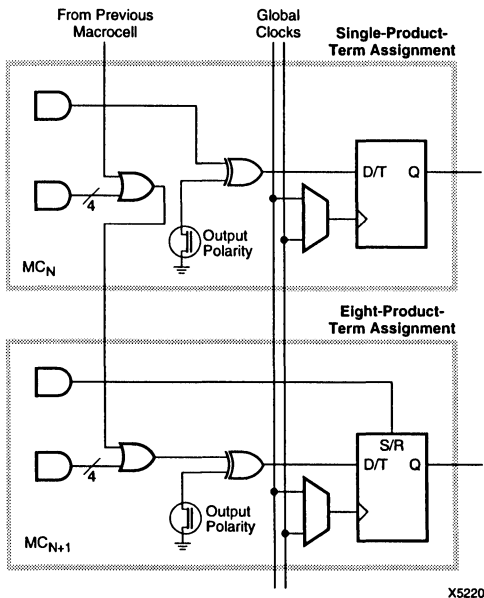
X5220

Figure 4. Fast Function Block Product-Term Assignment

High-Density Function Blocks

The XC7354, XC7372, XC73108 and XC73144 devices contain multiple, High-Density Function Blocks linked though the UIM. Each Function Block contains nine Macrocells. Each Macrocell can be configured for either registered or combinatorial logic. A detailed block diagram of the High-Density FB is shown in Figure 5.

Each FB receives 21 signals and their complements from the UIM and an additional three inputs from the Fast Input (FI) pins.

Shared and Private Product Terms

Each Macrocell contains five private product terms that can be used as the primary inputs for combinatorial functions implemented in the Arithmetic Logic Unit (ALU), or as individual Reset, Set, Output-Enable, and Clock logic functions for the flip-flop. Each Function Block also provides an additional 12 shared product terms, which are uncommitted product terms available for any of the nine Macrocells within the Function Block.

Four private product terms can be ORed together with up to four shared product terms to drive the D1 input to the ALU. The D2 input is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms. The shared product terms add no logic delay, and each shared product term can be connected to one or all nine Macrocells in the Function Block.

Arithmetic Logic Unit

The functional versatility of each Macrocell in the High-Density Function Block is enhanced through additional gating and control functions available in the ALU. A detailed block diagram of the XC7300 ALU is shown in Figure 6.

The ALU has two programmable modes; *logic* and *arithmetic*. In logic mode, the ALU functions as a 2-input function generator using a 4-bit look-up table that can be programmed to generate any Boolean function of its D1 and D2 inputs as illustrated in Table 1.

The function generator can OR its inputs, widening the OR function to a maximum of 17 inputs. It can AND them, which means that one sum-of-products can be used to mask the other. It can also XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored.
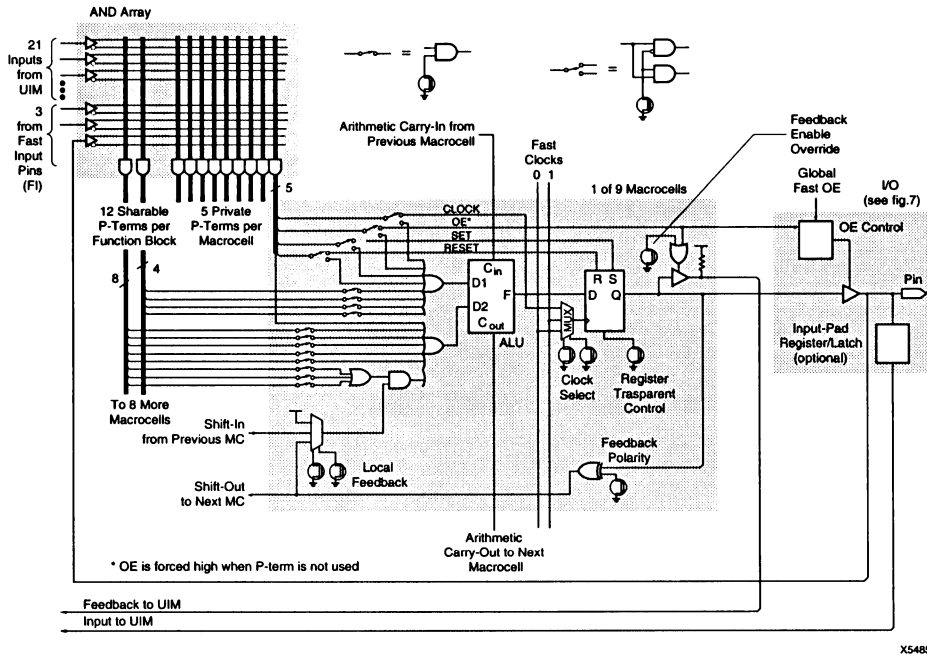
Figure 5. High-Density Function Block and Macrocell Schematic

Table 1. Function Generator Logic Operations

Function	
D1:+: D2	$\overline{\text{D1:+: D2}}$
D1 * D2	$\overline{\text{D1 * D2}}$
D1 + D2	$\overline{\text{D1 + D2}}$
D1	D2
$\overline{\text{D1}}$	$\overline{\text{D2}}$
D1 * $\overline{\text{D2}}$	$\overline{\text{D1}}$ * D2
D1 + $\overline{\text{D2}}$	$\overline{\text{D1}}$ + D2

Figure 6. ALU Schematic

Therefore, the ALU can implement one additional layer of logic without any speed penalty.

In arithmetic mode, the ALU block can be programmed to generate the arithmetic sum or difference of the D1 and D2 inputs. Combined with the carry input from the next lower Macrocell, the ALU operates as a 1-bit full adder generating a carry output to the next higher Macrocell. The carry chain propagates between adjacent Macrocells and also crosses the boundaries between Function Blocks. This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture when trying to perform arithmetic functions.

Carry Lookahead

Each Function Block provides a carry lookahead generator capable of anticipating the carry across all nine Macrocells. The carry lookahead generator reduces the ripple-carry delay of wide arithmetic functions such as add, subtract, and magnitude compare to that of the first nine bits, plus the carry lookahead delay of the higher-order Function Blocks.

Macrocell Flip-Flop

The ALU block output drives the input of a programmable D-type flip-flop. The flip-flop is triggered by the rising edge of the clock input, but it can be configured as transparent,
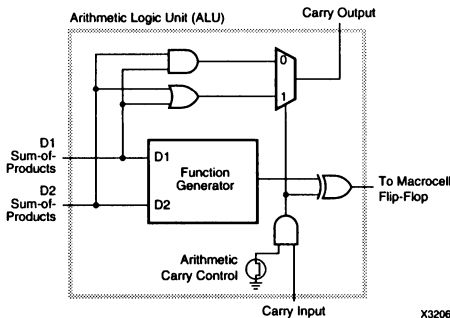
making the Q output identical to the D input, independent of the clock, or as a conventional flip-flop.

The Macrocell clock source is programmable and can be one of the private product terms or one of two global Fast-CLK signals (FCLK0 and FCLK1). Global FastCLK signals are distributed to every Macrocell flip-flop with short delay and minimal skew.

The asynchronous Set and Reset product terms override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set.

In addition to driving the chip output buffer, the Macrocell output is routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output buffer and/or the feedback to the UIM. If it is configured to control UIM feedback, the Output Enable product term forces the UIM feedback line High when the Macrocell output is disabled.

Universal Interconnect Matrix
The UIM receives inputs from each Macrocell output, I/O pin, and dedicated input pin. Acting as an unrestricted crossbar switch, the UIM generates 21 output signals to each High-Density Function Block and 24 output signals to each Fast Function Block.

Each UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant, regardless of the routing distance, fan-out, or fan-in.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal inversions at the input pins, Macrocell outputs and Function Block AND-array input, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Programming several such Macrocell outputs onto the same UIM output emulates a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes the enabled output's level.

Input/Output Blocks
Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. The Macrocell output can be inverted. An additional configuration option allows the output to be disabled permanently. Two dedicated FastOE inputs can also be configured to control any of the chip outputs instead of, or in conjunction with, the individual Output Enable product term. See Figure 7.
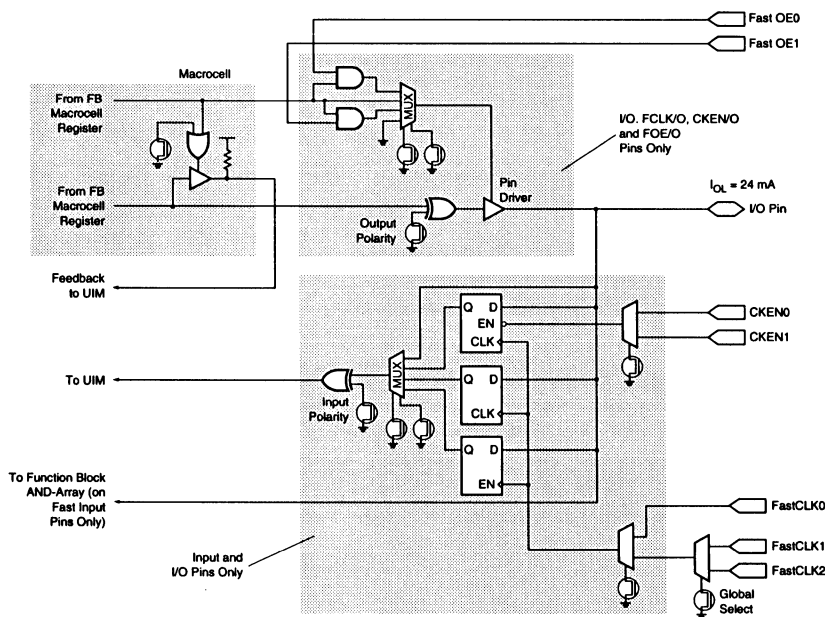
X5463

Figure 7. Input/Output Schematic (except XC7318/XC7336 which do not include I/O flip-flops)

Output buffers, except those connected to Fast Function Blocks, can sink 12 mA when V_{CCIO} = 5 V. Fast Function Block outputs can sink 24 mA when V_{CCIO} = 5 V. All outputs on the XC7318 and XC7336 devices connect to FFBs. Outputs listed as Fast Outputs (FO) on the XC7354, XC7372, XC73108 and XC73144 devices connect to FFBs.

Each signal input to the chip is connected to a programmable input structure that can be configured as direct, latched, or registered. The latch and flip-flop can use one of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. The flip-flop includes an active-low clock enable, which when High, holds the present state of the flip-flop and inhibits response to the input signal. The clock enable source is one of two global Clock Enable signals ($\overline{CE0}$ and $\overline{CE1}$). An additional configuration option is polarity inversion for each input signal.

3.3 V or 5 V Interface Configuration

XC7300 devices can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7300 device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O drivers (V_{CCIO}). V_{CCINT} must always be connected to a nominal 5 V supply, while V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7300 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus.

Power-On Characteristics/Master Reset

The XC7300 device undergoes a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the $\overline{MR}$ pin is tied to V_{CCINT}, the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If $\overline{MR}$ is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and $\overline{MR}$ is brought High. V_{CC} rise must be monotonic to insure the initialization sequence is performed correctly.

For additional flexibility, the $\overline{MR}$ pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of $\overline{MR}$, all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and $\overline{MR}$ is brought High. The minimum $\overline{MR}$ pulse with is t_{WMR}. If $\overline{MR}$ is brought high after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}.

During the initialization sequence, all input registers or latches are preloaded High and all FB and FFB Macrocell registers are preloaded to a known state. For FFB Macrocell registers where the Set/Reset product-term is defined, the preload is accomplished by asserting the product-term shortly before the end of the initialization sequence. When the Set/Reset product-term is defined and configured as Reset, the register preload value is Low. When the Set/Reset product-term is defined and configured as a Set, the register preload value is High. For FFB Macrocell registers where the Set/Reset product-term is not used, the register preload value is High.

For FB Macrocell registers, the preload value is defined by a separate preload configuration bit, independent of the Set and Reset product-terms. The value of this preload configuration bit is determined by the schematic capture library or in the user's design. If not specified, the register preload value is Low.

Power Management

The XC7300 family of devices feature a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a small part is speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To further reduce power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Erasure Characteristics

In windowed packages, the content of the EPROM array can be erased by exposure to ultraviolet light of wavelengths of approximately 4000 Å. The recommended erasure time is approximately 1 hr. when the device is placed within 1 in. of an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. To prevent unintentional exposure, place opaque labels over the device window.

When the device is exposed to high intensity UV light for much longer periods, permanent damage can occur. The

maximum integrated dose the XC7300 EPLD can be exposed to without damage is 7000 W • s/cm^2, or approximately one week at 12,000 µW/cm^2.

Design Recommendations

For proper operation, all unused input and I/O pins must be connected to a valid logic level (High or Low). The recommended decoupling for all V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Use electrostatic discharge (ESD) handling procedures with the XC7300 EPLDs to prevent damage to the device during programming, assembly, and test.

Design Security

Each member of the XC7300 family has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices. Programmed data within EPROM cells is invisible–even when examined under a microscope–and cannot be selectively erased. The EPROM security bits, and the device configuration data, reset when the device is erased.

High-Volume Production Programming

The XC7300 family offers flexibility for low-volume prototypes as well as cost-effectiveness for high-volume production. The designer can start with ceramic window package parts for prototypes, ramp up initial production using low-cost plastic parts programmed in-house, and then shift into high-volume production using Xilinx factory programmed and tested devices.

The Xilinx factory programmed concept offers significant advantages over competitive masked PLDs, or ASIC redesigns:

* No redesign is required – Even though masked devices are advertised as timing compatible, subtle differences in a chip layout can mean system failure.

* Devices are factory tested – Factory-programmed devices are tested as part of the manufacturing flow, insuring high-quality products.

* Shipments are delivered fast – Production shipments can begin within a few weeks, eliminating masking delays and qualification requirements.

For factory programming procedures, contact your local Xilinx representative.

XEPLD Development System

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator maps the design quickly and automatically onto a chosen EPLD device, produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

* Familiar design approach similar to TTL and PLD techniques

* Converts netlist to fuse map in minutes using a '486 PC or workstation platform

* Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages

* Schematic library with familiar and powerful TTL-like components, including PLDs and ALUs

* Predictable timing even before design entry, using library components and Boolean equations

Timing simulation using Viewsim, OrCAD VST, and other tools controlled by the Xilinx Design Manager (XDM) program

Timing Model

Timing within the XC7300 EPLDs is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 8.

The timing model is based on the fixed internal delays of the XC7300 architecture which consists of four basic parts: I/O Blocks, the UIM, Fast Function Blocks and High-Density Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for a particular EPLD.
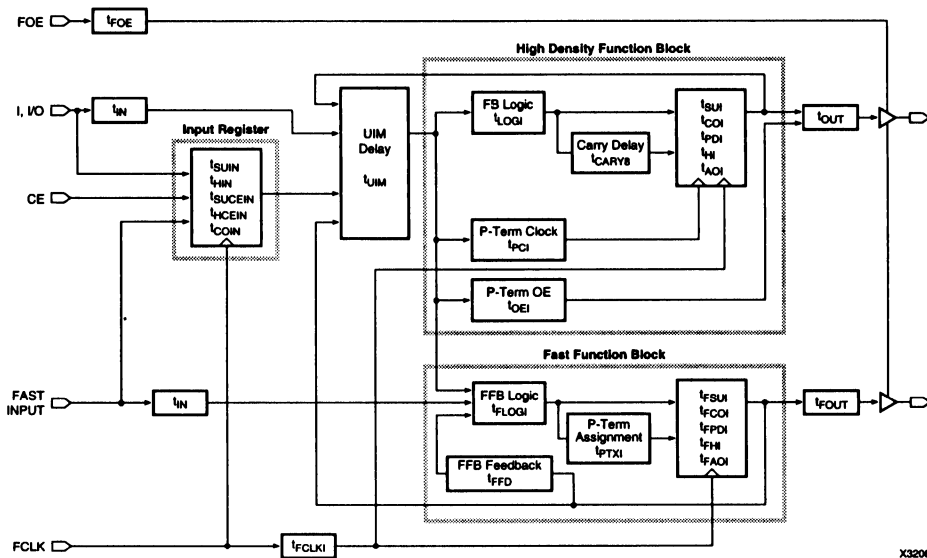
Figure 8. XC7300 Timing Model

Synchronous Clock Switching Characteristics
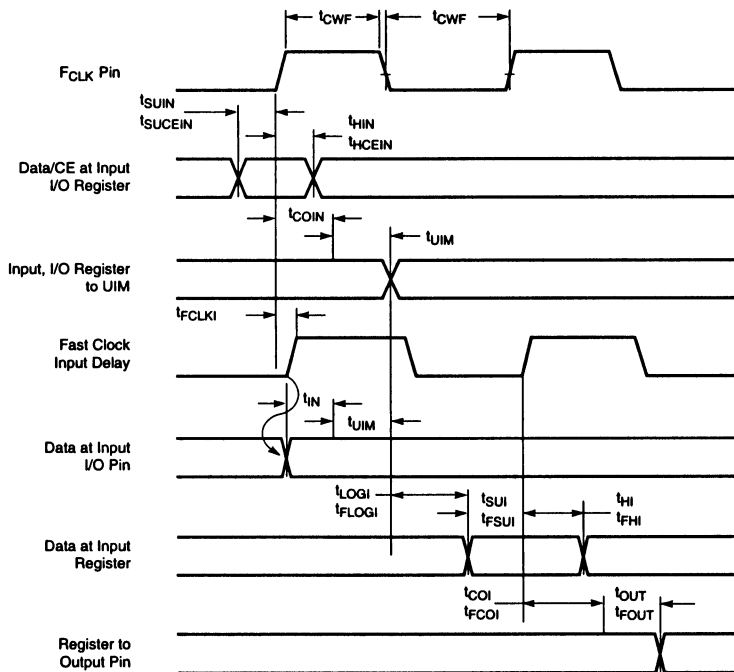
XILINX

Combinatorial Switching Characteristics

X3339

Asynchronous Clock Switching Characteristics

X3580

XILINX®

XC7318
18-Macrocell CMOS EPLD
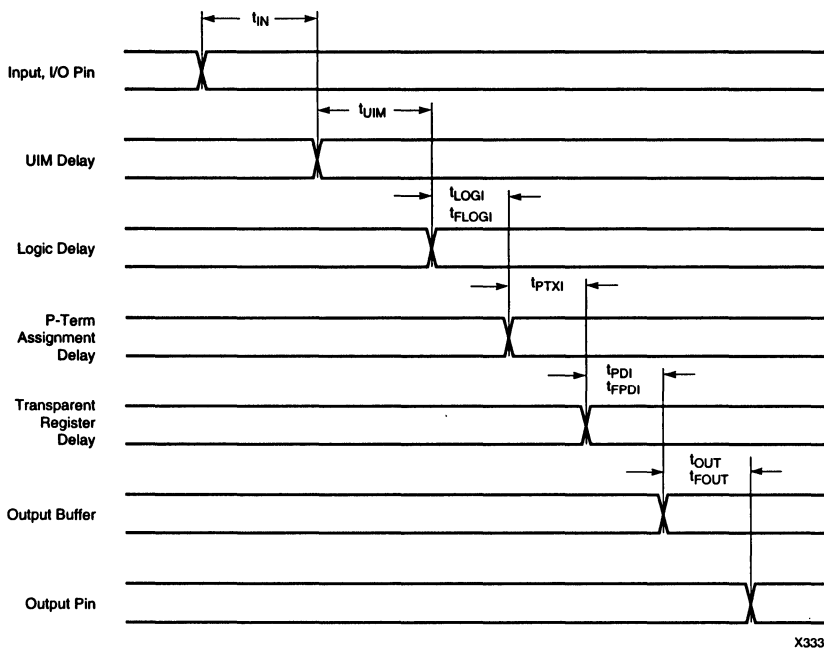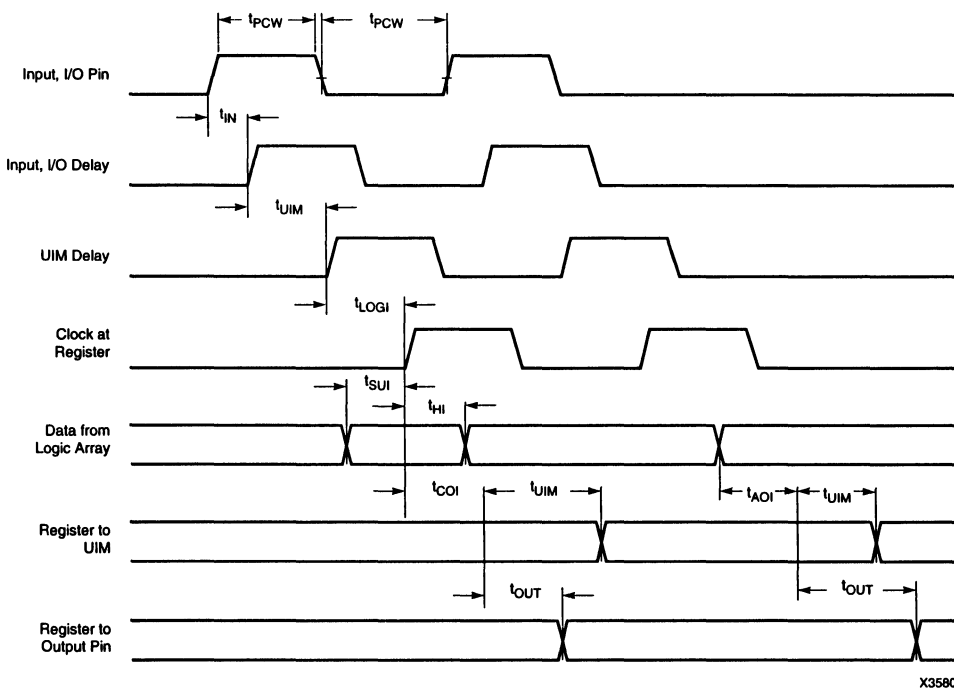
Product Specifications

Features

- Ultra high-performance EPLD
  - 5 ns pin-to-pin speed on all fast inputs
  - 167 MHz maximum clock frequency

- 100% routable with 100% utilization

- Incorporates two PAL-like 24V9 Fast Function Blocks

- 18 Output Macrocells
  - Programmable I/O architecture
  - 24 mA drive

- High-performance µP compatible

- JEDEC standard 3.3 V or 5 V I/O operation

- Multiple security bits for design protection

- 44-pin leaded chip carrier and 44-pin quad flat pack packages

- 100% PCI compliant

General Description

The XC7318 is a member of the Xilinx XC7300 EPLD family. It consists of two PAL-like 24V9 Fast Function Blocks inter-connected by the 100%-populated Universal Interconnect Matrix (UIM™).

Each Fast Function Block has 24 inputs and contains nine Macrocells configurable for registered or combinational logic. The nine Macrocell outputs feed back to the UIM and can simultaneously drive the output pads.

The UIM allows 100% connectivity between all function blocks and input pins, providing the ability to utilize 100% of the device while eliminating routing issues.

XC7318 device is designed in 0.8 µ CMOS EPROM technology

Device logic is automatically configured to the user's specifications using the XEPLD software. The XEPLD software is capable of optimizing and collapsing logic. The SMART-switch software/hardware feature allows implementation of buried combinatorial logic functions in the UIM, thus increasing device utilization. The XEPLD software supports third party schematic capture and HDL entry tools, as well as direct equation-based text files. Using a workstation or PC platform, designs are automatically mapped into the XC7318 in a matter of minutes.
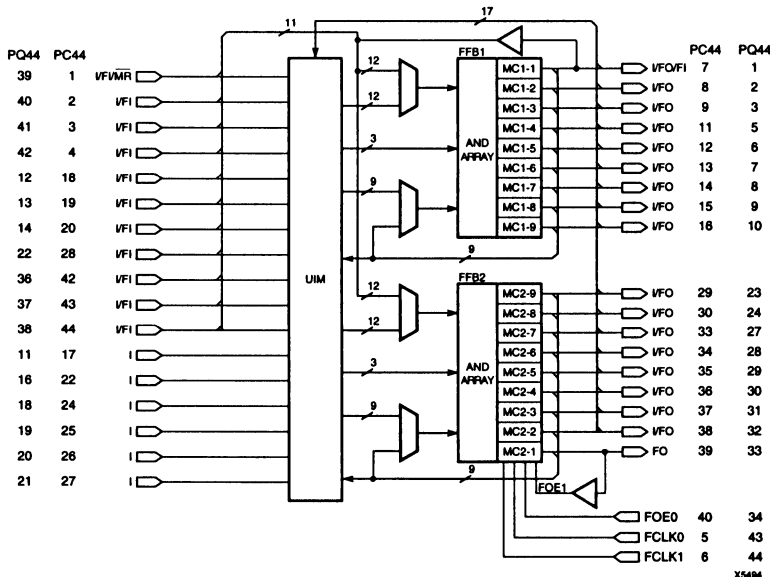
Figure 1. XC7318 Functional Block Diagram

Fast Function Blocks (FFB)

The XC7318 provides two Fast Function Blocks which have 24 inputs that can be individually selected from the UIM, 12 fast input pins, or the 9 Macrocell feedbacks from the Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive nine Macrocells in each FFB. Each Macrocell (Figure 2), can be configured for registered or combinatorial logic.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the Macrocell flip-flop. The flip-flop can be configured as a D-type flip-flop or Toggle flip-flop or transparent for combinatorial outputs.

The programmable clock source is one of two global Fast-CLK signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

I/O Block

The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated active-High Fast Output Enable inputs or permanently enabled or disabled. The Macrocell output can also be routed back as an input to the Fast Function Block, and the UIM.

Power-On Characteristics/Master Reset

The XC7318 device undergoes a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the $\overline{MR}$ pin is tied to V_{CCINT}, the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If $\overline{MR}$ is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and $\overline{MR}$ is brought High. V_{CC} rise must be monotonic to insure the initialization sequence is performed correctly.

For additional flexibility, the $\overline{MR}$ pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of $\overline{MR}$, all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and $\overline{MR}$ is brought High. The minimum $\overline{MR}$ pulse width is t_{WMR}. If $\overline{MR}$ is brought High after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}.

Figure 2. Fast Function Block and Macrocell Schematic

Figure 3. Fast Function Block Product Term Assignment

Product Term Assignment

Each Macrocell sum-of-product OR gate can be expanded using the Export product-term assignment feature. The Export function transfers product-terms in increments of four from one Macrocell to the neighboring Macrocell (Figure 3). Complex logic functions requiring up to 36 product-terms can be implemented using all nine Macrocells within the Fast Function Block. When product-terms are assigned to adjacent Macrocells, the product-term normally dedicated to the Set or Reset function becomes the input to the Macrocell register.

Universal Interconnect Matrix

The UIM receives input from Macrocell outputs, I/O pins, and dedicated input pins. Acting as an unrestricted cross-bar switch, the UIM generates 24 output signals to each Fast Function Block. Each UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal polarities at the input pins, Macrocell outputs and Fast Function Block AND-array inputs, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without additional speed penalty.

3.3 V or 5 V Interface Configuration

The XC7318 can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7318 device has separate V_{CC} connections to the internal logic (V_{CCINT}) and to the I/O pads (V_{CCIO}). V_{CCINT} must always be connected to a 5 V supply. V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V. This makes the XC7318 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus simultaneously.

Power Management

The XC7318 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (6.6) + MC_{LP} (5.0) + MC (0.005 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of Macrocells used

f = Clock frequency (MHz)

Figure 4 shows a typical power calculation for the XC7318 device, programmed as a 16-bit counter and operating at the indicated clock frequency.
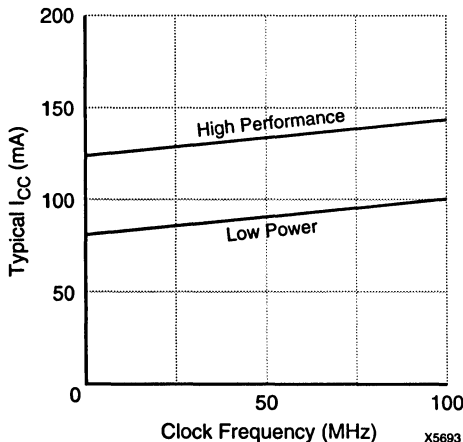
Figure 4. Typical I_{CC} vs Frequency for XC7318

Design Security

The XC7318 has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices.

Prototyping and Programming

If prototype systems require erasable devices, the XC7336 in a windowed ceramic LCC should be used. The XC7336-WC44 is pin-compatible with the XC7318-PC44. The XC7336 can be programmed to emulate the XC7318 by turning off FFB3 and FFB4. Production requirements are supported with the XC7318 in 44-pin Plastic Leaded Chip Carrier or Quad Flat Pack packages.

Xilinx offers the HW-120 programmer for use during prototyping as well as support from major third party programmer companies. For production volumes, Xilinx and their licensed distributors offer factory programming of the XC7318 devices.

For factory programming procedures, contact your local Xilinx representative.

XEPLD Translator Software

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD software. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions (Boolean, HDL etc.), or as a combination of both techniques. The XEPLD translator automatically optimizes, collapses, and implements the design as well as writing a programming file without user intervention. At the completion of the compilation process, the XEPLD translator writes detailed report files for design analysis and documentation.

Here are just a few of the XEPLD Development System features:

- *Automatic Optimization and Mapping*
  Designs are automatically minimized and mapped into the devices for optimal efficiently and high performance. Critical logic functions are automatically assigned to special resources such as high speed clocks and global output enable signals. This allows the user to concentrate on design functionality without concern for physical implementation.

- *Automatic use of UIM Resources – SMARTswitch*
  The Universal Interconnect Matrix (UIM) used in Xilinx EPLDs provides an additional level of logic at no additional delay. XEPLD automatically uses the inherent logic capability of the UIM when possible to reduce Macrocell requirements and increase speed.

- *N-to-1 PAL Conversion Utility*
  XEPLD automatically combines 20- and 24-pin standard PAL files into one top-level design file, checks for errors, and compiles the design into one or more EPLDs. The N-to-1 PAL converter is ideal for one step logic consolidation and board space reduction.

- *Complete Design Control*
  Users have the option to override the automatic features of XEPLD and selectively control any or all device resources.

- *Multiple Platform Support*
  XEPLD runs on IBM Compatible PCs, Sun, HP700, and IBM RS6000 platforms.

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CCINT}/$ V_{CCIO}	Supply voltage relative to GND Commercial $T_A = 0°$ C to 70° C	4.75	5.25	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.60	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.00	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	$I_{OH} = -4.0$ mA, $V_{CC} = $ Min	2.4		V
	3.3 V High-level output voltage	$I_{OH} = -3.2$ mA, $V_{CC} = $ Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	$I_{OL} = 24$ mA, $V_{CC} = $ Min		0.5	V
	3.3 V Low-level output voltage	$I_{OL} = 24$ mA, $V_{CC} = $ Min		0.4	V
I_{IL}	Input leakage current	$V_{CC} = $ Max, $V_{IN} = $ GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	$V_{CC} = $ Max, $V_{IN} = $ GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	$V_{IN} = $ GND, $f = 1.0$ MHz		6.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)	$V_{IN} = $ GND, $f = 1.0$ MHz		8.0	pF
C_{OUT}[1]	Output capacitance	$V_{IN} = $ GND, $f = 1.0$ MHz		10.0	pF
I_{CC}[2]	Supply current	$V_{IN} = V_{CC}$ or GND, $V_{CCINT} = V_{CCIO} = 5$V, $f = 1.0$ MHz @ 25°C	90 Typ		mA

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Notes: 1. Sample tested.
2. Measured with device programmed as two 16-bit counters.
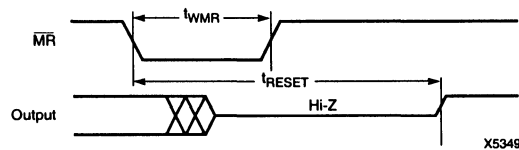
Figure 5. Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics [3]

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{PD}	Fast input to output valid [4]		5.0		7.5	ns
	I/O or input to output valid [4]		8.5		12.0	ns
t_{SU}	Fast input setup time before FCLK	4.0		5.0		ns
	I/O or input setup time before FCLK	7.0		8.5		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		ns
t_{CO}	FCLK input to output valid		4.0		4.5	ns
t_{FOE}	FOE input to output valid		7.0		7.5	ns
t_{FOD}	FOE input to output disable		7.0		7.5	ns
f_{MAX}	Max count frequency [4]	167.0		125.0		MHz
t_{WLH}	Fast Clock pulse width	3.0		4.0		ns

Notes: 3. All appropriate ac specifications tested using Figure 7 as test load circuit.
4. Assumes four product terms per output.
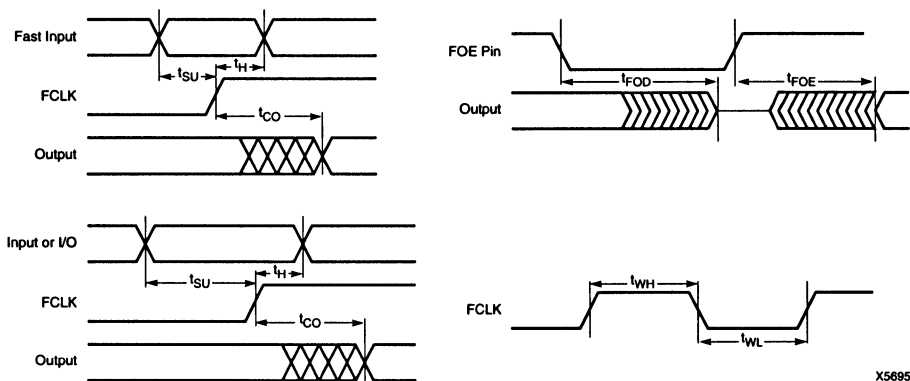
Figure 6. Switching Waveform
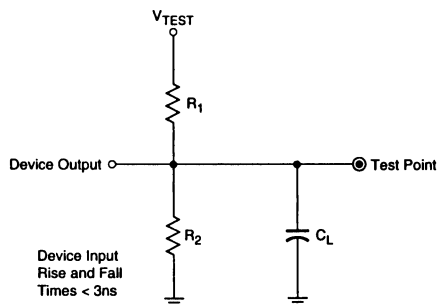
V_{CCIO} Level	V_{TEST}	R_1	R_2	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 7. AC Load Circuit
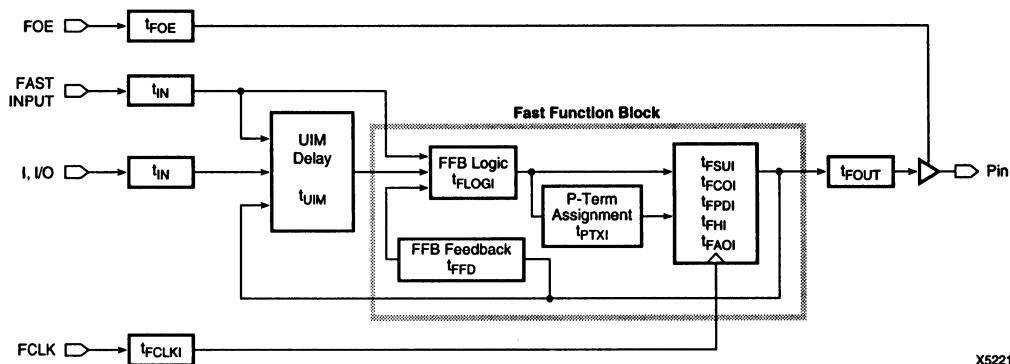
Figure 8. XC7318 Timing Model

Timing Model

Timing within the XC7318 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 8.

The timing model is based on the fixed internal delays of the XC7318 architecture which consists of three basic parts: I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7318.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [5]		1.0		1.5	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [5]		2.0		3.5	ns
t_{FSUI}	FFB register setup time	2.5		1.5		ns
t_{FHI}	FFB register hold time	1.0		2.5		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5	ns
t_{FAOI}	FFB register async. set delay		2.0		2.0	ns
t_{PTXI}	FFB p-term assignment delay		0.6		0.8	ns
t_{FFD}	FFB feedback delay		0.5		4.0	ns

Notes: 5. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		1.5		2.5	ns
t_{FOUT}	FFB output buffer and pad delay		2.0		3.0	ns
t_{UIM}	Universal Interconnect Matrix delay		3.5		4.5	ns
t_{FCLKI}	Fast clock buffer delay		1.5		1.5	ns

Combinatorial Switching Characteristics
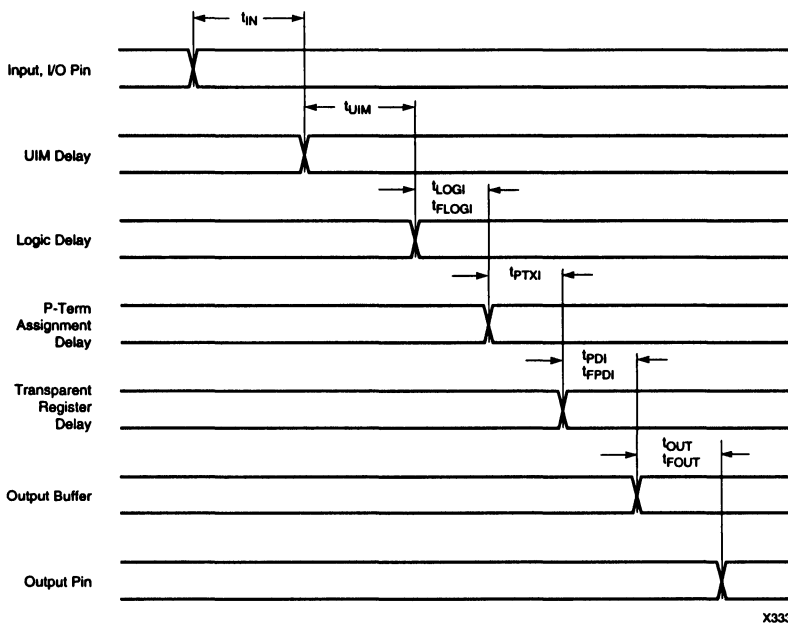
X3339

Asynchronous Clock Switching Characteristics

X3580

Synchronous Clock Switching Characteristics

F_{CLK} Pin

t_{CWF} t_{CWF}

t_{SUIN}
t_{SUCEIN}

Data/CE at Input
I/O Register

t_{HIN}
t_{HCEIN}

t_{COIN}

t_{UIM}

Input, I/O Register
to UIM

t_{FCLKI}

Fast Clock
Input Delay

t_{IN}

t_{UIM}

Data at Input
I/O Pin

t_{LOGI}
t_{FLOGI}

t_{SUI}
t_{FSUI}

t_{HI}
t_{FHI}

Data at Input
Register

t_{COI}
t_{FCOI}

t_{OUT}
t_{FOUT}

Register to
Output Pin
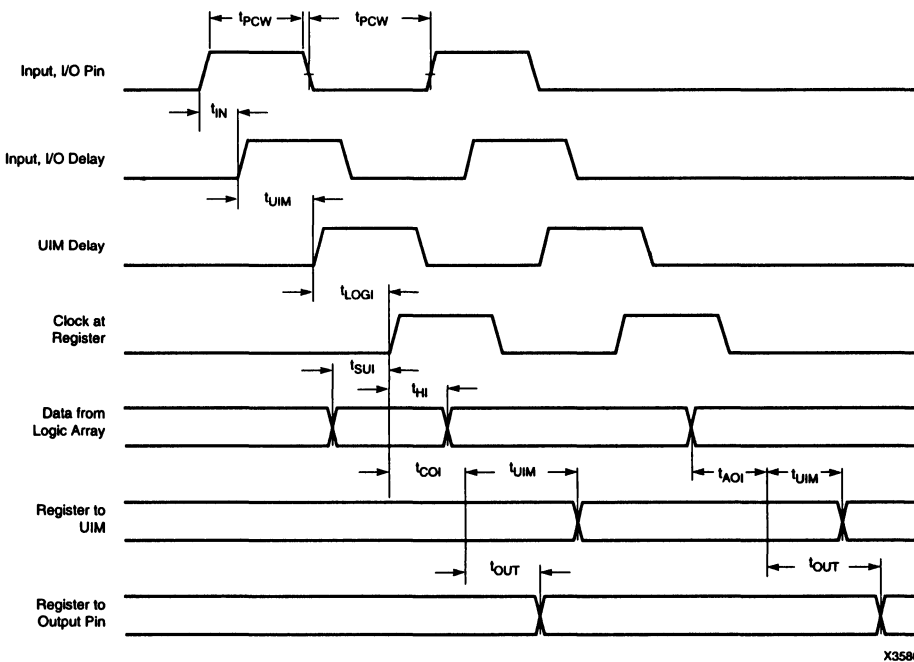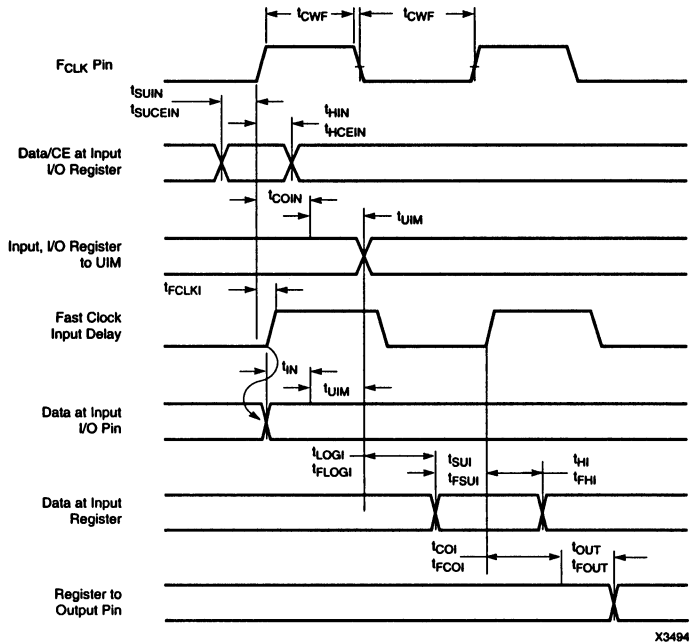
X3494

XC7318 Pinouts

PQ44	PC44	Input	XC7318	Output	PQ44	PC44	Input	XC7318	Output
39	1	I/FI	$\overline{MR}$		17	23		GND	
40	2	I/FI			18	24	I		
41	3	I/FI			19	25	I		
42	4	I/FI			20	26	I		
43	5	FCLK0			21	27	I		
44	6	FCLK1			22	28	I/FI		
1	7	I/FO/FI		MC1-1	23	29	I/FO		MC2-9
2	8	I/FO		MC1-2	24	30	I/FO		MC2-8
3	9	I/FO		MC1-3	25	31		GND	
4	10		GND		26	32		V_{CCIO}	
5	11	I/FO		MC1-4	27	33	I/FO		MC2-7
6	12	I/FO		MC1-5	28	34	I/FO		MC2-6
7	13	I/FO		MC1-6	29	35	I/FO		MC2-5
8	14	I/FO		MC1-7	30	36	I/FO		MC2-4
9	15	I/FO		MC1-8	31	37	I/FO		MC2-3
10	16	I/FO		MC1-9	32	38	I/FO		MC2-2
11	17	I			33	39	FOE1/FO		MC2-1
12	18	I/FI			34	40	FOE0		
13	19	I/FI			35	41		V_{CCINT}/V_{PP}	
14	20	I/FI			36	42	I/FI		
15	21		V_{CCINT}		37	43	I/FI		
16	22	I			38	44	I/FI		

Ordering Information

XC7318 - 5 PC 44 C

Device Type ─┘   └─ Temperature Range

Speed ─────┘   └── Number of Pins

└──── Package Type
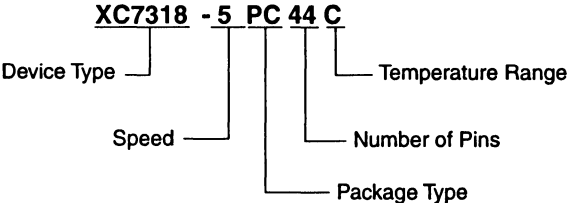
Speed Options
-7   7.5 ns pin-to-pin delay (commercial only)
-5   5 ns pin-to-pin delay (commercial only)

Packaging Options
PC44   44-Pin Plastic Leaded Chip Carrier
PQ44   44-Pin Plastic Quad Flat Pack

Temperature Options
C   Commercial   0°C to 70°C

Component Availability

Pins	44			68		84		100	144	160	225	
Type	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Windowed BGA
Code	PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC7318 -7	C		C									
-5	C		C									

C = Commercial = 0° to +70°C   X5649

XILINX®

XC7336
36-Macrocell CMOS EPLD

Product Specifications

Features

- Ultra high-performance EPLD
  - 5 ns pin-to-pin speed on all fast inputs
  - 167 MHz maximum clock frequency

- New low power XC7336Q

- 100% routable with 100% utilization

- Incorporates four PAL-like 24V9 Fast Function Blocks

- 36 Output Macrocells
  - Programmable I/O architecture
  - 24 mA drive

- High-performance µP compatible

- Peripheral Component Interface (PCI) compatible

- JEDEC standard 3.3 V or 5 V I/O operation

- Multiple security bits for design protection

- 44-pin leaded chip carrier and 44-pin quad flat pack packages

General Description

The XC7336 is a member of the Xilinx XC7300 EPLD family. It consists of four PAL-like 24V9 Fast Function Blocks

interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Each Fast Function Block has 24 inputs and contains nine Macrocells configurable for registered or combinational logic. The nine Macrocell outputs feed back to the UIM and can simultaneously drive the output pads.

The UIM allows 100% connectivity between all function blocks and input pins, providing the ability to utilize 100% of the device while eliminating routing issues.

The XC7336 is designed in 0.8 µ CMOS EPROM technology, in speed grades ranging from 5 to15 ns. The XC7336Q is also available now, providing lower power consumption in -10, -12 and -15 ns speed grades.

Device logic is automatically configured to the user's specifications using the XEPLD software. The XEPLD software is capable of optimizing and collapsing logic. The SMART-switch software/hardware feature allows implementation of buried combinatorial logic functions in the UIM, thus increasing device utilization. The XEPLD software supports third party schematic capture and HDL entry tools, as well as direct equation-based text files. Using a workstation or PC platform, designs are automatically mapped into the XC7336 in a matter of minutes.
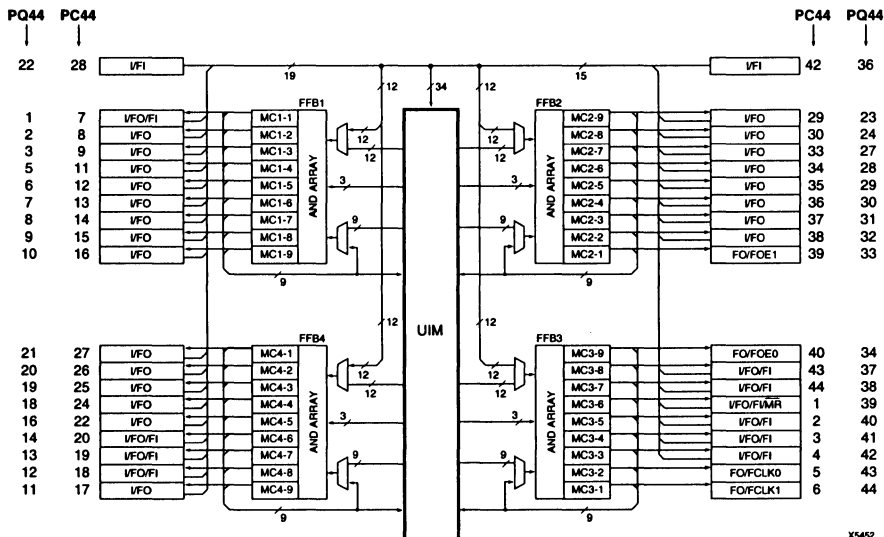
Figure 1. XC7336 Functional Block Diagram

Fast Function Blocks (FFB)

The XC7336 provides four Fast Function Blocks which have 24 inputs that can be individually selected from the UIM, 12 fast input pins, or the 9 Macrocell feedbacks from the Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive nine Macrocells in each FFB. Each Macrocell (Figure 2), can be configured for registered or combinatorial logic.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop or transparent for combinatorial outputs.

The programmable clock source is one of two global FastCLK signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

I/O Block

The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated active-High Fast Output Enable inputs or permanently enabled or disabled. The Macrocell output can also be routed back as an input to the Fast Function Block, and the UIM.

Power-On Characteristics/Master Reset

The XC7336 device undergoes a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the $\overline{MR}$ pin is tied to V_{CCINT}, the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If $\overline{MR}$ is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and $\overline{MR}$ is brought High. V_{CC} rise must be monotonic to insure the initialization sequence is performed correctly.

For additional flexibility, the $\overline{MR}$ pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of $\overline{MR}$, all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and $\overline{MR}$ is brought High. The minimum $\overline{MR}$ pulse width is t_{WMR}. If $\overline{MR}$ is brought High after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}.

Figure 2. Fast Function Block and Macrocell Schematic

X3374

Figure 3. Fast Function Block Product Term Assignment

Product Term Assignment
Each Macrocell sum-of-product OR gate can be expanded using the Export product-term assignment feature. The Export function transfers product-terms in increments of four from one Macrocell to the neighboring Macrocell (Figure 3). Complex logic functions requiring up to 36 product-terms can be implemented using all nine Macrocells within the Fast Function Block. When product-terms are assigned to adjacent Macrocells, the product-term normally dedicated to the Set or Reset function becomes the input to the Macrocell register.

Universal Interconnect Matrix
The UIM receives input from Macrocell outputs, I/O pins, and dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 24 output signals to each Fast Function Block. Each UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal polarities at the input pins, Macrocell outputs and Fast Function Block AND-array inputs, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without additional speed penalty.

3.3 V or 5 V Interface Configuration
The XC7336 can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7336 device has separate V_{CC} connections to the internal logic (V_{CCINT}) and to the I/O pads (V_{CCIO}). V_{CCINT} must always be connected to a 5 V supply. V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V. This makes the XC7336 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus simultaneously.

Low Power (Q) Devices
The XC7336-10, -12 and -15 are available in a low power variant, designated the XC7336Q.

Timing parameters for the XC7336 and the XC7336Q devices are identical. However, the XC7336Q features much lower power consumption. Using the XC7336Q will prove advantageous to any system design where power consumption and EM emissions are critical system parameters.

Power Management

The XC7336 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

For non-Q devices:

$$I_{CC}(mA) = MC_{HP} (4.3) + MC_{LP} (3.5) + MC (0.005 \, mA/MHz) \, f$$

For Q devices: (-10, -12, -15):

$$I_{CC} (mA) = MC_{HP} (2.0) + MC_{LP} (1.6) + MC (0.005 \, nA/MHz) \, f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of Macrocells used

f = Clock frequency (MHz)

Figure 4 shows a typical power calculation for the XC7336 device, programmed as two 16-bit counters and operating at the indicated clock frequency.
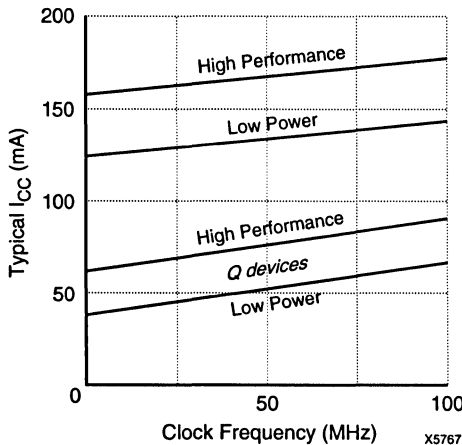
Design Security

The XC7336 has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices.

Prototyping and Programming

Xilinx offers the HW-120 programmer for use during prototyping as well as support from major third party programmer companies. For production volumes, Xilinx and their licensed distributors offer factory programming of the XC7336 devices.

For factory programming procedures, contact your local Xilinx representative.

XEPLD Translator Software

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD software. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions (Boolean, HDL etc.), or as a combination of both techniques. The XEPLD translator automatically optimizes, collapses, and implements the design as well as writing a programming file without user intervention. At the completion of the compilation process, the XEPLD translator writes detailed report files for design analysis and documentation.

Figure 4. Typical I_{CC} vs Frequency for XC7336

Here are just a few of the XEPLD Development System features:

- *Automatic Optimization and Mapping*
  Designs are automatically minimized and mapped into the devices for optimal efficiency and high performance. Critical logic functions are automatically assigned to special resources such as high speed clocks and global output enable signals. This allows the user to concentrate on design functionality without concern for physical implementation

- *Automatic use of UIM Resources – SMARTswitch*
  The Universal Interconnect Maticx (UIM) used in Xilinx EPLDs provides an additional level of logic at no additional delay. XEPLD automatically uses the inherent logic capability of the UIM when possible to reduce Macrocell requirements and increase speed.

- *N-to-1 PAL Conversion Utility*
  XEPLD automatically combines 20- and 24-pin standard PAL files into one top-level design file, checks for errors, and compiles the design into one or more EPLDs. The N-to-1 PAL converter is ideal for one step logic consolidation and board space reduction.

- *Complete Design Control*
  Users have the option to override the automatic features of XEPLD and selectively control any or all device resources.

- *Multiple Platform Support*
  XEPLD runs on IBM Compatible PCs, Sun, HP700, and IBM RS6000 platforms.

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+250	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
$V_{CCINT}/$ V_{CCIO}	Supply voltage relative to GND	Commercial	T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	T_A = -40°C to 85°C	4.50	5.50	V
	Supply voltage relative to GND	Military	T_A = -55°C to T_C = +125°C	4.50	5.50	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.60	V
V_{IL}	Low-level input voltage			0	0.80	V
V_{IH}	High-level input voltage			2.00	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage		$I_{OH} = -4.0$ mA $V_{CC} = $ Min	2.4		V
	3.3 V High-level output voltage		$I_{OH} = -3.2$ mA $V_{CC} = $ Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage		$I_{OL} = 24$ mA $V_{CC} = $ Min		0.5	V
	3.3 V Low-level output voltage		$I_{OL} = 24$ mA $V_{CC} = $ Min		0.4	V
I_{IL}	Input leakage current		$V_{CC} = $ Max $V_{IN} = $ GND or V_{CCIO}		±10.0	μA
I_{OZ}	Output high-Z leakage current		$V_{CC} = $ Max $V_{IN} = $ GND or V_{CCIO}		±10.0	μA
C_{IN}	Input capacitance for Input and I/O pins		$V_{IN} = $ GND $f = 1.0$ MHz		6.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)		$V_{IN} = $ GND $f = 1.0$ MHz		8.0	pF
C_{OUT}[1]	Output capacitance		$V_{IN} = $ GND $f = 1.0$ MHz		10.0	pF
I_{CC}[2]	Supply current	(Non-Q)	$V_{IN} = V_{CC}$ or GND $V_{CCOUT} = V_{CCCO} = 5$V $f = 1.0$ MHz @ 25°C	126 Typ		mA
		(Q)		55 Typ		

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	μs

Notes: 1. Sample tested.
2. Measured with device programmed as two 16-bit counters.

Figure 5. Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Fast input to output valid [4]		5.0		7.5		10.0		12.0		15.0	ns
	I/O or input to output valid [4]		8.5		12.0		15.0		19.0		23.0	ns
t_{SU}	Fast input setup time before FCLK	4.5		5.0		5.0		6.0		7.0		ns
	I/O or input setup time before FCLK	7.0		8.5		10.0		13.0		15.0		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		0		0		0		ns
t_{CO}	FCLK input to output valid		4.5		4.5		8.0		9.0		12.0	ns
t_{FOE}	FOE input to output valid		7.0		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.0		7.5		10.0		12.0		15.0	ns
f_{MAX}	Max count frequency [4]	167.0		125.0		100.0		80.0		66.7		MHz
t_{WLH}	Fast Clock pulse width	3.0		4.0		5.0		5.5		6.0		ns

Notes: 3. All appropriate ac specifications tested using Figure 7 as test load circuit.
4. Assumes four product terms per output.
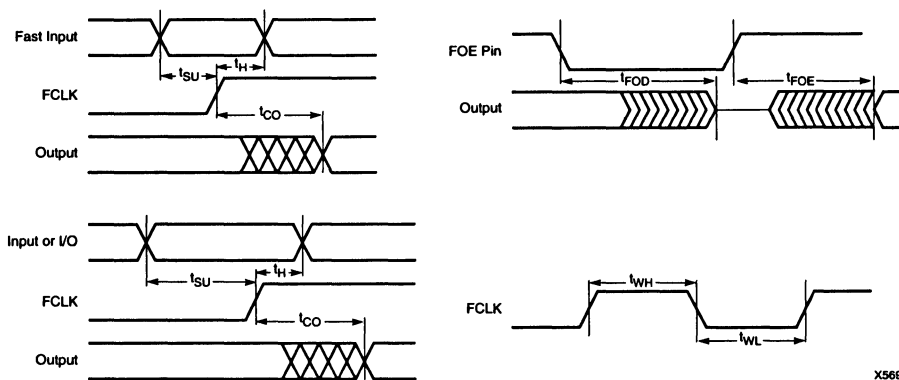
Figure 6. Switching Waveforms
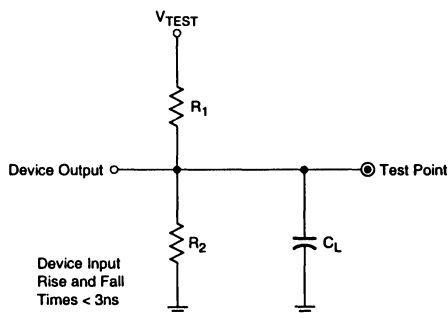
V_{CCIO} Level	V_{TEST}	R_1	R_2	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 7. AC Load Circuit
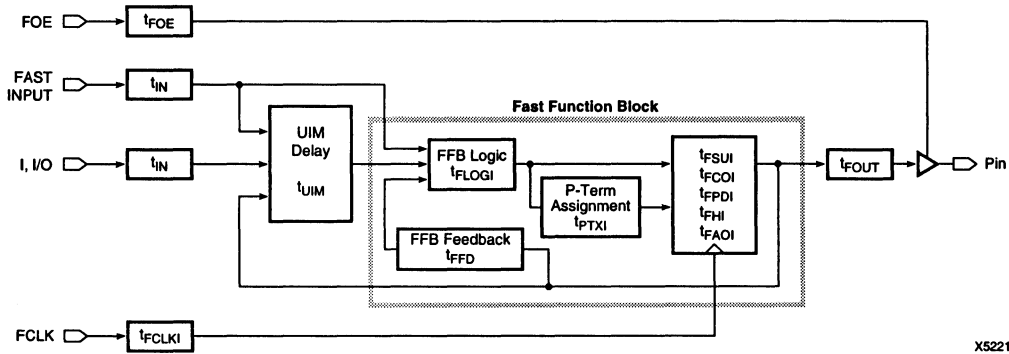
Figure 8. XC7336 Timing Model

Timing Model

Timing within the XC7336 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 8.

The timing model is based on the fixed internal delays of the XC7336 architecture which consists of three basic parts: I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7336.

Fast Function Block (FFB) Internal AC Characteristics

		XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{FLOGI}	FFB logic array delay [5]		1.0		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [5]		2.0		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	2.5		1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	1.0		2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.6		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		0.5		4.0		5.0		6.5		8.0	ns

Notes: 5. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Internal AC Characteristics

		XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{IN}	Input pad and buffer delay		1.5		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		2.0		3.0		4.5		5.0		7.0	ns
t_{UIM}	Universal Interconnect Matrix delay		3.5		4.5		5.0		7.0		8.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		1.5		2.5		3.0		4.0	ns

Combinatorial Switching Characteristics
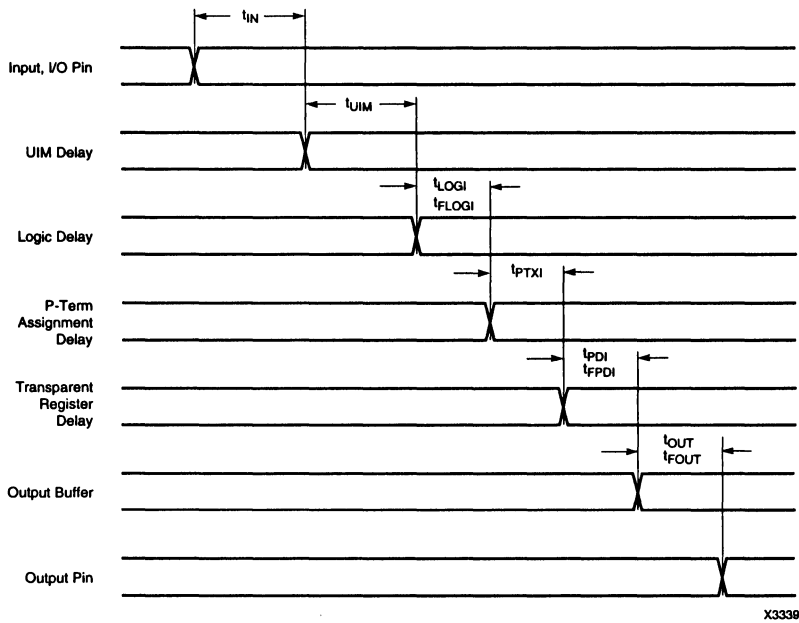
X3339

Asynchronous Clock Switching Characteristics

X3580

Synchronous Clock Switching Characteristics

X3494
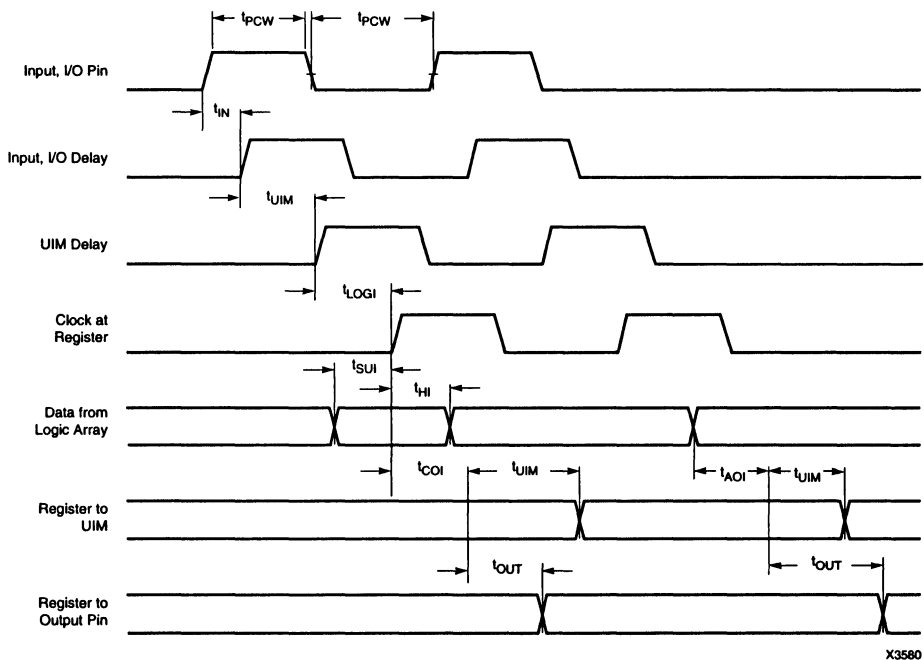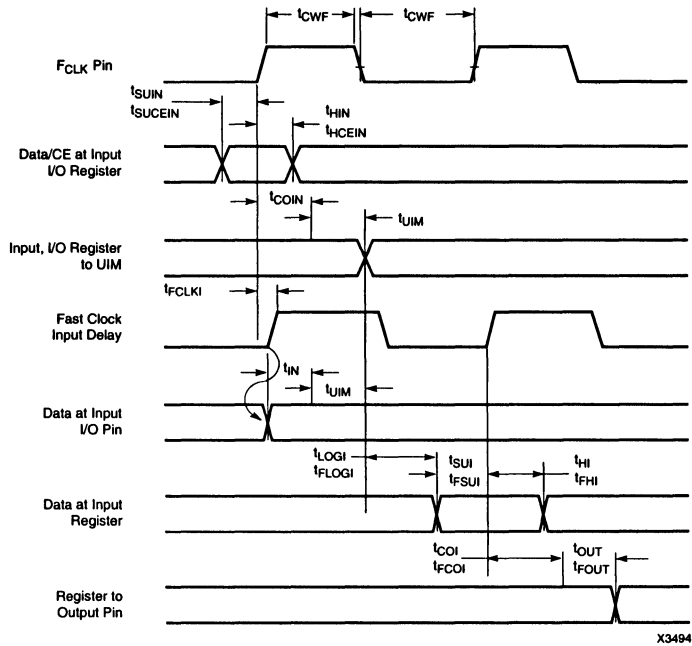
XC7336 Pinouts

PQ44	PC44	Input	XC7336	Output	PQ44	PC44	Input	XC7336	Output
39	1	I/FO/FI	$\overline{MR}$	MC3-6	17	23		GND	
40	2	I/FO/FI		MC3-5	18	24	I/FO		MC4-4
41	3	I/FO/FI		MC3-4	19	25	I/FO		MC4-3
42	4	I/FO/FI		MC3-3	20	26	I/FO		MC4-2
43	5	FO/FCLK0		MC3-2	21	27	I/FO		MC4-1
44	6	FO/FCLK1		MC3-1	22	28	I/FI		
1	7	I/FO/FI		MC1-1	23	29	I/FO		MC2-9
2	8	I/FO		MC1-2	24	30	I/FO		MC2-8
3	9	I/FO		MC1-3	25	31		GND	
4	10		GND		26	32		V_{CCIO}	
5	11	I/FO		MC1-4	27	33	I/FO		MC2-7
6	12	I/FO		MC1-5	28	34	I/FO		MC2-6
7	13	I/FO		MC1-6	29	35	I/FO		MC2-5
8	14	I/FO		MC1-7	30	36	I/FO		MC2-4
9	15	I/FO		MC1-8	31	37	I/FO		MC2-3
10	16	I/FO		MC1-9	32	38	I/FO		MC2-2
11	17	I/FO		MC4-9	33	39	FO/FOE1		MC2-1
12	18	I/FO/FI		MC4-8	34	40	FO/FOE0		MC3-9
13	19	I/FO/FI		MC4-7	35	41		V_{CCINT}/V_{PP}	
14	20	I/FO/FI		MC4-6	36	42	I/FI		
15	21		V_{CCINT}		37	43	I/FO/FI		MC3-8
16	22	I/FO		MC4-5	38	44	I/FO/FI		MC3-7

Ordering Information

XC7336 - 5 PC 44 C

Device Type ⎤
Power Option ⎯⎯ ⎤   └── Temperature Range
        Speed ⎯⎯ ⎤   └── Number of Pins
                            └── Package Type
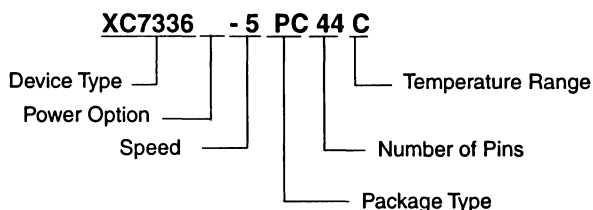
Power Options

Q   Low Power -10, -12, -15 speeds

Speed Options

-15   15 ns pin-to-pin delay
-12   12 ns pin-to-pin delay
-10   10 ns pin-to-pin delay
-7   7.5 ns pin-to-pin delay (commercial only)
-5   5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44   44-Pin Plastic Leaded Chip Carrier
WC44   44-Pin Windowed Ceramic Leaded Chip Carrier
PQ44   44-Pin Plastic Quad Flat Pack

Temperature Options

C   Commercial   0°C to70°C
I   Industrial   -40°C to 85°C

Component Availability

Pins		44			68		84		100	144	160	225	
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Windowed BGA
Code		PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC7336	-15	CI	CI	C									
	-12	CI	CI	C									
	-10	CI	CI	C									
	-7	C	C	C									
	-5	C	C	C									

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C   X5650

XILINX®

XC7354
54-Macrocell CMOS EPLD

Product Specifications

Features

- High-Performance EPLD
  - 7.5 ns pin-to-pin speed on all fast inputs
  - 125 MHz maximum clock frequency

- Advanced Dual-Block architecture
  - Two Fast Function Blocks
  - Four High-Density Function Blocks

- 100% interconnect matrix

- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators

- 54 Macrocells with programmable I/O architecture

- Up to 54 inputs programmable as direct, latched, or registered

- 18 outputs with 24 mA drive

- 3.3 V or 5 V I/O operation

- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V

- Power management options

- Multiple security bits for design protection

- 44- and 68-pin leaded chip carrier package

- 100% PCI compliant

General Description

The XC7354 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and four High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The six Function Blocks in the XC7354 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

The XC7354 device is designed in 0.8 μ CMOS EPROM technology.

Xilinx development software (XEPLD) supports all members of XC7300 family. The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator automatically performs logic optimization, collapsing, mapping and routing without user intervention. After compiling the design, XEPLD translator produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques

- Converts netlist to fuse map in minutes using a 386/486 PC or workstation platform

- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages

- Timing simulation using Viewsim, OrCAD VST, Mentor, LMC and other tools compatible with the Xilinx Netlist Format (XNF)

The XC7354 device is available in plastic and ceramic leaded chip carriers. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.
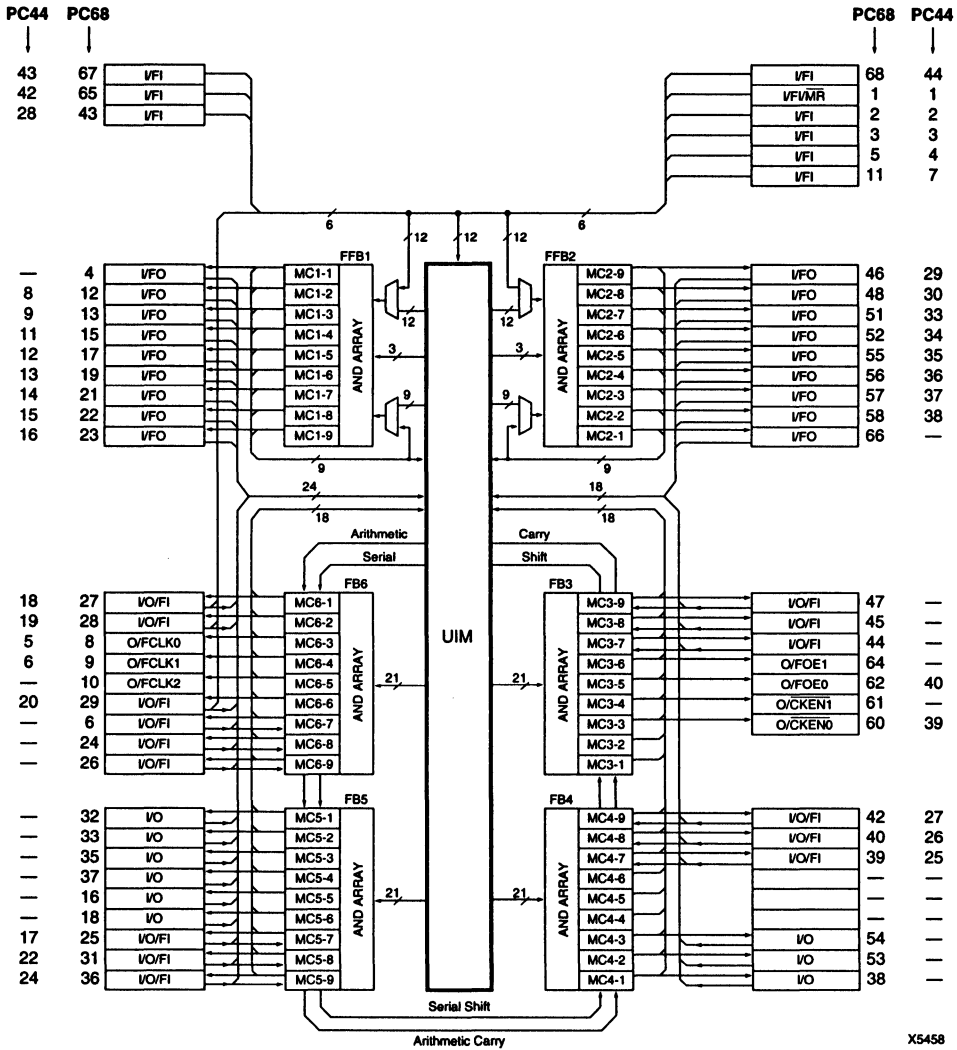
Figure 1. XC7354 Functional Block Diagram

X5458

Power Management

The XC7354 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (3.0) + MC_{LP} (2.6) + MC (0.006 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of Macrocells used

f = Clock frequency (MHz)

Figure 2 shows a typical power calculation for the XC7354 device, programmed as three 16-bit counters and operating at the indicated clock frequency.
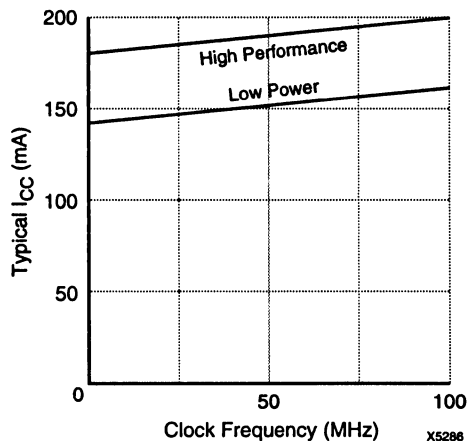
Figure 2. Typical I_{CC} vs Frequency for XC7354

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C

Warning. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
$V_{CCINT}/$ V_{CCIO}	Supply voltage relative to GND	Commercial	T_A = 0°C to 70°C		5.25	V
	Supply voltage relative to GND	Industrial	T_A = -40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	T_A= -55°C to T_C +125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA (I/O) V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_O = GND f = 1.0 MHz		20.0	pF
I_{CC1}[2]	Supply Current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5 V f = 1.0 MHz @ 25°C	140 Typ		mA

Notes: 1. Sample tested
2. Measured with device programmed as three 16-bit counters

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1,2]	125.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1,2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1,2]		12.0		16.0		19.0		23.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1,2]	95.2		76.9		66.7		55.6		MHz
t_{SU}	I/O setup time before FCLK ↑ [1,2]	10.5		13.0		15.0		18.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		13.5		17.0		20.0		24.0	ns
t_{PD}	I/O to output valid [1,2]		16.5		22.0		27.0		32.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [2]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [2]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [2]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [2]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	13.5		16.0		18.0		21.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [4]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [4]		1.0		1.5		2.0		3.0	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
4. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [2]	95.2		76.9		66.7		55.6		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		4.5		6.0		7.0		8.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3. AC Load Circuit

XC7354 Pinouts

PC68	PC44	Input	XC7354	Output	PC68	PC44	Input	XC7354	Output
1	1	I/FI/ $\overline{MR}$			35	–	I/O		MC5-3
2	2	I/FI			36	24	I/O/FI		MC5-9
3	3	I/FI			37	–	I/O		MC5-4
4	–	I/FO		MC1-1	38	–	I/O		MC4-1
5	4	I/FI			39	25	I/O/FI		MC4-7
6	–	I/O/FI		MC6-7	40	26	I/O/FI		MC4-8
7	–		GND		41	–		GND	
8	5	O/FCLK0		MC6-3	42	27	I/O/FI		MC4-9
9	6	O/FCLK1		MC6-4	43	28	I/FI		
10	–	O/FCLK2		MC6-5	44	–	I/O/FI		MC3-7
11	7	I/FI			45	–	I/O/FI		MC3-8
12	8	I/FO		MC1-2	46	29	I/FO		MC2-9
13	9	I/FO		MC1-3	47	–	I/O/FI		MC3-9
14	10		GND		48	30	I/FO		MC2-8
15	11	I/FO		MC1-4	49	31		GND	
16	–	I/O		MC5-5	50	32		V_{CCIO}	
17	12	I/FO		MC1-5	51	33	I/FO		MC2-7
18	–	I/O		MC5-6	52	34	I/FO		MC2-6
19	13	I/FO		MC1-6	53	–	I/O		MC4-2
20	–		V_{CCIO}		54	–	I/O		MC4-3
21	14	I/FO		MC1-7	55	35	I/FO		MC2-5
22	15	I/FO		MC1-8	56	36	I/FO		MC2-4
23	16	I/FO		MC1-9	57	37	I/FO		MC2-3
24	–	I/O/FI		MC6-8	58	38	I/FO		MC2-2
25	17	I/O/FI		MC5-7	59	–		V_{CCINT}	
26	–	I/O/FI		MC6-9	60	39	O/$\overline{CKEN0}$		MC3-3
27	18	I/O/FI		MC6-1	61	–	O/$\overline{CKEN1}$		MC3-4
28	19	I/O/FI		MC6-2	62	40	O/FOE0		MC3-5
29	20	I/O/FI		MC6-6	63	41		V_{CCINT}/V_{PP}	
30	21		V_{CCINT}		64	–	O/FOE1		MC3-6
31	22	I/O/FI		MC5-8	65	42	I/FI		
32	–	I/O		MC5-1	66	–	I/FO		MC2-1
33	–	I/O		MC5-2	67	43	I/FI		
34	23		GND		68	44	I/FI		

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 2-1 through 2-10.

For a detailed description of the device timing, see pages 2-8, 2-9 and 2-40 through 2-42.

For package physical dimensions and thermal data, see Section 4.
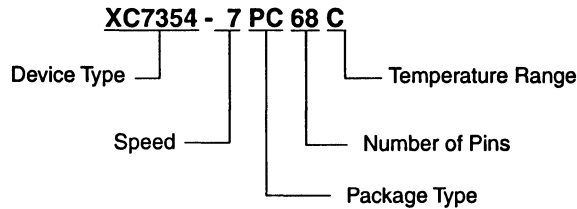
Ordering Information

XC7354 - 7 PC 68 C

Device Type ⏌

Speed ⏌

Package Type

Number of Pins

Temperature Range

Speed Options
- -15   15 ns pin-to-pin delay
- -12   12 ns pin-to-pin delay
- -10   10 ns pin-to-pin delay (commerial and industrial only)
- -7   7.5 ns pin-to-pin delay (commercial only)

Packaging Options
- PC44   44-Pin Plastic Leaded Chip Carrier
- WC44   44-Pin Windowed Ceramic Leaded Chip Carrier
- PC68   68-Pin Plastic Leaded Chip Carrier
- WC68   68-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options
- C   Commercial   0°C to 70°C
- I   Industrial   -40°C to 85°C
- M   Military   -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		44			68		84		100	144	160	225	
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Windowed BGA
Code		PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC7354	-15	CI	CI		CI	CIM							
	-12	CI	CI		CI	CIM							
	-10	CI	CI		CI	CI							
	-7	C	C		C	C							

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C   X5651

XILINX®

XC7372
72-Macrocell CMOS EPLD

Product Specifications

Features

- High-Performance EPLD
  - 7.5 ns pin-to-pin speed on all fast inputs
  - 125 MHz maximum clock frequency

- Advanced Dual-Block architecture
  - Two Fast Function Blocks
  - Six High-Density Function Blocks

- 100% interconnect matrix

- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators

- 72 Macrocells with programmable I/O architecture

- Up to 84 inputs programmable as direct, latched, or registered

- 18 outputs with 24 mA drive

- 3.3 V or 5 V I/O operation

- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V

- Power management options

- Multiple security bits for design protection

- 68-, 84-pin leaded chip carrier and 100-pin plastic quad flat pack

- 100% PCI compliant

General Description

The XC7372 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and six High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The eight Function Blocks in the XC7372 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100%

connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

The XC7372 device is designed in 0.8μ CMOS EPROM technology.

In addition, the XC7372 includes a programmable power management feature to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software (XEPLD) supports all members of the XC7300 family. The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator automatically performs logic optimization, collapsing, mapping and routing without user intervention. After compiling the design, XEPLD translator produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques

- Converts netlist to fuse map in minutes using a 386/ 486 PC or workstation platform

- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages

- Timing simulation using Viewsim, OrCAD VST, Mentor, LMC and other tools compatible with the Xilinx Netlist Format (XNF)

The XC7372 device is available in plastic and ceramic leaded chip carriers and plastic quad flat packs. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.
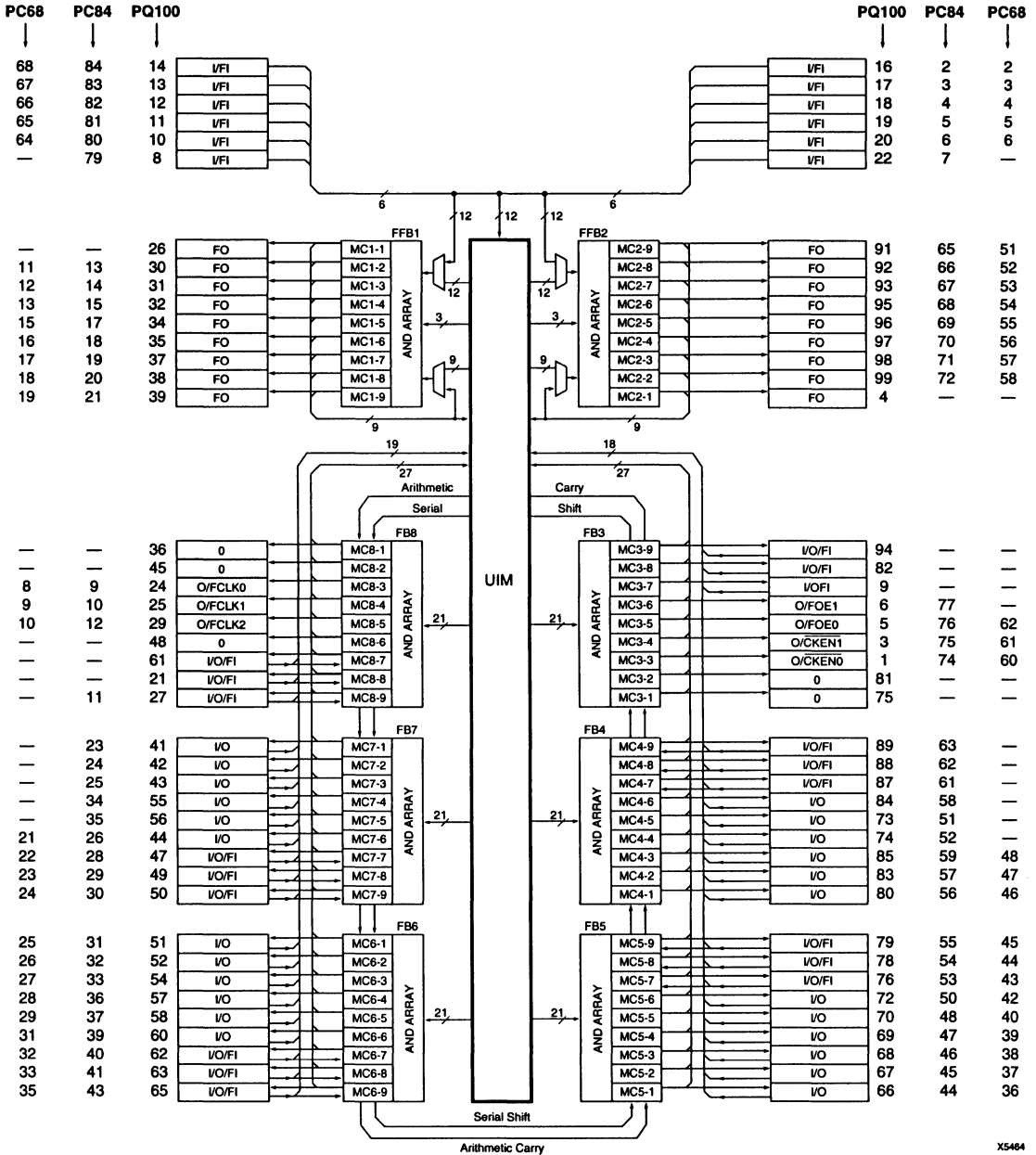
Figure 1. XC7372 Functional Block Diagram

Top I/FI blocks:

PC68	PC84	PQ100			PQ100	PC84	PC68
68	84	14	I/FI	I/FI	16	2	2
67	83	13	I/FI	I/FI	17	3	3
66	82	12	I/FI	I/FI	18	4	4
65	81	11	I/FI	I/FI	19	5	5
64	80	10	I/FI	I/FI	20	6	6
—	79	8	I/FI	I/FI	22	7	—

FFB1 / FFB2 (AND ARRAY):

PC68	PC84	PQ100					PQ100	PC84	PC68
—	—	26	FO	MC1-1	MC2-9	FO	91	65	51
11	13	30	FO	MC1-2	MC2-8	FO	92	66	52
12	14	31	FO	MC1-3	MC2-7	FO	93	67	53
13	15	32	FO	MC1-4	MC2-6	FO	95	68	54
15	17	34	FO	MC1-5	MC2-5	FO	96	69	55
16	18	35	FO	MC1-6	MC2-4	FO	97	70	56
17	19	37	FO	MC1-7	MC2-3	FO	98	71	57
18	20	38	FO	MC1-8	MC2-2	FO	99	72	58
19	21	39	FO	MC1-9	MC2-1	FO	4	—	—

Arithmetic Carry / Serial Shift

FB8 / FB3 (AND ARRAY, UIM):

PC68	PC84	PQ100					PQ100	PC84	PC68
—	—	36	0	MC8-1	MC3-9	I/O/FI	94	—	—
—	—	45	0	MC8-2	MC3-8	I/O/FI	82	—	—
8	9	24	O/FCLK0	MC8-3	MC3-7	I/OFI	9	—	—
9	10	25	O/FCLK1	MC8-4	MC3-6	O/FOE1	6	77	—
10	12	29	O/FCLK2	MC8-5	MC3-5	O/FOE0	5	76	62
—	—	48	0	MC8-6	MC3-4	O/CKEN1	3	75	61
—	—	61	I/O/FI	MC8-7	MC3-3	O/CKEN0	1	74	60
—	—	21	I/O/FI	MC8-8	MC3-2	0	81	—	—
—	11	27	I/O/FI	MC8-9	MC3-1	0	75	—	—

FB7 / FB4 (AND ARRAY):

PC68	PC84	PQ100					PQ100	PC84	PC68
—	23	41	I/O	MC7-1	MC4-9	I/O/FI	89	63	—
—	24	42	I/O	MC7-2	MC4-8	I/O/FI	88	62	—
—	25	43	I/O	MC7-3	MC4-7	I/O/FI	87	61	—
—	34	55	I/O	MC7-4	MC4-6	I/O	84	58	—
—	35	56	I/O	MC7-5	MC4-5	I/O	73	51	—
21	26	44	I/O	MC7-6	MC4-4	I/O	74	52	—
22	28	47	I/O/FI	MC7-7	MC4-3	I/O	85	59	48
23	29	49	I/O/FI	MC7-8	MC4-2	I/O	83	57	47
24	30	50	I/O/FI	MC7-9	MC4-1	I/O	80	56	46

FB6 / FB5 (AND ARRAY):

PC68	PC84	PQ100					PQ100	PC84	PC68
25	31	51	I/O	MC6-1	MC5-9	I/O/FI	79	55	45
26	32	52	I/O	MC6-2	MC5-8	I/O/FI	78	54	44
27	33	54	I/O	MC6-3	MC5-7	I/O/FI	76	53	43
28	36	57	I/O	MC6-4	MC5-6	I/O	72	50	42
29	37	58	I/O	MC6-5	MC5-5	I/O	70	48	40
31	39	60	I/O	MC6-6	MC5-4	I/O	69	47	39
32	40	62	I/O/FI	MC6-7	MC5-3	I/O	68	46	38
33	41	63	I/O/FI	MC6-8	MC5-2	I/O	67	45	37
35	43	65	I/O/FI	MC6-9	MC5-1	I/O	66	44	36

Serial Shift

Arithmetic Carry

X5464

Power Management

The XC7372 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} \text{ (3.1)} + MC_{LP} \text{ (2.6)} + MC \text{ (0.012 mA/MHz) f}$$

Where:

MC$_{HP}$ = Macrocells in high-performance mode

MC$_{LP}$ = Macrocells in low-power mode

MC = Total number of Macrocells used

f = Clock frequency (MHz)

Figure 2 shows typical power calculation for the XC7372 programmed as four 16-bit counters and operating at the indicated clock frequency.
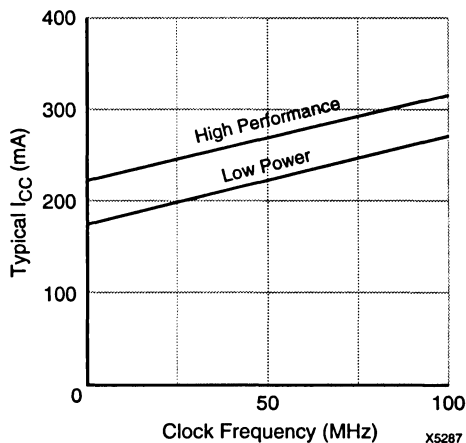
Figure 2. Typical I$_{CC}$ vs Frequency for XC7372

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
$V_{CCINT}/$ V_{CCIO}	Supply voltage relative to GND	Commercial	T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	T_A = -40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	T_A = -55°C to T_C +125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		10.0	pF
C_{OUT} [1]	Output capacitance	V_O = GND f = 1.0 MHz		20.0	pF
I_{CC1} [2]	Supply Current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5 V f = 1.0 MHz @ 25°C	187 Typ		mA

Notes: 1. Sample tested
2. Measured with device programmed as four 16-bit counters

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics [3]

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1,2]	125.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1,2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1,2]		12.0		17.0		20.0		24.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1,2]	95.2		71.4		62.5		52.6		MHz
t_{SU}	I/O setup time before FCLK ↑ [1,2]	10.5		14.0		16.0		19.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		13.5		18.0		21.0		25.0	ns
t_{PD}	I/O to output valid [1,2]		16.5		23.0		28.0		33.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes:
1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
3. All appropriate AC specifications using Figure 3 as test load circuit.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [2]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [2]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [2]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [2]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	13.5		17.0		19.0		22.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [4]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [4]		1.0		1.5		2.0		3.0	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
4. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [2]	95.2		71.4		62.5		52.6		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		4.5		7.0		8.0		9.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3. AC Load Circuit

XC7372 Pinouts

PQ100	PC84	PC68	Input	XC7372	Output
15	1	1		$\overline{\text{MR}}$	
16	2	2	I/FI		
17	3	3	I/FI		
18	4	4	I/FI		
19	5	5	I/FI		
20	6	6	I/FI		
21	–	–	I/O/FI		MC8-8
22	7	–	I/FI		
23	8	7		GND	
24	9	8	O/FCLK0		MC8-3
25	10	9	O/FCLK1		MC8-4
26	–	–	FO		MC1-1
27	11	–	I/O/FI		MC8-9
28	–	–		V_{CCIO}	
29	12	10	O/FCLK2		MC8-5
30	13	11	FO		MC1-2
31	14	12	FO		MC1-3
32	15	13	FO		MC1-4
33	16	14		GND	
34	17	15	FO		MC1-5
35	18	16	FO		MC1-6
36	–	–	O		MC8-1
37	19	17	FO		MC1-7
38	20	18	FO		MC1-8
39	21	19	FO		MC1-9
40	22	20		V_{CCIO}	
41	23	–	I/O		MC7-1
42	24	–	I/O		MC7-2
43	25	–	I/O		MC7-3
44	26	21	I/O		MC7-6
45	–	–	O		MC8-2
46	27	–		GND	
47	28	22	I/O/FI		MC7-7
48	–	–	O		MC8-6
49	29	23	I/O/FI		MC7-8
50	30	24	I/O/FI		MC7-9
51	31	25	I/O		MC6-1
52	32	26	I/O		MC6-2
53	–	–		V_{CCIO}	
54	33	27	I/O		MC6-3
55	34	–	I/O		MC7-4
56	35	–	I/O		MC7-5
57	36	28	I/O		MC6-4
58	37	29	I/O		MC6-5
59	38	30		V_{CCINT}	
60	39	31	I/O		MC6-6
61	–	–	I/O/FI		MC8-7
62	40	32	I/O/FI		MC6-7
63	41	33	I/O/FI		MC6-8
64	42	34		GND	
65	43	35	I/O/FI		MC6-9
66	44	36	I/O		MC5-1
67	45	37	I/O		MC5-2
68	46	38	I/O		MC5-3
69	47	39	I/O		MC5-4
70	48	40	I/O		MC5-5
71	49	41		GND	
72	50	42	I/O		MC5-6
73	51	–	I/O		MC4-5
74	52	–	I/O		MC4-4
75	–	–	O		MC3-1
76	53	43	I/O/FI		MC5-7
77	–	–		GND	
78	54	44	I/O/FI		MC5-8
79	55	45	I/O/FI		MC5-9
80	56	46	I/O		MC4-1
81	–	–	O		MC3-2
82	–	–	I/O/FI		MC3-8
83	57	47	I/O		MC4-2
84	58	–	I/O		MC4-6
85	59	48	I/O		MC4-3
86	60	49		GND	
87	61	–	I/O/FI		MC4-7
88	62	–	I/O/FI		MC4-8
89	63	–	I/O/FI		MC4-9
90	64	50		V_{CCIO}	
91	65	51	FO		MC2-9
92	66	52	FO		MC2-8
93	67	53	FO		MC2-7
94	–	–	I/O/FI		MC3-9
95	68	54	FO		MC2-6
96	69	55	FO		MC2-5
97	70	56	FO		MC2-4
98	71	57	FO		MC2-3
99	72	58	FO		MC2-2
100	73	59		V_{CCINT}	
1	74	60	O/$\overline{\text{CKEN0}}$		MC3-3
2	–	–		GND	
3	75	61	O/$\overline{\text{CKEN1}}$		MC3-4
4	–	–	FO		MC2-1
5	76	62	O/FOE0		MC3-5
6	77	–	O/FOE1		MC3-6
7	78	63		V_{CCINT}/V_{PP}	
8	79	–	I/FI		
9	–	–	I/O/FI		MC3-7
10	80	64	I/FI		
11	81	65	I/FI		
12	82	66	I/FI		
13	83	67	I/FI		
14	84	68	I/FI		

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 2-1 through 2-10.

For a detailed description of the device timing, see pages 2-9, 2-10 and 2-50 through 2-58.

For package physical dimensions and thermal data, see Section 4.
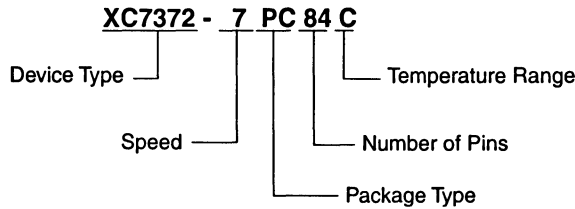
Ordering Information

XC7372 - 7 PC 84 C

Device Type ⎤

Speed ⎤

Temperature Range

Number of Pins

Package Type

Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PQ100	100-Pin Plastic Quad Flat Pack

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C (Ambient) to 125°C (Case)

Component Availability

Pins	44			68		84		100	144	160	225	
Type	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Windowed BGA
Code	PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC7372 -15				CI	CIM	CI	CIM	CI				
-12				CI	CIM	CI	CI	CI				
-10				CI	CI	CI	CI	CI				
-7				C	C	C	C	C				

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C

Parenthesis indicate future product plans

X5652

XILINX®

XC73108
108-Macrocell CMOS EPLD

Product Specifications

Features

- High-Performance EPLD
  - 7.5 ns pin-to-pin speed on all fast inputs
  - 125 MHz maximum clock frequency

- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 10 High-Density Function Blocks

- 100% interconnect matrix

- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 56 MHz 18-bit accumulators

- 108 Macrocells with programmable I/O architecture

- Up to 120 inputs programmable as direct, latched, or registered

- 18 outputs with 24 mA drive

- 3.3 V or 5 V I/O operation

- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V

- Power management options

- Multiple security bits for design protection

- 84-pin leaded chip carrier, 144-pin pin-grid-array packages, 100-, 160-pin plastic quad flat pack and 225-pin ball grid array

- 100% PCI compliant

General Description

The XC73108 is a member of the Xilinx Dual-Block EPLD family. It consists of two Fast Function Blocks and ten High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The eight Function Blocks in the XC73108 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

The XC73108 device is designed in 0.8μ CMOS EPROM technology.

In addition, the XC73108 includes a programmable power management feature to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software (XEPLD) supports all members of the XC7300 family. The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator automatically performs logic optimization, collapsing, mapping and routing without user intervention. After compiling the design, XEPLD translator produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques

- Converts netlist to fuse map in minutes using a 386/486 PC or workstation platform

- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages

- Timing simulation using Viewsim, OrCAD VST, Mentor, LMC and other tools compatible with the Xilinx Netlist Format (XNF)

The XC73108 device is available in plastic and ceramic leaded chip carriers, pin-grid-arrays, plastic quad flat packs and ball-grid-array packages. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.

Left side pin assignments

PC84	PQ100	BG225/PG144	PQ160	Type	MC	Block
84	14	H1	19	I/FI		
83	13	H2	18	I/FI		
82	12	G1	17	I/FI		
81	11	G3	15	I/FI		
80	10	E1	13	I/FI		
79	8	F3	11	I/FI		
—	26	N3	36	FO	MC1-1	FFB1
13	30	P4	44	FO	MC1-2	
14	31	P5	47	FO	MC1-3	
15	32	N6	49	FO	MC1-4	
17	34	P7	54	FO	MC1-5	
18	35	R6	56	FO	MC1-6	
19	37	P8	58	FO	MC1-7	
20	38	R8	59	FO	MC1-8	
21	39	N8	60	FO	MC1-9	
—	—	F14	105	I/O	MC12-1	FB12
—	—	E15	107	I/O	MC12-2	
—	—	D15	109	I/O	MC12-3	
—	—	E13	112	I/O	MC12-4	
—	—	B15	114	I/O	MC12-5	
—	—	A14	123	I/O	MC12-6	
—	—	C11	125	I/O/FI	MC12-7	
—	—	A12	128	I/O/FI	MC12-8	
—	75	C13	116	I/O/FI	MC12-9	
—	—	B10	130	I/O	MC11-1	FB11
—	—	A5	147	I/O	MC11-2	
—	—	A4	151	I/O	MC11-3	
—	—	B4	153	I/O	MC11-4	
—	—	B3	155	I/O	MC11-5	
—	—	C3	158	I/O	MC11-6	
—	81	C10	129	I/O/FI	MC11-7	
—	82	A11	133	I/O/FI	MC11-8	
—	94	B6	145	I/O/FI	MC11-9	
—	—	K2	25	O	MC10-1	FB10
—	—	L1	27	O	MC10-2	
9	24	N2	33	O/FCLK0	MC10-3	
10	25	M3	35	O/FCLK1	MC10-4	
12	29	P3	42	O/FCLK2	MC10-5	
—	—	P1	34	O	MC10-6	
—	—	L3	32	I/O/FI	MC10-7	
—	21	M1	29	I/O/FI	MC10-8	
11	27	P2	37	I/O/FI	MC10-9	
23	41	R9	62	I/O	MC9-1	FB9
24	42	R10	63	I/O	MC9-2	
25	43	P9	64	I/O	MC9-3	
34	55	M14	86	I/O	MC9-4	
35	56	N15	88	I/O	MC9-5	
26	44	N10	68	I/O	MC9-6	
28	47	R12	71	I/O/FI	MC9-7	
29	48	P12	73	I/O/FI	MC9-8	
30	50	P13	75	I/O/FI	MC9-9	
31	51	N12	77	I/O	MC8-1	FB8
32	52	P14	79	I/O	MC8-2	
33	54	N14	82	I/O	MC8-3	
36	57	M15	90	I/O	MC8-4	
37	58	K14	92	I/O	MC8-5	
39	60	J13	95	I/O	MC8-6	
40	62	J15	97	I/O/FI	MC8-7	
41	63	H14	98	I/O/FI	MC8-8	
43	65	G13	101	I/O/FI	MC8-9	

Right side pin assignments

Block	MC	Type	PQ160	BG225/PG144	PQ100	PC84
		I/FI	22	J1	16	2
		I/FI	23	K1	17	3
		I/FI	24	J2	18	4
		I/FI	26	K3	19	5
		I/FI	28	L2	20	6
		I/FI	30	N1	22	7
FFB2	MC2-9	FO	142	A7	91	65
	MC2-8	FO	143	A6	92	66
	MC2-7	FO	144	B7	93	67
	MC2-6	FO	146	C6	95	68
	MC2-5	FO	148	B5	96	69
	MC2-4	FO	152	A3	97	70
	MC2-3	FO	154	C5	98	71
	MC2-2	FO	156	A2	99	72
	MC2-1	FO	4	B1	4	—
FB3	MC3-9	I/O/FI	96	K15	61	—
	MC3-8	I/O/FI	93	L15	—	—
	MC3-7	I/O/FI	91	K13	—	—
	MC3-6	I/O	89	L14	—	—
	MC3-5	I/O	87	L13	—	—
	MC3-4	I/O	84	P15	—	—
	MC3-3	I/O	78	N13	—	—
	MC3-2	I/O	76	R14	—	—
	MC3-1	I/O	74	N11	—	—
FB4	MC4-9	I/O/FI	72	R13	48	—
	MC4-8	I/O/FI	69	R11	45	—
	MC4-7	I/O/FI	57	R7	36	—
	MC4-6	I/O	67	P10	—	—
	MC4-5	I/O	55	N7	—	—
	MC4-4	I/O	50	P6	—	—
	MC4-3	I/O	48	R4	—	—
	MC4-2	I/O	45	N5	—	—
	MC4-1	I/O	43	R2	—	—
FB5	MC5-9	I/O/FI	16	F1	—	—
	MC5-8	I/O/FI	14	G2	—	—
	MC5-7	I/O/FI	12	F2	9	—
	MC5-6	O/FOE1	8	C1	6	77
	MC5-5	O/FOE0	6	D2	5	76
	MC5-4	O/CKEN1	2	C2	3	75
	MC5-3	O/CKEN0	159	B2	1	74
	MC5-2	O	9	E2	—	—
	MC5-1	O	7	E3	—	—
FB6	MC6-9	I/O/FI	140	C8	89	63
	MC6-8	I/O/FI	139	A8	88	62
	MC6-7	I/O/FI	138	B8	87	61
	MC6-6	I/O	135	C9	84	58
	MC6-5	I/O	113	C14	73	51
	MC6-4	I/O	115	D13	74	52
	MC6-3	I/O	136	A10	85	59
	MC6-2	I/O	134	B9	83	57
	MC6-1	I/O	126	A13	80	56
FB7	MC7-9	I/O/FI	124	B12	79	55
	MC7-8	I/O/FI	122	B13	78	54
	MC7-7	I/O/FI	117	B14	76	53
	MC7-6	I/O	111	D14	72	50
	MC7-5	I/O	108	E14	70	48
	MC7-4	I/O	106	F13	69	47
	MC7-3	I/O	104	G14	68	46
	MC7-2	I/O	103	F15	67	45
	MC7-1	I/O	102	G15	66	44

Central interconnect block labels: UIM, AND ARRAY, Arithmetic, Serial, Carry, Shift, Serial Shift, Arithmetic Carry

X5454

Figure 1. XC73108 Functional Block Diagram

Power Management

The XC73108 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} \, (2.4) + MC_{LP} \, (2.1) + MC \, (0.015 \text{ mA/MHz}) \, f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of Macrocells used
f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC73108 device, programmed as six 16-bit counters and operating at the indicated clock frequency.
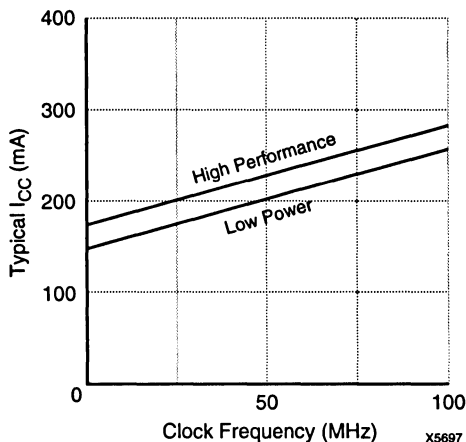

Figure 2. Typical I_{CC} vs Frequency for XC73108

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning. *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.*

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
$V_{CCINT}/$ V_{CCIO}	Supply voltage relative to GND	Commercial	$T_A = 0°C$ to $70°C$	4.75	5.25	V
	Supply voltage relative to GND	Industrial	$T_A = -40°C$ to $85°C$	4.5	5.5	V
	Supply voltage relative to GND	Military	$T_C = -55°C$ to $125°C$	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50.0	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	μA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	μA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT} [1]	Output capacitance	V_O = GND f = 1.0 MHz		20.0	pF
I_{CC1} [2]	Supply Current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5 V f = 1.0 MHz @ 25°C	227 Typ		mA

Notes: 1. Sample tested
2. Measured with device programmed as six 16-bit counters

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	μs

Fast Function Block (FFB) External AC Characteristics [3]

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1,2]	125.0		100.0		80.0		66.7		50.0		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		10.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0		15.0	ns
t_{PDFO}	Fast input to output valid [1,2]		7.5		10.0		12.0		15.0		20.0	ns
t_{PDFU}	I/O to output valid [1,2]		13.5		19.0		22.0		27.0		35.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		6.0		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1,2]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SU}	I/O setup time before FCLK ↑ [1,2]	12.0		16.0		18.0		22.0		28.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0		20.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		12.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		20.0		23.0		28.0		36.0	ns
t_{PD}	I/O to output valid [1,2]		18.0		25.0		30.0		36.0		45.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		12.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.

2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

3. All appropriate AC specifications tested using Figure 3 as test load circuit.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [2]		1.5		1.5		2.0		2.0		3.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [2]		3.5		5.5		7.0		8.0		11.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		4.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0		2.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0		6.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5		2.0	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0		10.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [2]		3.5		3.5		4.0		5.0		6.0	ns
t_{LOGILP}	Low power FB logic delay [2]		7.0		7.5		9.0		11.0		14.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		6.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0		7.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		31.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		20.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		12.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0		9.0	ns
t_{CARY8}	ALU carry delay within 1 FB [4]		5.0		6.0		8.0		12.0		15.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [4]		1.0		1.5		2.0		3.0		4.0	ns

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

4. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

I/O Block External AC Characteristics

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [2]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		10.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0		6.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		12.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		6.0		ns

Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com Only)		XC73108-10 (Com Only)		XC73108-12 (Com/Ind Only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0		6.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0		9.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0		14.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0		15.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0		20.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0		20.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0		5.0	ns

Note: 2.   Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.
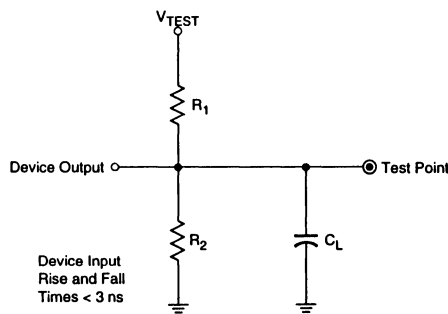
Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3. AC Load Circuit

XC73108 Pinouts

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output	PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
1	D3	–	–		V_{CCIO}		41	N4	28	–		V_{CCIO}	
2	C2	3	75	O/CKEN1		MC5-4	42	P3	29	12	O/FCLK2		MC10-5
3	–	–	–		N/C		43	R2	–	–	I/O		MC4-1
4	B1	4	–	FO		MC2-1	44	P4	30	13	FO		MC1-2
5	–	–	–		N/C		45	N5	–	–	I/O		MC4-2
6	D2	5	76	O/FOE0		MC5-5	46	R3	–	–		V_{CCINT}	
7	E3	–	–	O		MC5-1	47	P5	31	14	FO		MC1-3
8	C1	6	77	O/FOE1		MC5-6	48	R4	–	–	I/O		MC4-3
9	E2	–	–	O		MC5-2	49	N6	32	15	FO		MC1-4
10	D1	7	78		V_{CCINT}/V_{PP}		50	P6	–	–	I/O		MC4-4
11	F3	8	79	I/FI			51	R5	33	16		GND	
12	F2	9	–	I/O/FI		MC5-7	52	–	–	–		N/C	
13	E1	10	80	I/FI			53	–	–	–		N/C	
14	G2	–	–	I/O/FI		MC5-8	54	P7	34	17	FO		MC1-5
15	G3	11	81	I/FI			55	N7	–	–	I/O		MC4-5
16	F1	–	–	I/O/FI		MC5-9	56	R6	35	18	FO		MC1-6
17	G1	12	82	I/FI			57	R7	36	–	I/O/FI		MC4-7
18	H2	13	83	I/FI			58	P8	37	19	FO		MC1-7
19	H1	14	84	I/FI			59	R8	38	20	FO		MC1-8
20	H3	–	–		GND		60	N8	39	21	FO		MC1-9
21	J3	15	1		$\overline{MR}$		61	N9	40	22		V_{CCIO}	
22	J1	16	2	I/FI			62	R9	41	23	I/O		MC9-1
23	K1	17	3	I/FI			63	R10	42	24	I/O		MC9-2
24	J2	18	4	I/FI			64	P9	43	25	I/O		MC9-3
25	K2	–	–	O		MC10-1	65	–	–	–		N/C	
26	K3	19	5	I/FI			66	–	–	–		N/C	
27	L1	–	·	O		MC10-2	67	P10	–	–	I/O		MC4-6
28	L2	20	6	I/FI			68	N10	44	26	I/O		MC9-6
29	M1	21	–	I/O/FI		MC10-8	69	R11	45	–	I/O/FI		MC4-8
30	N1	22	7	I/FI			70	P11	46	27		GND	
31	M2	23	8		GND		71	R12	47	28	I/O/FI		MC9-7
32	L3	–	–	I/O/FI		MC10-7	72	R13	48	–	I/O/FI		MC4-9
33	N2	24	9	O/FCLK0		MC10-3	73	P12	49	29	I/O/FI		MC9-8
34	P1	–	–	O		MC10-6	74	N11	–	–	I/O		MC3-1
35	M3	25	10	O/FCLK1		MC10-4	75	P13	50	30	I/O/FI		MC9-9
36	N3	26	–	FO		MC1-1	76	R14	–	–	I/O		MC3-2
37	P2	27	11	I/O/FI		MC10-9	77	N12	51	31	I/O		MC8-1
38	–	–	–		N/C		78	N13	–	–	I/O		MC3-3
39	–	–	–		N/C		79	P14	52	32	I/O		MC8-2
40	R1	–	–		GND		80	R15	–	–		GND	

Note: With the XC73108 in the 225-pin ball grid array package, only 144 of the solder balls are connected, the remaining solder balls should be left unconnected

XC73108 Pinouts (continued)

PQ160	PG144 BG225	PQ100	PC84	Input	XC7308	Output	PQ160	PG144 BG225	PQ100	PC84	Input	XC7308	Output
81	M13	53	–		V_{CCIO}		121	C12	–	–		V_{CCIO}	
82	N14	54	33	I/O		MC8-3	122	B13	78	54	I/O/FI		MC7-8
83	–	–	–		N/C		123	A14	–	–	I/O		MC12-6
84	P15	–	–	I/O		MC3-4	124	B12	79	55	I/O/FI		MC7-9
85	–	–	–		N/C		125	C11	–	–	I/O/FI		MC12-7
86	M14	55	34	I/O		MC9-4	126	A13	80	56	I/O		MC6-1
87	L13	–	–	I/O		MC3-5	127	B11	–	–		GND	
88	N15	56	35	I/O		MC9-5	128	A12	–	–	I/O/FI		MC12-8
89	L14	–	–	I/O		MC3-6	129	C10	81	–	I/O/FI		MC11-7
90	M15	57	36	I/O		MC8-4	130	B10	–	–	I/O		MC11-1
91	K13	–	–	I/O/FI		MC3-7	131	–	–	–		N/C	
92	K14	58	37	I/O		MC8-5	132	–	–	–		N/C	
93	L15	–	–	I/O/FI		MC3-8	133	A11	82	–	I/O/FI		MC11-8
94	J14	59	38		V_{CCINT}		134	B9	83	57	I/O		MC6-2
95	J13	60	39	I/O		MC8-6	135	C9	84	58	I/O		MC6-6
96	K15	61	–	I/O/FI		MC3-9	136	A10	85	59	I/O		MC6-3
97	J15	62	40	I/O/FI		MC8-7	137	A9	86	60		GND	
98	H14	63	41	I/O/FI		MC8-8	138	B8	87	61	I/O/FI		MC6-7
99	H15	–	–		GND		139	A8	88	62	I/O/FI		MC6-8
100	H13	64	42		GND		140	C8	89	63	I/O/FI		MC6-9
101	G13	65	43	I/O/FI		MC8-9	141	C7	90	64		V_{CCIO}	
102	G15	66	44	I/O		MC7-1	142	A7	91	65	FO		MC2-9
103	F15	67	45	I/O		MC7-2	143	A6	92	66	FO		MC2-8
104	G14	68	46	I/O		MC7-3	144	B7	93	67	FO		MC2-7
105	F14	–	–	I/O		MC12-1	145	B6	94	–	I/O/FI		MC11-9
106	F13	69	47	I/O		MC7-4	146	C6	95	68	FO		MC2-6
107	E15	–	–	I/O		MC12-2	147	A5	–	–	I/O		MC11-2
108	E14	70	48	I/O		MC7-5	148	B5	96	69	FO		MC2-5
109	D15	–	–	I/O		MC12-3	149	–	–	–		N/C	
110	C15	71	49		GND		150	–	–	–		N/C	
111	D14	72	50	I/O		MC7-6	151	A4	–	–	I/O		MC11-3
112	E13	–	–	I/O		MC12-4	152	A3	97	70	FO		MC2-4
113	C14	73	51	I/O		MC6-5	153	B4	–	–	I/O		MC11-4
114	B15	–	–	I/O		MC12-5	154	C5	98	71	FO		MC2-3
115	D13	74	52	I/O		MC6-4	155	B3	–	–	I/O		MC11-5
116	C13	75	–	I/O/FI		MC12-9	156	A2	99	72	FO		MC2-2
117	B14	76	53	I/O/FI		MC7-7	157	C4	100	73		V_{CCINT}	
118	–	–	–		N/C		158	C3	–	–	I/O		MC11-6
119	–	–	–		N/C		159	B2	1	74	O/CKEN0		MC5-3
120	A15	77	–		GND		160	A1	2	–		GND	

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 2-1 through 2-10.

For a detailed description of the device timing, see pages 2-9, 2-10 and 2-59 through 2-61.

For package physical dimensions and thermal data, see Section 4.

Ordering Information

XC73108 - 7 PC 84 C

Device Type ⌐

Temperature Range

Speed ⌐

Number of Pins

Package Type
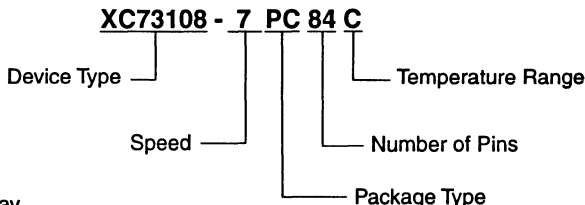
Speed Options
- -20 20 ns pin-to-pin delay
- -15 15 ns pin-to-pin delay
- -12 12 ns pin-to-pin delay (commercial and industrial only)
- -10 10 ns pin-to-pin delay (commercial only)
- -7 7.5 ns pin-to-pin delay (commercial only)

Temperature Options
- C Commercial 0°C to 70°C
- I Industrial -40°C to 85°C
- M Military -55°C (Ambient) to 125°C (Case)

Packaging Options
- PC84 84-Pin Plastic Leaded Chip Carrier
- WC84 84-Pin Windowed Ceramic Leaded Chip Carrier
- PQ100 100-Pin Plastic Quad Flat Pack
- PG144 144-Pin Windowed Pin-Grid-Array
- PQ160 160-Pin Plastic Quad Flat Pack
- BG225 225-Pin Plastic Ball-Grid-Array
- WB225 225-Pin Windowed Ball-Grid-Array

Component Availability

Pins		44			68		84		100	144	160	225	
Type	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Windowed BGA	
Code	PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225	
XC73108 -20						CI	CI	CI	CIM	CI	CI	(C)	
-15						CI	CI	CI	CIM	CI	CI	(C)	
-12						CI	CI	CI	CI	CI	CI	(C)	
-10						C	C	C	C	C	C	(C)	
-7						C	C	C	C	C	C	(C)	

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C

Parenthesis indicate future product plans

X5698

XC73144
144-Macrocell CMOS EPLD

Product Specifications

Features

- High-Performance EPLD
  - 7.5 ns pin-to-pin speed on all fast inputs
  - 100 MHz maximum clock frequency

- Advanced Dual-Block architecture
  - Four Fast Function Blocks
  - Twelve High-Density Function Blocks

- 100% interconnect matrix

- High-Speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 MHz 16-bit accumulators

- 144 Macrocells with programmable I/O architecture

- Up to 132 inputs programmable as direct, latched, or registered

- All outputs with 24 mA drive

- 3.3 V or 5 V I/O operation

- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V

- Power management options

- Multiple security bits for design protection

- 160-pin plastic quad flat pack and 225-pin ball-grid-array packages

- 100% PCI compliant

- Programmable slew rate

- Programmable ground control

General Description

The XC73144 is a member of the Xilinx Dual-Block EPLD family. It consists of four Fast Function Blocks and twelve High-Density Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The sixteen Function Blocks in the XC73144 are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM and output pins.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

The XC73144 is designed in a 0.8 μ CMOS EPROM technology.

In addition, the XC73144 includes a programmable power management feature to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to minimize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software (XEPLD) supports all members of XC7300 family. The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator automatically performs logic optimization, collapsing, mapping and routing without user intervention. After compiling the design, XEPLD translator produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques

- Converts netlist to fuse map in minutes using a 386/486 PC or workstation platform

- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages

- Timing simulation using Viewsim, OrCAD VST, Mentor, LMC and other tools compatible with the Xilinx Netlist Format (XNF)

Figure 1. XC73144 Functional Block, Diagram

X5653

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter			Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND	Commercial	$T_A = 0^oC$ to 70^oC	4.75	5.25	V
	Supply voltage relative to GND	Industrial	$T_A = -40^oC$ to 85^oC	4.5	5.5	V
	Supply voltage relative to GND	Military	$T_A = -55^oC$ to $T_C = +125^oC$	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND			3.0	3.6	V
V_{IL}	Low-level input voltage			0	0.8	V
V_{IH}	High-level input voltage			2.0	V_{CC} +0.5	V
V_O	Output voltage			0	V_{CCIO}	V
T_{IN}	Input signal transition time				50.0	ns

Power Management

The XC73144 features a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}(mA) = MC_{HP} (2.4) + MC_{LP} (2.1) + MC (0.015 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of Macrocells used
f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC73144 device, programmed as eight 16-bit counters and operating at the indicated clock frequency.
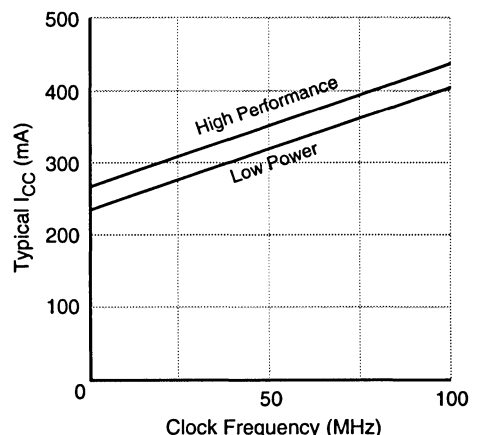

Figure 2. Typical I_{CC} vs Frequency for XC73144

X5768

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT} [1]	Output capacitance	V_O = GND f = 1.0 MHz		20.0	pF
I_{CC1} [2]	Supply Current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5 V f = 1.0 MHz @ 25°C	250 Typ		mA

Notes: 1. Sample tested
2. Measured with device programmed as eight 16-bit counters

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Slew Rate and Programmable Ground Control

Due to the large number of high current drivers available on the XC73144, two programmable signal management features have been included – slew rate control (SRC) and ground control (GC). Slew rate control is primarily for external system benefit, to reduce ringing and other coupling phenomenon. SRC permits designers to select either 1 V/ns or 1.5 V/ns slew rate on a pin-by-pin basis for any output or I/O signal. This can be done with PLUSASM or schematically, as needed. The defafult slew rate is 1 V/ns. To assign the pins with equations (PLUSASM), the designer needs to only declare them as follows:

FAST ON <signal name list>

This will assign the signals in the list to have a 1.5 V/ns slew rate. Omitting the signal name list will globally set all signals to be 1.5 V/ns. Specific signals therefore can be declared with 1 V/ns slew rate as follows:

FAST OFF <signal name list>

Schematic control of SRC is also straightforward. Again, the default is 1 V/ns, but to assign specific pins fast, the designer need only attach the "FAST" attribute to the I/O or output buffer or the corresponding pin.

Programmable ground control is useful for internal chip signal management. The output buffers of the Fast Function Blocks have an impedance of around 7 Ω when switching high to low, where the High Density Function Blocks impedance is around 14 Ω. Since this low impedance is negligible compared to the impedance of the pin inductance when output current transients occur, a reasonable ground connection can be made by driving unused output pins low and physically attaching them to external ground. The XC73144 architecture permits the automatic assignment of external ground signals to all Macrocells that are not declared as primary outputs or I/Os. Note that the logical function of the buried Macrocell is fully preserved, while its output driver is driving low and physically attached to ground. Should designers not wish to employ programmable ground control, they need only declare all such pins as primary I/Os whether they will be attached externally or not.

Fast Function Block (FFB) External AC Characteristics [3]

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1,2]	105.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1,2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1,2]		13.5		19.0		22.0		27.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1,2]	83.3		62.5		55.6		45.5		MHz
t_{SU}	I/O setup time before FCLK ↑ [1,2]	12.0		16.0		18.0		22.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		20.0		23.0		28.0	ns
t_{PD}	I/O to output valid [1,2]		18.0		25.0		30.0		36.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Preliminary

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.

2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

3. All appropriate AC specifications tested using Figure 3 as the test load circuit.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [2]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [2]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [2]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [2]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [4]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [4]		1.0		1.5		2.0		3.0	ns

Preliminary

Notes: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

4. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for adder with registered outputs.

## I/O Block External AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Max pipeline frequency (input register to FFB or FB register) [2]	83.3		62.5		55.6		45.5		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Internal AC Characteristics

Symbol	Parameter	XC73144-7 (Com Only)		XC73144-10 (Com Only)		XC73144-12 (Com/Ind Only)		XC73144-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns

Preliminary

Note: 2. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF
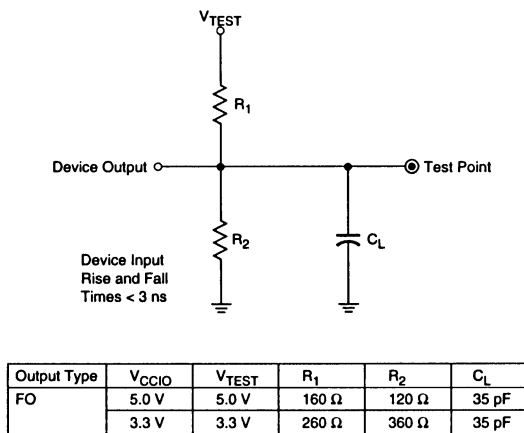
X3491

Figure 3. AC Load Circuit

XC73144 Pinouts

BG225	PQ160	Input	XC73144	Output
D3	1	V_{CCIO}		
E4	-	I/FO		MC3-4
F4	-	I/FO		MC3-2
C2	2	O/CKEN1		MC7-4
F5	-	I/FO		MC3-1
G4	3	I/FO		MC3-5
B1	4	I/FO		MC2-1
J4	5	I/FO		MC3-3
D2	6	O/FOE0		MC7-5
E3	7	O		MC7-1
C1	8	O/FOE1		MC7-6
E2	9	O		MC7-2
D1	10	V_{CCINT}/V_{PP}		
F3	11	I/FI		
F2	12	I/O/FI		MC7-7
E1	13	I/FI		
G2	14	I/O/FI		MC7-8
G3	15	I/FI		
F1	16	I/O/FI		MC7-9
G1	17	I/FI		
H2	18	I/FI		
H1	19	I/FI		
H3	20	GND		
J3	21	I/FI	MR	
K5	-	V_{CCIO}		
J1	22	I/FI		
K1	23	I/FI		
J2	24	I/FI		
K2	25	O		MC14-1
K3	26	I/FI		
L1	27	O		MC14-2
L2	28	I/FI		
M1	29	I/O/FI		MC14-8
N1	30	I/FI		
M2	31	GND		
L3	32	I/O/FI		MC14-7
N2	33	O/FCLK0		MC14-3
P1	34	O		MC14-6
M3	35	O/FCLK1		MC14-4
N3	36	I/FO		MC1-1
K4	-	I/FO		MC4-1
L4	-	I/FO		MC4-2
P2	37	I/O/FI		MC14-9
M4	38	I/FO		MC4-3
L5	39	I/FO		MC4-5
R1	40	GND		

BG225	PQ160	Input	XC73144	Output
N4	41	V_{CCIO}		
P3	42	O/FCLK2		MC14-5
R2	43	I/O		MC6-1
P4	44	I/FO		MC1-2
N5	45	I/O		MC6-2
R3	46	V_{CCINT}		
M5	-	I/FO		MC4-4
P5	47	I/FO		MC1-3
R4	48	I/O		MC6-3
L6	-	I/FO		MC4-6
M6	-	I/FO		MC4-8
N6	49	I/FO		MC1-4
P6	50	I/O		MC6-4
R5	51	GND		
M7	52	I/FO		MC4-7
M9	53	I/FO		MC4-9
P7	54	I/FO		MC1-5
N7	55	I/O		MC6-5
R6	56	I/FO		MC1-6
R7	57	I/O/FI		MC6-7
P8	58	I/FO		MC1-7
R8	59	I/FO		MC1-8
N8	60	I/FO		MC1-9
N9	61	V_{CCIO}		
M10	-	O		MC13-1
L10	-	O		MC13-2
R9	62	I/O		MC12-1
R10	63	I/O		MC12-2
P9	64	I/O		MC12-3
L11	65	O		MC13-6
M11	66	I/O/FI		MC13-7
M12	-	GND		
P10	67	I/O		MC6-6
N10	68	I/O		MC12-6
R11	69	I/O/FI		MC6-8
P11	70	GND		
R12	71	I/O/FI		MC12-7
R13	72	I/O/FI		MC6-9
P12	73	I/O/FI		MC12-8
N11	74	I/O		MC5-1
P13	75	I/O/FI		MC12-9
R14	76	I/O		MC5-2
N12	77	I/O		MC11-1
N13	78	I/O		MC5-3
P14	79	I/O		MC11-2
R15	80	GND		

XC73144 Pinouts (continued)

BG225	PQ160	Input	XC73144	Output
M13	81	V_{CCIO}		
L12	-	O		MC13-3
K12	-	O		MC13-4
N14	82	I/O		MC11-3
K11	-	O		MC13-5
J12	83	I/O/FI		MC13-8
P15	84	I/O		MC5-4
G12	85	I/O/FI		MC13-9
M14	86	I/O		MC12-4
L13	87	I/O		MC5-5
N15	88	I/O		MC12-5
L14	89	I/O		MC5-6
M15	90	I/O		MC11-4
K13	91	I/O/FI		MC5-7
K14	92	I/O		MC11-5
L15	93	I/O/FI		MC5-8
J14	94	V_{CCINT}		
J13	95	I/O		MC11-6
K15	96	I/O/FI		MC5-9
J15	97	I/O/FI		MC11-7
H14	98	I/O/FI		MC11-8
H15	99	GND		
H13	100	GND		
F11	-	V_{CCINT}		
G13	101	I/O		MC11-9
G15	102	I/O		MC10-1
F15	103	I/O		MC10-2
G14	104	I/O		MC10-3
F14	105	I/O		MC16-1
F13	106	I/O		MC10-4
E15	107	I/O		MC16-2
E14	108	I/O		MC10-5
D15	109	I/O		MC16-3
C15	110	GND		
D14	111	I/O		MC10-6
E13	112	I/O		MC16-4
C14	113	I/O		MC9-5
B15	114	I/O		MC16-5
D13	115	I/O		MC9-4
C13	116	I/OFI		MC16-9
F12	-	O		MC8-1
E12	-	O		MC8-2
B14	117	I/O/FI		MC10-7
E11	118	O		MC8-6
D12	119	I/O/FI		MC8-7
A15	120	GND		

BG225	PQ160	Input	XC73144	Output
C12	121	V_{CCIO}		
B13	122	I/O/FI		MC10-8
A14	123	I/O		MC16-6
B12	124	I/O/FI		MC10-9
C11	125	I/O/FI		MC16-7
A13	126	I/O		MC9-1
D11	-			
B11	127	GND		
A12	128	I/O/FI		MC16-8
E10	-			MC8-4
D10	-			MC8-5
C10	129	I/O/FI		MC15-7
B10	130	I/O		MC15-1
D9	131	I/O/FI		MC8-8
D7	132	I/O/FI		MC8-9
A11	133	I/O/FI		MC15-8
B9	134	I/O		MC9-2
C9	135	I/O		MC9-6
A10	136	I/O		MC9-3
A9	137	GND		
B8	138	I/O/FI		MC9-7
A8	139	I/O/FI		MC9-8
C8	140	I/O/FI		MC9-9
C7	141	V_{CCIO}		
A7	142	I/FO		MC2-9
A6	143	I/FO		MC2-8
B7	144	I/FO		MC2-7
B6	145	I/O/FI		MC15-9
C6	146	I/FO		MC2-6
D6	-	I/FO		MC3-8
E6	-	I/FO		MC3-6
A5	147	I/O		MC15-2
B5	148	I/FO		MC2-5
D5	149	I/FO		MC3-9
E5	150	I/FO		MC3-7
A4	151	I/O		MC15-3
A3	152	I/FO		MC2-4
B4	153	I/O		MC15-4
C5	154	I/FO		MC2-3
D4	-	GND		
B3	155	I/O		MC15-5
A2	156	I/FO		MC2-2
C4	157	V_{CCINT}		
C3	158	I/O		MC15-6
B2	159	O/CKEN0		MC7-3
A1	160	GND		

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 2-1 through 2-10.

For a detailed description of the device timing, see pages 2-9, 2-10 and 2-50 through 2-52.

For package physical dimensions and thermal data, see Section 4.
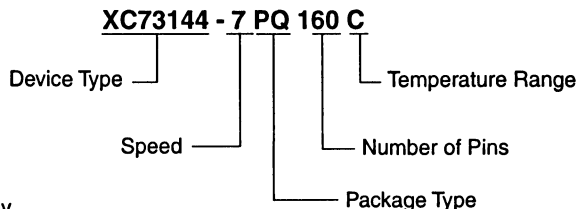
Ordering Information

XC73144 - 7 PQ 160 C

Device Type ⎤

Speed ⎤

Temperature Range

Number of Pins

Package Type

Speed Options
-15   15 ns pin-to-pin delay
-12   12 ns pin-to-pin delay
-10   10 ns pin-to-pin delay (commercial only)
-7   7.5 ns pin-to-pin delay (commercial only)

Packaging Options
PQ160   160-Pin Plastic Quad Flat Pack
BG225   225-Pin Plastic Ball-Grid-Array

Temperature Options
C   Commercial   0°C to 70°C
I   Industrial   -40°C to 85°C

Component Availability

Pins	44			68		84		100	144	160	225	
Type	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA	Ceramic BGA
Code	PC44	WC44	PQ44	PC68	WC68	PC84	WC84	PQ100	PG144	PQ160	BG225	WB225
XC73144 -15										CI	CI	CI
-12										CI	CI	CI
-10										C	C	C
-7										C	C	C

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C

Parenthesis indicate future product plans

X5654

1   Applications

2   XC7300 EPLD Family

3   XC7200A EPLD Family

4   Packages

5   Software and Programming

6   Quality, Testing and Reliability

7   Sales Offices

XILINX®

XC7200 EPLD Family

XILINX®

XC7236A
36-Macrocell CMOS EPLD

Product Specifications

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 36 Macrocells, grouped into four Function Blocks, interconnected by a programmable Universal Interconnect Matrix (UIM)
- Each Function Block contains a programmable AND-array with up to 24 complementary inputs, providing up to 17 product terms per Macrocell
- Enhanced logic features
  - Arithmetic Logic Unit in each Macrocell
  - Dedicated fast carry network between Macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all Macrocell logic paths
- 36 signal pins
  - 30 I/Os, 2 inputs, 4 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ± 0.3 V
- Three high-speed, low-skew global clock inputs
- 44-pin plastic and windowed ceramic leaded chip carrier packages

General Description

The XC7236A is a second-generation High Density Programmable Logic Device that combines the classical features of the PAL-like EPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output Macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each Macrocell. Dedicated fast arithmetic carry lines running directly between adjacent Macrocells and Function Blocks support fast adders, subtractors and comparators of any length up to 36 bits.

This additional ALU in each Macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent Macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and Macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Function Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 36 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7236A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Automated design mapping and optimization is supported by Xilinx XEPLD development software based on design capture using third-party schematic entry tools, PLD compilers or direct text-based equation files. Design mapping is completed in a few minutes on a PC or Worstation.

Architectural Overview

Figure 1 shows the XC7236A structure. Four Function Blocks (FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output Macrocells (MCs) that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macrocells drive a 3-state chip output; all feed back into the UIM.
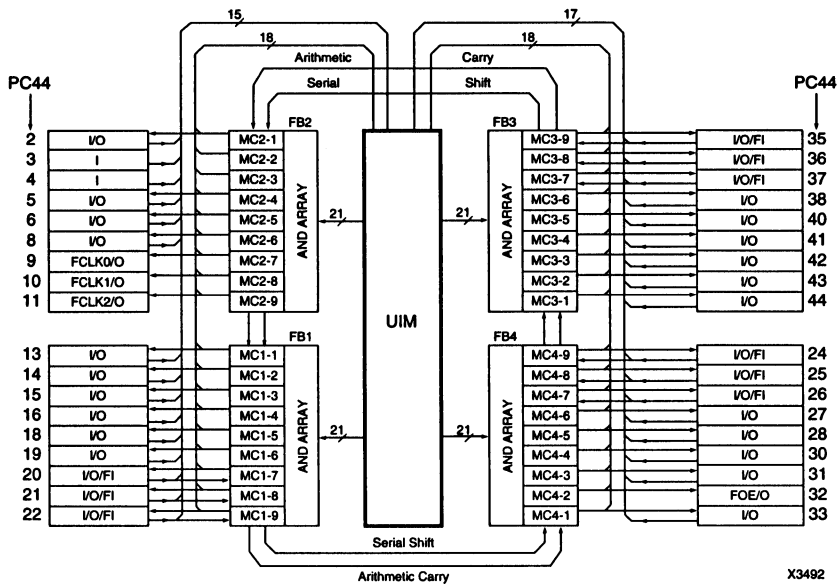
Figure 1. XC7236A Architecture

Function Blocks and Macrocells

The XC7236A contains 36 Macrocells with identical structure, grouped into four Function Blocks of nine Macrocells each. Each Macrocell is driven by product terms derived from a programmable AND array in the Function Block. The AND array in each Function Block receives 21 signals and their complements from the UIM. In three Function Blocks, the AND array receives three additional inputs and their complements directly from FastInput (FI) pins, thus offering faster logic paths.

Five product terms are private to each Macrocell; an additional 12 product terms are shared among the nine Macrocells in each Function Block. Four of the private product terms can be selectively ORed together with up to four of the shared product terms, and drive the D1 input to the ALU. The other input, D2, to the ALU is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms.

As a programmable option, four of the private product terms can be used for other purposes. One of the private product terms can be used as a dedicated clock for the flip-flop in the Macrocell. (See the subsequent description of other clocking options.) Another one of the private product terms can be the asynchronous active-High Reset of the Macrocell flip-flop, another one can be the asynchronous active-High Set of the Macrocell flip-flop, and another one can be the Output Enable signal.

As a configuration option, the Macrocell output can be fed back and ORed into the D2 input to the ALU after being ANDed with three of the shared product terms to implement counters and toggle flip-flops.

The ALU has two programmable modes: In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to max 17 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block in each Macrocell can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the next lower Macrocell. It also feeds a carry output to the next higher Macrocell. This carry propagation chain crosses the boundaries between Function Blocks. This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture, when trying to perform arithmetic functions.

The ALU output drives the D input of the Macrocell flip-flop. Each flip-flop has several programmable options. One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock. Otherwise, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable and is either the dedicated product term mentioned earlier, or one of two global FastCLK signals (FLCK0 or FLCK1) that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each Macrocell flip-flop can be preloaded with either 0 or 1.

X1829

Figure 2. Function Block and Macrocell Schematic

In addition to driving a chip output pin, the Macrocell output is also routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output pin driver and/or the feedback to the UIM. If configured to control UIM feedback, then when the OE product-term is de-asserted, the UIM feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 68 inputs: 36 from the Macrocell feedbacks, 30 from bidirectional I/O pins, and 2 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 84 output signals, 21 to each Function Block.

Any one of the 68 inputs can be programmed to be connected to any number of the 84 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity.

Routability is not an issue in that any UIM input can drive any UIM output or multiple outputs without additional delay.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion at the input pin, Macrocell outputs and Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function. This offers an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such Macrocell outputs programmed onto the same UIM output thus emulating a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Thirty-four of the 36 Macrocell drive chip outputs directly through individually programmable inverters followed by 3-state output buffers; each can be individually controlled by the Output Enable product term mentioned above. An additional configuration option disables the output permanently. One dedicated FastOE input can also be configured to control any of the chip outputs instead of, or in conjunction with the individual OE product term.

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip flop. Latch and flip-flop can be programmed with either of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they

Figure 3. Input/Output Schematic

incur the combinatorial delay in the device, provided the one-clock-period pipeline latency is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

3.3 V or 5 V Interface configuration

The XC7236A can be used in systems with two different supply voltages, 5 V or 3.3 V. The device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O output drivers (V_{CCIO}). V_{CCINT} is always connected to a nominal +5 V supply, but V_{CCIO} may be connected to either +5 V or +3.3 V, depending on the output interface requirement.

When V_{CCIO} is connected to +5 V, the input thresholds are TTL levels, and thus compatible with 5 V or 3.3 V logic, and the output high levels are compatible with 5 V systems. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7236A ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed such that the I/O can also safely interface to a mixed 3.3-V or 5-V bus.

Programming and Using the XC7236A

The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connec-
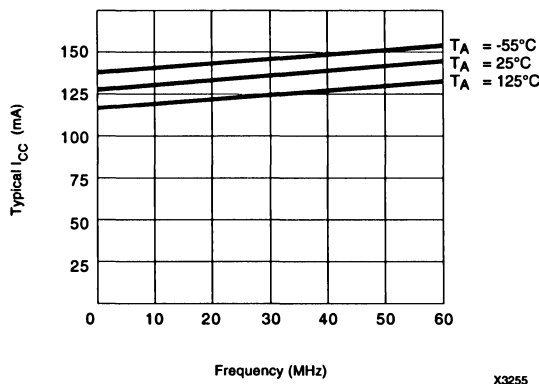
Figure 4. Typical I_{CC} vs Frequency for XC7236A Configured as Eight 4-bit Counters (V_{CC} = +5.0 V, V_{IN} = 0 or 5 V, all outputs open)

tions are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. This can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 μs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the Macrocell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 μF using high-speed (tantalum or ceramic) capacitors.

3-5

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
V_{CCIO}	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_C= –55°C to 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage 3.3 V	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL high-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V high-level output	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V low-level output voltage	I_{OL} = 12 mA V_{CC} = Min		0.5	V
	3.3 V low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{CC}	Supply Current	V_{IN}= 0 V V_{CC} = Max f = 0 MHz	126 mA Typ		
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output High-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance (sample tested)	V_{IN} = GND f = 1.0 MHz		10.0	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		*XC7236A-16		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK	6	40		50		60		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term clock	6	40		50		60		MHz
f_{CYC4} (Note 5)	Max Macrocell toggle frequency using local feedback and FastCLK		50		50		60		MHz
f_{CLK} (Note 5)	Max Macrocell register transmission frequency (without feedback) using FastCLK		45		50		60		MHz
f_{CLK1} (Note 5)	Max Macrocell register transmission frequency (without feedback) using a Product-Term clock		42		50		60		MHz
f_{CLK2} (Note 5)	Max input register transmission frequency (without feedback) using FastCLK		50		50		60		MHz
f_{CLK3} (Note 1)	Max input register to Macrocell register pipline frequency using FastCLK	7	33		40		60		MHz
t_W	FastCLK pulse width (High/Low)	11	10		8		6		ns
t_{W1}	Product-Term clock width (active/inactive)	11	12		9		7		ns
t_{SU}	Input to Macrocell register set-up time before FastCLK	9	29		24		18		ns
t_H	Input to Macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to Macrocell register set-up time before Product-Term clock	8	16		14		10		ns
t_{H1}	Input to Macrocell register hold time after Product-Term clock	8	0		0		0		ns
t_{SU2}	Input register/latch set-up time before FastCLK	10	8		8		6		ns
t_{H2}	Input register/latch hold time after FastCLK	10	0		0		0		ns
t_{SU5}	FastInput to Macrocell register set-up time before FastCLK		20		18		15		ns
t_{H5}	FastInput to Macrocell register hold time after FastCLK		0		0		0		ns
t_{WA}	Set/Reset pulse width (active)	11	12		12		10		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	30		25		20		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		0		0		ns
t_{RA1}	Set/Reset input recovery time before Product-Term clock	11	15		15		12		ns
t_{HA1}	Set/Reset input hold time after P-Term clock	11	9		9		8		ns
t_{HRS}	Product-Term clock width (active/inactive)		10		10		8		ns

*Commercial/Industrial Only

X5208

Propagation Delays

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		*XC7236A-16		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to register output delay	11	5	14	3	13	3	10	ns
t_{CO1}	P-Term clock input to registered output delay	11	10	30	5	24	5	20	ns
t_{AO}	Set/Reset input to registered output delay	11	10	40	5	32	5	25	ns
t_{PD} (Note 1)	Input to nonregistered output delay	11	10	40	5	32	5	25	ns
t_{OE}	Input to output enable	11	10	32	5	25	5	20	ns
t_{OD}	Input to output disable	11	10	32	5	25	5	20	ns
t_{PD5}	FastInput to non-registered Macrocell output delay		10	31	5	25	5	20	ns
t_{OE5}	FastInput to output enable		5	23	3	20	3	15	ns
t_{OD5}	FastInput to output disable		5	23	3	20	3	15	ns
t_{FOE}	FOE input to output enable		5	15	3	14	3	12	ns
t_{FOD}	FOE input to output disable		5	15	3	14	3	12	ns

*Commercial/Industrial Only

X5209

Incremental Parameters

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		*XC7236A-16		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent Macrocells	12		1.2		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent Macrocells in a Function Block	12		6		5		3	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 Macrocells from Macrocell #n to Macrocell #n in next F Block	12		9		6		4	ns
t_{COF1}	Incremental delay from UIM-input (for P-Term clock) to registered Macrocell feedback	13		12		7		5	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to nonregistered Macrocell feedback	13		22		14		10	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered Macrocell feedback	13		22		14		10	ns
$t_{OEF'}$ t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to Macrocell feedback	13		14		7		5	ns
t_{IN} + t_{OUT} (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from Macrocell)	13		18		18		15	ns

*Commercial/Industrial Only

X5210

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC} (Note 6)	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs

Notes: 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-Macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a Macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.
5. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.
6. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset and Set inputs must not be asserted until all applicable input and feedback set-up times are met.
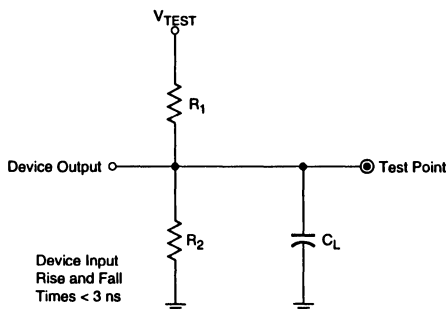
Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	310 Ω	195 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3489

Figure 5. AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

• Input Buffer and associated latch or register

• Logic Resource (UIM, AND-array and Macrocell)

• Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 6 defines the max clock frequency (with feedback). Any Macrocell output can be fed back to the UIM as an input for the next clock cycle. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the Macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the Macrocell and control paths.

Figure 12 defines the carry propagation delays between Macrocells and between Function Blocks. The parameters describe the delay from the CIN, D1 and D2 inputs of a Macrocell ALU to the CIN input of the adjacent Macrocell ALU. These delays must be added to the standard Macrocell delay path (t_{PD} or t_{SU})to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard Macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

Figure 6. Delay Path Specifications for f_{CYC} and f_{CYC1}

Figure 7. Delay Path Specification for f$_{CLK3}$

Figure 8. Delay Path Specification for t$_{SU1}$ and t$_{H1}$

Figure 9. Delay Path Specification for t_{SU} and t_H

Figure 10. Delay Path Specification for t_{SU2} and t_{H2}

Figure 11. Principal Pin-to-Pin Measurements

Figure 12. Arithmetic Timing Parameters

Figure 13. Incremental Timing Parameters

XC7236A Pinouts

PC44	Input	Output		PC44	Input	Output
1	Master Reset V_{PP}			23	V_{CCIO}	
2	Input	MC2-1		24	Input/FI	MC4-9
3	Input			25	Input/FI	MC4-8
4	Input			26	Input/FI	MC4-7
5	Input	MC2-4		27	Input	MC4-6
6	Input	MC2-5		28	Input	MC4-5
7	GND			29	GND	
8	Input	MC2-6		30	Input	MC4-4
9	FastCLK0	MC2-7		31	Input	MC4-3
10	FastCLK1	MC2-8		32	FastOE	MC4-2
11	FastCLK2	MC2-9		33	Input	MC4-1
12	V_{CCIO}			34	V_{CCINT}	
13	Input	MC1-1		35	Input/FI	MC3-9
14	Input	MC1-2		36	Input/FI	MC3-8
15	Input	MC1-3		37	Input/FI	MC3-7
16	Input	MC1-4		38	Input	MC3-6
17	GND			39	GND	
18	Input	MC1-5		40	Input	MC3-5
19	Input	MC1-6		41	Input	MC3-4
20	Input/FI	MC1-7		42	Input	MC3-3
21	Input/FI	MC1-8		43	Input	MC3-2
22	Input/FI	MC1-9		44	Input	MC3-1

FI = Fast Input

Ordering Information

XC7236A-16PC44C

Device Type ──┘

Speed ──────────┘

Temperature Range

Number of Pins

Package Type
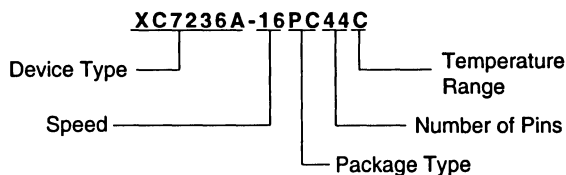
XC7236A	-25	25 ns (40 MHz) sequential cycle time
	-20	20 ns (50 MHz) sequential cycle time
	-16	16 ns (60 MHz) sequential cycle time (commercial and industrial only)

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C (Ambient) to 125°C (Case)

Package Options

PC44   44-Pin Plastic Leaded Chip Carrier
WC44   44-Pin Windowed Ceramic Leaded
Chip Carrier

Component Availability

Pins	44		68		84		
Type	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Ceramic PGA
Code	PC44	WC44	PC68	WC68	PC84	WC84	PG84
XC7236A -25	CI	CIM					
-20	CI	CIM					
-16	CI	CI					

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C
Parenthesis indicate future product plans

X5699

XILINX®

XC7272A
72-Macrocell CMOS EPLD

Product Specifications

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 72 Macrocells, grouped into eight Function Blocks, interconnected by a programmable Universal Interconnect Matrix
- Each Function Block contains a programmable AND-array with 21 complementary inputs, providing up to 16 product terms per Macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each Macrocell
  - Dedicated fast carry network between Macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all Macrocell logic paths
- 72 signal pins in the 84-pin packages
  - 42 I/Os, 12 inputs, 18 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O-pin is usable as input when Macrocell is buried
- Two high-speed, low-skew global clock inputs
- 68-pin and 84-pin leaded chip carrier packages and 84-pin Pin-Grid-Array packages

General Description

The XC7272A is a second-generation High Density Programmable Logic Device that combines the classical features of the PAL-like EPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output Macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each Macrocell. Dedicated fast arithmetic carry lines running directly between adjacent Macrocells and Function Blocks support fast adders, subtractors and comparators of any length up to 72 bits.

This additional ALU in each Macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent Macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and Macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Functional Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 72 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7272A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Automated design mapping and optimization is supported by Xilinx XEPLD development software based on design capture using third-party schematic entry tools, PLD compilers or direct text-based equation files. Design mapping is completed in a few minutes on a PC, or workstation.

Architectural Overview

Figure 1 shows the XC7272A structure. Eight Function Blocks (FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output Macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macrocells drive a 3-state chip output, all feed back into the UIM.
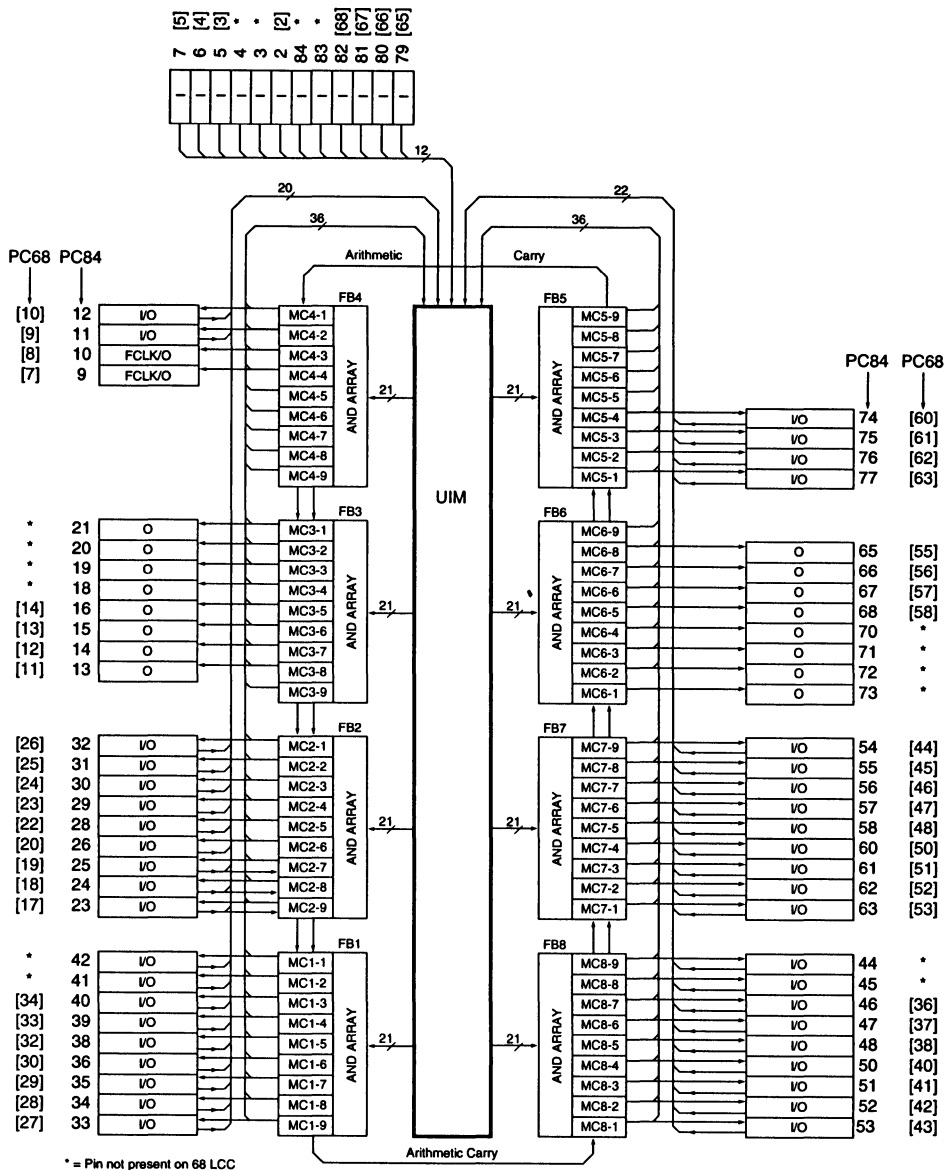
Figure 1. XC7272A Architecture

Function Blocks and Macrocells

The XC7272A contains 72 Macrocells with identical structure, grouped into eight Function Blocks of nine Macrocells each. Each Macrocell is driven by product terms derived from the 21 inputs from the UIM into the Function Block.

Five product terms are private to each Macrocell; an additional 12 product terms are shared among the nine Macrocells in any Function Block. One of the private product terms is a dedicated clock for the flip-flop in the Macrocell. See the description on page 3-24 for other clocking options.

The remaining four private product terms can be selectively ORed together with up to three of the shared product terms, and drive one input to an Arithmetic Logic Unit. The other input to the ALU is driven by the OR of up-to-nine product terms from the remaining shared product terms.

As a programmable option, two of the private product terms can be used for other purposes. One is the asynchronous active-High Reset of the Macrocell flip-flop, the other can be either an asynchronous active-High Set of the Macrocell flip-flop, or provide an active-High Output-Enable signal from any one of the Function Block inputs.

The Arithmetic Logic Unit has two programmable modes: In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to max 16 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the lower Macrocell; it also feeds a carry output to the next higher Macrocell. This carry propagation chain crosses the boundaries between Function Blocks, but it can also be configured 0 or 1 when it enters a Function Block.

This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture, when trying to perform arithmetic functions like add, subtract, and magnitude compare.
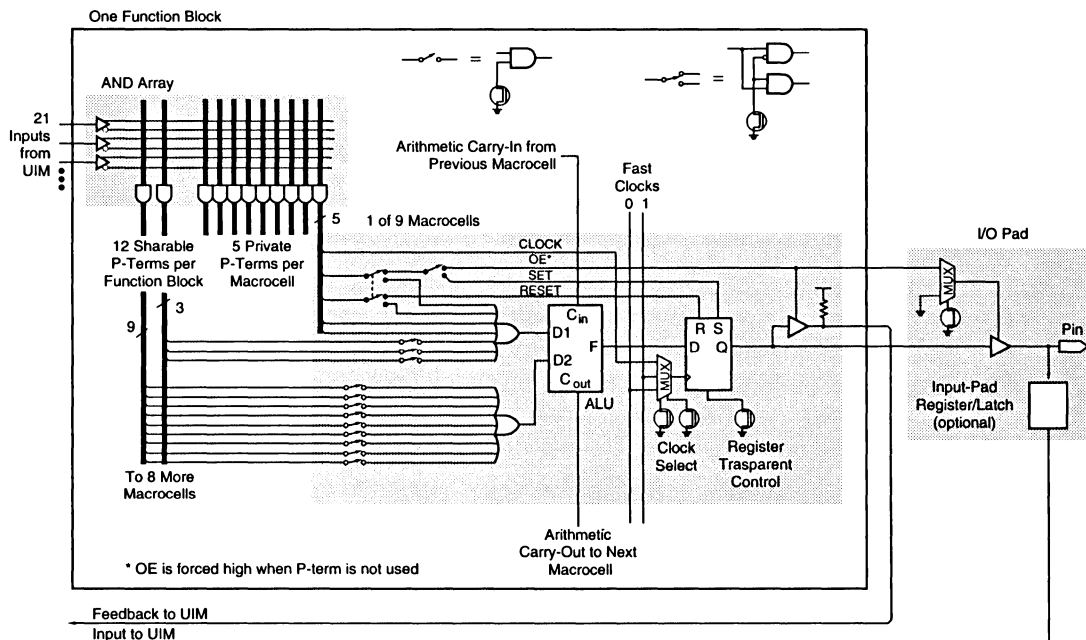
X5490

Figure 2. Function Block and Macrocell Schematic Diagram

The ALU output drives the D input of the Macrocell flip-flop.

Each flip-flop has several programmable options:

One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock.

If this option is *not* programmed, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable: It is either the dedicated product term mentioned above, or it is one of the two global FastCLK signals that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each Macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving the chip output buffer, the Macrocell output is also routed back as an input to the UIM. When the Output Enable product term mentioned above is not active, this feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 126 inputs: 72 from the 72 Macrocells, 42 from bidirectional I/O pins, and 12 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 168 output signals, 21 to each Function Block.

Any one of the 126 inputs can be programmed to be connected to any number of the 168 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity. Routability is not an issue: Any UIM input can drive any UIM output, even multiple outputs, and the delay is constant.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion in the Macrocell outputs and the Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function, thus offering an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such Macrocell outputs programmed onto the
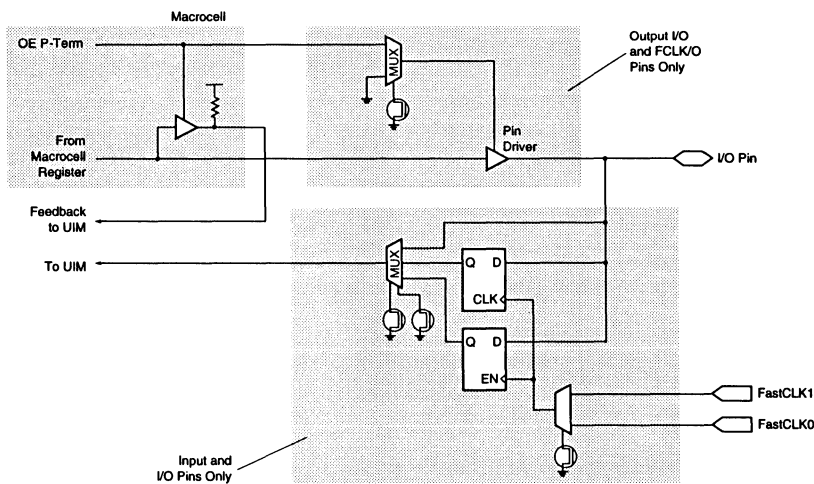
Figure 3. Input/Output Schematic

same UIM output thus emulating a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Sixty of the 72 Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. For bidirectional I/O pins, an additional programmable cell can optionally disable the output permanently. The buried flip-flop is then still available for internal feedback, and the pin can still be used as a separate input

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip-flop. Latch and flip-flop can be programmed with either of the two FastCLK signals as latch enable or clock. The latch is transparent when FastCLK is High, and the flip-flop clocks on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, in cases where a pipeline cycle is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

Programming and Using the XC7272A

The features and capabilities described above are used by the Xilinx XEPLD development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex or JEDEC format. Programming support is available from a number of programmer manufacturers. The UIM connections and Function Block AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires either a very fast V_{CC} rise time (<5 µs) or the application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. The latter can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macro-cell registers.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input-pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Figure 4. Typical I_{cc} vs Frequency for XC7272A Configured as Sixteen 4-bit Counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to 7.0	V
T_{STG}	Storage temperature	-65 to $+150$	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	$+260$	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial $T_A = 0°C$ to $70°C$	4.75	5.25	V
	Supply voltage relative to GND	Industrial $T_A = -40°C$ to $85°C$	4.5	5.5	V
	Supply voltage relative to GND	Military $T_C = -55°C$ to $125°C$	4.5	5.5	V
V_{IH}	High-level input voltage		2.0	V_{CC} +0.5	V
V_{IL}	Low-level input voltage		0	0.8	V

DC Characteristics Over Operating Conditions

		Min	Max	Units
V_{OH}	High-level output voltage @ $I_{OH} = -4$ mA , Vcc min	2.4		V
V_{OL}	Low-level output voltage @ $I_{OL} = 8$ mA , Vcc min		0.5	V
I_{CC}	Supply current $V_{IN} = 0$ V, V_{CC} = Max, f = 0 MHz	252 mA Typ		
I_{IL}	Input Leakage current	-10	$+10$	µA
I_{OZ}	Output High-Z leakage current	-100	$+100$	µA
C_{IN}	Input capacitance (sample tested)		10	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		*XC7272A-16		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK	6	40		50		60		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term clock	6	40		50		60		MHz
f_{CLK} (Note 5)	Max Macrocell register transmission frequency (without feedback) using FastCLK		59		60		60		MHz
f_{CLK1} (Note 5)	Max Macrocell register transmission frequency (without feedback) using a Product-Term clock		50		50		60		MHz
f_{CLK2} (Note 5)	Max input register transmission frequency (without feedback) using FastCLK		67		67		67		MHz
f_{CLK3} (Note 1)	Max input register to Macrocell register pipeline frequency using FastCLK	7	40		50		60		MHz
t_{WL}	FastCLK Low pulse width	11	7.5		7.5		6		ns
t_{WH}	FastCLK High pulse width	11	7.5		7.5		6		ns
t_{W1}	Product-Term clock pulse width (active/inactive)	11	10		9		7		ns
t_{SU}	Input to Macrocell register set-up time before FastCLK	9	24		19		15		ns
t_{H}	Input to Macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to Macrocell register set-up time before Product-Term clock	8	10		8		6		ns
t_{H1}	Input to Macrocell register hold time after Product-Term clock	8	0		0		0		ns
t_{SU2}	Input to register/latch set-up time before FastCLK	10	8		8		6		ns
t_{H2}	Input to register/latch set-up time after FastCLK	10	0		0		0		ns
t_{WA}	Set/Reset pulse width	11	12		10		8		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	20		20		16		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		-3		-3		ns
t_{RA1}	Set/Reset input recovery time before P-Term clock	11	6		5		4		ns
t_{HA1}	Set/Reset input hold time after P-Term clock	11	9		8		6		ns
t_{HRS}	Set/Reset input hold time after Reset/Set inactive		10		8		6		ns

*Commercial/Industrial Only

X5211

Propagation Delays

Symbol	Parameter	Fig.	XC7272A-25		XC7272A-20		*XC7272A-16		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to registered output delay	11	5	16	3	14	3	12	ns
t_{CO1}	P-Term clock input to registered output delay	11	10	30	6	25	6	21	ns
t_{AO}	Set/Reset input to registered output delay	11	13	40	8	32	8	25	ns
t_{PDD} (Note 1)	Input to nonregistered output delay	11	13	40	8	32	8	25	ns
t_{OE}	Input to output enable	11	11	32	7	25	7	22	ns
t_{OD}	Input to output disable		11	32	7	25	7	22	ns

*Commercial/Industrial Only   X5212

Notes 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

Incremental Parameters

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		*XC7236A-16		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent Macrocells	12		1.6		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent Macrocells in a Function Block	12		10		8		6	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 Macrocells from Macrocell #n to Macrocell #n in next F Block	12		14		12		10	ns
t_{COF}	Incremental delay from FastCLK net to registered output feedback	13		1		1		1	ns
t_{COF1}	Incremental delay from UIM-input (for P-Term clock) to registered Macrocell feedback	13		1.5		12		10	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to nonregistered Macrocell feedback	13		25		19		14	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered Macrocell feedback	13		25		19		14	ns
t_{OEF}, t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to Macrocell feedback	13		17		12		11	ns
t_{IN} + t_{OUT} (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from Macrocell)	13		15		13		11	ns

*Commercial/Industrial Only   X5213

Power-up/Reset Timing Parameters

Symbol	Description	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC}	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs

Notes 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent Macrocell(s) for an adder with registered outputs.

3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-Macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).

4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a Macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

5. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	450 Ω	245 Ω	35 pF

X3490

Figure 5. AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and Macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions
Figure 6 defines the max clock frequency (with feedback). Any Macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the Macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the Macrocell and control paths

Figure 12 defines the carry propagation delays between Macrocells and between Function Blocks. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a Macrocell ALU to the C_{IN} input of the adjacent Macrocell ALU. These delays must be added to the standard Macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard Macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

Figure 6. Delay Path Specifications for f_{CYC} and f_{CYC1}

Figure 7. Delay Path Specification for f$_{CLK3}$

Figure 8. Delay Path Specification for t$_{SU1}$ and t$_{H1}$

Figure 9. Delay Path Specification for t_{SU} and t_H

Figure 10. Delay Path Specification for t_{SU2} and t_{H2}

Figure 11. Principal Pin-to-Pin Measurements

Figure 12. Arithmetic Timing Parameters

Figure 13. Incremental Timing Parameters

XC7272A Pinouts

PC68	In	XC7272A out	PC84	PG84	PC68	In	XC7272A out	PC84	PG84
1	Master Reset		1	F-9	35	Vcc		43	F-3
2	Input		2	F-11	-	Input	MC8-9	44	G-3
-	Input		3	E-11	-	Input	MC8-8	45	G-1
-	Input		4	E-10	36	Input	MC8-7	46	G-2
3	Input		5	E-9	37	Input	MC8-6	47	F-1
4	Input		6	D-11	38	Input	MC8-5	48	H-1
5	Input		7	D-10	39	GROUND		49	H-2
6	GROUND		8	C-11	40	Input	MC8-4	50	J-1
7	Fast CLK0	MC4-4	9	B-11	41	Input	MC8-3	51	K-1
8	Fast CLK1	MC4-3	10	C-10	42	Input	MC8-2	52	J-2
9	Input	MC4-2	11	A-11	43	Input	MC8-1	53	L-1
10	Input	MC4-1	12	B-10	44	Input	MC7-9	54	K-2
11		MC3-8	13	B-9	45	Input	MC7-8	55	K-3
12		MC3-7	14	A-10	46	Input	MC7-7	56	L-2
13		MC3-6	15	A-9	47	Input	MC7-6	57	L-3
14		MC3-5	16	B-8	48	Input	MC7-5	58	K-4
15	GROUND		17	A-8	49	GROUND		59	L-4
-		MC3-4	18	B-6	50	Input	MC7-4	60	J-5
-		MC3-3	19	B-7	51	Input	MC7-3	61	K-5
-		MC3-2	20	A-7	52	Input	MC7-2	62	L-5
-		MC3-1	21	C-7	53	Input	MC7-1	63	K-6
16	Vcc		22	C-6	54	Vcc		64	J-6
17	Input	MC2-9	23	A-6	55		MC6-8	65	J-7
18	Input	MC2-8	24	A-5	56		MC6-7	66	L-7
19	Input	MC2-7	25	B-5	57		MC6-6	67	K-7
20	Input	MC2-6	26	C-5	58		MC6-5	68	L-6
21	GROUND		27	A-4	59	GROUND		69	L-8
22	Input	MC2-5	28	B-4	-		MC6-4	70	K-8
23	Input	MC2-4	29	A-3	-		MC6-3	71	L-9
24	Input	MC2-3	30	A-2	-		MC6-2	72	L-10
25	Input	MC2-2	31	B-3	-		MC6-1	73	K-9
26	Input	MC2-1	32	A-1	60	Input	MC5-4	74	L-11
27	Input	MC1-9	33	B-2	61	Input	MC5-3	75	K-10
28	Input	MC1-8	34	C-2	62	Input	MC5-2	76	J-10
29	Input	MC1-7	35	B-1	63	Input	MC5-1	77	K-11
30	Input	MC1-6	36	C-1	64	GROUND		78	J-11
31	GROUND		37	D-2	65	Input		79	H-10
32	Input	MC1-5	38	D-1	66	Input		80	H-11
33	Input	MC1-4	39	E-3	67	Input		81	F-10
34	Input	MC1-3	40	E-2	68	Input		82	G-10
-	Input	MC1-2	41	E-1	-	Input		83	G-11
-	Input	MC1-1	42	F-2	-	Input		84	G-9

Ordering Information

<div align="center">

XC7272A - 16 PC 84 C

Device Type ┘

Speed ──────

└─ Temperature Range

└─ Number of Pins

└─ Package Type   X3209

</div>
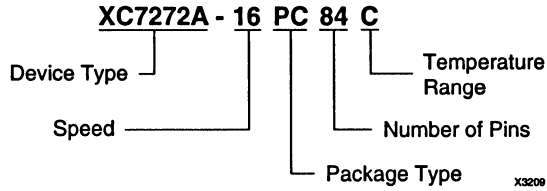
Speed Options

-25   25 ns (40 MHz) sequential cycle time
-20   20 ns (50 MHz) sequential cycle time
-16   16 ns (60 MHz) sequential cycle time
        (commerial and industrial only)

Package Options

PC68 68-Pin Plastic Leaded Chip Carrier
WC68 68-Pin Windowed Ceramic Leaded Chip Carrier
PC84 84-Pin Plastic Leaded Chip Carrier
WC84 84-Pin Windowed Ceramic Leaded Chip Carrier
PG84 84-Pin Ceramic Windowed Pin Grid Array

Temperature Options

C   Commercial   0°C to 70°C
I   Industrial   -40°C to 85°C
M Military   -55°C (Ambient) to 125°C (Case)

Component Availability

Pins	44		68		84		
Type	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Ceramic PGA
Code	PC44	WC44	PC68	WC68	PC84	WC84	PG84
-25			CI	CI	CI	CIM	CI
XC7272A -20			CI	CI	CI	CIM	CI
-16			CI	CI	CI	CI	CI

C = Commercial = 0° to +70°C   I = Industrial = -40° to 85°C
Parenthesis indicate future product plans

X5700

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3   XC7200A EPLD Family

4   Packages

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XILINX®

Pin 1 ID
(Either Pos.)

0.050 Typ
Non-Cumulative

Dimensions in Inches
Lead Pitch 50 Mil

Top View

Side View

X3038

44-Pin Plastic PLCC (PC44)

EPROM Window
0.350 Dia

Pin 1 ID
(Either Pos.)

Dimensions in Inches
Lead Pitch 50 Mil

Top View

Side View

X3039
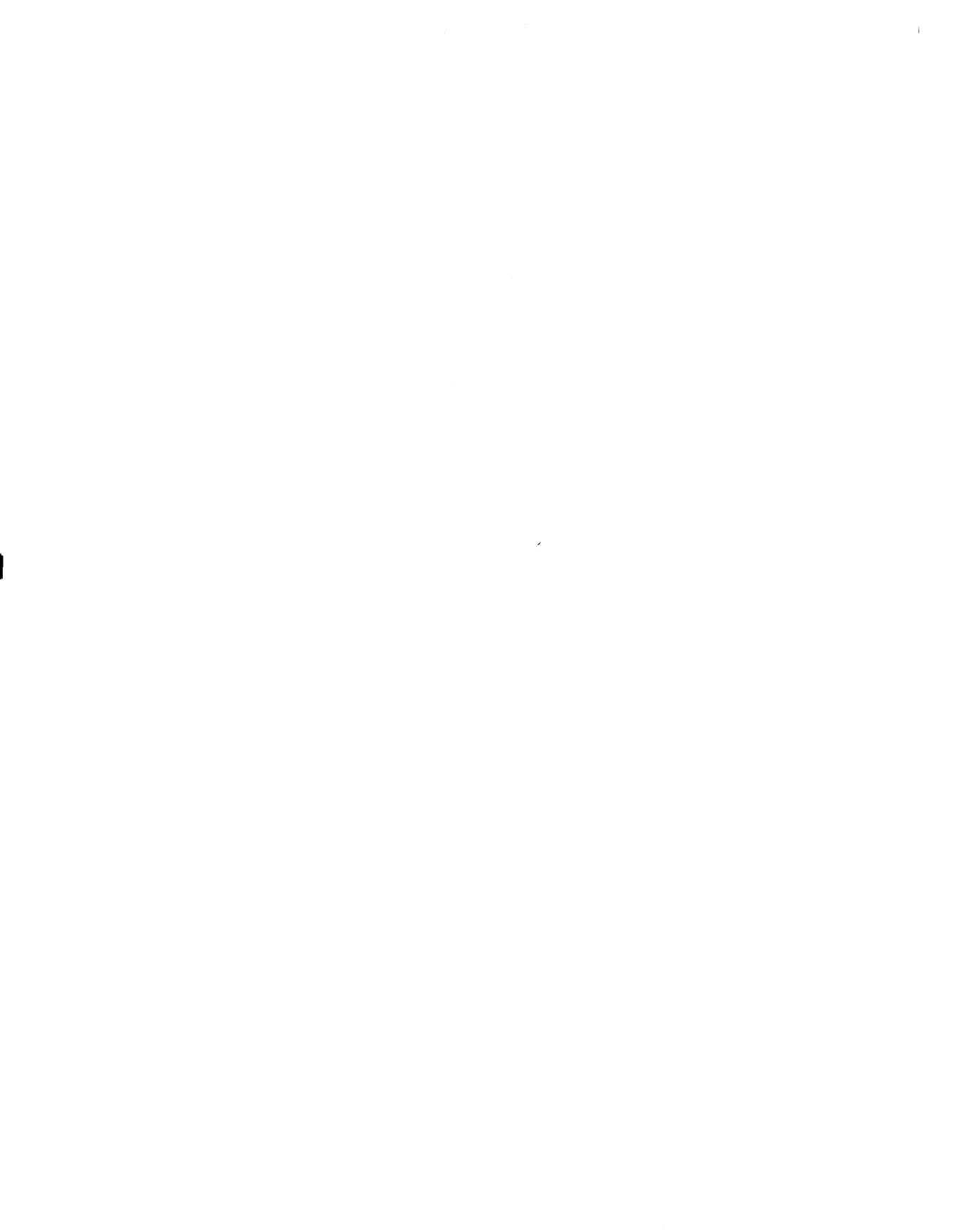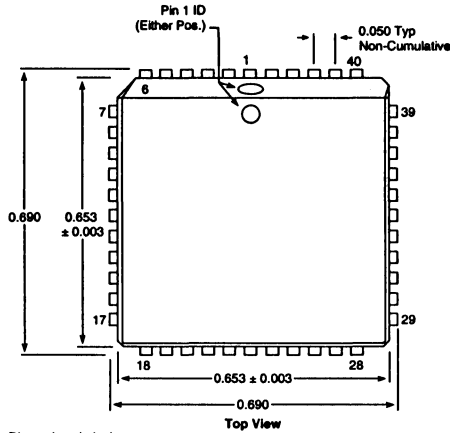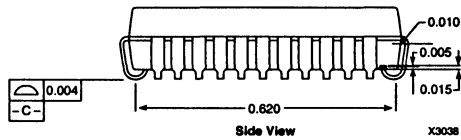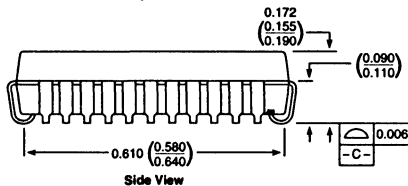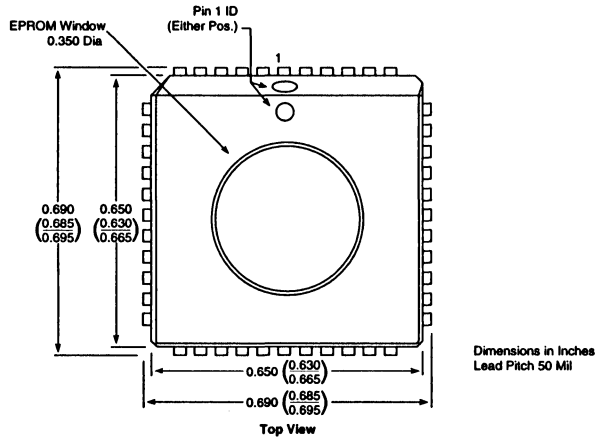
44-Pin Windowed Ceramic CLCC (WC44)

Pin 1 ID

44   35

1

0.35

11

12   22

34

23

13.2 Sq

10.0 Sq

Top View

Dimensions are in millimeters
Dimensions in parenthesis are in inches
Lead Pitch 0.80 mm

12°-16°
8 places

2.00

0.076

-C-

Stand-Off
0.15

Side View

X5616

44-Pin PQFP (PQ44)

0.045 x 45°

9   1   61

Pin 1 ID

0.990
± 0.005

0.954
± 0.004

27   43

0.954 ± 0.004

0.990 ± 0.005

Top View

0.170
± 0.0050

0.028

0.045

0.004

-C-

0.099

0.045

0.018

0.045

0.045

0.020

0.800

0.920 ± 0.010

Dimensions in Inches
Lead Pitch 50 Mil

Side View

X3042

68-Pin Plastic PLCC (PC68)
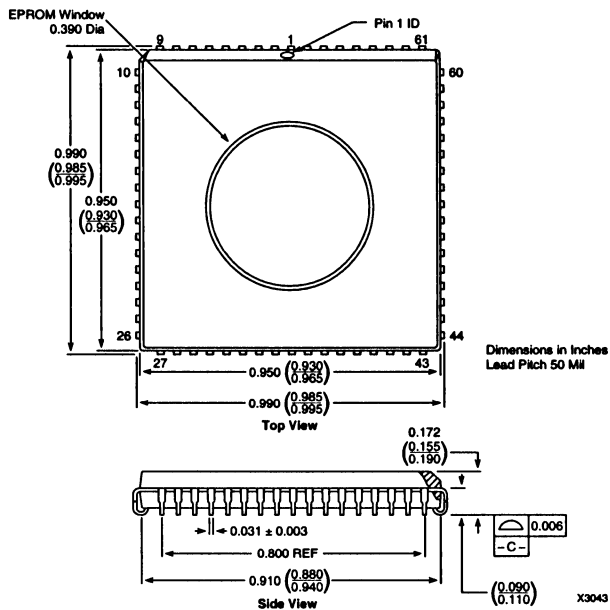
68-Pin Windowed CLCC (WC68)
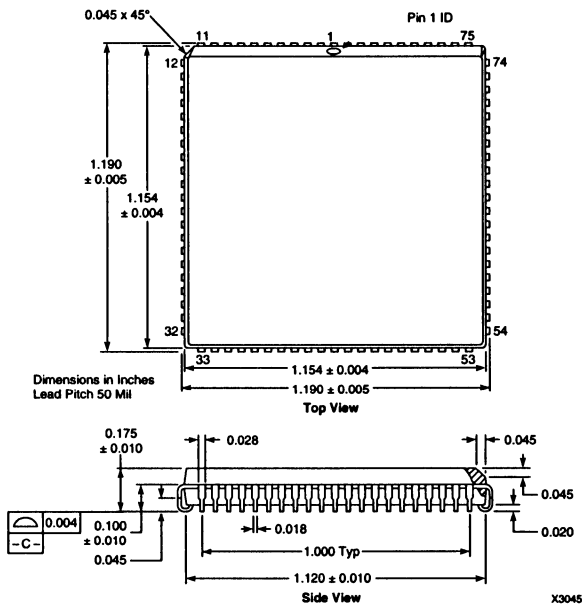
84-Pin Plastic PLCC (PC84)
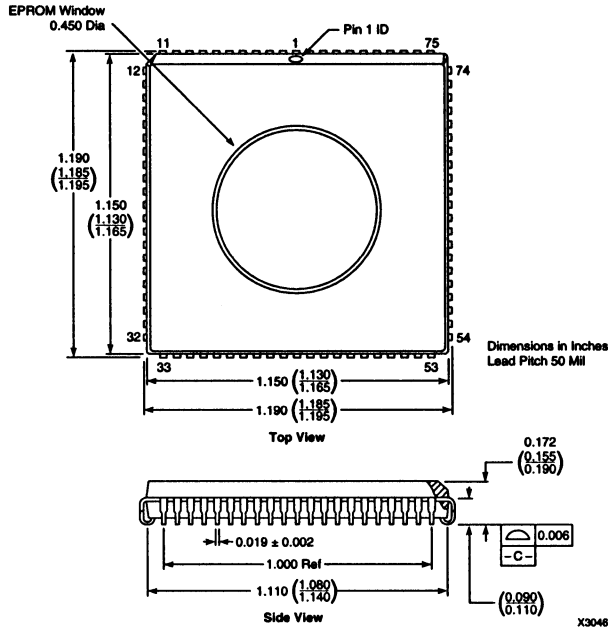
EPROM Window
0.450 Dia

Pin 1 ID

Dimensions in Inches
Lead Pitch 50 Mil

Top View

Side View

X3046

84-Pin Windowed CLCC (WC84)

Bottom View

Side View

Top View

Pin 1 ID

NOTE: Index Pin May or May Not Be
Electrically Connected to Pin C2

Dimensions in Inches   X3047

84-Pin Ceramic PGA (PG84)

Top View

Dimensions in Millimeters
Lead Pitch 0.65 mm

Side View

Stand-Off
0.13-0.23

X5617

100-Pin Plastic PQFP (PQ100)

Bottom View

Top View

Dimensions in Inches

Side View
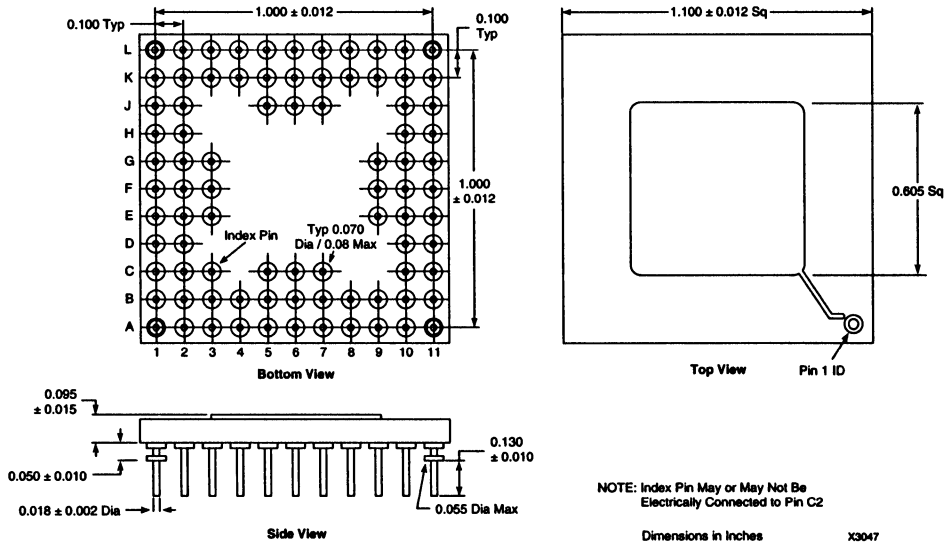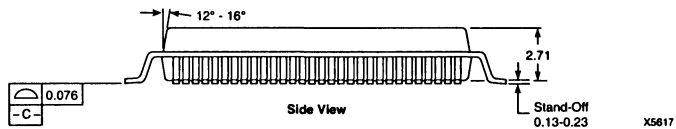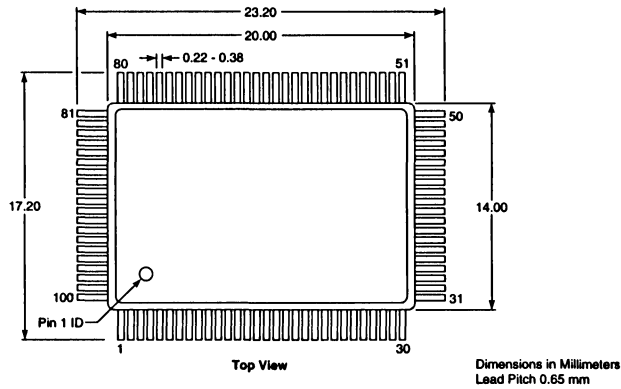
X3160

144-Pin Ceramic PGA (PG144)

4-5

1.228 ± 0.010 Sq
1.102 ± 0.004 Sq
0.998 Ref
120   81
121   80
160   41
1   40
Pin 1 ID
Top View
Dimensions in Inches
Lead Pitch 0.0256

0.004
-C-
0.144 ± 0.008
0.031 + 0.006 - 0.005
0.063 Ref
0.011 ± 0.002
5 - 7°
0.005 - 0.008
0.064 Ref
0.133 ± 0.008
Side View
X3054

160-Pin Plastic PQFP (PQ160)

27.00 ± 0.20 Sq
24.70 Max
45° Chamfer (4 Places)
Pin #1 ID
PC Board
Molded Body
1.00 Dia Ref
Top View

15° Typ All Sides
0.60 ± 0.10
0.15C
-C-
3.00 Ref   1.50 Typ
2.15 ± 0.015
Side View

0.9
0.6
R P N M L K J H G F E D C B A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Bottom View
PbSn Solder Balls
225 (15 x 15 Array)

Dimensions in Millimeters

X5215

225-Pin Plastic BGA (BG225)

4-6

Call Factory for 225-Pin Windowed Ball Grid Array Dimensions

Top View   Bottom View

X5701
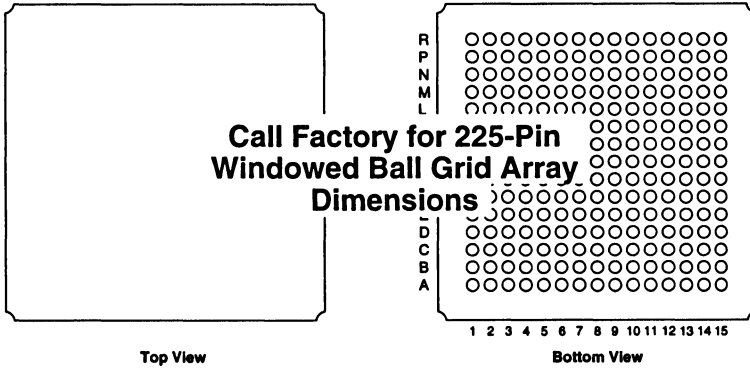
225-Pin Windowed BGA (WB225)

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XEPLD 5.1 Xilinx EPLD Development System

XEPLD 5.1 is the design implementation software for Xilinx EPLDs, providing a complete low-cost, user-friendly design environment for processing behavioral, schematic, and VHDL/HDL designs on PC, Sun-4, HP700, and RS6000 platforms.

XEPLD 5.1 Key Features

VHDL/ HDL support
* Use Synopsys, Exemplar Logic and ViewSynthesis to synthesize designs for Xilinx XC7000 EPLDs

Automatic Optimization, Minimization, Partitioning and Mapping
* Designs are automatically optimized, partitioned and mapped into the device for optimal efficiency and design performance

Complete control of all device resources
* Advanced users can easily fine-tune every aspect of their design with full control of the XEPLD fitter optimizations

Dual-Block™ architecture support for high speed and high density
* Users can easily flag critical paths for automatic partitioning of high speed logic into Fast Function Blocks and dense logic into High Density Function Blocks

SMARTswitch™
* Automatic use of the Universal Interconnect Matrix (UIM™) logic capability results in higher density and increased speed

Preserves Pinouts During Design Changes
* Automatic use of the Universal Interconnect Matrix 100% routing capability eliminates delays and costly printed circuit board rework

Static Timing Report
* Provides a complete pin-to-pin timing report of the design

Schematic Design Entry

XEPLD provides an open environment allowing designers to choose from a variety of schematic entry and simulation tools such as those from OrCAD, ViewLogic, Mentor Graphics, and Cadence Design Systems.

* Comprehensive unified component library allows you to use Xilinx EPLDs and FPGAs.
* Functional and timing verification with simulators such as Viewlogic ViewSim, OrCAD VST, Mentor QuickSim and Cadence Verilog and RapidSim.
* Board level simulation using EPLD models available from Logic Modeling Corporation.

Behavioral Design Entry

XEPLD operates as a complete stand-alone fitter or as an embedded fitter within PLD compilers such as ABEL, Xilinx ABEL, CUPL, and PALASM.

* Take advantage of the PLD compiler's high-level design entry methods such as state machines, truth tables and Boolean equations for implementing complex designs in a familiar HDL format
* Operates entirely within the PLD compiler environment when used as an embedded fitter
* Automatically processes Boolean equation test files and PLD compiler output files when used as stand-alone fitter
* PAL conversion utility automatically consolidates multiple PAL files into a single Xilinx XC7000 EPLD

Fully Automatic Features

More Logic With SMARTswitch
The SMARTswitch feature of XEPLD increases the effective logic capacity of the device by exploiting the AND-gate logic inherent in the Universal Interconnect Matrix (UIM) interconnect structure of Xilinx EPLDs.

The UIM provides 100% routing for all designs. It is composed of an AND array that is used not only for interconnecting macrocells but also for implementing additional levels of logic, with no additional delay.

SMARTswitch automatically analyzes your design, looking for DeMorgan equivalent functions that can be implemented in the UIM. Very wide zero-delay AND, OR, NAND and NOR gates can be created. Other functions such as terminal count signals for long counters and intermediate

expressions for complex state machines are also implemented in the UIM automatically. SMARTswitch provides a significant improvement in design performance without user intervention and the results are fully reported.

PAL Conversion

PAL designs such as those targeted for the 22V10 or 16V8 can be automatically converted for use in Xilinx EPLDs. XEPLD reads and combines the PAL files, optimizes the equations, identifies the I/O requirements and fits the resulting design into any target device. With XEPLD it is easy to combine multiple PAL designs into high density EPLDs to save power, space, and money.

- Redesign is not required.
- 100% routing via the UIM which guarantees that converted PAL designs will interconnect as they appear in the original design.
- Fast Function Blocks are used as high-speed PAL targets. With 5 ns pin-to-pin delay, they operate at up to 167 clock frequency.
- High Density Function Blocks are used as complex PAL targets. With up to 17 product terms per output, they operate at 95 MHz, including the interconnect.
- 100% routing via the UIM guarantees that converted PAL designs will interconnect as they appear in the original design.
- XEPLD converts, optimizes, and maps PALs into an EPLD, typically in less than 5 minutes on a PC.

XEPLD Stand-alone Design Environment

There are three steps involved in designing Xilinx EPLDs: 1) design entry, 2) implementation, and 3) verification.

1) Using familiar front-end tools, enter designs using behavioral equations, VHDL/HDL or schematics. Mixed-mode entry is also supported allowing one to embedded behavioral blocks such as state machines and PAL descriptions in schematics

2) XEPLD implements the design in the chosen XC7000 EPLD, automatically optimizing, partitioning and mapping the design for greatest efficiency and highest performance

3) Verify the design by reviewing fitter reports such as the Static Timing Report. The implemented design can also be simulated using a variety of third party timing simulators.

Embedded Third-Party Compiler Environments

Xilinx licenses its fitter technology to third-party development tool vendors, giving you the flexibility and versatility of industry standard design software environments with the speed, density, and routability of Xilinx EPLDs.

The Xilinx XEPLD fitter is fully integrated into the ABEL and CUPL design environments to ensure ease-of-use and to provide the most efficient optimization and fitting. For price and delivery information on these embedded third-party fitters, contact the development tool manufacturer.

XEPLD Provides Efficient EPLD Design Solutions

New users can quickly produce high performance, efficient designs with little effort because XEPLD 5.1 is easy to learn, easy to use, and provides a full range of automatic features. A detailed understanding of the Xilinx EPLD architecture is not required, however advanced users can override any of the automatic features and fine-tune every aspect of the design. XEPLD 5.1 is a total stand-alone solution for creating Xilinx EPLD designs. Now priced at only $89.95 for the PC version, the benefits of this comprehensive development environment are available to every designer.

Ordering Information

	Part Number	PC	Sun	HP700	IBM RS6000
Tools:					
XEPLD	DS-550 *	-PC1	-SN2	-HP7	2H94
Xilinx Abel	DS-371	-PC1	-SN2	-	-
Interfaces:					
Viewlogic	DS-290/390	-PC1	-SN2	-HP7	-
OrCAD	DS-35	-PC1	-	-	-
Mentor	DS-344	-	-SN2	-HP7	-
Synopsys	DS-401	-	-SN2	-HP7	-
Cadence	-	Supported directly by Cadence			

* The DS-550 is also available in the Base, Standard and Extended software packages.

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Using ABEL and the DS-550

ABEL can be used to generate design files that can be processed by the DS-550. An automatic translation program, PLA2EQNX, translates the ABEL-generated .TT2 file into an equation file that can be read by the DS-550.

PLA2EQNX is included in the DS-550 v5.1. It can also be downloaded, in compressed format, from the SWHELP area of the Xilinx BBS. The filenames are ABEL2XP.ZIP (for PCs) and ABEL2XS.ZIP (for workstations). Unzip the file and place the executable in your \xact directory.

ABEL

The ABEL source code should be device-independent. Instead of targeting a specific device in the ABEL device statement, use the device-independent format shown below:

design_name device;

Note: Only single product term expressions are allowed for asynchronous register set, reset, output enable and clocks in ABEL code for XC7000 devices. Also, signals assigned to the XC7000 global FASTCLOCK and FOE nets can't be used in logic equations. The DS-550 generates PLUSASM syntax errors if these design rules are violated.

Then compile and optimize the design as follows:

1. COMPILE -> COMPILE on the source code, design.ABL generates design.TT1
2. OPTIMIZE -> OPTIONS -> Reduce by Pin, Autopolarity selects the most efficient optimization options for the Xilinx XC7000 devices.
3. OPTIMIZE -> REDUCE performs boolean minimization of your logic in the design.TT1 file and generates the design.TT2 file

PLA2EQNX

PLA2EQNX translates the design.TT2 file to a PLUS-ASM top-level equation file, design.PLD. This file can be processed by the DS-550 without any modifications. From the command line type:

pla2eqnx design.tt2 -lan plus -str top_level

XDM

Invoke XDM and select either the XC7200 or XC7300 family, and your target device and speed grade. Then use the FITTER -> FITEQN command to compile the design.PLD file.

Translation Options

ABEL can also be used to generate equation files that can be linked to a symbol in a schematic design. If the ABEL code is for a standard 20 or 24 pin PAL, there is no need to change the device statement in the original ABEL source code. Just compile and optimize the design for that PAL type to generate the .TT2 file. From the command line type:

pla2eqnx design.tt2 -lan plus

Then follow the instructions in the Using PLD Files in Schematics chapter of the XEPLD Design Guide to link the design.PLD equation file to the symbol and process the design.

If the ABEL code is a behavioral module not already implemented in a low density PAL, write the design in device independent format, then compile and optimize the design. From the command line type:

pla2eqnx design.tt2 -lan plus

Then follow the instructions in the XEPLD Schematic Design Guide to create a custom symbol for the behavioral module.

CUPL Total Designer v4.5 contains a fitter that can be used to target Xilinx XC7000 devices from within the CUPL design environment. Other versions of CUPL can be used to generate design files that can be processed by the DS-550, as illustrated in this document. These design files may require an extra step with a text editor because CUPL generates files with extra, but truncated, SETF and RSTF equations.

CUPL

Use CUPL to translate equation files for 20 and 24-pin PALs into a PLUSASM-compatible equation file for processing by the DS-550.

Type the following at the command line to create the design.PDS file:

cupl -c design.pld

After editing, the design.PDS file is ready to be processed by the DS-550's PALCONVT utility.

CUPL source code for a device-independent design can also be written, then translated to PLUSASM format. To write device-independent CUPL code, use the VIRTUAL device in the CUPL device statement as shown below:

Device virtual;

Note 1: Only single product term equations are allowed for asynchronous register set, reset, output enable and clocks in CUPL code for XC7000 devices. Also, signals assigned to the XC7000 global FASTCLOCK and FOE nets can't be used in logic equations. The DS-550 generates PLUSASM syntax errors if these design rules are violated.

Note 2: When compiling the design, CUPL will issue a warning message that VIRTUAL is an unrecognized device type and then substitute USER for the device type in the design.PDS file's chip statement.

Text Editor

Use a text editor to remove extra signal_name.SETF and signal_name.RSTF equations from the CUPL generated equation file. These equations will be easy to spot because there will be no logical expressions to the right of the "=" sign.

Figure 1. Truncated SETF/RSTF Equations

```
a        = b
a.setf   =
a.setf   =
a.rstf   =
a.rstf   =
```

XDM

Invoke PALCONVT following the instructions in the XACT 5.0 XEPLD Design Guide. Be sure to use the CREATE NEW PLD AND PAL INTERCONNECT REPORT option and review the Top-Level file before running FITEQN on it.

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Using PALASM4 and the DS-550

PALASM4 can be used to generate design files that can be processed by the DS-550. The flow for PALASM4 requires an extra step using a text editor because PALASM4 generates files with a pinlist that is PLUSASM incompatible.

PALASM4

1. RUN -> COMPILATION on the source code, design.PDS
2. RUN -> OTHER OPERATIONS -> DISASSEMBLE FROM -> INTERMEDIATE FILE creates design.PL2. This file contains PLUSASM-compatible equations, and a pinlist that is not PLUSASM compatible.

Note: Extended memory versions of PALASM4 v1.5 executables may be needed to remove nested parenthesis from the PL2 file.

Text Editor

Use a text editor to remove pin numbers and signal types from the pinlist. All that should remain between the chip statement and the equations keyword is a list of all signals in the design. Change the extension of the design.PL2 file to

.PLD so the file will show up in the list of design files to be operated on by PALCONVT.

Unlike some other PAL compilers, PALASM4 does not insert NC's to represent unused pin positions. XEPLD recognizes the implied functionality of 22V10s and 20V8s. If the equation file came from these 24-pin PALs, the GND and V_{CC} pins must appear in the correct location in the pinlist. Insert NCs in the pinlist so that GND and V_{CC} appear in pin positions 12 and 24, respectively.

This can also be an issue for other PAL types when doing schematic-based designs and using the same pinout for the PAL component in the schematic as in the original design. Pin numbers are matched with signal names in a PLD file according to their relative order in the pinlist.

XDM

Invoke PALCONVT following the instructions in the XACT 5.0 XEPLD Design Guide. Be sure to use the CREATE NEW PLD AND PAL INTERCONNECT REPORT option so you can review the Top-Level file before you run FITEQN on it.

PL2 File Pinlist Generated by PALASM4
```
TITLE    TUTOR9.PDS
PATTERN   A
REVISION  2.0
AUTHOR    J.ENGINEER
COMPANY  ADVANCED MICRO DEVICES
DATE     01/01/90
CHIP  ANSWER  PAL22V10
PIN 1 CLOCK COMB
PIN 2 DIALTONE COMB
PIN 3 RING COMB
PIN 4 ENDGREETING COMB
PIN 5 ENDMESSAGE COMB
PIN 12 GND
PIN 17 ANSWER REG
PIN 18 PLAY REG
PIN 19 RECORD REG
PIN 23 /_ST0
PIN 24 VCC

EQUATIONS
```

EDITED PINLIST
```
TITLE    TUTOR9.PDS
PATTERN   A
REVISION  2.0
AUTHOR    J.ENGINEER
COMPANY ADVANCED MICRO DEVICES
DATE     01/01/90
CHIP  ANSWER  PAL22V10
CLOCK
DIALTONE
RING
ENDGREETING
ENDMESSAGE
NC NC NC NC NC NC
GND
NC NC NC NC
ANSWER
PLAY
RECORD
NC NC NC
/_ST0
VCC
EQUATIONS
```

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Xilinx HW-130 Programmer

The Xilinx HW-130 Programmer is an easy-to-use, desktop unit for quick programming of all Xilinx nonvolatile devices. The HW-130 has its own interface software which enables the user to select a device and download its algorithm to the programmer, ensure that the device is blank, program the device, and verify that the device has been programmed correctly. the software also includes on-line help.

Programs all Xilinx Nonvolatile Devices
- XC1700 Serial PROMs
- XC7000 EPLDs
- XC8100 FPGAs
- Supports all packages

System Requirements
- Any IBM PC compatible (Requires 512kB RAM)
- MS-DOS version 3.3 or higher
- 3.5" Floppy disk drive
- Hard disk drive (Requires 1 Mbytes hard disk space)
- RS-232 serial port
- Mouse (recommended)

Programmer Accessories
- Interface software
- Domestic/International power supply with cord and adapter
- Serial cable with DB9 connector
- User manual

Programmer Functional Specifications
- Device programming and verification
- Security control
- PROM Reset Polarity Control
- Checksum calculation and comparison
- Blank check and signature ID tests
- File transfer and comparison
- Master device program upload
- Self check and auto calibration

Programmer Electrical Requirements and Physical Specifications
- Operating voltage: 100 - 250 V AC, 50 - 60 Hz
- Power consumption: 0.3 A
- Dimensions: 6" X 7.75" X 2"
- Weight: 1 lb.
- Safety standards: Approved by UL, CSA, TUV

Socket Adapters
All package styles are supported including PLCC, PQFP, BGA, SOIC, PGA, and DIP.

Adapter Part Number	Product Family	Package Type
HW-132-PC44	XC7200A	PLCC/CLCC 44
HW-132-PC68	XC7200A	PLCC/CLCC 68
HW-132-PC84	XC7200A	PLCC/CLCC 84
HW-132-PG84	XC7200A	PGA 84
HW-133-PC44	XC7300	PLCC/CLCC 44
HW-133-PQ44	XC7300	PQFP 44
HW-133-PC68	XC7300	PLCC/CLCC 68
HW-133-PC84	XC7300	PLCC/CLCC 84
HW-133-PQ100	XC7300	PQFP 100
HW-133-PG144	XC7300	PGA 144
HW-133-PQ160	XC7300	PQFP 160
HW-133-BG225	XC7300	BGA 225
HW-137-PD8	XC1700	DIP 8
HW-137-PC20	XC1700	DIP 20
HW-138-PC84	XC8000	PLCC 84

Programming Algorithm Updates
The latest programming algorithms are available 24 hours a day via the Xilinx BBS (408-559-9327).

	XC7236	XC7236A	XC7272	XC7272A	XC7318	XC7336	XC7354	XC7372	XC73108	XC73144
Advin Systems, Inc. 1050-L East Duane Ave Sunnyvale, CA 94086 (408) 243-7000	Pilot-U40 Pilot-U84 v10.77E	Pilot-U40 Pilot-U84 v10.77E	Pilot-U40 Pilot-U84 v10.77E	Pilot-U40 Pilot-U84 v10.77E	Pilot-U84 v10.78B	Pilot-U84 v10.78B	Pilot-U84 v10.78B	Pilot-U84 v10.78B	Pilot-U84 v10.79	Contact Manu-facturer
BP Microsystems 1000 N. Post Oak Road Suite 225 Houston, TX 77065-7237 (800) 225-2102	BP-1200 v2.32	BP-1200 v2.32	BP-1200 v2.34	BP-1200 v2.34	BP-1200 v3.01	BP-1200 v3.01	BP-1200 v3.01 (44-pin pkg only)	Contact Manu-facturer	BP-1200 v3.06A	Contact Manu-facturer
B&C Microsystems 750 North Pastoria Ave Sunnyvale, CA 94086 (408) 730-5511	Proteus v3.6j	Proteus v3.6j	Proteus v3.7h	Proteus v3.7h	Proteus v3.7k	Proteus v3.7k	Proteus v3.7k	Contact Manu-facturer	Proteus v3.6j	Contact Manu-facturer
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (206) 881-6444	Unisite v4.3	Unisite v4.6	Unisite v4.5	Unisite v4.5	Unisite v4.7	Unisite v4.7	Unisite v4.7	Contact Manu-facturer	Contact Manu-facturer	Contact Manu-facturer
	2900 v3.4	2900 v3.4			2900 v3.5	2900 v3.5	2900 v3.5			
	3900 v2.1	3900 v2.4	3900 v2.3	3900 v2.3	3900 v2.5	3900 v2.5	3900 v2.5			
	Autosite v2.4	Autosite v2.4	Autosite v2.3	Autosite v2.3	Autosite v2.5	Autosite v2.5	Autosite v2.5			
Deus Ex Machine Engineering 1390 Carling Drive Suite 108 St. Paul, MN 55108 (612) 645-8088	XPGM v1.00	XPGM v1.00	XPGM v1.00	XPGM v1.00	XPGM v1.00	XPGM v1.00	XPGM v1.00	XPGM v1.10	XPGM v1.10	Contact Manu-facturer
Elan Digital System Ltd. Elan House Little Park Farm Road Segenworth West Fareham, Hampshire United Kingdom PO15 5SJ 44-489-579799	6000 APS K2.04	6000 APS K2.04	6000 APS K2.06	6000 APS K2.06	6000 APS K2.13	6000 APS K2.13	6000 APS K2.13	6000 APS K2.13	6000 APS K2.13	Contact Manu-facturer
HI-LO Systems Research 4F, No2, Sec5 Ming Shen E. Road Taipei, Taiwan ROC 886-2-7640215	All-03A v3.01	All-03A v3.01	All-03A v3.00	All-03A v3.00	All-03A v3.04	All-03A v3.04	All-03A v3.04		All-03A v3.00	Contact Manu-facturer
	All-07 v3.01	All-07 v3.01	All-07 v3.00	All-07 v3.00	All-07 v3.02	All-07 v3.02	All-07 v3.02	All-07 v3.01	All-07 v3.00	
ICE Technology Ltd. Unit 4 Penistone Court Station Buildings South Yorkshire United Kingdom S30 6HG 44-226-767404	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Micromaster 1000/E vX1.00	Contact Manu-facturer
	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	Speedmaster 1000/E vX1.00	
	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	Micromaster LV vX1.00	
	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	Speedmaster LV vX1.00	

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Third Party Programmer Support For Xilinx EPLDs

	XC7236	XC7236A	XC7272	XC7272A	XC7318	XC7336	XC7354	XC7372	XC73108	XC73144
Logical Devices 264 Southwest 12th Ave Deerfield Beach, FL 33442	ALLPRO-88 v2.2 / ALLPRO-88XR v1.35 / XPRO-1 v1.01	XPRO-1 v1.01	ALLPRO-88 v2.2 / ALLPRO-88XR v1.35 / XPRO-1 v1.01	XPRO-1 v1.01	XPRO-1 v1.01	XPRO-1 v1.01	XPRO-1 v1.01	XPRO-1 v1.01	XPRO-1 v1.01	Contact Manufacturer
MQP Eelectronicsn Ltd. Unit 2 Park Road Centre Malmesbury, Wilts United Kingdom SN16 OBX 44-666-825146	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer
SMS GmbH Im Grund 15 D-88239 Wangen, Germany 49-7522-97280 SMS North America (206) 883-8447	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer
Stag Programmers Ltd. Silver Court Watchmead Welwyn Garden City Herts United Kingdom A17 1LT 44-707-332148 Stag Microsystems 1600 Wyatt Drive Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer	Eclipse v4.10.31	Eclipse v4.10.31	Eclipse v4.10.31	Eclipse v4.10.31	Eclipse v4.10.31	Contact Manufacturer
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667	TURPRO-1 v2.12 / TURPRO-1 FX v2.12	TURPRO-1 v2.12 / TURPRO-1 FX v2.12	TURPRO-1 v2.12 / TURPRO-1 FX v2.12	TURPRO-1 v2.12 / TURPRO-1 FX v2.12	TURPRO-1 v2.2	TURPRO-1 v2.2	TURPRO-1 v2.2	TURPRO-1 v2.2	TURPRO-1 v2.2	Contact Manufacturer
Tribal Microsystems 44388 S. Grimmer Blvd. Fremont, CA 95438 (510) 623-8859	TUP-300 v3.0 / TUP-400 v3.0 / FLEX-700 v3.0	TUP-300 v3.0 / TUP-400 v3.0 / FLEX-700 v3.0	TUP-300 v3.0 / TUP-400 v3.0 / FLEX-700 v3.0	TUP-300 v3.0 / TUP-400 v3.0 / FLEX-700 v3.0	All-07 v3.02	All-07 v3.02	All-07 v3.02	All-07 v3.01	All-07 v3.00	Contact Manufacturer
Xeltek 757 North Pastoria Avenue Sunnyvale, CA 94086 (408) 524-1934	SUPERPRO v1.17C / SUPERPRO II v1.17C	SUPERPRO v2.2 / SUPERPRO II v2.2	SUPERPRO v2.1 / SUPERPRO II v2.1	SUPERPRO v2.1 / SUPERPRO II v2.1	SUPERPRO v2.1 / SUPERPRO II v2.1	SUPERPRO v2.1 / SUPERPRO II v2.1	SUPERPRO v2.1 / SUPERPRO II v2.1	Contact Manufacturer	Contact Manufacturer	Contact Manufacturer

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∑ XILINX®   Xilinx Quality Assurance

Quality Assurance Program

Quality Assurance encompasses all aspects of company business. Xilinx continually strives to improve quality to meet customer's changing needs and expectations. To do this, the company is dedicated to the following.

- To provide a broad range of products and services that satisfy both the expectations of customers and the company's stringent quality standards.

- To emphasize open communication with customers and suppliers, supported with the necessary statistical data.

- To continually improve the quality of Xilinx products, services, and company efficiency

- To maintain a work environment that fosters quality and reliability leadership and excellence.

From its inception, Xilinx has been committed to delivering the highest quality, most reliable programmable logic available. A strong Quality Assurance and Reliability program begins at the initial design stages and is carried through to final shipment. An extensive, on-going reliability-testing program is used to predict the field performance of all Xilinx devices.

These tests provide an accelerated method of emulating long-term system operation in severe field environments. From the performance of the devices during these tests, predictions of actual field performance under a variety of conditions can be easily calculated.

Xilinx is committed to customer satisfaction. By adhering to the highest quality standards, the company has achieved leadership in the EPLD and FPGA manufacturing areas.

Quarterly reports describing the nature and purpose of the various reliability tests performed on finished devices are available. Please contact the Quality Assurance and Reliability Department at Xilinx.
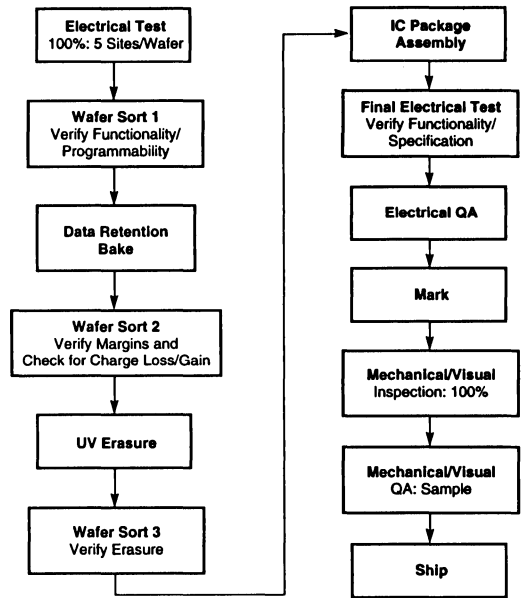
X5760

Wafer-Sort, Assembly and Final Test Flow for Xilinx EPLD Devices

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FAX: 818-865-6223

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Tustin, CA 92680
(714) 731-9206
FAX: 714-731-7801

Quest-Rep Inc.
6494 Weathers Pl, Suite 200
San Diego, CA 92121
(619) 622-5040
FAX: 619-622-5047

Norcomp
1267 Oakmead Pkwy
Sunnyvale, CA 94086
(408) 733-7707
FAX: 408-774-1947

Norcomp
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Granite Bay, CA 95746
(916) 791-7776
FAX: 916-791-2223

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FAX: 203-265-0235

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FAX: 407-831-2844

Semtronic Assoc., Inc.
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Ft. Lauderdale, FL 33309
(305) 731-2484
FAX: 305-731-1019

Semtronic Assoc., Inc.
1467 South Missouri Avenue
Clearwater, FL 34616
(813) 461-4675
FAX: 813-442-2234

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FAX: 404-734-9977

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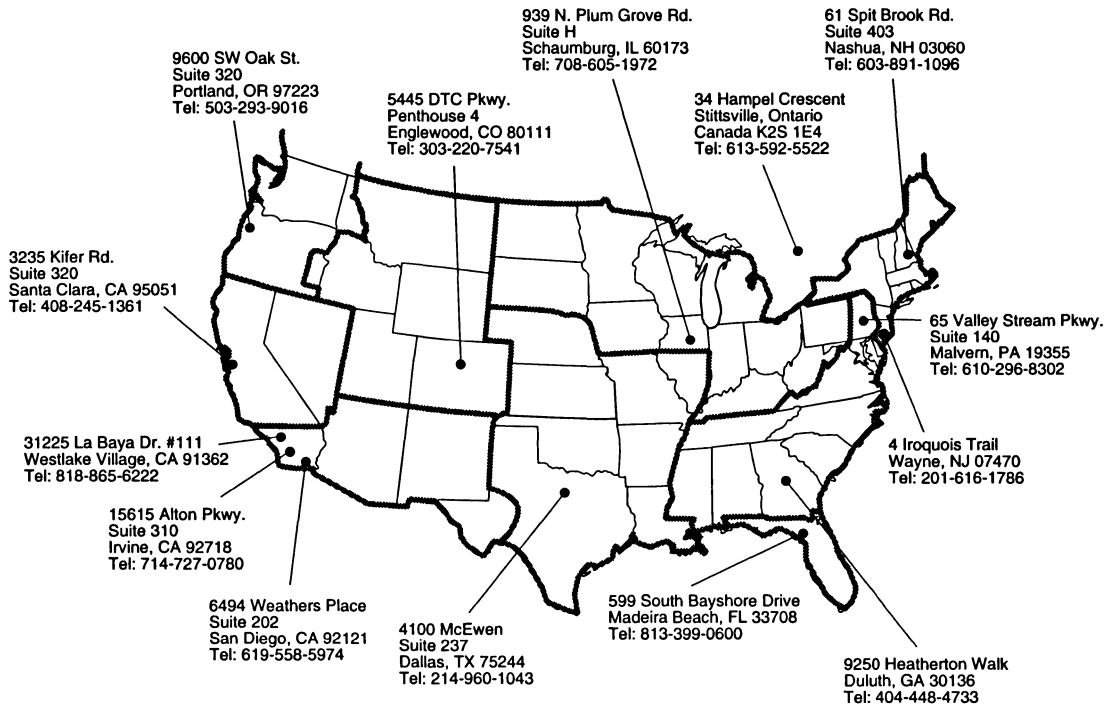Tel: (44) 01844-278278
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