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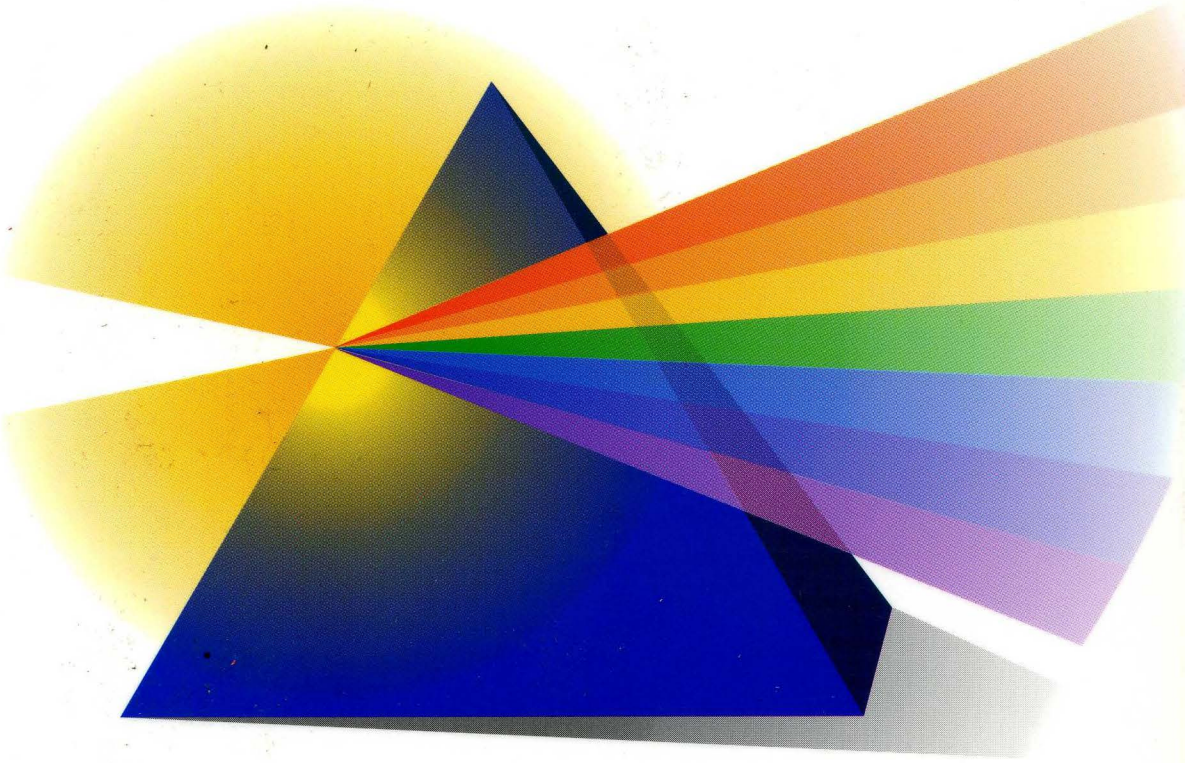
XC9500 CPLD Application Guide

with Data Sheets



February 1996

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SECTION TITLES

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SECTION 1

1 Product Overview

Introduction to FastFLASH™ XC9500 CPLDs

February 1996

Introduced in October 1995, the new XC9500 family of 5 V in-system programmable devices represents the next generation of CPLD solutions from Xilinx. Based on the innovative FastFLASH process technology, the XC9500 family incorporates a unique combination of product features specifically developed to meet all the needs for in-system programmability throughout what is typically known as the "customer's product life cycle".

This product life cycle starts with board level prototyping and system debug, programming and board level testing during manufacturing, and finally, field upgrades. The XC9500 addresses all these needs with industry-leading features such as 5 V ISP, predictable pin-to-pin delays as fast as 5 ns, density to 6,400 gates, 10,000 program/erase cycles, superior pin-locking and extended IEEE 1149.1 JTAG support. Add to this the industry's first 5 V FastFLASH process technology specifically optimized for high-performance in-system programmable CPLDs and Xilinx now has a product which offers customers the industry's best in-system programmable CPLD for their complete product life cycle.

This applications guide assists the CPLD user throughout every phase of their end product. Topics critical to in-system programmability such as pin pre-assignment and field upgrades where adding new features to a current product can be done by changing the software, with no hardware impact are included. In addition, there are detailed technical product specifications.

Xilinx products have always been designed to create a dramatically faster and more efficient product development process. By using these new XC9500 in-system programmable logic devices, customers can now add to those benefits the flexibility, performance, reliability and testability necessary for supporting the ever-shorter product life cycles.

FastFLASH Technology: A New Electrically Erasable CPLD Technology

February 1996

Summary

The Xilinx FastFLASH technology is a new 0.6 micron, double-polysilicon, 2-layer metal CMOS flash technology for CPLDs. The technology is capable of 5 V in system programming, high cell density needed for pin-locking, and a high endurance level of 10,000 in-system program/erase cycles. Compared to typical CPLD-EEPROM technology, FastFLASH technology affords advantages in reliability, density, and performance. The technology compatibility with industry-leading flash processes ensures the scalability of the basic process and the availability of foundry capacity.

Background

CPLDs are programmable by the user to implement the desired logic function. As non-volatile devices, CPLDs retain the programmed information even after power has been removed. This ability is provided by the underlying non-volatile process technology.

The process technology for CPLDs traditionally follows non-volatile memory (NVM) technologies. EPROM memory technology offers excellent memory cell density and low process cost, although it is not electrically erasable. EEPROM technology offers electrical erasability and reasonable process cost. However, it requires a relatively large memory cell size and offers limited endurance. Flash technology, which may be viewed as an electrically erasable extension of EPROM technology, offers the best long term technology solution by providing the cell density of EPROM, the electrical erasability of EEPROM, excellent endurance characteristics, and long term process cost benefits.

Compared to EEPROM technology, the proprietary FastFLASH technology supports the needs of CPLDs by providing:

- high-performance logic capability
- high memory cell density
- electrical erasability
- 5 V program and erase
- high reliability and endurance
- process scalability

This document describes the FastFLASH process technology and compares it with EEPROM technology.

EEPROM Technology

EEPROM technology was the first electrically erasable technology used for CPLDs. The programmable element is a special thin oxide capacitor that conducts a small current when a sufficient voltage is applied across the oxide. The tunnel oxide, approximately 80 Angstroms thick, is used to inject or extract charge from a floating gate via Fowler-Nordheim tunneling. The floating gate is connected to the gate of a sense transistor in order to sense the programming state. In addition to the tunnel oxide capacitor and sense transistor, two more transistors and an additional control capacitor is required to create a single EEPROM cell that can be programmed, erased, and used in a CPLD application.

Figure 1 shows the schematic and cross-section of an EEPROM cell used in CPLDs. The tunnel oxide capacitor transports charge to and from the floating gate, which controls the the sense transistor. Two additional transistors are used for program and read operations. A control gate capacitor is needed to transfer voltage to the floating node for program and erase operations. Compared to standard CMOS logic processes, three additional device structures must be created for the EEPROM cell: the tunnel oxide capacitor, the control gate capacitor and the high-voltage transistor. The resulting process complexity makes the process and EEPROM cell more difficult to scale on future generations of technology.

The EEPROM cell density is poor since each cell is a circuit consisting of five separate device structures. The EEPROM cell area in a typical 0.6 micron technology is 75 to 100 square microns. The poor cell density directly affects the pin-locking ability of the architecture since more routing switches greatly increases the overall die size. The large cell size also introduces parasitic capacitances which limit the overall performance.

FastFLASH Technology

FastFLASH technology is compatible with industry-leading flash processes. The basic programmable element is the flash transistor which incorporates the floating gate into the device structure for improved cell area (see Figure 2). The flash transistor is incorporated into the FastFLASH cell by the addition of an NMOS transistor in series (shown in Figure 3).

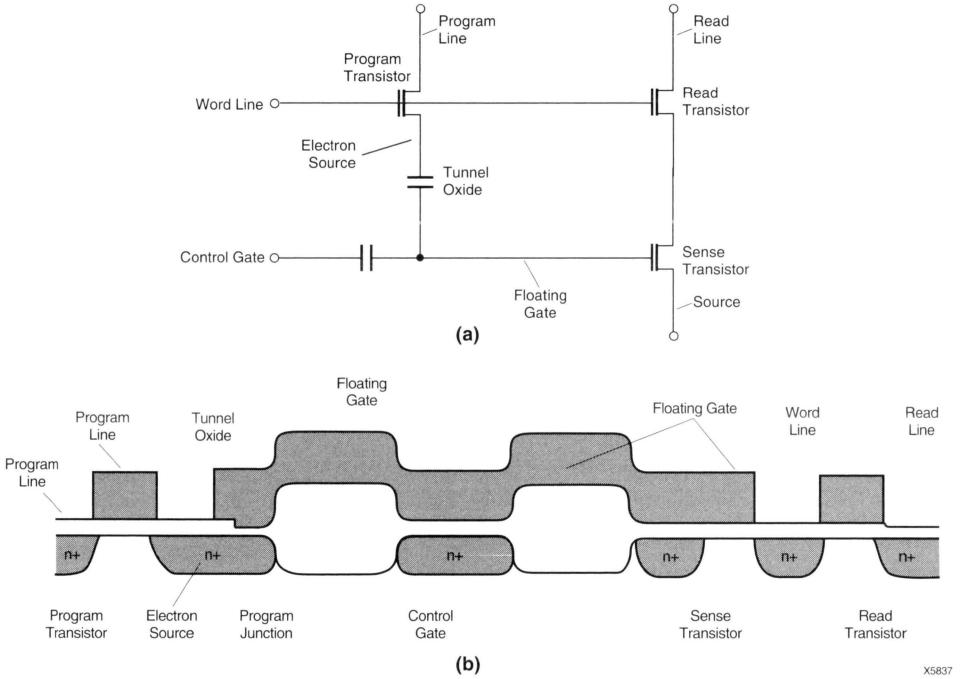

Figure 1. EEPROM Cell (a) Schematic and (b) Cross-section

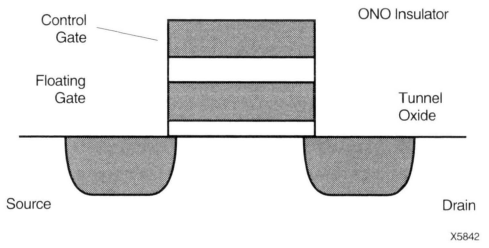

Figure 2. Flash Transistor Cross-section in FastFLASH Technology

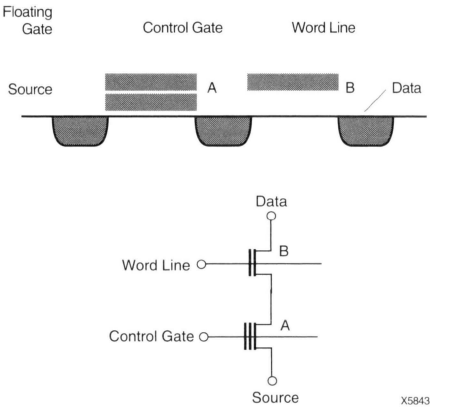

Figure 3. FastFLASH Cell Schematic and Cross Section

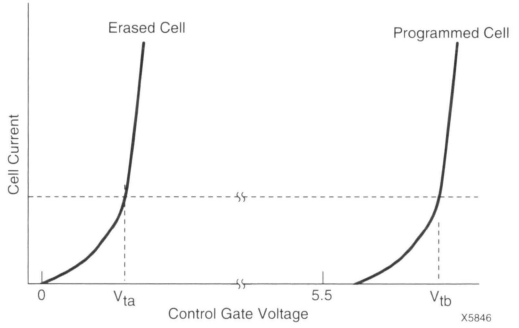

Figure 4. Current vs. Voltage For Programmed and Erased FastFLASH Cell

The behavior of an individual flash transistor can be changed by either programming or erasing operations. When a flash transistor is in the erased state, the threshold voltage (V_{ta}) is approximately 1 V. When the transistor is programmed, its threshold voltage (V_{tb}) is increased sufficiently above 5.5 V so that the transistor cannot be turned on during user logic operation. (See Figure 4.)

The physical structure of the flash transistor includes a floating gate polysilicon layer that is isolated from the silicon substrate by a thin oxide approximately 100 Angstroms thick. Above the floating gate is the control gate polysilicon layer, with an insulating oxide-nitride-oxide layer between them. The control gate is driven by internal logic circuits, while the floating gate is left unconnected. When the flash transistor is in the erased state, there is no net charge on the floating gate. By modifying the net electrical charge on the floating gate, the threshold voltage may be increased to 6 V or more.

The flash transistor is programmed by applying approximately 12 volts to the control gate, 5.5 volts to the drain, and 0 volts to the source (see Figure 5). The voltages can be supplied by internal voltage pumps or externally by a device programmer. During the programming operation, channel hot electrons (CHE) are created near the pinch-off region. Some CHEs have sufficient thermal

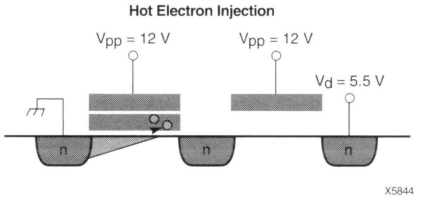

Figure 5. FastFLASH Cell Programming Operation

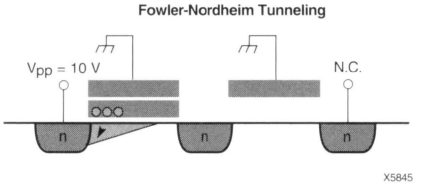

Figure 6. FastFLASH Cell Erase Operation

energy to pass through the thin oxide and remain on the floating gate. The collected electrons create a net negative voltage on the floating gate that opposes the electric field emanating from the control gate. The result is a net increase in the threshold voltage.

The flash transistor can then be erased by applying 0 volts to the control gate and approximately 10 volts to the source with the drain left floating. See Figure 6. In this case, the electric field between the floating gate and the source node is increased to the point when Fowler-Nordheim tunneling can take place. Excess electrons are transported from the floating gate to the source. The transistor is designed to make the erase process self-limiting. As electrons are removed from the floating gate, the electric field decreases. FN tunneling effectively stops when the floating gate is electrically neutral.

Reliability and Endurance

The reliability of the programmable cell relates to data retention and endurance. Data retention is how long the cell can keep its programmed and erased states. Endurance is the number of times a cell can be programmed and erased before failure.

When a cell is programmed and electrons are injected into the floating cell, the net charge should remain indefinitely. In practice, charge leaks off -- typically tens of years under normal storage and operating conditions. The charge transport can occur due to direct tunneling and thermal leakage. Direct tunneling is exponentially dependent on electric field. Generally, the direct tunneling leakage current is very small and largely negligible. Thermal leakage is the dominant leakage component. The leakage characteristics have been thoroughly characterized and modelled.

Endurance is determined by the magnitude of the applied E field and the quality of the thin oxide used for program and erase. When program and erase operations are performed in both FastFLASH and EEPROM cells, electrons are transported across the oxide in the direction of the applied electric field in both CHE injection and FN tunneling operations.

Endurance failures occur in the alteration of the tunnel oxide characteristics with repeated charge transport across the oxide. In FastFLASH technology, the maximum electric field is approximately 10 MV/cm. Consequently, the major cause of endurance failure is electron trapping in the tunnel oxide. After a large number of reprogramming cycles (typically over 100,000 and up to 1 million cycles), traps can be created within the oxide. When a sufficient number of electrons become trapped in the oxide, the localized electric field is distorted. The result is reduced program and erase efficiency, and reduced voltage margins between programmed and erased states. The FastFLASH technology endurance failure is a gradual degradation rather than an abrupt failure.

In EEPROM cells, the program and erase fields are 15 to 20 MV/cm. The substantially higher field makes the EEPROM cell susceptible to destructive tunnel oxide breakdown and electron trapping in the oxide. Since the oxide is physically ruptured, the cell is permanently damaged. The EEPROM endurance failure mechanism is a hard failure and difficult to screen.

In both flash and EEPROM technologies, oxide quality control becomes important. In typical CPLD EEPROM technologies, the tunnel oxide is approximately 80 Angstroms, among the thinnest tunneling oxides in use today. In contrast, FastFLASH technology uses industry-standard process steps to achieve a high-quality tunnel oxide of approximately 100 Angstroms.

There is a difference between the endurance of a single cell, and the overall endurance of the CPLD product which may use 100,000 cells or more. For the CPLD, failure statistics of a large number of cells suggest that the product endurance is typically 1.5 orders of magnitude lower than the endurance of an individual cell.

By using a significantly thicker tunnel oxide and lower electric fields than EEPROM technologies, the FastFLASH technology offers an endurance level of 10,000 cycles. This is compared with only 100 to 1000 cycles for current EEPROM CPLDs.

Cell Density

The FastFLASH cell, with its flash transistor and series read transistor, is considerably smaller than the comparable EEPROM cell with five device structures. Figure 7 shows the relative layouts of the FastFLASH cell and an EEPROM cell. The FastFLASH cell is approximately 25 square microns in 0.6 micron technology. In contrast, the EEPROM cell is approximately 75 to 100 square microns, or 3 to 4 times larger. Therefore, FastFLASH offers three or more times cell density than EEPROM technology.

Cell density is important in CPLD technology, since each routing switch is controlled by a programmable cell. EEPROM-based CPLD architectures use fewer programmable cells for routing, directly impacting the routability and pin-locking capability.

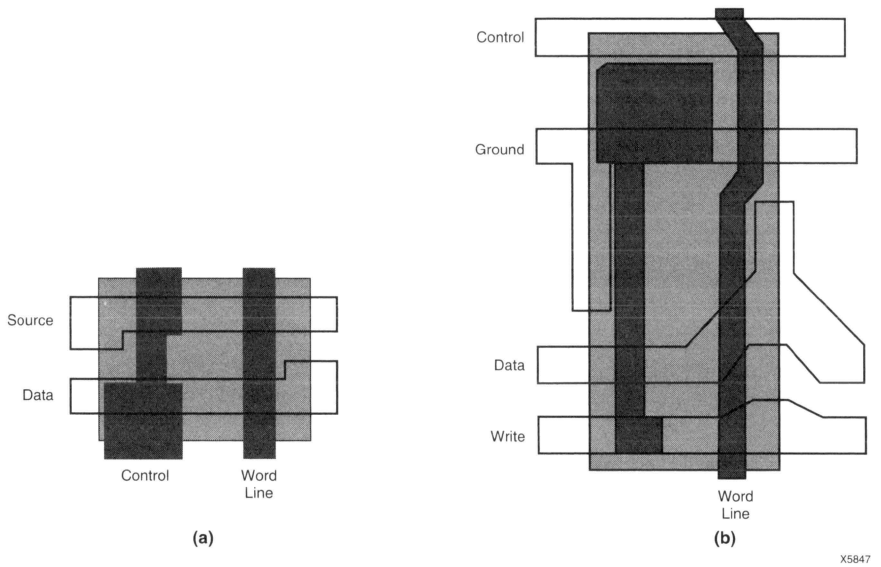

Figure 7. Layout Comparison of FastFLASH Cell (a) and EEPROM Cell (b)

Process Scalability

Process scalability is the ease of shrinking the process and chips to future generations of technology with smaller chip sizes, lower chip costs, and faster chips. It is important to ensure that a migration path to cost and speed improvements, as well as continued availability of the process to meet production requirements.

Factors that contribute to process scalability include:

- Number of different device structures
- Scalability of the programmable cell
- Compatibility with main-stream memory processes

The leading flash memory technologies are double-poly-silicon, stacked gate technologies with CHE injection for programming and FN tunneling for erase. These technologies offer superior process scaling and continued improvements in technology developments for cost and speed. Since the FastFLASH technology is compatible with these process technologies, it will continue to enjoy continued process migration to tighter geometries.

In contrast, EEPROM technology used in CPLDs are not used in high-volume memory technologies. Combined with a complex cell structure, EEPROM technologies are substantially more difficult to migrate to tighter geometries.

Conclusion

FastFLASH technology offers significant advantages in reliability, density, and performance over comparable EEPROM technologies. By utilizing a flash transistor structure that is compatible with the leading non-volatile memory technology, process scalability and future foundry availability is ensured.

References

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(3) S.K.Lai, V.K.Dham and D.Guterman, "Comparison and trends in today's dominant E^2 technologies", IEDM Tec. Dig., pp 580-583, 1986.

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SECTION 2

Designing With XC9500 CPLDs

February 1996 Application Note

Introduction

Xilinx XC9500 CPLDs solve a wide range of logic and state machine problems for today's high performance digital systems. This application note gives a series of useful design examples and practical details for successful designs. Since the architecture is uniform across the XC9500 family, these design techniques apply to all devices.

XC9500 Architecture

The XC9500 architecture is comprised of multiple identical function blocks internally connected with a fully populated FastCONNECT switch matrix. The XC9500 function block has 18 macrocells per block and supports pin-to- pin speeds as fast as 5 ns with clock rates up to 125 MHz. I/O signals can interface with 5 V, 3.3 V or both levels. Current software support includes XACT*step*, ABEL, VHDL, Verilog and operates with additional 3rd party schematic and simulation environments.

Figure 1 shows the global XC9500 architecture. Note the regular structure of high speed function blocks centrally connected by FastCONNECT and surrounded by pins. Signals enter and exit on the pins, form logic operations within the function blocks and form connections and logic operations within FastCONNECT. Each section will be briefly discussed, to show key functionality.

Interconnect within Function Blocks

Function blocks have 36 input sites. The blocks receive signals from FastCONNECT and block input pins. The logic blocks generate 18 signals per function block from the 18 macrocells in each block. Each macrocell signal can drive its own dedicated I/O pin or feedback by entering FastCONNECT. Additional local paths exist within the function block to connect signals at high speed.

FastCONNECT

FastCONNECT attaches high speed pin-signals to the function blocks. It also connects every macrocell output to the function blocks through a fully populated crosspoint

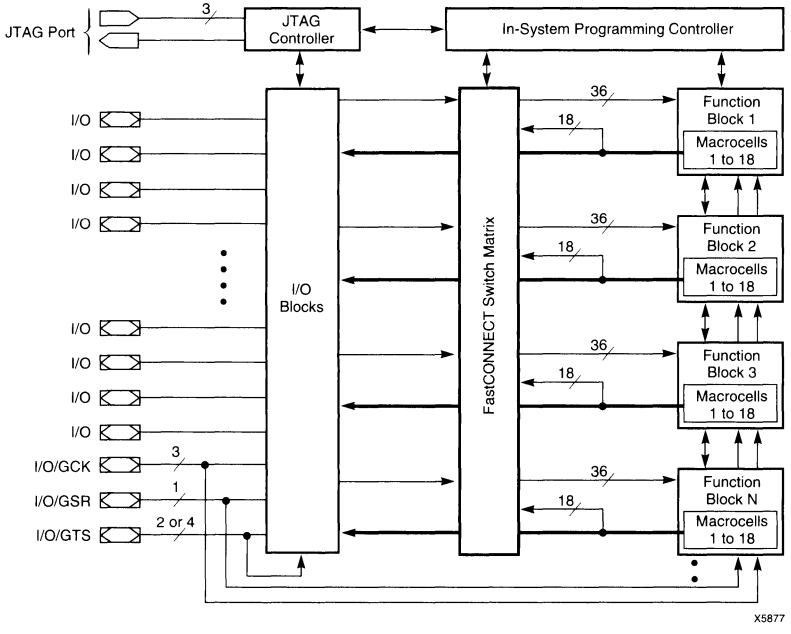

Figure 1. XC9500 Architecture

switch. This connectibility supports design changes when an XC9500 is attached to the printed circuit board.

Function Blocks

The function blocks (Figure 2) are groups of 18 macrocells. Each Function Block has 90 p-terms which can be assigned to any of the 18 macrocells via a proprietary allocation mechanism. This provides optimum logic flexibility within the function block and helps ensure pin-locked designs. Highest possible performance is attained by the software assigning a uniform five product terms per macrocell. The macrocell outputs can then drive output pins and/or feedback to both FastCONNECT and the function block in which it resides.

The Macrocell

In the default mode, there are 5 product terms that OR together driving the D input to the macrocell flip flop (see Figure 3). The most common arrangement includes an EX-OR gate capable of performing parity, full addition or logical inversion.

Another configuration exports product terms to a neighboring macrocell, increasing that macrocell's available product terms. Product term exporting is shown in Figure 3. Assigning all product terms as needed across the function block is possible.

As shown, XC9500 flip-flops can be configured as a D or T flip-flop. This permits efficient counters to be built using but a few gates to drive the state transitions. Table 1 summarizes the number of p-terms needed to build up common logic functions. Most datapath functions require one or fewer macrocells per bit.

Table 1: Macrocell/Product Term Allocation

Data Operation	P-Term Used
Shift Register	2
Counters	2-4
n:1 Mux	n
Adder	6
EX-OR	2
Storage registers	1

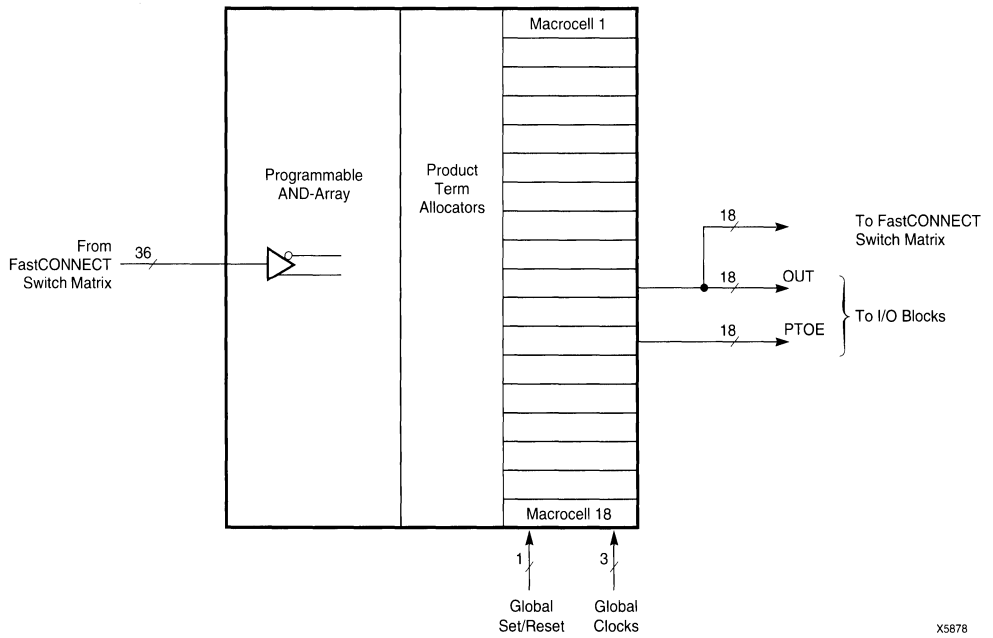

Figure 2. XC9500 Function Blocks

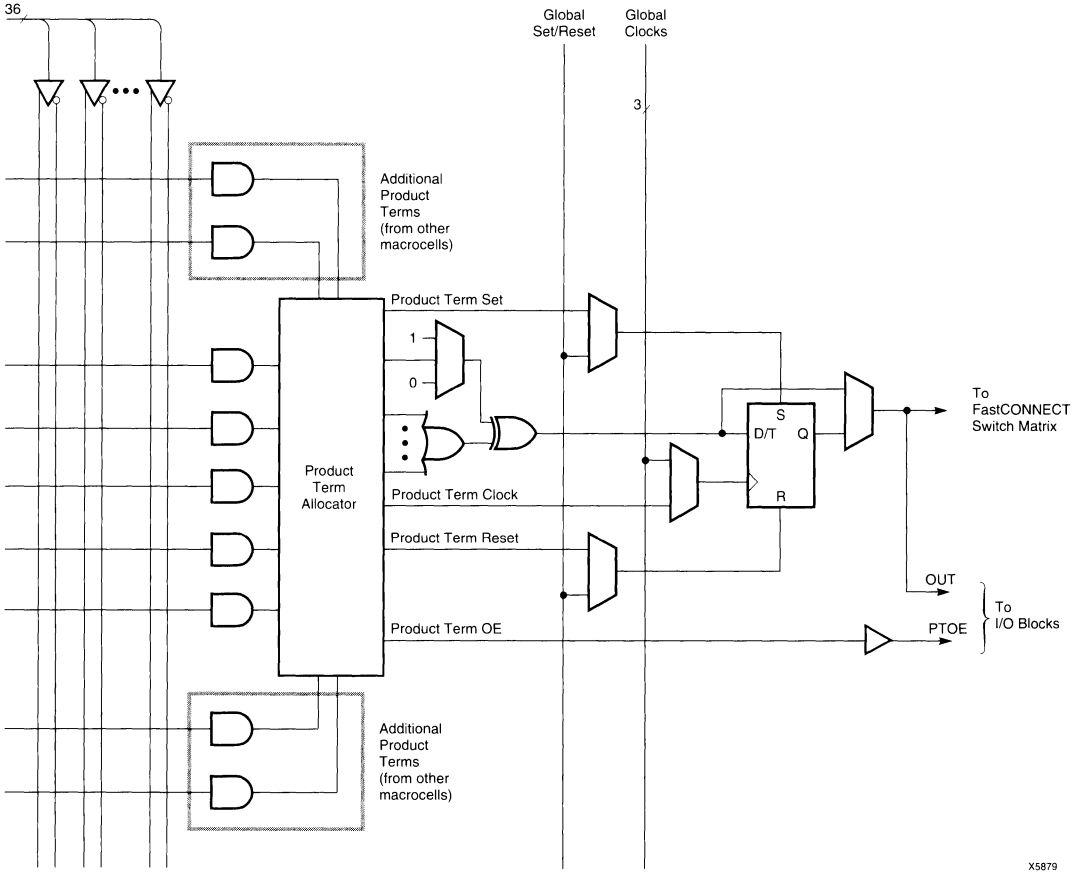

Figure 3. XC9500 Macrocell

Table 2 shows the pin compatibility of the XC9500 family. Specifically, designs can be migrated among the parts. In many cases, greater density with equivalent speed can be gained by using larger parts. Should a design initially target a small part, the exact same design can be moved into larger parts, if additional capability is required. This capability helps designs maintain their pin assignments if additional logic capacity is needed in a socket that is already committed to a printed circuit board.

Automatic Software

The design examples presented are shown using ABEL-which is simple and easy to understand. Typically,

Table 2: XC9500 Available Packages and Device I/O Pins

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288
44-Pin PLCC	34						
44-Pin VQFP	34						
84-Pin PLCC		69	69				
100-Pin PQFP		72	81	81			
100-Pin TQFP		72	81				
160-Pin PQFP			108	133	133	133	
208-Pin PQFP					168	168	168

Note: Does not include the dedicated JTAG pins.

designers won't designate specific function mapping into XC9500 designs, but occasionally, designers like to control how a solution is implemented, so these methods may be of interest.

Boolean operators used by ABEL are simply !,# and & for INVERT, OR and AND, respectively. Combinational logic expressions are formed with a simple equal (=) sign with operands and operators located on the right hand side of the expression.

Flip-flop expressions are formed by writing expressions for the specific control pins of the flip flop. The D-input is a special case, where the equal sign is replaced by the compound symbol :=. Clock inputs are determined by the syntax FFname.clk, and reset inputs are designated by FFname.rst.

A design file contains a header section including optional documentation sections and mandatory declaration of inputs, outputs, global signals and any user preferred arrangement of functions.

Logic AND

FastCONNECT is capable of combining signals with a wire AND function. As single lines enter FastCONNECT, they are assigned to function block inputs, making connections. However, multiple lines driving a FastCONNECT connection form a wired AND function, that is useful for making additional logic. This feature increases both the logic capacity and available entry points to the Function Blocks.

Gates

The following expressions show the basic logic operations.

```
ABAR = !A;

AORB = A#B;

AANDB = A&B;

ANORB = !(A#B);

ANANDB = !(A&B);

AEXORB = A$B;

AEXNORB = A!$B;
```

Muxes and Decoders

Using the above methods, compound expressions are formed to build up logic functions. Using A0 to A3, B0 to B3 and SEL (select) as inputs, a multiplexer follows:

```
DAT0 = SEL&A0 # !SEL&B0;

DAT1 = SEL&A1 # !SEL&B1;

DAT2 = SEL&A2 # !SEL&B2;

DAT3 = SEL&A3 # !SEL&B3;
```

The approach extends to larger multiplexers. The above uses one macrocell per data bit and leaves behind two unused product terms in each macrocell. To take advantage of four product terms per macrocell, the idea expands as follows:

```
DAT0 = S1&S0&D0 # S1&!S0&C0 #
       !S1&S0&B0 #!S1&!S0&A0

DAT1 = S1&S0&D1 # S1&!S0&C1 #
       !S1&S0&B1 #!S1&!S0&A1

DAT2 = S1&S0&D2 # S1&!S0&C2 #
       !S1&S0&B2 #!S1&!S0&A2

DAT3 = S1&S0&D3 # S1&!S0&C3 #
       !S1&S0&B3 #!S1&!S0&A3
```

Very high speed decoders can be built in the macrocells to form SRAM select signals, but do not use all of the macrocell product terms or the flip flop in most cases. Decoders are formed as follow:

```
DEC0 = !A3&!A2&!A1&!A0

DEC1 = !A3&!A2&!A1&A0;

DEC2 = !A3&!A2&A1&!A0;
```

Registers

Simple registers are formed as follows:

```
A:= DATAINPUT;
A.CLK = CLOCK;
A.RST = RESET;
```

This describes a D flip flop with its input tied to something named DATAINPUT, its clock tied to a signal called CLOCK and its reset input tied to a signal called RESET.

Shift Registers

Cascading registers results in a shift register as follows:

```
A:=DATAINPUT;
B:=A;
C:=B;
D:=C;
A.CLK = CLOCK;
B.CLK = CLOCK;
C.CLK = CLOCK;
D.CLK = CLOCK;
A.RST = RESET;
B.RST = RESET;
C.RST = RESET;
D.RST = RESET;
```

This shifter uses four macrocells. If the signals designated A,B,C,D are declared as outputs, they will appear somewhere at the pins of an XC9500 part. If A,B,C and D are declared as nodes (internal points), the software buries them.

Counters

Counters can be built in a number of different ways. The most efficient is to have the macrocell flip flops configured as T flip-flops. The following equations form T flip-flops, add logic to load, hold, increment and clear the flip-flops. Note the compact vector notation:

```
module Tcount

title '4 bit counter with load and clear'

    D0..D3          pin;
    Q3..Q0          pin istype 'reg_T';
    CLK, I0, I1     pin;
    Data    = [D3..D0];
    Count   = [Q3..Q0];
    Mode    = [I1,I0];
    Clear   = [0,0];
    Hold    = [0,1];
    Load    = [1,0];
    Inc     = [1,1];
equations

    Count.T =  ((Count.q+1)    & (Mode == Inc)
               # (Count.q)     & (Mode == Hold)
               # (Data)        & (Mode == Load)
               # ( 0 )         & (Mode == Clear))
               $ Count.q
    Count.C = CLK;
end
```

Comparators

Comparators are easily handled by the XC9500 macrocell. Single bit comparators do not use all available macrocell product terms. A more efficient use is to handle four bits at a time to generate multiple compares per macrocell:

```
COMP =   !B1&!B0&!A1&!A0 + B1&!B0&A1&!A0
         !B1&B0&!A1&A0   + B1&B0&A1&A0
```

Next, several COMP signals can be gated together to detect equality across larger groups of bits. Each group of four bits uses 4 function block inputs and several four bit compares can occur per function block. Another macrocell then forms the composite function of all the bit compares, as needed. Figure 4 shows this technique expanded to a 10-bit comparator, which is commonly used on the most significant address lines of a 32-bit microprocessor's address lines.

Parity

Similar to compares, parity can be calculated with multiple data bits per macrocell. The first three bits are calculated using four p-terms ORed. This result is then delivered to the macrocell EX-OR where a fourth data variable is introduced.

Latches

Occasionally, designers need a transparent latch within an XC9500 device. The latch is formed by feeding the macrocell combinatorial logic back upon itself per the following equation:

```
Q = ENA&DATA + !ENA&Q + Q&DATA
```

The signal Q&DATA is included to eliminate a hazard, making the Q output glitch free.

Practical Considerations for XC9500 Designs

XC9500 CPLDs offer additional system features. By following a few simple rules, the XC9500 device interfaces with systems using 3.3 V and 5 V devices. Also, very high speed CPLDs behave much better if standard high performance printed circuit board techniques are adhered to, so a small checklist is appropriate for those rules. Best CPLD behavior is obtained by following a

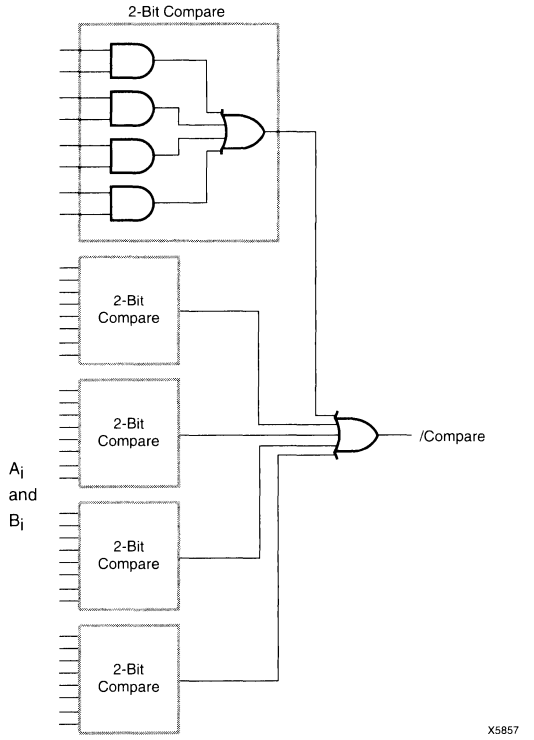

Figure 4. 10-Bit Comparator

few guidelines with respect to the power-on Master Reset capability.

Mixed Voltage Operation

XC9500 CPLDs support mixed voltage systems combining both 3.3 and 5 Volt components. (See Figure 5). The XC9500 family contains both logic and level shifting functions in a single programmable device. This eliminates the need for discrete level translation buffers. These CPLDs feature split power supply rails. The internal core logic always runs at 5 volts for the fastest possible performance. The output buffers can be powered by either 5 volts or 3.3 volts by connecting the I/O V_{CC} to a 3.3 volt or 5 volt supply. True TTL compatibility allows XC9500 CPLDs to drive and be driven by any combination of 3.3 and 5 volt logic without any performance penalty, even when the I/O V_{CC} pins are powered by 3.3 volts.

The XC9500 I/O structure is shown in Figure 6. Input protection diodes are connected to the internal 5 volt power supply rail and not the output buffer supply rail. This allows the input to withstand a maximum voltage of >5 volts, even when the I/O power pins connect to 3.3 volts. Since both output transistors are N-channel devices, there is no parasitic diode to be forward biased if the output is 3-stated and a 5 volt device is driving the XC9500 I/O pin. The CPLD then operates on a bus including both 3.3 V and 5 V devices.

Since the input protection circuitry is powered by the 5 volt core logic supply, the 5 volt supply must always be powered up before the 3.3 volt I/O supply. This prevents external 3.3 V devices from forward biasing the protection diodes. Similarly, the 3.3 volt I/O supply must be powered down before the 5 volt core logic supply. This is not an issue with 5 volt only systems.

XC9500 devices are TTL-compatible with 3.3 and 5 volt logic as shown in Figure 7. The 5 volt TTL logic input thresholds are VIH = 2.0 V and VIL = 0.8 V. XC9500 CPLDs drive HIGH greater than 2.4 V and LOW below 0.4 V at rated output drive currents, with at least 400 mV noise margin.

High Speed Design Considerations

XC9500 CPLDs are offered with pin-to-pin delays as fast as 7.5 and 5 ns. The actual parts may in fact be somewhat faster. Additional care should be taken when using these parts, because of this speed, so that adjoining chips will operate properly.

Many high speed designs also require high current drive outputs for handling capacitive loads. XC9500 CPLDs provide 24 mA drivers to eliminate the need for additional buffering that might impact system speed. This results in a need to manage the total current being switched, so a strategy to do that is provided.

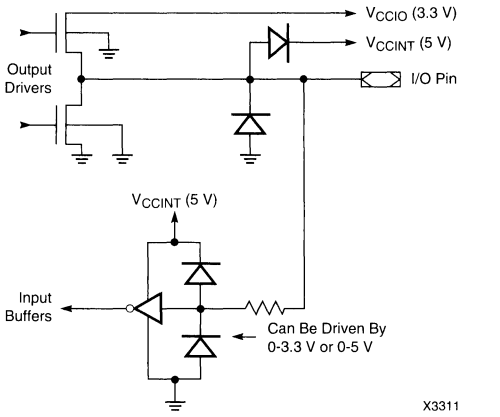

Figure 6. XC9500 I/O Structure

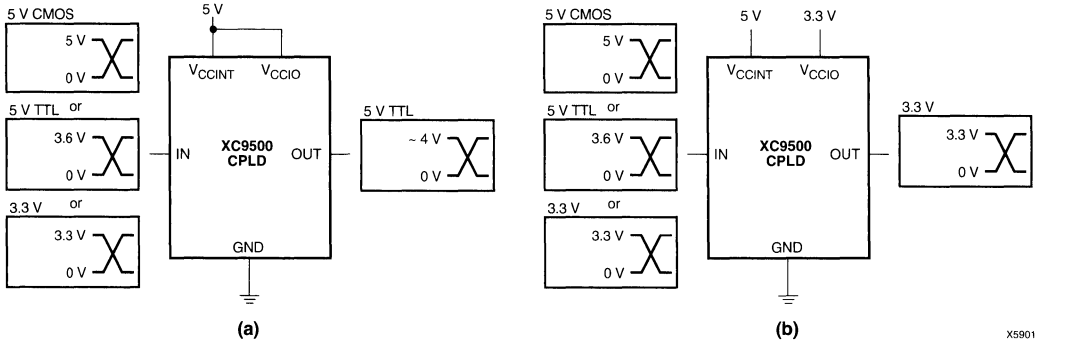

Figure 5. Typical Mixed Voltage System

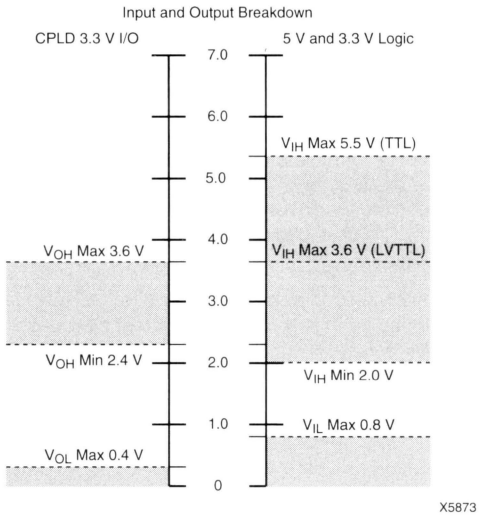

Figure 7. XC9500 CPLD Driving 3.3 V and 5 V Components

As with other high speed logic devices, XC9500 CPLDs should use low inductance capacitors located as close as possible to the V_{CC} and GND pins when mounted on a PC board. Care should be taken to mount the devices so that the PC interconnect traces are as close as possible to the target signal destinations.

Layout Checklist:

Complying with the following checklist assures a successful design with XC9500 CPLDs:

1. Tie unused inputs to ground.
2. Locate XC9500 CPLDs near chips they drive or are driven from to minimize transmission line effects.
3. Use wide spacing between fast signal lines (particularly clocks) to minimize crosstalk.
4. Power pins (V_{CC} and GND) are recommended to be placed on separate printed circuit board planes. Fast signals should reside on another plane, as well.
5. Decouple the chip V_{CC} with a 0.1 microfarad capacitor directly connecting each physical chip V_{CC} to the nearest ground plane. Low inductance, surface mounted capacitors are recommended.
6. Decouple the printed circuit board power inputs with 0.1 µF ceramic (high frequency) and 100 µF electrolytic (low frequency) filter capacitors.
7. All device ground pins must be connected together.
8. Avoid using sockets to attach XC9500 CPLDs to the PCB. Direct soldered connection minimizes inductance and reduces ground rise. XC9500 CPLDs are specifically designed for direct PCB attachment without need for sockets.

Managing Ground Rise

Today's high performance designers must also be aware of additional factors that can affect the performance of fast, high-current drive systems. As mentioned earlier, possible voltage rise on device ground pins can affect the driven output levels and be sensed by the switching CPLD.

Figure 8 shows how ground rise is typically observed with today's high-performance CPLDs. In this setup, multiple outputs are switched with a control variable, while one output is constantly being driven low and observed. As the multiple outputs switch, their in rushing current converges at the ground pin(s) of the CPLD. Lead impedance causes the reference ground to develop a voltage higher than before the switching occurred. The result is that the static output being observed also develops an observable voltage swing.

All digital ICs have this property. No harm is caused to the system unless the voltage swing on the static output is capable of switching another circuit down the line. Problems can occur if the voltage swing is excessive. This effect is particularly significant if the static (quiet) signal is attached to another circuit's clock input.

Two factors contribute to this ground rise. First, the amount of capacitive load being driven is important because charge on this capacitance is the source of the in rushing current. Second, the number of simultaneous switching outputs is a factor since each switching output adds to the total capacitance being discharged.

The XC9500 family includes User Programmable Ground for internal chip signal management. XC9500 devices are in symmetric packages with multiple ground pins. However, some designs need more ground pins for current.

User Programmable Ground allows the device I/O pins to be configured as additional ground pins. Tying programmable ground pins to the external ground connection reduces system noise. XACT*step* software automatically connects unused macrocell outputs to ground.

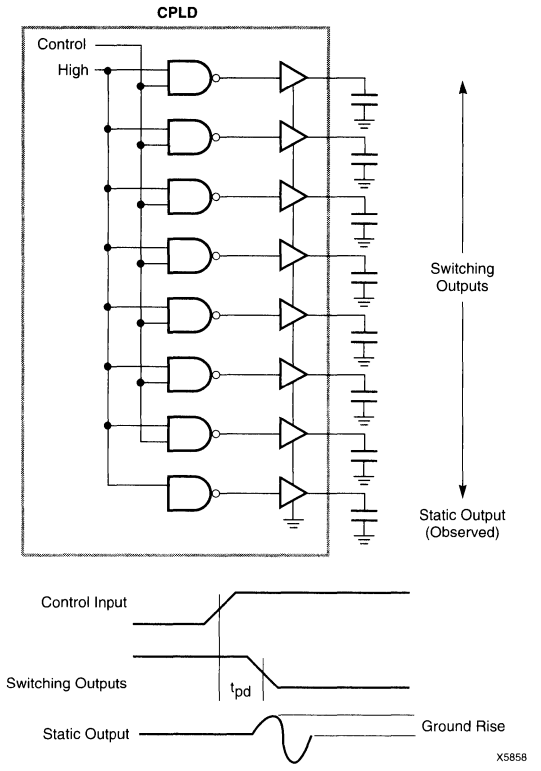

Figure 8. Ground Rise Test

The following checklist will reduce unnecessary ground noise:

1. Pinout only essential outputs. Intermediate shifter bits, and counter bits that need not drive outputs should remain buried.
2. Minimize the number of outputs switching simultaneously.
3. Two global clock inputs can be managed similar to the two GTS signals, by delaying one to gain signal skew.
4. Additional grounding can lower ground rise effects, and may be dealt with simply. Unused outputs can be tied directly to the PCB ground. This splits the current driven into heavily loaded ground pins and lowers the voltage rise.
5. Signal skewing can also reduce ground rise. This can be achieved by mixing ordinary and fast slew outputs. Only assign fast slew to signals that require it.

Power On Master Reset

XC9500 devices undergo a short internal initialization sequence upon device powerup. During this time the outputs remain 3-stated while the device is configured from its internal registers. While the internal initialization sequence occurs the device outputs remain 3-stated until the sequence is complete. Although the outputs are 3-stated, they are gently pulled up through 10K ohm impedance pullups. Alternate Master Reset can be accomplished by using the ISPEX JTAG instruction.

Conclusions

By using the techniques discribed in this application note, designers achieve a solution to their high-performance logic requirements with the XC9500 family. The XC9500 family datasheet contains additional descriptions of the important system features.

Pin Preassigning With XC9500 CPLDs

February 1996 Application Note

Summary

This application note details the planning required for successful pin preassigning with XC9500 CPLDs.

Xilinx Family

XC9500 CPLDs

Demonstrates

A step by step procedure to assure best results for designing when the pinouts are preassigned.

Guidelines to follow for best results.

Introduction

Reducing time to market is critical in today's high performance digital marketplace. Designers need to prototype their products as swiftly as possible. Many designers estimate their CPLD design needs and predict the pinouts required in advance to remove the printed circuit board bottleneck from the prototype schedule. The XC9500 CPLD architecture permits preassigning pins with a high degree of success by following a few simple guidelines. The architecture also allows future edits to the design while maintaining the existing pinout. However, some planning of the design at the outset is necessary. This application note details guidelines for sucessful pin preassignment.

Many designs can be partitioned into datapath and control logic portions. Datapath operations are regular, bit operation oriented and maintain relative positions among the bits. Datapath operations also maintain their functionality once they are designed.

Control operations change as timing is adjusted through the design cycle and specifications are altered. These operations evolve as a design progresses. Control operations are much less structured than data operations. The design strategy is different.

Obtaining a reasonable estimate of the design's logic requirements for both control and datapath operations is the key to preassigned pinouts. Once an estimate is obtained, pins are assigned with a high degree of confidence that the function block driving the pins will have the available resources to connect the logic needs of the corresponding macrocells. It is importatant to remember that since the design needs for datapath and control operations are different, estimating their initial requirements differ. Actual completion of the design with the software making the appropriate pin assignments assures sucess.

XC9500 Routing Resources

XC9500 CPLDs combine a locally efficient logic block with a globally flexible interconnect structure to provide ideal connectibility for a very large spectrum of designs. Here are a few of the key qualities of the logic block:

a. 36 input signals presented to the logic block

b. Automatic allocation of product terms as needed within the function block. The average is 5 product terms per macrocell, but up to 15 is easily obtained and more can be had when needed.

c. Formation of efficient counters, multiplexers, shifters and parity circuits with an efficiency of one macrocell or less per bit. The remaining logic is available for use by functions needing more logic.

Here are some properties of the interconnect structure:

a. Any input pin connects to any function block with constant high speed across the entire device.

b. Any macrocell output can connect to its own or any other function block with complete freedom.

c. Macrocells can be internally bused with bit level independent 3-state control forming internal databuses with global access to all logic blocks. No other CPLD architecture offers this capability, which saves macrocell logic by using the routing resources to form multiplexers.

These features are essential for editing integrated circuits already attached to boards. The flexibility of the XC9500 routing resources compensates for virtually all design changes.

Datapath Guidelines

Datapath operations include storage, shifting, multiplexing, arithmetic, comparison and boolean operations. In

the majority of cases, estimating the logic needs for a single bit is sufficient to quickly estimate the entire datapath. Table 1 gives the macrocell needs of various data operations.

Table 1: Macrocell/Product Term Allocation

Data Operation	P-Term Used
Shift Register	2
Counters	2-4
n:1 Mux	n
Adder	6
EX-OR	2
Storage registers	1

The primary guideline is to interleave output functions that need many product terms with functions that need few.

The design software easily finds the product terms for functions with excessive requirements from neighboring macrocells requiring few. As shown in Table 1, there are few functions requiring more than 4 product terms per macrocell. This suggests that all functions will easily fit into incremental macrocell units. The adder, which requires more than one macrocell (i.e. one for the full adder sum bit and additional carry logic distributed among the adder bits) and the n:1 Mux which may need more product terms than a single macrocell can supply are exceptions.

Control Path Guidelines

Control logic is less straightforward than datapath logic since the control circuitry's logic needs vary and the timing is tight. Simple combinatorial control signals are easy to estimate, however state machines are not. However, one-hot encoded state machines, which are flip-flop rich and input logic lean, may be used for estimation purposes. One-hot encoding works because:

a. There is no required sophisticated state encoding

b. The input signals can be managed in a straightforward way

c. Performance degradation can be quantified at the initial estimation time.

d. One-hot state machines are easily edited to add or delete states without upsetting the state encoding.

e. Encoded state machines usually produce more compact logic with no speed degradation in a CPLD, but one hot solutions give a worst-case estimation.

Editing one-hot machines without significantly altering the overall structure of the machine is easy. States may be inserted or deleted without major impact on the next state and output logic encoding. One-hot designs can also be implemented in either the Mealy or Moore versions as required. Figure 1 shows the basic one hot encoding structure. The shaded region of the figure shows additional logic added to alter the four state machine (A,B,C,D) to a five-state machine (A,B,C,D,E) without complete reencoding of the machine.

Recommendations

The general guidelines to preassign pins are very simple:

1. Do an estimated design first and let the design software assign the pins.

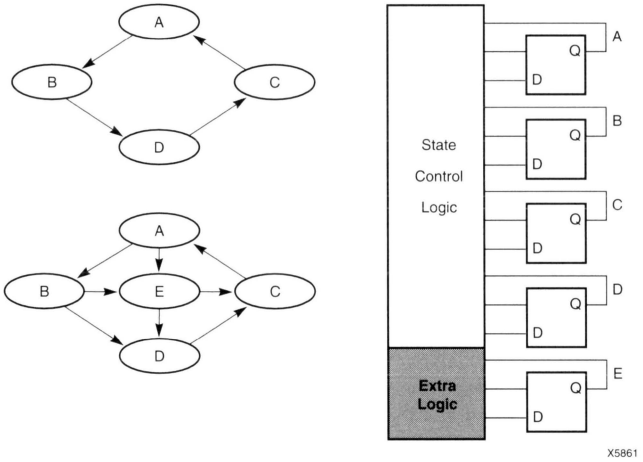

Figure 1. One-Hot Encoded State Machine Editing

2. Alternately minimize risk by estimating the design needs yourself:
   a. partition data and control portions
   b. estimate the needs of each portion
   c. consider one hot control unit designs to permit future editing and stable pin assignments
3. The following cell arrangement techniques should be adhered to:
   a. Spread the outputs among all function blocks
   b. Within Function Blocks, spread macrocells evenly, with unused macrocells interleaved.
   c. Assign outputs using common inputs to the same function blocks
   d. Don't use global pins (clocks, resets, tri-state enables) for logic inputs or outputs unless the global pins are not needed.
4. XC9500 CPLDs have common footprint packages for various density parts. By designing for the smallest capacity in a specific package footprint, there is always the option of a pin compatible density upgrade that matches the existing pinout. Table 2 below shows the available packages and device I/O pins in the XC9500 family.

Conclusion

Pin preassigning is successfully achieved with XC9500 CPLDs by following simple guidelines. It is always recommended to do an estimated design and let the design software assign pins before committing to a printed circuit board. The benefits of preassignment include faster time to prototype and ultimately faster time to market. Xilinx XC9500 CPLDs provide the speed and flexibility to make this goal a reality.

Table 2: XC9500 Available Packages and I/O Device Pins

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288
44-Pin PLCC	34						
44-Pin VQFP	34						
84-Pin PLCC		69	69				
100-Pin PQFP		72	81	81			
100-Pin TQFP		72	81				
160-Pin PQFP			108	133	133	133	
208-Pin PQFP					168	168	168

Note: Does not include the dedicated JTAG pins.

XC9500 CPLD Embedded Diagnostics

February 1996 Application Note

Summary

This application note describes how to build signature analysis circuitry into a remote system to isolate problems.

Xilinx Family

XC9500 CPLDs

Demonstrates

Using Linear Feedback Shift Registers to calculate signatures.

Planning for designs that will be altered in the future.

Overlaying diagnostic circuitry after a system has been installed in the field.

Introduction

Today's high performance systems are at a level of complexity where it may be difficult to determine functionality in a remote environment. Data communication systems and remote data acquisition are examples of this model. Designers need embedded diagnostics to isolate and identify potential problems before assigning on-site field personnel. Using available chip resources for test circuitry is an effective way to design embedded diagnostics. The function is accomplished by allocating extra circuitry or reprogramming existing circuitry in the system. XC9500 CPLDs may be used for either approach. However some planning in the original system design is necessary.This application note outlines the signature analysis approach to design remote embedded diagnostics.

Signature Analysis Fundamentals

Various nodes (outputs or signal points) in a system will exhibit repeatable behavior patterns under identical input signal sequences. Incorrect behavior will generate different sequences. Comparing the sequences in the failing system to the previously recorded node sequences will identify the problem.

This approach requires a large number of storage cells and circuitry to perform the comparisons. Signature analysis identifies a set of critical "test points" in a system. It also captures an encoded binary pattern using a polynomi encoding scheme similar to that of cyclic Linear Feedback Shift Registers (LFSRs). The circuitry consists of a moderate-sized shift register with Exclusive-Or functions embedded at key positions. These functions generate distinctive patterns called signatures. Figure 1 shows a typical setup of a signature analyzer in symbolic form.

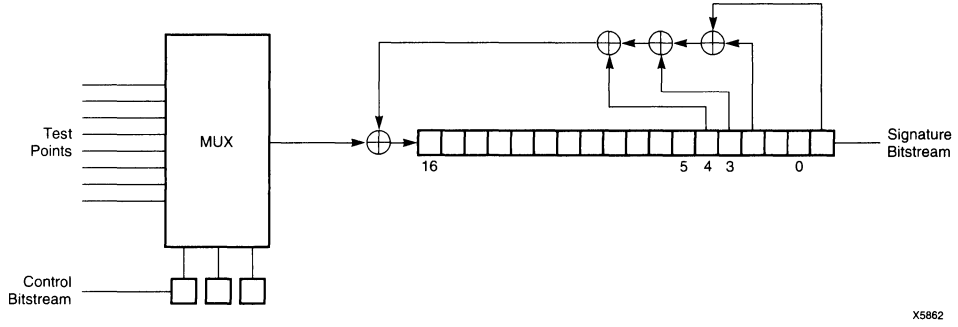

Figure 1. Basic Signature Analyzer Structure

XC9500 CPLD Signature Support

High performance CPLDs are frequently used in memory and system controllers. Memory controllers are centrally located and multiprocessing systems may have several CPLDs on different cards.This makes CPLDs a natural place to embed diagnostic circuitry. Here is a natural strategy to follow:

- Verify microprocessor operation at initialization by capturing signatures transitioning out of reset.
- Verify more signatures as the processor steps through its bootstrap ROM.
- Capture signatures as the processor tests the memory and subsequent I/O operations.

Figure 2 shows how such a configuration might be built.

XC9500 CPLDs easily implement any or all of the Figure 2 system. However, it is possible to build the signature analyzer for free. During the previously mentioned strategy, the DRAM may not be involved in the system diagnostic while the processor is booting from ROM. In this case, the signature analyzer is constructed from the logic later used as the DRAM controller. While the DRAM is tested, unused data communication's or I/O circuitry acts as the signature analyzer. Therefore different system pieces could be reused or adapted to suit the diagnostic needs.

Test Strategy Overview

The signature analyzer is a multiplexed shift register with Ex-Or gates. The shift register must be initialized. However, some patterns are inappropriate. For example, all zero initialization causes a signature analyzer to fail. The ability to initialize the register to a known pattern is necessary.

The test points, shown in Figure 1, are selected with a three bit serial register and a mux. The signatures must be unique. Each test point has an identical starting point.

Before signature testing occurs, capture known good signatures and store them for future comparison. Use exactly the same procedure outlined below:

- Aim the mux at a chosen test point
- Initialize the Linear Feedback Shift Register (LFSR)
- Enable the LFSR
- Enable the device under test (DUT)
- Count operation cycles of DUT until complete
- Disable the LFSR and DUT
- Read back signature
- Compare this signature to the known good signature

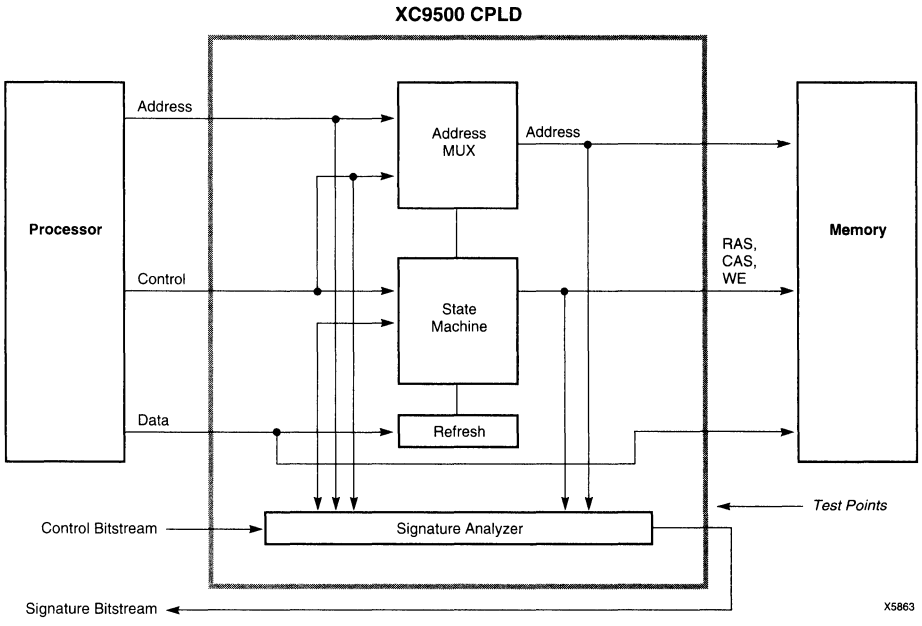

Figure 2. Embedded Signature Analyzer

Managing the sequence of captured patterns is important. Once a board has passed all signature tests, the scope of the diagnostic can be increased. For example, analizing data communication circuits with selected loopback tests. Additional tests may also be performed using the signature method. (See Figure 3).

Practical Considerations

Here are some guidelines to use when designing signature analysis experiments:

- Synchronous behavior is the most repeatable and the most desirable to use for signature analysis.
- Selection of test points should be done so their global influence is a factor for selection. Any processor status/ control lines which enable data transfers, generate interrupts or make bus requests are candidates.
- Most signatures are unique. However, there is a remote possibility of obtaining aliases. Check for aliases during the initial capture of healthy behavior.
- Table 1 supplies a set of feedback equations for building LFSRs which are the basic components for signature analyzers. Data entry can be Ex-Or'ed with the feedback input variable (n in this case).
- Avoid initializing the signature register with all 0s.
- Supplement signature analysis with other diagnostics, such as memory tests and disk CRC diagnostics.

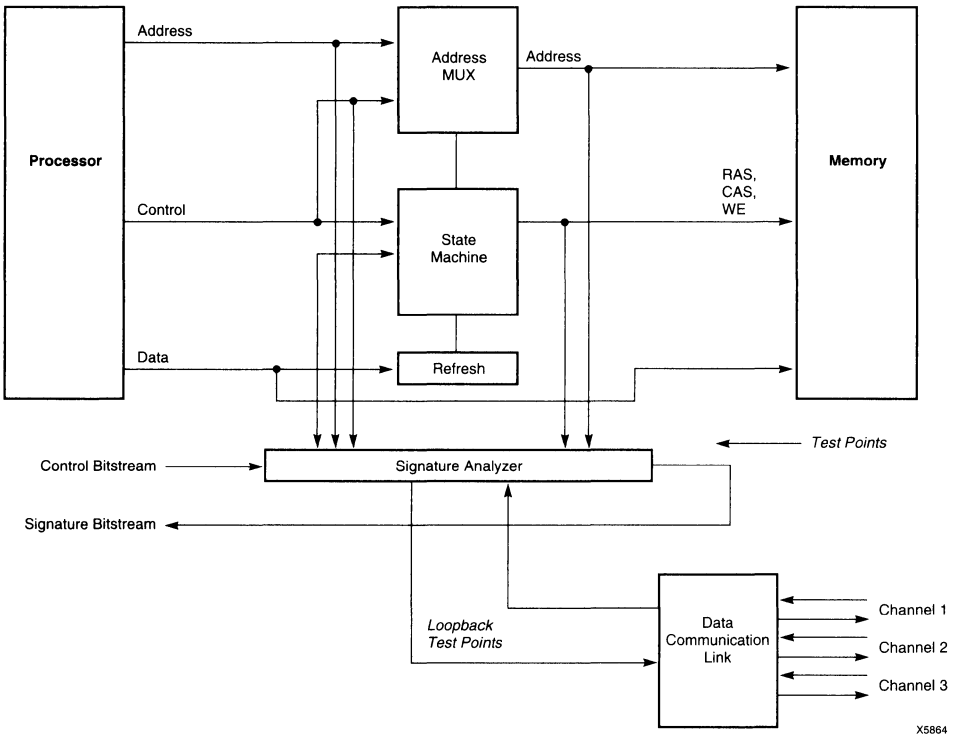

Figure 3. Adding in Data Communication Loopback

Table 1. LSFR Feedback Equations

n	Feedback Equation
2	X2 = X1 ⊕ X0
3	X3 = X1 ⊕ X0
4	X4 = X1 ⊕ X0
5	X5 = X2 ⊕ X0
6	X6 = X1 ⊕ X0
7	X7 = X3 ⊕ X0
8	X8 = X4 ⊕ X3 ⊕ X2 ⊕ X0
12	X12 = X6 ⊕ X4 ⊕ X1 ⊕ X0
16	X16 = X5 ⊕ X4 ⊕ X3 ⊕ X0
20	X20 = X3 ⊕ X0
24	X24 = X7 ⊕ X2 ⊕ X1 ⊕ X0
28	X28 = X3 ⊕ X0
32	X30 = X22 ⊕ X2 ⊕ X1 ⊕ X0

Conclusion

XC9500 CPLDs provide the technology to build effective but inexpensive embedded test circuitry in a wide range of microprocessor systems. However, this capability is not limited to microprocessor diagnostics, and may be easily expanded to include a wider range of digital systems.

References

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2. Design of Testable Logic Circuits, R.G. Bennets, Addison-Wesley, 1984
3. Digital Design (Principles and Practices), J. Wakerly, Prentice-Hall, 1994

XC95108 CPLD High Performance System Controller

February 1996 Application Note

Summary

The XC95108 is shown as a single chip high performance system controller. It handles all the address decode, state machines, and logic needs of a high performance microprocessor.

Xilinx Family

XC9500 CPLDs

Demonstrates

XC95108 device for high performance system applications.

Introduction

Today's modern computer systems have many different components. In addition to high-speed processors and system buses, the high performance system requires sophisticated interface logic and state machines. The need for this circuitry to support advanced system components is a main functional block of complete high performance systems. The XC95108 is an ideal solution for high performance system controllers. This application note outlines the use of state machines, address decoders and data path routing in support of high-performance systems.

A high performance system controller could implement any of the following features:

- Power-on logic
- System memory map decode
- DRAM state machine
- Flash memory state machine
- SDRAM state achine
- System peripheral interfaces
- Data path routing

The XC95108 can implement all of these functions. An outline of the functional requirements for each of the different interfaces follows. A typical system controller block diagram is shown in Figure 1.

Power-On Logic

A high performance system requires the proper start-up sequence for each different system circuit. The logic and power-up sequence of different components are an important element of the complete system design. Different components require reset and configuration, based on a predetermined power-up sequence. A power-up sequence might include some of the following functions:

- Reset signals
- Tristate data paths
- System clocks
- Control signals
- Self-test

Most of these functions are built with relatively few macrocells (2-10). The 5 volt in-system programmable capability of the XC95108 permits any future modification of the power-up sequence.

System Memory Map Decode

High performance systems require a memory map of all component accessible by the processor. System components are mapped into the address space based on their size and specific requirements. Most decode needs require wide fan-in, high speed (7 ns or less) and high current drive. The XC95108 delivers each of these requirements.

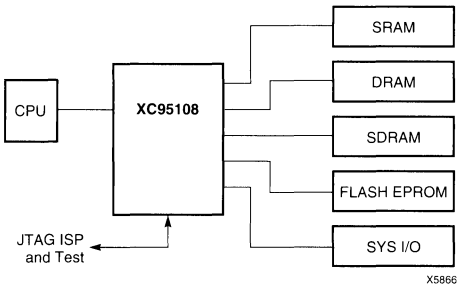


Figure 1. Typical High-Performance System Controller

The memory map function of the processor may require as many as ten macrocells. The memory map function also uses a large number of signal I/O pins. Memory decode may require as many as 40 signals pins. The ISP functionality of the XC95108 permits easy modification of the memory map.

DRAM State Machine

High performance systems include many different technologies. DRAM is the main memory type for todayís high performance systems. However, there are many different kinds of DRAM and each requires a different state machine.

The memory state machine usually performs the wait state generation and the refresh requirements of the interface. The DRAM controller also handles CAS and RAS generation.

The DRAM state machine may also require as many as ten macrocells. Another ten macrocells may be required for the remaining logic in the DRAM controller. A simple DRAM controller block diagram is shown in Figure 2.

Flash Memory Controller

An increasing number of high performance systems are being created with Flash memory devices. (See Figure 3). These non-volatile memory devices permit in-system modification. When configured as a Flash memory controller, the XC95108 responds to read, erase, and program commands and generates the corresponding control strobes. The controller also handles the address segmentation and data multiplexing.

SDRAM State Machine

High performance systems require a new type of DRAM called Synchronous DRAM (SDRAM). The SDRAM interface has a complex state machine that may require future modifications as SDRAM technologies evolve. SDRAM devices from different vendors use different commands and protocols.

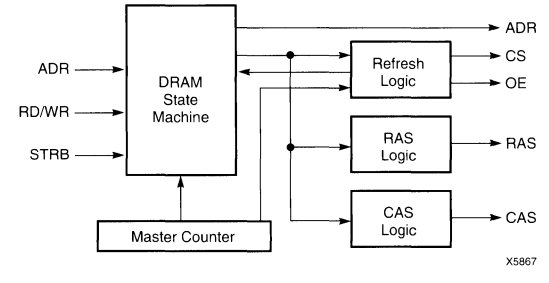


Figure 2. DRAM State Machine

The XC95108 permits modification of the SDRAM interface as a field upgrade. The interface requires about 15 macrocells and 20 signals. The SDRAM interface controls the address map segmentation and strobes for the high performance system.

System Peripheral Interfaces

System peripheral devices handle many functions of in high-performance systems. A fast system bus acts as the interface to the rest of the system. Peripheral Component Interconnect (PCI) is a high-speed bus supported by many vendors.

The XC95108 device is PCI compliant. The device could serve as either of a PCI bus target or a PCI bus initiator depending on the application requirements. The state machine for the bus functions requires between ten and twenty macrocells. The XC95108 may also form the data path and parity generation PCI functions.

Data Path Routing

Data path routing requirements of a high-performance system can be very significant. Many components of the system require different address and data signals. The assignment of the separate data and address bus signals to the components is a primary data path routing function.

The XC95108 is offered in multiple package and I/O combinations to deliver the necessary macrocells and signal pins. The JTAG ISP function allows in-system modification of data path routing.

Conclusions

The XC95108 can be used as a high-performance system controller. The requirements for these controllers are described in this application note. Details of specific counter, multiplexer, and data path building blocks are discussed in *Designing with XC9500 CPLDs.*

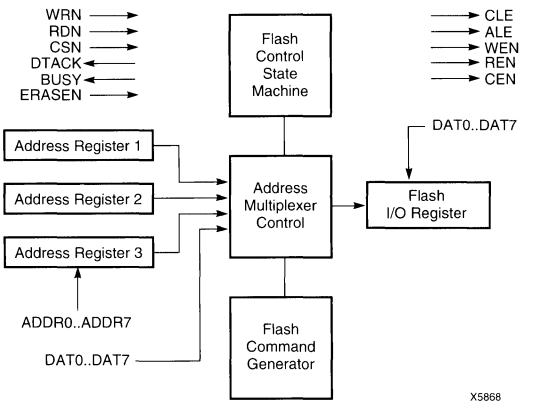


Figure 3. Flash Memory State Machine

XC95108 CPLD Serial Stream Interface

February 1996 — Application Note

Summary

The XC95108 is shown as a Serial Data Stream (SDS) application for datacom/telecom systems. Additionally, performance monitoring capabilities are outlined.

Xilinx Family

XC9500 CPLDs

Demonstrates

XC95108 device for datacom/telecom applications

XC95108 performance monitoring and remote field upgrade.

Introduction

Today's modern communications systems have many different SDS physical interfaces and components. The XC95108 is ideal for multiplexing and control of these different interfaces. This application note demonstrates the use of counters, shifters, and multiplexers in support of the SDS interface requirements.

Communications System Block Diagram

In all datacom/telecom systems, there are many different physical interface requirements and multiple system buses. The combination of the different interfaces and protocols is a main function of the system. Implementing a given interface, requires a physical electrical interface and a data framer for the protocol and transport layer processing of the SDS.

The connection of the physical interface circuit and framer to the rest of the system is done using a system data bus. The interface of different data streams into system data buses is an excellent application for the XC95108. A simple block diagram of some typical SDS XC95108 interfaces is shown in Figure 1.

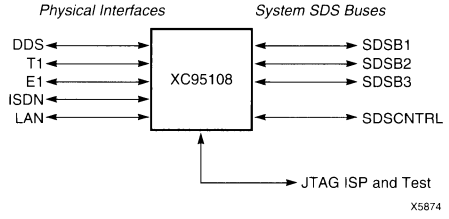


Figure 1. Typical SDS Interface

XC95108 SDS Application Example

A typical system requires a variety of different physical interfaces to be supported. Each physical interface circuit needs similar information related to the following:

- Channel boundary information
- Channel signaling Information
- Efficient CRC generation and checking
- Channel error conditions and status

SDS interfaces have some common characteristics. Each different interface processes the physical circuit and a framer. The framer removes encoding and embedded clock information. The I/O signals of the framer are divided into three categories:

- Channel data
- Channel control
- Signaling information

These signals are common to the different physical interface signals. The XC95108 interprets them to control SDS.

Different SDS Physical Interfaces

Direct Digital Service (DDS) is a simple 56/64 Kilobit/s digital interface for the simple digital terminal. This connection is typical for credit card verification, bank machines, and any other low bandwidth digital service requirement.

T1/E1 are the two main broad band interface bandwidths of the current digital telecom WAN hierarchy. The T1 interface is a 1.554 Megabit/s digital interface comprised of 24 x 64 Kilobit/s channels into a 125 uSecond frame. The E1 interface characteristics are 32 x 64 Kilobit/s channels into a 125 uSecond frame resulting in a bit rate of 2.56 Megabits/s.

Integrated Services Digital Network (ISDN) basic rate service is equivalent to 2 DDS service channels, each of 64 Kilobits/s, and a 16 Kilobits/s signaling channel. This service is frequently referred to as 2B+D or ISDN BRI.

Integrated Services Digital Network (ISDN) primary rate is the combination of 32 64 Kilobits/s channels similar to the E1 standard. This medium bandwidth wide area network interface allows integrated voice and data switching systems.

Ethernet is by far the most popular digital LAN physical interface standard. Current Ethernet is a 10 Megabits/s implementation over either coaxal or twisted copper pair cables. The 100 Megabits/s version of Ethernet is also available but not yet widely used.

Fiber Digital Data Interface (FDDI) is a 100 Megabits/s interface that has been increasing in popularity over the last few years. FDDI is best suited for LAN servers and high bandwidth data applications.

A Token Ring system of either 4 or 16 Megabits/s offers some new LAN system advantages over traditional Ethernet only backbone networks. An increase in the Token Ring switched network, connected to a high bandwidth backbone, is becoming more popular and will increase in the next few years.

Different Data Packet Standards

Each physical interface has the option of switching between different transport layer standards. The actual content and context of the data packets sent over a physical network link depends on the current standard being used. The need to support many different data packet formats will only increase with the expansion of new and diverse bearer services.

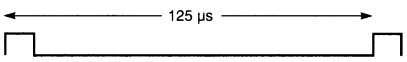
The physical interface is a small part of the complete functioning system. The data from the physical interface must be routed and processed by the correct protocol standard. The need to support future physical interface circuits and new standards requires flexible SDS interfaces.

T1/E1 System Upgrade Example

Current standard datacom/telecom SDS systems are increasing in complexity and capacity. Interface and framer circuits for different SDS formats are single channel device solutions. Dual and quad density SDS interface circuits will increase the complexity of the interface requiring more logic capacity.

The XC95108 is ideal for the previous system upgrade example. Consider the T1/E1 type interface circuit. The current single SDS interface of 1.554 and 2.048 MHz implements a set of logic functions for the system. The XC95108 requires a small amount logic capacity for counters, multiplexers, shifters, and state machines. When the interface is expanded to handle more streams, extra logic in the XC95108 is available. The appropriate data parameters are shown in Figure 2.

T1/E1 Data Rate Comparison



T1 - 1.554 Mbits/s - 192 Data + 1 Signal for each 125 µs Frame

E1 - 2.048 Mbits/s - 248 Data + 8 Signal for each 125 µs Frame

T1/E1 Signalling Protocol Comparison

T1-193E	T1-193S	E1
SF 6 Bit 8	SF 6 Bit 8	All Super Frames
SF 12 Bit 8	SF 12 Bit 8	Time Slot 16
SF 18 Bit 8		Bits 1-8
SF 24 Bit 8		

X5876

Figure 2. Performance Monitoring

XC95108 Performance Monitoring

The XC95108, as an SDS interface, allows for performance monitoring of the data content. Typical performance monitoring includes loop back testing, clear channel signaling and bit-error rate testing. These circuits require state machines, counters and pattern recognizers. The reconfigurability of the XC95108 "in-system", allows modification of the device to build these circuits. The required logic overhead is substantial. Device reconfiguration also eliminates the need for maintaining monitoring logic at all times. Figure 3 shows an additional performance monitoring port added to the SDS interface.

In addition to performance monitoring, the XC95108 may be remotely configured as any of the circuits. The choice of monitoring circuits can be made adaptively to suit the needs of the system administrator. The XC95108 JTAG circuitry permits in-system modification of the design by downloading changes as required.

Conclusions

The XC95108 meets all SDS interface requirements for datacom/telecom applications. With the XC95108 JTAG-based in-system programmable capability, users may easily build adaptive protocol data frame handlers. The XC95108 also handles built-in performance monitoring, thus eliminating the need for redundant circuitry in the design. Many of the building blocks described in this application note are discussed in more detail in *Designing with XC9500 CPLDs.*

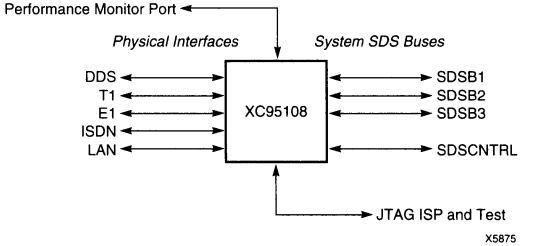


Figure 3. Performance Monitoring With XC95108

XILINX®

SECTION 3

XC9500 In-System Programmable CPLD Family

February 1996

Preliminary Product Information

Features

- High-performance
  - 5 ns pin-to-pin logic delays on all pins
  - f_{CNT} to 125 MHz
- Large density range
  - 36 to 288 macrocells with 800 to 6,400 usable gates
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced 0.6µm CMOS 5V FastFLASH technology

Description

The XC9500 CPLD family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members.

As shown in Table 1, the seven devices of the XC9500 family range in logic density from 800 to over 6,400 usable gates with 36 to 288 registers respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500 family is fully pin-compatible allowing easy design migration across multiple density options in a given package footprint.

The XC9500 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. An expanded JTAG instruction set allows version control of programming patterns and in-system debugging. In-system programming throughout the full device operating range and a minimum of 10,000 program/erase cycles provide worry-free reconfigurations and system field upgrades.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. I/Os may be configured for 3.3 V or 5 V operation. All outputs provide 24 mA drive.

Architecture Description

Each XC9500 device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with 36 inputs and 18 outputs. The FastCONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

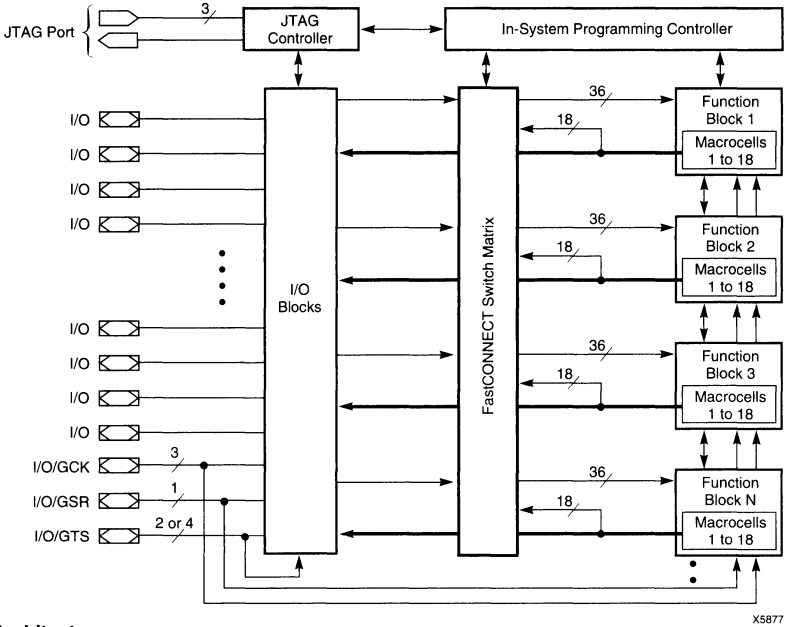


Figure 1. XC9500 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

Table 1. XC9500 Device Family

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288
Macrocells	36	72	108	144	180	216	288
Usable Gates	800	1,600	2,400	3,200	4,000	4,800	6,400
Registers	36	72	108	144	180	216	288
t_{PD} (ns)	5	7.5	7.5	7.5	10	10	10
t_{SU} (ns)	4.5	5.5	5.5	5.5	6.5	6.5	6.5
t_{CO} (ns)	4.5	5.5	5.5	5.5	6.5	6.5	6.5
f_{CNT} (MHz)	125	125	125	125	111	111	111
f_{SYSTEM} (MHz)	100	83	83	83	67	67	67

Note: f_{CNT} = Operating frequency for 16-bit counters

f_{SYSTEM} = Internal operating frequency for general purpose system designs spanning multiple FBs.

Table 2. Available Packages and Device I/O Pins

	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288
44-Pin PLCC	34						
44-Pin VQFP	34						
84-Pin PLCC		69	69				
100-Pin PQFP		72	81	81			
100-Pin TQFP		72	81				
160-Pin PQFP			108	133	133	133	
208-Pin HQFP					168	168	168

Note: Does not include the dedicated JTAG pins.

Function Block

Each Function Block as shown in Figure 2, is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Thirty-six inputs provide 72 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

Each FB supports local feedback paths that allow any number of FB outputs to drive into its own programmable AND-array without going outside the FB.

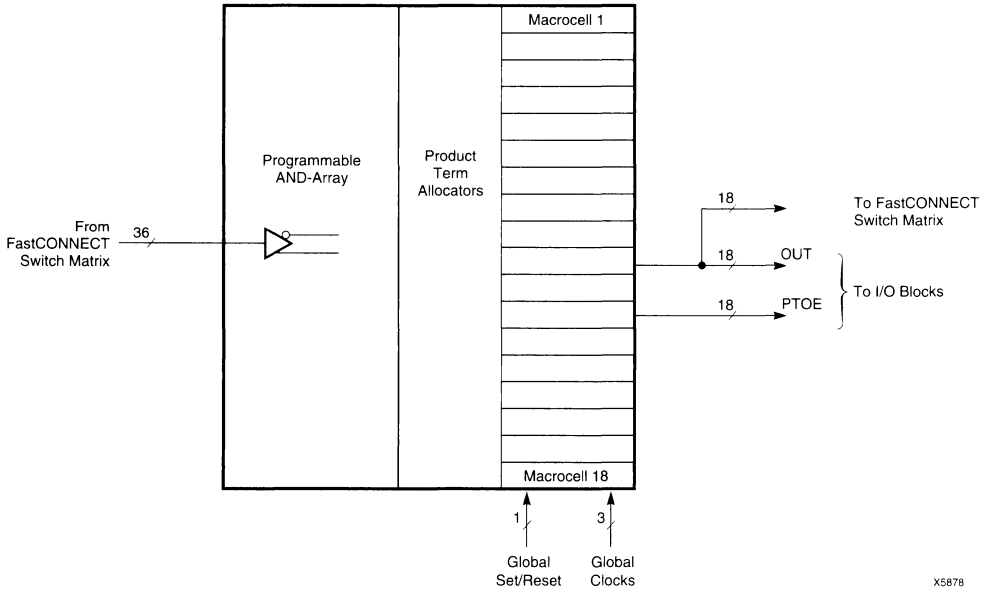


Figure 2. XC9500 Function Block

Macrocell

Each XC9500 macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, set/reset, and output enable. The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0).

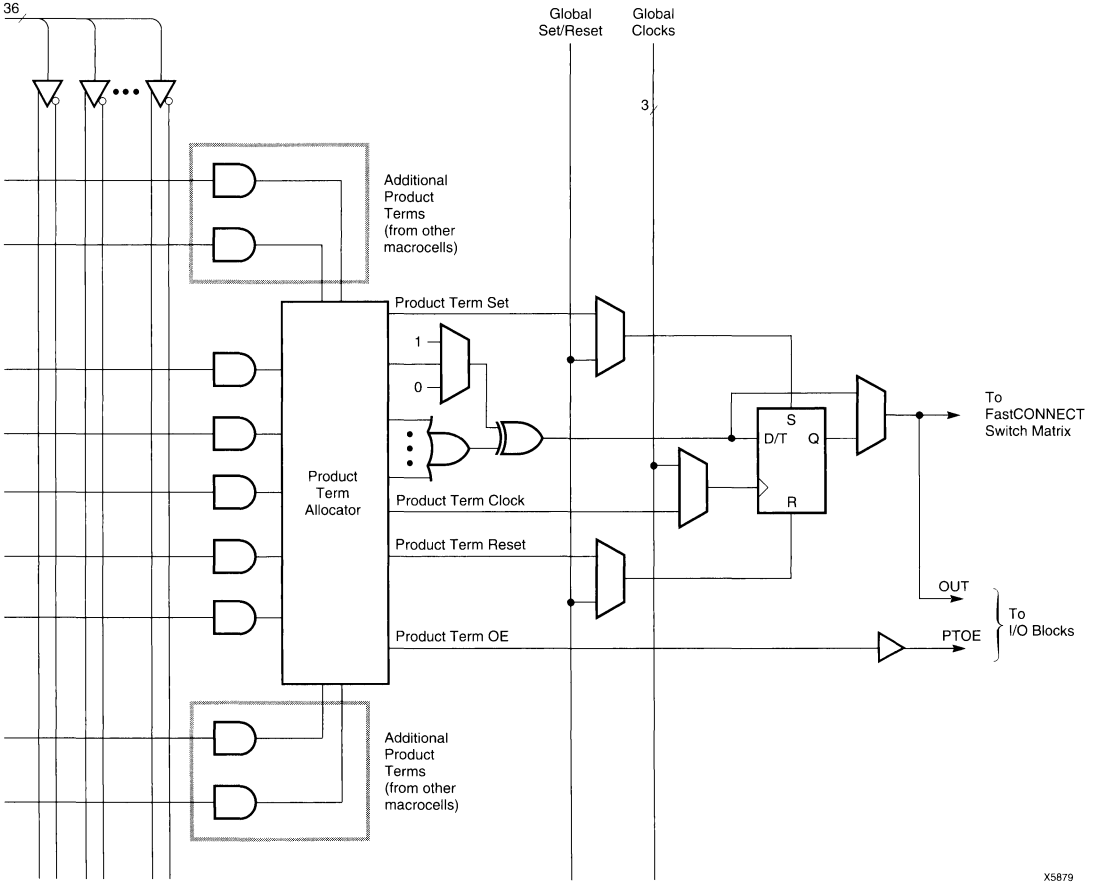


Figure 3. XC9500 Macrocell Within Function Block

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of a GCK pin can be used within the device. A GSR input is also provided to allow user registers to be set to a user-defined state.

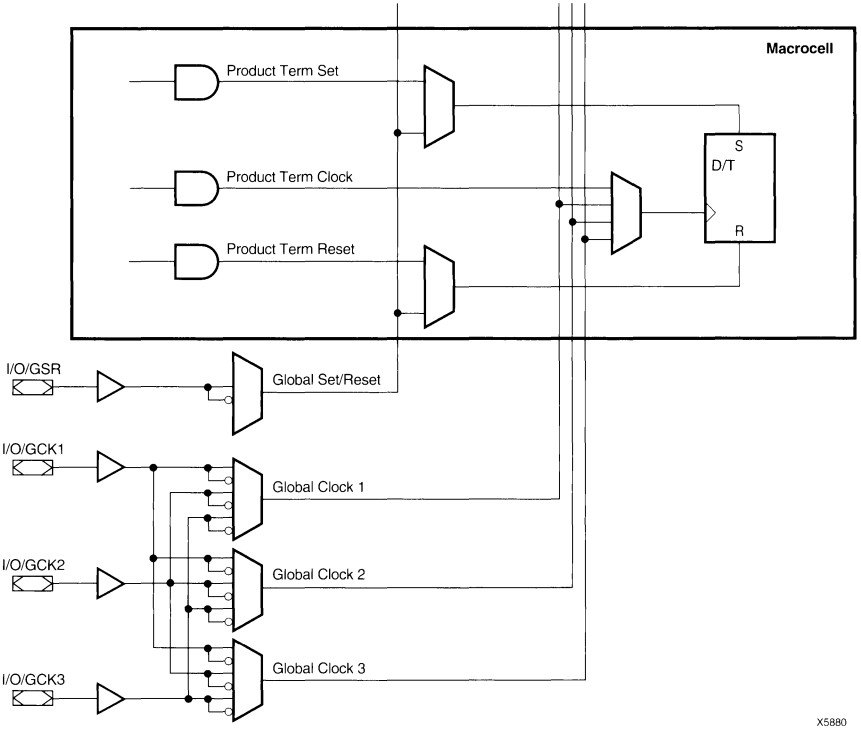


Figure 4. Macrocell Clock and Set/Reset Capability

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of t_{PTA}, as shown in Figure 6.

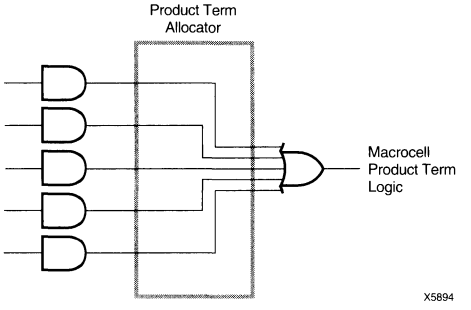


Figure 5. Macrocell Logic Using Direct Product Terms

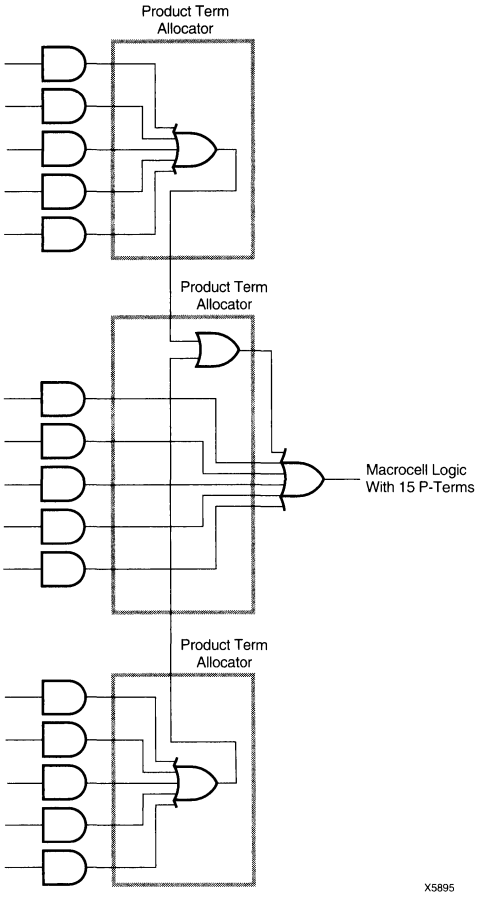


Figure 6. Product Term Allocation With 15 Product Terms

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7. In this example, the incremental delay is only $2 \cdot t_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8 \cdot t_{PTA}$.

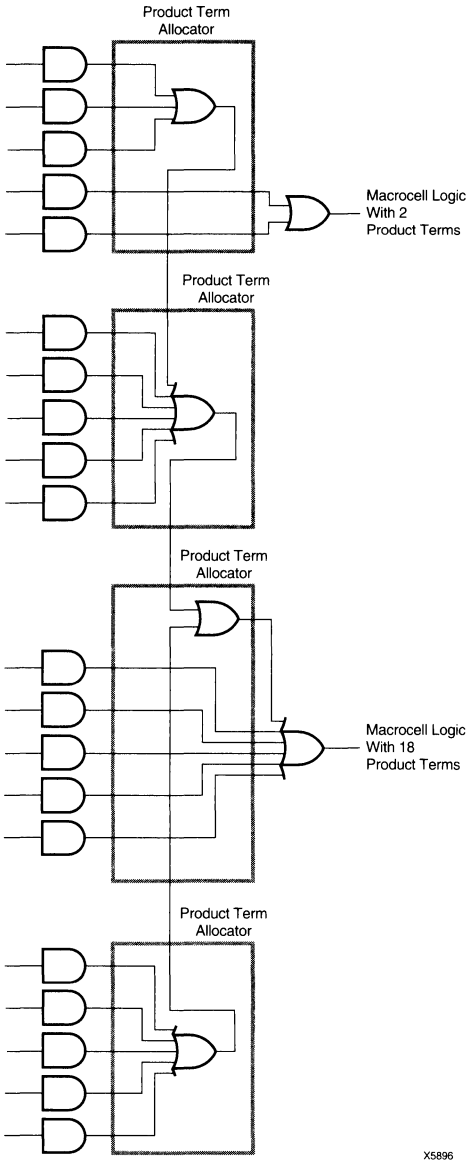


Figure 7. Product Term Allocation Over Several Macrocells

The internal logic of the product term allocator is shown in Figure 8.

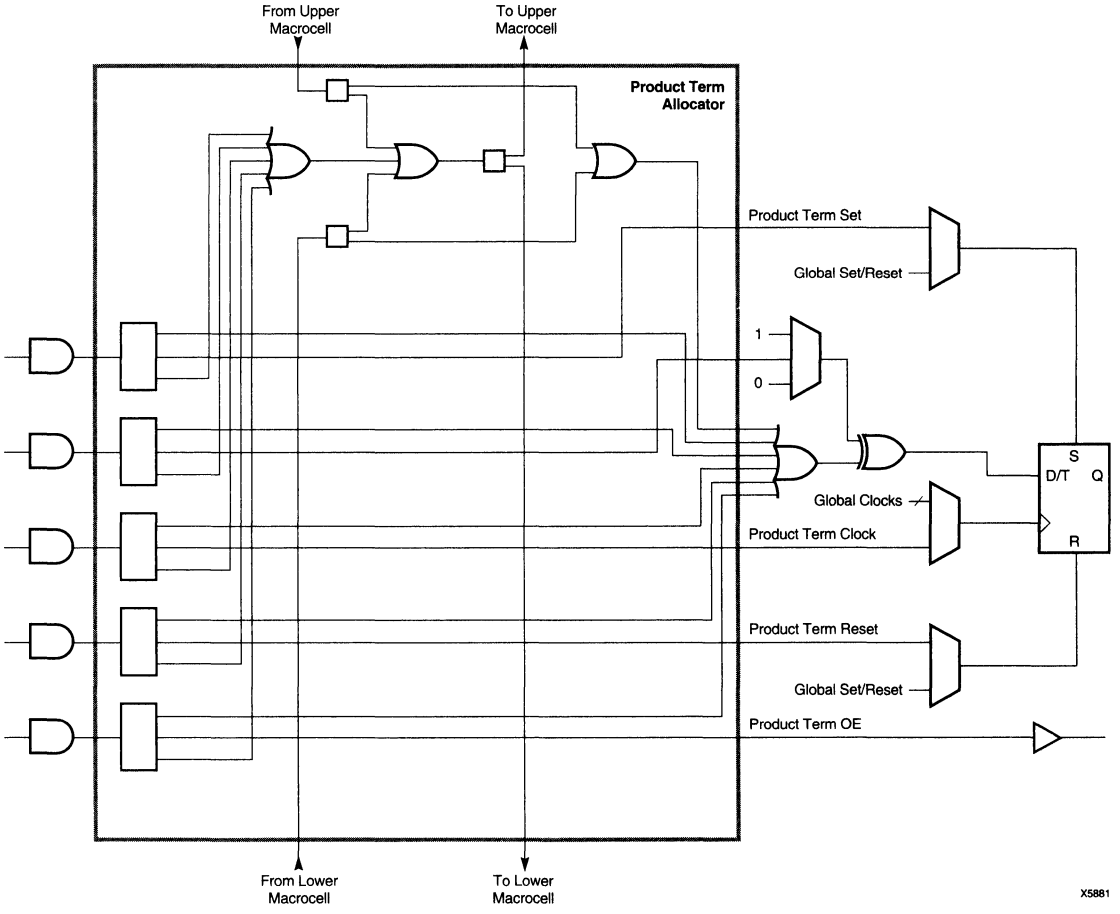


Figure 8. Product Term Allocator Logic

FastCONNECT Switch Matrix

The FastCONNECT switch matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT matrix. Any of these (up to a FB fan-in limit of 36) may be programmably selected to drive each FB with a uniform delay.

The FastCONNECT switch matrix is capable of combining multiple internal connections into a single wired-AND output before driving the destination FB. This provides additional logic capability and increases the effective logic fan-in of the destination FB without any additional timing delay. This capability is available for internal connections originating from FB outputs only. It is automatically invoked by the development software where applicable.

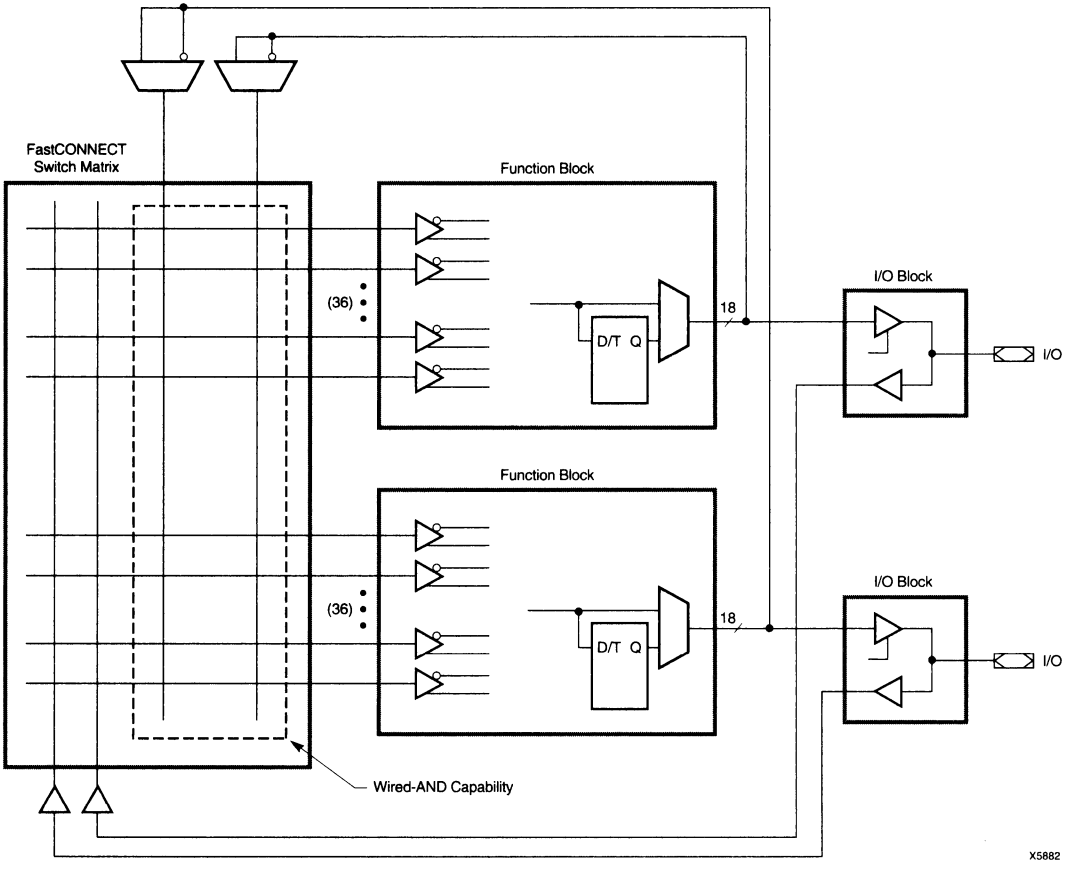


Figure 9. FastCONNECT Switch Matrix

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

The input buffer is compatible with standard 5 V CMOS, 5 V TTL and 3.3 V signal levels. The input buffer uses the internal 5 V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global OE signals, always "1", or always "0". There are two global output enables for devices with up to 144 macrocells, and four global output enables for devices with 180 or more macrocells. Both polarities of any of the global 3-state control (GTS) pins may be used within the device.

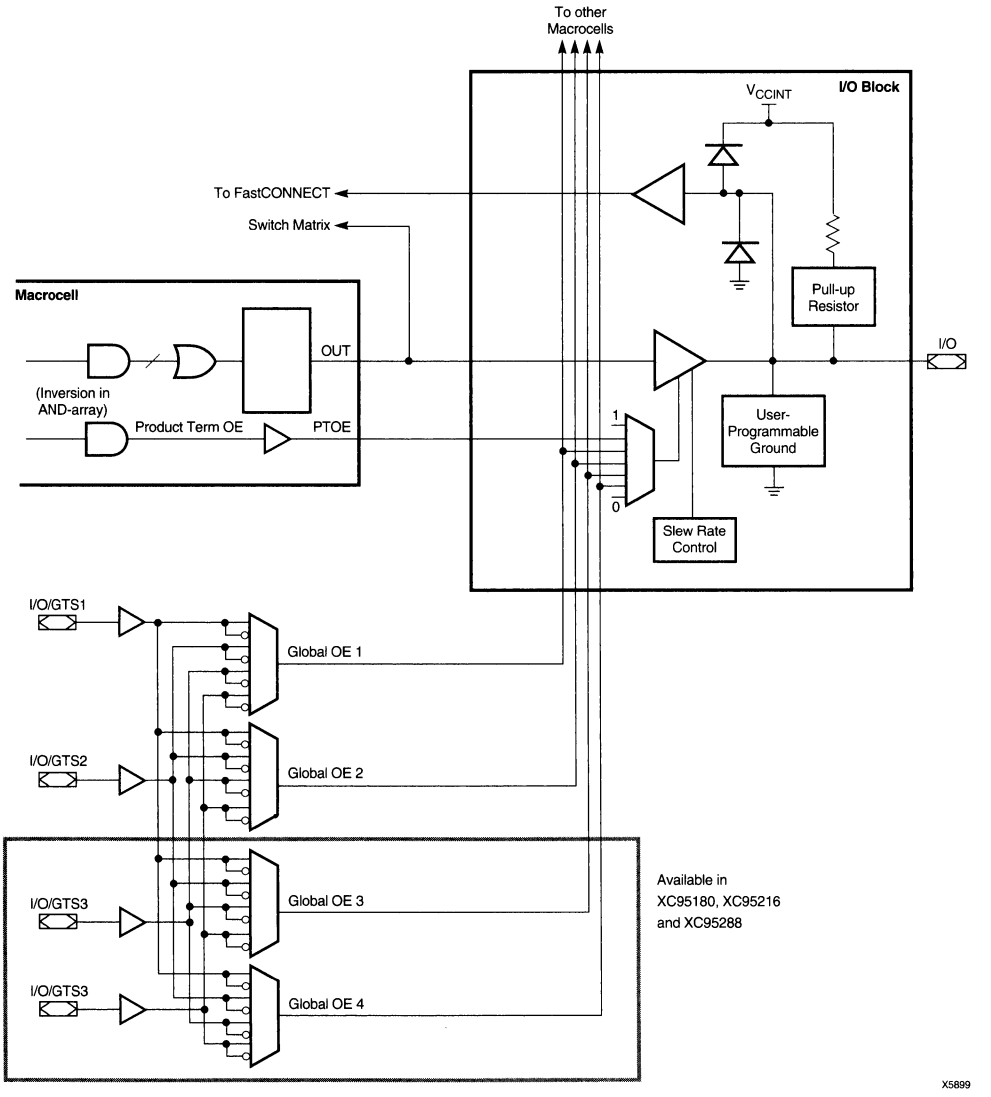


Figure 10. I/O Block and Output Enable Capability

Each output has independent slew rate control. Output edge rates may be programmably slowed down to reduce system noise (with an additional time delay of t_{SLEW}). See Figure 11.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins. By tying strategically located programmable ground pins to the external ground connection, system noise generated from large numbers of simultaneous switching outputs may be reduced.

A control pull-up resistor (typically 10K ohms) is attached to each device I/O pin to prevent device pins from floating when the device is not in normal user operation. This resistor is active during device programming mode and system power-up. It is also activated for an erased device. The resistor is deactivated during normal operation.

The output driver is capable of supplying 24 mA output drive. All output drivers in the device may be configured for either 5 V TTL levels or 3.3 V levels by connecting the device output voltage supply (V_{CCIO}) to a 5 V or 3.3 V voltage supply. Figure 12 shows how the XC9500 device can be used in 5 V only and mixed 3.3 V/5 V systems.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design changes depends on the ability of the architecture to adapt to unexpected changes. The XC9500 devices have architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500 provides 100% routing within the FastCONNECT switch matrix, and incorporates a flexible Function Block that allows block-wide allocation of available p-terms. This provides a high level of confidence of maintaining both input and output pin assignments for unexpected design changes.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments.

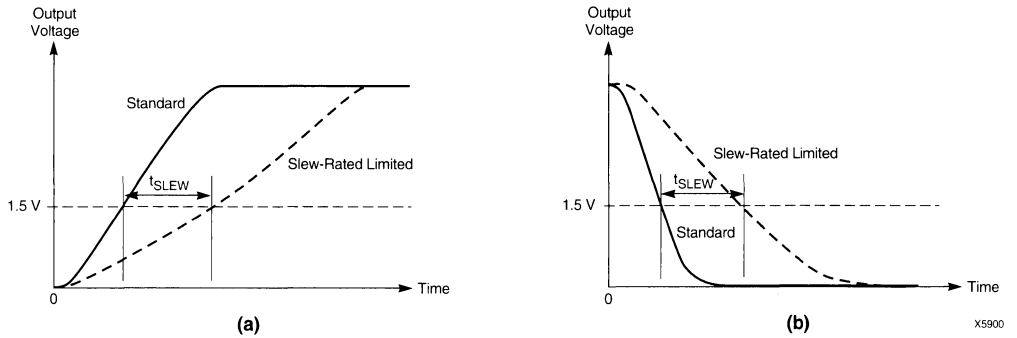


Figure 11. Output Slew-Rate Control For (a) Rising and (b) Falling Outputs

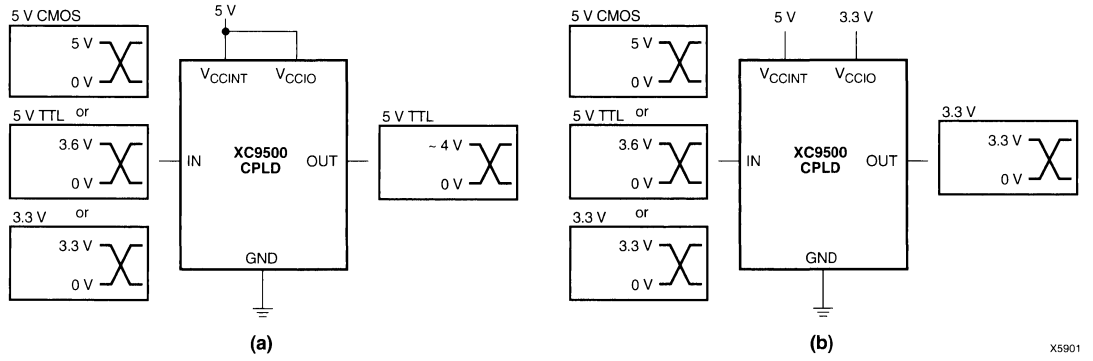


Figure 12. XC9500 Devices in (a) 5 V Systems and (b) Mixed 3.3 V/5 V Systems

In-System Programming

XC9500 devices are programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 13. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

The system designer must ensure that the system is well-behaved before the XC9500 device is programmed with a user pattern. During XC9500 programming, all I/Os are tri-stated and pulled-up.

XC9500 devices can also be programmed by third-party device programmers.

Endurance

All XC9500 CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500 devices fully support IEEE 1149.1 boundary-scan (JTAG). Extest, Sample/Preload, Bypass, Usercode, Intest, Idcode, and Highz instructions are supported in each device. All in-system programming, erase, and verify instructions are implemented as fully compliant extensions of the 1149.1 instruction set.

Refer to the application note on the XC9500 JTAG instruction set for additional information.

Design Security

XC9500 devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming by the user. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern.

Table 3. Data Security Options

Write Security	Read Security: Default	Read Security: Set
Default	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Allowed
Set	Read Allowed Program/Erase Inhibited	Read Inhibited Program/Erase Inhibited

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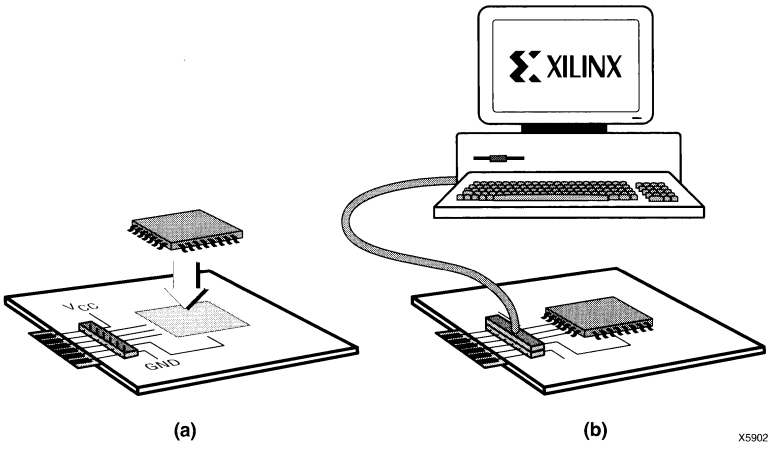


Figure 13. In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

Low Power Mode

All XC9500 devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (t_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500 architecture allows a simplified timing model for the entire device. The basic timing model is shown in Figure 14. Detailed timing information on a design, including secondary parameters, can be easily obtained from the timing report in the XACT*step* development system.

The basic timing model is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The Figure 6 example shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

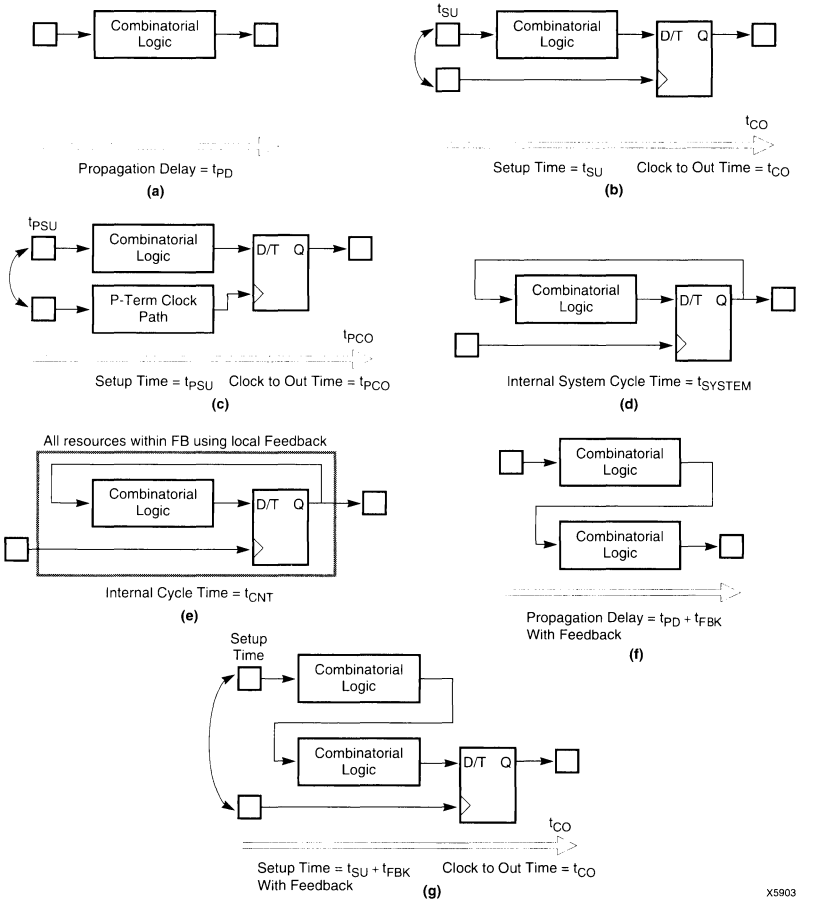


Figure 14. Basic Timing Model

Power-Up Characteristics

The XC9500 devices are well behaved under all operating conditions. During power-up each XC9500 device employs internal circuitry which keeps the device in the quiescent state until V_{CCINT} supply voltage is at a safe level (approximately 3.8 V). During this time, all device pins and JTAG pins are disabled, and all device outputs are disabled with the IOB pull-up resistors (~ 10K ohms) enabled. See Table 5. When the supply voltage reaches a safe level, all user registers become initialized (within 100 µs typical), and the device is immediately available for operation, as shown in Figure 15.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with the IOB pull-up resistors enabled. The JTAG pins are enabled to allow the device to be programmed at any time.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

In mixed 3.3 V/5 V systems, it is recommended that $V_{CCINT} \geq V_{CCIO}$ at all times during the power-up sequence.

XACT*step*™ Development System

The XC9500 CPLD family is fully supported by the Xilinx XACT*step* development system. The designer can create the design using ABEL, schematics, equations, VHDL or other HDL languages in a variety of software front-end tools. The XACT*step* development system can be used to implement the design and generate a JEDEC bitmap which can be used to program the XC9500 device. The XACT*step* development system includes JTAG download software that can be used to program the devices via a download cable.

FastFLASH Technology

An advanced 0.6 µm CMOS Flash process is used to fabricate all XC9500 devices. Specificially developed for Xilinx in-system programmable CPLDs, the process provides high performance logic capability and endurance of 10,000 program/erase cycles.

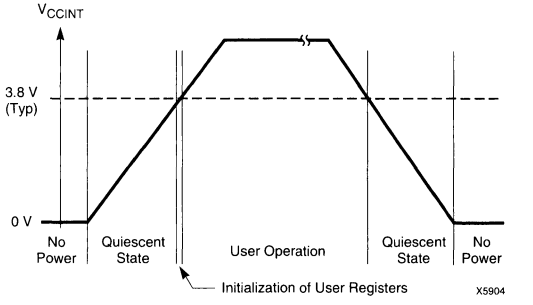


Figure 15. Device Behavior During Power-up

Table 4. Timing Model Parameters

Description	Parameter	Product Term Allocator[1]	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	t_{PD}	+ t_{PTA} * S	+ t_{LP}	+ t_{SLEW}
Global Clock Setup Time	t_{SU}	+ t_{PTA} * S	+ t_{LP}	–
Global Clock-to-output	t_{CO}	–	–	+ t_{SLEW}
Product Term Clock Setup Time	t_{PSU}	+ t_{PTA} * S	+ t_{LP}	–
Product Term Clock-to-output	t_{PCO}	–	–	+ t_{SLEW}
Internal System Cycle Period	t_{SYSTEM}	+ t_{PTA} * S	+ t_{LP}	–
Feedback Time	t_{FBK}	+ t_{PTA} * S	+ t_{LP}	–

Note (1) S = the logic span of the function, as defined in the text.

Table 5. XC9500 Device Characteristics

Device Feature	Quiescent State	Erased Device Operation	Valid User Operation
IOB Pull-up Resistors	Enabled	Enabled	Disabled
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

XC9536 In-System Programmable CPLD

February 1996

Preliminary Product Information

Features

- 5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 36 macrocells with 800 usable gates
- Up to 34 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 44-pin PLCC and 44-pin VQFP packages

Description

The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of two 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9536 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC9536 device.

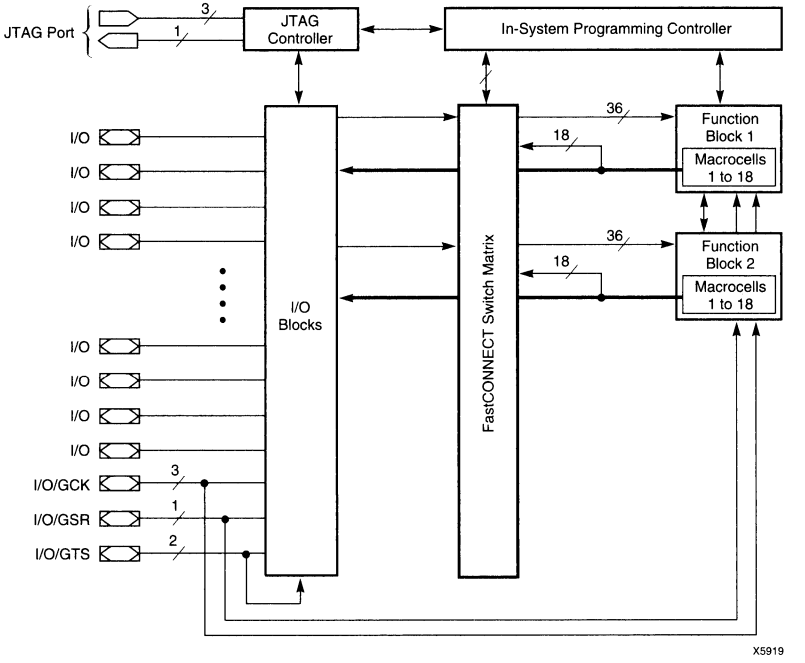


Figure 1. XC9536 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

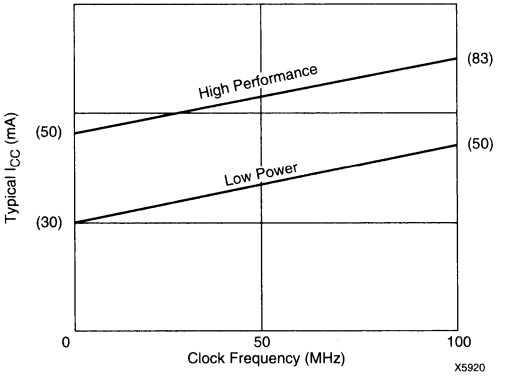


Figure 2. Typical I_{CC} vs Frequency For XC9536

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCINT} + 0.5	V
T_{IN}	Input signal transition time		50	ns

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

DC Characteristics Over Recommended Operating Conditions

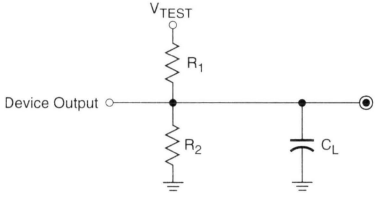
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	30 mA Typ		

AC Characteristics

Symbol	Parameter	XC9536-5		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		5.0		7.5		10		15	ns
t_{SU}	I/O setup time before GCK	4.5		5.5		6.5		8.0		ns
t_{H}	I/O hold time after GCK	0		0		0		0		ns
t_{CO}	GCK to output valid		4.5		5.5		6.5		8.0	ns
f_{CNT}	16-bit counter frequency	125		125		111.0		95.0		MHz
f_{SYSTEM} [2]	Multiple FB Internal Operating Frequency	100		83.0		67.0		55.0		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		0.5		1.0		2.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		5.0		5.5		6.0		ns
t_{PCO}	P-term clock to output valid		7.5		10.5		12.0		14.0	ns
t_{OE}	GTS to output valid		6.0		7.0		10.0		15.0	ns
t_{OD}	GTS to output disable		6.0		7.0		10.0		15.0	ns
t_{POE}	Product term OE to output valid		10.5		13.0		15.5		18.0	ns
t_{POD}	Product term OE to output disable		10.5		13.0		15.5		18.0	ns
t_{PTA}	Product term allocator delay		1.5		1.5		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		NA		8.5		12.0		17.0	ns
f_{WLH}	GCK pulse width	4.0		4.0		4.5		5.0		ns
t_{SLEW}	Slew rate time delay		3.5		4.0		4.5		5.5	ns
t_{LP}	Low power time delay adder		8.0		8.0		8.5		8.5	ns

Note 2. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.

Preliminary



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3. AC Load Circuit

XC9536 I/O Pins

Function Block	Macrocell	PC44	VQ44	BScan Order	Notes
1	1	2	40	105	
1	2	3	41	102	
1	3	5	43	99	[1]
1	4	4	42	96	
1	5	6	44	93	[1]
1	6	8	2	90	
1	7	7	1	87	[1]
1	8	9	3	84	
1	9	11	5	81	
1	10	12	6	78	
1	11	13	7	75	
1	12	14	8	72	
1	13	18	12	69	
1	14	19	13	66	
1	15	20	14	63	
1	16	22	16	60	
1	17	24	18	57	
1	18	–	–	54	

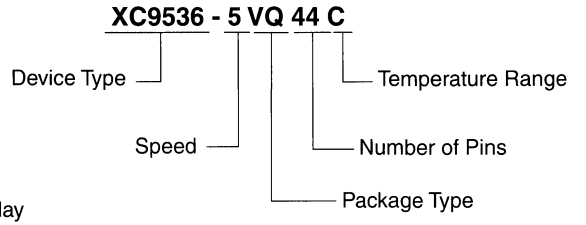
Function Block	Macrocell	PC44	VQ44	BScan Order	Notes
2	1	1	39	51	
2	2	44	38	48	
2	3	42	36	45	[1]
2	4	43	37	42	
2	5	40	34	39	[1]
2	6	39	33	36	[1]
2	7	38	32	33	
2	8	37	31	30	
2	9	36	30	27	
2	10	35	29	24	
2	11	34	28	21	
2	12	33	27	18	
2	13	29	23	15	
2	14	28	22	12	
2	15	27	21	9	
2	16	26	20	6	
2	17	25	19	3	
2	18	–	–	0	

Note: [1] Global control pin

XC9536 Global, JTAG and Power Pins

Pin Type	PC44	VQ44
I/O/GCK1	5	43
I/O/GCK2	6	44
I/O/GCK3	7	1
I/O/GTS1	42	36
I/O/GTS2	40	34
I/O/GSR	39	33
TCK	17	11
TDI	15	9
TDO	30	24
TMS	16	10
V_{CCINT} 5 V	21,41	15,35
V_{CCIO} 3.3 V/5 V	32	26
GND	23,10,31	17,4,25

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay
-5	5 ns pin-to-pin delay

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier (PLCC)
VQ44	44-Pin Very Thin Quad Flat Pack (VQFP)

Component Availability

Pins		44		84	100		160	208
Type		Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code		PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC9536	-15	C(I)	C(I)					
	-10	C(I)	C(I)					
	-7	C	C					
	-5	C	C					

X5907

XC9572 In-System Programmable CPLD

February 1996

Advance Product Information

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

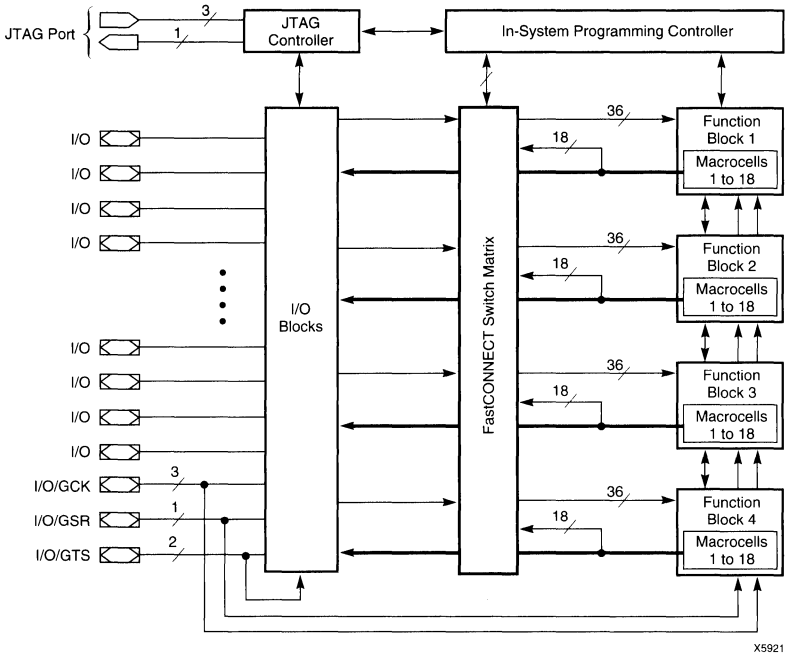


Figure 1. XC9572 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC9572 I/O Pins

Function Block	Macrocell	PQ100	PC84	BScan Order	Notes
1	1	18	4	213	
1	2	15	1	210	
1	3	20	6	207	
1	4	22	7	204	
1	5	16	2	201	
1	6	17	3	198	
1	7	27	11	195	
1	8	19	5	192	
1	9	24	9	189	[1]
1	10	30	13	186	
1	11	25	10	183	[1]
1	12	35	18	180	
1	13	38	20	177	
1	14	29	12	174	[1]
1	15	31	14	171	
1	16	41	23	168	
1	17	32	15	165	
1	18	42	24	162	
2	1	89	63	159	
2	2	96	69	156	
2	3	93	67	153	
2	4	95	68	150	
2	5	97	70	147	
2	6	98	71	144	
2	7	5	76	141	[1]
2	8	99	72	138	
2	9	1	74	135	[1]
2	10	3	75	132	
2	11	6	77	129	[1]
2	12	8	79	126	
2	13	10	80	123	
2	14	11	81	120	
2	15	13	83	117	
2	16	12	82	114	
2	17	14	84	111	
2	18	94	–	108	
3	1	43	25	105	
3	2	34	17	102	
3	3	51	31	99	
3	4	52	32	96	
3	5	37	19	93	
3	6	55	34	90	
3	7	56	35	87	
3	8	39	21	84	
3	9	44	26	81	
3	10	62	40	78	
3	11	54	33	75	
3	12	63	41	72	
3	13	65	43	69	
3	14	57	36	66	
3	15	58	37	63	
3	16	67	45	60	
3	17	60	39	57	
3	18	61	–	54	
4	1	68	46	51	
4	2	66	44	48	
4	3	73	51	45	
4	4	74	52	42	
4	5	69	47	39	
4	6	78	54	36	
4	7	79	55	33	
4	8	70	48	30	
4	9	72	50	27	
4	10	83	57	24	
4	11	76	53	21	
4	12	84	58	18	
4	13	87	61	15	
4	14	80	56	12	
4	15	91	65	9	
4	16	88	62	6	
4	17	92	66	3	
4	18	81	–	0	

Notes: [1] Global control pin

Contact factory for TQ100 pinouts

XC9572 Global, JTAG and Power Pins

Pin Type	PC84	PQ100
I/O/GCK1	9	24
I/O/GCK2	10	25
I/O/GCK3	12	29
I/O/GTS1	76	5
I/O/GTS2	77	6
I/O/GSR	74	1
TCK	30	50
TDI	28	47
TDO	59	85
TMS	29	49
V_{CCINT} 5 V	38,73,78	7,59,100
V_{CCIO} 3.3 V/5 V	22,64	28,40,53,90
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86

XC95108 In-System Programmable CPLD

February 1996

Preliminary Product Information

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 108 macrocells with 2400 usable gates
- Up to 108 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 84-pin PLCC, 100-pin PQFP, 100-pin TQFP and 160-pin PQFP packages

Description

The XC95108 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of six 36V18 Function Blocks, providing 2,400 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95108 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC95108 device.

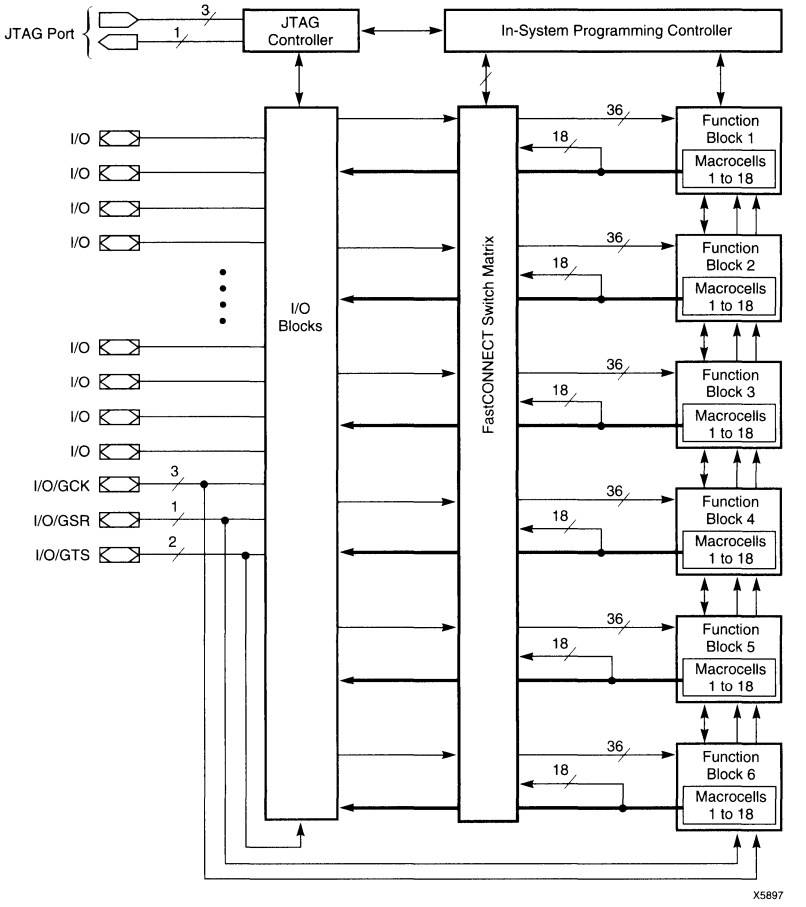


Figure 1. XC95108 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

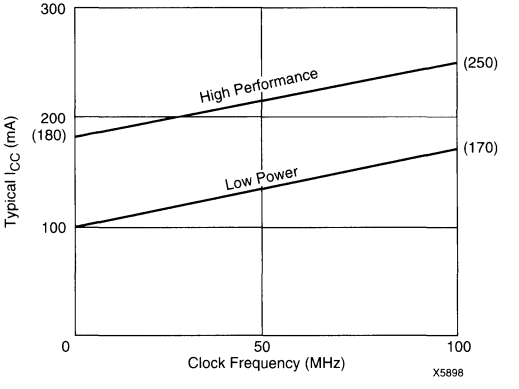


Figure 2. Typical I_{CC} vs Frequency For XC95108

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCINT} + 0.5	V
T_{IN}	Input signal transition time		50	ns

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

DC Characteristics Over Recommended Operating Conditions

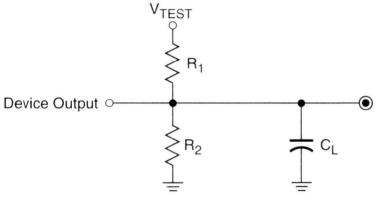
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	100 mA Typ		

AC Characteristics

Symbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		7.5		10		15		20	ns
t_{SU}	I/O setup time before GCK	5.5		6.5		8.0		10.0		ns
t_{H}	I/O hold time after GCK	0		0		0		0		ns
t_{CO}	GCK to output valid		5.5		6.5		8.0		10.0	ns
f_{CNT}	16-bit counter frequency	125		111		95.0		83.0		MHz
f_{SYSTEM} [2]	Multiple FB Internal Operating Frequency	83.0		67.0		55.0		50.0		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		1.0		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	5.0		5.5		6.0		6.0		ns
t_{PCO}	P-term clock to output valid		10.5		12.0		14.0		16.0	ns
t_{OE}	GTS to output valid		7.0		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		7.0		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output valid		13.0		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disable		13.0		15.5		18.0		22.0	ns
t_{PTA}	Product term allocator delay		1.5		2.0		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		8.5		12.0		17.0		20.0	ns
f_{WLH}	GCK pulse width	4.0		4.5		5.0		6.0		ns
t_{SLEW}	Slew rate time delay		4.0		4.5		5.0		5.5	ns
t_{LP}	Low power time delay adder		8.0		8.5		8.5		8.5	ns

Note 2. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.

Preliminary



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3. AC Load Circuit

XC95108 I/O Pins

Function Block	Macrocell	PC84	PQ100	PQ160	BScan Order	Notes
1	1	–	–	25	321	
1	2	1	15	21	318	
1	3	2	16	22	315	
1	4	–	21	29	312	
1	5	3	17	23	309	
1	6	4	18	24	306	
1	7	–	–	27	303	
1	8	5	19	26	300	
1	9	6	20	28	297	
1	10	–	26	36	294	
1	11	7	22	30	291	
1	12	9	24	33	288	[1]
1	13	–	–	34	285	
1	14	10	25	35	282	[1]
1	15	11	27	37	279	
1	16	12	29	42	276	[1]
1	17	13	30	44	273	
1	18	–	–	43	270	
2	1	–	–	158	267	
2	2	71	98	154	264	
2	3	72	99	156	261	
2	4	–	4	4	258	
2	5	74	1	159	255	[1]
2	6	75	3	2	252	
2	7	–	–	9	249	
2	8	76	5	6	246	[1]
2	9	77	6	8	243	[1]
2	10	–	9	12	240	
2	11	79	8	11	237	
2	12	80	10	13	234	
2	13	–	–	14	231	
2	14	81	11	15	228	
2	15	82	12	17	225	
2	16	83	13	18	222	
2	17	84	14	19	219	
2	18	–	–	16	216	
3	1	–	–	45	213	
3	2	14	31	47	210	
3	3	15	32	49	207	
3	4	–	36	57	204	
3	5	17	34	54	201	
3	6	18	35	56	198	
3	7	–	–	50	195	
3	8	19	37	58	192	
3	9	20	38	59	189	
3	10	–	45	69	186	
3	11	21	39	60	183	
3	12	23	41	62	180	
3	13	–	–	52	177	
3	14	24	42	63	174	
3	15	25	43	64	171	
3	16	26	44	68	168	
3	17	31	51	77	165	
3	18	–	–	74	162	
4	1	–	–	123	159	
4	2	57	83	134	156	
4	3	58	84	135	153	
4	4	–	82	133	150	
4	5	61	87	138	147	
4	6	62	88	139	144	
4	7	–	–	128	141	
4	8	63	89	140	138	
4	9	65	91	142	135	
4	10	–	–	147	132	
4	11	66	92	143	129	
4	12	67	93	144	126	
4	13	–	–	153	123	
4	14	68	95	146	120	
4	15	69	96	148	117	
4	16	–	94	145	114	
4	17	70	97	152	111	
4	18	–	–	155	108	

Notes: [1] Global control pin

Contact factory for TQ100 pinouts

XC95108 I/O Pins (continued)

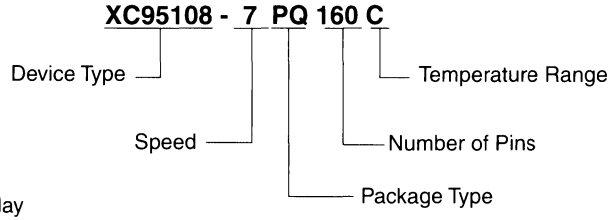
Function Block	Macrocell	PC84	PQ100	PQ160	BScan Order	Notes
5	1	–	–	76	105	
5	2	32	52	79	102	
5	3	33	54	82	99	
5	4	–	48	72	96	
5	5	34	55	86	93	
5	6	35	56	88	90	
5	7	–	–	78	87	
5	8	36	57	90	84	
5	9	37	58	92	81	
5	10	–	–	84	78	
5	11	39	60	95	75	
5	12	40	62	97	72	
5	13	–	–	87	69	
5	14	41	63	98	66	
5	15	43	65	101	63	
5	16	–	61	96	60	
5	17	44	66	102	57	
5	18	–	–	89	54	

Function Block	Macrocell	PC84	PQ100	PQ160	BScan Order	Notes
6	1	–	–	91	51	
6	2	45	67	103	48	
6	3	46	68	104	45	
6	4	–	75	116	42	
6	5	47	69	106	39	
6	6	48	70	108	36	
6	7	–	–	105	33	
6	8	50	72	111	30	
6	9	51	73	113	27	
6	10	–	–	107	24	
6	11	52	74	115	21	
6	12	53	76	117	18	
6	13	–	–	112	15	
6	14	54	78	122	12	
6	15	55	79	124	9	
6	16	–	81	129	6	
6	17	56	80	126	3	
6	18	–	–	114	0	

XC95108 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	PQ160
I/O/GCK1	9	24	33
I/O/GCK2	10	25	35
I/O/GCK3	12	29	42
I/O/GTS1	76	5	6
I/O/GTS2	77	6	8
I/O/GSR	74	1	159
TCK	30	50	75
TDI	28	47	71
TDO	59	85	136
TMS	29	49	73
V_{CCINT} 5 V	38,73,78	7,59,100	10,46,94,157
V_{CCIO} 3.3 V/5 V	22,64	28,40,53,90	1,41,61,81,121,141
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	20,31,40,51,70,80,99
GND	–	–	100,110,120,127,137
GND	–	–	160

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay

Packaging Options

PC84	84-Pin Plastic Leaded Chip Carrier (PLCC)
PQ100	100-Pin Plastic Quad Flat Pack (PQFP)
TQ100	100-Pin Thin Quad Flat Pack (TQFP)
PQ160	160-Pin Plastic Quad Flat Pack (PQFP)

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

Component Availability

Pins	44		84	100		160	208
Type	Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code	PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC95108 -20			C(I)	C(I)	C(I)	C(I)	
XC95108 -15			C(I)	C(I)	C(I)	C(I)	
XC95108 -10			C(I)	C(I)	C(I)	C(I)	
XC95108 -7			C	C	C	C	

X5941

XC95144 In-System Programmable CPLD

February 1996

Advance Product Information

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 100-pin PQFP, and 160-pin PQFP packages

Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

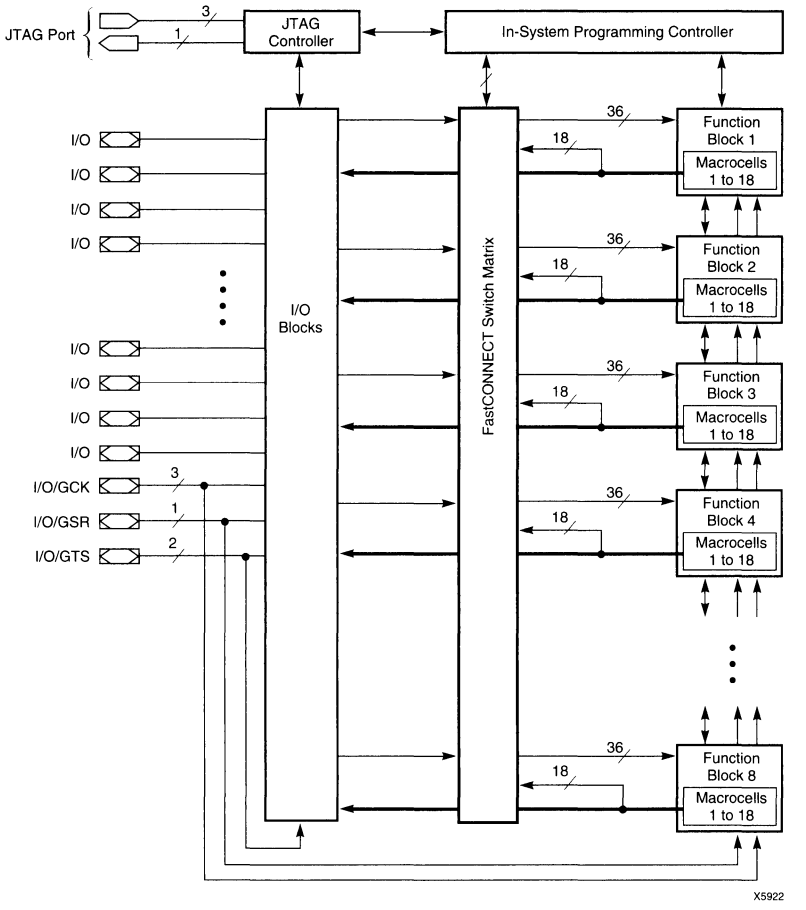


Figure 1. XC95144 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95144 I/O Pins

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
1	1	–	38	429	
1	2	15	21	426	
1	3	16	22	423	
1	4	–	25	420	
1	5	17	23	417	
1	6	18	24	414	
1	7	–	32	411	
1	8	19	26	408	
1	9	20	28	405	
1	10	–	74	402	
1	11	21	29	399	
1	12	22	30	396	
1	13	–	39	393	
1	14	24	33	390	[1]
1	15	25	35	387	[1]
1	16	–	78	384	
1	17	26	36	381	
1	18	–	–	378	
2	1	–	3	375	
2	2	4	4	372	[1]
2	3	–	147	369	
2	4	–	158	366	
2	5	5	6	363	[1]
2	6	6	8	360	[1]
2	7	–	7	357	
2	8	8	11	354	
2	9	9	12	351	
2	10	–	155	348	
2	11	10	13	345	
2	12	11	15	342	
2	13	–	5	339	
2	14	12	17	336	
2	15	13	18	333	
2	16	–	105	330	
2	17	14	19	327	
2	18	–	–	324	
3	1	–	53	321	
3	2	27	37	318	
3	3	–	84	315	
3	4	–	45	312	
3	5	29	42	309	[1]
3	6	30	44	306	
3	7	–	48	303	
3	8	31	47	300	
3	9	32	49	297	
3	10	–	89	294	
3	11	34	54	291	
3	12	35	56	288	
3	13	–	55	285	
3	14	36	57	282	
3	15	37	58	279	
3	16	–	34	276	
3	17	38	59	273	
3	18	–	–	270	
4	1	–	149	267	
4	2	92	143	264	
4	3	–	107	261	
4	4	–	123	258	
4	5	93	144	255	
4	6	94	145	252	
4	7	–	151	249	
4	8	95	146	246	
4	9	96	148	243	
4	10	–	114	240	
4	11	97	152	237	
4	12	98	154	234	
4	13	–	150	231	
4	14	99	156	228	
4	15	1	159	225	[1]
4	16	–	14	222	
4	17	3	2	219	[1]
4	18	–	–	216	

Notes: [1] Global control pin

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95144 I/O Pins (continued)

Function Block	Macrocell	PQ100	PQ160	BScan Order	Notes
5	1	–	65	213	
5	2	39	60	210	
5	3	–	27	207	
5	4	–	76	204	
5	5	41	62	201	
5	6	42	63	198	
5	7	–	67	195	
5	8	43	64	192	
5	9	44	68	189	
5	10	–	93	186	
5	11	45	69	183	
5	12	48	72	180	
5	13	–	66	177	
5	14	51	77	174	
5	15	52	79	171	
5	16	–	52	168	
5	17	54	82	165	
5	18	–	–	162	
6	1	–	–	159	
6	2	79	124	156	
6	3	–	9	153	
6	4	–	91	150	
6	5	80	126	147	
6	6	81	129	144	
6	7	–	131	141	
6	8	82	133	138	
6	9	83	134	135	
6	10	–	130	132	
6	11	84	135	129	
6	12	87	138	126	
6	13	–	132	123	
6	14	88	139	120	
6	15	89	140	117	
6	16	–	153	114	
6	17	91	142	111	
6	18	–	–	108	
7	1	–	–	105	
7	2	55	86	102	
7	3	–	50	99	
7	4	–	43	96	
7	5	56	88	93	
7	6	57	90	90	
7	7	–	83	87	
7	8	58	92	84	
7	9	60	95	81	
7	10	–	109	78	
7	11	61	96	75	
7	12	62	97	72	
7	13	–	85	69	
7	14	63	98	66	
7	15	65	101	63	
7	16	–	87	60	
7	17	66	102	57	
7	18	–	–	54	
8	1	–	–	51	
8	2	67	103	48	
8	3	–	128	45	
8	4	–	16	42	
8	5	68	104	39	
8	6	69	106	36	
8	7	–	118	33	
8	8	70	108	30	
8	9	72	111	27	
8	10	–	125	24	
8	11	73	113	21	
8	12	74	115	18	
8	13	–	119	15	
8	14	75	116	12	
8	15	76	117	9	
8	16	–	112	6	
8	17	78	122	3	
8	18	–	–	0	

XC95144 Global, JTAG and Power Pins

Pin Type	PQ100	PQ160
I/O/GCK1	24	33
I/O/GCK2	25	35
I/O/GCK3	29	42
I/O/GTS1	5	6
I/O/GTS2	6	8
I/O/GTS3	3	2
I/O/GTS4	4	4
I/O/GSR	1	159
TCK	50	75
TDI	47	71
TDO	85	136
TMS	49	73
V_{CCINT} 5 V	7,59,100	10,46,94,157
V_{CCIO} 3.3 V/5 V	28,40,53,90	1,41,61,81,121,141
GND	2,23,33,46,64,71, 77,86	20,31,40,51,70,80, 99,100,110,120,127, 137,160

XC95180 In-System Programmable CPLD

February 1996

Advance Product Information

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 180 macrocells with 4,000 usable gates
- Up to 168 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 160-pin PQFP, and 208-pin HQFP packages

Description

The XC95180 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of ten 36V18 Function Blocks, providing 4,000 usable gates with propagation delays of 10 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95180 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

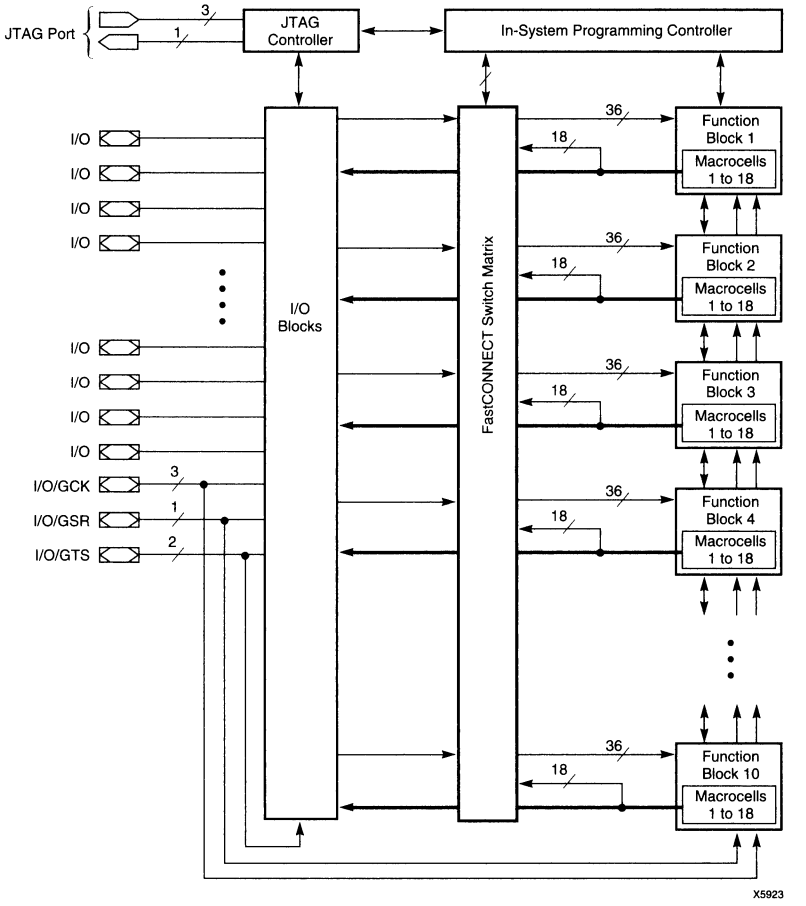


Figure 1. XC95180 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95180 I/O Pins

Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes
1	1	39	–	537	
1	2	30	22	534	
1	3	31	23	531	
1	4	32	24	528	
1	5	33	25	525	
1	6	34	26	522	
1	7	40	–	519	
1	8	35	27	516	
1	9	36	28	513	
1	10	37	29	510	
1	11	38	30	507	
1	12	43	32	504	
1	13	41	–	501	
1	14	44	33	498	[1]
1	15	45	34	495	
1	16	46	35	492	[1]
1	17	47	36	489	
1	18	–	–	486	
2	1	14	–	483	
2	2	7	6	480	[1]
2	3	8	7	477	
2	4	9	8	474	[1]
2	5	10	9	471	
2	6	15	11	468	
2	7	28	–	465	
2	8	16	12	462	
2	9	17	13	459	
2	10	18	14	456	
2	11	19	15	453	
2	12	20	16	450	
2	13	29	–	447	
2	14	21	17	444	
2	15	22	18	441	
2	16	23	19	438	
2	17	25	21	435	
2	18	–	–	432	

Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes
3	1	48	–	429	
3	2	49	37	426	
3	3	50	38	423	
3	4	51	39	420	
3	5	55	42	417	[1]
3	6	56	43	414	
3	7	54	–	411	
3	8	57	44	408	
3	9	58	45	405	
3	10	60	47	402	
3	11	61	48	399	
3	12	63	49	396	
3	13	62	–	393	
3	14	64	50	390	
3	15	70	52	387	
3	16	71	53	384	
3	17	74	56	381	
3	18	–	–	387	
4	1	196	–	375	
4	2	194	150	372	
4	3	197	151	369	
4	4	198	152	366	
4	5	199	153	363	
4	6	200	154	360	
4	7	203	–	357	
4	8	201	155	354	
4	9	202	156	351	
4	10	208	–	348	
4	11	205	158	345	
4	12	206	159	342	[1]
4	13	12	–	339	
4	14	3	2	336	[1]
4	15	4	3	333	
4	16	5	4	330	[1]
4	17	6	5	327	
4	18	–	–	324	

Notes: [1] Global control pin

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95180 I/O Pins (continued)

Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes
5	1	66	–	321	
5	2	72	54	318	
5	3	73	55	315	
5	4	75	57	312	
5	5	76	58	309	
5	6	77	59	306	
5	7	67	–	303	
5	8	78	60	300	
5	9	82	62	297	
5	10	69	–	294	
5	11	83	63	291	
5	12	84	64	288	
5	13	80	–	285	
5	14	85	65	282	
5	15	86	66	279	
5	16	87	67	276	
5	17	88	68	273	
5	18	–	–	270	
6	1	169	–	267	
6	2	174	134	264	
6	3	175	135	261	
6	4	178	138	258	
6	5	179	139	255	
6	6	180	140	252	
6	7	183	–	249	
6	8	182	142	246	
6	9	185	143	243	
6	10	189	–	240	
6	11	186	144	237	
6	12	187	145	234	
6	13	195	–	231	
6	14	188	146	228	
6	15	191	147	225	
6	16	192	148	222	
6	17	193	149	219	
6	18	–	–	216	

Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes
7	1	90	–	213	
7	2	89	69	210	
7	3	95	72	207	
7	4	97	74	204	
7	5	99	76	201	
7	6	100	77	198	
7	7	91	–	195	
7	8	102	78	192	
7	9	103	79	189	
7	10	101	–	186	
7	11	110	82	183	
7	12	111	83	180	
7	13	106	–	177	
7	14	112	84	174	
7	15	113	85	171	
7	16	114	86	168	
7	17	115	87	165	
7	18	–	–	162	
8	1	144	–	159	
8	2	154	118	156	
8	3	155	119	153	
8	4	158	122	150	
8	5	159	123	147	
8	6	160	124	144	
8	7	151	–	141	
8	8	161	125	138	
8	9	162	126	135	
8	10	165	–	132	
8	11	164	128	129	
8	12	166	129	126	
8	13	168	–	123	
8	14	167	130	120	
8	15	170	131	117	
8	16	171	132	114	
8	17	173	133	111	
8	18	–	–	108	

XC95180 I/O Pins (continued)

Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes	Function Block	Macrocell	HQ208	PQ160	BScan Order	Notes
9	1	–	–	105		10	1	–	–	51	
9	2	116	88	102		10	2	135	104	48	
9	3	117	89	99		10	3	136	105	45	
9	4	118	90	96		10	4	137	106	42	
9	5	121	91	93		10	5	138	107	39	
9	6	122	92	90		10	6	139	108	36	
9	7	107	–	87		10	7	120	–	33	
9	8	123	93	84		10	8	140	109	30	
9	9	125	95	81		10	9	145	111	27	
9	10	109	–	78		10	10	142	–	24	
9	11	126	96	75		10	11	146	112	21	
9	12	127	97	72		10	12	147	113	18	
9	13	119	–	69		10	13	143	–	15	
9	14	128	98	66		10	14	148	114	12	
9	15	131	101	63		10	15	149	115	9	
9	16	133	102	60		10	16	150	116	6	
9	17	134	103	57		10	17	152	117	3	
9	18	–	–	54		10	18	–	–	0	

XC95180 Global, JTAG and Power Pins

Pin Type	HQ208	PQ160
I/O/GCK1	44	33
I/O/GCK2	46	35
I/O/GCK3	55	42
I/O/GTS1	7	6
I/O/GTS2	9	8
I/O/GTS3	3	2
I/O/GTS4	5	4
I/O/GSR	206	159
TCK	98	75
TDI	94	71
TDO	176	136
TMS	96	73
V_{CCINT} 5 V	11,59,124,153,204	10,46,94,157
V_{CCIO} 3.3 V/5 V	1,26,53,65,79,92,105, 132,157,172,181,184	1,41,61,81,121,141
GND	2,13,24,27,42,52,68,81, 93,104,108,129,130, 141,156,163,177, 190,207	20,31,40,51,70,80, 99,100,110,120,127, 137,160

XC95216 In-System Programmable CPLD

February 1996

Preliminary Product Information

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 216 macrocells with 4800 usable gates
- Up to 168 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 160-pin PQFP and 208-pin HQFP packages

Description

The XC95216 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twelve 36V18 Function Blocks, providing 4,800 usable gates with propagation delays of 10 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95216 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 2 shows a typical calculation for the XC95216 device.

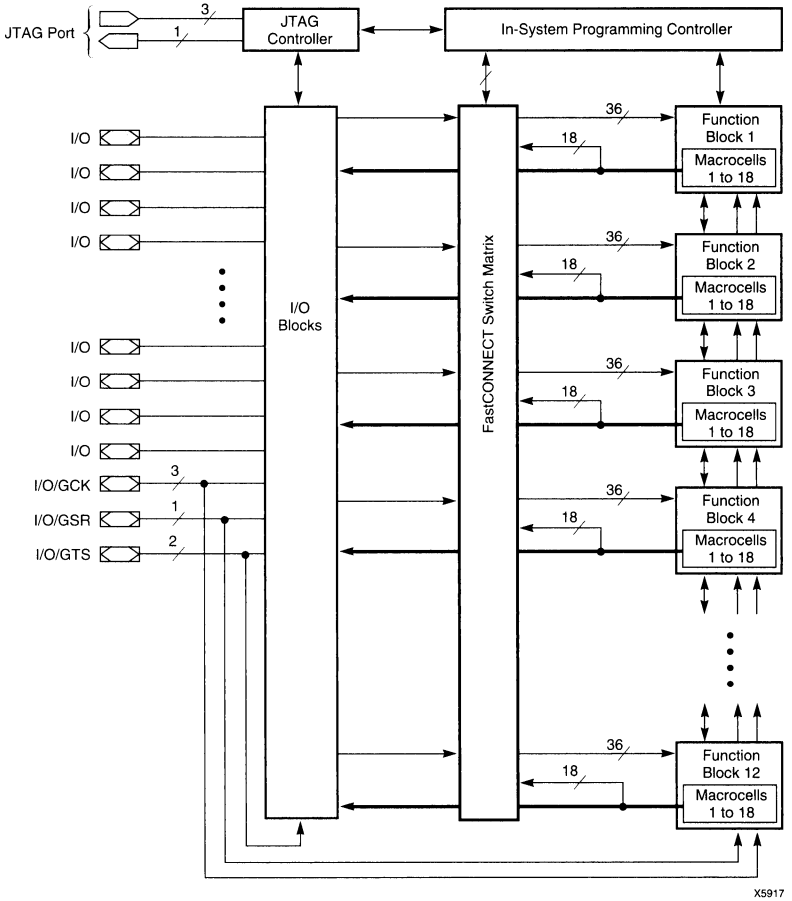


Figure 1. XC95216 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

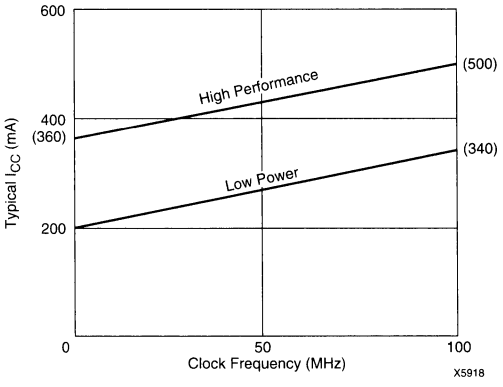


Figure 2. Typical I_{CC} vs Frequency For XC95216

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCINT} + 0.5	V
T_{IN}	Input signal transition time		50	ns

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

DC Characteristics Over Recommended Operating Conditions

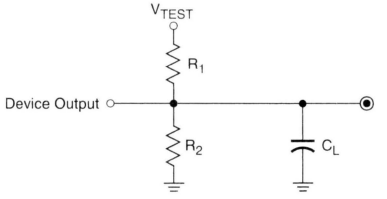
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	200 mA		

AC Characteristics

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		10		15		20	ns
t_{SU}	I/O setup time before GCK	6.5		8.0		10.0		ns
t_{H}	I/O hold time after GCK	0		0		0		ns
t_{CO}	GCK to output valid		6.5		8.0		10.0	ns
f_{CNT}	16-bit counter frequency	111		95.0		83.0		MHz
f_{SYSTEM} [2]	Multiple FB Internal Operating Frequency	67.0		55.0		50.0		MHz
t_{PSU}	I/O setup time before p-term clock input	1.0		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	5.5		6.0		6.0		ns
t_{PCO}	P-term clock to output valid		12.0		14.0		16.0	ns
t_{OE}	GTS to output valid		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output valid		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disable		15.5		18.0		22.0	ns
t_{PTA}	Product term allocator delay		2.0		2.0		2.0	ns
t_{FBK}	Internal combinatorial feedback delay		12.0		17.0		20.0	ns
f_{WLH}	GCK pulse width	4.5		5.0		6.0		ns
t_{SLEW}	Slew rate time delay		4.5		5.0		5.5	ns
t_{LP}	Low power time delay adder		8.5		8.5		8.5	ns

Note 2. f_{SYSTEM} = internal operating frequency for general purpose system designs spanning multiple FBs.

Preliminary



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3. AC Load Circuit

XC95216 I/O Pins

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
1	1	–	–	645	
1	2	18	22	642	
1	3	19	23	639	
1	4	–	28	636	
1	5	21	25	633	
1	6	22	30	630	
1	7	–	–	627	
1	8	23	31	624	
1	9	24	32	621	
1	10	–	12	618	
1	11	25	33	615	
1	12	26	34	612	
1	13	–	–	609	
1	14	27	35	606	
1	15	28	36	603	
1	16	29	37	600	
1	17	30	38	597	
1	18	–	–	594	
2	1	–	–	591	
2	2	6	7	588	[1]
2	3	7	8	585	
2	4	–	29	582	
2	5	8	9	579	[1]
2	6	9	10	576	
2	7	–	–	573	
2	8	11	15	570	
2	9	12	16	567	
2	10	–	66	564	
2	11	13	17	561	
2	12	14	18	558	
2	13	–	–	555	
2	14	15	19	552	
2	15	16	20	549	
2	16	–	14	546	
2	17	17	21	543	
2	18	–	–	540	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
3	1	–	–	537	
3	2	32	43	534	
3	3	33	44	531	[1]
3	4	–	39	528	
3	5	34	45	525	
3	6	35	46	522	[1]
3	7	–	–	519	
3	8	36	47	516	
3	9	37	49	513	
3	10	–	67	510	
3	11	38	50	507	
3	12	39	51	504	
3	13	–	–	501	
3	14	42	55	498	[1]
3	15	43	56	495	
3	16	–	80	492	
3	17	44	57	489	
3	18	–	–	486	
4	1	–	–	483	
4	2	152	198	480	
4	3	153	199	477	
4	4	–	196	474	
4	5	154	200	471	
4	6	155	201	468	
4	7	–	–	465	
4	8	156	202	462	
4	9	158	205	459	
4	10	–	69	456	
4	11	159	206	453	[1]
4	12	2	3	450	[1]
4	13	–	–	447	
4	14	3	4	444	
4	15	4	5	441	[1]
4	16	–	203	438	
4	17	5	6	435	
4	18	–	–	432	

Note: [1] Global control pin

XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
5	1	–	–	429	
5	2	45	58	426	
5	3	46	60	423	
5	4	–	41	420	
5	5	48	61	417	
5	6	49	63	414	
5	7	–	–	411	
5	8	50	64	408	
5	9	52	70	405	
5	10	–	109	402	
5	11	53	71	399	
5	12	54	72	396	
5	13	–	–	393	
5	14	55	73	390	
5	15	56	74	387	
5	16	–	40	384	
5	17	57	75	381	
5	18	–	–	378	
6	1	–	–	375	
6	2	140	180	372	
6	3	142	182	369	
6	4	–	208	366	
6	5	143	185	363	
6	6	144	186	360	
6	7	–	–	357	
6	8	145	187	354	
6	9	146	188	351	
6	10	–	183	348	
6	11	147	191	345	
6	12	148	192	342	
6	13	–	–	339	
6	14	149	193	336	
6	15	150	194	333	
6	16	–	169	330	
6	17	151	197	327	
6	18	–	–	324	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
7	1	–	–	321	
7	2	58	76	318	
7	3	59	77	315	
7	4	–	54	312	
7	5	60	78	309	
7	6	62	82	306	
7	7	–	–	303	
7	8	63	83	300	
7	9	64	84	297	
7	10	–	91	294	
7	11	65	85	291	
7	12	66	86	288	
7	13	–	–	285	
7	14	67	87	282	
7	15	68	88	279	
7	16	–	48	276	
7	17	69	89	273	
7	18	–	–	270	
8	1	–	–	267	
8	2	126	162	264	
8	3	128	164	261	
8	4	–	143	258	
8	5	129	166	255	
8	6	130	167	252	
8	7	–	–	249	
8	8	131	170	246	
8	9	132	171	243	
8	10	–	195	240	
8	11	133	173	237	
8	12	134	174	234	
8	13	–	–	231	
8	14	135	175	228	
8	15	138	178	225	
8	16	–	189	222	
8	17	139	179	219	
8	18	–	–	216	

XC95216 I/O Pins (continued)

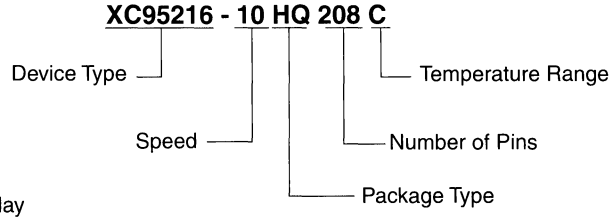
Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
9	1	–	–	213	
9	2	72	95	210	
9	3	74	97	207	
9	4	–	101	204	
9	5	76	99	201	
9	6	77	100	198	
9	7	–	–	195	
9	8	78	102	192	
9	9	79	103	189	
9	10	–	90	186	
9	11	82	110	183	
9	12	83	111	180	
9	13	–	–	177	
9	14	84	112	174	
9	15	85	113	171	
9	16	–	62	168	
9	17	86	114	165	
9	18	–	–	162	
10	1	–	–	159	
10	2	113	147	156	
10	3	114	148	153	
10	4	–	144	150	
10	5	115	149	147	
10	6	116	150	144	
10	7	–	–	141	
10	8	117	152	138	
10	9	118	154	135	
10	10	–	168	132	
10	11	119	155	129	
10	12	122	158	126	
10	13	–	–	123	
10	14	123	159	120	
10	15	124	160	117	
10	16	–	165	114	
10	17	125	161	111	
10	18	–	–	108	

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
11	1	–	–	105	
11	2	87	115	102	
11	3	88	116	99	
11	4	–	119	96	
11	5	89	117	93	
11	6	90	118	90	
11	7	–	–	87	
11	8	91	121	84	
11	9	92	122	81	
11	10	–	107	78	
11	11	93	123	75	
11	12	95	125	72	
11	13	–	–	69	
11	14	96	126	66	
11	15	97	127	63	
11	16	–	120	60	
11	17	98	128	57	
11	18	–	–	54	
12	1	–	–	51	
12	2	101	131	48	
12	3	102	133	45	
12	4	–	106	42	
12	5	103	134	39	
12	6	104	135	36	
12	7	–	–	33	
12	8	105	136	30	
12	9	106	137	27	
12	10	–	151	24	
12	11	107	138	21	
12	12	108	139	18	
12	13	–	–	15	
12	14	109	140	12	
12	15	111	145	9	
12	16	–	142	6	
12	17	112	146	3	
12	18	–	–	0	

XC95216 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208
I/O/GCK1	33	44
I/O/GCK2	35	46
I/O/GCK3	42	55
I/O/GTS1	6	7
I/O/GTS2	8	9
I/O/GTS3	2	3
I/O/GTS4	4	5
I/O/GSR	159	206
TCK	75	98
TDI	71	94
TDO	136	176
TMS	73	96
V_{CCINT} 5 V	10,46,94,157	11, 59, 124, 153, 204
V_{CCIO} 3.3 V/5 V	1,41,61,81,121,141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184
GND	20,31,40,51,70,80,99,100,110,120, 127,137,160	2, 13, 24, 27, 42, 52, 68, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207

Ordering Information



Speed Options

-20 20 ns pin-to-pin delay
-15 15 ns pin-to-pin delay
-10 10 ns pin-to-pin delay

Packaging Options

PQ160 160-Pin Plastic Quad Flat Pack (PQFP)
HQ208 208-Pin Power Quad Flat Pack (HQFP)

Temperature Options

C Commercial 0°C to 70°C
I Industrial -40°C to 85°C

Component Availability

Pins	44		84	100		160	208
Type	Plastic PLCC	Plastic VQFP	Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP	Power QFP
Code	PC44	VQ44	PC84	PQ100	TQ100	PQ160	HQ208
XC95216 -20						C(I)	C(I)
XC95216 -15						C	C
XC95216 -10						C	C

X5916

XC95288 In-System Programmable CPLD

February 1996

Advance Product Information

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 288 macrocells with 6,400 usable gates
- Up to 288 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in a 208-pin HQFP package

Description

The XC95288 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of sixteen 36V18 Function Blocks, providing 6,400 usable gates with propagation delays of 10 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95288 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

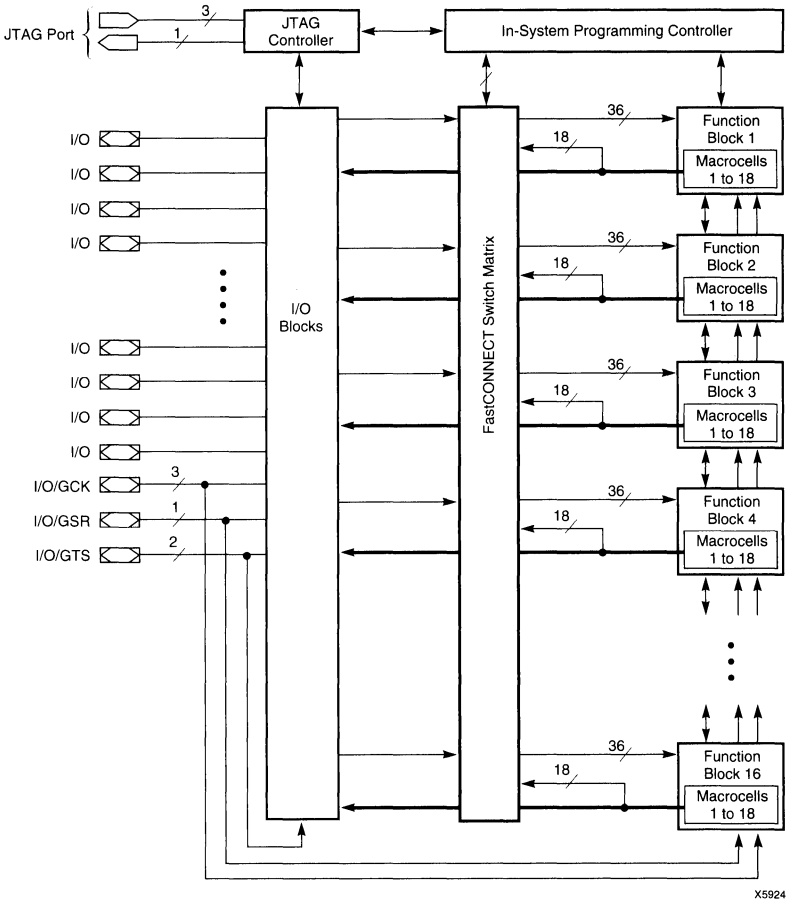


Figure 1. XC95288 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC95288 I/O Pins

Function Block	Macrocell	HQ208	BScan Order	Notes	Function Block	Macrocell	HQ208	BScan Order	Notes
1	1	–	861		3	1	–	753	
1	2	28	858		3	2	38	750	
1	3	29	855		3	3	39	747	
1	4	–	852		3	4	–	744	
1	5	30	849		3	5	40	741	
1	6	31	846		3	6	41	738	
1	7	–	843		3	7	–	735	
1	8	32	840		3	8	43	732	
1	9	–	837		3	9	–	729	
1	10	33	834		3	10	44	726	[1]
1	11	–	831		3	11	–	723	
1	12	34	828		3	12	45	720	
1	13	–	825		3	13	–	717	
1	14	35	822		3	14	46	714	[1]
1	15	36	819		3	15	47	711	
1	16	–	816		3	16	–	708	
1	17	37	813		3	17	48	705	
1	18	–	810		3	18	–	702	
2	1	–	807		4	1	–	699	
2	2	15	804		4	2	3	696	[1]
2	3	16	801		4	3	4	693	
2	4	–	798		4	4	–	690	
2	5	17	795		4	5	5	687	[1]
2	6	18	792		4	6	6	684	
2	7	–	789		4	7	–	681	
2	8	19	786		4	8	7	678	[1]
2	9	–	783		4	9	–	675	
2	10	20	780		4	10	8	672	
2	11	–	777		4	11	–	669	
2	12	21	774		4	12	9	666	[1]
2	13	–	771		4	13	–	663	
2	14	22	768		4	14	10	660	
2	15	23	765		4	15	12	657	
2	16	–	762		4	16	–	654	
2	17	25	759		4	17	14	651	
2	18	–	756		4	18	–	648	

Notes: [1] Global control pin

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
5	1	–	645	
5	2	49	642	
5	3	50	639	
5	4	–	636	
5	5	51	633	
5	6	54	630	
5	7	–	627	
5	8	55	624	[1]
5	9	–	621	
5	10	56	618	
5	11	–	615	
5	12	57	612	
5	13	–	609	
5	14	58	606	
5	15	60	603	
5	16	–	600	
5	17	61	597	
5	18	–	594	
6	1	–	591	
6	2	197	588	
6	3	198	585	
6	4	–	582	
6	5	199	579	
6	6	200	576	
6	7	–	573	
6	8	201	570	
6	9	–	567	
6	10	202	564	
6	11	–	561	
6	12	203	558	
6	13	–	555	
6	14	205	552	
6	15	206	549	[1]
6	16	–	546	
6	17	208	543	
6	18	–	540	
7	1	–	537	
7	2	62	534	
7	3	63	531	
7	4	–	528	
7	5	64	525	
7	6	66	522	
7	7	–	519	
7	8	67	516	
7	9	–	513	
7	10	69	510	
7	11	–	507	
7	12	70	504	
7	13	–	501	
7	14	71	498	
7	15	72	495	
7	16	–	492	
7	17	73	489	
7	18	–	486	
8	1	–	483	
8	2	186	480	
8	3	187	477	
8	4	–	474	
8	5	188	471	
8	6	189	468	
8	7	–	465	
8	8	191	462	
8	9	–	459	
8	10	192	456	
8	11	–	453	
8	12	193	450	
8	13	–	447	
8	14	194	444	
8	15	195	441	
8	16	–	438	
8	17	196	435	
8	18	–	432	

Note: [1] Global control pin

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
9	1	–	429	
9	2	74	426	
9	3	75	423	
9	4	–	420	
9	5	76	417	
9	6	77	414	
9	7	–	411	
9	8	78	408	
9	9	–	405	
9	10	80	402	
9	11	82	399	
9	12	83	396	
9	13	–	393	
9	14	84	390	
9	15	85	387	
9	16	–	384	
9	17	86	381	
9	18	–	378	
10	1	–	375	
10	2	170	372	
10	3	171	369	
10	4	–	366	
10	5	173	363	
10	6	174	360	
10	7	–	357	
10	8	175	354	
10	9	–	351	
10	10	178	348	
10	11	179	345	
10	12	180	342	
10	13	–	339	
10	14	182	336	
10	15	183	333	
10	16	–	330	
10	17	185	327	
10	18	–	324	

Function Block	Macrocell	HQ208	BScan Order	Notes
11	1	–	321	
11	2	87	318	
11	3	88	315	
11	4	–	312	
11	5	89	309	
11	6	90	306	
11	7	–	303	
11	8	91	300	
11	9	–	297	
11	10	95	294	
11	11	97	291	
11	12	99	288	
11	13	–	285	
11	14	100	282	
11	15	101	279	
11	16	–	276	
11	17	102	273	
11	18	–	270	
12	1	–	267	
12	2	158	264	
12	3	159	261	
12	4	–	258	
12	5	160	255	
12	6	161	252	
12	7	–	249	
12	8	162	246	
12	9	–	243	
12	10	164	240	
12	11	165	237	
12	12	166	234	
12	13	–	231	
12	14	167	228	
12	15	168	225	
12	16	–	222	
12	17	169	219	
12	18	–	216	

XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BScan Order	Notes
13	1	–	213	
13	2	103	210	
13	3	106	207	
13	4	–	204	
13	5	107	201	
13	6	109	198	
13	7	–	195	
13	8	110	192	
13	9	–	189	
13	10	111	186	
13	11	112	183	
13	12	113	180	
13	13	–	177	
13	14	114	174	
13	15	115	171	
13	16	–	168	
13	17	116	165	
13	18	–	162	
14	1	–	159	
14	2	144	156	
14	3	145	153	
14	4	–	150	
14	5	146	147	
14	6	147	144	
14	7	–	141	
14	8	148	138	
14	9	–	135	
14	10	149	132	
14	11	150	129	
14	12	151	126	
14	13	–	123	
14	14	152	120	
14	15	154	117	
14	16	–	114	
14	17	155	111	
14	18	–	108	

Function Block	Macrocell	HQ208	BScan Order	Notes
15	1	–	105	
15	2	117	102	
15	3	118	99	
15	4	–	96	
15	5	119	93	
15	6	120	90	
15	7	–	87	
15	8	121	84	
15	9	–	81	
15	10	122	78	
15	11	123	75	
15	12	125	72	
15	13	–	69	
15	14	126	66	
15	15	127	63	
15	16	–	60	
15	17	128	57	
15	18	–	54	
16	1	–	51	
16	2	131	48	
16	3	133	45	
16	4	–	42	
16	5	134	39	
16	6	135	36	
16	7	–	33	
16	8	136	30	
16	9	–	27	
16	10	137	24	
16	11	138	21	
16	12	139	18	
16	13	–	15	
16	14	140	12	
16	15	142	9	
16	16	–	6	
16	17	143	3	
16	18	–	0	

XC95288 Global, JTAG and Power Pins

Pin Type	HQ208
I/O/GCK1	44
I/O/GCK2	46
I/O/GCK3	55
I/O/GTS1	7
I/O/GTS2	9
I/O/GTS3	3
I/O/GTS4	5
I/O/GSR	206
TCK	98
TDI	94
TDO	176
TMS	96
V_{CCINT} 5 V	11,59,124,153,204
V_{CCIO} 3.3 V/5 V	1,26,53,65,79,92,105, 132,157,172,181,184
GND	2,13,24,27,42,52,68,81, 93,104,108,129,130, 141,156,163,177, 190,207

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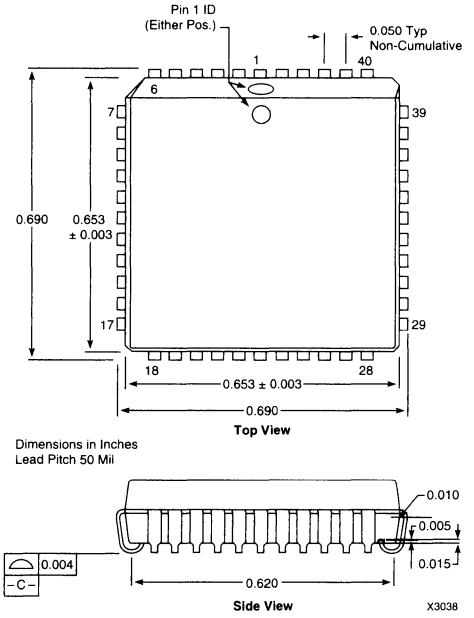
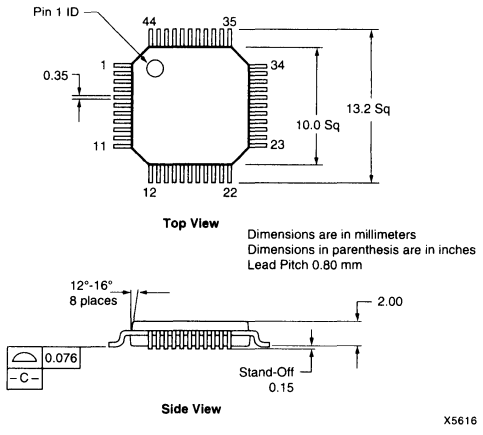
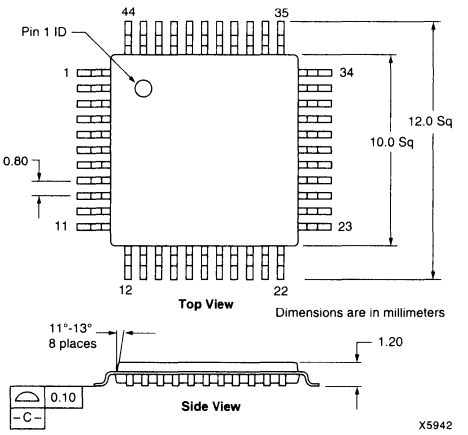
SECTION 4



44-Pin Plastic PLCC (PC44)



44-Pin Plastic PQFP (PQ44)



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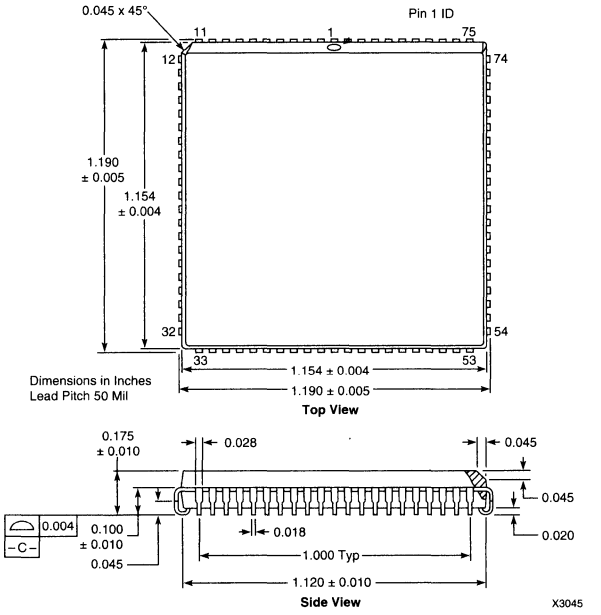
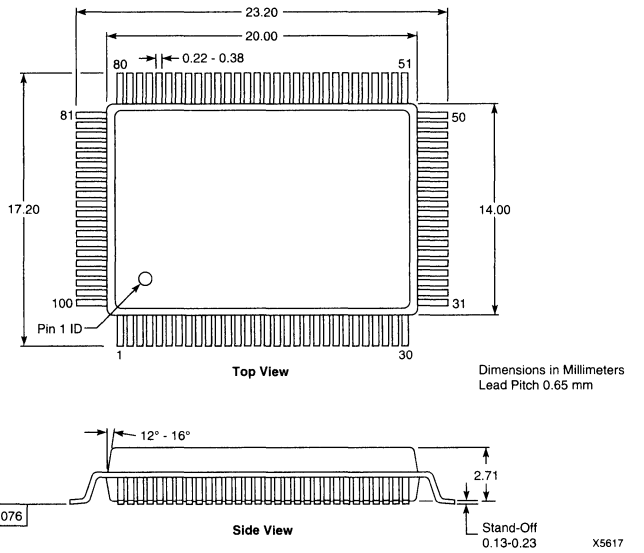
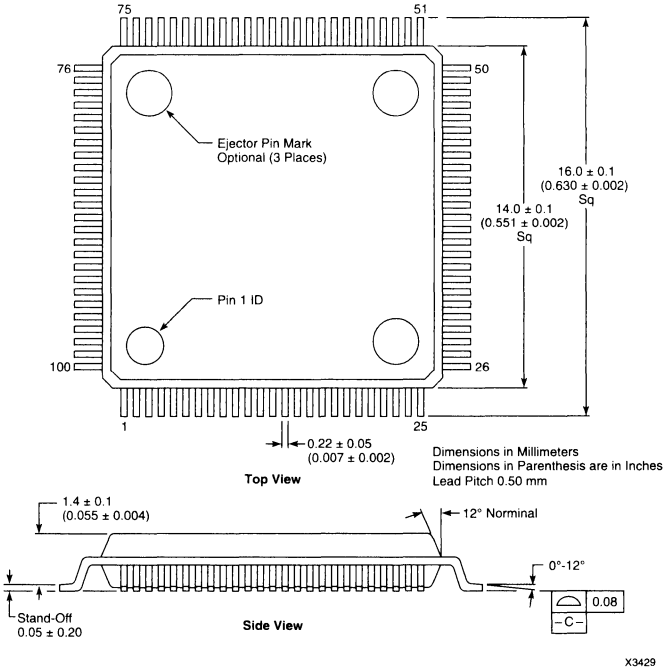


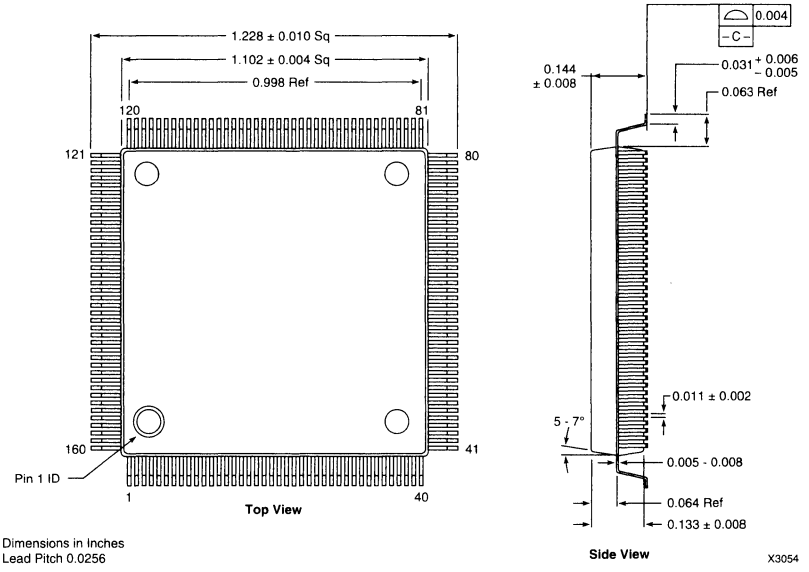
84-Pin Plastic PLCC (PC84)



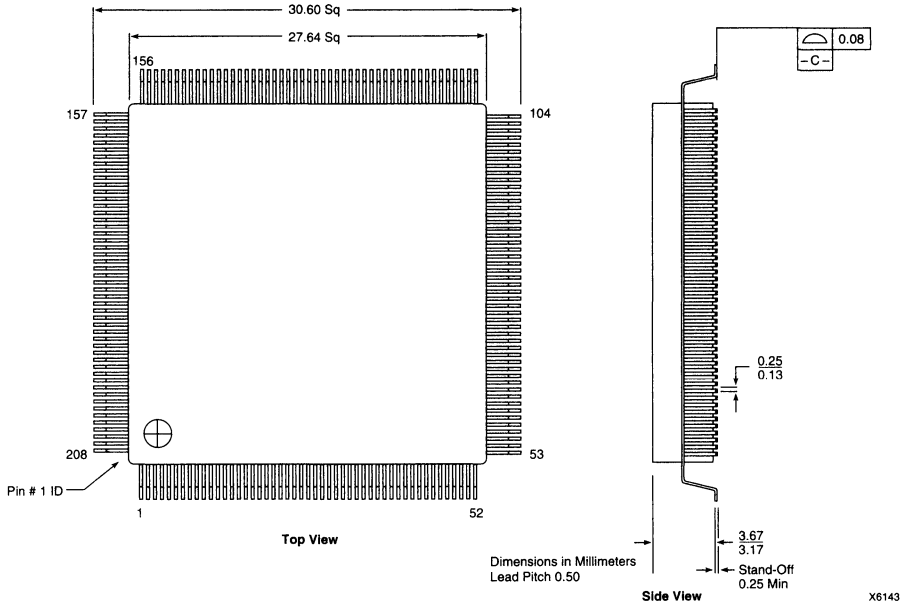
100-Pin Plastic PQFP (PQ100)



100-Pin Plastic TQFP (TQ100)



160-Pin Plastic PQFP (PQ160)



208-Pin Power QFP (HQ208)

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SECTION 5

Using the XC9500 JTAG Boundary-Scan Interface

February 1996

Application Note

Introduction

This document explains the XC9500 boundary-scan interface and demonstrates the software available for programming and testing XC9500 CPLDs. An appendix summarizes JTAG operations and overviews those additional operations supported by XC9500 CPLDs for in system programming.

Boundary Scan Overview

IEEE Boundary Scan Standard 1149.1, also known as JTAG, is a testing standard described by design rules that allow software to reduce test cost. The primary benefit of the standard is its ability to transform difficult printed circuit board testing problems into well-structured ones that software can deal with efficiently.

The standard defines a hardware architecture and the mechanisms for its use to solve these problems.

The JTAG standard itself defines instructions that can be used to perform functional and interconnect tests as well as built-in self test procedures. Vendor-specific extensions to the standard allow execution of maintenance and diagnostic applications as well as permit programming algorithms for reconfigurable parts. It is the latter that have been implemented (in addition to all the mandatory operations) in the XC9500 family.

Downloading a Programmed Design File

The EZTAG Download Cable (Figure 1) connects to the parallel printer port of any PC. The cable contains drivers to buffer the signals as they are driven into the system. The power for the drivers is derived from the target system. The cable's V_{CC} and GND wires must be connected to the corresponding signals on the target system. The remaining four wires are to be connected to the corresponding JTAG TAP inputs on the target system. These inputs are TCK, TDI and TMS and the output is TDO. TRST is not supported by the FastFLASH BSCAN Download cable and if any parts in the system have a TRST, this pin should be attached to V_{CC}. The cable pins are clearly labeled.

Figure 2 shows how the cable is connected to the printed circuit board for programming or JTAG testing. Be sure to connect all six flying leads to the target board and observe the power sequencing recommendations.

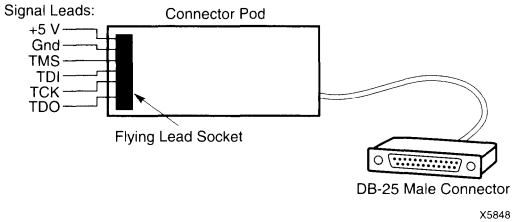

Figure 1. XC9500 JTAG Download Cable

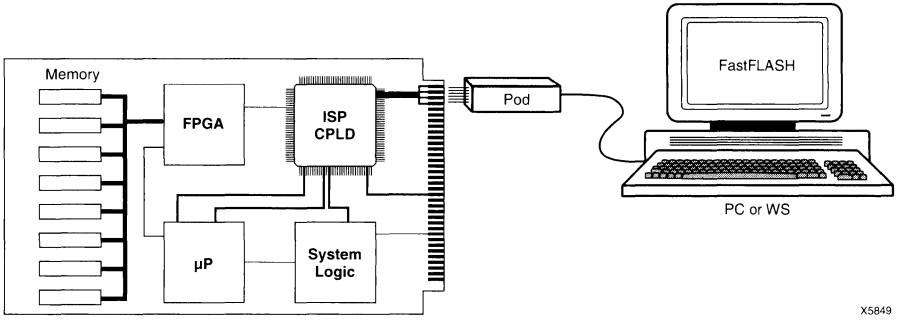

Figure 2. Target PCB Connected for Program/Test

Power sequencing

Cable protection ensures the parallel port cannot be damaged through normal cable operation. For increased safety, please ensure the PC is always powered up before the target system is.

EZTAG Download Software

Upon initiation of the EZTAG Download Software, the parallel port is queried to verify the connection of the EZTAG Download cable. The target system power must be on and the cable attached for proper verification. If an error message is returned stating the cable could not be found or indicating a cable other than the EZTAG Download cable was identified, check the cable power connections. Figure 3 shows the EZTAG user interface.

Using EZTAG

The following steps outline the downloading procedure:

1. Make sure that the BSDL files for XC9500 parts are stored along the XACT search path.
2. Invoke EZTAG.
3. Select the JEDEC files for XC9500 devices or BSDL files for other devices for each device in the chain ordered from system TDI to TDO.
4. Select the operations desired for each XC9500 part.
5. Select BYPASS for each non-XC9500 part (default).
6. Select the "execute" button and download begins.

Using the XChecker Cable

The XChecker cable can be used to program XC9500 parts as well as operate JTAG testing. In this case, attach the TDI, TCK, TMS, V_{CC}, and GND pins to the target board with the flying leads so labeled. See Figure 4. The TDO signal function will be performed by the XChecker signal labeled RD. The EZTAG software will automatically query the computer I/O ports and detect the existence of the XChecker cable and drive it appropriately.

See Appendix 1 for more details on specific JTAG features supported.

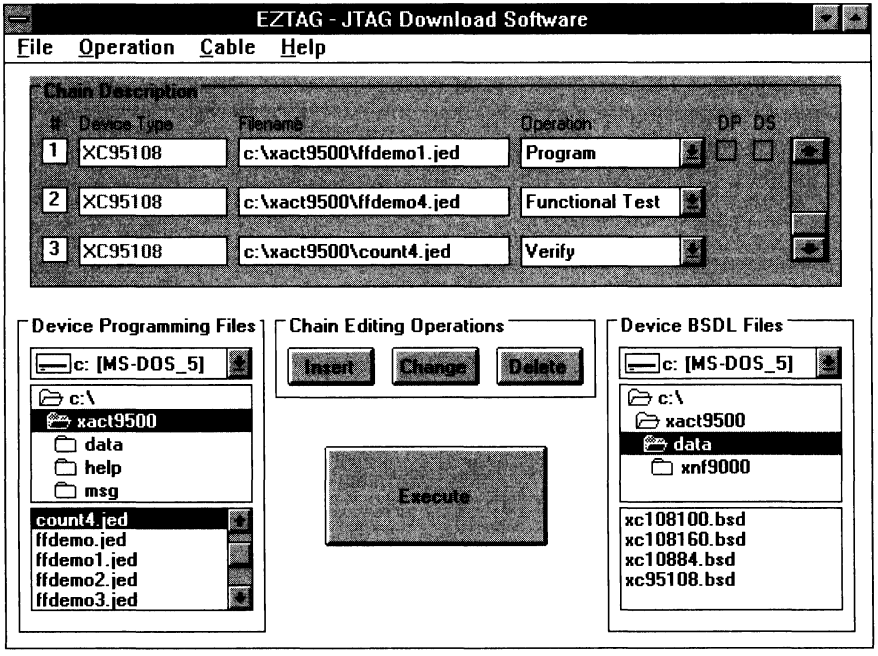

Figure 3. The EZTAG Download Software User Interface

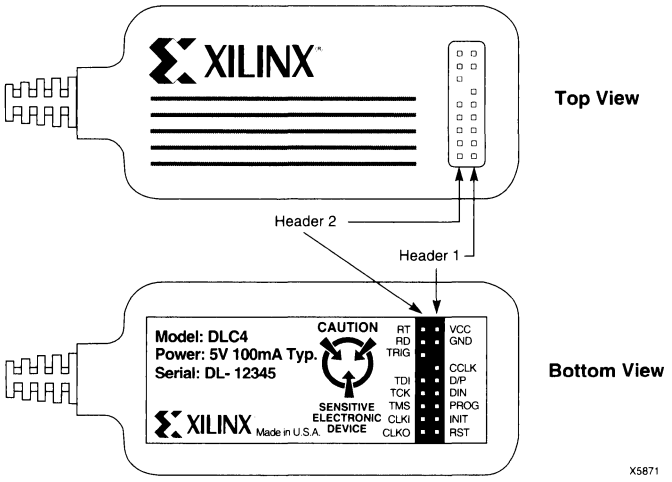

Figure 4. XChecker Cable

Appendix1 - JTAG Details

The top level schematic of the test logic defined by IEEE Std 1149.1 includes several key blocks (see Figure 5):

The TAP Controller

The TAP controller responds to control sequences supplied through the test access port (TAP) and generates the clocks and control signals required by the other circuit blocks.

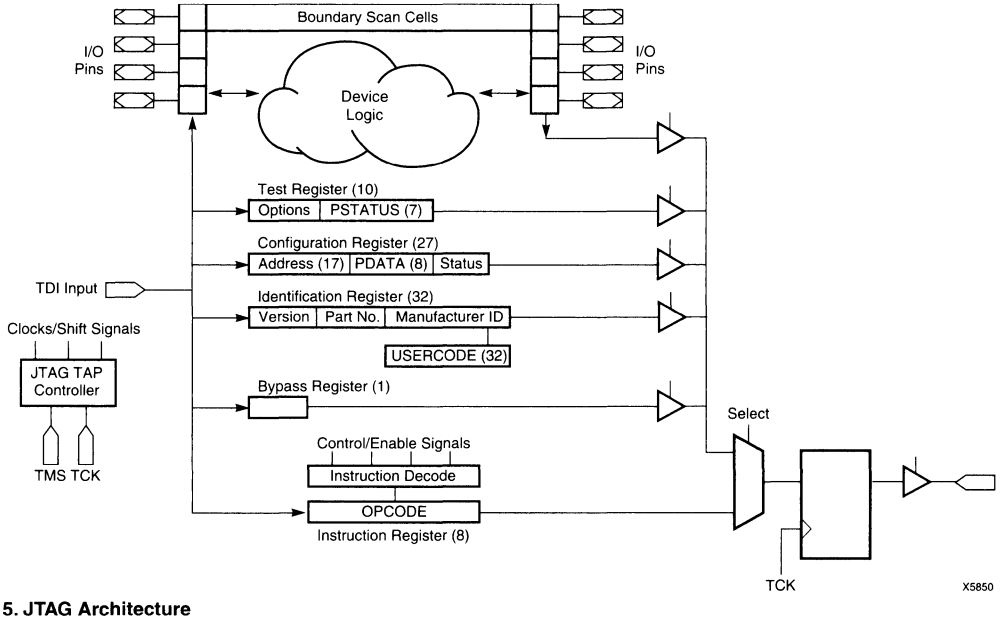

Figure 5. JTAG Architecture

The Instruction Register

The instruction register is a shift register-based circuit and is serially loaded with instructions that select an operation to be performed.

The Data Registers

These are a bank of shift registers. The stimuli required by an operation are serially loaded into the data registers, selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

The JTAG Test Access Port

The JTAG Test Access Port (TAP) has four pins that drive the circuit blocks and control specific operations. The TAP loads and unloads instructions and data. The four TAP pins are: TMS, TCK, TDI and TDO. The function of each TAP pin is:

TMS - Test Mode Select is the mode input signal to the TAP Controller. The TAP controller is a 16-state finite state machine (FSM) that controls the JTAG engine. At the rising edge of TCK, TMS determines the TAP controller state sequence. TMS has an internal pull-up resistor to provide a logic 1 to the system if TMS is not driven.

TCK - JTAG test clock. TCK sequences the TAP controller as well as all JTAG registers in FastFLASH.

TDI - Test Data Input is the serial data input to all JTAG instruction and data registers.

The TAP controller state and instruction register contents determine which register is fed by TDI for any operation. TDI has an internal pull-up resistor on it to provide a logic 1 to the system if TDI is not driven. TDI is loaded into the JTAG registers on TCK's rising edge.

TDO - Test Data Out is the serial data output for all JTAG instruction and data registers. The TAP controller state and instruction register contents determine which register feeds TDO for a specific operation. Only one register (instruction or data) is connected between TDI and TDO for any JTAG operation. TDO changes state on TCK's falling edge and is only active during the shifting of data through the device. TDO is three-stated at all other times.

JTAG TAP Controller

The TAP Controller is a 16-state FSM, that controls the loading of data into the various JTAG registers. A state diagram of the TAP controller is shown in Figure 6. The

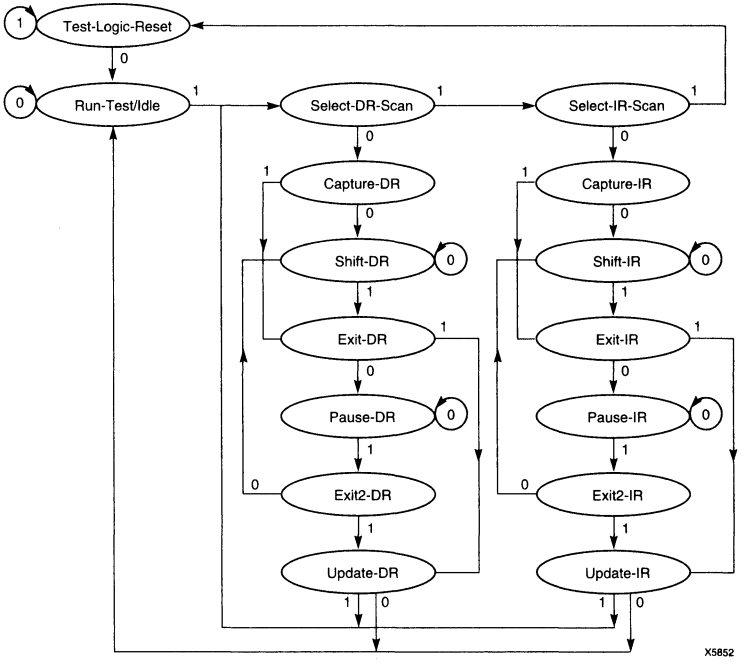

Figure 6. TAP Controller State Diagram

state of TMS at the rising edge of TCK determines the sequence of state transitions. There are basically two state transition paths for sampling the signal at TDI - one for shifting information to the instruction register and one for shifting data into the data register.

JTAG TAP Controller States

a) Test-Logic-Reset

This state is entered on device power-up when at least five TCK clocks occur with TMS held high. Entry into this state resets all JTAG logic to not interfere with the normal component logic, and loads the IDCODE instruction into the instruction register.

b) Run-Test-Idle

In this state certain operations can occur depending on the current instruction. For the XC9500 family, "Run-Test-Idle" causes generation of the program, verify, erase, and POR pulses when the associated ISP instruction is active.

c) Select-DR-Scan

This is a transitional state entered prior to performing a scan operation on a data register or in passing to the Select-IR-Scan state.

d) Select-IR-Scan

This is a transitional state entered prior to performing a scan operation on the instruction register or in returning to the Test-Logic-Reset state.

e) Capture-DR

"Capture-DR" allows data to be loaded from parallel inputs into the data register selected by the current instruction at the rising edge of TCK. If the selected data register has no parallel inputs, the register retains its state.

f) Shift-DR

In this state data is shifted by one stage in the currently selected register from TDI towards TDO by one stage on each rising edge of TCK.

g) Exit1-DR

This is a transitional state allowing the option of passing to the Pause- DR state or transitioning directly to the Update-DR state.

h) Pause-DR

This is a wait state that allows shifting of data to be temporarily halted.

i) Exit2-DR

This is a transitional state allowing the option of passing to the Update-DR state or returning to the Shift-DR state to continue accepting data.

j) Update-DR

In this state the data contained in the currently selected data register is loaded into a latched parallel output (for registers that have such a latch) on the falling edge of TCK after entering this state. The parallel latch prevents changes at the parallel register output from occurring during the shifting process.

k) Capture-IR

In this state data is loaded from parallel inputs into the instruction register on the rising edge of TCK. The least two significant bits of the parallel inputs must have the value 01, and the remaining 6 bits are either hard-coded or used for monitoring the security and data protect bits.

l) Shift-IR

In this state instruction register values are shifted one stage towards TDO on each rising TCK edge.

m) Exit1-IR

Exit1-IR is a transitional state allowing the option of transitioning to the Pause-IR state or the Update-IR state.

n) Pause-IR

Pause-IR allows shifting of the instruction to be temporarily halted.

o) Exit2-IR

Exit2-IR is a transitional state allowing the option of passing to the Update-IR state or returning to the Shift-IR state to continue shifting in data.

p) Update-IR

In this state instruction register values are parallel latched out on the falling edge of TCK. The parallel latch prevents changes at the parallel output of the instruction register from occurring during the shifting process.

JTAG Instructions Supported in XC9500 Parts

Mandatory Boundary Scan Instructions

BYPASS

The BYPASS instruction configures the part to bypass the scan registers and pass immediately to TDO.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of a components to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary scan shift register prior to the selection of other boundary-scan test instructions.

EXTEST

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections.

XC9500 Additional Boundary Scan Instructions

INTEST

The INTEST instruction allows testing of the on-chip system logic while the component is already on the board.

HIGHZ

HIGHZ permits automatic placement of all outputs on the XC9500 part to high impedance (3-state) mode. This condition can be beneficial for board testing strategies.

IDCODE

The IDCODE instruction allows blind interrogation of the components assembled onto a printed circuit board to determine what components exist in a system.

USERCODE

The USERCODE instruction allows a user-programmable identification code to be shifted out for examination. This allows the programmed function of the component to be determined.

XC9500 Reconfiguration Instructions

ISPEN

ISPEN instruction activates the XC9500 part for In-System Programming.

FPGM

The FPGM instruction programs bits at specified addresses.

FERASE

FERASE instruction erases a block of programming cells.

FVFY

FVFY verifies the programming at specified addresses.

ISPEX

ISPEX transfers the XC9500 memory cell contents to internal low power configuration latches.

Device Operations

The programming information is extracted from the JEDEC file generated by the fitter software. The JEDEC file name is defaulted to <design>.jed. The file of this name is searched for along the XACT path.

Device operation options available to users are:

1. Program & Verify

Download contents of the JEDEC file to the device programming registers. Configure the device and read back the contents of device programming registers and compare it with the JEDEC file. Report any differences to the user.

2. Verify

Read back contents of the device programming registers and compare it with the JEDEC file.

3. Erase

Clear the device configuration information.

4. Functional Test

Apply user-specified functional vectors from the JEDEC file to the device, comparing results obtained with expected values. Report any differences.

5. Read Device ID

Read and display the contents of the JTAG IDCODE register.

6. Read User Signature

The signature value will have been set by the user at programming time. It is valid only after programming. This function reads the contents of the JTAG USERCODE register and displays the result.

7. Bypass

Ignore this device when addressing devices in the JTAG boundary scan chain.

8. Readback

Extracts contents of device programming registers and creates a new JEDEC file with the results.

9. Checksum

Extract the contents of device programming registers and calculate a checksum for comparison with the expected value

Feedback

Detailed information regarding any failure conditions is located in the system log file. This file is displayed at the end of the run.

Disconnecting

Turn off the target system power before disconnecting the XC9500 BSCAN Download cable.

Modifying a Programmed Design File

The flow is identical for a modified programmed design file of any modification size.

BSDL Summary

The Boundary Scan Description Language (BSDL) describes the boundary scan features of a component. One BSDL file is required for each kind of XC9500 device in the system.The system looks for BSDL files along the XACT path and in the current working directory. The name of the BSDL file is assumed to be <device name>.bsd.

JEDEC Summary

Fuse map and functional verification vector file. The JEDEC file is an ASCII file containing the configuration information and optionally the vectors that can be used to verify the functional behaviour of the configured part. One JEDEC file is generated for each XC9500 device in the system.

The system looks for the JEDEC files along the XACT path and in the current working directory. The name of the JEDEC file is assumed to be <design name>.jed.

References

1. IEEE Std. 1149.1a 1993 Standard Test Access Port & Boundary-Scan Architecture. 1993
2. The Boundary-Scan Handbook, Ken Parker, Klewer Academic Publishers, 1992
3. JEDEC Standard, Standard Data Transfer Format Between Data Preparation System and Programmable Logic Device Programmer JESD3-C, June 1994.
4. IEEE Std. 1149.1b Supplement (B) to Standard Test Access Port & Boundary-Scan Architecture, IEEE Std 1149.1 - 1990, 1994.

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Xilinx Quality Assurance

Quality Assurance Program

Quality Assurance encompasses all aspects of company business. Xilinx continually strives to improve quality to meet customer's changing needs and expectations. To do this, the company is dedicated to the following.

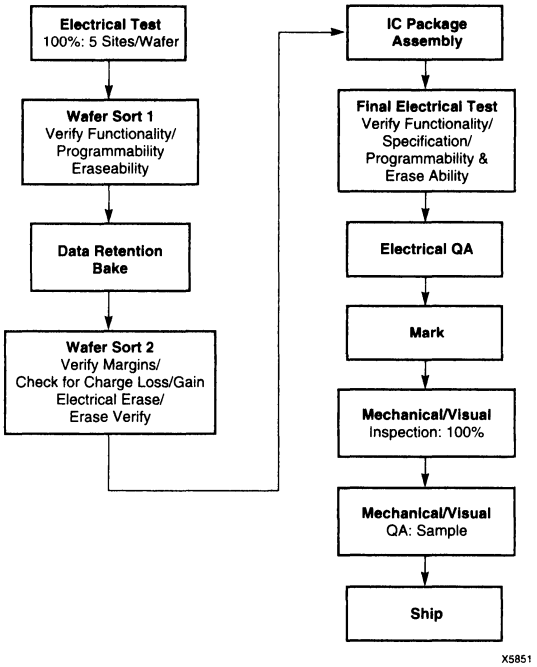
- To provide a broad range of products and services that satisfy both the expectations of customers and the company's stringent quality standards.
- To emphasize open communication with customers and suppliers, supported with the necessary statistical data.
- To continually improve the quality of Xilinx products, services, and company efficiency
- To maintain a work environment that fosters quality and reliability leadership and excellence.

From its inception, Xilinx has been committed to delivering the highest quality, most reliable programmable logic available. A strong Quality Assurance and Reliability program begins at the initial design stages and is carried through to final shipment. An extensive, ongoing reliability-testing program is used to predict the field performance of all Xilinx devices.

These tests provide an accelerated method of emulating long-term system operation in severe field environments. From the performance of the devices during these tests, predictions of actual field performance under a variety of conditions can be easily calculated.

Xilinx is committed to customer satisfaction. By adhering to the highest quality standards, the company has achieved leadership in the CPLD and FPGA manufacturing areas.

Quarterly reports describing the nature and purpose of the various reliability tests performed on finished devices are available. Please contact the Quality Assurance and Reliability Department at Xilinx.



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