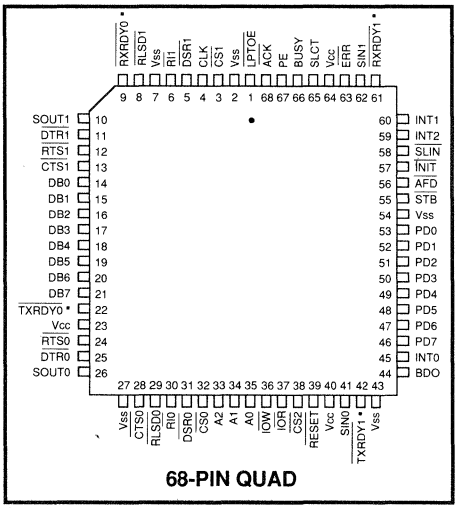
WD16C452/WD16C552
DUAL ENHANCED ASYNCHRONOUS COMMUNICATIONS ELEMENTS (ACE) WITH PARALLEL PORT

FEATURES

- Two fully programmable serial I/O channels (dc to 512K baud)
- THREE-STATE TTL drive capabilities for bi-directional data bus and control bus on each channel
- Loopback controls for communications link fault isolation for each ACE
- Line break generation and detection for each ACE
- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals for each channel
- Fully prioritized independent interrupt system controls for each channel
- 16 byte FIFO buffers on both transmit and receive of each channel for CPU relief during high speed data transfer †
- Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each channel †
- Two modes of DMA signaling available for transfer of data characters to and from FIFO buffers †



* INDICATES INTERNAL NO CONNECTS ON WD16C452

- Fully bi-directional Centronics compatible parallel port for direct printer interface
- CMOS implementation for high speed and low power requirements
- 68-pin QUAD package

DESCRIPTION

The low power CMOS WD16C452/552 is a single device solution for serving two serial input/output ports simultaneously and one fully bi-directional parallel port for the IBM* PC, PC XT*, PC AT*, PS/2*, and compatible systems. The parallel port is fully compatible to the Centronics printer port and IBM Serial/Parallel Adapter. Each Asynchronous Communications Element (ACE) is fully programmable. Each ACE in the WD16C552 is capable of buffering up to 16 bytes of data for transmission, and up to 16 bytes of data upon reception relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in a multitasking environment. DMA signaling, between the internal FIFO buffers and host CPU, allows single or multiple character transfers. Each ACE is fully compatible with the National NS16550A. Each ACE has a maximum recommended data rate of 512K with a clock frequency of 8.0 MHz.

(†) The FIFO mode of operation is not available in the WD16C452.

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1.0 DESCRIPTION

1.1 General

The WD16C452/WD16C552 is an enhanced dual channel version of the WD16C550 Asynchronous Communications Element (ACE), plus a bi-directional parallel data port which fully supports a Centronic's compatible printer interface. Each ACE is fully compatible with the National NS16550A.

The two serial input/output Asynchronous Communications Elements interface simultaneously in microprocessor-based systems. Each ACE performs parallel-to-serial conversion on the output and serial-to-parallel conversion on the input. Two modes of operation exist for each serial I/O channel. After powerup and hardware reset each ACE is functionally compatible to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode), which is only available on the WD16C552, can be activated through software, relieving the CPU of excessive overhead due to interrupts. The complete status of each ACE can be read at any time from internal registers.

The parallel port allows information received from the data bus to be printed. The parallel port, together with the two serial ports, provides IBM PC/AT and PS/2 compatibles with a single device solution for serving three ports.

The WD16C552 is an enhanced WD16C452 with FIFOs. FIFO mode is only available in the WD16C552.

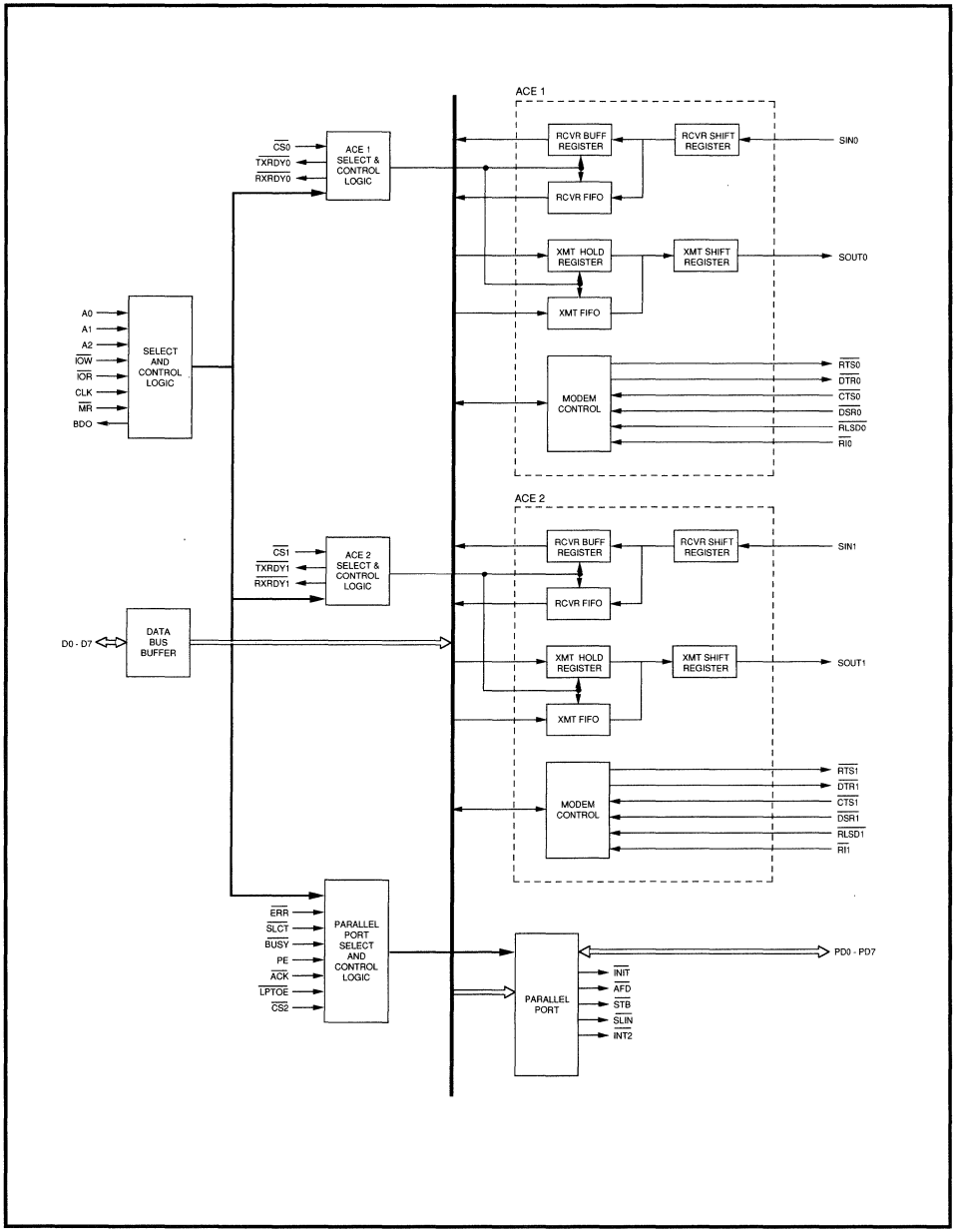


FIGURE 1-1. WD16C552 BLOCK DIAGRAM

2.0 SERIAL CHANNEL REGISTERS

The WD16C552 contains two serial ports, therefore, the following registers exist in duplicate, one per channel.

2.1 Serial Port Register Addressing

2.1.1 Chip Select ($\overline{CS0}$, $\overline{CS1}$): When $\overline{CS0}$ is low, registers for serial channel 0 can be accessed, and when $\overline{CS1}$ is low, registers for serial channel 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$) should ever be low at any time (an invalid condition).

Master Reset:
A low level input on this pin causes the ACE to reset to the condition listed in table 3-1.

Software Reset:
A software reset is performed by writing to the LCR, MCR, and Divisior Latches. Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to return to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

2.1.2 Register Select (A0, A1, A2): To select a register for read or write operation, see table 2-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

TABLE 2-1. REGISTER ADDRESSING

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

3.0 ACE OPERATIONAL DESCRIPTION

3.1 Master Reset

A low-level input on this pin causes the ACE to reset to the condition listed in table 3-1.

3.2 ACE Accessible Registers

The system programmer has access to any of the registers as summarized in table 3-2. For individual register descriptions, refer to the following pages under register heading.

TABLE 3-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	BDO = $\overline{RCLK \cdot IOR}$ (At Master Reset, the CPU sets RCLK and IOR = Low when device is selected.)	High
INTRPT (RCVR ERRS)	Master Reset/LSR	Low
INTRPT (RCVR DATA READY)	Master Reset/Read RBR	Low
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO	MR or FCR1• FCR0 or ΔFCR0	All Bits Low
XMIT FIFO	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	In THREE-STATE Mode, Unless IOR = Low or IOW = Low when Device is Selected	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

TABLE 3-2. ACCESSIBLE WD16C452/WD16C552 REGISTERS

	Register Address					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)♦	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

(♦) These bits are 0 in Character Mode.

TABLE 3-2. ACCESSIBLE WD16C452/WD16C552 REGISTERS (Continued)

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO♦ (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

(♦) These bits are 0 in Character Mode.

3.3 Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE Programmable Baud Rate Generator

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

TABLE 3-3. BAUD RATES USING 1.8432 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2▪	2.860

TABLE 3-4. BAUD RATE USING 3.072 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3▪	14.285

▪ Smallest allowable divisor when using corresponding clock.

TABLE 3-5. BAUD RATE USING 8.0 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1 ▪	2.344

▪ Smallest allowable divisor when using corresponding clock.

3.5 Line Status Register

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level).

When in FIFO Mode an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

> NOTE:
> Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator and is a read-only bit. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO is empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO.

3.6 Interrupt Identification Register

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to table 3-2).

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

TABLE 3-6. INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

3.7 Interrrupt Enable Register

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 Scratch Pad Register

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer as a general purpose register.

3.9 FIFO Control Register

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from both FIFOs. The FIFOs should be cleared before changing modes. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register is not cleared.

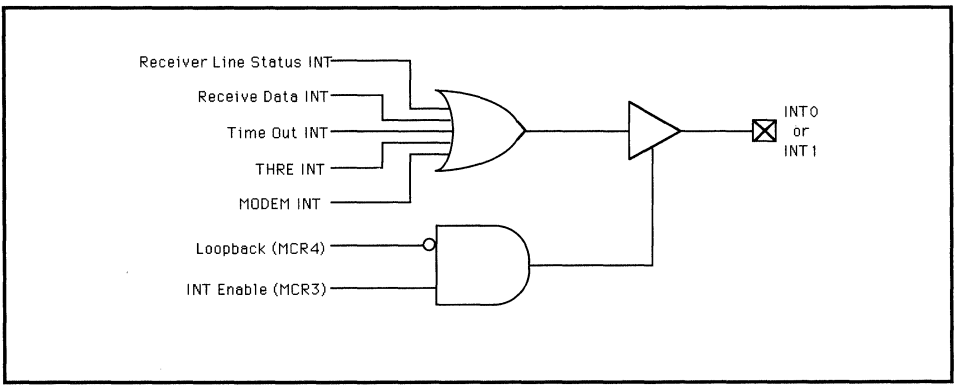
Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14



INTERRUPT SIGNAL LOGIC

4.0 MODEM Control Register

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 3-2.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

> NOTE:
> The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

Bit 3: This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is three-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control bits (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

5.0 MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 3-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

> NOTE:
> Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

5.1 FIFO Operation Notes

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt will occur if the following is true:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

5.2 Parallel Port Description

The parallel port supports Centronics type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to tables 5-1 and 5-2.)

Register Descriptions:

Read Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

Read Status Register

Bits 0 through 2: These bits are set to a logic one.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to table 5-2.

Read Control Register

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to table 5-2.

Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

Bits 5 through 7: These bits are set to a logic one.

Write Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to write data to the parallel bus.

Write Control

This register, which is used when writing to the associated lines, is a duplicate of the Read Control Register.

TABLE 5-1. PARALLEL PORT ($\overline{CS2}$ = 0) REGISTER ADDRESSES

A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Control
1	1	1	0	Invalid

TABLE 5-2. ACCESSIBLE PARALLEL PORT REGISTERS

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	1	$\overline{Init}$	$\overline{Init}$	Data Bit 2
3	Data Bit 3	$\overline{Error}$	Slin	Slin	Data Bit 3
4	Data Bit 4	Slct	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	1	Data Bit 5
6	Data Bit 6	$\overline{Ack}$	1	1	Data Bit 6
7	Data Bit 7	$\overline{Busy}$	1	1	Data Bit 7

6.0 TYPICAL APPLICATIONS

Figures 6-1 and 6-2 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

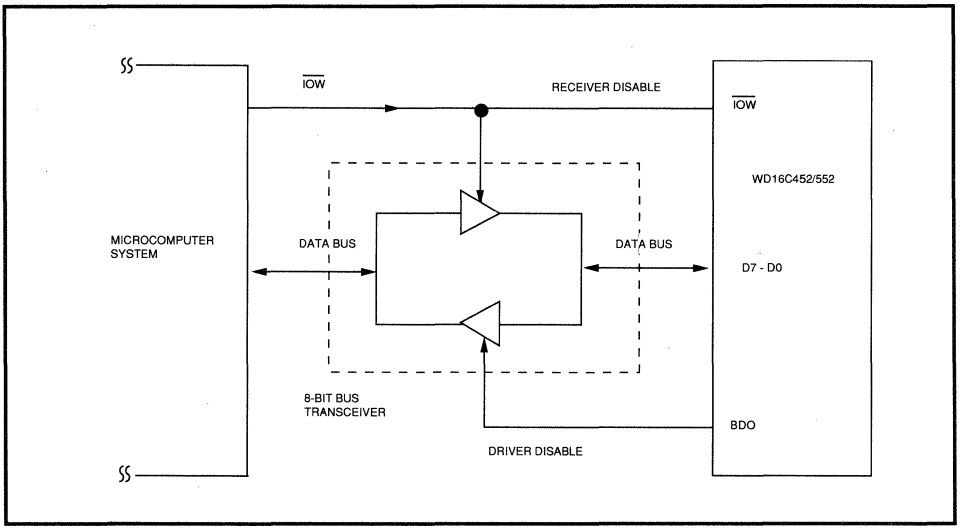


FIGURE 6-1. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

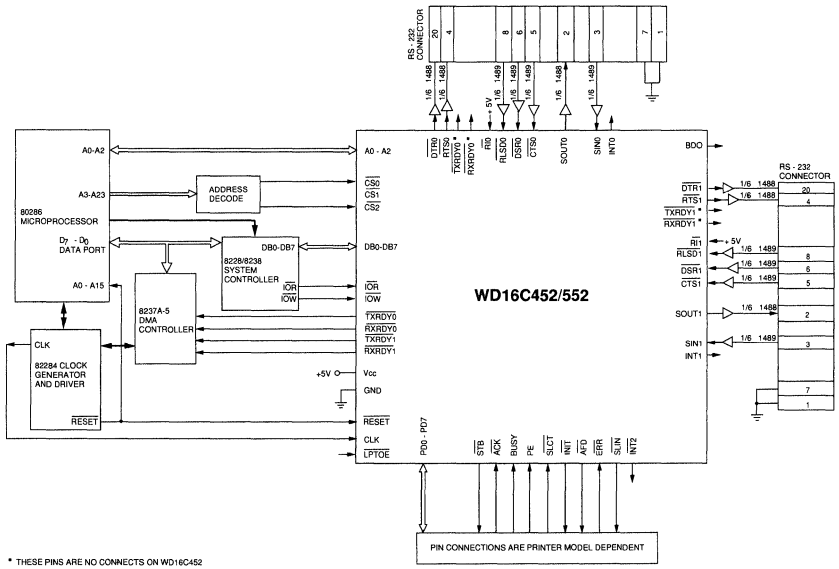
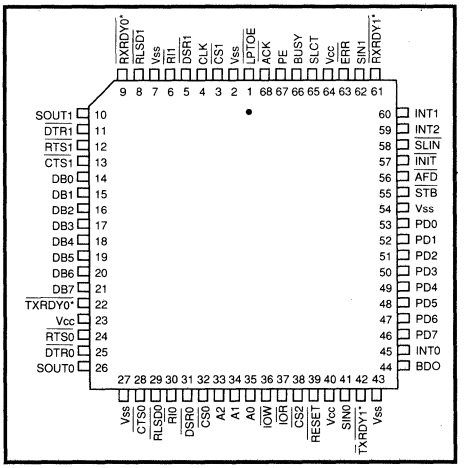


FIGURE 6-2. TYPICAL 16-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE WD16C452/WD16C552

APPENDIX A

A.0 PIN DESIGNATIONS

Figure A-1 illustrates the 68-Pin QUAD assembly. Table A - 1 lists all pin designations.



* INDICATES INTERNAL NO CONNECTS ON WD16C452

FIGURE A-1. WD16C452/WD16C552 68-PIN QUAD ASSEMBLY PIN DESIGNATIONS

TABLE A-1. PIN DESIGNATIONS

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{\text{LPTOE}}$	$\overline{\text{LINE PRINTER}}$ OUTPUT ENABLE	When low, this input signal enables the parallel line printer. When high, the line printer pins are held in a high-impedance state. For normal line printer operation this line may be permanently grounded.
2, 7, 27, 43, 54	Vss	Ground	System signal ground.
3	$\overline{\text{CS1}}$	$\overline{\text{Chip Select 1}}$	Chip Select input when active (low), selects serial channel 1.
4	CLK (1X)	Clock Input	External clock input.
5, 31	$\overline{\text{DSR1}}$, $\overline{\text{DSR0}}$	$\overline{\text{Data Set Ready}}$	When low, this input signal from the communication link indicates that it is ready to exchange data with the associated ACE. Bit 5 of the associated MODEM Status Register reflects the logical state of $\overline{\text{DSR}}$.
6, 30	$\overline{\text{RI1}}$, $\overline{\text{RI0}}$	$\overline{\text{Ring Indicator}}$	Input when low indicates, for the associated ACE, a ringing signal is being received by the MODEM or data set. This logical value is reflected in bit 6 of the associated MODEM Status Register.
8, 29	$\overline{\text{RLSD1}}$, $\overline{\text{RLSD0}}$	$\overline{\text{Received Line}}$ Signal Detect	Input from the DCE indicating that the associated ACE is receiving a signal which meets its signal quality conditions. Bit 3 of the associated MODEM Status Register reflects this value.
9, 61	$\overline{\text{RXRDY0}}$♦, $\overline{\text{RXRDY1}}$♦	$\overline{\text{Receiver Ready}}$	Receiver ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode. Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, RXRDY will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. RXRDY will go inactive when the RCVR FIFO (FIFO Mode), or holding register (Character Mode) is empty.

(♦) These pins are internal no connects on the WD16C452.

TABLE A-1. PIN DESIGNATIONS (Continued)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
			Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, RXRDY will go active (low) when the trigger level or time out has been reached. RXRDY goes inactive (high) when the FIFO is empty.
10, 26	SOUT1, SOUT0	Serial Data Output	Transmitted Serial Data Out to the communication link from the associated ACE. The SOUT signal is set to a marking condition (logical 1) upon a Master Reset.
11, 25	DTR1, DTR0	Data Terminal Ready	Output when low informs the MODEM or data set that the associated ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
12, 24	RTS1, RTS0	Request to Send	Output when low informs the MODEM or data set that the associated ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
13, 28	CTS1, CTS0	Clear to Send	Input from DCE to the associated ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
14 thru 21	DB0-DB7	Data Bits	Three-State, bi-directional communication lines between the ACE and Data Bus. D0 is the least significant bit (LSB) and the first serial transmitted or received bit.
22, 42	TXRDY0♦, TXRDY1♦	Transmitter Ready FIFO Control	Transmit ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode.
			Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, TXRDY will be active (low) if there are no characters in the Xmit FIFO (FIFO Mode) or Xmit holding register (Character Mode). TXRDY will go inactive after the first character is loaded.

(♦) These pins are internal no connects on the WD16C452.

TABLE A-1. PIN DESIGNATIONS (Continued)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
			Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one, or more, unfilled position in the Xmit FIFO TXRDY will be active (low). TXRDY will go inactive when the FIFO is completely full.
23, 40, 64	Vcc	Power Supply	+5V power supply.
32	CS0	Chip Select 0	Chip Select input when active (low) selects serial channel 0.
33 thru 35	A2, A1, A0	Address lines A2-A0	These three inputs are used to select an internal register of the ACE, or parallel port.
36	IOW	Input/Output Write Strobe	Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0, CS1, or CS2 to be ACE#1, ACE#2, or parallel port (respectively).
37	IOR	Input/Output Read Strobe	Output active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
38	CS2	Chip Select 2	Chip Select input when active (low), enables the line printer port.
39	Reset	Reset	Input when active (low), will force the device into an idle mode in which all serial data activities are suspended. The device will remain in an idle state until programmed to begin data activities.
41, 62	SIN0, SIN1	Serial Data Inputs	Received Serial Data Input from the communication link to the associated ACE. Data on the serial data inputs are disabled when exercising loop back mode, and internally connected to their respective SIN lines.
44	BDO	Bus Buffer Output	Output goes active when either serial channel, or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).

TABLE A-1. PIN DESIGNATIONS (Continued)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
45, 60	INT0, INT1	Serial Channel Interrupts	Three-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending for the associated ACE. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46 thru 53	PD7-PD0	Parallel Data Bits	Bi-directional data port which provides parallel input and output to the system. The eight lines are held in a high-impedance state when LPTOE is high.
55	$\overline{\text{STB}}$†	Line Printer Strobe	Output line, when active, provides the the line printer with a signal to latch the data currently on the parallel port.
56	$\overline{\text{AFD}}$†	Line Printer Autofeed	Output line, when active, provides a signal for the line printer to autofeed continuous form paper.
57	$\overline{\text{INIT}}$†	Line Printer Initialize	Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	$\overline{\text{SLIN}}$†	Line Printer Select	Output line, when active (low), selects the printer.
59	INT2	Interrupt Printer Port	Three-state output (enabled by bit 4 of WCR) goes active on the positive transition of ACK. This interrupt is reset low upon a reset operation, or after pending interrupts are serviced.
63	$\overline{\text{ERR}}$	Line Printer Error	Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.
65	SLCT	Line Printer Select	Input from the line printer that goes high when the line printer has been selected.
66	BUSY	Line Printer Busy	Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	Line Printer Paper Empty	Input from the line printer goes high when the printer is out of paper.
68	$\overline{\text{ACK}}$	Line Printer Acknowledge	Input from line printer that goes low to confirm the data transfer from the WD16C552 to the printer was successful.

(†) These outputs are open drain with internal pull-ups.

(♦) These pins are internal no connects on the WD16C452.

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages
with respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C452/WD16C552 ..... 300mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

TABLE B-1. DC OPERATING CHARACTERISTICS
Ta = 0°C (32°F) to =70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, unless otherwise specified.

		WD16C452/WD16C552			
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0mA on DB0-DB7. Iol = 12mA on PD0-PD7. Iol = 10mA on INIT, STB , SLIN, AFD (NOTE). Iol = 2.0mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = -0.4mA on DB0-DB7. Ioh = -2.0mA on PD0-PD7. Ioh = -0.2mA on INIT, AFD, STB, SLIN. Ioh = -0.2mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.25V, no loads on SIN0, SIN1; DSR0, DSR1; RLSD0, RLSD1; CTS0, CTS1. RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
Iil	Input Leakage		±10	µA	Vcc = 5.25V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage		±10	µA	Vin = 0.0V, 5.25V.
Idl	Data Bus Leakage		±10	µA	Vout = 0.4V, Vout = 4.6V Data Bus in High-Impedance State.
Ioz	3 State Leakage		± 20	µA	Vcc = 5.25V, GND = 0V, Vout = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE:
The SLIN, AFD, STB and INIT outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state each input will sink a minimum of 10mA. The internal pull-ups generate 2.0mA of internal Iol.

TABLE B-2. CAPACITANCE
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

		WD16C452/WD16C552			
SYMBOL	**CHARACTERISTIC**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

APPENDIX C

C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%

C.1 TIMING DIAGRAMS

TABLE C-1. WD16C452/WD16C552 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Receiver Timing
C-2	Transmitter Timing
C-3	MODEM Control Timing
C-4	Read Cycle Timing
C-5	Write Cycle Timing
C-6	RCVR FIFO Signaling Timing for First Byte
C-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-11	Transmitter DMA Mode 1 (FCR3 = 1)
C-12	Parallel Port Timing

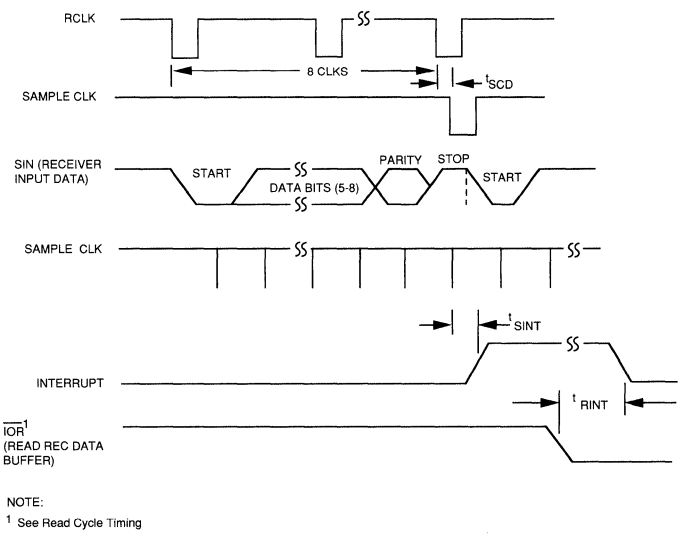


FIGURE C-1. RECEIVER TIMING

TABLE C-2. RECEIVER TIMING

		WD16C452/WD16C552			
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tSCD	Delay from RCLK† to Sample Time		2	µsec	
tSINT	Delay from Stop to Set Interrupt		1♦	RCLK† Cycles	100pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt	0.250	1	µsec	100pF Load

(♦) When receiving the first byte in FIFO Mode tSINT (only for timeout or trigger level interrupt) will be delayed 3 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 8 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16X the baud rate clock.

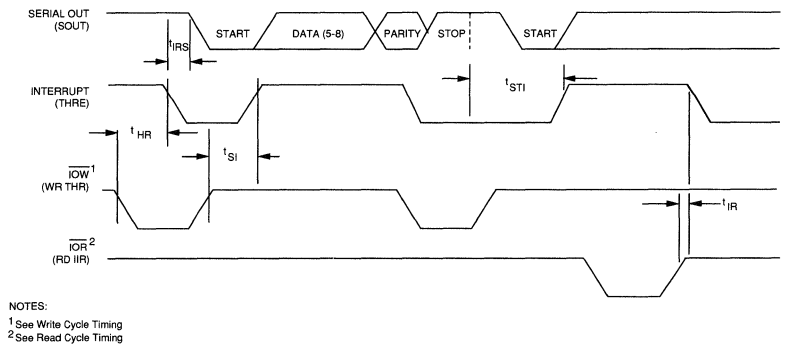


FIGURE C-2. TRANSMITTER TIMING

TABLE C-3. TRANSMITTER TIMING

		WD16C452/WD16C552			
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tHR	Delay from $\overline{IOW}$ (WR THR) to Reset Interrupt		175	nsec	100pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	RCLK† Clock Cycles	
tSI	Delay from Initial Write to Interrupt	16	24	RCLK† Clock Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	RCLK† Clock Cycles	
tIR	Delay from $\overline{IOR}$ (RD IIR toReset Interrupt (THRE)		250	nsec	100pF Load
tSXA	Delay from Start to TXRDY Active	0	8	RCLK† Clock Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	0.300	µsec	

(†) RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16X the baud rate clock.

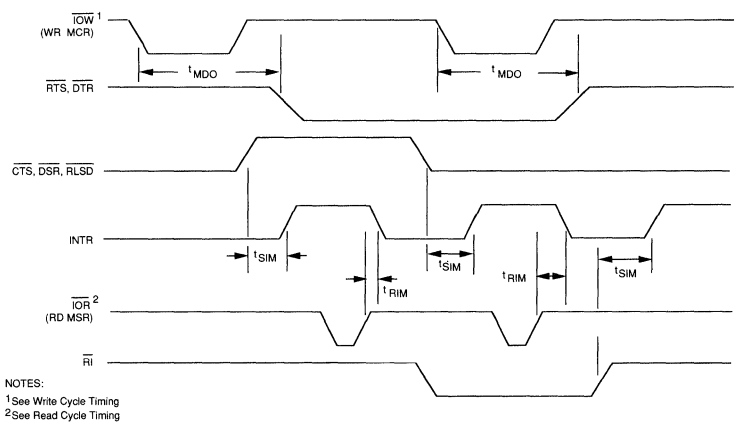


FIGURE C-3. MODEM CONTROL TIMING

TABLE C-4. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from $\overline{IOW}$ (WR MCR) to Output		0.200	µsec	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		0.250	µsec	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		0.250	µsec	100pF Load

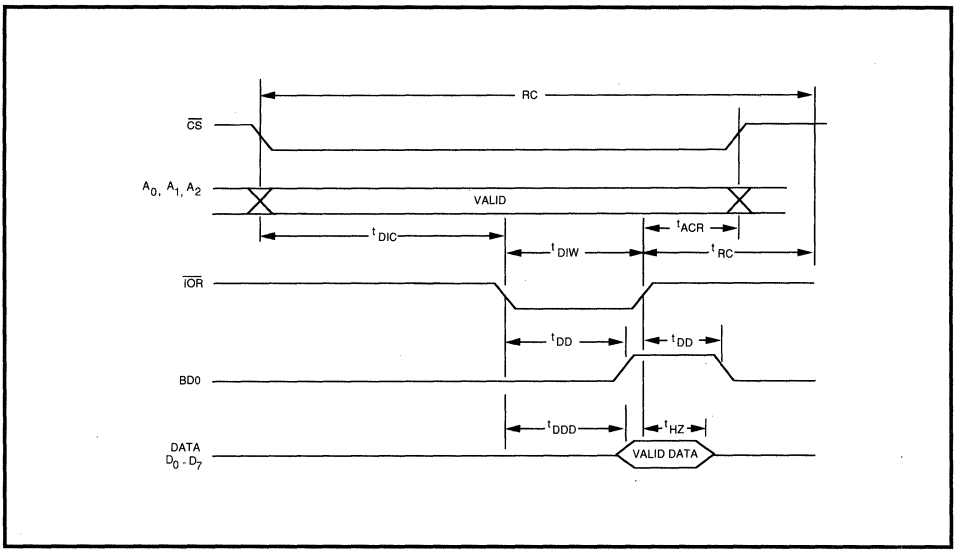


FIGURE C-4. READ CYCLE TIMING

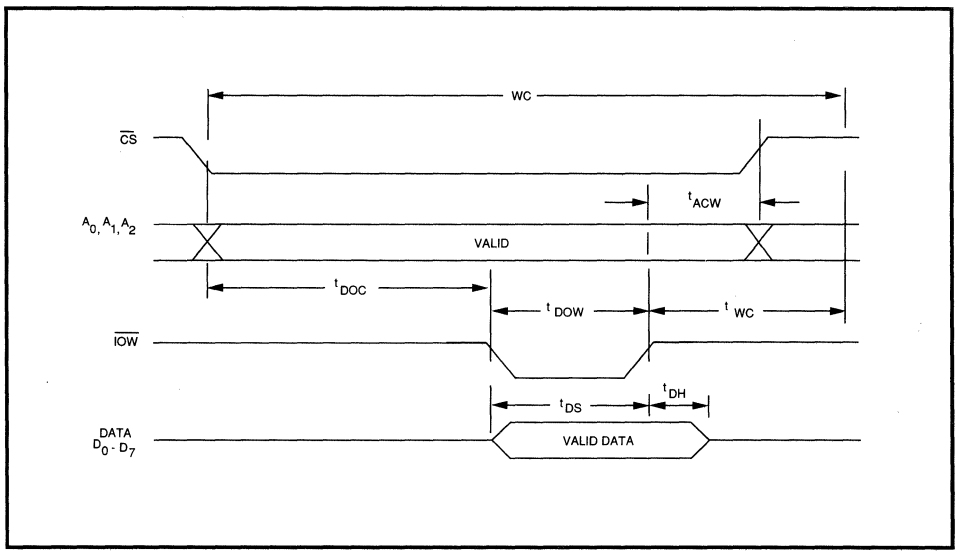


FIGURE C-5. WRITE CYCLE TIMING

TABLE C-5. READ/WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{DIW}	$\overline{IOR}$ Strobe Width	125		nsec	1TTL Load
tRC	Read Cycle Delay	125		nsec	1TTL Load
RC	Read Cycle = tDIC + tDIW + tRC + 20 nsec	280		nsec	1TTL Load
t_{DD}	$\overline{IOR}$ to Driver Enable (BDO) Delay		60	nsec	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to Data		100	nsec	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	nsec	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		nsec	1TTL Load
t_{WC}	Write Cycle Delay	150		nsec	1TTL Load
WC	Write Cycle = + tDOC + tDOW + tWC + 20 nsec	280		nsec	1TTL Load
t_{DS}	Data Setup Time	30		nsec	1TTL Load
t_{DH}	Data Hold Time	30		nsec	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		nsec	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		nsec	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from IOR	20		nsec	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from IOR	20		nsec	1TTL Load
t_{MR}	Master Reset Pulse Width	5.0		µsec	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse	55		nsec	
t_{XL}	Duration of Clock LOW Pulse	55		nsec	External Clock (8.0 MHz Max.)

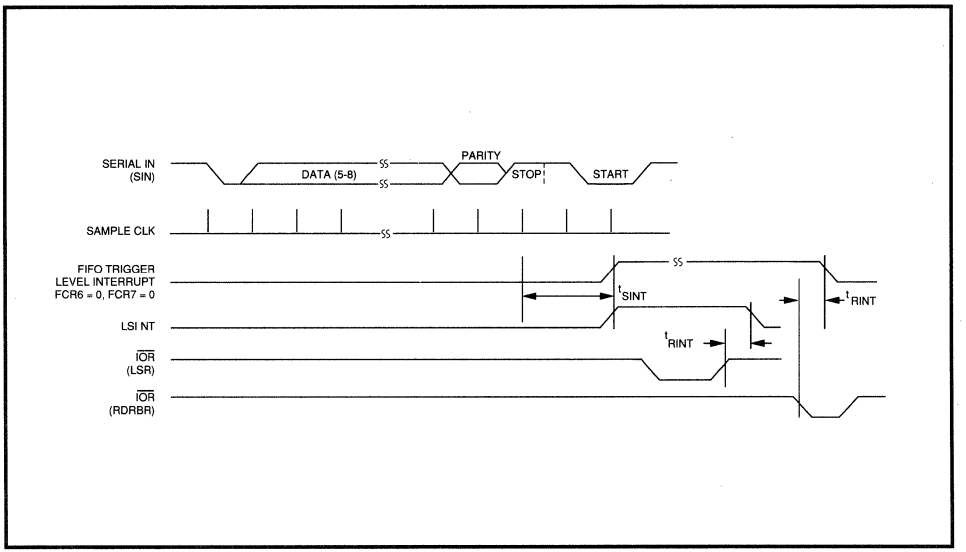


FIGURE C-6. RCVR FIFO SIGNALING TIMING FOR FIRST BYTE

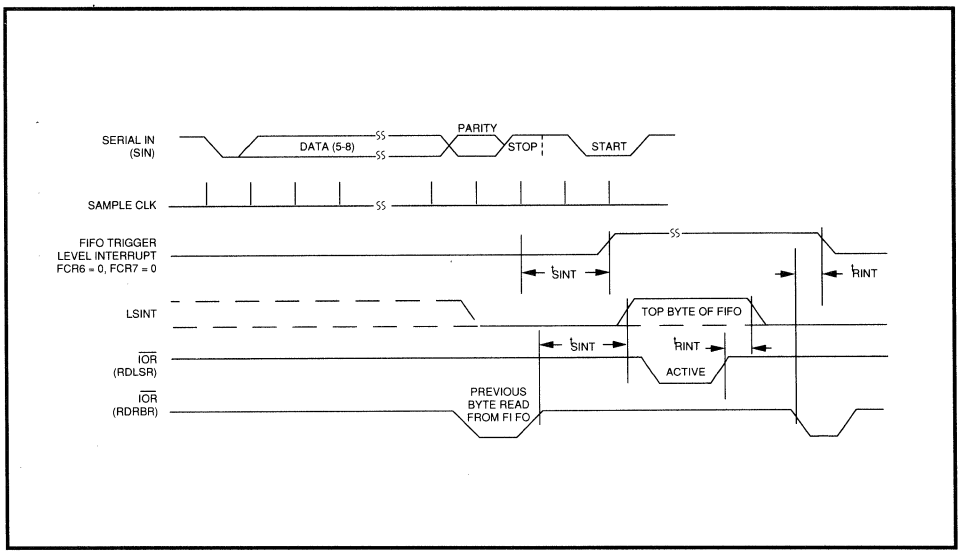


FIGURE C-7. RCVR FIFO SIGNALING TIMING AFTER FIRST BYTE (RBR ALREADY SET)

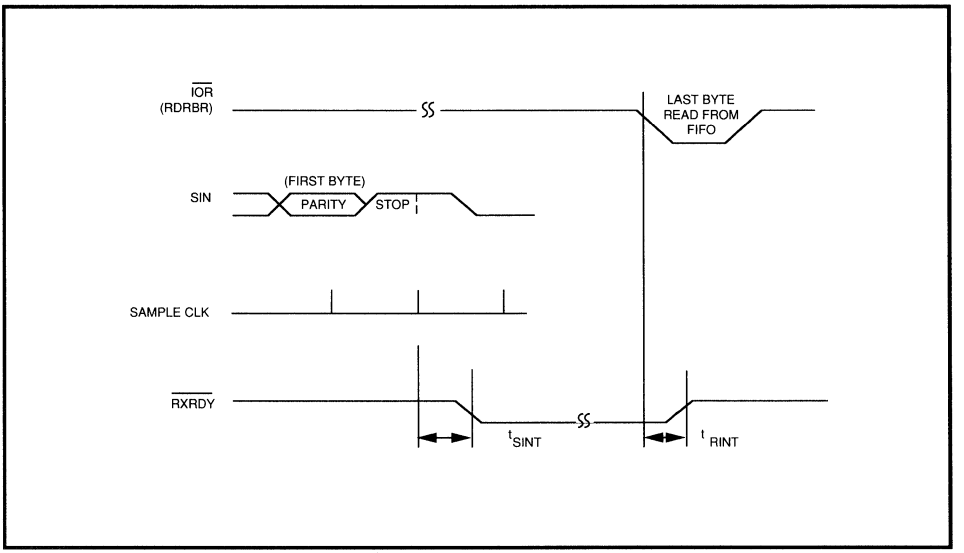


FIGURE C-8. RECEIVER DMA MODE 0 TIMING (FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0)

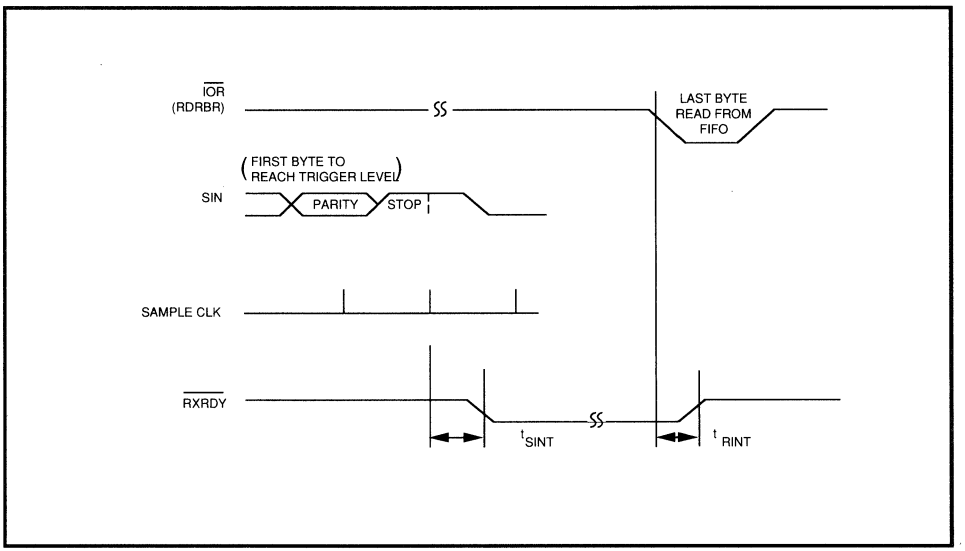


FIGURE C-9. RECEIVER DMA MODE 1 TIMING (FCR0 = 1 AND FCR3 = 1)

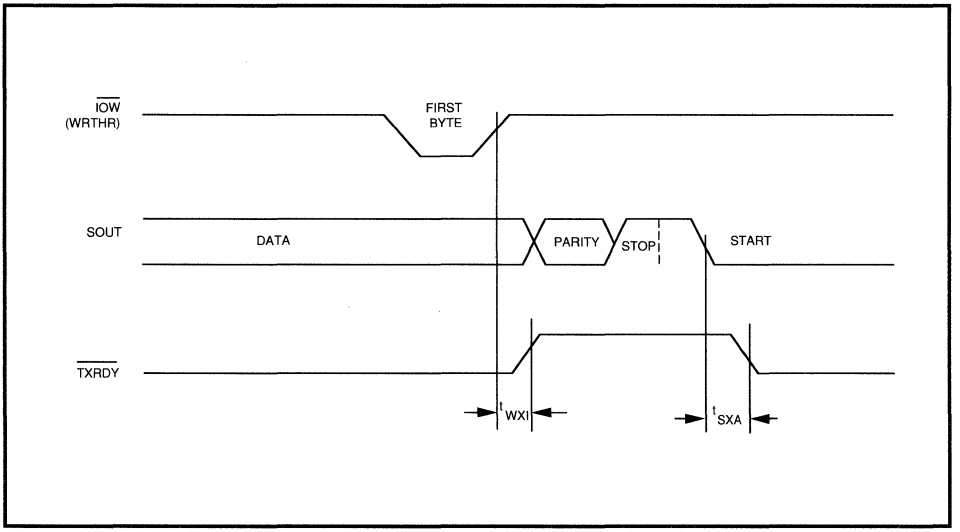


FIGURE C-10. TRANSMITTER DMA MODE 0 TIMING (FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0)

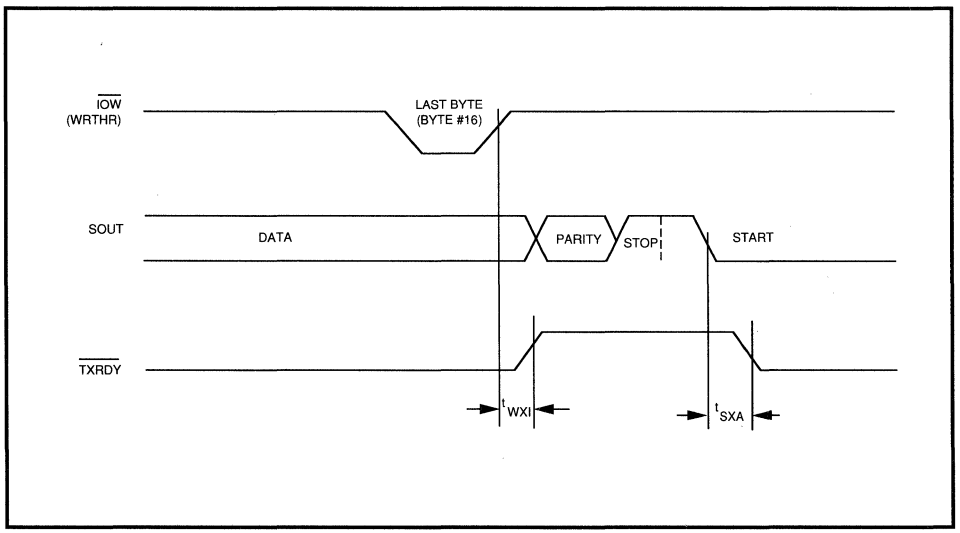
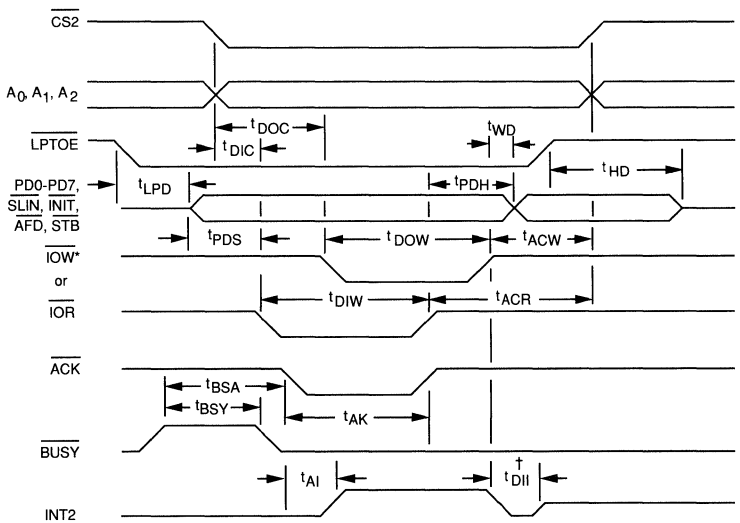


FIGURE C-11. TRANSMITTER DMA MODE 1 (FCR0 = 1 AND FCR3 = 1)



* See serial port timings for data set-up and hold times for Write Cycle.

† t_{DII} is the delay from the positive transition of $\overline{IOW}$ only when the Write Cycle, bit 4, of the Write Control Register (IRQ Enable Bit).

FIGURE C-12. PARALLEL PORT TIMING

TABLE C-6. PARALLEL PORT TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		nsec	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		nsec	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, $\overline{SLIN}$, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$	1		µsec	No External Pull-up Resistor and 50pF Load
t_{HD}	$\overline{LPTOE}$ High to PD0-PD7 3-State	120		nsec	
t_{LPD}	$\overline{LPTOE}$ Low to PD0-PD7 Delay	100		nsec	
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		nsec	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		nsec	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		nsec	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		nsec	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		nsec	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		nsec	
t_{BSA}	$\overline{BUSY}$ Start to $\overline{ACK}$			msec	Printer Dependent
t_{BSY}	$\overline{BUSY}$ Width			µsec	Printer Dependent
t_{AK}	$\overline{ACK}$ Width			µsec	Printer Dependent
t_{AI}	INT2 Delay from $\overline{ACK}$			µsec	

APPENDIX D

D.0 PACKAGE DIAGRAM

Figure D-1 illustrates the 68 Pin-QUAD package showing dimensions in inches.

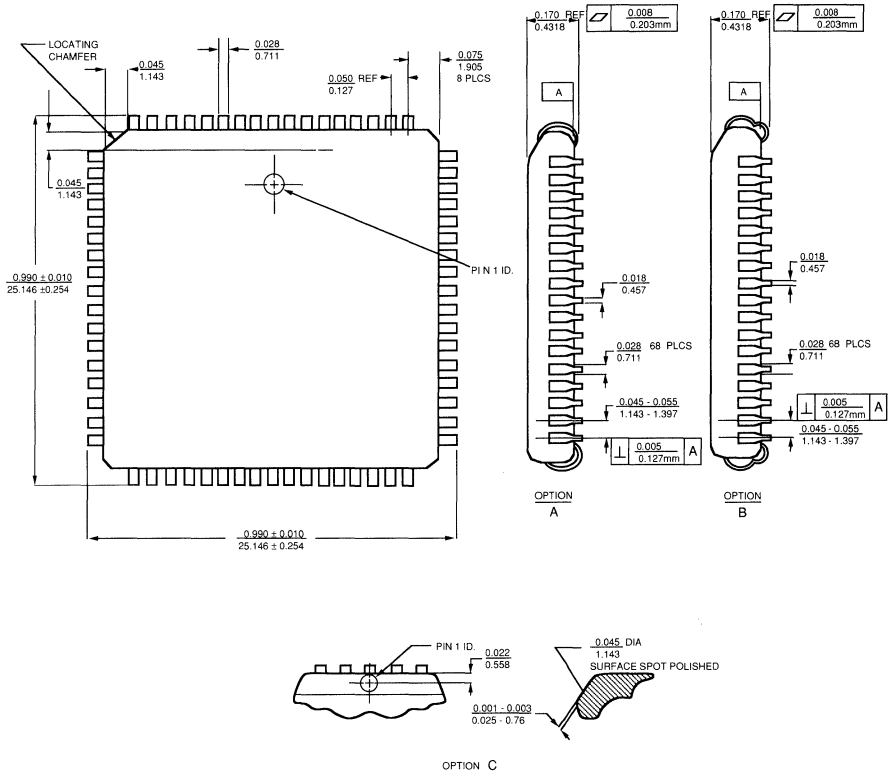


FIGURE D-1. 68-PIN QUAD PLASTIC AND CERAMIC PACKAGE

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WD16C452 Addendum

March 20, 1989

Although the current WD16C452 (first silicon) is fully functional, a second silicon for this device is scheduled to be released shortly. The second silicon will incorporate enhancements and changes so the WD16C452 conforms completely to the current data sheet specification.

The following are the differences between the first and second silicon of the WD16C452:

1. The second silicon will test the V_{IH} threshold to 2.0 volts, as specified in the data sheet. Currently, the V_{IH} threshold is tested to 2.2 volts.

2. The second silicon will test the XTAL1 input leakage to ±10 ua, as specified in the data sheet. Currently, this parameter is tested to ±15 ua.

3. The second silicon will test I_{OH} = -15ma and I_{OL} = 24ma for the parallel port data bus pins. Currently, these pins are tested to I_{OH} = -2ma and I_{OL} = 12ma.

4. The second silicon will test I_{OH} = -.55ma and I_{OL} = 20 ma for the parallel port open drain pins (-INIT, -AFD, -STB, -SLIN). Currently, these pins are tested to I_{OH} = -.2ma and I_{OL} = 10ma.

5. The second silicon will allow the Receiver Holding Register to continually receive characters in the event of an overrun error. The current WD16C452 will not allow characters to enter the Receiver Holding Register in the event of an overrun error

6. The second silicon will support ESD of 1200v or greater, a Western Digital standard. The current WD16C451 silicon passed this standard except pin 14 through pin 21; these pins passed ESD at 400v.

Accordingly, the WD16C552/16C452 datasheets will be updated when the second silicon is released.

Samples of the second silicon are scheduled for early May with full production by late June '89.

Western Digital, Communications Products, 2445 McCabe Way, Irvine, CA 92714, (800) 638-5323

Communications Products

WESTERN DIGITAL

WD16C552 Addendum

March 20, 1989

Although the current WD16C552 (first silicon) is fully functional, a second silicon for this device is scheduled to be released shortly. The second silicon will incorporate enhancements and changes so the WD16C552 conforms completely to the current data sheet specification.

The following are the differences between the first and second silicon of the WD16C552:

1. The second silicon will test the VIH threshold to 2.0 volts, as specified in the data sheet. Currently, the VIH threshold is tested to 2.2 volts.

2. The second silicon will test the XTAL1 input leakage to ±10 ua, as specified in the data sheet. Currently, this parameter is tested to ±15 ua.

3. The second silicon will test IOH = -15ma and IOL = 24ma for the parallel port data bus pins. Currently, these pins are tested to IOH = -2ma and IOL = 12ma.

4. The second silicon will test IOH = -.55ma and IOL = 20ma for the parallel port open drain pins (-INIT, -AFD, -STB, -SLIN). Currently, these pins are tested to IOH = - .2ma and IOL = 10ma.

5. The second silicon will trigger a reset of -RXRDY (TRINT timing) from the leading edge of -IOR, as represented in the data sheet. TRINT timing is currently triggered and measured from the trailing edge of -IOR for reset of -RXRDY (FIFO Mode) or for reset INT (for Receiver Holding Register Interrupt in Character Mode).

6. The second silicon will trigger and measure the TWXI timing from the trailing edge of -IOW to reset of -TXRDY, as represented in the data sheet. TWXI is currently triggered and measured from the leading edge of -IOW, to -TXRDY reset.

7. The second silicon, in character mode, will allow the Receiver Holding Register to continually receive characters in the event of an overrun error. The current WD16C552 will not allow characters to enter the Receiver Holding Register in the event of an overrun error.

8. The second silicon will latch an interrupt when an -ACK parallel port interrupt is received, and clear the interrupt following a read of the parallel port Status Register. The current silicon will not latch the status of the -ACK signal.

9. The second silicon will define bit 2 of the parallel port Status Register as -IRQ. When bit 2 is low (active), the printer has acknowledged the previous transfer using the -ACK signal. Reading the Status Register will clear this bit. Bit 2 of the Status Register is not defined in the current silicon.

10. The second silicon will define bit 5 of the parallel port Control Register as the "Direction" bit. The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus, as described in the table below. Currently, bit 5 of the Control Register is not define.

11. The second silicon will define pin one as BIDEN (Bidirectional Enable). The BIDEN pin will work in conjunction with the Direction Bit to determine the direction of the parallel port data bus, as described in the table below.

PORT MODE	PORT DIRECTION	PIN 1 BIDEN	DIRECTION BIT
EXTENDED	WRITE	1	0
EXTENDED	READ	1	1
COMPATIBLE	WRITE	0	N/A

12. The parallel port of the second silicon , upon a write, will latch the data into the Parallel Port Data Register, but the data will only be presented to the parallel port data bus if the Direction Bit is set to a high (parallel data bus out mode).

    Upon a read operation the data bus will present:

    - The data in the Parallel Port Data Register, if the direction bit is set to a one ("Parallel Data Bus Out" mode)

    - The data currently on the parallel port data bus, if the Direction Bit is set to a zero (Parallel Data Bus In" mode).

    In the current silicon, no Direction Bit exists to allow software controllable port direction

13. The second silicon will support ESD of 1200v or greater, a Western Digital standard. The current WD16C552 silicon passed this standard except pin 14 through pin 21; these pins passed ESD at 400v.

Accordingly, the WD16C452/16C552 datasheet will be updated when the second silicon is released.

Samples of the WD16C552 second silicon are scheduled for late May with full production by early July '89.