PVGA1A

Video Graphics Array Device

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DESCRIPTION

The Paradise Video Graphics Array (PVGA1A) is designed to enhance the VGA subsystem in IBM PC AT Bus or Personal System 2 (PS/2) Micro Channel compatible applications. The AT or Micro Channel Bus interface switch is set through the Configuration Register after power up.

Other improvements, such as an 8/16 bit wide CPU data path, a DRAM controller for up to 1 MB of video memory space, support for an 8/16 bit wide BIOS ROM data path, auto monitor detect input, and a CRT controller for fixed or variable scan analog monitors, are offered as standard features.

1.2 FEATURES

- Provides single Chip Video Graphics Solution for IBM PC / XT / AT and Personal System/2 compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% IBM VGA and EGA BIOS compatible
- 100% CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC / XT / AT, Micro Channel
- High performance FIFO memory architecture
- Includes 8- or 16-bit wide CPU data bus
- 800 by 600 by 16 colors, 640 x 400 x 256 colors
- 640 by 480 by 256 colors (512K DRAM)
- 132 column text modes, with 25, 43, or 50 rows
- Support for external Color Lookup Table (Palette Chip) with 256 Kbyte available colors
- Up to 40 MHz maximum video clock rate
- 1.25 Micron CMOS VLSI technology
- 100 pin Plastic Leadless Chip Carrier (PLCC), or 100 pin Plastic Flat Pack (PFP) JEDEC package
- Minimizes circuit board space requirements.

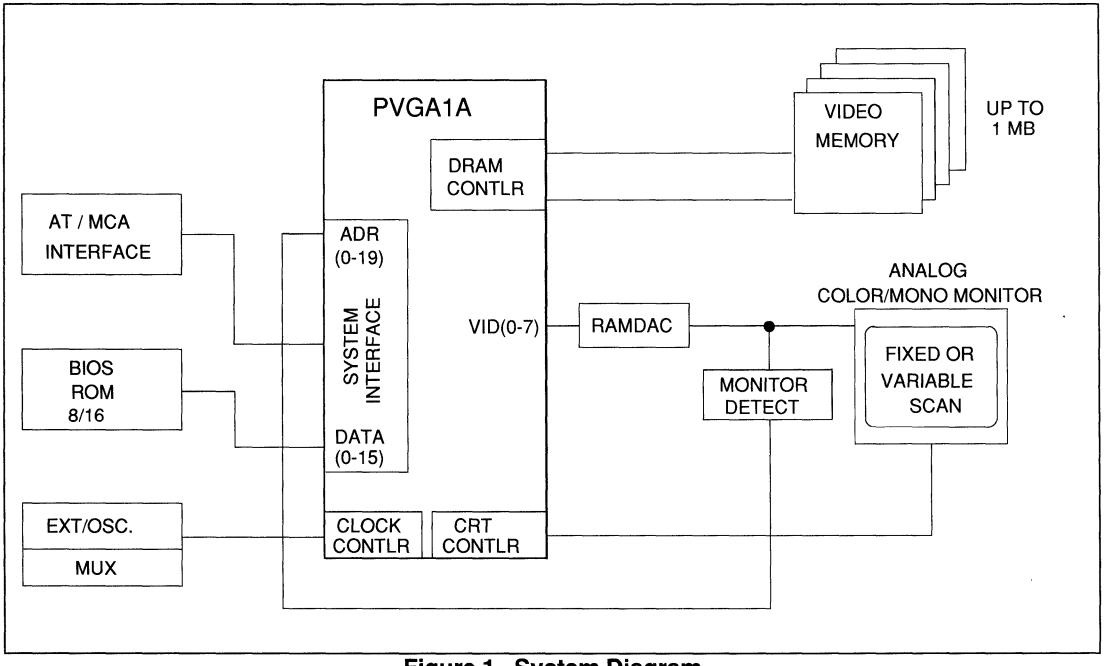

Figure 1. System Diagram

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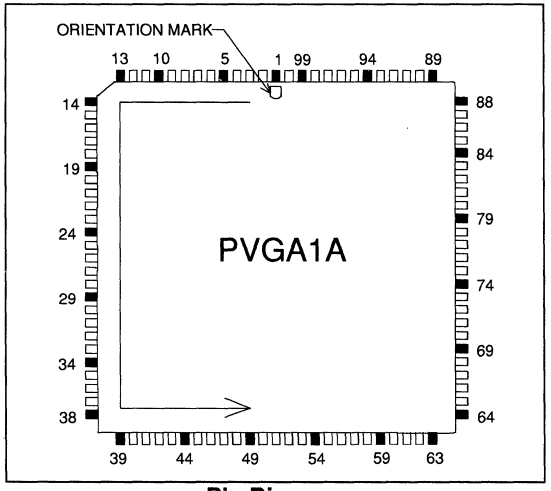
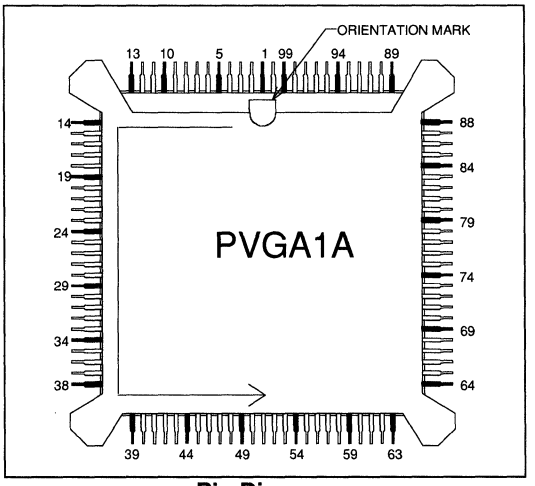


Pin Diagram



Pin Diagram

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	GND	26	GND	51	GND	76	MCLK
2	MD4	27	A18	52	VCC	77	GND
3	MD3	28	A19	53	VID4	78	VCC
4	MD2	29	IORN	54	VID3	79	RAS10N
5	MD1	30	IOWN	55	VID2	80	CAS10N
6	MD0	31	MRDN	56	VID1	81	OE10N
7	EBROMN	32	MWRN	57	VID0	82	RAS32N
8	DS16N	33	EION	58	WPLTN	83	CAS32N
9	BHEN	34	RDY	59	PCLK	84	OE32N
10	SFDBKN	35	IRQ	60	HSYNC	85	WE0N
11	EABUFN	36	RSET	61	VSYNC	86	WE1N
12	DA8	37	DIR	62	BLNKN	87	WE2N
13	DA9	38	EDBUFN	63	MA8	88	WE3N
14	DA10	39	DA0	64	GND	89	MD15
15	GND	40	DA1	65	MA7	90	MD14
16	DA11	41	DA2	66	MA6	91	MD13
17	DA12	42	DA3	67	MA5	92	MD12
18	DA13	43	DA4	68	MA4	93	MD11
19	DA14	44	DA5	69	MA3	94	MD10
20	DA15	45	DA6	70	MA2	95	MD9
21	EMEM	46	DA7	71	MA1	96	MD8
22	A15	47	RPLTN	72	MA0	97	MD7
23	A16	48	VID7	73	VCLK2	98	MD6
24	A17	49	VID6	74	VCLK1	99	MD5
25	VCC	50	VID5	75	VCLK0 1	00	VCC

PVGA1A Pin Descriptions

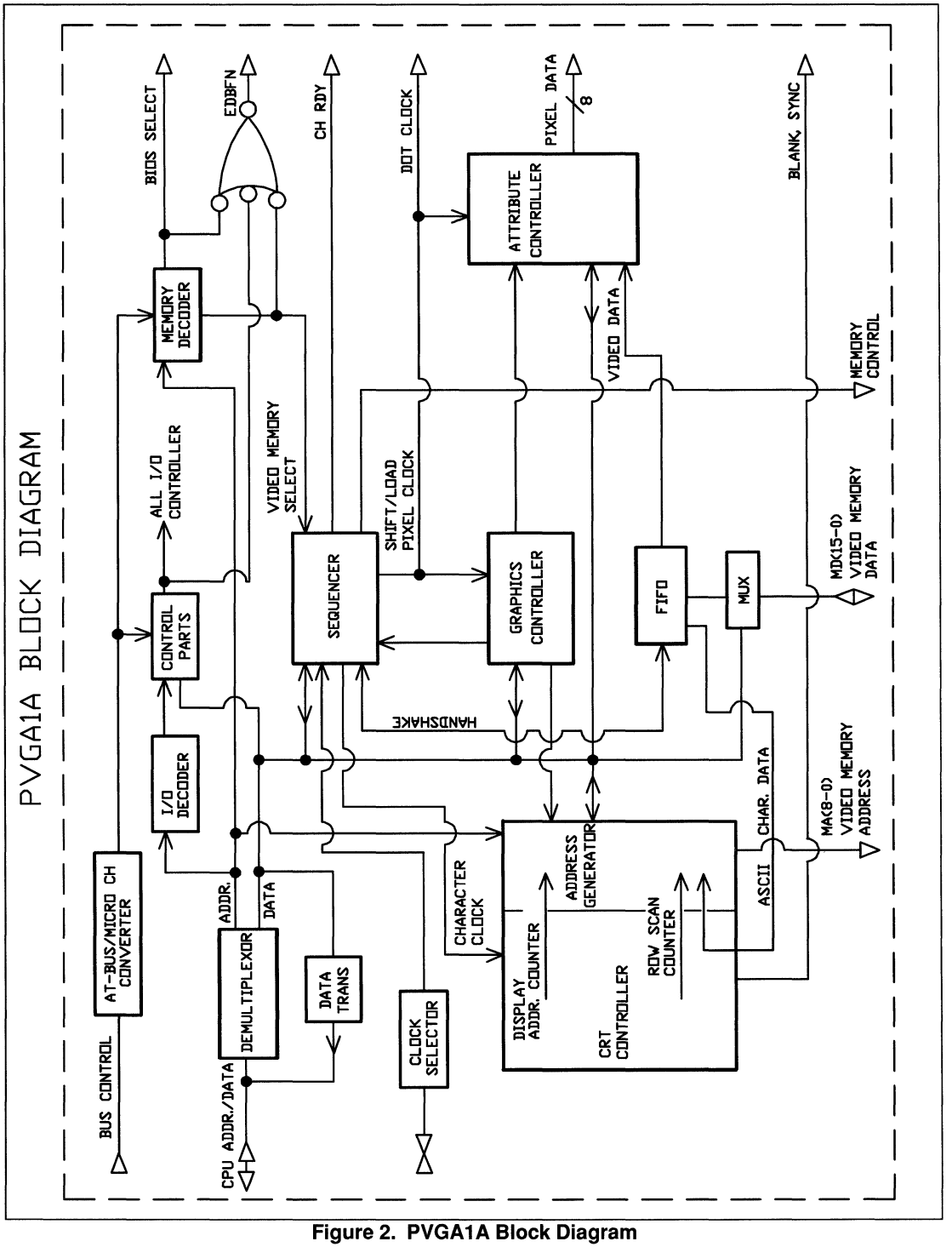


Figure 2. PVGA1A Block Diagram

2.0 SCOPE

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multicolor Graphics Array (MCGA), and the Video Graphics Array (VGA). The Paradise PVGA1A is a 1.25 micron, 12,000 gate CMOS VLSI device that allows the design of a very high performance VGA graphics subsystem able to interface with the PC/XT/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards. A major advantage of the PVGA1A is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, Hercules, AT&T 6300, and VGA hardware and BIOS compatibility, and also EGA BIOS compatibility, on analog or multifrequency monitors.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package mechanical information, and a list of associated references.

2.1 PVGA1A DESCRIPTION

The PVGA1A internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The PVGA1A has 4 major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAMDAC interface.

The PVGA1A internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The PVGA1A has 4 major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAMDAC interface.The PVGA1A controls the interfacing between the system microprocessor and video memory. Because PVGA1A controls arbitration for video memory between the system microprocessor and the CRT Controller function contained within the PVGA1A, all data passes through PVGA1A when the system microprocessor writes to or reads from video memory.

A FIFO is used internally to achieve the video display bandwidth necessary between CPU accesses and display refresh cycles, using standard DRAMs.

2.2 PVGA1A MODULES

The CRT Controller section within the PVGA1A maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The PVGA1A CRT Controller also generates horizontal sync (HSYNC), vertical sync (HSYNC), and blank pulses for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video, and background or foreground video, in VGA and enhanced VGA BIOS modes.

3.0 PVGA1A INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The PVGA1A is designed to operate in two different bus architecture configurations. These are the PC/XT/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the PVGA1A Paradise Register section of this data sheet.

The I/O data path is eight bit. The DRAM display buffer data path can be 8- or 16-bit. EGA Planar modes have an eight bit data path with the CPU. Text modes and 256 color extended modes (packed pixel modes) can have a 16-bit data path if the video subsystem supports a 16-bit bus.

The PVGA1A will provide the necessary waitstates for CPU accesses to the video memory. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports, such as 46E8H(AT) for setup, and 102H for VGA enable, have been implemented internally in the PVGA1A.

When configured for AT or Micro Channel operation, the PVGA1A operates functionally in a manner that is conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The PVGA1A provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8- or 16-bit data path modes. PVGA1A also provides the necessary decoding of the adapter video BIOS ROM, and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 display adapter. Using the provided signals, the user can implement designs able to multiplex the address/data signals to the PVGA1A in 8- or 16-bit mode, control an 8- or 16-bit BIOS ROM, and generate the desired control/handshake signals (such as -MEMCS16 in AT mode).

3.2 DRAM INTERFACE

The PVGA1A optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as 4 planes and the PVGA1A is designed for 3 configurations of DRAMs. Each plane can be configured as 64 Kbytes (256 Kbyte total), 128 Kbytes (512 Kbyte total), or 256 Kbytes (1 Mbyte total). cycles. PVGA1A will also refresh the DRAMs with 3 or 5 refresh cycles (page mode in graphics or RAS refresh in alpha) after every horizontal scan line.

The PVGA1A supports 256 Kbytes of DRAM by using eight 64 Kbyte by 4 page mode DRAM chips; 512 Kbytes of DRAM by using sixteen 64 Kbyte by 4 page mode DRAM chips; or 1 Mbyte of DRAM using eight 256 Kbyte by 4 page mode DRAM chips. Usually a 36 MHz MCLK and 120ns DRAMs are used. A 640 by 400 by 256 color mode is supported when 100 ns DRAMs and a 42 MHz MCLK is used. 640 by 480 by 256 color mode is supported when the 512 Kbyte DRAM configuration along with 100ns DRAMs and a 42 MHz MCLK are used. The PVGA1A Paradise registers provide support for accesses of up to 1 Mbyte of video memory.

The PVGA1A provides the necessary control signals and address/data lines to access the video memory as two 16-bit data interleaved banks. For display refresh cycles, the PVGA1A will perform page mode Read operations on the video memory in graphics modes, and in alpha modes it will generate standard RAS/CAS.

3.3 VIDEO INTERFACE

The PVGA1A is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the PVGA1A provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The PVGA1A can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays. In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to PVGA1A. PVGA1A also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The PVGA1A has four clock input signal pins. These are: the separate memory clock, MCLK, which drives the DRAM timing in graphics modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing and DRAM timing in alphanumeric modes. PVGA1A also provides the option to externally control a multiplexer that supplies the video clock.

3.5 PVGA1A POWER-UP CONFIGURATION

The PVGA1A uses the memory data pins to configure an internal configuration register upon power-up/reset. CNF(2) will determine whether the PVGA1A will operate in AT or Micro Channel bus mode.

Other CNF bits configured by PVGA1A at power-up/reset are used as status bits, or for clock source control. For more information on PVGA1A power-up configuration, refer to the Paradise Register section of this data sheet.

4.0 PIN DESCRIPTION

The table below provides PVGA1A pin definitions for the 100 Pin Plastic Leadless Chip Carrier (PLCC)and Plastic Flat Pack (PFP) package. The PVGA1A mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			POWER ON
36	RSET	I	RESET: This signal input will reset the PVGA1A. MCLK and VCLK0 should be connected to PVGA1A in order for the PVGA1A to initialize during Reset. Paradise registers PR1, and CNF are initialized at power-up reset based on the logic level on the MD7-0 bus as determined by pull-up/ pull-down resistors. Outputs EABUFN and EDBUFN are 3-stated during reset. The reset pulse width should be at least **ten** MCLK clock periods.
			CLOCK SELECTION
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 42.0 MHz for 100 ns DRAMS.
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK2.
			CPU ADDRESS AND DATA BUS
28	A19	I	ADDRESS-ONLY BUS (A15-A19): These active high inputs form the high-order five bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
27	A18	I	
24	A17	I	
23	A16	I	
22	A15	I	
20	DA15(*)	I/O	DATA/ADDRESS BUS (DA0-DA15): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information.
19	DA14	I/O	
18	DA13	I/O	
17	DA12	I/O	
16	DA11	I/O	
14	DA10	I/O	
13	DA9	I/O	
2	DA8	I/O	
46	DA7	I/O	
45	DA6	I/O	
44	DA5	I/O	
43	DA4	I/O	
42	DA3	I/O	
41	DA2	I/O	NOTE : " * "DA15 signal is multiplexed with data bit 15and CRT
40	DA1	I/O	monitor sense input for auto monitor detection. Refer to
39	DA0	I/O	technical brief on auto monitor detection circuit.
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the PVGA1A video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the PVGA1A. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
10	SFDBKN	O	16-BIT WIDE BIOS ROM: In AT mode this active low signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the BIOS ROM chip enable signal MEMCS16 in AT mode. In Micro Channel mode, its mnemonic is -CD SFDBK. -CD SFDBK is the unlatched decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback. For further details, refer to the reference literature.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the MCA or CPU bus cycles during video memory accesses. It is pulled inactive by PVGA1A to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
35	IRQ	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is not connected, but may be connected if desired. -IRQ9 is used to generate interrupt in the Micro Channel mode. For further details, refer to the reference literature and the CPU section in the introduction.
8	DS16N	O	DATA SIZE 16: Active low enable for 16-bit video memory word transfers. It is a mode dependent signal. In AT mode, the signal level is as programmed in bit PR1(2) and may be used to control 16 bit external data buffers. See the Paradise Register (PR1) description for further details. This signal is used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR1(1)) and/or during memory 16-bit data path access (if enabled by PR1(2)). See the section on Paradise Registers or consult the reference literature for more information.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
33	EION	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the PVGA1A. In Micro Channel mode, this signal is the set up input pin and is connected to the card set up or the VGA setup. The externally designed system I/O (96H for Adapter card or 94H bit 5 for system board design) is connected to the EION pin. When this signal is high, the PVGA1A is enabled or in the operating state. An active low signal on this pin puts the PVGA1A into set up mode. During the set up mode, write logic 1 to PVGA1A internal port 102H to awaken the PVGA1A after power on. Refer to application note for more information. When in set up mode, the PVGA1A will only respond to the internal I/O register located at 102H. Accesses to port 3C3H (external) and BIOS ROM addresses are not affected by setup mode, so they can be accessed.
9	BHEN	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates transfer of data on the high byte of the data bus (DA8-D15) when PVGA1A is in 16-bit mode. With address A0, it distinguishes between high byte (DA15-8) and low byte (DA0-7) data transfers. It is not used for I/O transfers in either AT mode or Micro Channel mode.
31	MRDN	I	MEMORY READ: In AT mode, this signal is called -SMEMR and is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-IO) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process. For further details, refer to the reference literature.
32	MWRN	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.
29	IORN	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in 8/16 bit I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
30	IOWN	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write for 8/16 bit I/O write cycles. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
			VIDEO MEMORY DATA
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA (D0-D15): These lines are the data bus to the video display DRAMS. Data lines MD0-7 are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD — Power-Up Function — Affected Register (bit) 7 — General Purpose — CNF(7) * 6 — General Purpose — CNF(6) * 5 — General Purpose — CNF(5) * 4 — General Purpose — CNF(4) * 3 — VCLK1,2 Input/Output — CNF(3) + 2 — AT/Micro Channel Mode — CNF(2) + 1 — BIOS ROM Data Path — PR1(1) * 0 — BIOS ROM Mapping — PR1(0) * NOTE : " * " Pulldown resistor sets these bits to logic 1. " + " Pullup resistor sets these bits to logic 1. For more details refer to the section on Paradise Registers.
			VIDEO MEMORY ADDRESS
63 65 66 67 68 69 70 71 72	MA8 † MA7 † MA6 † MA5 † MA4 † MA3 † MA2 † MA1 † MA0 †	O	MEMORY ADDRESS (MA0-MA8): Display memory DRAM address.

Note: "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
80	CAS10N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	CAS32N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 3 & 2 CAS output signal.
79	RAS10N †	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.
82	RAS32N †	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	OE10N †	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	OE32N †	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	WE0N †	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, lower byte (Memory map 0).
86	WE1N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1).
87	WE2N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	WE3N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3).

Note: "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7 § VID6 § VID5 § VID4 § VID3 § VID2 § VID1 § VID0 §	O	VIDEO (VD0-VD7): Pixel video output to DAC and color palette.
47	RPLTN	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses 3C6H, 3C8H, and 3C9H.
58	WPLTN	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1 or 2 is divided by two in 320/360 pixel display mode to derive PCLK.
62	BLNKN ‡	O	BLANK: Active low display monitor blank pulse.
			CRT CONTROL
60	HSYNC ‡	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming.
61	VSYNC ‡	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register.

Notes: "§" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(5)=1.
"‡" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(6)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			BIOS ROM CONTROL
7	EBROMN	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C0000H-C7FFFH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C6000H-C67FFH. In AT mode only, a write to the PVGA1A internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
			BUFFER CONTROL
11	EABUFN	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing address and data to PVGA1A. It is 3-stated while Reset is active.
38	EDBUFN	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to PVGA1A. It is 3-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the MD0-15 data bus in AT and Micro Channel modes. The default state is low until a read/write cycle occurs. Then the PVGA1A will drive DIR high to change the direction of the data buffers.
			POWER AND GROUND
25	VCC	-----	+5VDC
52	VCC	-----	+5VDC
78	VCC	-----	+5VDC
100	VCC	-----	+5VDC
1	GND	-----	Ground
15	GND	-----	Ground
26	GND	-----	Ground
51	GND	-----	Ground
64	GND	-----	Ground
77	GND	-----	Ground

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	$0^{o}C$ to $70^{o}C$
Storage temperature	$-40^{o}C$ to $125^{o}C$
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0^{o} to $70^{o}C$
Power supply voltage	4.75 to 5.25 Volts

NOTE :

5.1 D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS	NOTE
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 5V +/-5%	
VIH	Input High Voltage	2.0	VCC+0.3	V	VCC = 5V +/-5%	
IIL	Input Low Current	-----	+/-10	uA	VIN = 0.0V	
IIH	Input High Current	-----	+/-10	uA	VIN = VCC	
VOL	Output Low Voltage	-----	0.4	V	IOL +4.0 mA	1
VOH	Output High Voltage	2.4	-----	V	IOH = 4.0 mA	1
IOZ	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC	
ICC	Stand By Current (All Inputs at TTL Levels)	-----	22	mA	VCC = 5.25 VDC TA = $0^{o}C$, Static	
CIN	Input Capacitance	-----	10	pF	FC = 1MHZ	
COUT	Output Capacitance	-----	10	pF	FC = 1MHZ	

1. PVGA1A outputs have 4.0 mA maximum source and sink capability except as follows: RDY = 12.0 mA sink and 4.0 mA source.

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5.2 AC CHARACTERISTICS

I/O READ - AT MODE TIMING DIAGRAM (See Figure 4)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IORN	13	--	
2	Address Hold from IORN Active	4	--	
3	Read Data Valid from IORN Active	--	2Tp+20	1
4	IORN Pulse Width	2Tp+50	--	1
5	Read Data Hold from IORN Inactive	16	--	
6	EABUFN Inactive from IORN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IORN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	DIR Active to IORN Active	--	25	
11	DIR Inactive from IORN Inactive	--	26	
12	RPLTN Active from IORN Active	--	2Tp+34	1,2
13	RPLTN Inactive from IORN Inactive	13	--	2
14	EION Hold from IORN Inactive	5	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 03C6H-03C9H, except 03C7H.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.

** For reference only. RPLTN is in synchronization with MCLK.

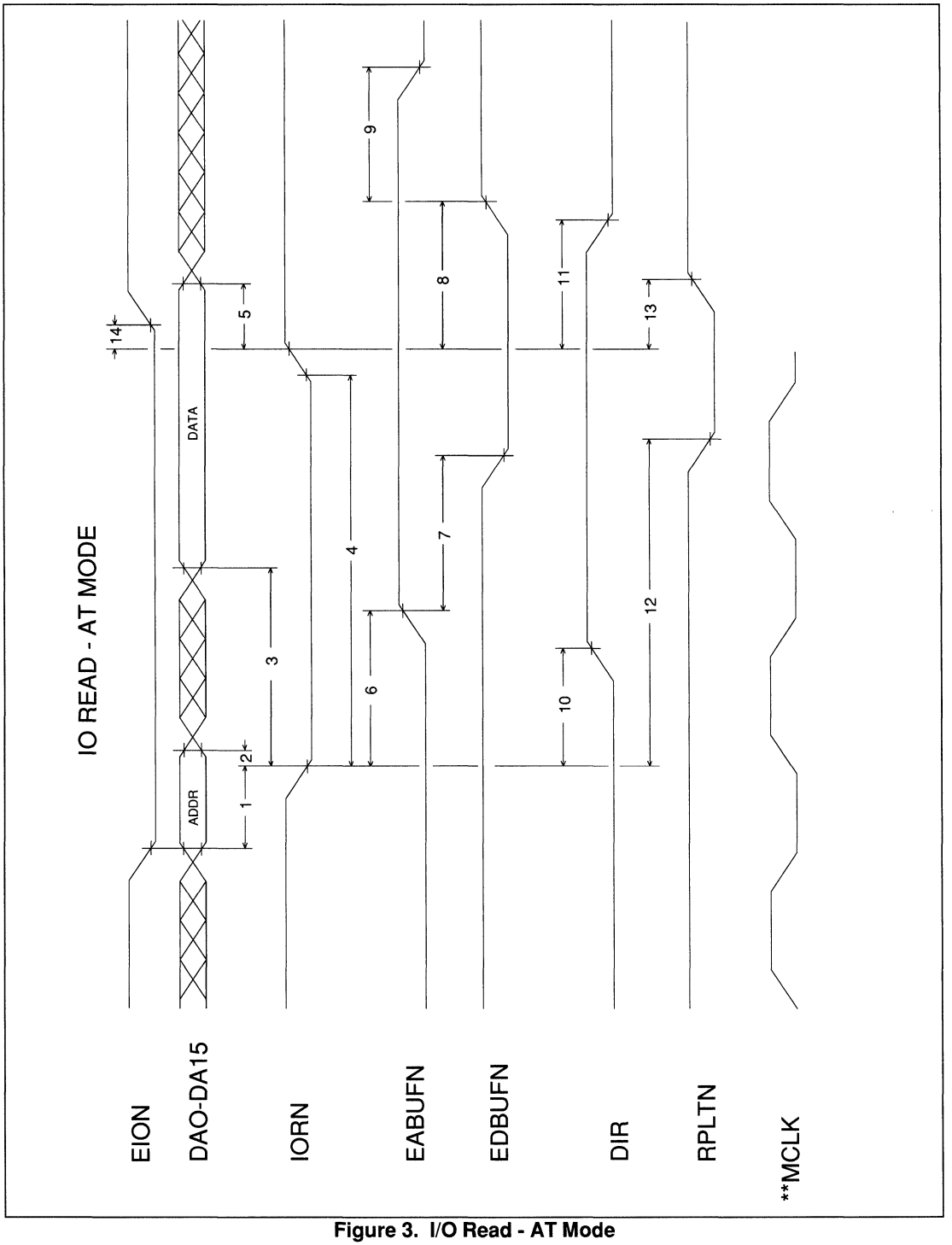

Figure 3. I/O Read - AT Mode

6.0 TIMING DIAGRAMS

6.1 I/O WRITE - AT MODE TIMING DIAGRAM (See Figure 5)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IOWN	13	--	
2	Address Hold From IOWN Active	4	--	
3	Write Data Valid from IOWN Active	--	3Tp-8	1
4	IOWN Pulse Width	3Tp+50	--	1
5	Write Data Hold from IOWN Inactive	16	--	
6	EABUFN Inactive from IOWN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IOWN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	WPLTN Active from IOWN Active	--	3Tp+Tv+15	1,2
11	WPLTN Inactive from IOWN Inactive	16	--	2
12	EION Hold from IOWN Inactive	5	--	
13	EBROMN Active from IOWN Active	--	29	3
14	EBROMN Inactive from IOWN Inactive	--	27	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes. Tv = 2/VCLK0 or 2/VCLK1 or 2/VCLK2 depending on selected video clock.
2. WPLTN signal active only with I/O addresses 03C6H-03C9H.
3. EBROMN signal is active only during I/O port 46E8H write operation.
4. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.

** For reference only. WPLTN is in synchronization with PCLK.

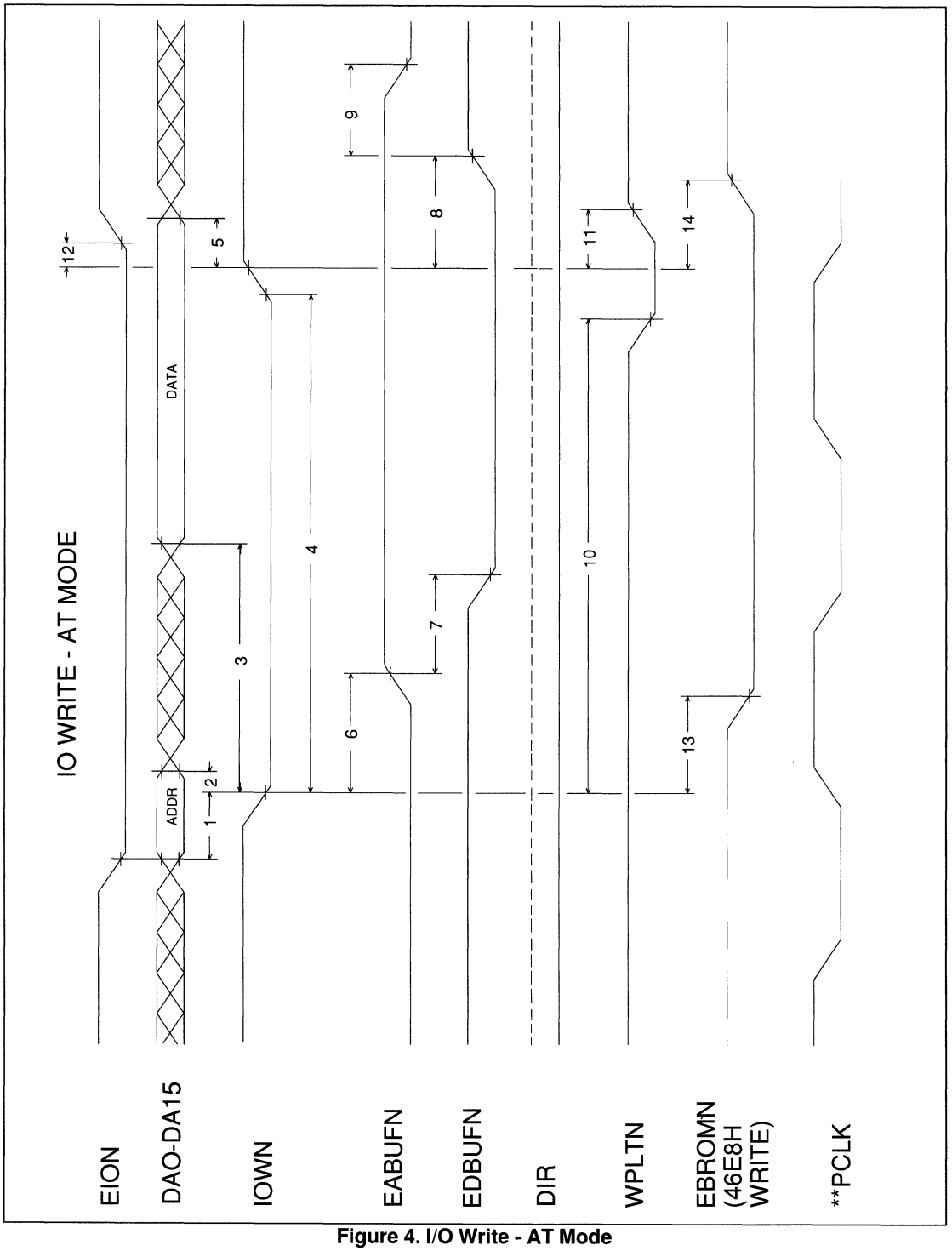

Figure 4. I/O Write - AT Mode

MEMORY READ - AT MODE TIMING DIAGRAM **(See Figure 6)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MRDN	13	--	
2	Address, BHEN Hold from MRDN Active	4	--	
3	Data Valid Setup to RDY	Tp+25	--	5
4	Data Hold from MRDN Inactive	10	--	
5	EABUFN Inactive from MRDN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MRDN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	DIR Active to MRDN Active	--	25	
10	DIR Inactive from MRDN Inactive	--	26	
11	RDY Inactive from MRDN Active	--	18	
12	RDY Active High from MRDN Active	--	2000	
13	RDY Inactive (Tri-state) from MRDN Inactive	--	180	4
14	EBROMN Active from MRDN Active	--	29	2
15	EBROMN Inactive from MRDN Inactive -	-	27	2
16	EMEM Hold from MRDN Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
2. EBROMN signal active for addresses C0000-C7FFFH excluding addresses C6000-C67FFH.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.
4. On AT bus, this signal is tri-state and pulled up to +5V externally.
5. Tp = 1 / MCLK

** For reference only. WPLTN is in synchronization with PCLK

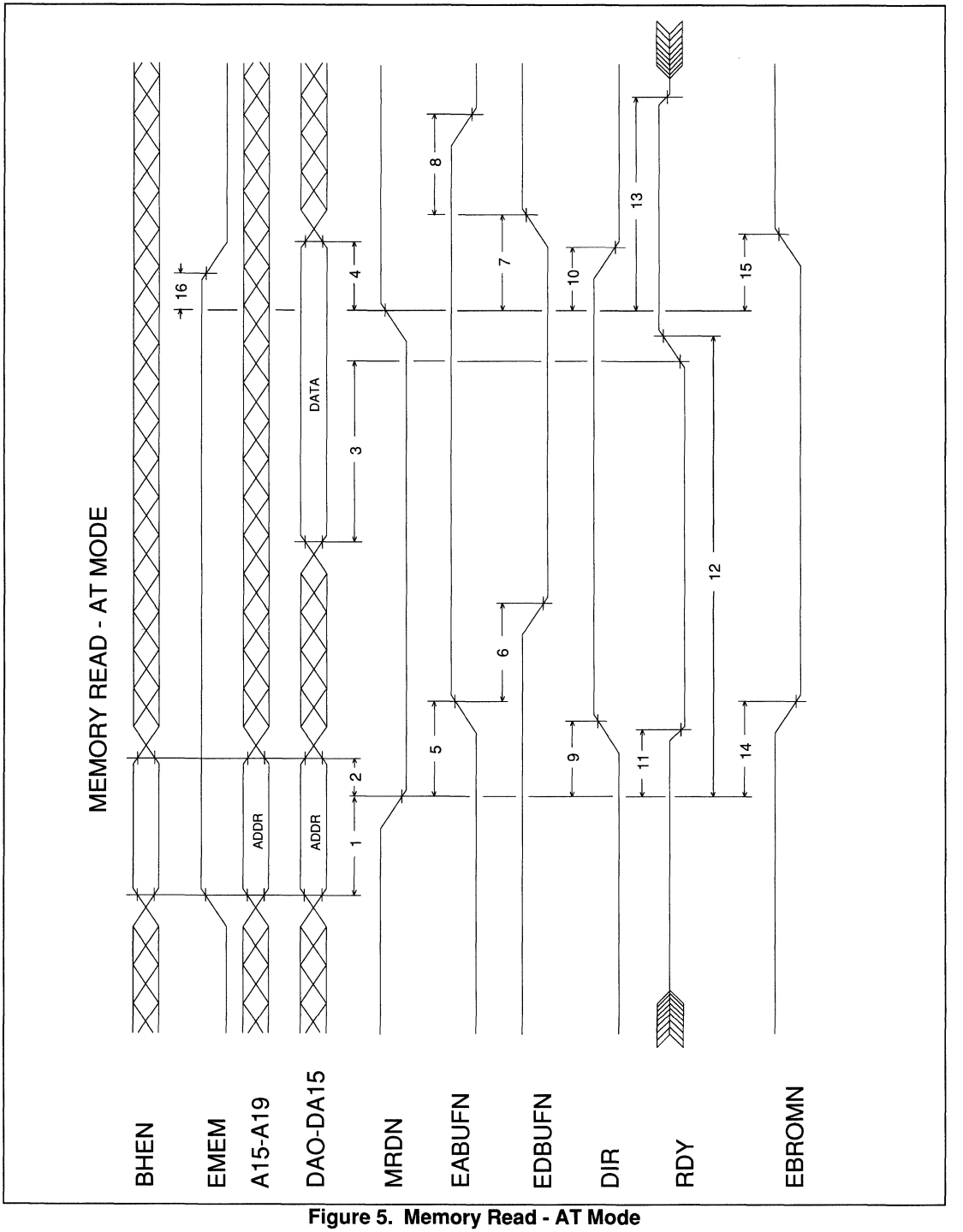

Figure 5. Memory Read - AT Mode

MEMORY WRITE- AT MODE TIMING DIAGRAM **(See Figure 7)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MWRN	13	--	
2	Address, BHEN Hold from MWRN Active	4	--	
3	Data Valid from MWRN Active --		3.5Tp-23	1
4	Data Hold from MWRN Inactive	0	--	
5	EABUFN Inactive from MWRN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MWRN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	RDY Inactive from MWRN Active	--	18	
10	RDY Active High from MWRN Active	--	2000	2
11	RDY Inactive (Tri-state) from MWRN Inactive	--	180	4
12	EMEM Hold from MWRN Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.
4. On AT bus, this signal is tri-state and pulled up to +5V externally.

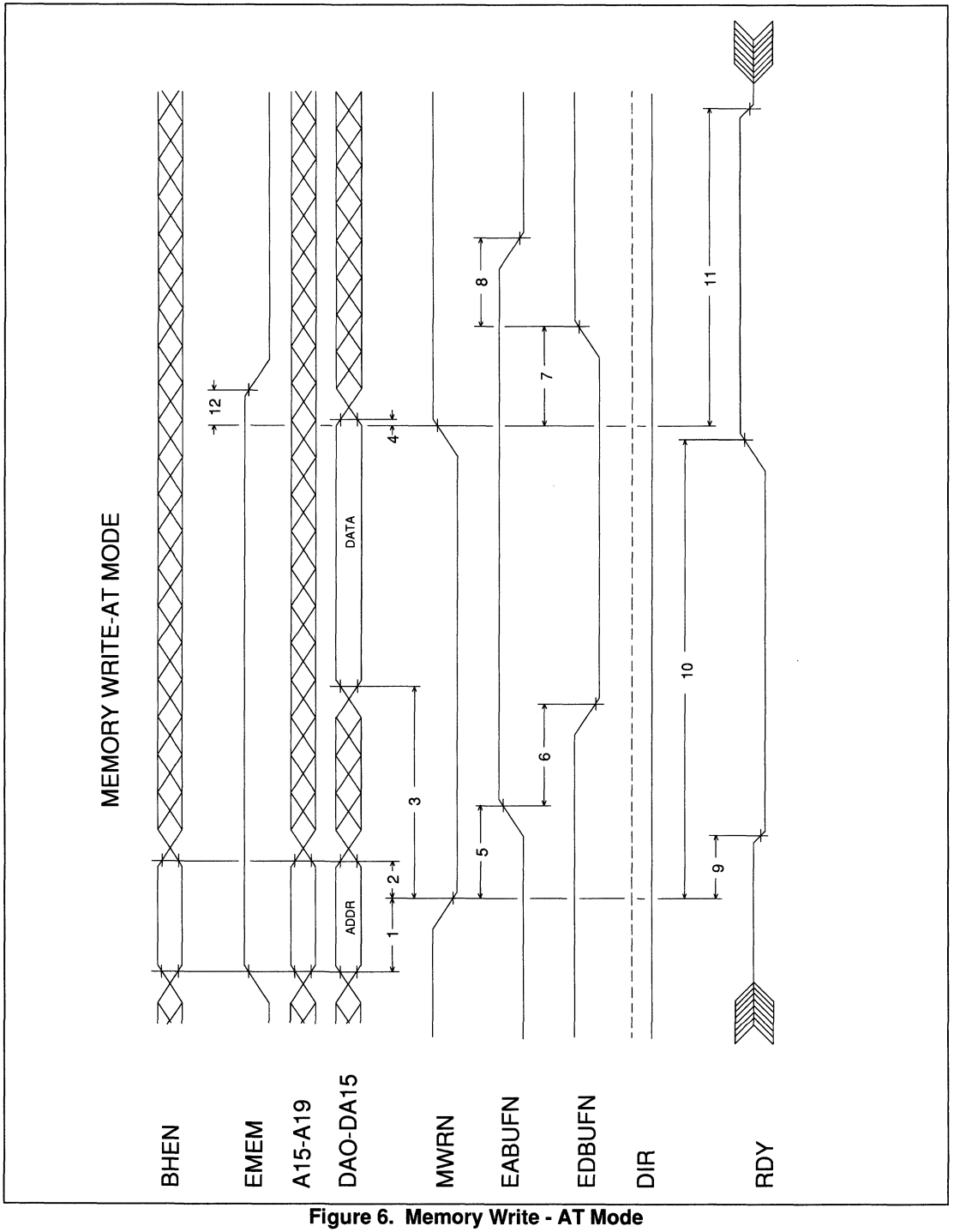

Figure 6. Memory Write - AT Mode

6.2 I/O READ - MICRO CHANNEL MODE TIMING DIAGRAM(See Figure 8)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Active	4	--	
5	-S1 Active to -CMD Active	3	--	
6	-S1 and M/IO Inactive from -CMD Active	5	--	
7	Read Data Valid from -CMD Active	--	2Tp+22	1
8	Read Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	2Tp+50	--	1,5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Iactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RPLTN Active from -CMD Active	--	2Tp+36	1,2
18	RPLTN Inactive from -CMD Inactive	13	--	2
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
20	SFDBKN Inactive from -CMD Inactive	--	32	4
21	-CD SETUP Active to -CMD Active	13	--	3
22	-CD SETUP Inactive from -CMD Inactive	4	--	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 03C6H-03C9H, except 03C7H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.
5. Read operation is internally delayed by two Tp clocks.
6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

** For reference only. RPLTN is in synchronization with MCLK.

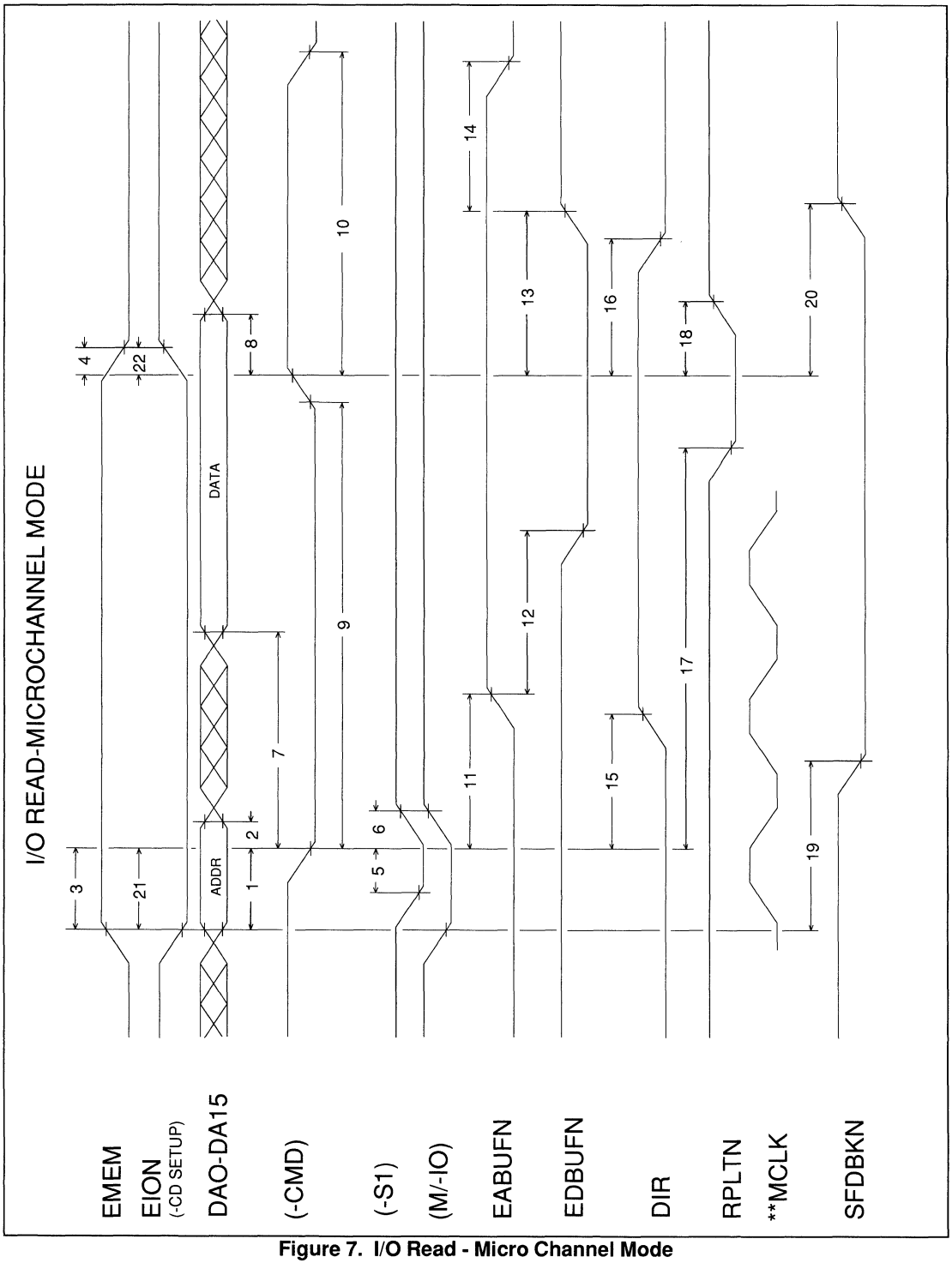

Figure 7. I/O Read - Micro Channel Mode

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I/O WRITE - MICRO CHANNEL MODE TIMING DIAGRAM(See Figure 9)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Inactive	4	--	
5	-S0 Active to -CMD Active	3	--	
6	-S0 and M/IO Inactive from -CMD Active	5	--	
7	Write Data from -CMD Active	--	3Tp-10	1
8	Write Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	3Tp+50	--	1,5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	WPLTN Active from -CMD Active	--	3Tp+Tv+17	1,2
16	WPLTN Inactive from -CMD Inactive	18	--	2
17	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
18	SFDBKN Inactive from -CMD Inactive	--	32	4
19	-CD SETUP Active to -CMD Active	13	--	3
20	-CD SETUP Inactive from -CMD Active	4	--	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes. Tv = 2/VCLK0 or 2/VCLK1 or 2/VCLK2 depending on selected video clock.
2. WPLTN signal active only with I/O addresses 03C6H-03C9H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.
5. Write operation is internally delayed three Tp clocks.
6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

** For reference only. WPLTN is in synchronization with PCLK.

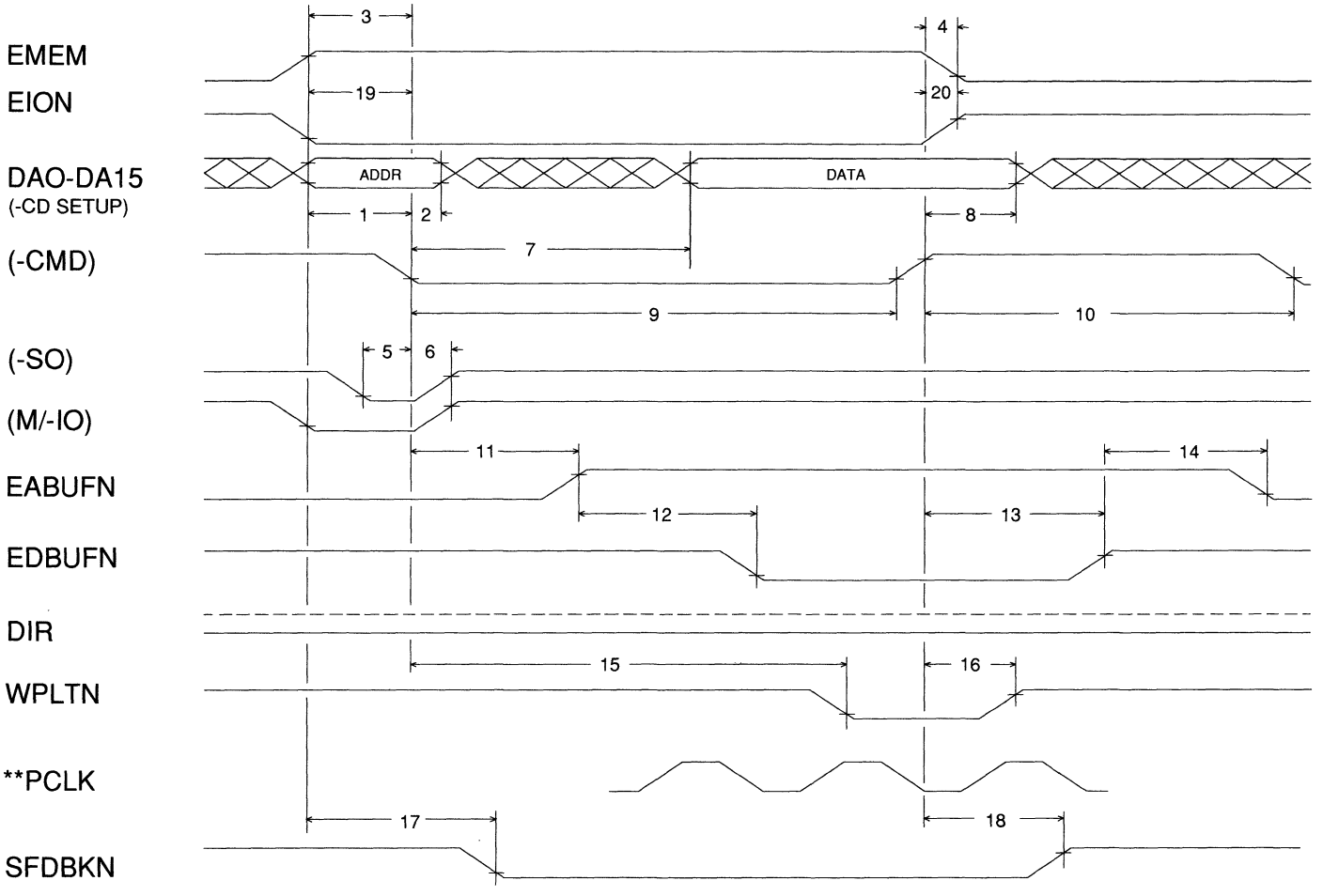

Figure 8. I/O Write - Micro Channel Mode

MEMORY READ - MICRO CHANNEL MODE TIMING DIAGRAM (See Figure 10)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	4	--	
3	BHEN, EMEM, M/IO Setup to -CMD Active	13	--	
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S1 Active to -CMD Active	3	--	
6	-S1 Hold from -CMD Active	5	--	
7	Read Data Valid Setup to RDY	Tp+25	--	5
8	Read Data Hold from -CMD Inactive	11	--	
9	-CMD Pulsewidth	2Tp+50	--	5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RDY Inactive from Active Status	--	27	
18	RDY Active High from -CMD Active	--	2000	1
19	RDY Inactive (Tri-state) from -CMD Inactive	--	180	7
20	EBROMN Active from -CMD Active	--	31	2
21	EBROMN Inactive from -CMD Inactive	--	29	2
22	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
23	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
24	SFDBKN Inactive from Address, M/IO, EMEM Invalid	--	32	
25	EMEM and M/IO Inactive from -CMD Inactive	5	--	4
26	Address, Hold from -CMD Inactive	4	--	

NOTES: * Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1 Duration of RDY signal inactive is dependent on video memory access contention and phase of clock. The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.

2 EBROMN signal active for addresses C0000-C7FFFH excluding addresses C6000-C67FFH.

3 DS16N signal active only for 16-bit access to memory and ROM addresses.

4 M/-IO, EMEM, & A15-A19 have to be latched during the command active period for the PVGA1A in 16 bit interface mode.

5 Tp = 1 / MCLK

6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

7 For Micro Channel mode, this signal is tri-state. It is pulled up externally through a resistor to +5V.

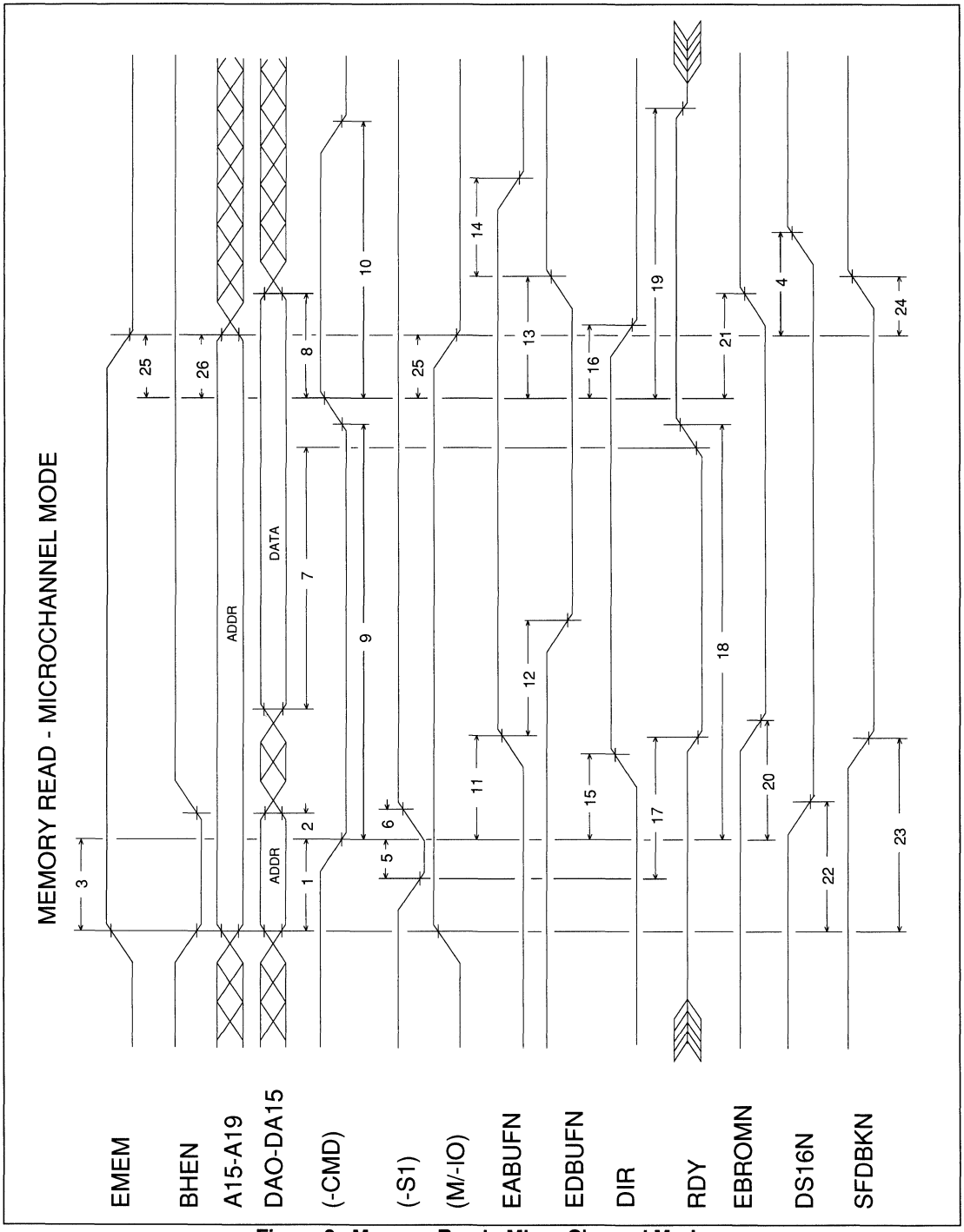

Figure 9. Memory Read - Micro Channel Mode

MEMORY WRITE - MICRO CHANNEL MODE TIMING DIAGRAM (See Figure 11)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	4	--	
3	BHEN,EMEM, M/IO Setup to -CMD Active	13	--	
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S0 Active to -CMD Active	3	--	
6	-S0 Hold from -CMD Active	5	--	
7	Write Data Valid from -CMD Active	--	3.5Tp-23	1
8	Write Data Hold from -CMD Inactive	0	--	
9	-CMD Pulsewidth	3Tp+50	--	1
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	RDY Inactive from Active Status	--	27	
16	RDY Active High from -CMD Active	--	2000	2
17	RDY Inactive (Tri-state) from -CMD Inactive	--	180	6
18	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
20	SFDBKN Inactive from, Address, M/IO, EMEM Invalid	--	32	
21	EMEM, and M/IO Inactive from -CMD Inactive	5	--	4
22	Address, Hold from -CMD Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
3. DS16N signal active only for 16-bit access to memory and ROM addresses.
4. M/-IO, EMEM, & A15-A19 have to be latched during the command active period for the PVGA1A in 16 bit interface mode.
5. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.
6. For Micro Channel mode, this signal is (tri-state). It is pulled up externally through a resistor to +5V.

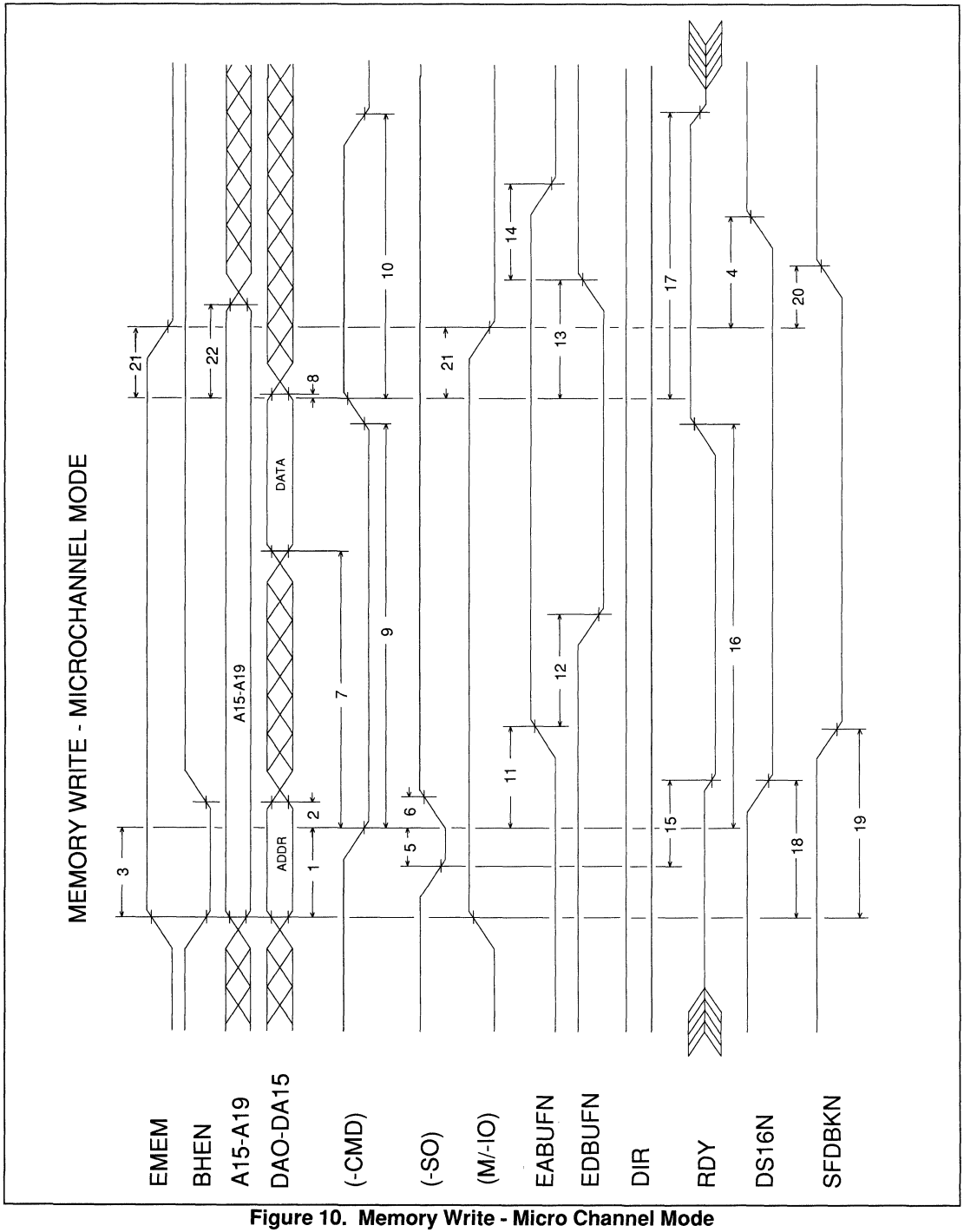

Figure 10. Memory Write - Micro Channel Mode

6.3 VIDEO MEMORY READ - ALPHA MODE TIMING DIAGRAM (See Figure 12)

SYMBOL	PARAMETER	MIN		MAX	NOTES*+
1	Row Address Valid from Clock Low	--		34	1
2	Column Address Valid from Clock High	--		34	1
3	RAS Active from Clock High	--		39	1
4	RAS Inactive from Clock high	--		37	1
5	CAS Active from Clock Low	--		41	1
6	CAS Inactive from Clock Low	--		37	1
7	Read Data Setup to CAS	20	--		
8	Read Data Hold from CAS	0	--		
9	Output Enable Active from Clock Low	--		54	1
10	Output Enable Inactive from Clock Low	--		39	1
11	RAS Refresh Cycle Period	--		7Tp	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. In refresh cycle, RAS period is 4 clocks active and 3 clocks for precharge.
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.
4. Tp = 1 / CLOCK (See note 1.)

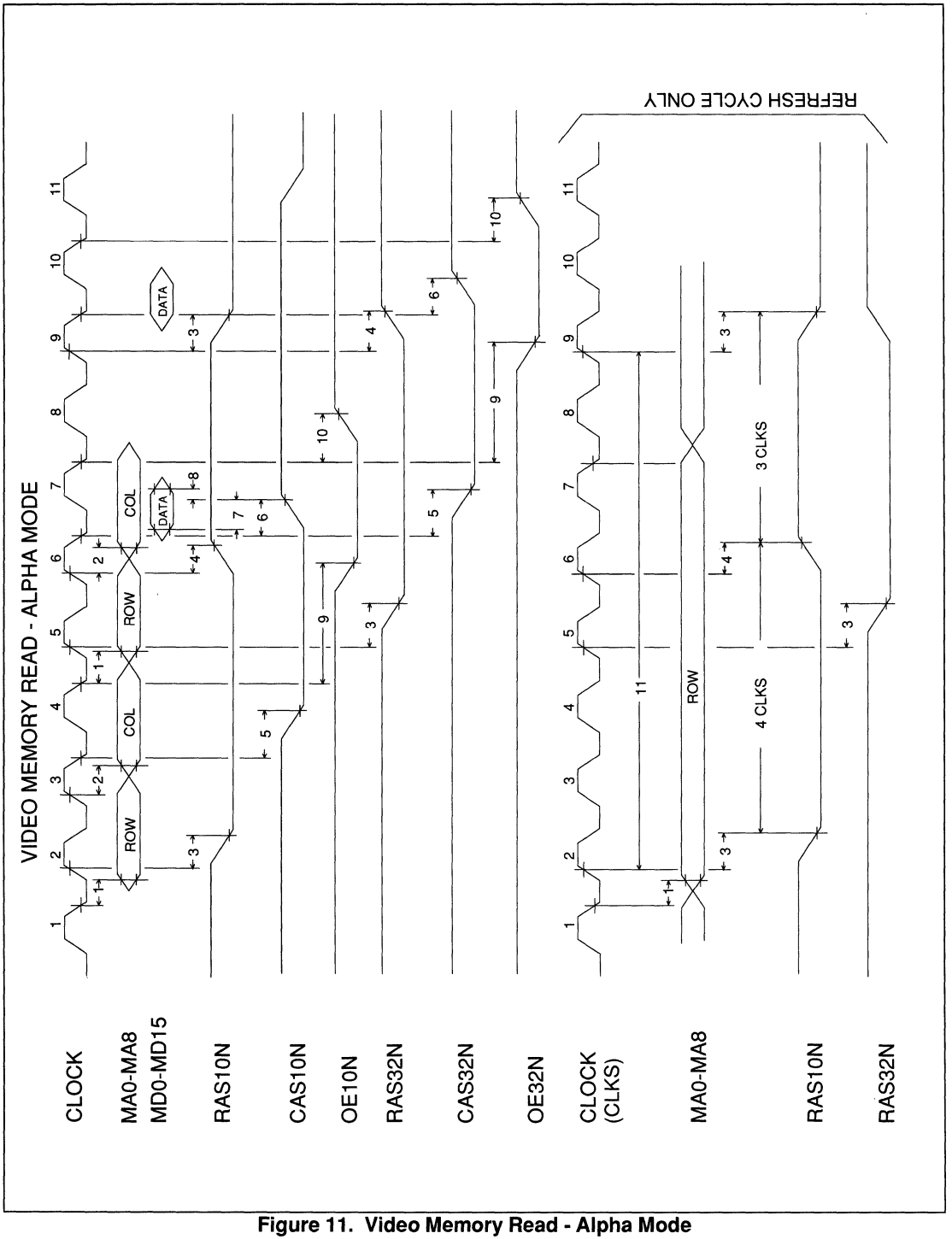

Figure 11. Video Memory Read - Alpha Mode

VIDEO MEMORY WRITE - ALPHA MODE TIMING DIAGRAM (See Figure 13)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	34	1
2	Column Address Valid from Clock High	--	34	1
3	RAS Active from Clock High	--	39	1
4	RAS Inactive from Clock High	--	37	1
5	CAS Active from Clock Low	--	41	1
6	CAS Inactive from Clock Low	--	37	1
7	Write Data Setup to Write Enable	1.5Tp-5	--	1,2
8	Write Data Hold from Write Enable	2Tp	--	1,2
9	Write Enable Active from Clock Low	--	54	1
10	Write Enable Inactive from Clock Low	--	57	1

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. Tp = 1/CLOCK (See Note 1.)
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

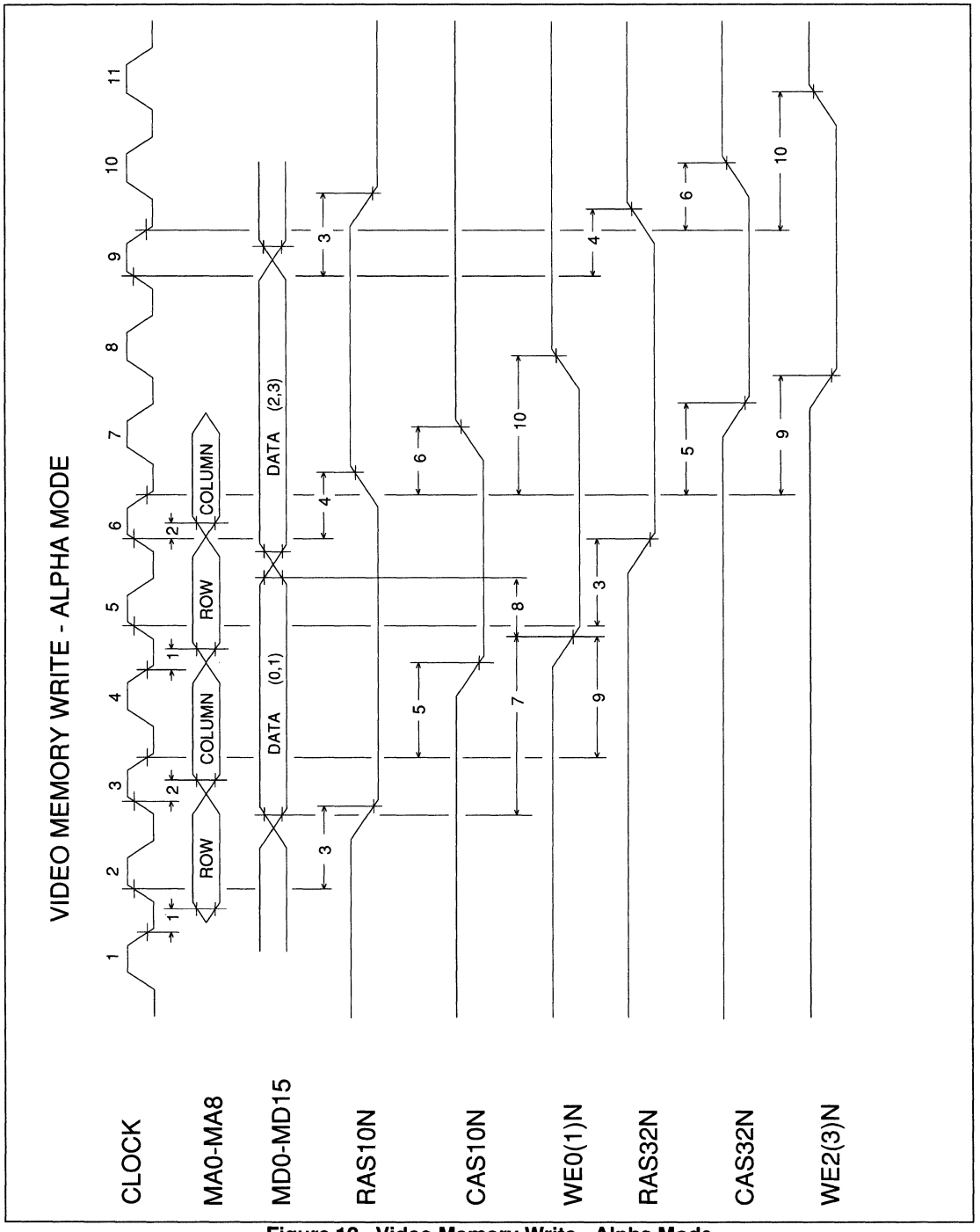

Figure 12. Video Memory Write - Alpha Mode

VIDEO MEMORY READ - GRAPHICS MODE TIMING DIAGRAM (See Figure 14)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1
2	Column Address Valid from Clock High	--	35	1
3	RAS Active from Clock High	--	36	1
4	RAS Inactive from Clock Low	--	34	1
5	CAS Active from Clock	--	36	1,3
6	CAS Inactive from Clock	--	34	1,3
7	Read Data Setup to CAS	20	--	
8	Read Data Hold from CAS	0	--	
9	Output Enable Active from Clock	--	36	1
10	Output Enable Inactive from Clock	--	34	1
11	RAS Refresh Cycle Period	--	10Tp	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. In refresh cycle, RAS period is 6.5 clocks active and 3.5 clocks for precharge.
3. CAS10N is referenced to Clock Low and CAS32N to Clock High.
4. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

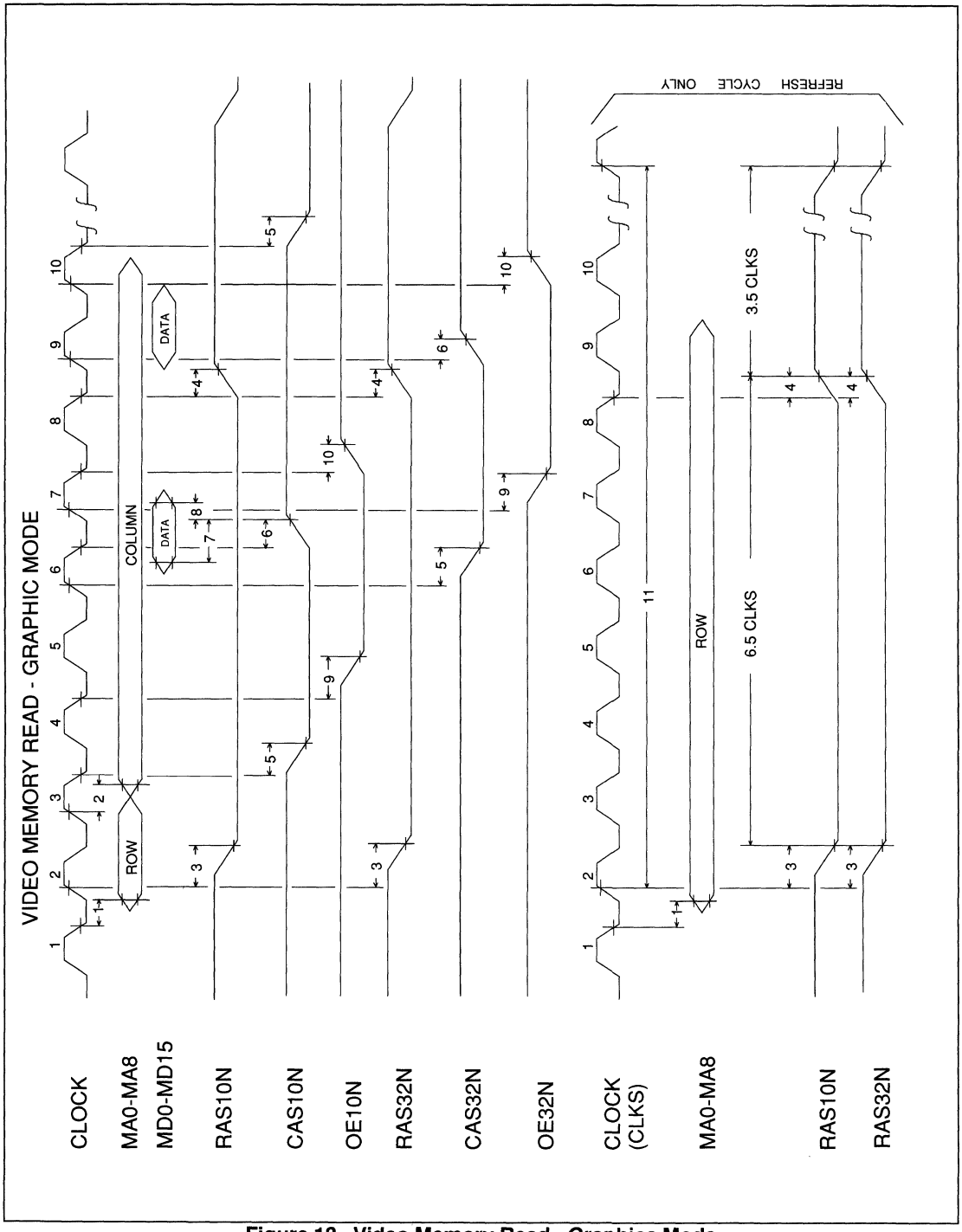

Figure 13. Video Memory Read - Graphics Mode

VIDEO MEMORY WRITE - GRAPHICS MODE TIMING DIAGRAM (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1
2	Column Address Valid from Clock High	--	35	1
3	RAS Active from Clock High	--	36	1
4	RAS Inactive from Clock Low	--	34	1
5	CAS Active from Clock	--	36	1,3
6	CAS Inactive from Clock	--	34	1,3
7	Write Data Setup to Write Enable	1.5Tp-5	--	1,2
8	Write Data Hold from Write Enable	1.5Tp	--	1,2
9	Write Enable Active from Clock	--	50	
10	Write Enable Inactive from Clock	--	48	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. Tp = 1/CLOCK (See Note 1.)
3. CAS10N is referenced to Clock Low and CAS32N to Clock High.

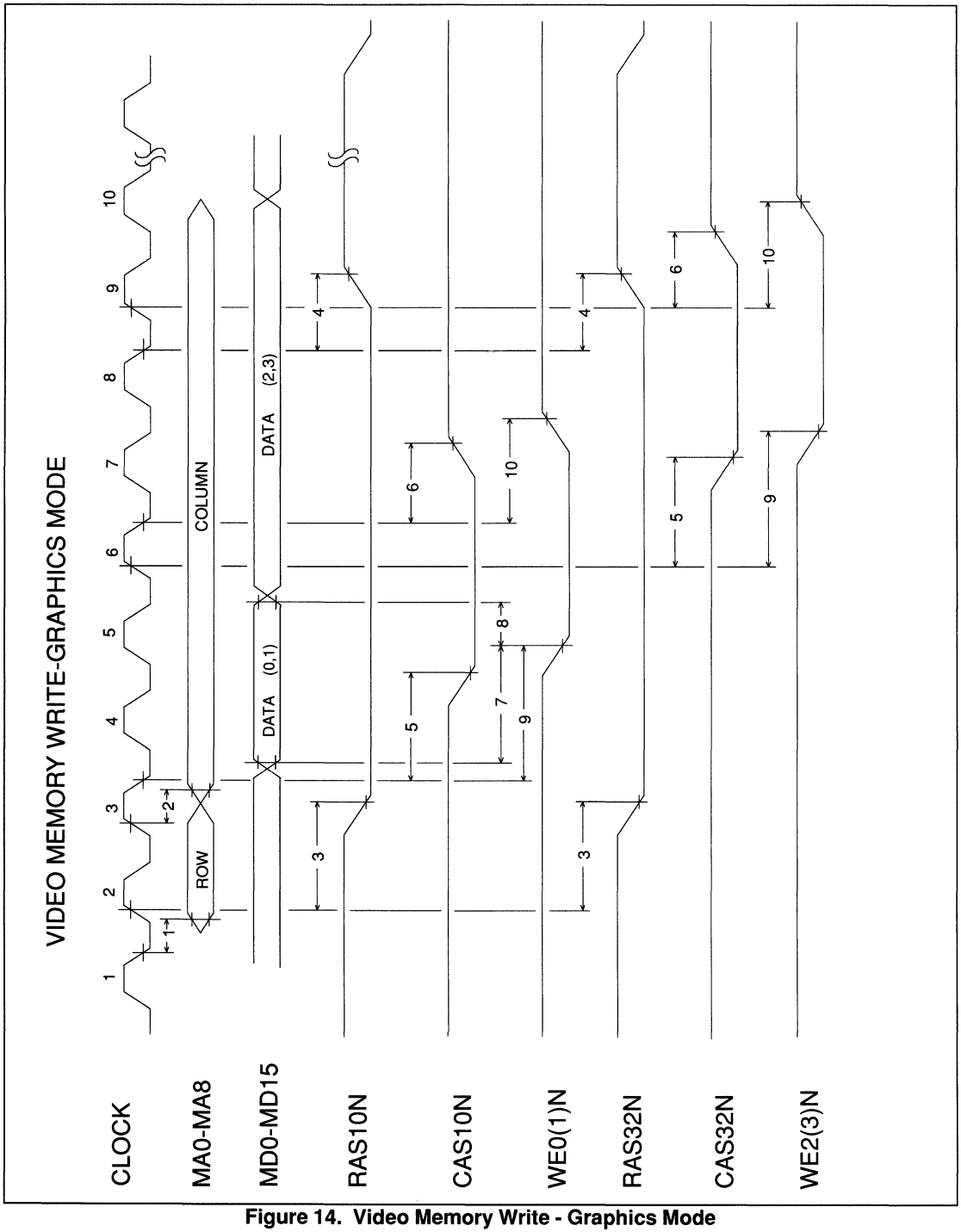

Figure 14. Video Memory Write - Graphics Mode

VIDEO MEMORY PAGE READ - GRAPHICS MODE TIMING DIAGRAM (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1,2
2	Column Address Valid from Clock High	--	35	1,2
3	RAS Active from Clock High	--	36	1,2
4	RAS Hold from Clock Low	--	34	1,2
5	CAS Active from Clock Low	--	36	2
6	CAS Hold from Clock High	--	34	2
7	Output Enable Active from Clock Low	--	36	2
8	Data Hold from CAS	0	--	
9	Data setup from CAS	22	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode.
2. See Video Memory Read - Graphics Timing Diagram.
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

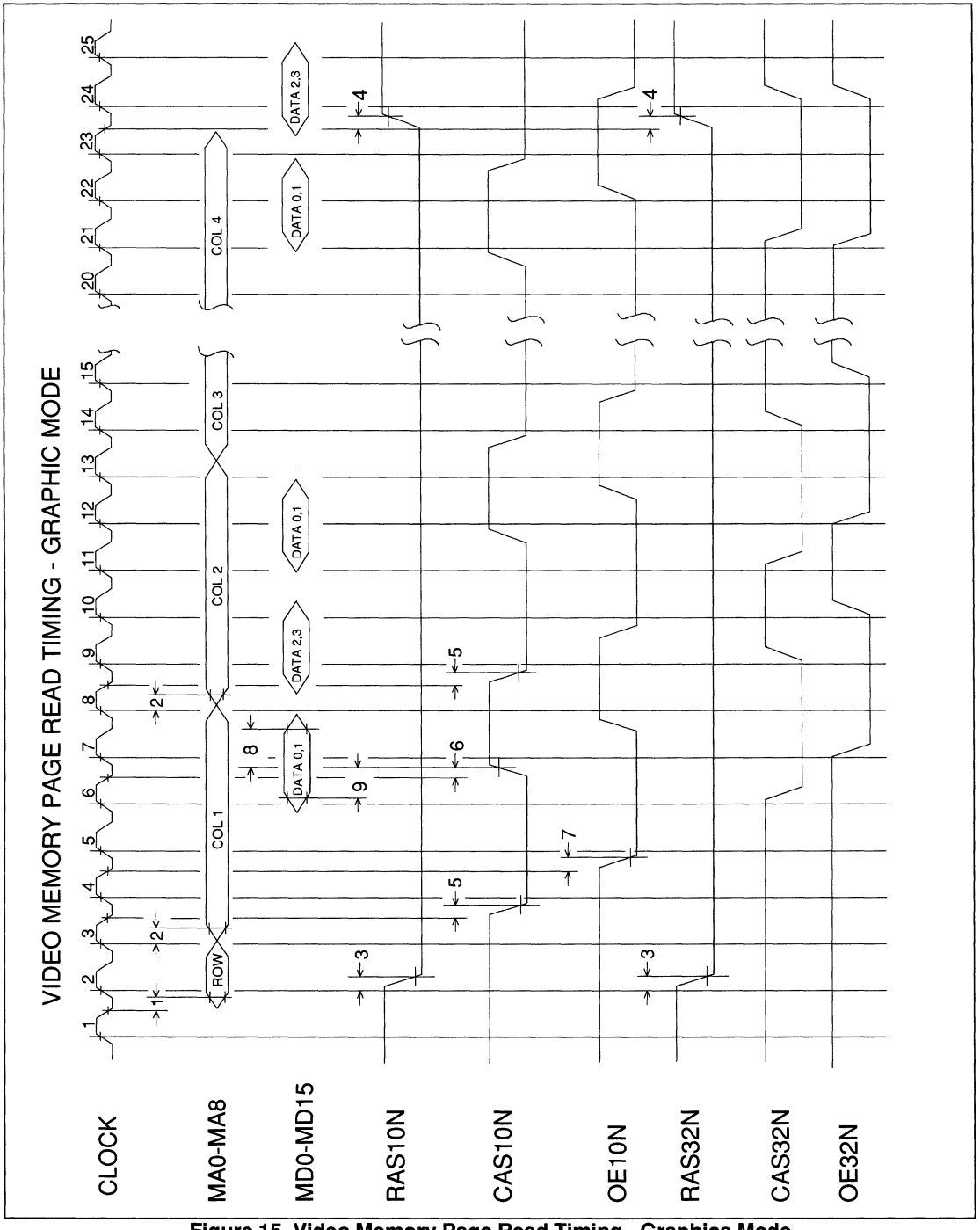

Figure 15. Video Memory Page Read Timing - Graphics Mode

6.4 CLOCK AND VIDEO SIGNALS TIMING DIAGRAM(See Figure 17)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	MCLK Clock Period	23.8	--	1
2	MCLK Clock High Time	10.7	--	
3	MCLK Clock Low Time	10.7	--	
4	VCLK0, VLCK1, VCLK2 Clock Period	25	--	1
5	VCLK0, VLCK1, VCLK2 Clock Low Time	11.2	--	
6	VCLK0, VLCK1, VCLK2 Clock High Time	11.2	--	
7	PCLK Low from VCLK High	--	30	5
8	BLNKN Active Delay from VCLK	--	37	
9	BLNKN Inactive Delay from VCLK	--	38	
10	VSYNC Active Delay from VCLK	--	37	2
11	VSYNC Inactive Delay from VCLK	--	37	2
12	HSYNC Active Delay from VCLK	--	34	2
13	HSYNC Inactive Delay from VCLK	--	38	2
14	VID(7:0) Data from VCLK	--	30	5

NOTES:

* Units are in nanoseconds (ns)

1. Input clocks require a 50% duty cycle with a tolerance of 10 %.
2. VSYNC and HSYNC polarity is positive or negative depending on video mode.
3. PCLK / 2 is for 40 x 25 alpha modes or 320 x 200 x 256 color graphics modes.
4. C_L for VID(0:7) and PCLK is 30 pF.
5. There is a limit on the maximum skew between video clock and data outputs. With respect to the falling edge of PCLK, the delay of VID(0:7) output will not exeed + / - 5ns at 1.4V output level.
6. Duty cycle variations from VCLK to PCLK:
   Values are referenced to a input 50% waveform from 0.8V to 2.0V, 30pF load, and 1.3V threshold.
   High pulse width = Input width - 1.5ns Min
   Input width + 3.2ns Max
   Low pulse width = Input width - 3.2ns Min
   Input width + 1.5ns Max

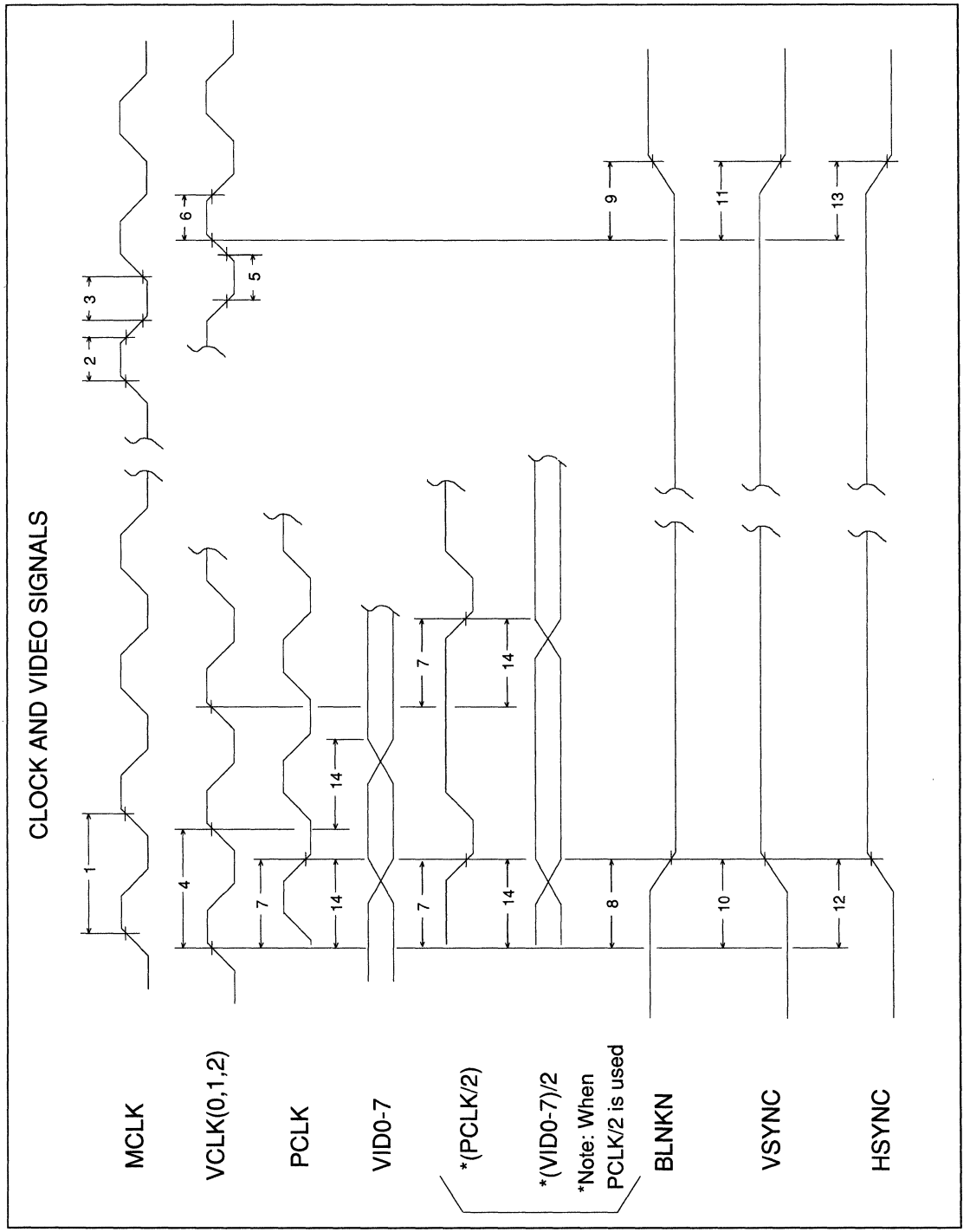

Figure 16. Clock and Video Signals

7.0 PVGA1A REGISTERS

All the standard IBM registers incorporated inside the PVGA1A are functionally equivalent to the VGA implementation while additional Paradise registers enhance the VGA video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail followed by the Paradise register description. For more information, refer to the reference literature.

VGA REGISTERS SUMMARY

	R/W	Monochrome	Color	Either
General Registers:				
Miscellaneous Output Reg	W			03C2
	R			03CC
Input Status Reg 0	RO			03C2
Input Status Reg 1	RO	03BA	03DA	
Feature Control Reg	W	03BA	03DA	
	R			03CA
‡Video Subsystem Enable	RW			03C3
Sequencer Registers:				
Sequencer Index Reg	RW			03C4
Sequencer Data Reg	RW			03C5
CRT Controller Registers:				
Index Reg	RW	03B4	03D4	
CRT Controller Data Reg	RW	03B5	03D5	
Graphics Controller Registers:				
Index Reg	RW			03CE
Other Graphics Reg	RW			03CF
Attribute Controller Registers:				
Index Reg	RW			03C0
Attribute Controller Data Reg	W			03C0
	R			03C1

NOTES: 1. **RO** = Read-Only, **RW** = Read/Write, **WO** = Write-Only. All Register addresses are in hex.
2. ‡ = Video Subsystem Enable Register 03C3 is to be implemented externally since it is not present inside the PVGA1A for Microchannel implementations.

PARADISE REGISTERS SUMMARY

	R/W	Monochrome	Color
Paradise Register Index	R/W	-----	03CE
PR0(A) Address Offset A	R/W	-----	03CF.09
PR0(B) Address Offset B	R/W	-----	03CF.0A
PR1 Memory Size	R/W	-----	03CF.0B
PR2 Video Select	R/W	-----	03CF.0C
PR3 CRT Control	R/W	-----	03CF.0D
PR4 Video Control	R/W	-----	03CF.0E
PR5 Lock/Status	R/W	-----	03CF.0F
** CNF Configuration	-----	-----	-----

COMPATIBILITY REGISTERS SUMMARY

	R/W	MDA	CGA	AT&T	Hercules
Mode Control Reg	WO	03B8	03D8	03D8	03B8
Color Select Reg	WO	-----	03D9	03D9	-----
Status Reg	RO	03BA	03DA	03DA	03BA
Preset Light Pen Latch	WO	03B9	03DC	03DC	-----
Clear Light Pen Latch	WO	03BB	03DB	03DB	-----
AT&T / M24 Reg	WO	-----	-----	03DE	-----
Hercules Reg	WO	-----	-----	-----	03BF
+ CRTC	RW	03B0-03B7	03D0-03D7	03D0-03D7	03B0-03B7

NOTES:
1. **RO** = Read-Only, **RW** = Read/Write, **WO** = Write-Only. All Register addresses are in hex.
2. **+** = 6845 Mode Registers
3. ** = This register is loaded during power on.

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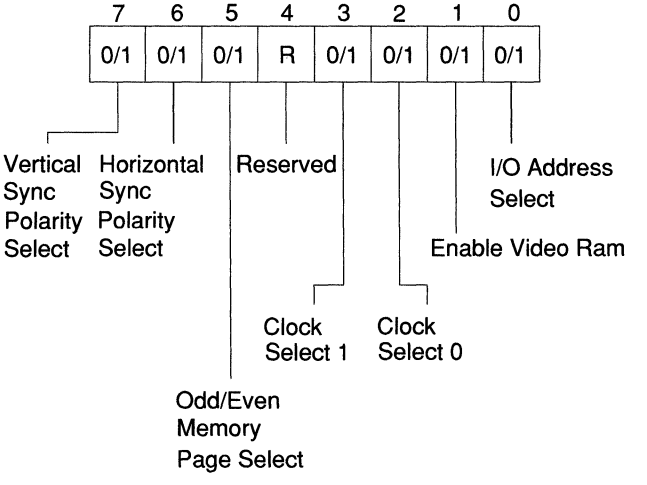
7.1 GENERAL REGISTERS

Name	Read Port	Write Port
Miscellaneous Output	03CC	03C2
Input Status Register 0	03C2	----
Input Status Register 1	03?A	03?A
Feature Control	03CA	03?A

NOTES:

1. Reserved bits should be set to zero.
2. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :
   ? = B in Monochrome Emulation Modes
   ? = D in Color Emulation Modes

Miscellaneous Output Register: Read Port = 03CC Write Port = 03C2



* Bit 7 Vertical Sync Polarity Selection.
  0 = Positive vertical sync polarity.
  1 = Negative vertical sync polarity.

* Bit 6 Horizontal Sync Polarity Selection.
  0 = Positive horizontal sync polarity
  1 = Negative vertical sync polarity.

Note: * These bits are determined by the monitor type. Their encoding is shown below:

Bit 7	Bit 6	Vertical Frame
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

MISCELLANEOUS OUTPUT REGISTER (contd)

Bit 5 Odd or Even Memory Page Select. When in modes 0 - 5 the page size is 64KB. One memory page is selected from the two 64 Kbyte pages. This bit is used for diagnostic purposes and has no effect if PR1(7) = 1 or PR1(6) = 1.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4 Reserved.

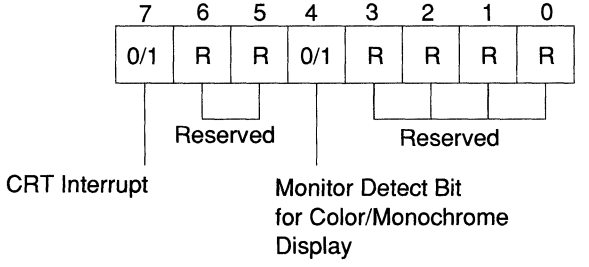
Bit 3, Bit 2 Clock Select 1, 0.

Bit 3	Bit 2	Function
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration
1	1	Register bit 3 = 0. Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1 System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0 CRT Controller I/O Address Range Selection.
Selection for MDA (03B4 and 03B5), or CGA (03D4 and 03D5) mode. Bit 0 also maps Input Status Register 1 at MDA (03BA) or CGA (03DA).
0 = CRTC addresses for MDA emulation mode.
1 = CRTC addresses for CGA emulation mode.

INPUT STATUS REGISTER 0 : READ ONLY PORT = 03C2



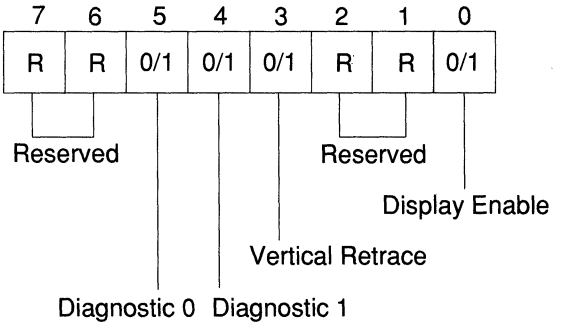
Bit 7 CRT Interrupt Pen ding or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit 6, Bit 5 Reserved.

Bit 4 Monitor Detection.
DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit 3-Bit 0 Reserved

INPUT STATUS REGISTER 1 : READ ONLY PORT = 03?A



Bit 7, Bit 6 Reserved.

Bit 5, Bit 4 Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined below:

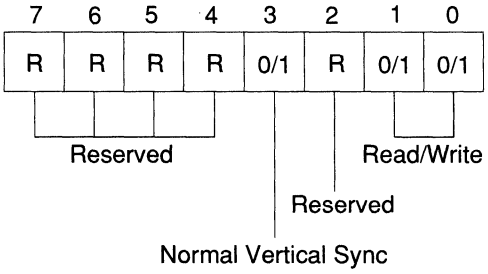
Color Plane Enable Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Bit 3 Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit 2, Bit 1 Reserved.

Bit 0 Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

FEATURE CONTROL REGISTER READ PORT = 03CA WRITE PORT = 03?A



Bit 7 - Bit 4 Reserved.

Bit 3 Normal Vertical Sync.
This bit should always be zero.
0 = Normal vertical sync enabled.
1 = Vertical sync output is the logical OR of vertical sync and vertical display enable.

Bit 2 Reserved.

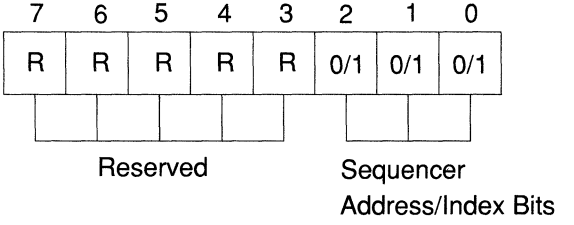
Bit1, Bit 0 Read and write bits.

7.2 SEQUENCER REGISTERS

Name	Port (hex)	Index (hex)
Sequencer Index	03C4	---
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

NOTE: 1. Reserved bits should be set to zero.

SEQUENCER INDEX REGISTER - READ/WRITE PORT = 03C4

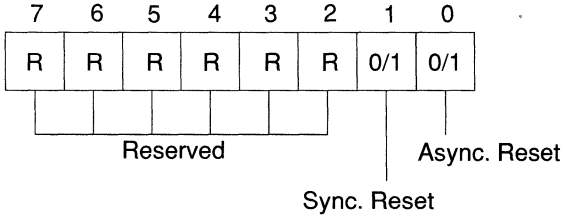


Bit 7 - Bit 3 Reserved.

Bit 2 - Bit 0 Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00H-04H) of the Seqencer register to be accessed.

RESET REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 00



Bit 7 - Bit 2 Reserved.

Bit 1 Synchronous Reset.

To prevent loss of data, bit 1 must be set to 0 during active display interval before changing clock selection through clocking mode, or Miscellaneous Output Register.

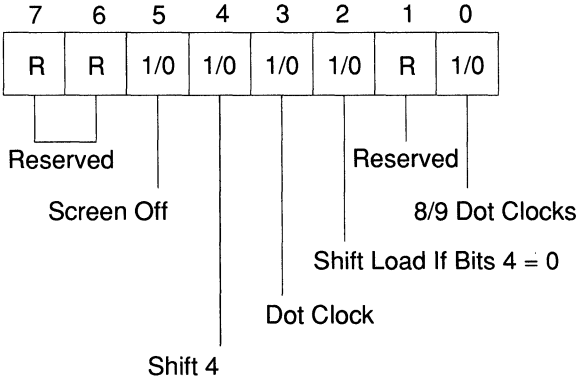
0 = Sequencer is cleared and halted synchronously.

1 = Operational mode (Bit 0 = 1).

RESET REGISTER (contd)

Bit 0 Asynchronous Reset.
Video data can be lost if Sequencer is reset with this bit.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

CLOCKING MODE REGISTER - READ/WRITE PORT 03C5 AND INDEX REGISTER = 01



Bit 7, Bit 6 Reserved.

Bit 5 Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4 Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character clock.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

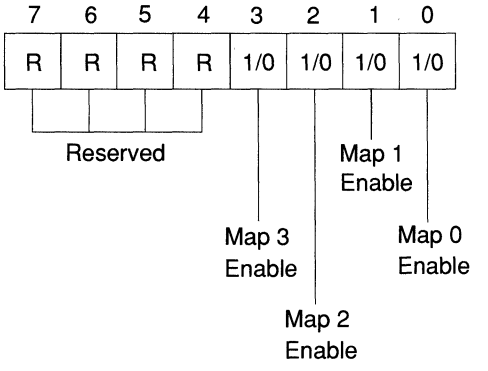
Bit 3 Dot Clock Selection
0 = Normal dot clock selected by VCLK0 input frequency (640 pixels).
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2 Shift Load.
0 = If bit 4 of this register also equals 0, then video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1 Reserved.

Bit 0 8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

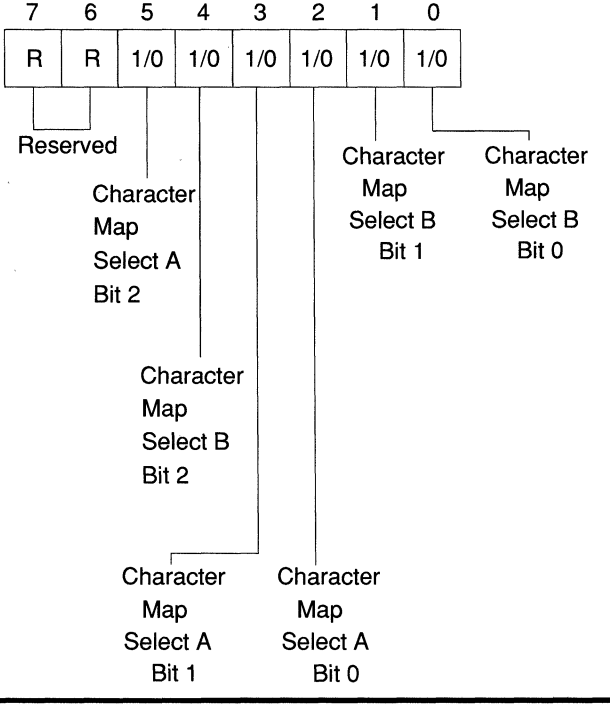
MAP MASK REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 02



Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Prohibit Access To Memory Maps (0 - 3).
0 = Access to maps (0 - 3) disallowed.
1 = Maps (0 - 3) accessible.

CHARACTER MAP SELECT REGISTER
READ/WRITE PORT 03C5 AND INDEX REGISTER = 03



CHARACTER MAP SELECT REGISTER (contd)

Bit 7, Bit 6 Reserved.

Bit 5 Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A is defined by bits 3 and 2, containing the character font table shown below:

Bits 5	3	2	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 4 Character Map B MSB Select.
MSB of character map B is defined by bits 1 and 0, containing the font table described below:

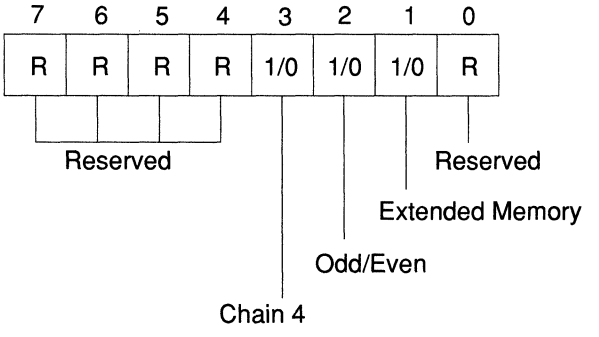
Bits 4	1	0	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 3, Bit 2 Characer Map Select A.
Refer to bit 5 table.

Bit 1, Bit 0 Character Map Select B.
Refer to bit 4 table.

NOTE: 1. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

MEMORY MODE REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 04



Bit 7 - Bit 4 Reserved.

Bit 3 Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0, MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	Map Enabled
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1 Extended Video Memory.
0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0 Reserved.

7.3 CRT CONTROLLER REGISTERS

VGA Register Name	*6845 Register Name	Port (hex)	Index (hex)
CRT Controller Address Register	CRT Controller Address Register	03?4	---
Horizontal Total	Horizontal Total	03?5	00
Horizontal Display Enable End	Horizontal Displayed	03?5	01
Start Horizontal Blanking	†-----	03?5	02
End Horizontal Blanking	†-----	03?5	03
Start Horizontal Retrace Pulse	†-----	03?5	04
End Horizontal Retrace	†-----	03?5	05
Vertical Total	Vertical Displayed	03?5	06
Overflow	†-----	03?5	07
Preset Row Scan	†-----	03?5	08
Maximum Scan Line/Others	Maximum Scan Line Address	03?5	09
Cursor Start	Cursor Start	03?5	0A
Cursor End	Cursor End	03?5	0B
Start Address High	Start Address High	03?5	0C
Start Address Low	Start Address Low	03?5	0D
Cursor Location High	Cursor Location High	03?5	0E
Cursor Location Low	Cursor Location Low	03?5	0F
Vertical Retrace Start	Light Pen High	03?5	10
Vertical Retrace End	Light Pen Low	03?5	11
Vertical Display Enable End		03?5	12
Offset		03?5	13
Underline Location		03?5	14
Start Vertical Blank		03?5	15
End Vertical Blank		03?5	16
CRTC Mode Control		03?5	17
Line Compare		03?5	18

NOTES :

1. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :
   ? = B in Monochrome Emulation Modes and
   ? = D in Color Emulation Modes
2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.
3. "†" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.

CRT CONTROLLER REGISTERS DESCRIPTION

CRT Address Register (Port = 03?4)

Bit 7 - Bit 5 Reserved.

Bit 4 - Bit 0 Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

†Horizontal Total Register (Port = 03?5, Index = 00H)

Bit 7 - Bit 0 Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line. In 6845 mode the character count is less 1.

†Horizontal Display Enable End Register (Port = 03?5, Index = 01H)

Bit 7 - Bit 0 Displayed Characters Less 1.
Program count of the displayed number of characters less 1 in VGA mode. For 6845 mode, load count of the number of characters to be displayed. Left or right borders and blanking time is excluded.

†Start Horizontal Blanking (Port = 03?5, Index = 02H)

Bit 7 - Bit 0 Character Clock Value.
Horizontal blanking begins when the horizontal character counter reaches this character clock value.

†End Horizontal Blanking (Port = 03?5, Index = 03H)

Bit 7 Reserved.

Bit 6, Bit 5 Display Enable Signal Skew Time.
They define the display enable signal skew time in relation to horizontal or vertical synchronization pulses. The skew table is shown below:

Bit 6	Bit 5	Skew in Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Blank Signal Width.
End horizontal blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the sixth bit is the Retrace Register (index 05H) programmed as bit 7 of the End Horizontal Register.

NOTE: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End. Register bit 7 = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

†Start Horizontal Retrace Pulse Register (Port = 03?5, Index = 04H)

Bit 7 - Bit 0 Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active.

†End Horizontal Retrace Register (Port = 03?5, Index = 05H)

Bit 7 MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit 6, Bit 5 Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

Bit 6	Bit 5	Character Clock Delay
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

‡Vertical Total Register (Port = 03?5, Index = 06H)

Bit 7 - Bit 0 Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync is also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the Maximum Scan Line Register (index 09H) bits 0 thru 4).

Overflow Vertical Register (Port = 03?5, Index = 07H)

‡Bit 7 Vertical Retrace Start Bit 9 (index = 10H).
**Bit 6 Vertical Display Enable End Bit 9 (index = 12H).
‡Bit 5 Vertical Total Bit 9 (index = 06H).
Bit 4 Line Compare Bit 8 (index = 18H).

‡Bit 3 Start Vertical Blank Bit 8 (index = 15H).
‡Bit 2 Vertical Retrace Start Bit 8 (index = 10H).
**Bit 1 Vertical Display Enable End Bit 8 (index = 12H).
‡Bit 0 Vertical Total Bit 8 (index = 06H).

NOTES: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the Paradise Register PR3(1) = 0 AND the Vertical Retrace End Register bit 7 = 1.

‡ This register is locked if the Paradise Register PR3(0) = 1 OR the Vertical Retrace End

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CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Preset Row Scan Register (Port = 03?5, Index = 08H)

Bit 7 Reserved.

Bit 6, Bit 5 Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes progammed as multiple shift modes.

Bit 6	Bit 5	Operation
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit 4 - Bit 0 Preset Row Scan Count.
These bits preset the vertical row scan count once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scroll of text.

Maximum Scan Line Register/ (Port = 03?5, Index = 09H)

Bit 7 200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines (each line is double scanned).

Bit 6 Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

§ Bit 5 Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H).

Bit 4 - Bit 0 Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

Cursor Start Register (Port = 03?5, Index = 0AH)

Bit 7, Bit 6 Reserved.

Bit 5 Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit 4 - Bit 0 These bits specify the row within the character box where the cursor begins.
These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Cursor End Register (Port = 03?5, Index = 0BH)

Bit 7 Reserved.

Bit 6, Bit 5 Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below:

Bit 6	Bit 5	Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 These bits specify the row within the character box where the cursor ends.
These bits contain the value of character row less 1. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

Start Address High Register (Port 03?5H, Index = 0CH)

Bit 7 - Bit 0 Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The Paradise Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 and 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

Start Address Low Register (Port = 03?5H, Index = 0DH)

Bit 7 - Bit 0 Display Screen Start Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

Cursor Location High Register (Port = 03?5, Index = 0EH)

Bit 7 - Bit 0 Cursor Address Upper Byte Bits.
The eight higher order bits of 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0F. In VGA mode, the Paradise Register PR3 bits 3 and 4 extend the Cursor Location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

Cursor Location Low Register (Port = 03?5, Index = 0FH)

Bit 7 - Bit 0 Cursor Address Lower Byte Bits.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

§Vertical Retrace Start Register (Port = 03?5, Index = 10H)

Bit 7 - Bit 0 Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 or EGA compatible mode, this register shows the high order six bits in positions 5-0 as the **light pen** read back value, and bits 6 and 7 are reserved. The lower order eight bits of the **light pen** read back register are at index 11H.

§Vertical Retrace End Register (Port = 03?5, Index = 11H)

Bit 7 CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6 DRAM Refresh /Horizontal Scan Line.
Selects 5 DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan lines for 15.75 KHZ display monitors.

Bit 5 Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4 Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by reseting (writing a 0 to) an internal flip-flop.
1 = Vertical retrace interrupt. Sets (writes a 1 to) an internal flip-flop after clearing interrupt, to prepare for next interrupt. The flip-flop must be set or it will hold interrupts inactive.

Bit 3 - Bit 0 Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan count for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of the **Light Pen Register**.

Vertical Display Enable End Register (Port = 03?5, Index = 12H)

Bit 7 - Bit 0 Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends. The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Offset Register (Port = 03?5, Index = 13H)

Bit 7 - Bit 0 Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

Underline Location Register (Port = 03?5, Index = 14H)

Bit 7 Reserved.

Bit 6 Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5 Count By 4 For Doubleword Access.
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit 4 - Bit 0 Underline Location.
These bits specify the scan line within a character matrix where underline is to be displayed. Load a value 1 less than the desired scan line number.

§Start Vertical Blank Register (Port = 03?5, Index = 15H).

Bit 7 - Bit 0 Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

§End Vertical Blank Register (Port = 03?5, Index = 16H)

Bit 7 - Bit 0 Vertical Blank Inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:

8-Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal in scan lines).

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

CRT Mode Control Register (Port = 03?5, Index = 17H)
This register is locked if Paradise Register PR3(5) = 1.

Bit 7 Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6 Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

Memory Address	Byte Address Mode	Word Address Mode	Doubleword Address Mode
MA0/RF0	MA0	* MA15 or MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE: * See bit 5, defining address wrap. This table is only applicable when Paradise Register PR1 bits 7 and 6 are zero.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H Bit 6	CRT17H Bit 6	Address Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 Address Wrap.
0 = In word address mode, this bit enables bit 13 or bit 15 to appear at MA0, otherwise bit 0 appears on MA0.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board. Bit MA13 is used in applications which do not use system board memory for CGA compatibility.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

CRT Mode Control Register (contd)

Bit 4 Reserved.

Bit 3 Count By Two
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments address counter. Selects byte or word refresh address of the display memory.

Bit 2 Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1 Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0 6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

Line Compare Register (Port = 03?5, Index = 18H)

Bit 7 - Bit 0 Line Compare Lower Eight Bits.

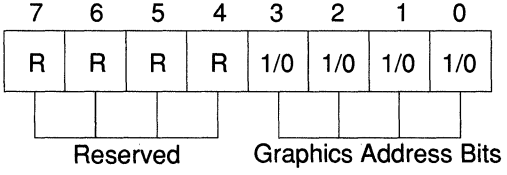
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.4 GRAPHICS CONTROLLER REGISTERS

Name	Port (Hex)	Index (Hex)
Graphics Index Register	03CE	---
Set / Reset	03CF	00
Enable Set/ Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode Register	03CF	05
Miscellaneous Register	03CF	06
Color Don't Care	03CF	07
Bit Mask Register	03CF	08

NOTE: 1. Reserved bits should be set to zero.

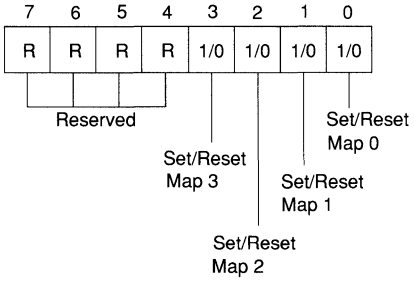
GRAPHICS INDEX REGISTER - READ/WRITE PORT = 03CE



Bit 7 - Bit 4 Reserved.

Bit 3 -Bit 0 Graphics Controller Register Index Pointer Bits.
Note that all the Paradise registers reside with the index pointer extension beyond graphics Controller registers.

SET / RESET REGISTER - READ / WRITE PORT 03CF AND INDEX REGISTER = 00



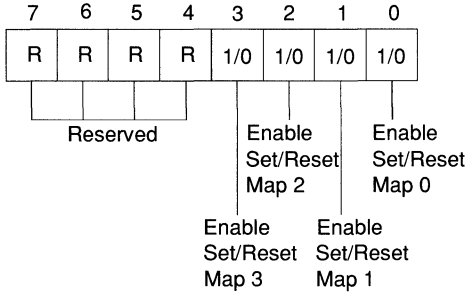
Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

Bit	Set/Reset
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: *The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

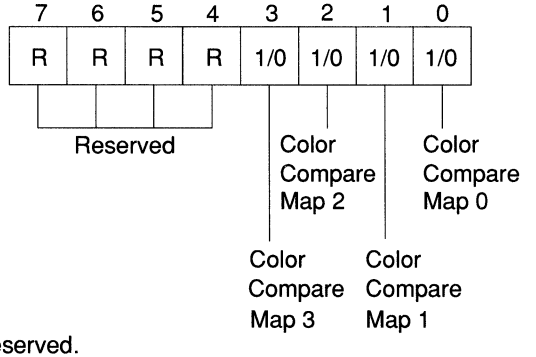
ENABLE SET / RESET REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 01



Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Enable The Set/Reset Register (Index = 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data value of the system microprocessor.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

COLOR COMPARE REGISTER - READ/WRITE PORT 03CF AND INDEX REGISTER = 02

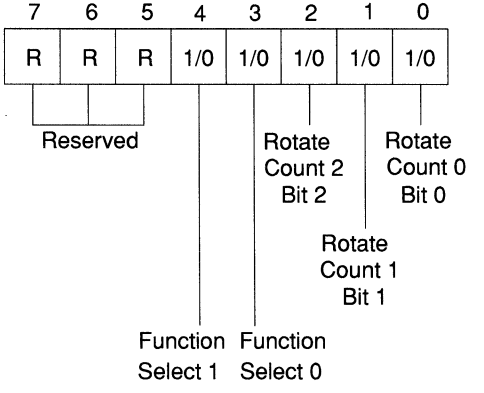


Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal their corresponding color compare value.
When read mode bit 3 in the Graphics Mode Register (index = 05H) is set to 1 and the system does a memory read, a 1 will be returned for each bit where the four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below:

Bit	Color Compare
3	Map 3
2	Map 2
1	Map 1
0	Map 0

DATA ROTATE REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 03



Bit 7 - Bit 5 Reserved.

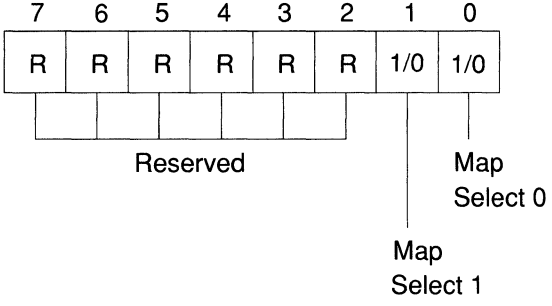
Bit 4, Bit 3 Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows:

DATA ROTATE REGISTER (contd)

Bit 4	Bit 3	Function
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit 2 - Bit 0 Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

READ MAP SELECT REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 04



Bit 7 - Bit 2 Reserved.

Bit1, Bit 0 Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. Map read is defined as shown under:

Bit 1	Bit 0	Read Map
0	0	0
0	1	1
1	0	2
1	1	3

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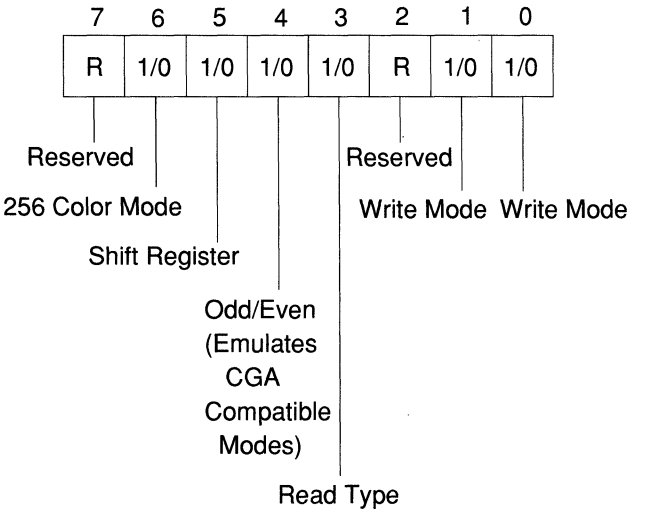
GRAPHICS MODE REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 05



Bit 7 Reserved.

Bit 6 256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5 Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of the even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3 Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

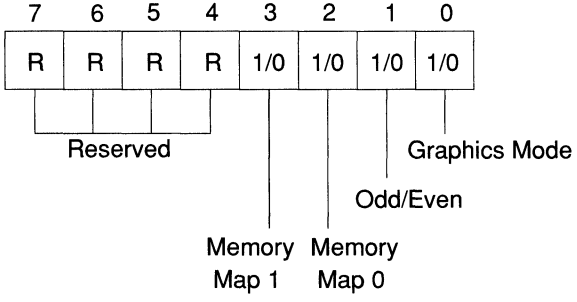
Bit 2 Reserved.

GRAPHICS MODE REGISTER (contd)

Bit 1, Bit 0 Write Mode.
The following table defines the four write modes.

Bit 0	Bit 1	Write Mode
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3 : 0) are filled with the 8-bit value of the corresponding CPU data bits (3 : 0). The 32 bit output of the four memory maps is operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

MISCELLANEOUS REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 06



Bit 7 - Bit 4 Reserved.

MISCELLANEOUS REGISTER (contd)

Bit3, Bit 2 Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

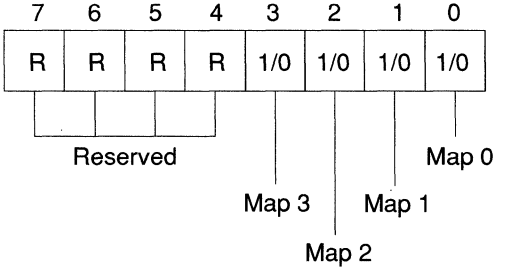
Bit 3	Bit 2	CPU Address Range	Length
0	0	A0000 - BFFFFH	128KB
0	1	A0000 - AFFFFH	64KB
1	0	B0000 - B7FFFH	32KB
1	1	B8000 - BFFFFH	32KB

Bit 1 Odd/Even Mode.
0 = CPU address bit A0 is output on PVGA1A memory pin MA0.

1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0 Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selected.
1 = Graphics mode selected.

COLOR DON'T CARE REGISTER - READ/ WRITE PORT 03CF AND INDEX REGISTER = 07

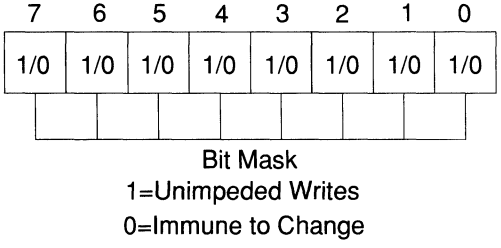


Bit 7 - Bit 4 Reserved.
Bit 3 - Bit 0 Memory Map Color Compare Operation.
Map coding is shown below:

	Bit 3	Bit 2	Bit 1	Bit 0
Map #	3	2	1	0

0 = Disable color compare operation.
1 = Enable color compare operation.

BIT MASK REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 08



Bit 7 - Bit 0 Bit mask.
Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.

1 = Bit position value is unmasked and can be changed in the corresponding map.

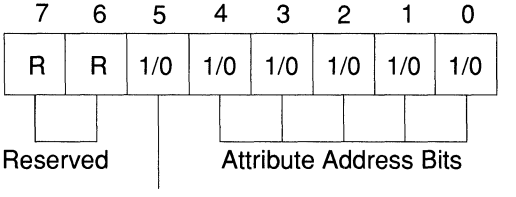
7.5 ATTRIBUTE CONTROLLER REGISTERS

Name	Port (Hex)	Index (Hex)
Index Register	03C0	---
Palette Registers	03C0	00---0F
Attribute Mode Control Register	03C0	10
Overscan Control Register	03C0	11
Color Plane Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

NOTES: 1. Each attribute data register is written at 03C0 and register data is read from address 03C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :

? = B in Monochrome Emulation Modes and
? = D in Color Emulation Modes

ATTRIBUTE INDEX REGISTER - READ/WRITE PORT = 03C0



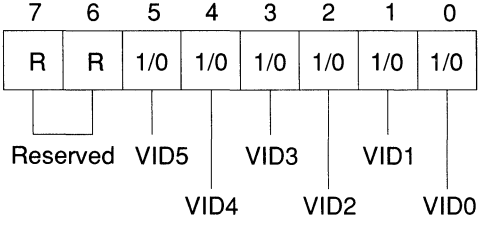
Bit 7 , Bit 6 Reserved.

Bit 5 Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit 4 - Bit 0 Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 03?A) clears the flip-flop and selects the Address Register, which is read thru address 03C1 and written at address 03C0. Once the Address Register has been loaded with an index, the next write operation to 03C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 03C0, but does not toggle for reads to address 03C1.

PALETTE REGISTERS (00-0F Hex) - READ PORT 03C1/WRITE PORT 03C0



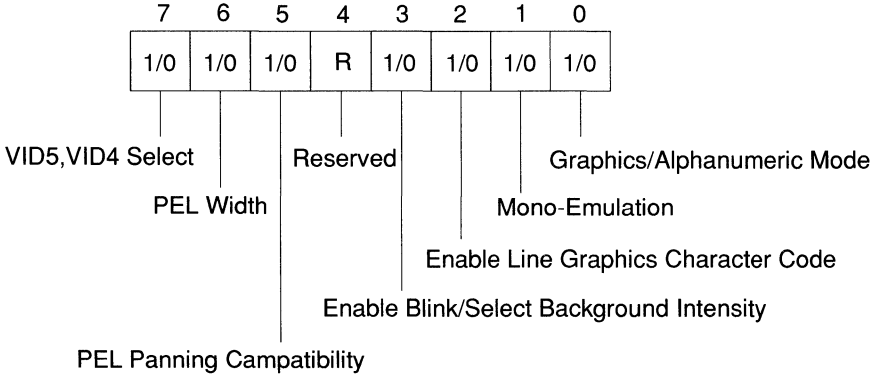
Bit 7, Bit 6 Reserved.

Bit 5 - Bit 0 Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below:

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

ATTRIBUTE MODE CONTROL REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 10



Bit 7 VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 Pixel Width.
0 = Disable 256 color mode pulse width.
1 = Enable pulse width for 256 color mode.

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ATTRIBUTE MODE CONTROL REGISTER (contd)

Bit 5 PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.

1 = Allows a successful line compare to disable the PEL Panning Register until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4 Reserved.

Bit 3 Back Ground Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

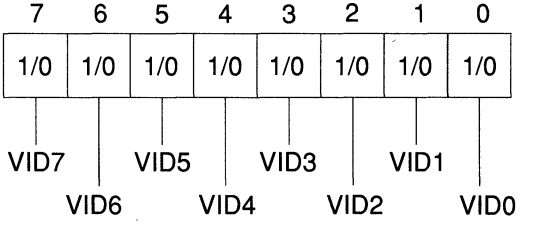
Bit 2 Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0 Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

OVERSCAN COLOR REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 11

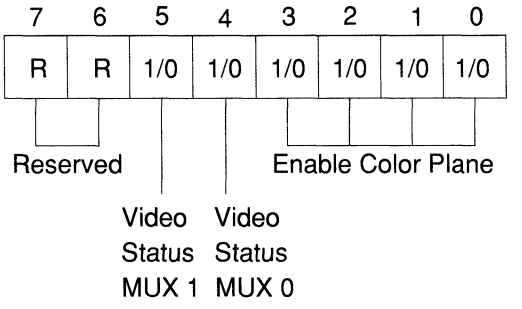


Bit 7 - Bit 0 Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown below:

Bit 7 VID7
Bit 6 VID6
Bit 5 VID5
Bit 4 VID4
Bit 3 VID3
Bit 2 VID2
Bit 1 VID1
Bit 0 VID0

COLOR PLANE ENABLE REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 12



Bit7, Bit 6 Reserved.

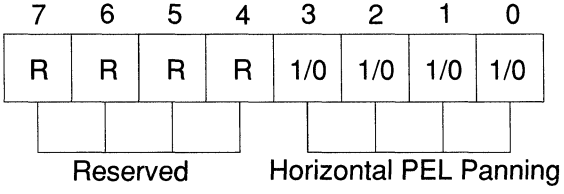
Bit 5, Bit 4 Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

Color Plane		Input Status Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3 - Bit 0 Color Plane Enable.
0 = Disables respective color planes.
1 = Enables the respective display memory color plane.

HORIZONTAL PEL PANING REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 13



Bit 7 - Bit 4 Reserved.

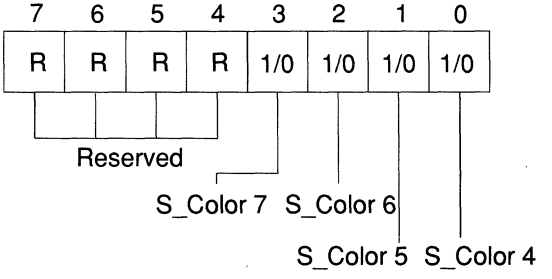
Bit 3 - Bit 0 Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes:

HORIZONTAL PEL PANNING REGISTER (contd)

Register Value	Left Shift Pixel Value 9 Dots/Character	8 Dots/Character	256 color Mode
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

COLOR SELECT REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 14



Bit 7 - Bit 4 Reserved.

Bit 3, Bit 2 Color Value MSB.
Two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 250 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6.

Bit 1, Bit 0 Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

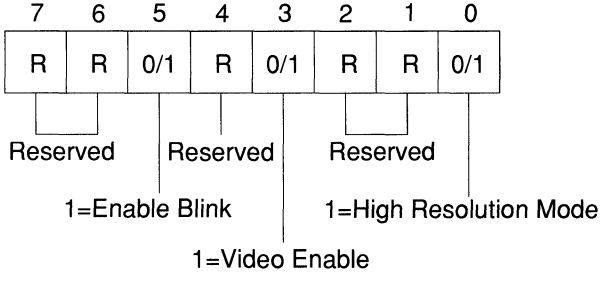
7.6 COMPATIBILITY REGISTERS

Name	Port (Hex)
Mode Control Register	03?8
Color Select Register	03D9
Status Register	03?A
AT&T/M24 Register	03DE
Hercules Register	03BF
Preset Light Pen Latch	03B9 (Mono) & 03DC (CGA)
Clear Light Pen Latch	03?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting Paradise Register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting Paradise Register PR2(7) = 1.
3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   ? = B in Monochrome Emulation Modes
   ? = D in Color Emulation Modes

MODE CONTROL REGISTER
MONOCHROME (HIGH RESOLUTION) MDA OPERATION - WRITE ONLY PORT = 03B8



Bit 7, Bit 6 Reserved.

Bit 5 Enable Blink.
0 = Disable blink.
1 = Enable blink.

Bit 4 Reserved.

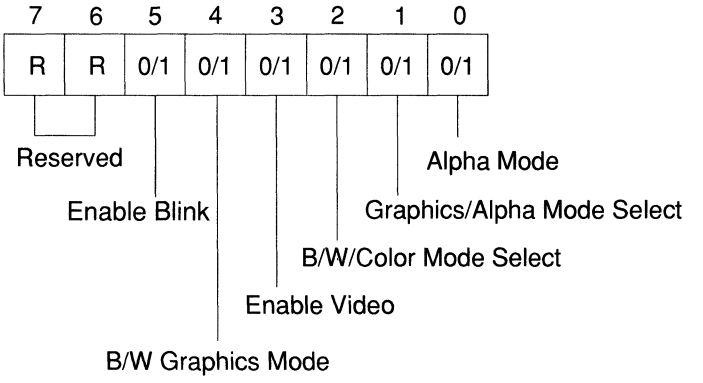
Bit 3 Video Enable.
0 = Video disable.
1= Video activated.

Bit 2, Bit 1 Reserved.

Bit 0 High Resolution Mode.
0 = High resolution disabled. This is not allowed in MDA designs.
1 = High resolution is enabled.

MODE CONTROL REGISTER (contd)

COLOR CGA OPERATION - WRITE ONLY PORT = 03D8



Bit 7, Bit 6 Reserved.

Bit 5 Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4 B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

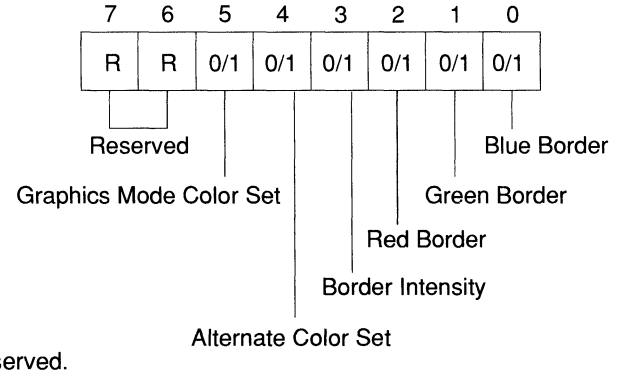
Bit 3 Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2 B/W or Color Display Mode.
0 = Color mode selected.
1 = B/W mode enabled.

Bit 1 Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0 (40 by 25) or (80 by 25) Text Mode Selection.
0 = (40 by 25) alpha mode enabled.
1 = (80 by 25) alpha mode activated.

CGA COLOR SELECT REGISTER - WRITE ONLY PORT = 03D9



Bit 7, Bit 6 Reserved.

Bit 5 320 by 200 Color Set Select.
0 = Disable 320 by 200 color mode.
1 = Color set selection for 320 by 200 color mode.

Bit 4 Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3 Border Intensity.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2 Red Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

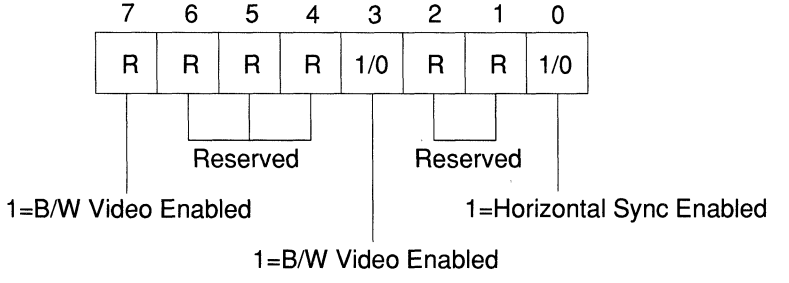
Bit 1 Green Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

CGA COLOR SELECT REGISTER CONTD

Bit 0 Blue Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Selects blue background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

CRT STATUS REGISTER

MDA OPERATION - READ ONLY PORT = 03BA



Bit 7 B/W Video Status.
0 = B/W Video disabled.
1 = B/W video enabled.

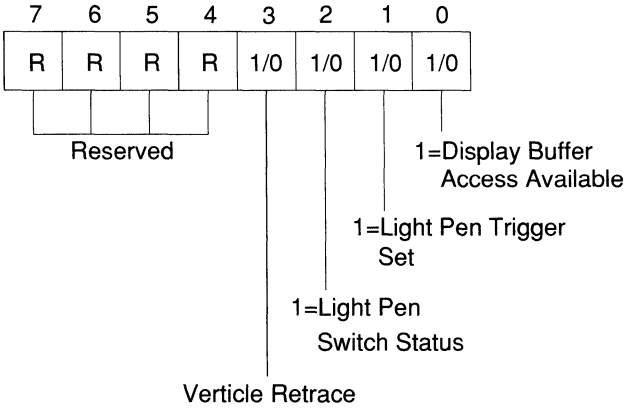
Bit 6 - Bit 4 Reserved.

Bit 3 B/W Video Status.
0 = B/W Video disabled.
1 = B/W video enabled.

Bit 2 - Bit 1 Reserved.

Bit 0 Horizontal Sync Status.
0 = Horizontal sync not active.
1 = Horizontal sync enabled.

CGA OPERATION - READ ONLY PORT = 03DA



Bit 7 - Bit 4 Reserved.

Bit 3 Video Signal Output Status.
0 = Video signal enabled.
1 = Video signal disabled.

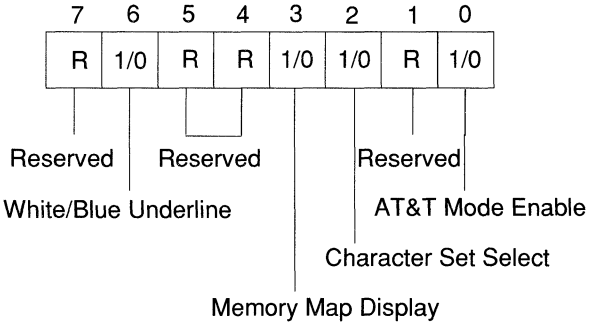
Bit 2 Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1 Light Pen Trigger Set.
0 = Light pen not triggered.
2 = Positive going edge from the light pen input has triggered its latch.

Bit 0 Display Buffer Access Status.
0 = Display buffer access is not allowed.
1 = Display buffer access is permitted without interfering with the display.

AT&T / M24 REGISTER - WRITE ONLY PORT = 03DE

This is a write only, 8-bit register located at address 03DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in Paradise Register 2 (PR2).



Bit 7 Reserved.

Bit 6 White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit 5, Bit 4 Reserved.

Bit 3 Page Select.
Selects between one or two 16KB RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B8000H (16 Kbyte length).
1 = Display memory address starts at BC000H (16 Kbyte length).

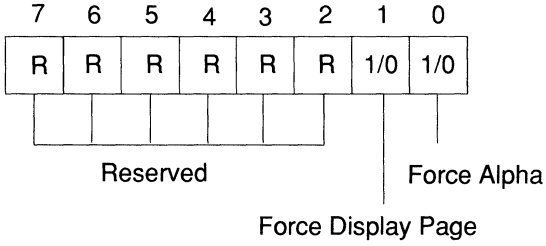
Bit 2 Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1 Reserved.

Bit 0 M24 or Non-IBM Graphics Mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

HERCULES REGISTER - WRITE ONLY PORT = 03BF

The Hercules Mode Register is a 2-bit write only register located at I/O port address 03BF hex. Its bits only effect device operation in 6845 mode. Both of the bits are set to low (0) by reset, or when the device is put into a color mode.



Bit7 - Bit 2 Reserved.

Bit 1 Force Display Page.
Enables Mode Register bit 7 of the Hercules Graphics Card to select displayed memory page in graphics mode. When reset, bit 1 also prevents access of display of second memory page.
0 = Bit 7 of the Mode Register can't be set, and the upper memory page is mapped out.
1 = Bit 7 of the Mode Register can be set, and the upper memory page is accessible.

Bit 0 Force Alpha.
Enables Mode Register Bit 1. This bit forces alpha mode.
0 = Bit 1 of the Mode Register can't be set forcing alpha mode.
1 = Bit 1 of the Mode Register may be changed. Therefore, text or graphics modes may be displayed.

8.0 PVGA1A PARADISE REGISTERS (PR)

The PVGA1A incorporates six additional I/O registers to enhance the functions of the basic VGA. The registers are lock protected and located in the graphics controller I/O section at register locations which have not been used by IBM. All PR registers listed below are read or write able.

NAME	DESIGNATION	I/O LOCATION
Address Offset A	PR0A (6:0)	3CF.09
Address Offset B	PR0B (6:0)	3CF.0A
Memory Size	PR1 (7:0)	3CF.0B
Video Select	PR2 (7:0)	3CF.0C
CRT Control	PR3 (7:0)	3CF.0D
Video Control	PR4 (7:0)	3CF.0E
Lock/Status	PR5 (7:0)	3CF.0F
Configuration	CNF (7:2)	---------

Paradise Register Notation: XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F --> 3CE (select index register) followed by (data byte) --> 3CF (data port).

Registers PR0 through PR4 are normally locked after power up. In order to access registers (PR0-PR4), the PR5 register has to be loaded with the value 05H. These registers stay unlocked until the PR5 register is loaded with another value.

All PR registers, except for PR1 (1:0), are set to 0 at power on reset. The PR1 (1:0) bits are latched internally at power on reset from the corresponding video memory data bus pins MD (1:0), connected to the pullup or pulldown external resistors. Pullup resistors on MD(1:0) causes PR(1:0) to be latched low.

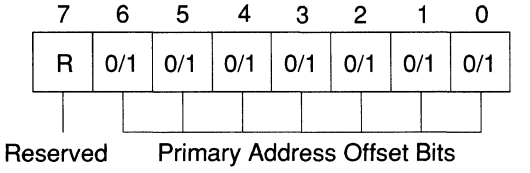
8.1 PR0 A,B Address Offset Registers A & B.

The PVGA1A can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1MB total system space to the video controller. Therefore, the video memory space starts at A0000H and ends at BFFFFH. To allow a second video card to co-exist, this space is furthur limited to a 64 Kbyte video memory partition. Primary offset register (PR0A), is always enabled if PR1 bit3 is 0. PR0A is normally used to control 64KB of the available video address space.

Alternatively, Paradise address offset register (PR0A) and address offset register (PR0B) may be used to access two 32KB video RAM windows. PR0A window is mapped from A8000H-AFFFF while PR0B is mapped from A0000H-7FFFFH if PR1 bit 3 is set to 1 (Alternate address register PR0B is enabled).

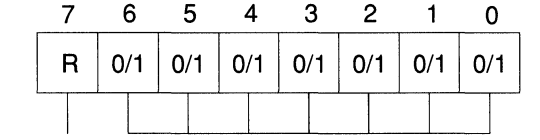
These registers contain an offset which gets added to the system address when accessing 1MB of video memory. Address offset register A is the primary address offset register and is always enabled. On the other hand, alternate address offset register B is enabled only if PR1 bit3 is set to 1. PR0A,B register six bit offset is added to address bits (12:18) of the system address bus SA(0:19) to form a 20-bit address. It can be thought of as being segment registers DS and ES of the 8088 architecture. PR0A,B will have 4KB segments.

PR0 A - ADDRESS OFFSET REGISTER A - READ/WRITE PORT= 3CF & INDEX REGISTER=09



Address Offset Register A
Added to the System Address
Selected When Address Bit A15=1
it is the Default Address
Offset Register

PR0 B - ADDRESS OFFSET REGISTER B - READ/WRITE PORT=3CF & INDEX REGISTER=0A



Address Offset Register B
Selected by System Address
only if PR1(bit 3)=1

8.2 PR1 Memory Size

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD (1:0), using either pullup or pulldown external resistors. Pullup resistors on MD(1:0) causes PR1(1:0) bits to be latched low. According to the VGA video memory organization, 256 Kbyte of the available memory space is divided into four 64 Kbyte maps (0-3) each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane.

The starting address of the 256 Kbyte video memory buffer can be configured to match other video adapters, and, or, application programs. For example, 256 Kbyte video display buffer with 128 Kbyte or 64 Kbyte segments can start at address A0000 (Hex) while 32 Kbyte segments start at address B0000 (Hex) or B8000 (Hex). PVGA1A enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512 Kbyte or 1024 Kbyte. The DRAM organizations supported by the PVGA1A and its associated video space table are shown below:

DRAMS	MA8 Pin	Video Space	Memory Planes
64Kx4	N/U	256KB	4 (64KB per plane)
64Kx4	Bank Select	512KB	4 (128KB per plane)
256Kx4	DRAM Pin A8	1024KB	4 (256KB per plane)

When video memory size is 512 Kbyte, and 64 Kbyte by 4 DRAMS are used, two banks of 64 Kbyte form 128 Kbyte per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane. Four planes form the desired 512 Kbyte video memory space. For 1024 Kbyte video memory size, MA8 is directly connected to the A8 address pin of the 256 Kbyte by 4 DRAMS, and two DRAMS form a 256 Kbyte per plane. Four planes make the desired 1024 Kbyte video memory space. For more details, refer to the programming section listed on the next page:

MEMORY SIZE REGISTER

GRAPHICS MODE RAM ADDRESSING:

PR1(7) **PR1(6)**

0 0 256 K TOTAL; 64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

PR1(7) **PR1(6)**

0 1 256K TOTAL; 64K/PLANE; PVGA1A MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) **PR1(6)**
1 0 512 KBYTE TOTAL IN FOUR PLANES ; 128KB / PLANE IN PVGA1A MEMORY ORGANIZATION (EACH PLANE IS 2 BANKS OF 64 KBYTE BY 8)

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	------	-----	-----	------	-----	-----
MA(16)*	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: "*" Controls CAS external to PVGA1A

PR1(7) **PR1(6)**
1 1 1024 KBYTE TOTAL IN FOUR PLANES ; 256K/PLANE IN PVGA1A MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

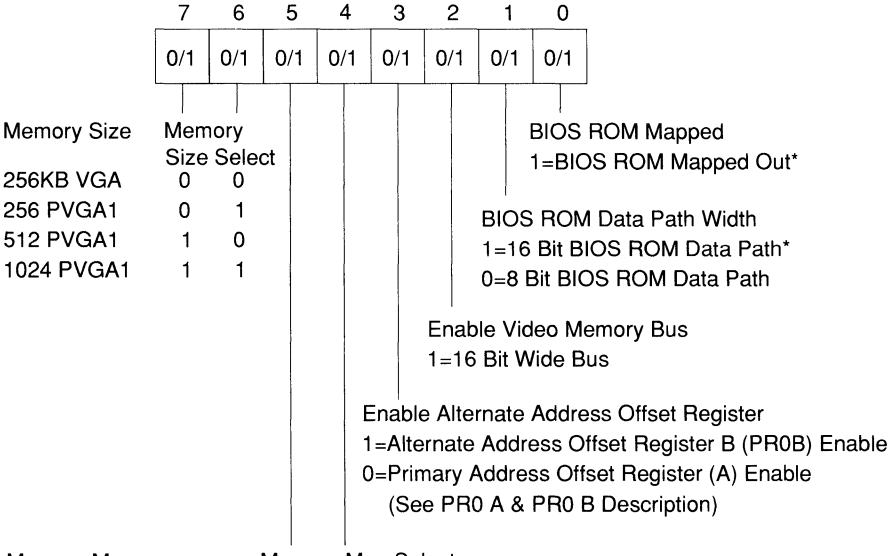
NOTES: 1. A(19)-A(0) are modified System Addresses through PR0A or PR0B.

2. CA(17)-CA(0) are CRT Controller Character Address Counter bits.

3. XRN(5) is Miscellaneous Output Register 3C2, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5)is selected as MA(0) if GR6(3) OR GR6(2) = 1.

4. CA(13) is selected as MA(0) if CRTC Mode Register R17(5) = 0.

PR1 - MEMORY SIZE REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0B



NOTE: * = A Pull Up Resister On MD(0) Or MD(1) Line Sets These Bits To 0 At Power On Reset

Bit7	Bit6	MEMORY SIZE
0	0	256KB VGA
0	1	256KB PVGA
1	0	512KB PVGA
1	1	1024KB PVGA

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping
0	1	1st 256KB in 1MB space
1	0	1st 512KB in 1MB space
1	1	1st 1024KB in larger space

Bit3 Enable Alternate Address Offset Register
(Refer to PR0A and PR0B descriptions)

Bit2
Bit1 Enable 16 bit bus for Video Memory
When set to 1, the BIOS ROM has 16 bits data path.
If set to 0, the BIOS ROM data path is 8 bits wide.
A pullup on MD (1) sets this bit to 0 at power on reset.

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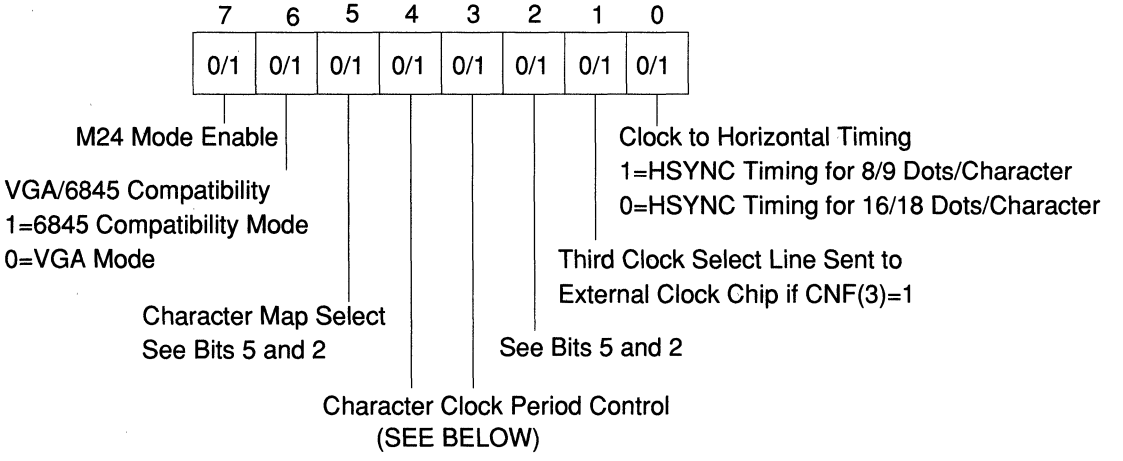
8.3 PR2 - VIDEO SELECT REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0C



Bit 7 It enables M24 mode.

Bit 6 0 = VGA mode.
1 = 6845 Compatibility Mode

Bit 5 Character Map Select. This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	Plane Select
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

Bit4	Bit3	Character Clock Period Control
0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Bit 2 Enable special color underline using all odd numbered attributes (e.g. Programming 1 gives blue colored underline). In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1 This bit is the third clock select line sent to the external clock chip if CNF (3) is set to 1. If CNF register(Bit3) is set to 0, the internal clock select multiplexor is locked.

Bit 0 1 = Set horizontal sync timing for 8/9 dots/character
0 = Set horizontal sync timing for 16/18 dots/character

8.4 PR3 - CRT CONTROL AND GROUP LOCKING

The CRT control register description and software notation are summarized. For example, 3?5.11(7) refers to bit 7 of the CRTC data register 11 (Hex). To read this bit, first write 11 (Hex) to to 3?4, then read 3?5 and test bit 7's value.

PVGA1A CRT CONTROLLER - REGISTER LOCKING

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT contoller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the section below:

GROUP 0

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 ------ Horizontal Total characters per scan
CRT controller register 01 ------- Horizontal Display Enable End
CRT controller register 02 ------ Start Horizontal Blanking
CRT controller register 03 ------ End Horizontal Blanking
CRT controller register 04 ------ Start Horizontal Retrace
CRT controller register 05 ------ End Horizontal Retrace

GROUP 1

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) ------ Vertical Display Enable End bit 9
CRT controller register 07(Bit1) ------ Vertical Display Enable End bit 8

GROUP 2

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 -------- Vertical Total
CRT controller register 07(Bit7) ------ Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ------ Vertical Total bit 9
CRT controller register 07(Bit3) ------ Start Vertical Blank bit 8
CRT controller register 07(Bit2) ------ Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ------ Vertical Total bit 8

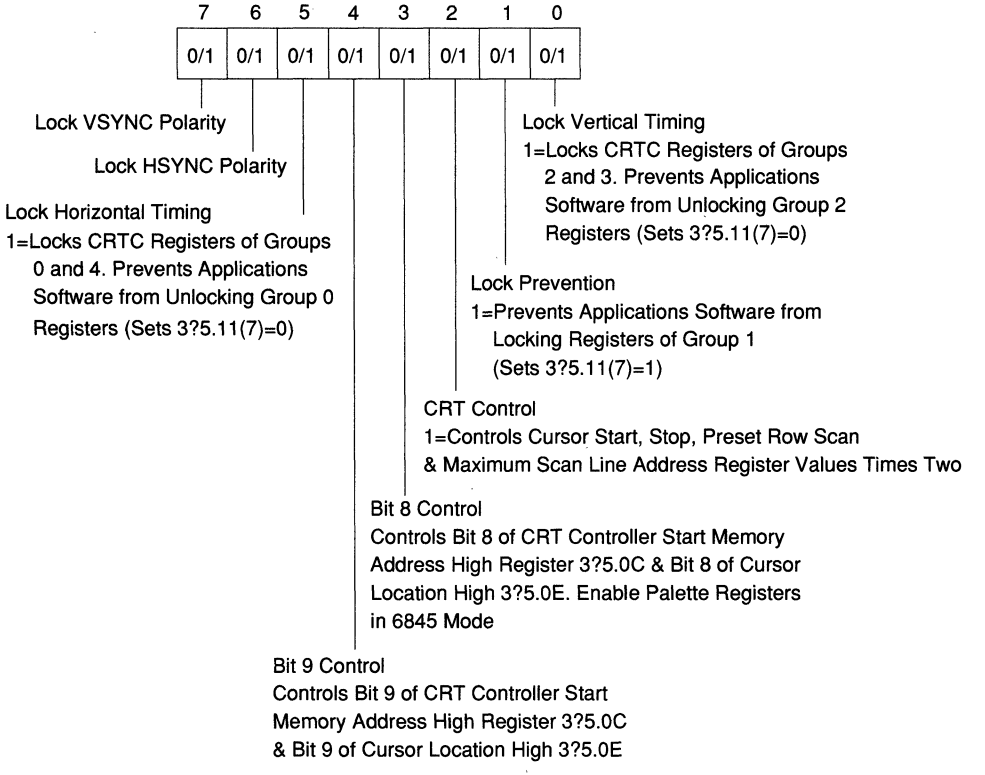
GROUP 3

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ------ Start Vertical Blank bit 9
CRT controller register 10 ------ Vertical Retrace Start
CRT controller register 11(Bits 3-0) ------ Vertical Retrace End
CRT controller register 15 ------ Start Vertical Blanking
CRT controller register 16 ------- End Vertical Blanking

GROUP 4

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ----- Selects divide by two vertical timing

PR3 - CRT LOCK CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0D



Bit0 If set to 1 the BIOS ROM is mapped out. Pullup reisistor latches 0 after power up. A pullup on MD (0) sets this bit to 0 at power on reset.

Bit 7 Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6 Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5 Lock horizontal timing.
Locks CRTC registers of Groups 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0.

Bit 4 Bit 9 of CRT Controller Start Memory Address High Register 3?5 .0C, and bit 9 of Cursor Location High 3?5 .0E. This bit corresponds to Character Address CA (17).

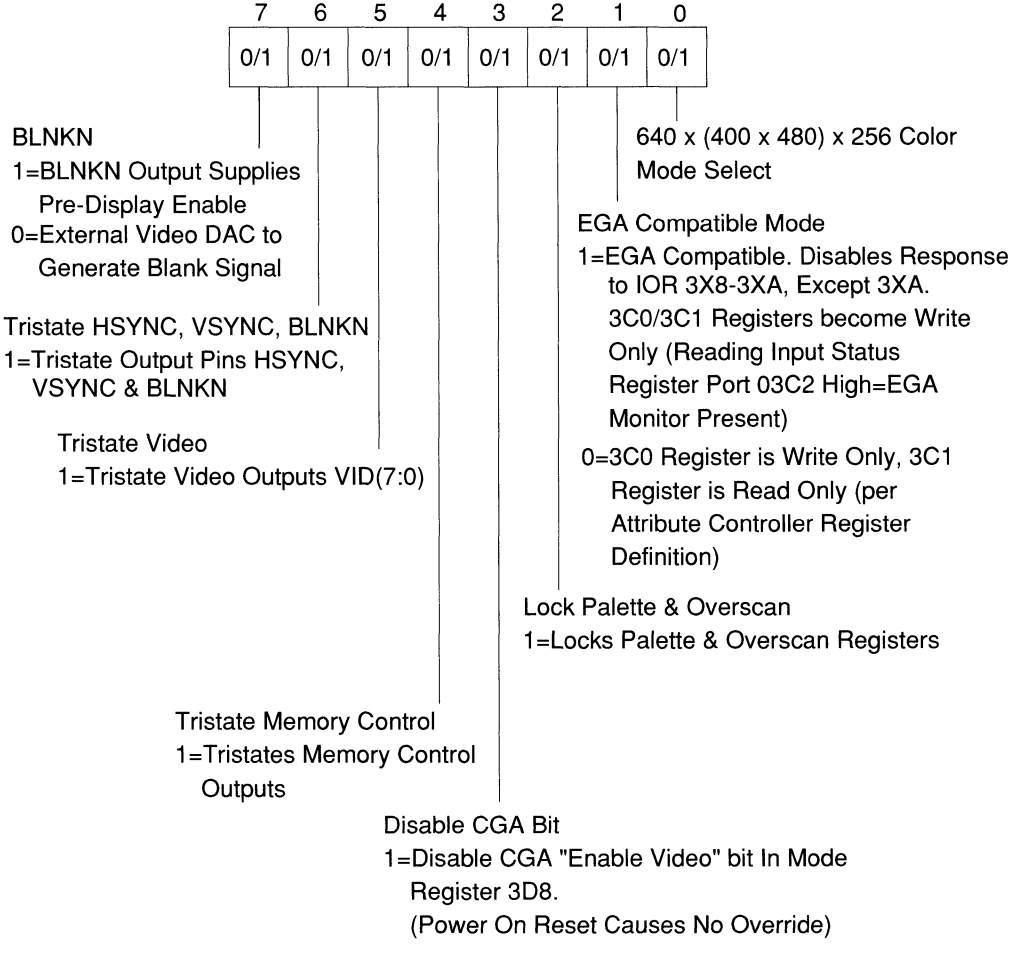
Bit 3 Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16). This bit is used to enable palette registers in non EGA (6845) mode. In the PVGA1A, the palette will be enabled all of the time.

Bit 2 Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1 1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5 .11 bit 7=1.

8.5 PR4 - VIDEO CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.



PR4 - VIDEO CONTROL REGISTER (contd)

Bit 7 This bit controls the output signal BLNKN, which normally in the VGA mode, is used by the external video DAC chip to generate blanking.
1 = Display enable.
0 = Blank.

Bit 6 1 = Tristate the output pins HSYNC, VSYNC, and BLNKN.
0 = Normal operation.

Bit 5 1 = Tristate the video outputs VID (7:0).
0 = Normal operation.

Bit 4 1 = Tristates the memory control outputs RAS32N, RAS10N, CAS32N, CAS10N, OE32N, OE10N, WE3N, WE2N, WE1N, WE0N, and MA (0 : 8).
0 = Normal operation.

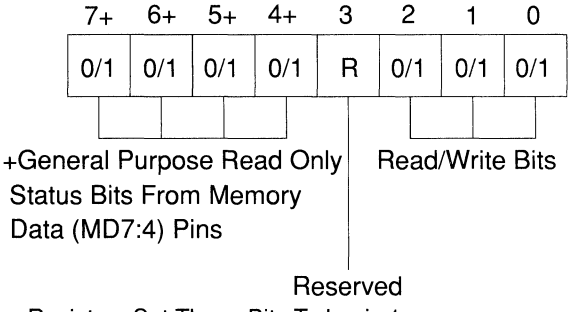
Bit 3 1 = Disables the CGA "enable video" bit in mode register 3D8. Power on reset causes no override.
0 = Normal operation.

Bit 2 1 = Lock palette and overscan registers.
0 = Normal operation.

Bit 1 1 = EGA Compatible Mode. It disables response to IOR 3X8-3XA, to turn off 6845 compatible modes except status register 3XA. Reading Input Status register port 03C2 high implies the presence of EGA monitor in VGA mode.. Also, registers at 3C0/3C1 change to write only mode if EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is write only, while 3C1 register is read only, per the Attribute Controller registers definition.

Bit 0 Paradise shift register control. It selects 640(400 by 480) by 256 color mode, in addition to the PVGA1A operation by enhancing IBM Mode 13, which has only 320 by 200 dot resolution.

8.6 PR5 - GENERAL PURPOSE STATUS BITS - READ/WRITE PORT=3CF & INDEX REGISTER =0F



NOTE: += Pull Down Resistors Set These Bits To Logic 1

Bit 0 Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5 .11 bit 7=0.

General purpose status bits (7:4) and Paradise register lock/unlock bits (2:0) are stored in the Paradise Register (PR5)

Bits (7:4) These are general purpose status bits. They are latched at power on reset from the corresponding memory data bus pins MD (7:4) connected to the external

INTERNAL I/O PORTS

I / O PORT 46E8H (AT MODE - WRITE ONLY)

IBM has implemented a scheme for mapping the BIOS ROM on the PS/2 VGA display adapter card. This mapping is not done on Micro Channel based VGA implementations. The mapping is controlled through a five bit, write only register located at I/O address 46E8H. The card does not fully decode the address and it also appears at addresses 56E8H, 66E8H and 76E8H. The use of bits within the register are as follows:

D7:D5	Unused
D4	Setup
D3	Enable I/O and memory acceses
D2:D0	BIOS ROM page select (External Implementation)

The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The I/O port 46E8H bits (4 : 3) are provided inside the PVGA1A. Bits (2 : 0) are implemented externally. PVGA1A provides EBROMN as the write strobe to external circuitry inplementing BIOS ROM page mapping whenever 46E8H is accessed.

I / O PORT 102H - VIDEO ENABLE (AT AND MICRO CHANNEL MODES)

Power On Self Test (POST) sleep bit 0 is used to awaken the PVGA1A after power on in the MCA mode. Program the I/O port 102H Option Select Byte #1 to enter the set up mode. Port 102H is **internal** to the PVGA1A. If the port 102H bit 0 is set to 1, the PVGA1A is functional. However, if the bit 0 is programmed as 0, the PVGA1A will only respond to setup read and write operations. It will disregard I/O or memory read / write operations and cause no interrupts in the set up mode. To enter the set up mode in AT bus applications, bit 4 of the **partially** decoded **internal** I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the CDSETUP (EION) signal pin is active low, the PVGA1A is in setup mode and port 102H can be accessed.

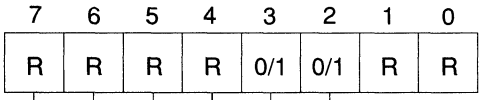
VIDEO RAMDAC PORTS

Video RAMDAC is implemented external to the PVGA1A. However, the WPLTN and RPLTN signals required by the RAMDAC are provided by the PVGA1A. WPLTN and RPLTN signals to the RAMDAC are generated when the following I / O ports are written to or read from :

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
* 3C7H	* DAC state (read only)	* If bits 0/1 =1, DAC in read operation When bits 0/1 =0, DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

*** NOTE : This port is internal to PVGA1A.**

PVGA1A CONFIGURATION BITS CNF (2:3) - NON-READ / NON-WRITE PORT



Read Back As
PR5 Bits (4:7)

Bus Architecture Select
1=IBM PC AT Bus Architecture Signals
0=IBM Microchannel Architecture Signals

Video Clock Source Control
1=Configures PVGA1A Pins VCLK1 & VCLK2 as Outputs
0=Configures PVGA1A Pins VCLK1 & VCLK2 as Inputs

Bits CNF (2:3) are latched internally at power on reset from the corresponding memory data bus pins MD (2:3), connected to the external pullup or pulldown resistors. Pullup resistor sets MD(2:3) to logic 1. Note, that the configuration bits (2:3) are not readable since they are latched after power up. However, the configuration register bits (4:7) are readable after power up as PR5 bits (4:7). They appear as general purpose read only status bits in the PR5 register.

CNF Bit(2) Bus Architecture Select

Pulled low = IBM Microchannel architecture.
Pulled high = IBM PC AT BUS architecture.

CNF Bit(3) Video Clock Source Control.

CNF bit3 configures PVGA1A pins VCLK1 and VCLK2 as inputs or outputs. It is reset to 0 for inputs and set to 1 for outputs.When used as inputs, these pins supply alternate video dot clocks. The selection of dot clocks is done by an internal multiplexer. When used as outputs, VCLK1 becomes an active low load pulse for an external Paradise Clock chip (the PCLK1), active during I/O writes to the port 3C2. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input.
For more details, refer to the PCLK1 data sheet.

9.0 APPLICATION

The PVGA1A applications chapter is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), analog monitor, and clock. The description and block diagrams are generic. **No attempt is made to present schematic level details.** Currently available application notes, technical briefs, and referenced literature at the end of the data sheet should supplement the information provided in this chapter. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 17 through 25 are shown along with their brief description on the subsequent pages.

9.1 I / O PORT 3C3H - VIDEO SUBSYSTEM ENABLE REGISTER

The Paradise PVGA1A does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I / O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I / O port 102H bit 0) of the Programmable Option Select (POS). When, PVGA1A is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally

The Figure 17 shows a block diagram of the PVGA1A with 8-bit PC/XT interface using 8-bit BIOS. The system data bus SD(0:7) and address bus SA(0:19) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: " * " = Logic **AND** function, " / " = **Inverted** function, and " + " = Logic **OR** function

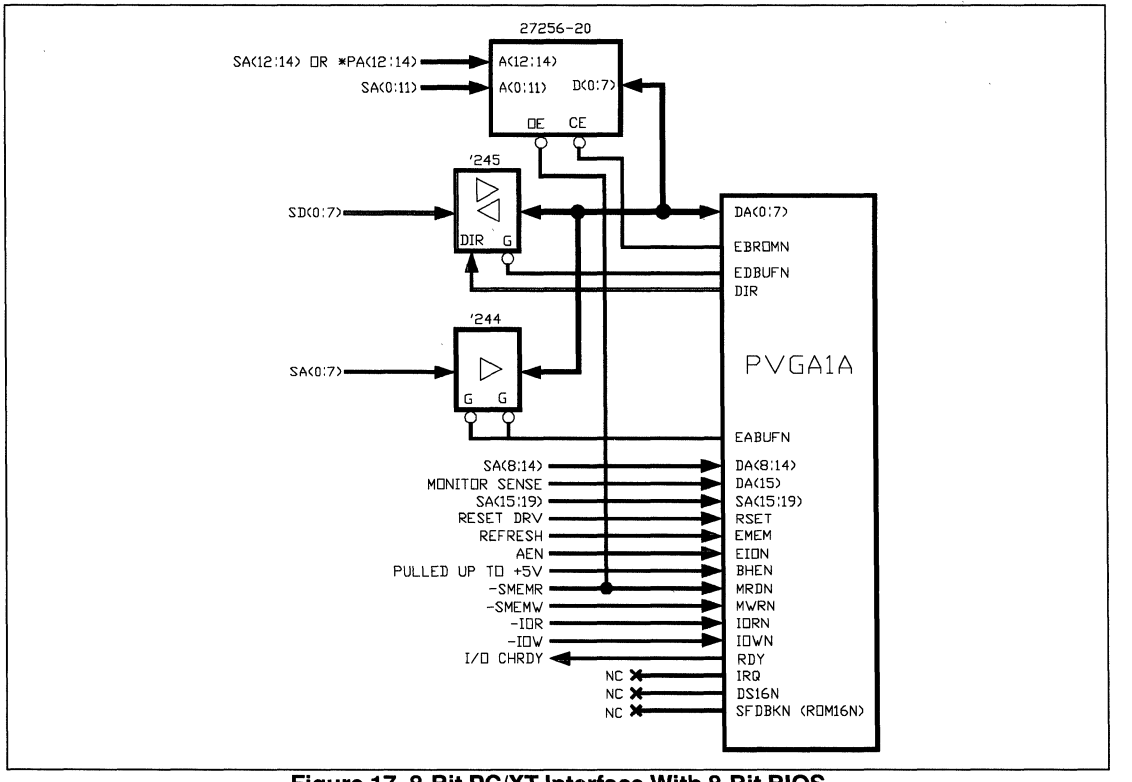


Figure 17. 8-Bit PC/XT Interface With 8-Bit BIOS

Figure 18 illustrates 16-bit PC/AT interface with 8 bit BIOS using PVGA1A. The processor data bus SD(0:15), and the system address bus SA(0:19) are shown. Associated address and data bus buffers, BIOSROM, and auto monitor sense are also shown in it. Note, PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBF1.

/EDBF1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N
+ /EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N

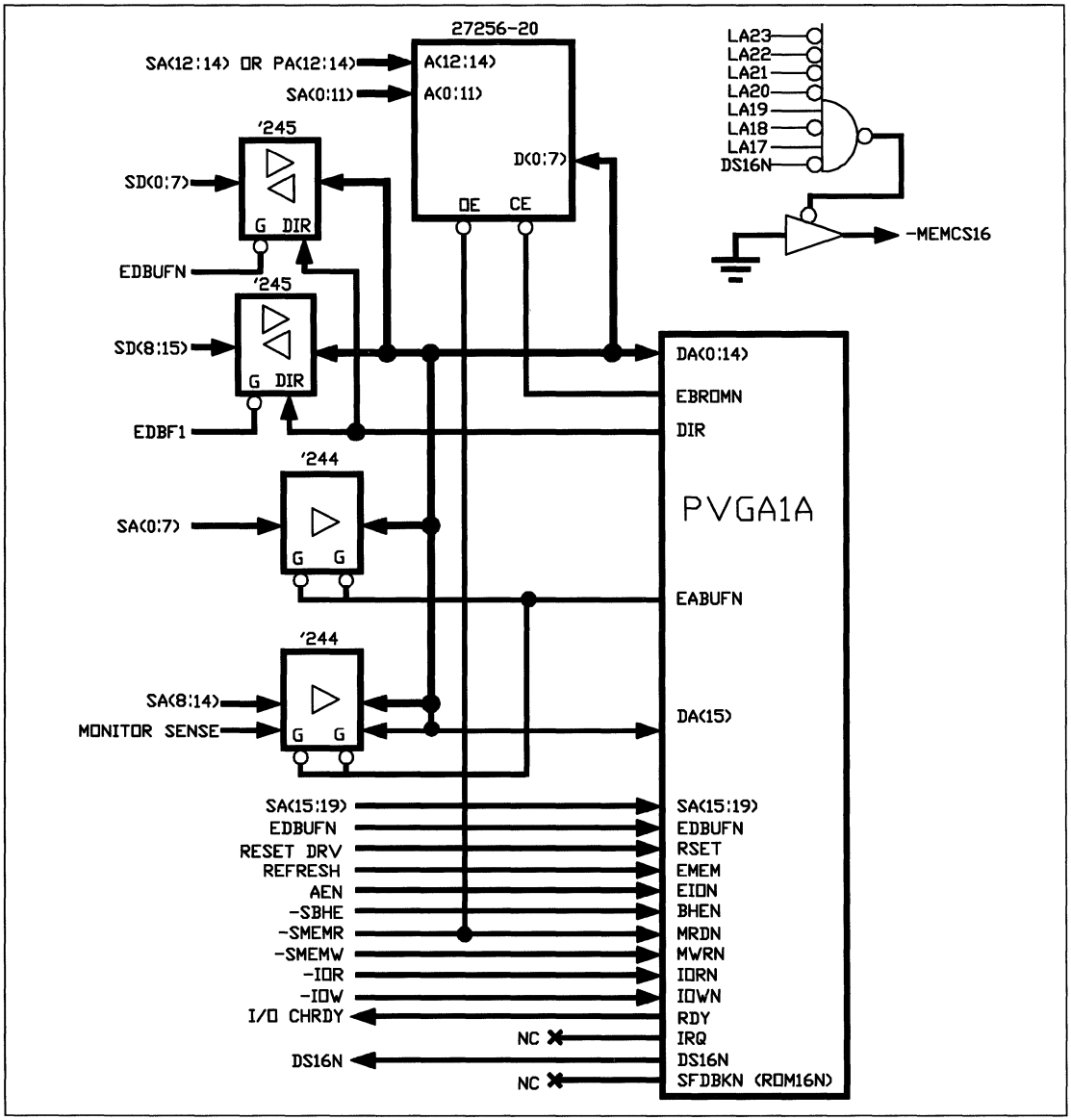


Figure 18. 16-Bit PC/AT Interface With 8-Bit BIOS

Figure 19 describes 16-bit PC/AT interface with 16-bit BIOS ROM implementation using PVGA1A. The system data bus SD(0:15), address bus SA(0:19), address and data bus buffers, and auto monitor sense input is presented. The (16KX8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), and EPROM buffer (Gated by EDBFX) are shown. Note that PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation limits addition of 8 bit cards with memory addresses at the locations of segment C000H for 128 Kbyte memory space. Boolean equations for some of the important signals are listed:

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N
+ /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN

Figure 19 is illustrated on the subsequent page.

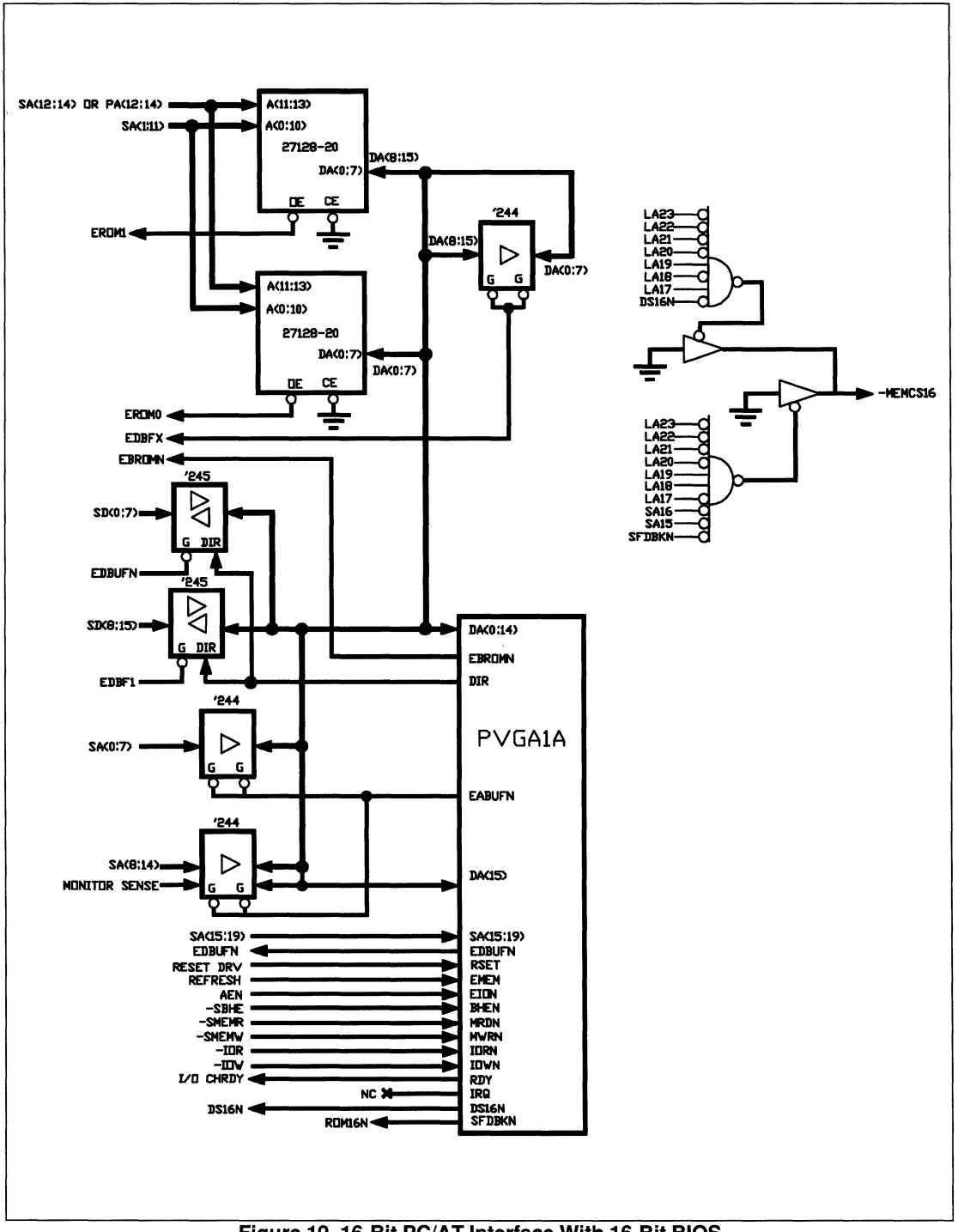


Figure 19. 16-Bit PC/AT Interface With 16-Bit BIOS

Figure 20 indicates PVGA1A and 16-bit Micro Channel interface. The system data bus upper byte bits D(8:14) and lower data bus byte D(0:7) are sampled and buffered for the PVGA1A input pins DA(0:14). Likewise, system address byte upper bits A(8:14) and lower address byte A(0:7) are buffered and gated to the PVGA1A input pins DA(0:14). The most significant system address bits A(15:19) are latched and sent to the PVGA1A. The monitor sense input buffer and D15 are gated into the DA15 input of the PVGA1A. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the PVGA1A.

Associated Boolean equations are shown below:

EMEM = (-CMD) * 3C3.D0 * /A23 * /A22 * /A21 * /A20 * (M/-IO) * (MADE24) +
(-CMD) * 3C3.D0 * /(M/-IO) + /(-CMD) * EMEM

NOTE:

1.0 ASYNCHRONOUS EXTENDED CYCLE (300NS) IS REQUIRED IN THIS CONFIGURATION. SIGNAL (-CD SFDBK) MAY NEED TO BE TRANSPARENTLY LATCHED WITH (-CMD). 3C3 IS AN EXTERNAL I/O PORT.

2.0 RPLTN AND WPLTN GO TO THE RAMDAC.

3.0 WPLTN AND RPLTN TO RAMDAC PORTS 3C6H-3C9H WILL NEED ADDITION OF TWO EXTERNAL WAIT STATES OR EXTERNAL SIGNAL GENERATION AS SHOWN BELOW.

/WPLTN = /(M/-IO) * /(-S0) * (-S1) * /A4 * /A3 * A2 * A1 * (-CMD) * /(-CDSFDBK)
+ /(M/-IO) * /(-S0) *(-S1) * /A4 * A3 * /A2 * /A1 * (-CMD) * /(-CDSFDBK)
+ /(-CMD) * /WPLTN

/RPLTN = /(M/-IO) * (-S0) * /(-S1) * /A4 * A3 * /A2 * /A1 * (-CMD) * /(-CDSFDBK)
+ /(M/-IO) * (-S0) * /(-S1) * /A4 * /A3 * A2 * A1 * /A0 * (-CMD) * /(-CDSFDBK)
+ /(-CMD) * /RPLTN

Figure 20 is drawn on the following page.

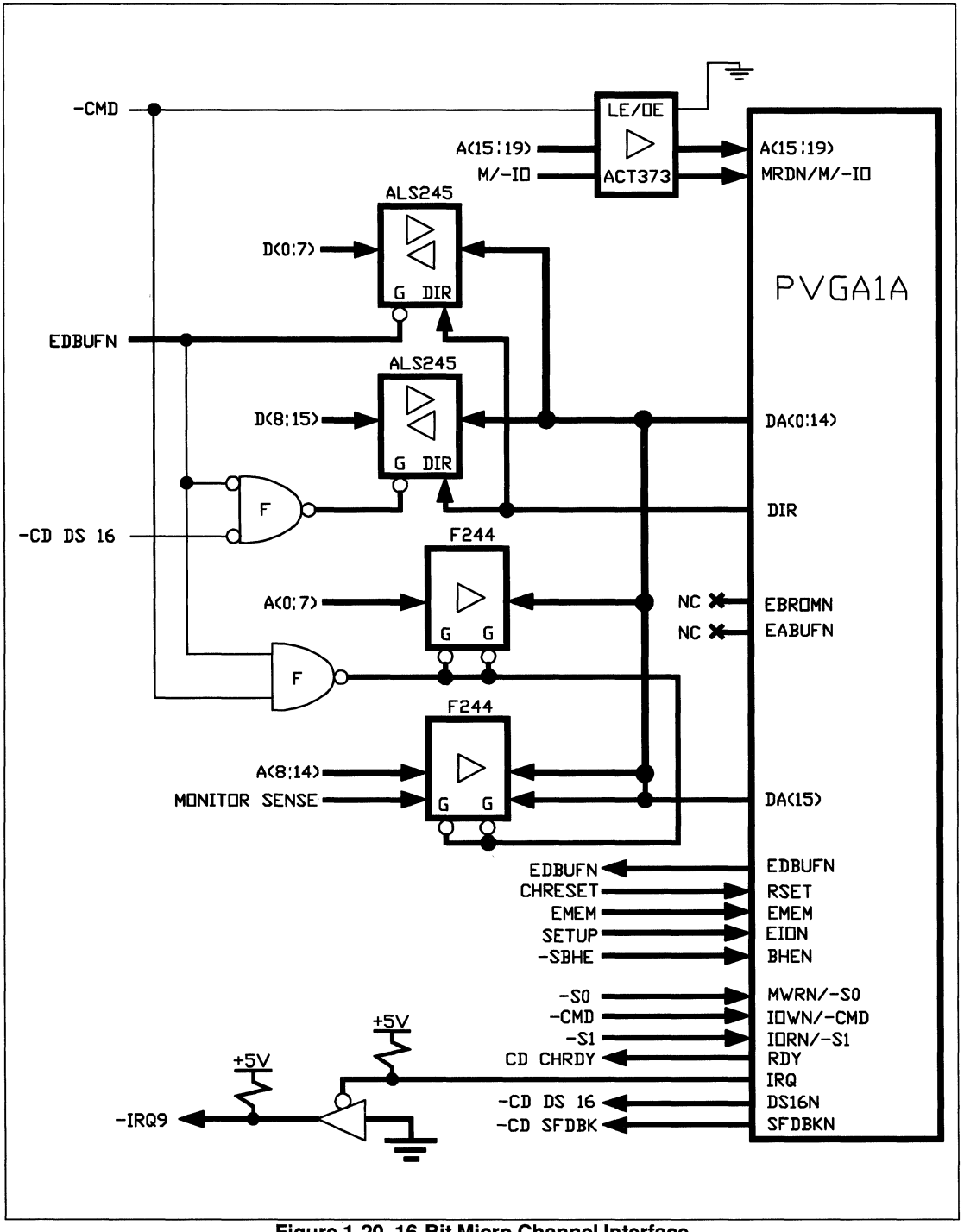


Figure 1-20. 16-Bit Micro Channel Interface

Figure 21 presents PVGA1A with 256 Kbyte video memory organization using four 64 Kbyte maps. Each 64 Kbyte map is made from two (64KX4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles.

The PVGA1A also supports 512 Kbyte, or 1024 Kbyte video memory organization using (64KX4) DRAM modules.

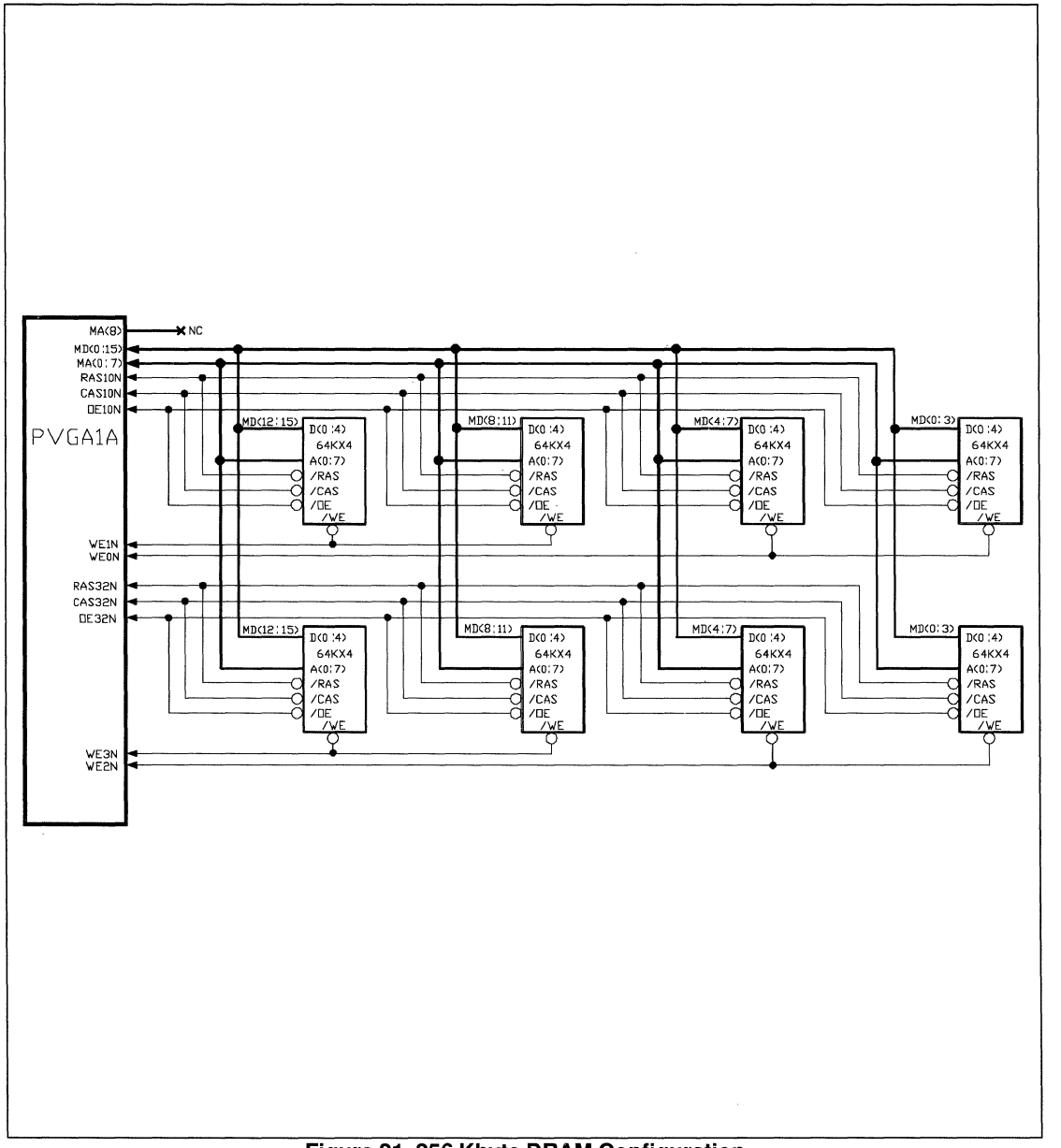


Figure 21. 256 Kbyte DRAM Configuration

Figure 22 illustrates the PVGA1A and RAMDAC (INMOS G171) interface block diagram for analog monitors.

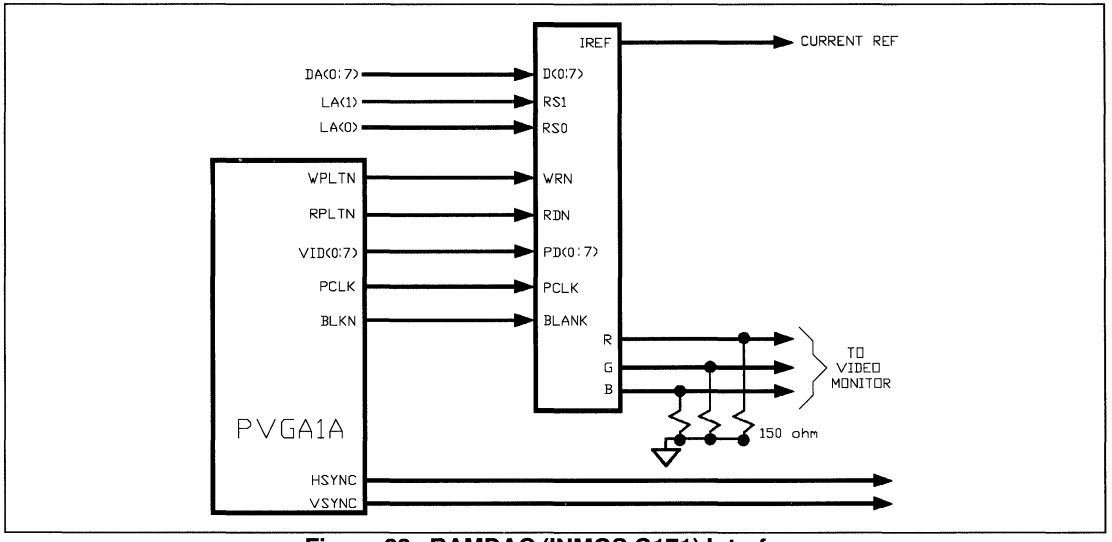


Figure 22. RAMDAC (INMOS G171) Interface

NOTE: LA (1), LA(0) are latched addresses.

Figure 23 shows the PVGA1A and digital monitor connections.

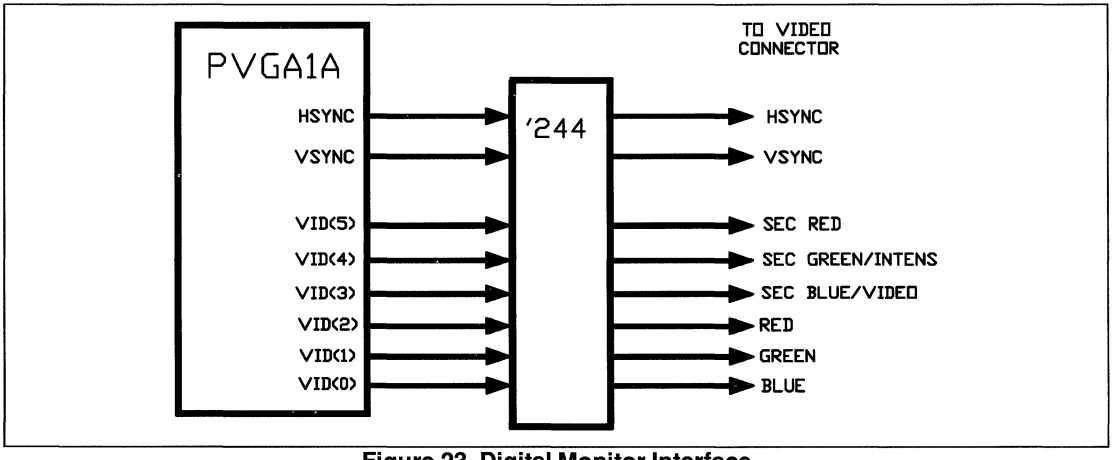


Figure 23. Digital Monitor Interface

Figure 24 presents PVGA1A with external oscillators at the clock pins configured as inputs.. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H Bit 3	3C2H Bit 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the PVGA1A signal pins (VCLK1, VCLK2) inputs.

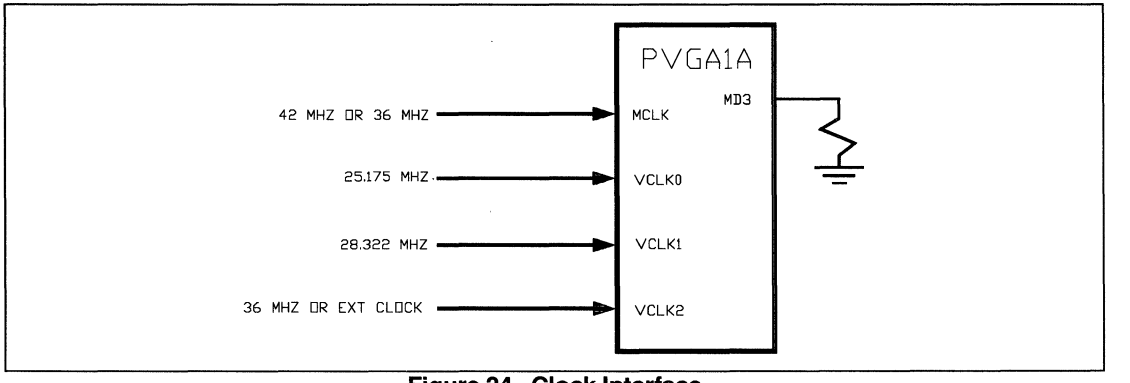


Figure 24. Clock Interface

Figure 25 illustrates PVGA1A pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high. The figure also shows how the VCLK1 and VCLK2 signals can be used to control external input clock multiplexor to select 1 of 8 possible clock frequencies.

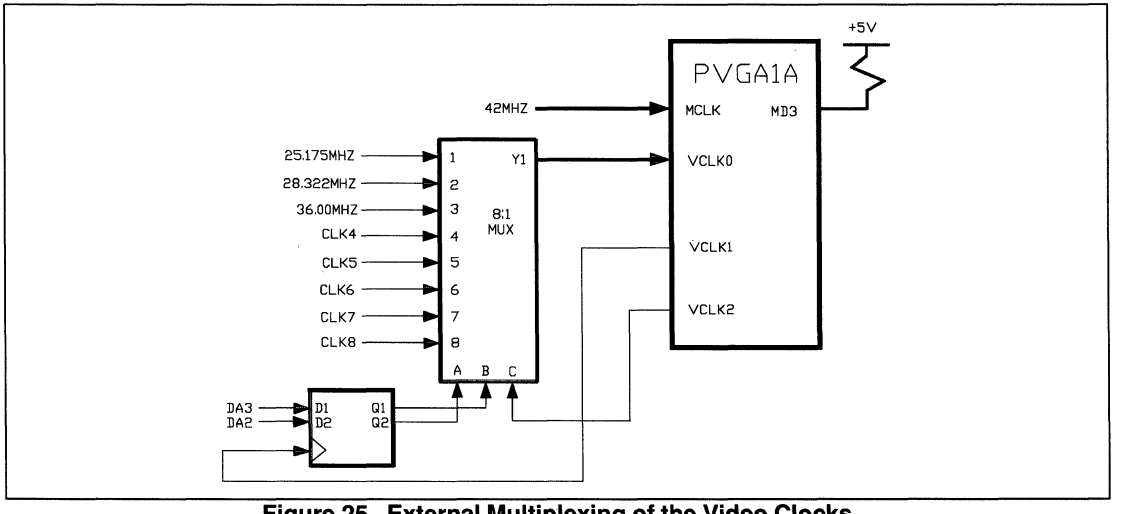


Figure 25. External Multiplexing of the Video Clocks

PVGA1A POWER UP CONFIGURATION

The PVGA1A uses the MD(0:7) input pin to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0) and CNF(7:2) are the internal registers that are configured on power up. CNF(3:2) will latch a noninverted value (pull up resister = 1) into it and the others will latch an inverted value.

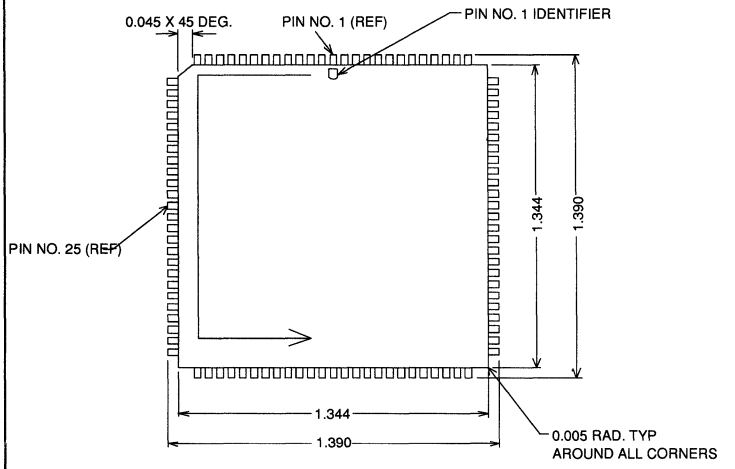
PR1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the PVGA1A. A value of 0 will map it in.

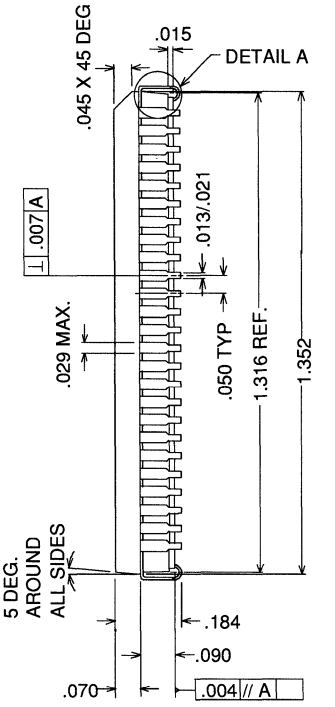
PR1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the PVGA1A that the ROM BIOS data path is 16 bits. The PVGA1A will bring SFDBKN active low in AT mode (static signal) and SFDBKN can be used to externally generate -MEMCS16 (off the AT Bus) for 16-bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the PVGA1A for IBM PC/XT/AT architecture. A value of 0 will configure the PVGA1A for IBM PS/2 Micro Channel Architecture. VGA1A Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the PVGA1A pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

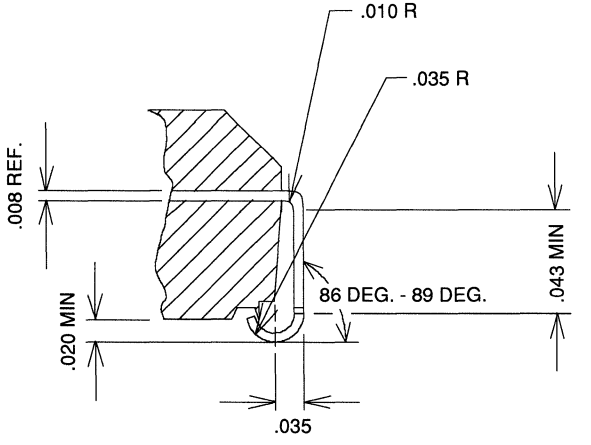
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through Paradise Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If reserved or unused by the BIOS, they are available to the application software.





(TOP VIEW)

DETAIL A



NOTE: All dimensions are in millimeters

Figure 26. 100 Pin PLCC Package

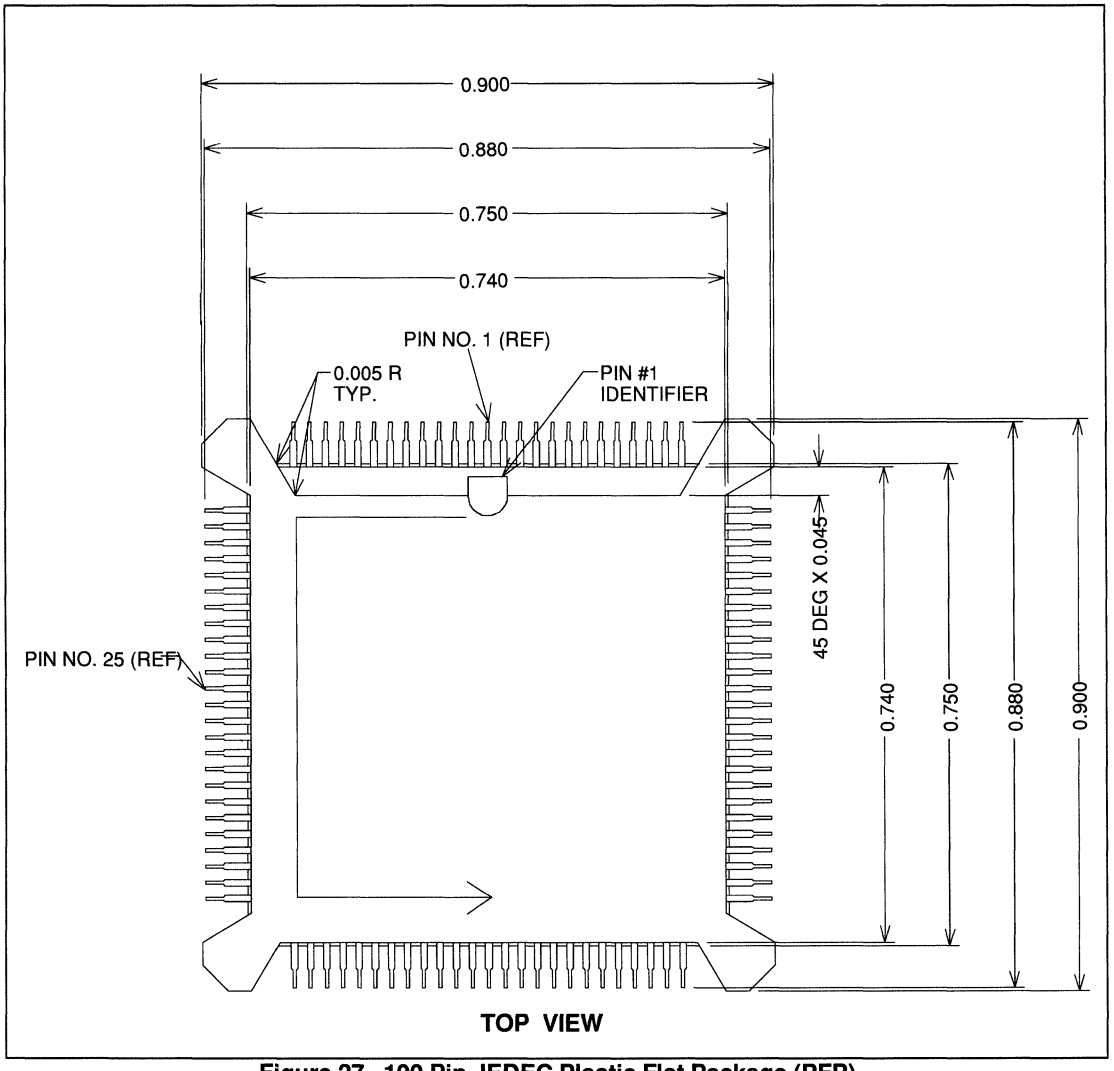


Figure 27. 100 Pin JEDEC Plastic Flat Package (PFP)

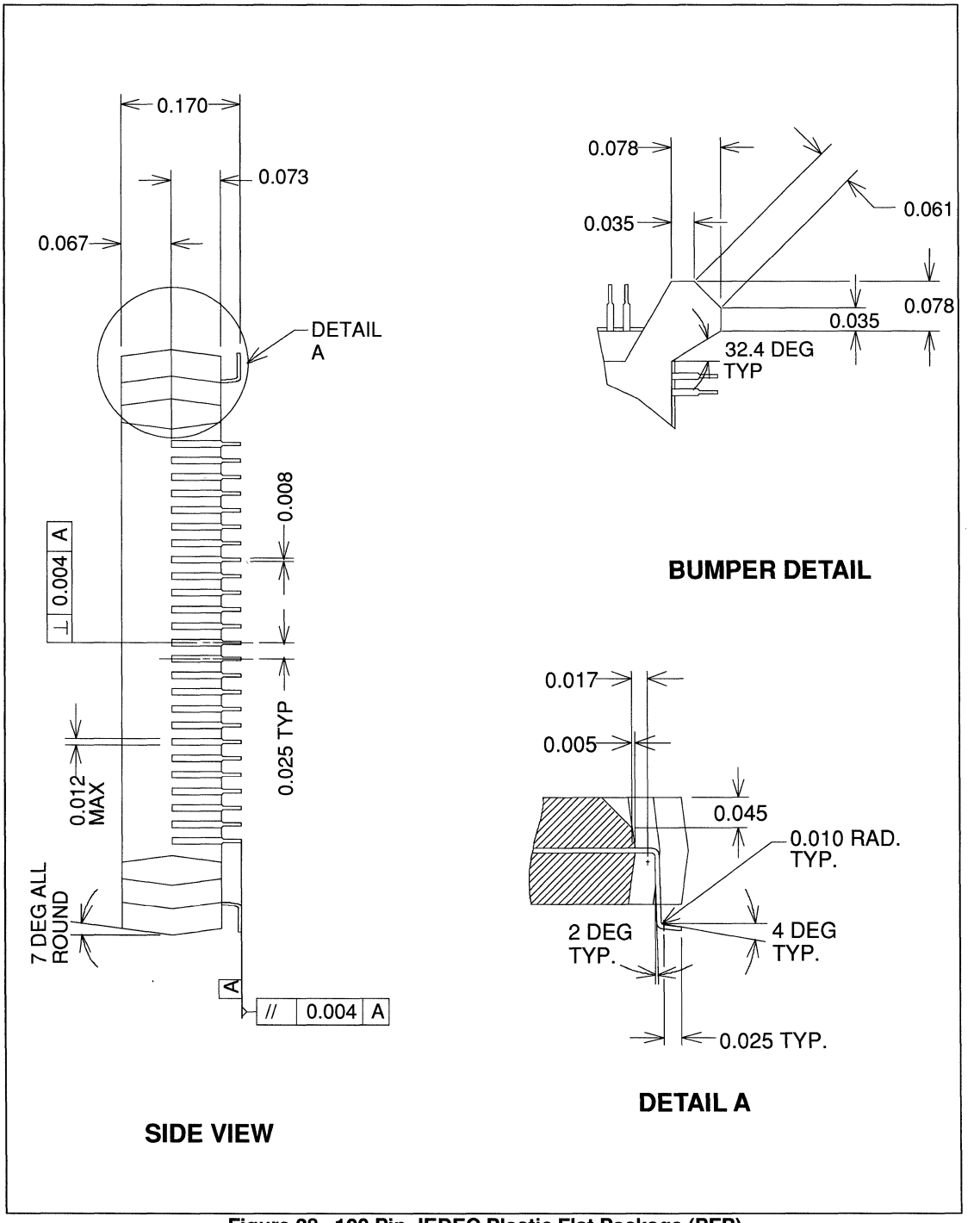


Figure 28. 100 Pin JEDEC Plastic Flat Package (PFP)

REFERENCES

A list of references for generating the PVGA1A data sheet information is shown below:

IBM Personal Computer Hardware User Guide (IBM # 6322510)

IBM Personal Computer XT Hardware User Guide (IBM # 6322511)

IBM Personal Computer AT Hardware User Guide (IBM # 6280066)

IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)

IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)

IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)

IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)

IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)

Personal Computer Reference Manual (IBM # 6025005)

AT &T Video Display Controller VDC 750 / VDC 600 Installation Guide

Hercules Graphics Card Owner's Manual

Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from **other** books and literature available in the market.