WD75C10, WD76C10, WD76C10LP System Controller for 80386SX and 80286 Desktop and Portable Compatibles

WESTERN DIGITAL

TABLE OF CONTENTS

16

Page

Page

16

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD75C10, WD76C10, and WD76C10LP System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD75C10, WD76C10, and WD76C10LP operate similarly and will be referred to in this document as the "System Controller". Where there are differences, the devices will be identified specifically.

1.2 FEATURES

Features Common to WD75C10, WD76C10, and WD76C10LP

- Interfaces with 80286 CPU at speeds of up to 12.5 MHz
- Non-Page mode, zero wait state access, with two-way 100 nsec interleaved memory banks
- Supports 8 Mbytes of real memory, or up to 8 Mbytes of EMS 4.0 using 40 EMS multitasking registers and fast task switching
- Supports memory in four banks with 64 Kbit, 256 Kbit, or 1 Mbit DRAMs
- Employs an internal self-tuning delay line for DRAM control
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and EGA BIOS may be mapped into one physical PROM
- Advanced 64K and 128K ROM shadowing allows main BIOS and video BIOS shadowing along with 320K and 256K remap to extended or expanded memory
- Parity generation and checking
- Low power 1.25 micron CMOS technology
- 132-pin JEDEC plastic QUAD flat package

Additional Features Of WD76C10 and WD76C10LP

- Operates at speeds of 16 MHz, 20 MHz, and 25 MHz
- Interfaces with 80286, or 80386SX CPUs
- Maintains controlled propagation delay for 80386SX reset
- Page mode zero wait state access at 25 MHz with 70 ns DRAM
- Supports 4 Mbit DRAM, up to 16 Mbyte of real memory, or 32 Mbyte of EMS memory
- Supports low-cost cache memory control for any speed 80286 or 80386SX

Additional Features Of WD76C10LP Only

- Power control with suspend and resume
- Processor stop clock
- CAS before RAS refresh for portable applications
- Automatic processor clock speed switching

1.3 GENERAL DESCRIPTION

The WD75C10 is designed for use by low cost AT compatible desktop computers using an 80286 processor at up to 12.5 MHz. The WD76C10 has all the capabilities of the WD75C10 plus the ability to operate in a high performance desktop AT computer using an 80286 or 80386SX processor up to 25 MHz. The WD76C10LP has the features of the WD76C10 and is designed to operate in a high performance laptop AT compatible computer using an 80286 or 80386SX processor.

1.3.1 WD75C10

The WD75C10 contains a high performance memory controller with programmable modes of operation. It supports two-way interleaved, non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, or 1 Mbit DRAM may be controlled, allowing up to 8 Mbytes of real or EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used.

The eight Mbytes of on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

16

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line information is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

1.3.2 WD76C10

The WD76C10 supports all of the features provided by the WD75C10, as well as controlling page mode DRAM or static column DRAM with page mode operation. The WD76C10 also controls 4 Mbit DRAM, allowing up to 16 Mbytes of real memory or 32 Mbytes of EMS memory, for a maximum of 32 Mbytes of on-board memory.

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

An external discrete logic cache controller is supported through the use of a processor ready input signal ($\overline{\text{RDYIN}}$ pin 51). If the external cache makes a zero wait state cache hit cycle, the WD76C10 aborts the DRAM cycle. The WD76C10 only makes DRAM accesses on write cycles and cache read misses.

The WD76C10 interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power-up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.3 WD76C10LP

In addition to supporting all the features of the WD75C10 and WD76C10, the WD76C10LP also supports laptop portables. To provide this support, the WD76C10LP makes use of Power Management Control (PMC) for powering down peripherals or the processor, processor stop clock, slow clock and auto speed clock modes and CAS before RAS refresh. Suspend and resume is supported, where low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 1 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

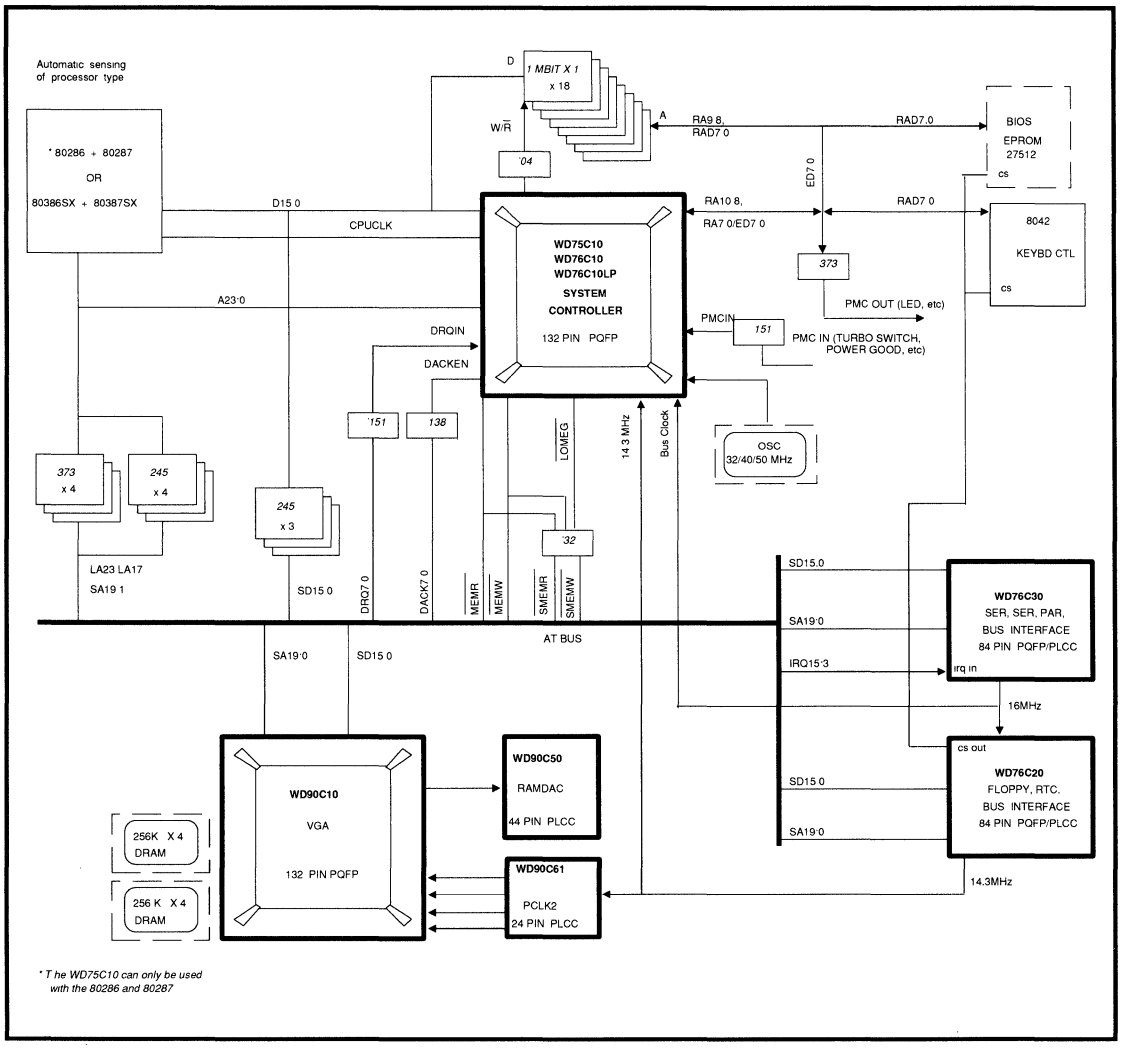

FIGURE 1-1. SYSTEM BLOCK DIAGRAM

16

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control
- Register File

Sections 2.1 through 2.8 provide an overview of these blocks. They are described in more detail in sections 4 through 9.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal which it in turn uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal. It is at this time that the type of processor in use (286, 287 or 386SX, 387SX) is determined.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests, and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the S1[W/R#] signal. The WD75C10 only interfaces with an 80286. This block also controls whether the CPUCLK is to be an input or output. While all three devices have the ability to reduce the processor clock rate, only the WD76C10LP has the ability to stop the clock to the processor. The WD76C10LP also has the ability to power down the processor, at which time it tri-states signals CPUCLK, READY, HOLD, INTRQ, and NMI.

The WD76C10 and WD76C10LP use RDYIN to support an external discrete logic cache controller.

2.4 NUMERIC PROCESSOR CONTROL

While all three System Controllers support an 80287 processor, only the WD76C10 and WD76C10LP support the 80387SX.

2.5 DATA BUS

The Data Bus is a 16 bit (two bytes) bidirectional bus that connects to the processors, System Controllers, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory (for the WD75C10 it is 8 Mbytes of real or 8 Mbytes of expanded memory). All versions of the System Controller supports non-page mode two-way interleaved memory. The WD76C10 and WD76C10LP also provide independent two-way or four-way interleave page mode access to the RAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD76C10LP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable laptop computers. When in a power down state, the WD76C10LP tri-states the CPUCLK, READY, HOLD, INTRQ, and NMI output signals to the main processor.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at port 1872, serve more than one area. In this instance the register description appears only in one section, but is referred to in all appropriate sections.

The registers and the section in which they are described are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092 - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072 and E872, all registers located at Ports 1072 through F872 are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72 twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72 - Read only

15	14	13	12	11	10	09	08
T				DMA #2			
				CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1				P			
CH3	CH2	CH1	CH0				

Bits 11-03 are particularly usefull in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bit 03 - P, Parallel Port direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit refer to the WD76C30 Data Book, section 6.2.5

Bits 02-00 - Not used, state is ignored

16

2.8.2 Lock/Unlock Register

Port Address F073 - Write only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
L/UL							

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -
11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -
Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

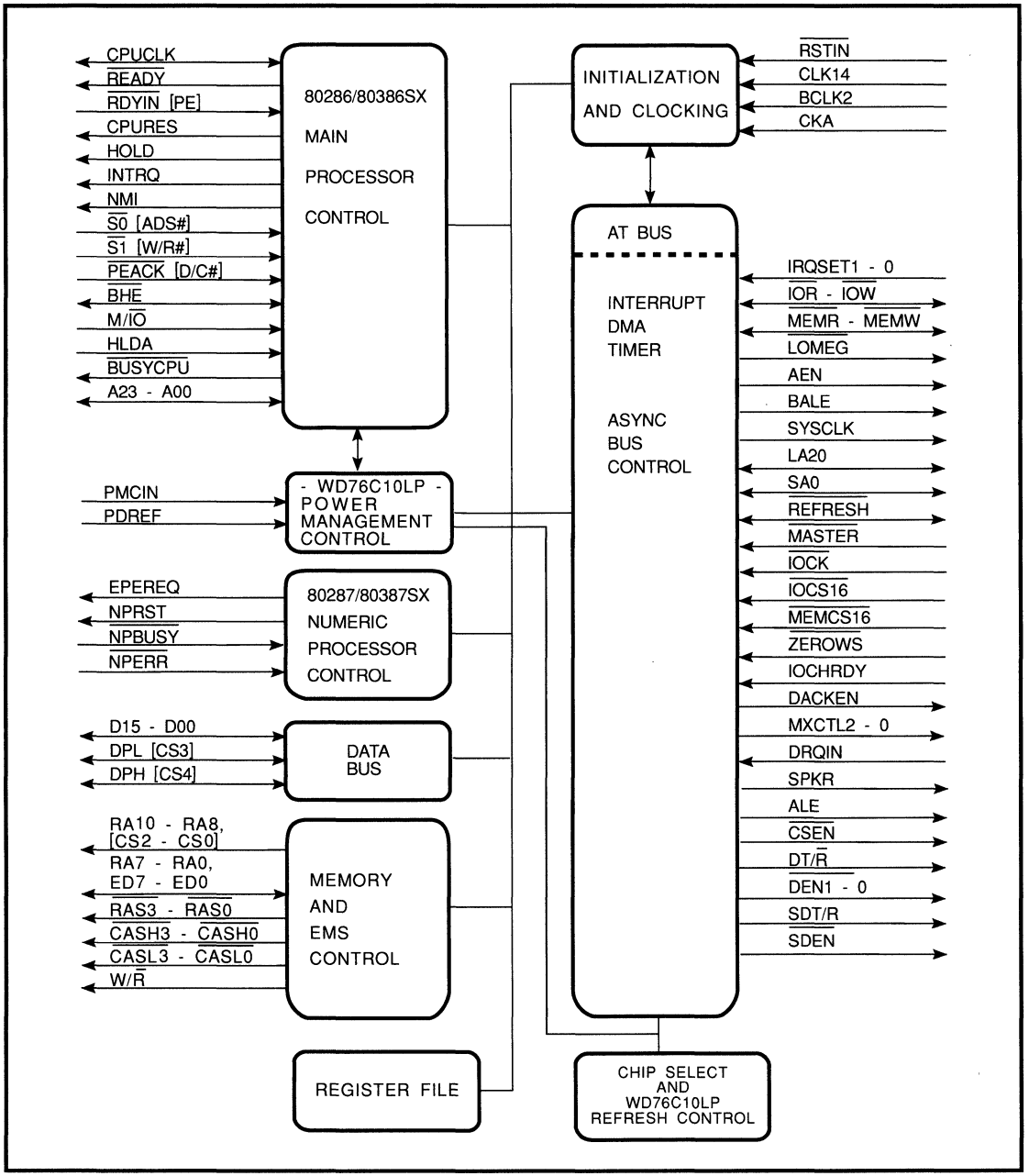

FIGURE 2-1. WD75C10, WD76C10, AND WD76C10LP BLOCK DIAGRAM

16

PORT ADDRESS	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	7.5, Table 7-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real Time Clock Address Register	No	5.8.1
071 - 07F odd	Real Time Clock Data Register	No	5.8.2
080 - 09F	(except 092) DMA Page Registers	No	
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	CLEAR 287 BUSY	No	5.3.2
00F1	RESET 287/387SX	No	5.3.3
1072	Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	7.1
2872	Chip Selects	Yes	7.2
3072	Programmable Chip Select Address	Yes	7.3
3872	Memory Control	Yes	6.2.1
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
6072	RAM Shadow And Write Protect	Yes	6.2.4
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
7072	PMC Output Control 7:0	Yes	8.1
7872	PMC Output Control 15:8	Yes	8.1
8072	PMC Timers	Yes	8.2
8872	PMC Inputs 7:0	Yes	8.3
9072	NMI Status	Yes	8.5
9872	Diagnostic	Yes	9.1
A072	Delay Line	Yes	9.2
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	8.4
D072	Shadow Register		8.6
E072	EMS Page Register Pointer	No	6.4.2
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	7.5, Table 7-1
F472	48 MHz Oscillator Enable	Yes	7.5, Table 7-1
F872	Cache Flush	Yes	7.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	Yes	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX

3.0 PIN DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - RA5/ED5	36 - LOMEG	68 - D11	103 - A8
2 - Vcc	37 - MEMW	69 - Vcc	104 - A7
3 - RA4/ED4	38 - MEMR	70 - D12	105 - A6
4 - RA3/ED3	39 - IOW	71 - D13	106 - A5
5 - Vss	40 - IOR	72 - D14	107 - A4
6 - RA2/ED2	41 - BHE	73 - D15	108 - A3
7- -RA1/ED1	42 - NPERR	74 - DT/R	109 - A2
8 - RA0/ED0	43 - PEACK [D/C#]	75 - DEN1	110 - IRQSET1
9 - CASH2	43 - WD75C10	76 - DEN0	111 - IRQSET0
10 - CASL2	NOT USED	77 - SYSCLK	112 - MXCTL0
11 - RAS2	44 - M/IO	78 - CPURES	113 - MXCTL1
12 - CASH3	45 - S0 [ADS#]	79 - BALE	114 - MXCTL2
13 - CASL3	46 - S1 [W/R#]	80 - A23	115 - CSEN
14 - RAS3	47 - READY	81 - A22	116 - DACKEN
15 - DPH [CS4]	48 - HLDA	82 - A21	117 - RESERVED -
16 - DPL [CS3]	49 - HOLD	83 - IOCK	WD75C10
17 - RSTIN	50 - BCLK2	84 - CLK14	117 - PDREF -
18 - DRQIN	51 - RDYIN [CKA]	85 - NPBUSY	WD76C10LP
19 - IOCHRDY	[PE]	86 - A0 [BLE#]	118 - PMCIN
20 - ZEROWS	52 - CPUCLK	87 - A1	119 - W/R
21 - IOCS16	53 - BUSYCPU	88 - A20	120 - CASH0
22 - MEMCS16	54 - NMI	89 - A19	121 - CASL0
23 - SPKR	55 - INTRQ	90 - A18	122 - RAS0
24 - SA0	56 - D0	91 - A17	123 - CASH1
25 - LA20	57 - D1	92 - A16	124 - CASL1
26 - MASTER	58 - D2	93 - A15	125 - RAS1
27 - ALE	59 - D3	94 - A14	126 - RA10 [CS2]
28 - AEN	60 - D4	95 - A13	127 - RA9 [CS1]
29 - SDEN	61 - D5	96 - A12	128 - RA8 [CS0]
30 - SDT/R	62 - D6	97 - A11	129 - Vss
31 - Vcc	63 - D7	98 - Vss	130 - RA7/ED7
32 - REFRESH	64 - D8	99 - Vss	131 - RA6/ED6
33 - Vss	65 - D9	100 - A10	132 - Vss
34 - EPEREQ	66 - D10	101 - Vcc	
35 - NPRST	67 - Vss	102 - A9	

TABLE 3-1. PIN ASSIGNMENTS

NOTE: Some pins are multi-functional depending upon the mode of operation. The alternate signal for these pins is enclosed in [].

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		INITIALIZATION AND CLOCKING		
17	$\overline{\text{RSTIN}}$	System Reset	I	$\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at power up. For a detailed description, refer to Section 4, Initialization And Clocking.
50	BCLK2	Bus Clock	I	BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input. BCLK2 may also be used to drive the processor clock. For additional information, refer to section 4, Initialization And Clocking.
84	CLK14	Clock 14	I	CLK14 is derived from a 14.3 MHz oscillator and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
		AT BUS		
40	$\overline{\text{IOR}}$	I/O Read	I/O	$\overline{\text{IOR}}$ is an output and asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. $\overline{\text{IOR}}$ is an input during Master Mode.
39	$\overline{\text{IOW}}$	I/O Write	I/O	$\overline{\text{IOW}}$ is an output and asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. $\overline{\text{IOW}}$ is an input during Master Mode.
38	$\overline{\text{MEMR}}$	Memory Read	I/O	$\overline{\text{MEMR}}$ is an output and is asserted by the System Controller when a memory read access to the AT bus is to take place. $\overline{\text{MEMR}}$ is an input during Master Mode.

TABLE 3-2. PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
37	$\overline{\text{MEMW}}$	$\overline{\text{Memory Write}}$	I/O	$\overline{\text{MEMW}}$ is an output and asserted by the System Controller when a memory write access to the AT bus is to take place. $\overline{\text{MEMW}}$ is an input during Master Mode.
36	$\overline{\text{LOMEG}}$	First Megabyte	O	$\overline{\text{LOMEG}}$ is asserted when the AT bus address is below 1 Mbyte. Used with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ to generate $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$.
28	AEN	Address Enable	O	AEN is asserted by the System Controller while performing DMA and Refresh cycles.
79	BALE	AT Bus Address Latch Enable	O	Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
77	SYSCLK	System Clock	O	In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.
25	LA20	Early Address 20	I/O	When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
24	SA0	System Address 0	I/O	When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line. When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
32	$\overline{\text{REFRESH}}$	$\overline{\text{Refresh}}$	I/O	As an output, $\overline{\text{REFRESH}}$ is asserted by the System Controller to refresh memory on the AT Bus. As an input, $\overline{\text{REFRESH}}$ is asserted by the Bus Master in conjunction with $\overline{\text{MEMR}}$ to refresh memory on the AT Bus and DRAM controlled by the System Controller.
26	$\overline{\text{MASTER}}$	$\overline{\text{Master}}$	I	$\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to become input signals.
83	$\overline{\text{IOCK}}$	$\overline{\text{I/O Check}}$	I	When asserted, $\overline{\text{IOCK}}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
21	$\overline{\text{IOCS16}}$	$\overline{\text{16 Bit I/O Cycle}}$	I	Initiates a 16 bit I/O AT bus cycle.
22	$\overline{\text{MEMCS16}}$	$\overline{\text{16 Bit Memory Cycle}}$	I	Initiates a 16 bit memory AT bus cycle.
20	$\overline{\text{ZEROWS}}$	$\overline{\text{Zero Wait States}}$	I	Initiates a zero wait AT bus cycle.
19	IOCHRDY	I/O Channel Ready	I	Initiates wait states during AT bus cycles.
116	DACKEN	DACK Enable	O	When DACKEN is asserted, MXCTL2-0 are used to generated DACK7-5, 3-0, and BUS_RST. Refer to Table 5-1 and Figure 5-1.
114	MXCTL2	Multiplexer Control 2	O	MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0, and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, and A20GT. Refer to Table 5-1 and Figure 5-1.
113	MXCTL1	Multiplexer Control 1	O	
112	MXCTL0	Multiplexer Control 0	O	

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
18	DRQIN	Multiplexed DRQ Inputs	I	DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1.
110	IRQSET1	Interrupt Request Set 1	I	IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
111	IRQSET0	Interrupt Request Set 0	I	IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, CPURES, IRQ8, IRQ9 - IRQ11, IRQ14, and IRQ15. Refer to Table 5-1 and Figure 5-1.
23	SPKR	Speaker	O	SPKR drives the speaker transistor and is used for diagnostics.
27	ALE	Address Latch Enable	O	ALE is used to clock the SA1 - SA19 address latches.
115	$\overline{\text{CSEN}}$	Chip Select Enable	O	When asserted, DPH, DPL, and RA10-RA8 are used to generate one of 24 different chip selects.
74	DT/$\overline{\text{R}}$	Data Transmit/ Receive	O	DT/$\overline{\text{R}}$ controls the direction of the AT Data Bus D00 - D15. When DT/$\overline{\text{R}}$ is high, data is directed to the AT Bus. When DT/$\overline{\text{R}}$ is low, data is transferred from the AT bus.
76	$\overline{\text{DEN0}}$	Data Bus Enable 0	O	When asserted, $\overline{\text{DEN0}}$ enables the low order byte data buffer.
75	$\overline{\text{DEN1}}$	Data Bus Enable 1	O	When asserted, $\overline{\text{DEN1}}$ enables the high order byte data buffer.
29	$\overline{\text{SDEN}}$	Swap Data Enable	O	$\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
30	SDT/$\overline{R}$	Swap Data Transmit/ $\overline{\text{Receive}}$	O	When SDT/$\overline{R}$ is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{R}$ is low, it directs data from the high byte of the AT bus to the low byte.
		MAIN PROCESSOR CONTROL		
52	CPUCLK	Processor Clock	I/O	CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at port address 1072. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.
47	$\overline{\text{READY}}$	$\overline{\text{Processor Ready}}$	O	$\overline{\text{READY}}$ is an output to the processor.
51	$\overline{\text{RDYIN}}$/CKA/ PE	$\overline{\text{Processor Ready In}}$/ Alternate Clock/ Parity Error	I	Whether pin 51 is to be used as $\overline{\text{RDYIN}}$, CKA, or PE is determined by the Memory Control Register at port address 3872. $\overline{\text{RDYIN}}$ is used in a discrete cache system and indicates a hit or miss. CKA may be used as an alternate source for CPUCLK processor clock. When used as PE, it indicates a parity error from an external memory controller.
78	CPURES	Main Processor Reset	O	CPURES is a synchronous processor reset signal.
49	HOLD	Hold Request	O	Processor hold cycle request.
55	INTRQ	Interrupt Request	O	Processor interrupt cycle request.
54	NMI	Non-Maskable Interrupt	O	Processor non-maskable interrupt cycle request.
45	$\overline{\text{S0}}$ [ADS#]	$\overline{\text{Processor Status 0}}$ [Address Status]	I	In the 80286 mode this pin is $\overline{\text{S0}}$. In the 80386SX mode this pin is ADS#.

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MAIN PROCESSOR CONTROL (cont.)		
46	$\overline{S1}$ [W/R#]	Processor Status 1 [Write Read]	I	In the 80286 mode pin 46 is $\overline{S1}$. In the 80386SX mode pin 46 is W/R#
4	$\overline{BHE}$	Bus High Enable	I/O	As an input, $\overline{BHE}$ indicates a transfer of the high byte on the processor data bus. $\overline{BHE}$ is an output during DMA transfers.
43	$\overline{PEACK}$ [D/C#]	Processor Extension Acknowledge [Data/Control]	I	In the 80286 mode pin 43 is $\overline{PEACK}$. In the 80387SX mode pin 43 is D/C#. This pin is not used by the WD75C10.
44	M/$\overline{IO}$	Memory or $\overline{I/O}$	I	Processor Memory cycle or $\overline{I/O}$ Status cycle.
48	HLDA	Hold Acknowledge	I	Processor hold acknowledge.
53	$\overline{BUSYCPU}$	Processor Busy	O	Numeric Processor Busy (80287 or 80387SX) signal to CPU (80286 or 80386SX).
80 - 82 88 - 97 100 102 - 109 87 86	A23 - A21 A20 - A11 A10 A9 - A2 A1 A0, [BLE#]	Processor Address A23 through A00, Bus Low Enable	I/O	A23 through A1 are address lines from the 80286 or 80386SX. A0 is address bit A0 for the 80286, BLE# for the 80386SX, and is controlled by SA0 (AT Bus pin 24) during Master Mode operations. A21, A19 through A1 are outputs during refresh and DMA cycles and inputs in other modes. A20 and A0 are outputs during refresh, DMA and Master mode cycles, and inputs in other modes.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		NUMERIC PROCESSOR CONTROL		
34	EPEREQ	Extend PERQ	O	PERQ extend signal to the 80386 for IRQ13 handling. Used only for the 80386SX.
35	NPRST	Numeric Processor Reset	O	Reset to the numeric processor 80287 or 80387SX.
42	NPERR	Numeric Processor Error	I	Error signal from the numeric processor 80287 or 80387SX.
85	NPBUSY	Numeric Processor Busy	I	Busy signal from the numeric processor 80287 or 80387SX.
		DATA BUS		
73 - 70 68 66 - 56	D15 - D12 D11 D10 - D0	Data Bit 15 - Data Bit 12, Data Bit 11 Data Bit 10 - Data Bit 0	I/O	The Data Bits are connected directly to the Local and Numeric processors, DRAM data, and AT Bus data transceivers.
16	DPL [CS3]	Data Parity Low Byte [Chip Select 3}	I/O	For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.
15	DPH [CS4]	Data Parity High Byte [Chip Select 4]	I/O	For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.
		MEMORY AND EMS CONTROL		
126 - 128	RA10/CS2 RA9/CS1 RA8/CS0	DRAM Address Bit 10 through DRAM Address Bit 8, Chip Select 2 through Chip Select 0	O	The DRAM Address Bus is multi-functional. During DRAM cycles, RA10 through RA0 select the DRAM Row and Column.
130, 131 1, 3, 4, 6 - 8	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	DRAM Address Bit 7 through DRAM Address Bit 0, EDATA 7 through 0	I/O	During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MEMORY AND EMS CONTROL (cont.)		
14, 11, 125, 122	$\overline{RAS3}$ $\overline{RAS2}$ $\overline{RAS1}$ $\overline{RAS0}$	Row Address Select 3 through Row Address Select 0	O	$\overline{RAS3}$ through $\overline{RAS0}$ are designed to access the DRAM without the use of external drivers.
12, 9, 123, 120	$\overline{CASH3}$ $\overline{CASH2}$ $\overline{CASH1}$ $\overline{CASH0}$	Column Address Select High 3 through Column Address Select High 0	O	$\overline{CASH3}$ through $\overline{CASH0}$ are designed to access the DRAM without the use of external drivers.
13, 10, 124, 121	$\overline{CASL3}$ $\overline{CASL2}$ $\overline{CASL1}$ $\overline{CASL0}$	Column Address Select Low 3 through Column Address Select Low 0	O	$\overline{CASL3}$ through $\overline{CASL0}$ are designed to access the DRAM without the use of external drivers.
119	W/$\overline{R}$	Write/$\overline{Read}$	O	W/$\overline{R}$ is output as a high signal to write to memory and output as a low signal to read from memory. W/$\overline{R}$ should be buffered before use.
		POWER MANAGEMENT CONTROL		
117	PDREF	Power Down Refresh	I	PDREF is a 64 KHz signal from the WD76C20. During power down, PDREF is passed internally to pin 32 ($\overline{REFRESH}$).
118	PMCIN	Power Management Control Input	I	PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
		MISCELLANEOUS		
5, 33, 67, 98, 99, 129 132	Vss		I	Ground (7 pins)
2, 31, 69, 101	Vcc		I	+5 Volts (4 pins)

TABLE 3-2. PIN DESCRIPTION cont.

16

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK), and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, RSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor and also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which is decoded externally as DACK4. DACK4 is used to drive the bus reset signal. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the WD76C10 or WD76C10LP enter the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. The WD75C10 only operates with an 80286. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA, and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.3 MHz oscillator and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD76C20 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872. SYSCLK will always be one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds of 40 MHz or higher, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872. The PMC control output 0 tri-states the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by Port Address 1072 bits 1 or 0, or divided down by bits 14, 13 and 12. Only the WD76C10LP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so bits 14, 13 and 12 also provide some choices of clock duty cycle. The other method is used when the CPUCLK is an input and generated by an external oscillator. In this case, bits 6, 5 and 4 are used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is established by the setting of bit 15 at Port Address 1072.

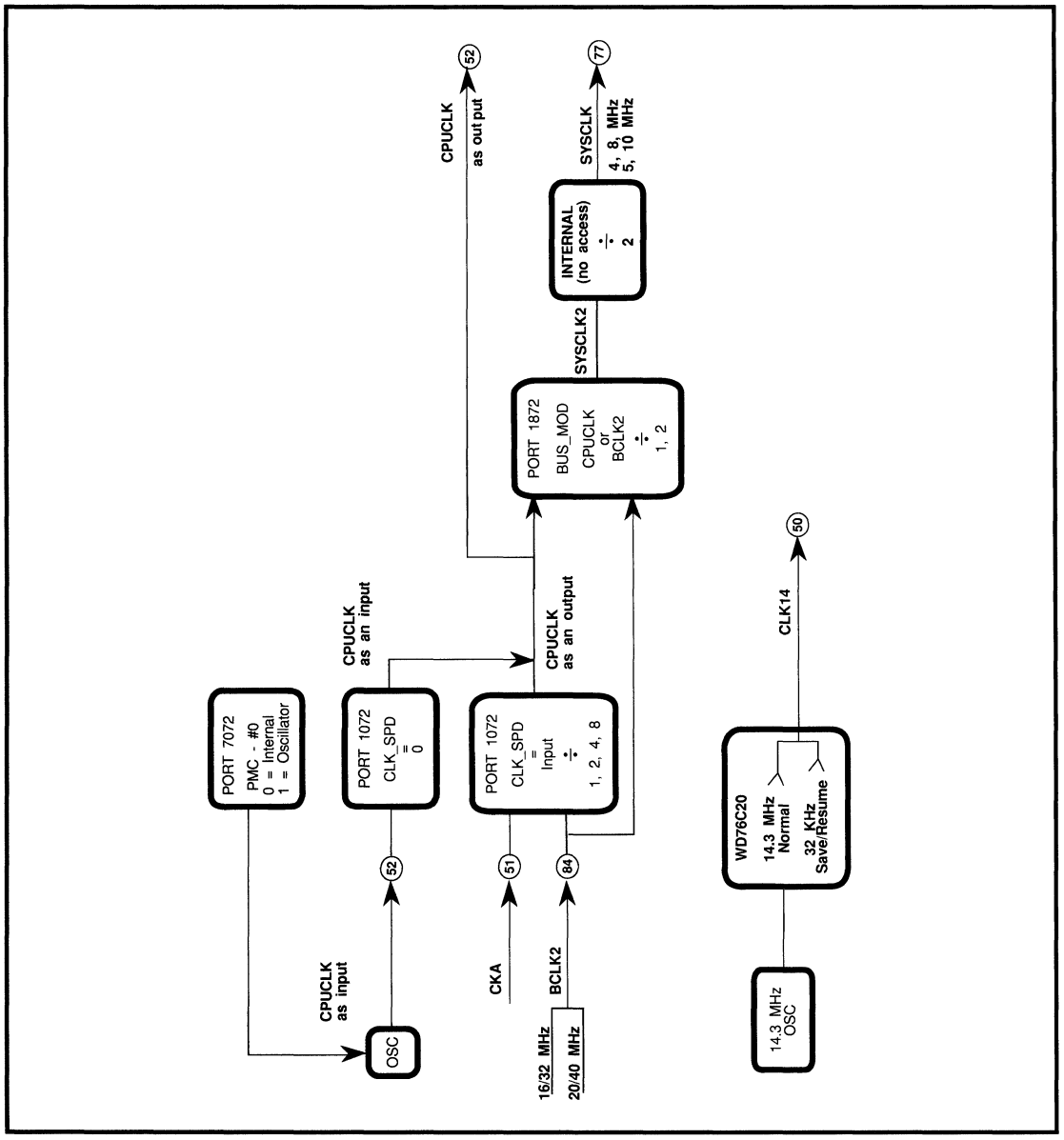

FIGURE 4-1. CLOCK CONTROL

16

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072 - Read and Write

15	14 13 12	11	10 09 08
SRC	CLK_SPD	AUT_ FST	ALT_CLK_SP

07	06 05 04	03	02	01	00
	EXT_HOLD			SCH	SCHH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	001
AUT_FST ☆	0
ALT_CLK_SPD ☆	000
EXTEND_HOLD	000
SCH ☆	0
SCHH ☆	0

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Bit 15 - SRC, CPUCLK clock source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted.

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state during this period.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK clock speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD defaults to 001 at power up. Changing the CPUCLK from an input (000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One µs later, CPUCLK becomes active as an output. One µs and 16 CPUCLK clocks (or one ms) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated because the clock driver cannot synchronously switch the clock. The one µs and 16 clocks or one ms. selection is made through the Diagnostic Register at Port 9872.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source.
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

Bit 11 - AUT_FST, Auto clock speed
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When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external $\overline{\text{TURBO}}$ signal is de-asserted when auto-speed is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-1. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external $\overline{\text{TURBO}}$ signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCH or SCHH field is programmed to stop the clock. The clock

restarts or returns to the faster rate when any interrupt occurs.

Table 4-1 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
No Automatic Clock Switching

AUT_FST = 1 -
Automatic CPUCLK Switching. The EXT_HOLD field must be 000 when AUT_FST = 1

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-1. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate clock speed
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ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value)

0 0 1 - Equals source

0 1 0 - Equals source div by 2

0 1 1 - Equals source div by 4, 25% duty cycle

1 0 0 - Equals source div by 4, 75% duty cycle

1 0 1 - Equals source div by 8, 12% duty cycle

1 1 0 - Equals source div by 8, 88% duty cycle

Bits 07-04 - EXT_HOLD, Extend processor hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external $\overline{\text{TURBO}}$ signal is asserted, EXT_HOLD is forced to 000. When the external $\overline{\text{TURBO}}$ signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value)

0 0 0 1 - 1 µs hold after refresh

0 0 1 0 - 2 µs hold after refresh

0 0 1 1 - 3 µs hold after refresh

0 1 0 0 - 4 µs hold after refresh

↕

1 1 0 1 - 13 µs hold after refresh

1 1 1 0 - 14 µs hold after refresh

1 1 1 1 - 15 µs hold after refresh

Bits 03-02 - Reserved for future use, should be set to zero

Bit 01 - SCH, Stop CPUCLK at next Hold
Featured only in the WD76C10LP

SCH is applicable only for 80286 type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10LP instead of an external oscillator.

Any unmasked processor interrupt or NMI restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at port address 041, or at the slower rate as selected by the Refresh Control Register at Port 2072.

SCH = 0 -
Normal processor clock (Default value)

SCH = 1 -
Stop processor clock at next processor hold cycle

16

Bit 00 - SCHH, Stop CPUCLK at next Halt and Hold. Featured only in the WD76C10LP

SCHH is applicable only for 80286 type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10LP instead of an external oscillator.

Any unmasked processor interrupt or NMI restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at port address 041, or at the slower rate selected by the Refresh Control Register at Port 2072.

SCHH = 0 -
Normal processor clock (default value)

SCHH = 1 -
Stop processor clock at next halt and hold cycle

5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8), and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external '138 3 to 8 decoder uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 8 to 1 multiplexer to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{RSTIN}$ to determine ROM data width (ROM8). The CPURES and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus And Terminal Count (TC) Signal

The AT Address Bus SA19-00 and $\overline{BHE}$ are generated from A19-00 with external latches and tri-state buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and $\overline{CSEN}$ are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD75C10 and WD76C10, the TURBO signal may be connected directly to PMCIN. In the WD76C10LP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of port 1872 (Section 5.3) control the power down of the processor and peripheral.

16

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{\text{IRQ8}}$	IRQ12	$\overline{\text{TURBO}}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	CPURES	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

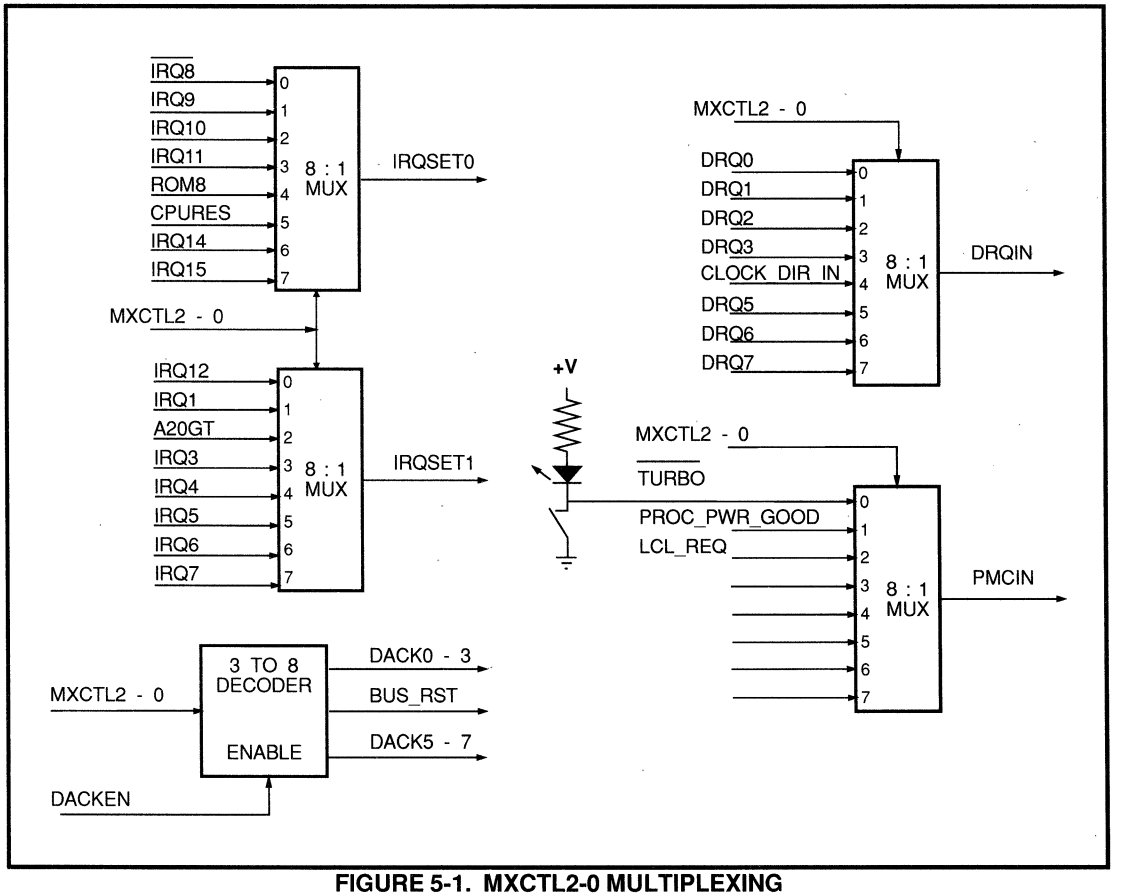

FIGURE 5-1. MXCTL2-0 MULTIPLEXING

5.3 NUMERIC PROCESSOR

5.3 .1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872 - Read and Write

15	14	13	12	11	10	09	08
NP_ BSY	PRO_ PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI_ 16	WSM_ 16	WSI8		WSM8	

Signal Name	Default At RSTIN
NP_BSY	0
PRO_PD ☆	0
FPD ☆	0
BUS_MOD	0 0
BRQ_DEL	0 0
BAK_DEL	1 1
WSI_16	0
WSM_16	0
WS18	1 0
WSM8	1 0

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Bit 15 - NP_BSY, Numeric processor busy

For systems using an 80286 CPU, the 80287 numeric processor must have the NPBUSY signal generated earlier to meet the processor timing specifications when the processor runs faster than the bus. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Forces an early $\overline{\text{BUSYCPU}}$ when the co-processor address is F8 through FF and IOW (Default value)

NP_BSY = 1 -
Numeric processor busy

Bit 14 - PRO_PD, Processor power down
Featured only in the WD76C10LP

When PRO_PD has been changed from a zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated and the expansion bus continues to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD76C10LP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from port 7072 (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tri-stated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a "Processor Power Good" signal. The PPG signal is sampled by bit 01 of the NMI Status Register at Port Address 9072. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power
(Default value)

PRO_PD = 1 -
Start processor power down sequence

Bit 13 - FPD, Full power down
Featured only in the WD76C10LP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and $\overline{\text{RA/ED}}$ bus are tri-stated and all inputs except $\overline{\text{RSTIN}}$, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072. All circuitry except the PMC and refresh timer logic is stopped. PMC output 7 (Full Power Down) from port 7072 is set. This enables the powering down of all chips except DRAM, WD76C10LP, WD76C20, WD76C30 and WD90C00. The WD76C20 provides PDREF (a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the $\overline{\text{REFRESH}}$ signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at port 7072 is reset, enabling the power up sequence. A $\overline{\text{CPURES}}$ and $\overline{\text{RSTIN}}$ is asserted until the PMCIN 01 "processor power good"

16

at port 9072 input is high. The tri-stated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be slower than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two, regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are eliminated. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

0 0 - Bus logic uses BCLK2 divided by 2 (Default value).

0 1 - Bus logic uses BCLK2 divided by 1.

1 0 - Bus logic uses CPUCLK divided by 2.

1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus request delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

0 0 - 1 Bus clock delay (Default value)

0 1 - .5 Bus clock delay

1 0 - No clock delay

1 1 - Reserved

Bits 07, 06 - BAK_DEL, Bus acknowledge delay

An asynchronous AT bus state machine requires a synchronization delay at the end of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

0 0 - No delay

0 1 - -.5 Bus clock delay

1 0 - -1 Bus clock delay

1 1 - +.5 Bus clock delay (Default value)

Bit 05 - WSI16, Wait state for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state (Default value)

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait state for 16 bit memory

WSM16 = 0 -
1 Bus clock wait state (Default value)

WSM16 = 1 -
2 Bus clock wait state

Bits 03, 02 - WSI8, Wait state for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state

0 1 - 3 Bus clock wait state

1 0 - 4 Bus clock wait state (Default value)

1 1 - 5 Bus clock wait state

Bits 01, 00 - WSM8, Wait state for 8 bit memory

WSM8
01 00

0 0 - 2 Bus clock wait state

0 1 - 3 Bus clock wait state

1 0 - 4 Bus clock wait state (Default value)

1 1 - 5 Bus clock wait state

5.3.2 Numeric Processor Busy (NPBUSY) Reset

Port Address 0F0 - Write only

7	6	5	4	3	2	1	0

Writing any data to this port resets the 80287 busy signal (de-asserts NPBUSY).

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1 - Write only

7	6	5	4	3	2	1	0

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port.

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	S YNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two 8237 equivalent DMA controllers. DMA controller #1 is in the I/O address space from 000 to 00F and is used for 8-bit transfers. DMA controller #2 is in the I/O space from 0C0 to 0DE and is used for 16-bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

5.4.1.1 Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a TC is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

5.4.1.2 Single Transfer Mode - 01

In single transfer mode the channel makes one transfer for each request. The word count is decremented and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000 to FFFF, a terminal count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

5.4.1.3 Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

5.4.1.4 Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tri-stated when the $\overline{MASTER}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: write, read and verify.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

5.4.2.1 Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or $\overline{MEMW}$ signals.

5.4.2.2 Write - 01

A write transfers data from an I/O device to memory.

5.4.2.3 Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority. The DMA controller #2 has priority over the DMA controller #1.

5.4.5 Extended Write

In normal timing the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008, 0D0 - Write only

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

The Command Register is reset by a reset or Master Clear Command.

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008, 0D0 - Read only

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0 TC

Bits 3-0 are reset by a reset, a Master Clear Command, or when read by a Status Read Command.

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009, 0D2 - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by a reset or a Master Clear command.

7	6	5	4	3	2	1	0
					CRQ	CH#	

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or reset by software or set by a TC if the channel is not in autoinitialize mode. All the bits are set by a reset or a Master Clear function.

5.4.11.1 Single Mask Register

Port Addresses 00A, 0D4 - Write only

7	6	5	4	3	2	1	0
					SE_ MA	CH#	

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

16

Bits 1, 0 - CH#, Channel Number Requested

CH# 1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00E, 0DC - Write only

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.11.3 Mask All Register

Port Addresses 00F, 0DE - Write only

7	6	5	4	3	2	1	0
				CH3_MA	CH2_MA	CH1_MA	CH0_MA

Bits 7-4 - Not used, state is ignored.

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00B, 0D6 - Write only

This register selects the mode and type of transfer for each channel. Refer to Sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, Sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types, and Section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_MOD		AD_DEC	AUTO	TRA_TYP		CHA# SEL	

Bits 7, 6 - TRA_MOD, Transfer mode

TRA_MOD

7 6

0 0 - Demand

0 1 - Single

1 0 - Block

1 1 - Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled

AUTO = 1
Autoinitialization is enabled

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP

3 2

0 0 - Verify

0 1 - Write

1 0 - Read

1 1 - Not used

Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL

1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00C, 0D8 - Write only

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip flop is reset, bits 7-0 are accessed," and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register. The data is ignored.

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.14 Master Clear Rgister

Port Addresses 00D, 0DA - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip Flop

All data is ignored.

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.15 DMA Mode Shadow Register

Port Address B872 - Read only

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00B (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6 (see Table 5-4).

16

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two 8259 equivalent interrupt controllers. Interrupt controller #1 is in the I/O space of 020 to 021, and interrupt controller #2 is in the I/O space of 0A0 to 0A1. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may be programmed to be level or edge sensitive. In the level mode, the interrupts occur as long as the interrupt is kept high. In the edge mode, it must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	R.T.C.
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

   Fixed

   In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

   Automatic Rotation

   In automatic rotation, the last interrupt serviced has the lowest priority.

   Specific Rotation

   In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA that causes the interrupt controller to send a vector to the CPU and set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's.

   Specific

   An EOI is issued by software for a specific interrupt.

   Non-Specific

   A non-specific EOI is issued by software. The hardware generates an EOI for the highest level active interrupt.

   Automatic

   An automatic EOI is a non-specific EOI that is caused by the second INTA.

   The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

   When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts

to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are setup by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW 4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020, 0A0 - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1.

Interrupt Controller	Address	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

Bit 3 - L_T, Level Trigger

The state of this bit is ignored. Edge triggered interrupts are always selected.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021, 0A1 - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021 - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Bits 7-3 - Not used, must be set to 0

Bit **2 - I2 H_L**, Interrupt 2 has slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

Port Addresses 0A1 - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021, 0A1 - Write only

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Special Fully Nested Mode not selected

S F N M = 1 -
Special Fully Nested Mode selected

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal EOI

AUT_EOI = 1 -
Automatic end of interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021, 0A1 - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

16

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020, 0A0 - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT 7	6	5	
0	0	0	- Clear Rotate On Automatic EOI
0	0	1	- Non-specific EOI
0	1	0	- Not used
0	1	1	- Specific EOI
1	0	0	- Select Rotate on Automatic EOI
1	0	1	- Rotate on Non-Specific EOI
1	1	0	- Set Priority
1	1	1	- Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

INT_LEV 2	1	0	
0	0	0	- Interrupt Level 0
	↕		
1	1	1	- Interrupt Level 7

5.5.3.3 OCW3

Port Address 020, 0A0 - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ ISR	

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM 6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 - No Poll Command

P_C = 1 - Poll Command

Bits 1-0 - IRR_ISR

IRR_ISR 1	0	
0	0	- Not used
0	1	- Not used
1	0	- Read Interrupt Request Register
1	1	- Read Interrupt Service Register

5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

16

5.6.1 Setup

Each counter may be set in one of five modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0 the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low, then OUT will go high.

If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

Address 9	8	7	6	5	4	3	2	1	0	Decodes	Hex
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PI0)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6
008A	DMA Channel 7
008F	Refresh

TABLE 5-9. PAGE REGISTER DECODES

Note: Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

5.8 NMI AND REAL TIME CLOCK

5.8.1 Real Time Clock Address Register

Port Address 070-07E even - Write only

There is only one RTC Address Register. All even number addresses from 070 through 07E access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1

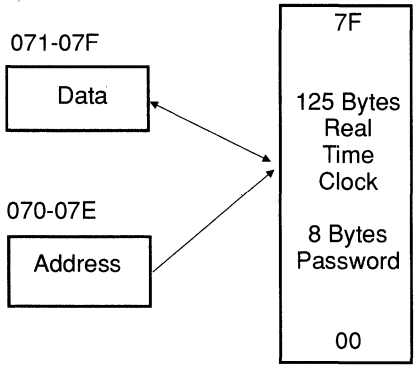
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071-07F.



5.8.2 Real Time Clock Data Register

Port Address 071-07F odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071 through 07F access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at port address 2872 (refer to Section 7.2).

7	6	5	4	3	2	1	0
Real Time Clock Data							

5.8.3 Lock Pass, Alternate A20, And Hot Reset

Port Address 092 - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at port address 2872 must be set to 0. Once LOCK_PASS is set, it can only be reset by RSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

16

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872, to automatically change state to match that of the Keyboard's A20GATE. In this mode, the ALT_A20G signal is used exclusively, and the keyboard A20GATE signal is ignored.

Bit 0 - HOT_RST, Host reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Odd numbered port addresses 061 through 06F provide access to parity error and I/O channel check of the expansion bus.

Port Address 061- 06F odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O channel check from the expansion bus (read only)

IOCK = 0 -
No I/O channel check error

IOCK = 1 -
I/O channel check error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O channel check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable parity error check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by port address register 6072, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled.

Bit 1 - ENSPK, Enable speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for timer channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA10 through RA0. During I/O cycles, RA10, RA9 and RA8 become CS2, CS1 and CS0 and, along with CS3, are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA10 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{MEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128K to 640K, 256K to 640K, and 512K to 640K.

The WD76C10 and WD76C10LP provide support for DRAM banks to be independent, two-way, or four-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size. The WD75C10, WD76C10 and WD76C10LP support non-page mode two-way interleaved memory.

16

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872 - Read and Write

15	14	13	12	11	10	09	08
PG_ CAS		CA		PG		ILV_	

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS ☆	0
CA☆	0 0
PG ☆	0
ILV	0 0
SIZE_BNK3 ☆ ☆	0 0
SIZE_BNK2 ☆ ☆	0 0
SIZE_BNK1 ☆ ☆	0 0
SIZE_BNK0 ☆ ☆	0 0

☆ Not featured in the WD75C10
☆ ☆ The WD75C10 does not support 4 Mb DRAM

Bit 15 - PG_CAS, Page mode CAS width
Not featured in the WD75C10

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache mode
Not featured in the WD75C10

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the RDYIN signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the RDYIN (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)

0 1 - Cache Mode enabled. RDYIN at pin 51 indicates discrete cache hit or miss.

1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the Discrete Cache controller.

Bit 11 - PG, Page mode
Not featured in the WD75C10

PG = 0 - Non-page mode (Default value)
Word interleaving is employed when bank interleaving is enabled by ILV.

PG = 1 - Page mode
Page mode interleaving is employed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In non-page mode (PG = 0), word interleaving is used. In Page Mode (PG = 1), page mode interleaving is used. Four way interleave is only supported in Page Mode and therefore, is not available to the WD75C10. Interleave of 64K DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size when they are interleaved together.

ILV 10 09 08

0 0 0 - No interleaving performed.
0 0 1 - Banks 0 and 1 are interleaved. Banks 2 and 3 are not interleaved. Banks 0 and 1 must be the same size.
0 1 0 - Banks 0 and 1 are not interleaved. Banks 2 and 3 are interleaved.
0 1 1 - Banks 0 and 1 are interleaved. Banks 2 and 3 are interleaved. Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.
1 0 0 - Page Mode four way interleave.

Bits 07, 06 - SIZE_BNK3, Size of bank 3

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK3
07 06

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 05, 04 - SIZE_BNK2, Size of bank 2

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK2
05 04

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 03, 02 - SIZE_BNK1, Size of bank 1

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK1
03 02

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 01, 00 - SIZE_BNK0, Size of bank 0

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK0
01 00

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872 - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 1 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 0 start address					

Port Address 5072 - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 3 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 2 start address					

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes.

RAM SIZE	PAGE SIZE	BANK SIZE
64 Kbits X 1	512 Bytes	128 KBytes
256 Kbits X 1	1024 Bytes	512 KBytes
1 Mbits X 1	2048 Bytes	2048 KBytes
4 Mbits X 1	4096 Bytes	8192 KBytes

6.2.3 Split Starting Address

Port Address 5872 - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At RSTIN
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	0 0
SPLIT_SIZE	0 0

Bit 15 - EN_BK3, Enable bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value).

EN_BK3 = 1 -
Bank 3 is enabled.

Bit 14 - EN_BK2, Enable bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value).

EN_BK2 = 1 -
Bank 2 is enabled.

Bit 13 - EN_BK1, Enable bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value).

EN_BK1 = 1 -
Bank 1 is enabled.

Bit 12 - EN_BK0, Enable bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value).

EN_BK0 = 1 -
Bank 0 is enabled.

Bits 11, 10 - DRAM_DRV, DRAM driver strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage, and manufacturing process.

DRAM_DRV
11 10

0 0 - Full strength DRAM address drive, up to 350 pF. (Default value)

0 1 - Low strength DRAM address drive, up to 100 pF.

1 0 - Medium strength DRAM address drive, up to 180 pF.

1 1 - High strength DRAM address drive, up to 260 pF.

Bits 09, 08 - SP_SIZE, Split size

The split is implemented by moving the block of memory between 0A0000 through 0FFFFF to another area. The destination area must start on a 512K boundary. If BIOS is to be shadowed, the split size must be 320K for a 64K shadow or 256K for a 128K shadow, and the RAM Shadow And Write Protect Register (Port 6072) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000 hex (640K) to 100000 hex (1024K) is available for remapping. The remapping may start at 100000 hex, providing 384K of extended memory, or may start at 0F0000 hex to allow BIOS shadowing, with 320K of extended memory. Only a single bank may be split. The bank to be split must be at least 512K or larger.

SPLIT SIZE
09 08

0 0 - No split (Default value)
0 1 - 256K split, memory moved from 0A0000 to 0DFFFF
1 0 - 320K split, memory moved from 0A0000 to 0EFFFF
1 1 - 384K split, memory moved from 0A0000 to 0FFFFF

Bits 07-02 - A24-A19, Split starting address

Bits 01, 00 - Not used, state is ignored

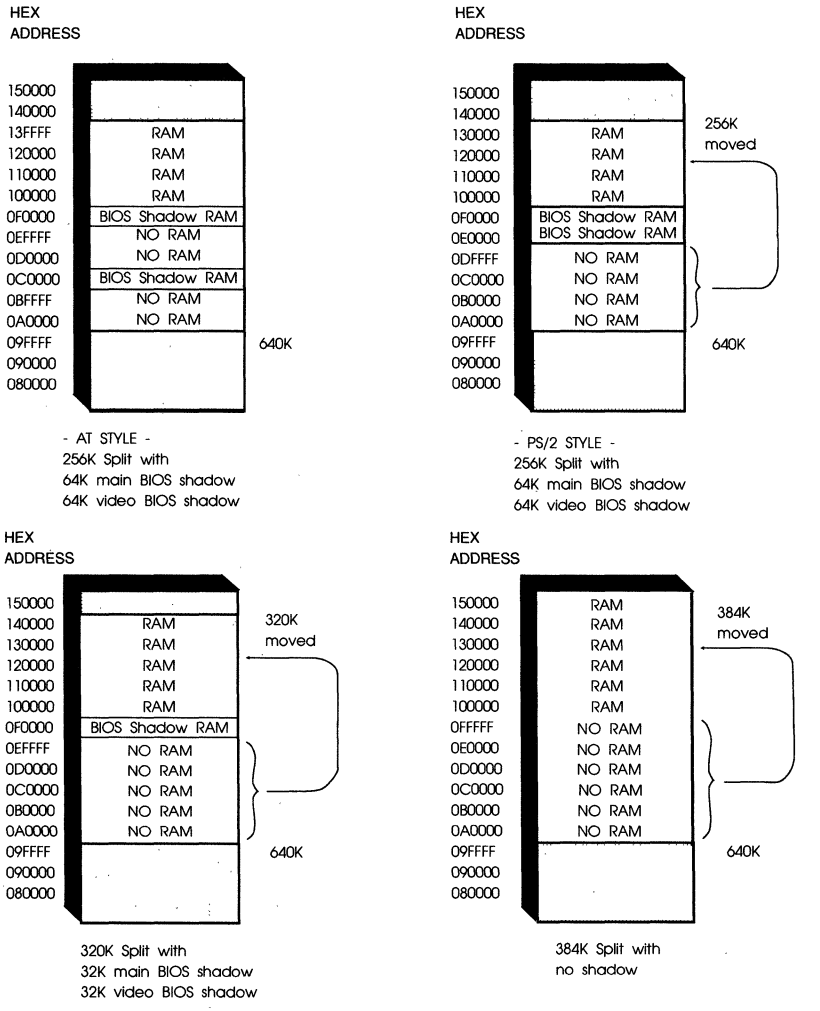


FIGURE 6-1. SPLIT SIZE

6.2.4 RAM Shadow And Write Protect

Port Address 6072 - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
0		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	0 0
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	0 0
Bit 7	0
VB_SIZ	0 0
ROM_TYP	0 0
BL_MOU	0 0

Bit 15, 14 - DIS_MEM, Disable on-board memory

DIS_MEM
15 14

0 0 - On-board memory from 128K to 640K not disabled (Default value)

0 1 - On-board memory from 512K to 640K disabled

1 0 - On-board memory from 256K to 640K disabled

1 1 - On-board memory from 128K to 640K disabled

Bit 13 - HM_WP, High memory write protect enable

This bit enables the write protection for the memory boundary established by the register at port C072.

HM_WP = 0 -
High memory write protect not enabled (Default value)

HM_WP = 1 -
High memory write protect enabled

Bit 12 - WP, Shadowed BIOS write protect enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value)

WP = 1 -
Write protect for shadowed BIOS enabled

Bit 11 - INV_PAR, Invert parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value)

INV_PAR = 1 -
Invert parity when writing to on-board DRAM

Bit 10 - PAR_DIS, Parity checking disabled

Parity checking is normally enabled or disabled by port 061. Setting PAR_DIS overrides the port 061 setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by port 061 (Default value)

PAR_DIS = 1 -
Parity checking disabled

Bits 09, 08 - SHD, Shadow BIOS

ROM at FE0000 - FFFFFF, the top of 16 MB address space is never shadowed.

Option SHD 11 should be used when video and system BIOS combined equal more than 64K.

64K of system BIOS at 0F0000 - 0FFFFF, and up to 64K of video BIOS at 0C0000 - 0CFFFF, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000 - 0FFFFF. When SHD is set to 11, the video BIOS appears at 0C0000 - 0CFFFF rather than 0E0000 - 0EFFFF.

The video shadow size at 0C0000 - 0CFFFF is determined by VB_SIZ, the video BIOS size field.

16

SHD
09 08

- 0 0 - No BIOS shadowing, allows 384K remap (Default value)
- 0 1 - 64K system BIOS shadow, 0F0000-0FFFFF, allows 320K remap
- 1 0 - 128K system BIOS shadow, 0E0000-0FFFFF, allows 256K remap
- 1 1 - 64K system BIOS shadow, 0F0000-0FFFFF and video BIOS shadow, allows 256K remap

Bits 07 - Reserved for future use, must be set to 0

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS size

VB_SIZ
05 04

- 0 0 - 16K video BIOS (Default value)
- 0 1 - 32K video BIOS
- 1 0 - 48K video BIOS
- 1 1 - 64K video BIOS

Bits 03, 02 - ROM_TYP, ROM type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000 - 0FFFFF or FE0000 - FFFFFF.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000 - 0FFFFF or FF0000 - FFFFFF.

For ROM type 10, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000 - 0FFFFF, FF0000 - FFFFFF or 0C0000 - 0CXFFF where X is determined by VB_SIZ. This allows either a 128K BIOS, with a 64K system BIOS and a 64K video BIOS, or a 64K BIOS, with a 32K system BIOS and a 32K video BIOS. The 32K video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000 - CX000 and F0000 - FX000. A 64K EPROM needs addresses SA15 - SA0. A128K EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128K system BIOS, located at E0000 - FFFFF.
- 0 1 - 64K system BIOS, located at F0000 - FFFFF (Default value).
- 1 0 - 64K or 128K shared BIOS. System BIOS located at F0000 - FFFFF, video BIOS is located at C0000 - CX000.

Bits 01, 00 - BL_MOU, Back Light Mouse Control

Enabling the Back Light Mouse Control increases the CPU speed for one second if the Autofast is on. The AUT_FST bit is located at port 1072 bit 11.

BL_MOU
01 00

- 0 0 - No mouse control (Default value)
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

6.2.5 High Memory Write Protect Boundary

Port Address C072 - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At RSTIN
A24 - A17	00

Bits 07-00 - A24-A17, Boundary address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at port 6072. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at port 4072, the memory timing mode changes immediately, so the code that programs this register should be in ROM and not shadowed in RAM.

For non-page mode DRAM operations, the row address hold time is fixed at one CPUCLK.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072 - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_ RAW	NP_WR_ DEL		NP_RD_ DEL	

07	06	05	04	03	02	01	00
	NP_RAS_ HLD		NP_CAS			NP_WS	

Signal Name	Default At RSTIN
NP_MODE	0 0
NP_RAW	0
NP_WR_DEL	0 0
NP_RD_DEL	0 0
NP_RAS_HLD	0 0
NP_CAS	0 0 0
NP_WS	0 0

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-page RAS delay

The start of RAS is normally measured from the middle of $\overline{S0}$ or $\overline{S1}$. When operating in the 80386SX mode, the WD76C10 and WD76C10LP generate the $\overline{S0}$ and $\overline{S1}$ internally (the WD75C10 operates only with an 80286). The timing specifications in section 10 show the relationship of ADS to the internal $\overline{S0}$ and $\overline{S1}$ when in the 80386SX mode.

For 12.5 MHz 80286 operation, the RAS can be started from the status signals $\overline{S0}$ and $\overline{S1}$. This allows interleaved zero wait state operation from 120 ns. DRAM.

For 16 MHz 80386SX operation, the RAS can be started from the translated 80286 status signals. This allows interleaved zero wait state operation in pipeline mode from 100 ns. DRAM.

These two types of operation are selected by setting NP_MODE = 11.

For non-page mode operation with an 80286 at 16 MHz or 80386SX at 20 MHz, NP_MODE should be set to 00.

Discrete cache mode is not supported in non-page mode memory operation.

See Table 6-1 for more information regarding non-page mode operation.

RAS is delayed until the middle of the first command cycle when the non-page mode interleave is selected and back-to-back memory accesses are made to the same bank of DRAM.

This guarantees a RAS precharge time of three CPUCLK clocks.

NP_MODE
14 13

0 0 - RAS starts with 0 clock delay

1 1 - RAS starts from $\overline{S0}$ or $\overline{S1}$

Bit 12 - NP_RAW, Non-page disable RAW

NP_RAW = 0 -
Read after write cycles have additional wait states. See Table 6-2 for situations where wait states are added.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bits 11, 10 - NP_WR_DEL, Non-page write cycle delay

If RAS has been programmed by NP_RAS_DEL (bits 14, 13 = 11) to start from $\overline{S0}$ or $\overline{S1}$ active, the CAS delay is referenced to the middle of $\overline{S0}$ or $\overline{S1}$.

If the NP_WR_DEL is set to 01 or 10, the write CAS pulse width is shortened by .5 clock from the value programmed by the NP_CAS field (bits 4, 3 and 2).

NP_WR_DEL
11 10

0 0 - 1 CPUCLK (non-page)

0 1 - 1.5 CPUCLK (non-page)

1 0 - 2.0 CPUCLK (non-page)

1 1 - 2.5 CPUCLK (non-page)

Bits 09, 08 - NP_RD_DEL, Non-page read cycle delay

If RAS has been programmed by NP_RAS_DEL (bits 14, 13 = 11) to start from $\overline{S0}$ or $\overline{S1}$ active, the CAS delay is referenced to the middle of $\overline{S0}$ or $\overline{S1}$.

If the NP_RD_DEL is set to 01 or 10, the read CAS pulse width is shortened by .5 clock from the value programmed by the NP_CAS field (bits 4, 3, and 2).

NP_RD_DEL
11 10

0 0 - 1 CPUCLK (non-page)
0 1 - 1.5 CPUCLK (non-page)
1 0 - 2.0 CPUCLK (non-page)
1 1 - 2.5 CPUCLK (non-page)

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS hold time

The CAS to RAS hold time is reduced by half a clock if the RAS to CAS delay is 1.5 or 2.5 clocks.

For example:

If NP_RAS_HLD is set for RAS active until 1.5 clocks after CAS and NP_RD_DEL is set for a 2.0 CPUCLK, the CAS to RAS hold time is 1.0 CPUCLK.

If NP_RAS_HLD is set for RAS active until 1.5 clocks after CAS and NP_RD_DEL is set for 1.5 or 2.5 CPUCLKs, the CAS to RAS hold time is reduced to .5 CPUCLKs.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS
0 1 - RAS active until 1.5 clock after CAS
1 0 - RAS active until 2.0 clock after CAS
1 1 - RAS active until 2.5 clock after CAS

Bits 04-02 - NP_CAS, Non-page CAS pulse width

NP_CAS
04 03 02

0 0 0 - 1 CPUCLK (non-page)
0 0 1 - 1.5 CPUCLK (non-page)
0 1 0 - 2.0 CPUCLK (non-page)
0 1 1 - 2.5 CPUCLK (non-page)
1 0 0 - 3.0 CPUCLK (non-page)
1 0 1 - 3.5 CPUCLK (non-page)
1 1 0 - 4.0 CPUCLK (non-page)
1 1 1 - 4.5 CPUCLK (non-page)

Bits 01, 00 - NP_WS, Non-page wait states

NP_WS establishes the minimum duration of a DRAM cycle. If a read after write miss EMS access or interleave miss cycle occurs, an additional wait state is generated.

The System Controller holds the DRAM data until latched by the processor. If CAS ends at the command cycle boundary, to prevent data bus contention, an additional wait state should be programmed by NP_WS. Contention on the data bus can occur on a write cycle immediately following a read cycle, when the processor drives the data bus before the DRAM can tri-state its outputs.

NP_WS
01 00

0 0 - 0 Wait states
0 1 - 1 Wait states
1 0 - 2 Wait states
1 1 - 3 Wait states

16

NON-PAGE MODE	PROCESSOR SPEED	MIN W.S.	RAS START	ADDITIONAL WAIT STATES RD	WR	
00	16-20 MHz 80286, 20-25 MHz 80386SX	0	Tsm	No add'l	No add'l	Non-EMS, not interleave wait, not read after write.
			Tsm+1	+1	NA	Read after write, Non-EMS.
			Tsm+2	+2	+1	EMS or Interleave wait.
			Tsm+4	+3	NA	Simultaneous read after write and interleave wait.
11	8-12 MHz 80286, 16 MHz 80386SX	0	By $\overline{S0}$ $\overline{S1}$	No add'l	No add'l	Non-EMS, not interleave wait, not read after write.
			Tsm+1	+1	NA	Read after write, Non-EMS.
			Tsm+2	+2	+1	EMS or Interleave wait.
			Tsm+4	+3	NA	Simultaneous read after write and interleave wait.

NOTE: NA = Not Applicable
Tsm = middle of status cycle, Tsm+1 = 1 CPUCLK after Tsm = end of status cycle
Tsm+2 = 2 CPUCLKs after Tsm, Tsm+4 = 4 CPUCLKs after Tsm.
Non-Page Mode column represents the NP_MODE setting in Non Page Mode Register at port 4072.

TABLE 6-1. NON-PAGE MODE WAIT STATES

6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access ☆	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access ☆	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access ☆	1
	Write page miss	3
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	2
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access ☆	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit ☆	1
	Read page first access ☆	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access ☆	1
	Write page miss	3
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	2
	Read cache miss, page miss	4

TABLE 6-2. PAGE MODE WAIT STATES

☆ Equal Bank sizes, non-EMS cycle

16

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64K, 256K, 1 Mb or 4 Mb SIMM memory modules.

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
64K NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
64K 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
64K 4-WAY, 256K 2-WAY INTERLEAVE OR 1 Mb NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
256K 4-WAY, 1 Mb 2-WAY INTERLEAVE OR 4 Mb NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 Mb 4-WAY OR 4 Mb 2-WAY INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Mb 4-WAY INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS											
ROW	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	ALL	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE NON-INTERLEAVE ADDRESS CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	ALL	A11	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE 2-WAY INTERLEAVE ADDRESS CONFIGURATION

16

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872 - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	0 0
EMS_EN	0 0
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS pointer

The INC bit controls whether the EMS Pointer at port E072 is to be incremented after each read or write of the EMS Page Register at port E872.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper page frame location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000 (Default value)

0 1 - Upper page frame starts at C8000

1 0 - Upper page frame starts at CC000

1 1 - Upper page frame starts at D0000

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming

1 0 - Enable upper page frame assignments

1 1 - Enable upper and lower page frame assignments

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable lower boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17,
LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128K below the actual start address. For example, to start EMS at the 1 Meg boundary, this field should be set to 07H (000 0111) binary).

6.4.2 EMS Page Register Pointer

Port Address E072 - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
0	0	POINTER					

Signal Name	Default At RSTIN
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in port 6872, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at port E872. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF

EMS registers 32 through 39 can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See port E872 description.

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 are enabled or disabled as a block. If the EMS_EN field of port 6872 is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See port E872 description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872 - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
P11-P00	0

There are 40 EMS Page Registers accessible through port E872. Only EMS registers 32 through 39 are initialized to zero, EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at port E072 provides the offset location for port E872.

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at port 6872. When EMS_EN equals 11, the EN bit in this register is treated as a one.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MB of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16K, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128K of memory, and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MB, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOREADY to make the transfer.

7.0 PORT CHIP SELECT AND WD76C10 REFRESH CONTROL

This section describes refresh control logic peculiar to the WD76C10LP, and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real Time Clock bus location
- Access to the CMOS RAM password

Table 7-1 identifies the ports, their Chip Select number, I/O address, and function.

7.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072 - Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF ☆	0
V_REF ☆	0
CBR_REF ☆	0
CBR_SR	0
SCSI	0
PAR	0 0
PAR_L	0
SER_A	0 0 0
SER_AL	0
SER_B	0 0 0
SER_BL	0

☆ Featured only in the WD76C10LP

Bit 15 - M_REF, Memory refresh power down mode
Featured only in the WD76C10LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at port 1872, and M_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value)

M_REF = 1 -
Slow refresh main on-board memory

Bit 14 - V_REF, Video refresh power down mode
Featured only in the WD76C10LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at port 1872, and V_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS before RAS refresh for on-board DRAM
Featured only in the WD76C10LP

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS before RAS self refresh

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface chip select

The SCSI is selected by chip select number 12. See Table 7-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353X

Bits 10, 09 - PAR, parallel port chip select

The parallel port is selected by chip select number 0F and may be located at I/O address 278 through 27B, 378 through 37F, or 3BC through 3BF. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 7-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BC - 3BF

1 0 - PAR chip select at I/O port 378 - 37F

1 1 - PAR chip select at I/O port 278 - 27F

Bit 08 - PAR_L, parallel port bus location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, serial port A chip select

The serial port A is selected by chip select number 0E and may be located at I/O address 2E8 through 2EF, 2F8 through 2FF, 3E8 through 3EF or 3F8 through 3FF. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8 - 3FF

0 1 0 - Serial port A chip select at I/O port 2F8 - 2FF

0 1 1 - Serial port A chip select at I/O port 3E8 - 3EF

1 0 0 - Serial port A chip select at I/O port 2E8 - 2EF

Bit 04 - SER_AL, serial A port bus location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B serial port B chip select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8 through 2EF, 2F8 through 2FF, 3E8 through 3EF or 3F8 through 3FF. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

16

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8 - 3FF

0 1 0 - Serial port B chip select at I/O port 2F8 - 2FF

0 1 1 - Serial port B chip select at I/O port 3E8 - 3EF

1 0 0 - Serial port B chip select at I/O port 2E8 - 2EF

Bit 00 - SER_BL, serial B port bus location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus

SER_BL = 1 -
Serial port B is located on the expansion data bus

7.2 RTC, PVGA, 80287 TIMING, DISK CHIP SELECTS

Port Address 2872 - Read and Write

15	14	13	12	11	10	09	08
RTC_L	FST_VGA	FST_SCSI	EN_PCS	U_MSK	L_MSK		

07	06	05	04	03	02	01	00
PRG_L	HS_HD		P/S	HS_287	LK_PSW	DS_HD	DS FLP

Signal Name	Default At RSTIN
RTC_L ☆	0
FST_VGA ☆	0
FST_SCSI	0
EN_PCS ☆	0
U_MSK	0 0
LMSK	0 0
PRG_L	0
HS_HD	0 0 0
P/S	0 0 0
HS_287	0
LK_PSW	0
DS_HD	0
DS_FLP	0

☆ Featured only in the WD76C10 AND WD76C10LP

Bits 12 through 07 and port location 3072 control the use and location of the Programmable Chip Select.

Bit 15 - RTC_L, Real Time Clock

The Real Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real Time Clock is on the expansion data bus.

Bit 14 - FST_VGA, Fast VGA video

The performance of Paradise PVGA display controllers may be enhanced by terminating video access earlier than normal. This feature should only be used with Western Digital Imaging/Paradise PVGA1A and PVGA1B devices. I/O cycles to ports 3C0 - 3CF are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
Early PVGA wait state generation

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 is enhanced by perfroming eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS, Enable programmable chip select

The programmable chip select logic is selected with chip select 11 and may be disabled or enabled. See Table 7-1.

EN_PCS = 0 -
Disable programmable chip select. (Default value)

EN_PCS = 1 -
Enable programmable chip select

Bit 11 - U_MSK, Upper address bits masked

U_MSK determines whether the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at port 3072.

U_MSK = 0 -
A15 through A10 are ignored (Default value).

U_MSK = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK, Lower address bits masked

L_MSK determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at port 3072.

L_MSK
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value)

0 0 1 - A00 is ignored

0 1 0 - A00, A01 are ignored

0 1 1 - A00, A01, A02 are ignored

1 0 0 - A00, A01, A02, A03 are ignored

Bit 07 - PRG_L, Programmable chip select bus location

PRG_L = 0 -
Programmable chip select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable chip select is on the expansion bus.

Bit 06 - HS_HD, High speed hard disk data transfer rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with BALE (pin 79) suppressed, and the expansion bus addresses remain fixed at the hard disk data I/O port address.

HS_HD = 0 -
Compatible bus timing enabled (Default value)

HS_HD = 1 -
High speed hard disk accesses enabled

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary or secondary disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 7-1, chip select numbers 08 through 0B.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value)

P/S = 1 -
Secondary hard disk and Floppy address selected

Bit 03 - HS_287, Co-processor 80287 high speed timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_286 results in 16 bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value)

HS_287 = 1 -
Fast 80287 timing

Bit 02 - LK_PSW, Prevent locking password

Port 092 bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092 bit 3, Lock_Pass can be set (Default value)

LK_PSW = 1 -
Port 092 bit 3, Lock_Pass can not be set

Bit 01 - DS_HD, Hard disk chip select 0C, 0D

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy disk chip select 08, 09, 0A, 0B

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

7.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072 - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

7.4 CACHE FLUSH

Port Address F872 - Write only

15	14	13	12	11	10	09	08
X	X	X	X	X	X	X	X

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

7.5 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 7-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value

PORT	I/O ADDRESS	CS #	FUNCTION
ROM Chip Select	N/A	00	Chip Select For BIOS ROM
Keyboard ControL	060 - 06E Even	01	Chip Select For 8042
80287	00E0 - 00FF	02	Chip Select For Numeric Processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real Time Clock	070	05	RTC ALE
Real Time Clock	071	06	RTC Write Strobe
Real Time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary Address Secondary Address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary Address Secondary Address
Floppy Control Chip Select	3F7 377	0A	Primary Address Secondary Address (Floppy Enabled, HD Disabled)
Floppy And HD Control Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address

TABLE 7-1. I/O ADDRESS AND CHIP SELECT ASSIGNMENTS

16

PORT	I/O ADDRESS	CS # ②	FUNCTION
Hard Disk Chip Select	3F6 3F7 ① 376 377 ①	OD	Primary Address, IDE Mode Only Secondary Address, IDE Mode Only
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ②	
Parallel Port 0 Chip Select	278 - 27B 378 - 37F 3BC - 3BF	0F	
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ②	
Program Chip Select	PROG	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Reserved		1E	Reserved
Reserved		1F	Reserved

① IDE Hard disk enabled, floppy disabled

② The CS # (Chip Select number) is the decoded value of CS4 - CS0. If the programmed chip select corresponds to any other decode, the programmed chip select is suppressed. If serial port A and B are programmed for the same address, serial port B chip select is suppressed.

TABLE 7-1. I/O PORT ADDRESS CHIP SELECT ASSIGNMENTS cont.

8.0 POWER MANAGEMENT CONTROL

The WD75C10 and WD76C10 support only the PMC inputs and do not support any of the PMC outputs or PMC interrupt functions. The WD76C10LP supports all PMC input, output and interrupt functions.

The processor power down mode is initiated by writing to the PMC control registers located at ports 7072 and 7872. The CPURES signal is asserted, then tri-stated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control register is used to control the power converter from the processor. The WD76C10LP holds CPUCLK, READY, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the power up mode. The power up mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change resulting in an unmasked NMI to port 9072. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, READY, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT373 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD76C10LP's internal registers by way of the PMC logic. The keyboard processor starts a local access by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at port 8872 (see Figure 5-1 and Table 8-2). The WD76C10LP arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD76C10LP asserts LCL_ACK (PMC output 3 from port 7072) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD76C10LP on the data bus and drops the LCL_REQ. The WD76C10LP responds by de-asserting LCL_ACK.

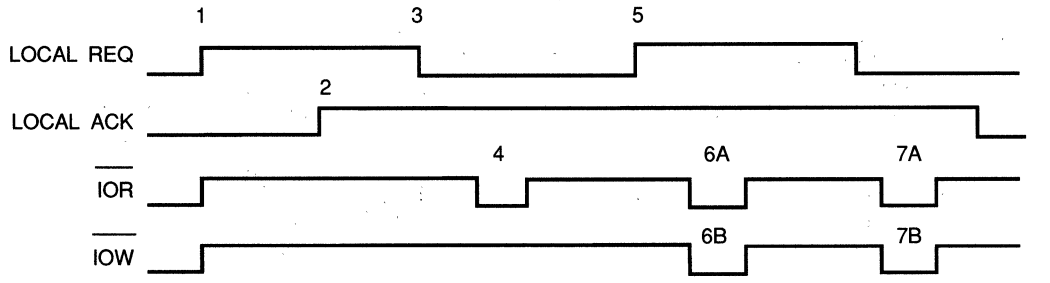
If the opcode specified a register write, data high (DEN1, D15 through D00) and data low (DEN0, D15 through D00) bytes are passed to the WD76C10LP. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD76C10LP to the keyboard processor.

All special operation registers within the WD76C10LP may be accessed in this manner without first unlocking the register. See Section 2.8.2, port address F073, for lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 8-1 shows the handshake procedure, followed by the keyboard controller and the WD76C10LP.

Figures 8-2 and 8-3 represents the power down and power up sequence and control.

16



1 8042 Requests local data transfer

2 WD76C10LP returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD76C10LP reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD76C10LP Reads high byte

7A WD76C10LP Read low byte, writes to internal register

FOR READ CYCLE OF WD76C10LP INTERNAL REGISTER:

6B WD76C10LP Writes high byte to 8042

7B WD76C10LP writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	RSV

DIR = 1 - Read register (generates IOW to 8082)

DIR = 0 - Write register (generates IOR to 8082)

FIGURE 8-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

8.1 PMC OUTPUT CONTROL REGISTERS

PMC OUTPUT CONTROL 7:0

Port Address 7072 - Bits 07-00 are read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Featured only in the WD76C10LP

PMC OUTPUT CONTROL 15:08

Port Address 7872 - Bits 07-00 are read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

PMC NO.	PMC OUTPUT SIGNAL PORT 7072	PMC NO.	OUTPUT SIGNAL PORT 7872
0	CPU Clock driver enable	8	User defined
1	LCD Enable	9	User defined
2	Backlight enabled	A	User defined
3	LCL_ACK	B	User defined
4	LCL_ATN	C	User defined
5	Processor power down	D	User defined
6	Gate A20	E	User defined
7	Full power down	F	User defined

TABLE 8-1. PMC OUTPUT SIGNALS

16

8.2 PMC TIMERS

Port Address 8072 - Read and Write

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default At RSTIN
BL_TIMEOUT ☆	0 0 hex
LCD_TIMEOUT ☆	0 0 hex

☆ Featured only in the WD76C10LP

When no keyboard interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072 (see Table 8-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a keyboard interrupt. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 16 seconds.

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00 hex - Backlight always disabled
01 hex - Enabled for 5 seconds
02 hex - Enabled for 10 seconds

Through

FE hex - enabled for 254 X 5 seconds
FF hex - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00 hex - LCD always disabled
01 hex - Enabled for 5 seconds
02 hex - Enabled for 10 seconds

Through

FE hex - enabled for 254 X 5 seconds
FF hex - LCD enabled

8.3 PMC INPUTS

Port Address 8872 - Read and Write

15	14	13	12	11	10	09	08
PMC_UPD	EN_LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD ☆☆	0
EN_LCL ☆	0
AF7-AF2 ☆	0
IN7-IN0	NA

☆ Featured only in the WD76C10LP

☆☆ Not Featured in the WD75C10

Bit 15 - PMC_UPD, Enable PMC update
Not featured in the WD75C10

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (port address 7072) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

Bit 14 - EN_LCL, Enable local request
Featured only in the WD76C10LP

EN_LCL enables the PMCIN 2 to initiate a local access of the WD76C10LP internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ

Bits 13-08 - AF7-AF2, ATN (attention flags)
Featured only in the WD76C10LP

Transitions of certain PMC inputs (IN7-0 of this register) generate an ATN to the keyboard controller and set the PMC interrupt flags at port 9072. A PMC interrupt flag is cleared by writing a 0 to the particular IF7-IF2 bit in port 9072. Writing a 1 does not set the interrupt flag. The corresponding PMC input (IN7-0) cannot be changed until the interrupt flag at port 9072 is cleared. The interrupt enables (EI7-EI2) are controlled by port C872. AF7-AF2 operate independently from EA7-EA2 in port C872.

AF7-AF2 = 0 -
A PMC ATN is not generated

AF7-AF2 = 1 -
A PMC ATN is generated

Bits 07-00 - IN7-IN0, PMC inputs 7-0

The state of IN7 through IN0 are available to all three System Controllers. In the WD76C10LP, the individual IN7 - IN0 bits are locked when an interrupt is generated and can not be changed until the corresponding interrupt enable (EI7 - EI2) in port C872 is reset (see Table 8-2).

16

8.4 PMC INTERRUPT ENABLES

Port Address C872 - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
Interrupt Enable							

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
Attention Enable							

Signal Name	Default At RSTIN
EI7-EI2 ☆	0-0
EA7-EA2 ☆	0-0

☆ Featured only in the WD76C10LP

Bits 15-10 - EI7-EI2, Interrupt enable 7 through 2

EI7 through EI2 enable the generation of an NMI when the corresponding PMC input in port 8872 changes state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Interrupts not enabled

EI7-EI2 = 1 -
Interrupts are enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Attention enable

EA7 through EA2 enable the generation of an ATN by the corresponding IN_7 through IN_2. ATN is the attention signal to the keyboard controller.

EA7-EA2 = 0 -
ATN is not enabled

EA7-EA2 = 1 -
ATN is enabled

Bits 01, 00 - Not used, state is ignored

PMC INPUT NUMBER ①	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER ②
00	$\overline{\text{TURBO}}$		
01	PROC_PWR_ GOOD		
02	LCL_REQ or User Defined	Transition	IF2
03	User Defined	Transition	IF3
04	User Defined	Transition	IF4
05	User Defined	Transition	IF5
06	User Defined	Transition	IF6
07	User Defined	Active Edge	IF7

① Port Address 8872, section 8.3

② Port Address 9072, section 8.5

TABLE 8-2. PMCIN INPUTS

8.5 NMI STATUS

Port Address 9072 - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
		Interrupt Flags					

Signal Name	Default At RSTIN
IF7-IF2 ☆	0-0

☆ Featured only in the WD76C10LP

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Interrupt flags 7 through 2
Featured only in the WD76C10LP

An NMI is generated and the PMC interrupt flags (IF7-IF2) are set by transitions of the PMC inputs listed in Table 8-2. IF7 through IF2 may be reset by writing a 0 to the corresponding EI7 through EI2 or EA7 through EA2. If both EI and EA are set, both must be reset to clear the interrupt flag. The corresponding PMC input cannot be changed until the interrupt flag is reset. EI and EA are located at port C872.

Bits 01, 00 - Not used, must be 0

8.6 Shadow Register

Port Address D072 - Read only

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN

This register is particulary usefull in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

16

8.7 SAVE AND RESUME

When the WD76C10LP is in the Save And Resume mode, the power supply current for the WD76C10LP is typically less than 500 µA.

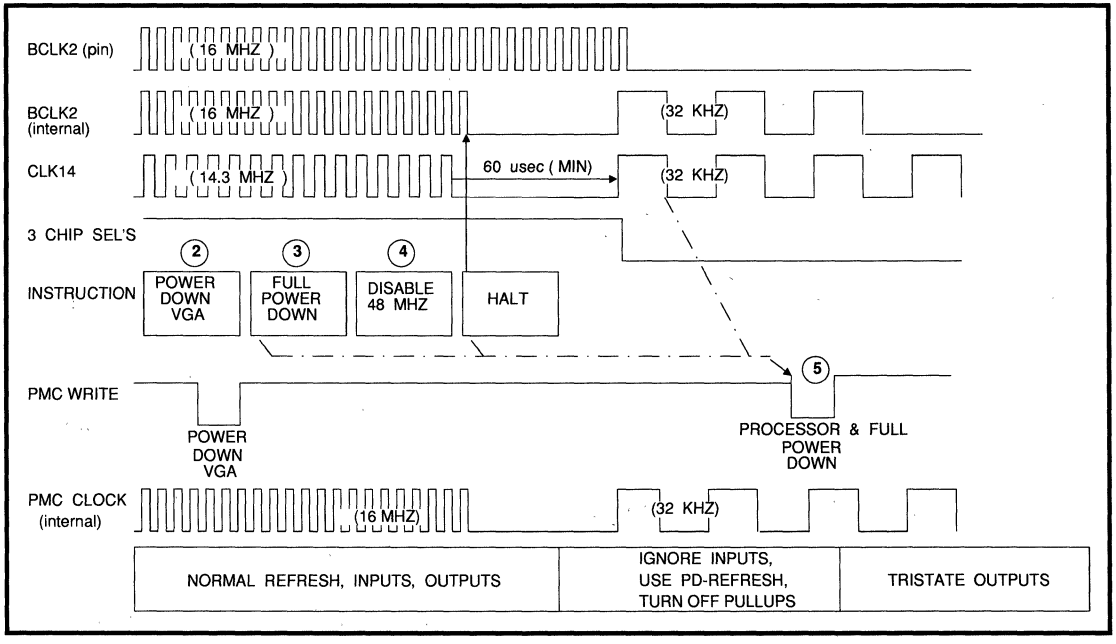


FIGURE 8-2. POWER DOWN

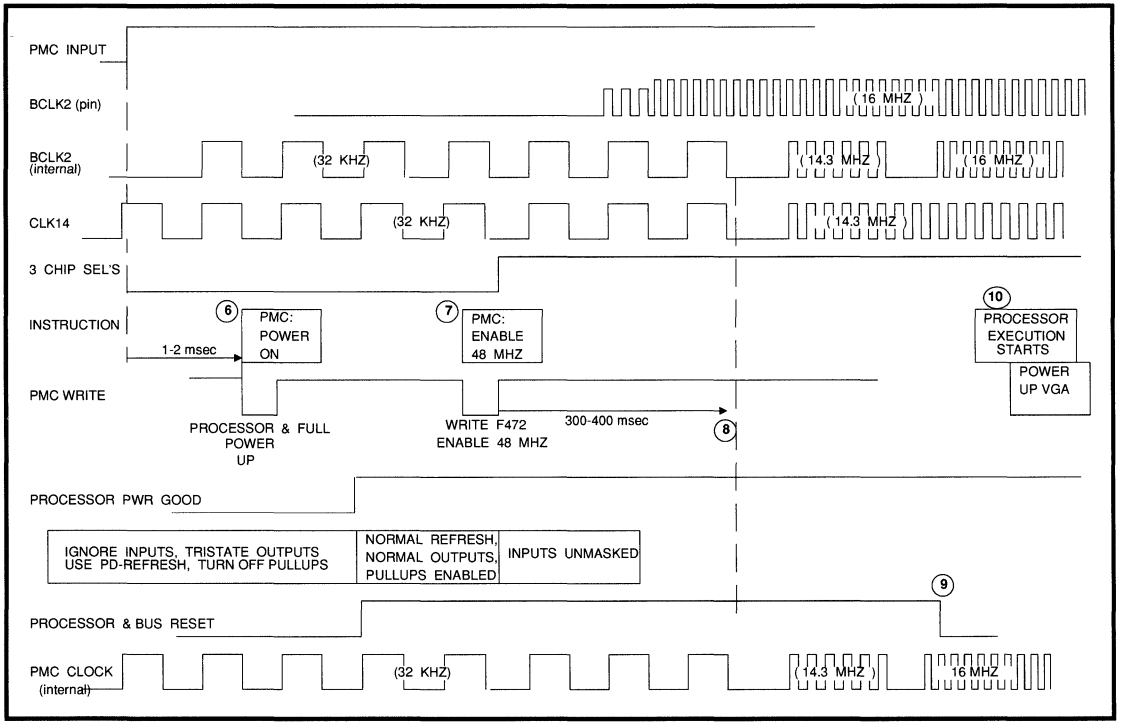


FIGURE 8-3. POWER UP

16

9.0 DIAGNOSTIC MODE

Simultaneously asserting $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$, while $\overline{\text{RSTIN}}$ is asserted, causes all output pins to become tri-stated. The outputs remain tri-stated if $\overline{\text{RSTIN}}$ is de-asserted while $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ are asserted. The outputs become active drivers when $\overline{\text{RSTIN}}$ is asserted and any of the $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$ are not asserted. This all output tri-state mode allows an in-circuit board tester to drive the System Controller's output pins.

9.1 DIAGNOSTIC REGISTER

Port Address 9872 - Read and Write

15	14	13	12	11	10	09	08
VER			CLK_ TST	REF_ MAS	ALT_ A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default At RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
ALT_A20	0
CLK_SW	0
SX	X
DS	0
DIAG	00000

Bits 15, 14 ,13 - VER, version number

The initial version number is 000 and is incremented with every mask change.

Version
- 000 Initial
- 010 Early production
- 011 Production

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, bus master refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - ALT_A20, Alternate Gate A20

Normally, the Alternate Gate A20 signal from port 092 is OR'ed with the 8042 Gate A20.

When the ALT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of port 092 is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 is replaced by that of ALT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading port 7072 (see Table 8-1). The state of PMC output 6 changes immediately if port 092 is used, and changes at the next refresh if the keyboard A20 gate function is used.

ALT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

ALT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, clock switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, diagnostic signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, diagnostic function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 9-1. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	"
00010	Reserved	10010	"
00011	"	10011	"
00100	"	10100	"
00101	"	10101	"
00110	"	10110	"
00111	"	10111	"
01000	"	11000	"
01001	"	11001	"
01010	"	11010	"
01011	"	11011	"
01100	"	11100	"
01101	"	11101	"
01110	"	11110	"
01111	"	11111	"

TABLE 9-1. DIAGNOSTIC TESTS

16

9.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072 - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default At RSTIN
LAT	0
DL	0
DELAY	NA

Bit 07 - LAT, Latch output strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay counter value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

10.0 ELECTRICAL SPECIFICATIONS

10.1 MAXIMUM RATINGS

Supply Voltage (VCC) with respect to VSS (ground) . . . . Volts

Voltage on any pin with respect to VSS (ground) . . . . . Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -C (-F) to C (F)

Power Dissipation . . . . . mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

10.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)

Vcc = +5V ±.5V (10%) for WD76C10LP

Vcc = +5V ±.25V (5%) for WD75C10 and WD76C10

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tri-state And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD76C10LP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 10-1. DC OPERATING CHARACTERISTICS

16

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, S0, S1, BHE, M/IO, HLDA, PEACK, NPBUSY, NPERR, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-12	-50	µA	Not save and resume mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage		.4	V	IOUT = 2 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage		.4	V	IOUT = 4 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:
$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:
$\overline{REFRESH}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

16

10.3 AC OPERATING CHARACTERISTICS

Table 10-2 lists the timing categories and their Figure and Table numbers.

FIGURE NUMBER	TABLE NUMBER	TITLE
10-1	10-3	Page Mode

TABLE 10-2. TIMING FIGURE/TABLE NUMBERS

50 pF	MXCTL2-0, DACKEN, SPKR, CPUCLK, $\overline{\text{READY}}$, CPURES, HOLD, INTRQ, NMI, W/$\overline{\text{R}}$, DT/$\overline{\text{R}}$, $\overline{\text{DENO}}$, $\overline{\text{DEN1}}$, $\overline{\text{CSEN}}$, ALE, $\overline{\text{BUSYCPU}}$, SDT/$\overline{\text{R}}$, $\overline{\text{SDEN}}$, LOMEG, $\overline{\text{BHE}}$
100 pF	D15-D0, DPH, DPL, A23-A0, $\overline{\text{CASH3}}$-$\overline{\text{CASH0}}$, $\overline{\text{CASL3}}$-$\overline{\text{CASL0}}$
200 pF	$\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, AEN, SYSCLK, $\overline{\text{REFRESH}}$, BALE, LA20, SA0, $\overline{\text{RAS3}}$-$\overline{\text{RAS0}}$
350 pF	RA10-RA8, RA7/ED7-RA0/ED0

TABLE 10-3. LOAD CAPACITANCE

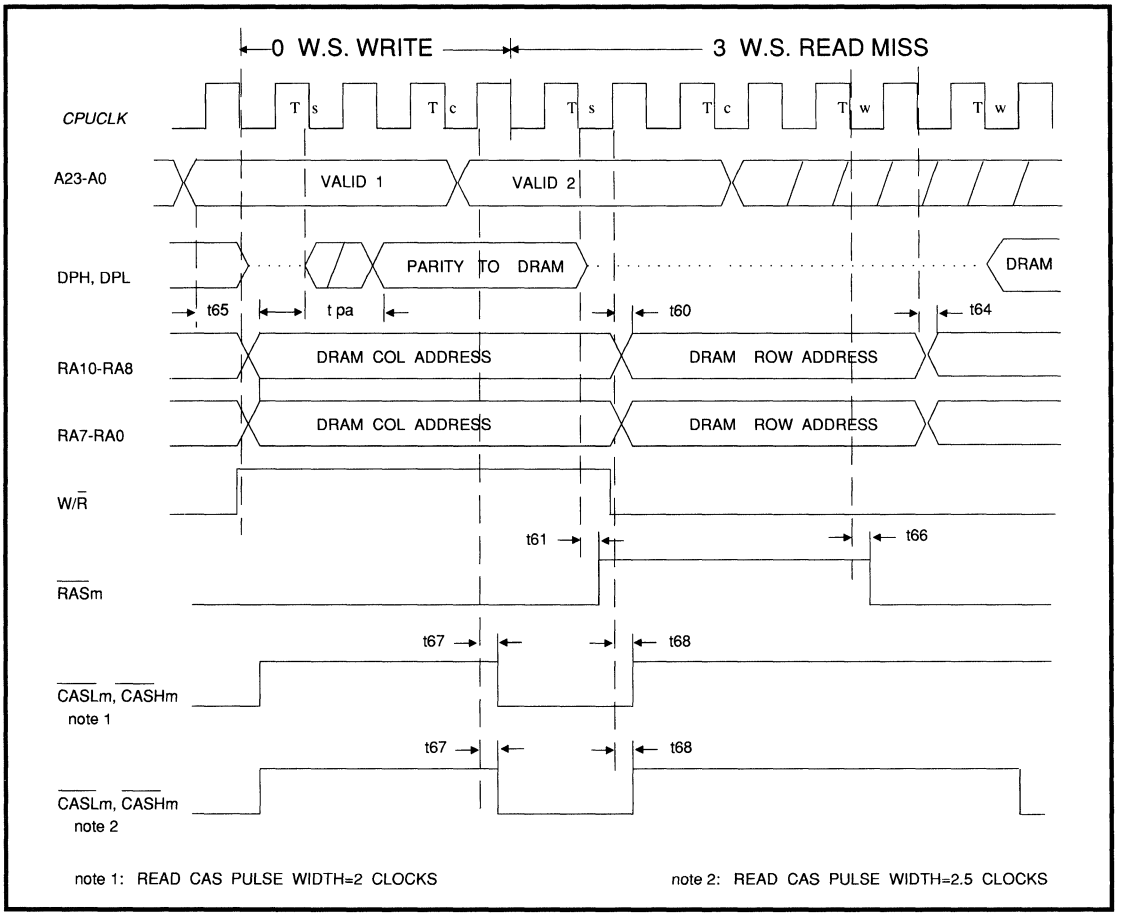


FIGURE 10-1. PAGE MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
tWR	Clock, $\overline{S0}$, or $\overline{S1}$ to W/$\overline{R}$		20	ns	Load 50 pF
t67, t68	Clock to $\overline{CAS}$		20	ns	Load 100 pF
t61, t66	Clock to $\overline{RAS}$		25	ns	Load 200 pF
t65	Column Address from A23-A0		35	ns	Load 350 pF
tPA	Parity Data from D15-D0		25	ns	Load 100 pF
t60	Clock to Row Address		35	ns	Load 350 pF
t64	Clock to Column Address		35	ns	Load 350 pF

TABLE 10-4. PAGE MODE TIMING

16

11.0 PACKAGE DIMENSIONS

Figure 11-1. Illustrates the 132-Pin PQFP package showing the dimensions in inches.

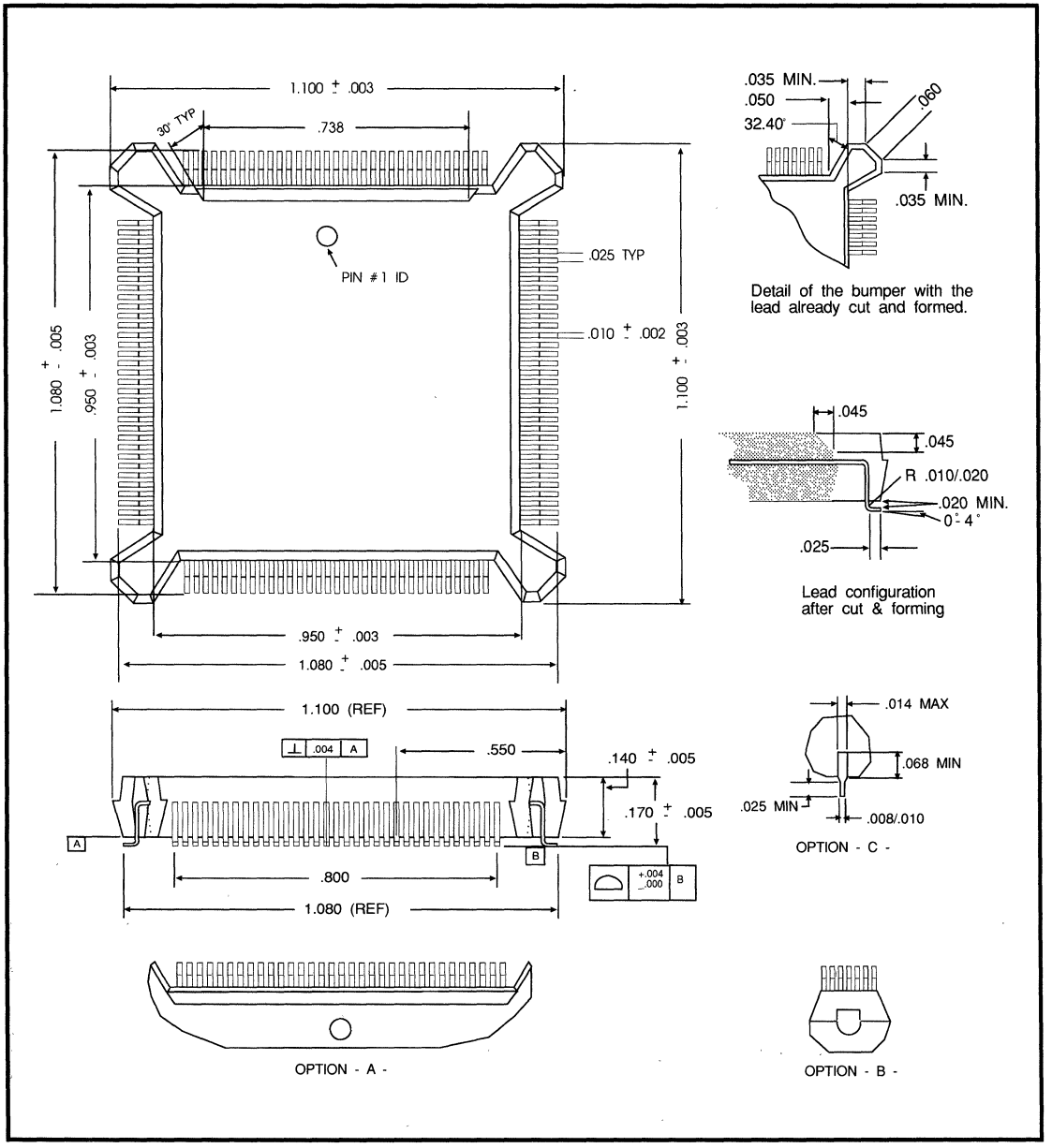


FIGURE 11-1. 132-PIN PQFP PACKAGE