SYSTEMS LOGIC/PERIPHERAL

WD16C550

Enhanced Asynchronous Communications Element (ACE) with FIFOs

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WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DESCRIPTION

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the National NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive overhead during high data rates due to interrupts.

1.2 FEATURES

- Designed to be easily interfaced to most 8-, 16-, and 32-bit microprocessors
- Generating and stripping of serial asynchronous data control bits (start, stop, parity)
- Provides 16-byte FIFO buffers on the transmitter and receiver for CPU relief during high speed data transfer
- FIFO or Character Modes are user selectable
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16} -1) and generates the internal clock
- Independent receiver 16X clock input
- MODEM interface capabilities
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1 1/2-, or 2-stop bit generation
  - baud rate generation (dc to 512K baud)
- False start bit detector
- Complete status reporting capabilities
- Three-state TTL drive capabilities for bi-directional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communication link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Single +5 Volt power supply
- CMOS implementation for high speed and low power requirements
- Available in 40-Pin DIP and 44-Pin QUAD packages

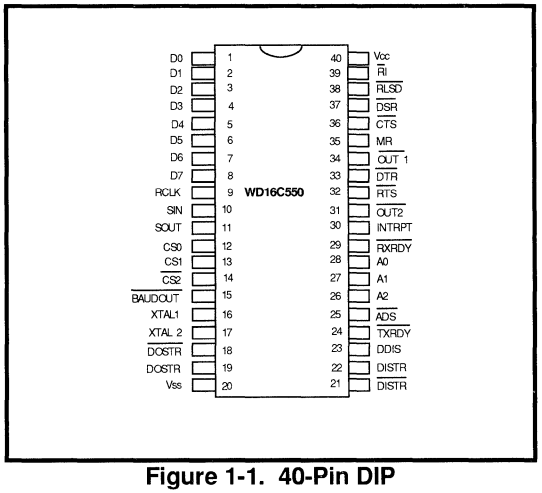

Figure 1-1. 40-Pin DIP

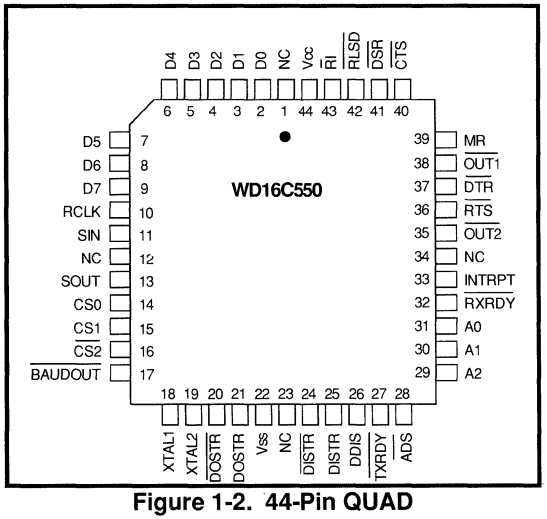

Figure 1-2. 44-Pin QUAD

1.3 GENERAL

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) with FIFOs (hereafter referred to as ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive interrupt overhead during high data rates.
(Refer to figure 1-1.)

In FIFO Mode, internal 16-byte FIFOs (with an additional 3 error data bits per byte in the receiver FIFO) are located on the transmitter and receiver lines. Two FIFO control pins have been added for signaling of DMA transfers.

The ACE is a software-oriented device using a three-state, 8-bit, bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format,in order of transmission and reception, is a start bit, followed by 5 to 8 data bits, a parity bit (if programmed) and 1-, 1 1/2- (5-bit format only), or 2-stop bits (all but the 5-bit format). The maximum recommended data rate is 512K baud.

Internal registers enable the user to program various types of interrupts, MODEM controls, and character formats. The user can read the status of the ACE at any time, monitoring word conditions, interrupts and MODEM status.

An additional feature of the ACE is a programmable baud rate generator capable of dividing a TTL signal clock by a divisor of 1 to (2^{16} - 1).

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by user's software.

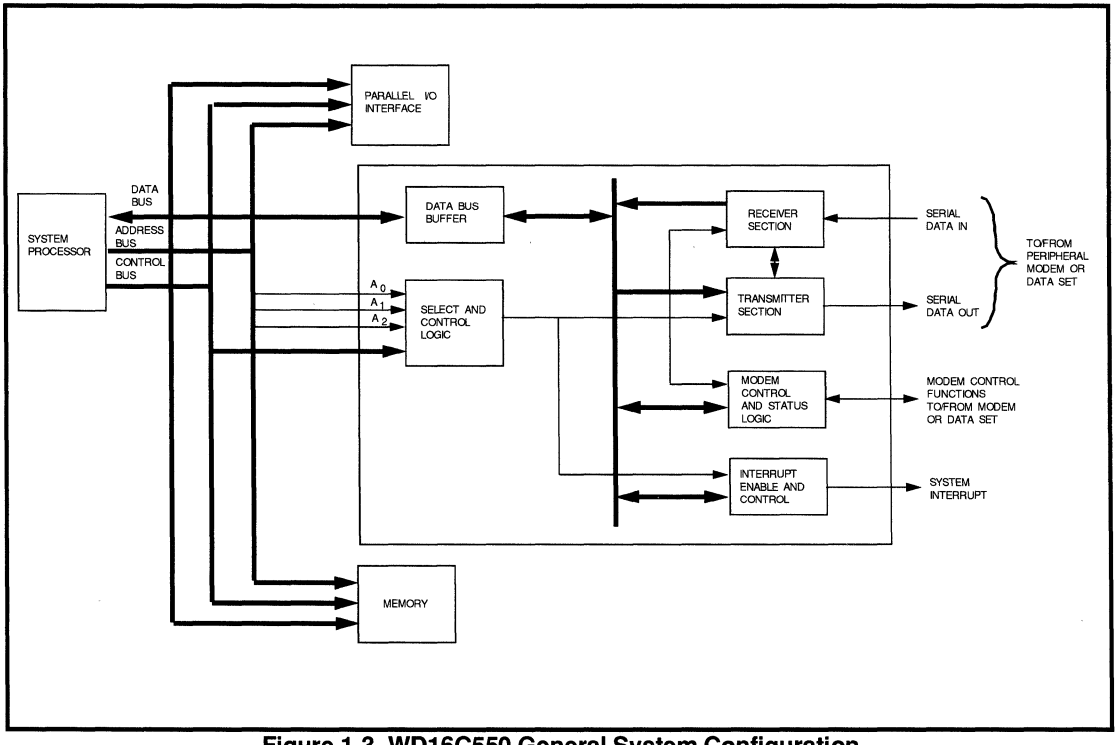

Figure 1-3. WD16C550 General System Configuration

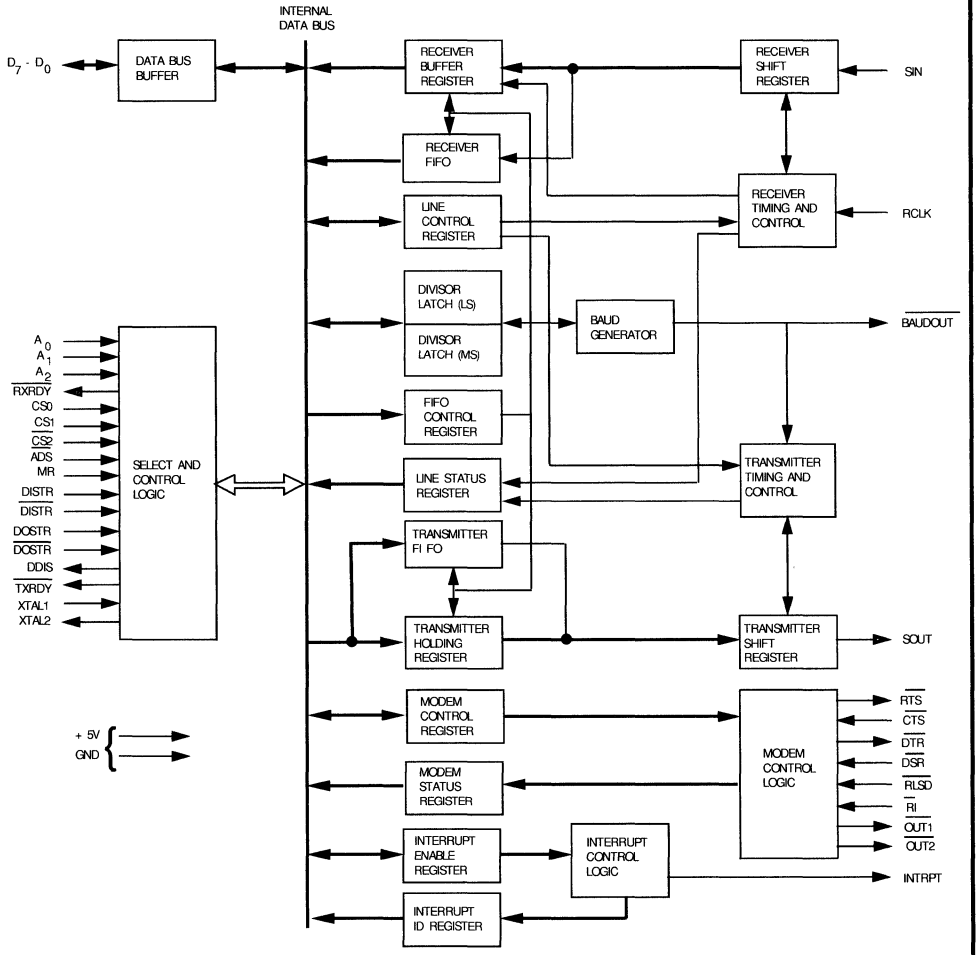

Figure 1-4. WD16C550 Block Diagram

2.0 CHIP SELECTION AND REGISTER ADDRESSING

2.1 ADDRESS STROBE ($\overline{ADS}$)

When low, provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$). (Refer to figure 1-2.)

NOTE:
The rising edge (↑) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is required for latching, this input can be tied permanently low.

2.2 CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The definition of a chip selected is CS0, CS1 both high and $\overline{CS2}$ low. Chip selection is complete when latched by ADS or $\overline{ADS}$ is tied low.

2.3 REGISTER SELECT (A0, A1, A2)

To select a register for read or write operation, see table 2-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status (read only)
X	1	1	0	MODEM Status
X	1	1	1	Scratch Pad
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Table 2-1. Register Addressing

3.0 ACE OPERATIONAL DESCRIPTION

3.1 MASTER RESET

A high-level input on this pin causes the ACE to reset to the condition listed in table 3-1.

3.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in table 3-2. For individual register descriptions, refer to the following pages under register heading.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 Permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, and Bits 1-3, 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low (0-3 forced and and 4-7 Premanent)
Line Status Register	Master Reset	Bits 0-4 and 7 forced Low, Bits 5 and 6 forced High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 - Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
DDIS	DDIS = $\overline{\text{RCLK} \bullet \text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low when device is selected.)	High
INTRPT (RCVR ERRS)	Master Reset/LSR	Low
INTRPT (RCVR DATA READY)	Master Reset/Read RBR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
RCVR FIFO	MR or FCR1 • FCR0 or ΔFCR0	All Bits Low
XMIT FIFO	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL	Master Reset	All Bits Low (Bits 0-3, 7 forced Low; Bits 4 and 5 Permanently Low)
D7 - D0 Data Bus Lines	In THREE-STATE Mode, Unless DISTR = HIGH or DOSTR = HIGH when device is selected	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 3-1. Reset Control of Registers and Pinout Signals

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	Register Address					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending ID Bit 0 (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)*	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	StickParity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

* These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C550 Registers

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO* (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

* These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C550 Registers (Contd)

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3.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

See Crystal Specifications.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2*	2.860

Table 3-3. BAUD Rates Using 1.8432 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
5600	3*	14.285

Table 3-4. BAUD Rate Using 3.072 MHz Clock

* Smallest allowable divisor when using corresponding clock.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1*	2.344

Table 3-5. BAUD Rate Using 8.0 MHz Clock

* Smallest allowable divisor when using corresponding clock.

3.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode, Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level).

When in FIFO Mode, an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled.

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Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator and is a read-only bit. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode, this bit is set when the XMIT FIFO is empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to table 3-2)

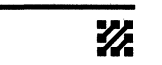
This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).



Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3-6. Interrupt Control Functions

3.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the chip Interrupt (INTRPT) output signal. Its contents are indicated in table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the WD16C550. It is a read/write register that can be used by the programmer as a general purpose register.

3.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from both FIFOs. The FIFOs should be cleared before changing modes. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register is not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

4.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 3-2.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

> NOTE:
> The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxilliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{RTS}$, $\overline{DTR}$, $\overline{OUT2}$, $\overline{OUT1}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

5.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 3-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

NOTE:
Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to OUT1 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to OUT2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

5.1 FIFO OPERATION NOTES

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt will occur if the following is true:
   a. There is at least one byte in the RCVR FIFO.
   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

The timeout counter uses RCLK for an input to calculate character times; therefore, this delay is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

6.0 TYPICAL APPLICATIONS

Figures 6-1 and 6-2 show how to use the ACE device in an 80286 system and in a microcomputer system with a high-capacity data bus.

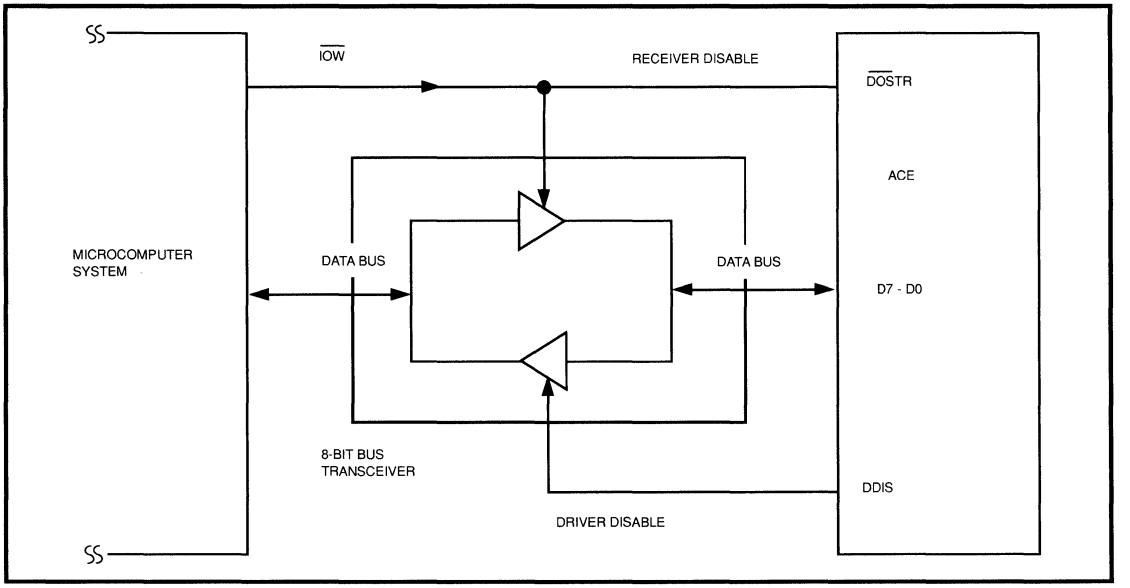


Figure 6-1. Typical Interface for a High-Capacity Data Bus

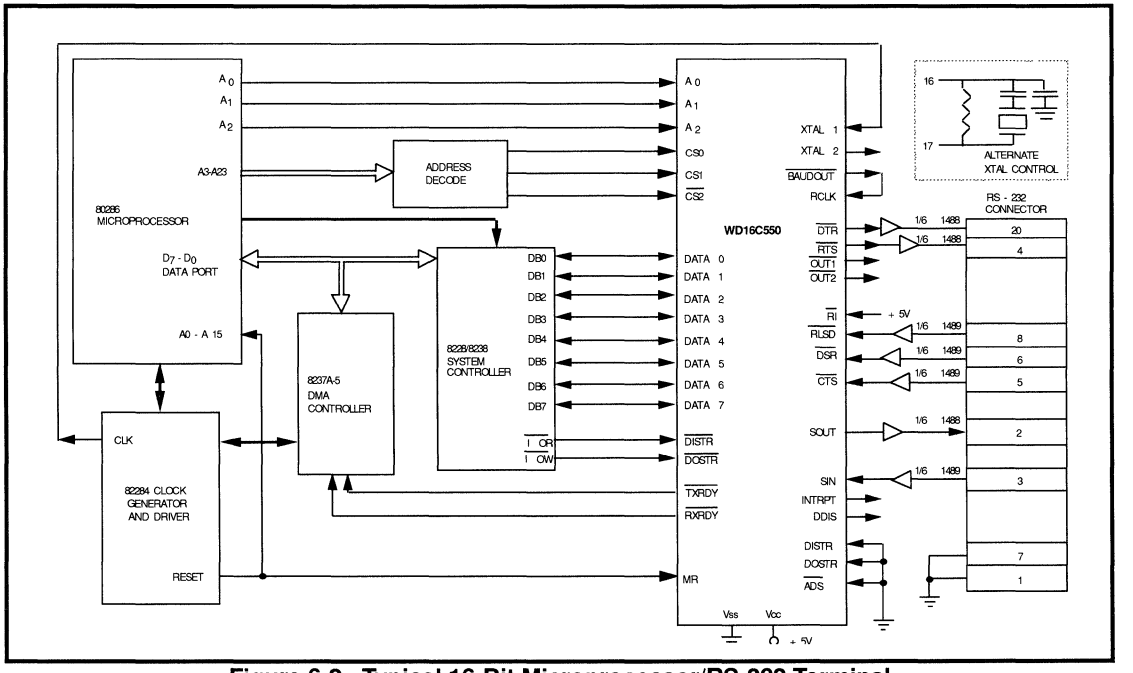


Figure 6-2. Typical 16-Bit Microprocessor/RS-232 Terminal Interface Using the ACE

7.0 CRYSTAL MANUFACTURERS (Partial List)

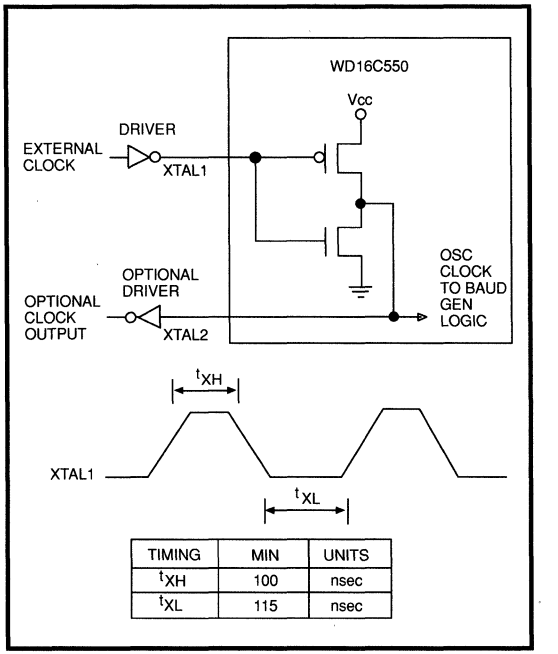
American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Erie, Pennsylvania 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626



TIMING	MIN	UNITS
t_{XH}	100	nsec
t_{XL}	115	nsec

Figure 7-1. External Clock Input (8.0 MHz Max.)

CRYSTAL SPECIFICATIONS

Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz.
Type: Microprocessor Crystal

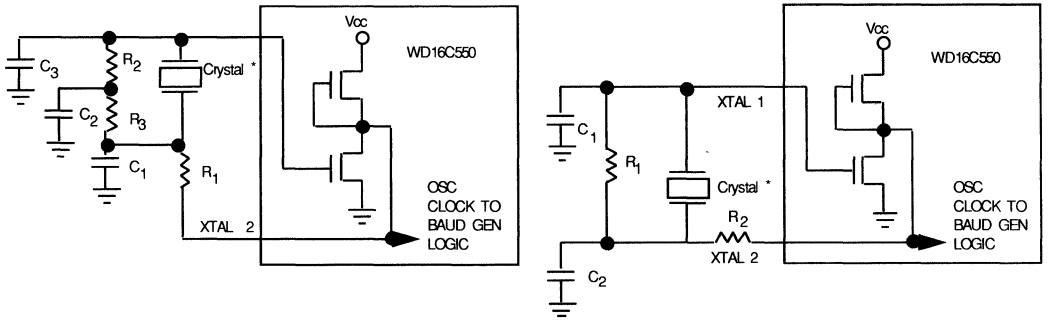
Temperature Range: 0°C(32°F) to + 70°C(158°F)

Series Resistance: 200 Ohms to 500 Ohms
(1.8432 MHz)

100 Ohms to 200 Ohms
(3.072 MHz)

20 Ohms to 40 Ohms
(8.0 MHz)

Series Resonant
Overall Tolerance: ±0.01%



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01pF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01pF	10-15pF

Crystal	R_1	R_2	C_1	C_2
8.0 MHZ	1 M?	1.68K	22pF	40pF
3.1 MHz	1 M?	1.5K	10-30pF	40-60pF
1.8 MHz	1 M?	1.0K	5-15pF	50-100pF

Figure 7-2. Typical Crystal Oscillator Networks

* See Crystal Specifications

APPENDIX A

A.0 PIN DESIGNATIONS

Figures A-1 and A-2 illustrate the 40 - Pin DIP and 44 - Pin QUAD assemblies. Table A - 1 lists all pin designations.

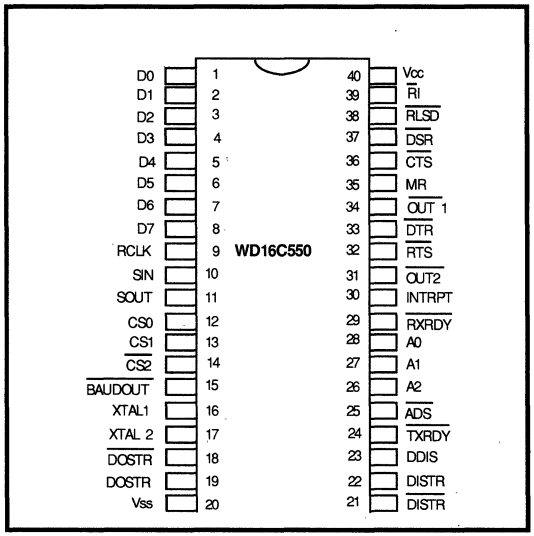


Figure A-1. WD16C550 40-Pin DIP Assembly Pin Designations

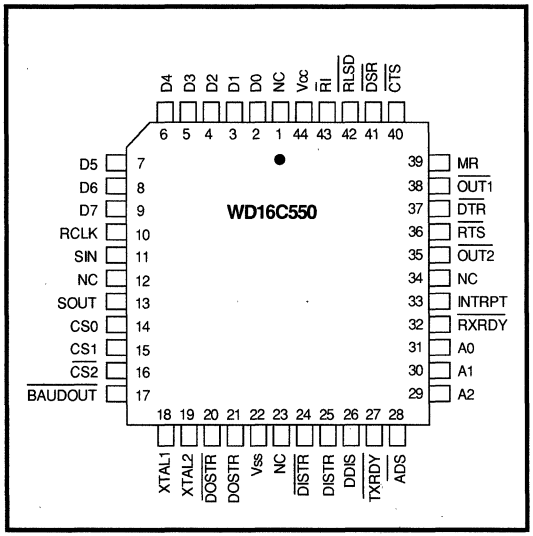


Figure A-2. WD16C550 44-Pin QUAD Assembly Pin Designations

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
1 thru 8	2 thru 9	D0 thru D7	DATA BUS	3-state, bi-directional communication lines between the ACE and Data bus. All prepared TX and assembled REC data, Control characters, and Status information are transferred via the data (D0-D7).
--	1	NC	NO CONNECTION	No Connection.
9	10	RCLK	RECEIVE CLK	This input is the 16X baud rate clock for the receiver section of the chip, may be tied to BAUDOUT (pin 15 for DIP package and/or pin 17 for QUAD package).
10	11	SIN	SERIAL INPUT	Received Serial Data In from the communications link (peripheral device, modem or data set).
--	12	NC	NO CONNECTION	No Connection
11	13	SOUT	SERIAL OUTPUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12	14	CS0	CHIP SELECT	When CS0 and CS1 are high, and CS2 is low, chip is selected. Selection is complete when the address strobe ADS latches the chip select signals.
13	15	CS1	CHIP SELECT 1	Same as CS0.
14	16	$\overline{CS2}$	$\overline{CHIP\ SELECT\ 2}$	Same as CS0.
15	17	$\overline{BAUDOUT}$	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the ACE. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to RCLK (pin 9 for DIP package and/or pin 10 for QUAD package).

Table A-1. Pin Designations

10

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
16	18	XTAL 1	EXTERNAL CLOCK IN	These pins connect the crystal or signal clock to the ACE baud rate divisor circuit. See Fig.7-1 and 7-2 for circuit connection diagrams.
17	19	XTAL 2	EXTERNAL CLOCK OUT	
18	20	$\overline{\text{DOSTR}}$	$\overline{\text{DATA OUT}}$ STROBE	When the chip has been selected, a low DOSTR or high DOSTR will latch into the selected WD16C550 register (a CPU write). Only one of these lines Need be used. Tie unused line to its inactive state, DOSTR - high or DOSTR - low.
19	21	DOSTR	DATA OUT	
20	22	Vss	GROUND	System signal ground.
--	23	NC	NO CONNECTION	No Connection.
21	24	$\overline{\text{DISTR}}$	$\overline{\text{DATA IN}}$ STROBE	When chip has been selected, a low DISTR or high DISTR will allow a read of the selected WD16C550 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state, DISTR - high or DISTR - low.
22	25	DISTR	DATA IN STROBE	
23	26	DDIS	DRIVER DISABLE	Output goes low whenever data is being read from the ACE. Can be used to reverse data direction of external transceiver.
24	27	$\overline{\text{TXRDY}}$	$\overline{\text{TRANSMIT}}$ READY	$\overline{\text{TXRDY}}$ output is used to DMA transfers. Two modes of operatoin are available when using FIFO Mo;de, and one (Mode 0) is available when using Character Mode. Mode 0 (FCR0=0 OR FCR0=1 AND FCR3=0): DMA transfers are interleaved between bus cycles. In character mode with FCR3=0, $\overline{\text{TXRDY}}$ will be active (low) if there are no characters in the XMIT FIFO (FIFO Mode) or Xmit Holding Register (CHAR Mode). $\overline{\text{TXRDY}}$ will go inactive after the first character is loaded.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
				Mode 1: Multiple DMA bursts are made until TXMT **is empty or XMIT is full. In FIFO Mode (FCR=1) with FCR3=1, if there is at least one unfilled position in the Xmit FIFO,** TXRDY will be active (low). TXRDY will go inactive after the first character is loaded into the Xmit FIFO.
25	**28**	$\overline{\text{ADS}}$	$\overline{\text{ADDRESS}}$ STROBE	When low, provides latching for Register Select (A0,A1,A2) and Chip Select (CS0,CS1,CS2). NOTE: The rising edge (↑) of the ADS signal is required when the Register Select (A0,A1,A2) and the Chip Select (CS0, CS1, CS2) signals are not stable for the duration of a read or write operation. If not required, the ADS input can be tied perman -ently low.
26	29	A2	REGISTER SELECT A2	These three inputs are used to select an internal register of the ACE during a read or a write. See Table 2-1.
27	30	A1	REGISTER SELECT A1	
28	31	A0	REGISTER SELECT A0	
29	32	$\overline{\text{RXRDY}}$	$\overline{\text{RECEIVER}}$ READY	Receiver Ready output is used to signal DMA transfes. Two modes of operation are available when using FIFO Mode, and one mode (Mode 0) is available when using Character Mode. Mode 0: DMA transfers are interleaved between bus cycles When in Character Mode (FCR0=0) or in the FIFO Mode (FCR0=1), with FCR3=0, and there is at least 1 character in the Rcvr FIFO Register or Rcvr Holding Register, the RXRDY will be active (low). It will go inactive when the Rcvr FIFO (FIFO Mode) or Holding Register (Character Mode) is empty.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
				Mode 1: Multiple DMA bursts are made until RCVR FIFO is empty or XMIT FIFO is full. In FIFO Mode (FCR0=1) and FCR3=1, will go active (low) when the trigger level or time out has been reached. RXRDY becomes inactive (high) when the FIFO is empty.
30	33	INTRPT	INTERRUPT	Output goes high whenever an enabled interrupt is pending.
--	34	NC	NO CONNECTION	No Connection.
31	**35**	$\overline{OUT2}$	$\overline{OUTPUT\ 2}$	User-designated output that can be programmed by Bit 3 of the Modem Control Register (OUT2 goes low when Bit 3 = 1).
32	36	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	Output when low informs the modem or data set that the ACE is ready to transmit data. See Modem Control Register.
33	37	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	Output when low informs the modem or data set that the ACE is ready to receive data.
34	38	$\overline{OUT\ 1}$	$\overline{OUTPUT\ 1}$	User-designated output that can be programmed by Bit 2 of Modem Control Register (OUT1 goes low when Bit 2 = 1).
35	39	MR	MASTER RESET	When high clears the registers to the states as indicated in Table 3-1.
36	40	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	Input from DCE indicating remote device is ready to Transmit data. See Modem Status Register.
37	41	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	Input from DCE used to indicate the status of the local data set. See Modem Status Register.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
38	42	$\overline{RLSD}$	$\overline{RECEIVER\ LINE\ SIGNAL\ DETECT}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Status Register.
39	43	$\overline{RI}$	$\overline{RING\ INDICATOR}$	Input when low indicates that a ringing signal is being received by the modem or data set. See Modem Status Register.
40	44	Vcc	+5V	+5 Volt Supply.

Table A-1. Pin Designations (Contd)

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature
Ceramic ..... -65°C (-85°F) to +150°C (302°F)
Plastic ..... -50°C (-58°F) to +125°C (257°F)

All Input or Output Voltages
with respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C550 ..... 40mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

SYMBOL	CHARACTERISTIC	WD16C550 MIN	MAX	UNITS	TEST CONDITIONS
Vil x	Clock Input Low Voltage	-0.5	0.8	V	
Vih x	Clock Input High Voltage	0.2	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 1.6mA on all outputs
Voh	Output High Voltage	2.4		V	Ioh = -100µA
Icc	(AV) Average Power Supply Current (Vcc)		8	mA	Vcc = 5.25V Ta = 25°C. No (Vcc) loads on SIN, DSR,RLSD, CTS. RI = 2.0V. All other inputs = 0.8V. Baud rate generator at 8 MHz. Baud rate at 512K.
Iil	Input Leakage		±15	uA	Vcc = 5.25V. Vss = 0V. All other pins floating.
Icl	Clock Leakage		±10	uA	Vin = 0V, 5.25V
Idl	Data Bus Leakage		±10	uA	Vout = 0.0V Vout = 5.25V Data Bus is at High-Impedance State
Vilmr	MR Schmitt Vil		0.8	V	
Vihmr	MR Schmitt Vih	2.0		V	

Table B-1. DC Operating Characteristics
Ta = 0°C (32°F) to +70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, Unless Otherwise Specified.

SYMBOL	CHARACTERISTIC	WD16C550 TYP	MAX	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Table B-2. Capacitance
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

APPENDIX C

C.O AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%,

C.1 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Baud Rate Generator Timing
C-2	Receiver Timing
C-3	Transmitter Timing
C-4	MODEM Control Timing
C-5	Read Cycle Timing
C-6	Write Cycle Timing
C-7	RCVR FIFO Signaling Timing for First Byte
C-8	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-9	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-10	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-11	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-12	Transmitter DMA Mode 1 (FCR0 = 1 and FCR3 = 1)

Table C-1. WD16C550 Timing Diagrams

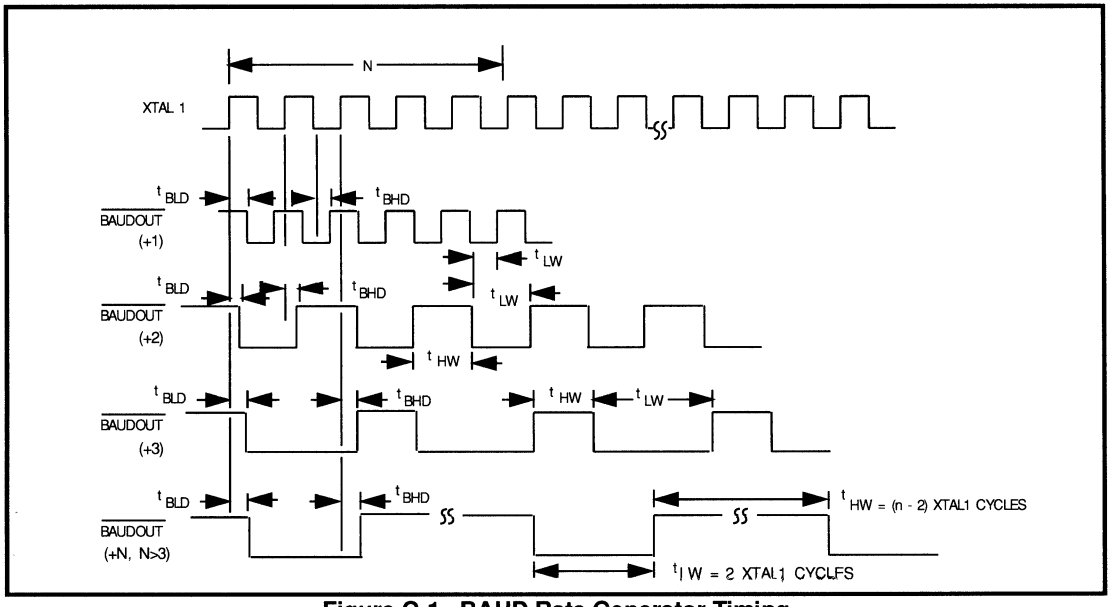


Figure C-1. BAUD Rate Generator Timing

10

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
N	Baud Rate Divisor	1	$(2^{16} - 1)$		
t_{BLD}	Baud Output Negative Edge Delay		100	nsec	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		100	nsec	100pF Load
t_{LW}	Baud Output Low Time	32		nsec	100pF Load (fx = 8. 0 MHz÷1)
t_{HW}	Baud Output High Time	30		nsec	100pF Load (fx = 8. 0 MHz÷1)

Table C-2. BAUD Rate Generator Timing

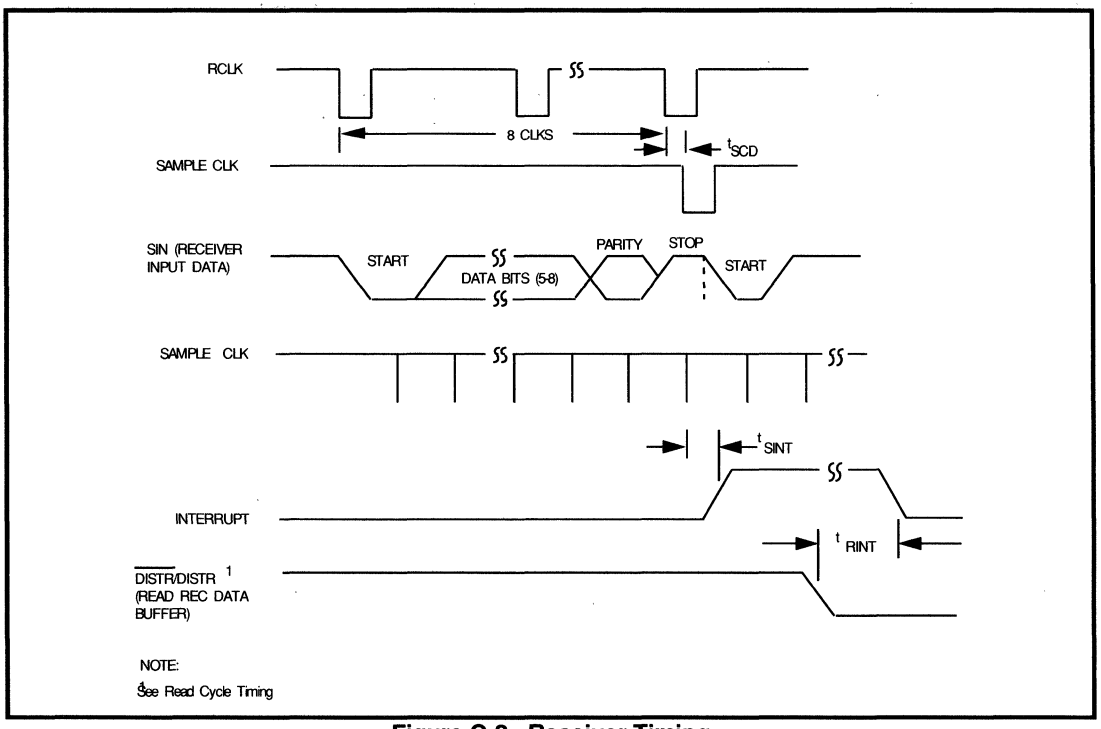


Figure C-2. Receiver Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK to Sample Time		2	µsec	
tSINT	Delay from Stop to Set Interrupt		1*	RCLK Cycles	100pF Load
tRINT	Delay from DIST/DISTR (RD RBR) Reset Interrupt	0.250	1	µsec	100pF Load

Table C-3. Receiver Timing

* When receiving the first byte in FIFO mode tSINT (only for timeout or trigger level interrupt) will be delayed 3 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 8 RCLK cycles.

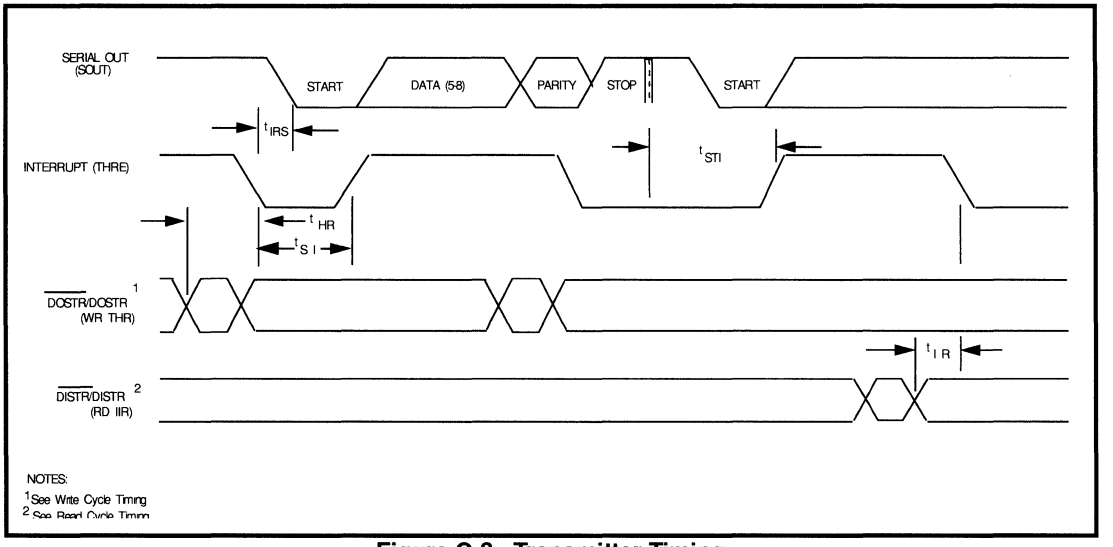


Figure C-3. Transmitter Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tHR	Delay from $\overline{\text{DOSTR}}$/ DOSTR (WR THR) to Reset Interrupt		0.175	µsec	100pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSI	Delay from Initial Write to Interrupt	16	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSTI	Delay from Stop to Interrupt ($\overline{\text{THRE}}$)	8	8	$\overline{\text{BAUDOUT}}$ Cycles	
tIR	Delay from $\overline{\text{DISTR}}$/ DISTR (RD IIR to Reset Interrupt (THRE)		0.250	µsec	100pF Load
tSXA	Delay from Start to TXRDY Active	0	8	$\overline{\text{BAUDOUT}}$ Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	0.195	µsec	

Table C-4. Transmitter Timing

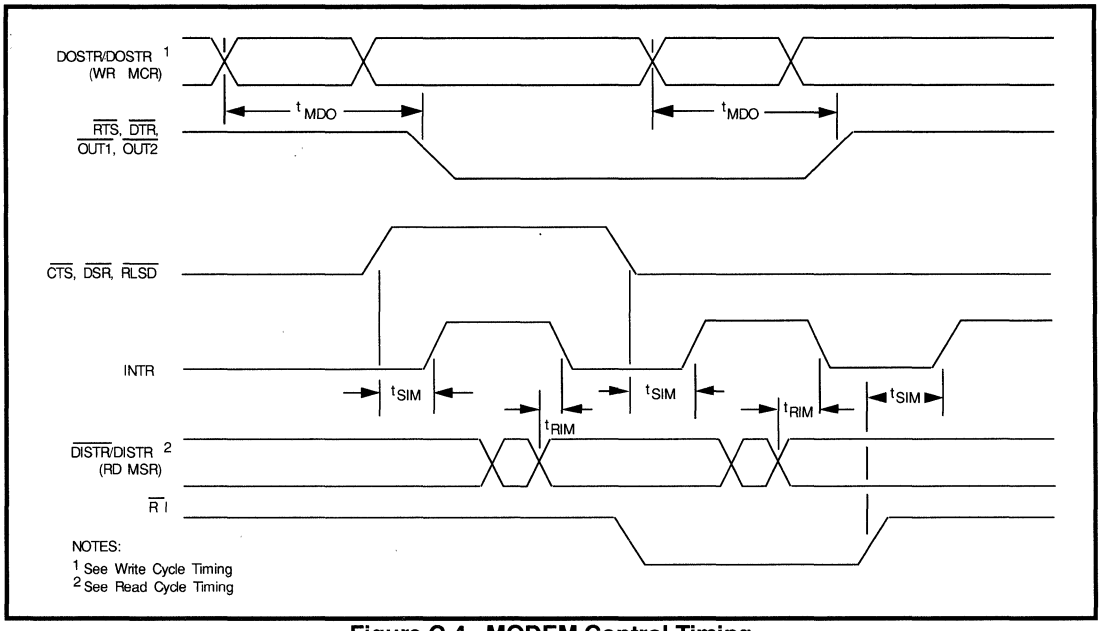


Figure C-4. MODEM Control Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from $\overline{DOSTR}$/ DOSTR (WR MCR) to Output		0.200	µsec	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		0.250	µsec	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)		0.250	µsec	100pF Load

Table C-5. MODEM Control Timing

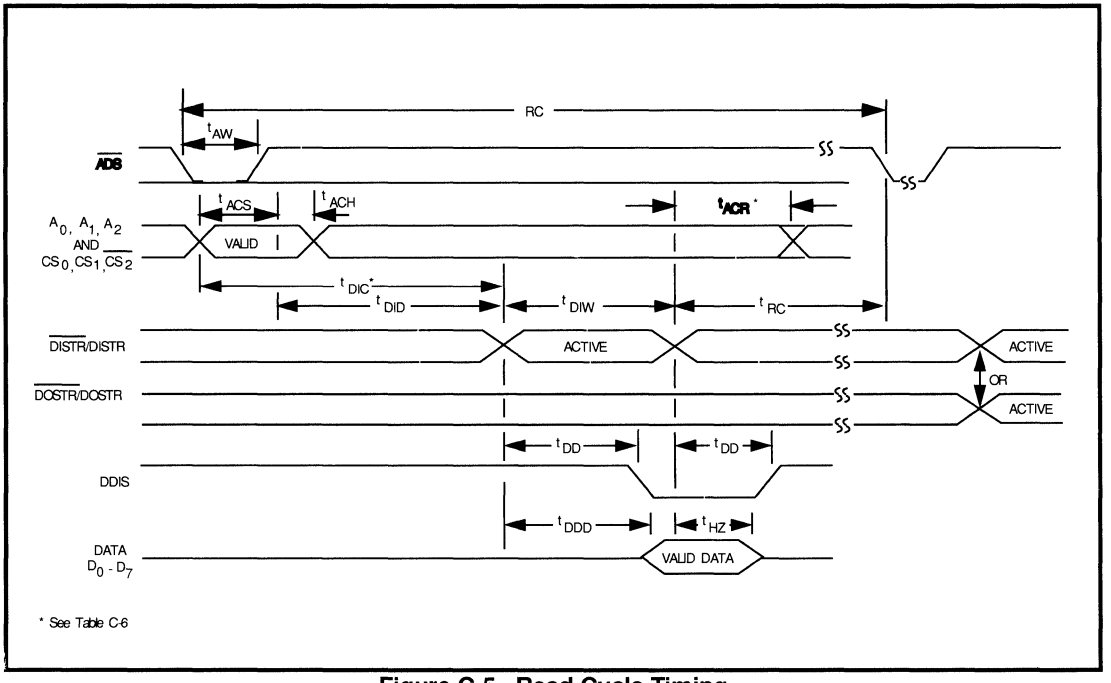


Figure C-5. Read Cycle Timing

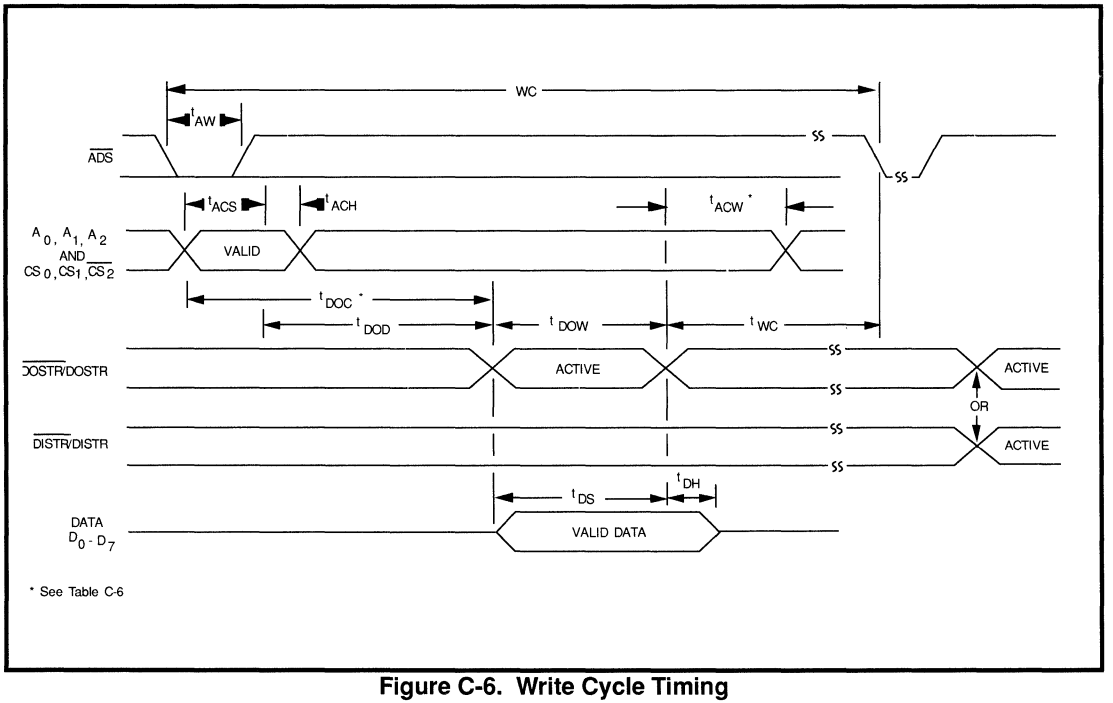


Figure C-6. Write Cycle Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tAW	Address Strobe Width	60		nsec	1TTL Load
tACS	Address and Chip Select Setup Time	60		nsec	1TTL Load
tACH	Address and Chip Select Hold Time	0		nsec	1TTL Load
tDID	$\overline{\text{DISTR}}$/DISTR Delay from latch			nsec	1TTL Load
tDIW	$\overline{\text{DISTR}}$/DISTR Strobe Width	125		nsec	1TTL Load
tRC	Read Cycle Delay	125		nsec	1TTL Load
RC	Read Cycle = tACS + tDID + tDIW + tRC + 20 nsec	280		nsec	1TTL Load
tDD	$\overline{\text{DISTR}}$/DISTR to Driver Disable Delay		60	nsec	1TTL Load
tDDD	Delay from $\overline{\text{DISTR}}$/DISTR to Data		100	nsec	1TTL Load
tHZ	$\overline{\text{DISTR}}$/DISTR to Floating Data Delay	0	100	nsec	1TTL Load
tDOD	DOSTR/DOSTR Delay from Latch			nsec	1TTL Load
tDOW	DOSTR/DOSTR Strobe Width	100		nsec	1TTL Load
tWC	Write Cycle Delay	150		nsec	1TTL Load
WC	Write Cycle =tACS + tDOD + tDOW + tWC + 20 nsec	280		nsec	1TTL Load
tDS	Data Setup Time	30		nsec	1TTL Load
tDH	Data Hold Time	30		nsec	1TTL Load
tDIC*	DISTR/DISTR DELAY from Select or Address	30		nsec	1TTL Load
tDOC*	$\overline{\text{DOSTR}}$/DOSTR Delay from Select or Address	30		nsec	1TTL Load
tACR*	Address and Chip Select Hold Time from DISTR/DISTR	20		nsec	1TTL Load
tACW*	Address and Chip Select Hold Time from DOSTR/DOSTR	20		nsec	1TTL Load
tMR	Master Reset Pulse Width	5.0		µsec	1TTL Load
tXH	Duration of Clock HIGH Pulse	55		nsec	
tXL	Duration of Clock LOW Pulse	55		nsec	External Clock (8.0 MHz Max.)

* Only applicable when $\overline{\text{ADS}}$ is permanently low.

Table C-6. Read/Write Cycle Timing

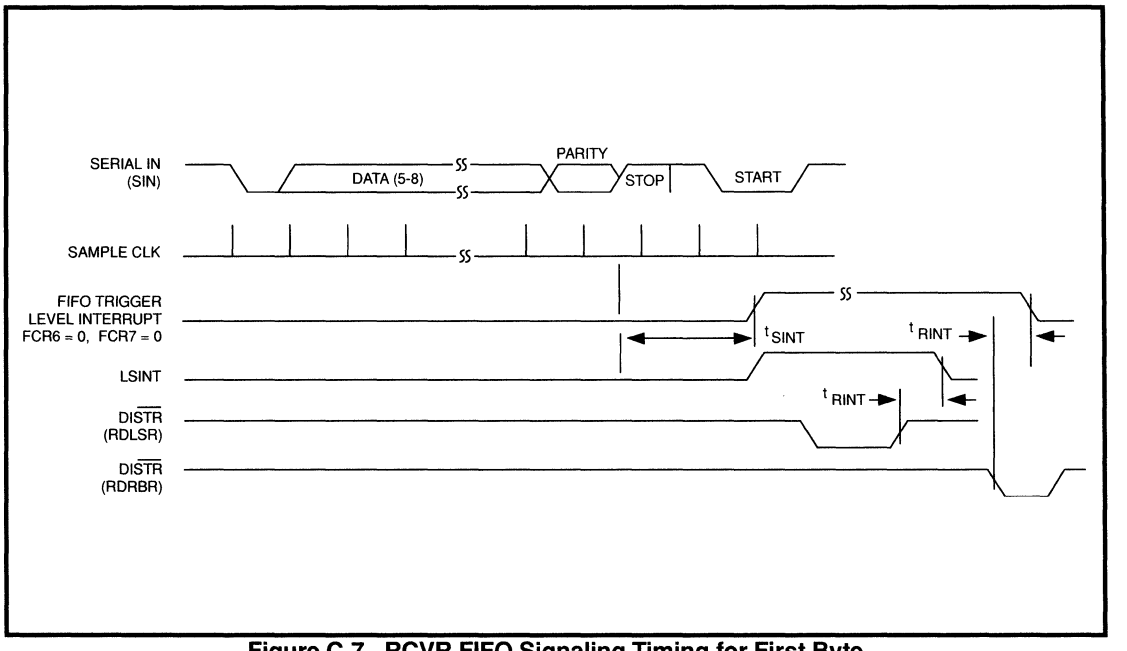


Figure C-7. RCVR FIFO Signaling Timing for First Byte

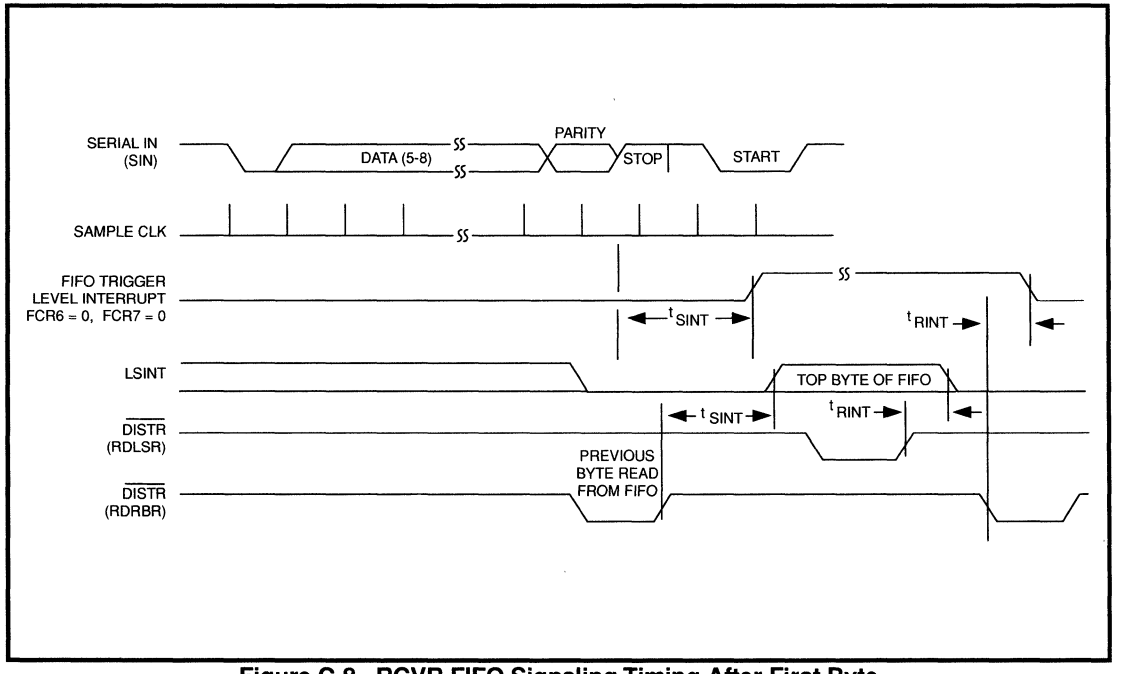


Figure C-8. RCVR FIFO Signaling Timing After First Byte (RBR Already Set)

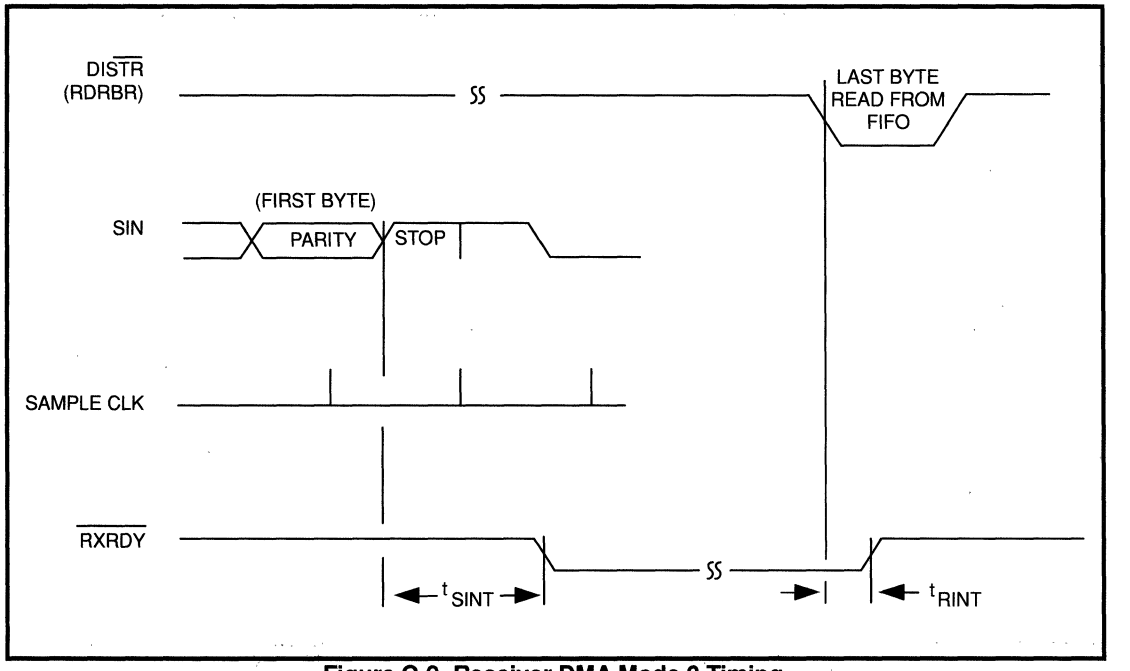


Figure C-9. Receiver DMA Mode 0 Timing
(FCR0=0 or FCR0=1, FCR3=0)

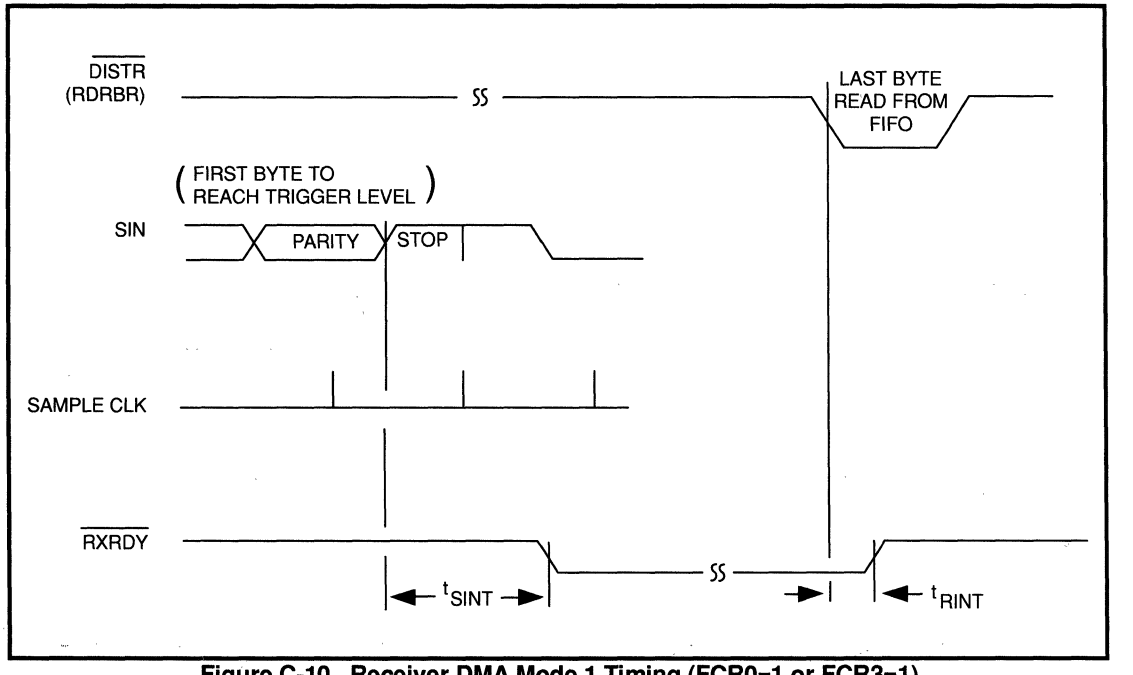


Figure C-10. Receiver DMA Mode 1 Timing (FCR0=1 or FCR3=1)

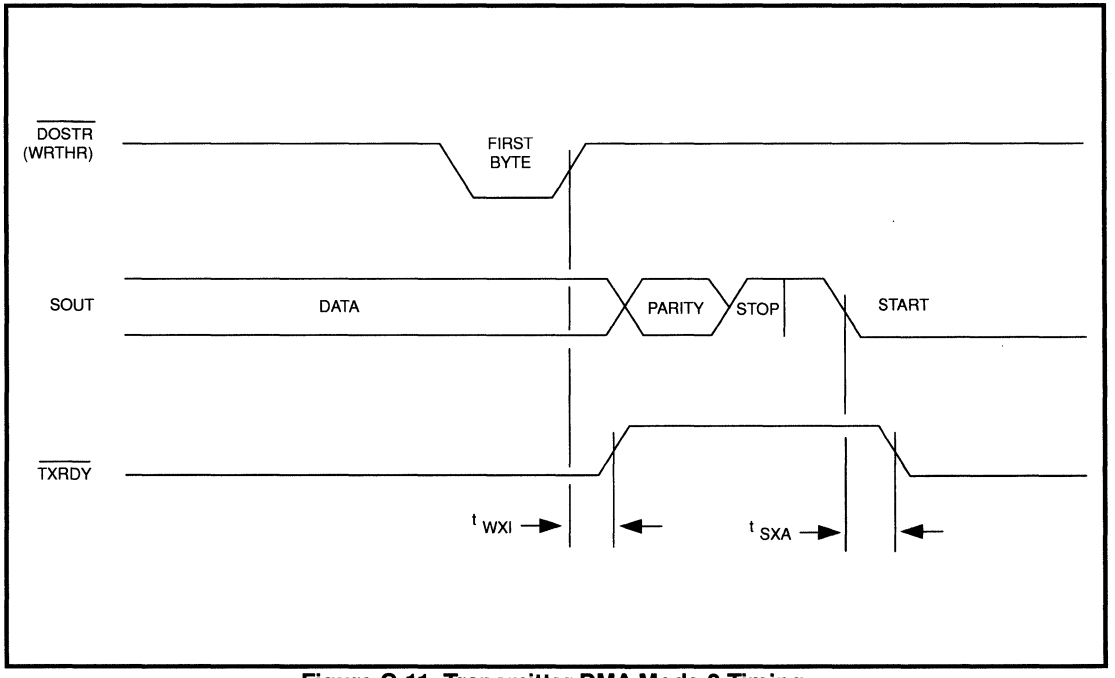


Figure C-11. Transmitter DMA Mode 0 Timing (FCR0=0 or FCR0=1 and FCR3=0)

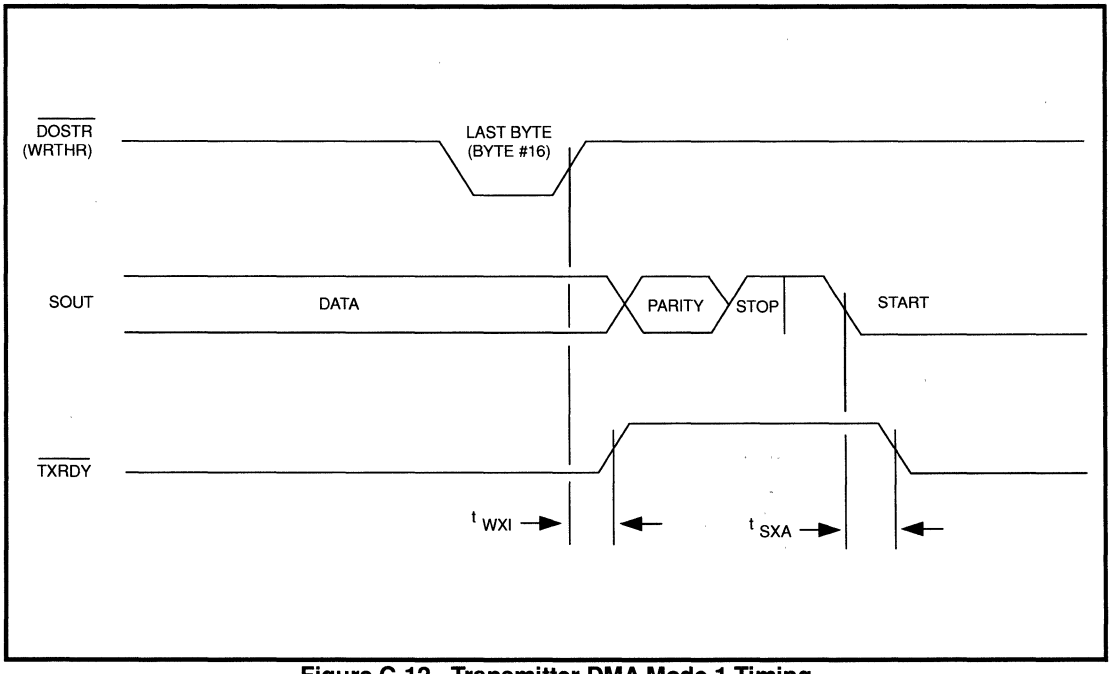


Figure C-12. Transmitter DMA Mode 1 Timing (FCR0=0 or FCR0=1 and FCR3=0)

APPENDIX D

D.O PACKAGE DIAGRAMS

Figures D-1, D-2, and D-3 illustrate the 40-Pin DIP packages and 44-Pin QUAD package showing dimensions in inches.

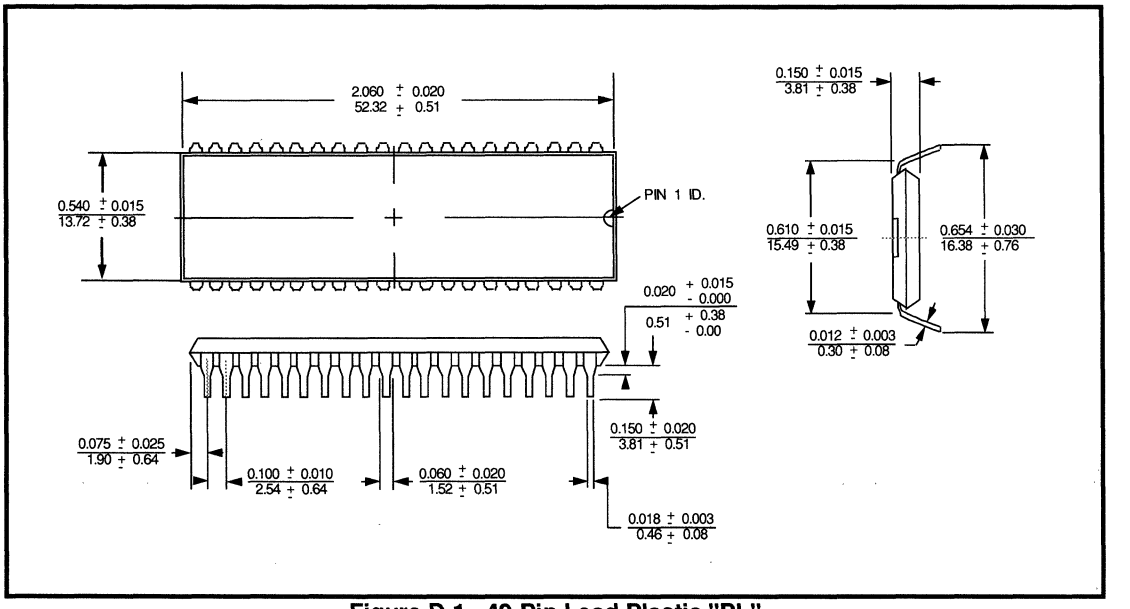


Figure D-1. 40-Pin Lead Plastic "PL"

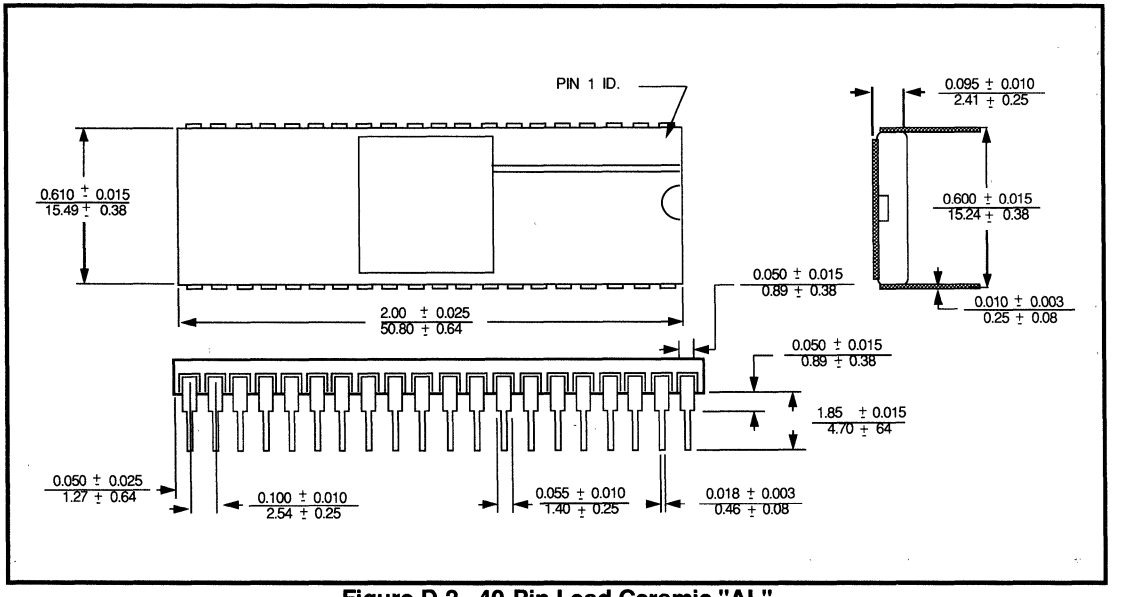


Figure D-2. 40-Pin Lead Ceramic "AL"

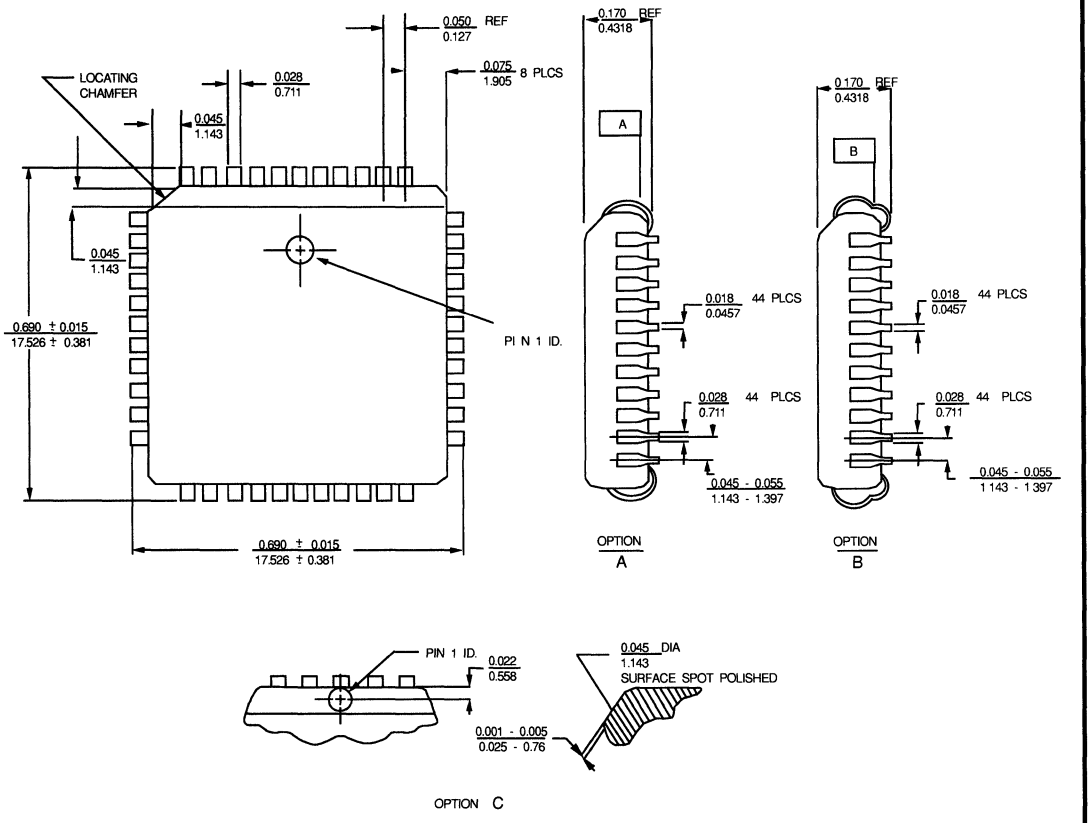


Figure D-3. 44-Pin QUAD Lead Plastic "JM"