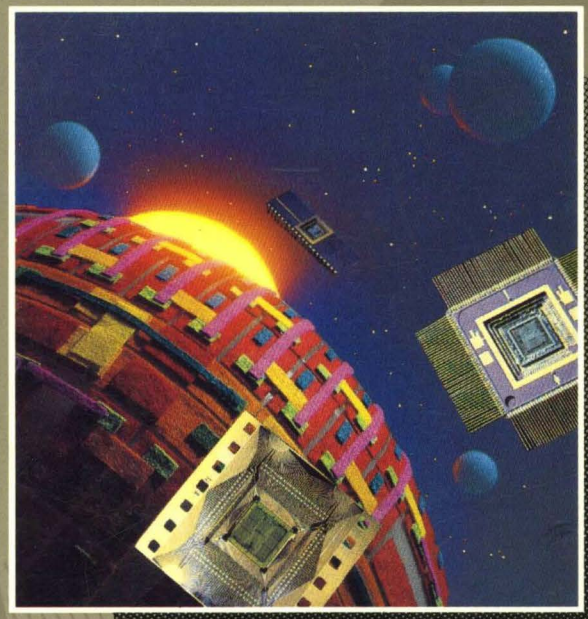
HIGH-PERFORMANCE INTEGRATED CIRCUITS

DATA BOOK AND APPLICATIONS MANUAL

- CMOS A·C·T Interface Logic Family
- Linear Signal Processing Circuits
- Analog Master Chips
- Linear/Digital Bipolar Cell Library
- High-Performance Digital Bipolar Cell Library



On the Silicon Frontier...™

VTC Incorporated

HIGH-PERFORMANCE INTEGRATED CIRCUITS
DATA BOOK AND APPLICATIONS MANUAL

VTC

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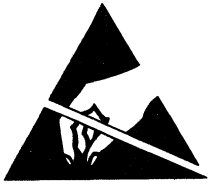

ATTENTION

JEDEC-14/Symbol

All VTC products have input and output circuits that protect against damage due to high static voltages or electrostatic fields. However, VTC still recommends following normal ESD precautions for handling semiconductor devices.

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VTC INCORPORATED

VTC is a specialist manufacturer of high-performance integrated circuits. The company consists of two operating divisions - Microcircuits, founded in 1967, uses advanced bipolar technology; the VHSIC Technology division, established in 1984, produces state-of-the-art CMOS products. Both operations are dedicated to the quality production of well-defined and specified high-performance circuits, focusing on high-speed and offering both standard products and semi-custom services.

Microcircuits utilizes 2 and 3 micron bipolar technologies to produce analog, digital, and combined analog/digital functions. These include the VL1000 linear standard cell library and the VL2000 high-speed digital standard cell library. Both systems are work station based, and the 2000 offers the 300 picosecond internal gate delays of CML technology, 1500 to 5000 gate complexity, and inputs and outputs compatible with ALS, HCT, and 10KH ECL.

The VHSIC Technology division uses an advanced 1.6 micron, double level metal, N well process to produce the ACT family of interface functions and the VLSI 6000 gate array. The 6000 provides 800 picosecond internal gate delays with an on-chip maintenance system and the comprehensive Midas™ software simulation tools. It is provided in a choice of 172 pin packages - leadless chip carrier, pin grid array, or hermetic PTAB™. The division has developed a 1.2 micron double level metal P well process in both commercial and radiation-hardened flows, exhibiting hardness to a level beyond a megarad.

Both divisions are located in suburban Minneapolis, far from the costs and problems that plague semiconductor companies based in California's Silicon Valley. The company is well financed and has a complete capability to manufacture highly reliable integrated circuits.

Our designers are experienced and have the latest and best software and hardware tools to ensure a highly productive team that produces the most competitive circuits. We make our own masks in a shop equipped with E-beam technology.

VTC's manufacturing processes are the result of years of development and refinement with proven quality and reliability. Our R and D engineers and scientists will provide near-micron bipolar and submicron CMOS capability to maintain VTC's position at the leading edge of manufacturable semiconductor technology.

Our factories are designed for efficient, high-volume production with the most advanced manufacturing and test equipment. Our wafer fabrication areas use direct step-on-wafer fine-line photolithography; isotropic reactive ion etching to control small features; dry plasma etching; ion implantation to maintain rigid control over junction depths, profiles and transistor threshold voltages; and bias sputtered quartz to provide planar surfaces between metal layers. Rigorous process controls and cleanliness standards in class 10 clean rooms with class 1 work spaces are critical to achieving VTC's high yields in the production of complex VLSI circuits.

VTC's in-house packaging capability is well advanced and includes plastic and hermetic packages, dual in-line and surface mounted, from 6 to 172 pins. VTC's Tape Automated Bonding technique, PTAB™, offers a unique alternative to conventional wire bonding. Various testers are used with capabilities up to 120 pins. These include Sentry Series 80 and LTX systems, the latter having laser trim capability.

VTC's quality department has many millions of hours of operating life test data, and has the latest equipment to control vendor quality, provide process control, qualify new products, and provide critical feedback to R and D as new technology is developed.

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VTC'S ACT INTERFACE FAMILY

VTC's VHSIC Technology Division has produced a new family of interface circuits using an advanced 1.6 micron, double level metal CMOS process. This third generation CMOS logic family moves beyond the HCT products to match the high speed and drive capability of the bipolar ALS family with traditional CMOS power requirements.

The new family, designated ACT, uses familiar 74 series functions and pinouts to offer a new standard for interfacing requirements for systems engineers in several areas.

- direct *replacement of the ALS* family, with the benefit of three to five orders of magnitude of power reduction in the quiescent state;
- *performance upgrade* for existing systems using HCT products;
- *state of the art interfaces* for the latest generation of microprocessors, memories, and gate arrays.

All the possible requirements to set a new standard in a logic family have been incorporated into VTC's new ACT family:

- *Low Power:* input current several orders of magnitude less than equivalent ALS functions
- *High Speed:* propagation delays that meet and exceed those of ALS, 5 ns typical
- *TTL Level Drive:* 48 mA driving a 50Ω line for commercial temperature range (32 mA military)
- *Pin-Outs:* same as ALS
- *Latch-Up:* typical current required exceeds 200 mA
- *ESD Protection:* greater than 2000 volts as defined by MIL-STD-883C Method 301
- *Fully Characterized and Guaranteed:* minimums and maximums, over temperature and voltage, 50 pF and 300 pF loads, commercial and military temperature ranges, test jig definition.

The application sections of the VTC data book are written to help designers gain maximum competitive advantage in their systems. The various sections include characterization of the family, test and correlation procedures, good system design and layout practices, comparison of ACT to other TTL and CMOS families, quality and reliability, and packaging.

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SYSTEM DESIGN CONSIDERATIONS

INTRODUCTION

As the digital integrated-circuit market has expanded, the need has increased for a very-high-speed logic family with low power dissipation. Present system design demands a logic family with high clock rate capability, short propagation delays, and a minimum of layout constraints. The V54/74ACT family of TTL-compatible CMOS logic has evolved from these factors.

The 1.0 ns gate propagation delay of CMOS gives the family a speed range between the ALS and AS families. Additional characteristics, such as low power dissipation, low input load currents, low input capacitance, and slower rise and fall times have eased the difficulties encountered in trying to balance system speed versus ease of design.

The V54/74ACT components have the capability of performing in a system that uses clock rates up to 75 MHz. To permit such high-speed operation, gate propagation delays must be short. To simplify wiring techniques and to minimize the use of transmission lines, rise and fall times have been kept to slower values. The typical rise time is 3 ns for 50 pF type loads, with propagation delays through the buffers and transceivers of less than 10 ns.

The V54/74ACT family can be used to obtain maximum versatility with low power and ease of layout design. The V54/74ACT family has the capability to drive long lines and is specified to be functionally compatible with their equivalent ALS part. In order to take full advantage of this family's capabilities, some restraints and cautions must be observed in laying out the board, power bussing to components, driving long lines, and using large fan-outs at maximum frequency.

The following material will give the system designer insight into these areas of concern:

-the use of non-transmission line interconnections
-power supply needs and constraints
-the characteristics of transmission lines that affect the V54/74ACT interconnections.

PRINTED CIRCUIT BOARD CONNECTIONS

Layout rules for designing with the V54/74ACT family depend on the criteria of the system used. This circuit family may be used in layouts ranging from a single-layer printed circuit board (PCB) with wired interconnects, to the most elaborate multilayer board with a complete transmission line environment. The optimization of system layout will include considerations of system size, performance, and cost.

GROUND INTERCONNECTION CRITERIA

When possible, the use of power distribution elements (PDEs) or a ground plane is suggested. A ground plane is beneficial for maintaining a low noise voltage plane for the V_{CC} supply and maintaining constant characteristic impedance when transmission wires are necessary. A ground plane may be established by using a single-sided board with wired interconnects, or by using a double or multilayer PC board. Power distribution elements are also beneficial for providing low noise environments, and are strongly recommended by VTC. PDEs will be discussed later in this section.

To illustrate how ground noise can couple through a common ground path and cause noise problems in the system, consider the situation outlined in Figure 1.1A. This figure shows a double-sided board with power and ground distribution on one side and signal traces on the other side. A typical ground and supply distribution system can be created by use of interwoven fingers of supply and ground paths, as illustrated in Figure 1.2.

The following text illustrates a possible scenario using this type of layout. Figure 1.1A shows four IC packages, where gate G3 drives gate G1 and gate G2 drives gate G4. Gates G2 and G3 share a common ground path. Figure 1.1B shows an electrical equivalent circuit for this set-up.

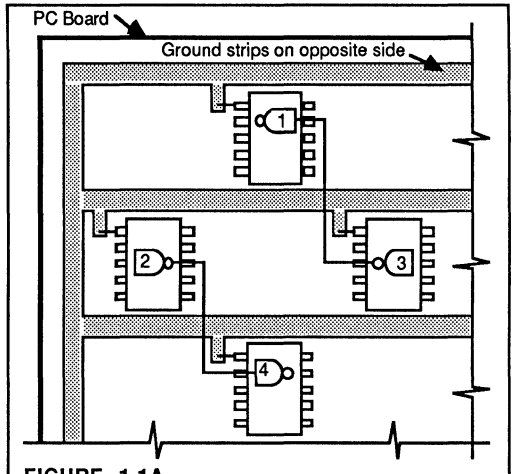


FIGURE 1.1A
GROUND NOISE EXAMPLE

The inductors L1, L2, L3, and L4 represent the distributed inductance of the ground strips. As gate G3 switches from high to low, the transient ground current from G3 flows in the ground pin of G2. But there is a ground strip common for G2 and G3 with an equivalent inductance L2. The transient ground current from G3, acting on L2, appears as a positive spike on the ground

strip and could couple through to the output of gate G2, if G2 was on and in the low state. This happens because the V_{OL} level of G2 is always referenced to its ground pin. Thus, if the ground voltage changes, so does the V_{OL} signal.

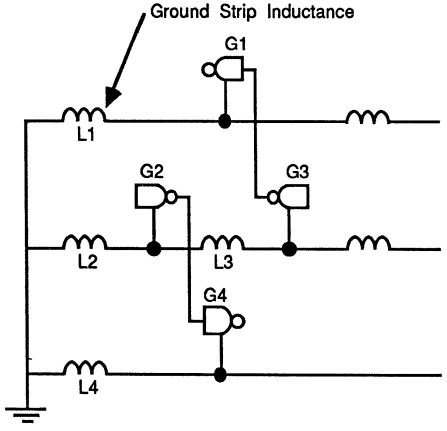


FIGURE 1.1B
EQUIVALENT CIRCUIT

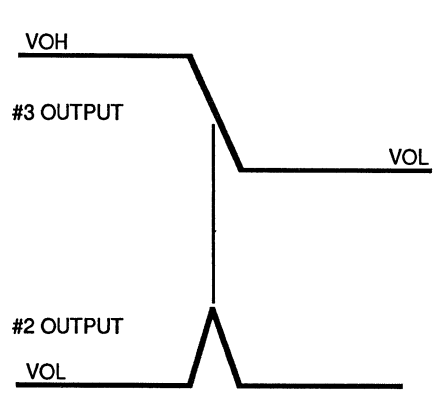


FIGURE 1.1C
GATE OUTPUT WAVEFORMS

The positive spike on G2 appears at the input of G4. Figure 1.1C illustrates these waveforms. If the sum of the quiescent V_{OL} of G2 plus the positive spike due to ground bounce is big enough, the input of G4 could be driven into the threshold region, which could cause G4's output to amplify the spike and propagate it through the rest of the system.

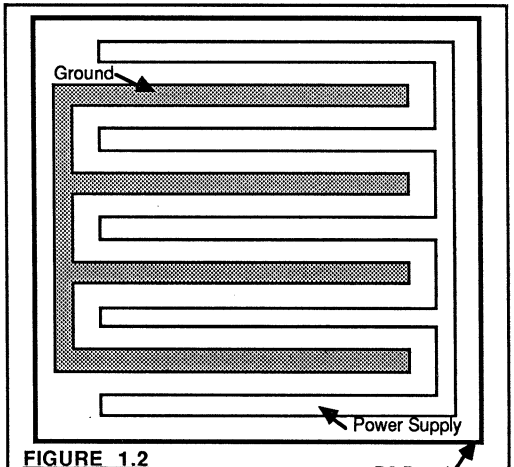


FIGURE 1.2
GROUND AND SUPPLY DISTRIBUTION SYSTEM (2-SIDED BOARD)

Figure 1.3 suggests an approach to minimize these ground spikes for two-sided boards if PDEs or a ground plane are not provided. The ground distribution strips are periodically connected by narrow traces on the top of the board. This reduces the common ground inductance component of any two packages and minimizes the ground spike. These links need not be straight, as shown in the sketch. Typically, a spacing of a few inches will suffice.

Bus drivers need closer attention. The simultaneous switching of a group of bus drivers on a common ground strip only an inch or two long can cause large spikes. It is recommended that buffers driving a backplane be grouped at the edge of the board and have their ground isolated and brought in on a separate pin from the backplane supply structure. This is also recommended for any drivers or buffers on a board that will be driving long, heavily loaded buses on the PC board. Breadboarding will also work with fewer problems if the guidelines above are followed. Thus, the use of jumper wires to provide the ground connection is not recommended. The preferred

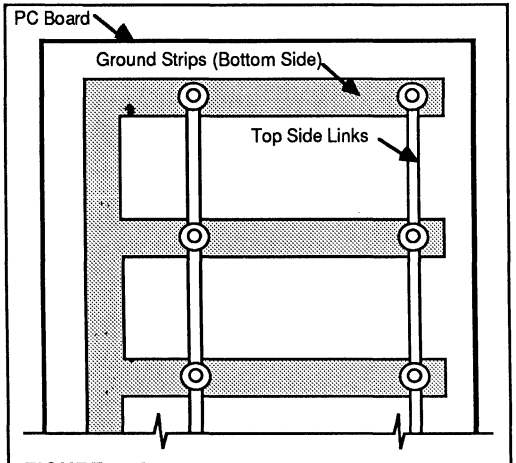


FIGURE 1.3
TOP SIDE LINKS

approach is to solder ground and supply pins. This would lead to realistic evaluations when using breadboards. For non-standard power pin-out, use copper braids or strips.

POWER DISTRIBUTION ELEMENTS

Transient noise voltages on the power distribution system of a circuit are caused by sudden changes in the current demand of the load. In high-speed digital circuits, the current and voltage changes can be assumed to be instantaneous for the purpose of calculating the demands on the power distribution system. Thus, assuming the current change is instantaneous, the resulting voltage change is a function of the characteristic impedance (Z_0) of the power distribution system:

$$Z_0 = \sqrt{(L_T/C_T)}$$

The instantaneous voltage change ΔV will then be:

$$\Delta V = \Delta I \cdot Z_0$$

From this equation it is obvious that the characteristic impedance of the power distribution system should be as low as possible to keep transient noise voltage to a minimum.

For comparison, consider the characteristic impedance of a copper power bus over a ground plane separated by a glass epoxy board. This is a typical power distribution system for two-sided PCB's. Figure 1.6 illustrates this setup. If 1 oz. copper (t = 0.0015") is used over a glass epoxy board (h = 0.0625", e_R = 4.7) and the power strip is 0.1" wide, then the characteristic impedance is:

$$Z_0 = [\ 87 / \sqrt{(4.7 + 1.41)}\ ] \cdot \ln(\ [5.98 \cdot 0.0625]/[0.8 \cdot 0.1 + 0.0015]\ ) \approx 54\Omega$$

An excellent method of providing a good power distribution system using only a two-sided copper PCB is to incorporate power distribution elements (PDEs) into the circuitry. The use of PDEs is strongly recommended by VTC, and results in electronic assemblies that have low noise levels on their power and ground lines because of the inherent noise suppression of the PDEs.

A PDE is composed of two flat conductors placed on top of each other and separated by a thin dielectric. This "sandwich" arrangement is then encapsulated with an insulative material. Contact pins are placed at specified intervals for easy access to the two conductors. Figure 1.4 shows a PDE. PDEs are available in either horizontal or vertical packages and

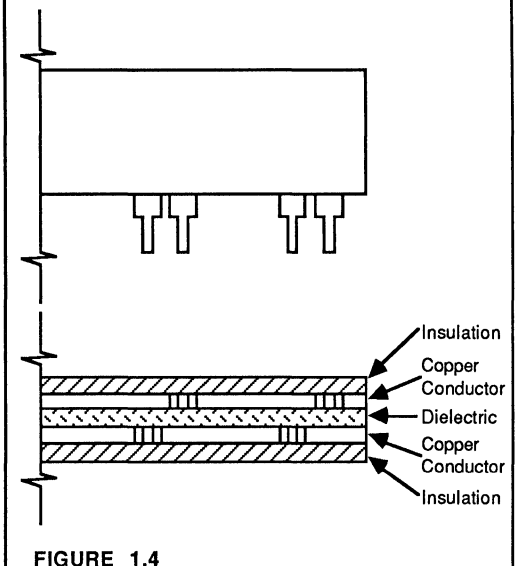
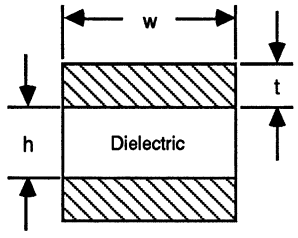


FIGURE 1.4
POWER DISTRIBUTION ELEMENT (PDE)



$$Z_0 = (377 / \sqrt{e_R}) \cdot (h / w)$$

FIGURE 1.5
PARALLEL FLAT CONDUCTORS

standard or custom lengths and pinout configurations from several manufacturers, such as Rogers Corporation in Tempe, Arizona.

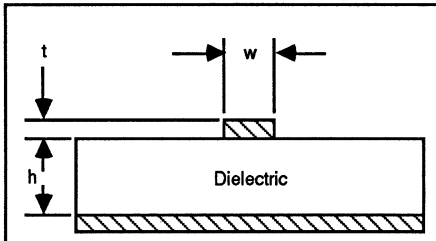
The characteristic impedance of a PDE can be calculated using the impedance equation for parallel flat conductors. An illustration of parallel flat conductors and their impedance equation is shown in Figure 1.5.

If the conductors in a PDE were 0.20" wide and separated by a 0.005" sheet of mylar ($e_R = 5.0$), then the characteristic impedance would be:

$$Z_0 = (377/\sqrt{5.0}) \cdot (0.005 / 0.20) = 4.2\Omega$$

The characteristic impedance of the PDE is more than ten times smaller than the characteristic impedance of the two-sided printed circuit board power distribution system mentioned in the preceding text. This illustrates the low impedance of a PDE, which makes it an excellent choice for power distribution.

To further reduce noise in a power distribution system using PDEs, use decoupling capacitors at each end of the PDEs. High-frequency ceramic disk capacitors with values of at least 0.01 µF are recommended. It is also a good idea to decouple each power supply voltage brought on to the board edge contacts.



$$Z_0 = \frac{87}{\sqrt{e_R + 1.41}} \cdot \ln\left[\frac{5.98h}{0.8w + t}\right]$$

FIGURE 1.6
FLAT CONDUCTOR OVER GROUND PLANE

The recommended decoupling elements are a 0.1µF hf ceramic-disk capacitor paralleling a 20 to 30 µF tantalum capacitor.

When using PDEs in a circuit, it is best to arrange the PDEs so that each PDE handles only one type of circuit function. Interface components must always have a separate PDE because of their high source/sink capability. It is also a good practice to keep interface components at the edge of the board. This prevents switching noise from affecting more than one section of logic.

For example, consider the 32-bit microprocessor board outlined in Figure 1.7. Separate PDEs should supply the memory, interface, and microprocessor sections, as shown in Figure 1.8.

To avoid couplings between PDEs, which would increase the noise level, each bus bar should have a separate ground and power connection, with both connected at the same end and as close to the edge contacts as possible. Each chip should receive its power and ground from one PDE. If power and ground come from separate PDEs, the chip will couple noise from one PDE to another. Layout of a board using these guidelines helps isolate and lower the switching noise found in high-speed digital circuits.

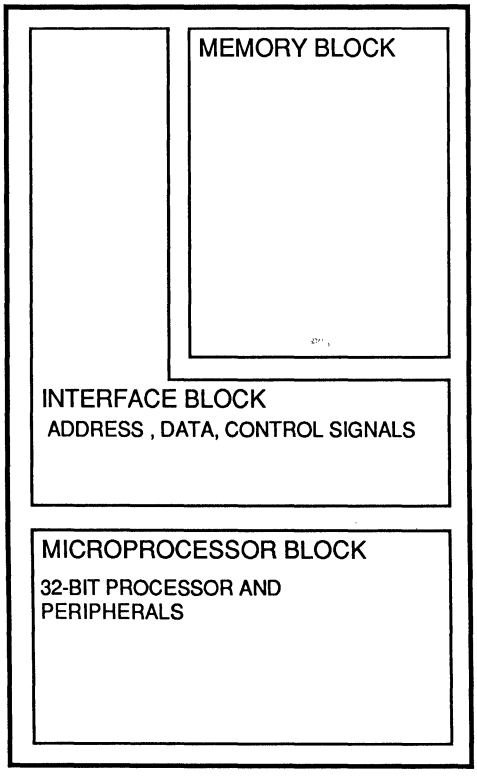


FIGURE 1.7
32-BIT MICROPROCESSOR BOARD

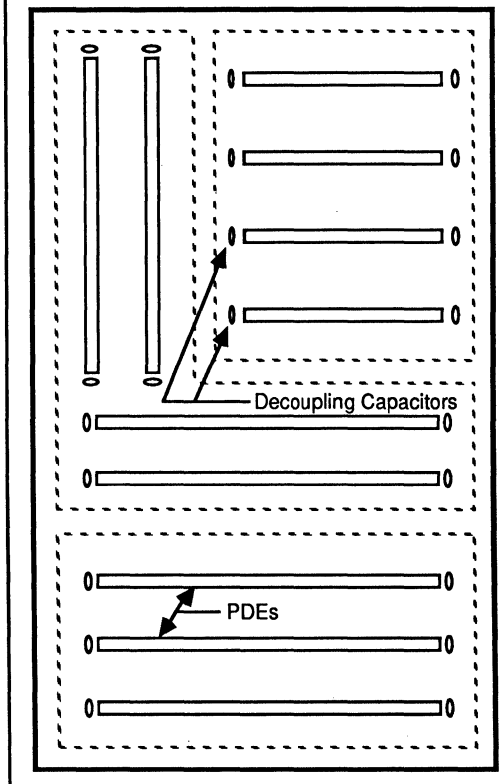


FIGURE 1.8
PDEs AND CAPACITORS ON BOARD

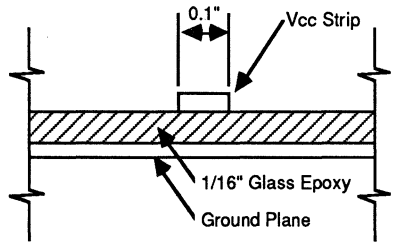


FIGURE 1.9A
50 Ω Vcc IMPEDANCE

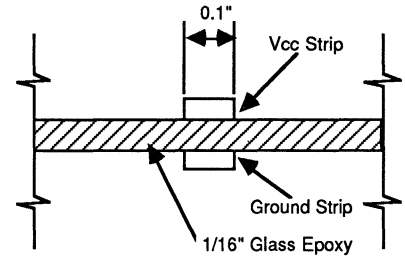


FIGURE 1.9C
68 Ω Vcc IMPEDANCE

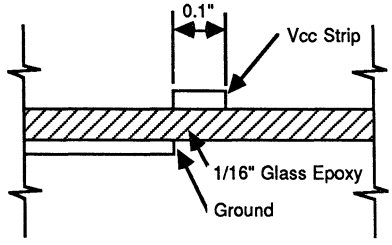


FIGURE 1.9B
100 Ω Vcc IMPEDANCE

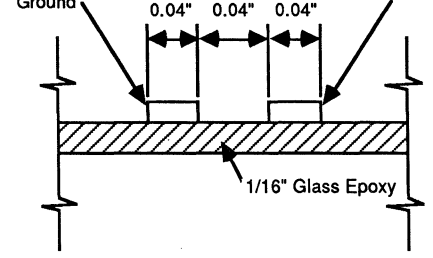


FIGURE 1.9D
90 Ω Vcc IMPEDANCE

NON-PDE SUPPLY INTERCONNECTION CRITERIA

It is now apparent that logic gates and bus drivers need extra current when they switch. This in turn will cause transients on the power supply buses. In many cases V_{CC} is distributed by V_{CC} strips, which exhibit a fairly high impedance to transient loads. Figures 1.9A-D show examples of some typical V_{CC} runs that might exist on the PC board and their corresponding impedance values.

In Figure 1.9A, the dynamic impedance of V_{CC} with respect to ground is 50 Ω, even though the V_{CC} trace width is generous and there is a complete ground plane. In B, the dynamic impedance doubles to 100 Ω. In C, the ground bus is also 0.1" wide and runs along under the V_{CC} bus. This exhibits a dynamic impedance of 68 Ω. In D, the trace widths and spacing are such that the traces can run under a DIP package, between two rows of pins. In this configuration, the dynamic impedance is 90Ω.

These typical dynamic impedances for copper-foil power distribution point out that unless a bypass capacitor is located near the IC, a sudden current demand due to an IC output switching will cause a momentary reduction in V_{CC}.

Consider the example illustrated in Figure 1.10A. It shows a buffer driving a line of 120 Ω. The buffer actually sees two 120 Ω lines in parallel, or a net dynamic load of 60 Ω. For this load impedance, the buffer output forces an initial low to high transition in about 3 ns. A 60 Ω load line on the I_{OH}-V_{OH}

characteristics shows a low to high step of approximately 3.0 V. Thus, a net change of 3.0 V into a 60 Ω load gives rise to a 50 mA current. If 10 outputs of the buffer IC switch simultaneously, the total current demand will be 0.5 A. This is a substantial current, requiring a bypass capacitor to supply it.

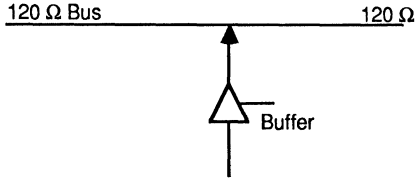


FIGURE 1.10A
EXAMPLE: BUFFER DRIVING LINE

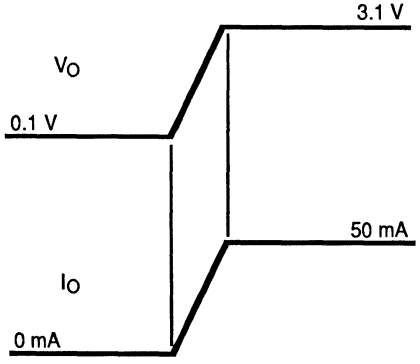


FIGURE 1.10B
BUFFER OUTPUT WAVEFORMS

CALCULATION OF BYPASS CAPACITOR VALUES

To evaluate the size of the bypass capacitor, we need to specify the tolerable V_{CC} drop. From circuit theory: $Q = C \cdot V$

$$I = C \cdot dV/dt = C \cdot \Delta V/\Delta t$$

I is current demand.

C is required capacitor value.

ΔV is tolerable V_{CC} drop.

Δt is the transition time of the signal.

In the above illustration, where 10 outputs switched simultaneously:

$\Delta t = 3$ ns
$\Delta V = 0.1$ V
$I = 0.5$ A

Hence: $C = (0.5\ A \cdot 3 \times 10^{-9})/0.1\ V$
$= 15 \times 10^{-9}$
$= 0.015\ \mu F$
$\approx 0.02\ \mu F$

These equations illustrate an approximate method of estimating the size of a bypass capacitor based on current demand, V_{CC} drop, and the length of time that a capacitor must supply the charge. The following guidelines should be adhered to for bypassing purposes:

- Use bypass capacitors, one for each buffer and transceiver IC. If PDEs are used, place bypass capacitors at each end of the PDEs instead of at each buffer or transceiver.
- Bypass capacitors should have low inductance, high-frequency qualities.
- RF quality capacitors are preferred.
- Use decoupling capacitors where V_{CC} comes onto the board. The recommended decoupling elements are a 0.1 μF ceramic disk capacitor in parallel with a 20 to 30 μF tantalum capacitor.
- Distribute capacitors evenly throughout the board.

SIGNAL PROPAGATION IN TRANSMISSION LINES

A transmission line is a signal path that exhibits a characteristic impedance. Transmission lines can be approximated by the lumped constant representation shown in Figure 1.11. For lossless lines $R_O = 0$. We will assume that the effect of R_O on Z_O is negligible.

With a ground plane present, three types of transmission line geometries are feasible: a) wire over ground, b) microstrip, and c) strip line. These geometries are shown in Figure 1.12. The characteristic impedance of each can be evaluated by the following formulas: (References 1-14)

a) Wire Over Ground

$$Z_O = [60/\sqrt{(E_r+1.41)}] \cdot \ln(4h/d)$$

b) Microstrip Line

$$Z_O = [87/\sqrt{(E_r+1.41)}] \cdot \ln[5.98h/(0.8w+t)]$$

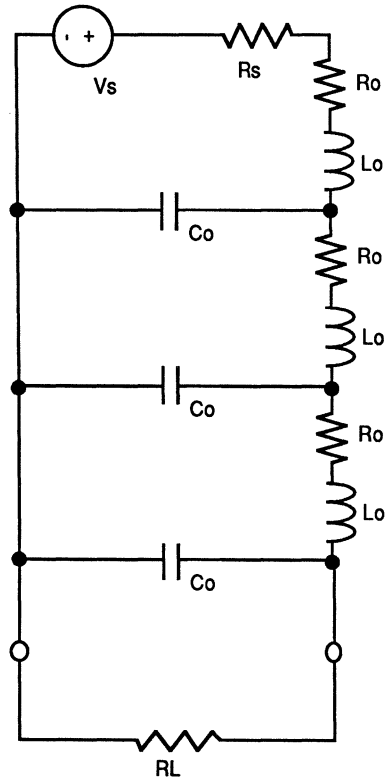


FIGURE 1.11
TRANSMISSION LINE

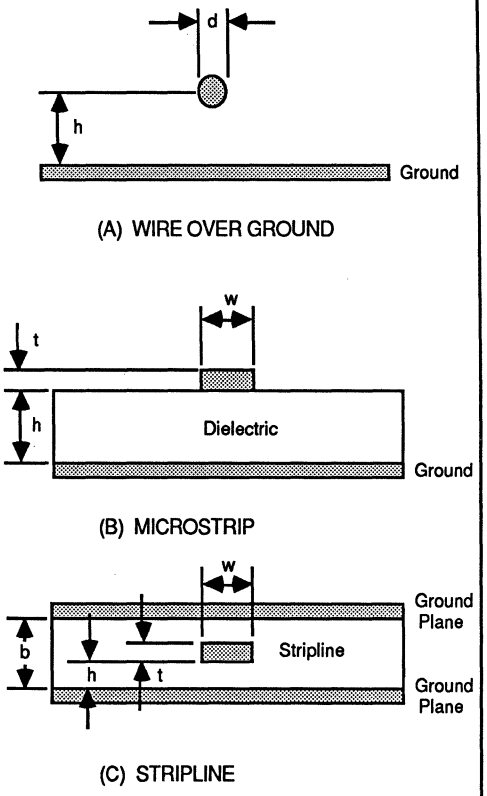


FIGURE 1.12
TRANSMISSION LINE GEOMETRIES

c) Strip Line

$Z_O = (60/\sqrt{E_r})\cdot\ln[4b/(0.67\pi w\cdot(0.8+(t/w)))]$

(E_r is the dielectric constant)

REFLECTIONS AND LOADING

Consider a driving gate as shown in Figure 1.13, driving onto a transmission line of characteristic impedance Z_O. When the output of the driving gate changes state, the voltage at point A is a function of the voltage swing, output impedance, and line impedance.

$$V_A(t) = V_{IN}\cdot[Z_O/(R_O+Z_O)]$$

R_O is the internal resistance of the driver.

Some time later, this voltage step reaches point B, where it may be reflected. The reflection coefficient f_L depends on the load at the other end of the line.

$$f_L = (R_L-Z_O)/(R_L+Z_O)$$

A reflection will always occur, except when $R_L = Z_O$. The reflection will continue to bounce back and forth on the line, getting successively smaller in amplitude. The result is ringing on the signal line.

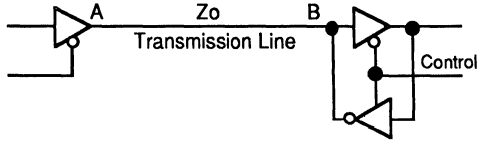


FIGURE 1.13
GATE DRIVING TRANSMISSION LINE

Rise time effects can be understood by considering the delay time of the line. If the line length 'l' is sufficiently short, the first reflections are seen at the sending end of the line while the driver is still changing state. The reflections are hidden by the rising edge of the pulse, and ringing is reduced. To limit undershoot to about 12% of the logic swing, the maximum open line length permitted would be:

$$L_{MAX} = t_r/2t_{pd}$$

t_r is the rise time of the driving gate.

t_{pd} is the propagation delay per unit line length (ns/ft).

For the microstrip line, the propagation delay of the line may be calculated by:

$$t_{pd} = 1.017\sqrt{(0.475E_r+0.67)} \text{ ns/ft.}$$

E_r is the dielectric constant of the board.

For fiberglass epoxy boards $E_r \approx 5.0$, hence t_{pd} is approximately 1.75 ns/ft.

REFLECTIONS AND LOADING FOR VARIOUS TERMINATIONS

The previous discussion assumed a line without any termination. If a termination resistor is used, the reflection value will be reduced, as given by the reflection coefficient:

$$f_L = (R_L-Z_O)/(R_L+Z_O)$$

Figure 1.14 shows a scheme for terminating each end of a data bus to limit reflections and establish a high level when all buffer outputs are in the high-Z state. Table 1.1 shows the percent reflection and the quiescent I_{OL} load on a buffer for various values of R_1.

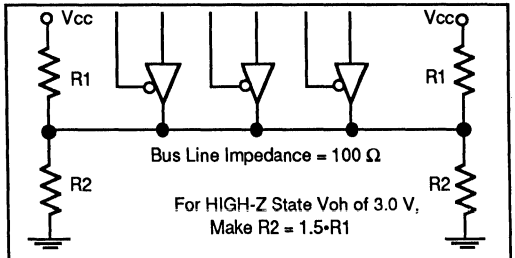


FIGURE 1.14 REFLECTIONS & LOADING FOR VARIOUS TERMINATIONS

R_2 is set at 1.5 times R_1, and I_{OL} is the load current due to the termination resistors.

TABLE 1.1

R_1 Ω	% Reflection	I_{OL} Load mA (Each End)
∞	100	0
510	51	8
330	33	13
240	18	17
180	4	23
160	-2	26

Until now, the effect of loading on the terminated line has been ignored. Fan-out along a signal line lowers the effective characteristic impedance. The effect of this is given by the equation:

$$Z_O' = Z_O/\sqrt{[1+(C_D/C_O \cdot l)]}$$

Z_O' is the loaded line impedance.

Z_O is the unloaded line impedance.

C_D is the total distributed capacitance due to loads.

C_O is the intrinsic capacitance per unit length.

l is the length of the line.

This shows that, in a bus or backplane environment, it is very difficult to prevent reflections by various line terminations if the number of loads are likely to change over the life of the system.

Loading also increases delay in the transmission line. Propagation delay of a loaded line may be calculated from the following equation:

$$t_{pd}' = t_{pd}\sqrt{[1+(C_D/C_O \cdot l)]}$$

t_{pd}' is the propagation delay of the loaded line.
t_{pd} is the propagation delay of the unloaded line.
C_D is the total distributed capacitance due to loads.
C_O is the intrinsic capacitance per unit length.
l is the length of the line.

Increased capacitive loading also slows the rise time of the signal because the driver must drive a larger load. All these factors should be considered when evaluating the signal propagation along a transmission line.

REFLECTION DIAGRAMS

A reflection diagram is a graphic technique used to evaluate the effect of signal propagation and reflection over a transmission line. The graph has both the output-low and output-high (I-V) characteristics of the driver. The dashed line passing through the 3V point on the voltage axis is the I-V characteristic of the termination in parallel with the driver gate. Figure 1.15 and 1.16 show the reflection diagrams for the V54/74ACT family of drivers.

To make a low-to-high transition reflection diagram, as shown in Figure 1.15, start by drawing a -120 Ω (or the impedance of the driven line) line from point 1, the quiescent low condition. The intercept with the I_{OH}:V_{OH} characteristic, point 2, is the first step at the driver output. From point 2, draw a +120 Ω line to the termination line, intersecting at point 3. From point 3, draw a -120 Ω line, intersecting the I_{OH}:V_{OH} characteristic at point 4. Successive intercepts converge in the quiescent high condition. The voltage vs. time graphs illustrate the voltage changes at either end of the line. The changes at the receiver and driver are separated by a time T equal to the line delay of the line.

Figure 1.16 shows the high-to-low transition diagram. These transitions can be evaluated graphically while maintaining an acceptable level of accuracy. The mathematical calculations tend to be tedious and fail to reveal the physical mechanisms taking place.

CROSSTALK

Crosstalk is caused by capacitive and inductive coupling of signals along parallel lines. Figure 1.17A shows an electrical equivalent circuit of two parallel lines. A pulse propagating down line CD is capacitively coupled into line AB. The effect of the coupled pulse is lumped at point X. The coupled voltage on line AB causes current I_C to flow from the point of coupling to both ends.

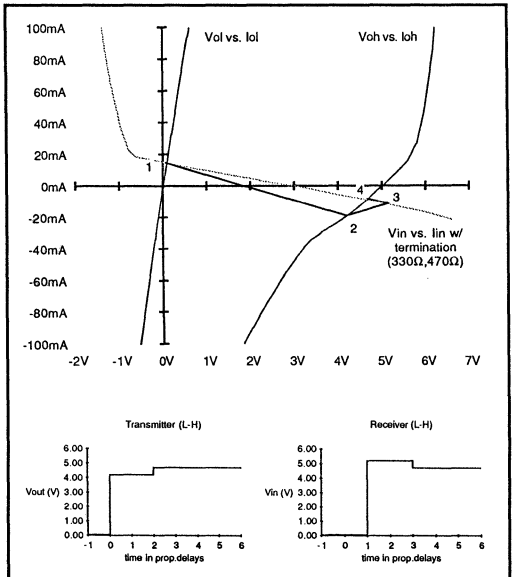


FIGURE 1.15
GATE DRIVING 120 Ω LINE REFLECTION DIAGRAM LOW-TO-HIGH TRANSITION

Current in the direction of A is called "backward crosstalk" and current in the direction of B is called "forward crosstalk." Similar coupling is caused by the mutual inductance of the lines, this current couples in the direction of "backward crosstalk."

Because the line is not terminated, these signals also go through reflections at A, and after $2t_d$'s reach B. The crosstalk amplitude can be calculated by the following equation: (Reference 11)

$$V(x_1,t) = k_f \cdot x \cdot d/dt\{V_{IN}[t-T_D(x/l)]+k_b[V_{IN}(t-T_D(x/l))-V_{IN}(t-2T_D+T_D(x/l))]\}$$

k_f = forward crosstalk coefficient = $-1/2[(L_M/Z_O)-C_M \cdot Z_O]$
k_b = backward crosstalk coefficient = $(l/4T_D)[(L_M/Z_O)+C_M \cdot Z_O]$
L_M = mutual line inductance per unit length.
C_M = mutual line capacitance per unit length.
Z_O = characteristic line impedance.

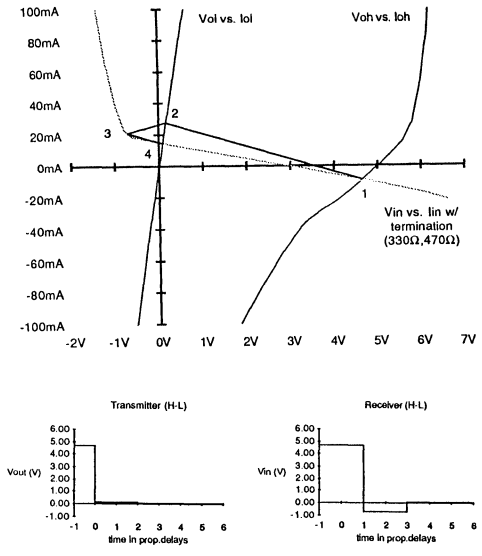


FIGURE 1.16
GATE DRIVING 120 Ω LINE REFLECTION DIAGRAM HIGH-TO-LOW TRANSITION

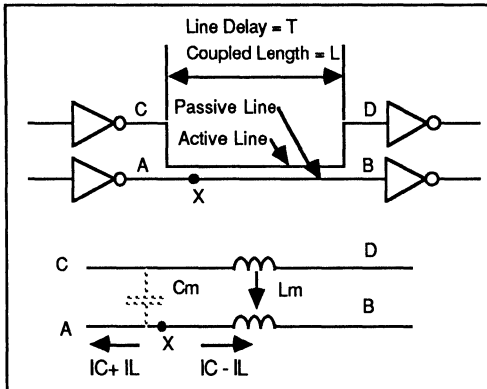


FIGURE 1.17A
CROSSTALK COUPLING IN PARALLEL LINES - ELECTRICAL MODEL

l = line length.
x = an arbitrary point along line.
T_D = delay through the line.

The amplitude of crosstalk is a function of line length for short lines. Short lines are defined as lines that have a propagation delay less than one-half the input rise time. The width of the crosstalk pulse will always be a function of the length of the line. The rise and fall times of the crosstalk pulse on line AB are the same as the rise time of the signal propagating down line CD. Figure 1.17B illustrates a crosstalk (noise) pulse that would be seen at point B for various line delays.

Termination reduces the amplitude of crosstalk signals. Even partial termination will reduce the amplitude of a signal appearing at the end of the line. Table 1.2 illustrates this point. A terminating resistor twice the value of the line impedance reduces the noise amplitude by one-third. A matched termination cuts the noise amplitude in half, relative to the nonterminated line.

TABLE 1.2

Noise Amplitude	Termination R, in terms of Z
100%	R = 0
67%	R = 2•Z
60%	R = 1.5•Z
50%	R = 1•Z

General recommendations for crosstalk reduction are:

a) Maximize the spacing between signal lines, which reduces coupling inductance and capacitance.
b) Minimize spacing between signal line and ground.
c) Wrap a wire around the talker to confine its field, or around the listener to shield it.
d) Use split-resistor termination.
e) Locate a ground trace next to the active wires.
f) Make every other conductor in a flat cable a ground.

For multilayer crosstalk reduction, position signal lines perpendicular to each other in adjacent planes and use power planes as shields between pairs of signal planes.

SUMMARY AND CONCLUSION

The preceding text has been an overview of the problems and issues common to most system design environments. General design guidelines with numerical illustrations and formulas were provided. These guidelines are useful tools for analysis of specific

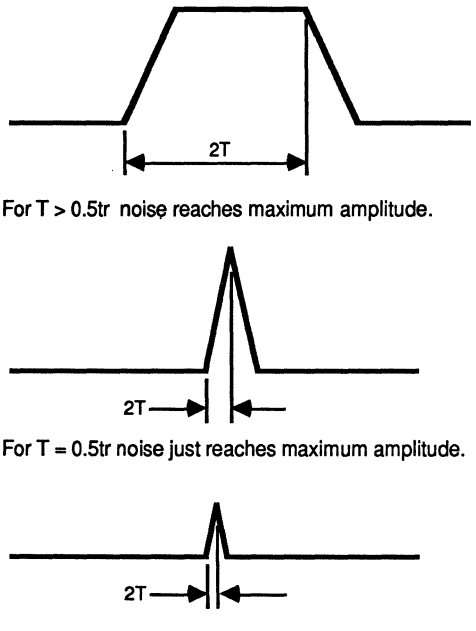


FIGURE 1.17B
CROSSTALK COUPLING IN PARALLEL LINES - NOISE PULSES AT POINT B

design issues the system designer will encounter. References are provided for further information.

The VTC interface buffer, driver, latch, and transceiver families offer short delay and setup times, high drive capability (fan-out), low power dissipation, low input capacitance, and a low input current requirement for modern high-performance TTL systems environments.

Improved performance, fast edge rates, and high drive capability means that care must be exercised in the design of the layout environment of both signal paths and the grounding system. Every line behaves like a transmission line, so careful consideration should be given to the relationships between loading, termination, noise margins, and ringing.

The power distribution network could require PDEs, heavier bussing, a grid approach, or a separate ground plane, depending on the driver layout and overall current densities. The device capability to sink 48 mA per bit and the charging/discharging of bus lines can cause large ground currents. Supply decoupling should be located close to the actual drivers to provide the current required for the charging of bus lines.

The following are general suggestions to minimize grounding and noise problems:

Minimize Crosstalk:
- Use power distribution elements.
- Use topside links for the ground grid.
- Use a dedicated ground plane in multilayer boards.
- Make every other wire in a flat cable a ground wire.
- Minimize spacing between a signal line and ground line.
- Maximize spacing between signal lines.
- If possible, use a four layer board with a dedicated ground and supply plane.

Increase Decoupling:
- Use high-frequency capacitors of the tantalum and ceramic types.
- Provide a bypass capacitor close to the buffer package.
- Use a dedicated supply plane if the system warrants it.

If the system has mostly CMOS or NMOS components, the current requirements of the system may not be very high. In this case, dedicated supply planes may not be necessary; decoupling capacitors with a good ground grid might do the job. Analyze your component's requirement and follow the relevant guidelines from above in the general layout of your system.

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NOTES

DESIGN CASE

INTRODUCTION

A bus line is designed to interconnect several points in a system with a common data path. Normally, drivers and receivers are located at each end of the line, so data can flow in either direction. Additional drivers and receivers often connect to the bus at various points along the line, requiring that the driver be capable of sending a signal in both directions.

Due to this criteria, a high-speed bus driver should be capable of operating into a load equal to one-half the characteristic line impedance. At any given time, only one driver on a bus can send data. In this section, single-ended buses will be considered with an illustrated example of the VMEbus™.

HIGH-SPEED REQUIREMENTS

A sample specification of the VMEbus™'s electrical requirements is discussed and analyzed.

Generally, high-speed single-ended buses can have a high fan-out density and use TTL/CMOS/ ECL type circuits as drivers and receivers. The signal type and voltage levels are determined by system requirements. The VMEbus™ specifies typical TTL voltage signals.

All VMEbus™ signals are limited to positive levels between 0 and 5 volts. The signal levels are:

a) 0.0 V ≤ Driver low output level (V_{OL}) ≤ 0.6V.

b) 0.0 V ≤ Receiver low input level (V_{IL}) ≤ 0.8V.

c) 2.4 V ≤ Driver high output level (V_{OH}) ≤ 5.0V.

d) 2.0 V ≤ Receiver high input level (V_{IH}) ≤ 5.0V.

Figure 2.1 gives a simple representation of these levels. The V54/74ACT series bus interface circuit family meets the specifications in Figure 2.1.

VMEBUS™ SPECIFICATIONS

The VMEbus™ calls out the electrical specifications for standard 3-state signal lines. This class of signals consists of address lines A00-A31, data lines D00-D31, and transfer signals Am0-Am5. The following paragraph lists in detail the voltage and current specification for this class of lines.

DRIVER CHARACTERISTICS FOR STANDARD 3-STATE CLASS LINES

a) Low state output current: $I_{OL} \geq 48$ mA.

b) Low state output voltage: $V_{OL} \leq 0.6$ V at I_{OL} = 48 mA.

c) High state output current: $I_{OH} \geq -3$ mA.

d) High state output voltage: $V_{OH} \geq 2.4$ V at I_{OH} = -3 mA.

e) High level output current: $I_{OZH} \leq 100\ \mu A$ at V_O = 2.7 V 3-state off.

f) Low level output current: $I_{OZL} \leq -100\ \mu A$ at V_O = 0.6 V 3-state off.

g) Short circuit current: I_{OS} minimum -25 mA, maximum -225 mA, at 0 V.

h) Output capacitance: Driver, $C_{OUT} \leq 15$ pF Transceiver, $C_{BUS} \leq 18$ pF.

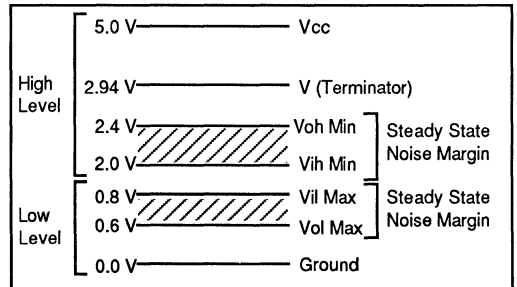


FIGURE 2.1 VMEBUS™ SIGNAL LEVELS

The total capacitive load presented by a VME module to any of these lines shall not exceed 20 pF.

All bus receivers should have an input diode clamp that prevents negative voltage excursions from going below -1.5 V. The other requirements for the VMEbus™ signals are given in the following paragraph.

Receiver circuits for signals should provide the following electrical characteristics as a maximum:

a) Low level input current: $I_{IL} \leq -600\ \mu A$ at V_{IL} = 0.5V.

b) High level input current: $I_{IH} \leq 50\ \mu A$ at V_{IH} = 2.4V.

c) Positive or negative going threshold voltages: 0.8 V ≤ V_T ≤ 2.0 V.

(Receivers on these lines are recommended, but *not required*, to have hysteresis inputs)

d) Input capacitance: Receiver, $C_{IN} \leq 7$ pF. Transceiver, $C_{BUS} \leq 18$ pF.

The V74/54ACT interface family meets or exceeds these specifications. The input currents are in the 1μA range. The quiescent supply currents are small, in the 25 μA range. The V54/74ACT series has a high current sink/source capability for low and high states. Refer to the DC characteristics table for the detailed specification numbers.

BACKPLANE SIGNAL LINE INTERCONNECTIONS

The VMEbus™ is an asynchronous, high-speed bus intended for high-performance systems. The backplane signals must be treated as transmission lines. These backplanes are characterized by the following features:

- Maximum signal line length is 19".
- Maximum number of slots (loads) is 20.
- Termination networks at each end of the bus.

Thus, the fan-out is limited to a maximum of 20 loads. The VMEbus™ can be modeled as a transmission line with distributed loads. The backplane line has an intrinsic characteristic impedance Z_O. The fan-out along a signal line lowers the effective characteristic impedance to Z_O', as given by the equation:

$$Z_O' = Z_O/\{\sqrt{[1+(C_D/C_O \cdot l)]}\} \quad \text{(for strip lines)}$$

Z_O is the unloaded line impedance.
C_D is the total distributed capacitance.
C_O is the line intrinsic capacitance per unit length.
l is the line length.

TRANSMISSION LINE CHARACTERISTICS OF SOME INTERCONNECT MEDIA

Figures 2.2 through 2.5 show various transmission line types that can be used for interconnecting high-speed logic systems. A brief description and general impedance estimation formulas are given in the following section. This is included to give a flavor of the information and data needed to do a typical design of bus driver circuits. The description is by no means complete and comprehensive, but is used to illustrate the procedure that should be followed for the actual design.

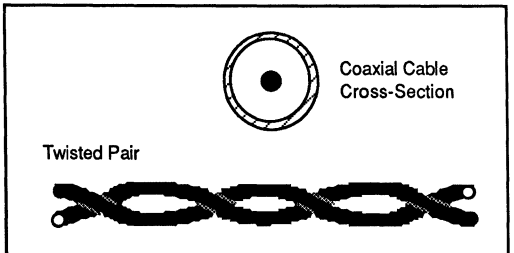


FIGURE 2.2
COAXIAL CABLE, TWISTED PAIR

1) COAXIAL CABLE, TWISTED PAIR

Figure 2.2 shows a coaxial cable and a twisted pair. Coaxial cable is available with characteristic impedances of 50, 75, 100, and 125 ohms. The twisted pair can be made from standard hookup wire. A twisted pair has a characteristic impedance of approximately 110 Ω. This wire type can be used for long line lengths located in the backplane.

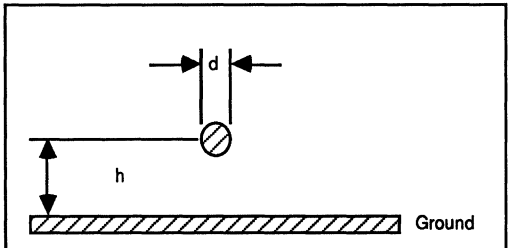


FIGURE 2.3 WIRE OVER GROUND

2) WIRE OVER GROUND

Figure 2.3 shows the cross-section of a wire over a ground. It can be used for backplane wiring and general breadboarding. The characteristic impedance of this wire is:

$$Z_O = (60/\sqrt{E_r}) \cdot \ln(4h/d)$$

E_r is the dielectric constant of the medium.
d is the diameter of the wire.
h is the distance from the ground plane.

3) MICROSTRIP LINES

Figure 2.4 shows the microstrip line. The characteristic impedance Z_O of a microstrip line is:

$$Z_O = [87/\sqrt{(E_r+1.41)}] \cdot \ln[5.98h/(0.8w+t)]$$

E_r is the dielectric constant of the board.
h is the thickness of the dielectric.
t is the thickness of the line.
w is the line width.

The above equation is fairly accurate for ratios of width to thickness between 0.1 and 3.0, and dielectric constants between 1 and 12.

Figures 2.5 and 2.6 show curves for microstrip impedance and capacitance per foot as a function of

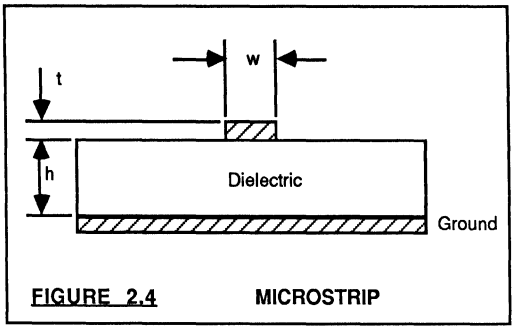


FIGURE 2.4 MICROSTRIP

line width and spacing. The inductance per foot can be calculated using the following formula:

$$L_O = Z_O^2 \cdot C_O$$

C_O is capacitance per foot.

Z_O is the characteristic impedance.

The propagation delay of the line can be calculated by using the following formula:

$$t_{PD} = 1.017\sqrt{[0.475E_r+0.67]} \text{ ns/ft.}$$

For G-10 fiberglass epoxy boards ($E_r = 5.0$) the propagation delay of the microstrip line is 1.77 ns/ft.

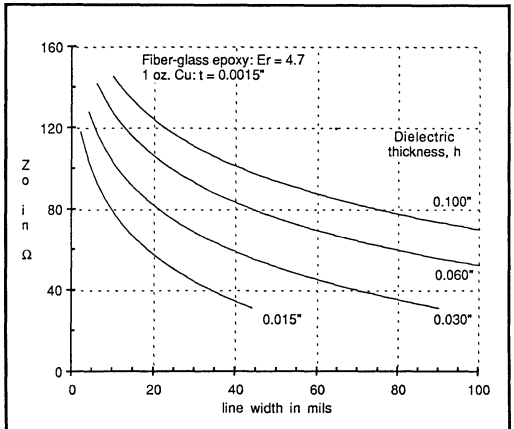


FIGURE 2.5
CHARACTERISTIC IMPEDANCE FOR MICROSTRIP LINES

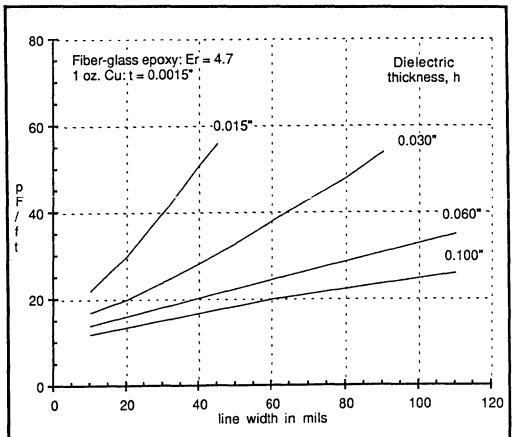


FIGURE 2.6
CAPACITANCE PER UNIT LENGTH FOR MICROSTRIP LINES

4) STRIPLINE

A strip line consists of a copper strip centered in a dielectric medium between two conducting planes, as shown in Figure 2.7. The characteristic impedance of a stripline, as given by theory, is:

$$Z_O = [60/\sqrt{E_r}] \cdot \ln\{4b/[0.67\pi w(0.8+(t/w))]\}$$

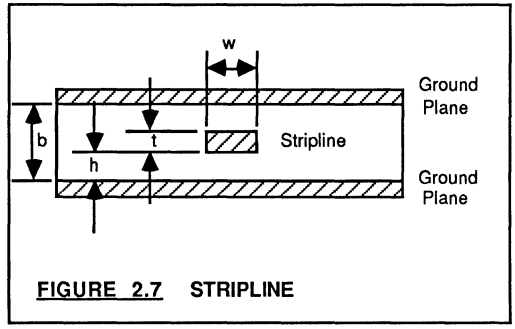


FIGURE 2.7 STRIPLINE

Figures 2.8 and 2.9 show values of Z_O and capacitance for various stripline widths and thicknesses. The inductance can be found using the formula:

$$L_O = Z_O^2 \cdot C_O$$

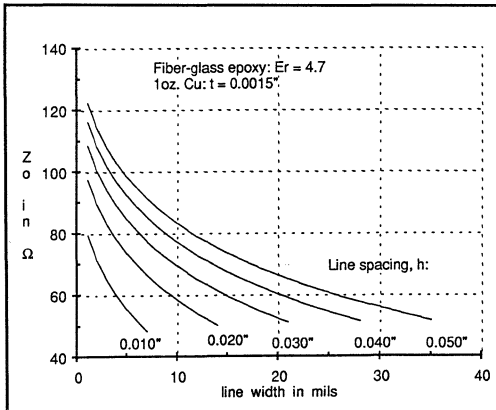


FIGURE 2.8
CHARACTERISTIC IMPEDANCE FOR STRIP LINES

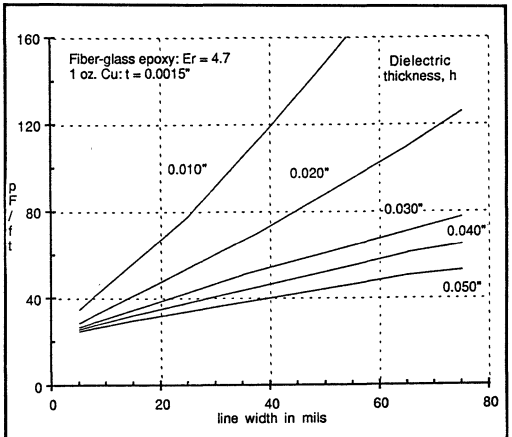


FIGURE 2.9
CAPACITANCE PER UNIT LENGTH FOR STRIP LINES

The propagation delay is given by the relation:

$$t_{PD} = 1.017\sqrt{E_r}\ \text{ns/ft.}$$

The previous text summarizes the various types of interconnect technologies. The actual numbers can be found by measurements or from the PC board vendors. These numbers will serve as a guide to set up and work through a typical design problem. For further technical information, refer to the reference section at the end of section 1, "System Design Considerations."

DESIGN RULES

The VMEbus™ specification recommends the following design rules for designing VME boards:

1) Circuit traces from the DIN connectors to the on-board circuitry shall not have a length greater than 2".
2) No more than one driver and one receiver (or one transceiver) may be connected to any VMEbus™ signal line.
3) A standard termination should be used on each end of all VMEbus™ signal lines, as shown in Figure 2.10. A Thevenin equivalent for each termination is also shown.

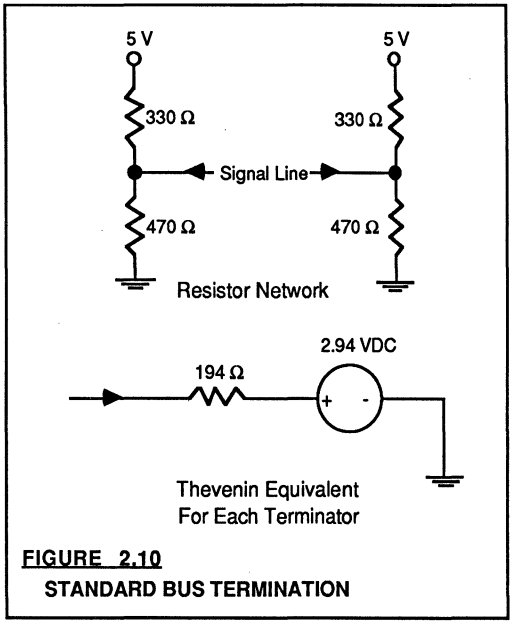


FIGURE 2.10
STANDARD BUS TERMINATION

DESIGN CALCULATIONS

The microstrip line backplane will be used for the bus lines. Also, the intrinsic impedance must be as high as possible, because Z_O will decrease due to loading.

Let us select: Z_O = 120 Ω and w = 25 mils, then C_O = 18 pF/ft or 1.5 pF/inch.

$$Z_O' = Z_O/\{\sqrt{[1+(20/1.5)]}\}$$

The bus is 20" long and has at most 20 pF of load on each connector. Hence, under fully-loaded conditions:

$$Z_O' = 120/\sqrt{[1+(20/1.5)]} = 31.7\ \Omega$$

The propagation delay time of a loaded line may be calculated from the following equation: $t_{PD}' = t_{PD}\sqrt{[1+(C_D/C_O)]}$

The unloaded microstrip line has a propagation delay of 1.77 ns/ft.

So: $t_{PD} = (20/12)\cdot 1.77 = 2.95$ ns

And: $t_{PD}' = 2.95\sqrt{[1+(20/1.5)]} = 11.2$ ns.

Thus, a bus line that is fully-loaded with boards, with each board presenting a load as dictated by design rules of no more than 20pF, has a propagation delay of 11.2 ns.

The total capacitive load presented by the bus line is approximately 20•(20) = 400 pF. The driver circuits of the V54/74ACT family will have a typical rise time of 10ns to drive this type of load. Thus, if the bus is driven from one end, the total propagation time for a round trip will be $2\cdot t_{PD}' = 2\cdot 11.2 = 22.4$ ns. This implies that $t_{RISE} < 2\cdot t_{PD}'$ and the reflected waveforms will cause a certain amount of ringing. This situation requires the use of termination networks. Reflection diagrams are drawn in Figures 2.11A and 2.11B to show the various voltage and current steps for low-to-high and high-to-low transitions.

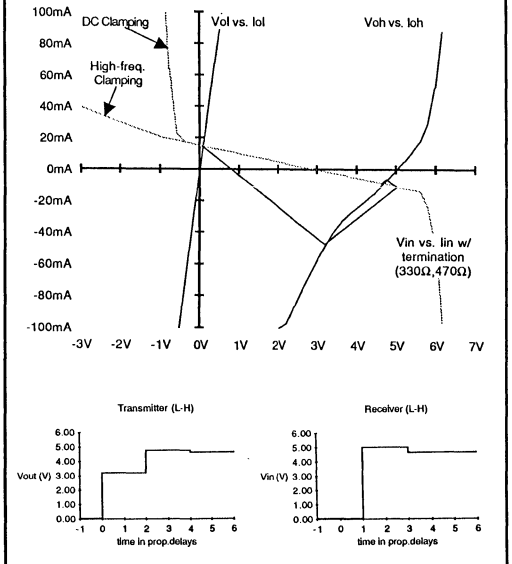


FIGURE 2.11A
LOW-TO-HIGH REFLECTION DIAGRAM

POWER DISSIPATION ADVANTAGE OF ACT PARTS OVER ALS PARTS FOR VMEBUS™ IMPLEMENTATION

Consider a VMEbus™ with transceivers driving the address lines A00-A31, data lines D00-D31, and transfer signals Am0-Am5. This would require nine part types for the full VMEbus™ at each interface. The bus is 20" long and has 20 other transceivers connected to it.

Power Dissipation Calculation: CMOS parts

From the specification sheet for 245s, the typical output capacitance of each output is known to be 10 pF. The total capacitance on the bus can be calculated as (number of drivers)•(capacitance of each driver) = (20)•(10pF) = 200pF. The capacitance of the 20" bus itself is 20 pF, so the total capacitive load is 20 pF + 200 pF = 220 pF.

Assuming a 1 MHz switching rate and V_{CC} = 5V, the power dissipation per line can be found:

$$P = V_{CC}^2 \cdot f \cdot C_L$$

$$= (25)\cdot(1.0 \times 10^6)\cdot(220 \times 10^{-12})$$

$$\approx 0.006 \text{ Watts}$$

Therefore, each 245 component will use 8•0.008 = 0.048 watts. For nine parts at each node, the power dissipation for the bus is 9•0.048W = 0.432 watts for the complete backplane. The components that are not driving the bus do not dissipate any significant power, having a typical quiescent current of 10μA. Therefore, the total power dissipation is 0.576 watts/MHz.

Power Dissipation Calculation: ALS parts.

From specifications for the ALS 245 parts we find that I_{CC} of the disabled parts = 63mA. The system has a total of 180 parts - 20 nodes times 9 per node. Therefore the total quiescent power dissipation = 63mA

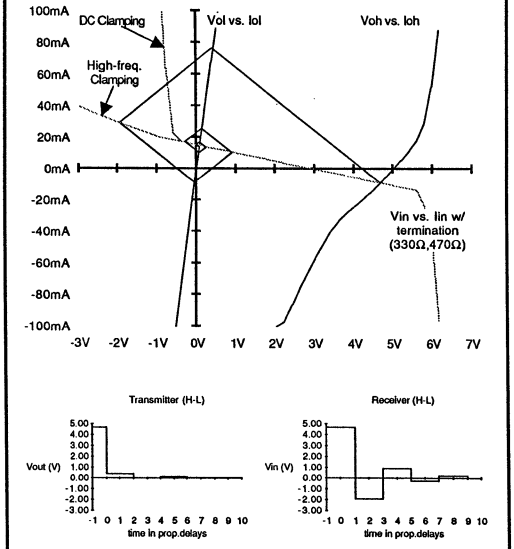


FIGURE 2.11B

HIGH-TO-LOW REFLECTION DIAGRAM

x 180 parts x 5V = 56.7 watts. This does not include the extra power dissipated due to switching. Figure 2.12 compares the ALS and ACT power dissipations for this system over frequency. The CMOS implementation dissipates 0.576 W/MHz and is linear, while the ALS implementation has a quiescent DC power dissipation of 56.7 watts. This will increase over frequency similar to the CMOS implementation.

The preceding illustration demonstrates the advantage of the V54/74ACT series of parts over the bipolar parts in an actual system environment.

CONCLUSION

In summary, a short description of a VMEbus™ specification was given, followed by calculations to illustrate how the V54/74ACT series of bus drivers/line transceivers would be used to drive the bus interface to the VMEbus™. The example used the fully-loaded and configured 20 slot VMEbus™. This is the worst-case situation that would be encountered. In a real-life situation, it may not be completely loaded. This would improve the rise/fall times, but also result in higher ringing. The bus should be as per the VME specification. Follow the general design criteria as

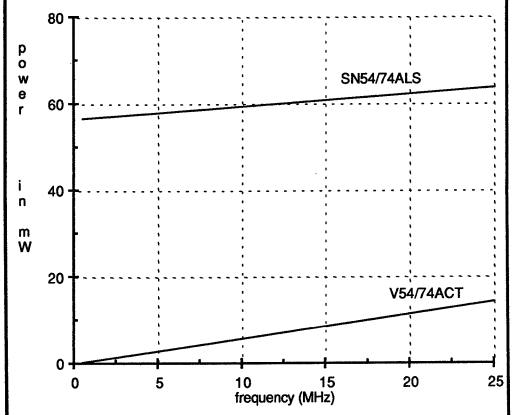


FIGURE 2.12

POWER DISSIPATION FOR ALS AND ACT SYSTEMS OVER FREQUENCY

outlined in section 1, "System Design Considerations," to do a complete design of physical and electrical aspects of the system.

This section is a simple illustration of the complex task of designing bus interface circuits in a system environment. No timing, speed, performance, or power objectives were considered. The section illustrates that the V54/74ACT family of parts meets the general electrical specifications of the VMEbus™ specification and can be used to design a bus interface. The power dissipation illustration is a case of the overwhelming superiority of the V54/74ACT interface family over ALS and other TTL families.

REFERENCES

1) Kaupp, H.R.,"Characteristics of Microstrip Transmission Lines," IEEE Transactions on Electronic Computers, Vol.EC-16, No.2, April 1967, pp.185-193.

2) VMEbus™ Specification Manual, Rev.B, Aug 1982, Motorola Inc.

NOTES

POWER DISSIPATION FOR THE V54/74ACT FAMILY

INTRODUCTION

Extremely low power dissipation with high-speed, high drive capability is a unique feature of the V54/74ACT family of interface components. VTC's ACT series of parts draws three to five orders of magnitude less power than the equivalent ALS parts in the quiescent state. The input current is also less (several orders of magnitude) than that of the equivalent ALS parts, which the ACT series was designed to replace.

The main component of power consumed during switching is dynamic in nature. Dynamic power consumption is due to load capacitance, charging and discharging of internal capacitance, and, to a lesser extent, current spiking during switching.

This section will describe the various causes of power consumption and compare the power dissipation of the V54/74ACT and SN74ALS families of bus interface parts.

QUIESCENT POWER CONSUMPTION

The V54/74ACT family is designed using advanced CMOS technology. The complementary nature of this technology prevents any direct current path to form between V_{CC} and ground, under stable conditions.

Figure 3.1 shows a simple inverter in a steady state. Either the P or the N transistor is off, breaking any direct path between V_{CC} and ground. However, a small amount of leakage current will usually flow across the reverse-biased diode junctions of the inverter. This reverse-biased leakage current is a function of the thermally generated minority carriers. A change in temperature will cause a change in this current. This reverse-biased leakage current is also known as the quiescent supply current, I_{CC}. Table 3.1 lists typical values of quiescent current for a V74ACT240 buffer over operating temperature.

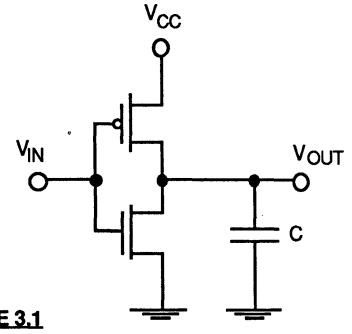


FIGURE 3.1
SIMPLE INVERTER IN STEADY STATE

Each device specification contains the quiescent supply current values for that device. This is a direct current that flows from V_{CC} to ground when the device is in its quiescent state:

All inputs = V_{CC} or ground.
All outputs tristate and open.

TABLE 3.1
SUPPLY CURRENT I_{CC} FOR V74ACT240
V_{CC} = 5 V

Temperature	I_{CC}	Units
-55°C	0.01	µA
25°C	0.20	µA
125°C	7.00	µA

The value of this current is a function of input voltage and is higher when the inputs are not at V_{CC} or ground. The higher quiescent current is caused by the input transistors partially conducting; thus, it is important that in a system environment, the input voltages stay as close as possible to V_{CC} or ground. This results in minimal current flow and power dissipation.

Figure 3.2 shows the typical quiescent current, I_{CC}, for various levels of input voltage. To obtain the quiescent power consumption, simply multiply I_{CC} by the supply voltage, typically 5 volts.

$$P_{DC} = I_{CC} \cdot V_{CC}$$

For V74ACT interface parts, the typical power dissipation is: 5 V • 10 µA = 50 µW

DYNAMIC POWER CONSUMPTION

As mentioned earlier, the main components of the power dissipation in this family of interface parts are dynamic in nature. These dynamic components can be attributed to the following causes:

1) Current flow during switching or switching currents.
2) Internal currents due to capacitive switching.
3) Dissipation due to external load capacitance.

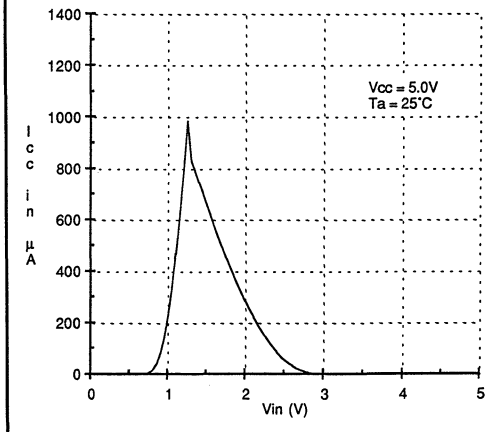


FIGURE 3.2
TYPICAL QUIESCENT CURRENT

1) SWITCHING CURRENT:

When the inputs to a gate make a transition, both P and N-channel transistors go through a state where one is turning on while the other is turning off. The length and duration of this state is dependent on the rise and fall times of the inputs. Figure 3.3 is a simplified diagram to show the electrical equivalent model of an inverter in transition. The partially on/off devices behave as resistors, allowing a current to flow from V_{CC} to ground.

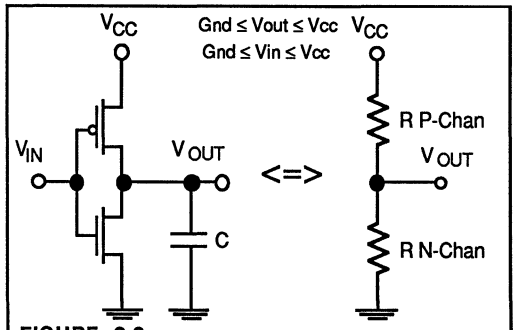


FIGURE 3.3
MODEL OF AN INVERTER IN TRANSITION

In a typical system environment the inputs rise or fall quickly, within 15 ns. In this situation, a current spike of short duration occurs during switching. The total power dissipation in this condition is frequency dependent and can be lumped into the second component of power, namely the internal capacitive switching power.

It is difficult to evaluate these two components independently, so they are usually lumped together in an equivalent capacitance, represented by $C_{PD\emptyset}$, the charging and discharging of which would result in an equivalent power dissipation.

The relationship of interest is the dependence of the component of power dissipation on the rise and fall times of the inputs. If the inputs do not rise fast enough (typically ≤ 10 ns), the devices stay turned on for a longer duration. In this case, the base line power dissipation due to $C_{PD\emptyset}$ is not adequate to account for the extra power. This can be compensated by varying the value of the capacitor with changes in the rise times of the inputs. Figure 3.4 shows a plot of this new capacitance, C_{PD}, normalized with respect to $C_{PD\emptyset}$, versus rise time. The two curves show C_{PD} for

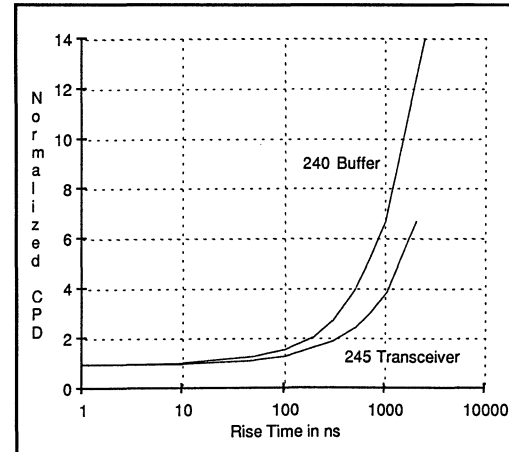


FIGURE 3.4
C_{PD} (NORMALIZED) VS. RISE TIME

transceivers and buffers respectively. All the interface parts will have an effective capacitance C_{PD} between these two curves. The total power dissipation due to switching frequency 'f' is given by:

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f$$

V_{CC} is the supply voltage.
C_{PD} is the effective capacitance due to internal capacitance and switching currents.
f is the frequency of the system.
P_D is the total internal power dissipation.

2) INTERNAL CAPACITANCE TRANSIENT DISSIPATION:

For interface buffers, latches, and transceivers, there exists a certain amount of capacitive load internal to the device itself. This capacitance is due to a variety of factors, such as the gate capacitance, Miller capacitance, and junction capacitance, which are shown in Figure 3.5.

All the capacitances get charged and discharged during the course of the circuits switching. These components of power dissipation are dependent on the technology used, the oxide thickness of the field and gate, and the topology of the individual component.

As mentioned above, any capacitive power dissipation is a function of the frequency of operation. The internal power dissipation is given by:

$$P_I = C_I \cdot V_{CC}^2 \cdot f$$

V_{CC} is the supply voltage.
f is the frequency of the system.
C_I is the total internal equivalent capacitance.
P_I is the internal power dissipation due to internal capacitance.

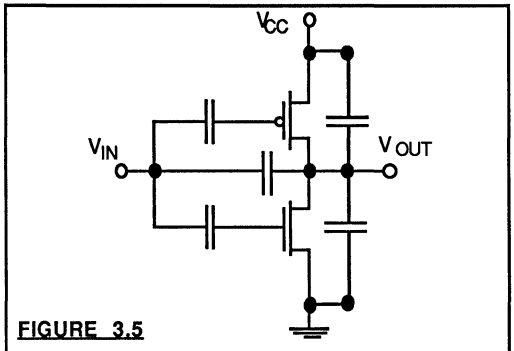


FIGURE 3.5
PARASITIC INTERNAL CAPACITANCES

As mentioned earlier in relationship to switching current equivalent power dissipation, internal capacitance and switching current components of power dissipation are rather difficult to isolate. For all further discussion, they will be lumped together and represented by C_{PD}. Note: C_{PD} could be a function of rise time for rise times greater than 100 ns.

3) EXTERNAL LOAD CAPACITANCE TRANSIENT DISSIPATION:

For the bus drivers and transceivers, external load capacitance is usually the biggest component of power dissipation in the system environment. The interconnect or bus lines present capacitance, and the various other devices present on the line also contribute their respective input or output capacitance.

Stray capacitance due to coupling and other factors is also present. All of these capacitors need to be charged and discharged during the normal course of signal switching. The power dissipation as a result of charging and discharging this external load capacitance can be evaluated by:

$$P_L = V_{CC}^2 \cdot (C_{L1} \cdot f_1 + C_{L2} \cdot f_2 + C_{L3} \cdot f_3 + \ldots C_{Ln} \cdot f_n)$$

C_{Ln} are the various loads on the respective outputs.
f_n are the respective switching frequencies for each output.
V_{CC} is the supply voltage.
P_L is the power dissipation due to the load.

As is apparent from the above equation, determination of the load on each output pin and its frequency of operation has to be taken into account to calculate the total power dissipation of an IC. The total power dissipation, internal and external, will dictate the need for power supply bussing, decoupling capacitors, etc. An example of this calculation is presented below:

EXAMPLE: A V74ACT245 transceiver is used to drive an eight-bit data bus, as shown in Figure 3.6. The intrinsic capacitance of the bus is 18 pF/ft. The bus is10" long and has six other transceivers connected to

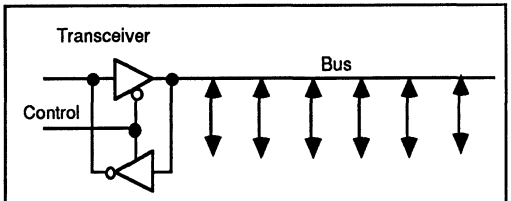


FIGURE 3.6 TRANSCEIVER DRIVING A BUS

it. Calculate the typical power dissipation of a driver IC driving this bus at a 1 MHz switching rate.

From the spec sheet for 245s the typical output capacitance of each output = 10 pF.

Total capacitance on the bus = (no. of drivers)•(capacitance of each driver)
= (6)•(10 pF)
= 60 pF

Capacitance of the bus (10" long) = (10/12)•18 pF = 15 pF

So, the Load Capacitance C_L = 15 pF + 60 pF = 75 pF

C_{PD}, the typical power dissipation capacitance, = 35 pF

Assuming a 1 MHz switching rate and V_{CC} = 5 V:

$$P = P_L + P_D = V_{CC}^2 \cdot f \cdot (C_L + C_{PD})$$
$$= 25 \cdot 1x10^6 \cdot 110x10^{-12}$$
= 2.75mW

(Quiescent power $I_{CC}V_{CC}$ has not been added because it is orders of magnitude less than the total power dissipation.)

Since the IC has eight I/O buffers: Total power consumption for the IC = $2.75x10^{-3} \cdot 8$ = 0.022 W

In this setup, only one out of seven IC's is dissipating power. If the bus speed was 10 MHz, the total power for this setup will be only 0.22 watts maximum. This is a simplistic example that does not consider duty cycle, bus terminations, etc. The actual power would be lower for an nonterminated bus.

A comparison of this setup with an ALS part:

I_{CC}, output disabled = 63 mA

Number of ICs disabled = 6

Total power of the inactive ICs = (6•63 mA)•5 V = 378 mA•5 V = 1.890 W

Power of the active ICs = 60 mA•5 V = 0.300 W

(Ignoring any increase due to the bus capacitance)

Total power dissipation = 2.19 W

Compared to 0.22 W for the V74ACT design, a 10:1 power advantage.

COMPARISON OF POWER DISSIPATION FOR AN UNLOADED IC

Total internal capacitance of the 245 is 8•50 pF = 400 pF.

Power/f = $C \cdot V_{CC}^2$ = 400 pF•(5 V)^2 =10 mW/MHz

or, for a 5V supply, you need 2 mA/MHz.

Figure 3.7 compares ALS240 and V54/74ACT240. The parts were selected at random and the measurement was made with all outputs switching, 50% duty cycle, 5V, and 25°C. Here the ACT240 shows a clear power advantage over the ALS parts.

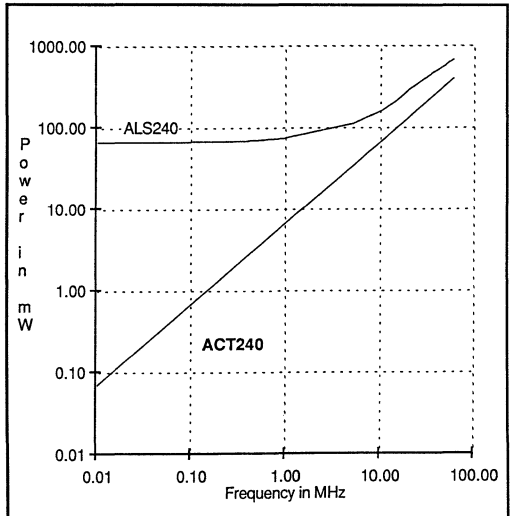


FIGURE 3.7
ALS & ACT POWER DISSIPATION VS. FREQUENCY

SUMMARY

The V54/74ACT family of high-speed interface parts was described. A comparison with the ALS family showed that VTC's ACT family is 10:1 better in total power dissipation in a system environment. Input current is improved 1000:1 for comparable performances. The current drive capability is also improved 2:1. Systems run cooler using VTC's ACT family parts, and it is not necessary to use ceramic packages to improve cooling.

AC CHARACTERISTICS OF THE V54/74 ACT INTERFACE FAMILY

INTRODUCTION

The following text offers the designer the V54/74ACT family's expected performance under various conditions.

- What the data sheet specifications imply.
- The impact on performance due to variations in temperature, power supply, external capacitive loading, rise/fall times, and setup/hold times.

The intent is to give sufficient information on the expected derating for the specification sheet parameters over the desired operating range of the components. This will provide ease of component application without unnecessary and extensive evaluation procedures.

Effort is made to provide the highest accuracy at the time of publication. In time, these curves may not reflect the latest quality and performance data. Current derating curves should be obtained and used whenever possible. These curves are fairly accurate, reflect the proper trends to be expected, and should be used only to project performance variations under given environmental conditions. Methods for determining propagation delay in most situations are described using examples and illustrations.

WHAT THE SPECIFICATIONS IMPLY

The V54/74ACT family is ALS compatible, meets TTL input and output requirements, and provides ALS performance with CMOS power dissipation. The interface logic family is implemented in an advanced double metal, poly-silicon CMOS process that gives the family slightly different capabilities.

The specification data sheets are written in a format similar to the common TTL formats. The complete specifications are written around 0 to 3.5 V waveforms, with a 1.5 V measurement point for delay measurements. The inputs behave very close to the TTL waveform levels and will not cause noticeable differences in actual system environments. The outputs, specified for the 0 to 3.5 V range, are typically capable of rail to rail swings of 0 to V_{CC}. This feature provides a very high current drive capability for the outputs pulling high. The DC performance specifications give a clear idea of this high-drive capability. There is no easy way to reflect this in the AC performance sheets.

One consequence of the improved drive in the 2 to 3 V range is the improved delay numbers for low to high. The devices are designed to be symmetric in rise/fall times and this gives them improved performance compared to the ALS family's low-to-high transition.

On the average, the output drive capability of the V54/74ACT family is much higher than the ALS family. All V54/74ACT devices have the capability to source and sink 48 mA under commercial conditions and 32 mA under military conditions. In the ALS family, special parts must be specified to achieve this drive capability. This high-drive capability is in line with the intended application of the V54/74ACT parts. These parts are designed for driving 3-stated buses on boards as well as off-board and in back-plane environments.

All parts in this family - buffers, latches, transceivers, and flip-flops - are capable of operating under a harsh environment. These parts meet and exceed the mil STD883 input protection requirements. They are also latch- up immune to 200 mA current pulses.

The 3-state measurements, along with other delay measurements, are made as shown in Figures 4.1A-4.1H. The test circuit load is a 50 pF or a 300 pF capacitor. The characterization under the 300 pF load is to provide data for a typical bus loading environment. (Refer to section 2 for further details.)

All specifications call for rise and fall times of 3 ns. To bring out the performance capabilities of the higher speed parts, this is an important requirement. The delay measurements are specified at 1.5 V points to make easier the comparison with the TTL families. The rise and fall times are measured at the 10 to 90% level of the typical TTL swing in the 0 to 3.5 V range. For tri-state measurement, the 500 Ω resister is switched to ground for the t_{PHZ} measurement, and is switched to V_{CC} for the t_{PLZ} measurement. The timing measurements measure the time required for outputs to go from active levels to 10 or 90% for low to Z or high to Z respectively. This is done to keep in line with the TTL world.

The performance numbers are specified under a typical environment of 25°C, 5 V, and presume nominal processing parameters. The guaranteed numbers reflect the worst-case processing parameters. In reality, the devices will normally exceed these performance numbers. The guaranteed commercial or military numbers take into account the derating in performance due to the supply and temperature for the respective family.

TEMPERATURE, ITS EFFECT ON AC PERFORMANCE

Temperature has an effect on the performance of the V54/74ACT family of parts. The performance degrades linearly with increasing temperature. In the data sheets, the performance is specified for 25°C and 85°C for commercial, and 125°C for military. The specification numbers also contain the effects due to other changes, such as supply, load, and process variations. The following equation can be used to predict the temperature component of the delay :

FIGURE 4.1A 3-STATE TEST PARAMETERS

PARAMETER	R_L	SWITCH
t_{PZH}	500 Ω	R_L to Gnd
t_{PZL}	500 Ω	R_L to V_{CC}
t_{PHZ}	500 Ω	R_L to Gnd
t_{PLZ}	500 Ω	R_L to V_{CC}
t_{PLH} or t_{PHL}	500 Ω	R_L to Gnd or R_L Open*

* Use this for capacitive loads only

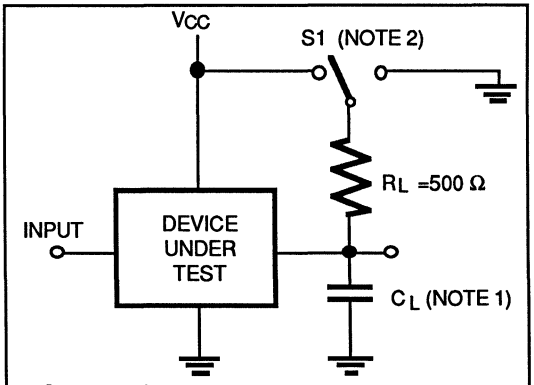


FIGURE 4.1B
TEST CIRCUIT FOR 3-STATE OUTPUT TESTS

NOTE 1: C_L includes load and test jig capacitance.
NOTE 2: S1= V_{CC} for t_{PZL} , and t_{PLZ} measurements.
S1=Gnd for t_{PZH} , and t_{PHZ} measurements.

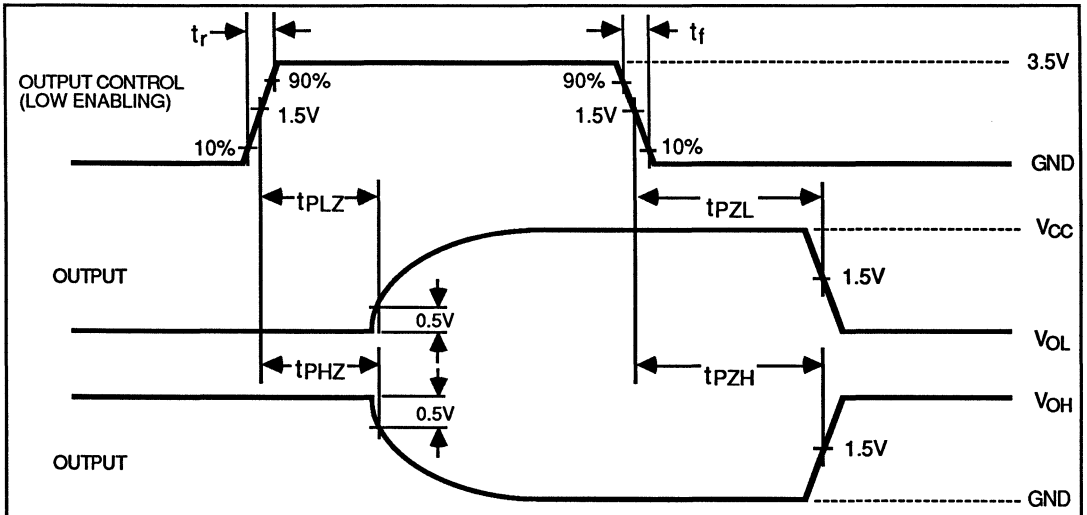


FIGURE 4.1C
3-STATE OUTPUT ENABLE AND DISABLE WAVEFORMS

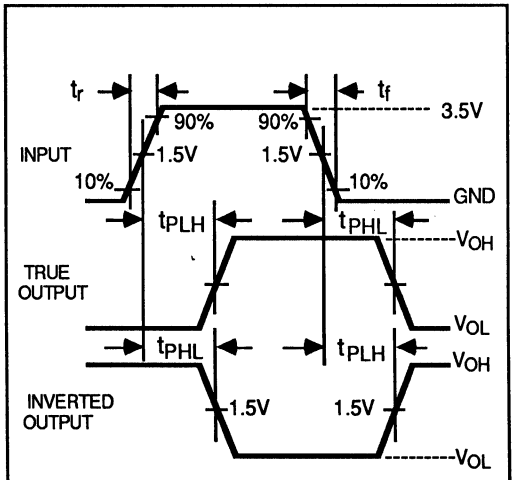


FIGURE 4.1D
PROPAGATION DELAY WAVEFORMS

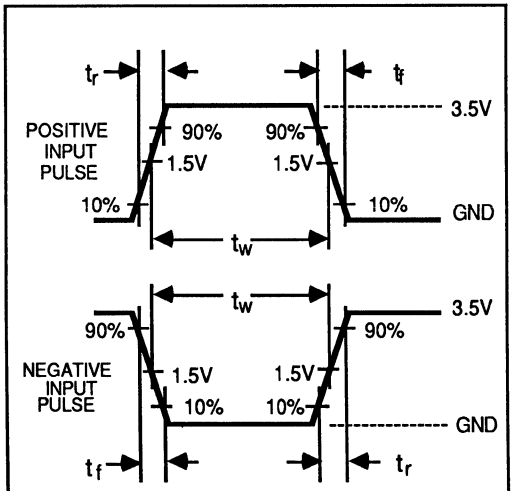


FIGURE 4.1F
INPUT PULSE WIDTH WAVEFORMS

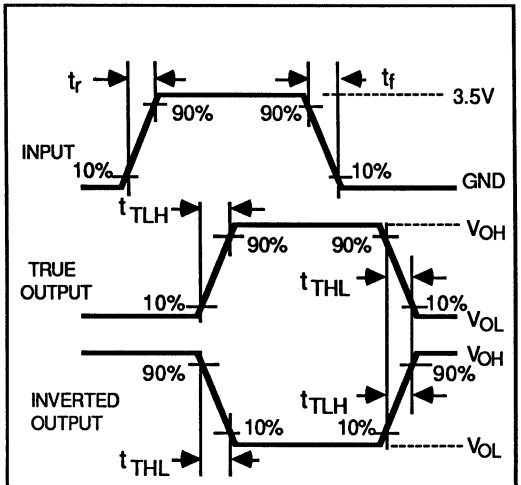


FIGURE 4.1E
OUTPUT TRANSITION TIME WAVEFORMS (10-90% of 3.5V)

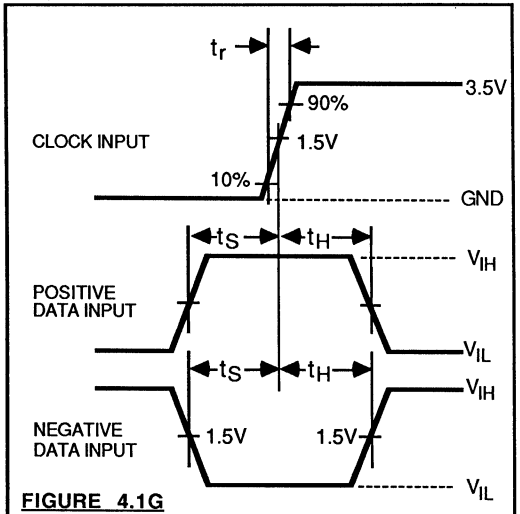


FIGURE 4.1G
SETUP AND HOLD TIME WAVEFORMS FOR FLIP-FLOPS

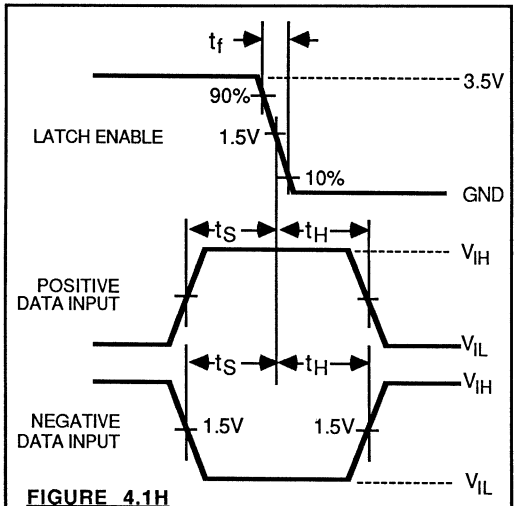


FIGURE 4.1H
SETUP AND HOLD TIME WAVEFORMS FOR LATCHES

$t_{PD}(T) = t_K(t) \cdot t_{PD}(25)$

$t_{PD}(25)$ is the propagation delay at 25°C for a specified load and supply.
$t_K(t)$ is the propagation delay derating factor due to temperature variations, taken from Figure 4.2.
$t_{PD}(T)$ is the propagation delay at temperature T.

Figure 4.2 shows plots of the propagation delay derating factor due to temperature over the specified temperature range for buffers, transceivers, latches, and flip-flops. The normalized value is the typical number for each family. To determine delay for a buffer at 85°C, locate the value on the buffer curve, which is **1.3**. Thus the buffer delay has increased from t_{PD} to **1.3**t_{PD}.

POWER SUPPLY, ITS EFFECT ON AC PERFORMANCE

Figure 4.3 shows the propagation delay derating due to power supply variations over the specified supply range of 4.5 to 5.5 V. The CMOS family is capable of operating in this range with small degradation in performance. It is important to remember that power supply variation not only affects the performance values, but the drive capability. The specification data sheets present conservative drive current numbers. Power supply bussing should be given proper attention. Otherwise, under AC conditions, the power supply on the board may fall outside the operating range, resulting in timing or logic errors.

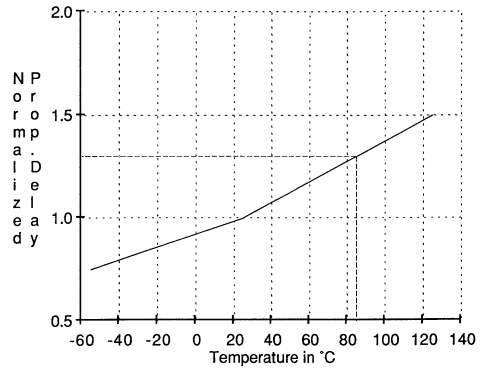


FIGURE 4.2
NORMALIZED PROPAGATION DELAY VS. TEMPERATURE AT 50 pF, 5V

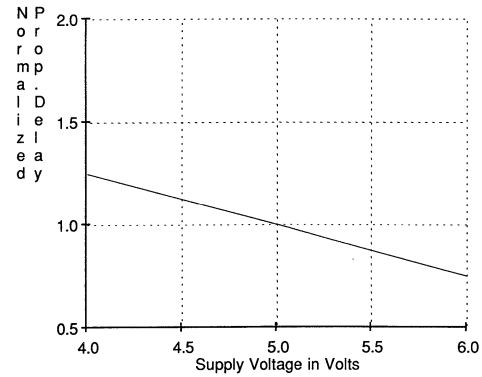


FIGURE 4.3
NORMALIZED PROPAGATION DELAY VS. SUPPLY VOLTAGE AT 50 pF, 25°C

To calculate the expected propagation delay at a voltage V, use the following equation:

$t_{PD}(V) = t_V(V)[t_{PD}(5V)]$

$t_{PD}(5V)$ is the propagation delay with a 5 V supply for a specified temperature and load.
$t_V(V)$ is the propagation delay derating factor due to power supply variations, taken from Figure 4.3.
$t_{PD}(V)$ is the propagation delay for V_{CC} = V.

Note: The curve is drawn over a 4 to 6 volt range. The performance numbers are only guaranteed for the 4.5 to 5.5 V range. Under typical conditions the device will operate below this range, but the performance numbers are not guaranteed.

CAPACITIVE LOAD, ITS EFFECT ON AC PERFORMANCE

The V54/74ACT family of interface drivers is designed to drive large loads encountered in system buses. For performance evaluation purposes, the load seen by each driver is the sum of the input capacitances due to fan-out, the 3-state output capacitance of other transceivers connected to the bus line, and the intrinsic wiring capacitance of the line itself. The delay is directly proportional to the load driven. Figure 4.4 shows the delay variation, under nominal conditions, for buffers, latches, flip-flops, and transceivers.

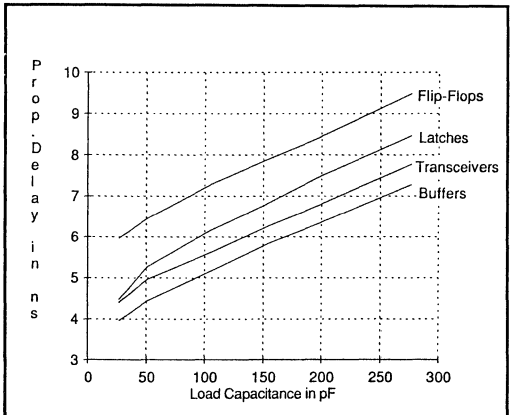


FIGURE 4.4
PROPAGATION DELAY VS. LOAD CAPACITANCE AT 5V, 25°C

Figure 4.5 shows plots of the normalized delay variation constant for the V54/74ACT interface family. There is only one curve required for this, because all family devices have identical driver circuitry. This gives the same variation for various loads throughout the family. The delay at any load capacitance C_L is evaluated by using the following equation :

$t_{PD}(C_L) = t_C(C) \cdot t_{PD}(50)$

$t_{PD}(50)$ is the delay at 50pF for a specified temperature and supply.
$t_C(C)$ is the propagation delay derating factor due to load capacitance, taken from Figure 4.5.
$t_{PD}(C_L)$ is the propagation delay for a load C_L.

COMPOSITE CALCULATION

Let us consider an example by evaluating the delay expected at 75°C, 4.8 V, and 250 pF for a 240 type line driver. This value can be obtained by evaluating the three derating coefficients at the above values, and then multiplying the results by the delay at 5V, 25°C, and 50pF.

From Figure 4.2, find the propagation delay derating factor due to temperature: $t_K(75°C)$ = 1.38

From Figure 4.3, find the propagation delay

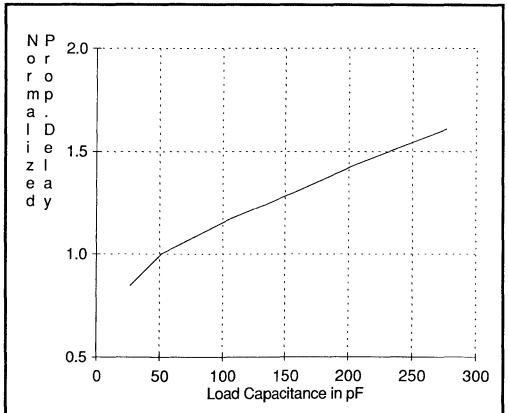


FIGURE 4.5
NORMALIZED PROPAGATION DELAY VS. LOAD CAPACITANCE AT 5V, 25°C

derating factor due to power supply variation: t_V(4.8 V) = 1.05

From Figure 4.5, find the propagation delay derating factor due to load variation: t_C(250 pF) = 1.54

Then (equation 4.1):

t_{PD} (@ 4.5 V, 75°C, 250pF)
= $t_K \cdot t_V \cdot t_C \cdot t_{PD}$ (@ 5.0 V, 25°C, 50 pF)
= 2.23·t_{PD}(@ 5.0V, 25°C, 50 pF)

Thus, the effect of any parameter on the delay can be evaluated either independently or in any combination by using equation 4.1.

SETUP/HOLD TIME AND PULSE WIDTH VARIATIONS

Setup time, hold time and pulse width are parameters that reflect the internal delay of the device. These parameters will follow the same trends, with similar coefficients of variation with respect to power supply and temperature, as the external numbers. An exact evaluation can be made for these parameters using the procedure outlined in the preceding sections.

OUTPUT RISE AND FALL TIME

Figure 4.6 shows a plot of the variation of normalized output rise and fall time with load capacitance. The propagation delay factor due to output capacitance will not work for calculating output rise and fall times. This is bacause the propagation delay measurements only require the outputs to reach the 1.5V point, while the rise and fall measurements require the output to travel between 0.35V and 3.15V.

To calculate output rise and fall times, equation 4.1 may still be used. In place of t_{PD}, use t_R or t_F. The variation with temperature and supply will be the same as for propagation delay measurements, so the only other change required is the substitution of t_C, the rise and fall time derating factor due to load capacitance, from Figure 4.6, for the t_C in equation 4.1.

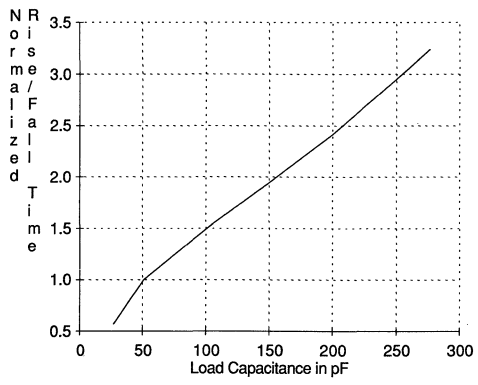


FIGURE 4.6
OUTPUT RISE/FALL TIME VS. OUTPUT LOAD CAPACITANCE

INPUT RISE AND FALL TIME

Another item of concern is input rise and fall time. The V54/74ACT family is designed for use in high-performance systems with fast rise/fall times.

If the rise/fall times are too slow, two important events occur. First, power dissipation increases if the device is in the intermediate stage for an increased period of time, rise/fall time > 50ns. Second, if the rise/fall time is extended for an unusually long period of time, over 100 ns, the likelihood of oscillations due to noise riding on the inputs can cause problems.

Latches and flip-flops are especially vulnerable to this situation. These devices are likely to go into a meta-stable state from which data integrity is lost. A few micro-seconds will be required for the device to come out of this state.

So, if a long rise/fall time is present at some stage in the system, it should be filtered out by using Schmitt triggers or other types of input hysteresis with a dead zone in the 0.8 to 2.0 volt range.

COMPARISON TO OTHER FAMILIES

The V54/74ACT family is designed to be compatible with the ALS logic family, but subtle differences exist between the two families.

Temperature variation is the major difference. Although the maximum delays are identical for both families, the effect of temperature is different when considering typical performance numbers. It is imperative the designer understand the environment of operation and use the derating coefficients to predict the exact values when higher accuracy is desired.

Tables 4.1 through 4.4 compare the V54/74ACT family with other TTL and CMOS logic families. They can be used as a reference guide for the selection of the appropriate devices. For greater details about the comparison, refer to section 8 on performance comparison.

TABLE 4.1: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 244 Octal Buffer and Line Driver with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay A to Y	Typical [25°C, 5V, C_L = 50pF]			14	5	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	10	6.2	25	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	13	9	30	12	ns
t_{PZH} Output enable time Enable to Y	Typical [25°C, 5V, C_L = 50pF]			15	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	20	9	38	12	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	25	10	45	14	ns

TABLE 4.2: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 245 Octal Bus Transceiver with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay A to B/B to A	Typical [25°C, 5V, C_L = 50pF]		6	14	5	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	10		29	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	15		34	12	ns
t_{PZH} Prop. Delay Output Enable to A/B	Typical [25°C, 5V, C_L = 50pF]		8	31	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	20		53	13	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	25		63	15	ns

TABLE 4.3: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 373 Octal Transparent Latch with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay D to Q	Typical [25°C, 5V, C_L = 50pF]			22	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	12	6	37	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	14	8	45	12	ns
t_{PLH} Latch enable time Enable to Q	Typical [25°C, 5V, C_L = 50pF]			21	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	22	11.5	37	12	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	26	14	45	14	ns

TABLE 4.4: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 374 D-Type Edge-Triggered Flip-Flop with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay CLK to Q	Typical [25°C, 5V, C_L = 50pF]			22	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	12	8	37	13	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	15	11	45	15	ns
t_{PZH} Prop. Delay Output Enable to Q	Typical [25°C, 5V, C_L = 50pF]			21	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	17	6	37	14	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	19	7	45	16	ns

CONCLUSION

Effort has been made to bring out the impact of environmental parameters - such as temperature, power supply, and loading - on the AC performance of this new family of logic devices. This information will give the designer a good feel for the performance potential of the high-speed V54/74ACT parts, and will equip him to utilize their full potential.

NOTES

DC CHARACTERISTICS OF THE V54/74 ACT INTERFACE FAMILY

INTRODUCTION

This section covers the basics of the V54/74ACT family's DC characteristics, and compares these to the other logic families. The topics covered in detail are:

- Data sheet specifications.
- Input characteristics: voltage levels, currents, and capacitive loading.
- Output characteristics: voltage levels, currents, and capacitive loading.
- Power supply voltage and quiescent currents.

DATA SHEET SPECIFICATIONS

The V54/74ACT family is a TTL-compatible logic interface family of 3-state drivers and transceivers. The main functions fall into four categories: buffers, latches, flip-flops, and transceivers.The recommended operating conditions and specifications under DC conditions are listed in Table 5.1.

The key feature of this family, as stressed in this specification sheet, is the nearly symmetrical current source/sink capacity. This logic family will have the same current drive capability across the complete set. Under guaranteed conditions, the devices are specified with a DC drive capability of 48 mA for commercial and 32 mA for military operating ranges.

A second feature unique to this family of parts is the DC current and loading at the inputs. The devices present capacitive loads at their inputs, with very low leakage currents in the μA range.

The third feature of interest is the very low quiescent currents under DC conditions. Compared to their TTL counterparts, this family has a much lower power dissipation. Typical power dissipation for these parts is 10 μW.

INPUT CHARACTERISTICS: VOLTAGE LEVELS, NOISE IMMUNITY, CURRENTS, AND CAPACITIVE LOADING

A rudimentary CMOS input detector is a simple two transistor inverter. In order to detect TTL levels of V_{IH} = 2.0V and V_{IL} = 0.8V, the ratios of the N and P transistors must be changed in such a way as to shift the inverter's switching point (V_{SP}) from the normal V_{SP} = 2.5V (1/2 V_{CC}) down to the TTL level of V_{SP} = 1.4V (1/2[V_{IH} + V_{IL}]). With the switching point at 1.4V, the noise margin for a logical 1 (NM1) will equal the noise margin for a logical 0 (NM0), both being 0.6V. Thus, the equation V_{IH} - V_{IL} = NM1 + NM0 holds, even if the switching point should deviate from 1.4V. Figure 5.1A shows a graphic representation of the TTL noise margins.

A major problem of using a simple CMOS inverter to detect TTL input levels is that the circuitry will have poor drive capabilities and will draw a large amount of quiescent current (I_{CC}) when the input is held at V_{IH} = 2.0V. With the input at 2.0V, the V_{GS} of the P channel transistor is 3.0V and the V_{GS} of the N channel is 2.0V, both well above normal threshold voltages; thus, both transistors are conducting. To keep this current low, the sizes of the two transistors must be kept small, but this further reduces the drive capability of the input detector.

The input detector VTC uses on interface parts consists of six transistors. Two have their gates controlled by the input signal, and four are used to control both the V_{GS}s and the current flow. Using such a network allows these parts to draw a much smaller quiescent current (I_{CC}) when the input is held at V_{IH} = 2.0V. This in turn allows VTC to build input detectors using larger transistors that have greater drive capabilities while still maintaining very low quiescent supply currents.

Another advantage of the input detectors used by VTC is the improved noise margins for both the logical one and the logical zero. With both NM1 and NM0 being larger than a simple inverter, we have been able to achieve: V_{IH} - V_{IL} < NM1 + NM0. This is possible because our input detector also includes a bit of inherent hysteresis. In fact, we have not one, but two switching points for our input detectors. These are known as the maximum positive going threshold voltage (V_T^+), applicable when going from a 0 to a 1, and the minimum negative going threshold voltage (V_T^-), which applies when going from a 1 to a 0.

Thus, NM1 is now V_{IH} - V_T^+, while NM0 = V_{IL} - V_T^-. The hysteresis voltage (V_H) is defined by V_H = V_T^+ - V_T^-. For the V54/74ACT family, V_H is around 0.4V, and both noise margins have approximately an additional 0.2V margin (about a 33% increase) compared to TTL. Figure 5.1B shows a graphic representation of the V54/74ACT noise margins.

Figure 5.2 shows the transfer function of the V54/74ACT family over its temperature range. In Figures 5.3A-5.3C, the high-to-low transfer function is compared to the LS-TTL and ALS-TTL families. From these curves, it can be concluded that, compared to the others, the transfer curves stay fairly constant for the V54/74ACT family. The ALS and LS families show the greatest variation over temperature, and the switching curves vary with a change in supply voltage. For V54/74ACT, the established crossover point tracks linearly with supply variation. For example, a switch at 1.5 V, for V_{CC} = 5 V, gives a switching voltage of

TABLE 5.1: RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			Vcc+0.5	Vcc+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS		Military -55° to 125° C		Commercial -40° to 85° C		UNITS
				Typ	Guar	Typ	Guar	
V_{IH}	Minimum High Level Input Voltage				2.0		2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8		0.8	V
V_{OH}	Minimum High Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OH}\|$					
			20µA		4.4		4.4	V
			24mA		2.4		2.6	V
V_{OL}	Maximum Low Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OL}\|$					
			20µA		0.1		0.1	V
			32mA		0.5		0.4	V
			48mA		0.65		0.5	V
I_L	Maximum Input Leakage Current	Vcc=5.5V V_{IN} =Vcc or Gnd			±1.0		±1.0	µA
V_{IK}	Input Clamp Voltage	Vcc=4.5V	I_{IN}					
			-18mA		-1.2		-1.2	V
			18mA		Vcc+1.2		Vcc+1.2	V
I_{OZ}	Maximum Output Leakage Current	Vcc=5.5V VOUT =Vcc or Gnd All Outputs Disabled		1.0	±10.0	0.5	±5.0	µA
I_{CC}	Maximum Quiescent Supply Current	Vcc=5.5V V_{IN} =Vcc or Gnd #All Outputs Disabled		10.0	160.0	10.0	120.0	µA
		*V_{IN} =2.0V		0.5	1.5	0.5	1.0	mA
		*V_{IN} =0.8V		0.5	1.5	0.5	1.0	mA

*Worst case leakage current at the TTL input receivers. One input only, all others tied to ground.
#Outputs floating, except for transceivers which must have outputs tied to Vcc or ground.

1.5/5 = 0.3 V_{CC}. Thus, the switching curves will vary in the range of (4.5)•(0.3) through (5.5)•(0.3), or 1.35 V through 1.65 V.

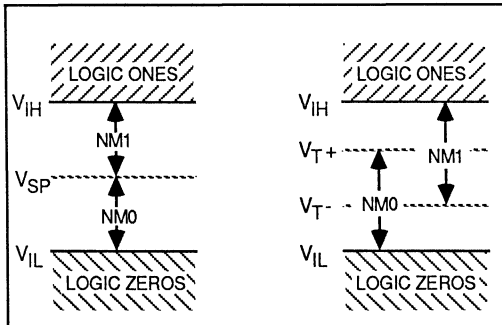


FIGURE 5.1
NOISE MARGINS BASED ON THRESHOLD VOLTAGES

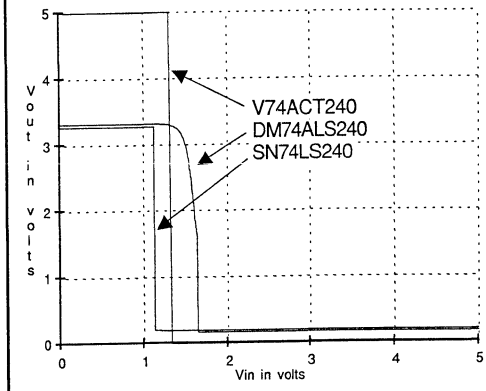


FIGURE 5.3A
HIGH-TO-LOW TRANSFER FUNCTION COMPARISON AT -55°C, Vcc = 5.0V

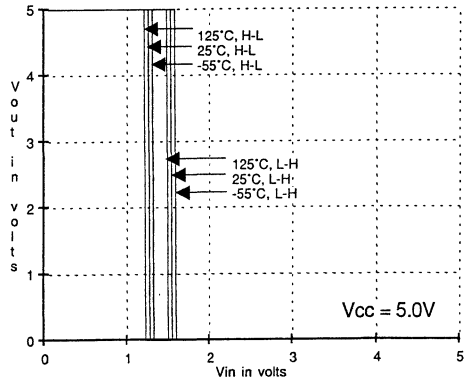


FIGURE 5.2
LOW-TO-HIGH AND HIGH-TO -LOW TRANSFER FUNCTIONS FOR V54/74ACT OVER TEMPERATURE WITH Vcc = 5.0V

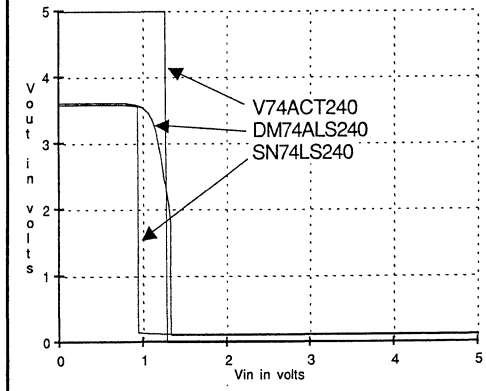


FIGURE 5.3B
HIGH-TO-LOW TRANSFER FUNCTION COMPARISON AT 25°C, Vcc = 5.0V

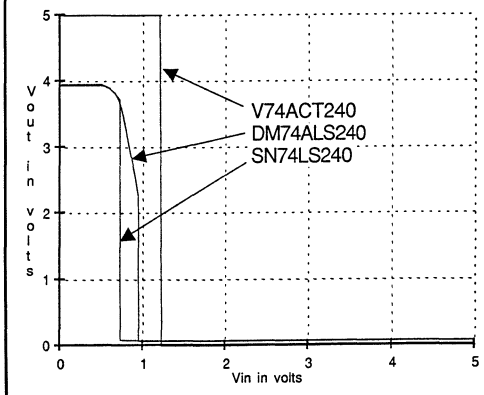


FIGURE 5.3C
HIGH-TO-LOW TRANSFER FUNCTION COMPARISON AT 125°C, Vcc = 5.0V

Input currents for the V54/74ACT result from junction leakage in the input protection circuitry. The typical values, under nominal conditions, are in the nano-ampere range. This current varies exponentially over temperature, rising to no more than 100s of nA at 125°C ambient temperature. The DC specification lists the worst-case specification for the V54/74ACT parts.

The low leakage currents allow the V54/74ACT parts to have a very high fan-out compared with the ALS or LS parts. Each input has some capacitance associated with it due to package type, leadframe, and the input circuitry. This capacitance is typically 3 to 5 pF for the V54/74ACT parts.

TABLE 5.2
INPUT CURRENT REQUIREMENTS

	Input Current Low I_{IL}	Input Current High I_{IH}
LS-TTL	-0.2 mA max	20 µA max
S-TTL	-400µA max	50 µA max
ALS-TTL	-0.1 mA typ	20 µA max
V-ACT	1 µA max	1 µA max
HC	1 µA max	1 µA max

This type of capacitive loading is also present in the TTL parts, along with additional resistive loading. The resistive loading causes the TTL families to require significant input currents. Table 5.2 lists the input current requirements for the various families.

INPUT PROTECTION

The input circuitry of the V54/74ACT family has been designed with clamping diodes to V_{CC} and ground. The characteristics of the clamping diode to ground are shown in Figure 5.4. The characteristics of the other clamping diode are similar, but around V_{CC} instead of ground.

One of the reasons for the clamping diode is to limit undershoot (or overshoot) at the end of a signal line following a low-to-high transition. For example, an output signal change from 3.5V to 0.5V into a 100Ω line propagates to the end of the line accompanied by a 30mA current change. If the line is terminated in a high impedance, such as a CMOS gate input, the 3V signal change doubles, driving the terminal voltage down to -2.5V.

However, the clamping diode on V54/74ACT family parts limits the negative excursion to about -0.7V. The same high-to-low signal change on a 50Ω line is clamped at about -1.0V. If the transition had been low-to-high, a positive excursion above V_{CC} would take place. This excursion would be limited to approximately V_{CC} + 0.7V (100Ω line) or V_{CC} + 1.0V (50Ω line). The maximum values of the input clamp voltage, V_{IK}, are shown in Table 5.1.

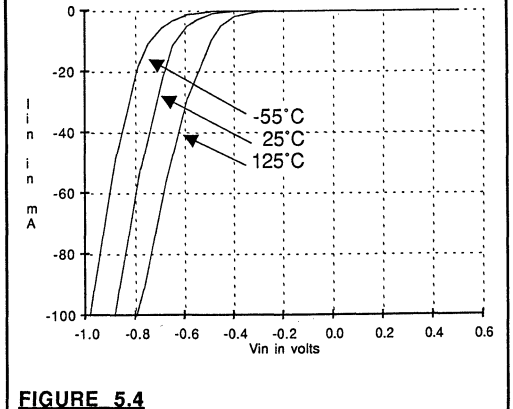


FIGURE 5.4
INPUT CLAMPING CHARACTERISTICS FOR V54/74ACT FAMILY

The clamping diodes also function as part of the V54/74ACT family's excellent ESD protection circuitry. The inputs are designed to meet or exceed MIL-STD 883B. They will withstand the discharge of a 100 pF capacitor, charged to 2000V, and discharged through a 1.5kΩ resistor. Further explanation and an input circuit diagram can be found in section 7, ESD and Latch-up.

The inputs are also designed with proprietary circuit techniques to prevent latch-up problems. Effective latch-up protection up to 300 mA (typical) at 25°C has been demonstrated on these devices. Again, see section 7 for further details.

OUTPUT CHARACTERISTICS

A standard CMOS output buffer consists of a P-channel pullup transistor and an N-channel pulldown transistor as shown in Figure 5.5. Each of the two paths is controlled by a separate set of gates so that the output can be put into a high impedance state. A current vs. time plot is shown in Figure 5.6A. Since the output drivers are much larger than any other devices in the chip, almost all of the current drawn by the chip under AC conditions is used for the switching of these drivers. This switching current appears as an instantaneous spike when the output switches. This standard output buffer works for low drive applications but is unacceptable for the high drive conditions of ACT.

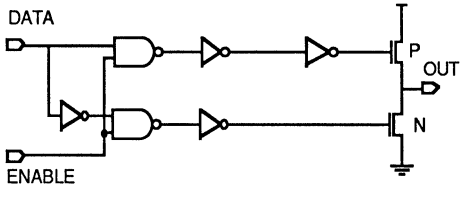


FIGURE 5.5
STANDARD CMOS OUTPUT BUFFER

Sudden surges of current through the lead inductances of the part cause ground bounce and output ringing. VTC has overcome this problem by distributing the current spike over time to soften the di/dt as shown in Figure 5.6B. This ordinarily will slow down the part, but the design used by VTC minimizes this delay. VTC's output circuit (patent pending) is shown in Figure 5.7.

The large pull-down transistor in the standard buffer is split into two devices separated by a resistor. The resistor delays the turn on of the second device so that rather than getting one large current spike, there are two smaller ones separated in time, their sum being the

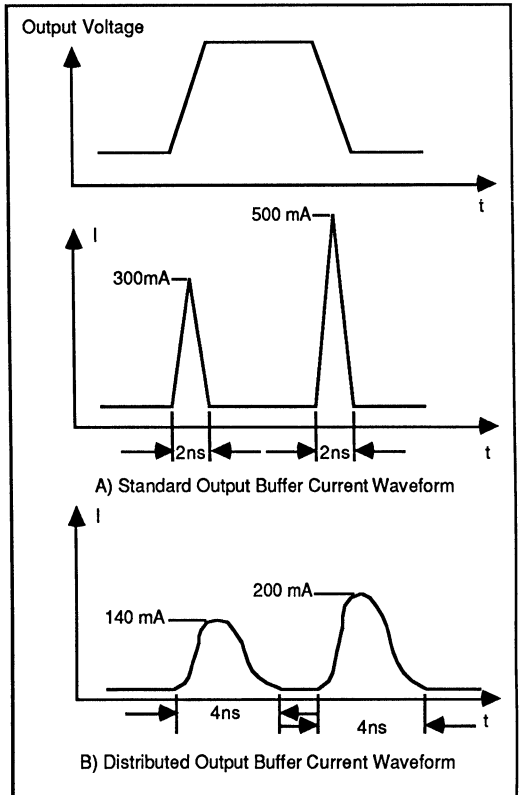


FIGURE 5.6
SWITCHING CURRENT WAVEFORMS

rounded curve shown in Figure 5.6B. The N-channel device connected to the gate of the second N-driver provides for a fast turn-off, reducing crowbar current (current that flows from power to ground when both the pull-up and pull-down are on simultaneously during switching).

An N-channel pull-up is used to provide more drive than the equivalent sized P-channel, and to limit the output V_{OH} due to the threshold drop. This lower V_{OH} level speeds up the high-to-low transition since the logic transition is reduced. A small P-channel pull-up takes over the pull-up detail when the N-channel turns off. Since the output voltage has already switched most of the way, this P-channel needn't be made as large as the single P-channel pull-up in the standard design. The inverter needed to give the proper phase to the P-

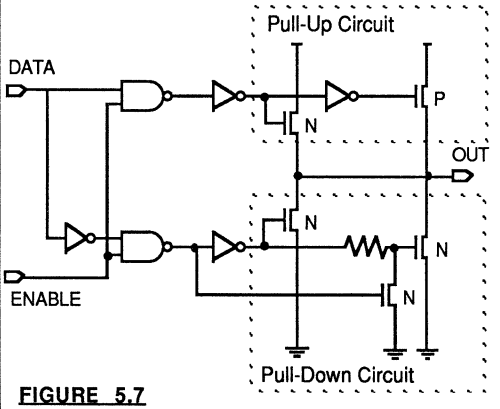


FIGURE 5.7
VTC's DISTRIBUTED OUTPUT BUFFER DESIGN

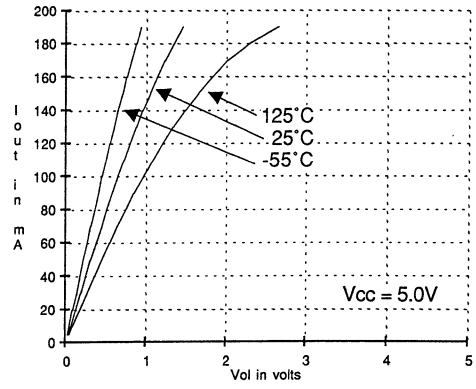
channel acts to delay the turn-on, thus distributing the current spike.

By splitting the drivers, the load on the previous stages is reduced, allowing these stages to be made smaller. This savings propagates back through the chip and winds up eliminating two stages in the overall design. Thus, ground bounce and ringing are reduced by spreading out the current pulse and slowing down the output buffer, plus the resulting reduced load allows the previous stages to be faster, keeping the overall delay of the part to a minimum.

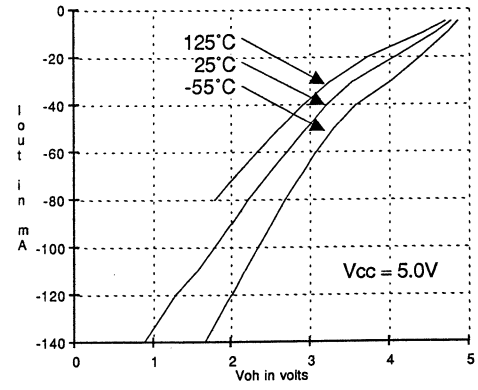
The V54/74ACT family has a constant drive capability across the entire family of parts. As stated earlier, this family has been designed to provide the high drive requirements of the bus interface type circuit. The parts are capable of I_{OH} and I_{OL} in the 48 mA and higher range. Figure 5.8 illustrates the drive capabilities over the entire voltage range for output high and output low. These plots illustrate the salient features of the V54/74ACT parts.

The V54/74ACT parts are designed to drive 100 and 50 ohm lines with high capacitive values. The data sheets specify the devices under the worst-case temperature and voltage conditions. Under typical conditions, the devices are capable of sourcing almost 1.5 times as much current, as demonstrated in Figure 5.9. The high current capability allows us to specify the devices at 50 and 300 pF capacitive loads.

The output current and voltage characteristics of a logic circuit determine how well that circuit will switch its output when driving capacitive loads and transmission



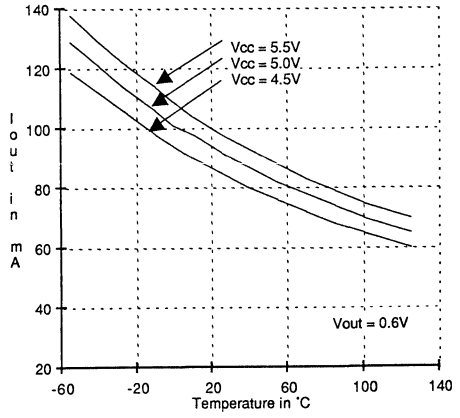
OUTPUT SINK CURRENT VS.
OUTPUT LOW VOLTAGE



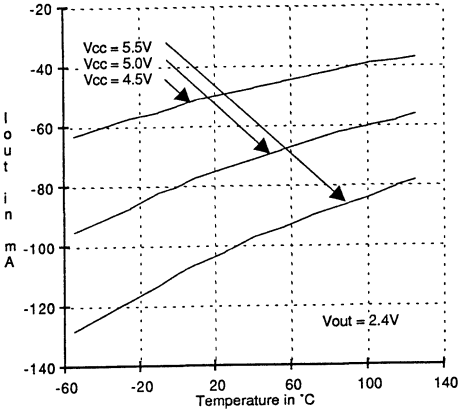
OUTPUT SOURCE CURRENT VS.
OUTPUT HIGH VOLTAGE

FIGURE 5.8 OUTPUT CHARACTERISTICS

lines. The more current available, the faster the load can be switched. In order for V54/74ACT to achieve ALS performance, the outputs should have characteristics comparable to or better than ALS. The above discussion and figure illustrated this claim. The V54/74ACT family meets and exceeds the drive capability of ALS.



OUTPUT SINK CURRENT



OUTPUT SOURCE CURRENT

FIGURE 5.9
TYPICAL OUTPUT SOURCE AND SINK CURRENT VS. TEMPERATURE

POWER SUPPLY VOLTAGES, QUIESCENT CURRENTS, AND TEMPERATURE

The V54/74ACT family is specified to operate in the same power supply range as the standard ALS family. A power supply variation of ±10% around 5 V nominal is the common specification. For CMOS technology, variations in the power supply influence the switching point of the device. The inputs switch at approximately 0.3 V_{CC} volts. Thus, as V_{CC} varies from 4.5 to 5.5 volts, the input switching point varies. The same is true of the internal nodes and the output driver. All nodes other than the input circuits typically switch at the mid-point of the power supply (i.e. 0.5 V_{CC}). This causes the switching point, except for the inputs, to vary in the 2.25 to 2.75 volt range.

Power supply variation has a great impact on delay and drive currents at the output. To the first order, the current through the MOS transistor is given by the following equation:

$$I_O = ß(\text{width/length})[(V_{GS}-V_T)V_{DS}-0.5(V_{DS})^2]$$

Where:

V_{GS} is the gate voltage.

V_{DS} is the drain voltage.

ß is the device transconductance.

The equation illustrates the influence of the supply voltage on the drive current capability of the CMOS parts. Reduced supply voltage will cause the parts to slow down because drive will be reduced. Thus, it will take longer to charge or discharge external load capacitances.

The quiescent power supply current of the high speed V54/74ACT family is shown in Figure 5.10. This

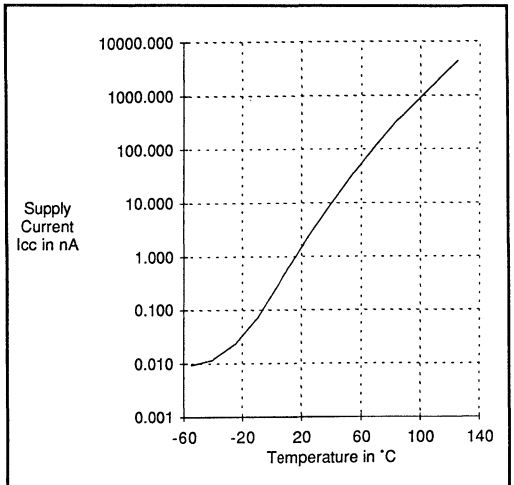


FIGURE 5.10
TYPICAL QUIESCENT SUPPLY CURRENT VS. TEMPERATURE

TABLE 5.3: ABSOLUTE MAXIMUM RATINGS[1]	
Supply Voltage, VCC	-0.5V to +7.0V
Input Voltage	7.0V
Off-State Output Voltage	7.0V
Operating Free-Air Temperature	
Military Temp	-55°C to 125°C
Commercial Temp	-40°C to 85°C
Storage Temperature Range	-85°C to 150°C
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2000V
Note 1: Maximum ratings are those values beyond which damage to the device may occur.	

plot shows the variation of the quiescent current with temperature. During steady state, no direct path exists between V_{CC} and ground. The quiescent current is therefore due to leakage current in the reverse-biased junctions of the various transistors. Because it is leakage current, it varies exponentially with temperature.

The V54/74ACT family has a large amount of area in reverse-biased junctions. This is required for the high drive abilities of this interface family. The high diode area does lead to higher leakage currents, but these are still very small, in the nano to microampere range.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings define the limits in which the V54/74ACT family can be operated without causing device malfunction and possible damage. These limits are shown in Table 5.3.

CONCLUSION

The V54/74ACT family has superior DC characteristics compared to the other interface families. This is due to the advanced CMOS process used by VTC Incorporated. The V54/74ACT family greatly exceeds the drive characteristics of the ALS logic family, to which it was designed to be compatible.

CHARACTERIZATION AND SPECIFICATION

INTRODUCTION

This section covers methods of testing V54/74ACT logic and describes how to design and use a universal test fixture to characterize our circuits.

DC ELECTRICAL CHARACTERIZATION

The recommended operating conditions and specifications under DC conditions are listed in Table 6.1. In establishing these DC electrical characteristics, VTC used the following equipment:

- HP4145A Parameter Analyzer to provide DC stimulus and response.
- Temptronic Thermostream to control thermal environment.
- Universal test fixture, described in this section, to make connections.

DC electrical tests for the parameters of Table 6.1 are described below:

V_{IH},V_{IL} are measured by sweeping one input from 0V to 5V while monitoring its corresponding output. V_{CC}=5.0V and all unused inputs are grounded. Unused outputs should float. If parameter analyzer oscillation is noticed during this measurement, insert a 0.1uF capacitor between the input and ground.

V_{OH},V_{OL} are measured by biasing one input to V_{CC} or ground to make the corresponding output high for V_{OH} or low for V_{OL}. Output current is then swept from 0 to 64mA while monitoring the output voltage. V_{CC}=4.5V and all unused inputs are grounded. Unused outputs should float.

I_I is measured by sweeping one input from 0V to 5.5V while monitoring current at that input. V_{CC}=5.5V and all unused inputs are grounded. All outputs should float.

V_{IK} is measured by sweeping an input from -18mA to +18 mA while monitoring the input voltage. V_{CC}=4.5V and all unused inputs are grounded. All outputs should float.

I_{OZ} is measured by sweeping an output from 0V to 5.5V while monitoring current at that output. V_{CC}=5.5V and all inputs are grounded. All outputs are 3-state, enable off.

I_{CC} is measured by sweeping all inputs from 0V to 5.5V while monitoring I_{CC}. V_{CC}=5.5V. All outputs should float.

TABLE 6.1: RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			Vcc+0.5	Vcc+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS		Military -55° to 125° C		Commercial -40° to 85° C		UNITS
				Typ	Guar	Typ	Guar	
V_{IH}	Minimum High Level Input Voltage				2.0		2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8		0.8	V
V_{OH}	Minimum High Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OH}\|$					
			20μA		4.4		4.4	V
			24mA		2.4		2.6	V
V_{OL}	Maximum Low Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OL}\|$					
			20μA		0.1		0.1	V
			32mA		0.5		0.4	V
			48mA		0.65		0.5	V
I_L	Maximum Input Leakage Current	Vcc=5.5V V_{IN} =Vcc or Gnd			±1.0		±1.0	μA
V_{IK}	Input Clamp Voltage	Vcc=4.5V	I_{IN}					
			-18mA		-1.2		-1.2	V
			18mA		Vcc+1.2		Vcc+1.2	V
I_{OZ}	Maximum Output Leakage Current	Vcc=5.5V V_{OUT} =Vcc or Gnd All Outputs Disabled		1.0	±10.0	0.5	±5.0	μA
I_{CC}	Maximum Quiescent Supply Current	Vcc=5.5V V_{IN} =Vcc or Gnd #All Outputs Disabled		10.0	160.0	10.0	120.0	μA
		*V_{IN} =2.0V		0.5	1.5	0.5	1.0	mA
		*V_{IN} =0.8V		0.5	1.5	0.5	1.0	mA

*Worst case leakage current at the TTL input receivers. One input only, all others tied to ground.
#Outputs floating, except for transceivers which must have outputs tied to Vcc or ground.

AC ELECTRICAL CHARACTERIZATION

The timing requirements and specifications under AC operating conditions are listed in Table 6.2. In establishing these AC electrical characteristics, VTC used the following equipment:

- HP8082A pulse generators for AC stimulus.
- HP54100D digital oscilloscope for AC response.
- HP54001A oscilloscope probes with 1 GHz bandwidth, 1 pF input capacitance, and 1 MΩ impedance.
- HP4275A LCR meter.
- Universal test fixture, described in this section, to make connections.

AC electrical tests for the values of Table 6.2 are described below:

T_{PLH}, T_{PHL} are the propagation delays measured between the 1.5V point on the input edge and the corresponding 1.5V point on the low-to-high or high-to-low output edge, as illustrated in Figure 6.5. They are measured with a load of 500Ω in parallel with a capacitive load of 50 or 300 pF.

T_{PZH}, T_{PZL} are the output enable times measured between the 1.5V point on the output control (high to low impedance) and the corresponding 1.5V point on the active high or active low output, as shown in Figure 6.4. They are measured with a capacitive load of 50 or 300 pF. A resistive load of 500Ω is tied to ground for T_{PZH} and V_{CC} for T_{PZL}. (See Figure 6.3 and Table 6.3.)

T_{PHZ}, T_{PLZ} are the output disable times measured between the 1.5V point on the output control (low-to-high impedance) and the V_{OH} - 0.5V or V_{OL} + 0.5V point on the corresponding disabled output, as shown in Figure 6.4. A capacitive load of 10 or 50 pF is tied to ground. A resistive load of 500Ω is tied to ground for T_{PHZ} and V_{CC} for T_{PLZ}. (See Figure 6.3 and Table 6.3.)

C_{IN},C_{OUT} are measured at an input or output with a capacitance meter. VTC uses a HP 4275A LCR meter set to a 1MHz signal frequency. V_{CC}=5V and all unused inputs are grounded. Outputs are disabled.

C_{PD} is the power dissipation capacitance. Power dissipation = $fC_{PD}V_{CC}{}^2n$, where f is frequency and n is the number of buffers. It is measured at 1MHz and V_{CC} = 5V.

T_S is the minimum setup time measured between D and C or D and CLK, as illustrated in Figures 6.1 and 6.2 for flip-flops and latches. Measurements start and end at the 1.5V points on the appropriate waveforms. A load of 500Ω is used in parallel with 50 or 300 pF to ground.

T_H is the minimum hold time measured between C and D or CLK and D, as illustrated in Figures 6.1 and 6.2 for flip-flops and latches. Measurements start and end at the 1.5V points on the appropriate waveforms.

T_W is the minimum input signal pulse width measured at C or CLK, as shown in Figure 6.7. The width is defined as the time between the 1.5V point on the leading edge of the pulse and the 1.5V point on the trailing edge.

F_{MAX} is the highest speed at which the circuit can toggle.

TABLE 6.2: AC ELECTRICAL CHARACTERISTICS

SYMBOL	*PARAMETER AND TEST CONDITIONS* *Input rise/fall times = 3ns* *All unused inputs = GND*		*LOAD CAP (pF)*
T_{PLH}	Propagation Delay Output Low to High Measured @ 1.5V Outputs 500 ohm to GND	Bus Driver A to Y	50/300
		Latch D to Q	50/300
		Latch C to Q	50/300
		Flip-Flop CLK to Q	50/300
T_{PHL}	Propagation Delay Output High to Low Measured @ 1.5V Outputs 500 ohm to GND	Bus Driver A to Y	50/300
		Latch D to Q	50/300
		Latch C to Q	50/300
		Flip-Flop CLK to Q	50/300
T_{PZH}	3-State Propagation Delay High Z to Active High Measured @ 1.5V Outputs 500 ohm to GND	Bus Driver G to Y	10/50
		Latch OC to Q	10/50
		Flip-Flop OC to Q	10/50
T_{PZL}	3-State Propagation Delay High Z to Active Low Measured @ 1.5V Outputs 500 ohm to Vcc	Bus Driver G to Y	10/50
		Latch OC to Q	10/50
		Flip-Flop OC to Q	10/50
T_{PHZ}	3-State Propagation Delay Active High to High Z Measured @ 1.5V Outputs 500 ohm to GND	Bus Driver G to Y	10/50
		Latch OC to Q	10/50
		Flip-Flop OC to Q	10/50
T_{PLZ}	3-State Propagation Delay Active Low to High Z Measured @ 1.5V Outputs 500 ohm to Vcc	Bus Driver G to Y	10/50
		Latch OC to Q	10/50
		Flip-Flop OC to Q	10/50
C_{IN}	Input Capacitance	Transceiver	50/300
		Buffer, Latch, Flip-flop	50/300
C_{OUT}	Output Capacitance	Buffer, Transceiver	50/300
		Latch, Flip-flop	50/300
C_{PD}	Power Dissipation Capacitance * (per buffer)	Transceiver	50/300
		Buffer, Latch, Flip-flop	50/300

TABLE 6.2 (CONT'D) TIMING REQUIREMENTS: INPUT t_r, $t_f \leq$ 3 nsec

SYMBOL	*PARAMETER AND TEST CONDITIONS* *Input rise/fall times = 3ns* *All unused inputs = GND*	
T_S	Minimum Setup Time Measured @ 1.5V Outputs 500 ohm to GND	Latch D to C
		Flip-Flop D to CLK
T_H	Minimum Hold Time Measured @ 1.5V Outputs 500 ohm to GND	Latch C to D
		Flip-Flop CLK toD
T_W	Minimum Pulse Width	Latch C
		Flip-Flop CLK
F_{MAX}	Maximum Frequency	

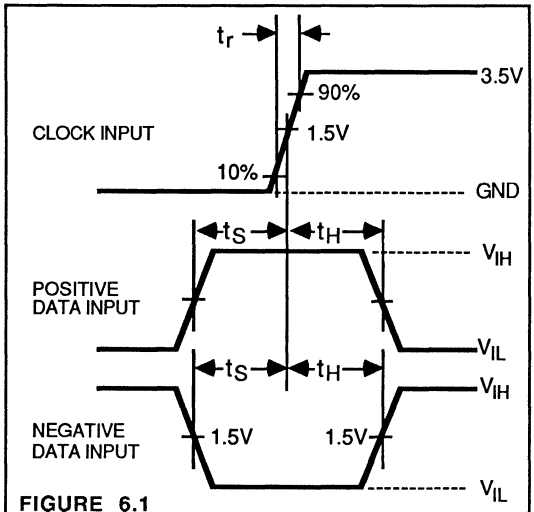


FIGURE 6.1
SETUP AND HOLD TIME WAVEFORMS FOR FLIP-FLOPS

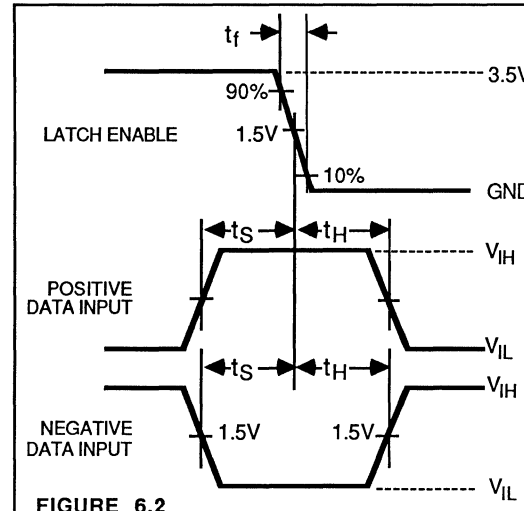


FIGURE 6.2
SETUP AND HOLD TIME WAVEFORMS FOR LATCHES

TABLE 6.3 3-STATE TEST PARAMETERS

PARAMETER	R_L	SWITCH
t_{PZH}	500 Ω	R_L to Gnd
t_{PZL}	500 Ω	R_L to V_{CC}
t_{PHZ}	500 Ω	R_L to Gnd
t_{PLZ}	500 Ω	R_L to V_{CC}
t_{PLH} or t_{PHL}	500 Ω	R_L to Gnd or R_L Open*

* Use this for capacitive loads only

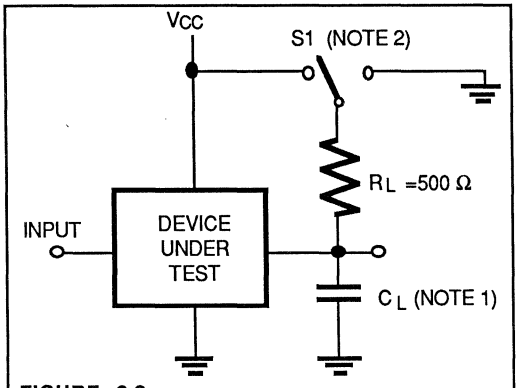


FIGURE 6.3
TEST CIRCUIT FOR 3-STATE OUTPUT TESTS

NOTE 1: C_L includes load and test jig capacitance.
NOTE 2: S1= V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1=Gnd for t_{PZH}, and t_{PHZ} measurements.

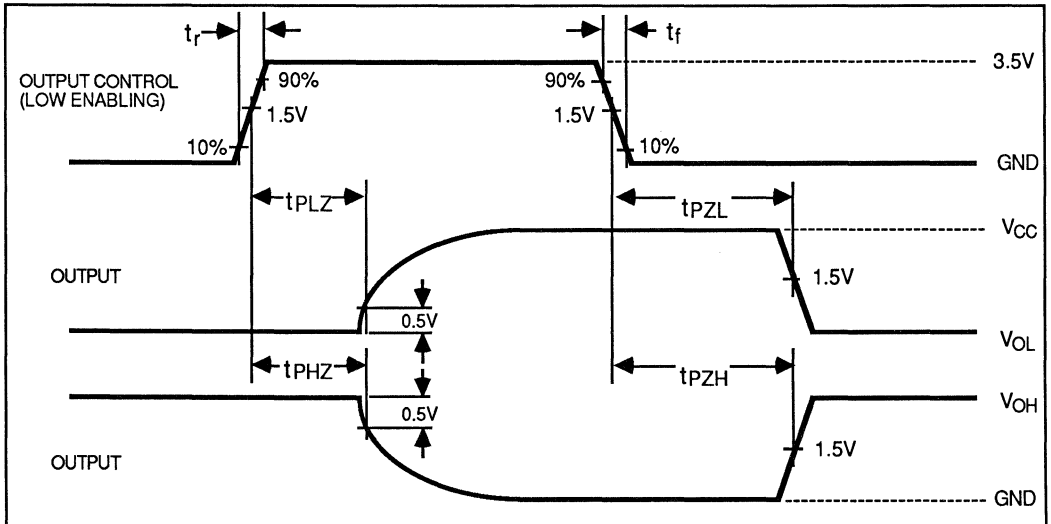


FIGURE 6.4
3-STATE OUTPUT ENABLE AND DISABLE WAVEFORMS

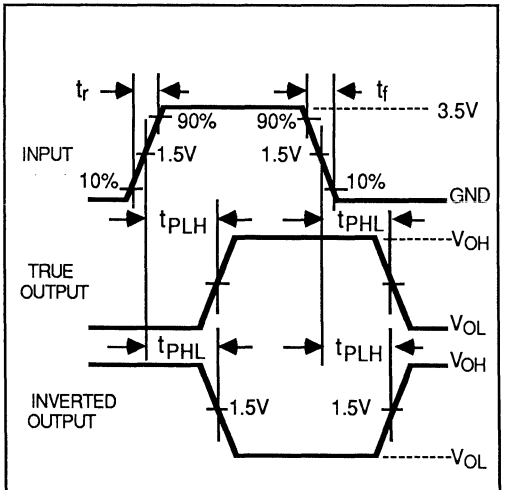


FIGURE 6.5
PROPAGATION DELAY WAVEFORMS

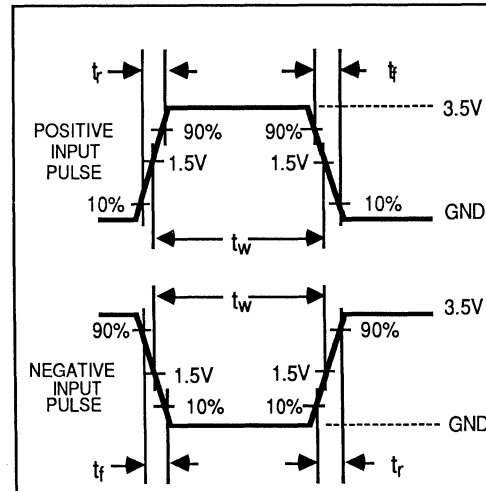


FIGURE 6.7
INPUT PULSE WIDTH WAVEFORMS

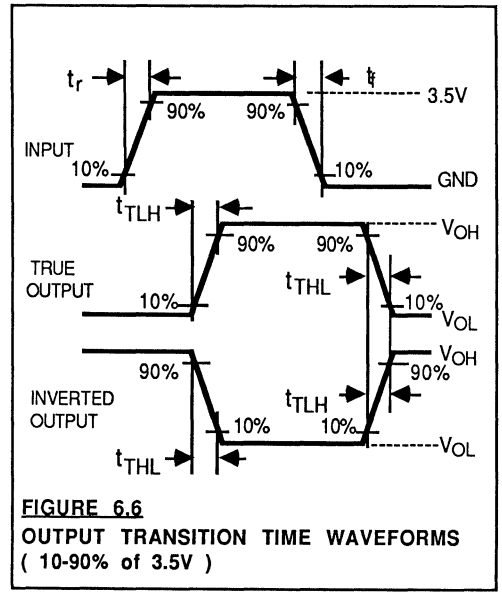


FIGURE 6.6
OUTPUT TRANSITION TIME WAVEFORMS (10-90% of 3.5V)

AC TEST JIGS AND SETUPS

V54/74ACT data sheets describe the waveforms, test loads, measurement points, etc. Test jigs, testing techniques, and equipment setups are not typically outlined; however, these items must be carefully considered.

DC evaluation is fairly easy to perform. Care should be taken when measuring very low leakage currents so that no other parallel leakage paths are present.

AC device evaluation is more difficult to perform due to the high frequencies involved. Output rise and fall times are very sharp. The effective sine wave equivalents of these edge rates are several hundred MHz. Close attention to RF phenomena is required.

Care must be taken when designing a test jig to minimize distortion of both input and output waveforms. Inductance, capacitance and characteristic impedance must be considered. The following items are important to proper jig construction.

GROUNDING

Improper grounding can be one of the biggest contributers to waveform degradation. Ground loops can be a major source of distortion when using PC boards. The VTC test jig uses a copper ground plane fastened to a 4" diameter aluminum ring. The test socket is mounted to the ground plane, with the ground pin soldered directly to it. This procedure will provide an

excellent ground and prevent ground loops. It will also provide a clean, low inductance, low resistance ground path.

DECOUPLING CAPACITORS

Very sharp output rise and fall times can cause high instantaneous current spikes on power supply lines. It is therefore necessary to filter all DC lines. High quality RF capacitors must be used to decouple the power supply lines on the test jig, running directly from the V_{CC} pin to the ground plane. For optimal performance, three capacitors with minimum lead length should be used in parallel. They are a 1μF dipped tantalum, a 0.1 μF dipped tantalum or ceramic, and a 0.002 μF ceramic.

WIRING

The next concern is getting the input signal to the device and the output signal to the measurement system. The most important consideration is to keep leads as short as possible to reduce reflections and inductance. Wires should be at least 18 guage to keep inductance low. All wires should be positioned close to the ground plane to maintain a constant impedance over the entire length. All leads must be equal in length to provide uniform delay.

JIG DELAY

The test jig will introduce a certain amount of delay, which must be taken into consideration when taking measurements. The input signal is sampled at the jig input. It takes a finite amount of time for this signal to travel to the device pin. This delay cannot be considered part of the device propagation delay, and must be subtracted. Similarly, as the output travels from the device output pin to the test jig output connector, there is another finite delay that must be subtracted from the measured device propagation delay.

VTC test jigs typically demonstrate 0.50-0.75ns delay times. It should be noted that the frequency response of the test jig must be high to prevent jig delay from varying with edge rates. Propagation delay of a transmission line is related to its characteristic impedance.

If the characteristic impedance of the jig changes over frequency, then delay per unit length will also change. Therefore, it is important to know how well the jig responds over frequency. Frequency response is also affected by the phase and magnitude of the impedance. An S-parameter set should be used to evaluate jig response. The characteristic impedance of the test jig in terms of a transmission line is:

$$Z_0 = V/I = \sqrt{(L_0/C_0)}$$

Z_0 is in Ohms
L_0 is in Henrys per unit length
C_0 is in Farads per unit length.

Propagation per unit length is expressed as:

$$\partial = \sqrt{(L_0 C_0)}$$

∂ is in nanoseconds
L_0 is in microhenrys per unit length
C_0 is in microfarads per unit length.

Phase and magnitude of the impedance also affect frequency response. S-parameter analysis is helpful to fully characterize test jigs.

UNIVERSAL JIG CONSTRUCTION

VTC test jigs are constructed using a Textool ZIF socket mounted in the center of a 4" copper disk. Socket pins are connected with 18 guage wire to BNC connectors equally spaced on a 4" diameter aluminum ring which mounts on the copper disc. Each wire is cut equal length and trimmed as short as possible. They are dressed close to the copper ground plane to maintain constant characteristic impedance. A photo of the test jig is shown in Figure 6.8.

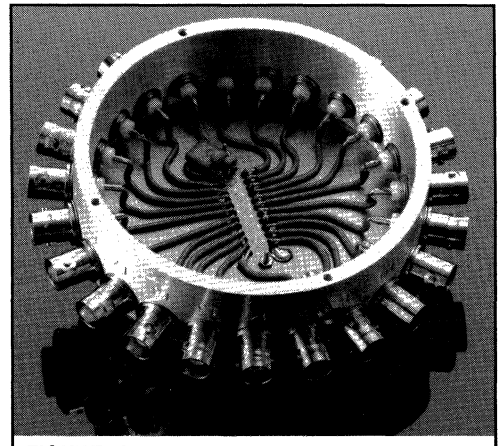


FIGURE 6.8
VTC TEST FIXTURE

It is important that the jig has a flat frequency response. An S-parameter analysis is helpful to optimize the jig design for frequencies needed to test

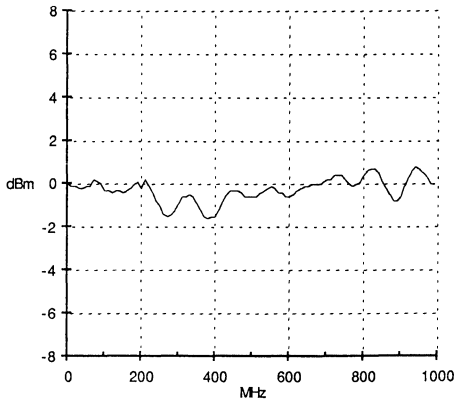


FIGURE 6.9

TRANSFER CHARACTERISTICS OVER FREQUENCY FOR VTC TEST FIXTURE

V54/74ACT devices. VTC test jig characterization results are shown in Figure 6.9. Equipment used to characterize the VTC test jig included: Tektronix 7L13 Spectrum Analyzer and HP 8656A Signal Generator.

AC TEST LOADS

V54/74ACT devices are specified at 50 and 300 pF load capacitance with a 500 ohm load resistance to ground. VTC uses Trompeter TNA2 BNC connectors with the total load mounted internally. To make a 50 pF load, one 15pF and two 12pF capacitors are mounted in parallel, resulting in a 39pF load. By using three capacitors the inductance is reduced and the series resonance is raised above 800 MHz. This, along with a 10pF jig capacitance and 1 pF probe capacitance, yields the necessary 50 pF load. A 1/8 watt 500 ohm resistor is also mounted internally to provide the required resistive load.

Characterization results showing transfer characteristics of the VTC load using one capacitor verses three smaller capacitors in parallel is shown in Figure 6.10. VTC uses three capacitors in parallel.

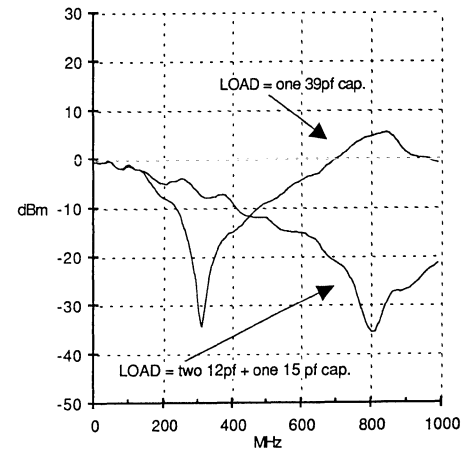


FIGURE 6.10

TRANSFER CHARACTERISTICS OF THE LOAD OVER FREQUENCY

CORRELATION

Many good ATE systems are available today. However, it is necessary to correlate ATE data with a fully characterized bench test jig. VTC uses the jig described in this section for correlation of all V54/74ACT devices. It is important that the user's test jig has similar characteristics for a good correlation with the data sheets.

NOTES

INTRODUCTION

VTC is dedicated to designing quality and reliability into every circuit. Two examples are the development of excellent latch-up and electrostatic discharge protection circuitry. These circuits have eliminated many of the hazards suffered by early CMOS technologies. It is useful to understand the latch-up and electrostatic discharge phenomena as well as VTC's protective circuitry.

The following explains in detail the effect of latch-up and electrostatic discharge phenomena. The preventive circuitry and test results achieved on V54/74ACT family of parts are also included in this section. The test results demonstrate the tolerance levels that are designed into the circuits.

LATCH-UP PHENOMENON

Latch-up is a parasitic phenomenon that is inherent in bulk CMOS technologies. When triggered, latch-up causes a large current to flow from V_{CC} to ground. This large current can cause system errors and possibly destroy the chip and other circuitry.

It is impossible to completely eliminate the possibility of latch-up from bulk CMOS. However, it is possible to make it extremely difficult for latch-up to occur in standard system enviroments. The V54/74ACT product family has been designed to be latch-up free with normal system design and operating conditions.

DISCRETE SCR FUNCTIONING

To understand the latch-up phenomenon, it is useful to first examine the discrete SCR structure. An SCR is a four-layer diode, as shown in figure 7.1A. The electrical characteristics are easily understood by treating the four-layer diode as two interconnected transistors, as shown in figures 7.1B and 7.1C.

If current started to flow in the base of transistor Q_A, this transistor would turn on and feed current into the base of Q_B. This base current would cause Q_B to draw current from the base of transistor Q_A. If the product of the two transistors' gains is greater than 1, this positive feedback causes the two transistors to keep each other going until they saturate and latch-up the device. With both transistors on, a large current will flow from the power supply to ground.

The DC conditions for latch-up can be initiated two ways. First, a current can be injected into the base of Q_A or Q_B. After latch-up has started, the injected current can be stopped because the positive feedback will keep the two transistors conducting. Second, the supply voltage can be increased until the reverse leakage currents are sufficient to trigger latch-up.

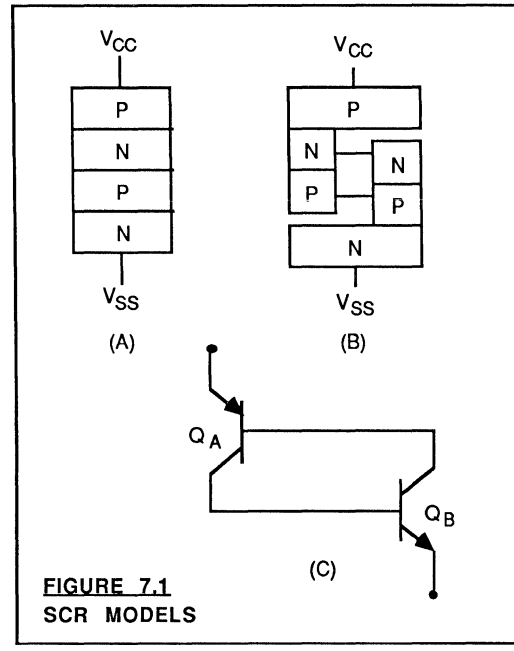


FIGURE 7.1
SCR MODELS

The AC conditions for latch-up are similar. The primary concern is the length of time the base current is injected. If the current pulse is very short, there will be insufficient time for the positive feedback to initiate latch-up. In general, the shorter the duration of the current pulse, the larger the magnitude of the current pulse needed to trigger latch-up.

CMOS SCR STRUCTURE

Although the SCR structures in bulk CMOS are similar to the discrete SCR, there are some important differences. A cross section of a CMOS inverter-like structure is shown in figure 7.2A along with the schematic of the corresponding parasitic elements. This SCR structure exists not only with the MOS transistors, but also with the input protect resistors and diodes. The schematic is very simplified. For accurate analysis, the transistors and resistors should be treated as distributed elements. For understanding the phenomenon and its solutions, the simplified schematic of figure 7.2B is sufficient.

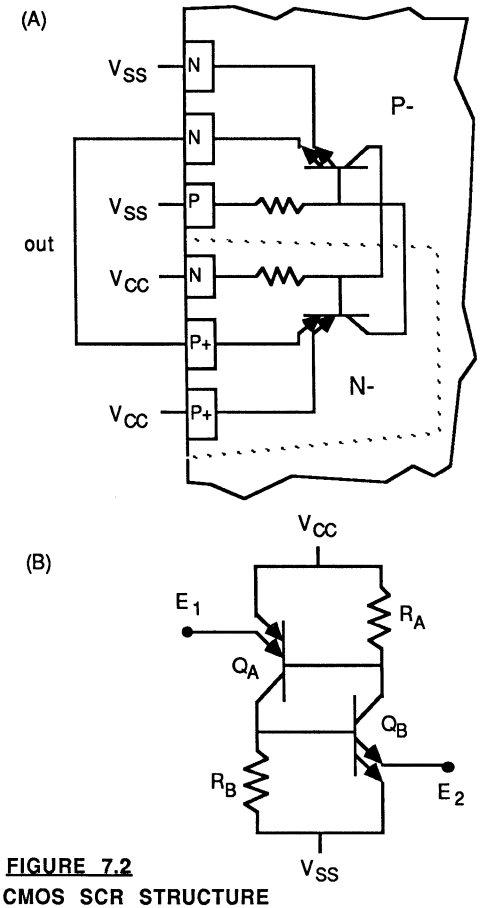


FIGURE 7.2
CMOS SCR STRUCTURE

The latch-up mechanism in the CMOS structure is similar to the discrete SCR structure. If current is flowing in the base of one of the transistors, that transistor will turn on and provide the base drive for the other transistor. If the gain product is greater than one, the positive feedback will keep the part latched-up.

There are two important differences that affect the CMOS SCR structure. The additional emitters on the two transistors, labeled E1 and E2 on the schematic, provide an additional mechanism to initiate latch-up. If the emitter E1 of Q_A is raised above V_{CC} by one diode drop, or the emitter E2 of Q_B is dropped below V_{SS} by one diode drop, the emitter base junction is forward biased. This allows a current to flow, which initiates the latch-up phenomenon.

The second difference is that the CMOS SCR structure contains two additional resistors R_A and R_B. The effect of these two resistors is to draw current away from the bases of the transistors. This effectively lowers the apparent gain of the two transistors and thus makes it harder to latch-up. If the resistances are low, a very large current must flow through both of the resistors to cause the base emitter junctions to forward bias and permit latch-up.

Considering the CMOS SCR as a part of a complete chip, there are three ways to trigger the latch-up.

1. Radiation induced latch-up.

A heavy ion going through a piece of silicon can generate a large amount of stray charge. This charge may be large enough to provide the base current necessary to initiate latch-up. In heavy radiation environments, special precautions and design strategies must be used. For most commercial environments, however, radiation that can cause latch-up will rarely exist.

2. Internally induced latch-up.

In very high speed circuits, the fast transitions of internal signals can cause voltage spikes and current injection. The voltage spikes can be due to signal bouncing from interconnect inductances. Charge can be injected into the substrate and wells due to depletion region movements. With the use of many precautions in design and process, as discussed later, the V54/74ACT part family does not latch-up due to internally induced circumstances.

3. Externally induced latch-up.

The primary concern to system designers is the externally induced latch-up. Each of the inputs and outputs on a CMOS circuit are eventually connected to diffusion regions. On the inputs, these are the clamping diodes and the input protection circuitry. On the outputs, these are the drains of the output transistors. These diffusions act as additional emitters E1 and E2, as shown on the schematic in figure 7.2B.

If any of these connections are brought outside the voltage rails, the base emitter junctions may become forward biased and start latch-up. Because of the precautions taken with the V54/74ACT family of parts, such a large current is needed that most systems are not capable of causing the parts to latch-up.

Because this is generally limited by current supply capability rather than voltage, the sensitivity to latch-up is generally characterized in terms of currents that must be injected into a pin to cause latch-up.

LATCH-UP PREVENTION

Latch-up protection and avoidance is a complex process. To insure that the V54/74ACT family of parts are sufficiently latch-up resistant for easy use, VTC undertook an extensive analysis of latch-up prevention design techniques. Because many of the means of reducing latch-up, if used alone, would degrade circuit performance, a multifaceted approach was needed to eliminate latch-up while maintaining the high performance of VTC CMOS circuits. The result of this program was a five point latch-up protection program.

1. CMOS processing.

When creating a discrete SCR, the doping of the junctions can be optimized to enhance latch-up operation. Similarly, the doping can be adjusted to impede latch-up. VTC has adjusted the CMOS process to minimize latch-up while maintaining high circuit performance.

2. Layout rules.

The gain of the lateral NPN transistor is affected by the length of the base region. Reducing the gain of parasitic transistors will reduce the feedback and thus make it more difficult to trigger latch-up. VTC used this concept to set up design rules that lowered the gain of this transistor while maintaining small die size to reduce cost.

3. Clamping diodes.

On all inputs and outputs there exist diodes to both supply rails. These diodes clamp the voltages to within one diode drop of the supply rails and draw off the current that could otherwise lead to latch-up. This greatly increases the amount of current needed to cause the part to latch-up. The diodes will also clip signal levels to help protect other parts from latch-up. The use of clamping diodes enhance the latch-up tolerance of VTC devices.

4. Guardbanding.

Guardbands are highly doped diffusions that connect either the bulk or well to one of the supply rails. The guardbands provide the connection from the base of the transistors to the supply lines and are represented by the resistors R_A and R_B in the schematic. Extensive use of the guardbands lowers the effective resistance of the two resistors. Extensive guardbanding is used in VTC's CMOS designs. This increases the amount of current necessary to trigger latch-up.

5. Power supply and signal isolation.

The output drivers can draw large amounts of current during switching. This causes signal and supply line to bounce. To keep this bouncing from causing latch-up problems with the rest of the circuitry, the output transistors and their supply lines are isolated from the rest of the chip circuitry.

These five precautions make the VTC parts practically immune to latch-up in most systems. This does not mean the user can neglect good system design practices. All chips must be supplied with stable power supplies. Signal lines should be short and terminated to avoid ringing and bounce.

TESTING FOR LATCH-UP

V54/74ACT are latch-up free under the following conditions:

1. The power supply voltage is a 5.5V maximum.This is the maximum recommended power supply voltage. Lower power supply voltages will reduce the latch-up susceptibility even further.

2. The maximum applied voltage to any pin is limited to 0.5V beyond either supply rail.

3. Temperature is limited to 125°C, the maximum permitted operating condition.

Two test circuits are used to measure latch-up characteristics. The circuit in figure 7.3A tests for positive current injection, the circuit in figure 7.3B is used for negative current injection. Except for the polarity of the voltages and currents, the tests for the two circuits are the same.

The current injected into a pin is supplied by the DC voltage source which is current limited to 400mA. Injected current is measured with an ammeter in line with the voltage source. The power supply which is connected to the circuit is also current limited to 800 mA. An ammeter is placed in line to measure the supply current to determine if the part has latched-up.

To test an output for latch-up due to positive injection, the test circuit in figure 7.3A is used. The input pins should be biased to provide a high output signal on the pin being tested. The input voltage is raised until the maximum input current, or maximum pin voltage, is reached. When the power supply current suddenly increases and cannot be decreased by

removing the input signal, the part is considered to have latched up.

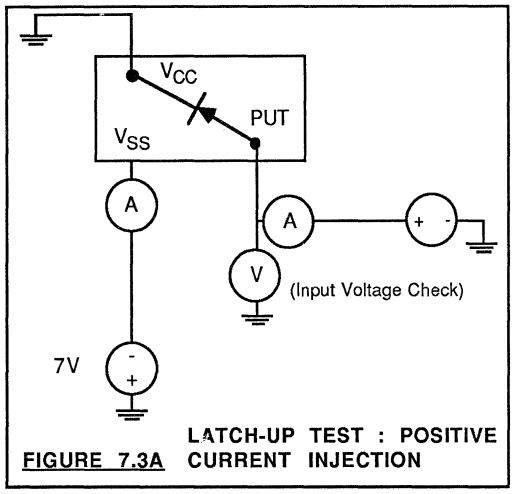


FIGURE 7.3A **LATCH-UP TEST : POSITIVE CURRENT INJECTION**

To test for negative injection latch-up on an output, the circuit in figure 7.3B is used. The inputs are biased to give a low voltage output on the pin being tested. The test is then the same as for positive injection except a negative input pulse voltage is used.

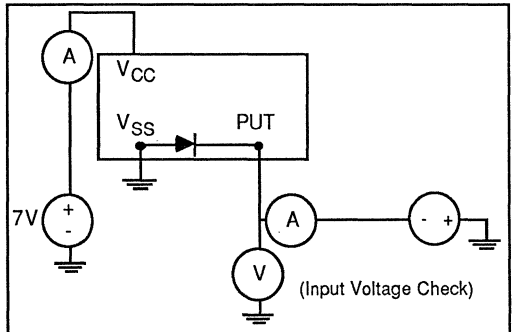


FIGURE 7.3B

LATCH-UP TEST: NEGATIVE CURRENT INJECTION

Inputs should be tested the same way as outputs. Bidirectional pins should be treated as output pins.

To cause latch-up will require currents and voltages that exceed the maximum allowed DC operating conditions. Sustained operation under these conditions could damage or destroy the part. Care should be taken to reduce the currents quickly after triggering latch-up. Any part forced to latch-up should not be used for production or further characterization.

TESTING ANALYSIS

The V54/74ACT parts have been extensively tested for latch-up characteristics. They have shown to be resistant to latch-up currents of up to 750mA, and have typical latch-up currents of 200mA at 125°C.

The test specifications and procedures define worst case latch-up conditions. Operating temperature will affect the amount of current necessary to trigger latch-up. Temperature affects the resistances and the gain of the bipolar transistors. Generally, as temperature increases, the amount of current needed to induce latch-up is reduced. Figure 7.4 illustrates this temperature dependence.

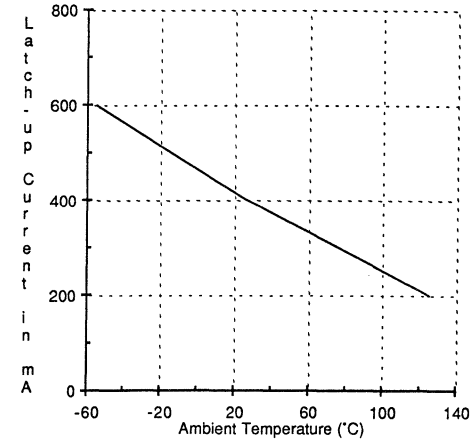


FIGURE 7.4

TYPICAL LATCH-UP CURRENT VS. TEMPERATURE

Figure 7.4 illustrates this temperature dependence.

The pulse width of the injected current will also affect the latch-up susceptibility. For short pulses, a much larger current is required to trigger latch-up. This is due to the poor frequency response of the SCR structure.

ELECTROSTATIC DISCHARGE PROTECTION

All MOS devices must have internal protection structures to guard against electrostatic discharge (ESD) damage to their input or output circuitry. The trend toward thinner oxides and smaller geometries has tended to increase the vulnerability of VLSI MOS circuits to damage from ESD. All V54/74ACT parts have protection that will meet MIL-STD-883C's highest specification for ESD protection. This specification defines these parts: "Category B devices may be ESD sensitive to damage in a range above 2000V, but normal good practice for the handling of semiconductors should suffice. Category B devices are preferred for use in military equipment because they require no special ESD packaging or handling precautions other than normal good practice for semiconductor devices."

VTC's ESD protection circuitry has been designed to guard against both current-induced damage and voltage-induced damage. The input protection circuit (patent pending) for all V54/74ACT parts is schematically illustrated in Figure 7.5. To guard against high ESD currents vaporizing conductors, no minimum metal widths are used as conductors from any bond pad. A resistor-diode is connected to the bondpad to limit the current and provide an RC delay to slow down discharge pulses. This delay provides time for the diodes and protection transistors to start conducting. Active area resistors (N-type) are used rather than poly-silicon resistors because the substrate provides an efficient heat sink for the resistors while polysilicon resistors are thermally and electrically isolated and therefore subject to vaporization.

When an ESD pulse is transferred from the bondpad to the diffusion resistor-diode, large currents will flow due to the junction going into avalanche breakdown. The bondpad metal to diffusion contact area is made very large to handle the high current. The large contact will reduce the localized heating, which would allow the aluminum to alloy through the junction bottom or sidewall.

The active area surrounding the contact is also made very large with rounded corners to reduce the electric field intensity and reduce current crowding. A strip of N-well is added under the bondpad metal to diffusion contact to extend the junction deeper therefore making it harder for the aluminum to alloy into the substrate. Polysilicon strips, which contact to the bondpad metal, are added to help "dope" the metal with more silicon to further reduce the chance of alloying by reducing the aluminum's affinity for silicon.

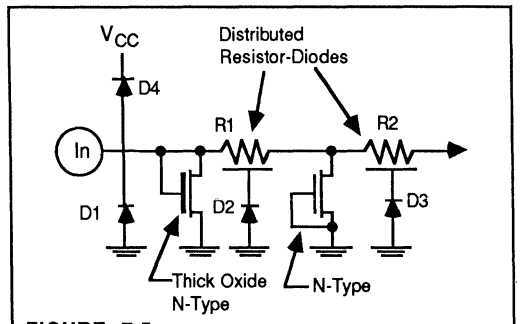


FIGURE 7.5
VTC'S INPUT PROTECTION CIRCUIT

The thick field oxide N-type transistor is made as large as possible in order to handle high peak currents. After turn-on or punch through, this transistor provides additional capacitance and a low-resistance path to ground through its source. In normal operation the channel of the field transistor does not conduct, so the source does not add to the input capacitance and slow down normal device operation. In effect, the field transistor has the nice property of adding significant capacitance only when it is needed for ESD protection.

A thin oxide N-type transistor to V_{SS} with the gate grounded is included to break down any remaining low voltage spikes via gate aided avalanche breakdown and punch-through to the source diffusion.

A diode (D4) to V_{CC} is included to clip any input signal which is greater than a diode drop over the supply and also to add breakdown protection for negative ESD pulses.

Testing is done according to MIL-STD-883C method 3015.2. A schematic of the test setup is illustrated in Figure 7.6. The capacitor is charged to 2000V and then discharged into the pin under test. This is repeated five times at five second intervals. This test is then repeated with the capacitor charged to -2000V. The part is then functionally tested to determine whether damage has occurred.

Testing is done between all of the following pin pairs:

1. Any input to ground.
2. Any output to ground.
3. Any input to any output pin.
4. Vcc to ground.

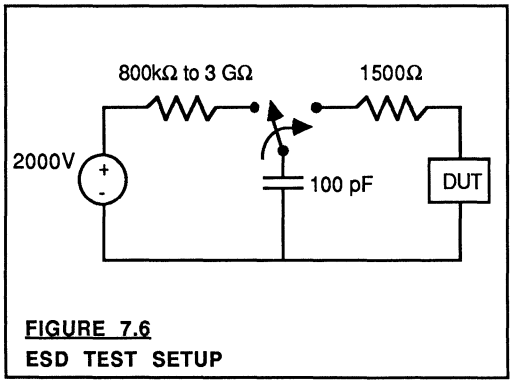


FIGURE 7.6
ESD TEST SETUP

Extensive testing has shown the V54/74ACT parts to have effective ESD protection up to 8000V. VTC will not release a design until it can reliably provide at least 2000V of ESD protection.

While the input protection provides good protection from ESD damage, it is not completely immune to ESD damage. Very large static voltage, 4KV to 15KV, can be generated by a person using the parts. Good handling practices should include:

1. Storing and transporting parts in anti-static or shielded containers.
2. Appropriately grounding all test and assembly benches and equipment.
3. Having all people who handle parts wear a grounded wrist strap.
4. Connecting low impedance test equipment to the inputs only after the part has been powered up.
5. Connecting all unused inputs to V_{CC} or ground.

COMPARISON OF ACT TO LS, S, AND ALS FAMILIES

INTRODUCTION

The V54/74ACT family of interface parts provides a speed and power advantage unmatched by any logic family. This family of interface parts is ideal for the highest performance applications. The V54/74ACT is fully upward compatible with the 'ALS' characteristics, both AC and DC specifications. Power dissipation of this family is orders of magnitude less than the comparable ALS or LS family of bipolar parts.

The V54/74ACT family spans the complete spectrum of interface parts in widths of octal, 9 bits, and 10 bits. The following logic functions are provided:

- Buffers
- Latches
- Flip-Flops
- Transceivers

The pin-outs are industry standard and are available in a variety of popular package styles. For more information on package styles, see Ordering and Packaging.

Although the functions and performances of the V54/74ACT are the same as the 54/74ALS, some of the electrical characteristics differ from the ALS-TTL, S-TTL, and AS-TTL. The following sections compare and discuss the common abilities and differences as they relate to the AC, DC, and power characteristics in the context of plug-in replacement of the TTL parts.

DC PERFORMANCE

The V54/74ACT logic family is designed to be fully TTL-compatible. Table 8.1 gives the detailed DC input characteristics of the V54/74ACT family. (Refer to section 5, DC Characteristics of the V54/74ACT Family, for more detail)

Figure 8.1 shows the quiescent supply current for various input voltage conditions. Note that the current peaks at around 1.2V and approaches 0 as V_{IN} approaches either 0 or V_{CC}. Therefore, to reduce DC power dissipation, the inputs should be located close to ground or V_{CC}.

A second difference between the TTL world and this family of parts is the output drive capability. For an output high, the output source capability is that of the output pull-up circuitry. Similarly, for an output low, the output sink capability is that of the output pull-down circuitry. Figures 8.2 and 8.3 show the I-V characteristics of both of these circuits. As can be seen from these curves, the output drive for pulling high or low is fairly balanced. At TTL voltages, this logic family is capable of sourcing and sinking very high DC currents.

A third difference is the fan-out capability of this family. Typical fanout for the V54/74ACT interface family is 4800 gates, 20 times greater than ALS. Since

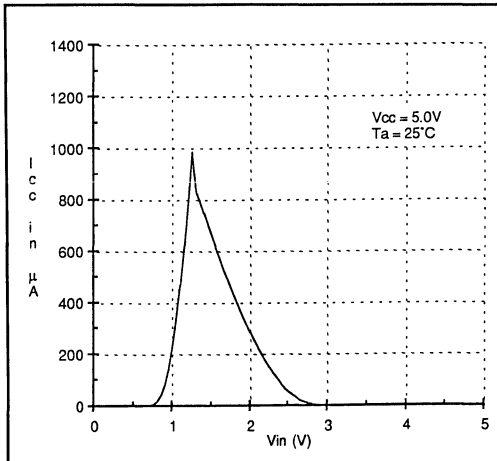


FIGURE 8.1
QUIESCENT SUPPLY CURRENT VS. INPUT VOLTAGE FOR V54/74ACT FAMILY

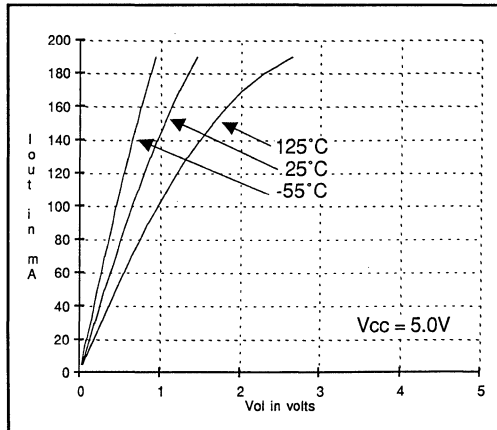


FIGURE 8.2
I-V CHARACTERISTIC FOR OUTPUT PULL-DOWN CIRCUITRY

the V54/74ACT family has CMOS transistors at their inputs, they sink very little current under DC conditions. This gives these parts the characteristics of almost ideal capacitive loads, having only a small amount of leakage

TABLE 8.1: RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			Vcc+0.5	Vcc+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS		Military -55° to 125° C		Commercial -40° to 85° C		UNITS
				Typ	Guar	Typ	Guar	
V_{IH}	Minimum High Level Input Voltage				2.0		2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8		0.8	V
V_{OH}	Minimum High Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OH}\|$					
			20μA		4.4		4.4	V
			24mA		2.4		2.6	V
V_{OL}	Maximum Low Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OL}\|$					
			20μA		0.1		0.1	V
			32mA		0.5		0.4	V
			48mA		0.65		0.5	V
I_L	Maximum Input Leakage Current	Vcc=5.5V V_{IN} =Vcc or Gnd			±1.0		±1.0	μA
V_{IK}	Input Clamp Voltage	Vcc=4.5V	I_{IN}					
			-18mA		-1.2		-1.2	V
			18mA		Vcc+1.2		Vcc+1.2	V
I_{OZ}	Maximum Output Leakage Current	Vcc=5.5V V_{OUT} =Vcc or Gnd All Outputs Disabled		1.0	±10.0	0.5	±5.0	μA
I_{CC}	Maximum Quiescent Supply Current	Vcc=5.5V V_{IN} =Vcc or Gnd #All Outputs Disabled		10.0	160.0	10.0	120.0	μA
		*V_{IN} =2.0V		0.5	1.5	0.5	1.0	mA
		*V_{IN} =0.8V		0.5	1.5	0.5	1.0	mA

*Worst case leakage current at the TTL input receivers. One input only, all others tied to ground.

#Outputs floating, except for transceivers which must have outputs tied to Vcc or ground.

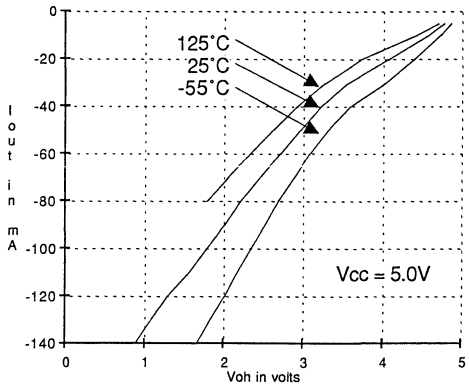


FIGURE 8.3
I-V CHARACTERISTIC FOR OUTPUT PULL-UP CIRCUITRY

current due to the reverse-biased diodes in the input protection circuitry.

AC PERFORMANCE

The V54/74ACT family has been designed for superior performance compared to the 54/74ALS and 54/74S families. Tables 8.2 through 8.5 compare the performance ratings of the V54/74ACT family with other logic families in reference to four distinct logic functions: buffers, latches, flip-flops, and transceivers.

Figure 8.4 shows the propagation delay variations for different capacitive loads. This clearly illustrates the high current drive capability of the V54/74ACT interface logic family. The V54/74ACT family has a much better drive capability than the ALS family, and is competitive with the Schottky family. The V54/74ACT family should be able to slip into any socket, in a reasonable situation, and perform without system degradation or timing problems, and allow an immediate decrease in system power.

PERFORMANCE

The V54/74ACT parts are specified for ease of use. The parts have typical specifications for room temperature as well as guaranteed specifications over the commercial and military ranges. The parts are specified at 50 pF and 300 pF loads for easy use in heavy load conditions. Specific performance under a given condition can be obtained by using the various derating curves for temperature, load, and drive currents.

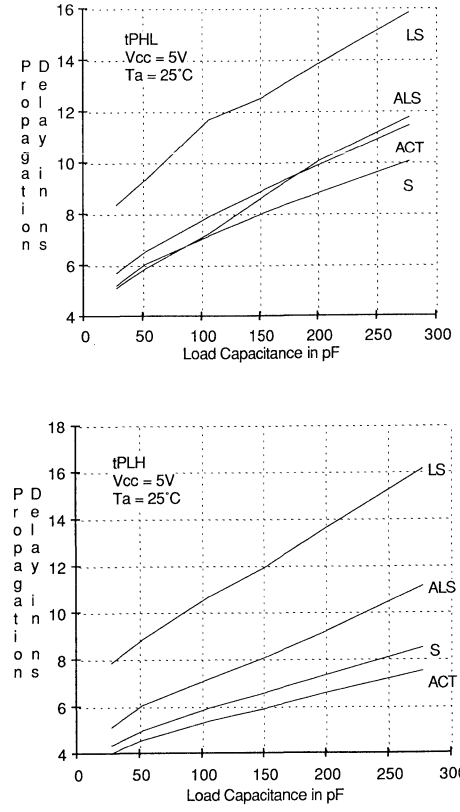


FIGURE 8.4
PROPAGATION DELAY VS. LOAD CAPACITANCE FOR ACT, ALS, LS, AND S FAMILIES

POWER DISSIPATION

Power dissipation is the most important reason for introducing this new family of interface circuits. The VT54/74ACT interface family utilizes state of the art CMOS technology fabrication with 1.6 micron features. The V54/74ACT interface family has the excellent power dissipation qualities of CMOS combined with the drive capabilities of bipolar. Table 8.6 compares typical static power consumption with the LS, ALS, and S-TTL.

TABLE 8.2: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 244 Octal Buffer and Line Driver with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay A to Y	Typical [25°C, 5V, C_L = 50pF]			14	5	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	10	6.2	25	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	13	9	30	12	ns
t_{PZH} Output enable time Enable to Y	Typical [25°C, 5V, C_L = 50pF]			15	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	20	9	38	12	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	25	10	45	14	ns

TABLE 8.3: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 373 Octal Transparent Latch with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay D to Q	Typical [25°C, 5V, C_L = 50pF]			22	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	12	6	37	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	14	8	45	12	ns
t_{PLH} Latch enable time Enable to Q	Typical [25°C, 5V, C_L = 50pF]			21	6	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	22	11.5	37	12	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	26	14	45	14	ns

TABLE 8.4: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 374 D-Type Edge-Triggered Flip-Flop with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay CLK to Q	Typical [25°C, 5V, C_L = 50pF]			22	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	12	8	37	13	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	15	11	45	15	ns
t_{PZH} Prop. Delay Output Enable to Q	Typical [25°C, 5V, C_L = 50pF]			21	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	17	6	37	14	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	19	7	45	16	ns

TABLE 8.5: COMPARISON TO OTHER STANDARD PRODUCT FAMILIES

Part Type: 245 Octal Bus Transceiver with Three-State Outputs						
Parameter	*Conditions*	*ALS*	*AS*	*HCT*	***V54/74ACT***	*Units*
t_{PLH} Prop. Delay A to B/B to A	Typical [25°C, 5V, C_L = 50pF]		6	14	5	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	10		29	10	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	15		34	12	ns
t_{PZH} Prop. Delay Output Enable to A/B	Typical [25°C, 5V, C_L = 50pF]		8	31	7	ns
	Guaranteed [85°C, 4.5V, C_L = 50pF]	20		53	13	ns
	Guaranteed [125°C, 4.5V, C_L = 50pF]	25		63	15	ns

TABLE 8.6
COMPARISON OF TYPICAL POWER DISSIPATION FOR A 245 UNDER STATIC LOAD

V74ACT	74ALS	74LS	74S	74HC
0.125 mW	65 mW	130 mW	500 mW	0.04 mW

CMOS power dissipation increases with frequency. The power dissipation with frequency can be evaluated with the following equation:

$$P_D = (C_{PD}+C_L)(f)V_{CC}^2 + I_{CC}V_{CC}$$

C_{PD} is the power dissipation within the device due to internal capacitances and switching currents.
C_L is load capacitance.
f is the frequency at which the system is switching.
I_{CC} is the quiescent supply current.
V_{CC} is the supply voltage.

Refer to section 3 on power dissipation for a detailed comparison using a design example.

Figure 8.5 shows curves for power dissipation versus frequency for an unloaded interface part. The LS, S, and ALS curves are essentially flat for lower frequencies. In this region, the quiescent currents mask out capacitive effects for the bipolar logic family. For low power TTL logic, as frequency increases, system power will become increasingly dependent on capacitive load effects, which are similar to CMOS for similar logic swings. Notice that the V54/74ACT parts never consume more power than TTL parts. It is possible that the V54/74ACT parts will converge with bipolar parts at some extremely high frequency, but since this frequency would be well above the maximum operating frequencies of the V54/74ACT and bipolar families it is impossible to measure. Thus, for all practical cases, the V54/74ACT family has low power dissipation compared to their bipolar counterparts, such as the LS and ALS series.

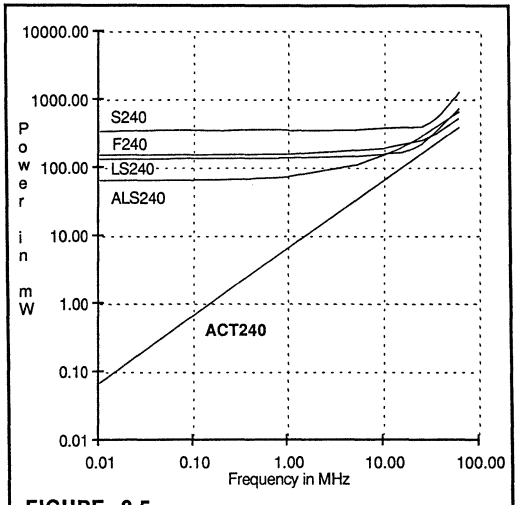


FIGURE 8.5
POWER DISSIPATION VS. FREQUENCY FOR AN UNLOADED 240

INPUT VOLTAGE CHARACTERISTICS

Figures 8.6A-C show the transfer function of the 240 gate for LS-TTL, ALS-TTL, and V54/74ACT. The V54/74ACT has a very sharp transition, typically at 1.4 V, and this transition point is fairly stable over temperature. The bipolar transfer functions are not as sharp, and vary over several hundred millivolts with temperature. This transfer characteristic improves noise immunity for the V54/74ACT family.

OPERATING TEMPERATURE RANGE

The operating temperature range and temperature effects are different for bipolar logic. The ALS and LS

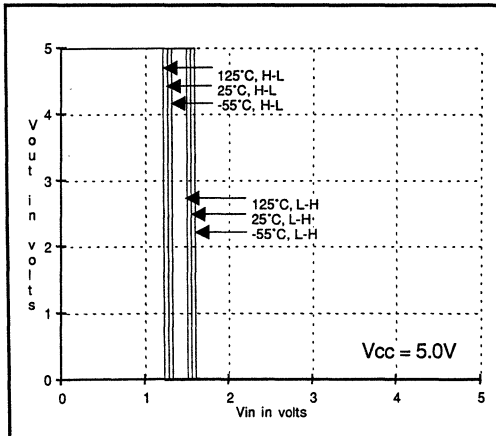


FIGURE 8.6A
TRANSFER FUNCTION FOR V74ACT240 GOING LOW-TO-HIGH AND HIGH-TO-LOW

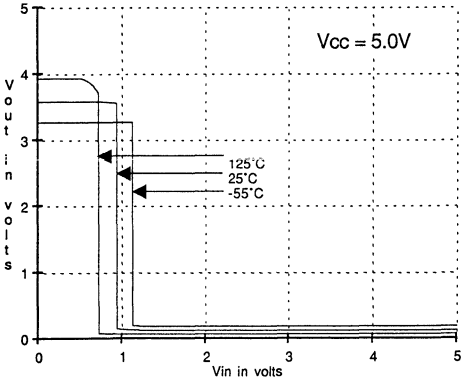


FIGURE 8.6B
TRANSFER FUNCTION FOR LS240 GOING HIGH-TO-LOW

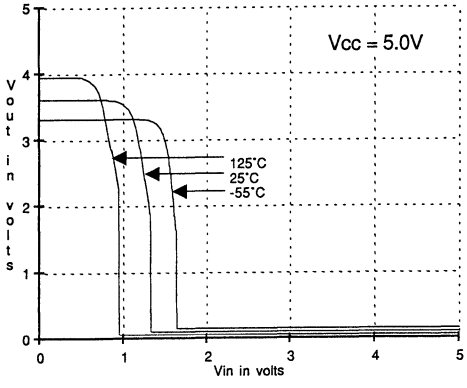


FIGURE 8.6C
TRANSFER FUNCTION FOR ALS240 GOING HIGH-TO-LOW

have a recommended operating range of 0° to 70°C. But the V54/74ACT family can operate down to -55°C. In fact, as temperature drops, the V54/74ACT family improves in performance and the quiescent supply currents are reduced. Figure 8.7 shows the derating of delay and current driving capability over temperature, of ALS and V54/74ACT.

The curves illustrate the degradation of the V54/74ACT family over temperature. This is much higher than the bipolar devices and can be an important design issue, especially when the machine is turned on cold. Care should be exercised to prevent race conditions from developing at low temperatures.

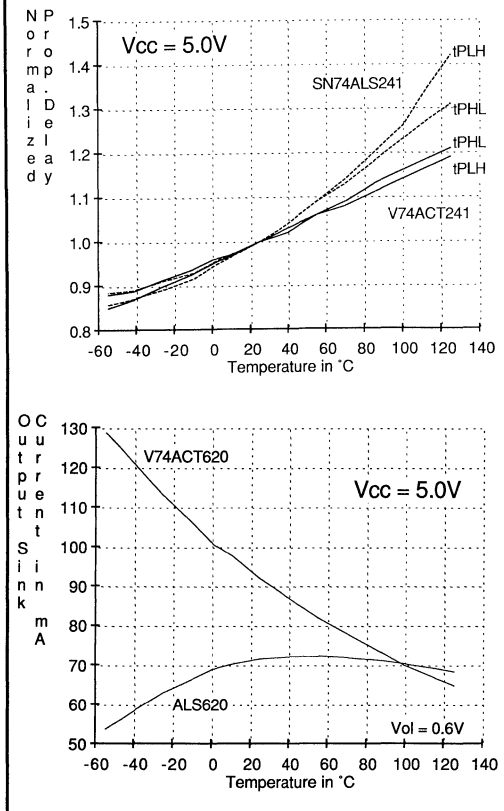


FIGURE 8.7
DERATING OF DELAY AND CURRENT DRIVING CAPABILITY OVER TEMPERATURE

CONCLUSION

The V54/74ACT family of interface parts has the best power and performance ratios of any family. They are pin compatible with ALS-TTL, LS-TTL, S-TTL, and HCT-CMOS. They are the ideal choice for systems that demand high performance interface parts. These parts are designed to supply the need for improved performance over the HCT series while maintaining the low power dissipation characteristics of typical CMOS parts.

NOTES

NOTES

A·C·T FAMILY
APPLICATION NOTES

A·C·T FAMILY DATA SHEETS

LINEAR SIGNAL PROCESSING

BIPOLAR SEMICUSTOM

QUALITY

ORDERING AND PACKAGING

TABLE OF CONTENTS
SECTION II

A.C.T. FAMILY DATA SHEETS

GENERAL CHARACTERISTICS

CMOS INTERFACE PARTS

BUFFERS

TRANSCEIVERS

LATCHES

FLIP-FLOPS

GENERAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage, VCC	-0.5V to +7.0V
Input Voltage	7.0V
Off-State Output Voltage	7.0V
Operating Free-Air Temperature	Military Temp -55°C to 125°C Commercial Temp -40°C to 85°C
Storage Temperature Range	-85°C to 150°C
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2000V

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 10%

SYMBOL	*PARAMETER*	*TEST CONDITIONS*		*Military -55° to 125° C*		*Commercial -40° to 85° C*		*UNITS*
				Typ	*Guar*	*Typ*	*Guar*	
V_{IH}	Minimum High Level Input Voltage				2.0		2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8		0.8	V
V_{OH}	Minimum High Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OH}\|$					
			20µA		4.4		4.4	V
			24mA		2.4		2.6	V
V_{OL}	Maximum Low Level Output Voltage	Vcc=4.5V V_{IN} = V_{IH} or V_{IL}	$\|I_{OL}\|$					
			20µA		0.1		0.1	V
			32mA		0.5		0.4	V
			48mA		0.65		0.5	V
I_L	Maximum Input Leakage Current	Vcc=5.5V V_{IN} =Vcc or Gnd			±1.0		±1.0	µA
V_{IK}	Input Clamp Voltage	Vcc=4.5V	I_{IN}					
			-18mA		-1.2		-1.2	V
			18mA		Vcc+1.2		Vcc+1.2	V
I_{OZ}	Maximum Output Leakage Current	Vcc=5.5V V_{OUT} =Vcc or Gnd All Outputs Disabled		1.0	±10.0	0.5	±5.0	µA
I_{CC}	Maximum Quiescent Supply Current	Vcc=5.5V V_{IN} =Vcc or Gnd #All Outputs Disabled		10.0	160.0	10.0	120.0	µA
		*V_{IN} =2.0V		0.5	1.5	0.5	1.2	mA
		*V_{IN} =0.8V		0.5	1.5	0.5	1.2	mA

*Worst case leakage current at the TTL input receivers. One input only, all others tied to ground.
#Outputs floating, except for transceivers which must have outputs tied to Vcc or ground.

Note 1: Maximum ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	nS
V_{IH}	High Level Input Voltage	2.0	2.0			Vcc+0.5	Vcc+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

WAVEFORM DEFINITIONS

TABLE 2 3-STATE TEST PARAMETERS

PARAMETER	R_L	SWITCH
t_{PZH}	500 Ω	R_L to Gnd
t_{PZL}	500 Ω	R_L to V_{CC}
t_{PHZ}	500 Ω	R_L to Gnd
t_{PLZ}	500 Ω	R_L to V_{CC}
t_{PLH} or t_{PHL}	500 Ω	R_L to Gnd or R_L Open*

*Use this for capacitive loads only

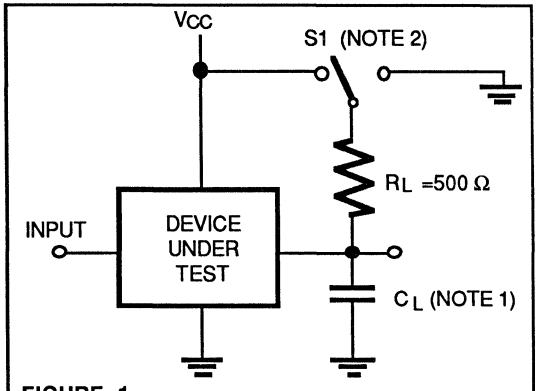


FIGURE 1
TEST CIRCUIT FOR 3-STATE OUTPUT TESTS

NOTE 1: C_L includes load and test jig capacitance.
NOTE 2: S1= V_{CC} for t_{PZL} , and t_{PLZ} measurements.
S1=Gnd for t_{PZH} , and t_{PHZ} measurements.

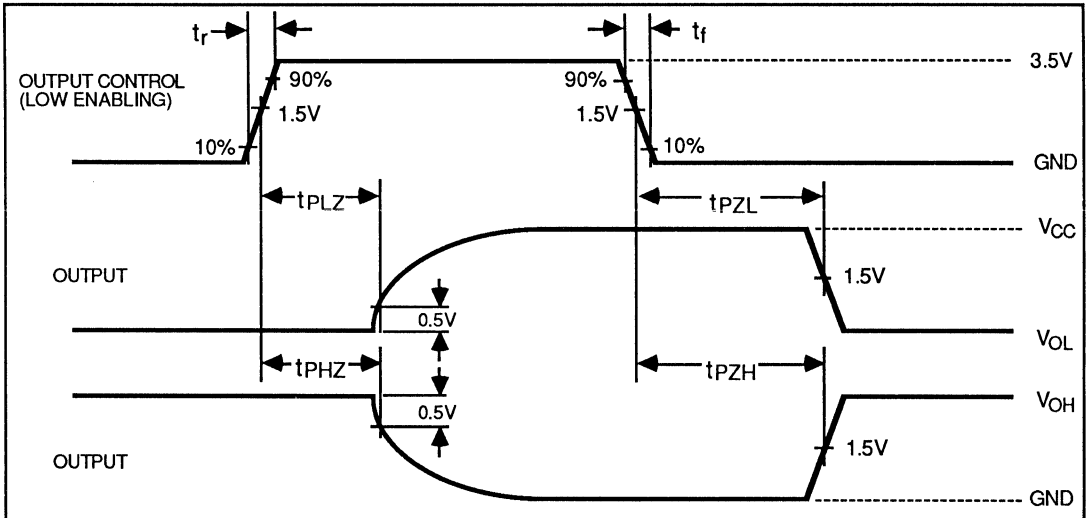


FIGURE 2
3-STATE OUTPUT ENABLE AND DISABLE WAVEFORMS

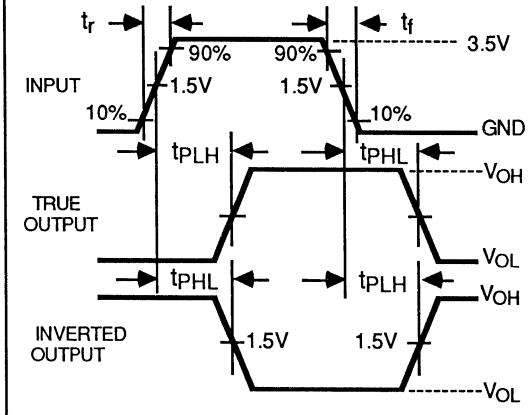


FIGURE 3
PROPAGATION DELAY WAVEFORMS

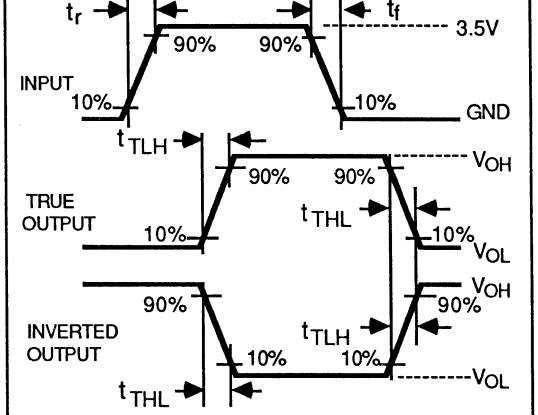


FIGURE 4
OUTPUT TRANSITION TIME WAVEFORMS
(10-90% of 3.5V)

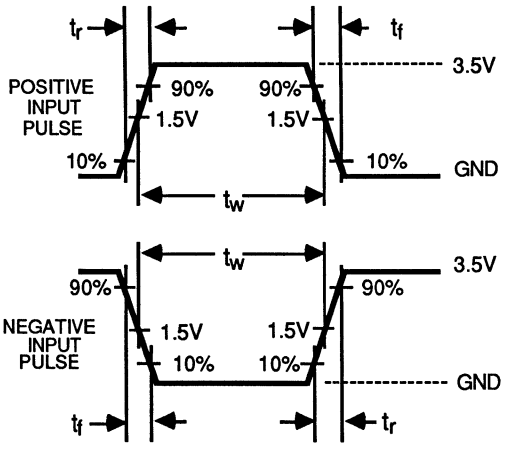


FIGURE 5
INPUT PULSE WIDTH WAVEFORMS

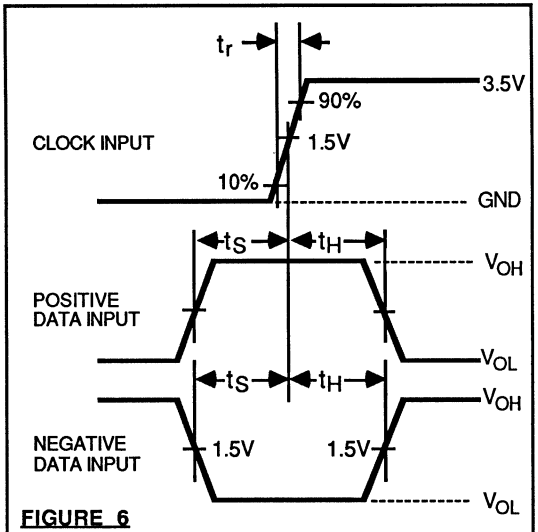


FIGURE 6
SETUP AND HOLD TIME WAVEFORMS FOR FLIP-FLOPS

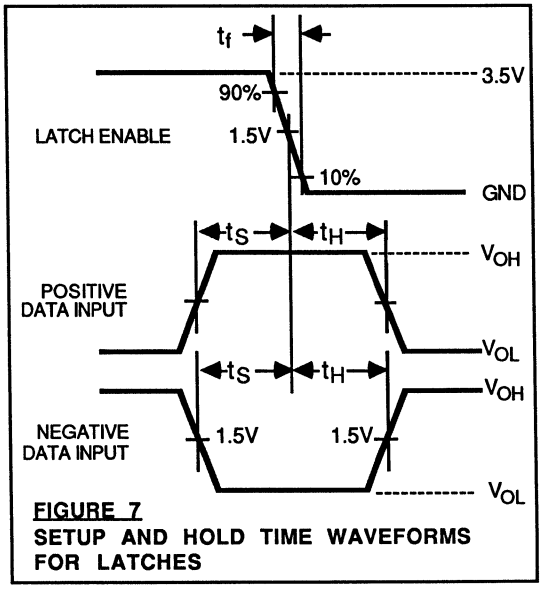


FIGURE 7
SETUP AND HOLD TIME WAVEFORMS FOR LATCHES

DERATING CURVES

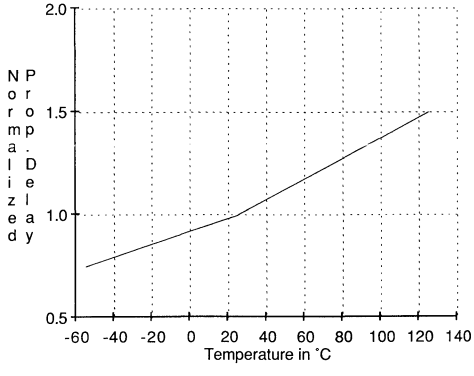


FIGURE 8
NORMALIZED PROPAGATION DELAY VERSUS TEMPERATURE AT 50 pF, 5V

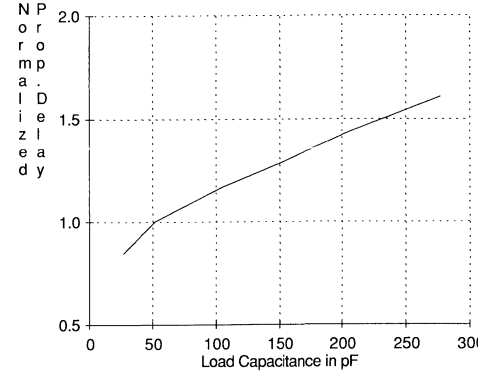


FIGURE 9
NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE AT 5V, 25°C

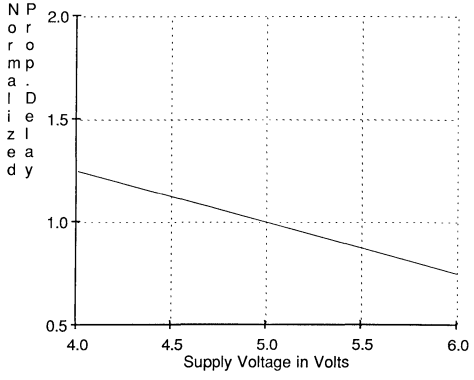


FIGURE 10
NORMALIZED PROPAGATION DELAY VERSUS SUPPLY VOLTAGE AT 50 pF, 25°C

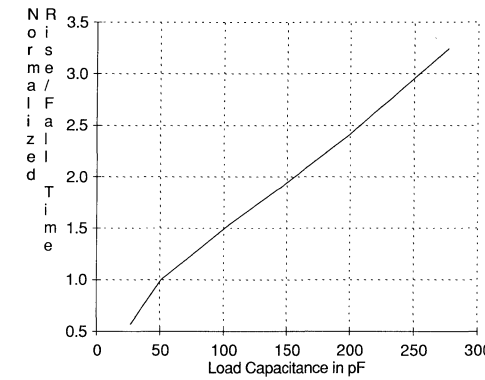


FIGURE 11
OUTPUT RISE/FALL TIME VERSUS OUTPUT LOAD CAPACITANCE

V54ACT240
V74ACT240
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

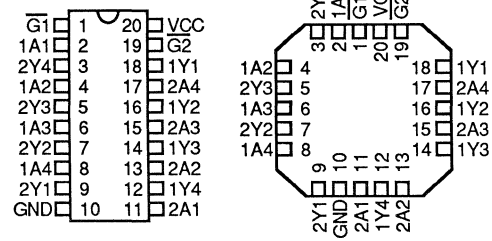
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are dual 4-bit inverting buffer drivers. $\overline{G1}$ and $\overline{G2}$ are the two separate enable lines. When $\overline{G}$ is low, the buffers are enabled and bus Y gets $\overline{A}$ values. A high value of $\overline{G}$ disables the buffers.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

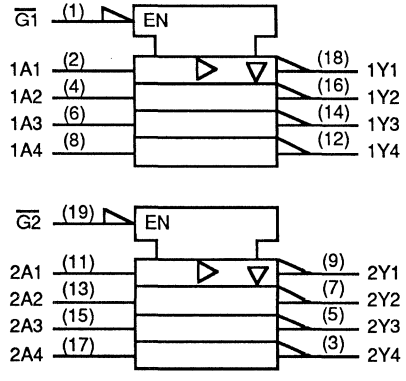
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

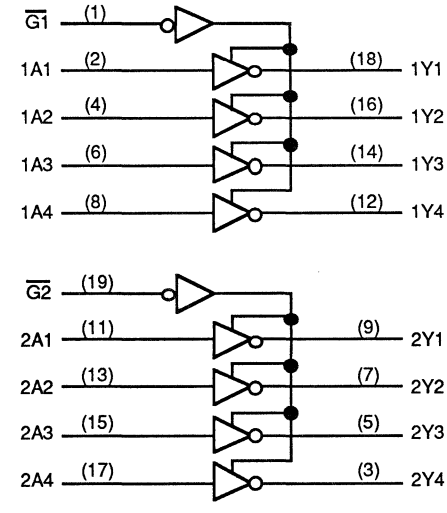
LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{Gi}$	Ai	Yi
H	X	Z
L	L	H
L	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	8	11	13	ns	3
		300	7	9	12	15	17	ns	3
t_{PHL}		50	3	5	7	9	12	ns	3
		300	7	9	12	15	17	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	9	12	14	ns	2
		300	6	9	11	14	16	ns	2
t_{PZL}		50	4	7	10	13	15	ns	2
		300	8	12	14	17	20	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	3	6	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{PLZ}		10	3	6	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	2.5	4	4	ns	4
		300	5	8	12	15	18	ns	4
t_{THL}		50	1	2	2.5	4	4	ns	4
		300	5	7	9	12	13	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT241
V74ACT241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

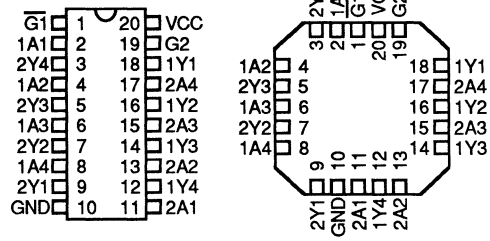
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are dual 4-bit line drivers, with separate enable lines. When $\overline{G}$ is low, the values on bus A are transmitted to bus Y. When $\overline{G}$ is high, the buffers are disabled and the two buses are isolated.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

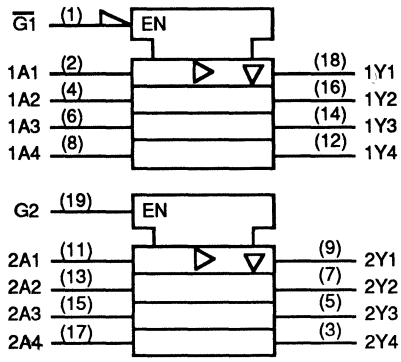
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

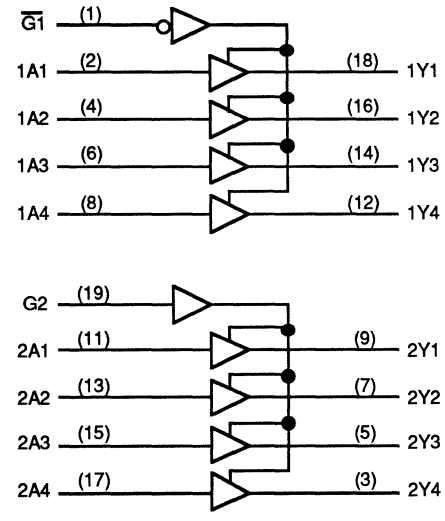
LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{G1}$	1Ai	1Yi	G2	2Ai	2Yi
H	X	Z	L	X	Z
L	H	H	H	L	L
L	L	L	H	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300	5	8	11	14	16	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	7	10	14	17	20	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	6	9	12	14	ns	2
		300	6	10	13	17	19	ns	2
t_{PZL}		50	4	7	10	13	15	ns	2
		300	7	11	15	19	22	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	4	6	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{PLZ}		10	4	6	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4.5	5	ns	4
		300	5	9	13	17	19	ns	4
t_{THL}		50	1	2	3	4.5	5	ns	4
		300	4	7	9	12	13	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT244
V74ACT244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

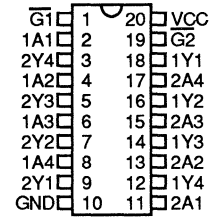
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

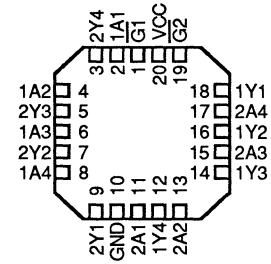
These are dual 4-bit line drivers, with separate enable lines. When $\overline{G}$ is low, the values on bus A are transmitted to bus Y. When $\overline{G}$ is high, the buffers are disabled and the two buses are isolated.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

CONNECTION DIAGRAMS

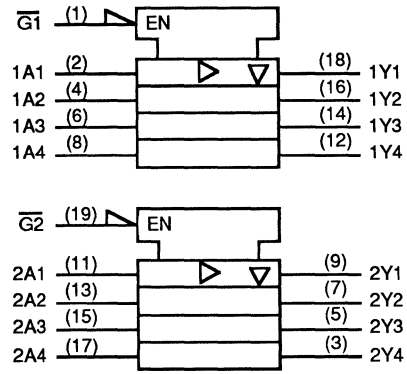


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

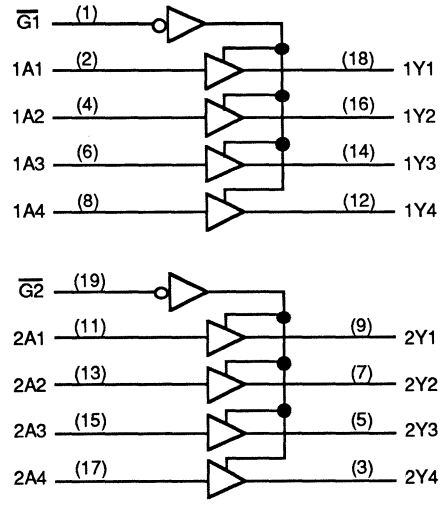
LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{G}i$	Ai	Yi
H	X	Z
L	L	L
L	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300	4	7	10	13	15	ns	3
t_{PHL}		50	3	7	9	12	14	ns	3
		300	5	10	15	19	22	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	6	9	12	14	ns	2
		300	5	9	12	15	17	ns	2
t_{PZL}		50	4	7	10	13	15	ns	2
		300	7	12	15	19	22	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	4	6	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	8	11	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	13	17	19	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	9	12	13	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT245
V74ACT245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

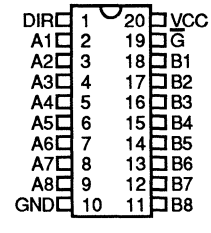
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

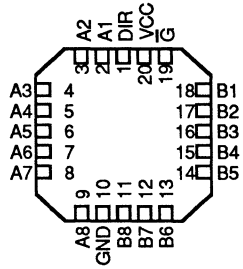
These 8-bit transceivers allow synchronous two way communication between data buses A and B. The DIR signal controls the direction of data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A. The $\overline{G}$ signal enables the buffer.

These parts are designed to interface with 3-state buses and I/O ports. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

CONNECTION DIAGRAMS

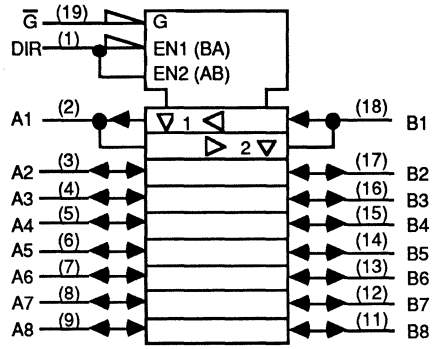


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

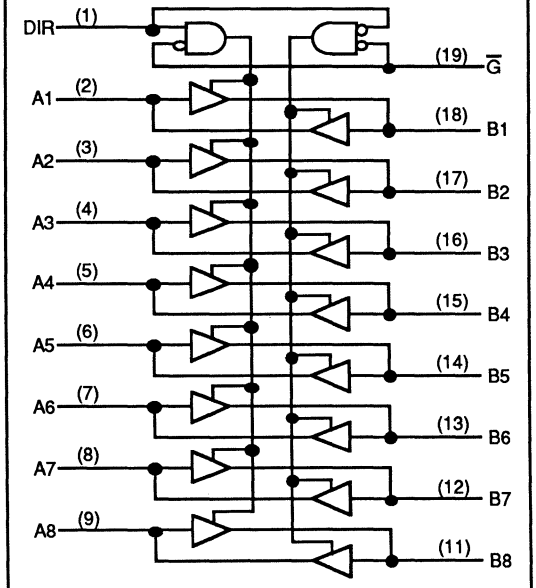
LOGIC SYMBOL



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	7	10	12	ns	3
		300	5	8	11	13	15	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	6	11	15	19	22	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	7	11	13	15	ns	2
		300	5	9	14	18	21	ns	2
t_{PZL}		50	4	8	12	15	17	ns	2
		300	8	12	17	21	24	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	13	17	19	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	9	12	13	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT373
V74ACT373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

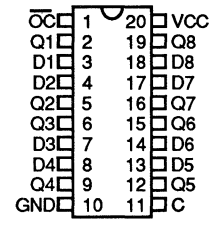
FUNCTIONAL DESCRIPTION:

These are 8-bit transparent D-type latches. While latch enable C is high, the latch output will follow the data input. The data at input D is latched when the enable is taken low.

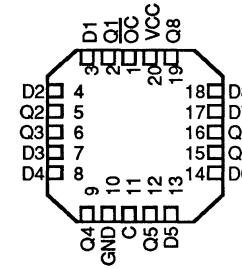
The $\overline{OC}$ output-control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

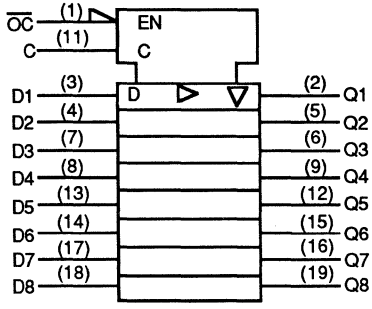


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

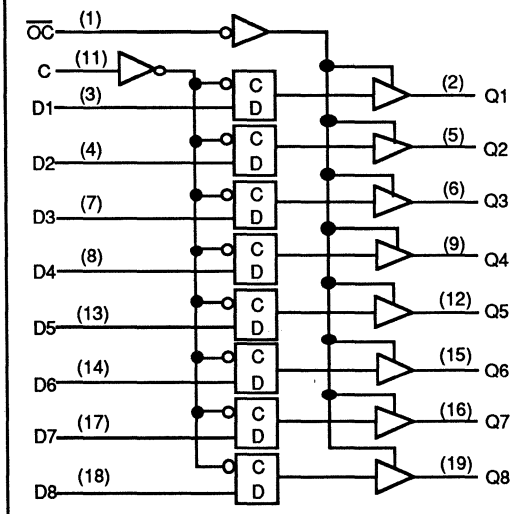
LOGIC SYMBOL



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	10	12	ns	3
		300	6	9	12	15	17	ns	3
t_{PHL}		50	4	7	9	12	14	ns	3
		300	7	11	16	20	24	ns	3
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	9	12	14	ns	3
		300	7	9	13	17	19	ns	3
t_{PHL}		50	4	6	9	12	14	ns	3
		300	7	10	15	19	22	ns	3
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	7	10	13	15	ns	2
		300	6	10	15	19	22	ns	2
t_{PZL}		50	4	9	12	15	17	ns	2
		300	7	11	18	24	37	ns	2
t_{PHZ}	Prop. Delay Output Disable to Q	10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT374
V74ACT374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

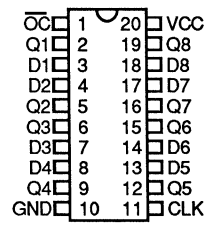
FUNCTIONAL DESCRIPTION:

These are 8-bit flip-flops which are edge triggered on the positive transition of the clock.

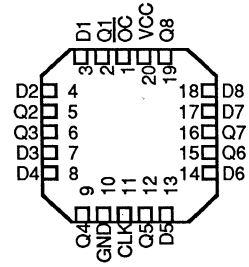
The $\overline{OC}$ control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

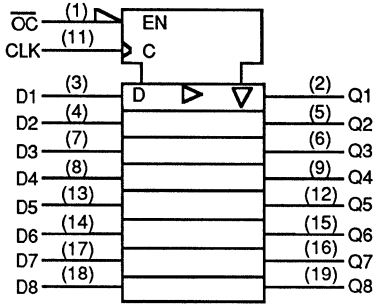


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

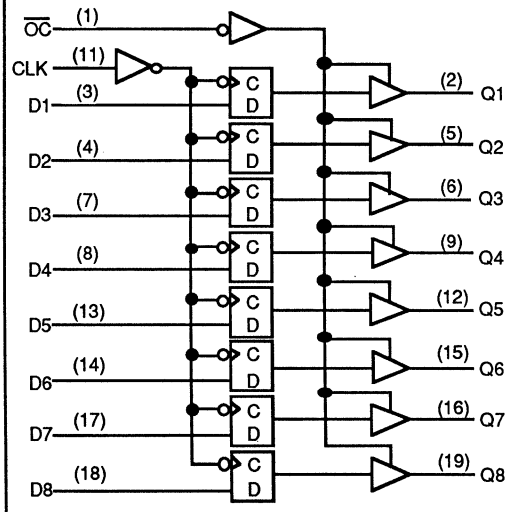
LOGIC SYMBOL



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Clock to Q	50	4	7	10	13	15	ns	3
		300	6	10	14	18	21	ns	3
t_{PHL}		50	4	7	10	13	15	ns	3
		300	9	13	16	20	24	ns	3
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	11	14	16	ns	2
		300	6	11	16	20	24	ns	2
t_{PZL}		50	4	8	12	15	17	ns	2
		300	7	14	19	24	28	ns	2
t_{PHZ}	Prop. Delay Output Disable to Q	10	3	5	8	10	12	ns	2
		50	5	7	10	13	15	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	5	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	6	8	15	19	22	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	6	11	14	16	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT465
V74ACT465
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

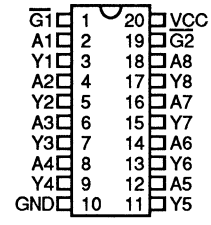
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

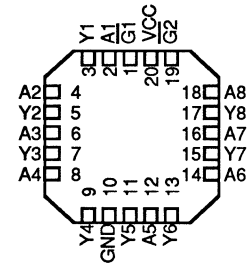
This is an octal line driver with dual control lines. When both $\overline{G1}$ and $\overline{G2}$ are low, the buffers are enabled and the value on bus A is driven to bus Y.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

CONNECTION DIAGRAMS

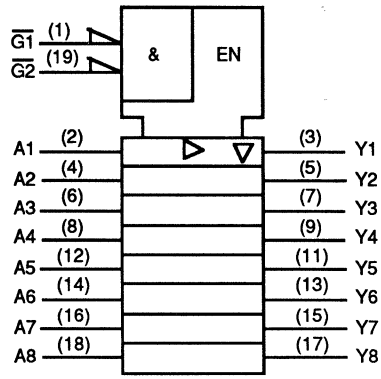


DIP and SOIC (Top View)



PLCC and LCC (Top View)

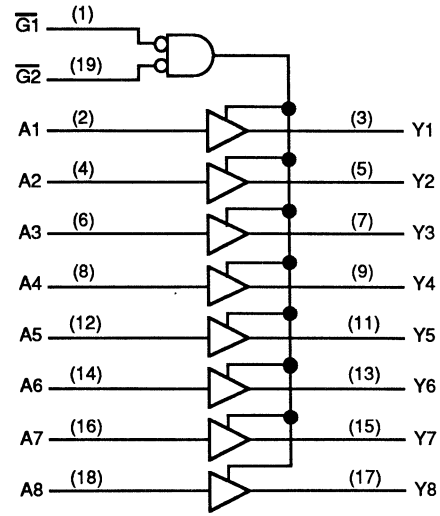
LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{G1}$	$\overline{G2}$	Ai	Yi
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	L
L	L	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300	6	8	11	14	16	ns	3
t_{PHL}		50	3	7	9	12	14	ns	3
		300	6	10	14	18	21	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	10	13	15	ns	2
		300	6	10	14	18	21	ns	2
t_{PZL}		50	4	8	11	14	16	ns	2
		300	8	12	18	24	27	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	4	6	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	4	6	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	6	9	15	18	20	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	6	10	12	14	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT466
V74ACT466
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

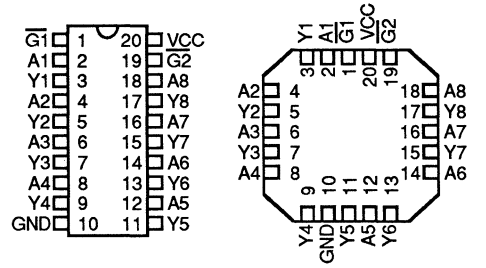
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

This is an inverting octal line driver with dual control lines. When both $\overline{G1}$ and $\overline{G2}$ are low, the buffers are enabled and the inverted value on bus A is driven to bus Y.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatable with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

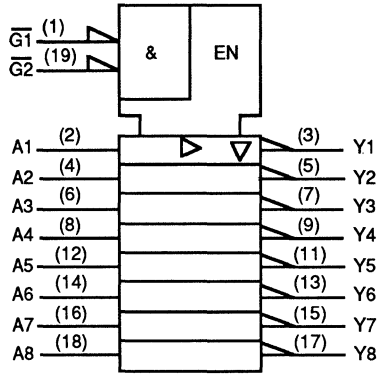
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

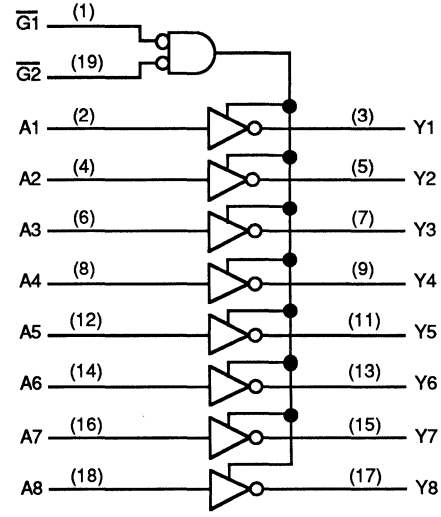
LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{G1}$	$\overline{G2}$	Ai	Yi
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	H
L	L	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	7	9	12	14	ns	3
		300	6	10	13	17	20	ns	3
t_{PHL}		50	3	6	8	10	12	ns	3
		300	7	11	14	18	21	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	11	14	16	ns	2
		300	8	12	15	19	22	ns	2
t_{PZL}		50	4	7	12	15	17	ns	2
		300	10	14	18	24	27	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	3	5	10	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	7	10	13	17	20	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	10	13	15	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT467
V74ACT467
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

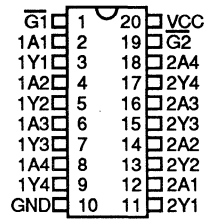
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1µA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

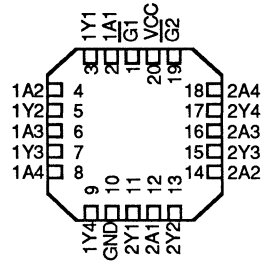
These are dual 4-bit line drivers, with separate enable lines. When enable is low, the values on bus A are transmitted to bus Y. When $\overline{G}$ is high, the buffers are disabled.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

CONNECTION DIAGRAMS

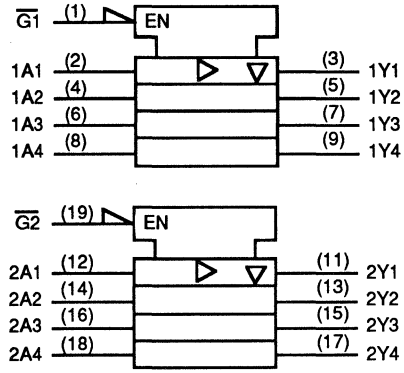


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

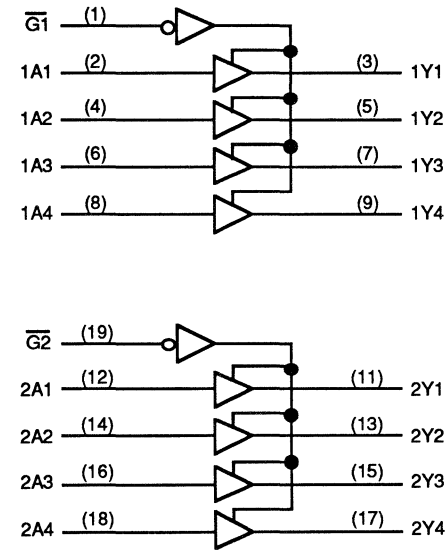
LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{G}i$	Ai	Yi
H	X	Z
L	L	L
L	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300	5	8	11	14	16	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	8	12	15	19	22	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	9	12	14	ns	2
		300	6	10	12	15	17	ns	2
t_{PZL}		50	4	8	10	13	15	ns	2
		300	8	12	15	19	22	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	7	11	14	18	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	10	13	15	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT468
V74ACT468
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

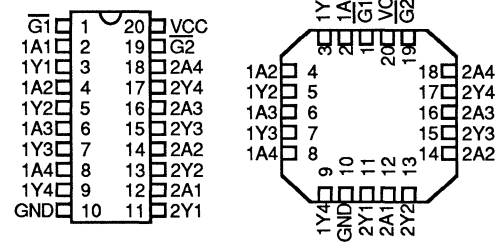
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are dual 4-bit inverting buffer drivers. $\overline{G1}$ and $\overline{G2}$ are the two separate enable lines. When $\overline{G}$ is low, the buffers are enabled and bus Y gets A values. A high value of $\overline{G}$ disables the buffers.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

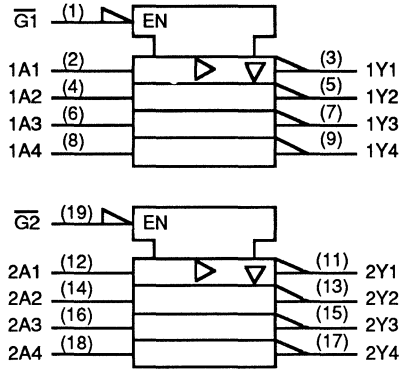
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

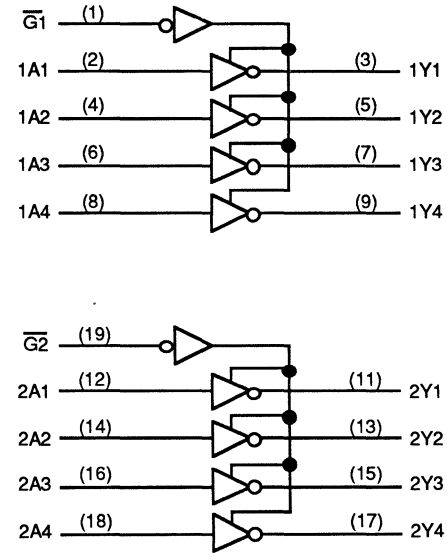
LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{Gi}$	Ai	Yi
H	X	Z
L	L	H
L	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	9	12	14	ns	3
		300	6	10	13	17	20	ns	3
t_{PHL}		50	3	5	8	10	12	ns	3
		300	7	11	14	18	21	ns	3
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	10	13	15	ns	2
		300	6	10	13	17	20	ns	2
t_{PZL}		50	4	7	11	14	16	ns	2
		300	9	13	16	20	24	ns	2
t_{PHZ}	Prop. Delay Output Disable	10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	7	11	14	18	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	10	13	15	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			25	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT533
V74ACT533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

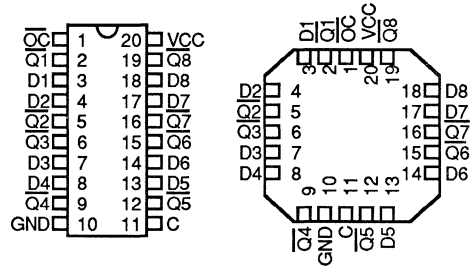
FUNCTIONAL DESCRIPTION:

These are 8-bit transparent D-type latches of the inverting type. While the latch enable C is high, the latch output will follow the inverse of the data input. The data at input D is latched when the enable is taken low.

The $\overline{OC}$ output-control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

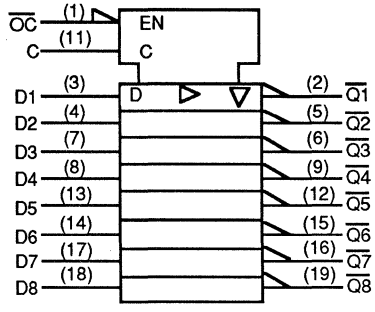
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

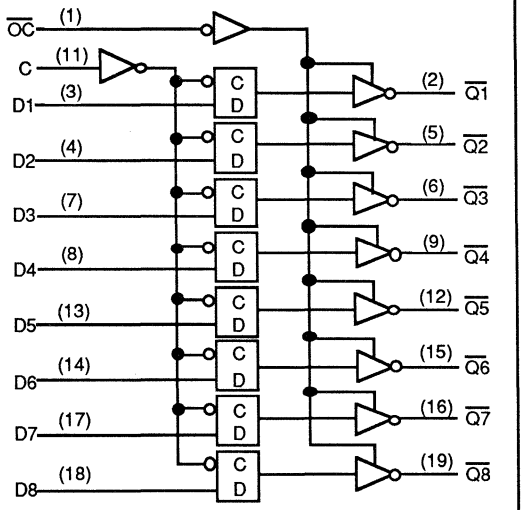
LOGIC SYMBOL



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Input D to Q	50	4	7	10	13	15	ns	3
		300	6	10	14	18	21	ns	3
t_{PHL}		50	4	6	9	12	14	ns	3
		300	7	11	15	19	22	ns	3
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	9	12	14	ns	3
		300	6	10	13	17	21	ns	3
t_{PHL}		50	4	7	10	13	15	ns	3
		300	7	12	16	21	24	ns	3
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	7	11	14	16	ns	2
		300	6	10	15	19	22	ns	2
t_{PZL}		50	4	7	12	15	17	ns	2
		300	8	13	18	24	27	ns	2
t_{PHZ}	Prop. Delay Output Disable to Q	10	3	5	8	10	12	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	8	8	8	10	12	ns	5

V54ACT534
V74ACT534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

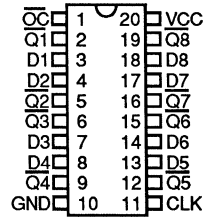
FUNCTIONAL DESCRIPTION:

These 8-bit registers invert the data between input and output. The data is latched by the positive edge transition of the clock. The inverted data appears at the output $\overline{Q}$'s when enabled by the output-control signal $\overline{OC}$.

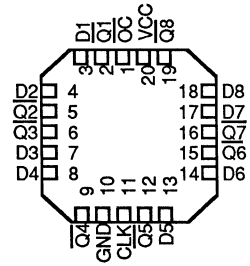
The $\overline{OC}$ output-control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

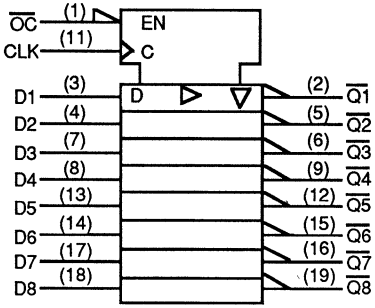


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

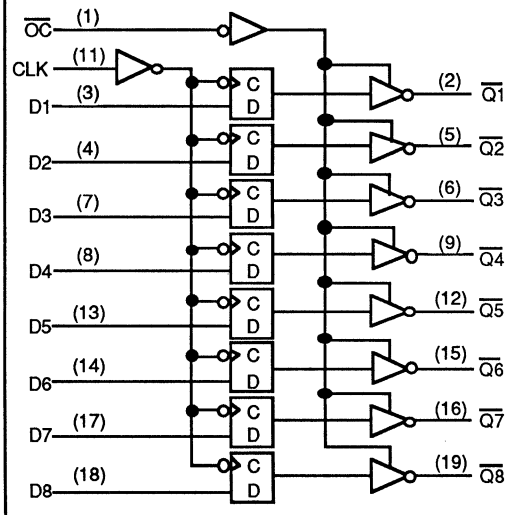
LOGIC SYMBOL



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300	6	8	13	17	20	ns	3
t_{PHL}		50	4	6	10	13	15	ns	3
		300	8	12	16	20	24	ns	3
t_{PZH}	Prop. Delay Output Enable to Q	50	4	8	11	14	16	ns	2
		300	7	11	16	20	24	ns	2
t_{PZL}		50	4	8	12	15	17	ns	2
		300	8	13	19	24	28	ns	2
t_{PHZ}	Prop. Delay Output Disable to Q	10	3	5	8	10	12	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	3	6	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	6	9	15	19	22	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	6	10	13	15	ns	4
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT540
V74ACT540
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

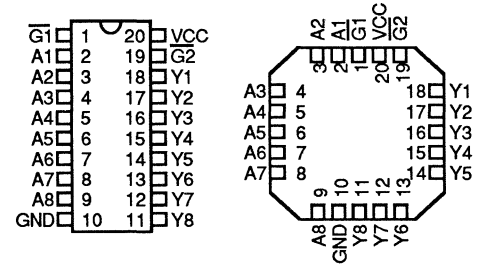
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1µA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

This is an inverting octal line driver with dual control lines. When both $\overline{G1}$ and $\overline{G2}$ are low, the buffers are enabled and the inverted value on bus A is driven to bus Y.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

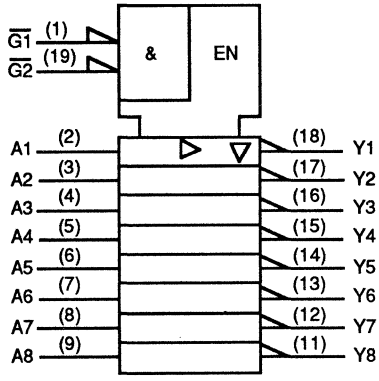
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

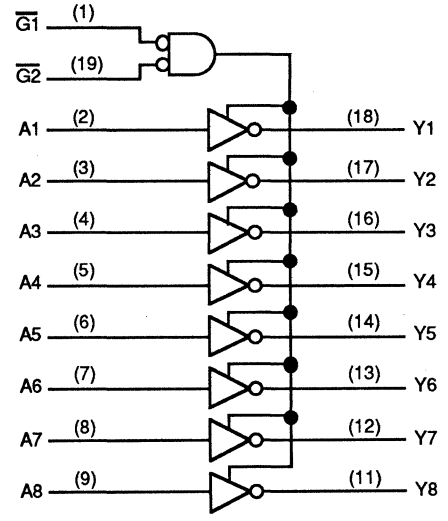
LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{G1}$	$\overline{G2}$	Ai	Yi
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	H
L	L	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300						ns	
t_{PHL}		50	3	5	8	11	13	ns	3
		300						ns	
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	8	11	13	ns	2
		300						ns	
t_{PZL}		50	4	7	9	12	14	ns	2
		300						ns	
t_{PHZ}	Prop. Delay Output Disable	10	4	7	10	13	15	ns	2
		50						ns	
t_{PLZ}		10	4	7	9	12	14	ns	2
		50						ns	
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300						ns	
t_{THL}		50	1	2	3	4	5	ns	4
		300						ns	
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			25	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT541
V74ACT541
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

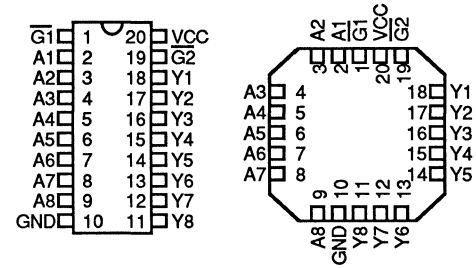
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

This is an octal line driver with dual control lines. When both $\overline{G1}$ and $\overline{G2}$ are low, the buffers are enabled and the value on bus A is driven to bus Y.

This octal high performance interface family is designed for high capacitance, low impedance load drive. It is compatible with TTL I/O and ALS performance. These features are ideal for bus oriented interface buffering, memory drives, and clock or line drives.

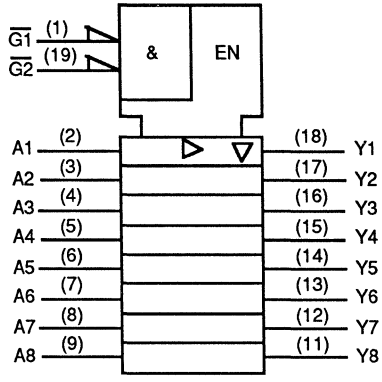
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

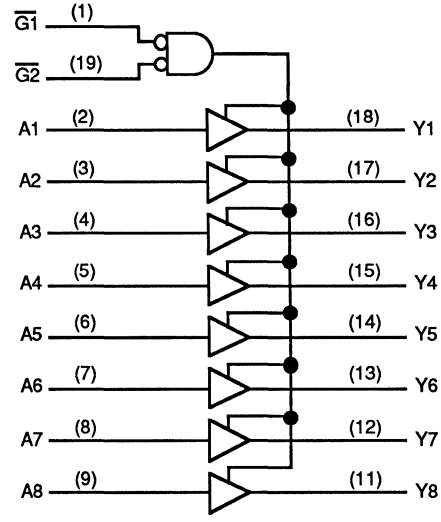
LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{G1}$	$\overline{G2}$	Ai	Yi
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	L
L	L	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300						ns	
t_{PHL}		50	3	5	8	11	13	ns	3
		300						ns	
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	8	11	13	ns	2
		300						ns	
t_{PZL}		50	4	7	10	13	15	ns	2
		300						ns	
t_{PHZ}	Prop. Delay Output Disable	10	4	7	10	13	15	ns	2
		50						ns	
t_{PLZ}		10	4	7	9	12	14	ns	2
		50						ns	
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300						ns	
t_{THL}		50	1	2	3	4	5	ns	4
		300						ns	
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			25	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

A·C·T FAMILY DATA SHEETS

V54ACT563
V74ACT563
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1µA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

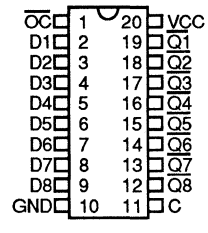
FUNCTIONAL DESCRIPTION:

These are 8-bit transparent inverting D-type latches. While the enable C is high, the $\overline{Q}$ output will follow the inverse of the data input. The data at input D is latched when the enable is taken low.

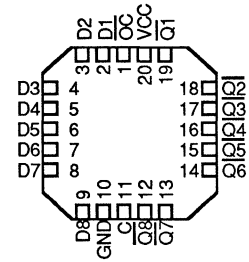
The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

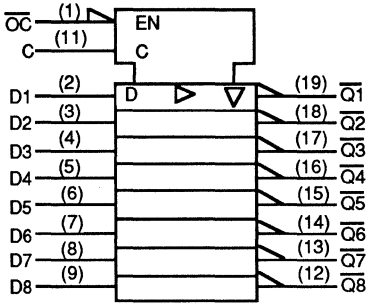


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

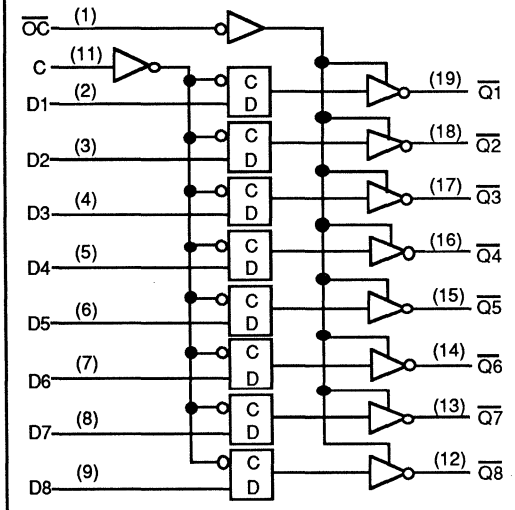
LOGIC SYMBOL



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input D	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT564
V74ACT564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

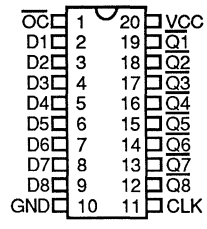
FUNCTIONAL DESCRIPTION:

This 8-bit register inverts the data between input and output. The data is latched by the positive edge transition of the clock. The inverted data appears at the output $\overline{Q}$'s when enabled by the output control signal $\overline{OC}$.

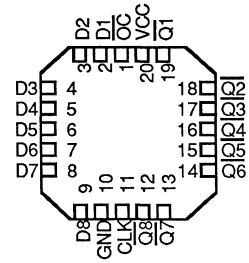
The $\overline{OC}$ signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

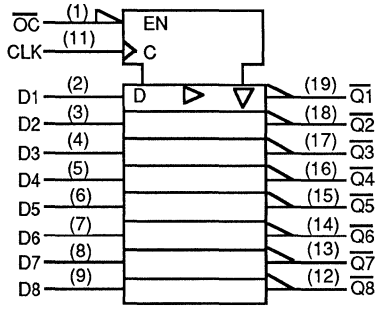


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

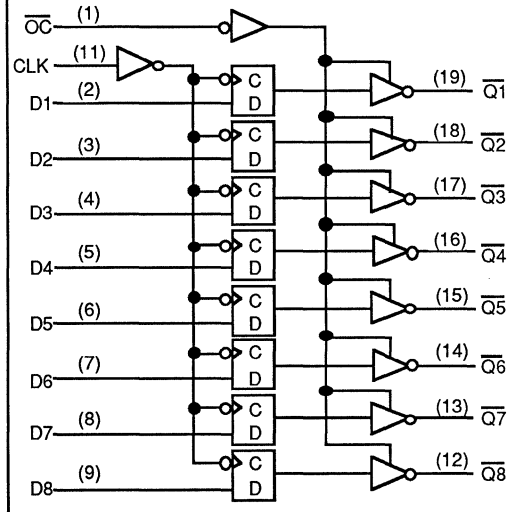
LOGIC SYMBOL



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	1	2	3	4	5	ns	
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT573
V74ACT573
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

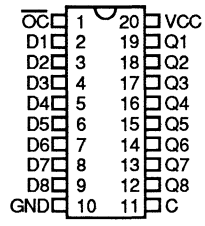
FUNCTIONAL DESCRIPTION:

These are 8-bit transparent D-type latches. While the enable C is high, the Q outputs will follow the data inputs. The data at input D is latched when the enable is taken low.

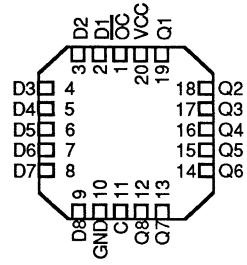
The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

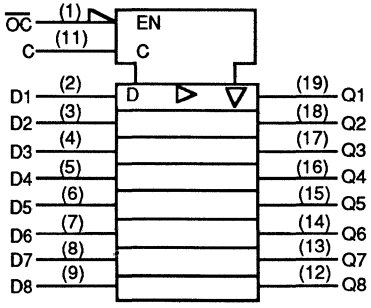


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

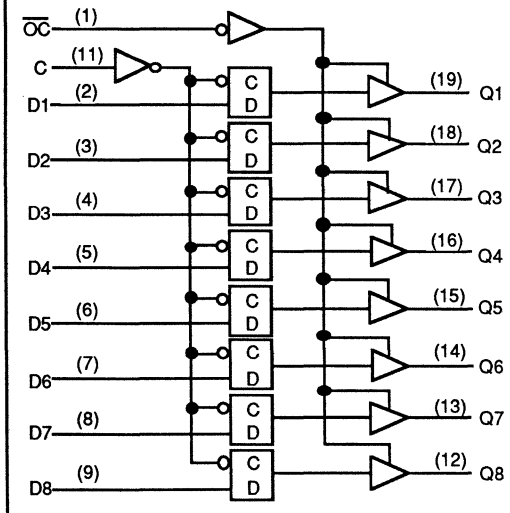
LOGIC SYMBOL



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS — PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input D	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT574
V74ACT574
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

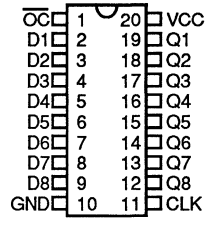
FUNCTIONAL DESCRIPTION:

These are 8-bit flip-flops which are triggered on the positive transition of the clock. The input data is latched by a positive edge transition of the clock.

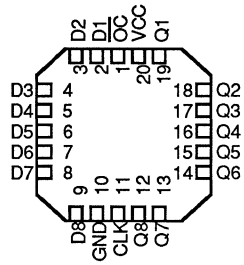
The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

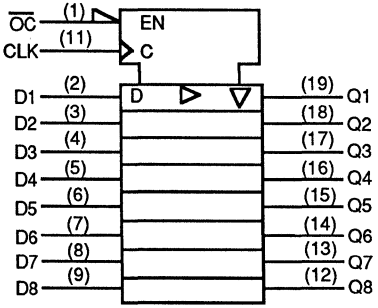


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

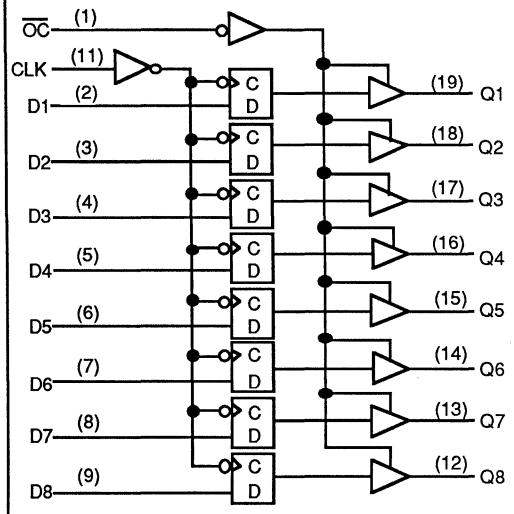
LOGIC SYMBOL



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,$t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	1	2	3	4	5	ns	
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT575
V74ACT575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

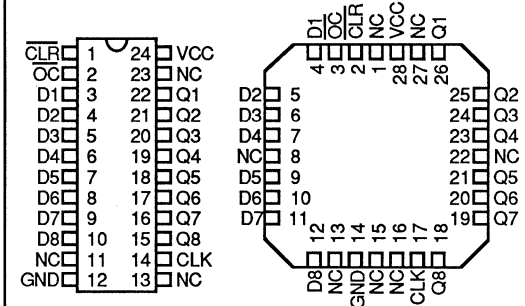
FUNCTIONAL DESCRIPTION:

This 8-bit register features a positive edge triggered clock and a clear control signal $\overline{CLR}$. The register can be synchronously cleared by taking the $\overline{CLR}$ input low before the clock transition.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

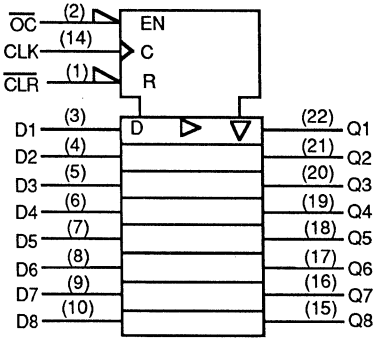
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

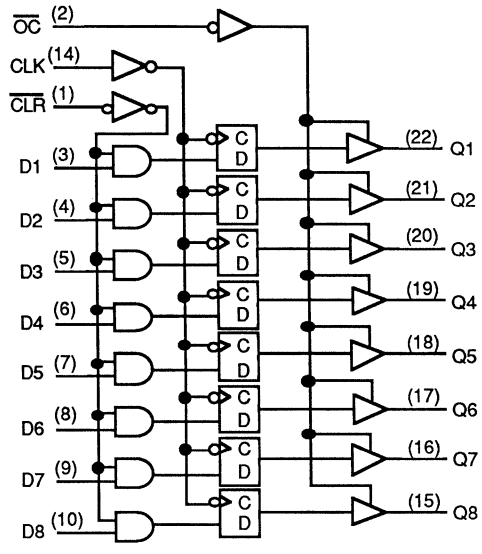
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS — PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	8	11	13	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT576
V74ACT576
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

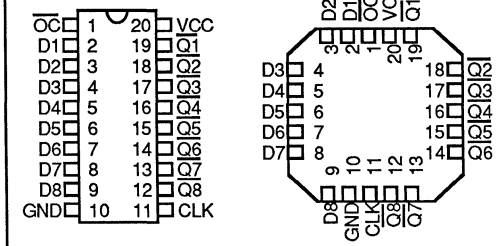
FUNCTIONAL DESCRIPTION:

This 8-bit register inverts the data between input and output. The data is latched by the positive edge transition of the clock. The inverted data appears at the output $\overline{Q}$'s when enabled by the control signal $\overline{OC}$.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

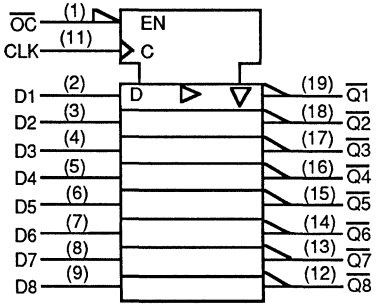
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

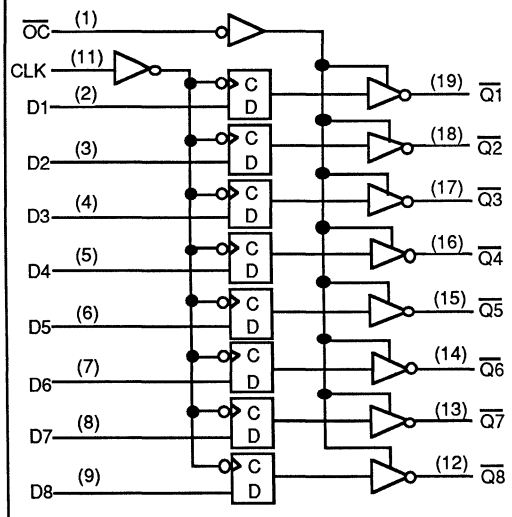
LOGIC SYMBOL



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	1	2	3	4	5	ns	
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	$\overline{\text{Clock Enable}}$ ($\overline{\text{CLKEN}}$) setup time		1	2	2	2	ns	
t_H	$\overline{\text{Clock Enable}}$ ($\overline{\text{CLKEN}}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT577
V74ACT577
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

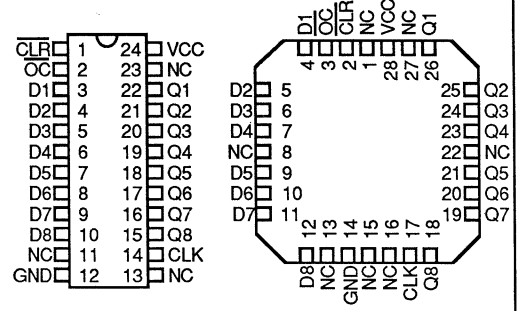
FUNCTIONAL DESCRIPTION:

This 8-bit register inverts the data between input and output. The control signal $\overline{CLR}$ clears the outputs when applied along with the clock signal. The clock signal clocks in the data. $\overline{OC}$ outputs the data when activated low.

Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

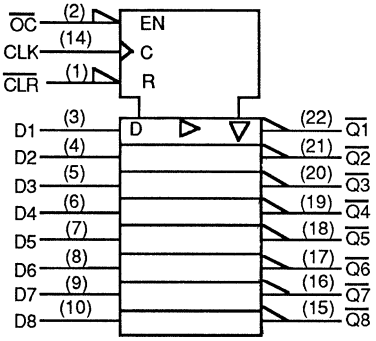
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

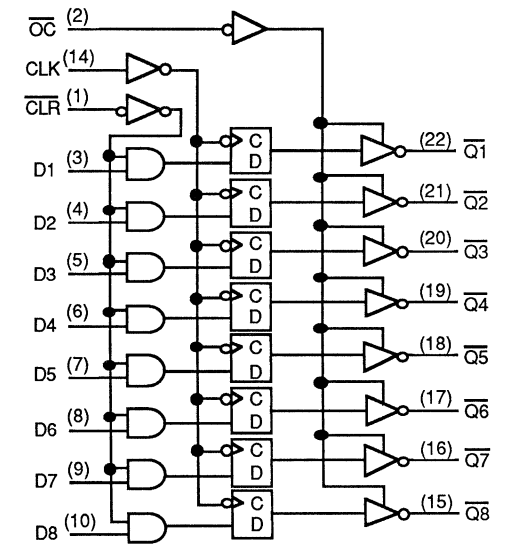
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,$t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	7.5	10	11	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	8	11	13	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT580
V74ACT580
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

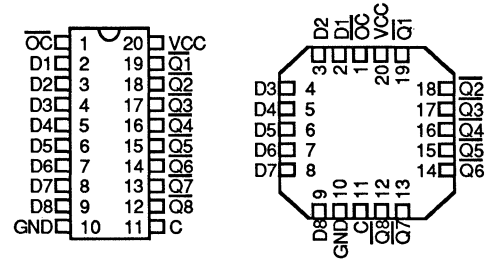
FUNCTIONAL DESCRIPTION:

These are 8-bit transparent inverting D-type latches. While the enable C is high, the $\overline{Q}$ output will follow the inverse of the data input. The data at input D is latched when the enable is taken low.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

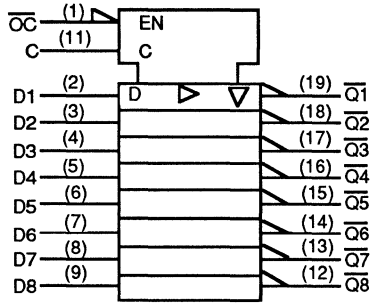
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

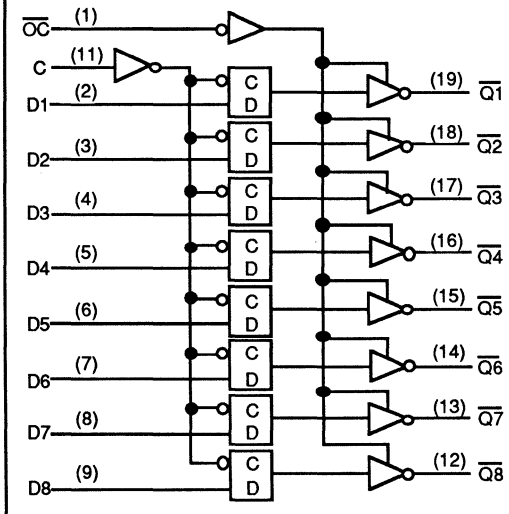
LOGIC SYMBOL



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input D	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT620
V74ACT620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

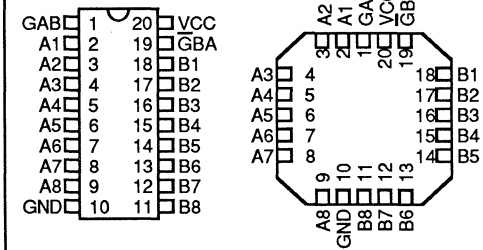
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These octal bus transceivers are inverting type and designed for asynchronous communication between data buses A and B. The function table describes the four states the device can be put into. The simultaneous enable gives the device a latch like capability. When both control inputs are enabled and the data sources for buses A and B are at high impedance, the bus lines (all 16) will remain at their last states.

These parts are designed to interface with 3-state buses and I/O ports.

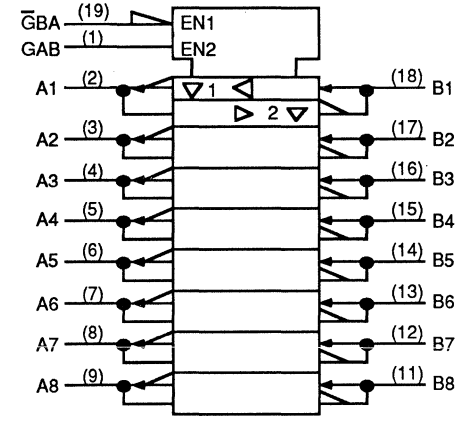
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

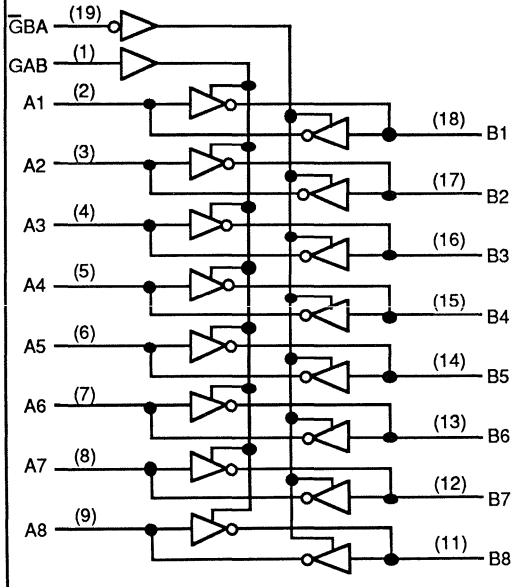
LOGIC SYMBOL



FUNCTION TABLE

ENABLE INPUTS $\overline{G}BA$	ENABLE INPUTS GAB	OPERATION
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	9	12	14	ns	3
		300	5	8	13	17	20	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	6	9	14	19	24	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	7	11	14	16	ns	2
		300	6	10	15	19	22	ns	2
t_{PZL}		50	4	7	12	15	17	ns	2
		300	7	12	17	22	25	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	8	12	15	17	ns	2
		50	6	9	14	19	24	ns	2
t_{PLZ}		10	4	7	11	14	16	ns	2
		50	7	8	13	17	20	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	7	13	17	20	ns	4
t_{THL}		50	1	2	4	4	5	ns	4
		300	4	6	11	14	16	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT623
V74ACT623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

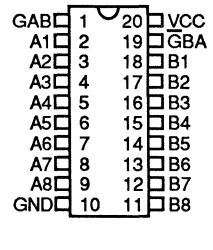
FEATURES:

* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

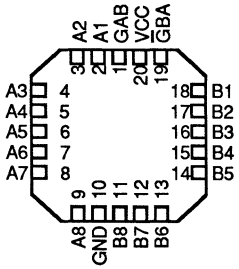
FUNCTIONAL DESCRIPTION:

These octal bus transceivers are non-inverting type and designed for asynchronous communication between data buses A and B. The function table describes the four states the device can be put into. The simultaneous enable gives the device a latch like capability.When both control inputs are enabled and the data sources for buses A and B are at high impedance, the bus lines (all 16) will remain at their last states.
These parts are designed to interface with 3-state buses and I/O ports.

CONNECTION DIAGRAMS

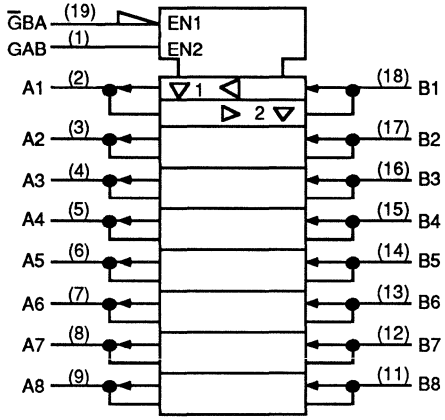


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

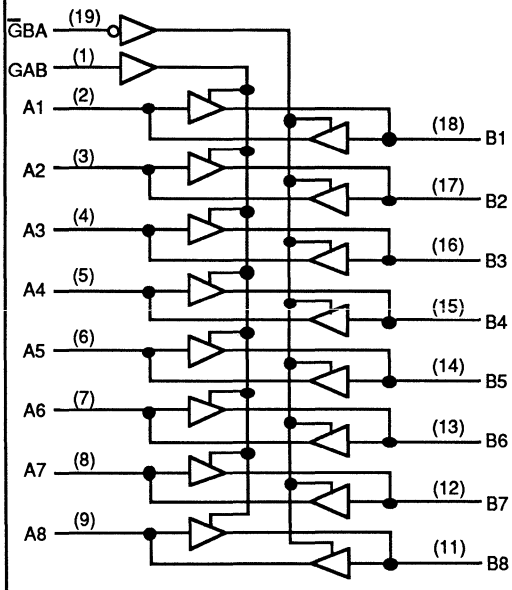
LOGIC SYMBOL



FUNCTION TABLE

ENABLE INPUTS $\overline{G}BA$	GAB	OPERATION
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus A data to B bus

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	Vcc =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	8	10	12	ns	3
		300	6	9	12	15	17	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	8	12	16	21	24	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	11	14	16	ns	2
		300	6	11	15	19	22	ns	2
t_{PZL}		50	4	9	13	17	20	ns	2
		300	8	15	21	27	30	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	6	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	3	5	8	10	12	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	6	8	14	19	24	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	11	14	16	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT640
V74ACT640
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

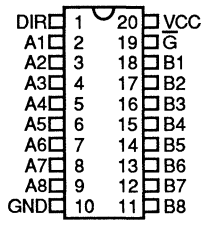
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

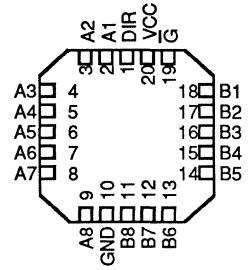
These inverting 8-bit transceivers allow synchronous two way communication between data buses A and B. The DIR signal controls the direction of data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A.

These parts are designed to interface with 3-state buses and I/O ports. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

CONNECTION DIAGRAMS

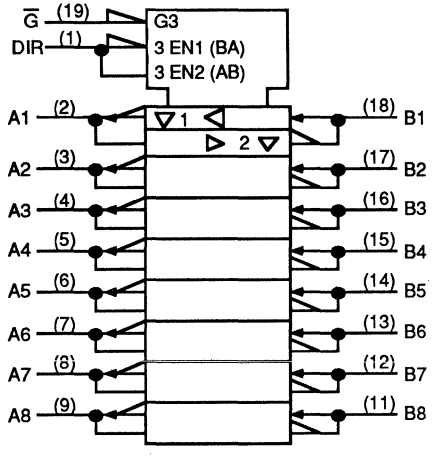


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

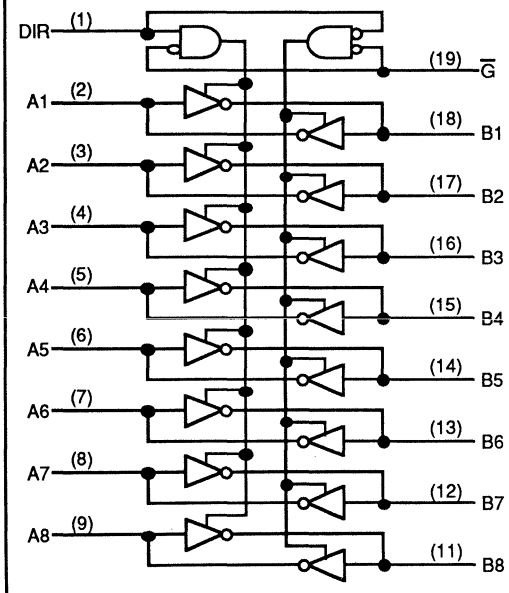
LOGIC SYMBOL



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	6	9	12	14	ns	3
		300	5	8	13	17	20	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	6	10	14	19	24	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	6	11	16	21	24	ns	2
t_{PZL}		50	4	9	13	17	20	ns	2
		300	8	15	20	26	30	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	3	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	3	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	4	8	13	17	20	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	6	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT643
V74ACT643
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

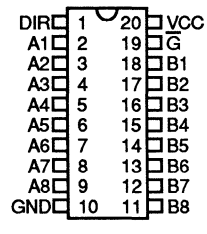
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

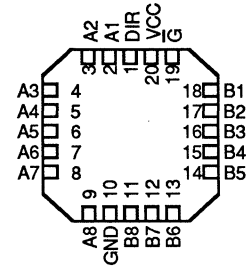
These true and inverting octal bus transceivers allow synchronous two way communication between data buses A and B. The DIR signal controls the direction of data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A. The $\overline{G}$ signal enables the chip.

These parts are designed to interface with 3-state buses and I/O ports.

CONNECTION DIAGRAMS

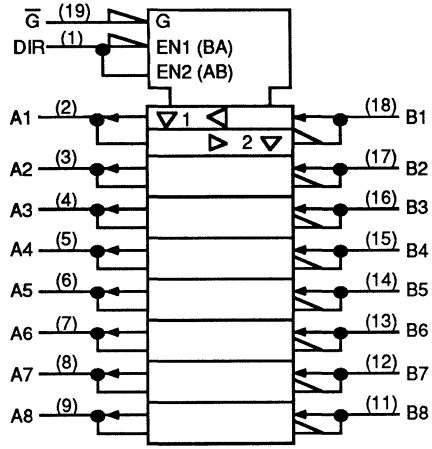


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

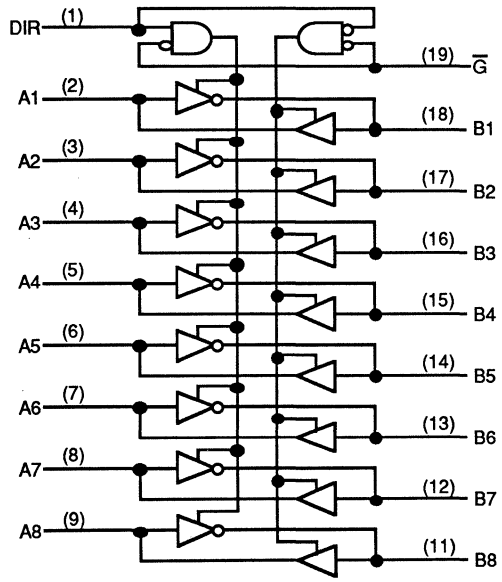
LOGIC SYMBOL



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	6	9	12	14	ns	3
		300	5	8	12	15	17	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	7	11	16	21	24	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	6	11	16	21	24	ns	2
t_{PZL}		50	4	9	13	17	20	ns	2
		300	8	14	19	24	28	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	3	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	3	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	4	8	14	19	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	6	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT645
V74ACT645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

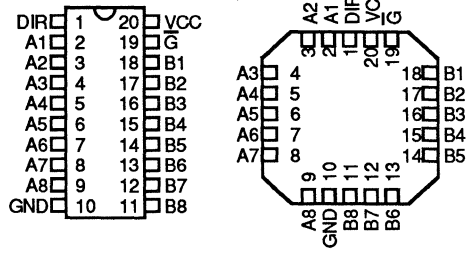
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These 8-bit bus transceivers allow synchronous two way communication between data buses A and B. The DIR signal controls the direction of data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A. The $\overline{G}$ signal enables the transceiver.

These parts are designed to interface with 3-state buses and I/O ports.

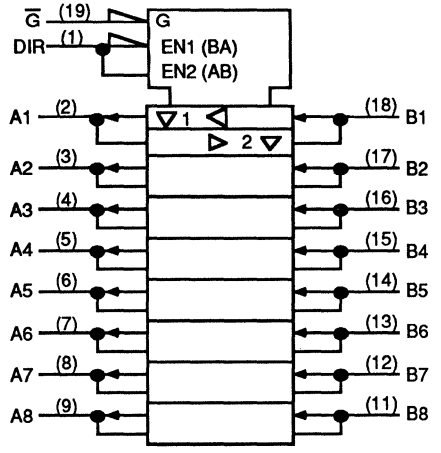
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

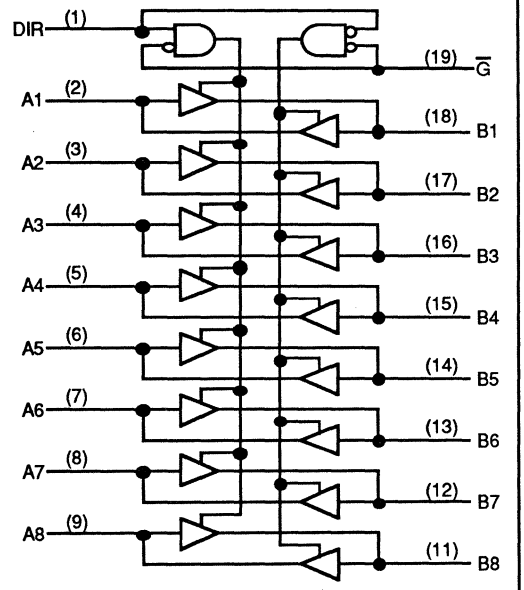
LOGIC SYMBOL



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	7	10	12	ns	3
		300	5	8	11	13	15	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	6	11	15	19	22	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	7	11	13	15	ns	2
		300	5	9	14	18	21	ns	2
t_{PZL}		50	4	8	12	15	17	ns	2
		300	8	12	17	21	24	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	7	10	13	15	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	7	10	13	15	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	13	17	19	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	4	7	9	12	13	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

A·C·T FAMILY DATA SHEETS

V54ACT821
V74ACT821
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

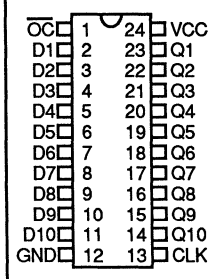
FUNCTIONAL DESCRIPTION:

These are 10-bit edge triggered flip-flops.The data is latched by the low to high edge transition of the CLK signal.

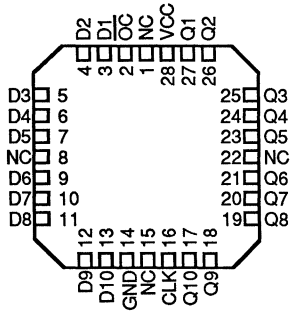
The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

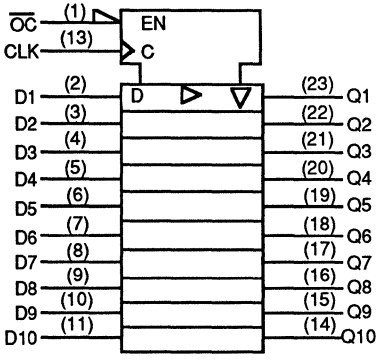


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

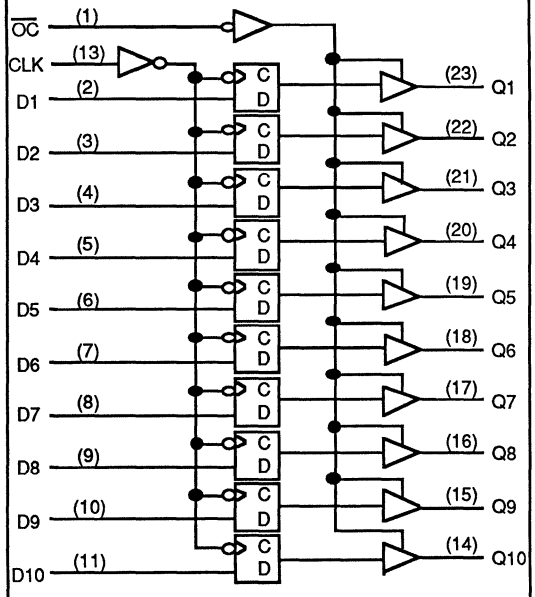
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	1	2	3	4	5	ns	
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT822
V74ACT822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

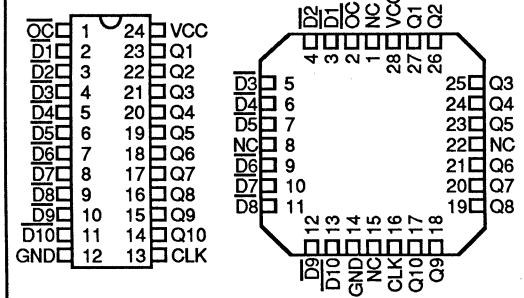
FUNCTIONAL DESCRIPTION:

These are 10-bit inverting type edge triggered flip-flops. The data is latched by the low to high edge transition of the CLK signal.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of OC.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The high drive capability, 48mA I_{OL}/I_{OH}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads.

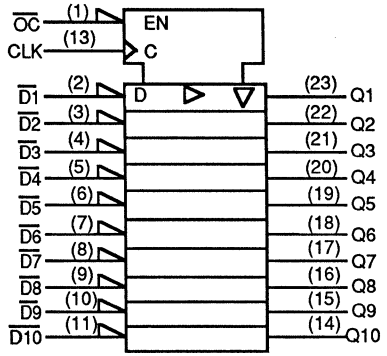
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

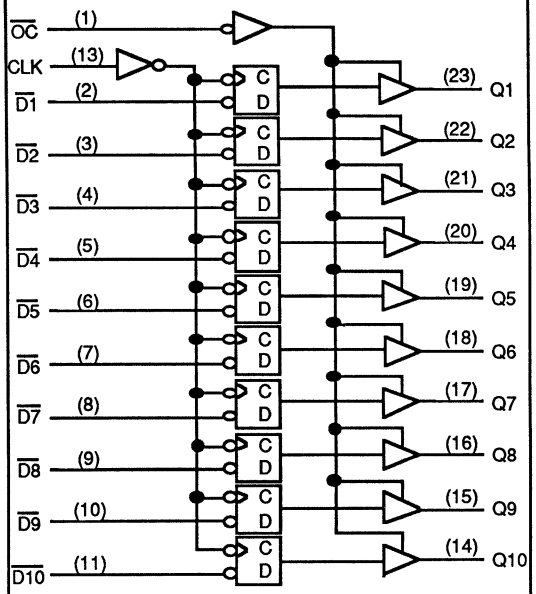
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,$t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	1	2	3	4	5	ns	
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT823
V74ACT823
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48 mA Commercial, 32 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

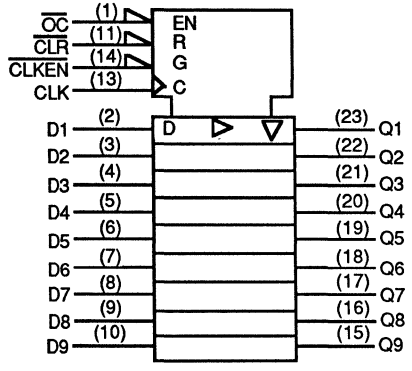
FUNCTIONAL DESCRIPTION:

These are 9-bit non-inverting edge triggered flip-flops. The nine D-type edge triggered flip-flops enter data on a low to high transition of the clock when $\overline{CLKEN}$ is low. $\overline{CLR}$ input low causes the Q outputs to go low independent of the clock.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

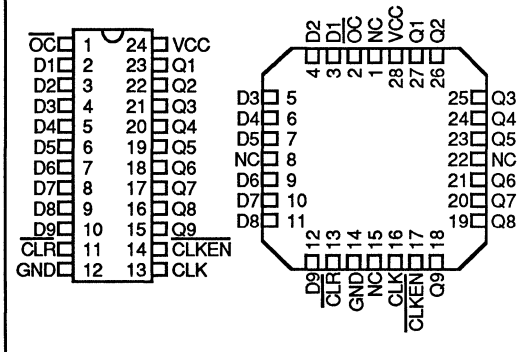
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS					OUTPUT
$\overline{OC}$	CLR	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

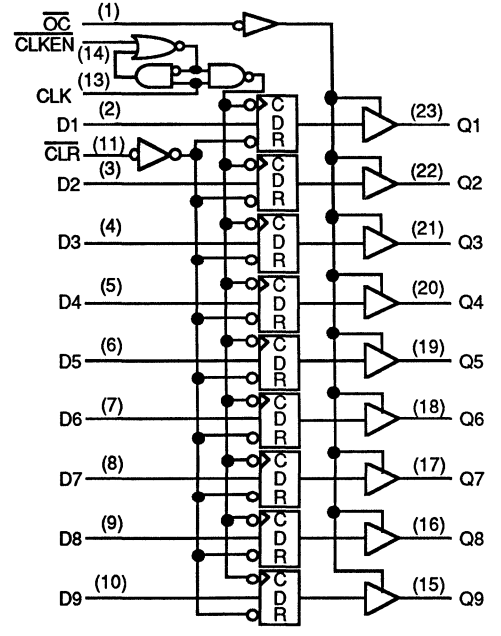
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable (CLKEN) setup time		1	2	2	2	ns	
t_H	Clock Enable (CLKEN) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT824
V74ACT824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1μA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

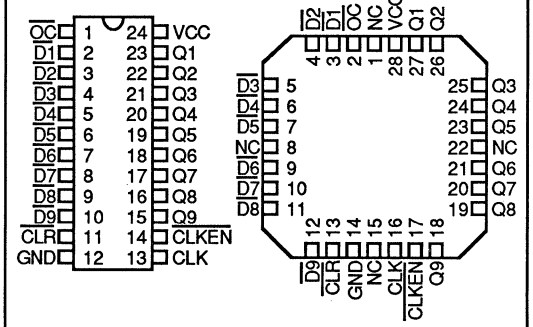
FUNCTIONAL DESCRIPTION:

These are 9-bit inverting type edge triggered flip-flops. The nine flip-flops enter data on a low to high transition of the clock when CLKEN is low. CLR input low causes the Q outputs to go low independant of the clock.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

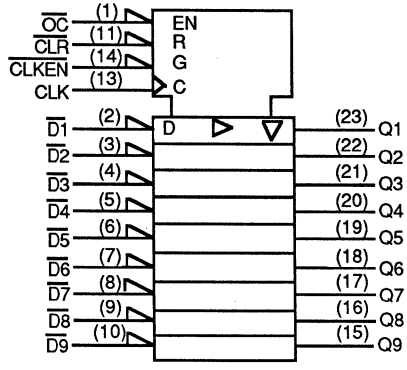
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

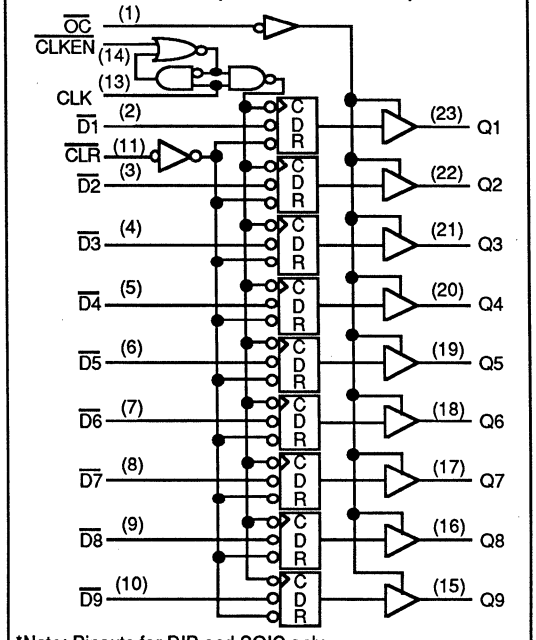
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS					OUTPUT
$\overline{OC}$	CLR	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,$t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT825
V74ACT825
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
*Low Input Current, 1µA Max
*Fully Specified: 5V ± 10% Power Supply
50pF and 300pF Loading
Min and Max over Temperature

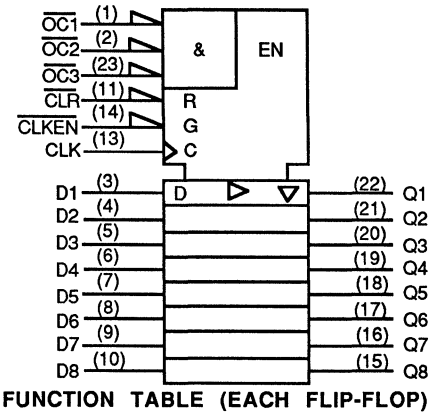
FUNCTIONAL DESCRIPTION:

These are 8-bit edge triggered flip-flops with three output enables for multi-use control. The $\overline{CLKEN}$ low causes the flip-flops to accept data on a low to high transition of the clock. $\overline{CLKEN}$ high disables the buffer and latches the output Q. $\overline{CLR}$ input low causes the Q outputs to go low independent of the clock.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

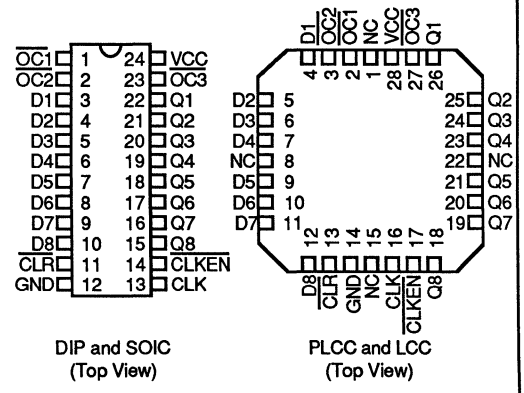
LOGIC SYMBOL*



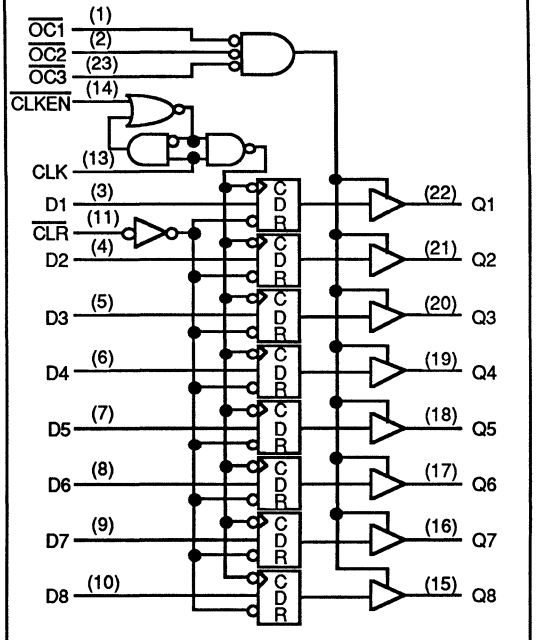
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS							OUTPUT
$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	L	L	X	X	X	L
L	L	L	H	L	↑	H	H
L	L	L	H	L	↑	L	L
L	L	L	H	H	X	X	Q_0
H	X	X	X	X	X	X	Z
X	H	X	X	X	X	X	Z
X	X	H	X	X	X	X	Z

CONNECTION DIAGRAMS



LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,$t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT826
V74ACT826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

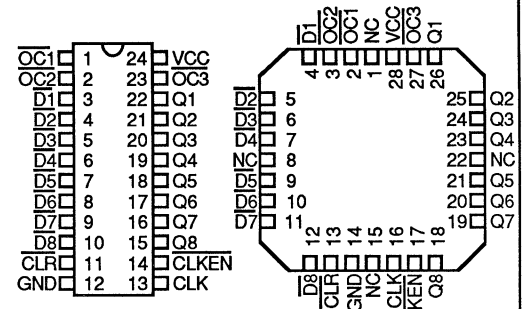
FUNCTIONAL DESCRIPTION:

These are 8-bit inverting type edge triggered flip-flops with three output enables for multi-use control. The $\overline{CLKEN}$ low causes the flip-flops to accept data on a low to high transition of the clock. $\overline{CLKEN}$ high disables the buffer and latches the output Q. $\overline{CLR}$ input low causes the Q outputs to go low independent of the clock.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

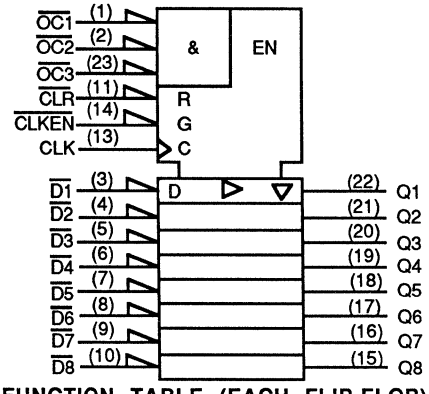
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

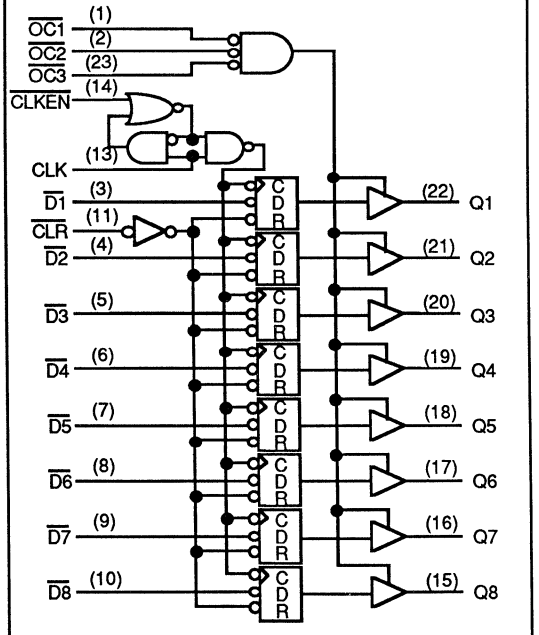
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS							OUTPUT
$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	L	L	X	X	X	L
L	L	L	H	L	↑	H	L
L	L	L	H	L	↑	L	H
L	L	L	H	H	X	X	Q_0
H	X	X	X	X	X	X	Z
X	H	X	X	X	X	X	Z
X	X	H	X	X	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	10	12	14	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable (CLKEN) setup time		1	2	2	2	ns	
t_H	Clock Enable (CLKEN) hold time		1	2	2	2	ns	
Fmax	Maximum Frequency		75	70	60	50	MHz	

V54ACT827
V74ACT827
10-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

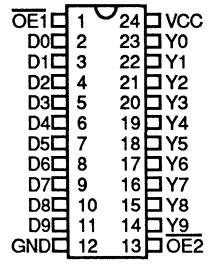
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

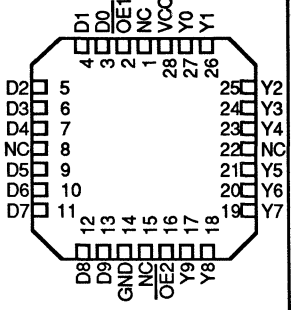
This 10-bit buffer provides non-inverted bus interface buffering for wide data/address and control signals. The buffers have NORed output enables for control flexibility.

This high performance interface family is designed for high capacitance load drive capability. It is compatible with the ALS/AS family of TTL parts.

CONNECTION DIAGRAMS

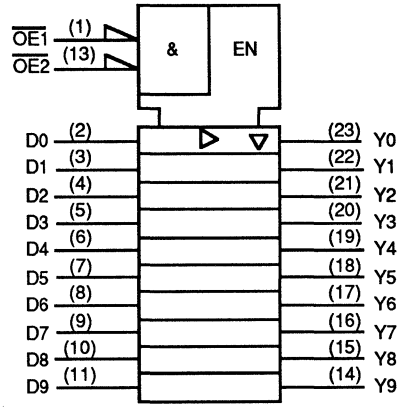


DIP and SOIC (Top View)



PLCC and LCC (Top View)

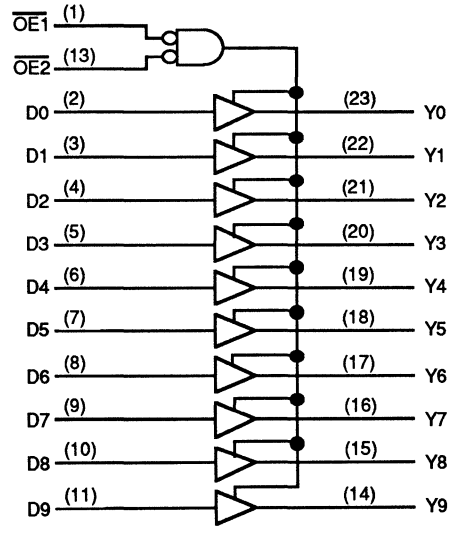
LOGIC SYMBOL*



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	D	Y
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	L
L	L	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300						ns	
t_{PHL}		50	3	5	8	11	13	ns	3
		300						ns	
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	8	11	13	ns	2
		300						ns	
t_{PZL}		50	4	7	10	13	15	ns	2
		300						ns	
t_{PHZ}	Prop. Delay Output Disable	10	4	7	10	13	15	ns	2
		50						ns	
t_{PLZ}		10	4	7	9	12	14	ns	2
		50						ns	
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300						ns	
t_{THL}		50	1	2	3	4	5	ns	4
		300						ns	
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			25	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

A-C-T FAMILY DATA SHEETS

V54ACT828
V74ACT828
10-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

FEATURES:

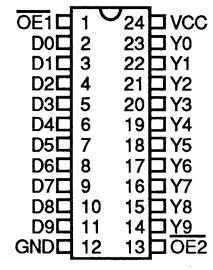
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

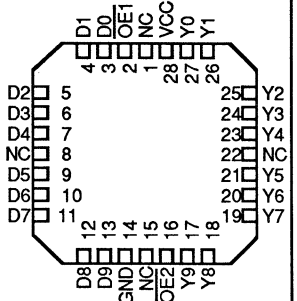
This 10-bit buffer provides inverted bus interface buffering for wide data/address and control signals. The buffers have NORed output enables for control flexibility.

This high performance interface family is designed for high capacitance load drive capability. It is compatible with the ALS/AS family of TTL parts.

CONNECTION DIAGRAMS

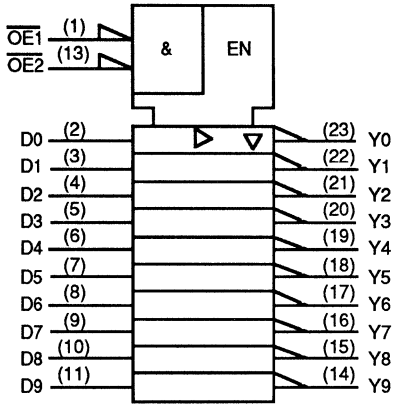


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

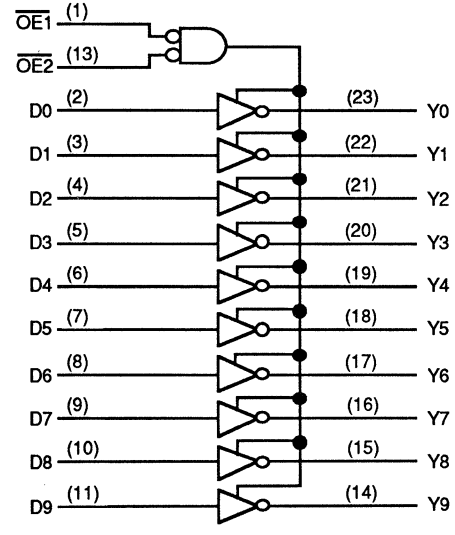
LOGIC SYMBOL*



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	D	Y
H	H	X	Z
H	L	X	Z
L	H	X	Z
L	L	L	H
L	L	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to Ya or B to Yb	50	3	5	7	10	12	ns	3
		300						ns	
t_{PHL}		50	3	5	8	11	13	ns	3
		300						ns	
t_{PZH}	Prop. Delay Output Enable to Ya or Yb	50	4	7	8	11	13	ns	2
		300						ns	
t_{PZL}		50	4	7	9	12	14	ns	2
		300						ns	
t_{PHZ}	Prop. Delay Output Disable	10	4	7	10	13	15	ns	2
		50						ns	
t_{PLZ}		10	4	7	9	12	14	ns	2
		50						ns	
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300						ns	
t_{THL}		50	1	2	3	4	5	ns	4
		300						ns	
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			25	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

A-C-T FAMILY DATA SHEETS

V54ACT841
V74ACT841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

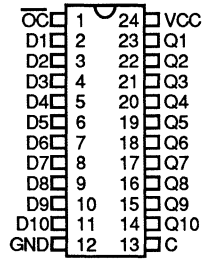
FUNCTIONAL DESCRIPTION:

These are 10-bit transparent D-type latches. While the enable C is high, the Q outputs will follow the data inputs. The data at input D is latched when the clock goes low.

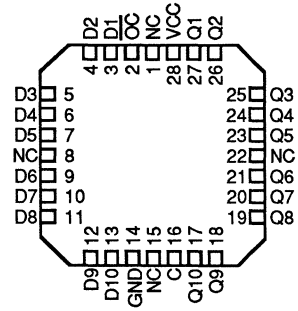
The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

CONNECTION DIAGRAMS

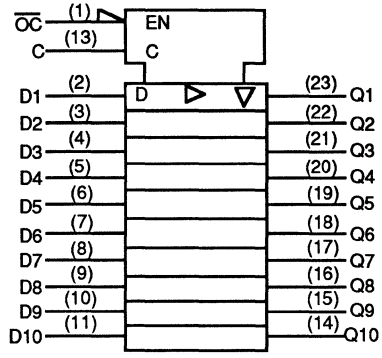


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

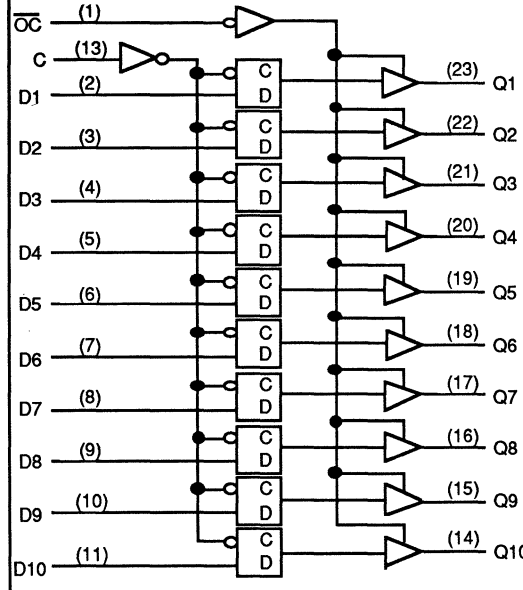
LOGIC SYMBOL*



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input D	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT842
V74ACT842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

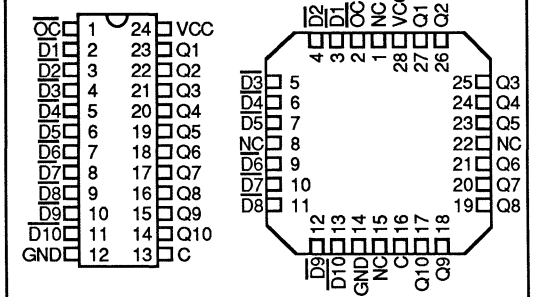
FUNCTIONAL DESCRIPTION:

These are 10-bit transparent inverting D-type latches. While the enable C is high, the Q outputs will follow the inverse of the data input. The data at input $\overline{D}$ is latched when the clock goes low.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements. The TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

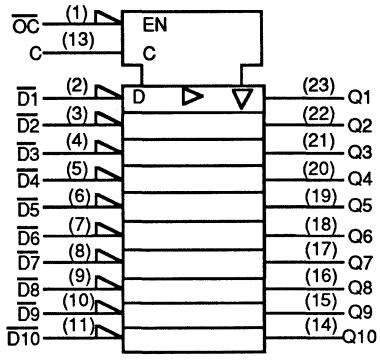
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

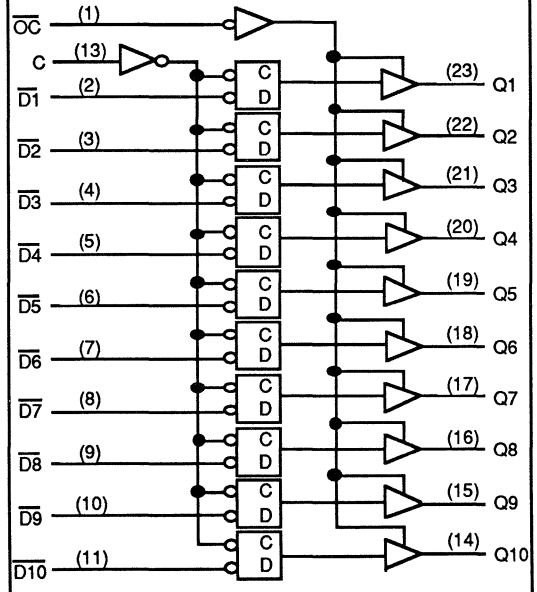
LOGIC SYMBOL*



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
					25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Input D to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input D	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT843
V74ACT843
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

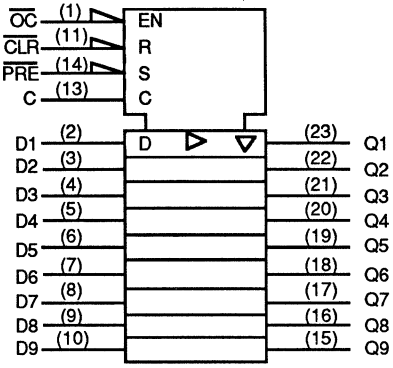
FUNCTIONAL DESCRIPTION:

These are 9-bit transparent D-type latches. Independent of enable C, when $\overline{PRE}$ is low, the output Q goes high. When $\overline{CLR}$ alone goes low, the output Q goes low. When both $\overline{PRE}$ and $\overline{CLR}$ are low, the output Q is high. When enable C is high the output will follow the data D if $\overline{PRE}$ and $\overline{CLR}$ are both high.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or be used as storage elements.

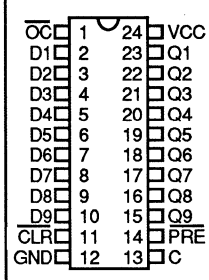
LOGIC SYMBOL*



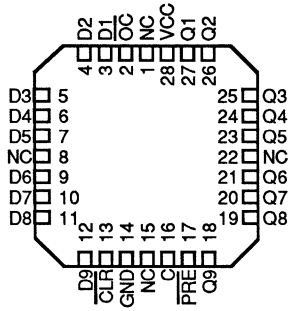
FUNCTION TABLE (EACH LATCH)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	L	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

CONNECTION DIAGRAMS

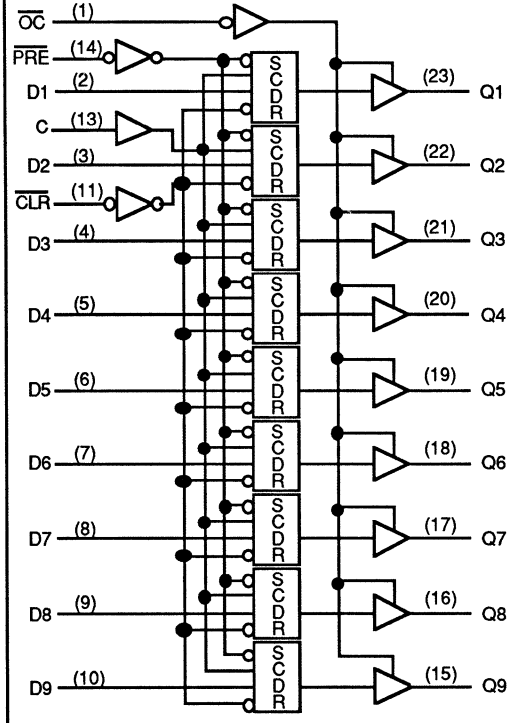


DIP and SOIC (Top View)



PLCC and LCC (Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS — PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq 3$ nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{THZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{TLZ}		10							
		50	4	7	9	12	14	ns	2
t_{PLH}	$\overline{PRE}$ to Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}	$\overline{CLR}$ to Q	50	4	7	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq 3$ nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT844
V74ACT844

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

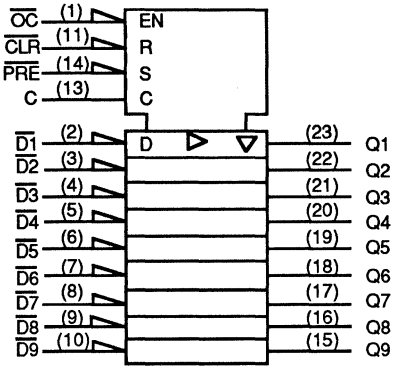
FUNCTIONAL DESCRIPTION:

These are 9-bit transparent D-type inverting latches. Independent of enable C, when $\overline{PRE}$ is low, the output Q goes high. When $\overline{CLR}$ alone is low, the output Q goes low. When both $\overline{PRE}$ and $\overline{CLR}$ are low, the output Q is high. When enable C is high, the output is the inverse of the input if $\overline{PRE}$ and $\overline{CLR}$ are both high.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or be used as storage elements.

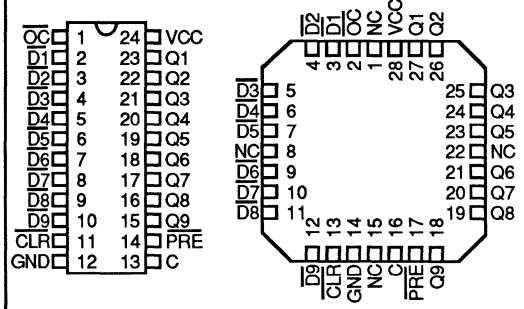
LOGIC SYMBOL*



FUNCTION TABLE (EACH LATCH)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	H
H	H	L	L	H	L
H	H	L	X	X	Q_0
X	X	H	X	X	Z

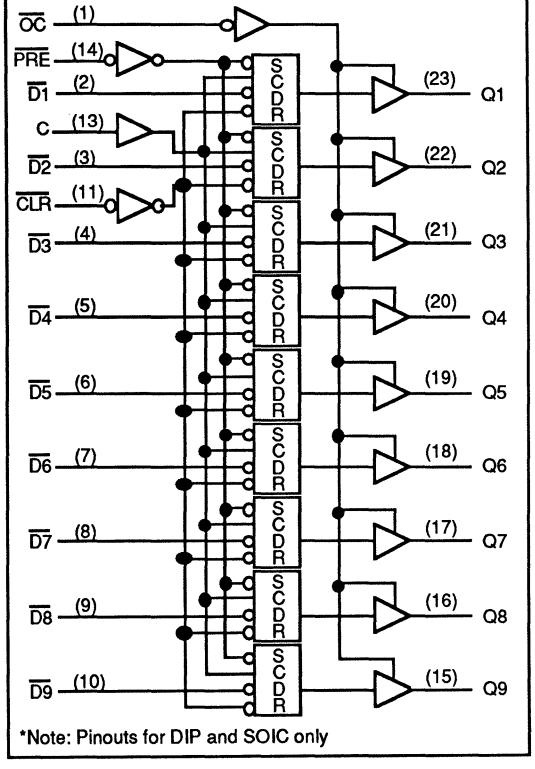
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{THZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{TLZ}		10							
		50	4	7	9	12	14	ns	2
t_{PLH}	$\overline{PRE}$ to Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}	$\overline{CLR}$ to Q	50	4	7	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT845
V74ACT845
OCTAL BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

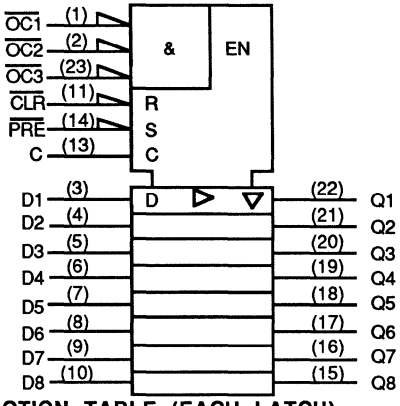
FUNCTIONAL DESCRIPTION:

These are octal transparent D-type latches. Independent of enable C, when $\overline{PRE}$ is low, the output Q goes high. When $\overline{CLR}$ alone goes low, the output Q goes low. When both $\overline{PRE}$ and $\overline{CLR}$ are low, the output Q is high. When enable C is high the output will follow the input D if $\overline{PRE}$ and $\overline{CLR}$ are both high.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or be used as storage elements.

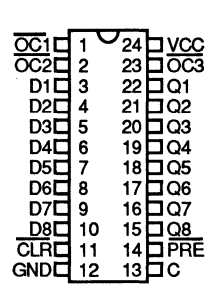
LOGIC SYMBOL*



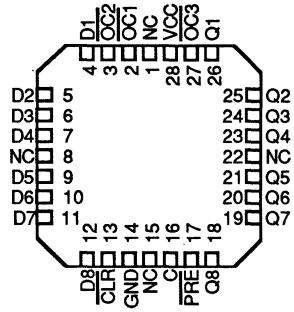
FUNCTION TABLE (EACH LATCH)

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	H	X	X	X	X	Z
X	X	X	H	X	X	X	Z
X	X	X	X	H	X	X	Z

CONNECTION DIAGRAMS

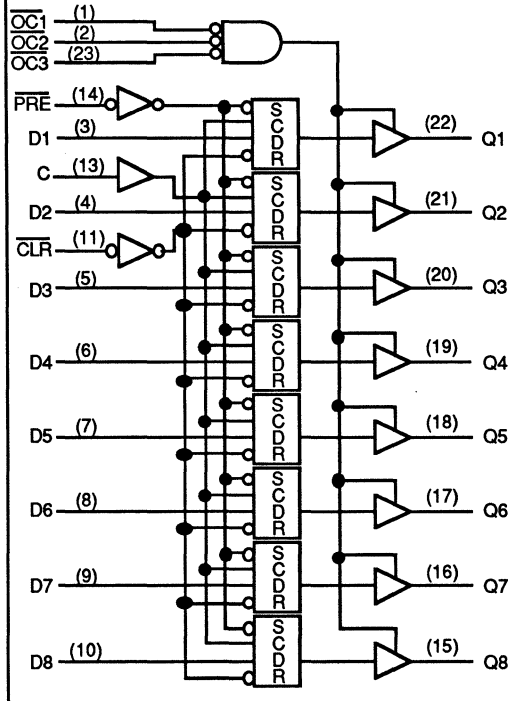


DIP and SOIC
(Top View)



PLCC and LCC
(Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS — PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	7	8.5	11	13	ns	3
		300							
t_{PHL}		50	4	7	9.5	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	7	8.5	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9.5	12	14	ns	2
		300							
t_{THZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{TLZ}		10							
		50	4	7	9	12	14	ns	2
t_{PLH}	$\overline{PRE}$ to Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}	$\overline{CLR}$ to Q	50	4	7	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT846
V74ACT846
OCTAL BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

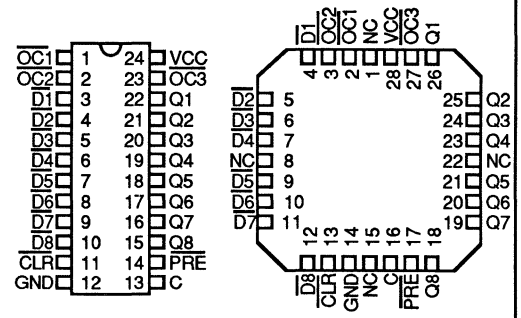
* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply
  50pF and 300pF Loading
  Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are octal transparent D-type inverting latches. In- dependent of enable C, when $\overline{PRE}$ is low, the output Q goes high. When $\overline{CLR}$ alone is low, the output Q goes low. When both $\overline{PRE}$ and $\overline{CLR}$ are low, the output Q is high. When enable C is high, the output is the inverse of the input if $\overline{PRE}$ and $\overline{CLR}$ are The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or be used as storage elements.

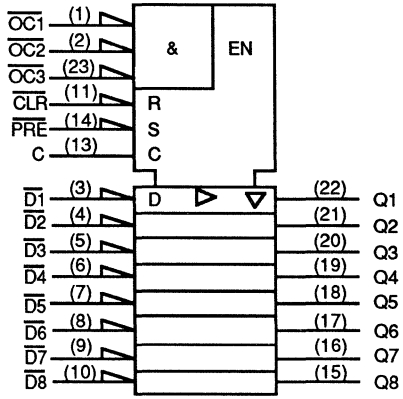
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

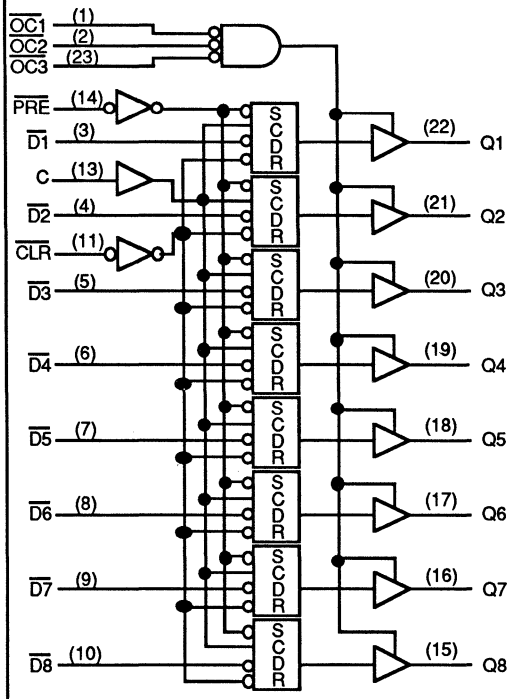
LOGIC SYMBOL*



FUNCTION TABLE (EACH LATCH)

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	H	X	X	X	X	Z
X	X	X	H	X	X	X	Z
X	X	X	X	H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS — PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{THZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{TLZ}		10							
		50	4	7	9	12	14	ns	2
t_{PLH}	$\overline{PRE}$ to Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}	$\overline{CLR}$ to Q	50	4	7	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

V54ACT861
V74ACT861
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

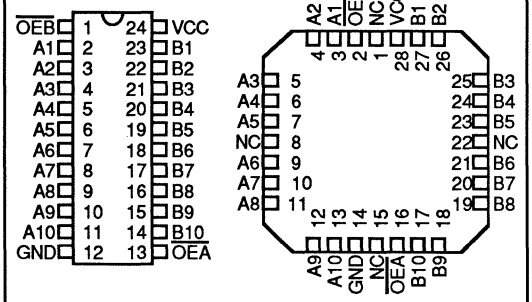
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are 10-bit transceivers with control enables $\overline{OEA}$ and $\overline{OEB}$. When $\overline{OEA}$ is low, the data on bus B is transmitted to bus A. When $\overline{OEB}$ is low, the data on bus A is transmitted to bus B. The ten bits provide extra bits for parity, clock, or control signals on the bus by just using a simple component.

These parts are designed to interface with 3-state buses and I/O ports. The high drive capability, 48 mA I_{OH}/I_{OL}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

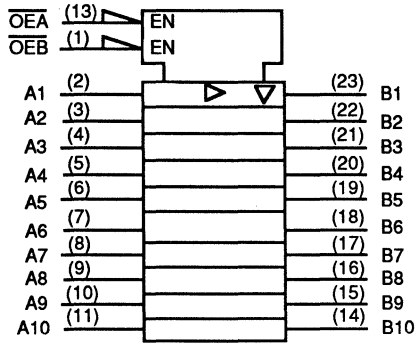
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC SYMBOL*

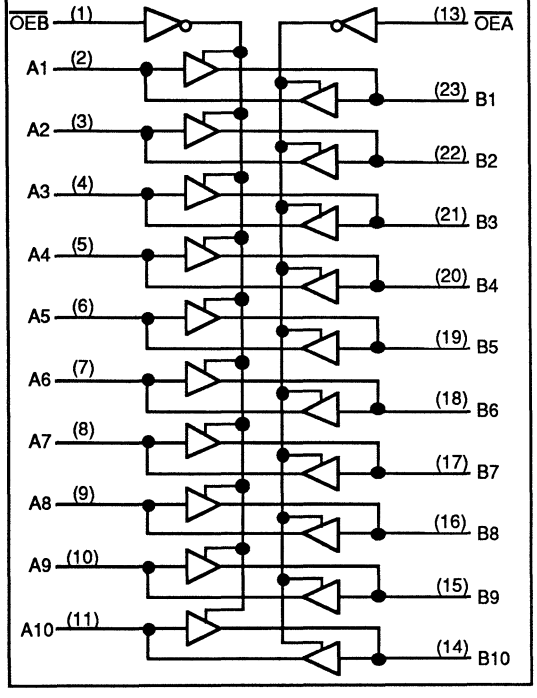


FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{OEB}$	$\overline{OEA}$	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation
L	L	Latch

*Note: Pinouts are for DIP and SOIC only

LOGIC DIAGRAM (POSITIVE LOGIC)*



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	8	10	12	ns	3
		300	5	8	12	15	17	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	7	12	16	21	24	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	7	11	16	21	24	ns	2
t_{PZL}		50	4	9	13	17	20	ns	2
		300	8	15	20	26	29	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	4′	8	14	19	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	6	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT862
V74ACT862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

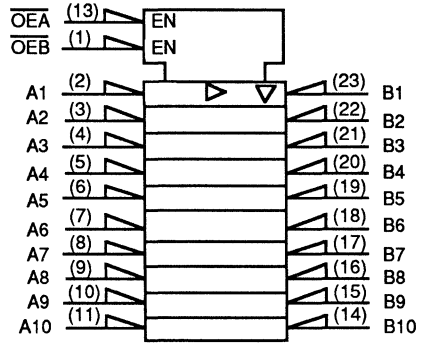
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are 10-bit inverting transceivers with control enables $\overline{OEA}$ and $\overline{OEB}$. When $\overline{OEA}$ is low, the inverse of the data on bus B is transmitted to bus A. When $\overline{OEB}$ is low, the inverse of the data on bus A is transmitted to bus B. The ten bits provide extra bits for parity, clock, or control signals on the bus by just using a simple component.

These parts are designed to interface with 3-state buses and I/O ports. The high drive capability, 48 mA I_{OH}/I_{OL}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

LOGIC SYMBOL*

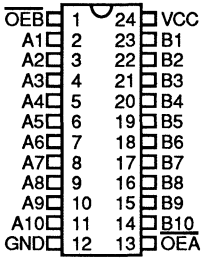


FUNCTION TABLE

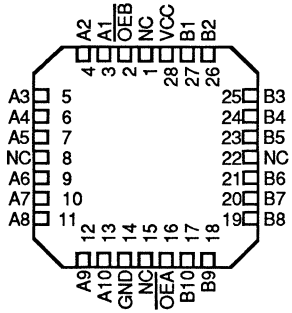
ENABLE INPUTS		OPERATION
$\overline{OEB}$	$\overline{OEA}$	
H	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	H	Isolation
L	L	Latch

*Note: Pinouts are for DIP and SOIC only

CONNECTION DIAGRAMS

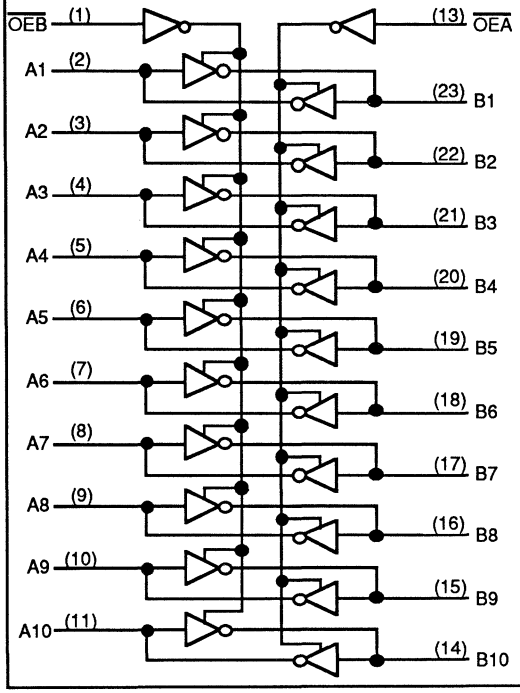


DIP and SOIC (Top View)



PLCC and LCC (Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	6	9	12	14	ns	3
		300	5	8	12	15	17	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	6	11	14	19	21	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	7	11	16	21	24	ns	2
t_{PZL}		50	4	10	13	17	20	ns	2
		300	8	15	20	26	29	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	14	19	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	7	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT863
V74ACT863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

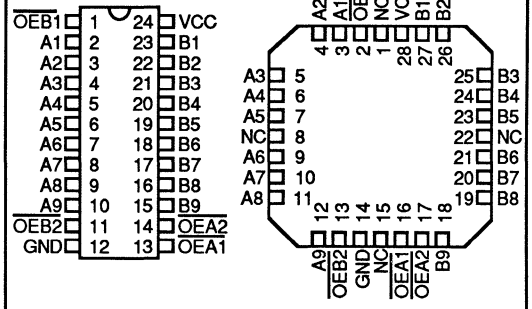
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are 9-bit transceivers with dual-control enables $\overline{OEA1}$, $\overline{OEA2}$ and $\overline{OEB1}$, $\overline{OEB2}$. When both enables are low, the transceivers conduct from one port to the other. The nine bits provide the capability to transmit parity on the system buses among other possible uses.

These parts are designed to interface with 3-state buses and I/O ports. The high drive capability, 48 mA I_{OH}/I_{OL}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

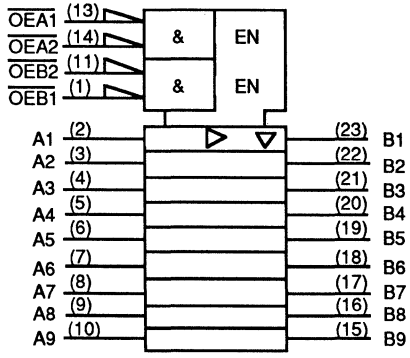
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

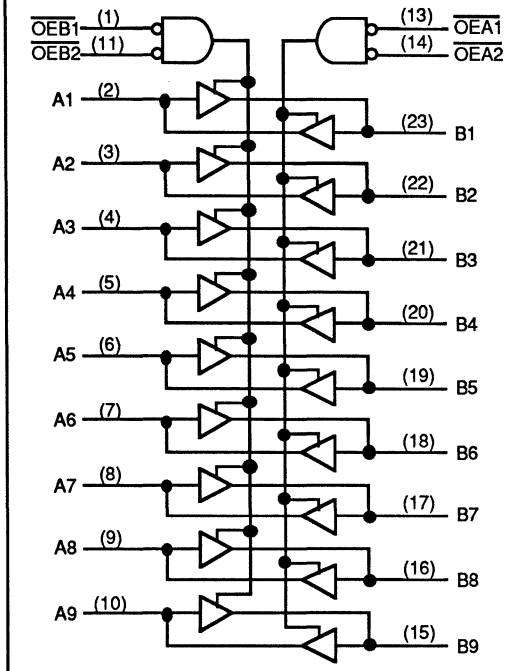
LOGIC SYMBOL*



FUNCTION TABLE

ENABLE INPUTS				OPERATION
$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEA1}$	$\overline{OEA2}$	
H	X	L	L	B data to A bus
X	H	L	L	B data to A bus
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	H	X	Isolation
X	H	X	H	Isolation
L	L	L	L	Latch

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts are for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	5	8	10	12	ns	3
		300	4	8	11	14	16	ns	3
t_{PHL}		50	3	5	9	12	14	ns	3
		300	7	11	15	20	23	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	7	11	16	21	24	ns	2
t_{PZL}		50	4	10	13	17	20	ns	2
		300	8	15	20	26	29	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	14	19	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	7	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT864
V74ACT864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES:

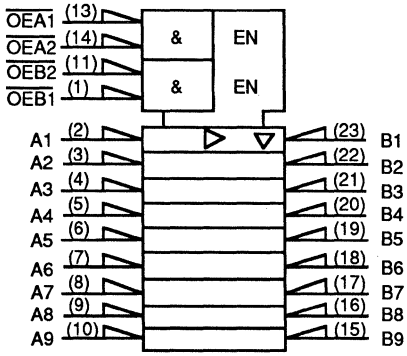
* CMOS Replacement for ALS
* High speed, 5ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

FUNCTIONAL DESCRIPTION:

These are inverting 9-bit transceivers with dual-control enables $\overline{OEA1}$, $\overline{OEA2}$ and $\overline{OEB1}$, $\overline{OEB2}$. When both enables are low, the transceivers conduct from one port to the other. The nine bits provide the capability to transmit parity on the system buses among other possible uses.

These parts are designed to interface with 3-state buses and I/O ports. The high drive capability, 48 mA I_{OH}/I_{OL}, at the TTL logic levels is ideal for interfacing with high-capacitance, low impedance loads on both buses A and B.

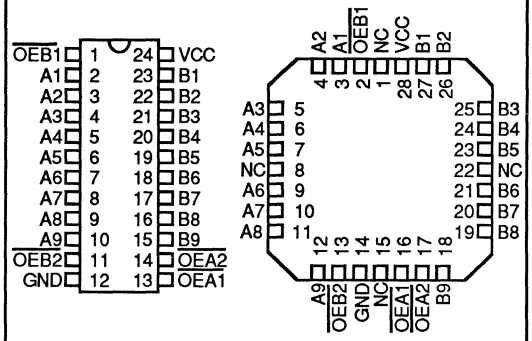
LOGIC SYMBOL*



FUNCTION TABLE

ENABLE INPUTS				OPERATION
$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEA1}$	$\overline{OEA2}$	
H	X	L	L	B data to A bus
X	H	L	L	B data to A bus
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	H	X	Isolation
X	H	X	H	Isolation
L	L	L	L	Latch

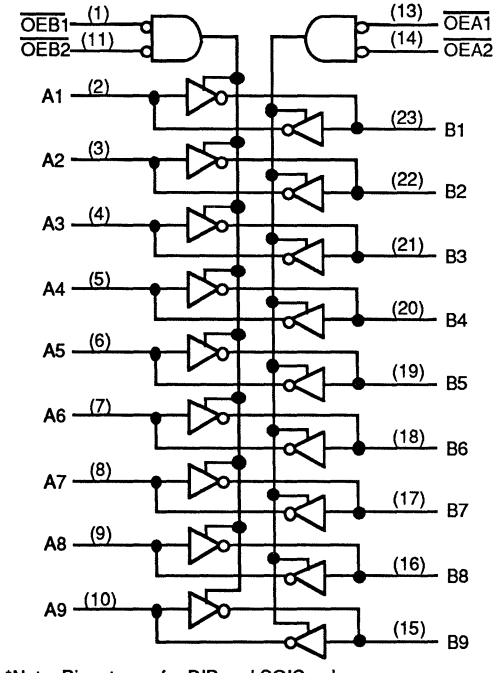
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts are for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE						UNIT
		Min		Typ		Max		
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: Input t_r, t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC} =5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	50	3	6	9	12	14	ns	3
		300	5	8	12	15	17	ns	3
t_{PHL}		50	3	6	9	12	14	ns	3
		300	7	11	14	19	21	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	50	4	8	12	15	17	ns	2
		300	7	11	16	21	24	ns	2
t_{PZL}		50	4	8	13	17	20	ns	2
		300	8	15	20	26	29	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{PLZ}		10	4	7	9	12	14	ns	2
		50	4	8	11	14	16	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300	5	9	14	19	21	ns	4
t_{THL}		50	1	2	3	4	5	ns	4
		300	3	7	10	13	15	ns	4
C_{IN}	Input Capacitance			10	12	12	12	pF	
C_{OUT}	Output Capacitance			10	12	12	12	pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)			35	45	45	45	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

V54ACT874
V74ACT874
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

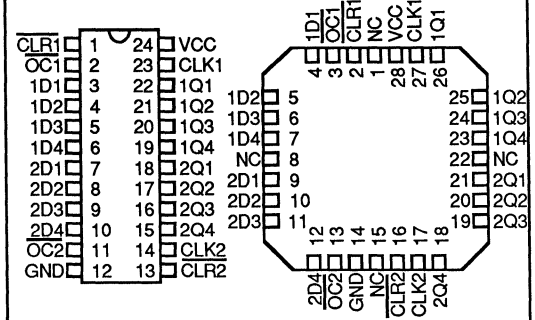
FUNCTIONAL DESCRIPTION:

These two sets of 4-bit registers have independent control signals. The $\overline{CLR}$ input clears the storage elements independent of the clock. The data is latched at the low to high transition of the clock.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

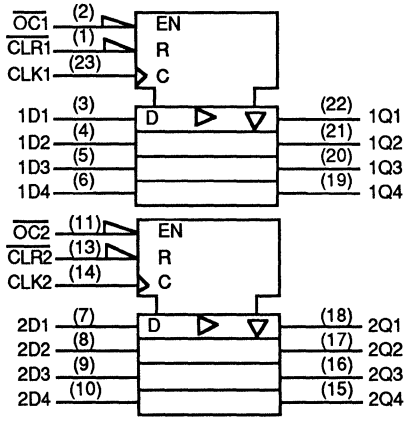
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

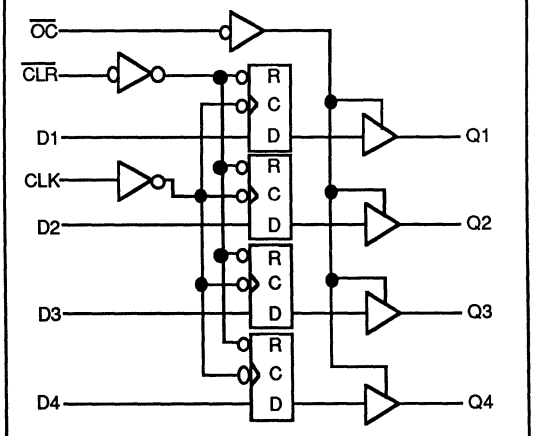
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

LOGIC DIAGRAM (EACH QUAD FLIP-FLOP, POSITIVE LOGIC)



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT876
V74ACT876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

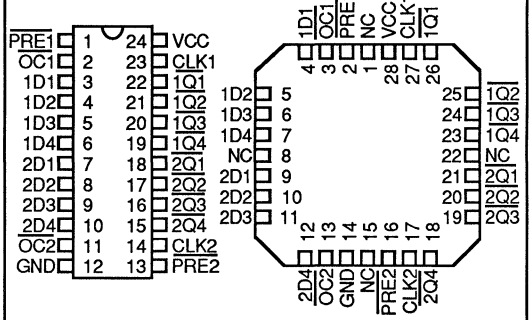
FUNCTIONAL DESCRIPTION:

These two sets of 4-bit registers have inverting outputs and independent control signals $\overline{OC}$, $\overline{PRE}$, and CLK. The $\overline{PRE}$ input low sets a logic one in the flip-flops and a logic low at the output $\overline{Q}$'s. $\overline{PRE}$ operates independent of the clock. All data is captured during the low to high transition of the clock signal.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TTL logic levels are ideal for interfacing with high-capacitance, low impedance loads.

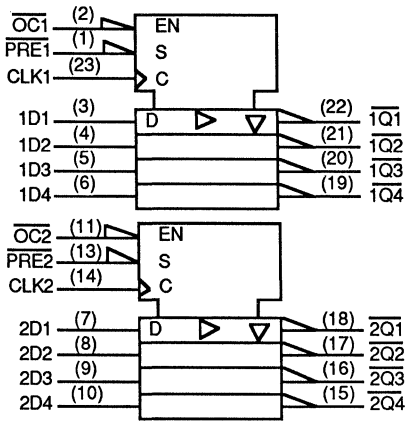
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

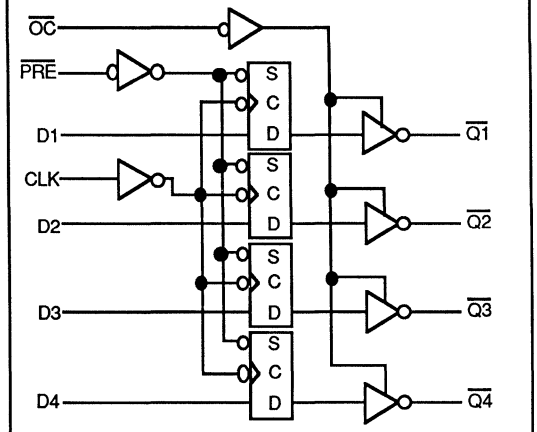
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

LOGIC DIAGRAM*
(EACH QUAD FLIP-FLOP, POSITIVE LOGIC)



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq 3$ nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	9	12	14	ns	2
t_{PLZ}		10							
		50	4	7	8	11	13	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq 3$ nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°CTyp	V_{CC}=5V±10% 25°CMax	85°CMax	125°CMax	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT878
V74ACT878
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

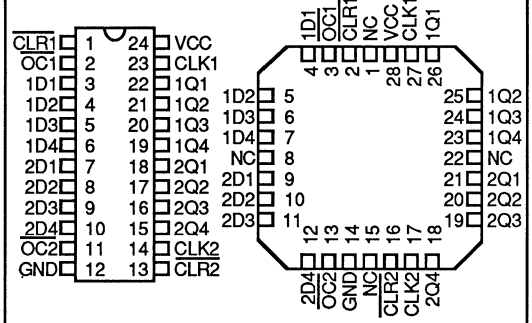
FUNCTIONAL DESCRIPTION:

These dual 4-bit registers have synchronous clear ($\overline{CLR}$). Both data and clear are latched by the low to high transition of the clock signal.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. The TTL logic levels are ideal for interfacing with high capacitance, low impedance loads.

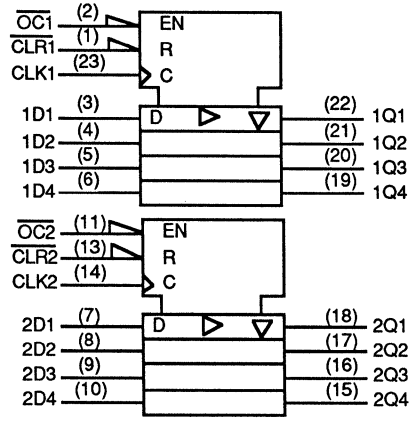
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

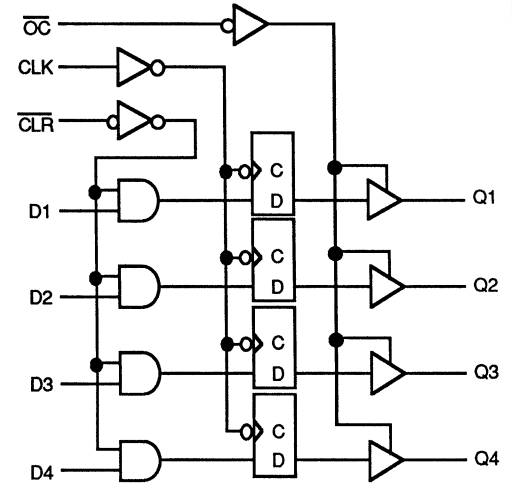
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

LOGIC DIAGRAM (EACH QUAD FLIP-FLOP, POSITIVE LOGIC)



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r ,t_f ≤ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Clock to Q	50	4	6	9	12	14	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	8	11	13	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , t_f ≤ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT879
V74ACT879
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48 mA Commercial, 32 mA Military
* Low Input Current, 1μA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

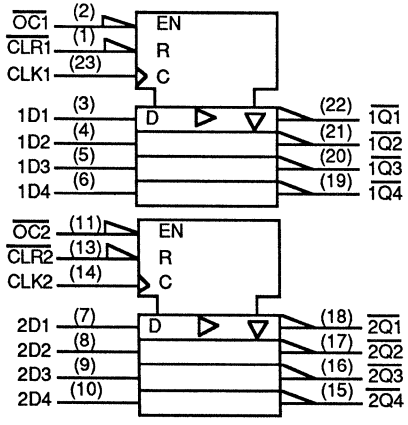
FUNCTIONAL DESCRIPTION:

These dual 4-bit registers have inverting outputs and synchronous clear ($\overline{CLR}$). Both data and clear are latched by the low to high transition of the clock signal.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. Data in flip-flops can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as working registers. TheTTL logic levels are ideal for interfacing with high capacitance, low impedance loads.

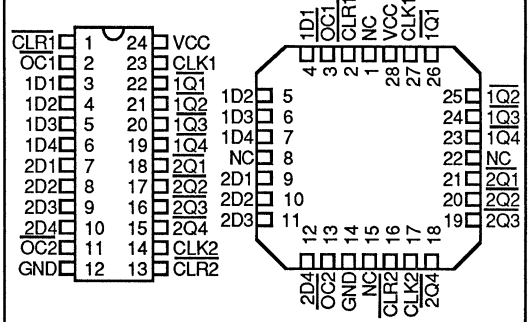
LOGIC SYMBOL*



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

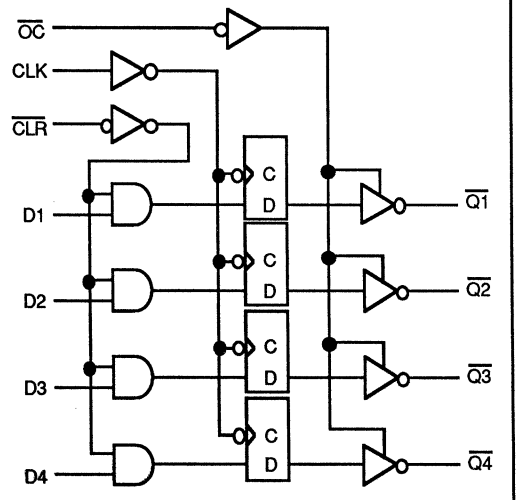
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC DIAGRAM (EACH QUAD FLIP-FLOP, POSITIVE LOGIC)



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V	V_{CC}=5V±10%			UNITS	FIGURE
				25°C Typ	25°C Max	85°C Max	125°C Max		
t_{PLH}	Prop. Delay Clock to Q	50	4	6	8	11	13	ns	3
		300							
t_{PHL}		50	4	6	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to Q	50	4	7	7	10	12	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{PHZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{PLZ}		10							
		50	4	7	9	12	14	ns	2
t_{TLH}	Output Trans. Time, Any Output 10-90% of 0-3.5V	50	1	2	3	4	5	ns	4
		300							
t_{THL}		50	1	2	3	4	5	ns	4
		300							
t_{PLH}	$\overline{CLR}$ to Q	50	4	6	8	11	13	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance			8	10	10	10	pF	
C_{PD}	Power Dissipation Cap. (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V	V_{CC}=5V±10%			UNITS	FIGURE
			25°C Typ	25°C Max	85°C Max	125°C Max		
t_S	Min Setup Time, Input D to Clock	1	2	3	3	3	ns	6
t_H	Min Hold Time, Clock to Input D	1	2	3	3	3	ns	6
t_W	Minimum Pulse Width, Clock	10	10	12	14	16	ns	5
t_S	Clock Enable ($\overline{CLKEN}$) setup time		1	2	2	2	ns	
t_H	Clock Enable ($\overline{CLKEN}$) hold time		1	2	2	2	ns	
F_{max}	Maximum Frequency		75	70	60	50	MHz	

V54ACT880
V74ACT880
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

FEATURES:

* CMOS Replacement for ALS
* High speed, 6ns Typical
* TTL Levels, I_{OL}/I_{OH} = 48/24 mA Commercial, 32/24 mA Military
* Low Input Current, 1µA Max
* Fully Specified: 5V ± 10% Power Supply, 50pF and 300pF Loading, Min and Max over Temperature

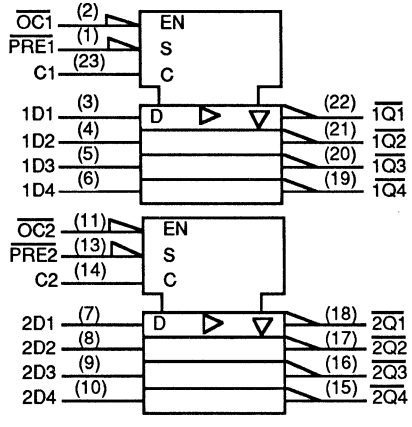
FUNCTIONAL DESCRIPTION:

These are dual 4-bit transparent inverting latches. While the enable C is high, the output $\overline{Q}$ will follow the inverted input D. When $\overline{PRE}$ is low, the output $\overline{Q}$ goes low.

The $\overline{OC}$ output control signal can be used to place all the outputs in active or high impedance state. The latch data can be changed independent of $\overline{OC}$.

These parts have been designed to interface with 3-state buses and I/O ports or used as storage elements.

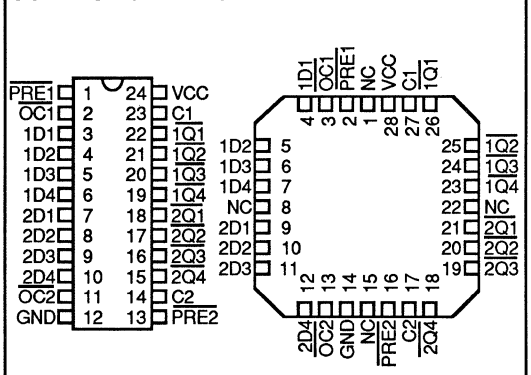
LOGIC SYMBOL*



FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	C	D	$\overline{Q}$
L	L	X	X	L
L	H	H	H	L
L	H	H	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

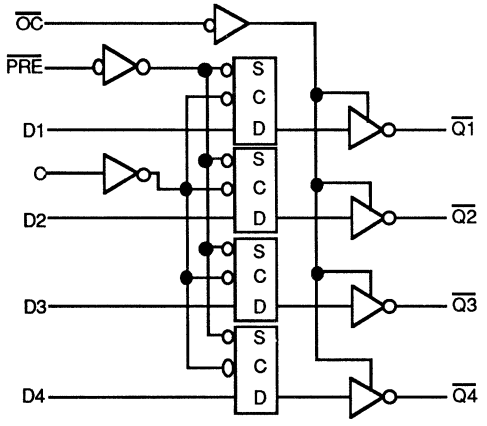
CONNECTION DIAGRAMS



DIP and SOIC (Top View)

PLCC and LCC (Top View)

LOGIC DIAGRAM (EACH QUAD LATCH, POSITIVE LOGIC)



*Note: Pinouts for DIP and SOIC only

RECOMMENDED OPERATING CONDITIONS

PRELIMINARY

SYMBOL	PARAMETER	Min		Typ		Max		UNIT
		Mil	Comm	Mil	Comm	Mil	Comm	
V_{CC}	Supply Voltage	4.5	4.5	5.0	5.0	5.5	5.5	V
T_A	Operating Free-Air Temp	-55	-40			125	85	°C
t_r , t_f	Input Rise and Fall Time			3	3	500	500	ns
V_{IH}	High Level Input Voltage	2.0	2.0			V_{CC}+0.5	V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage	-0.5	-0.5			0.8	0.8	V

AC CHARACTERISTICS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	C_L in pF	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay Input D to Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PLH}	Prop. Delay Latch Enable C to any Q	50	4	7	8	11	13	ns	3
		300							
t_{PHL}		50	4	7	9	12	14	ns	3
		300							
t_{PZH}	Prop. Delay Output Enable to any Q	50	4	6	8	11	13	ns	2
		300							
t_{PZL}		50	4	7	9	12	14	ns	2
		300							
t_{THZ}	Prop. Delay Output Disable to Q	10							
		50	4	7	10	13	15	ns	2
t_{TLZ}		10							
		50	4	7	9	12	14	ns	2
t_{PLH}	$\overline{PRE}$ to Q	50	4	7	9	12	14	ns	3
		300							
t_{PHL}	$\overline{CLR}$ to Q	50	4	7	9	12	14	ns	3
		300							
C_{IN}	Input Capacitance			4	6	6	6	pF	
C_{OUT}	Output Capacitance (Outputs Off)			8	10	10	10	pF	
C_{PD}	Power Dissipation Capacitance * (per buffer)			30	35	35	35	pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation where n = # of buffers

TIMING REQUIREMENTS: INPUT t_r , $t_f \leq$ 3 nsec

SYMBOL	PARAMETER	Min	V_{CC}=5V 25°C Typ	V_{CC}=5V±10% 25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_S	Min Setup Time, Input D to Latch Enable	1	2	3	3	3	ns	7
t_H	Min Hold Time, Latch Enable to Input Q	1	2	3	3	3	ns	7
t_W	Minimum Pulse Width	6	7	8	10	12	ns	5

NOTES

NOTES

TABLE OF CONTENTS
SECTION III

LINEAR SIGNAL PROCESSING

INTRODUCTION: LINEAR SIGNAL PROCESSING

The linear signal processing (LSP) product line is part of the system solution for such applications as scientific and medical instrumentation, data acquisition, process control and general signal processing on either side of the A/D and D/A conversion block.

VTC's unique complementary bipolar process (CBP) couples high speed with close device matching along with laser trimming capability. It forms the groundwork for LSP products such as operational, instrumentation, buffer, sample-hold, and transconductance amplifiers, comparators, timers, multipliers, and active filters.

As in all product lines offered by VTC, the emphasis is on performance and reliability. The devices are designed to fit applications where high-performance (high slew rate, low offsets or large power bandwidth, and output current capability) is required with reliability as a premium.

NOTES

VA033

VIDEO BUFFER

ADVANCE INFORMATION

FEATURES:

- High Slew Rate: 1300V/µs.
- Fast Rise Time: 3.0ns
- High Output Current: ±100mA
- Wide Bandwidth: 100MHz
- Replace Costly Hybrids
- Pin Compatible with HA-5033 and LH0033
- Output Short-Circuit Protection

DESCRIPTION:

The VA033 is a high speed video buffer amplifier designed to supply high current drive to more than 100MHz. The device will provide ±100mA into 100 ohm loads at slew rates of 1300V/µs. The VA033 offers excellent phase linearity up to 20MHz. It is intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, op amp isolation buffer for driving reactive loads, and high impedance input buffers for high speed A to Ds and comparators.

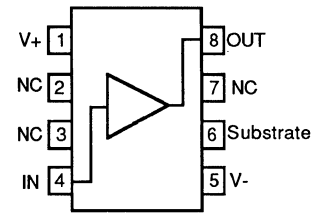
The VA033 is offered in either an 8-pin cerdip or TO-8, 12-pin metal can.

KEY PARAMETERS

Supply Voltage	±3V to ±6V
Slew Rate	1000V/µs, Min.
Input Offset Voltage	10mV, Max. at 25°C
Input Bias Current	.5µA, Max.
Output Voltage Swing	±3.5V @ R_L = 100 ohms
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	300mW, Typ.

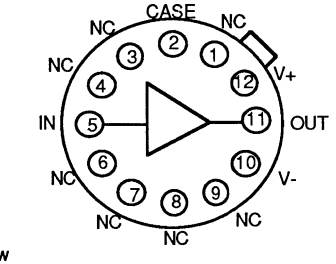
CONNECTION DIAGRAMS

Dual-In-Line Package



Top View

Metal Can Package



Top View

NOTES

VA705

HIGH-SPEED, PRECISION OPERATIONAL AMPLIFIER

PRELIMINARY

FEATURES

- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/µs
- Wide Bandwidth: 40MHz at A_{CL} = +1
- Low Offset Voltage: 1mV
- Low Offset Current: 10nA
- Ease of Use: Internally Compensated, Unity gain stable at C_L = 500pF
- Large Output Current: ±50mA
- Low Supply Voltage Operation: ±4V
- Wide Input Voltage Range: Within 1.5V of V+ and 0.5V of V-
- Short Circuit Protection

DESCRIPTION

The VA705 is a general purpose operational amplifier which combines the attributes of high speed with low offset voltage and current. This combination, along with a high open loop gain of 20,000V/V, allows the amplifier to fit into video processing, as well as signal conditioning applications where accuracy is at a premium. The same processing innovations which permit the high speed/low offset combination also allow very high output currents capable of driving large capacitive loads at high speeds.

The VA705 is internally compensated for stable operation even when driving capacitive loads of 500pF. The wide bandwidth of 40MHz and 35V/µs slew rate results in ±0.1% settling times of 250ns, which makes the amplifier ideal for fast data conversion systems.

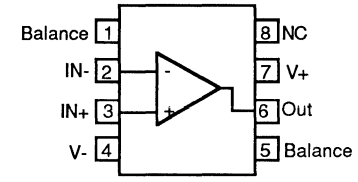
The high output current capability of ±50mA allows the amplifier to drive terminated transmission lines of 50 Ω with amplitudes of 5V peak to peak.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	|Vs| -0.5V
Power Dissipation	300 mW
Output Short Circuit Current Duration	Indefinite
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Lead Temperature (Soldering to 60 Sec.)	300°C

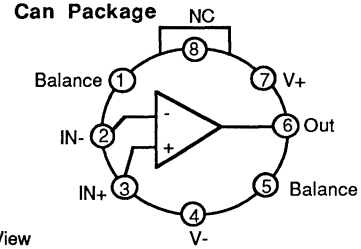
CONNECTION DIAGRAMS

Dual-In-Line Package



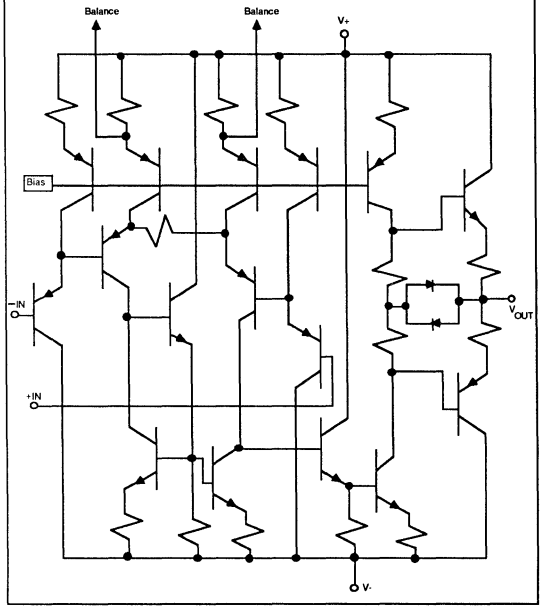
Top View

Metal Can Package



Top View

SIMPLIFIED SCHEMATIC



ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$ unless otherwise stated

			VA705J			VA705K			VA705L			
PARAMETER	*SYMBOL*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*MIN*	*TYP*	*MAX*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Offset Voltage	V_{OS}			6	10		3	5		1	2	mV
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		9	14		4	7		1.5	3	
Input Bias Current	I_B			550	850		550	700		500	600	nA
Input Offset Current	I_{OS}			35	100		25	50		25	50	nA
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		70	200		50	100		50	100	
Input Common Mode Range	V_{CM}		3 -4	3.5 -4.7		3 -4	3.5 -4.7		3 -4	3.5 -4.7		V
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$ $R_L = 2k\Omega$	2	5		4	10		10	20		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.5	+4 -4.2		±3.5	+4 -4.2		±3.5	+4 -4.2		V
		$R_L = 51\Omega$	±2.5			±2.5			±2.5			
Power Supply Current	I_S			7	10		7	10		7	10	mA
Minimum Supply Voltage	V_S	For Min. Open Loop Gain (A_V) of 2V/mV at $V_O = \pm 2V$	±4			±4			±4			V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	58	70		58	70		58	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	58	66		58	66		58	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	30	35		30	35		30	35		V/µs
Settling Time	t_S	To ±0.1% of Final Value (Figure 1)		250	300		250	300		250	300	ns
Gain Bandwidth Product	GBW	$A_V = +1$ $R_L = 2k\Omega$ $C_L = 50pF$ (Figure 1)		40			40			40		MHz
Small Signal Rise/Fall Time	t_r /t_f	E_O ±100mV 10-90% pts.		7			7			7		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6V$ p-p		1.8			1.8			1.8		MHz

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$ unless otherwise stated

			VA705M			VA705N			
PARAMETER	*SYMBOL*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Offset Voltage	V_{OS}			3	5		1	2	mV
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		4	7		1.5	3	
Input Bias Current	I_B			500	600		500	600	nA
Input Offset Current	I_{OS}			15	25		10	15	nA
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		30	50		20	30	
Input Common Mode Range	V_{CM}		3 -4	3.5 -4.7		3 -4	3.5 -4.7		V
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$ $R_L = 2k\Omega$	4	10		10	20		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.5	+4 -4.2		±3.5	+4 -4.2		V
		$R_L = 51\Omega$	±2.5			±2.5			
Power Supply Current	I_S			7	10		7	10	mA
Minimum Supply Voltage	V_S	For Min. Open Loop Gain (A_V) of 2V/mV $V_O = \pm 2V$	±4			±4			V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	58	70		58	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	58	66		58	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	30	35		30	35		V/μs
Settling Time	t_S	To ±0.1% of Final Value (Figure 1)		250	300		250	300	ns
Gain Bandwidth Product	GBW	$A_V = +1$ $R_L = 2k\Omega$ $C_L = 50pF$ (Figure 1)		40			40		MHz
Small Signal Rise/Fall Time	t_r /t_f	$E_O = \pm 100mV$ 10-90% pts.		7			7		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6V$ p-p		1.8			1.8		MHz

WAFER TEST LIMITS

V_S = ±5V, T_A = 25°C unless otherwise stated

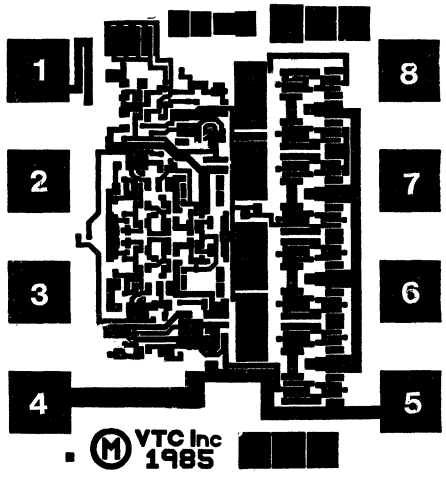
PARAMETER	SYM	CONDITIONS	VA705XK LIMIT	UNITS
Input Offset Voltage	V_{OS}		5	mV Max.
Input Bias Current	I_B		700	nA Max.
Input Offset Current	I_{OS}		50	nA Max.
Input Common Mode Range	V_{CM}		3 -4	V Min.
Open Loop Voltage Gain	A_V	V_{OUT} = ±3V R_L = 2k	4	V/mV Min.
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	±3.5	V Min.
		R_L = 51Ω	±2.5	
Power Supply Current	I_S		10	mA Max.
Minimum Supply Voltage	V_S	For Min. Open Loop Gain of 2V/mv at V_O = ±2V	±4	V Min.
Common Mode Rejection Ratio	CMRR	V_{CM} = ±2V	58	dB Min.
Power Supply Rejection Ratio	PSRR	ΔV_{PS} = ±0.5V	58	dB Min.
Slew Rate	SR	10-90% of Leading Edge (Fig. 1)	30	V/μs Min.

TYPICAL ELECTRICAL CHARACTERISTICS

V_S = ±5V, T_A = 25°C unless otherwise stated

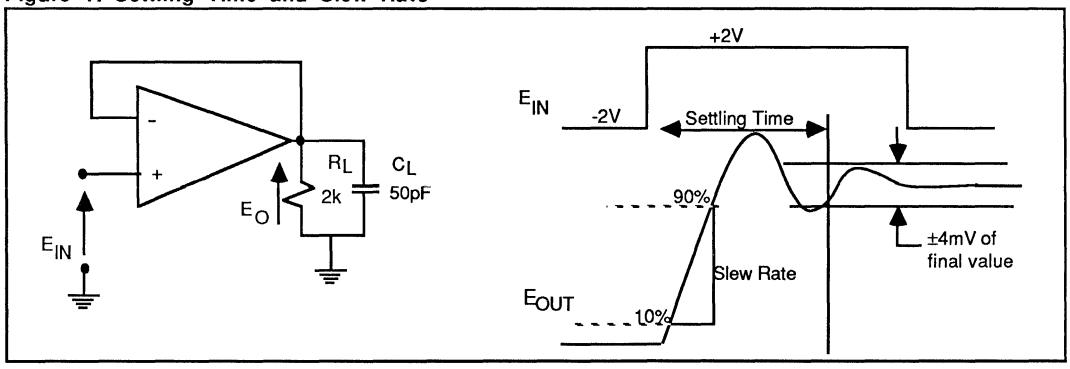
PARAMETER	SYM	CONDITIONS	VA705XK TYPICAL	UNITS
Input Offset Voltage $T_{Min.}$ to $T_{Max.}$	V_{OS}		4	mV
Input Offset Current $T_{Min.}$ to $T_{Max.}$	I_{OS}		50	nA
Settling Time	t_S	To ±0.1% of Final Value (Fig. 1)	250	ns
Gain Bandwidth Product	GBW	A_V = +1 R_L = 2kΩ C_L = 50pf (Fig. 1)	40	MHz
Small Signal Rise/Fall Time	r_t/f_t	E_O = ±100mV 10-90% (Fig. 1)	7	ns
Full Power Bandwidth	BW_{FP}	R_L = 2kΩ C_L = 50pf V_{OUT} = 6V p-p	1.8	MHz

DIE



Die size = 0.035 x 0.035 inch (1225 sq. mils)
0.89 x 0.89 mm (0.79 sq. mm)
Shipped in die crates (400 die per crate)

Figure 1: Settling Time and Slew Rate



APPLICATION INFORMATION

Layout Considerations:

As with any high speed wide band amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1µF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

Frequency Compensation:

Although the amplifier is unconditionally stable at a non-inverting gain of 1, even when driving a capacitive load of 500pF, certain applications require frequency response tailoring if such characteristics as bandwidth and settling time are to be optimized.

For applications in which a large value of feedback resistor is used (Figure 2), it may be necessary to add a small capacitor (C2 = 1-3pF) in parallel with R2 in order to minimize settling time. Without C2 the input capacitance introduces an additional pole in the loop response, which has an adverse effect on stability and resulting settling time.

Also, with capacitive loads of 750pF and larger, it may be desirable to decouple the load with a small resistor of 10 to 30 ohms (R3, Figure 2) to minimize amplifier ringing.

Figure 2: Frequency Compensation Techniques

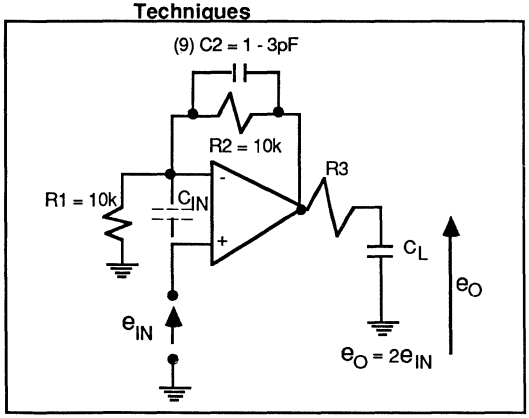
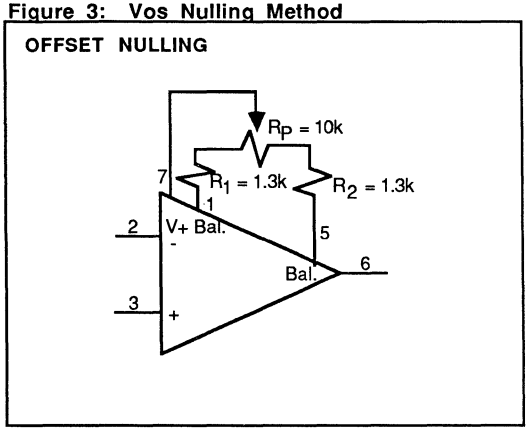


Figure 3: Vos Nulling Method



The configuration of Figure 3 will give a typical V_{OS} nulling range of ±15mV. If a smaller adjustment t range is desired, resistor values R1 = R2 can be increased accordingly. For example, at R1 = 3.6kΩ, the adjustment range is ±5mV.

VA2705

DUAL HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES:

- Dual Version of VA705 Fast Settling Op Amp
- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/µs
- Wide Gain Bandwidth: 40 MHz at A_{CL} = +1
- Low Offset Voltage: 1mV
- Low Offset Current: 10nA
- Large Output Current: ±50mA
- Short Circuit Protection
- Industry Standard Pinout

DESCRIPTION:

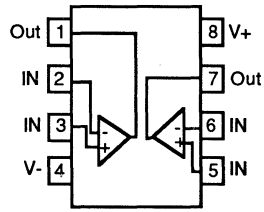
The VA2705 offers the high-speed (35V/µs), precision advantages of theVA705 in a dual package configuration. The small offsets and open-loop gain (20k V/V) make the amplifier ideal for video processing and signal conditioning applications where accuracy is at a premium. The VA2705 is offered in an 8-pin cerdip, plastic or metal can package.

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	.30V/µs, Min.
Input Offset Voltage	.2, 5, 10mV at 25°C
Input Offset Current	15nA Max., at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	550mW, Typ.

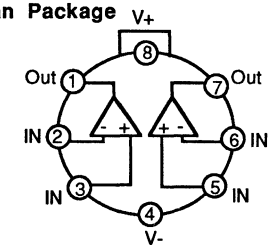
CONNECTION DIAGRAMS:

Dual-In-Line Package



Top View

Metal Can Package



Top View

LINEAR SIGNAL PROCESSING

VA2715

DUAL HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- Complete Dual Version of VA705 Fast Settling Op Amp
- Dual Includes Balance for Both Amplifiers
- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/µs
- Wide Bandwidth: 40MHz at A_{CL}= +1
- Low Offset Voltage: 1mV
- Low Offset Current: 10nA
- Large Output Current: ±50mA
- Short Circuit Protection

DESCRIPTION

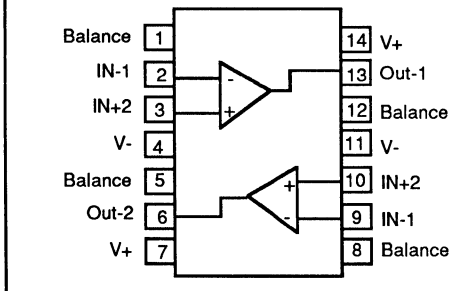
The VA2715 offers the high-speed (35V/µs) precision advantages of the VA705 in a dual package configuration. This dual isunique because it offers balancing inputs for both amplifiers for those applications which require nulling. The small offsets and high open-loop gain (20k V/V) make the amplifier ideal for video processing and signal conditioning applications where accuracy is at a premium. The VA2715 is available in either a 14-pin cerdip or plastic package.

KEY PARAMETERS

Supply Voltages	±4V to ±6V
Differential Input Voltages	±9V
Input Offset Voltage	2, 5, 10mV at 25°C
Input Offset Current	15nA, Max. at 25°C
Sew Rate	30V/µs, Min.
Operating Temperature	0° to 70°C
Storage Temperature	-65° to +150°C
Power Dissipation	550mW

CONNECTION DIAGRAM:

Dual In-Line Package



Top View

LINEAR SIGNAL PROCESSING

VA4705

QUAD HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

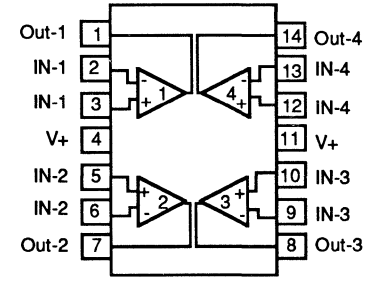
- Quad Version of VA705 Fast Settling Op Amp
- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/µs
- Wide Gain Bandwidth: 40 MHz at A_{CL} = +1
- Low Offset Voltage: 1mV
- Low Offset Current: 10nA
- Large Output Current: ±50mA
- Short Circuit Protection
- Industry Standard Pinout

DESCRIPTION

The VA4705 offers the high-speed (35V/µs) precision advantages of the VA705 in a quad package configuration. The small offsets and open-loop gain (20k V/V) make the amplifier ideal for video processing and signal conditioning applications where accuracy is at a premium. The VA4705 is offered in either a 14-pin cerdip or plastic package.

CONNECTION DIAGRAM:

Dual In-Line Package



Top View

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	30V/µs, Min.
Input Offset Voltage	2, 5,10mV at 25°C
Input Offset Current	15nA Max., at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	750mW, Typ.

VA706

HIGH-SPEED, FAST-SETTLING OPERATIONAL AMPLIFIER

PRELIMINARY

FEATURES

- Fast Settling Time: ±0.1% in 200ns
- High Slew Rate: 42V/µs
- Wide Bandwidth: 40MHz at A_{CL} = +1
- Ease of Use: Internally Compensated, Unity gain stable at C_L = 500pF
- Large Output Current: ±50mA
- Low Supply Voltage Operation: ±4V
- Wide Input Voltage Range: Within 1.5V of V+ and 0.5V of V-
- Short Circuit Protection

DESCRIPTION

The VA706 is a high-speed general purpose monolithic operational amplifier useful for signal frequencies extending into the video range. The same processing innovations which permit the high speed also allow very high output currents capable of driving large capacitive loads at high speeds.

The high open-loop voltage gain of 5000V/V and high slew rate of 40V/µs make the VA706 ideal for analog amplification and processing of high-speed signals.

The VA706 is internally compensated for stable operation when driving capacitive loads up to 500pF. The wide bandwidth of 40MHz and 40V/µs slew rate results in ±0.1% settling times of 200ns, which makes the amplifier ideal for fast data conversion systems.

The high output current capability of ±50mA allows the amplifier to drive terminated transmission lines of 50 Ω with amplitudes of 5V peak to peak.

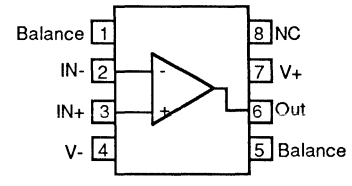
Along with the high speed and output drive capability, a 25nA offset current and trimmable offset voltage make the VA706 usable for signal conditioning applications where accuracy must be maintained.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	$\|V_S\|$ -0.5V
Power Dissipation	300mW
Output Short Circuit Current Duration	Indefinite
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Lead Temperature (Soldering to 60 Sec.)	300°C

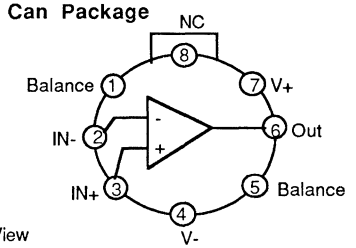
CONNECTION DIAGRAMS

Dual-In-Line Package



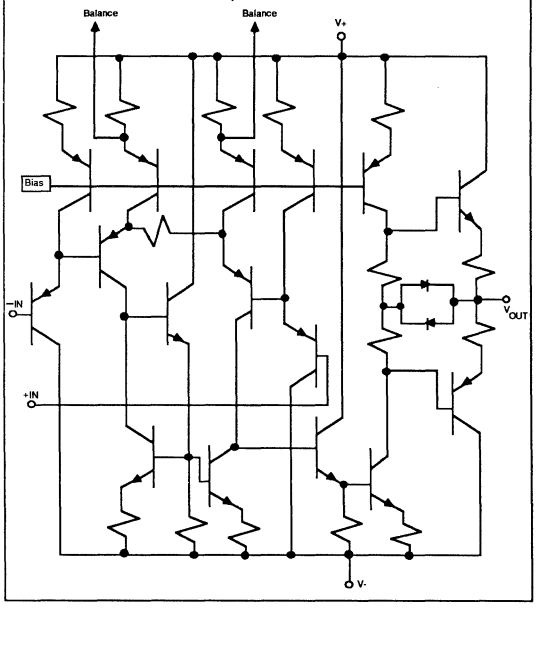
Top View

Metal Can Package



Top View

SIMPLIFIED SCHEMATIC



ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$ unless otherwise stated

			VA706J			VA706K			VA706L			
PARAMETER	*SYMBOL*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*MIN*	*TYP*	*MAX*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Offset Voltage	V_{OS}			8	20		6	15		4	10	mV
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		11	28		9	22		6	14	
Input Bias Current	I_B			550	850		550	700		550	700	nA
Input Offset Current	I_{OS}			35	100		25	50		25	50	nA
$T_{Min.}$ to $T_{Max.}$		$0° \le T_A \le 70°C$		70	200		50	100		50	100	
Input Common Mode Range	V_{CM}		3 -4	3.5 -4.7		3 -4	3.5 -4.7		3 -4	3.5 -4.7		V
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$ $R_L = 2k\Omega$	1	5		2	5		2	5		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.5	+4 -4.2		±3.5	+4 -4.2		±3.5	+4 -4.2		V
		$R_L = 51\Omega$	±2.5			±2.5			±2.5			
Power Supply Current	I_S			7	10		7	10		7	10	mA
Minimum Supply Voltage	V_S	For Min. Open Loop Gain (A_V) of 1V/mV at $V_O = \pm 2V$	±4			±4			±4			V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	58	70		58	70		58	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	58	66		58	66		58	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	38	42		38	42		38	42		V/µs
Settling Time	t_S	To ±0.1% of Final Value (Figure 1)		200	250		200	250		200	250	ns
Gain Bandwidth Product	GBW	$A_V = +1$ $R_L = 2k\Omega$ $C_L = 50pF$ (Figure 1)		40			40			40		MHz
Small Signal Rise/Fall Time	t_r / t_f	E_O ±100mV 10-90% pts.		7			7			7		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6V$ p-p		2.2			2.2			2.2		MHz

WAFER TEST LIMITS

V_S = ±5V, T_A = 25°C unless otherwise stated

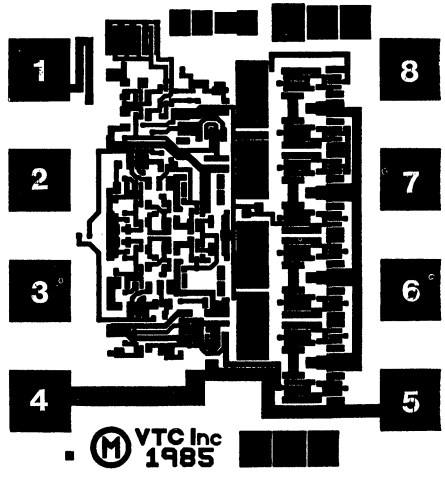
PARAMETER	SYM	CONDITIONS	VA706XK LIMIT	UNITS
Input Offset Voltage	V_{OS}		15	mV Max.
Input Bias Current	I_B		700	nA Max.
Input Offset Current	I_{OS}		50	nA Max.
Input Common Mode Range	V_{CM}		3 -4	V Min.
Open Loop Voltage Gain	A_V	V_{OUT} = ±3V R_L = 2k	2	V/mV Min.
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	±3.5	V Min.
		R_L = 51Ω	±2.5	
Power Supply Current	I_S		10	mA Max.
Minimum Supply Voltage	V_S	For Min. Open Loop Gain of 2V/mv at V_O = ±2V	±4	V Min.
Common Mode Rejection Ratio	CMRR	V_{CM} = ±2V	58	dB Min.
Power Supply Rejection Ratio	PSRR	ΔVPS = ±0.5V	58	dB Min.
Slew Rate	SR	10-90% of Leading Edge (Fig. 1)	38	V/μs Min.

TYPICAL ELECTRICAL CHARACTERISTICS

V_S = ±5V, T_A = 25°C unless otherwise stated

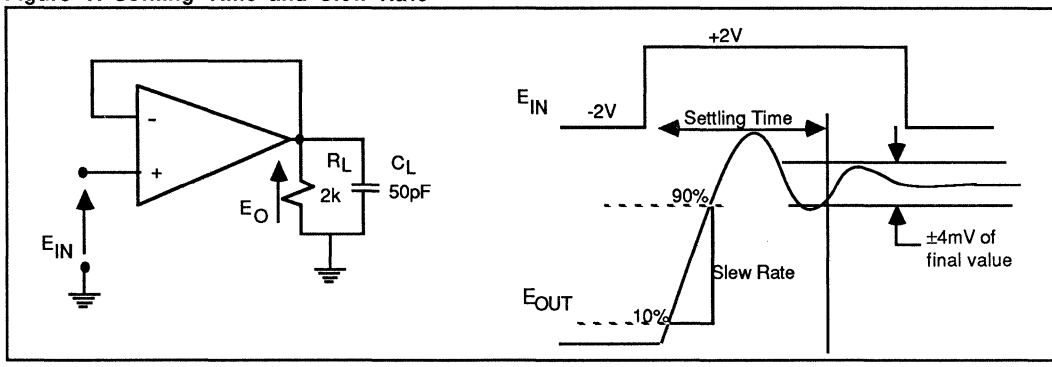
PARAMETER	SYM	CONDITIONS	VA706XK TYPICAL	UNITS
Input Offset Voltage $T_{Min.}$ to $T_{Max.}$	V_{OS}		9	mV
Input Offset Current $T_{Min.}$ to $T_{Max.}$	I_{OS}		50	nA
Settling Time	t_S	To ±0.1% of Final Value (Fig. 1)	200	ns
Gain Bandwidth Product	GBW	A_V = +1 R_L = 2kΩ C_L = 50pf (Fig. 1)	40	MHz
Small Signal Rise/Fall Time	r_t/f_t	E_O = ±100mV 10-90% (Fig. 1)	7	ns
Full Power Bandwidth	BW_{FP}	R_L = 2kΩ C_L = 50pf V_{OUT} = 6V p-p	2.2	MHz

DIE



Die size = 0.035 x 0.035 inch (1225 sq. mils)
0.89 x 0.89 mm (0.79 sq. mm)
Shipped in die crates

Figure 1: Settling Time and Slew Rate



APPLICATION INFORMATION

Layout Considerations:

As with any high speed wide band amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1µF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

Frequency Compensation:

Although the amplifier is unconditionally stable at a non-inverting gain of 1, even when driving a capacitive load of 500pF, certain applications require frequency response tailoring if such characteristics as bandwidth and settling time are to be optimized.

For applications in which a large value of feedback resistor is used (Figure 2), it may be necessary to add a small capacitor (C2 = 1-3pF) in parallel with R2 in order to minimize settling time. Without C2 the input capacitance introduces an additional pole in the loop response, which has an adverse effect on stability and resulting settling time.

Also, with capacitive loads of 750pF and larger, it may be desirable to decouple the load with a small resistor of 10 to 30 ohms (R3, Figure 2) to minimize amplifier ringing.

Figure 2: Frequency Compensation Techniques

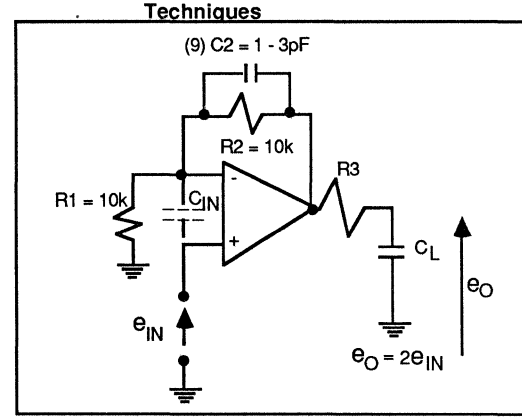
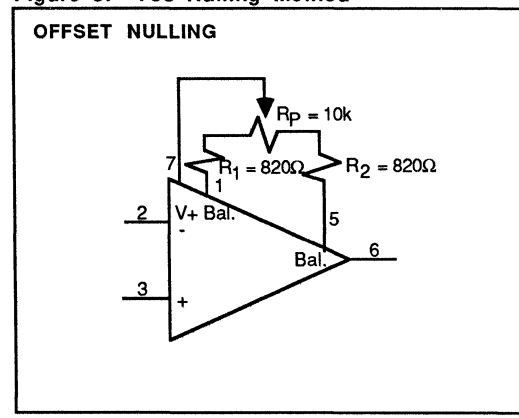


Figure 3: Vos Nulling Method



The configuration of Figure 3 will give a typical V_{OS} nulling range of ±25mV. If a smaller adjustment t range is desired, resistor values R1 = R2 can be increased accordingly. For example, at R1 = 1.3kΩ, the adjustment range is ±15mV.

VA2706

DUAL HIGH-SPEED, FAST-SETTLING OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES:

- Dual Version of VA706 Fast Settling Op Amp
- Fast Settling Time: ±0.1% in 200ns
- High Slew Rate: 42V/µs
- Wide Gain Bandwidth: 40 MHz at A_{CL} = +1
- Low Offset Voltage: 4mV
- Low Offset Current: 25nA
- Large Output Current: ±50mA
- Short Circuit Protection
- Industry Standard Pinout

DESCRIPTION:

The VA2706 offers the high-speed (40V/µs) fast settling advantages of the VA706 in a dual package configuration. The high slew rate, output drive and open loop-gain (5k V/V) allows the amplifier to fit analog amplification and high-speed processing applications capable of driving large capacitance loads at high speeds.

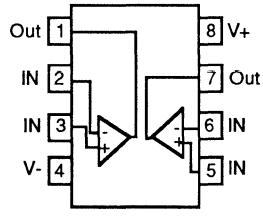
The VA2706 is offered in an 8-pin cerdip, plastic or metal can package.

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	.38V/µs, Min.
Input Offset Voltage	10mV Max.
Input Offset Current	15nA Max., at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	550mW, Typ.

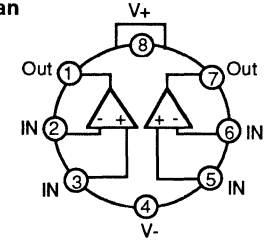
CONNECTION DIAGRAMS:

Dual-In-Line Package



Top View

Metal Can



Top View

VA2716

DUAL HIGH-SPEED, FAST-SETTLING OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- Complete Dual Version of VA706 Fast Settling Op Amp
- Dual Includes Balance for Both Amplifiers
- Fast Settling Time: ±0.1% in 200ns
- High Slew Rate: 42V/µs
- Wide Bandwidth: 40MHz at A_{CL}= +1
- Low Offset Voltage: 4mV
- Low Offset Current: 25nA
- Large Output Current: ±50mA
- Short Circuit Protection

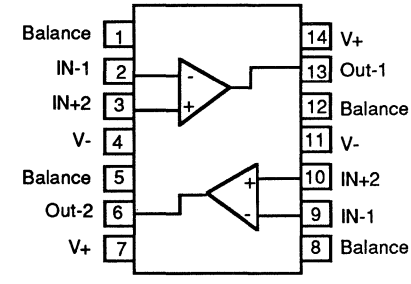
DESCRIPTION

The VA2716 offers the high-speed (40V/µs) fast settling advantages of theVA706 in a dual package configuration. This dual is unique because it offers balancing inputs for both amplifiers for those applications which require nulling. The high slew rate, output drive and open-loop gain (5k V/V) allows the amplifier to fit analog amplification and high speed processing applications, capable of driving large capacitance loads at high speeds.

The VA2715 is available in either a 14-pin cerdip or plastic package.

CONNECTION DIAGRAM:

Dual In-Line Package



Top View

KEY PARAMETERS

Supply Voltages	±4V to ±6V
Differential Input Voltages	±9V
Input Offset Voltage	10mV at 25°C
Input Offset Current	15nA, Max. at 25°C
Slew Rate	38V/µs, Min.
Operating Temperature	0° to 70°C
Storage Temperature	-65° to +150°C
Power Dissipation	550mW

VA4706

QUAD HIGH-SPEED, FAST-SETTLING OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- Quad Version of VA706 Fast Settling Op Amp
- Fast Settling Time: ±0.1% in 200ns
- High Slew Rate: 42V/µs
- Wide Bandwidth: 40MHz at A_{CL} = +1
- Low Offset Voltage: 4mV
- Low Offset Current: 25nA
- Large Output Current: ±50mA
- Short Circuit Protection

DESCRIPTION

The VA4706 offers the high-speed (40V/µs) fast settling advantages of the VA706 in a quad package configuration. The high slew rate, output drive and open-loop gain (5k V/V) allows the amplifier to fit analog amplification and high speed processing applications, capable of driving large capacitance loads at high speeds.

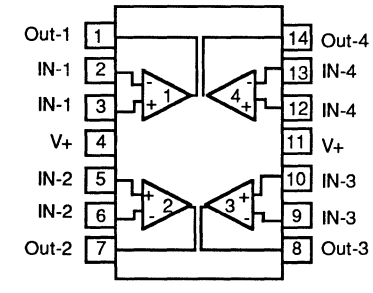
The VA4706 is available in either a 14-pin cerdip or plastic package.

KEY PARAMETERS

Supply Voltages	±4V to ±6V
Differential Input Voltages	±9V
Input Offset Voltage	10mV at 25°C
Input Offset Current	15nA, Max. at 25°C
Slew Rate	38V/µs, Min.
Operating Temperature	0° to 70°C
Storage Temperature	-65° to +150°C
Power Dissipation	750mW

CONNECTION DIAGRAM:

Dual In-Line Package



Top View

LINEAR SIGNAL PROCESSING

VA707

HIGH SLEW RATE, WIDEBAND OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- High Slew Rate: 150V/µs
- Wide Gain Bandwidth: 200 MHz at A_{CL}= +5
- Full Power Bandwidth: 7.5MHz
- Low Offset Voltage: 5mV
- Open Loop Gain: 10k V/V
- High Output Current: ±50mA

DESCRIPTION

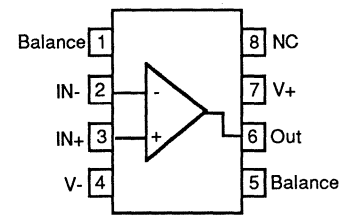
The VA707 provides the same high performance as the VA705 and VA706, but the design has been optimized for circuits with gains greater than 5. This design change in the VA707 increases the slew rate to 150V/µs and gain bandwidth product to 200MHz. As with the VA705 and VA706, it is especially suited to video processing and signal conditioning applications where speed and accuracy are at a premium. The ±50mA output capability allows the amplifier to drive large capacitive loads at high speeds in addition to delivering a 5V p-p output to a 50 ohm terminated transmission line. The VA707 is offered in an 8-pin cerdip, plastic or TO-99 metal can package.

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	100V/µs, Min.
Input Offset Voltage	10mV, Max. at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	300mW, Typ.

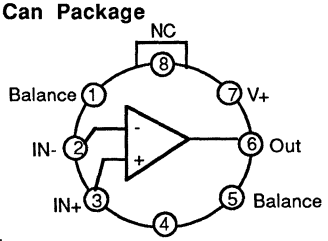
CONNECTION DIAGRAMS:

Dual-In-Line Package



Top View

Metal Can Package



Top View

VA2707

DUAL HIGH SLEW RATE, WIDEBAND OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- Dual Version of VA707 Fast Settling Op Amp
- High Slew Rate: 150V/µs
- Wide Gain Bandwidth: 200 MHz at A_{CL} = +5
- Full Power Bandwidth: 7.5MHz
- Low Offset Voltage: 5mV
- Open Loop Gain: 10k V/V
- High Output Current: ±50mA
- Industry Standard Pinout

DESCRIPTION

The VA2707 is a dual version of the VA707. The design has been optimized for circuits with gains greater than 5. The VA2707 offers the same high slew rate of the VA707 (150 V/µs) and gain bandwidth product to 200MHz. As with the VA707, it is especially suited to video processing and signal conditioning applications where speed and accuracy are at a premium. The ±50mA output capability allows the amplifier to drive large capacitance loads at high speeds in addition to delivering a 5V p-p output to a 50 ohm terminated transmission line.

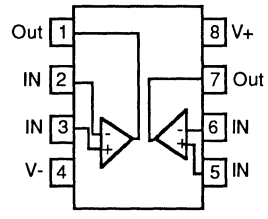
The VA2707 is offered in an 8-pin cerdip, plastic or TO-99 metal can package.

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	100V/µs, Min.
Input Offset Voltage	10mV Max. at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	550mW, Typ.

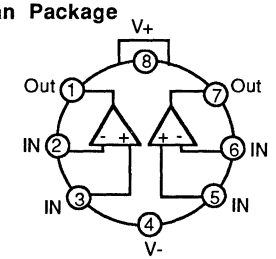
CONNECTION DIAGRAMS:

Dual-In-Line Package



Top View

Metal Can Package



Top View

VA4707

QUAD HIGH SLEW RATE, WIDEBAND OPERATIONAL AMPLIFIER

ADVANCE INFORMATION

FEATURES

- Quad Version of VA707 High Speed Op Amp
- High Slew Rate: 150V/µs
- Wide Gain Bandwidth: 200 MHz at A_{CL} = +5
- Full Power Bandwidth: 7.5MHz
- Low Offset Voltage: 5mV
- Open Loop Gain: 10k V/V
- High Output Current: ±50mA
- Industry Standard Pinout

DESCRIPTION

The VA4707 is a quad version of the VA707. The design has been optimized for circuits with gains greater than 5. The VA4707 offers the same high slew rate of the VA707 (150 V/µs) and gain bandwidth product to 200MHz. As with the VA707, it is especially suited to video processing and signal conditioning applications where speed and accuracy are at a premium. The ±50mA output capability allows the amplifier to drive large capacitance loads at high speeds in addition to delivering a 5V p-p output to a 50 ohm terminated transmission line.

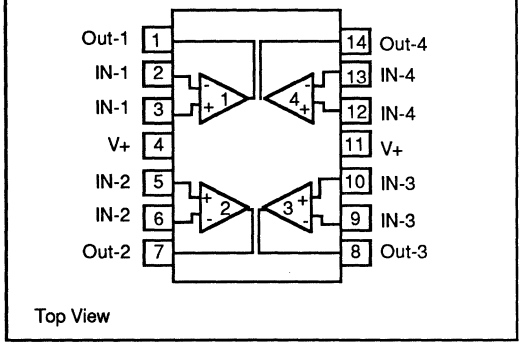
The VA4707 is offered in a14-pin cerdip or plastic package.

KEY PARAMETERS

Supply Voltage	±4V to ±6V
Differential Input Voltages	±9V
Slew Rate	100V/µs, Min.
Input Offset Voltage	10mV Max. at 25°C
Operating Temperature Range	0° to 70°C
Storage Temperature Range	-65° to +150°C
Power Dissipation	750mW, Typ.

CONNECTION DIAGRAM:

Dual In-Line Package



Top View

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SECTION IV

BIPOLAR SEMICUSTOM

INTRODUCTION: BIPOLAR SEMICUSTOM

VTC's semicustom products offer solutions for linear/digital bipolar and high-speed digital bipolar circuits.

The VJ800 family of analog master chips is a cost-effective solution for low-volume linear/digital applications.

The VL1000 Linear Bipolar Cell Library has flexible, high performance LSI linear/digital solutions on a common chip. It consists of a predefined cell library with versatile linear and digital functions.

The VL2000 High Performance Digital Bipolar Cell Library provides sophisticated cell-based subnano-second circuitry which solves digital systems problems with either TTL or ECL input/outputs.

Full custom designs are available where volumes or system requirements make this a more viable solution.

All semicustom products are workstation and personal computer-based, with excellent documentation and applications support.

NOTES

VJ800
ANALOG MASTER CHIP

FEATURES
- 636 Transistors
- 706 Resistors, 150 Ω to 15k Ω
- 18 On-Chip Junction Capacitors
- Suitable for 5V or 12V Power Supplies
- NPN, f_T of 800MHz Minimum
- Economical Chip Size: 126x126 Mils
- Two-Layer Metal for Excellent Utilization and Routability
- 1.5ns CML Functions Easily Integrated
- Workstation/PC-Based Schematic Entry and Simulation Available
- Accommodates up to 40 Pins

APPLICATIONS
- Peripherals
- Instrumentation
- Telecommunications
- Discrete Circuit Replacement
- Analog Signal Processing
- Linear/Digital Subsystems
- Linear LSI Subsystems

DESCRIPTION
The VJ800 Analog Master Chip is a versatile, high-performance, bipolar integrated circuit containing prediffused transistors, resistors and capacitors. The components interconnect to define either analog or associated 1.5ns current mode logic (CML) functions. Diffused resistor values are user-programmable. Implanted resistors have fixed taps.

The chip is ideal for high-performance amplifiers with low-noise inputs—for example, in disk or tape drives. The VJ800 component library is available on diskettes for schematic entry and SPICE simulation.

ORGANIZATION
The VJ800 Analog Master Chip is organized with components symmetrical around the Y-axis. This organization allows for maximum density and routability.

On the VJ800 chip periphery are 40 bonding pads and 18 5pF junction capacitors.

The low-noise NPN transistors are located at the top of the chip and arranged in a common-centroid configuration for low offset voltage and differential input stage use. These transistors are located close to the I/O pads and across the chip from the power transistors to avoid noise or crosstalk.

The power-transistors are located at the bottom of the chip and close to the bonding pads.

The small NPN transistors at the center of the chip are laid out for easy current mode logic (CML) implementation. A two-input CML NOR gate can be formed from each cell. These transistors can also be used for analog functions.

The remaining small and medium NPN transistors are uniformly positioned around the chip for easy use.

The two-collector PNP transistors are evenly divided into two groups centered on the Y-axis between the small transistors in the center of the chip and the large transistors on the outer chip edge.

The diffused and implanted resistors are located near the transistor cells for easy connection. The diffused resistors are available in approximately 20-Ohm increments while the implanted resistors have fixed taps. Resistors can be placed in series or parallel combinations.

Components are interconnected using two layers of metal. Unused components can be routed over to increase component utilization and to ease routing.

EVALUATION CIRCUIT
A VJ800 evaluation circuit is available to allow the prospective user to easily evaluate performance. The evaluation circuit contains a bandgap reference, a 733 video amplifier, a 4-bit counter and an operational amplifier implemented on a single chip and available in a 40-pin DIP package.

DESIGNING
Designing with the VJ800 is straightforward. The design kit provides all information necessary to design on a workstation or computer and includes:
- VJ800 User's Guide
- Analog Master Chip Design Manual
- VJ800 component library on diskette for Mentor Graphics workstation, with instruction manual
- Symbolic mylar plot for layout

The VJ800 component library is used on a Mentor Graphics workstation for schematic entry and simulation, or simulation models from the User's Guide can be loaded into any computer running SPICE simulation.

The VJ800 User's Guide and Design Manual provide detailed information to aid the user in Analog Master Chip design philosophy, circuit design and simulation, circuit layout and forms for easy transmittal of circuit test requirements.

TESTING
The VJ800 User's Guide specifies requirements for automatic circuit testing.

SUBMITTAL
When design is complete, the circuit components are interconnected on the mylar plot by the user (or, for an optional charge, this can be done by VTC Incorporated). The circuit schematic, test specification and mylar plot are then forwarded to VTC. VTC will enter the data into its CAD system, fabricate masks and wafers, package, test and ship 15 prototypes.

VJ800 COMPONENT LIST:

QUANTITY	TYPE	COMPONENT	NAME	COMMENTS
310	NPN	Small Transistor, 0.5mA	T3	$f_T = 800$ MHz
168	NPN	Medium Transistor, 2mA	T12	$f_T = 800$ MHz
26	NPN	Low Noise Transistor, 10mA	TLN1	$f_T = 800$ MHz
5	NPN	Power Transistor, 180mA	T50	$f_T = 800$ MHz
32	NPN	Small Schottky, 5mA	T3S	$f_T = 800$ MHz
54	NPN	Medium Schottky, 8mA	T30S	$f_T = 800$ MHz
5	NPN	Power Schottky, 180mA	T50S	$f_T = 800$ MHz
36	PNP	Two Collector, 0.33mA	TLP1	$f_T = 80$ MHz
74	DIFFUSED	300 Ohm Resistor	A	Variable *(Note 1)*
153	DIFFUSED	600 Ohm Resistor	B	Variable *(Note 2)*
112	DIFFUSED	1200 Ohm Resistor	C	Variable *(Note 2)*
293	IMPLANT	3.2K Ohm Resistor	D	Tapped *(Note 3)*
74	IMPLANT	15K Ohm Resistor	E	Tapped *(Note 4)*
18	JUNCTION	Capacitor, 5pF	JCAP	

NOTES:
(1) Minimum single value is 130 Ohm.
(2) Minimum single value is 150 Ohm.
(3) Fixed tap values of 1.6K Ohm and 3.2K Ohm.
(4) Fixed Tap Values of 5K, 10K and 15K Ohm.

ELECTRICAL CHARACTERISTICS:

TRANSISTORS

NAME	TYPE	I_C (mA) (Note 1)	BETA			BVCBO (V)			BVEBO (V)			LVCEO (V)
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN
T3	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T12	NPN	2	50	100	200	25	30	35	5.6	5.85	6.2	7
TLN1	NPN	10	50	100	200	25	30	35	5.6	5.85	6.2	7
T50	NPN	180	50	100	200	25	30	35	5.6	5.85	6.2	7
T3S	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T30S	NPN	8	50	100	200	25	30	35	5.6	5.85	6.2	7
T50S	NPN	180	50	100	200	25	30	35	5.6	5.85	6.2	7
TLP1 (Note 2)	PNP	0.16	50	120	250	25	30	35	25	30	35	13.2

RESISTORS:

NAME	RESISTOR TYPE	LINEAR TEMPERATURE COEFFICIENT	QUADRATIC TEMPERATURE COEFFICIENT	CAPACITANCE PICOFARAD OV BIAS	TOLERANCE %	
					ABS.	MATCH (Note 3)
A	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.116	20	1
B	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.136	20	1
C	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.24	20	1
D	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.114	20	2
E	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.192	20	2

NOTES:
(1) Switching time and frequence response will be best at maximum I_C.
(2) Applies to each of the two collectors.
(3) Adjacent resistors in the same plane.

VJ801

EVALUATION CHIP FOR THE VJ800 ANALOG MASTER CHIP

FEATURES:

- Low-Noise 733 Video Amplifier
- Bandgap Voltage Reference
- 4-Bit CML Counter with TTL I/O
- CML Bias generator
- 0.5mA NPN Transistor
- 8mA Schottky NPN Transistor
- Lateral PNP Transistor

DESCRIPTION:

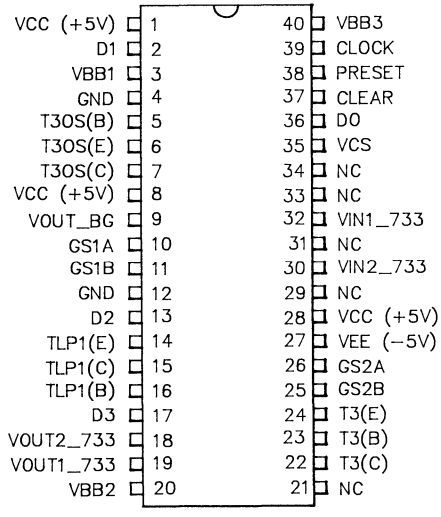
The VJ801 Evaluation Chip contains several analog and digital circuits that were built using the VJ800 Analog Master Chip. This chip serves as a vehicle for evaluating the capabilities of the VJ800 Analog Master Chip. All inputs and outputs of the individual circuits are pinned-out individually to allow for evaluation of each circuit separately. Several of the VJ800 transistors are also pinned out individually for evaluation.

733 VIDEO AMPLIFIER: This circuit is a low-noise version of the industry-standard 733 video amplifier. Nominal voltage gains of 10, 100 or 300 are available depending upon connections to the gain select pins.

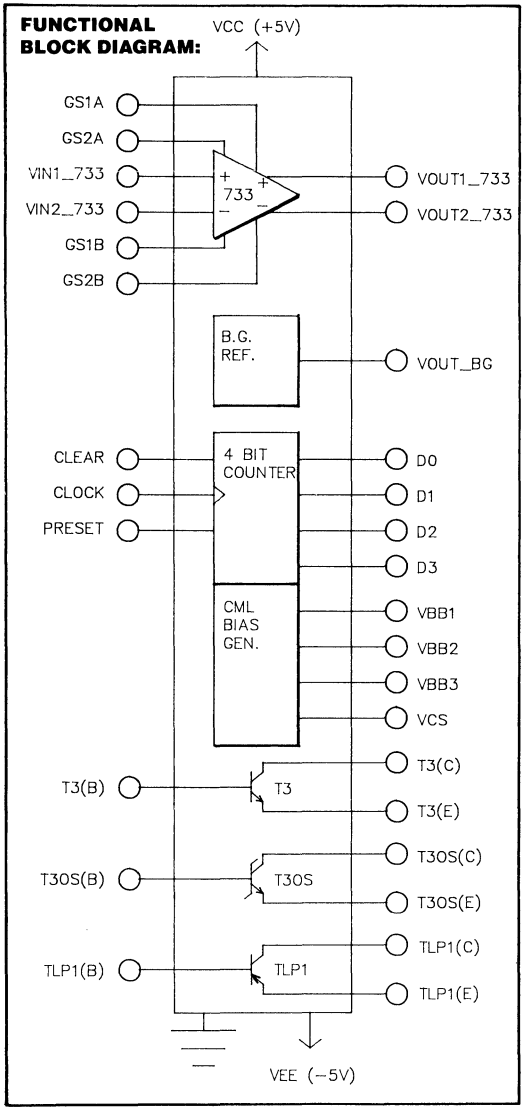
BANDGAP VOLTAGE REFERENCE: This circuit provides a temperature and power supply voltage compensated voltage reference of approximately 1.13 volts.

4-BIT COUNTER: The 4-bit counter is implemented with current mode logic (CML) internally. TTL input and output buffers are provided so that all I/O is TTL compatible.

CONNECTION DIAGRAM:



FUNCTIONAL BLOCK DIAGRAM:



TRUTH TABLE

CLEAR	PRESET	CLOCK	OUTPUT
1	0	x	All 0's
0	1	x	All 1's
0	0	/	Count Advances

/ = Rising Edge
x= Don't Care

TTL INPUT/OUTPUT ELECTRICAL CHARACTERISTICS:

Unless Otherwise Specified, V_{CC} = 5V, V_{EE} = −5V, Tj = 25°C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IH}		2			V
V_{IL}				0.8	V
V_{OH}	I_{OH} = −400μA	2.7	3.2		V
V_{OL}	I_{OL} = 4mA		0.18	0.4	V
	I_{OL} = 8mA		0.30	0.5	V
I_{IH}	V_{IH} = 2.7V		0	20	μA
I_{IL}	V_{IL} = 0.4V		−320	−400	μA

BANDGAP REFERENCE ELECTRICAL CHARACTERISTICS:

Unless Otherwise Specified, V_{CC} = 5V, V_{EE} = −5V, Tj = 25°C

PARAMETER	SYM	TYP	UNITS
Output Voltage (I_O = 0mA)	V_O	1.13	V
Output Voltage Temperature Coefficient (−0°C≤T≤100°C)	V_O/T	110	ppm/°C
Maximum Output Voltage Change (−0°C≤T≤100°C)	V_{OC}	23	mV
Line Regulation (4.5V≤V_{CC}≤5.5V, I_O = 0mA)	V_{REG}	10	mV
Output Resistance	R_O	100	Ohms
Maximum Output Current	I_{OMAX}	2	mA

CML BIAS GENERATOR:

The CML bias generator provides the CML current source reference voltage (VCS) and the CML reference voltages (VBB1, VBB2 and VBB3). See the CML logic Design Note for more information on CML logic.

Unless Otherwise Specified, V_{CC} = 5V, V_{EE} = −5V, Tj = 25°C

PARAMETER	SYM	TYP	UNITS
A Level CML Reference Voltage	VBB1	4.75	V
B Level CML Reference Voltage	VBB2	4	V
C Level CML Reference Voltage	VBB3	3.25	V
CML Current Source Reference Voltage	VCS	1.25	V

733 VIDEO AMPLIFIER ELECTRICAL CHARACTERISTICS:

Unless Otherwise Specified, V_{CC} = 5V, V_{EE} = −5V, Tj = 25°C

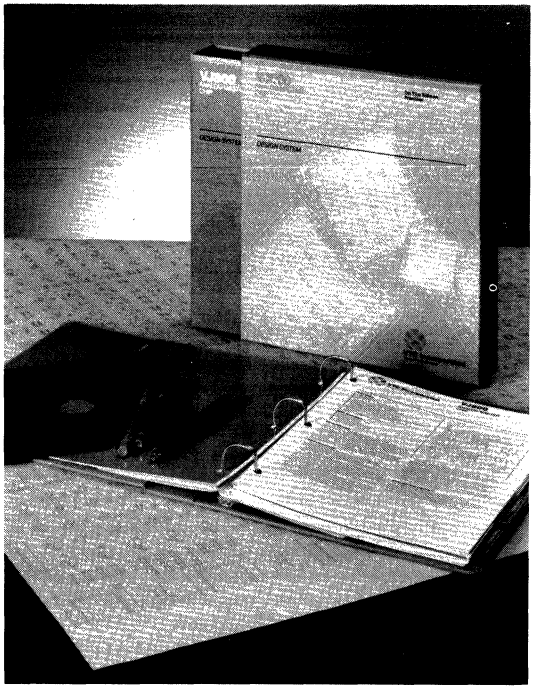
PARAMETER	SYM	TYP	UNITS
Differential Voltage Gain (R_S = 50 Ohms, R_L = 2K Ohms, V_O = 3Vpp	A_V		
Gain 1 (Note 1)		300	V/V
Gain 2 (Note 2)		100	V/V
Gain 3 (Note 3)		10	V/V
Bandwidth (R_S = 50 Ohms, C_L≤15pF)	BW		
Gain 1		40	MHz
Gain 2		90	MHz
Gain 3		130	MHz
Rise Time (R_S = 50 Ohms, V_O = 1Vpp)	t_R		
Gain 1		7	ns
Gain 2		5	ns
Gain 3		3	ns
Propagation Delay (R_S = 50 Ohms, V_O = 1Vpp)	t_{PD}		
Gain 1		6.5	ns
Gain 2		5	ns
Gain 3		3.5	ns
Input Resistance	R_{IN}		
Gain 1		1	K Ohms
Gain 2		10	K Ohms
Gain 3		200	K Ohms
Input Capacitance	C_{IN}		
Gain 1		12	pF
Gain 2		10	pF
Gain 3		4	pF
Input Offset Current	I_{IO}	6	μA
Input Bias Current	I_{IB}	40	μA
Input Noise Voltage (R_S = 50 Ohms, BW = 1KHz to 10MHz)	e_{IN}		
Gain 1		0.8	nV/√Hz
Gain 2		2	nV/√Hz
Gain 3		7	nV/√Hz
Input Voltage Range	V_{IR}	±1	V
Common-Mode Rejection Ratio	CMRR		
Gain 2 (V_{CM} = ±1V, f≤100KHz)		75	dB
Gain 2 (V_{CM} = ±1V, f≤5MHz)		55	dB
Output Common-Mode Voltage	V_{OCR}	2.5	V
Output Voltage Swing (R_L = 2K Ohms)	V_{OS}	3	Vpp
Output Sink Current	I_{SINK}	2	mA
Output Resistance	R_O	20	Ohms
Power Supply Rejection Ratio	PSRR	70	dB
Output Offset Voltage	V_{OS}		
Gain 1		0.6	V
Gain 2 and 3		0.35	V

Note 1: Pins GS1A and GS1B connected together.
Note 2: Pins GS2A and GS2B connected together.
Note 3: Gain Select pins open.

DESIGN SYSTEM
VJ800 ANALOG MASTER CHIP

FEATURES
- Data Sheet
- User's Guide
- Design Manual
- Design Notes
- Evaluation Chip Data Sheet (chip available on request)
- Database Software
- Mylar Plot with Marking Pens
- Technical Support

APPLICATIONS
- Disk Drive Subsystems
- Communications
- Analog Signal Processing
- Linear/Digital Subsystems
- Linear LSI Subsystems



DESCRIPTION

The VJ800 Analog Master Chip Design System contains the information necessary to design semicustom linear circuits on a workstation or computer.

The User's Guide provides the data needed to design with the master chip components and a description of the various components. It also supplies data for computer modeling of components using software routines such as SPICE.

In addition to the User's guide, a Design Manual is provided which covers general practices and usage for bipolar linear design, including material on parasitic elements, special practices at I/O ports, and reliability considerations.

Design Notes give helpful information on various design methods.

Testing requirements with associated forms, and packaging information are also a part of the design system.

In addition, the designer receives a symbolic mylar plot of the master chip with instructions on its use.

The database software is provided for a Mentor/Apollo workstation schematic entry and simulation, or simulation models from the User's Guide can be loaded into any computer running SPICE simulation.

VTC provides technical support for design system users whenever necessary.

VJ830
ANALOG MASTER CHIP
PRELIMINARY

FEATURES
- 188 Transistors
- 248 Resistors, 150 Ω to 15k Ω
- 8 On-chip Junction Capacitors
- Suitable for 5V or 12V Power Supplies
- NPN f_T of 800MHz Minimum
- Economical Chip Size: 83 x 79 Mils
- Two Layer Metal for Excellent Utilization and Routability
- Workstation/PC-based Schematic Entry and Simulation Available
- Accommodates up to 28 Pins

APPLICATIONS
- Peripherals
- Instrumentation
- Telecommunications
- Discrete Circuit Replacement
- Analog Signal Processing
- Linear Subsystems
- Linear LSI Subsystems

DESCRIPTION
The VJ830 Analog Master Chip is a versatile, high-performance, bipolar integrated circuit containing prediffused transistors, resistors and capacitors. The components interconnect to define analog functions. Diffused resistor values are user-programmable. Implanted resistors have fixed taps.

The chip is ideal for high-performance amplifiers with low noise inputs—for example, in disk or tape drives. The VJ830 component library is available on diskettes for schematic entry and SPICE simulation.

DESIGNING
Designing with the VJ830 is straightforward. The design system provides all information necessary to design on a workstation or computer and includes:
- VJ830 User's Guide
- Design Manual for the LHD Process
- VJ830 Component Library on Diskette with Instruction Manual
- Symbolic Mylar Plot for Layout

The VJ830 component library is used on a workstation for schematic entry and simulation. Simulation models from the User's Guide can be loaded into any computer running SPICE.

The VJ830 User's Guide and Design Manual give detailed information to aid the user in analog master chip design philosophy, circuit design and simulation and circuit layout. It also includes the forms necessary to transmit circuit test requirements.

TESTING
The VJ830 User's Guide specifies requirements for automatic circuit testing.

SUBMITTAL
When design is complete, the circuit components are interconnected on the mylar plot by the user (or for an optional charge this can be done by VTC).

The circuit schematic, test specification and mylar plot are then sent to VTC where the data is entered into a CAD system, masks and wafers fabricated and 15 prototypes packaged, tested and returned to the customer.

VJ830 COMPONENT LIST

QUANTITY	TYPE	COMPONENT	NAME	COMMENTS
64	NPN	Small Transistor, 0.5mA	T3	$f_T = 800$ MHz
56	NPN	Medium Transistor, 2mA	T12	$f_T = 800$ MHz
8	NPN	Low Noise Transistor, 10mA	TLN1	$f_T = 800$ MHz
4	NPN	Power Transistor, 60mA	T50	$f_T = 800$ MHz
8	NPN	Small Schottky, 5mA	T3S	$f_T = 800$ MHz
20	NPN	Medium Schottky, 8mA	T30S	$f_T = 800$ MHz
4	NPN	Power Schottky, 60mA	T50S	$f_T = 800$ MHz
24	PNP	Two Collector, 0.33mA	TLP1	$f_T = 80$ MHz
24	DIFFUSED	300 Ohm Resistor	A	Variable *(Note 1)*
56	DIFFUSED	600 Ohm Resistor	B	Variable *(Note 2)*
32	DIFFUSED	1200 Ohm Resistor	C	Variable *(Note 2)*
112	IMPLANT	3.2K Ohm Resistor	D	Tapped *(Note 3)*
24	IMPLANT	15K Ohm Resistor	E	Tapped *(Note 4)*
8	JUNCTION	Capacitor, 5pF	JCAP	

NOTES:
(1) Minimum single value is 130 Ohm.
(2) Minimum single value is 150 Ohm.
(3) Fixed tap values of 1.6K Ohm and 3.2K Ohm.
(4) Fixed Tap Values of 5K, 10K and 15K Ohm.

ELECTRICAL CHARACTERISTICS:

TRANSISTORS

NAME	TYPE	I_C (mA) (Note 1)	BETA			BVCBO (V)			BVEBO (V)			LVCEO (V)
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN
T3	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T12	NPN	2	50	100	200	25	30	35	5.6	5.85	6.2	7
TLN1	NPN	10	50	100	200	25	30	35	5.6	5.85	6.2	7
T50	NPN	60	50	100	200	25	30	35	5.6	5.85	6.2	7
T3S	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T30S	NPN	8	50	100	200	25	30	35	5.6	5.85	6.2	7
T50S	NPN	60	50	100	200	25	30	35	5.6	5.85	6.2	7
TLP1 (Note 2)	PNP	0.16	50	120	250	25	30	35	25	30	35	13.2

RESISTORS:

NAME	RESISTOR TYPE	LINEAR TEMPERATURE COEFFICIENT	QUADRATIC TEMPERATURE COEFFICIENT	CAPACITANCE PICOFARAD OV BIAS	TOLERANCE %	
					ABS.	MATCH (Note 3)
A	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.116	20	1
B	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.136	20	1
C	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.24	20	1
D	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.114	20	2
E	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.192	20	2

NOTES:
(1) Switching time and frequence response will be best at maximum I_C.
(2) Applies to each of the two collectors.
(3) Adjacent resistors in the same plane.

VJ831

EVALUATION CHIP
FOR THE VJ830
ANALOG MASTER CHIP
PRELIMINARY

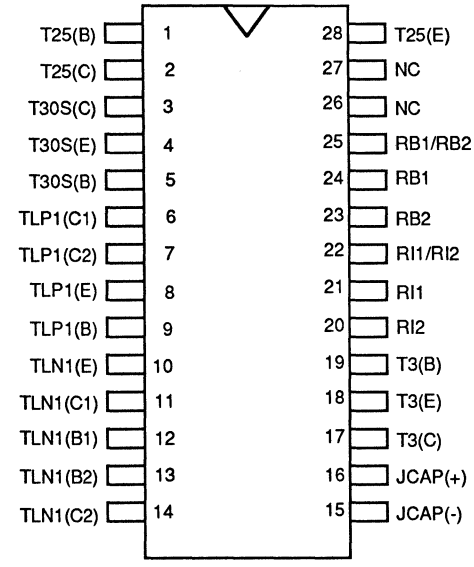
FEATURES

- 0.5mA NPN Transistor
- Lateral PNP Transistor
- Typ. Low-Noise NPN Transistor
- 60mA NPN Power Transistor
- 8mA Schottky NPN Transistor
- Two 1.2KOhm Base Resistors
- Two 15KOhm Implant Resistors
- 5pF Junction Capacitor

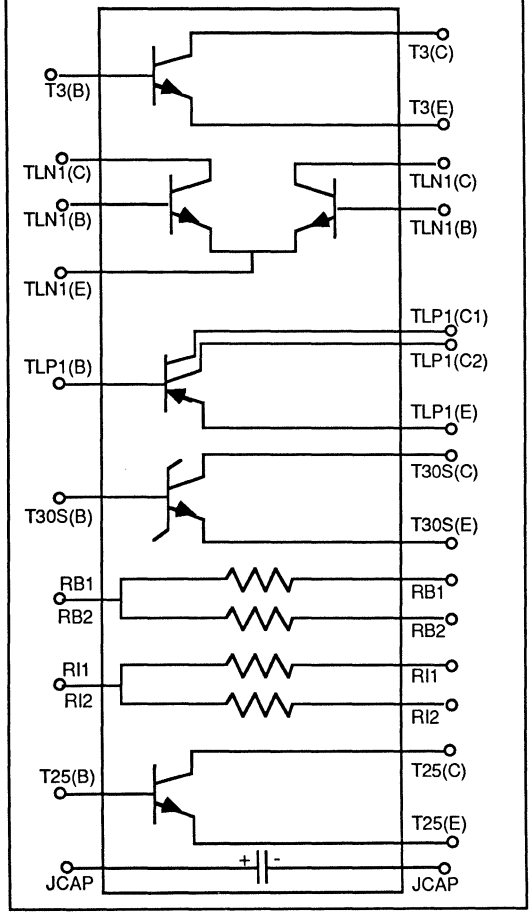
DESCRIPTION

The VJ831 Evaluation Chip contains a number of devices found on the VJ830 Analog Master Chip. All transistors and resistors are pinned out individually for evaluation. A list of transistor parametrics is included for the purpose of comparison. Several components are included in pairs to allow for evaluation of matching capabilities.

CONNECTION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PARAMETERS

Component	*Beta Typ.*	*BV_{CEO} Min.*	*BV_{CBO} Min.*	*Maximun Collector Current*	*f_T (MHz) Min.*
T3	84	7.0	25	0.5mA	800
TLN1	86	7.0	25	10.0mA	800
TLP1	55	13.2	25	0.32mA*	80
T30S	120	7.0	25	8mA	800
T25	65	7.0	25	60mA	800

**0.160 mA per collector*

VJ860
ANALOG MASTER CHIP
PRELIMINARY

FEATURES
- 408 Transistors
- 612 Resistors, 150 Ω to 15k Ω
- 18 On-chip Junction Capacitors
- Suitable for 5V or 12V Power Supplies
- NPN f_T of 800MHz Miniumum
- Economical Chip Size: Approx.110 x 106 Mils
- Two Layer Metal for Excellent Utilization and Routability
- Workstation/PC--Based Schematic Entry and Simulation Available
- Accommodates up to 40 Pins

APPLICATIONS
- Peripherals
- Instrumentation
- Telecommunications
- Discrete Circuit Replacement
- Analog Signal Processing
- Linear Subsystems
- Linear LSI Subsystems

DESCRIPTION
The VJ860 Analog Master Chip is a versatile, high-performance, bipolar integrated circuit containing prediffused transistors, resistors and capacitors. The components interconnect to define analog functions. Diffused resistor values are user-programmable. Implanted resistors have fixed taps.

The chip is ideal for high-performance amplifiers with low noise inputs—for example, in disk or tape drives. The VJ860 component library is available on diskettes for schematic entry and SPICE simulation.

DESIGNING
Designing with the VJ860 is straightforward. The design system provides all information necessary to design on a workstation or computer and includes:
- VJ860 User's Guide
- Design Manual for the LHD Process
- VJ860 Component Library on Diskette with Instruction Manual
- Symbolic Mylar Plot for Layout

The VJ860 component library is used on a workstation for schematic entry and simulation. Simulation models from the User's Guide can be loaded into any computer running SPICE simulation.

The VJ860 User's Guide and Design Manual provide detailed information to aid the user in analog master chip design philosophy, circuit design and simulation and circuit layout. It also includes the forms necessary for transmittal of circuit test requirements.

TESTING
The VJ860 User's Guide specifies requirements for automatic circuit testing.

SUBMITTAL
When design is complete, the circuit components are interconnected on the mylar plot by the user (or for an optional charge this can be done by VTC Incorporated). The circuit schematic, test specification and mylar plot are then sent to VTC where the data is entered into a CAD system, masks and wafers fabricated and 15 prototypes packaged, tested and returned to the customer.

VJ860 COMPONENT LIST:

QUANTITY	TYPE	COMPONENT	NAME	COMMENTS
144	NPN	Small Transistor, 0.5mA	T3	$f_T = 800$ MHz
126	NPN	Medium Transistor, 2mA	T12	$f_T = 800$ MHz
18	NPN	Low Noise Transistor, 10mA	TLN1	$f_T = 800$ MHz
8	NPN	Power Transistor, 60mA	T50	$f_T = 800$ MHz
18	NPN	Small Schottky, 5mA	T3S	$f_T = 800$ MHz
36	NPN	Medium Schottky, 8mA	T30S	$f_T = 800$ MHz
4	NPN	Power Schottky, 60mA	T50S	$f_T = 800$ MHz
54	PNP	Two Collector, 0.33mA	TLP1	$f_T = 80$ MHz
54	DIFFUSED	300 Ohm Resistor	A	Variable *(Note 1)*
126	DIFFUSED	600 Ohm Resistor	B	Variable *(Note 2)*
72	DIFFUSED	1200 Ohm Resistor	C	Variable *(Note 2)*
252	IMPLANT	3.2K Ohm Resistor	D	Tapped *(Note 3)*
54	IMPLANT	15K Ohm Resistor	E	Tapped *(Note 4)*
18	JUNCTION	Capacitor, 5pF	JCAP	

NOTES:
(1) Minimum single value is 130 Ohm.
(2) Minimum single value is 150 Ohm.
(3) Fixed tap values of 1.6K Ohm and 3.2K Ohm.
(4) Fixed Tap Values of 5K, 10K and 15K Ohm.

ELECTRICAL CHARACTERISTICS:

TRANSISTORS

NAME	TYPE	I_C (mA) (Note 1)	BETA			BVCBO (V)			BVEBO (V)			LVCEO (V)
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN
T3	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T12	NPN	2	50	100	200	25	30	35	5.6	5.85	6.2	7
TLN1	NPN	10	50	100	200	25	30	35	5.6	5.85	6.2	7
T50	NPN	60	50	100	200	25	30	35	5.6	5.85	6.2	7
T3S	NPN	0.5	50	100	200	25	30	35	5.6	5.85	6.2	7
T30S	NPN	8	50	100	200	25	30	35	5.6	5.85	6.2	7
T50S	NPN	60	50	100	200	25	30	35	5.6	5.85	6.2	7
TLP1 (Note 2)	PNP	0.16	50	120	250	25	30	35	25	30	35	13.2

RESISTORS:

NAME	RESISTOR TYPE	LINEAR TEMPERATURE COEFFICIENT	QUADRATIC TEMPERATURE COEFFICIENT	CAPACITANCE PICOFARAD OV BIAS	TOLERANCE %	
					ABS.	MATCH (Note 3)
A	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.116	20	1
B	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.136	20	1
C	DIFFUSED	3.0×10^{-4}	5.8×10^{-6}	0.24	20	1
D	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.114	20	2
E	IMPLANT	29.2×10^{-4}	6.9×10^{-6}	0.192	20	2

NOTES:
(1) Switching time and frequence response will be best at maximum I_C.
(2) Applies to each of the two collectors.
(3) Adjacent resistors in the same plane.

VJ861

EVALUATION CHIP
FOR THE VJ860
ANALOG MASTER CHIP
PRELIMINARY

FEATURES

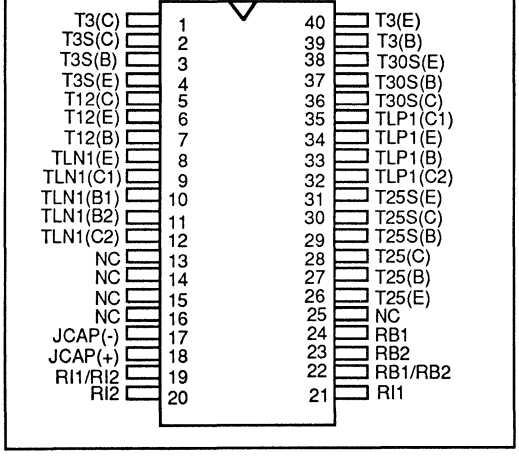
- 0.5mA NPN Transistor
- 0.5mA Schottky NPN Transistor
- Lateral PNP Split-Collector Transistor
- Low-Noise NPN Matched-Pair Transistors
- 60mA NPN Power Transistor
- 60mA Schottky NPN Transistor
- 2mA NPN Transistor
- 8mA Schottky NPN Transistor
- Two 1.2KOhm Base Resistors
- Two 15KOhm Implant Resistors
- 5pF Junction Capacitor

TRANSISTOR PARAMETERS

Component	*Beta Typ.*	*BV_{CEO} Min.*	*BV_{CBO} Min.*	*Maximun Collector Current*	*f_T (MHz) Min.*
T3	84	7.0	25	0.5mA	800
TLN1	86	7.0	25	10.0mA	800
TLP1	55	13.2	25	0.32mA*	80
T30S	120	7.0	25	8mA	800
T25	65	7.0	25	60mA	800
T25S	65	7.0	25	60mA	800
T3S	84	7.0	25	0.5mA	800
T12	101	7.0	25	2mA	800

**0.160mA per collector*

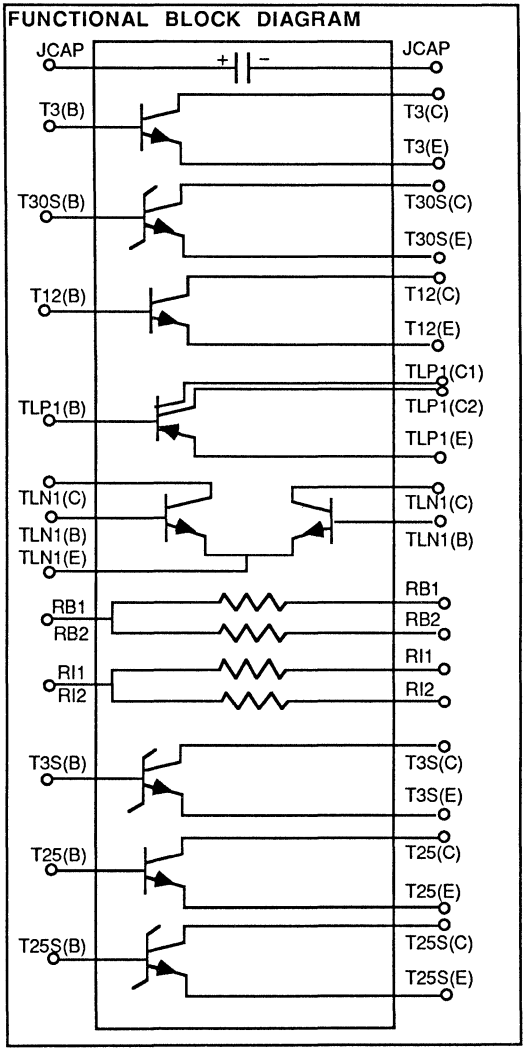
CONNECTION DIAGRAM



DESCRIPTION

The VJ861 Evaluation Chip contains a number of devices found on the VJ860 Analog Master Chip. All transistors and resistors are pinned out individually for evaluation. A list of transistor parametrics is included for the purpose of comparison. Several components are included in pairs to allow for evaluation of macthing capabilities.

FUNCTIONAL BLOCK DIAGRAM



NOTES

VJ800 FAMILY
ANALOG MASTER CHIP USER'S GUIDE

VJ800 USER'S GUIDE CONTENTS

TABLES

FIGURES

INTRODUCTION

The VJ800 Analog Master Chip contains a set of unconnected, integrated components on a monolithic chip. Development of the chip for a particular application requires the user to create the necessary circuitry, which is then implemented through unique interconnection masks. This User's Guide contains data needed to design with the master chip components, a description of various components, and data for computer modeling of components using software routines such as SPICE.

In addition to this User's Guide, VTC provides a Design Manual which covers general practices and usage for bipolar linear design, including material on parasitic elements, special practices at I/O ports, and reliability considerations.

GETTING STARTED

The first step in designing a master chip is to create the required circuitry. Circuit diagrams are drawn similar to those used with discrete designs. Although a breadboard is not built, the circuit is simulated using a computer simulation program which solves the equations for a mathematical model of the circuit.

To begin designing a master chip, the following items are needed:

1. The VJ800 Design System, which includes:
   - •The VJ800 User's Guide
   - •A Design Manual
   - •Mylar Layout Sheet
   - •Design Notes (helpful for some aspects of circuit design)
   - •Diskette for Mentor Graphics™ Workstation
   - •VJ800 Mentor Graphics Instructions

2. Access to a computer system which runs ASPEC or SPICE simulation programs. (If a Mentor Graphics workstation is available, the Mentor Graphics Instructions and diskette that come with the VJ800 Design System contain the computer models which save data entry time.)

3. A textbook on analog integrated circuit design: *Analysis and Design of Analog Integrated Circuits (2nd Ed.)*, by P. Gray and R. Meyer (J. Wiley & Sons, 1984).

THE VJ800 COMPONENT SET

Table 1 describes the VJ800 component set. The first column gives the total number of a given kind of component available on the chip. The second column gives the component name, which is also used on the mylar chip plot and is the name of the SPICE model for the component.

Table 1: The VJ800 Component Set

Number on chip	Comp. Name	Comments and Description
310	T3	Minimum-sized NPN Transistor Maximum Ic = .5mA
168	T12	Medium-sized NPN Transistor Maximum Ic = 2.0mA
26	TLN1	Low-noise NPN Transistor Maximum Ic = 10.0mA
5	T50	Power NPN Maximum Ic = 180mA
32	T3S	Minimum-sized Schottky NPN Maximun Ic = .5mA Overlap-type Schottky
54	T30S	Large Schottky NPN Maximum Ic = 8mA Guard-ring Schottky Diode
5	T50S	Power Schottky NPN Maximum Ic = 180mA Guard-ring Schottky Diode
36	TLP1	Two-collector lateral PNP Maximim Ic = .16mA/collector
74	A	Base Resistor -- Adjustable for 159-300 ohms nominal resistance
153	B	Base Resistor -- Adjustable for 188-600 ohms nominal resistance
112	C	Base Resistor -- Adjustable for 181-1200 ohms nominal resistance
293	D	Implanted Resistor -- Center-tapped for two 1.6k ohm segments
74	E	Implanted Resistor -- Tapped in two places for three 5k ohm segments
18	JCAP	Junction Capacitor, Type C Nominal capacitance 5pF at V=O

Design With Layout in Mind: When choosing components for the design of a circuit subsection, the designer should look at the layout plot and choose components that are relatively close together. As the

circuit design proceeds, a layout plan should evolve. The designer should plan the position of each circuit subsection, along with power bussing and chip pinout.

Power Dissipation: If all the transistors in the VJ800 are used with each carrying its maximum collector current, the total chip current would be 2800mA. When the average collector voltage is 5V, the dissipated power is 14W, and ordinary packages cannot dissipate this much heat. Therefore, it is important for the designer to keep track of the total power dissipation of the chip and keep it in line with the thermal properties of the intended package.

As a rough guide, small ceramic DIP (14 and 16 pins) can safely dissipate about .5W; larger DIP (24 and 28 pins) up to 1W; and 40-pin ceramic DIPs up to 1.5W. The guide for other packages is that junction temperature should be kept below 125°C.

The designer should consider how much current to use in each subcircuit. It is not necessary to operate transistors at maximum Ic. Small currents may be fast enough for many parts of the circuit. A typical on-chip parasitic node capacitance is about .5pF, and 100 microamperes is enough to slew the voltage at the node at 200mV/nsec. This is sufficient for many applications.

Component Utilization: It is not possible to use 100% of the VJ800 components because of interconnection constraints. Many first metal interconnection lines must cross over component locations, which is accomplished by eliminating the connections to silicon at these locations. A designer should plan for a 60% maximum utilization of available components.

BIPOLAR TRANSISTOR MODELING

The SPICE models for the VJ800 bipolar transistors are given in Tables 10, 10.1 , 10.2 and 10.3 for nominal beta, worst-case low beta, worst-case high beta and worse-case fast, respectively. The model used is the Gummel-Poon type. More data on transistor usage is given in parts II and III of the Design Manual, and it is recommended the designer read this material before beginning a design. Graphs of typical I-V characteristics for a minimum NPN at various temperatures are given in part II of the Design Manual.

The nominal beta, worst-case low beta and worst-case high beta transistor models given are considered worst-case SLOW models. Their performance will not be worse than predicted by SPICE as long as the parasitics of resistors, interconnections, etc., are properly taken into account. These models are convenient for most cases, but are not suitable for stability analyses (for example, feedback loops) where worst-case FAST models are desired. The worst-case FAST (Table 10.3) models are derived from the worst-case SLOW ones by changes to the SPICE model parameters as given in Table 2.

Table 2: Changes to Find Worst-Case FAST SPICE Parameters

SPICE Parameter(s)	Multiply by
IKF	1.20
CJE, CJC, RB	.80
RC, RE	.75
CJS	.85
TF (for NPNs)	.85
(for PNPs)	.60

The remaining SPICE parameters have no influence on the circuit speed and are left unchanged.

Breakdown Voltages and Beta: The junction breakdown voltages of the transistors are not part of the SPICE model. The designer must account for these and ensure that voltages occurring in the circuit do not exceed the breakdown voltages (Table 3).

Table 3: Breakdown Voltages and Beta for VJ800

NPN Parameter	Min.	Typ.	Max.
BVcbo (base-coll.)	25	30	35
BVebo (base emit.)	5.8	6.0	6.2
BVceo (coll.-emit.)	7.0	---	---
Beta	50	100	200
PNP Parameter	**Min.**	**Typ.**	**Max.**
BVcbo (base-coll.)	25	30	35
BVebo (base emit.)	25	30	35
BVceo (coll.-emit.)	13.2	---	---
Beta (TLP1) at Ic = .05mA	50	80	180
Beta (TLP1) at Ic = .33mA	20	30	---

Maximum Collector Current: Each transistor has a maximum collector current as shown in Table 1. This current is at the approximate boundary between high-level and low-level injection, and the device performance usually deteriorates above this current.

The SPICE models are also less accurate above the stated maximum collector current, and all data on modeling, matching, temperature coefficient, etc., is of unknown accuracy above the maximum Ic.

Temperature Dependences: The temperature dependences of the transistor currents and voltages are contained in the SPICE models and do not need to be considered explicitly. The most significant transistor temperature dependence is the drop of Vbe (ON) by about 1.8mV per degree centigrade.

Transistor Matching: Many kinds of circuits (such as differential amplifiers) require close matching between the properties of paired transistors. Table 4 gives data on the matching properties of LHD-process transistors. This data is valid for transistors with identical geometries (i.e., the same component name) that are located immediately adjacent to each other on the chip. The matching properties are expressed in terms of the standard deviation defined in the statistical sense and are based on detailed measurements of LHD transistors. For the table entries where the unit is percent, the standard deviation is found by taking the percentage of the typical or nominal value.

Table 4: Typical Transistor Matching Properties

Parameter	Std. Dev.	Unit
Input Offset -- T3 or T3S	1.4	mV
Input Offset -- T12 NPN	1.0	mV
Input Offset -- TLN1 NPN	.30	mV
Input Offset -- T50 or T50S	.5	mV
Input Offset -- T30S NPN	.8	mV
Input Offset -- TLP1 PNP	.3	mV
Beta -- All NPNs and PNPs	1.5	%
Collector Current Diff. for 2-Coll. Lateral PNP (TLP1)	1.0	%

The matching data given in Table 4 is typical of situations in which the temperature and stress gradients in the chip are negligible. Temperature gradients depend on the chip layout and placement of circuit elements which dissipate large amounts of heat. These factors are dealt with in part VII of the Design Manual.

Frequency Response: The frequency response is contained in the SPICE models. NPN transistors have unity-gain frequencies (e.g., for a common-base or common-collector stage) of about 1GHz (800MHz guaranteed minimum). The unity-gain frequencies of the PNPs are about 100MHz (80MHz guaranteed minimum). SPICE simulations should give accurate predictions of frequency response for a given circuit, along with its dependence on temperature, supply voltage, etc.

Parasitic Transistors and Diodes: Standard bipolar processes contain numerous parasitic elements which are described in part VII of the Design Manual. Parasitic elements will not be a problem if the following rules are followed. Transistor saturation is a forbidden practice for non-Schottky transistors, as well as for the operation of transistors in the inverted mode. Numerous resistor tub and substrate contacts should be placed in the layout as described in the layout instructions.

Labeling and Modeling Conventions for Transistors: The labeling conventions for the NPN and PNP transistors are shown in Figures 7 and 8. The labeling of a transistor in a schematic diagram should be Qxxx (e.g., Q11, Q23). The lateral PNP has two collectors (see Figure 8), and is modeled by using two transistors. Alternatively, if both collectors are connected to the same node, only a single transistor with the area factor 1.0 can be used instead of the .5 shown in Figure 8. Part III of the Design Manual contains details of PNP transistor modeling.

The PNP transistor model (Figure 8) also requires an extra parasitic diode which uses the SPICE model DRN as given in Table 10.

Schottky Transistor Models: Because of the extra elements in a Schottky transistor, its model is more complicated. A modeling scheme for available Schottky transistors and a set of SPICE statements for the model using four elements and five nodes are shown in Figures 9,10 and 11. The Schottky diode is modeled by means of the SPICE model SCH1 as given in Table 10. This model corresponds to a Schottky diode with an area of one square micron.

INTEGRATED RESISTORS

Integrated resistors differ from discrete resistors in that:1) they have an important parasitic capacitance to the silicon body in which they are embedded; 2) they have a substantial temperature coefficient; and 3) they have a diode isolating them from other regions of the chip, which must be biased to keep it OFF. Details on resistors can be found in part V of the Design Manual.

Temperature Coefficients: This process has two types of resistors, base and implant. These differ in doping levels, and temperature coefficients. The base

resistor has the lower temperature coefficient, but is of very limited use for resistor values over 1k ohm. The implant type achieves higher values (to 15k ohm), but at the expense of a higher temperature coefficient. SPICE uses two temperature coefficients (linear and quadratic). The values for these are given in Table 5.

Table 5: Temperature Coefficients for LHD Resistors

Resistor Type	Linear TC	Quadr. TC
Base (A, B, C)	.00030	5.8E-6
Implant (D, E)	.00292	6.9E-6

The Design Manual contains a graph of the temperature dependences of the base and implant resistor types. It shows that base resistors pass through a minimum somewhat below room temperature, and begin to rise in value for lower temperatures. For the purpose of rough hand calculations, base resistors increase at 0.07%/°C and implant resistors increase at 0.34%/°C for junction temperatures of 50 to 75°C.

Resistor Adjustment: The base-type resistors (A, B, C) are adjustable in value. The adjustment is made by moving a contact point to silicon, thus varying the effective length of the resistor. The available resistor values are given in Table 12.

Resistor Parasitic Capacitance: Figure 1 shows how a typical base resistor (Type A) is modeled. A diode representing about half the capacitance is loaded on each end of the resistor. (Note that if either end goes to a DC voltage the load diode at that end can be omitted.) The cathodes of the load diodes are connected to the V_{CC} supply voltage (the most positive supply voltage is denoted as node nV_{CC}, as detailed in part V of the Design Manual). The area factors, c1(0) and c2(0), differ with placement of the contact opening (which is varied to adjust the resistor value) and can be found in Table 12.

The implant resistors are modeled similarly, with modifications needed to account for intermediate taps. These models are shown in Figures 4 and 5. Both resistor types need a SPICE model for the junction which surrounds the resistor body, and is provided by a diode model, DRP. The SPICE model for DRP is given in Table 10.

Resistor Matching and Tolerances: The ability to match resistors to close tolerances is one of the more favorable features of monolithic IC design. The absolute tolerances, however, are less favorable. The absolute worst-case tolerance for resistor value at a given temperature is ±20% of the nominal value for both base and implant resistors. There is no correlation in the fluctuations of the base and implant resistors. If the base resistor happens to be 12% low on a given lot, the implant resistors may be 15% high. Therefore, base resistors should not be ratioed against implant resistors. Resistor ratioing rules are covered in more detail in Section 35 of the Design Manual.

The resistor matching parameters are given in Table 6. The standard deviation is observed if the values of a large number of identically sized and identically oriented resistors are placed in close proximity on the chip, and the resulting distribution is fitted to the normal distribution. It is defined as a percentage of resistor nominal value. The resistor ratio standard deviations are somewhat worse than this, because the percentage standard deviation of a ratio is larger than those of either parameter entering the ratio.

Table 6: Typical Resistor Matching

Resistor Type	Std. Deviation (%)
Base (A, B, C)	.18
Implant (D, E)	.40

The resistors are affected, just as transistors, by temperature gradients (through temperature coefficient and stress effects). Details on this are in Sections 56 and 57 of the Design Manual. These are not taken into account in Table 6 since they depend on the user-generated layout.

DIODES AND JUNCTION CAPACITORS

This subject is covered in part IV of the Design Manual.

Diode-Connected Transistors: This form of diode, the most common type in bipolar IC design, is created by connecting the base and collector of an NPN transistor. Figure 12 shows how these diodes are modeled in SPICE.

Schottky Diodes: The VJ800 does not provide Schottky diodes other than those contained in the transistor cells. Figures 13 and 14 show how Schottky diodes are created from transistor cells by wiring collector and emitter together. The details of Schottky diodes are covered in Sections 26 and 27 of the Design Manual. Schottky diodes cannot carry arbitrarily large

currents--the upper limit is 10μA per square micron of area.

The area of the Schottky diode in square microns is just the SPICE area parameter in the diode statement given in Figures 9, 10 and 11. The T30S transistor type, for example, is 362.8 square microns.

Junction Capacitors: The VJ800 does not contain dielectric capacitors. It is, however, possible to use nonlinear junction capacitors to stabilize (compensate) feedback loops, etc., and the VJ800 provides some special structures for this purpose. Figure 6 shows how this component is labeled and modeled in SPICE. The diode used for the junction capacitor has a parasitic capacitance to the substrate and is represented by an additional parasitic diode from the cathode of the junction capacitor to the V_{EE} node (nV_{EE}). The model for the parasitic capacitor DRN and the model JCPC needed for the capacitor junction are both given in Table 10.

Zener Diodes: A Zener diode is created by operating a diode-connected NPN transistor with the E-B junction in reverse avalanche breakdown. This results in a constant voltage of about 6V and is used in DC reference voltage sources and level shifters. The Zener voltage is the same as the NPN transistor parameter BVebo. Its values and limits are in Table 3.

The SPICE modeling for Zener diodes differs depending on whether a DC or AC model is desired.

The DC SPICE model is shown in Figure 16. This model contains a current source, I_A, which forces a current through a fictitious resistor, R_Z, with a temperature coefficient set to represent the observed temperature dependence of the Zener voltage. The voltage dropped across R_Z is duplicated in the voltage-controlled voltage source E_Z which then has the right temperature coefficient to represent the Zener voltage. The resistor R_S represents the effective output impedance of the Zener diode. To obtain the worst-case minimum and maximum DC Zener diode models, the Zener voltage/temperature coefficient should be changed from 6.0V/3.5E-4 to 5.8V/3.0E-4 and 6.2V/4.0E-4 respectively.

The AC SPICE model is created by using the SPICE diode model and setting the reverse breakdown parameter to appropriately represent the Zener voltage. This model does not contain any temperature dependence for the Zener voltage. Therefore, if the temperature dependence is important, the breakdown voltage parameter must be re-entered for each simulation temperature. The AC Zener model requires special SPICE models, ZT3, ZT12, etc. given in Table 10, for the nominal case. Worst-case minimum and maximum AC Zener models are given in Table 10.1 and 10.2.

Zener diodes have a type of noise arising from microplasmas, which is not modeled by SPICE, and may be a hazard in some applications. Details on Zener diodes are given in Sections 32 and 33 of the Design Manual.

Zener Matching: In some cases (for example, differential level shifters) the matching of Zener voltage between transistors is important. The standard deviation of the difference in Zener voltages for two identical Zener-connected NPNs (with identical currents) is about 5mV, provided the current levels in Table 7 are maintained.

Table 7: Current Limits for Matched Zener Diodes

NPN Types	Imin	Imax	Unit
T3	.1	.5	mA
T12	.25	1.25	mA
TLN1	1.1	5.6	mA
T50	10	50	mA

RESISTANCE AND CAPACITANCE OF THE INTERCONNECTIONS

The resistance and capacitance of interconnections (the lines in the schematic) are often neglected in discrete-component designs. In integrated circuit design, this is not always possible because the interconnections are less than ideal. Data on the properties of interconnections, which relate to simulation and layout, are given in this section and in part VI of the Design Manual.

A unique feature of integrated circuit design is the presence of electromigration--a wear-out mechanism for the interconnections. To prevent failure from this, the currents in interconnection lines must be limited to the values given in Table 8. The widths of the lines are given in terms of the number of standard-width grid lines they occupy on the layout. Ordinarily the only place where wider-than-minimum lines are used is in power transistors , output drivers and power-supply lines.

Table 8: Maximum Currents in Interconnections

Type of Connection	Max I (mA)
Minimum-width First Metal Line	3.5
Double-width First Metal Line	12.5
Triple-width First Metal Line	21.5
Minimum-width Second Metal Line	10.0
Double-width Second Metal Line	40.0
Triple-width Second Metal Line	70.0
Minimum-size Via	3.0

The capacitance and resistance of the interconnection lines shown in Table 9 are important. The resistance of aluminum interconnections has a substantial temperature coefficient of .44%/°C.

To determine the length of an interconnection line, it should be measured with a metric ruler on the mylar layout plot. The true length is obtained by dividing by the scale factor shown on the plot. A measurement in millimeters on the plot, divided by the scale factor, yields millimeters on the chip, which is the appropriate unit for use with Table 9.

The lengths of the interconnections depend on the placement of the components and should be taken into account in circuit simulations. For instance, a circuit that uses a JCAP and a lateral PNP transistor will have a long line connecting them, because the nearest components are quite distant on the chip. Thus, layout considerations should be made during simulation in order to avoid using components that are far apart physically in a given subcircuit, or to include their parasitic R and C in the simulation.

Table 9: Typical Resistance and Capacitance of Interconnection Lines per 1000 Microns Length (1000 Microns = 1 Millimeter)

Type of Connection	Line Width[1]	Resist. (ohm)	Capac[2] (pF)	Capac[3] (pF)
First Metal	1	18.8	0.51	1.02
	2	6.03	1.32	2.79
	3	3.57	2.13	4.60
	4	2.54	3.94	6.41
	5	1.97	5.75	8.22
	6	1.61	7.56	10.03
	7	1.36	9.37	11.84
	8	1.18	11.18	13.65
Second Metal	1	5.03	.29	.51
	2	1.14	.84	1.72
	3	.64	1.38	2.92
	4	.45	1.92	4.12
	5	.35	2.46	5.32
	6	.28	3.00	6.52
Min. Size Via	—	1.0	—	—

(1) Line width refers to the number of first or second metal routing channels used.
(2) Capacitance for first or second metal over field oxide.
(3) For first metal—Capacitance of first metal over field oxide and under wide second metal. For second metal—Capacitance over wide first metal.

SUBSTRATE CONTACTS AND V_{CC} CONNECTIONS

Some circumstances lead to current flow in the substrate or resistor tubs (Design Manual, part VII). The IR drops arising from these currents can cause thyristor latchup or other malfunctions. The user must specify where the substrate connections (to V_{EE}) and V_{CC} connections to resistor tubs are to be placed on the layout.

A SPICE EXAMPLE

Figure 18 illustrates the use of SPICE in simulating a circuit created with the VJ800 Analog Master Chip. Table 11 gives a detailed listing of the SPICE input statements.

LOGIC IMPLEMENTATION

It is often necessary to create a limited amount of logic circuitry in addition to analog circuits. The VJ800 has special features which make this easier, because the middle of the chip is laid out for convenient implementation of current mode logic.

VTC Design Note DN-4 describes current-mode logic, gives examples of basic logic circuits, and should be consulted when in doubt.

WORST-CASE SPICE SIMULATIONS

The initial SPICE simulations are usually done under nominal conditions--nominal supply voltages, room temperature, etc. This is a good way to define the circuit and show that desired circuit functions are realized. There are, however, significant variations in a realistic environment to which the chip is exposed--supply voltage, temperature, etc. These variations are serious enough that nominal designs fail to work correctly at the limits of supply voltage and temperature. A set of simulation conditions are outlined below, and should be used to verify satisfactory operation.

1. Temperature

The SPICE models contain the temperature dependence of the transistor currents and voltages, and give a realistic account of temperature variation. Some of the more significant temperature effects are: a) the transistor Vbe drops at about 1.7-1.9mV/° C; b) the resistors increase in value as temperature rises; and c) beta increases with temperature.

The temperature in SPICE simulation is the junction temperature--the actual temperature of the chip. To find the temperature it is necessary to know the type of package to be used, the thermal conductance of the package for the type of cooling used and the chip power dissipation. For most commercial applications, an assumption of 0° C and 125° C for temperature extremes is reasonable.

2. Supply Voltage

Ordinarily, the supply voltages are specified as ±10%. Thus a 5V chip should be simulated at 4.5V and 5.5V. If there are two supply voltages, for example +5V and +12V, then simulation should be done with all four combinations: (4.5, 13.2), (4.5, 10.8), (5.5, 13.2) and (5.5, 10.8).

Difficulties are usually encountered at worst-case low voltage and low temperature where Vbe is high, the supply voltage is low and beta is low. The most common source of difficulty is inadequate collector-base bias for some transistors, resulting in saturation and erroneous operation.

3. Beta

Beta is difficult to accurately control in manufacturing, and often affects important chip parameters. Thus, simulations should be done for the worst-case beta limits given in this User's Guide, and proper operation verified for the entire range of beta. Minimum and maximum beta transistor models are provided in Tables 10.1 and 10.2.

4. Zener Voltage

The tolerance for the Zener diode voltage and temperature coefficient is given in the Zener diode section of this User's Guide for the DC model. Worst-case minimum and maximum AC Zener diode models are given in Table 10.1 and 10.2.

5. Resistor Values

As noted above, the resistors are two types, base and implant, and they vary independently. The tolerances are ±20%, therefore, the following cases should be simulated:

- All base resistors at 1.2x their nominal values
  All implant resistors at 1.2x their nominal values
- All base resistors at 0.8x their nominal values
  All implant resistors at 1.2x their nominal values
- All base resistors at 1.2x their nominal values
  All implant resistors at 0.8x their nominal values
- All base resistors at 0.8x their nominal values
  All implant resistors at 0.8x their nominal values

6. Component Matching

Some circuits are sensitive to transistor and resistor matching and should be simulated for worst-case (or statistical) matching as described previously in this User's Guide.

7. Worst-Case Fast

If a circuit uses a feedback loop it should be simulated for stability using the worst-case fast models given in Table 10.3.

THE LAYOUT PLOT

The VJ800 Design System contains a symbolic mylar plot of the chip drawn to scale, which represents the various transistors and resistors in symbolic fashion. Thus, a transistor is shown by the usual schematic symbol.

A description of the various symbols on the layout plot is included in the VJ800 Design System, as well as detailed instructions on coding the plot and preparing for layout.

COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

BASE RESISTORS

Figure 1: A: 159–300 ohms

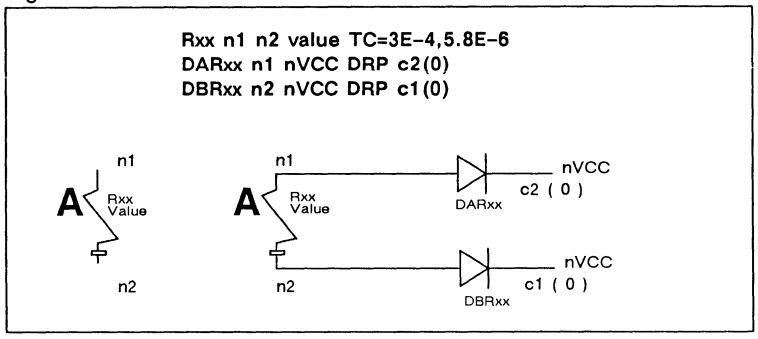


Figure 2: B: 188–600 ohms

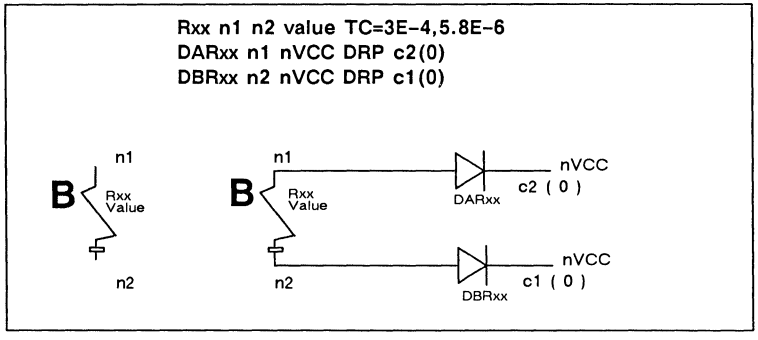
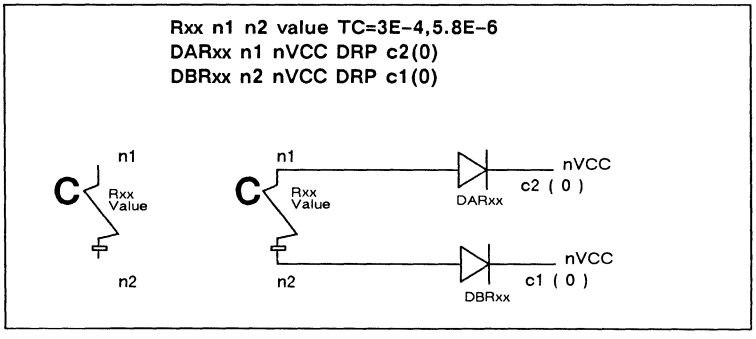


Figure 3: C: 181–1200 ohms



COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

IMPLANT RESISTORS

Figure 4: D: Two 1.6k ohm segments

```
Rxx n1 n2 1.6K TC=.00292,6.9E-6
Ryy n2 n3 1.6K TC=.00292,6.9E-6
DARxx n1 nVCC DRP  .03
DRxy n2 nVCC DRP  .06
DARyy n3 nVCC DRP  .03
```

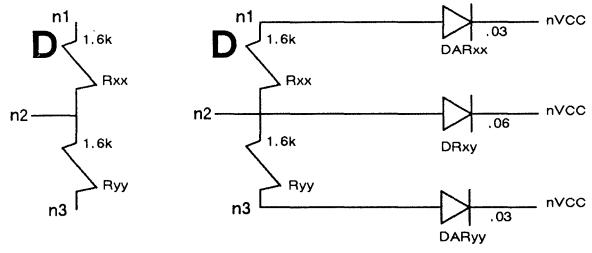
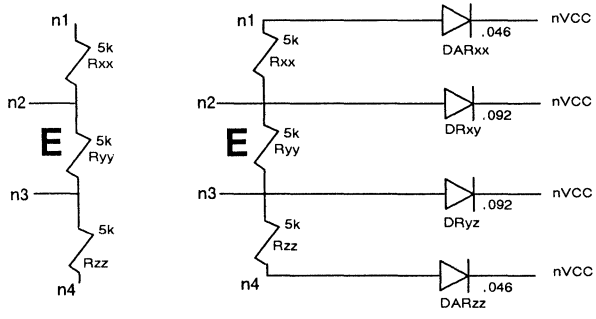


Figure 5: E: Three 5k ohm segments

```
Rxx n1 n2 5K TC=.00292,6.9E-6
Ryy n2 n3 5K TC=.00292,6.9E-6
Rzz n3 n4 5K TC=.00292,6.9E-6
DARxx n1 nVCC DRP .046
DRxy n2 nVCC DRP  .092
DRyz n3 nVCC DRP  .092
DARzz n4 nVCC DRP .046
```

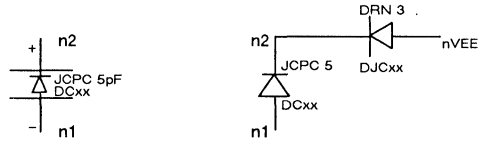


COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

CAPACITORS

Figure 6: JCAP

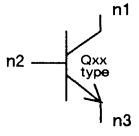
DCxx n1 n2 JCPC 5
DJCxx nVEE n2 DRN 3



NPN TRANSISTORS

Figure 7: T3, T12, TLN1, T50

Qxx n1 n2 n3 type

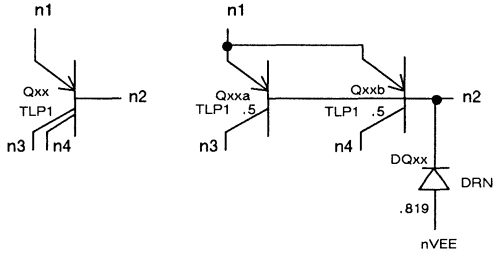


type = T3, T12, TLN1, OR T50

LATERAL PNP TRANSISTOR

Figure 8: TLP1 (two collector)

Qxxa n3 n2 n1 TLP1 .5
Qxxb n4 n2 n1 TLP1 .5
DQxx nVEE n2 DRN .819



COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

SCHOTTKY NPN TRANSISTORS

Figure 9: T3S

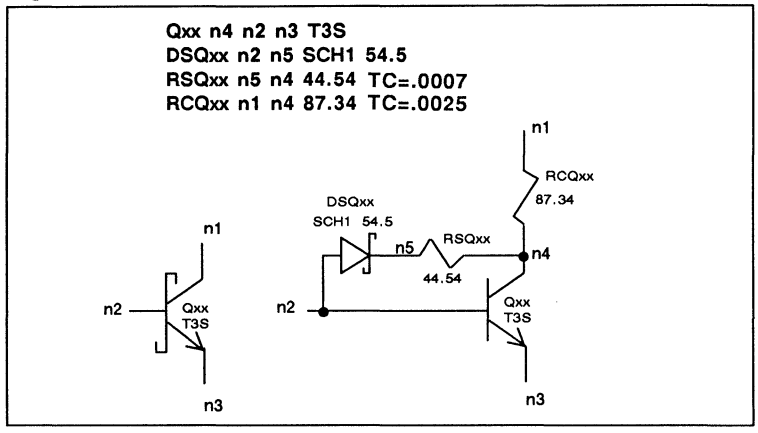


Figure 10: T30S

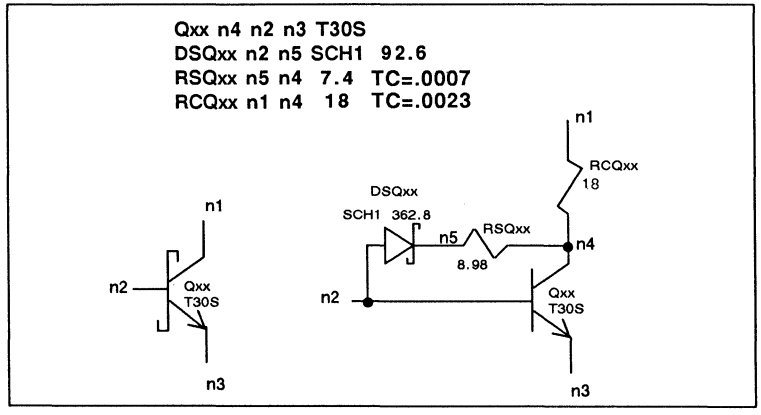
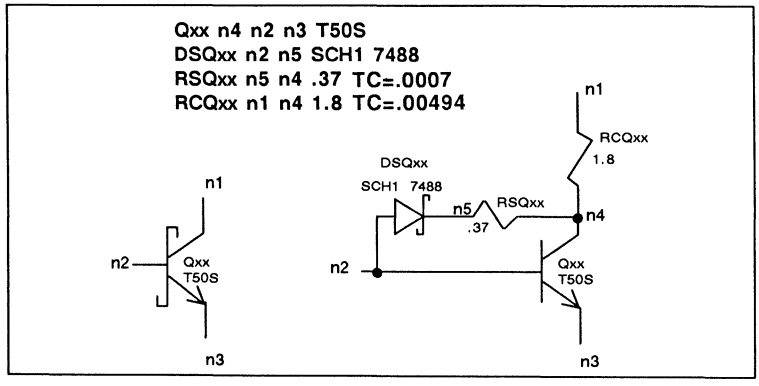


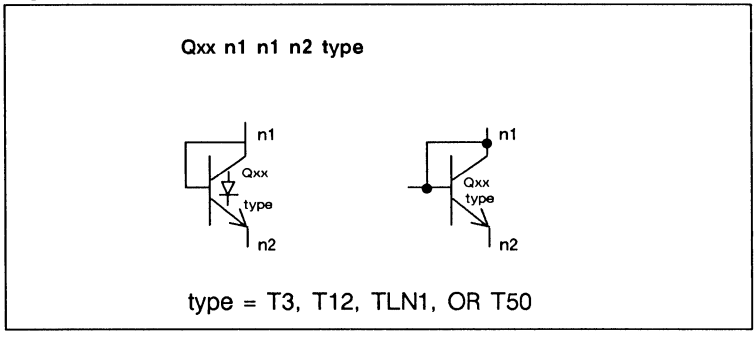
Figure 11: T50S



COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

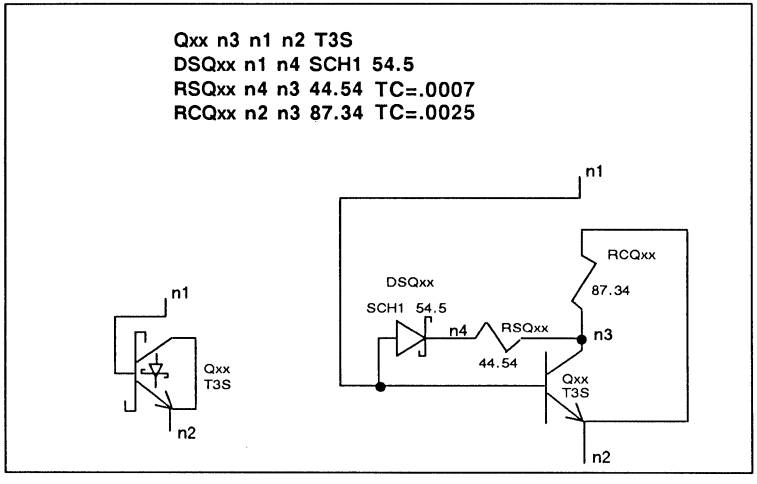
DIODES (Diode-Connected npn Transistor)

Figure 12: T3, T12, TLN1, T50



SCHOTTKY DIODES (Diode-Connected npn Transistor)

Figure 13: T3S



COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

Figure 14: T30S

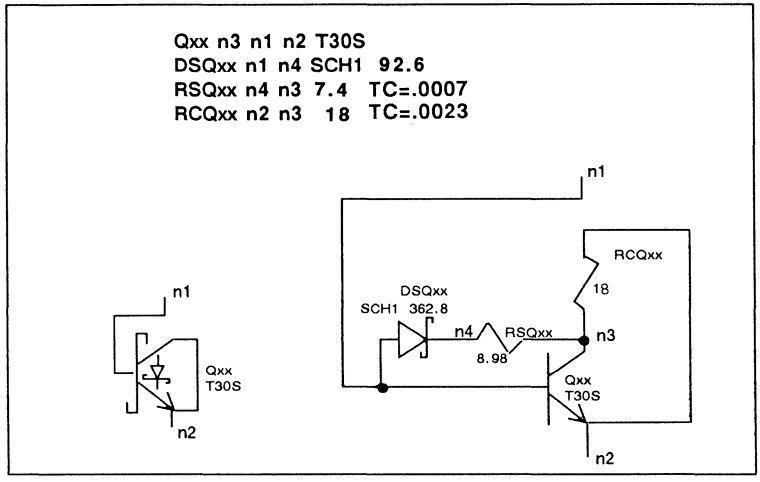
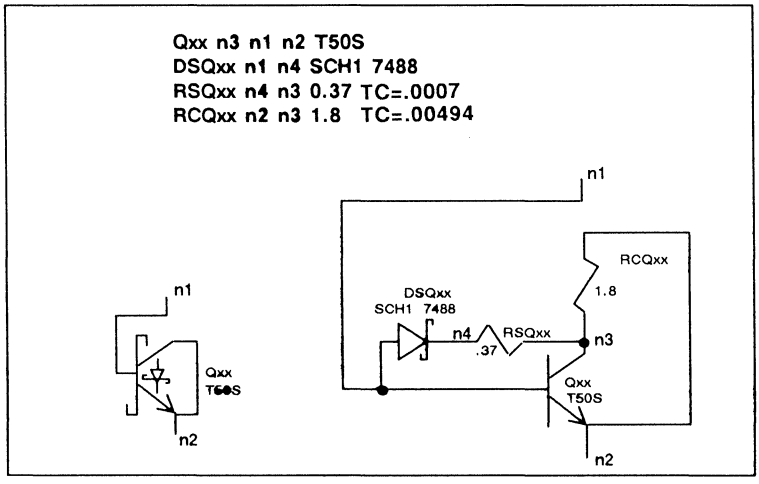


Figure 15: T50S

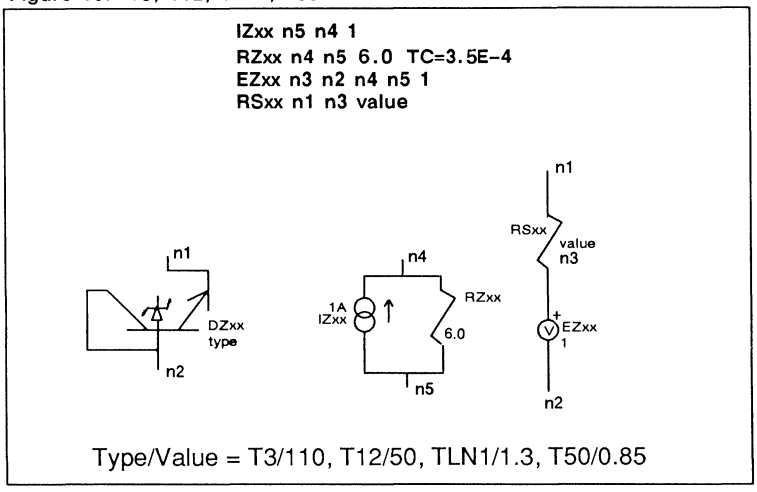


BIPOLAR SEMICUSTOM

COMPONENT SYMBOLS and SPICE MODELS for VJ800 ANALOG MASTER CHIP

DC ZENER DIODES

Figure 16: T3, T12, TLN1, T50



AC ZENER DIODES

Figure 17: T3, T12, TLN1, T50

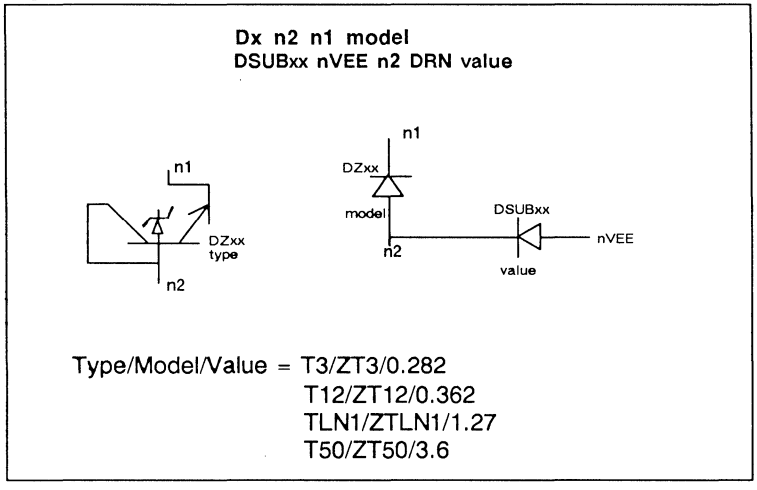


Table 10: Transistor Models at Nominal Beta and Nominal Zener Voltage

```
.MODEL T3 NPN(IS=1.26E-17 BF=84 BR=Ø.7 ISE=Ø ISC=Ø IKF=2.7E-3 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=5.47E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.82E-13 VJS=Ø.67 MJS=Ø.44 VAF=29 VAR=7.3 RC=87.34
+RB=621.33 RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.13)

.MODEL T12 NPN(IS=5.Ø4E-17 BF=1Ø1 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.Ø8E-2 IKR=2.88E-2
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=2.Ø3E-13 CJC=1.Ø1E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=3.62E-13 VJS=Ø.67 MJS=Ø.44 VAF=29 VAR=7.3
+RC=55.72 RB=282.4 RE=Ø.397 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.28)

.MODEL TLN1 NPN(IS=5.6E-16 BF=86 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.2E-1 IKR=3.2E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=2.74E-12 CJC=1.35E-12 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=1.27E-12 VJS=0.67 MJS=0.44 VAF=29 VAR=7.3
+RC=18.88 RB=7.48 RE=Ø.Ø36 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.1Ø)

.MODEL T5Ø NPN(IS=3.ØE-15 BF=1Ø3 BR=.7 ISE=Ø ISC=Ø IKF=.67 IKR=1.79 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=5.75E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=3.3E-12 VJS=.67 MJS=.44 VAF=29 VAR=7.3 RC=.6 RB=3.2
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5 XCJC=.3)

.MODEL T3S NPN(IS=1.26E-17 BF=84 BR=.Ø7 ISE=Ø ISC=Ø IKF=2.7E-3 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=6.Ø3E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.87E-13 VJS=Ø.67 MJS=Ø.44 VAF=29 VAR=7.3 RC=Ø
+RB=621.33 RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.12)
*COLL R=87 SCH AREA=5Ø SCH RES=45

.MODEL T3ØS NPN(IS=3.36E-16 BF=12Ø BR=Ø.7 ISE=Ø ISC=Ø IKF=7.2E-2 IKR=1.92E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=9.78E-13 CJC=4.15E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=7.96E-13 VJS=Ø.67 MJS=Ø.44 VAF=29 VAR=7.3
+RC=Ø RB=87.83 RE=Ø.Ø6 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.39)
*COLL R=7.4 SCH AREA=92.6 SCH RES=18

.MODEL TLP1 PNP(IS=2.8E-16 BF=55 BR=Ø.5 ISE=Ø ISC=Ø IKF=Ø.3E-3 IKR=9E-4
+NE=1.5 NC=1.5 TF=3.54E-8 TR=1.Ø6E-7 CJE=1.14E-13 CJC=5.8E-13 VJE=Ø.74
+VJC=Ø.74 MJE=Ø.41 MJC=Ø.41 CJS=Ø VJS=1.Ø MJS=1.Ø VAF=27 VAR=9 RC=1ØØ
+RB=5Ø RE=5 XTB=.81Ø9 EG=1.17 FC=Ø.5 XTI=3.5 XCJC=.8Ø)
*BASE SUBSTRATE CAP=.815

.MODEL T5ØS NPN(IS=3.ØE-15 BF=1Ø3 BR=.7 ISE=Ø ISC=Ø IKF=.65 IKR=1.2 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=6.6E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=4.6E-12 VJS=.67 MJS=.44 VAF=29 VAR=7.3 RC=Ø RB=3.3
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5 XCJC =.25)
*COLL R=7.25 SCH AREA=654 SCH RES=3.75

.MODEL SCH1 D(IS=1.2E-13 CJO=3.8E-16 RS=2.2E4 VJ=Ø.75 M=Ø.5 EG=Ø.75 XTI=2
+N=1.13 BV=12)

.MODEL DRN D(IS=2E-16 CJO=1E-12 VJ=Ø.67 M=Ø.44)

.MODEL DRP D(IS=2E-16 CJO=1E-12 VJ=Ø.74 M=Ø.41)

.MODEL ZT3 D(IS=1.26E-17 IBV=1E-9 BV=6.0 RS=11Ø CJO=7.92E-14)

.MODEL ZT12 D(IS=5.Ø4E-17 IBV=1E-9 BV=6.0 RS=5Ø CJO=2.Ø3E-13)

.MODEL ZTLN1 D(IS=5.6E-16 IBV=1E-9 BV=6.0 RS=1.3 CJO=2.74E-12)

.MODEL ZT5Ø D(IS=3.ØE-15 IBV=1E-9 BV=6.0 RS=Ø.85 CJO=12.7E-12)

.MODEL JCPC D(IS=2E-16 CJO=1E-12 VJ=Ø.9Ø M=.35 BV=5)
```

Table 10.1: Transistor Models at Minimum Beta and Minimum Zener Voltage

```
.MODEL T3 NPN(IS=1.26E-17 BF=52 BR=Ø.7 ISE=Ø ISC=Ø IKF=2.7E-3 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=5.74E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.82E-13 VJS=Ø.67 MJS=Ø.44 VAF=48 VAR=12 RC=87.34
+RB=4Ø8 RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL T12 NPN(IS=5.Ø4E-17 BF=62 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.Ø8E-2 IKR=2.88E-2
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=2.Ø3E-13 CJC=1.Ø1E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=3.62E-13 VJS=Ø.67 MJS=Ø.44 VAF=48 VAR=12
+RC=55.72 RB=185 RE=Ø.397 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL TLN1 NPN(IS=5.6E-16 BF=53 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.2E-1 IKR=3.2E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=2.74E-12 CJC=1.35E-12 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=1.27E-12 VJS=Ø.67 MJS=Ø.44 VAF=48 VAR=12
+RC=18.88 RB=5.64 RE=Ø.Ø36 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL T3S NPN(IS=1.26E-17 BF=52 BR=Ø.7 ISE=Ø ISC=Ø IKF=2.7E-2 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=6.Ø3E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.87E-13 VJS=Ø.67 MJS=Ø.44 VAF=48 VAR=9 RC=Ø
+RB=4Ø8 RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)
*COLL R=87.3 SCH AREA=5Ø SCH RES=44.5

.MODEL T3ØS NPN(IS=3.36E-16 BF=57.3 BR=Ø.7 ISE=Ø ISC=Ø IKF=7.2E-2 IKR=1.92E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=9.78E-13 CJC=4.15E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=-Ø.41 CJS=7.96E-13 VJS=Ø.67 MJS=Ø.44 VAF=48 VAR=9
+RC=Ø RB=56.9 RE=Ø.Ø6 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)
*COLL R=7.4 SCH AREA=92.6 SCH RES=18

.MODEL TLP1 PNP(IS=2.8E-16 BF=33 BR=Ø.5 ISE=Ø ISC=Ø IKF=Ø.3E-3 IKR=1E-3
+NE=1.5 NC=1.5 TF=3.54E-8 TR=1.Ø6E-7 CJE=1.14E-13 CJC=5.8E-13 VJE=Ø.74
+VJC=Ø.74 MJE=Ø.41 MJC=Ø.41 CJS=Ø VJS=1.Ø MJS=1.Ø VAF=45 VAR=15 RC=1ØØ RB=5Ø
+RE=5 XTB=.811 EG=1.17 FC=Ø.5 XTI=3.5)
*BASE-SUBSTRATE CAP=.815

.MODEL T5Ø NPN(IS=3.ØE-15 BF=63 BR=.7 ISE=Ø ISC=Ø IKF=.67 IKR=1.79 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=5.75E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=3.3E-12 VJS=.67 MJS=.44 VAF=48 VAR=12 RC=.6 RB=3.2
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5)

.MODEL T5ØS NPN(IS=3.ØE-15 BF=63 BR=.7 ISE=Ø ISC=Ø IKF=.67 IKR=1.79 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=5.75E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=4.6E-12 VJS=.67 MJS=.44 VAF=48 VAR=12 RC=Ø RB=3.2
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5)

.MODEL SCH1 D(IS=1.2E-13 CJO=3.8E-16 RS=2.2E4 VJ=Ø.75 M=Ø.5 EG=Ø.75 XTI=2
+N=1.13 BV=12)

.MODEL DRN D(IS=2E-16 CJO=1E-12 VJ=Ø.67 M=Ø.44)

.MODEL DRP D(IS=2E-16 CJO=1E-12 VJ=Ø.74 M=Ø.41)

.MODEL ZT3 D(IS=1.26E-17 IBV=1E-9 BV=5.8 RS=11Ø CJO=7.92E-14)

.MODEL ZT12 D(IS=5.Ø4E-17 IBV=1E-9 BV=5.8 RS=5Ø CJO=2.Ø3E-13)

.MODEL ZTLN1 D(IS=5.6E-16 IBV=1E-9 BV=5.8 RS=1.3 CJO=2.74E-12)

.MODEL ZT5Ø D(IS=3.ØE-15 IBV=1E-9 BV=5.8 RS=Ø.85 CJO=12.7E-12)

.MODEL JCPC D(IS=2E-16 CJO=1E-12 VJ-Ø.9Ø M=.35 BV=5)
```

Table 10.2: Transistor Models at Maximum Beta and Maximum Zener Voltage

```
.MODEL T3 NPN(IS=1.26E-17 BF=147 BR=Ø.7 ISE=Ø ISC=Ø IKF=2.7E-3 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=5.74E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.82E-13 VJS=Ø.67 MJS=Ø.44 VAF=17 VAR=4.25 RC=87.34
+RB=1Ø4Ø RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL T12 NPN(IS=5.Ø4E-17 BF=177 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.Ø8E-2 IKR=2.88E-2
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=2.Ø3E-13 CJC=1.Ø1E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=3.62E-13 VJS=Ø.67 MJS=Ø.44 VAF=17 VAR=4.25
+RC=55.72 RB=473 RE=Ø.397 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL TLN1 NPN(IS=5.6E-16 BF=151 BR=Ø.7 ISE=Ø ISC=Ø IKF=1.2E-1 IKR=3.2E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9CJE=2.74E-12 CJC=1.35E-12 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=1.27E-12 VJS=Ø.67 MJS=Ø.44 VAF=17 VAR=4.25
+RC=18.88 RB=12.3 RE=Ø.Ø36 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)

.MODEL T3S NPN(IS=1.26E-17 BF=147 BR=Ø.7 ISE=Ø ISC=Ø IKF=2.7E-3 IKR=7.2E-3
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=7.71E-14 CJC=6.Ø3E-14 VJE=Ø.88 VJC=Ø.74
+MJE=Ø.42 MJC=Ø.41 CJS=2.87E-13 VJS=Ø.67 MJS=Ø.44 VAF=17 VAR=4.25 RC=Ø
+RB=1Ø4Ø RE=1.587 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)
*COLL R=87.3 SCH AREA=5Ø SCH RES=44.5

.MODEL T3ØS NPN(IS=3.36E-16 BF=211 BR=Ø.7 ISE=Ø ISC=Ø IKF=7.2E-2 IKR=1.92E-1
+NE=1.5 NC=1.5 TF=2.27E-1Ø TR=2.27E-9 CJE=9.78E-13 CJC=4.15E-13 VJE=Ø.88
+VJC=Ø.74 MJE=Ø.42 MJC=Ø.41 CJS=7.96E-13 VJS=Ø.67 MJS=Ø.44 VAF=17 VAR=4.25
+RC=Ø RB=149 RE=Ø.Ø6 XTB=1.58936 EG=1.17 FC=Ø.5 XTI=3.5)
*COLL R=7.4 SCH AREA=92.6 SCH RES=18

.MODEL TLP1 PNP(IS=2.8E-16 BF=92 BR=Ø.5 ISE=Ø ISC=Ø IKF=Ø.3E-3 IKR=9E-4
+NE=1.5 NC=1.5 TF=3.54E-8 TR=1.Ø6E-7 CJE=1.14E-13 CJC=5.8E-13 VJE=Ø.74
+VJC=Ø.74 MJE=Ø.41 MJC=Ø.41 CJS=Ø VAF=16.1 VAR=5.38 RC=1ØØ RB=5Ø RE=5 XTB=1.3
+EG=1.17 FC=Ø.5 XTI=3.5)
*BASE-SUBSTRATE CAPC=.815

.MODEL T5Ø NPN(IS=3.6E-14 BF=18Ø BR=.7 ISE=Ø ISC=Ø IKF=.67 IKR=1.79 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=5.75E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=4.6E-12 VJS=.67 MJS=.44 VAF=17 VAR=4.25 RC=.6 RB=8.1
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5)

.MODEL T5ØS NPN(IS=3.6E-14 BF=18Ø BR=.7 ISE=Ø ISC=Ø IKF=.67 IKR=1.79 NE=1.5
+NC=1.5 TF=2.27E-1Ø TR=8.97E-8 CJE=12.12E-12 CJC=6.6E-12 VJE=.88 VJC=.74
+MJE=.42 MJC=.41 CJS=6.Ø4E-12 VJS=.67 MJS=.44 VAF=17 VAR=4.25 RC=Ø RB=8.1
+RE=.ØØ6 XTB=1.58 EG=1.17 FC=.5 XTI=3.5)
*COLL R=6.82 SCH AREA=5ØØ SCH RES=6.56

.MODEL SCH1 D(IS=1.2E-13 CJO=3.8E-16 RS=2.2E4 VJ=Ø.75 M=Ø.5 EG=Ø.75 XTI=2
+N=1.13 BV=12

.MODEL DRN D(IS=2E-16 CJO=1E-12 VJ=Ø.67 M=Ø.44)

.MODEL DRP D(IS=2E-16 CJO=1E-12 VJ=Ø.74 M=.Ø41)

.MODEL ZT3 D(IS=1.26E-17 IBV=1E-9 BV=6.2 RS=11Ø CJO=7.92E-14)

.MODEL ZT12 D(IS=5.Ø4E-17 IBV=1E-9 BV=6.2 RS=5Ø CJO=2.Ø3E-13)

.MODEL ZTLN1 D(IS=5.6E-16 IBV=1E-9 BV=6.2 RS=1.3 CJO=2.74E-12)

.MODEL ZT5Ø D(IS=3.ØE-15 IBV=1E-9 BV=6.2 RS=Ø.85 CJO=12.7E-12)

.MODEL JCPC D(IS=2E-16 CJO=1E-12 VJO=Ø.9Ø M=.35 BV=5)
```

Table 10.3: Transistor Models at Worst-Case Fast

```
.MODEL T3 NPN(IS=1.26E-17 BF=84 BR=.7 ISE=Ø IKF=.ØØ324 IKR=.ØØ864 NE=1.5 NC=1.5
+TF=1.98E=1Ø TR=1.98E-9 CJE=6.17E-14 CJC=4.65E-14 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=2.17E-13 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=76.6 RB=615 RE=1.32 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.129)

.MODEL T12 NPN(IS=5.Ø4E-17 BF=1Ø1 BR=.7 ISE=Ø IKF=.Ø13 IKR=.Ø346 NE=1.5 NC=1.5
+TF=1.98E-1Ø TR=1.98E-9 CJE=1.62E-13 CJC=8.62E-14 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=2.77E-13 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=48.9 RB=28Ø RE=.331 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.278)

.MODEL TLN1 NPN(IS=5.6E-16 BF=86 BR=.7 ISE=Ø IKF=.144 IKR=.384 NE=1.5 NC=1.5
+TF=1.98E-1Ø TR=1.98E-9 CJE=2.19E-12 CJC=1.14E-12 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=9.41E-13 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=16.5 RB=7.37 RE=.Ø298 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.Ø981)

.MODEL T5Ø NPN(IS=3.1E-15 BF=1Ø3 BR=.7 ISE=Ø IKF=.84 IKR=2.15 NE=1.5 NC=1.5
+TF=1.98E=1Ø TR=1.98E-9 CJE=9.67E-12 CJC=4.88E-12 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=3.31E-12 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=.5Ø RB=4.8 RE=.ØØ5 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.3)

.MODEL T3S NPN(IS=1.26E-17 BF=84 BR=.7 ISE=Ø IKF=.ØØ324 IKR=.ØØ864 NE=1.5 NC=1.5
+TF=1.98E-1Ø TR=1.98E-9 CJE=6.17E-14 CJC=5.12E-14 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=2.22E-13 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=Ø RB=615 RE=1.32 XTB=1.59
+EG=-1.17 FC=.5 XTI=3.5 XCJC=.117)
*COLL R=76.6 SCH AREA=5Ø SCH RES=4Ø.1

.MODEL T3ØS NPN(IS=3.36E-16 BF=12Ø BR=.7 ISE=Ø IKF=.Ø864 IKR=.23 NE=1.5 NC=1.5
+TF=1.98E=1Ø TR=1.98E-9 CJE=7.83E-13 CJC=3.53E-13 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=7.96E-13 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=Ø RB=87.2 RE=.Ø496 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.386)
*COLL R=6.45 SCH AREA=92.6 SCH RES=16.2

.MODEL T5ØS NPN(IS=3.1E-15 BF=1Ø3 BR=.7 ISE=Ø IKF=.84 IKR=2.15 NE=1.5 NC=1.5
+TF=1.98E-1Ø TR=1.98E-9 CJE=9.67E-12 CJC=5.6Ø4E-12 VJE=.88 VJC=.74 MJE=.42 MJC=.41
+CJS=4.34E-12 VJS=.67 MJS=.44 VAF=29 VAR=7.25 RC=.5Ø RB=4.8 RE=.ØØ5 XTB=1.59
+EG=1.17 FC=.5 XTI=3.5 XCJC=.25)
*COLL R=6.Ø5 SCH AREA=5ØØ SCH RES=5.91

.MODEL TLP1 PNP(IS=2.8E-16 BF=55 BR=.632 ISE=Ø IKF=.ØØØ36 IKR=.ØØ1Ø8 NE=1.5 NC=1.5
+TF=2.83E-8 TR=8.5E-8 CJE=9.69E-14 CJC=4.93E-13 VJE=.74 VJC=.74 MJE=.41 MJC=.41
+CJS=Ø VJS=1 MJS=1 VAF=27 VAR=9 RC=76.5 RB=42.5 RE=4.Ø5 XTB=.811 EG=1.17
+FC=.5 XTI=3.5 XCJC=.8)
*BASE-SUBSTRATE CAPAC= .612

.MODEL SCH1 D(IS=1.2E-13 CJO=3.8E-16 RS=2.2E4 VJ=Ø.75 M=Ø.5 EG=Ø.75 XTI=2
+N=1.13 BV=12

.MODEL DRN D(IS=2E-16 CJO=.8E-12 VJ=Ø.67 M=Ø.44)

.MODEL DRP D(IS=2E-16 CJO=.8E-12 VJ=Ø.74 M=Ø.41)

.MODEL ZT3 D(IS=1.26E-17 IBV=1E-9 BV=6.0 RS=11Ø CJO=6.34E-14)

.MODEL ZT12 D(IS=5.Ø4E-17 IBV=1E-9 BV=6.0 RS=5Ø CJO=1.62E-13)

.MODEL ZTLN1 D(IS=5.6E-16 IBV=1E-9 BV=6.0 RS=1.3 CJO=2.19E-12)

.MODEL ZT5Ø D(IS=3.ØE-15 IBV=1E-9 BV=6.0 RS=Ø.85 CJO=10.16E-12)

.MODEL JCPC D(IS=2E-16 CJO=.8E-12 VJO=Ø.9Ø M=.35 BV=5)
```

Figure 18: Schematic for SPICE Netlist Example

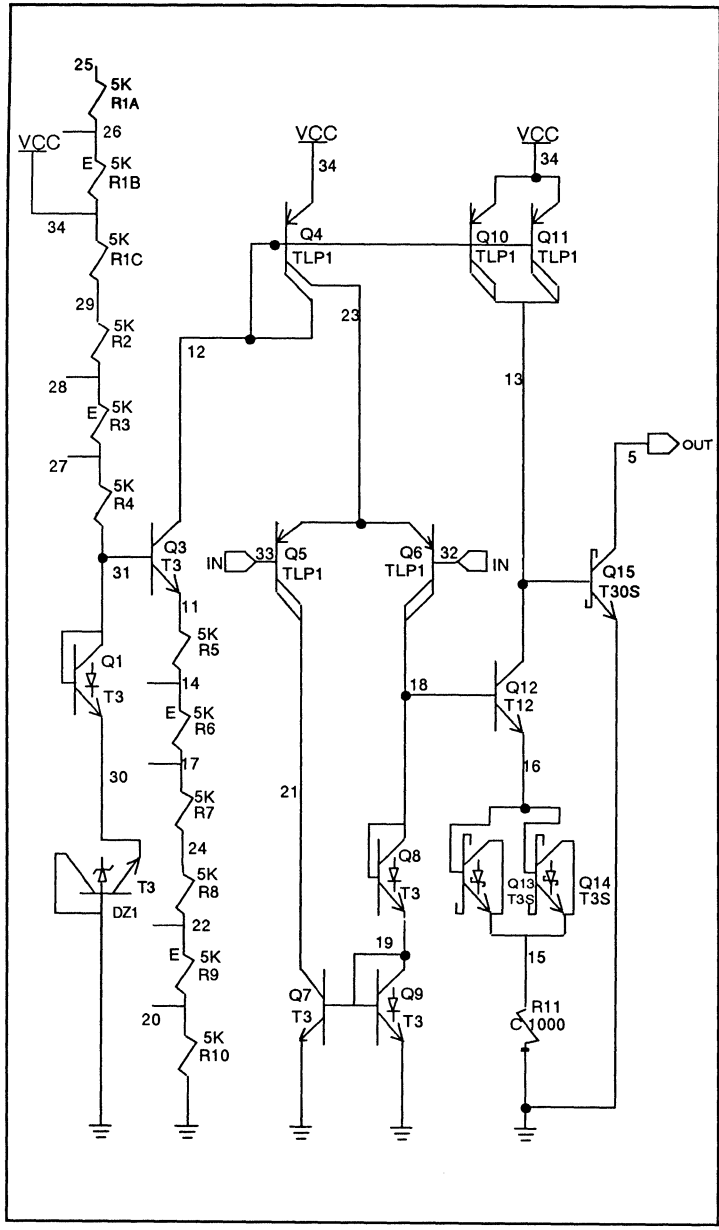


Table 11: SPICE Netlist Example

VCC	34	0		DC	12.0
R1A	26	25		5000	TC=.00292, 6.9E-6
R1B	34	26		5000	TC=.00292, 6.9E-6
R1C	34	29		5000	TC=.00292, 6.9E-6
DAR1A	25	34		DRP	.046
DR1A1B	26	34		DRP	.092
DAR1C	29	34		DRP	.046
R2	29	28		5000	TC=.00292, 6.9E-6
R3	28	27		5000	TC=.00292, 6.9E-6
R4	27	31		5000	TC=.00292, 6.9E-6
DAR2	29	34		DRP	.046
DR23	28	34		DRP	.092
DR34	27	34		DRP	.092
DAR4	31	34		DRP	.046
Q1	31	31	30	T3	
IZ1	0	200	1		
RZ1	200	0	6.0		
EZ1	111	0	200	0	1
RS1	30	111	110		
Q3	12	31	11	T3	
Q4A	12	12	34	TLP1	.5
Q4B	23	12	34	TLP1	.5
DQ4	0	12		DRN	.819
R5	11	14		5000	TC=.00292, 6.9E-6
R6	14	17		5000	TC=.00292, 6.9E-6
R7	17	24		5000	TC=.00292, 6.9E-6
DAR5	11	34		DRP	.046
DR56	14	34		DRP	.092
DR67	17	34		DRP	.092
DAR7	24	34		DRP	.046
R8	24	22		5000	TC=.00292, 6.9E-6
R9	22	20		5000	TC=.00292, 6.9E-6
R10	20	0		5000	TC=.00292, 6.9E-6
DAR8	24	34		DRP	.046
DR89	22	34		DRP	.092
DR910	20	34		DRP	.092
DAR10	0	34		DRP	.046
Q5A	21	33	23	TLP1	.5
Q5B	21	33	23	TLP1	.5
DQ5	33	0		DRN	.819
Q6A	18	32	23	TLP1	.5
Q6B	18	32	23	TLP1	.5
DQ6	32	0		DRN	.819
Q7	21	19	0	T3	
Q8	18	18	19	T3	
Q9	19	19	0	T3	
Q10A	13	12	34	TLP1	.5
Q10B	13	12	34	TLP1	.5
DQ10	12	0		DRN	.819
Q11A	13	12	34	TLP1	.5
Q11B	13	12	34	TLP1	.5
DQ11	12	0		DRN	.819
Q12	13	18	16	T12	
Q13	105	16	15	T3S	
DSQ13	16	106		SCH1	54.5
RSQ13	106	105		44.54	TC=.0007
RCQ13	105	15		87.34	TC=.0025
Q14	107	16	15	T3S	
DSQ14	16	108		SCH1	54.5
RSQ14	108	107		44.54	TC=.0007
RCQ14	107	15		87.34	TC=.0025
Q15	109	13	0	T30S	
DSQ15	13	110		SCH1	362.8
RSQ15	110	109		8.98	TC=.0007
RCQ15	5	109		17.89	TC=.0023
R11	15	0		1000	TC=.0003, 5.8E-6
DAR11	15	34		DRP	.14
DBR11	0	34		DRP	.19

Table 12.1

RESISTOR TABLE FOR VJ800 ANALOG MASTER CHIP
BASE TYPE RESISTOR
Name: A

R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N
159	.042	.086	0	165	.042	.086	0	170	.043	.085	0
176	.044	.084	0	181	.045	.083	0	187	.046	.082	0
192	.047	.081	0	198	.048	.080	0	203	.049	.079	0
209	.049	.079	1	214	.050	.078	1	220	.051	.077	1
225	.052	.076	1	231	.053	.075	1	236	.054	.074	1
242	.055	.073	1	247	.056	.072	1	253	.056	.072	1
258	.057	.071	1	264	.058	.070	1	269	.059	.069	1
275	.060	.068	1	280	.061	.067	1	286	.062	.066	1
291	.063	.065	1	297	.063	.065	1	300	.064	.064	1

N is the number of available route channels.

Table 12.2

RESISTOR TABLE FOR VJ800 ANALOG MASTER CHIP
BASE TYPE RESISTOR
NAME: B

R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N
188	.036	.132	0	195	.037	.131	0	201	.037	.131	0
208	.038	.130	0	214	.039	.129	0	221	.040	.128	0
227	.040	.128	0	234	.041	.127	0	240	.042	.126	0
247	.043	.125	1	253	.043	.125	1	260	.044	.124	1
266	.045	.123	1	273	.046	.122	1	279	.046	.122	1
286	.047	.121	1	292	.048	.120	1	299	.049	.119	1
305	.050	.119	1	312	.050	.118	1	318	.051	.117	1
325	.052	.116	1	331	.053	.116	1	338	.053	.115	1
344	.054	.114	1	351	.055	.113	1	357	.056	.112	1
364	.056	.112	2	370	.057	.111	2	377	.058	.110	2
383	.059	.109	2	390	.059	.109	2	396	.060	.108	2
403	.061	.107	2	409	.062	.106	2	416	.062	.106	2
422	.063	.105	2	429	.064	.104	2	435	.065	.103	2
442	.066	.103	2	448	.066	.102	2	455	.067	.101	2
461	.068	.100	2	468	.069	.100	2	474	.069	.099	2
481	.070	.098	3	487	.071	.097	3	494	.072	.097	3
500	.072	.096	3	506	.073	.095	3	513	.074	.094	3
519	.075	.093	3	526	.075	.093	3	532	.076	.092	3
539	.077	.091	3	545	.078	.090	3	552	.078	.090	3
558	.079	.089	3	565	.080	.088	3	571	.081	.087	3
578	.081	.087	3	584	.082	.086	3	591	.083	.085	3
597	.084	.084	4	600	.084	.084	4				

Table 12.3
RESISTOR TABLE FOR VJ800 ANALOG MASTER CHIP
BASE TYPE RESISTOR
NAME: C

R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N
181	.037	.293	0	188	.038	.292	0	194	.039	.291	0
200	.039	.291	0	206	.040	.290	0	212	.041	.289	0
219	.042	.288	0	225	.043	.287	0	231	.043	.287	0
238	.044	.286	1	244	.045	.285	1	250	.046	.284	1
256	.047	.283	1	263	.047	.283	1	269	.048	.282	1
275	.049	.281	1	281	.050	.280	1	288	.050	.280	1
294	.051	.279	1	300	.052	.278	1	306	.053	.277	1
313	.054	.276	1	319	.054	.276	1	325	.055	.275	1
331	.056	.274	1	338	.057	.273	1	344	.057	.273	1
350	.058	.272	2	356	.059	.271	2	362	.060	.270	2
369	.061	.269	2	375	.061	.269	2	381	.062	.268	2
388	.063	.267	2	394	.064	.266	2	400	.065	.265	2
406	.065	.265	2	413	.066	.264	2	419	.067	.263	2
425	.068	.262	2	431	.068	.262	2	438	.069	.261	2
444	.070	.260	2	450	.071	.259	2	456	.072	.258	2
463	.072	.258	3	469	.073	.257	3	475	.074	.256	3
481	.075	.255	3	487	.076	.254	3	494	.076	.254	3
500	.077	.253	3	506	.078	.252	3	512	.079	.251	3
519	.079	.251	3	525	.080	.250	3	531	.081	.249	3
537	.082	.248	3	544	.083	.247	3	550	.083	.247	3
556	.084	.246	3	563	.085	.245	3	569	.086	.244	3
575	.087	.243	4	581	.087	.243	4	588	.088	.242	4
594	.089	.241	4	600	.090	.240	4	606	.090	.240	4
613	.091	.239	4	619	.092	.238	4	625	.093	.237	4
631	.094	.236	4	638	.094	.236	4	644	.095	.235	4
650	.096	.234	4	656	.097	.233	4	662	.098	.232	4
669	.098	.232	4	675	.099	.231	4	681	.100	.230	4
688	.101	.229	5	694	.101	.229	5	700	.102	.228	5
706	.103	.227	5	713	.104	.226	5	719	.105	.225	5
725	.105	.225	5	731	.106	.224	5	738	.107	.223	5
744	.108	.222	5	750	.108	.221	5	756	.109	.221	5
763	.110	.220	5	769	.111	.219	5	775	.112	.218	5
781	.112	.218	5	787	.113	.217	5	794	.114	.216	5
800	.115	.215	6	806	.116	.214	6	813	.116	.214	6
819	.117	.213	6	825	.118	.212	6	831	.119	.211	6
838	.119	.211	6	844	.120	.210	6	850	.121	,209	6
856	.122	.208	6	863	.123	.207	6	869	.123	.207	6
875	.124	.206	6	881	.125	.205	6	888	.126	.204	6
894	.127	.203	6	900	.127	.203	6	906	.128	.202	6
912	.129	.201	7	919	.130	.200	7	925	.130	.200	7
931	.131	.199	7	938	.132	.198	7	944	.133	.197	7
950	.134	.196	7	956	.134	.196	7	963	.135	.195	7

R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N	R ohm	c1 pF	c2 pF	N
969	.136	.194	7	975	.137	.193	7	981	.138	.192	7
988	.138	.192	7	994	.139	.191	7	1000	.140	.190	7
1006	.141	.189	7	1013	.141	.189	7	1019	.142	.188	7
1025	.143	.187	8	1031	.144	.186	8	1038	.145	.185	8
1044	.145	.185	8	1050	.146	.184	8	1056	.147	.183	8
1063	.148	.182	8	1069	.149	.181	8	1075	.149	.181	8
1081	.150	.180	8	1087	.151	.179	8	1094	.152	.178	8
1100	.152	.178	8	1106	.153	.177	8	1113	.154	.176	8
1119	.155	.175	8	1125	.156	.174	8	1131	.156	.174	8
1138	.157	.173	9	1144	.158	.172	9	1150	.159	.171	9
1156	.160	.170	9	1163	.160	.170	9	1169	.161	.169	9
1175	.162	.168	9	1181	.163	.167	9	1188	.163	.167	9
1194	.164	.166	9	1200	.165	.165	9				

Table 13
VJ800 CHIP PAD TO PACKAGE PIN CORRESPONDENCE TABLE

Chip Pad #	18 Pin Package	20 Pin Package	22 Pin Package	24 Pin Package	28 Pin Package	40 Pin Package
1	–	–	1	–	1	1
2	1	–	–	1	2	2
3	–	–	2	–	3	3
4	2	1	–	2	–	4
5	–	–	3	–	4	5
6	3	2	4	3	5	6
7	–	–	–	–	–	7
8	4	3	5	4	6	8
9	–	4	–	5	7	9
10	5	5	6	6	–	10
11	–	6	–	7	8	11
12	–	7	–	8	9	12
13	6	8	7	9	10	13
14	–	–	–	–	–	14
15	7	9	8	10	11	15
16	–	–	9	–	12	16
17	8	10	–	11	–	17
18	–	–	10	–	13	18
19	9	–	–	12	14	19
20	–	–	11	–	–	20
21	–	–	12	–	15	21
22	10	–	–	13	16	22
23	–	–	13	–	17	23
24	11	11	–	14	–	24
25	–	–	14	–	18	25
26	12	12	15	15	19	26
27	–	–	–	–	–	27
28	13	13	16	16	20	28
29	–	–	–	17	21	29
30	–	14	–	18	–	30
31	14	15	17	19	22	31
32	–	16	–	20	23	32
33	15	17	18	21	24	33
34	–	18	–	–	–	34
35	16	19	19	22	25	35
36	–	–	20	–	26	36
37	17	20	–	23	–	37
38	–	–	21	–	27	38
39	18	–	–	24	28	39
40	–	–	22	–	–	40

TESTING FOR THE VJ800

Packaged sample parts are tested on VTC's Automatic Test Equipment (ATE). Simple DC functional and parametric tests (force and measure voltages and currents) are performed. More detailed tests require a special quote. Loads are soldered to a header, which will be plugged into a socket close to the socket for the Device Under Test (DUT). VJ800 users must provide the following information:

Load Schematic: Using the schematic provided with the VJ800 Design System (Figure 19), connections for loads (shorts, diodes, resistors, and/or capacitors) are drawn between any of the DUT pins as required. (Note: A 40-pin DUT is shown. Edit pinouts for devices of less than 40 pins.) The diodes are 1N914s. The resistors are 1%, 1/4W, metal film resistors of values from 10.0 to 1,000,000 ohms. All available resistor values are listed in Table 14.

The capacitors are 10%, 50 VDC, radial leaded monolithic ceramic capacitors of values from 10pF to 2.2μF. All available capacitor values are listed in Table 15. Other values or types of diodes, resistors and capacitors may be used if supplied by the VJ800 user.

Test Step Specification: The test specification sheet (Figure 20) must be filled out for every test desired. Several pins may be measured in a single test step. Any pin may be simultaneously forced and measured in the same test step. Voltages of ±1.0mV to ±100V and currents of ±5nA to ±256mA may be forced and/or measured.

Table 14: Readily Available Load Resistor Values (in ohms)

10.0	12.1	15.0	20.0	24.9	30.1	39.2	49.9
51.1	60.4	75.0	82.5	90.9	100	133	150
182	200	221	249	301	332	392	402
432	475	499	511	604	634	698	750
825	909	1000	1100	1210	1400	1500	2000
2100	2430	2490	2800	3010	3240	3320	3920
4020	4220	4530	4640	4750	4990	5110	5230
5620	6040	6490	6810	6980	7500	8060	8250
9090	9530	10.0K	11.0K	12.1K	13.0K	15.0K	15.8K
16.2K	18.2K	20.0K	21.0K	22.1K	24.3K	24.9K	28.0K
30.1K	35.7K	36.5K	39.2K	40.2K	46.4K	49.9K	51.1K
56.2K	60.4K	61.9K	68.1K	69.8K	75.0K	80.6K	82.5K
90.9K	100K	110K	121K	130K	140K	150K	178K
200K	210K	221K	232K	267K	301K	332K	357K
402K	453K	475K	499K	511K	604K	750K	1.00M

Table 15: Readily Available Capacitor Values

10pF	12pF	15pF	18pF
22pF	27pF	33pF	47pF
56pF	68pF	82pF	100pF
120pF	150pF	220pF	330pF
470pF	680pF	820pF	.001mF
.0015mF	.0022mF	.0033mF	.0047mF
.0056mF	.0068mF	.01mF	.015mF
.022mF	.033mF	.047mF	.068mF
.1mF	.15mF	.22mF	.33mF
.47mF	.68mF	1.0mF	2.2mF

Figure 19: DUT Schematic:

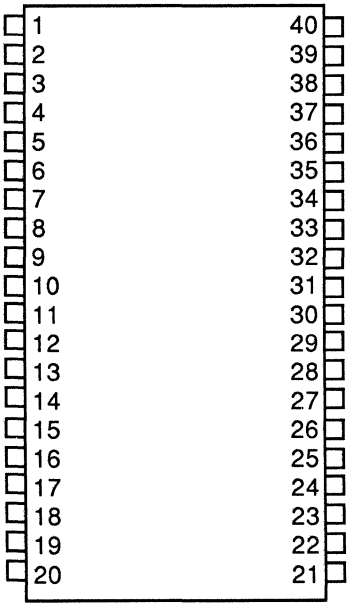


Figure 20: Test Specification Sheet

VJ800 TEST SPECIFICATION SHEET (Page _____ of _____)												
TEST NO.												
TEST NAME												
PIN	*FORCE*	*MEASURE*		*FORCE*	*MEASURE*		*FORCE*	*MEASURE*		*FORCE*	*MEASURE*	
		MIN	*MAX*		*MIN*	*MAX*		*MIN*	*MAX*		*MIN*	*MAX*
1												
2												
3												
4												
5												
35												
36												
37												
38												
39												
40												

DESIGNER'S CHECKLIST FOR THE VJ800 ANALOG MASTER CHIP

Below is a list of items which must be completed before the design can be considered finished:

DESIGN

- ☐ DC performance characteristics checked by simulation. Critical AC performance characteristics checked by simulation.
- ☐ Breakdown voltage limits are not exceeded.
- ☐ Worst-case simulation performed over temperature, power supply voltage, beta and resistance variations. DC, AC and proper circuit bias characteristics maintained over all conditions. Transistor saturation avoided under all conditions.
- ☐ Critical circuits simulated for resistor and/or transistor mismatch.
- ☐ Circuits with multiple supply voltages analyzed for possible power sequencing problems.
- ☐ Maximum chip power dissipation within acceptable limits for package used.

LAYOUT

- ☐ Layout checked against schematic.
- ☐ Metal line resistance and/or capacitance and via resistance calculated and evaluated where important.
- ☐ Maximum metal and/or via current not exceeded under worst-case conditions.
- ☐ Power supply bussing arranged to minimize crosstalk between large-signal and small-signal circuits.
- ☐ Adequate substrate contacts and resistor island contacts.

INFORMATION RETURNED TO VTC

- ☐ Completed layout plot.
- ☐ Complete circuit schematic.
- ☐ Description of package type and pinout.
- ☐ Table of resistor number versus resistor value.
- ☐ DUT schematic showing loads for testing.
- ☐ Test specification sheets.

NOTES

VL1000
LINEAR BIPOLAR CELL LIBRARY

FEATURES
- Linear Functions: Amplifiers, Comparators, DACs, References
- Digital Functions: Gates, Flip-Flops, Decoders, Three Power/Speed Levels for Optimum Performance
- Memory Functions: RAM or ROM
- TTL or ECL 10k I/O Levels
- Component Library Available to Create Unique or Proprietary Functions
- Workstation/PC-Based
- Amplifier Bandwidth to 200MHz
- Digital Clock Rates to 60MHz
- Suitable for ±5 or 12 Volt Power Supplies
- Available in Most Industry-Standard Packages
- Samples Available in 10 Weeks

APPLICATIONS
- Peripherals
- Telecommunications
- Automatic Test Equipment
- Discrete Circuit Replacement
- Analog Signal Processing
- Linear/Digital Subsystems
- Linear LSI Subsystems

DESCRIPTION
The VL1000 Linear Bipolar Cell Library contains a wide variety of predesigned linear, digital and memory functions, which provide the system designer versatile, cost-effective methods for LSI circuit design. With the VL1000, the designer can mix linear and digital circuits on the same chip without having to design at the transistor level, and still maintain high performance.

The well-defined, basic linear functions (i.e., Amplifiers, Comparators, etc.) can be used directly to convert discrete designs into LSI linear designs.

The digital cells have three power/speed levels that allow optimal power-speed trade-off. The input and output cells offer both TTL and ECL 10K compatibility.

Both RAM and ROM memory functions are available by special request. The need for these functions should be discussed with VTC.

Included as a subset to the VL1000 Cell Library is a component library for custom cell design. This allows design of unique or proprietary circuits from predefined transistors, resistors and capacitors.

The VL1000's advanced semiconductor process provides low noise, wide bandwidth linear circuits, and high-speed digital and memory circuits. The dual-metal, high-density cells are structured to minimize silicon area, and to facilitate interconnect and routing. This means increased performance and economical chip size.

DESIGNING WITH THE VL1000
Easy implementation of complex linear and digital LSI designs on a single integrated circuit is accomplished with the VL1000 Cell Library. The design system includes:
- VL1000 Data Sheet
- VL1000 User's Guide
- Component Design Manual
- Workstation Instructions

Using a workstation, the designer can enter and simulate a custom design with the library's predesigned cells. If there is a need for unique or proprietary circuits, the VL1000 component library is available. The custom cells can be mixed with standard cells.

The VL1000 methodology results in an efficient, quick-turn, error free design.

When circuit simulation is complete a diskette or tape is sent to VTC for circuit layout and fabrication. Layout time is minimal because only the cells need to be interconnected.

The designer has the option to receive either:
1. Samples tested to a simple DC functional test; or
2. Fully tested samples to the designer's specification.*

**Costs and time required for fully-tested samples are greater than for DC-tested samples.*

DIGITAL CELLS

NAME	AREA MILS²	TYPICAL PERFORMANCE, 5V, 25°C, 2 LOADS					
		HIGH		MED		LOW	
		P(mW)	S(nSec)	P	S	P	S
SIMPLE GATES:							
ORNOR2	40.6	2.25	2.0	1.13	2.3	0.56	4.2
ORNOR3	40.6	2.25	2.0	1.13	2.5	0.56	4.2
ORNOR4	40.6	2.25	2.0	1.13	2.5	0.56	4.4
ORNOR5	43.7	2.25	2.0	1.13	2.5	0.56	4.4
ORNOR6	43.7	2.25	2.0	1.13	2.7	0.56	4.6
ORNOR7	43.7	2.25	2.0	1.13	2.8	0.56	4.8
ANDNAND2	43.7	4.50	2.1	2.25	2.6	1.13	4.6
ANDNAND3	59.4	6.75	2.5	3.38	3.1	1.69	5.3
EXORNOR2	50.0	4.50	2.2	2.25	2.9	1.13	5.1
FLIP FLOPS:							
RS LATCH	40.6	2.25	5.6	1.13	7.7	0.56	12.8
D LATCH	46.9	4.50	2.2	2.25	3.1	1.13	5.5
D FF1	112.5	5.40	4.9	2.70	6.7	1.35	11.2
JKFF1	162.5	7.20	5.1	3.60	6.8	1.80	11.2
TFF1	112.5	5.40	4.9	2.70	6.7	1.35	11.2
DFF2	103.1	3.15	4.1	1.58	6.0	0.79	10.2
JKFF2	150.0	3.15	4.1	1.58	6.0	0.79	10.2
SPECIAL PURPOSE:							
CLOCKBUF	40.6	11.5	1.8	10.4	1.9	9.90	2.5
SIGBUF	21.9	—	—	5.0	1.4	—	—
POSNEGSHFT	37.5	4.10	1.5	2.05	2.1	1.02	2.3
INPUT/OUTPUT BUFFERS:							
IB BUFIN	46.9	—	—	6.35	1.2	—	—
OB BUFOUT	65.6	—	—	10.8	7.3	—	—
OB BUFOUTTS	81.2	—	—	10.8	8.7	—	—
OB BUFOUTOC	65.6	—	—	10.8	12.2	—	—
IB SCHMITT1	34.4	—	—	6.70	3.3	—	—
IB BUFIN10K	40.6	—	—	2.40	1.0	—	—
OB BUFOUT10K	65.6	—	—	49.4	2.3	—	—
MSI FUNCTIONS:							
DECODER 1OF4	56.2	4.50	2.0	2.25	2.7	1.13	4.5
DECODER 1OF8	128.1	6.75	2.2	3.38	2.9	1.69	4.8
MUX 2TO1	56.2	4.50	2.3	2.25	3.0	1.13	5.0
MUX 4TO1	100.0	6.75	2.7	3.38	3.6	1.69	6.3
BIAS GENERATORS:							
VCSGEN	34.4	—	—	3.23	—	—	—
VBBGEN	84.4	19.6	—	—	—	9.80	—
BIASGEN10K	43.7	—	—	10.4	—	—	—

LINEAR CELLS

NAME	AREA MILS²	I_{CC} MA	SUPPLIES $V_{CC} - V_{EE}$	COMMENTS
DIGITAL TO ANALOG CONVERTERS:				
Five Bit DAC	732	4.25	5	Five Bit Digital to Analog Converter with Current Output
Six Bit DAC	875	5.0	5	Six Bit Digital to Analog Converter with Current Output
Seven Bit DAC	1044	5.6	5	Seven Bit Digital to Analog Converter with Current Output
Eight Bit DAC	1225	6.2	5	Eight Bit Digital to Analog Converter with Current Output
OPERATIONAL AMPLIFIERS:				
OPAMP-A	269	1.0	5, 10, 12	General Purpose 741 Operational Amplifier
OPAMP-B	325	1.0	5, 10, 12	High Input Impedance 741 Operational Amplifier
OPAMP-C	207	1.0	5, 10, 12	Minimum Size 741 Operational Amplifier
OPAMP-D	444	4.0	5, 10, 12	High Drive 741 Operational Amplifier
VOLTAGE REFERENCES:				
Widlar Bandgap	207	2.0	5, 10, 12	Temperature and Supply Compensated Voltage Reference
Brokaw Bandgap	280	0.65	5, 10, 12	Temperature and Supply Compensated Voltage Reference with Variable Output
PTAT Bandgap	157	2.0	5, 10, 12	Temperature and Supply Compensated Voltage Reference
Widlar 2-Bandgap	110	1.0	10, 12	Temperature and Supply Compensated Voltage Reference with Positive Supply Referenced Output
CURRENT REFERENCES:				
Zener Current Reference	107	0.6	10, 12	Temperature and Supply Compensated Current Reference
External Zener Reference	119	*	12	Temperature and Supply Compensated Current Reference. Magnitude of Output Current is Controlled Externally
PTAT Current Reference	109	0.6	5, 10, 12	Generates Output Current Proportional to Absolute Temperature
Bandgap Current Source	244	0.5	10, 12	Temperature and Supply Compensated DAC Reference
COMPARATORS:				
339 Comparator	147	0.5	5, 10, 12	General Purpose Voltage Comparator
CML Compatible Comparator	154	1.0	5	Voltage Comparator with CML Compatible Outputs
WIDEBAND AMPLIFIERS:				
733 Video Amplifier	294	15	10, 12	Differential Input, Differential Output, Low Noise Amplifier

**Dependent on Output Current Magnitude*

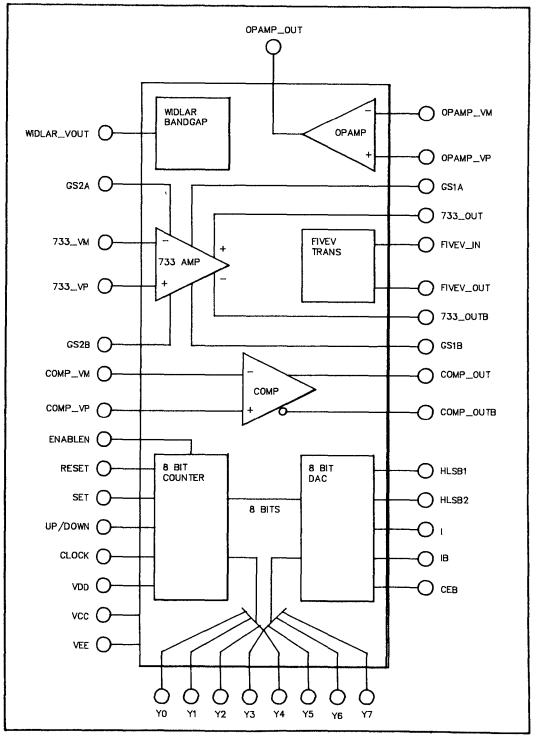
VL1001

EVALUATION CHIP FOR THE VL1000 LINEAR BIPOLAR CELL LIBRARY

FEATURES:

- Eight Bit Digital-to-Analog Converter
- Eight Bit Counter
- 733 Differential Video Amplifier
- Widlar Bandgap Voltage Reference
- High Speed Comparator
- High Output 741 Operational Amplifier

FUNCTIONAL BLOCK DIAGRAM:



DESCRIPTION:

The VL1001 evaluation chip is an integrated sample of analog and digital cells from the VL1000 Linear Bipolar Cell Library. The chip contains examples of several basic analog functions, as well as examples of digital functions. All of the inputs and outputs to the cells are pinned out individually to allow the user to exercise the cells on an individual basis. The cells on the chip can also be connected together to form an analog-to-digital converter subsystem. Suggested power supplies are $V_{DD} = 10$ volts, $V_{CC} = 5$ volts and V_{EE} = GROUND.

More information about the cells contained on the chip, is in the VL1000 Design Manual.

HIGH OUTPUT OPAMP This cell is a 741 architecture operational amplifier. The output of the opamp can supply 25mA of load current. The inverting input is identified as OPAMP_VM and the non-inverting input as OPAMP_VP.

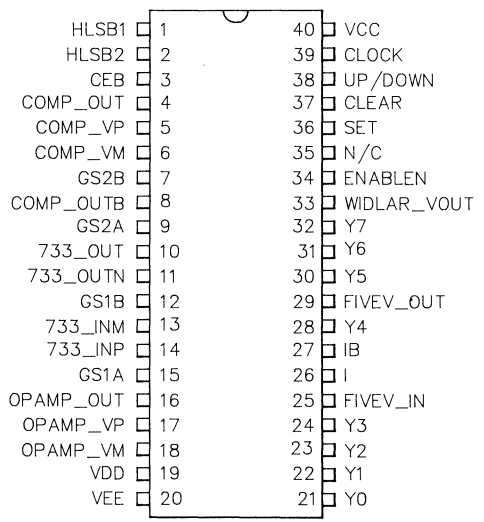
HIGH SPEED COMPARATOR The comparator on the chip is a high speed comparator with CML compatible outputs that are buffered to the external pins. The comparator exhibits 5mV of hysteresis for faster switching and shorter rise and fall times. The inverting input to the comparator is designated as COMP_VM and the non-inverting input to the comparator is designated as COMP_VP. The cell has complementary CML outputs, which are buffered to TTL levels for external outputs.

733 DIFFERENTIAL VIDEO AMPLIFIER This cell is a wideband differential input, differential output amplifier. The cell can be connected in three different gain configurations. The inverting input to the cell is designated 733_VM and the non-inverting input is 733_VP.

DIFFERENTIAL VOLTAGE GAIN ($R_S = 50$ Ohms, $R_L = 2K$ Ohms, $V_{OUT} = 3Vpp$)	SYMBOL	TYP
Gain 1 (Note 1)	A_v	400
Gain 2 (Note 2)		100
Gain 3 (Note 3)		10

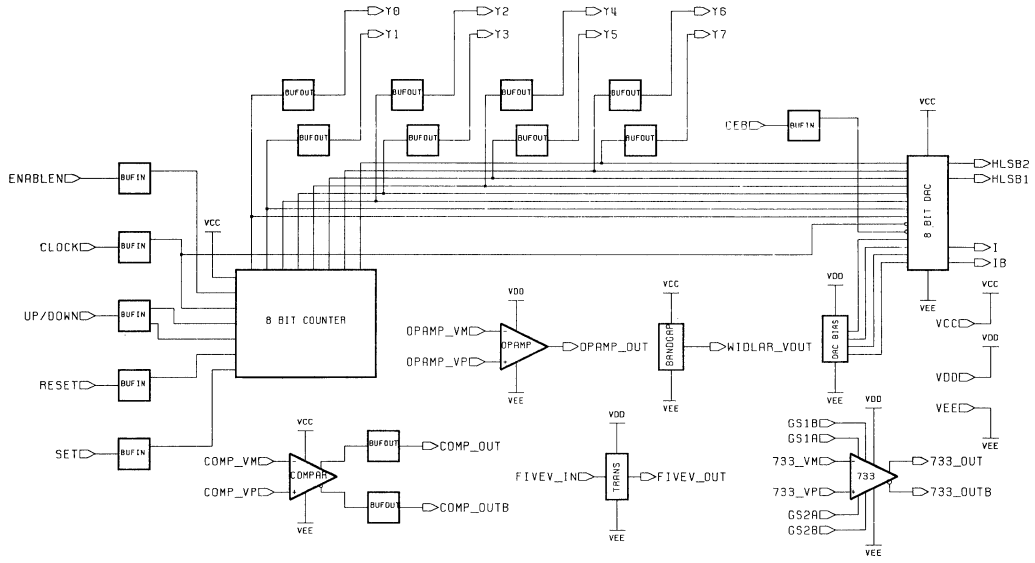
Note 1: Pins GS1A and GS1B connected together.
Note 2: Pins GS2A and GS2B connected together.
Note 3: Gain Select pins open.

CONNECTION DIAGRAM:



BIPOLAR SEMICUSTOM

CELL LEVEL BLOCK DIAGRAM



WIDLAR BANDGAP The Widlar Bandgap cell is an example of a voltage and temperature compensated voltage reference. The nominal output voltage of the cell is 1.24 volts. The cell is powered from the V_{CC} power supply. The output impedance of the cell is typically 2 Ohms for I_{OUT}<1.5mA.

8 BIT COUNTER This function is realized using various types of CML combinational and sequential logic from the VL1000 Cell Library. All of the inputs and outputs of the counter are TTL compatible. The counter will count in an up or down mode. Asynchronous set and reset inputs are provided as well as a counter enable input. A truth table is shown below:

ENABLEN	RESET	SET	UP/DOWN	CLOCK	EFFECT
1	0	0	X	X	No Action
X	1	0	X	X	Outputs Reset to 0
X	0	1	X	X	Outputs Set to 1
X	1	1	X	X	Undefined State
0	0	0	0	\	Count Up
0	0	0	1	\	Count Down

X = Don't Care
\ = Falling Edge

8 BIT DIGITAL-TO-ANALOG CONVERTER This cell is an 8 bit digital-to-analog converter with analog current output. The data inputs to the cell are accessible only from the output of the 8 bit counter. The CEB input is used as a DAC enable and is TTL-compatible. Four outputs are provided from the DAC: two 1/2LSB lines called HLSB1 and HLSB2, a true analog output current "I" and its complement "IB." These outputs must be tied to V_{CC} when not in use. When using I or IB as an analog current output, the output pin must be held at a voltage greater than or equal to V_{CC}. This ensures that the ouput will not saturate.

Full Scale Output Current	1mA
Relative Accuracy	1/4LSB

D	*CEB*	*CLOCK*	*EFFECT*
X	1	X	No Data Input
0	0	/	0 Data Input
1	0	/	1 Data Input

X = Don't Care
/ = Rising Edge

TTL Inputs and Outputs for Input and Output Buffers:

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IH}		2			V
V_{IL}				0.8	V
V_{OH}	$I_{OH} = -400\mu A$	2.7	3.4		V
V_{OL}	$I_{OL} = 4mA$		0.25	0.4	V
	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	$V_{IH} = 2.7V$			20	μA
I_{IL}	$V_{IL} = 0.4V$			−400	μA

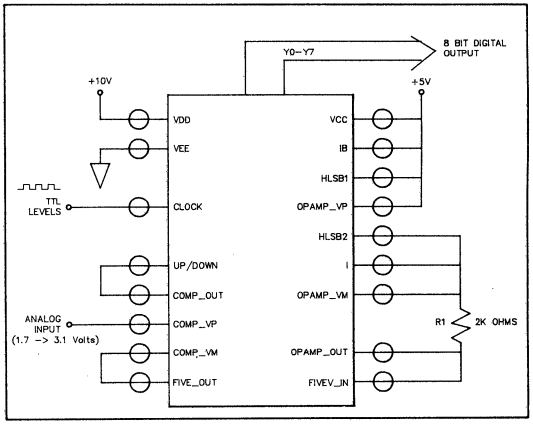
FIVE VOLT TRANSLATOR This cell is not part of the VL1000 Cell Library and is provided on the chip for the purpose of realizing the typical application as shown below.

TYPICAL APPLICATION:

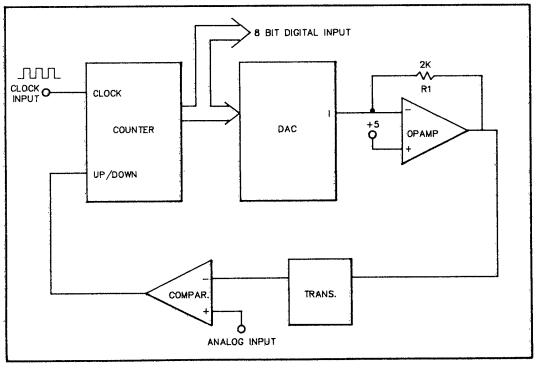
Function: Refer to the functional diagram shown below for a functional description. After being powered up, the Clock signal will start the counter cell counting up. The counter output is the input to the DAC, and the output current of the DAC is turned into a voltage with the OPAMP. The translator cell shifts the output voltage of the OPAMP into the input range of the comparator. The comparator cell compares the OPAMP output with the analog input and decides if the counter cell should count up or count down. When the final digital output is reached, the counter will toggle between two outputs, separated by a least significant bit.

The maximum clock frequency will be controlled by the loop propagation delay. The clock period cannot be less than the loop delay or the converter will be unstable. The analog input must be between 1.7 and 3.1 volts to be in the input range of the comparator. The value of R1 can be adjusted to control the output voltage swing of the OPAMP.

VL1001 CONNECTION DIAGRAM FOR AN 8 BIT ANALOG-TO-DIGITAL CONVERTER



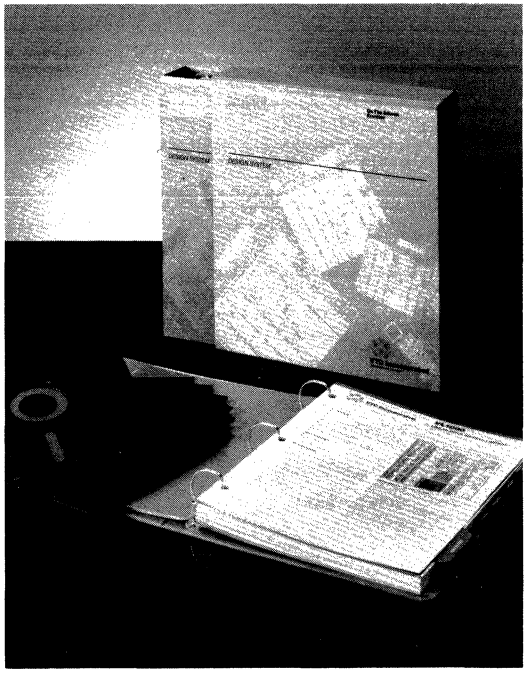
VL1001 FUNCTION DIAGRAM FOR AN 8 BIT ANALOG-TO-DIGITAL CONVERTER



BIPOLAR SEMICUSTOM

DESIGN SYSTEM

VL1000 LINEAR BIPOLAR CELL LIBRARY



FEATURES
- Data Sheet
- User's Guide
- Design Manual
- Design Notes
- Evaluation Chip Data Sheet (chip available on request)
- Database Software
- Technical Support

APPLICATIONS
- Peripherals
- Telecommunications
- Automatic Test Equipment
- Instrumentation
- Local Area Networks
- Discrete Circuit Replacement

DESCRIPTION

The information and procedures given in the VL1000 Linear Bipolar Cell Library Design System result in efficient, quick-turn, error-free designs.

The designer can implement complex linear and digital LSI designs on a single integrated circuit using the cell library provided with the VL1000 Design System.

The VL1000 User's Guide contains instructions for loading the cell library on an Apollo/Mentor workstation. The database software includes all the cell and component libraries needed to begin designing. The User's Guide describes how to create diagrams and schematics using the VL1000 cells and components, and how to execute simulations. A summary description and specification for each linear cell is given, along with digital cell design guidelines and specifications. In addition, it provides information for the designer to create special circuits. Custom designs are made easy with use of predesigned cells. Unique and proprietary circuits (cells) can also be built with the VL1000 component library. Custom cells can be mixed with standard cells in the design.

Testing requirements are given, and packaging characteristics described.

The Design Manual section of the VL1000 Design System gives the engineer the information needed to begin designing integrated circuitry. It assists engineering and development organizations in their attempt to incorporate application-specific LSI and VLSI chips into their products on a large scale. The Design Manual covers basic integrated circuit design concepts.

Design Notes give helpful information on various design methods.

VTC provides technical support for design system users whenever necessary.

VL1000

LINEAR BIPOLAR CELL LIBRARY

ADVANCE INFORMATION

CELL RELEASE 2.0

(Planned for Q1 1986 Availability)

- 5-Bit Analog-to-Digital Converter
- 6-Bit Analog-to-Digital Converter
- 7-Bit Analog-to-Digital Converter
- 8-Bit Analog-to-Digital Converter
- 10mA Voltage Regulator
- 60mA Voltage Regulator
- 592 Video Amp
- 4MHz Crystal Oscillator
- Retriggerable One-Shot
- AND/NAND, 2-2
- AND/NAND, 3-3
- AND/NAND, 2-2-2
- AND/NAND, 3-3-3
- Differential ECL10k Input Buffer
- TTL Tristate Buffer
- CML Tristate Driver
- CML Level Shifter
- D Flip-Flop with Self Test
- PNP Current Mirror
- NPN Current Mirror
- DAC Bias Generator
- Differential CML Comparator with 10V Input Range

CELL RELEASE 3.0

(Planned for Q3 1986 Availability)

- 9-Bit Digital -to-Analog Converter
- 10-Bit Digital-to-Analog Converter
- Transconductance Amplifier
- 555 Timer
- Precision Voltage Reference, Laser Trimmable
- Precision Operational Amplifier, Laser Trimmable
- 256 X N ROM
- Counter/Adder, 4-Bit
- 1350 IF Amp
- 124 Op Amp
- Precision Sample/Hold Amp
- 318 High Performance Op Amp
- 360 High Speed Comparator
- 1595 Multiplexer
- 1596 Modulator/Demodulator
- Component Library to Include Laser Trimmable Resistors and True Dielectric Capacitors

VL1000
LINEAR BIPOLAR CELL LIBRARY USER'S GUIDE

VL1000 USER'S GUIDE CONTENTS

TABLES

FIGURES

FOREWORD

VTC's VL1000 Linear Bipolar Cell Library uses versatile LSI design techniques. Although it is primarily intended for linear LSI applications, the VL1000 also allows digital and memory functions in the same circuit.

The VL1000 User's Guide shown here in condensed form contains information necessary to complete a circuit design, assuming the designer understands use of the workstation. A detailed review of the User's Guide found in the VL1000 Design System is recommended before proceeding.

The Design System User's Guide consists of the following sections:

Workstation Instructions — This section describes how to load the VL1000 Cell Library onto the Mentor Graphics™ workstation; how to create diagrams and schematics using the VL1000 cells and components; and how to execute simulations.

Linear Cell Specifications — This section gives a summary, description and specification for each of the linear cells.

Digital Cell Design Guidelines and Specifications — This section provides a digital cell summary, guidelines for designing with digital cells and specifications for each of the cells.

Custom Cell Design — This has information for the designer to create special circuits, assuming the designer is familiar with basic circuit design techniques.

Testing — This section describes how to specify circuit test requirements in order to ensure first-time circuit success.

Packaging — A description of the dimensions and thermal characteristics of packages available for the VL1000 can be found in the Design System.

The VL1000 gives a new dimension to LSI linear cell design. Proper use of this User's Guide will help make the first pass a success.

CUSTOMER INTERFACE

The interface between VTC and the customer for the VL1000 Linear Bipolar Cell Library involves several issues.

Technical Support — General technical support is available at no charge to the customer. It can be arranged by calling a VTC representative.

Ordering — After the customer has completed the VL1000 design, a purchase order is necessary to initiate layout and fabrication efforts at VTC. Each circuit is quoted individually and quotes can be requested at any time. VTC's quote, however, is only valid for the final design submitted for integration.

Custom Cells — If a custom cell is planned as pat of the design, it should be discussed with VTC as early in the design cycle as possible. This will enable VTC to allocate the necessary resources to do the cell layout prior to circuit integration.

Packaging — Information concerning package requirements must be defined at the time the circuit purchase order is submitted.

Testing — Testing requirements must bed at the time the circuit purchase order is initiated. Option 1 testing is included in every VL1000 contract. The Option 1 test requirement forms found in the Design System must be submitted with the purchase order. Option 2 testing requires submission of a test specification and test circuits.

Special Requirements — Any special circuit requirements should be discussed with VTC's product manager for the VL1000.

LINEAR CELL SPECIFICATIONS

DIGITAL-TO-ANALOG CONVERTERS

Included in the VL1000 Cell Library are four Digital-to-Analog Converters (DAC) with 5, 6, 7 and 8 bit resolution. The difference between the four converters is in the cell layout area and number of input bits. The output of each DAC is an analog current. Both true and complement output currents are available, as well as two 1/2 LSB currents. The data (D) inputs to the cell are captured on the rising clock edge by latches internal to the circuit. The clock enable (CEB) enables or disables the input latches. (Refer to Figure 1 for a functional truth table.)

All digital inputs to the cell are CML compatible. Because the DAC cells contain CML logic, VCSGEN and VBBGEN bias generators must be resident on the chip and present for any SPICE simulation. The power-supply voltages for the bias generators must match the power-supply voltages of the DACs.

For accurate and consistent results, the I, IB, HLSB1 and HLSB2 pins of the DACs must be held at a voltage greater than V_{CC}. This ensures that the output of the DAC will not saturate.

The DAC cells can be biased in the following two different configurations: 1) The DACs can be biased using the BANDGAP CURRENT SOURCE cell provided in the VL1000 Cell Library. A connection diagram for this biasing method is shown in Figure 2. This cell is designed as a DAC bias circuit and provides a nominal full-scale output current of 1mA. Refer to the data sheet for this cell for further information; 2) The DACs can be biased using an OPAMP in the negative feedback configuration as shown in Figure 3. The voltage references should be set as shown in Figure 3. The value of the full-scale output current can be calculated using the equation $I_{FB} = 2[V_{CC} - V_{REF}]/R1$. The negative feedback ensures that the voltage at the bottom of R1 will be equal to V_{REF}. All current going through R1 must go into the IDACREF pin due to the high input resistance of the OPAMP.

If R1 is external to the chip and V_{REF} is independent of temperature, then the temperature characteristics of the DAC output current will depend solely on the temperature characteristics of the external resistor. If R1 is internal to the chip and the output current of the DAC is forced across an internal resistor of the same type, a temperature independent output voltage will result. In either case, best results are obtained if V_{REF} tracks with V_{DD} because the voltage difference of $V_{DD} - V_{REF}$ determines the output current of the DAC. The WIDLAR2 Bandgap voltage reference is ideal for supplying V_{REF} because its output voltage tracks with V_{DD}.

FIGURE 1: TRUTH TABLE

CLKB	*CEB*	*ON*	*EFFECT*
/	0	0	0 Data Latched
/	0	1	1 Data Latched
X	1	X	No Data Change

/ = Rising Edge
X = Don't Care

Figure 2: DAC Biasing with Bandgap Current Source

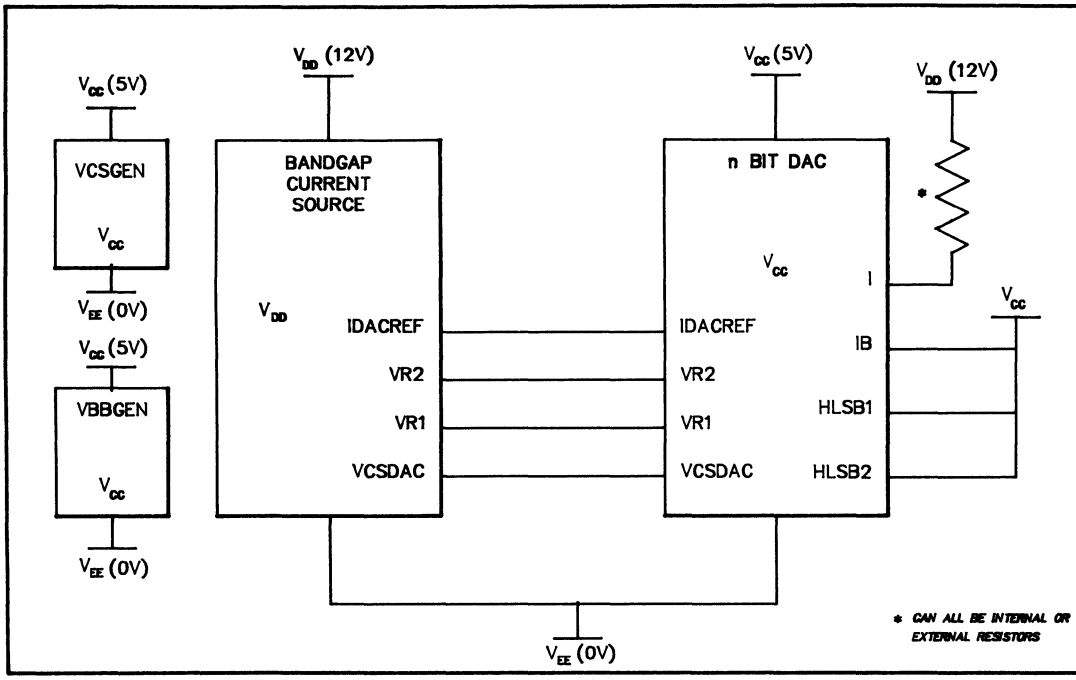
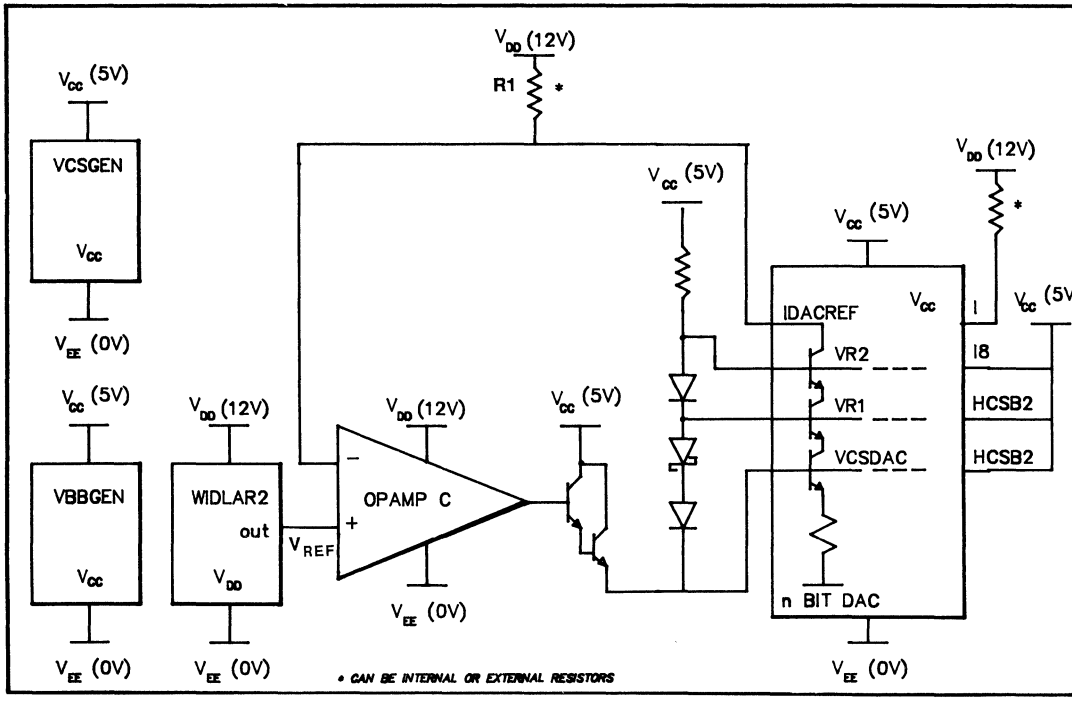


Figure 3: DAC Biasing with Op Amp

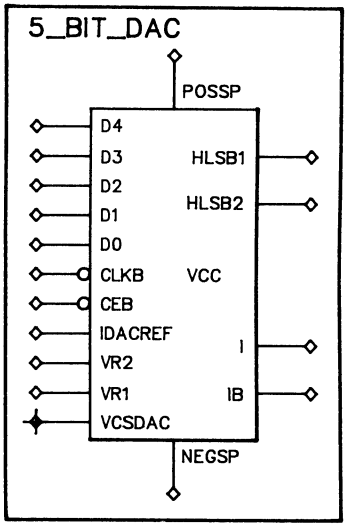


BIPOLAR SEMICUSTOM

FIVE BIT DAC

CELL AREA:
471744 Sq. Microns
732 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

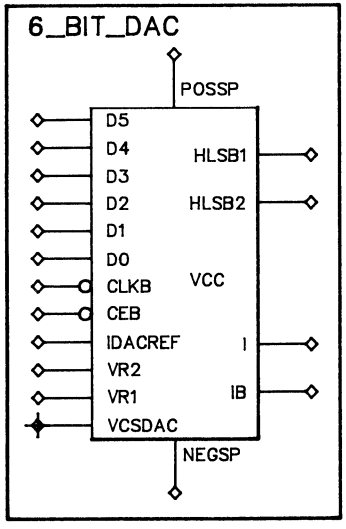
(Unless otherwise specified, V_{CC} = 5 V, V_{EE} = OV, Tj = 25°C)
(Reference Current Provided by Bandgap Current Source)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Relative Accuracy (Error relative to full scale I_O = 1mA)	E_r		1/4	1/2	LSB
Settling Time (within 1/2 LSB <includes t_{PD}> Tj = 25°C)	t_S		25	35	nS
Propagation Delay Time (D Input 50% to Output Current 50%)	t_{PD}		7	12	nS
Output Current (All Bits Low)	I_O		0.05	0.1	µA
(Full Scale)		0.5		2	mA
Output Voltage Compliance ($E_r \leq \pm$ 1/2LSB)	V_{O+} V_{O-}		1.5 1		V V
Output Current Power Supply Sensitivity	I_{OS}		10	20	µA/V
Positive Supply Current (1mA Full Scale Output)	I_{CC}		4.25	5.5	mA
Power Supply Dissipation	P_D		21.3	27.7	mW

SIX BIT DAC

CELL AREA:
564480 Sq. Microns
875 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

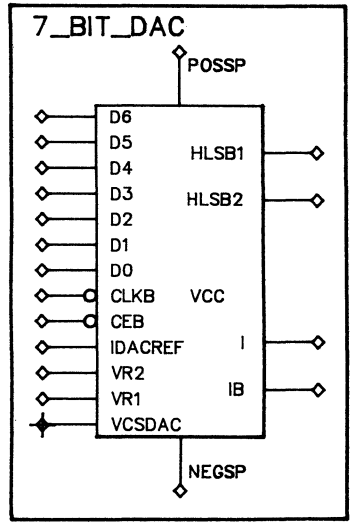
(Unless otherwise specified, V_{CC} = 5 V, V_{EE} = OV, Tj = 25°C)
(Reference Current Provided by Bandgap Current Source)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Relative Accuracy (Error relative to full scale I_O = 1mA)	E_r		1/4	1/2	LSB
Settling Time (within 1/2 LSB <includes t_{PD}> Tj = 25°C)	t_S		30	40	nS
Propagation Delay Time (D Input 50% to Output Current 50%)	t_{PD}		7	12	nS
Output Current (All Bits Low)	I_O		0.05	0.1	µA
(Full Scale)		0.5		2	mA
Output Voltage Compliance ($E_r \leq \pm$ 1/2LSB)	V_{O+} V_{O-}		1.4 0.9		V V
Output Current Power Supply Sensitivity	I_{OS}		10	20	µA/V
Positive Supply Current (1mA Full Scale Output)	I_{CC}		5	6.5	mA
Power Supply Dissipation	P_D		25	32.5	mW

SEVEN BIT DAC

CELL AREA:
673344 Sq. Microns
1044 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

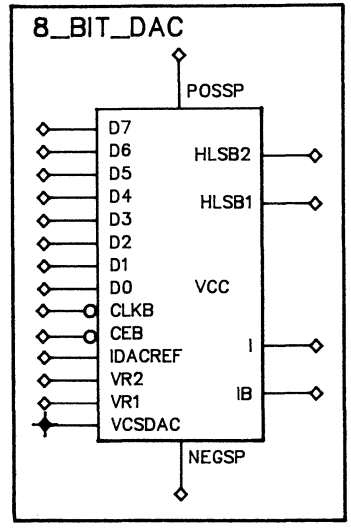
(Unless otherwise specified, V_{CC} = 5 V, V_{EE} = OV, Tj = 25°C)
(Reference Current Provided by Bandgap Current Source)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Relative Accuracy (Error relative to full scale I_O = 1mA)	E_r		1/4	1/2	LSB
Settling Time (within 1/2 LSB <includes t_{PD}> Tj = 25°C)	t_S		35	45	nS
Propagation Delay Time (D Input 50% to Output Current 50%)	t_{PD}		7	12	nS
Output Current (All Bits Low)	I_O		0.05	0.1	µA
(Full Scale)		0.5		2	mA
Output Voltage Compliance ($E_r \leq \pm$ 1/2LSB)	V_{O+} V_{O-}		1.3 0.8		V V
Output Current Power Supply Sensitivity	I_{OS}		10	20	µA/V
Positive Supply Current (1mA Full Scale Output)	I_{CC}		5.6	7.3	mA
Power Supply Dissipation	P_D		28	36.5	mW

EIGHT BIT DAC

CELL AREA:
790272 Sq. Microns
1225 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 5 V, V_{EE} = OV, Tj = 25°C)
(Reference Current Provided by Bandgap Current Source)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Relative Accuracy (Error relative to full scale I_O = 1mA)	E_r		1/4	1/2	LSB
Settling Time (within 1/2 LSB <includes t_{PD}> Tj = 25°C)	t_S		40	50	nS
Propagation Delay Time (D Input 50% to Output Current 50%)	t_{PD}		7	12	nS
Output Current (All Bits Low)	I_O		0.05	0.1	µA
(Full Scale)		0.5		2	mA
Output Voltage Compliance ($E_r \leq \pm$ 1/2LSB)	V_{O+} V_{O-}		1.2 0.7		V V
Output Current Power Supply Sensitivity	I_{OS}		10	20	µA/V
Positive Supply Current (1mA Full Scale Output)	I_{CC}		6.2	8	mA
Power Supply Dissipation	P_D		31	40	mW

OPERATIONAL AMPLIFIERS

The VL1000 Cell Library offers four basic versions of operational amplifiers. Each is designed to fill a specific application. The VL1000 operational amplifiers have standard power supply options for 5, 10 or 12 volt operation. The Type A OPAMP is a general purpose amplifier similar to the 741. The Type B OPAMP is similar to the Type A amplifier with the addition of input bias current compensation for lower input current and higher input resistance. This feature results in a lower input voltage range and a larger cell area. The Type C OPAMP is a minimum size amplifier for use where minimum cell area is important and lower voltage gain is acceptable. The Type D OPAMP is a large cell designed to deliver 25mA of load current. This is the only opamp that is recommended for driving external loads. A summary of all the operational amplifiers is given in the accompanying table. All figures are typical values at $T_j = 25°C$.

	CELL AREA (mil^2)	*VOLT. GAIN (V/mV)*	*INPUT CUR. (nA)*	*INPUT RES. (Ohms)*	*OUTPUT RES. (Ohms)*	*COMMON MODE INPUT RANGE*	*QUIE. CUR. (mA)*	*MAX. OUTPUT CUR.*
Type A	269	90	170	700K	300	$V_{CC}-0.9V$ $V_{EE}+2.2V$	1	500μA
Type B	325	90	20	6000K	300	$V_{CC}-2.3V$ $V_{EE}+2.2V$	1	500μA
Type C	207	23	170	600K	300	$V_{CC}-0.9V$ $V_{EE}+2.2V$	1	500μA
Type D	444	25	150	700K	70	$V_{CC}-0.9V$ $V_{EE}+2.2V$	4	25 mA

TYPE A OP AMP

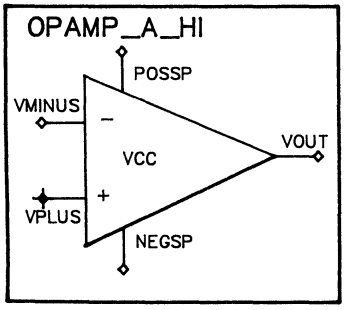
DESCRIPTION:

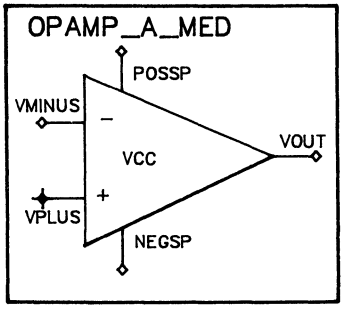
The Type A OPAMP is a 741 architecture, unconditionally stable operational amplifier. It offers high common mode rejection ratio, fast transient response and low power dissipation. The maximum output current for the cell is 0.5mA, making it well suited for driving internal loads. The cell can be powered from three different supply configurations: OPAMP A HI for V_{DD} - V_{EE} = 12 volts; OPAMP A MED for V_{DD} - V_{EE} = 10 volts; and OPAMP A LO for V_{CC} - V_{EE} = 5 volts. For all supply configurations the performance specifications are constant except as noted.

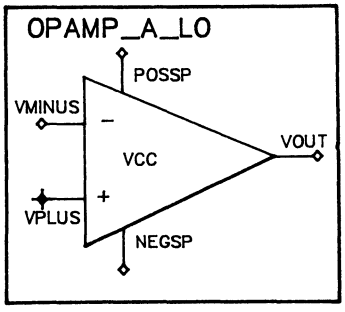
CELL AREA:

173376 Sq. Microns
269 Sq. Mils

SYMBOL:







ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 5V, V_{EE} = −5V, Tj = 25°C)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Input Offset Voltage ($R_S \leq$ 10K Ohms)	V_{OS}		2	5	mV
Input Offset Current	I_{OS}		20	200	nA
Input Bias Current	I_{IB}		170	400	nA
Input Resistance	R_{IN}	200	700		K Ohms
Input Capacitance	C_{IN}		1.4		pF
Input Common Mode Voltage Range	V_{CM}	$V_{CC}-1.1$ $V_{EE}+2.4$	$V_{CC}-0.9$ $V_{EE}+2.2$		V V
Large Signal Voltage Gain (V_O = ±4V, $R_L \geq$ 8K Ohms)	A_{VL}	20	90		V/mV
Output Resistance	R_O		300		Ohms
Common Mode Rejection Ratio ($R_S \leq$ 10K Ohms)	CMRR	70	90		dB
Power Supply Rejection Ratio ($R_S \leq$ 10K Ohms)	PSRR		30	150	µV/V
Output Voltage Swing ($R_L \geq$ 10K Ohms)	V_{OUT}	$V_{CC}-0.7$ $V_{EE}+2.1$	$V_{CC}-0.4$ $V_{EE}+1.7$		V V
Supply Current	I_S		1	1.5	mA
Power Consumption*	P_C		10	15	mW
Transient Response Slew Rate (Unity Gain - Non-Inverting) (V_I = 10V, $R_L \geq$ 10K Ohms, $C_L \leq$ 100pF)	SR		3		V/µS
Maximum Output Current	I_O			500	µA
Gain Bandwidth Product	GBW		5.5		MHz

**Power Consumption is a function of supply configuration.*

TYPE B OP AMP

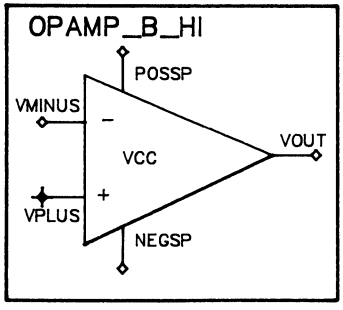
DESCRIPTION:

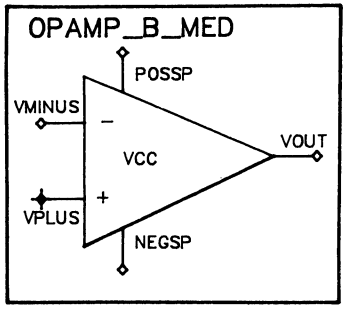
The Type B OPAMP is a 741 architecture, unconditionally stable operational amplifier with input bias current compensation. It offers high common mode rejection ratio, fast transient response and high input impedance. The maximum output current for the cell is 0.5mA, making it well suited for driving internal loads. The cell can be powered from two different supply configurations: OPAMP B HI for V_{DD} - V_{EE} = 12 volts; and OPAMP B MED for V_{DD} - V_{EE} = 10 volts. For all supply configurations the performance specifications are constant except as noted.

CELL AREA:

209664 Sq. Microns
325 Sq. Mils

SYMBOL:





ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 5V, V_{EE} = −5V, Tj = 25°C)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Input Offset Voltage ($R_S \leq 10K$ Ohms)	V_{OS}		2	5	mV
Input Offset Current	I_{OS}		5	25	nA
Input Bias Current	I_{IB}		20	50	nA
Input Resistance	R_{IN}	1000	6000		K Ohms
Input Capacitance	C_{IN}		1.4		pF
Input Common Mode Voltage Range	V_{CM}	$V_{CC}-2.5$ $V_{EE}+2.4$	$V_{CC}-2.3$ $V_{EE}+2.2$		V V
Large Signal Voltage Gain ($V_O = \pm 4V$, $R_L \geq 8K$ Ohms)	A_{VL}	20	90		V/mV
Output Resistance	R_O		300		Ohms
Common Mode Rejection Ratio ($R_S \leq 10K$ Ohms)	CMRR	70	90		dB
Supply Voltage Rejection Ratio ($R_S \leq 10K$ Ohms)	PSRR		30	150	μV/V
Output Voltage Swing ($R_L \geq 10K$ Ohms)	V_{OUT}	$V_{CC}-0.7$ $V_{EE}+2.1$	$V_{CC}-0.4$ $V_{EE}+1.7$		V V
Supply Current	I_S		1	1.5	mA
Power Consumption*	P_C		10	15	mW
Transient Response Slew Rate (Unity Gain — Non-Inverting) (V_I = 10V, $R_L \geq 10K$ Ohms, $C_L \leq 100pF$)	SR		3		V/μS
Maximum Output Current	I_O			500	μA
Gain Bandwidth Product	GBW		4		MHz

**Power Dissipation is a function of supply configuration.*

TYPE C OP AMP

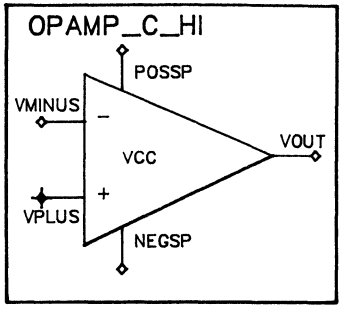
DESCRIPTION:

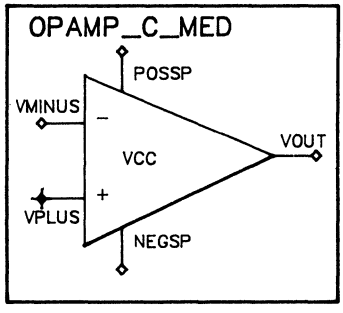
The Type C OPAMP is a 741 architecture, unconditionally stable operational amplifier. It offers fast transient response, low power dissipation and small layout area. The maximum output current for the cell is 0.5mA, making it well suited for driving internal loads. The cell can be powered from three different supply configurations: OPAMP C HI for V_{DD} - V_{EE} = 12 volts; OPAMP C MED for V_{DD} - V_{EE} = 10 volts; and OPAMP C LO for V_{CC} - V_{EE} = 5 volts. For all supply configurations the performance specifications are constant except as noted.

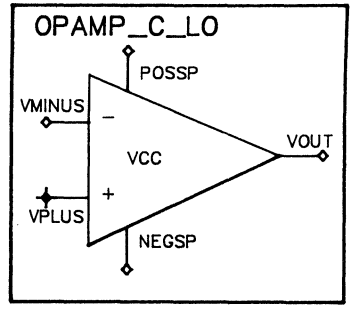
CELL AREA:

133056 Sq. Microns
207 Sq. Mils

SYMBOL:







ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 5V, V_{EE} = −5V, Tj = 25°C)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Input Offset Voltage ($R_S \leq 10K$ Ohms)	V_{OS}		2	5	mV
Input Offset Current	I_{OS}		20	200	nA
Input Bias Current	I_{IB}		170	400	nA
Input Resistance	R_{IN}	150	600		K Ohms
Input Capacitance	C_{IN}		1.4		pF
Input Common Mode Voltage Range	V_{CM}	$V_{CC}-1.1$ $V_{EE}+2.4$	$V_{CC}-0.9$ $V_{EE}+2.2$		V V
Large Signal Voltage Gain (V_O = ±4V, $R_L \geq 8K$ Ohms)	A_{VL}	5	23		V/mV
Output Resistance	R_O		300		Ohms
Common Mode Rejection Ratio ($R_S \leq 10K$ Ohms)	CMRR	63	83		dB
Supply Voltage Rejection Ratio ($R_S \leq 10K$ Ohms)	PSRR		30	150	µV/V
Output Voltage Swing ($R_L \geq 10K$ Ohms)	V_{OUT}	$V_{CC}-0.7$ $V_{EE}+2.1$	$V_{CC}-0.4$ $V_{EE}+1.7$		V V
Supply Current	I_S		1	1.5	mA
Power Consumption*	P_C		10	15	mW
Transient Response Slew Rate (Unity Gain — Non-Inverting) (V_I = 10V, $R_L \geq 10K$ Ohms, $C_L \leq$ 100pF)	SR		3		V/µS
Maximum Output Current	I_O			500	µA
Gain Bandwidth Product	GBW		6		MHz

Power Dissipation is a function of supply configuration.

TYPE D OP AMP

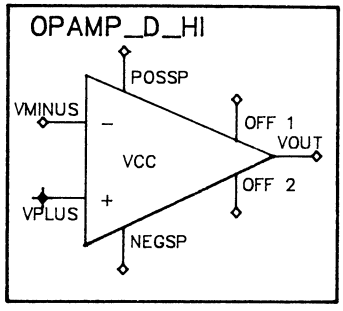
DESCRIPTION:

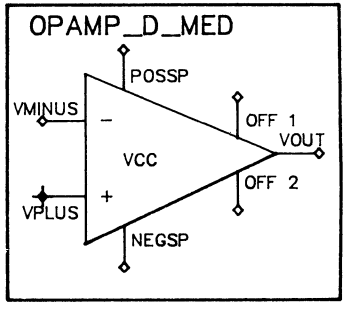
The Type D OPAMP is a 741 architecture, unconditionally stable operational amplifier. If offers high common mode rejection ratio, fast transient response and high drive capability. The maximum output current for the cell is 25mA, making it ideal for driving external loads. The cell can be powered from three different supply configurations: OPAMP D HI for V_{DD} - V_{EE} = 12 volts; OPAMP D MED for V_{DD} - V_{EE} = 10 volts; and OPAMP D LO for V_{CC} - V_{EE} = 5 volts. For all supply configurations the performance specifications are constant except as noted.

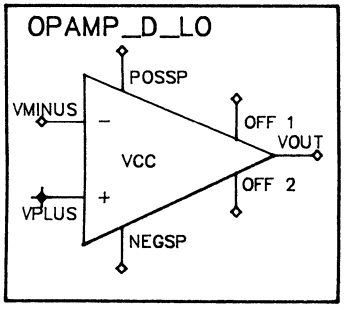
CELL AREA:

286277 Sq. Microns
444 Sq. Mils

SYMBOL:







ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 5V, V_{EE} = −5V, Tj = 25°C)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Input Offset Voltage ($R_S \leq$ 10K Ohms)	V_{OS}		2	5	mV
Input Offset Current	I_{OS}		20	200	nA
Input Bias Current	I_{IB}		150	400	nA
Input Resistance	R_{IN}	200	700		K Ohms
Input Capacitance	C_{IN}		1.4		pF
Input Common Mode Voltage Range	V_{CM}	$V_{CC}-1.1$ $V_{EE}+2.4$	$V_{CC}-0.9$ $V_{EE}+2.2$		V V
Large Signal Voltage Gain (V_O = ±4V, $R_L \geq$ 8K Ohms)	A_{VL}	6	25		V/mV
Output Resistance	R_O		70		Ohms
Common Mode Rejection Ratio ($R_S \leq$ 10K Ohms)	CMRR	80	100		dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10K Ohms)	PSRR		30	150	µV/V
Output Voltage Swing ($R_L \geq$ 10K Ohms)	V_{OUT}	$V_{CC}-0.8$ $V_{EE}+2.3$	$V_{CC}-0.5$ $V_{EE}+2$		V V
Output Short-Circuit Current	I_{OS}		25		mA
Supply Current	I_S		4	5	mA
Power Consumption*	P_C		40	50	mW
Transient Response Slew Rate (Unity Gain — Non-Inverting) (V_I = 10V, $R_L \geq$ 10K Ohms, $C_L \leq$ 100pF)	SR		3		V/µS
Gain Bandwidth Product	GBW		6		MHz

**Power Dissipation is a function of supply configuration.*

VOLTAGE REFERENCES

DESCRIPTION:

The VL1000 Cell Library offers four temperature-compensated, supply-independent voltage references. All four references use a bandgap technique to generate a compensated output voltage. The Brokaw Bandgap, Widlar Bandgap and PTAT Bandgap circuits generate output voltages that are referenced to the most negative supply of the cell. The output voltages of these cells track with variations of the most negative supply. The Widlar 2 Bandgap generates an output voltage that is referenced to the most positive supply of the cell.

CIRCUIT OPERATION:

The Widlar Bandgap is a moderate size cell that can be powered from three supply configurations: $V_{CC} - V_{EE}$ = 5, 10 or 12 volts.

The Brokaw Bandgap is a large cell that offers low power consumption and low output resistance. It also can be powered from three supply configurations: $V_{CC} - V_{EE}$ = 5, 10 or 12 volts. The advantage of the Brokaw Bandgap is that its output voltage is adjustable by the user. The Brokaw Bandgap data sheet gives limitations in the output voltage adjustability.

The PTAT Bandgap is a small cell that uses a PTAT current generator to create a bandgap output voltage. It can be powered from three supply configurations: $V_{CC} - V_{EE}$ = 5, 10 or 12 volts.

The Widlar 2 Bandgap offers the smallest cell size of all the reference cells. Its output voltage is referenced to the most positive supply voltage.

Output voltage, output resistance, and quiescent current figures shown in the following table are typical values with Tj = 25°C.

BANDGAP TYPE	*CELL AREA (mil²)*	*OUTPUT VOLTAGE (V)*	*OUTPUT RESISTANCE (Ohms)*	*QUIESCENT CURRENT (mA)*	*OUTPUT VOLTAGE REFERENCE SUPPLY*
WIDLAR	207	1.24	2	2	Negative
BROKAW	280	Adjustable	0.5	0.65	Negative
PTAT	157	1.21	30	2	Negative
WIDLAR 2	110	1.33	370	1	Positive

WIDLAR BANDGAP

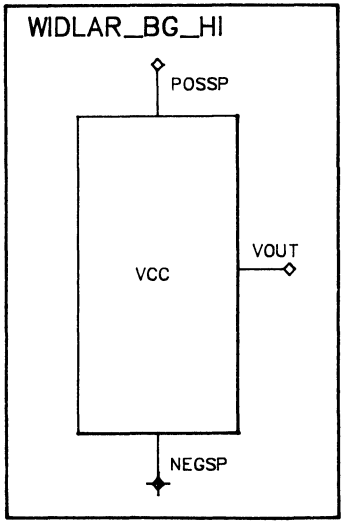
DESCRIPTION:

The Widlar Bandgap cell is a temperature-compensated voltage reference. The circuit offers low output resistance, low power consumption and a moderate cell area. There are two versions of the Widlar Bandgap cell resident in the VL1000 Cell Library. The WIDLAR BANDGAP LO is used when the cell is powered from the V_{CC} - V_{EE} = 5 volt supply configuration. The WIDLAR BANDGAP HI is used with the V_{DD} - V_{EE} = 10 volt or 12 volt supply configuration. For both versions, the performance specifications are constant. The output voltage of the circuit tracks with variations in the most negative supply of the cell.

CELL AREA:

133056 Sq. Microns
207 Sq. Mils

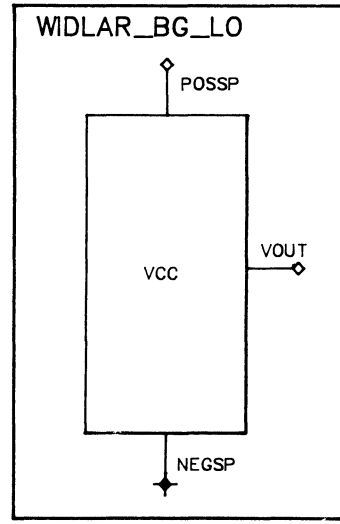
SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 5V, Tj = 25°C)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Voltage (I_O = 0mA) (Referenced to Power Bus on Chip)	V_o	1.22	1.24	1.26	V
Output Voltage Temperature Coefficient (0°C≤T≤100°C)	$\Delta V_o/\Delta T$		32	64	ppm/°C
Maximum Output Voltage Change (0°C≤T≤100°C)	V_{OC}		4	8	mV
Line Regulation (4.5V≤V_{CC}≤5.5V, I_o = 0mA)	V_{REG}		2	5	mV
Supply Current (I_o = 0mA)	I_S		2	2.5	mA
Output Resistance	R_o		2		Ohms
Maximum Output Current	I_o			1.5	mA



BROKAW BANDGAP

DESCRIPTION:

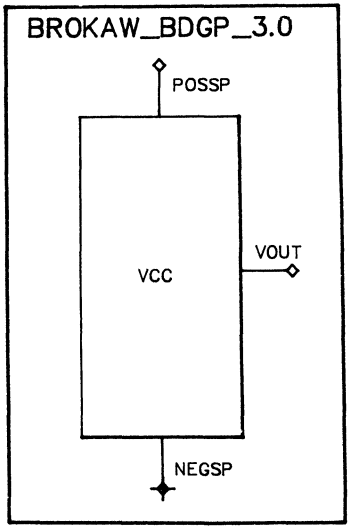
The Brokaw Bandgap is a temperature-compensated voltage reference with variable output. The cell offers low output resistance, low power consumption and good output voltage line regulation. The Brokaw Bandgap can be powered from three different supply configurations: V_{DD} - V_{EE} = 12 volts; V_{DD} - V_{EE} = 10 volts; and V_{CC} - V_{EE} = 5 volts. The output voltage of the circuit tracks with variations in the most negative supply of the cell.

To adjust the output voltage of the cell, the user must change the value of the VBG property located on the symbol for the cell. The default value for this property is 3.0. The value of this property will be the output voltage of the cell. For V_{DD} - V_{EE} = 12 volts or V_{DD} - V_{EE} = 10 volts, the maximum output voltage for the cell is 5 volts and the minimum output voltage is1.6 volts. Any value between these two extremes is acceptable. For V_{CC} - V_{EE} = 5 volts, the maximum and minimum output voltages are 2.2 and 1.6 volts respectively.

CELL AREA:

181440 Sq. Microns
282 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

*(Unless otherwise specified, V_{CC} = 10V, Tj = 25°C, V_{OUT} = 3V)					
CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Voltage (I_O = 0mA) (Referenced to Power Bus on Chip)	V_O	2.94	3	3.06	V
Output Voltage Temperature Coefficient (0°C≤T≤100°C)	$\Delta V_O/\Delta T$		32	64	ppm/°C
Maximum Output Voltage Change (0°C≤T≤100°C)	V_{OC}		9.5	19	mV
Line Regulation (9V≤V_{CC}≤11V, I_O = 0mA)	V_{REG}		2	5	mV
Supply Current (I_O = 0mA)	I_S		1.45	1.9	mA
Output Resistance	R_O		0.5		Ohms
Maximum Output Current	I_O			1.2	mA

**For all supply configurations the performance specifications are constant.*

PTAT BANDGAP

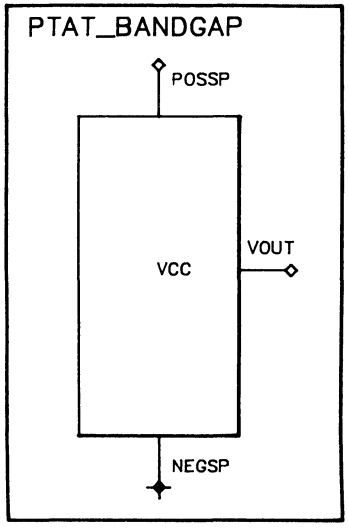
DESCRIPTION:

The PTAT Bandgap is a temperature-compensated voltage reference. The circuit generates a bandgap output voltage by using a PTAT current reference and offers a small cell size. The PTAT Bandgap can be powered from three different supply configurations: V_{DD} - V_{EE} = 12 volts; V_{DD} - V_{EE} = 10 volts; and V_{CC} - V_{EE} = 5 volts. For all supply configurations the performance specifications are constant. The output voltage of the circuit tracks with variations in the most negative supply of the cell.

CELL AREA:

100800 Sq. Microns
152 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 10V, Tj = 25°C)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Voltage (I_o = 0mA) (Referenced to Power Bus on Chip)	V_o	1.18	1.21	1.24	V
Output Voltage Temperature Coefficient (0°C≤T≤100°C)	$\Delta V_o/\Delta T$		32	64	ppm/°C
Maximum Output Voltage Change (0°C≤T≤100°C)	V_{OC}		4	8	mV
Line Regulation (9V≤V_{CC}≤11V, I_o = 0mA)	V_{REG}		2	4	mV
Supply Current (I_o = 0mA)	I_S		2	2.5	mA
Output Resistance	R_o		30		Ohms
Maximum Output Current	I_o			1.2	mA

WIDLAR 2 BANDGAP

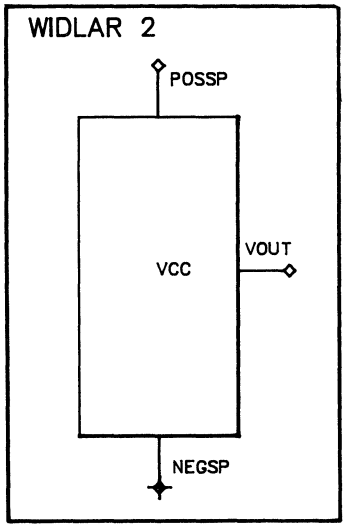
DESCRIPTION:

The Widlar 2 Bandgap is a temperature-compensated voltage reference. The cell offers low power dissipation and a small layout area. The Widlar 2 Bandgap is designed to operate from a nominal supply configuration of V_{DD} - V_{EE} = 10 or 12 volts. The output voltage of the circuit tracks with variations in the most positive supply of the cell.

CELL AREA:

70560 Sq. Microns
110 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 10V, Tj = 25°C)					
CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Voltage (I_o = 0mA) (Referenced to Power Bus on Chip)	V_o	1.30	1.33	1.36	V
Output Voltage Temperature Coefficient (0°C≤T≤100°C)	$\Delta V_o/\Delta T$		32	64	ppm/°C
Maximum Output Voltage Change (0°C≤T≤100°C)	V_{oc}		4.2	8.4	mV
Line Regulation (9V≤V_{cc}≤11V, I_o = 0mA)	V_{REG}		5	10	mV
Supply Current (I_o = 0mA)	I_S		1	1.3	mA
Output Resistance	R_o		370		Ohms
Maximum Output Current	I_o			0.3	mA

CURRENT REFERENCES

The VL1000 Cell Library offers four different current reference cells: 1) The BANDGAP CURRENT SOURCE is a large, low-power cell intended as a DAC bias circuit. The cell can operate from nominal voltages V_{DD} - V_{EE} = 10 or 12 volts; 2) The EXTERNAL ZENER REFERENCE is a small cell that offers a user-adjustable temperature- and voltage-compensated output current. An external resistor sets the output current value. This circuit can operate from a nominal supply voltage of V_{DD} - V_{EE} = 12 volts; 3) The PTAT CURRENT REFERENCE is a small cell that generates a proportional-to-absolute-temperature output current. This type of cell can be useful when designing bandgap voltage references or temperature-stabilized differential amplifiers. This circuit can operate from nominal supply voltages of V_{CC} - V_{EE} = 5, 10 or 12 volts; 4) The ZENER CURRENT REFERENCE is a small cell that generates a voltage and temperature-compensated output current. The cell can operate from nominal supply voltages of V_{DD} - V_{EE} = 10 or 12 volts.

All of the current references, except the BANDGAP CURRENT SOURCE, rely on the designer to use a current mirroring technique to obtain the final output current. This technique allows the designer to set the nominal value of the output current, while at the same time utilizing the basic temperature and voltage characteristics of the cell. For consistent results the output transistor supplied by the designer should be the same type as the mirroring transistor in the cell. All current ratioing should be done using different size emitter resistors in the output stage. The output stage emitter resistor should be the same type and the same width as the emitter resistor in the mirroring stage. This insures that the proper temperature characteristics will be exhibited by the circuit and that consistent nominal output currents will result.

On the following data sheets all values given assume the circuit is connected in a 1-to-1 mirror output configuration. The typical application diagram should be used to help the user pick the proper mirroring components for consistent results.

BANDGAP CURRENT SOURCE

DESCRIPTION:

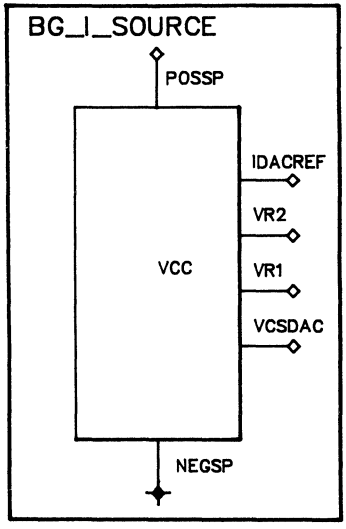
The BANDGAP CURRENT SOURCE is a large cell intended to be used as a digital-to-analog-convertor bias generator. For details on how to use the cell in this way, refer to the typical applications diagram. The cell can be operated from nominal supply voltages of V_{DD} - V_{EE} = 10 or 12 volts. For either case the specifications quoted are the same.

The nominal value of the output current of the cell will vary directly with the base sheet resistance. Because of this direct relationship, the output current of the cell should be forced across a base type resistor. In this way a process independent output voltage will result. The base resistor that generates the output voltage should have a width of 11 microns. This insures good resistor matching between the output resistor and the resistor internal to the cell.

CELL AREA:

157248 Sq. Microns
244 Sq. Mils

SYMBOL:

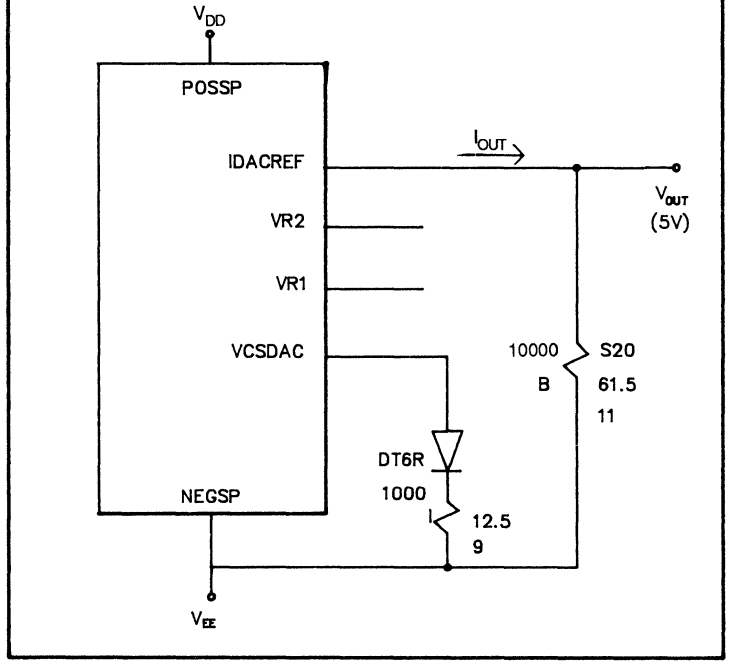


ELECTRICAL CHARACTERISTICS:

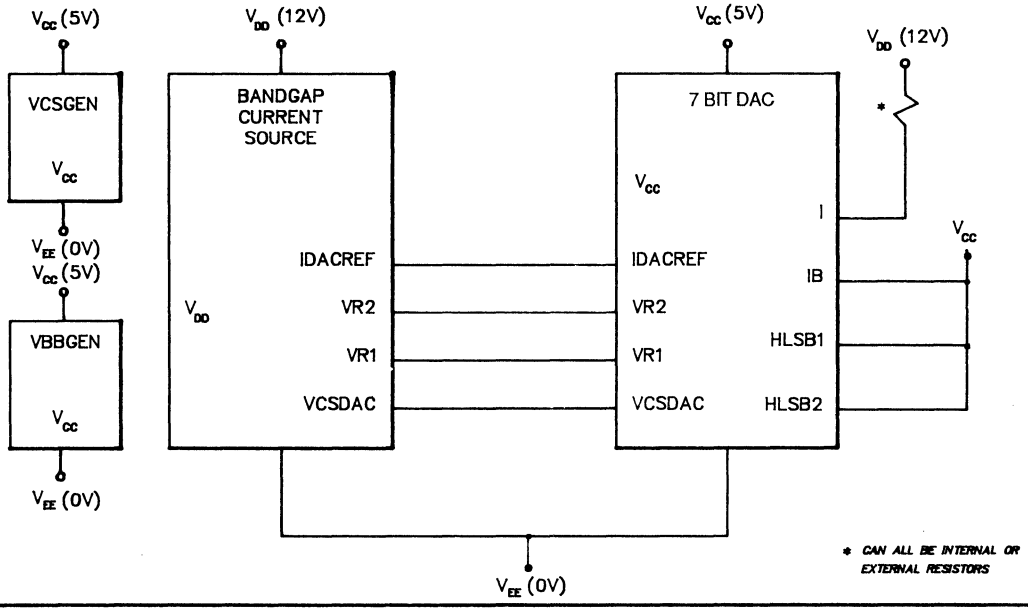
(Unless otherwise specified, V_{DD} = 10V, V_{EE} = 0V, Tj = 25°C)					
CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Current (VCSDAC = 1.05V) (Note 1)	I_{OUT}	400	500	600	µA
Output Voltage (As Shown in Test Diagram)	V_{OUT}	4.75	5	5.25	V
Output Current Temperature Coefficient (0°C≤Tj≤100°C)	$\Delta I_{OUT}/\Delta T$		250	350	ppm/°C
Maximum Output Current Change (0°C≤Tj≤100°C)	ΔI_{OUT}		6	8.5	µA
Line Regulation (9V≤V_{CC}≤11V)	I_{REG}		6	10	µA
Supply Current	I_{CC}		0.7	0.9	mA

Note 1: Output current will vary directly with base sheet resistance.

FIGURE 1: TEST DIAGRAM



TYPICAL APPLICATION:



EXTERNAL ZENER REFERENCE

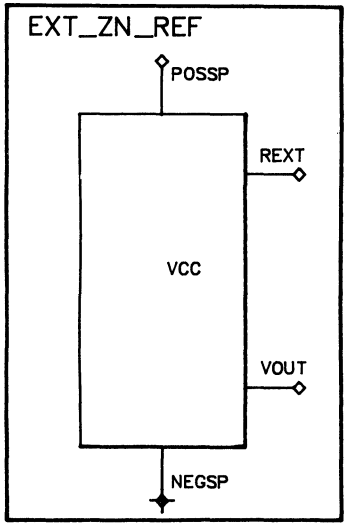
DESCRIPTION:

The EXTERNAL ZENER REFERENCE is a small cell that offers the ability to externally control the output current of the circuit. The cell operates from a nominal supply voltage of V_{DD} - V_{EE} = 12 volts. The cell also offers a wide range in possible output current of 2.5mA to 6mA. As explained in the general description, a mirroring technique must be employed to generate the output current. A typical application is shown below.

CELL AREA:

68544 Sq. Microns
107 Sq. Mils

SYMBOL:

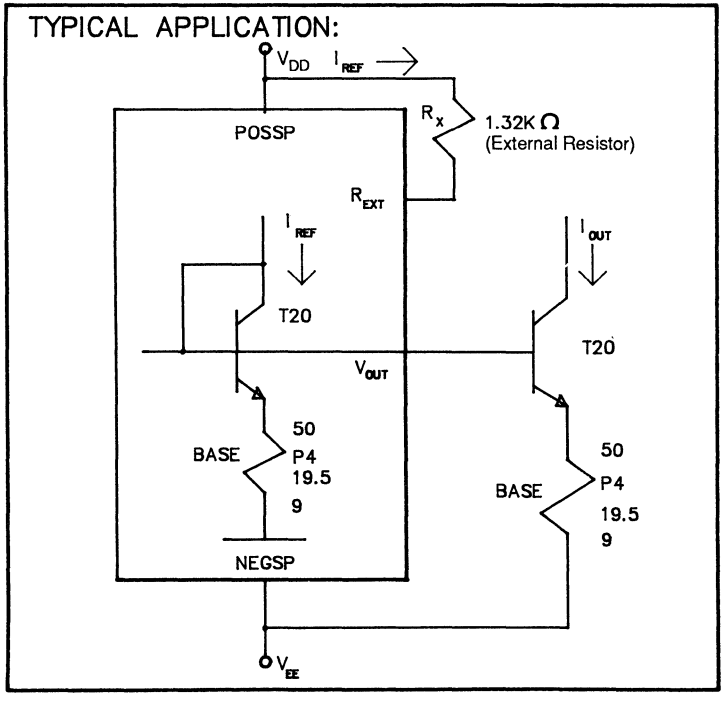


ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD}= 10V, V_{EE} = 0V, Tj = 25°C)
(Circuit is Connected in a 1-to-1 Mirror Output)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Current (R_x = 1.32K Ohms) (Note 1)	I_{OUT}	4.95	5	5.05	mA
Output Current Compliance (Error ≤ ±2.5%)	V_{O+}		V_{CC}		V
	V_{O-}		V_{EE} + 1		V
Adjustable Reference Current Range	I_{REF}	2.5		6	mA
Output Current Temperature Coefficient (0°C≤Tj≤100°C)	$\Delta I_{OUT}/\Delta T$		20	50	ppm/°C
Maximum Output Current Change (0°C≤Tj≤100°C)	ΔI_{OUT}		10	25	µA
Line Regulation (10.8V≤V_{CC}≤13.2V)	I_{REG}		40	60	µA
Supply Current (R_x = 1.32K Ohms) (Note 2)	I_{CC}		10.2	13.3	mA

Note 1: When connected in a 1-to-1 mirror output, $I_{REF} = I_{OUT} = 6.59/R_X$.
Note 2: When connected in a 1-to-1 mirror output, $I_{CC} = [2(I_{REF}) + 0.2]$mA.



PTAT CURRENT REFERENCE

DESCRIPTION:

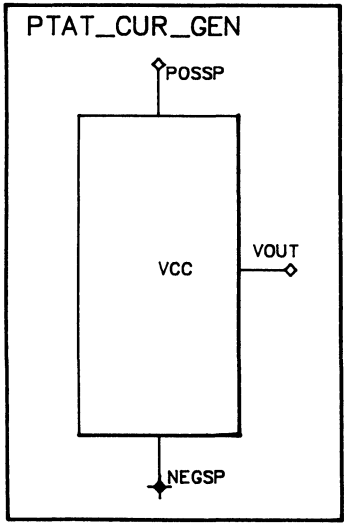
The PTAT CURRENT REFERENCE is a small cell that generates a proportional-to-absolute-temperature output current. This type of current is useful when the user is designing bandgap voltage references, temperature compensated differential amplifiers, or other temperature compensated circuits. The cell can operate from nominal supply voltages of $V_{CC} - V_{EE}$ = 5, 10 or 12 volts. As explained in the general description, a mirroring technique must be employed to generate the output current.

The nominal output current of the cell and mirror will vary directly with the base sheet resistance. When designing a temperature-compensated circuit with this cell, the designer should be sure that all critical resistors in the circuit are base resistors with a width of 9 microns. This will insure proper temperature characteristics and consistent performance from part to part. A typical application is shown below. The nominal output voltage V_{REF} is a process independent circuit characteristic.

CELL AREA:

70560 Sq. Microns
110 Sq. Mils

SYMBOL:

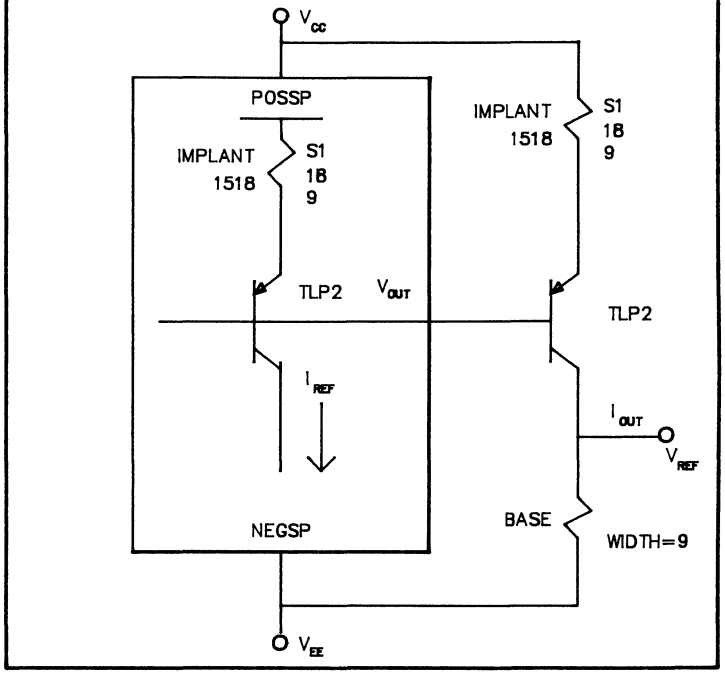


ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 5V, V_{EE} = 0V, Tj = 25°C)
(Circuit is Connected in a 1-to-1 Mirror Output)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Current	I_{OUT}	200	220	240	µA
Output Current Compliance (Error ≤ ±3%)	V_{O+}		$V_{CC}-2$		V
	V_{O-}		V_{EE}		V
Output Current Proportionality Constant (0°C≤Tj≤100°C)	K	0.6	0.67	0.7	µA/°K
Proportionality Constant Temperature Coefficient (0°C≤Tj≤100°C)	ΔK/ΔT		1000	1500	ppm/°K
Line Regulation (4.5V≤V_{CC}≤5.5V)	I_{REG}		2	4	µA
Supply Current	I_{CC}		0.65	0.85	mA

TYPICAL APPLICATION:



ZENER CURRENT REFERENCE

DESCRIPTION:

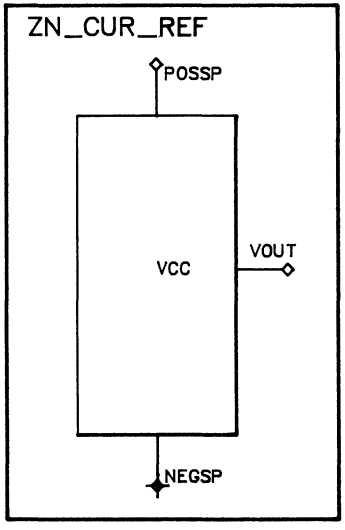
The ZENER CURRENT REFERENCE is a small cell that uses a zener diode to generate a temperature- and supply-independent output current. The cell can operate from a nominal supply voltage of V_{DD} - V_{EE} = 10 or 12 volts. As explained in the general description, a mirroring technique must be employed to generate the output current.

The nominal output current of the mirror will vary directly with the implant sheet resistance. When using this cell, all critical resistors external to the cell and mirror should be implant resistors with a width of 7 microns. This will insure proper temperature characteristics and consistent performance from part to part. A typical application is shown below. The nominal output voltage V_O is a process independent circuit characteristic.

CELL AREA:

68544 Sq. Microns
107 Sq. Mils

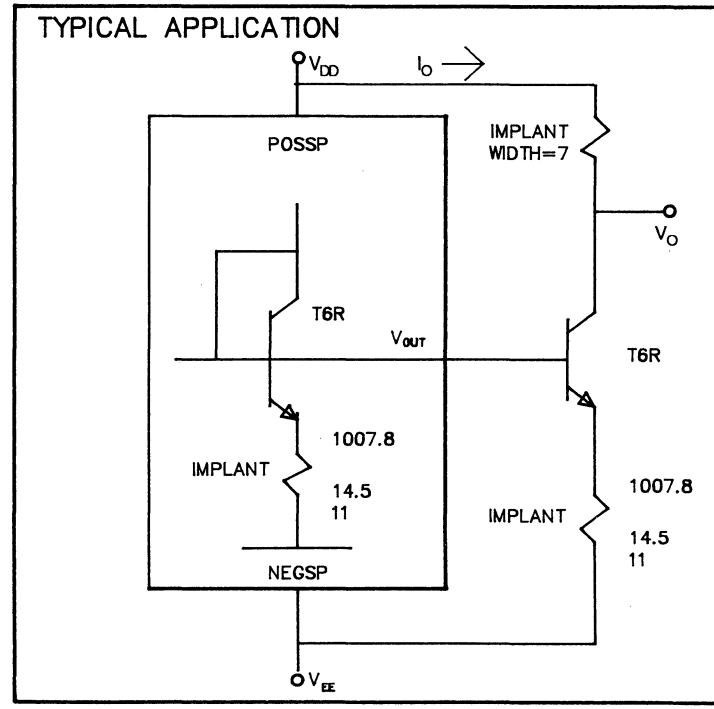
SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 10V, V_{EE} = 0V, Tj = 25°C)
(Circuit is Connected in a 1-to-1 Mirror Output)

CHARACTERISTIC	*SYM.*	*MIN.*	*TYP.*	*MAX.*	*UNIT*
Output Current	I_{OUT}	170	190	210	µA
Output Current Compliance (Error ≤ ±2.5%)	V_{O+}		V_{CC}		V
	V_{O-}		$V_{EE}+1$		V
Output Current Temperature Coefficient (0°C≤Tj≤100°C)	$\Delta I_{OUT}/\Delta T$		150	225	ppm/°C
Maximum Output Current Change (0°C≤Tj≤100°C)	ΔI_{OUT}		4	8	µA
Line Regulation (9V≤V_{CC}≤11V)	I_{REG}		0.5	1	µA
Supply Current	I_{CC}		0.8	1.1	mA



VOLTAGE COMPARATORS

The VL1000 Cell Library offers two voltage comparator cells. First, the CML COMPAT COMPAR comparator cell provides fast propagation delays and CML output voltage levels. This cell requires that the VCS CML voltage reference level is available on the chip. Second, the COMPARATOR 339 comparator cell is a general purpose comparator which provides multiple power supply operation, a large input range and an open collector output. A summary of the electrical performance for these two comparators is given in the table below. All figures are typical values at Tj = 25°C.

TYPE	*CELL AREA (mil²)*	*ICC (mA)*	*IN-PUT RES. (Ohms)*	*PROPA-TATION DELAY (nS)*	*VCC-VEE (Volts)*	*OUT-PUT DRIVE*	*INPUT VOLT. RANGE*
CML Compat Compar	154	1	100K	10	5	10 Gates	$V_{CC}-1.9$ $V_{EE}+1.7$
339 Com-parator	147	0.5*	50M	800	5, 10 or 12	2 mA	$V_{CC}-1.5$ $V_{EE}-0.2$

**Not including output stage current.*

CML COMPATIBLE COMPARATOR

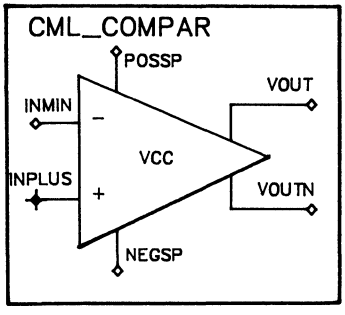
DESCRIPTION:

The CML Compatible Comparator is a high speed comparator with complementary CML outputs. The output of the comparator is centered around the VBB1 reference level, making it compatible with all CML gates. The cell requires the VCS reference voltage from the CML bias generator. The nominal supply configuration for the cell is V_{CC}-V_{EE} = 5 volts. The cell is designed to exhibit 5mV of hysteresis on the inputs for cleaner switching and shorter output rise and fall times.

CELL AREA:

98784 Sq. Microns
154 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 5V, V_{EE} = OV, Tj = 25°C)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Input Offset Voltage	V_{IO}		1.5	5	mV
Input Offset Current	I_{IO}		125	800	nA
Input Bias Current	I_{IB}		2	5	µA
Input Common Mode Voltage Range	V_{ICR}	$V_{CC}-2.0$ $V_{EE}+1.8$	$V_{CC}-1.9$ $V_{EE}+1.7$		V V
Voltage Gain	A_V		0.75		V/mV
Propagation Delay Time V_{IN} = 600mV, F_{OUT} = 2	t_{PD}		12	19	nS
Loading Factor	t_{LF}		1	2	nS/Gate
Output Rise Time V_{IN} = 600 mV, I_{OUT} = OmA (10-90%)	t_{RO}		2	4	nS
Input Resistance	R_{IN}	25	100		KOhms
Maximum Output Fanout (High Power Gates)	F_{OUT}			10	Gates
Supply Current	I_{CC}		1	1.3	mA

COMPARATOR 339

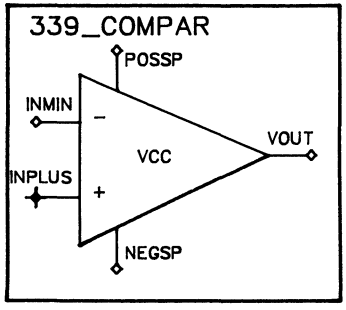
DESCRIPTION:

The 339 Comparator is a low-power, general-purpose comparator. Depending on the application, the 339 Comparator can operate from supply configurations of VDD - VEE = 12 volts, 10 volts or 5 volts with constant performance specifications. The comparator's common mode input range includes the most negative supply of the cell, making the circuit useful in applications where low-level input voltage sensing is necessary. The cell has an open collector output allowing the user to customize the output characteristics of the circuit.

CELL AREA:

94752 Sq. Microns
147 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{CC} = 5V, V_{EE} = OV, Tj = 25°C)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Input Offset Voltage	V_{IO}		3	6	mV
Input Offset Current	I_{IO}		5	50	nA
Input Bias Current (NOTE 1)	I_{IB}		25	250	nA
Input Common Mode Voltage Range	V_{ICR}	$V_{CC}-1.7$ $V_{EE}-0.1$	$V_{CC}-1.5$ $V_{EE}-0.2$		V V
Voltage Gain	A_V	5	20		V/mV
Propagation Delay Time V_{IN} = 600 µV, I_{OUT} = OmA	t_{PD}		800	1600	nS
Output Rise Time V_{RL} = 5V, R_L = 5.1K Ohms, 10-90%	t_{RO}		2	4	nS
Input Resistance	R_{IN}	5	50		M Ohms
Output Saturation Voltage $V_{IN-} \geq 1V$, V_{IN-} = OV, $I_{SINK} \leq 2mA$	V_{OL}		320	450	mV
Output Leakage Current V_{IN-} = OV, $V_{IN+} \geq 1V$, V_O = 5V	I_{OL}		0.1		µA
Maximum Output Sink Current	I_{SINK}			2	mA
Supply Current	I_{CC}		0.5	0.65	mA

NOTE 1: Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.

WIDEBAND AMPLIFIERS

VIDEO AMP 733

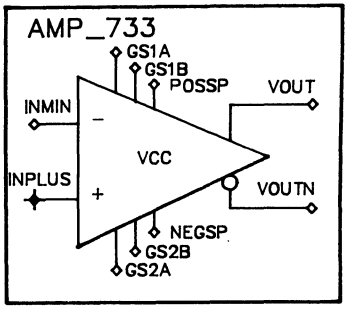
DESCRIPTION:

The 733 Video Amplifier is a two-stage differential input, differential output, wideband video amplifier. The cell can be configured for gain values of 400, 100 or 10. For all configurations the circuit requires no external frequency compensation. It offers low output impedance, low input referenced noise voltage and a wide bandwidth at all gain levels. The cell can be operated from supply configurations of V_{DD} - V_{EE} = 10 volts or 12 volts.

CELL AREA:

189504 Sq. Microns
294 Sq. Mils

SYMBOL:



ELECTRICAL CHARACTERISTICS:

(Unless otherwise specified, V_{DD} = 6V, V_{EE} = −6V, T_j = 25°C)

CHARACTERISTIC	*SYM*	*MIN*	*TYP*	*MAX*	*UNIT*
Differential Voltage Gain (R_S = 50 Ohms, R_L = 2K Ohms, V_O = 3Vpp)	A_V				
Gain 1 (Note 1)		250	400	600	V/V
Gain 2 (Note 2)		80	100	120	V/V
Gain 3 (Note 3)		8	10	12	V/V
Bandwidth (R_S = 50 Ohms, $C_L \leq$ 1pF) (Driving on Chip Load)	BW				
Gain 1			120		MHz
Gain 2			125		MHz
Gain 3			130		MHz
Rise Time (R_S = 50 Ohms, V_O = 1Vpp)	t_R				
Gain 1			5		nS
Gain 2			4	10	nS
Gain 3			2.5		nS
Propagation Delay (R_S = 50 Ohms, V_O = 1Vpp)	t_{PD}				
Gain 1			2.5		nS
Gain 2			2.2	6	nS
Gain 3			2		nS
Input Resistance	R_{IN}				
Gain 1			1.7		K Ohm
Gain 2		5	8		K Ohm
Gain 3			80		K Ohm
Input Capacitance	C_{IN}				
Gain 1			12		pF
Gain 2			10		pF
Gain 3			4		pF
Input Offset Current	I_{IO}		6	60	μA
Input Bias Current	I_{IB}		40	320	μA
Input Noise Voltage (R_S = 50 Ohms, BW = 1KHz to 10MHz)	b_{IN}				
Gain 1			0.7		nV/√Hz
Gain 2			2		nV/√Hz
Gain 3			7		nV/√Hz
Input Voltage Range	V_{IR}	±1			V
Common-Mode Rejection Ratio	CMRR				
Gain 2 (V_{CM} = ±1V, f ≤ 100KHz)		60	85		dB
Gain 2 (V_{CM} = ±1V, f = 5MHz)			60		dB
Output Common-Mode Voltage	V_{OCR}		3	3.4	V
Output Voltage Swing (R_L = 2K Ohm)	V_{OS}	3	4		Vpp
Output Sink Current	I_{SINK}			3	mA
Output Resistance	R_O		13		Ohms
Power Supply Current	I_{CC}		15		mA
Power Supply Rejection Ratio	PSRR	50	70		dB
Output Offset Voltage	V_{OS}				
Gain 1			0.6	1.5	V
Gain 2 and 3			0.35	1	V

NOTE 1: Pins GS1A and GS1B connected together.
NOTE 2: Pins GS2A and GS2B connected together.
NOTE 3: Gain Select pins open.

VL1000 DIGITAL CELL DESIGN GUIDELINES

INTRODUCTION

This section of the VL1000 User's Guide explains the special considerations a designer must understand in order to successfully define a working digital circuit using the VL1000 Linear Bipolar Cell Library. It is divided into four subsections that discuss the CML logic family, bias generators, power supply conventions and I/O buffers. (Refer to VTC Design Note-4, "Current Mode Logic," for further information.)

CML LOGIC FAMILY, GENERAL CONSIDERATIONS

Current Mode Logic (CML) is the basis for all internal digital logic cells in the VL1000 Cell Library. CML logic provides a relatively high performance level, and convenient interface to the linear cells also supported in the library.

A basic CML combinational logic schematic is shown in Figure 2-1. This schematic shows all of the principals needed for a user to understand and begin design with CML logic. There are three levels of "series gated" logic available in this implementation of CML. They are referred to respectively as levels A, B, and C, proceeding from levels with most positive to most negative voltages. These logic levels will uniformly switch to the "1" and "0" states above and below three successive reference levels named VBB1, VBB2 and VBB3.

A convention established in this cell library is that all outputs of logic gates are on level "A". If it is necessary to switch from one level to another, that function is performed automatically after the input of the following gate. In the example schematic Figure 2-1, a 2-input OR/NOR gate has an inverting, level A output at the collector of transistor Q13. This output feeds directly to the level A input of a 3-input AND/NAND at transistor Q1. The transistor is an emitter-follower lying within the AND/NAND logic cell, and is driven by a current source, translating the signal down through diode D1 to level C logic for proper operation of the gate. The result is, for purposes of design simplicity, the interconnections between internal logic cells are always on level A, and the designer does not have to worry about incorrectly connecting two incompatible logic levels. If special cases arise (such as flip-flop clock inputs) where it is more efficient to fanout at the B or C level, those inputs are identified with one or two asterisks respectively in the cell symbols.

It is only necessary to be concerned about logic levels when entering or leaving the chip through I/O buffers or when interfacing logic with linear circuitry (discussed in the linear cell data sheets). Again, a more extensive treatment of CML logic design is available for interested users in the VTC CML Logic Design Note.

D.C. OPERATING CONDITIONS

A feature of the VL1000 Cell Library is that the designer has the freedom to trade speed for power dissipation as required in the design. Three power levels are available for all logic gates, identified as high (H), medium (M) and low (L). The three power levels allow a designer to improve performance on critical paths, while conserving power on non-critical paths.

From an operational standpoint, the user may change freely from one power level to the next with only one concern: The total equivalent DC fanout load for any output may not exceed 10. Table 2-1 presents the equivalent DC fanout load that any input at a specific power level represents to an output at each power level. For fanout greater than 10, a special cell (SIGBUF) is available.

TABLE 2-1: D.C. FANOUT LOADING

Output Power Level	*INPUT POWER LEVEL* *High*	*Medium*	*Low*
High	1.0	0.5	0.25
Medium	2.0	1.0	0.5
Low	4.0	2.0	1.0

*The value show in the table is the proportion of a unit load that an input pin represents to an output pin, each at specific power levels.
*In no case may the total equivalent DC load of a given output exceed 10 unit loads.

Table 2-2 shows the nominal current source value along with the typical power dissipation for each of the three power levels, for a two input ORNOR gate (CELL NAME = ORNOR2). This information is useful in comparing the tradeoffs between speed, power, and total current. The power dissipation is given for reference in the data sheets for every VL1000 standard cell. Since all CML gates are powered from a differential supply voltage that is nominally 5V, total current for the digital section of the chip may be estimated by dividing the total power dissipation of a design by 5V.

TABLE 2-2: D.C. CURRENT AND POWER DISSIPATION ORNOR2 CML GATE

	POWER LEVEL *High*	*Medium*	*Low*
Cell Current	450 μA	225 μA	113 μA
Power Diss.	2.25 mW	1.13 mW	0.56 mW

Table 2-3 shows the nominal design values for internal logic and logic reference voltage levels. The reference values represent voltages that are ¼ diode drop below V_{CC} for the A level, 1¼ diode drops for the B level, and 2¼ diode drops for the C level. Note the actual values depend upon the voltage selected for the V_{CC} supply.

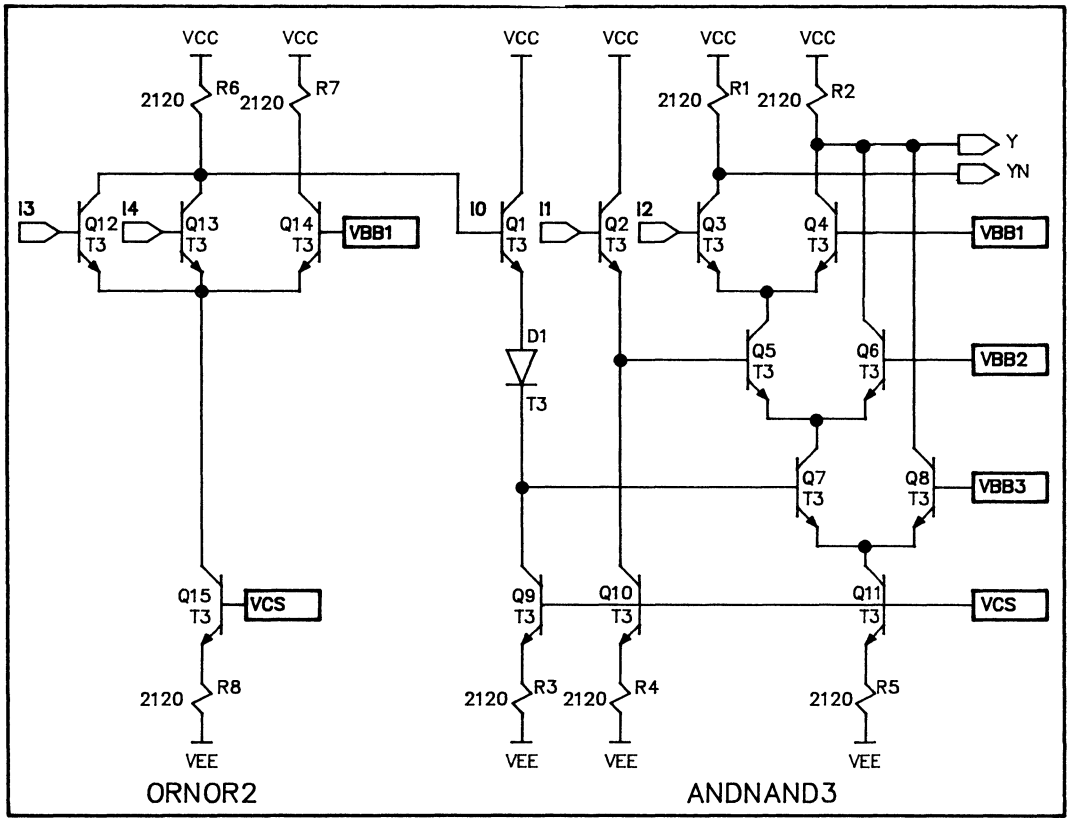
TABLE 2-3: LOGIC AND REFERENCE LEVELS INTERNAL CML LOGIC

(Conditions: V_{CC} = +5.0 V, V_{EE} = Gnd)
TEMP = 25 DEG. C.

Logic Level	*I/O Voltage*	*Reference Voltage*
A	HIGH (1) = 5.0 LOW (0) = 4.6	REF. = 4.8
B	HIGH (1) = 4.2 LOW (0) = 3.8	REF. = 4.0
C	HIGH (1) = 3.4 LOW (0) = 3.0	REF. = 3.2

Note: Internal Logic and Logic Reference Voltages are referenced from V_{CC}, and will remain so under all values of V_{CC}.

Figure 2-1: CML Logic Schematic



A.C. OPERATING CONDITIONS

The VL1000 cell library data sheets included in the User's Guide detail the expected performance of each of the CML gates for power, chip area, function, and propagation delay. Propagation delay in CML logic is sensitive to many parameters. These include environmental conditions, such as power supply voltage and temperature; processing variations such as transistor beta, resistor value, doping concentrations, epitaxial thickness, and oxide thickness; and design variables such as fanout and metal capacitance of the interconnect. Detail simulations of the effects of the variables, as well as actual data under controlled conditions, have been factored into the propagation delay information in the data sheets to provide numbers that are indicative of the extremes that could result from the various combinations of the above mentioned factors.

As it is impractical to specify a complete matrix of expected delay numbers for all of these factors, and inasmuch as many of the factors do not contribute significantly to variation in delay compared to others, a summarized table is shown for each of the digital functions, for delay paths of most critical interest. The user can be assured when using the digital logic simulator, minimum and maximum delay information accounts for the extreme combinations that could occur in actual practice.

There are several degrees of freedom available to the more sophisticated user of logic simulators, and the VL1000 Cell Library digital cell delay files are designed to allow as much flexibility in critical path analysis as desired. Specifically, it provides the user with the ability to vary the following parameters: (a.) fanout, (b.) power, and (c.) to select one of three combinations of process and environmental extremes that are as follows: minimum delay, which occurs at low temperature, with low resistors, high voltage, and high beta; maximum delay, occuring at high temperature, with high resistors, low voltage, and low beta; and a nominal delay, that occurs with nominal or average values for the same parameters.

The data presented in the data sheets show minimum, typical and maximum as listed above, with the additional conditions of:

a. fanout of 2 unit AC loads.
b. estimated average metal line-length equal to 50 mils of metal.

The fanout factor shown in the digital data sheets is used to more accurately predict logic simulation results. During a logic simulation run, the actual delay is calculated by adding the delay due to fanout to the delay assuming zero fanout. The equation is shown below:

Gate Delay (no load) + (# AC unit loads) * (fanout factor) = prop. delay

Most input pins represent an equivalent AC unit load of 1. If the AC load is different than 1, it is shown on that input pin on the Mentor symbol.

The logic simulator automatically accounts for actual fanout before the logic simulation is run. The metal line length is fixed for the purposes of simulation, and there is currently no provision for simulation based on actual metal line length after layout is complete. For critical path analysis on a limited number of paths, provisions may be made with VTC for special delay analysis after routing. Since layout is under the control of VTC, special layout requirements can be accommodated in order to keep critical path nets as short as possible during layout.

BIAS GENERATORS

Required elements in CML logic design include the bias generator circuits that set the reference levels for the logic comparison, and control the current in the logic cells. There are two sections for the CML bias generator. The master bias generator (VCSGEN) provides the V_{CS} reference that controls all currents on the digital section of the chip. This reference voltage is connected to all digital cells on the chip. The Slave bias generator (VBBGEN) provides three logic comparison reference levels for internal logic at the A, B, and C levels (referred to as VBB1, VBB2, and VBB3 respectively). A completed chip will have one VCSGEN and one or more VBBGEN. The number of VBBGEN cells required is a function of the number of logic cells used. Two versions of the VBBGEN cell are provided. The desired version is selected through the FOUT property on the VBBGEN cell. The options are HIF and LOF. The HIF version is the default. It can drive 40 high, 80 medium, or 160 low power gates. The LOF version can drive 20 high, 40 medium, or 80 low power gates.

The correct number of VBBGEN cells must be placed in the schematic and connected to the power supplies. This is necessary for correct completion of layout, and for proper SPICE simulation. A single VCSGEN cell must also be properly placed in the schematic for the same reasons.

There is one more bias generator, named BIASGEN10K. The purpose of this generator is to provide the proper reference levels for the ECL input and output buffers. This cell must be used with the BUFIN10K, BUFOUT10K, and POSNEGSHFT cells.

POWER SUPPLY CONVENTIONS

There are three power supply names available in the VL1000 Cell Library: V_{DD}, V_{CC} and V_{EE}. The conventions established for allowable values for these power supplies is discussed in the section titled Mentor Instructions, Power Supply Conventions.

There are some special considerations in using the I/O buffers and gates, with regard to the power supplies. These considerations are demonstrated in Table 4.1.

TABLE 4.1: POWER SUPPLY SELECTION, AND LOGIC — I/O BUFFER INTERFACING

POWER SUPPLIES USED			*LOGIC LEVEL INTERFACING*			*POSITIVE SUPPLY*
V_{DD}	V_{CC}	V_{EE}	*TTL I/O*	*CML*[NOTE 1]	*ECL I/O*[NOTE 1]	VP_{OS}
+5.0	0.0	−5.2	+5.0; 0.0	+5.0; 0.0	0.0; −5.2	V_{DD}[NOTE 2]
N/A	0.0	−5.2	N/A	0.0; −5.2	0.0; −5.2	V_{CC}
N/A	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	+5.0; 0.0	V_{CC}
N/A	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	N/A	V_{CC}
+12.0	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	+5.0; 0.0	V_{CC}
+10.0	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	+5.0; 0.0	V_{CC}

NOTE 1: This includes the associated bias generators.
NOTE 2: In this case a POSNEGSHFT cell is used as a level shift between CML logic gates and the ECL output buffer (BUFOUT10K).

The critical task is to properly identify the conditions that determine whether the internal CML logic operates above or below ground. Coupled with this is the fact that the I/O buffers must operate between power supplies that allow them to be compatible with the internal logic. The important point to observe is, that the only time internal CML logic operates below ground is when all I/O interfacing is through ECL compatible buffers operating exclusively below ground. Note that the ECL I/O buffers will operate either above or below ground. The TTL I/O buffers will only operate above ground.

The VPOS property value shown in Table 4.1 applies to CML cells and input or output buffer cells. The Mentor instructions in the Design System give more information on setting the VPOS property. Note that some cells like the BUFOUT10K, POSNEGSHFT, and BIASGEN10K do not have a VPOS property shown on the cell symbol since V_{CC} is always the most positive power supply for these cells. These cells have a VPOS property that is set to V_{CC}, but it is hidden and fixed.

Note that proper interfacing from above-ground CML logic to below-ground ECL logic requires the POSNEGSHFT cell as a translator interface between the internal logic cells and the ECL output buffer. However, if the ECL output buffer is used above ground, the CML logic connects directly to the ECL output buffer.

I/O BUFFERS

Interfacing the digital logic internal CML gates to the outside may be accomplished in several ways. Input and output buffers are available that are compatible with the ECL 10kH specifications, and a separate set of buffers are compatible with the LSTTL logic family. The selection of the buffer type is a customer option.

There are special conditions that must be met in order to guarantee proper operation of these buffers. Some have already been mentioned in the preceeding section. Other conditions include:

When using the high impedance state TTL output buffer (OB_BUFOUTTS), a special connection must be made to the high impedance control pin, labeled TSENABLEN. An open collector output buffer (OB_BUFOUTOC) is used to drive that pin. The user must connect a CML logic level control signal to the input of the OB_BUFOUTOC cell in order to complete that functional control. The OB_BUFOUTOC cell can drive up to eight output buffer enable pins in parallel.

Tables 5-1 and 5-2 include the DC electrical characteristics for both the TTL and ECL compatible input and output buffers. Please refer to these tables for details related to any of the respective cells shown in the data sheets.

Figure 2-2: ECL Transfer Curves

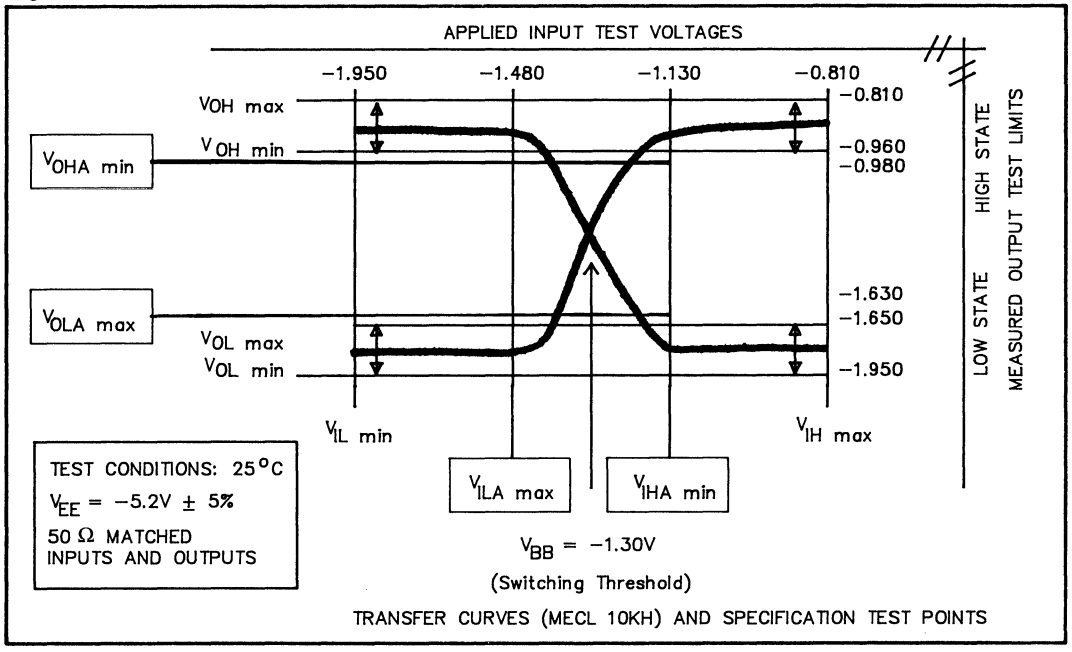


TABLE 5-1: ECL10KH COMPATIBLE DC ELECTRICAL CHARACTERISTICS

INPUT FORCING VOLTAGES	*PARAMETER*	*MECL 10KH COMPATIBLE SPEC LIMITS[1] AMBIENT TEMPERATURE 0°C*	*25°C*	*70°C*	*UNIT*
V_{IH} Max and V_{IL} Min	V_{OH} Max	−0.840	−0.810	−0.740	Vdc
	V_{OH} Min	−1.000	−0.960	−0.900	Vdc
	V_{OL} Max	−1.650	−1.650	−1.620	Vdc
	V_{OL} Min	−1.950	−1.950	−1.950	Vdc
V_{IHA} Min and V_{ILA} Max	V_{OHA} Min	−1.020	−0.980	−0.920	Vdc
	V_{OLA} Max	−1.630	−1.630	−1.600	Vdc
V_{IH} Max	I_{INH} Max	25	25	25	µA
Input Voltage Values	V_{IH} Max	−0.840	−0.810	−0.730	Vdc
	V_{IL} Min	−1.950	−1.950	−1.950	Vdc
	V_{IHA} Min	−1.170	−1.130	−1.070	Vdc
	V_{ILA} Max	−1.480	−1.480	−1.450	Vdc

NOTES:
1. DC test limits are specified after thermal equilibrium has been established with the device having a controlled transverse air flow of 750 lfpm. V_{EE} = −5.2 V ± 5%. All ECL outputs are loaded with 50 Ohms to −2.0 V.

TABLE 5-2: LSTTL COMPATIBLE DC ELECTRICAL CHARACTERISTICS

				Note 1			
SYMBOL	*PARAMETER*	*TEST CONDITIONS* **Note 2**		*MIN*	*TYP*	*MAX*	*UNITS*
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage		2.0			volts
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage				0.8	volts
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V; I_{IN} = −12.0mA			−0.65	−1.5	volts
V_{OH}	Output HIGH Voltage	V_{CC} = 4.75V; I_{OH} = −400µA		2.7	3.4		volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.75V	I_{OL} = 4.0mA		0.25	0.4	volts
			I_{OL} = 8.0mA		0.35	0.5	volts
I_{IH}	Input HIGH Current	V_{CC} = 5.25V	V_{IN} = 2.7V		10	20	µA
			V_{IN} = 5.25V			0.1	mA
I_{IL}	Input LOW Current	V_{CC} = 5.25V; V_{IN} = 0.4V				−0.4	mA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.25V; V_{IN} = 0V *Note3*		−20		−100	mA
I_{OZH}	Output Off-Z Current HIGH	V_{CC} = 5.25V; V_{OUT} = 2.7V				20	µA
I_{OZL}	Output Off-Z Current LOW	V_{CC} = 5.25V; V_{OUT} = 0.4V				−20	µA
I_{IHT}	Input HIGH Current Bidirectional Tri-State Output	V_{CC} = Max; V_{IN} = 2.7V				50	µA
I_{IHC}	Input HIGH Current Bidirectional Open Collector Output	V_{CC} = Max; V_{IN} = 5.5V				180	µA
I_{ILT}	Input LOW Current Bidirectional Tri-State Output	V_{CC} = Max; V_{IN} = 0.4V				−420	µA
I_{ILC}	Input LOW Current Bidirectional Open Collector Output	V_{CC} = Max; V_{IN} = 0.4V				−420	µA
I_{OHC}	Output HIGH Current Open Collector Output	V_{CC} = Max; V_{OH} = 5.5V				100	µA

Note 1 *V_{CC} = 4.75V to 5.25V; T_A = 0°C to 70°C unless otherwise noted.*

Note 2 *Typical limits are at V_{CC} = 5.0V, T_A = 25°C.*

Note 3 *Not more than one output shorted at one time, duration of test not to exceed one second.*

DIGITAL CELLS

NAME	AREA MILS²	TYPICAL PERFORMANCE, 5V, 25°C, 2 LOADS					
		HIGH		MED		LOW	
		P (mW)	S (nSec)	P (mW)	S (nSec)	P (mW)	S (nSec)
SIMPLE GATES:							
ORNOR2	40.6	2.25	2.0	1.13	2.3	0.56	4.2
ORNOR3	40.6	2.25	2.0	1.13	2.5	0.56	4.2
ORNOR4	40.6	2.25	2.0	1.13	2.5	0.56	4.4
ORNOR5	43.7	2.25	2.0	1.13	2.5	0.56	4.4
ORNOR6	43.7	2.25	2.0	1.13	2.7	0.56	4.6
ORNOR7	43.7	2.25	2.0	1.13	2.8	0.56	4.8
ANDNAND2	43.7	4.50	2.1	2.25	2.6	1.13	4.6
ANDNAND3	59.4	6.75	2.5	3.38	3.1	1.69	5.3
EXORNOR2	50.0	4.50	2.2	2.25	2.9	1.13	5.1
FLIP FLOPS:							
RS LATCH	40.6	2.25	5.6	1.13	7.7	0.56	12.8
D LATCH	46.9	4.50	2.2	2.25	3.1	1.13	5.5
D FF1	112.5	5.40	4.9	2.70	6.7	1.35	11.2
JKFF1	162.5	7.20	5.1	3.60	6.8	1.80	11.2
TFF1	112.5	5.40	4.9	2.70	6.7	1.35	11.2
DFF2	103.1	3.15	4.1	1.58	6.0	0.79	10.2
JKFF2	150.0	3.15	4.1	1.58	6.0	0.79	10.2
SPECIAL PURPOSE:							
CLOCKBUF	40.6	11.5	1.8	10.4	1.9	9.90	2.5
SIGBUF	21.9	—	—	5.0	1.4	—	—
POSNEGSHFT	37.5	4.10	1.5	2.05	2.1	1.02	2.3
INPUT/OUTPUT BUFFERS:							
IB BUFIN	46.9	—	—	6.35	1.2	—	—
OB BUFOUT	65.6	—	—	10.8	7.3	—	—
OB BUFOUTTS	81.2	—	—	10.8	8.7	—	—
OB BUFOUTOC	65.6	—	—	10.8	12.2	—	—
IB SCHMITT1	34.4	—	—	6.70	3.3	—	—
IB BUFIN10K	40.6	—	—	2.40	1.0	—	—
OB BUFOUT10K	65.6	—	—	49.4	2.3	—	—
MSI FUNCTIONS:							
DECODER 1OF4	56.2	4.50	2.0	2.25	2.7	1.13	4.5
DECODER 1OF8	128.1	6.75	2.2	3.38	2.9	1.69	4.8
MUX 2TO1	56.2	4.50	2.3	2.25	3.0	1.13	5.0
MUX 4TO1	100.0	6.75	2.7	3.38	3.6	1.69	6.3
BIAS GENERATORS:							
VCSGEN	34.4	—	—	3.23	—	—	—
VBBGEN	84.4	19.6	—	—	—	9.80	—
BIASGEN10K	43.7	—	—	10.4	—	—	—

CELL SPECIFICATIONS WITH SYMBOLS ARE GIVEN IN THE VL1000 USER'S GUIDE IN THE DESIGN SYSTEM

CUSTOM CELL DESIGN

1. INTRODUCTION

The VL1000 Linear Bipolar Cell Library contains a set of predesigned and characterized standard analog and digital cells. When a designer begins to design a chip using these standard cells, he will often find that there are necessary functions for analog and digital circuitry not available in the standard set. Many times the standard functions are too slow (or fast), consume too much power or do not perform the required function. Thus, in most chip designs, there will be a few functions for which new circuitry will have to be constructed. This section of the User's Guide gives information on how to design customer-specific cells using the components available in the VL1000.

When a suitable cell design has been created and checked by simulation, the user documents this with a circuit schematic created on a Mentor workstation and sends it to VTC incorporated. A layout of the cell is then made, and it is integrated into the overall chip circuitry.

In addition to this information, VTC also provides a Design Manual which covers general practices and usage for bipolar linear design.

2. GETTING STARTED

The first step to design a user-specific cell is to find a trial circuit which performs the required function. Circuit diagrams are drawn similar to those used with discrete designs. No breadboard is built, but the circuit is *simulated* using a computer simulation program such as SPICE, which solves the equations for a mathematical model of the circuit.

The trial circuit is simulated, and the simulation repeated as needed with "cut and try" variations until the user is satisfied with the design.

To begin designing user-specific cells, the following items are needed (in addition to this User's Guide):

- A copy of the Design Manual
- A set of VTC Design Notes (helpful for some aspects of circuit design)
- Access to an Apollo workstation running Mentor software
- A textbook on analog-integrated circuit design such as *Analysis and Design of Analog Integrated Circuits* (2nd Ed.) by P. Gray and R. Meyer (J. Wiley & Sons, 1984), is also helpful.

3. GENERAL DESIGN CONSIDERATIONS

Power dissipation. There is nothing in the VL1000 software to prevent the designer from creating circuits with very high power dissipation. The available components can easily be used to create chips dissipating 10 or 20 Watts. Ordinary packages cannot dissipate this much heat. It is therefore important for the designer to keep track of the total power dissipation of the chip (including both standard and user-specific cells), and keep this in line with thermal properties of the intended package. As a rough guide, small ceramic DIPs (14 and 16 pins) can safely dissipate about .5 W. Larger DIPs, such as the 24 and 28 pin sizes, can dissipate up to 1 W. The 40-pin ceramic DIP can dissipate up to 1.5 W. In other packages, the junction temperature should be kept *below 125°C.*

The designer should carefully consider how much current to use in each subcircuit. Transistors should not be operated at their maximum Ic. Small currents may be large enough for many parts of a circuit. A typical *on-chip parasitic node capacitance* is only about .5pF, and 100μA suffices to slew the voltage at the node at 200 mV/nsec. This is sufficient for many applications.

4. LHD TRANSISTORS

TABLE 4.1: NPN TRANSISTORS*

NAME	MAX I_C (mA)	COMMENTS
NPN TRANSISTORS:		
T3	0.5	Minimum-geometry NPN, used for the majority of the circuitry.
T6	1.0	Larger NPN for more current.
T6R	0.5	A transistor with double base stripes and a 6x6 micron octagonal emitter. To be used where better Vbe matching is needed or emitter ratioing is used. Larger multi-emitter T6R transistors can be created using the area factor.
T12	2.0	A larger NPN.
T15	4.0	A larger NPN with double collectors.
T20	6.0	A larger NPN with double collectors.
T40	22.0	An output driver for ECL circuits or other high-current outputs with six emitters.
TLN1	10.0	A large NPN with four 50x2 micron emitter stripes intended for use in low-noise amplifiers. Very low base resistance.
TPWR	>15.0	This is a *modular power* device. By combining several sections, using the transistor area factor, NPNs up to 200-300 mA can be built (in multiples of 15 mA).
SCHOTTKY TRANSISTORS:		
T3S	0.5	Schottky version of T3.
T6S	1.0	Schottky version of T6.
T6RS	0.5	Schottky version of T6R.
T12S	2.0	Schottky version of T12.
T30S	10.0	Large Schottky transistor for TTL output drivers. Has double emitter and double collector stripes, and a guard-ring Schottky diode.
TPWRS	>15.0	Schottky *modular power* device.

**Diode-connected versions of all NPN transistors are available.*

TABLE 4.2: PNP TRANSISTORS

NAME	MAX IC PER COLL.	COMMENTS
TLP1	.33 mA	General-purpose lateral PNP with a "large" emitter diameter. Has better Vbe matching than TLP2. Also available in double-collector and four-collector versions.
TLP2	.33 mA	General-purpose lateral PNP with a "small" emitter diameter. This is the "minimum" lateral PNP and is considerably smaller than TLP1. It has lower parasitic capacitances, but Vbe matching is not so good as for TLP1. A double-collector version is available.
TVP1	.10 mA	Standard substrate (vertical) PNP. The low allowed current is due to the inherent high collector resistance.

5. BIPOLAR TRANSISTOR MODELING

The SPICE models for the VL1000 bipolar transistors are in the Mentor data base (see "Mentor Instructions" section of the User's Guide). The model used is the Gummel-Poon type. More data on transistor usage is given in parts II and III of the Design Manual, and it is recommended the designer read this material before undertaking a design. Graphs of typical I-V characteristics for a minimum NPN at various temperatures are given in part II of the VTC Design Manual.

5.1 Transistor Models

The transistor models included in the Mentor data base are considered *worst-case SLOW* models. The performance will not be worse than predicted by SPICE with these models as long as parasitic capacitance is taken into account. These models are convenient, but not suitable for *stability analyses* (for example in feedback loops), where worst-case FAST models are needed. The worst-case FAST models are derived from the worst-case SLOW models by the following changes to the SPICE model parameters:

TABLE 5.1: CHANGES TO FIND WORST-CASE FAST SPICE PARAMETERS

SPICE PARAMETER(S)	MULTIPLY BY
IKF	1.20
CJE, CJC, RB	0.80
RC, RE	0.75
CJS	0.85
TF (for NPNs) (for PNPs)	0.85 0.60

The remaining SPICE parameters have little influence on the circuit speed and are left unchanged.

5.2 Breakdown Voltages and Beta

The junction breakdown voltages of the transistors are not part of the SPICE model. The designer must ensure the voltages occurring in the circuit do not exceed the breakdown voltages. A list follows:

TABLE 5.2: BREAKDOWN VOLTAGES AND BETA

NPN PARAMETER	MIN.	TYP.	MAX.
BVcbo (base-coll)	25	30	35
BVebo (base-emit)	5.8	6.0	6.2
BVceo (coll-emit)	7.0		
Beta	50	100	200

PNP PARAMETER	MIN.	TYP.	MAX.
BVcbo (base-coll)	25	30	35
BVebo (base-emit)	25	30	35
BVceo (coll-emit)	13.2		
Beta (TLP1) at Ic = .05 mA	50	80	180
Beta (TLP1) at Ic = .33 mA	20	30	

5.3 Maximum Collector Current

Each transistor has a maximum collector current (see Tables 4.1 and 4.2) at the approximate boundary between high-level and low-level injection. The device performance usually gets worse above this current. The SPICE models are also less accurate above the stated maximum collector current, and all of the data on modeling, matching, or temperature coefficient is of unknown accuracy above the maximum Ic.

5.4 Temperature Dependences

The temperature dependences of the transistor currents and voltages are contained in the SPICE model and need not be considered explicitly. The most significant transistor temperature dependence is the drop of V_{be}(ON) by about 1.8mV per degree.

5.5 Transistor Matching

Many circuits (such as differential amplifiers) require close matching between the properties of "paired" transistors. Table 5.3 gives data on the matching properties of LHD-process transistors. This data is valid for *transistors with identical geometries (i.e., the same component name) which are located immediately adjacent to each other on the chip.* The matching properties are expressed in terms of the *standard deviation* defined in the usual statistical sense, and are based on detailed measurements of LHD transistors. For those table entries where the unit is percent, the standard deviation is found by taking the percentage of the typical or nominal value.

TABLE 5.3: TYPICAL TRANSISTOR MATCHING PROPERTIES

PARAMETER	STD. DEV.	UNIT
Input offset -- T3 or T3S	1.4	mV
Input offset -- T6 NPN	1.2	mV
Input offset -- T6R NPN	0.7	mV
Input offset -- T12 NPN	1.0	mV
Input offset -- TLN1 NPN	0.3	mV
Input offset -- T30S NPN	0.8	mV
Input offset -- TLP1 PNP	0.3	mV
Input offset -- TLP2 PNP	0.45	mV
Beta -- all NPNs and PNPs	1.5	%
Collector current diff. for 2-coll lat. PNP (TLP1)	1.0	%

The matching data given in Table 5.3 is typical of situations in which the *temperature* and *stress gradients* in the chip are negligible. Temperature gradients depend on chip layout and placement of circuit elements which dissipate large amounts of heat, and are thus influenced by the layout. Circuits requiring very tight matching of circuit elements should be called to the attention of VTC layout personnel so a suitable strategy can be followed. These factors are discussed in more detail in the Design Manual, part VII.

Circuits which are sensitive to transistor mismatch should be simulated for worst-case transistor matching. Methods of performing this type of worst-case simulation are given in Section 10 of the VTC Design Manual.

5.6 Frequency Response

The frequency response is contained in the SPICE models. In general the NPN transistors have minimum unity-gain frequencies of about .8 GHz. The unity-gain frequencies of PNPs are about 100 MHz. SPICE simulations should give accurate worst-case SLOW predictions of frequency response for a given circuit, along with its dependence on temperature, supply voltage, etc.

5.7 Parasitic Transistors and Diodes

Standard bipolar proceses contain numerous parasitic elements which are described in part VII of the Design Manual. Transistor *saturation* is a forbidden practice for non-Schottky transistors. Operation of transistors in the *inverted mode* is also forbidden. The reasons for these rules are discussed in the VTC Design Manual.

5.8 The PNP Transistor Model

The lateral PNP transistor model requires an extra diode to accurately model the substrate capacitance (see Design Manual, part III). The extra diode is supplied automatically when the PNP symbol from the LHD_LIB Mentor Graphics library is used (see Mentor Graphics Instructions section of the User's Guide in the VL1000 Design System.

5.9 Schottky Transistor Models

Because of the extra elements in a Schottky transistor, its model must be more complicated (see Design Manual, Section 17). The necessary elements are provided automatically when VL1000 LHD_LIB components are used.

6. INTEGRATED RESISTORS

Integrated resistors differ from discrete resistors in several respects: a) They have an important parasitic capacitance to the silicon "body" in which they are embedded; b) They have a substantial temperature coefficient; c) They have a diode isolating them from the other regions of be biased to keep it OFF. Resistors are covered in greater detail in the Design Manual, part V.

6.1 Temperature Coefficients

The LHD process has two resistor types, *base* and *implant*. These differ in doping level, and therefore in temperature coefficient. The base resistor has a much lower temperature coefficient, but is of very limited use for resistor values over 1 kOhm. The implant type achieves higher values (to tens of kOhms), but at the expense of a greater temperature dependence. The required temperature coefficients are built into the VL1000 component library, and the user only designates a resistor as B (for base) or I (for implant).

The temperature coefficients are given here for reference. When using the Mentor software, the temperature coefficient is automatically put into the SPICE source file.

TABLE 6.1: TEMPERATURE COEFFICIENTS FOR LHD RESISTORS

RESISTOR TYPE	*LINEAR TC*	*QUADR. TC*
Base	.00030	5.8E-6
Implant	.00292	6.9E-6

The Design Manual contains a graph of the temperature dependences of the base and implant resistor types. The base resistors pass through a minimum below room temperature, and begin to rise in value for lower temperature.

6.2 Resistor Adjustment

If it may be necessary to change a resistor value after evaluation of first-pass circuits, VTC should be notified when the schematic is sent, and a notation of the percentage adjustment required should be written on the schematic. Allowance can then be made for later resistor adjustment when performing the layout. This can mean the difference between a one-mask change and an all-layers redesign. Resistor adjustment is discussed in more detail in Section 40 of the VTC Design Manual.

6.3 Resistor Parasitic Capacitance

The model used for an integrated resistor is shown in part V of the Design Manual. A diode representing half the capacitance is loaded on each end of the resistor. The cathodes of the diodes are connected to the *most positive* supply voltage (see part V of the Design Manual). Correctly scaled parasitic capacitors are provided automatically when VL1000 LHD_LIB component symbols are used.

6.4 Resistor Matching and Tolerances

The ability to match resistors to close tolerances is one of the more favorable features of monolithic IC design. The *absolute tolerances*, however, are less favorable -- the absolute worst-case tolerance for resistor values at a given temperature is to be taken as ±20% of the nominal value for both base and implant types. There is no correlation in the fluctuations of the base and implant resistors -- if the base resistor happens to be 12% low on a given lot the implant resistors may be 15% high. Therefore, *do not ratio base resistors against implant resistors.* Resistor ratioing rules are discussed in detail in Section 35 of the VTC Design Manual.

The resistor matching parameters are given in Table 6.2 The standard deviation would be observed if one measured the values of a large number of identically sized and identically oriented resistors placed in close proximity on a chip and fitted the resulting distribution to normal distribution. It is defined as a percentage of resistor nominal value. The resistor *ratio* standard deviations will be somewhat worse because the percentage standard deviation of a ratio is larger than those of the parameters entering the ratio.

TABLE 6.2: TYPICAL RESISTOR MATCHING

RESISTOR WIDTH (MICRONS)	*STD. DEV. (%)*	
	BASE	*IMPLT*
3	—	.30
5	.18	.25
7	.15	.19
9	.13	.14
11	.11	.11
13	.10	.10
15 or more	.09	.09

Like the transistors, the resistors are affected by temperature gradients (through the temperature coefficient) and stress effects (see Sections 56 and 57 of the Design Manual), and are not taken into account in Table 6.2 since they depend on the final circuit layout.

Resistors of completely arbitrary value may not be used in the LHD process because the length and width increments are limited to multiples of .5 microns. To assist in the design of resistors, tables of resistor value versus length and width are supplied.

6.5 Choosing the Resistor Length and Width

The procedure for choosing a resistor follows: 1) Choose a resistor width. This is done according to the degree of matching and precision required. In general, wider resistors have better matching and better absolute value control; 2) Choose resistor length to get the required value; 3) If tight matching or ratioing is required, resistor segments with identical width and nearly identical length should be used. Parallel or series combinations of resistors can then be used to achieve the desired ratio. Resistor ratio rules are discussed in Section 35 of the Design Manual. The longer resistors are listed on coarser increments, and it is legitimate to interpolate on .5 micron intervals if necessary.

The designer is requested to stay on the charts. If resistors too low or too high for the charts are needed, they can be made using series and parallel combinations of those which are on the chart. Such series/parallel combinations also allow the resistor value to be set to finer increments.

It is strongly recommended that the designer read the material in part V of the Design Manual before beginning a design with integrated resistors.

TABLE 6.3: NARROW IMPLANT RESISTOR VALUES

	WIDTH						
LENGTH	3	5	7	9	11	13	15
12.5	2270.8	1602.9	1238.6	1009.2	851.5	736.4	648.8
13	2375.0	1676.4	1295.4	1055.5	890.6	770.2	678.5
13.5	2479.1	1750.0	1352.2	1101.8	929.6	804.0	708.3
14	2583.3	1823.5	1409.0	1148.1	968.7	837.8	738.0
14.5	2687.5	1897.0	1465.9	1194.4	1007.8	871.6	767.8
15	2791.6	1970.5	1522.7	1240.7	1046.8	905.4	797.6
15.5	2895.8	2044.1	1579.5	1287.0	1085.9	939.1	827.3
16	3000.0	2117.6	1636.3	1333.3	1125.0	972.9	857.1
16.5	3104.1	2191.1	1693.1	1379.6	1164.0	1006.7	886.9
17	3208.3	2264.7	1750.0	1425.9	1203.1	1040.5	916.6
17.5	3312.5	2338.2	1806.8	1472.2	1242.1	1074.3	946.4
18	3416.6	2411.7	1863.6	1518.5	1281.2	1108.1	976.1
18.5	3520.8	2485.2	1920.4	1564.8	1320.3	1141.8	1005.9
19	3625.0	2558.8	1977.2	1611.1	1359.3	1175.6	1035.7
19.5	3729.1	2632.3	2034.0	1657.4	1398.4	1209.4	1065.4
20	3833.3	2705.8	2090.9	1703.7	1437.5	1243.2	1095.2
20.5	3937.5	2779.4	2147.7	1750.0	1476.5	1277.0	1125.0
21	4041.6	2852.9	2204.5	1796.2	1515.6	1310.8	1154.7
21.5	4145.8	2926.4	2261.3	1842.5	1554.6	1344.5	1184.5
22	4250.0	3000.0	2318.1	1888.8	1593.7	1378.3	1214.2
22.5	4354.1	3073.5	2375.0	1935.1	1632.8	1412.1	1244.0
23	4458.3	3147.0	2431.8	1981.4	1671.8	1445.9	1273.8
23.5	4562.5	3220.5	2488.6	2027.7	1710.9	1479.7	1303.5
24	4666.6	3294.1	2545.4	2074.0	1750.0	1513.5	1333.3
24.5	4770.8	3367.6	2602.2	2120.3	1789.0	1547.2	1363.0
25	4875.0	3441.1	2659.0	2166.6	1828.1	1581.0	1392.8
25.5	4979.1	3514.7	2715.9	2212.9	1867.1	1614.8	1422.6
26	5083.3	3588.2	2772.7	2259.2	1906.2	1648.6	1452.3
26.5	5187.5	3661.7	2829.5	2305.5	1945.3	1682.4	1482.1
27	5291.6	3735.2	2886.3	2351.8	1984.3	1716.2	1511.9
27.5	5395.8	3808.8	2943.1	2398.1	2023.4	1750.0	1541.6
28	5500.0	3882.3	3000.0	2444.4	2062.5	1783.7	1571.4
28.5	5604.1	3955.8	3056.8	2490.7	2101.5	1817.5	1601.1
29	5708.3	4029.4	3113.6	2537.0	2140.6	1851.3	1630.9
29.5	5812.5	4102.9	3170.4	2583.3	2179.6	1885.1	1660.7
30	5916.6	4176.4	3227.2	2629.6	2218.7	1918.9	1690.4
30.5	6020.8	4250.0	3284.0	2675.9	2257.8	1952.7	1720.2
31	6125.0	4323.5	3340.9	2722.2	2296.8	1986.4	1750.0
31.5	6229.1	4397.0	3397.7	2768.5	2335.9	2020.2	1779.7
32	6333.3	4470.5	3454.5	2814.8	2375.0	2054.0	1809.5
32.5	6437.5	4544.1	3511.3	2861.1	2414.0	2087.8	1839.2
33	6541.6	4617.6	3568.1	2907.4	2453.1	2121.6	1869.0
33.5	6645.8	4691.1	3625.0	2953.7	2492.1	2155.4	1898.8
34	6750.0	4764.7	3681.8	3000.0	2531.2	2189.1	1928.5
34.5	6854.1	4838.2	3738.6	3046.2	2570.3	2222.9	1958.3
35	6958.3	4911.7	3795.4	3092.5	2609.3	2256.7	1988.0
35.5	7062.5	4985.2	3852.2	3138.8	2648.4	2290.5	2017.8
36	7166.6	5058.8	3909.0	3185.1	2687.5	2324.3	2047.6
37	7375.0	5205.8	4022.7	3277.7	2765.6	2391.8	2107.1
38	7583.3	5352.9	4136.3	3370.3	2843.7	2459.4	2166.6

LENGTH	WIDTH						
	3	5	7	9	11	13	15
39	7791.6	5500.0	4250.0	3462.9	2921.8	2527.0	2226.1
40	8000.0	5647.0	4363.6	3555.5	3000.0	2594.5	2285.7
41	8208.3	5794.1	4477.2	3648.1	3078.1	2662.1	2345.2
42	8416.6	5941.1	4590.9	3740.7	3156.2	2729.7	2404.7
43	8625.0	6088.2	4704.5	3833.3	3234.3	2797.2	2464.2
44	8833.3	6235.2	4818.1	3925.9	3312.5	2964.8	2523.8
45	9041.6	6382.3	4931.8	4018.5	3390.6	2932.4	2583.3
46	9250.0	6529.4	5045.4	4111.1	3468.7	3000.0	2642.8
47	9458.3	6676.4	5159.0	4203.7	3546.8	3067.5	2702.3
48	9666.6	6823.5	5272.7	4296.2	3625.0	3135.1	2761.9
49	9875.0	6970.5	5386.3	4388.8	3703.1	3202.7	2821.4
50	10083.3	7117.6	5500.0	4481.4	3781.2	3270.2	2880.9
51	10291.6	7264.7	5613.6	4574.0	3859.3	3337.8	2940.4
52	10500.0	7411.7	5727.2	4666.6	3937.5	3405.4	3000.0
53	10708.3	7558.8	5840.9	4759.2	4015.6	3472.9	3059.5
54	10916.6	7705.8	5954.5	4851.8	4093.7	3540.5	3119.0
55	11125.0	7852.9	6068.1	4944.4	4171.8	3608.1	3178.5
56	11333.3	8000.0	6181.8	5037.0	4250.0	3675.6	3238.0
57	11541.6	8147.0	6295.4	5129.6	4328.1	3743.2	3297.6
58	11750.0	8294.1	6409.0	5222.2	4406.2	3810.8	3357.1
59	11958.3	8441.1	6522.7	5314.8	4484.3	3878.3	3416.6
60	12166.6	8588.2	6636.3	5407.4	4562.5	3945.9	3476.1
61	12375.0	8735.2	6750.0	5500.0	4640.6	4013.5	3535.7
62	12583.3	8882.3	6863.6	5592.5	4718.7	4081.0	3595.2
63	12791.6	9029.4	6977.2	5685.1	4796.8	4148.6	3654.7
64	13000.0	9176.4	7090.9	5777.7	4875.0	4216.2	3714.2
65	13208.3	9323.5	7204.5	5870.3	4953.1	4283.7	3773.8
66	13416.6	9470.5	7318.1	5962.9	5031.2	4351.3	3833.3
67	13625.0	9617.6	7431.8	6055.5	5109.3	4418.9	3892.8
68	13833.3	9764.7	7545.4	6148.1	5187.5	4486.4	3952.3
69	14041.6	9911.7	7659.0	6240.7	5265.6	4554.0	4011.9
70	14250.0	10058.8	7772.7	6333.3	5343.7	4621.6	4071.4
71	14458.3	10205.8	7886.3	6425.9	5421.8	4689.1	4130.9
72	14666.6	10352.9	8000.0	6518.5	5500.0	4756.7	4190.4
73	14875.0	10500.0	8113.6	6611.1	5578.1	4824.3	4250.0
74	15083.3	10647.0	8227.2	6703.7	5656.2	4891.8	4309.5
75	15291.6	10794.1	8340.9	6796.2	5734.3	4959.4	4369.0
76	15500.0	10941.1	8454.5	6888.8	5812.5	5027.0	4428.5
77	15708.3	11088.2	8568.1	6981.4	5890.6	5094.5	4488.0
78	15916.6	11235.2	8681.8	7074.0	5968.7	5162.1	4547.6
79	16125.0	11382.3	8795.4	7166.6	6046.8	5229.7	4607.1
80	16333.3	11529.4	8909.0	7259.2	6125.0	5297.2	4666.6
82	16750.0	11823.5	9136.3	7444.4	6281.2	5432.4	4785.7
84	17166.6	12117.6	9363.6	7629.6	6437.5	5567.5	4904.7
86	17583.3	12411.7	9590.9	7814.8	6593.7	5702.7	5023.8
88	18000.0	12705.8	9818.1	8000.0	6750.0	5837.8	5142.8
90	18416.6	13000.0	10045.4	8185.1	6906.2	5972.9	5261.9
92	18833.3	13294.1	10272.7	8370.3	7062.5	6108.1	5380.9
94	19250.0	13588.2	10500.0	8555.5	7218.7	6243.2	5500.0
96	19666.6	13882.3	10727.2	8740.7	7375.0	6378.3	5619.0
98	20083.3	14176.4	10954.5	8925.9	7531.2	6513.5	5738.0
100	20500.0	14470.5	11181.8	9111.1	7687.5	6648.6	5857.1

TABLE 6.4: WIDE IMPLANT RESISTOR VALUES

LENGTH	WIDTH						
	18	20	22	24	26	28	30
20	929.2	844.0	773.1	713.1	661.8	617.4	578.6
20.5	954.5	866.9	794.1	732.5	679.8	634.2	594.3
21	979.7	889.9	815.1	751.9	697.8	651.0	610.0
21.5	1005.0	912.8	836.1	771.3	715.8	667.7	625.7
22	1030.3	935.7	857.1	790.6	733.8	684.5	641.5
22.5	1055.5	958.7	878.1	810.0	751.7	701.3	657.2
23	1080.8	981.6	899.1	829.4	769.7	718.1	672.9
23.5	1106.0	1004.5	920.1	848.8	787.7	734.8	688.6
24	1131.3	1027.5	941.1	868.2	805.7	751.6	704.4
24.5	1156.5	1050.4	962.1	887.5	823.7	768.4	720.1
25	1181.8	1073.3	983.1	906.9	841.7	785.2	735.8
25.5	1207.0	1096.3	1004.2	926.3	859.7	802.0	751.5
26	1232.3	1119.2	1025.2	945.7	877.6	818.7	767.2
26.5	1257.5	1142.2	1046.2	965.1	895.6	835.5	783.0
27	1282.8	1165.1	1067.2	984.4	913.6	852.3	798.7
27.5	1308.0	1188.0	1088.2	1003.8	931.6	869.1	814.4
28	1333.3	1211.0	1109.2	1023.2	949.6	885.9	830.1
28.5	1358.5	1233.9	1130.2	1042.6	967.6	902.6	845.9
29	1383.8	1256.8	1151.2	1062.0	985.6	919.4	861.6
29.5	1409.0	1279.8	1172.2	1081.3	1003.5	936.2	877.3
30	1434.3	1302.7	1193.2	1100.7	1021.5	953.0	893.0
30.5	1459.5	1325.6	1214.2	1120.1	1039.5	969.7	908.8
31	1484.8	1348.6	1235.2	1139.5	1057.5	986.5	924.5
31.5	1510.1	1371.5	1256.3	1158.9	1075.5	1003.3	940.2
32	1535.3	1394.4	1277.3	1178.2	1093.5	1020.1	955.9
32.5	1560.6	1417.4	1298.3	1197.6	1111.5	1036.9	971.6
33	1585.8	1440.3	1319.3	1217.0	1129.4	1053.6	987.4
33.5	1611.1	1463.3	1340.3	1236.4	1147.4	1070.4	1003.1
34	1636.3	1486.2	1361.3	1255.8	1165.4	1087.2	1018.8
34.5	1661.6	1509.1	1382.3	1275.1	1183.4	1104.0	1034.5
35	1686.8	1532.1	1403.3	1294.5	1201.4	1120.8	1050.3
35.5	1712.1	1555.0	1424.3	1313.9	1219.4	1137.5	1066.0
36	1737.3	1577.9	1445.3	1333.3	1237.4	1154.3	1081.7
36.5	1762.6	1600.9	1466.3	1352.7	1255.3	1171.1	1097.4
37	1787.8	1623.8	1487.3	1372.0	1273.3	1187.9	1113.2
37.5	1813.1	1646.7	1508.4	1391.4	1291.3	1204.6	1128.9
38	1838.3	1669.7	1529.4	1410.8	1309.3	1221.4	1144.6
38.5	1863.6	1692.6	1550.4	1430.2	1327.3	1238.2	1160.3
39	1888.8	1715.5	1571.4	1449.6	1345.3	1255.0	1176.1
39.5	1914.1	1738.5	1592.4	1468.9	1363.3	1271.8	1191.8
40	1939.3	1761.4	1613.4	1488.3	1381.2	1288.5	1207.5
40.5	1964.6	1784.4	1634.4	1507.7	1399.2	1305.3	1223.2
41	1989.8	1807.3	1655.4	1527.1	1417.2	1322.1	1238.9
41.5	2015.1	1830.2	1676.4	1546.5	1435.2	1338.9	1254.7
42	2040.4	1853.2	1697.4	1565.8	1453.2	1355.7	1270.4
42.5	2065.6	1876.1	1718.4	1585.2	1471.2	1372.4	1286.1
43	2090.9	1899.0	1739.4	1604.6	1489.2	1389.2	1301.8
43.5	2116.1	1922.0	1760.5	1624.0	1507.1	1406.0	1317.6
44	2141.4	1944.9	1781.5	1643.4	1525.1	1422.8	1333.3
44.5	2166.6	1967.8	1802.5	1662.7	1543.1	1439.5	1349.0
45	2191.9	1990.8	1823.5	1682.1	1561.1	1456.3	1364.7
45.5	2217.1	2013.7	1844.5	1701.5	1579.1	1473.1	1380.5
46	2242.4	2036.6	1865.5	1720.9	1597.1	1489.9	1396.2
46.5	2267.6	2059.6	1886.5	1740.3	1615.1	1506.7	1411.9
47	2292.9	2082.5	1907.5	1759.6	1633.0	1523.4	1427.6
47.5	2318.1	2105.5	1928.5	1779.0	1651.0	1540.2	1443.3
48	2343.4	2128.4	1949.5	1798.4	1669.0	1557.0	1459.1
48.5	2368.6	2151.3	1970.5	1817.8	1687.0	1573.8	1474.8
49	2393.9	2174.3	1991.5	1837.2	1705.0	1590.6	1490.5
49.5	2419.1	2197.2	2012.6	1856.5	1723.0	1607.3	1506.2

LENGTH	WIDTH						
	18	20	22	24	26	28	30
50	2444.4	2220.1	2033.6	1875.9	1741.0	1624.1	1522.0
50.5	2469.6	2243.1	2054.6	1895.3	1758.9	1640.9	1537.7
51	2494.9	2266.0	2075.6	1914.7	1776.9	1657.7	1553.4
51.5	2520.2	2288.9	2096.6	1934.1	1794.9	1674.4	1569.1
52	2545.4	2311.9	2117.6	1953.4	1812.9	1691.2	1584.9
52.5	2570.7	2334.8	2138.6	1972.8	1830.9	1708.0	1600.6
53	2595.9	2357.7	2159.6	1992.2	1848.9	1724.8	1616.3
53.5	2621.2	2380.7	2180.6	2011.6	1866.9	1741.6	1632.0
54	2646.4	2403.6	2201.6	2031.0	1884.8	1758.3	1647.7
54.5	2671.7	2426.6	2222.6	2050.3	1902.8	1775.1	1663.5
55	2696.9	2449.5	2243.6	2069.7	1920.8	1791.9	1679.2
55.5	2722.2	2472.4	2264.7	2089.1	1938.8	1808.7	1694.9
56	2747.4	2495.4	2285.7	2108.5	1956.8	1825.5	1710.6
57	2797.9	2541.2	2327.7	2147.2	1992.8	1859.0	1742.1
58	2848.4	2587.1	2369.7	2186.0	2028.7	1892.6	1773.5
59	2898.9	2633.0	2411.7	2224.8	2064.7	1926.1	1805.0
60	2949.4	2678.8	2453.7	2263.5	2100.7	1959.7	1836.4
61	3000.0	2724.7	2495.7	2302.3	2136.6	1993.2	1867.9
62	3050.5	2770.6	2537.8	2341.0	2172.6	2026.8	1899.3
63	3101.0	2816.5	2579.8	2379.8	2208.6	2060.4	1930.8
64	3151.5	2862.3	2621.8	2418.6	2244.6	2093.9	1962.2
65	3202.0	2908.2	2663.8	2457.3	2280.5	2127.5	1993.7
66	3252.5	2954.1	2705.8	2496.1	2316.5	2161.0	2025.1
67	3303.0	3000.0	2747.8	2534.8	2352.5	2194.6	2056.6
68	3353.5	3045.8	2789.9	2573.6	2388.4	2228.1	2088.0
69	3404.0	3091.7	2831.9	2612.4	2424.4	2261.7	2119.4
70	3454.5	3137.6	2873.9	2651.1	2460.4	2295.3	2150.9
71	3505.0	3183.4	2915.9	2689.9	2496.4	2328.8	2182.3
72	3555.5	3229.3	2957.9	2728.6	2532.3	2362.4	2213.8
73	3606.0	3275.2	3000.0	2767.4	2568.3	2395.9	2245.2
74	3656.5	3321.1	3042.0	2806.2	2604.3	2429.5	2276.7
75	3707.0	3366.9	3084.0	2844.9	2640.2	2463.0	2308.1
76	3757.5	3412.8	3126.0	2883.7	2676.2	2496.6	2339.6
77	3808.0	3458.7	3168.0	2922.4	2712.2	3530.2	2371.0
78	3858.5	3504.5	3210.0	2961.2	2748.2	2563.7	2402.5
79	3909.0	3550.4	3252.1	3000.0	2784.1	2597.3	2433.9
80	3959.5	3596.3	3294.1	3038.7	2820.1	2630.8	2465.4
81	4010.1	3642.2	3336.1	3077.5	2856.1	2664.4	2496.8
82	4060.6	3688.0	3378.1	3116.2	2892.0	2697.9	2528.3
83	4111.1	3733.9	3420.1	3155.0	2928.0	2731.5	2559.7
84	4161.6	3779.8	3462.1	3193.7	2964.0	2765.1	2591.1
85	4212.1	3825.6	3504.2	3232.5	3000.0	2798.6	2622.6
86	4262.6	3871.5	3546.2	3271.3	3035.9	2832.2	2654.0
87	4313.1	3917.4	3588.2	3310.0	3071.9	2865.7	2685.5
88	4363.6	3963.3	3630.2	3348.8	3107.9	2899.3	2716.9
89	4414.1	4009.1	3672.2	3387.5	3143.8	2932.8	2748.4
90	4464.6	4055.0	3714.2	3426.3	3179.8	2966.4	2779.8
91	4515.1	4100.9	3756.3	3465.1	3215.8	3000.0	2811.3
92	4565.6	4146.7	3798.3	3503.8	3251.7	3033.5	2842.7
93	4616.1	4192.6	3840.3	3542.6	3287.7	3067.1	2874.2
94	4666.6	4238.5	3882.3	3581.3	3323.7	3100.6	2905.6
95	4717.1	4284.4	3924.3	3620.1	3359.7	3134.2	2937.1
96	4767.6	4330.2	3966.3	3658.9	3395.6	3167.7	2968.5
97	4818.1	4376.1	4008.4	3697.6	3431.6	3201.3	3000.0
98	4868.6	4422.0	4050.4	3736.4	3467.6	3234.8	3031.4
99	4919.1	4467.8	4092.4	3775.1	3503.5	3268.4	3062.8
100	4969.6	4513.7	4134.4	3813.9	3539.5	3302.0	3094.3

TABLE 6.5: BASE RESISTOR VALUES

	WIDTH						
LENGTH	5	7	9	11	13	15	17
12.5	216.4	166.6	135.5	114.1	98.6	86.8	77.5
13	223.8	172.4	140.1	118.1	102.0	89.8	80.2
13.5	231.3	178.1	144.8	122.0	105.4	92.8	82.8
14	238.8	183.9	149.5	125.9	108.8	95.8	85.5
14.5	246.2	189.6	154.2	129.9	112.2	98.8	88.2
15	253.7	195.4	158.8	133.8	115.6	101.7	90.9
15.5	261.1	201.1	163.5	137.7	119.0	104.7	93.5
16	268.6	206.8	168.2	141.7	122.4	107.7	96.2
16.5	276.1	212.6	172.8	145.6	125.8	110.7	98.9
17	283.5	218.3	177.5	149.6	129.2	113.7	101.6
17.5	291.0	224.1	182.2	153.5	132.6	116.7	104.2
18	298.5	229.8	186.9	157.4	136.0	119.7	106.9
18.5	305.9	235.6	191.5	161.4	139.4	122.7	109.6
19	313.4	241.3	196.2	165.3	142.8	125.7	112.2
19.5	320.8	247.1	200.9	169.2	146.2	128.7	114.9
20	328.3	252.8	205.6	173.2	149.6	131.7	117.6
20.5	335.8	258.6	210.2	177.1	153.0	134.7	120.3
21	343.2	264.3	214.9	181.1	156.4	137.7	122.9
21.5	350.7	270.1	219.6	185.0	159.8	140.7	125.6
22	358.2	275.8	224.2	188.9	163.2	143.7	128.3
22.5	365.6	281.6	228.9	192.9	166.6	146.7	131.0
23	373.1	287.3	233.6	196.8	170.0	149.7	133.6
23.5	380.5	293.1	238.3	200.7	173.4	152.6	136.3
24	388.0	298.8	242.9	204.7	176.8	155.6	139.0
24.5	395.5	304.5	247.6	208.6	180.2	158.6	141.7
25	402.9	310.3	252.3	212.5	183.6	161.6	144.3
25.5	410.4	316.0	257.0	216.5	187.0	164.6	147.0
26	417.9	321.8	261.6	220.4	190.4	167.6	149.7
26.5	425.3	327.5	266.3	224.4	193.8	170.6	152.4
27	432.8	333.3	271.0	228.3	197.2	173.6	155.0
27.5	440.2	339.0	275.7	232.2	200.6	176.6	157.7
28	447.7	344.8	280.3	236.2	204.0	179.6	160.4
28.5	455.2	350.5	285.0	240.1	207.4	182.6	163.1
29	462.6	356.3	289.7	244.0	210.8	185.6	165.7
29.5	470.1	362.0	294.3	248.0	214.2	188.6	168.4
30	477.6	367.8	299.0	251.9	217.6	191.6	171.1
30.5	485.0	373.5	303.7	255.9	221.0	194.6	173.7
31	492.5	379.3	308.4	259.8	224.4	197.6	176.4
31.5	500.0	385.0	313.0	263.7	227.8	200.5	179.1
32	507.4	390.8	317.7	267.7	231.2	203.5	181.8
32.5	514.9	396.5	322.4	271.6	234.6	206.5	184.4
33	522.3	402.2	327.1	275.5	238.0	209.5	187.1
33.5	529.8	408.0	331.7	279.5	241.4	212.5	189.8
34	537.3	413.7	336.4	283.4	244.8	215.5	192.5
34.5	544.7	419.5	341.1	287.4	248.2	218.5	195.1
35	552.2	425.2	345.7	291.3	251.7	221.5	197.8
35.5	559.7	431.0	350.4	295.2	255.1	224.5	200.5
36	567.1	436.7	355.1	299.2	258.5	227.5	203.2
37	582.0	448.2	364.4	307.0	265.3	233.5	208.5
38	597.0	459.7	373.8	314.9	272.1	239.5	213.9
39	611.9	471.2	383.1	322.8	278.9	245.5	219.2
40	626.8	482.7	392.5	330.7	285.7	251.4	224.5
41	641.7	494.2	401.8	338.5	292.5	257.4	229.9
42	656.7	505.7	411.2	346.4	299.3	263.4	235.2
43	671.6	517.2	420.5	354.3	306.1	269.4	240.6
44	686.5	528.7	429.9	362.2	312.9	275.4	245.9
45	701.4	540.2	439.2	370.0	319.7	281.4	251.3
46	716.4	551.7	448.5	377.9	326.5	287.4	256.6
47	731.3	563.2	457.9	385.8	333.3	293.4	262.0
48	746.2	574.7	467.2	393.7	340.1	299.4	267.3

LENGTH	WIDTH						
	5	7	9	11	13	15	17
49	761.1	586.2	476.6	401.5	346.9	305.3	272.7
50	776.1	597.7	485.9	409.4	353.7	311.3	278.0
51	791.0	609.1	495.3	417.3	360.5	317.3	283.4
52	805.9	620.6	504.6	425.1	367.3	323.3	288.7
53	820.8	632.1	514.0	433.0	374.1	329.3	294.1
54	835.8	643.6	523.3	440.9	380.9	335.3	299.4
55	850.7	655.1	532.7	448.8	387.7	341.3	304.8
56	865.6	666.6	542.0	456.6	394.5	347.3	310.1
57	880.5	678.1	551.4	464.5	401.3	353.2	315.5
58	895.5	689.6	560.7	472.4	408.1	359.2	320.8
59	910.4	701.1	570.0	480.3	414.9	365.2	326.2
60	925.3	712.6	579.4	488.1	421.7	371.2	331.5
61	940.2	724.1	588.7	496.0	428.5	377.2	336.8
62	955.2	735.6	598.1	503.9	435.3	383.2	342.2
63	970.1	747.1	607.4	511.8	442.1	389.2	347.5
64	985.0	758.6	616.8	519.6	448.9	395.2	352.9
65	1000.0	770.1	626.1	527.5	455.7	401.1	358.2
66	1014.9	781.6	635.5	535.4	462.5	407.1	363.6
67	1029.8	793.1	644.8	543.3	469.3	413.1	368.9
68	1044.7	804.5	654.2	551.1	476.1	419.1	374.3
69	1059.7	816.0	663.5	559.0	482.9	425.1	379.6
70	1074.6	827.5	672.8	566.9	489.7	431.1	385.0
71	1089.5	839.0	682.2	574.8	496.5	437.1	390.3
72	1104.4	850.5	691.5	582.6	503.4	443.1	395.7
73	1119.4	862.0	700.9	590.5	510.2	449.1	401.0
74	1134.3	873.5	710.2	598.4	517.0	455.0	406.4
75	1149.2	885.0	719.6	606.2	523.8	461.0	411.7
76	1164.1	896.5	728.9	614.1	530.6	467.0	417.1
77	1179.1	908.0	738.3	622.0	537.4	473.0	422.4
78	1194.0	919.5	747.6	629.9	544.2	479.0	427.8
79	1208.9	931.0	757.0	637.7	551.0	485.0	433.1
80	1223.8	942.5	766.3	645.6	557.8	491.0	438.5
82	1253.7	965.5	785.0	661.4	571.4	502.9	449.1
84	1283.5	988.5	803.7	677.1	585.0	514.9	459.8
86	1313.4	1011.4	822.4	692.9	598.6	526.9	470.5
88	1343.2	1034.4	841.1	708.6	612.2	538.9	481.2
90	1373.1	1057.4	859.8	724.4	625.8	550.8	491.9
92	1402.9	1080.4	878.5	740.1	639.4	562.8	502.6
94	1432.8	1103.4	897.1	755.9	653.0	574.8	513.3
96	1462.6	1126.4	915.8	771.6	666.6	586.8	524.0
98	1492.5	1149.4	934.5	787.4	680.2	598.8	534.7
100	1522.3	1172.4	953.2	803.1	693.8	610.7	545.4

7. DIODES AND JUNCTION CAPACITORS

This subject is covered in more detail in part IV of the VTC Design Manual.

7.1 Schottky Diodes

The VL1000 allows the user to create a variety of Schottky diode types and sizes. Schottky diodes are extensively discussed in Sections 26 and 27 of the Design Manual. Schottky diodes cannot carry arbitrarily large currents -- the *upper limit* is 10 μA per square micron of Schottky area.

The LHD_LIB component set has several standard Schottky diode geometries as described in the Mentor Instructions of the Design System. The maximum current for the overlap Schottky diodes SD1 and SD3 is 1.0mA and 3.0mA. The minimum breakdown voltage for an overlap Schottky diode is 8V. The maximum current for the guardring Schottky diodes SDGR1 and SDGR2 is 0.15 mA and 0.3mA. The minimum breakdown voltage for guardring Schottky diodes is 25V. Nonstandard Schottky diode geometries can be created if needed. The various dimensions needed to specify a nonstandard Schottky diode can be found in the accompanying Schottky diode tables (Tables 7.1 and 7.2).

7.2 Junction Capacitors

The LHD process does not provide true dielectric capacitors. However, in many cases it is possible to use (nonlinear) junction capacitors for such purposes as stabilizing (compensating) and feedback loops. The procedures for using junction capacitors in the LHD_LIB component set are described in the Mentor Graphics instructions in the Design System. The designer should remember that the capacitance value specified is the value at zero bias voltage and with any substantial reverse bias the capacitance will be lower. The breakdown voltages and junction capacitance for the TYPE A capacitor is 25 volts and 3.2E-4 pF per square micron. The breakdown voltage and junction capacitance for the TYPE C capacitor is 5 volts and 1.2E-3 pF per square micron.

7.3 Zener Diodes

A Zener diode is created by operating a diode-connected NPN transistor with the EB junction in reverse avalanche breakdown. This results in a constant voltage of about 6V, and is used in DC reference voltage sources and also in level shifters. The "Zener voltage" is the same as the NPN transistor parameter BVebo, and its values and limits can be found inTable 5.2.

The SPICE models are in the LHD_LIB Mentor data base and the needed components are created automatically when the symbol is used. The details of Zener diodes are discussed further in Sections 32 and 33 of VTC's Design Manual.

TABLE 7.1: OVERLAP SCHOTTKY DIODES

The maximum current listed here is an absolute upper limit. In practical designs, the forward drop may limit currents to lower values.

This device has an N+ anode contact of width CW. "Length" is parallel to current flow (PERP to contact STRIPE). W and L are the dimensions of the Schottky opening. CW is the width of the cathode contact STRIPE. Use Linear Interpolation for unlisted sizes.

L	*W*	*CW*	I_{MAX} *(mA)*
12	10	6	1.53
12	20	6	2.87
12	30	6	4.21
12	40	6	5.55
12	50	6	6.89
12	60	6	8.23
12	70	6	9.57
12	80	6	10.91
16	20	7	3.72
16	30	7	5.46
16	40	7	7.20
16	50	7	8.94
16	60	7	10.68
16	70	7	12.42
16	80	7	14.16
20	20	8	4.58
20	30	8	6.72
20	40	8	8.86
20	50	8	11.00
20	60	8	13.14
20	70	8	15.28
20	80	8	17.42
24	30	9	7.98
24	40	9	10.52
24	50	9	13.06
24	60	9	15.60
24	70	9	18.14
24	80	9	20.68
28	30	10	9.23
28	40	10	12.17
28	50	10	15.11
28	60	10	18.05
28	70	10	20.99
28	80	10	23.93

TABLE 7.2: GUARD-RING SCHOTTKY DIODES

The maximum current listed here is an absolute upper limit. In practical designs the forward drop may limit currents to lower values.

This device has an N+ anode contact of width CW. "Length" is parallel to current flow (PERP to contact STRIPE). W and L are the dimensions of the P contact opening. CW is the width of the Cathode contact STRIPE. Use Linear Interpolation for unlisted sizes.

L	*W*	*CW*	I_{MAX} *(mA)*
18	30	6	2.67
18	40	6	3.81
18	50	6	4.95
18	60	6	6.09
18	70	6	7.23
18	80	6	8.37
18	90	6	9.51
22	30	7	3.60
22	40	7	5.14
22	50	7	6.68
22	60	7	8.22
22	70	7	9.76
22	80	7	11.30
22	90	7	12.84
26	40	8	6.48
26	50	8	8.42
26	60	8	10.36
26	70	8	12.30
26	80	8	14.24
26	90	8	16.18
30	40	9	7.82
30	50	9	10.16
30	60	9	12.50
30	70	9	14.84
30	80	9	17.18
30	90	9	19.52
34	50	10	11.89
34	60	10	14.63
34	70	10	17.37
34	80	10	20.11
34	90	10	22.85

7.3.1 Zener Matching

In some cases (for example differential level shifters) the matching of Zener voltages between transistors may be important. It is found that the standard deviation of the difference in Zener voltages for two identical Zener-connected NPNs (with identical currents) is about 5mV, provided the following current levels are maintained:

TABLE 7.1: CURRENT LIMITS FOR MATCHED ZENER DIODES

ZENER TYPE	I_{MIN}	I_{MAX}	*UNIT*
D3	.1	.5	mA
D12	.25	1.25	mA

8. PROPERTIES OF THE INTERCONNECTIONS

The resistance and capacitance of interconnections (the "lines" in the schematic) are usually neglected in discrete-component designs. In integrated design this is not always possible — the interconnections are less than ideal. Typical data on interconnection capacitances are given in part VI of the Design Manual.

A unique feature of integrated design is the presence of *electromigration* — a wear-out mechanism for the interconnections. In order to prevent failure from this the currents in interconnection lines must be limited. Detailed information is given in part VI of the Design Manual. To avoid reliability problems from this, *any interconnection line carrying more than 4mA should be called to the attention of VTC* when the schematic is transferred.

9. WORST-CASE *SPICE* SIMULATIONS

Usually the initial SPICE simulations are done under nominal" conditions — nominal supply voltages, room temperature, etc. This is a good way to proceed to get the circuits defined and show that the desired circuit functions are realized. However, there are significant variations in the "environment" seen by the chip — the supply voltage, temperature, etc. These variations are sufficiently serious that "nominal" designs often fail to work correctly at the limits of supply voltage and temperature. A set of simulation conditions which should be used to verify satisfactory operation over a variety of conditions is outlined below.

9.1 Temperature

The SPICE models contain the temperature dependence of the transistor currents and voltages, and give a realistic account of temperature variation. Some significant temperature effects are: a) The transistor Vbe drops at about 1.7-1.9 mV/deg C; b) The resistors increase in value as temperature rises; c) Beta increases with temperature.

The temperature in the SPICE simulation is the *junction temperature* — the actual temperature of the chip. To find this temperature it is necessary to know the package type for the chip, the thermal conductance of the package for the type of cooling used, and the chip power dissipation. For most commercial applications assumption of 0° and 125°C for worst-case temperature extremes is reasonable.

9.2 Supply Voltage

Ordinarily the supply voltages are specified as ± 10%. Thus a 5V chip should be simulated at 4.5 and 5.5V. If there are two supply voltages, 5 and 12V, all four combinations should be simulated: (4.5, 13.2), (4.5, 10.8), (5.5, 13.2), (5.5, 10.8).

Difficulties are usually seen at worst-case low voltage and low temperature. Here Vbe is high, the supply voltage is low, and beta is low. A common source of difficulty is inadequate collector-base bias for some transistors, resulting in saturation and erroneous operation.

9.3 Beta

Beta is hard to control accurately in manufacturing, and often affects important chip parameters. Thus, simulations should be done for the worst-case beta limits given in this User's Guide and proper operation verified for the entire range of beta. Worst-case models for low and high beta are provided in the Mentor data base.

9.4 Resistor Values

As noted above, the resistors are of two types, base and implant, and vary independently. The tolerances are given in Section 5 of the Custom Dell Design section of this User's Guide. If, for example, the tolerances are ±20%, there are four cases to cover:

All base resistors made 1.2x their nominal values
All implant resistors made 1.2x their nominal values

All base resistors made 0.8x their nominal values
All implant resistors made 1.2x their nominal values

All base resistors made 1.2x their nominal values
All implant resistors made 0.8x their nominal values

All base resistors made 0.8x their nominal values
All implant resistors made 0.8x their nominal values

The resistor tolerance can be chosen at the time of circuit expansion (see Mentor instructions).

9.5 Component Matching

Some circuits are very sensitive to transistor and resistor matching and should be simulated for worst-case (or statistical) matching as described in sections 4, 5, and 6.

TESTING FOR THE VL1000

Two options are available for testing the VL1000.

OPTION 1

The customer specifies an elementary DC functional test program by completing the forms on the following pages. Although this test method is not thorough enough for a full production test, it is sufficient for prototypes and preproduction samples. When the parts have been checked and characterized by the customer, a complete production test can then be defined using option 2.

Option 1 testing is included in the basic VL1000 development costs.

OPTION 2

Additional testing is available when the customer requires a full production test. In Option 2, the customer submits a well defined specification for the VL1000 circuit including the following information:

- A brief functional description of the circuit
- A schematic or block diagram of the circuit
- A package pin assignment diagram of the circuit
- DC and functional requirements with any associated test diagrams. DC and functional requirements may be specified over commercial temperature and power supply voltage range.
- AC test requirements with any associated test diagrams. AC requirements can only be specified at 25°C and normal power supply voltage.
- Package requirements
- If appropriate, a burn-in connection diagram with specified time and temperature

VTC's semicustom applications engineers are available for assistance.

Option 2 testing is not included in the basic VL1000 development cost, but is quoted for individual circuit test specifications. Typical costs are available on request. Burn-in testing also requires a separate quotation.

OPTION 1 TESTING METHOD

Packaged sample parts are tested on VTC's ATE. Option 1 testing is a simple DC functional and parametric test (force and measure voltages and currents). Devices of more than 40 pins require special test hardware and a special quote. VL1000 users must provide the following information:

Load Schematic: Using the schematic shown in Figure 1, draw connections for loads (shorts, diodes, resistors and/or capacitors) between any of the DUT pins as required. (Note that a 40-pin DUT is shown in the drawing. Edit pinouts for devices of less than 40 pins or prepare a special schematic for devices of more than 40 pins.) The diodes are 1N914s. The resistors are1%, 1/4W, metal-film resistors of values from 10.0 ohms to 1 megaohm. All available resistor values are listed in Table 1. The capacitors are 10%, >50VDC, radial leaded monolithic ceramic capacitors of values from 10pF to 2.2μF. All available capacitor values are listed in Table 2. Other values or types of diodes, resistors and capacitors may be used if supplied by the VL1000 user.

Test Step Specification: Fill out the test specification sheet (Figure 2) for every test desired. Several pins may be measured in a single test step. Any pin may be simultaneously forced and measured in the same test step. Voltages of +1.00mV to +100V and currents of +5nA to +256mA may be forced and/or measured.

TABLE 1: READILY AVAILABLE LOAD RESISTOR VALUES (IN OHMS)

10.0	12.1	15.0	20.0	24.9	30.1	39.2	49.9
51.1	60.4	75.0	82.5	90.9	100	133	150
182	200	221	249	301	332	392	402
432	475	499	511	604	634	698	750
825	909	1000	1100	1210	1400	1500	2000
2100	2430	2490	2800	3010	3240	3320	3920
4020	4220	4530	4640	4750	4990	5110	5230
5620	6040	6490	6810	6980	7500	8060	8250
9090	9530	10.0K	11.0K	12.1K	13.0K	15.0K	15.8K
16.2K	18.2K	20.0K	21.0K	22.1K	24.3K	24.9K	28.0K
30.1K	35.7K	36.5K	39.2K	40.2K	46.4K	49.9K	51.1K
56.2K	60.4K	61.9K	68.1K	69.8K	75.0K	80.6K	82.5K
90.9K	100K	110K	121K	130K	140K	150K	178K
200K	210K	221K	232K	267K	301K	332K	357K
402K	453K	475K	499K	511K	604K	750K	1.00M

TABLE 2: READILY AVAILABLE CAPACITOR VALUES

10pF	12pF	15pF	18pF
22pF	27pF	33pF	47pF
56pF	68pF	82pF	100pF
120pF	150pF	220pF	330pF
470pF	680pF	820pF	.001mF
.0015mF	.0022mF	.0033mF	.0047mF
.0056mF	.0068mF	.01mF	.015mF
.022mF	.033mF	.047mF	.068mF
.1mF	.15mF	.22mF	.33mF
.47mF	.68mF	1.0mF	2.2mF

Figure 1: DUT Schematic:

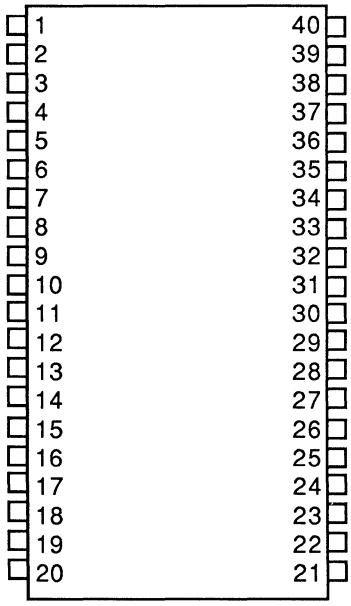


Figure 2: Test Specification Sheet

VL1000 TEST SPECIFICATION SHEET (PAGE of)												
TEST NO.												
TEST NAME												
PIN	*FORCE*	*MEASURE*		*FORCE*	*MEASURE*		*FORCE*	*MEASURE*		*FORCE*	*MEASURE*	
		MIN	*MAX*		*MIN*	*MAX*		*MIN*	*MAX*		*MIN*	*MAX*
1												
2												
3												
4												
5												
35												
36												
37												
38												
39												
40												

DESIGNER'S CHECKLIST

This check list is provided for the designer to identify all items to complete before the design is finished.

DESIGN

☐ DC performance characteristics checked by simulation.
☐ Critical AC performance characteristics checked by simulation.
☐ Breakdown voltage limits not exceeded.
☐ Worst-case simulation performed over temperature, power supply voltage, beta, and resistance variations. DC, AC, and proper circuit bias characteristics maintained over all conditions. Transistor saturation avoided under all conditions.
☐ Critical circuits simulated for resistor and/or transistor mismatch.
☐ Circuits with multiple supply voltages analyzed for possible power sequencing problems.
☐ Maxirnum chip power dissipation within acceptable limits for package used.

INFORMATION RETURNED TO VTC

☐ Complete circuit schematic.
☐ Table of resistor number versus type, length, and width for user-designed cells.
☐ The schematic should note any currents greater than 4 mA.
☐ The designer should supply information on which elements (if any) require close matching.
☐ The designer should supply information on which (if any) resistors may need adjustment during a second pass and what range of adjustment may be required.
☐ Package type and pinout.
☐ Electrical Specification.
☐ The designer should supply information in which (if any) digital timing paths have critical timing requirements.

VL2000

HIGH-PERFORMANCE BIPOLAR DIGITAL CELL LIBRARY

FEATURES

- Ultra High Gate Speed:
  - -High Power Option, 1 Load = 440pSec
  - -Low Power Option, 1 Load = 800pSec
- Low Power:
  - -1000 Gates, 40-Pin Circuit = 1.0 Watt Typical*
  - -4000 Gates, 84-Pin Circuit = 3.0 Watt Typical*
- High-Density 2.0 Micron Process
- Digital Clock Rates to 500MHz
- Cell Library of Digital Functions
- Two Speed/Power Options for Most Cells
- ECL10KH or TTL Input/Output Available
- Commercial or Military Temperature Range With Full Voltage Compensated ECL10KH Compatibility
- Mainframe, Workstation or PC-Based
- Suitable for +5, -5 or -5.2 Volt Supplies
- Available in Industry-Standard Packages

**Based on one-third of the cells using the high power option and two-thirds of the cells using the low power option; input/outputs evenly split.*

APPLICATIONS

- High-Speed Computers
- Communications
- Local Area Networks
- Instrumentation
- Digital Signal Processing
- LSI Replacement for ECL Logic
- LSI Replacement for High-Speed TTL Logic

DESCRIPTION

The VL2000 High Performance Bipolar Digital Cell Library provides the ultra high-speed logic functions at comparatively low power levels. The VL2000 library contains a wide selection of digital functions, memory cells and either ECL10KH or TTL inputs or outputs. The I/O cells can be mixed on any given design.

Most logic cells have two speed/power levels, allowing speed to be traded for power dissipation as required in the design. Critical paths can use fast, high-power cells, while the more numerous noncritical paths can use slow, low-power cells.

The VL2000 has design options that are mainframe, workstation or personal computer-based, and it provides the systems designer a simple, straightforward means to integrate either new or existing designs.

DESIGNING WITH THE VL2000

The VL2000 Design System includes:

- VL2000 Data Sheet
- VL2000 User's Guide
- VL2000 Database

Using a workstation, the designer can enter and simulate a custom design with the library's predesigned cells.

The methods used in the VL2000 result in an efficient, quick-turn, error-free design.

When circuit simulation is complete, a diskette or tape is sent to VTC for circuit layout and fabrication. Layout time is minimal because only the cells need to be interconnected.

Samples are fully tested to user-supplied specifications.

DIGITAL CELLS:

	TYPICAL PERFORMANCE (5v, T_A = 25°C, Fanout of 1)					
	HIGH			LOW		
NAME	t,pSec	P,mW	AREA (mil²)	t,pSec	P,mW	AREA (mil²)
SIMPLE GATES						
2 Input OR	420	2.25	16.46	790	0.750	18.02
3 Input OR	420	2.25	23.80	810	0.750	23.58
4 Input OR	440	2.25	23.80	860	0.750	27.36
2 Input OR-NOR	420	2.25	16.46	770	0.750	18.02
3 Input OR-NOR	430	2.25	23.80	850	0.750	23.58
4 Input OR-NOR	465	2.25	23.80	895	0.750	27.36
3 Input AND	805	2.25	24.91	1575	0.750	24.91
2 Input AND-NAND	600	2.25	24.02	1095	0.750	24.02
2-2 OR-AND-Invert	660	2.25	28.03	1245	0.750	28.03
3-3 OR-AND-Invert	700	2.25	32.03	1400	0.750	32.03
2 Input EX-OR-NOR	530	2.25	31.14	1050	0.750	31.14
FLIP-FLOPS						
Data Latch W/Reset	675	2.25	28.03	1450	0.750	28.03
Set Reset Latch, Overriding Reset	650	2.25	25.58	1400	0.750	25.58
Data Latch, Multiplexed Data Inputs	615	2.25	36.92	1440	0.750	36.92
Data Flip-Flop w/Multiplexed Data Input	705	4.50	55.61	1535	1.50	55.61
Data Flip-Flop With Reset	875	4.50	50.26	1900	1.50	50.26
Toggle Flip-Flop, Asynchronous Reset	880	11.25	93.42	1880	3.75	93.42
JK Flip-Flop, Asynchronous Reset	880	11.25	93.42	1880	3.75	93.42
INPUT/OUTPUT BUFFERS						
10KH Input Buffer	450	**2.34**	22.67	—	—	—
Differential Input Receiver	475	**3.90**	36.09	—	—	—
Inverting 10KH Output Buffer	1500	**19.24**	**37.48**	—	—	—
Non-Inverting 10KH Output Buffer	1500	**19.24**	**37.48**	—	—	—
Differential Output Driver	1100	**19.24**	33.78	—	—	—
Inverting and Non-Inverting TTL Input Buffer	325	4.50	24.98	—	—	—
Inverting Bistate TTL Output Buffer	4150	10.00	97.62	—	—	—
Non-Inverting Bistate TTL Output Buffer	4150	10.00	97.62	—	—	—
Inverting Tristate TTL Output Buffer	4450	10.00	**103.87**	—	—	—

DIGITAL CELLS (cont'd):

	TYPICAL PERFORMANCE (5v, T_A= 25°C, Fanout of 1)					
	HIGH			*LOW*		
NAME	*t,pSec*	*P,mW*	*AREA (mil²)*	*t,pSec*	*P,mW*	*AREA (mil²)*
Non-Inverting Tristate TTL Output Buffer	4450	10.00	**103.87**	—	—	—
Tristate Output Buffer Enable Gate	3000	10.30	68.71	—	—	—
Inverting Open Collector TTL Output Buffer	9400	10.00	**94.85**	—	—	—
Non-Inverting Open Collector TTL Output Buffer	9400	10.00	**94.85**	—	—	—
MSI AND LSI FUNCTIONS						
Decoder 1 of 4	470	2.25	31.14	880	0.750	31.14
Decoder 1 of 8	IN DEVELOPMENT					
MUX 2 Input (A)	475	2.25	24.47	950	0.750	24.47
MUX 2 Input (B)	450	2.25	24.47	850	0.750	24.47
MUX 4 Input	575	2.25	49.38	1375	0.750	49.38
Shift Register, 4 Bit	IN DEVELOPMENT					
Counter, 4 Bit	IN DEVELOPMENT					
Comparator, 4 Bit	IN DEVELOPMENT					
Carry Look Ahead, 4 Bit	IN DEVELOPMENT					
Parity Generator Checker, 9 Bit	IN DEVELOPMENT					
Full Adder, 2 Bit	1130	7.02	56.05	2280	2.25	56.05
Priority Interrupt Encoder	IN DEVELOPMENT					
2901, 4 Bit **ALU**	IN DEVELOPMENT					
RAM, 16 x 4 Dual Port	IN DEVELOPMENT					
SPECIAL PURPOSE						
Level Shift Down L	110	0.750	16.68	—	—	—
Level Shift Down M	60	2.25	16.68	—	—	—
Level Shift Down H	40	8.00	18.46	—	—	—
Clock Driver	505	38.50	72.51	—	—	—
Signal Buffer	IN DEVELOPMENT					
Shifter, Positive to Negative	IN DEVELOPMENT					
Shifter, Negative to Positive	IN DEVELOPMENT					
BIAS GENERATORS						
Master Bias	—	28.08	250.53	—	—	—
Internal Bias	—	11.70	47.42	—	—	—
TTL Reference	—	1.60	22.21	—	—	—

VL2001

EVALUATION CHIP FOR THE VL2000 HIGH-PERFORMANCE BIPOLAR DIGITAL CELL LIBRARY

FEATURES

- High Speed D Flip-Flop, F_{TOG} = 500 MHz Typ.
- Low Power D Flip-Flop, I_{EE} = 320µA Max.
- High Speed DATA LATCH, Propagation Delays = 700ps Typ.
- Low Power DATA LATCH, I_{EE} = 195µA, Max.
- Each Cell is ECL 10KH Buffered and Includes a Reset Pin

DESCRIPTION

The VL2001 Evaluation Chip is an integrated sample of four digital cells from the VL2000 High Performance Bipolar Digital Cell Library. The chip contains examples of four digital functions. All inputs and outputs to the cells are pinned out to allow the user to evaluate each part independently.

High Speed D Flip-Flop:

This circuit offers a high toggle frequency flip-flop that triggers on the high-to-low transition of the clock pulse.

Low Power D Flip-Flop:

This circuit contains a low power version of the high speed D flip-flop.

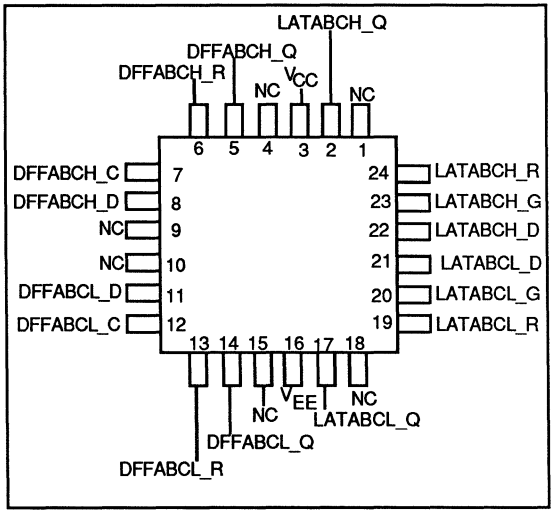
High Speed Data Latch:

This circuit contains a high speed data latch complete with reset.

Low Power Data Latch:

This circuit offers the option of a v DATA LATCH low power.

CONNECTION DIAGRAM



TRUTH TABLES

DFFABCH & DFFABCL			
R	C	D	Q
L	X	X	L
H	↓	L	H
H	↓	H	L
H	⊣	X	Q_N

LATABCH & LATABCL			
R	G	D	Q
L	X	X	L
H	H	L	H
H	H	H	L
H	L	X	Q_N

H = HIGH Voltage Level Steady State
L = LOW Voltage Level Steady State
X = Don't Care
↓ = HIGH-to-LOW Clock Transition
⊣ = Not a HIGH-to-LOW Clock Transition

NOTE: Truth table information pertains to logic state present at the package pin. Refer to circuit diagrams for details.

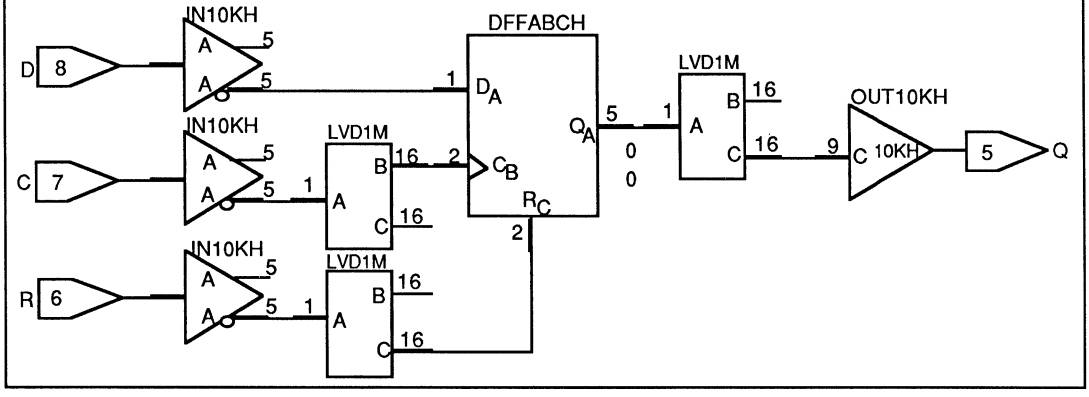
BIPOLAR SEMICUSTOM

D FLIP-FLOP SPECIFICATIONS

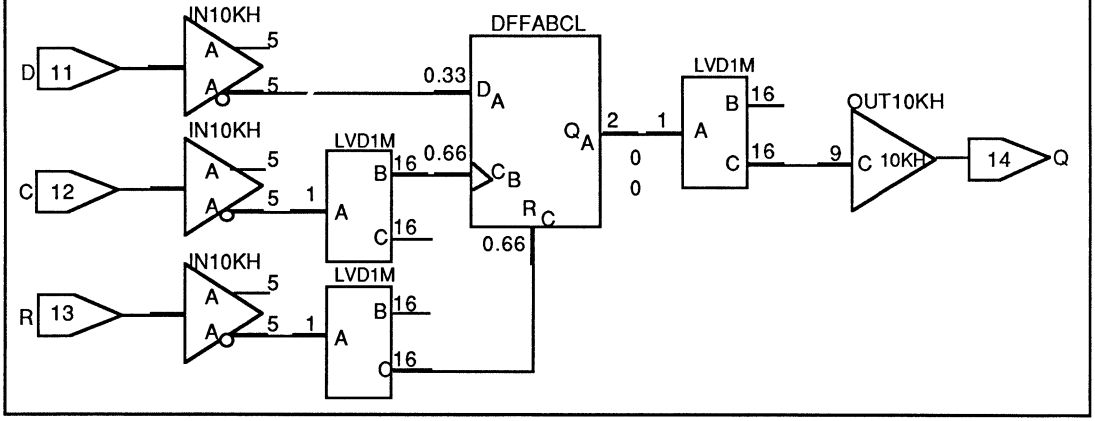
PARAMETER			HIGH SPEED	LOW POWER	UNITS
Test	In	Out			
I_{EE}			9.26 Max	7.46 Max	mA
T_{PHL}	C	Q	3320	4420	ps
T_{PLH}	C	Q	2980	3970	ps
T_{PHL}	R	Q	3030	3600	ps
T_{SET}			1000 Min	2500 Min	ps
T_{HOLD}			0	0	ps
R	Pulse Width Low		600	1200	ps
C	Pulse Width High		1000	2000	ps
F_{MAX}			230	145	MHz

NOTE: All specified delay times take into account the additional delays introduced by the ECL10KH input/output buffers and voltage level shifters.

HIGH SPEED D-FLIP-FLOP CIRCUIT



LOW POWER D-FLIP-FLOP CIRCUIT

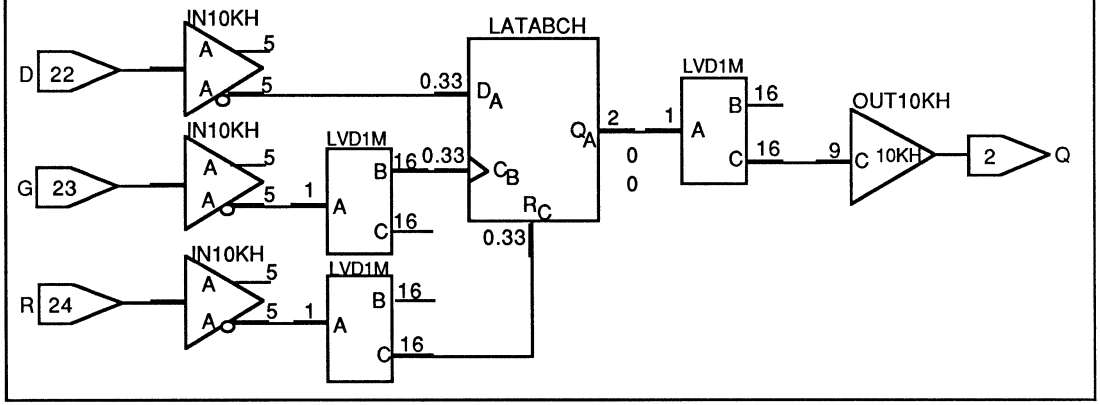


DATA LATCH SPECIFICATIONS

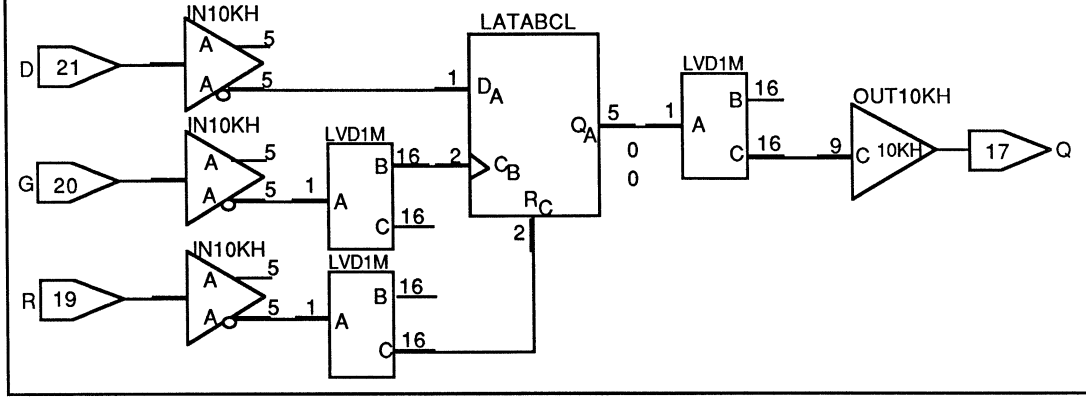
PARAMETER			HIGH SPEED	LOW POWER	UNITS
Test	In	Out			
I_{EE}			8.79 Max	7.34 Max	mA
T_{PHL}	D	Q	3000	3570	ps
T_{PLH}	D	Q	2790	3730	ps
T_{PHL}	G	Q	3250	4320	ps
T_{PLH}	G	Q	2840	3930	ps
T_{PHL}	R	Q	3030	3560	ps
T_{SET}			700	1700	ps
T_{HOLD}			0	0	ps
R	Pulse Width Low		600	1200	ps
G	Pulse Width High		900	2000	ps

NOTE: All specified delay times take into account the additional delays introduced by the ECL10KH input/output buffers and voltage level shifters.

HIGH SPEED DATA LATCH CIRCUIT

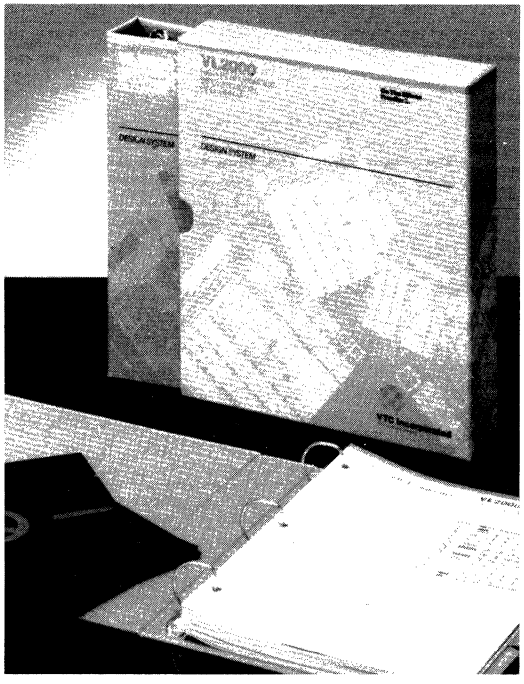


LOW POWER DATA LATCH CIRCUIT



DESIGN SYSTEM

VL2000 HIGH-PERFORMANCE BIPOLAR DIGITAL CELL LIBRARY



FEATURES

- Data Sheet
- User's Guide
- Design Manual
- Design Notes
- Evaluation Chip Data Sheet (Chip Available on Request)
- Database Software
- Technical Support

APPLICATIONS

- High Speed Computers
- Communications
- Local Area Networks
- Instrumentation
- Digital Signal Processing
- LSI Replacement for ECL Logic
- LSI Replacement for High Speed TTL Logic

DESCRIPTION

The information and procedures given in the VL2000 High Performance Bipolar Digital Cell Library System result in efficient, quick-turn, error-free designs.

The designer can implement complex digital LSI designs on a single integrated circuit using the cell library provided with the VL2000 Design System.

The VL2000 User's Guide contains instructions for loading the cell library on the user's workstation or personal computer. The database software includes the cell library with all specifications needed to begin designing. The User's Guide describes how to create diagrams using the VL2000 cells and how to execute simulations. A summary description and specification for each cell is given, along with digital cell design guidelines and specifications. The use of predesigned cells makes custom designing easy.

A set of Design Notes which give helpful information on various design methods are a part of the design system.

Testing requirements and packaging characteristics are also described.

The VL2000 Design System gives the engineer the information needed to begin designing integrated circuitry. It assists engineering and development organizations in their attempt to incorporate application-specific LSI and VLSI chips into their products.

VTC offers technical support for design system users whenever necessary.

VL2000

HIGH-PERFORMANCE BIPOLAR DIGITAL CELL LIBRARY

ADVANCE INFORMATION

CELL RELEASE 2.0

(Planned for Q1 1986 Availability)

- Decoder, 1 of 8
- Shift Register, 4-Bit
- Counter, 4-Bit
- Comparator, 5-Bit
- Carry Look Ahead, 4-Bit
- Parity Generator Checker, 9-Bit
- Priority Interrupt Encoder
- 2901, 4-Bit ALU
- RAM, 16x4 Dual Port
- Shifter, Positive to Negative
- Shifter, Negative to Positive
- TTL Tristate Buffers
- TTL Open Collector Buffers
- TTL Bistate Buffers

CELL RELEASE 3.0

(Planned for Q3 1986 Availability)

- 6-Bit Digital-to-Analog Converter
- 8-Bit Digital-to-Analog Converter
- 6-Bit Analog-to-Digital Converter
- 8-Bit Analog-to-Digital Converter
- 710 Comparator
- CML-Compatible Comparator
- Voltage Reference
- RS-422/423 Line Driver
- RS-422/423 Line Receiver
- Backplane Transceiver
- 8288 Bus Controller
- 733 Video Amp
- DAC Bandgap Current Sources

VL2000
HIGH-PERFORMANCE BIPOLAR DIGITAL CELL LIBRARY USER'S GUIDE

VL2000 USER'S GUIDE CONTENTS

TABLES

FIGURES

FOREWORD

VTC's VL2000 High Performance Bipolar Digital Cell Library uses versatile LSI design techniques, and allows digital and memory functions in the same circuit.

The VL2000 User's Guide contains information necessary to complete a circuit design. A detailed review of the User's Guide is recommended before proceeding.

The User's Guide consists of the following information:

Digital Cell Design Guidelines and Specifications — This section gives a digital cell summary, guidelines for designing with digital cells and specifications for each of the cells.

Testing — This section describes how to specify circuit test requirements in order to ensure first time circuit success.

Customer Interface — Here the designer is given information on ordering, schedules, responsibilities and the assistance available from VTC.

Packaging — The VL2000 Design System packaging section describes the dimensions and thermal characteristics of the packages available for the VL2000.

The VL2000 gives a new outlook to LSI cell design. Proper use of the User's Guide will help make the first pass a success.

CUSTOMER INTERFACE

The Interface between VTC and the customer for the VL2000 High Performance Digital Bipolar Cell Library involves several issues.

Technical Support — General technical support is available at no cost and can be arranged by calling a VTC representative.

Ordering — After the customer has completed the VL2000 design, a purchase order is necessary to initiate layout and fabrication efforts at VTC. Each circuit is quoted individually and quotes can be requested at any time. VTC's quote, however, is only valid for the final design submitted for integration.

Custom Cells — If a custom cell is required as part of the design, it should be discussed with VTC as early in the design cycle as possible. This will enable VTC to allocate the necessary resources to do the cell layout prior to circuit integration.

Packaging — Information concerning package requirements must be defined at the time the circuit purchase order is submitted.

Testing — Test requirements must be defined at the time the circuit purchase order is initiated.

Special Requirements — Any special circuit requirements should be discussed with VTC's product manager for the VL2000.

DIGITAL CELL DESIGN GUIDELINES

1.0 Introduction

This section of the VL2000 User's Guide explains the special considerations that a designer must understand in order to successfully define a working digital circuit using the VL2000 Digital Cell Library. This section is divided into four subsections that discuss the CML logic family, bias generators, power supply conventions, and I/O buffers. (Refer to the VTC CML Design Note-4 for further information.)

2.0 CML Logic Family, General Considerations

Current Mode Logic (CML) is the basis for all internal digital logic cells in the VL2000 Digital Cell Library. CML logic provides the highest performance level available in silicon today, and at the same time provides a speed-power product and improved packing density.

A basic CML combinational logic schematic is shown in Figure 2.1. This schematic shows all of the basic principles needed for a user to understand and begin design with CML logic. There are three levels of "series gated" logic available in the implementation of CML. They are referred to respectively as levels A, B, and C, proceeding from levels with most positive to most negative voltages. These logic levels will uniformly switch to the "1" and "0" states above and below three successive reference levels named VA, VB, and VC.

A convention established in this cell library is that all outputs of logic gates are on level "A". If it is necessary to switch from one level to another, it is performed through a level shifter cell that provides logic translation to the B and C levels while simultaneously providing a high fanout drive capability. In the example schematic (Figure 2.1), a 2-input OR/NOR gate (ON2BH) has an inverting, level A output at the collector of transistor Q13. This output feeds directly to the level A input of a level shifter cell (LVD1M), where the C-level output then feeds to a 3-input AND (A3ABCH) at transistor Q7. This allows the designer freedom to maximize performance by staying at the A level on critical paths, while going to the mutiple logic levels of series gated logic for gate utilization efficiency and fanout drive improvements where necessary. The designer need never worry about whether two incompatible logic levels are incorrectly connected, because the logic design simulation package checks before simulation run time to see that gate interconnections are logic level compatible.

It is only necessary to be concerned about logic levels when entering or leaving the chip through I/O buffers. Again, a more extensive treatment of CML design is available for interested users in the VTC CML Design Note-4.

2.1 D.C. Operating Conditions

One of the features of the VL2000 Digital Cell Library is that the designer has the freedom to trade speed for power dissipation as required in the design. Two power levels are available for all logic gates, identified as high (H) and low (L). The fastest gates are the highest power, which allows a designer to improve performance on critical paths while conserving power on non-critical paths.

From an operational standpoint, the user may change freely from one power level to the next with only one concern: ***The total equivalent D.C. fanout load for any output may not exceed the value given in the cell specifications.***

In general, D.C. fanout is defined through the unit load. One unit load in the VL2000 Cell Library is represented by the worst-case base current of a high power cell input pin. Generally, high power gate outputs may drive five unit loads, and low power gates may drive two. Also, generally, input pins on high power gates represent one unit load, and input pins on low power gates represent 0.333 unit load. Significantly higher fanout (up to 16) may be obtained through the use of the level shifters with very small performance loss. The VL2000 logic simulation package is designed to perform checks to ensure that basic D. C. fanout guidelines are not violated in the schematics. For a variety of reasons, not all cells have identical loading conditions, and the designer should be familiar with the load specifications of the cells used in a design. Information on each logic symbol is listed in the cell specifications.

Table 2.1 shows the nominal current source value along with the typical power dissipation for each of the two power levels, for a two input ORNOR gate (CELL NAME = ON2BH, ON2BL). This information is useful for comparing the tradeoffs between speed, power, and total current. The cell power is given for reference in the data sheets for every VL2000 standard cell. Since all CML gates are powered from a differential supply that is nominally either +5.0 or -5.2 volts, total current for a chip may be estimated by adding all cell power and then dividing the total by the nominal supply voltage. Table 2.2 shows the nominal design values for internal logic and logic reference voltage levels. In general the reference values represent voltages that are 1/4 diode drop below V_{CC} for the A level, 1 1/4 diode drops for the B level, and 2 1/4 diode drops for the C level. Note that the actual values depend upon the voltage selected for the V_{CC} supply.

Figure 2.1: CML Combinational Logic Schematic

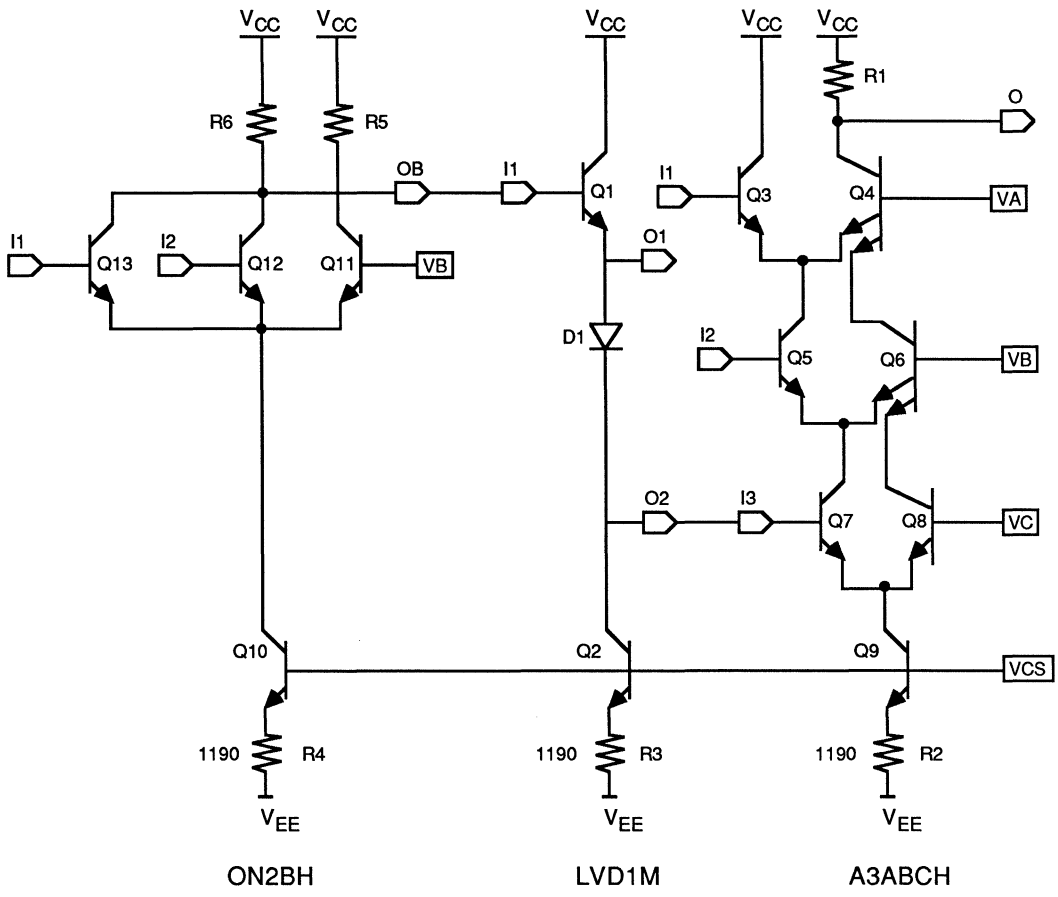


Table 2.1: DC Current and Power Dissipation for 2 Input OR/NOR CML Gate

PARAMETER	*HIGH SPEED*	*LOW POWER*
CELL CURRENT	450 µA	150 µA
POWER DISS.	2.25 mW	0.75 mW

Table 2.2: Logic and Reference Levels for Internal CML Logic

Conditions: V_{CC} = +5.0 V, V_{EE} = Gnd, Temperature = 25°C			
LOGIC LEVEL	*I/O VOLTAGE*		*REFERENCE VOLTAGE*
	HIGH(1)	*LOW(0)*	
A	4.94 V	4.49 V	4.71 V
B	4.20 V	3.75 V	3.97 V
C	3.45 V	3.00 V	3.22 V

Note: Internal logic and reference levels are referenced from V_{CC}, and will remain so under all values of V_{CC}.

2.2 A.C. Operating conditions

The VL2000 cell library data sheets included with this user's guide detail the expected performance of each of the CML gates for power, chip area, function and propagation delay. Propagation delay in CML logic is sensitive to many parameters. These include enviromental conditions, such as power supply voltage and temperature; processing variations such as transistor beta, resistor value, doping concentrations, epitaxial thickness, and oxide thickness; and design variables such as fanout and metal capacitance of the interconnect. Detailed circuit simulations of the effects of these variables, as well as actual data under controlled conditions are factored into the propagation delay information in the data sheets. It gives numbers that indicate the extremes that could result from the various combinations of the above mentioned factors.

Because it is impractical to specify a complete matrix of expected delay numbers with respect to all of these factors, and inasmuch as many of the factors do not contribute significantly to variation in delay compared to others, a summarized table is shown for each of the digital functions, for delay paths of most critical interest.

The VL2000 Cell Library logic simulator provides designers with the capability to run nominal simulations with typical delay parameters. (Typical delay occurs with nominal or average values for temperature, resistors, voltage, and beta.) The logic simulator has the ability to account for delay variation due to fanout and metal capacitance. The data sheets show typical delays which assume typical conditions of:

a. Fanout of 1 unit A.C. load
b. NO capacitive load (for metal interconnect)
c. 25° C ambient
d. Nominal supply voltage

During a logic simulation run, the actual delay is calculated by starting with the typical delay for no fanout, and adding the loaded delay due to fanout and capacitance.

The factors that affect delay are given by:

Marginal Rise Time (M_{RISE}): the additional delay per fanout unit load obseved on the rising edge (t_{PLH}) of the output pin (units of psec/pFarad).

Marginal Fall Time (M_{FALL}): the additional delay per fanout unit load observed on the falling edge (t_{PHL}) of the output pin (units of psec/pFarad).

A 0.15 pFarad capacitance is placed on each input pin to account for delay increase due to fanout. Metal capacitance due to physical layout may be fed in after routing for analysis of critical paths. Information to allow the designer to calculate worst case slow delays for critical paths over temperature and process variations is provided in the form of derating factors as follows:

Maximum delay occurs at high temperature, with high resistors, low voltage, and low beta. Once the typical loaded delay is obtained from the simulator, the designer may apply a multiplicative derating factor (K_p) due to process variations. K_p = 1.4 for worst case slow delays. To calculate the delay over temperature, the following derating factors must be used: K_t is the parameter, and its values for each temperature condition are: 0.72 at -55 ° C; 1.0 at 25 ° C; 1.25 at 125 ° C.

The equations, then, for calculating actual delays are:

$$t_{PLH} = ((\text{typical delay}) + (M_{RISE} \cdot 0.15) \cdot (\#\text{ of unit loads} - 1)) \cdot K_p \cdot K_t$$

$$t_{PHL} = ((\text{typical delay}) + (M_{FALL} \cdot 0.15) \cdot (\#\text{ of unit loads} - 1)) \cdot K_p \cdot K_t$$

Note that typical delay assumes a fanout of one and the above equation accounts for this by subtracting one unit load in the calculation. Also, since M_{RISE} and M_{FALL} are specified in units of psec/pF, the factor 0.15 accounts for the fact that one unit load is given as 0.15 pF.

As an example calculation, refer to Figure (2.2). This simple logic schematic shows a critical path through

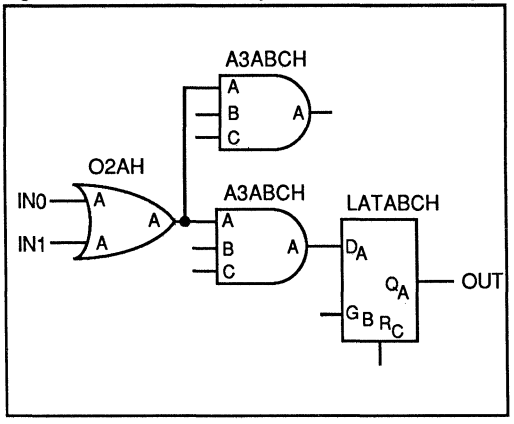
that the OR gate (O2AH) drives 2 unit loads, the AND gate (A3ABCH) drives one unit load, and the LATCH cell (LATABCH) drives one unit load. Using the typical delays from the cell specifications, along with the M_{RISE} and M_{FALL} information, the calculations for actual worst case delay for worst case processing at -55 ° C and 125°C are presented below. The method used is to first add all delays for typical conditions, then apply the proper derating factors for process and temperature:

$$t_{PHL}\,(typ) = 420 + (780 \cdot 0.15 \cdot (2\text{-}1)) + 830 + 675 = 2042\ psec$$

$$t_{PHL}\,(WC, -55\ ^\circ C) = 2042 \cdot (1.4) \cdot (0.72) = 2058\ psec$$

$$t_{PHL}\,(WC, 125\ ^\circ C) = 2042 \cdot (1.4) \cdot (1.25) = 3778\ psec$$

Figure 2.2: Critical Delay Path Circuit Example



3.0 Bias Generators

Required elements in CML logic design include the bias generator circuits that set the reference levels for the logic comparison, and control the current in the logic cells. There are three bias generators used in the VL2000 Cell Library. The main bias generator (VCS) provides the V_{CS} reference that controls all cell currents on the chip. It also provides the ECL10KH compatible reference voltage (VBB) for all ECL input buffers. The internal bias generator (IBIAS) provides three logic comparison reference levels for internal logic at the A, B, and C levels (referred to as VA, VB, and VC respectively). The third bias generator (TBIAS) is reserved exclusively for translating TTL logic levels to CML at the TTL input buffer. A completed chip will have at least one VCS and one or more IBIAS and TBIAS cells. The number of cells required is a function of the number of logic cells used. The correct number of bias generator cells must be placed in the schematic and connected to the power supplies. This is necessary for correct completion of layout. Refer to appropriate workstation instructions for implementation. For very large chips, it is possible that more than one VCS cell would be required. The unit load fanout capabilities for each of these cells is given in the cell specifications. The fanout capability refers to the number of cells that may be driven from that bias generator. Refer to these requirements in determining the number of bias generator cells that a particular design will require.

The unit load fanin for the voltage references on each cell determines the total loading for each bias generator. Reference fanin for the majority of cells is 1.0 for high speed cells and 0.333 for low power cells. Refer to Table 3.1 for cells that are exceptions.

Table 3.1: Reference Voltage Fanin Loading

Note: All high speed cells have reference fanin loading = 1.0 and all low power cells have reference fanin loading = 0.333 except as listed below.

CELL NAME	*REFERENCE FANIN LOADING**
MXFFABCL	0.66
MXFFABCH	2.0
DFFABCL	0.66
DFFABCH	2.0
TFFBCL	1.67 VCS; 1.0 VB, VC
TFFBCH	5.0 VCS; 3.0 VB, VC
JKFFBCL	1.67 VCS; 1.0 VB, VC
JKFFBCH	5.0 VCS; 3.0 VB, VC
DIFFIN	1.67
OUT10KH	9
OUT10KHN	9
DIFFOUT	8.22
FABCL	1.0 VCS; 0.66 VB, VC
FABCH	3.0 VCS; 2.0 VB, VC
LVDIH	3.5
LVDIM	1.0
LVDIL	0.33
CLKAB	17.11 VCS; 4.0 VB; 3.0 VC

**Applies to all references unless otherwise noted (VA, VB, VC, VCS, VBB, VTTL)*

4.0 Power Supply Convention

There are three power supply names available in the VL2000 Cell Library: VDD, VCC, and VEE. The conventions established for allowable values for these power supplies is discussed in the section titled Workstation Instructions, Power Supply Conventions.

There are some special considerations in using the I/O buffers and gates, with regard to the power supplies. These considerations are demonstrated in Table 4.1.

The critical task is to properly identify the conditions that determine whether the internal CML logic operates above or below ground. Coupled with this is

the fact that the I/O buffers must operate between power supplies that allow them to be compatiable with the internal logic. The important point is that the CML gates always operate between the two most negative power supplies. Note that the ECL I/O buffers will operate either above or below ground. The TTL I/O buffers will only operate above ground.

Note that proper interfacing from above-ground TTL logic to below-ground CML logic requires the POSNEGSHFT cell as a translator interface between the TTL input buffers and the internal logic cells. However, if the CML logic is used above ground (only when there is no below ground power supply), it connects directly to the TTL input and output buffers.

Table 4.1: Power Supply Selection and Logic-I/O Buffer Interfacing

POWER SUPPLIES USED (V)			*LOGIC LEVEL INTERFACING*		
V_{DD}	V_{CC}	V_{EE}	TTL I/O	CML*	ECL I/O*
+5.0	0.0	-5.2	+5.0; 0.0	0.0; -5.2	0.0; -5.2**
N/A	0.0	-5.2	N/A	0.0; -5.2	0.0; -5.2
N/A	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	+5.0; 0.0
N/A	+5.0	0.0	+5.0; 0.0	+5.0; 0.0	N/A

**Note: This includes the associate d bias generators.*
***Note: In this case a POSNEGSHFT cell is used as a level shift between CML logic gates and the TTL input buffer (INTTL), and a NEGPOSSHFT cell is used between the CML logic gates and the TTL output buffers (OUTTTL, OUTNTTL, etc.)*

5.0 I/O Buffers

Interfacing the digital logic internal CML gates to the outside may be accomplished in several ways. Input and output buffers are available that are compatible with the ECL 10KH specifications, and a separate set of buffers are compatible with the AS (Advanced Schottky) logic family. The selection of the buffer type is a customer option.

There are certain special conditions that must be met in order to guarantee proper operation of these buffers. Some of these have already been mentioned in the immediately preceeding section. Other conditions include:

When using the high impedance state TTL output buffer (such as OUTNTRI), a special connection must be made to the high impedance control pin, labeled OE. A special output enable gate (OEN3SI) is used to drive that pin from CML logic gates. The user must connect a CML logic level control signal to the C input of the OEN3SI cell, in order to complete that functional control. The OEN3SI cell can drive up to 8 output buffer enable pins in parallel.

Tables 5.1 and 5.2 include the DC electrical characteristics for both the TTL and ECL compatible input and output buffers. Refer to these tables for details related to any of the respective cells shown in the data sheets.

Table 5.1: ECL10KH Compatible DC Electrical Characteristics

INPUT FORCING VOLTAGES	*PARA-METER*	*ECL 10KH COMPATIBLE SPEC LIMITS* AMBIENT TEMP.*			*UNITS*
		0°C	*25°C*	*75°C*	
V_{IH} max. V_{IL} min.	V_{OH} max.[1]	-0.840	-0.810	-0.735	Vdc
	V_{OH} min.[1]	-1.020	-0.980	-0.920	Vdc
	V_{OL} max.[1]	-1.630	-1.630	-1.060	Vdc
	V_{OL} min.[1]	-1.950	-1.950	-1.950	Vdc
V_{IH} max.	I_{INH}max.	25	25	25	µA
V_{EE}	I_{CBO}max	1.5	1.5	1.5	µA
Input Voltage Values	V_{IH} max.	-0.840	-0.810	-0.735	Vdc
	V_{IH} min.	-1.170	-1.130	-1.070	Vdc
	V_{IL} max.	-1.480	-1.480	-1.450	Vdc
	V_{IL} min.	-1.950	-1.950	-1.950	Vdc
		MILITARY RATED SPEC LIMITS			
		-55°C	*25°C*	*125°C*	
V_{IH} max. V_{IL} min.	V_{OH} max.[2]	-0.880	-0.780	-0.630	Vdc
	V_{OH} min.[2]	-1.080	-0.930	-0.825	Vdc
	V_{OL} max.[2]	-1.655	-1.620	-1.545	Vdc
	V_{OL} min.[2]	-1.920	-1.850	-1.820	Vdc

**Note: DC test limits are specified after thermal equilibrium has been established with the device having a controlled transverse air flow of 75 lfpm. V_{EE} = -5.2 ± 10%. All ECL outputs are loaded with 50Ω to -2.0V.*

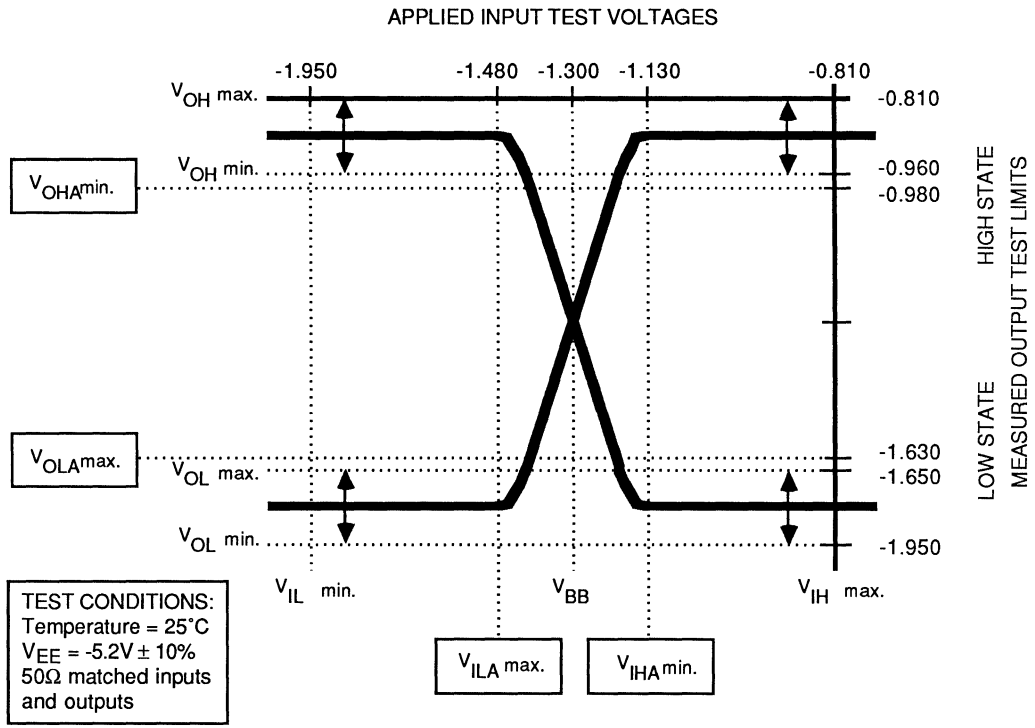
1 Output loading is 50 ohms to -2.0 volts.
2 Output loading is 100 ohms to -2.0 volts.

Table 5.2: AS (Advanced Schottky) Compatible DC Electrical Characteristics

PARAMETER	*SYM*	*TEST CONDITIONS* (1,2)	*MIN.*	*TYP.*	*MAX.*	*UNITS*
Input HIGH Voltage	V_{IH}	Guaranteed Input HIGH Voltage	2.0			Volts
Input LOW Voltage	V_{IL}	Guaranteed Input LOW Voltage			0.8	Volts
Input Clamp Voltage	V_{CD}	V_{CC}=4.50 V; I_{IN} = - 18.0mA			- 1.2	Volts
Output HIGH Voltage	V_{OH}	V_{CC}=4.50 V; I_{OH} = - 3.0mA	2.5			Volts
Output LOW Voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 4.0mA			0.4	Volts
		V_{CC} = 4.5 V; I_{OL} = 8.0mA			0.5	
Input HIGH Current	I_{IH}	V_{CC} = 5.5 V; V_{IN} =2.7 V			20	µA
		V_{CC} = 5.5 V; V_{IN} =7.0 V			0.1	mA
Input LOW Current	I_{IL}	V_{CC} = 5.5 V; V_{IN} =0.5V			- 0.6	mA
Output Short Circuit Current	I_{OS}	V_{CC}= 5.5 V; V_{IN} =0V (3)	- 20		- 130	mA
Output Off-Z Current HIGH	I_{OZH}	V_{CC}= 5.5 V ; V_{OUT} =2.7V			50	µA
Output Off-Z Current LOW	I_{OZL}	V_{CC}= 5.5 V; V_{OUT} =0.5V			- 50	µA
Input HIGH Current Bidirectional Tri-State Output	I_{IHT}	V_{CC}= 5.5V; V_{IN} =2.7V			50	µA
Input HIGH Current Bidirectional Open Collector Output	I_{IHC}	V_{CC}= 5.5V; V_{IN} =5.5V			180	µA
Input LOW Current Bidirectional Tri-State	I_{ILT}	V_{CC}= 5.5V; V_{IN} =0.5V			- 650	µA
Input LOW Current Bidirectional Open Collector Output	I_{ILC}	V_{CC}=5.5V; V_{IN} =0.5V			- 650	µA
Output HIGH Current Open Collector Output	I_{OHC}	V_{CC}= 5.5V; V_{OUT} =5.5V			100	µA

NOTES: 1. V_{CC} = 4.50 to 5.50 V; T_A = -55 to 125 °C unless otherwise noted.
2. Typical limits are at V_{CC}= 5.0 V, T_A = 25 °C.
3. Not more than one output shorted at one time duration of test not to exceed one second.

TRANSFER CURVES (ECL 10KH) AND SPECIFICATION TEST POINTS



CELL SPECIFICATIONS

SIMPLE GATES

O2AH/O2AL

DESCRIPTION:
2 input OR gate

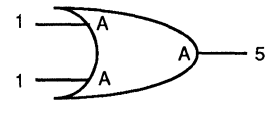
CELL AREA:
High Speed:
10,619 sq. microns
16.46 sq. mils
Low Power:
15,211 sq. microns
23.58 sq. mils

TRUTH TABLE:

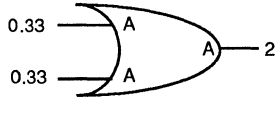
I1	*I2*	*O*
1	0	1
1	1	1
0	1	1
0	0	0

SYMBOLS:

O2AH (HIGH SPEED)



O2AL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	420	680	ps
t_{PLH}	ANY I	O	420	900	ps
M_{rise}		O	750	2600	ps/pF
M_{fall}		O	780	2350	ps/pF

O3AH/O3AL

DESCRIPTION:

3 input OR gate

CELL AREA:

High Speed:
15,354 sq. microns
23.80 sq. mils
Low Power
17,651 sq. microns
27.36 sq. mils

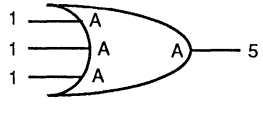
TRUTH TABLE:

I0	I1	I2	O
1	X	X	1
X	1	X	1
X	X	1	1
0	0	0	0

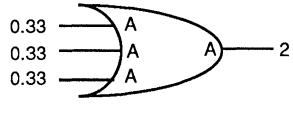
X = Don't care

SYMBOLS:

O3AH (HIGH SPEED)



O3AL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	INPUT	OUTPUT	HIGH SPEED	LOW POWER	UNITS
t_{PHL}	ANY I	O	420	720	ps
t_{PLH}	ANY I	O	420	900	ps
M_{rise}		O	750	2600	ps/pF
M_{fall}		O	780	2350	ps/pF

O4AH/O4AL

DESCRIPTION:

4 input OR gate

CELL AREA:

High Speed:
15,211 sq. microns
23.58 sq. mils

Low Power:
17,651 sq. microns
27.36 sq. mils

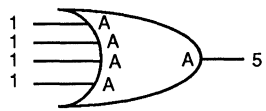
TRUTH TABLE:

I1	I2	I3	I4	O
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1
0	0	0	0	0

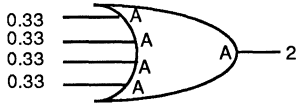
X = Don't care

SYMBOLS:

O4AH (HIGH SPEED)



O4AL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	440	800	ps
t_{PLH}	ANY I	O	440	920	ps
M_{rise}		O	750	2600	ps/pF
M_{fall}		O	780	2350	ps/pF

ON2BH/ON2BL

DESCRIPTION:
2 input OR-NOR gate

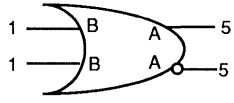
CELL AREA:
High Speed:
10,619 sq. microns
16.46 sq. mils
Low Power:
11,624 sq. microns
18.02 sq. mils

TRUTH TABLE:

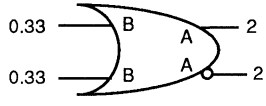
I1	*I2*	*O*	*OB*
1	0	1	0
1	1	1	0
0	1	1	0
0	0	0	1

SYMBOLS:

ON2BH (HIGH SPEED)



ON2BL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
^tPHL	ANY I	O	400	620	ps
^tPLH	ANY I	O	380	820	ps
^tPHL	ANY I	OB	440	620	ps
^tPLH	ANY I	OB	400	1020	ps
M_{rise}		O or OB	730	2600	ps/pF
M_{fall}		O or OB	760	2450	ps/pF

ON3BH/ON3BL

DESCRIPTION:

3 input OR-NOR gate

CELL AREA:

High Speed:
15,355 sq. microns
23.80 sq. mils
Low Power
15,211 sq. microns
23.58 sq. mils

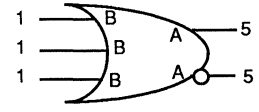
TRUTH TABLE:

I0	I1	I2	O	OB
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
0	0	0	0	1

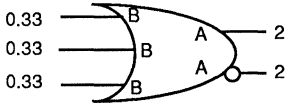
X = Don't care

SYMBOLS:

ON3BH (HIGH SPEED)



ON3BL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	INPUT	OUTPUT	HIGH SPEED	LOW POWER	UNITS
t_{PHL}	ANY I	O	420	700	ps
t_{PLH}	ANY I	O	380	840	ps
t_{PHL}	ANY I	OB	480	650	ps
t_{PLH}	ANY I	OB	450	1200	ps
M_{rise}		O or OB	730	2600	ps/pF
M_{fall}		O or OB	760	2450	ps/pF

ON4BH/ON4BL

DESCRIPTION:
4 input OR-NOR gate

CELL AREA:
High Speed:
15,211 sq. microns
23.58 sq. mils
Low Power:
17,651 sq. microns
27.36 sq. mil

TRUTH TABLE:

I1	I2	I3	I4	O	OB
1	X	X	X	1	0
X	1	X	X	1	0
X	X	1	X	1	0
X	X	X	1	1	0
0	0	0	0	0	1

X = Don't care

PERFORMANCE:

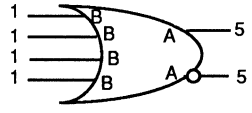
Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

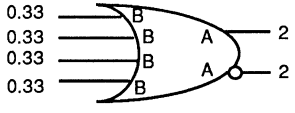
TEST	INPUT	OUTPUT	HIGH SPEED	LOW POWER	UNITS
^tPHL	ANY I	O	440	780	ps
^tPLH	ANY I	O	420	840	ps
^tPHL	ANY I	OB	520	680	ps
^tPLH	ANY I	OB	480	1380	ps
M_{rise}		O or OB	730	2600	ps/pF
M_{fall}		O or OB	760	2450	ps/pF

SYMBOLS:

ON4BH (HIGH SPEED)



ON4BL (LOW POWER)



A3ABCH/A3ABCL

DESCRIPTION:
3 input AND gate

CELL AREA:
High Speed/Low Power
16,072 sq. microns
24.91 sq. mils

TRUTH TABLE:

I1	*I2*	*I3*	*O*
1	1	1	1
X	X	0	0
X	0	X	0
0	X	X	0

X = Don't care

PERFORMANCE:

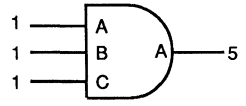
Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

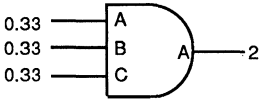
TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	830	1550	ps
t_{PLH}	ANY I	O	780	1600	ps
M_{rise}		O	830	2760	ps/pF
M_{fall}		O	800	2710	ps/pF

SYMBOLS:

A3ABCH (HIGH SPEED)



A3ABCL (LOW POWER)



BIPOLAR SEMICUSTOM

AN2BCH/AN2BCL

DESCRIPTION:
2 input AND-NAND gate

CELL AREA:
High Speed/Low Power
15,498 sq. microns
24.02 sq. mils

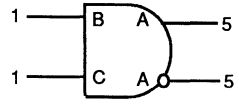
TRUTH TABLE:

I1	*I2*	*O*	*OB*
1	1	1	0
0	X	0	1
X	0	0	1

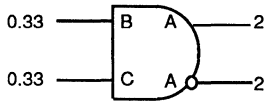
X = Don't care

SYMBOLS:

AN2BCH (HIGH SPEED)



AN2BCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	620	1000	ps
t_{PLH}	ANY I	O	600	1260	ps
t_{PHL}	ANY I	OB	620	900	ps
t_{PLH}	ANY I	OB	560	1220	ps
M_{rise}		O or OB	840	2840	ps/pF
M_{fall}		O or OB	740	2780	ps/pF

OAI2BCH/OAI2BCL

DESCRIPTION:
2-2 OR-AND-INVERT gate

CELL AREA:
High Speed/Low Power
18,081 sq. microns
28.03 sq. mils

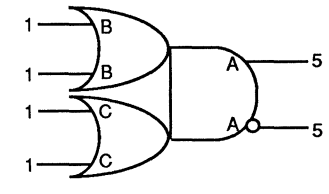
TRUTH TABLE:

I1	*I2*	*I3*	*I4*	*O*	*OB*
1	X	1	X	1	0
1	X	X	1	1	0
X	1	1	X	1	0
X	1	X	1	1	0
0	0	0	0	0	1

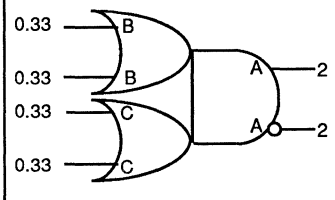
X = Don't care

SYMBOLS:

OAI2BCH (HIGH SPEED)



OAI2BCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	620	1020	ps
t_{PLH}	ANY I	O	620	1280	ps
t_{PHL}	ANY I	OB	740	1140	ps
t_{PLH}	ANY I	OB	650	1540	ps
M_{rise}		O or OB	860	2900	ps/pF
M_{fall}		O or OB	740	2800	ps/pF

OAI3BCH/OAI3BCL

DESCRIPTION:
3-3 OR-AND-INVERT gate

CELL AREA:
High Speed/Low Power
20,664 sq. microns
32.03 sq. mils

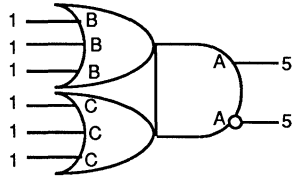
TRUTH TABLE:

I0+I1+I2	*I3+I4+I5*	*O*	*OB*
1	1	1	0
0	X	0	1
X	0	0	1

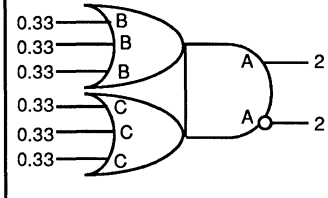
X = Don't care

SYMBOLS:

OAI3BCH (HIGH SPEED)



OAI3BCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY I	O	630	1050	ps
t_{PLH}	ANY I	O	610	1280	ps
t_{PHL}	ANY I	OB	820	1410	ps
t_{PLH}	ANY I	OB	750	1860	ps
M_{rise}		O or OB	860	2900	ps/pF
M_{fall}		O or OB	740	2800	ps/pF

XONBCH/XONBCL

DESCRIPTION:
Two input exclusive ORNOR gate

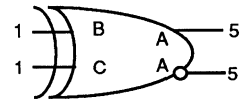
CELL AREA:
High Speed/Low Power
20,090 sq. microns
31.14 sq. mils

TRUTH TABLE:

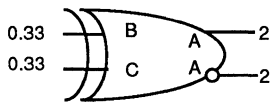
I0	I1	O	OB
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	1

SYMBOLS:

XONBCH (HIGH SPEED)



XONBCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	INPUT	OUTPUT	PHASE	HIGH SPEED	LOW POWER	UNITS
t_{PHL}	IO	ANY	IN	420	620	ps
t_{PLH}	IO	ANY	IN	430	1040	ps
t_{PHL}	IO	ANY	OUT	420	620	ps
t_{PLH}	IO	ANY	OUT	430	1040	ps
t_{PHL}	I1	ANY	IN	640	1170	ps
t_{PLH}	I1	ANY	IN	610	1380	ps
t_{PHL}	I1	ANY	OUT	710	1260	ps
t_{PLH}	I1	ANY	OUT	600	1450	ps
M_{rise}		O		830	2870	ps/pF
M_{fall}		O		730	2680	ps/pF
M_{rise}		OB		830	2870	ps/pF
M_{fall}		OB		730	2680	ps/pF

FLIP-FLOPS

LATABCH/LATABCL

DESCRIPTION:
Data latch with reset

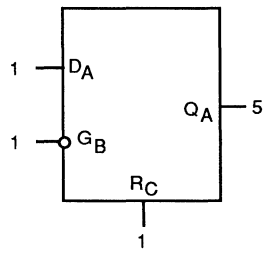
CELL AREA:
High Speed/Low Power
18,081 sq. microns
28.03 sq. mils

TRUTH TABLE:

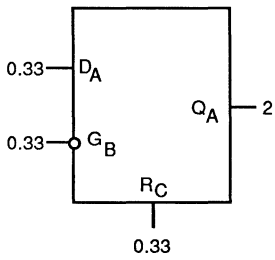
R	*G*	*D*	*Q*
1	X	X	0
0	0	1	1
0	0	0	0
0	1	X	Q_N

SYMBOLS:

LATABCH (HIGH SPEED)



LATABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
^tPHL	D	Q	675	1250	ps
^tPLH	D	Q	670	1650	ps
^tPHL	G	Q	860	2000	ps
^tPLH	G	Q	680	1800	ps
^tPHL	R	Q	580	1150	ps
^tSET			700	1700	ps
^tHOLD			0	0	ps
PULSE WIDTH					
R HIGH			600	1200	ps
G LOW			900	2000	ps

SRLABH/SRLABL

DESCRIPTION:

Set-reset latch with reset overriding set

CELL AREA:

High Speed/Low Power
16,503 sq. microns
25.58 sq. mils

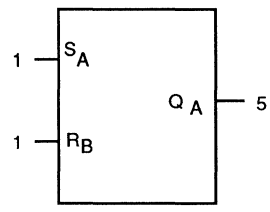
TRUTH TABLE:

R	*S*	*Q*
1	X	0
0	1	1
0	0	Q_N

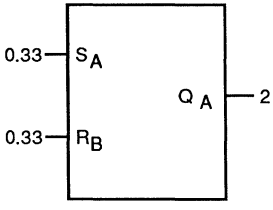
X = Don't care

SYMBOLS:

SRLABH (HIGH SPEED)



SRLABL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
^tPLH	S	Q	550	1300	ps
^tPHL	R	Q	750	1500	ps
M_{rise}		Q	790	2900	ps/pF
M_{fall}		Q	900	2380	ps/pF

MX2LABCH/MX2LABCL

DESCRIPTION:

Data latch with multiplexed data inputs

CELL AREA:

High Speed/Low Power
23,821 sq. microns
36.92 sq. mils

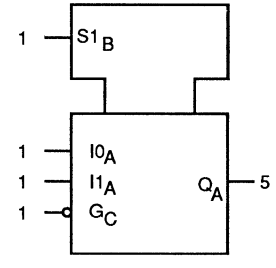
TRUTH TABLE:

S1	*I0*	*I1*	*G*	*Q*
1	X	1	0	1
1	X	0	0	0
0	1	X	0	1
0	0	X	0	0
X	X	X	1	Q_N

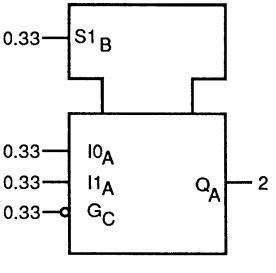
X = Don't care

SYMBOLS:

MX2LABCH (HIGH SPEED)



MX2LABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*PHASE*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY 1	Q		600	1240	ps
t_{PLH}	ANY 1	Q		630	1640	ps
t_{PHL}	S1	Q	IN	760	1740	ps
t_{PLH}	S1	Q	IN	760	1920	ps
t_{PHL}	S1	Q	OUT	800	1750	ps
t_{PLH}	S1	Q	OUT	750	1960	ps
t_{PHL}	G	Q		990	2230	ps
t_{PLH}	G	Q		720	1850	ps
t_{SET}	ANY I	G		750	1750	ps
t_{SET}	S1	G		900	2050	ps
t_{HOLD}	ANY 1	G		0	0	ps
t_{HOLD}	S1	G		0	0	ps
M_{rise}		Q		830	2820	ps/pF
M_{fall}		Q		960	2390	ps/pF
PULSE WIDTHS						
G LOW				1100	2300	ps

MXFFABCH/MXFFABCL

DESCRIPTION:

Data flip-flop with multiplexed inputs

CELL AREA:

High Speed/Low Power
35,875 sq. microns
55.60 sq. mils

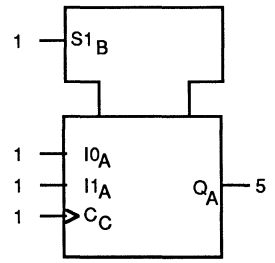
TRUTH TABLE:

S1	*I0*	*I1*	*C*	*Q*
1	X	1	U	1
1	X	0	U	0
0	1	X	U	1
0	0	X	U	0

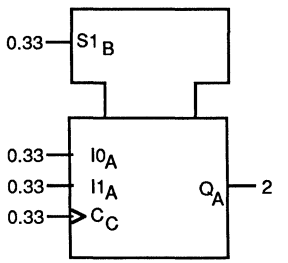
U = Low to High Transition
X = Don't care

SYMBOLS:

MXFFABCH (HIGH SPEED)



MXFFABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 4.50mW Typ.
(Low Power): 1.50mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
^tPHL	C	Q	750	1550	ps
^tPLH	C	Q	660	1520	ps
^tSET	ANY I	C	610	1600	ps
^tSET	S1	C	800	1950	ps
^tHOLD	ANY I	G	0	0	ps
^tHOLD	S1	G	0	0	ps
M_{rise}		Q	880	2850	ps/pF
M_{fall}		Q	770	2260	ps/pF
PULSE WIDTHS					
C HIGH			850	1650	ps
C LOW			1200	2600	ps

DFFABCH/DFFABCL

DESCRIPTION:
Data flip-flop with reset

CELL AREA:
High Speed/Low Power
32,431 sq. microns
50.26 sq. mils

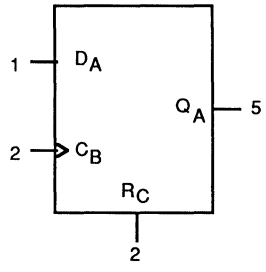
TRUTH TABLE:

R	*D*	*C*	*Q*
1	X	X	0
0	1	U	1
0	0	U	0
0	X	N	Q_N

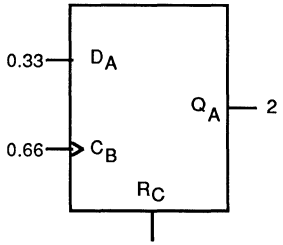
U = Low to High Transition
N = Not a Low to High Transition
X = Don't care

SYMBOLS:

DFFABCH (HIGH SPEED)



DFFABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 4.50mW Typ.
(Low Power): 1.50mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	R	Q	580	1100	ps
t_{PHL}	C	Q	900	2000	ps
t_{PLH}	C	Q	750	1800	ps
t_{SET} - minimum			1000	2500	ps
t_{HOLD}			0	0	ps
F_{max}			500	200	MHz
PULSE WIDTHS					
R HIGH			600	1200	ps
C LOW			1000	2000	ps

TFFBCH/TFFBCL

DESCRIPTION:

Toggle flip-flop with asynchronous reset

CELL AREA:

High Speed/Low Power
60,270 sq. microns
93.42 sq. mils

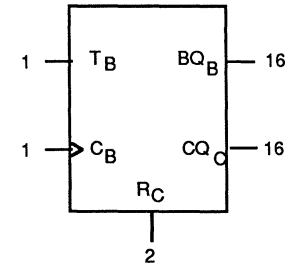
TRUTH TABLE:

R	*T*	*C*	*BQ*	*CQ*
1	X	X	0	0
0	1	U	Q_N	Q_N
0	0	U	Q	Q

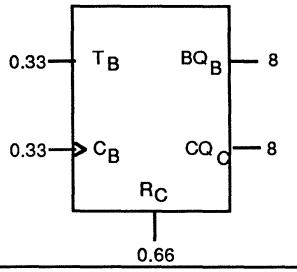
U = Low to High Transition
X = Don't care

SYMBOLS:

TFFBCH (HIGH SPEED)



TFFBCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 3.75mW Typ.
(Low Power): 11.25mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	R	ANY	660	1480	ps
t_{PHL}	C	ANY	910	2120	ps
t_{PLH}	C	ANY	860	1640	ps
t_{SET}	T	C	1100	2600	ps
t_{HOLD}	T	C	0	0	ps
M_{rise}		ANY	160	230	ps/pF
M_{fall}		ANY	400	1050	ps/pF
Reset recovery time			550	1400	ps
Reset recovery time - worst case			1000	2500	ps
F_{tog}			250	125	MHz
F_{tog} - worst case			150	85	MHz
PULSE WIDTHS					
R HIGH			750	1200	ps
C HIGH			1100	2000	ps
C LOW			1100	2000	ps

JKFFBCH/JKFFBCL

DESCRIPTION:
J-K flip-flop with asynchronous reset

CELL AREA:
High Speed/Low Power
60,270 sq. microns
93.42 sq. mils

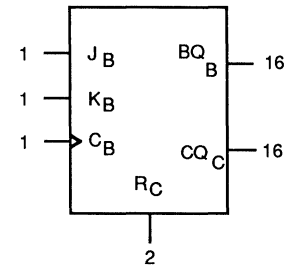
TRUTH TABLE:

R	*J*	*K*	*C*	*BQ*	*CQ*
1	X	X	X	0	0
0	1	1	U	Q_N	Q_N
0	1	0	U	1	1
0	0	1	U	0	0
0	0	0	U	Q	Q

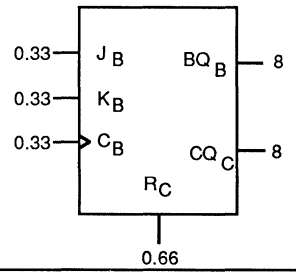
U = Low to High Transition
X = Don't care

SYMBOLS:

JKFFBCH (HIGH SPEED)



JKFFBCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 11.25mW Typ.
(Low Power): 3.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	R	Any	660	1480	ps
t_{PHL}	C	Any	910	2120	ps
t_{PLH}	C	Any	860	1640	ps
t_{SET}	T	C	1100	2600	ps
t_{HOLD}	T	C	0	0	ps
M_{rise}		Any	160	230	ps/pF
M_{fall}		Any	400	1050	ps/pF
Reset recovery time			550	1400	ps
Reset recovery time - worst case			1000	2500	ps
F_{tog}			250	125	MHz
F_{tog} - worst case			150	85	MHz
PULSE WIDTHS					
R HIGH			750	1200	ps
C HIGH			1100	2000	ps
C LOW			1100	2000	ps

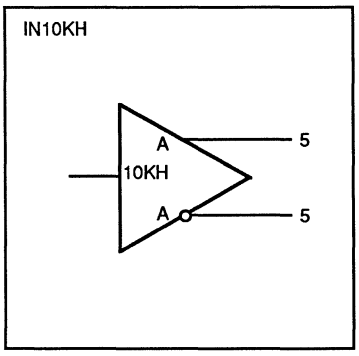
INPUT/OUTPUT BUFFERS

IN10KH

DESCRIPTION:
10 KH ECL input buffer

CELL AREA:
14,627 sq. microns
22.67 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 2.34 mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*TYPICAL*	*UNITS*
t_{PHL}	I_1	O	460	ps
t_{PLH}	I_1	O	450	ps
t_{PHL}	I_1	OB	430	ps
t_{PLH}	I_1	OB	470	ps
M_{rise}		O or OB	730	ps/pF
M_{fall}		O or OB	760	ps/pF

DIFFIN

DESCRIPTION:

Differential input receiver
(Compatible with ECL 10KH and
DIFFOUT output levels)

CELL AREA:

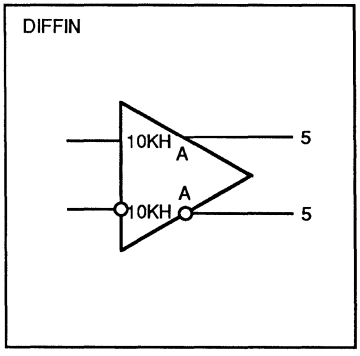
23,283 sq. microns
36.1 sq. mils

TRUTH TABLE:

I	*IN*	*O*	*OB*
1	0	1	0
0	1	0	1
1	1	X	X
0	0	X	X

X = Don't care

SYMBOL:



PERFORMANCE:

Power Dissipation: 3.9mW Typ.

DC Characteristics: V_{EE} = -5.2 ±10%, T_A = 55° C to 125° C

COMMON MODE INPUT VOLTAGE (V)	Max. - 0.3, Min. - 2.3
DIFFERENTIAL INPUT VOLTAGE (mV)	Min. 200

AC Characteristics:
V_{EE} = - 5.2 V ±10 %, C_L = 0, FO = 1

TEST	*INPUT*	*OUTPUT*	*TYPICAL*	*UNITS*
t_{PHL}	DIFF	O	530	ps
t_{PLH}	DIFF	O	500	ps
t_{PHL}	DIFF	OB	450	ps
t_{PLH}	DIFF	OB	420	ps
M_{rise}		O	730	ps/pF
M_{fall}		O	680	ps/pF
M_{rise}		OB	730	ps/pF
M_{fall}		OB	660	ps/pF

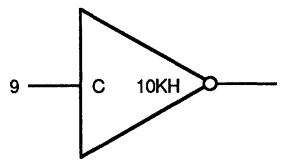
OUT10KHN

DESCRIPTION:
Inverting ECL10KH compatible output buffer

CELL AREA:
24,179 sq. microns
37.48 sq. mils

SYMBOL:

OUT10KHN



PERFORMANCE:

Power Dissipation: 19.24mW Typ.

DC Characteristics: V_{EE} = - 5.2V ±10%

TEST	-55°C		0°C		25°C		75°C		125°C		UNITS
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} 1	-1.08	-0.88			-0.93	-0.78			-0.83	-0.63	V
V_{OH} 2			-1.02	-0.84	-0.98	-0.81	-0.92	-0.74			V
V_{OL} 1	-1.92	-1.65			-1.85	-1.62			-1.82	-1.54	V
V_{OL} 2			-1.95	-1.63	-1.95	-1.63	-1.95	-1.60			V

NOTES: 1. Output loading is 100 Ohms to - 2V
2. Output loading is 50 Ohms to - 2V

AC Characterics:[1]
V_{EE} = - 5.2 V ±10 %,

TEST	-55°C		25°C			125°C		UNITS
	Min	Max	Min	Typ	Max	Min	Max	
t_{PHL}	0.7			1.5				ns
t_{PLH}	0.7			1.5				ns
t_r	0.7	2.2	0.7		2.2	0.7	2.2	ns
t_f	0.7	2.2	0.7		2.2	0.7	2.2	ns

NOTES: 1. Output loading is 50 Ohms to -2V; C_L <5pF

OUT10KH

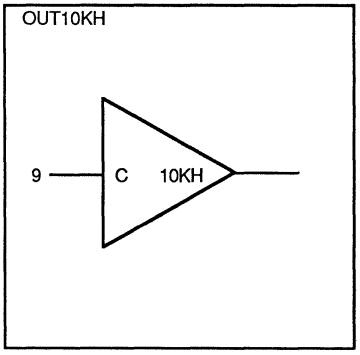
DESCRIPTION:

Non-inverting ECL10KH compatible output buffer

CELL AREA:

24,179 sq. microns
37.48 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 19.24mW Typ.

DC Characteristics: V_{EE}= - 5.2 V ±10%

TEST	-55°C		0°C		25°C		75°C		125°C		UNITS
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} 1	-1.08	-0.88			-0.93	-0.78			-0.83	-0.63	V
V_{OH} 2			-1.02	-0.84	-0.98	-0.81	-0.92	-0.74			V
V_{OL} 1	-1.92	-1.65			-1.85	-1.62			-1.82	-1.54	V
V_{OL} 2			-1.95	-1.63	-1.95	-1.63	-1.95	-1.60			V

NOTES: 1. Output loading is 100 Ohms to - 2v
2. Output loading is 50 Ohms to - 2v

AC Characterics:[1]
V_{EE} = - 5.2V ±10 %,

TEST	-55°C		25°C			125°C		UNITS
	Min	Max	Min	Typ	Max	Min	Max	
t_{PHL}	0.7			1.5				ns
t_{PLH}	0.7			1.5				ns
t_r	0.7	2.2	0.7		2.2	0.7	2.2	ns
t_f	0.7	2.2	0.7		2.2	0.7	2.2	ns

NOTES: 1. Output loading is 50 Ohms to -2V; C_L <5pF

DIFFOUT

DESCRIPTION:
Differential Output Driver
Note: Output Levels are not ECL10KH compatible

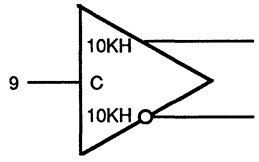
CELL AREA:
21,791 sq. microns
33.78 sq. mils

TRUTH TABLE:

IN	OUT	OUTN
1	1	0
0	0	1

SYMBOL:

DIFFOUT



PERFORMANCE:

Power Dissipation: 19.24mW Typ.

DC Characteristics: V_{EE} = - 5.2V ±10%

TEST	-55°C		0°C		25°C		75°C		125°C		UNITS
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} [1]	-1.08	-0.83			-0.93	-0.73			-0.83	-0.6	V
V_{OH} [2]			-1.02	-0.78	-0.98	-0.75	-0.92	-0.66			V
V_{OL} [1]	-1.92	-1.65			-1.85	-1.62			-1.82	-1.54	V
V_{OL} [2]			-1.95	-1.63	-1.95	-1.63	-1.95	-1.60			V
V_{DIF}	0.5								0.5		V

NOTES: 1. Output loading is 100 Ohms to - 2V
2. Output loading is 50 Ohms to - 2V

AC Characterics: [1]
V_{EE} = - 5.2 V ±10 %,

TEST	-55° C		25° C			125° C		UNITS
	Min	Max	Min	Typ	Max	Min	Max	
t_{PHL}	0.7			1.1			1.9	ns
t_{PLH}	0.7			1.1			1.9	ns
M rise	0.7	2.2	0.7		2.2	0.7	2.2	ns
M fall	0.7	2.2	0.7		2.2	0.7	2.2	ns

NOTES: 1. Output loading is 50 Ohms to - 2v; C_L < 5 pF.
Progagation delay is measured from input switching thresold to output voltage level where OUT equals OUTN.

INTTL

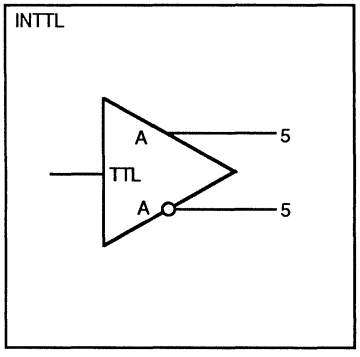
DESCRIPTION:

Inverting and non-inverting
TTL input buffer

CELL AREA:

16,119 sq. microns
24.98 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 4.5mW Typ.

DC Characteristics: V_{CC}= 5.0 ±10%

TEST	*MIN*	*MAX*	*CONDITIONS*	*UNITS*
V_{IH}	2.0			V
V_{IL}		0.8		V
V_{FCD}		-1.2	I_{IN} = - 18 mA *	V
I_{IH}		20	V_{IN} = 2.7 V **	µA
I_{BVI}		100	V_{IN} = 7.0 V **	µA
I_{IL}		- 0.6	V_{IN} =0.5 V **	mA

**V_{CC}= Max
*V_{CC}= Min

AC Characteristics: V_{CC} = 5.0 V±10%, C_L = 0, FO = 1, V_A = 25° C

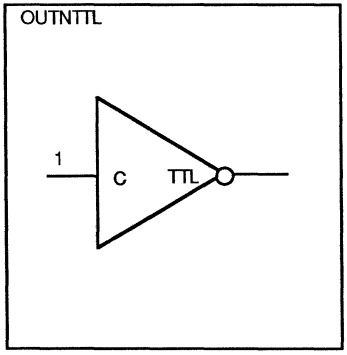
TEST	*TYPICAL*	*UNITS*
I to O, OB t_{PHL}	350	ps
t_{PLH}	300	ps
M_{rise} (O)	550	ps/pF
M_{fall} (O)	550	ps/pF
M_{rise} (OB)	900	ps/pF
M_{fall} (OB)	900	ps/pF

OUTNTTL

DESCRIPTION:
Bistate TTL 8/4mA
inverting output buffer

CELL AREA:
62,984 sq. microns
97.62 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 2.25mW Typ.

DC Characteristics: V_{CC} = 5.0V ±10%; T_A = -55°C to 125°C unless otherwise noted

TEST	*MIN*	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}		1.62	2.23		mA
I_{CCH}		1.91	2.63		mA
I_{OS}		110	130		mA
V_{OH}	2.5			I_{OH} =3.0mA	V
V_{OL} T_A = 0° to 70°C			0.5	I_{OL} = 8.0mA	V
V_{OL}			0.4	I_{OL} =4.0mA	V

AC Characteristics: V_{CC} = - 5.0V ±10%; C_L =15pF; FO = 1; T_A = 25 ° C

TEST	*MIN*	*TYPICAL*	*MAX*	*UNITS*
t_{PHL} (I/O)	2.0	4.0	5.2	ns
t_{PLH} (I/O)	2.0	4.3	6.4	ns

OUTTTL

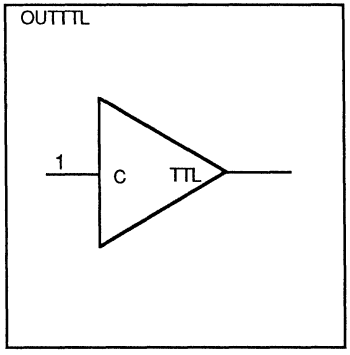
DESCRIPTION:

Bistate TTL 8/4 mA non-inverting output buffer

CELL AREA:

62,981 sq. microns
97.62 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 2.25mW Typ.

DC Characteristics: V_{CC}= 5.0V ±10%; T_A = -55°C to 125°C unless otherwise noted

TEST	*MIN*	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}		1.91	2.52		mA
I_{CCH}		1.62	2.12		mA
I_{OS}		110	130		mA
V_{OH}	2.5			I_{OH} =3.0mA	V
V_{OL} T_A = 0° to 70°C			0.5	I_{OL} = 8.0mA	V
V_{OL}			0.4	I_{OL} =4.0mA	V

AC Characteristics: V_{CC} = - 5.0V ±10%; C_L = 15 pF; FO = 1; T_A = 25°C

TEST	*MIN*	*TYPICAL*	*MAX*	*UNITS*
t_{PHL} (I/O)	2.0	4.0	5.2	ns
t_{PLH} (I/O)	2.0	4.3	6.4	ns

OUTNTRI

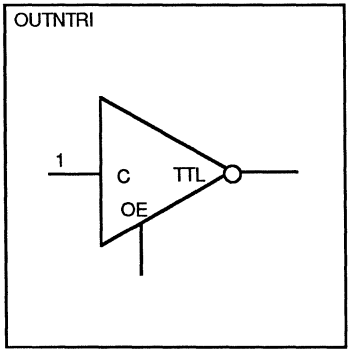
DESCRIPTION:

Tristate TTL 8/4mA inverting output buffer

CELL AREA:

67,014 sq. microns
103.87 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 2.25mW Typ.

DC Characteristics: V_{CC} = 5.0V ±10%; T_A = -55°C to 125°C unless otherwise noted

TEST	*MIN*	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}		2.23	3.0		mA
I_{CCH}		1.94	2.60		mA
I_{CCZ}			2.84		mA
I_{OS}		110	130		mA
I_{OZL}			- 50	V_{OUT} = 0.5v	µA
I_{OZH}			50	V_{OUT} =2.4v	µA
V_{OH}	2.5			I_{OH} =3.0mA	V
V_{OL} T_A = 0°C to 70°C			0.5	I_{OL} = 8.0mA	V
V_{OH}			0.4	I_{OL} =4.0mA	V

AC Characteristics: V_{CC} = - 5.2 V±10%; C_L = 15 pF; FO = 1; T_A = 25°C

TEST	*MIN*	*TYPICAL*	*MAX*	*UNITS*
t_{PHL} (I/O)	2.0	4.0	5.2	ns
t_{PLH} (I/O)	2.0	4.9	7.4	ns
OE to OUT, LZ	2.0	2.8	5.7	ns
OE to OUT, ZL	2.0	5.5	7.2	ns
OE to OUT, HZ	0.5	1.1	1.9	ns
OE to OUT, ZH	1.5	2.1	3.4	ns

OUTTRI

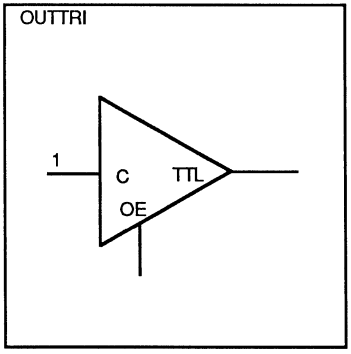
DESCRIPTION:

Tristate TTL 8/4mA
non-inverting output buffer

CELL AREA:

67,014 sq. microns
103.87 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 2.25mW Typ.

DC Characteristics: V_{CC}= 5.0V ±10%; T_A = -55°C to 125°C unless otherwise noted

TEST	*MIN*	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}		2.23	3.0		mA
I_{CCH}		1.94	2.60		mA
I_{CCZ}			2.84		mA
I_{OS}		110	130		mA
I_{OZL}			- 50	V_{OUT} = 0.5v	µA
I_{OZH}			50	V_{OUT} =2.4v	µA
V_{OH}	2.5			I_{OH} =3.0mA	V
V_{OL} T_A = 0°C to 70°C			0.5	I_{OL} = 8.0mA	V
V_{OH}			0.4	I_{OL} =4.0mA	V

AC Characteristics: V_{CC} = - 5.2 V±10%; C_L = 15pF; FO = 1; T_A = 25°C

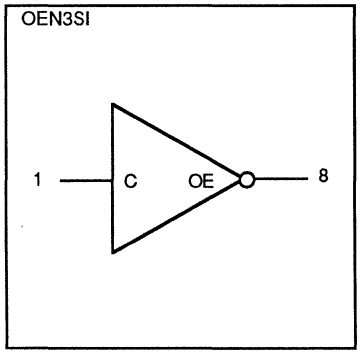
TEST	*MIN*	*TYPICAL*	*MAX*	*UNITS*
t_{PHL} (I/O)	2.0	4.0	5.2	ns
t_{PLH} (I/O)	2.0	4.9	7.4	ns
OE to OUT, LZ	2.0	2.8	5.7	ns
OE to OUT, ZL	2.0	5.5	7.2	ns
OE to OUT, HZ	0.5	1.1	1.9	ns
OE to OUT, ZH	1.5	2.1	3.4	ns

OEN3SI

DESCRIPTION:
Output enable gate for tristate output buffers

CELL AREA:
44,327 sq. microns
68.71 sq. mils

SYMBOL:



PERFORMANCE:

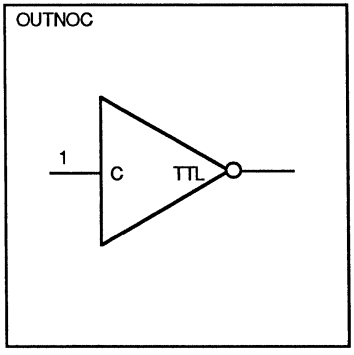
Power Dissipation: 10.30mW Typ.		
AC Characteristics: $V_{CC} = 5.0 \pm 10\%$, $C_L = 0$, FO = 1, $T_A = 25°C$		
TEST	*TYPICAL*	*UNITS*
t_{PHL}	3.0	ns
t_{PLH}	3.0	ns
M_{rise}	20	ps/pF
M_{fall}	80	ps/pF

OUTNOC

DESCRIPTION:
Open collector TTL 8/4 mA
inverting output buffer

CELL AREA:
61,193 sq. microns
94.85 sq. mils

SYMBOL:



PERFORMANCE:

Power Dissipation: 10.0mW Typ.

DC Characteristics: V_{CC}= 5.0V ±10%; T_A = -55°C to 125°C

TEST	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}	1.91	2.52		mA
I_{CCH}	1.62	2.12		mA
V_{OL} T_A = 0° to 70°C		0.50	I_{OL} = 8.0 mA	V
V_{OL}		0.40	I_{OL} = 4.0 mA	V

AC Characteristics: V_{CC} = - 5.0 V ±10%; C_L = 15 pF; FO = 1; T_A = 25°C

TEST	*TYPICAL*	*UNITS*
t_{PHL}	9.4	ns
t_{PLH}	5.3	ns

OUTOC

DESCRIPTION:

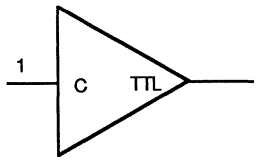
Open collector TTL 8/4 mA
non-inverting output buffer

CELL AREA:

61,193 sq. microns
94.85 sq. mils

SYMBOL:

OUTOC



PERFORMANCE:

Power Dissipation: 10.0mW Typ.

DC Characteristics: V_{CC}= 5.0V ±10%; T_A = -55°C to 125°C

TEST	*TYPICAL*	*MAX*	*CONDITIONS*	*UNITS*
I_{CCL}	1.91	2.52		mA
I_{CCH}	1.62	2.12		mA
V_{OL} (COM)		0.50	I_{OL} = 8.0 mA	V
V_{OL} (MIL)		0.40	I_{OL} =4.0 mA	V

AC Characteristics: V_{CC} = - 5.0 V ±10%; C_L = 15 pF; FO = 1; T_A = 25°C

TEST	*TYPICAL*	*UNITS*
t_{PHL}	9.4	ns
t_{PLH}	5.3	ns

MSI AND LSI FUNCTIONS

DEC4BCH/DEC4BCL

DESCRIPTION:

One-of-four decoder (active low outputs)

CELL AREA:

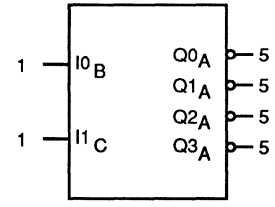
High Speed/Low Power
20,090 sq. microns
31.14 sq. mils

TRUTH TABLE:

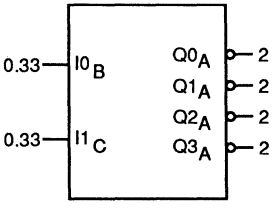
I0	I1	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

SYMBOLS:

DEC4BCH (HIGH SPEED)



DEC4BCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	INPUT	OUTPUT	PHASE	HIGH SPEED	LOW POWER	UNITS
^tPHL	I0	ANY Q	IN	390	560	ps
^tPLH	I0	ANY Q	IN	390	870	ps
^tPHL	I0	ANY Q	OUT	390	560	ps
^tPLH	I0	ANY Q	OUT	390	870	ps
^tPHL	I1	ANY Q	IN	590	970	ps
^tPLH	I1	ANY Q	IN	540	1120	ps
^tPHL	I1	ANY Q	OUT	660	1070	ps
^tPLH	I1	ANY Q	OUT	530	1190	ps
M_{rise}		ANY Q		820	2860	ps/pF
M_{fall}		ANY Q		700	2330	ps/pF

MUX2ABH/MUX2ABL

DESCRIPTION:
Two input multiplexer

CELL AREA:
High Speed/Low Power
15,785 sq. microns
24.47 sq. mils

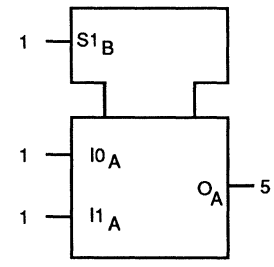
TRUTH TABLE:

S1	*I0*	*I1*	*O*
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

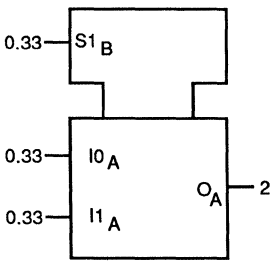
X = Don't care

SYMBOLS:

MUX2ABH (HIGH SPEED)



MUX2ABL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*PHASE*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY 1	O		450	750	ps
t_{PLH}	ANY 1	O		500	1150	ps
t_{PHL}	S1	O	IN	650	1200	ps
t_{PLH}	S1	O	IN	600	1400	ps
t_{PHL}	S1	O	OUT	700	1250	ps
t_{PLH}	S1	O	OUT	600	1450	ps
M_{rise}				840	2870	ps/pF
M_{fall}				760	2660	ps/pF

MUX2BCH/MUX2BCL

DESCRIPTION:
Two input multiplexer

CELL AREA:
High Speed/Low Power
15,785 sq. microns
24.47 sq. mils

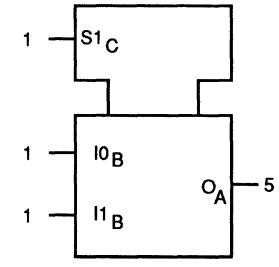
TRUTH TABLE:

S1	*I0*	*I1*	*O*
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

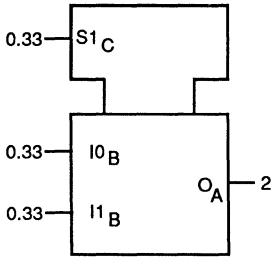
X = Don't care

SYMBOLS:

MUX2BCH (HIGH SPEED)



MUX2BCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*PHASE*	*HIGH SPEED*	*LOW POWER*	*UNITS*
t_{PHL}	ANY 1	O		450	650	ps
t_{PLH}	ANY 1	O		450	1050	ps
t_{PHL}	S1	O	IN	650	1100	ps
t_{PLH}	S1	O	IN	600	1300	ps
t_{PHL}	S1	O	OUT	700	1200	ps
t_{PLH}	S1	O	OUT	600	1400	ps
M_{rise}				840	2870	ps/pF
M_{fall}				760	2660	ps/pF

MUX4ABCH/MUX4ABCL

DESCRIPTION:
Four input multiplexer

CELL AREA:
High Speed/Low Power
31,857 sq. microns
49.38 sq. mils

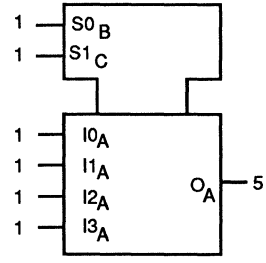
TRUTH TABLE:

S0	S1	I0	I1	I2	I3	Q
0	0	1	X	X	X	1
0	0	0	X	X	X	0
1	0	X	1	X	X	1
1	0	X	0	X	X	0
0	1	X	X	1	X	1
0	1	X	X	0	X	0
1	1	X	X	X	1	1
1	1	X	X	X	0	0

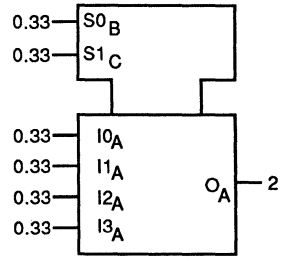
X = Don't care

SYMBOLS:

MUX4ABCH (HIGH SPEED)



MUX4ABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	INPUT	OUTPUT	PHASE	HIGH SPEED	LOW POWER	UNITS
t_{PHL}	ANY 1	O		550	1150	ps
t_{PLH}	ANY 1	O		600	1600	ps
t_{PHL}	S0	O	IN	750	1700	ps
t_{PLH}	S0	O	IN	750	1850	ps
t_{PHL}	S0	O	OUT	800	1650	ps
t_{PLH}	S0	O	OUT	750	1900	ps
t_{PHL}	S1	O	IN	950	2100	ps
t_{PLH}	S1	O	IN	900	2100	ps
t_{PHL}	S1	O	OUT	1000	2250	ps
t_{PLH}	S1	O	OUT	850	2220	ps
M_{rise}				840	2840	ps/pF
M_{fall}				910	2370	ps/pF

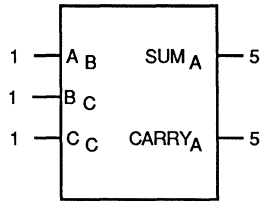
FABCH/FABCL

DESCRIPTION:
Two bit full adder

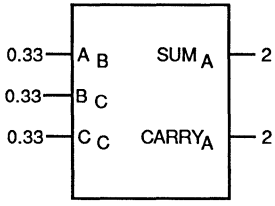
CELL AREA:
High Speed/Low Power
36,162 sq. microns
56.05 sq. mils

SYMBOLS:

FABCH (HIGH SPEED)



FABCL (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 7.02mW Typ.
(Low Power): 2.25mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*LOW POWER*	*UNITS*
^tPHL	A, B, or C	SUM	1130	2000	ps
^tPLH	A, B, or C	SUM	1120	2490	ps
^tPHL	A, B, or C	CARRY	1130	2250	ps
^tPLH	A, B, or C	CARRY	1130	2380	ps
M_{rise}		SUM or CARRY	820	2700	ps/pF
M_{fall}		SUM or CARRY	820	2100	ps/pF

SPECIAL PURPOSE

LVD1H/LVD1M/LVD1L

DESCRIPTION:

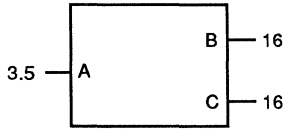
A to B, A to C level shift down

CELL AREA:

High Speed:
11,910 sq. microns
18.46 sq.mils
Medium, Low Power:
10,763 sq. microns
16.68 sq. mils

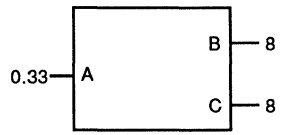
SYMBOLS:

LVD1H (HIGH SPEED)



LVD1M (MEDIUM POWER)

LVD1L (LOW POWER)



PERFORMANCE:

Power Dissipation (High Speed): 8.0mW Typ.
(Medium Power): 2.25mW Typ.
(Low Power): 0.75mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*HIGH SPEED*	*MEDIUM*	*LOW POWER*	*UNITS*
t_{PHL}	A	B or C	0	40	180	ps
t_{PLH}	A	B or C	80	80	40	ps
M_{rise}		B or C	25	70	100	ps/pF
M_{fall}		B or C	85	520	1760	ps/pF

CLKAB

DESCRIPTION:

Inverting clock driver with enable (enable input will not cause false clocking in either state of clock input)

CELL AREA:

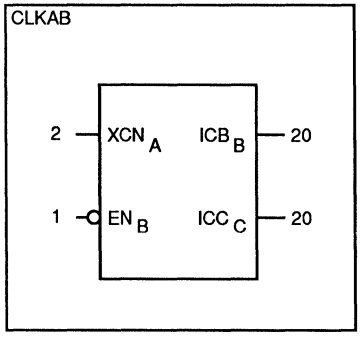
46,781 sq. microns
72.51 sq. mils

TRUTH TABLE:

EN	*XCN*	*ICB*	*ICC*
0	U	D	D
0	D	U	U
1	0	0	0
1	1	0	0

U = Low to High Transition
D = High to Low Transition
X = Don't care

SYMBOL:



PERFORMANCE:

Power Dissipation: 38.5mW Typ.

AC Characteristics:
V_{EE} = -5.2 V ± 10%, C_L = 0, FO = 1
Unless otherwise noted: T_A = 25°C, All numbers typical

TEST	*INPUT*	*OUTPUT*	*25°C TYP.*	*UNITS*
^tPHL	XCN	ICB or ICC	490	ps
^tPLH	XCN	ICB or ICC	520	ps
^tSET	EN	XCN	900	ps
^tHOLD	EN	XCN	0	ps
M_{rise}		ICB or ICC	50	ps/pF
M_{fall}		ICB or ICC	50	ps/pF

BIAS GENERATORS

MBIAS

DESCRIPTION:
Master bias generator for VCS and VBB

CELL AREA:
161,638 sq. microns
250.53 sq. mils

PERFORMANCE:

Power Dissipation: 28.08mW Typ.	
PIN NAME	*FANOUT UNIT LOADS*
V_{CS}	450
V_{BB}	40

IBIAS

DESCRIPTION:
Internal bias generator for VA,VB, and VC

CELL AREA:
30,591 sq. microns
47.42 sq. mils

PERFORMANCE:

Power Dissipation: 11.70mW Typ.	
PIN NAME	*FANOUT UNIT LOADS*
V_A	20
V_B	40
V_C	40

TBIAS

DESCRIPTION:
Reference supply for TTL input buffers

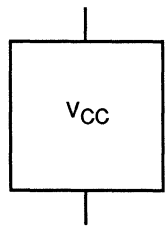
CELL AREA:
14,328 sq. microns
22.21 sq. mils

PERFORMANCE:

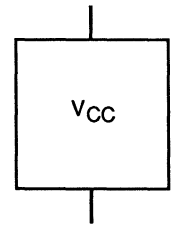
Power Dissipation: 1.60mW	
PIN NAME	*FANOUT UNIT LOAD*
V_{TTL}	40

SYMBOLS:

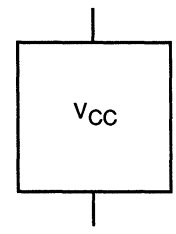
MBIAS



IBIAS



TBIAS



TESTING FOR THE VL2000

To ensure adequate testing the customer should submit a well-defined specification for the VL2000 circuit that includes the following information:

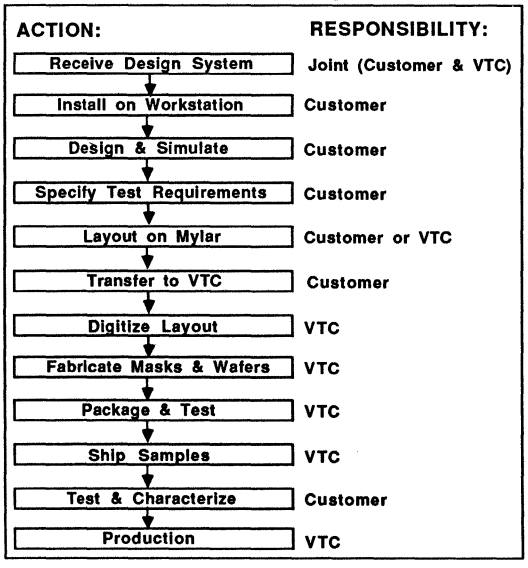
1. A brief functional description of the circuit.
2. A schematic or block diagram of the circuit.
3. A package pin assignment diagram of the circuit.
4. DC and functional requirements with any associated test diagrams. DC and functional requirements may be specified over commercial or military temperature and power supply voltage range.
5. AC test requirements with any associated test diagrams. AC requirements are normally specified at 25°C and nominal supply voltage.
6. A list of test vectors generated by designer during fault simulation.
7. Package requirements.
8. If appropriate, a burn-in connection diagram with specified time and temperature.

VTC's semicustom applications engineers are available for assistance.

Typical costs are quoted on request. Burn-in testing requires a separate quotation.

SEMICUSTOM PRODUCT DESIGN FLOW AND PACKAGE SELECTION

VJ800 ANALOG MASTER CHIP

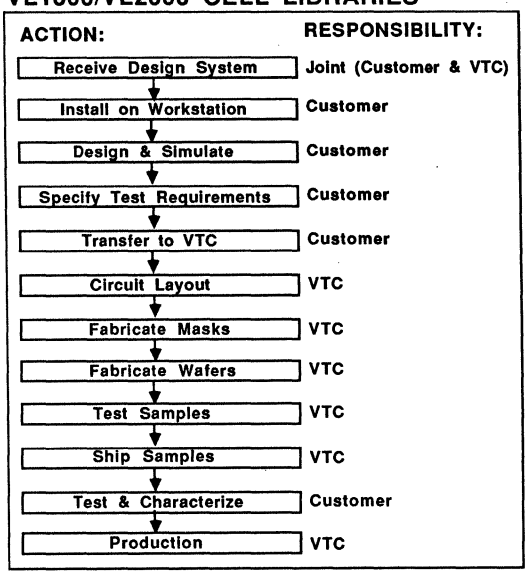


VJ800 PACKAGE SELECTION

PIN COUNT	*18*	*20*	*22*	*24*	*28*	*40*
Plastic DIP*	X				X	X
Cerdip*	X					X
Ceramic DIP*	X		X		X	X
Flatpack		X		X		
TAB Pack**						X
PLCC**					X	X

*Common Footprint
**Common Footprint

VL1000/VL2000 CELL LIBRARIES



VL2000 PACKAGE SELECTION
VL1000 PACKAGE SELECTION

PIN COUNT	*8*	*14*	*16*	*18*	*20*	*22*	*24*	*28*	*40*	*44*	*48*	*64*	*68*	*72*	*84*	*120*	*172*
Plastic DIP		X	X	X	X		X	X	X								
Cerdip	X	X	X	X					X								
Ceram. DIP					X	X	X	X	X								
Flat-pack			X		X		X										
PLCC					X			X		X			X		X		
LCC				X	X			X		X			X		X		
Pin Grid Array																X	X
TAB Pack	Available in a variety of configurations																

NOTES

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SECTION V

QUALITY ASSURANCE

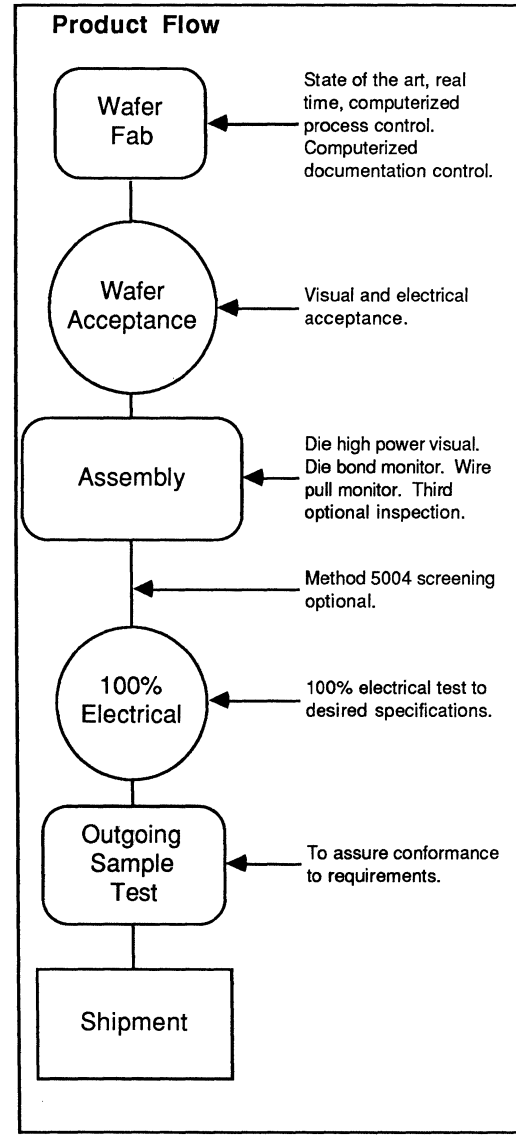
INTRODUCTION: QUALITY ASSURANCE

VTC supplies a quality product at a competitive price.

Since the industry has moved away from AQLs (acceptable quality levels) toward ppm (parts per million), VTC structures its quality program of defect prevention through process control with the goal of zero defects. From initial design to product release, from order entry through on-time delivery, process controls are positioned to ensure the best possible product.

Through extensive automation and computerized data collection and analysis, VTC uses the full spectrum of statistical analysis techniques and minimizes fluctuations that occur in the process. The result is a product that conforms to requirements.

Wafers are processed in a closely monitored class-100/class-10/class-1 fabrication area. As data is gleaned at numerous process control points, it is fed to a central host computer where it is analyzed and reduced to valuable real-time feedback in the form of process control charts, trend evaluations, etc. Standard products receive the same care and process controls as military products. The standard product flow is given here.



TESTING

VTC utilizes Method 5005 of MIL-STD-883 as a model for qualifying new products and processes. For plastic encapsulated devices, alternate tests are performed to ensure expected reliability.

Plastic encapsulated devices are subjected to the following qualification testing:

1) Full electrical characterization at rated temperatures.
2) Steady State Life Test at 125°C. This accelerated life test is performed to simulate long term operation and develop reliability data to predict field failure rate. Based on a 0.7 eV activation energy and the Arrhenious equation, extensive reliability data can be generated in a relatively short period of time.
3) Devices are subjected to an environment of 85°C and 85% humidity while under bias. This test is designed to evaluate the moisture resistance of the plastic encapsulated packages. It detects corrosion-type failure mechanisms caused by ionic contaminants that may have entered the package during the manufacturing process or are bound in the integrated circuit packaging materials. These contaminants are activated by moisture and applied electrical fields.
4) The autoclave test is also designed to evaluate the moisture resistance of plastic encapsulated packages, but in a much shorter time than 85/85 test. It detects corrosion-type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes.
5) Temperature cycling and thermal shock tests are performed to ensure thermal expansion compatability of the materials used in device construction.
6) Industry-standard precautions for electrostatic discharge are performed. Static-free workstations, antistatic floor mats and conductive work surfaces are used when devices are handled. Devices are also stored and shipped in static shielding tubes and containers.
7) Parts are tested to ensure they are latch-up resistant to at least 200mA. Information on ESD and latch-up were covered previously in this book.

Hermetic devices are subjected to the same qualification testing as outlined in MIL-STD-883, Method 5005, as shown in the following table:

Group A - Electrical Tests	LTPD
Static tests at 25°C	2
Static tests at maximum rated operating temperature	3
Static tests at minimum rated operating temperature	5
Dynamic tests at 25°C	2
Dynamic tests at maximum rated operating temperature	3
Dynamic tests at minimum rated operating temperature	5
Functional tests at 25°C	2
Functional tests at maximum and minimum operating temperatures	5
Switching tests at 25°C	2
Switching tests at maximum rated operating temperature	3
Switching tests at minimum rated operating temperature	5

Group B tests			
Test	MIL-STD-883		Quantity/ (accept no.) or LTPD
	Method	Condition	
Physical dimensions	2016		2 devices (no failures)
Resistance to solvents	2015		4 devices (no failures)
Solderability	2022 or 2003	Soldering temperature of 245 ±5°C	15
Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (no failures)
Bond strength (1) Thermo-compression (2)Ultrasonic or wedge	2011	 (1) Test condition D (2) Test condition D	15
Seal: (1) Fine (2) Gross	1014	Fine leak: Condition A Gross leak: Condition C	5
(a) Electrical parameters (b) Electro-static discharge sensitivity classification (c) Electrical parameters	3015	Static electrical at 25°C	15(0)

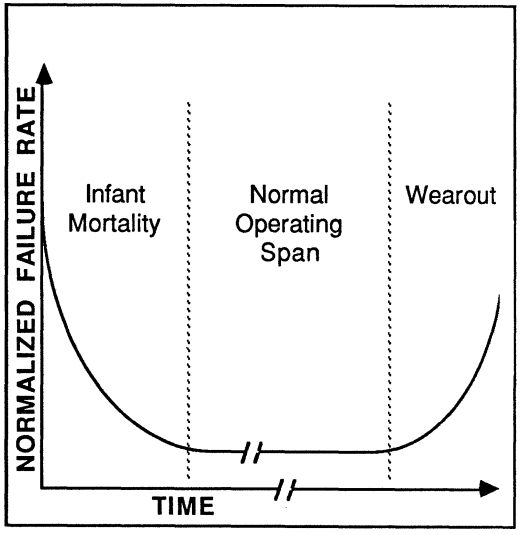
Group C (die related tests)			
Test	MIL-STD-883		Quantity/ (accept no.) or LTPD
	Method	Condition	
(a) Steady state life test (b) End-point electrical parameters	1005	(1000 hours at 125°C) As specified in the applicable device spec.	5
(a) Temperature cycling (b) Constant accelaration (c) Seal (1) Fine (2) Gross (d) Visual examination (e) End-point electrical parameters	1010 2001 1014	Test condition C Test condition E min. Y1 orientation only As applicable As specified in the applicable device specification	15

Group D (package related tests) (for all classes)			
Test	MIL-STD-883		Quantity/ (accept no.) or LTPD
	Method	Condition	
(a) Lead integrity (b) Seal (1)Fine (2)Gross	2004 1014	Test condition B2 (lead fatigue) As applicable	15
(a) Thermal shock (b) Temperature cycling (c) Moisture resistance (d) Seal (1)Fine (2)Gross (e) Visual examination (f) End-point electrical parameters	1011 1010 1004 1014	Test condition B, 15 cycles min. Test condition C, 10 cycles min. As applicable Per visual criteria - methods1004,1010 As specified in the applicable device specification	15
(a) Mechanical shock (b) Vibration, variable frequency (c) Constant acceleration (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End-point electrical parameters	2002 2007 2001 1014	Test condition B minimum Test condition A minimum Test condition E minimum (see 3) As applicable As specified in applicable device specification	15
(a) Salt atmosphere (b) Seal (1) Fine (2) Gross (c) Visual examination	1009 1014	Test condition A minimum Per visual criteria of method 1009	15
(a) Internal water-vapor content	1018	5000 ppm maximum water content at 100°C	3 devices (0 failures) or 5 devices (1 failure)
(a) Adhesion of lead finish	2025		15
(a) Lid torque	2024	Cerdip package only	5(0)

Data from these tests is continually gathered to provide timely feedback for process and reliability improvement. The data collected through an ongoing life test program provides the necessary information to decrease infant mortality and extend the normal operating span of the product.

The operating life of a device is depicted in the classical "bathtub curve," as illustrated. With proper device design and process control, today's integrated circuits generally do not reach the wearout portion of the curve when operated under normal conditions.

VTC 's QA efforts emphasize the elimination of infant mortality and the decrease in failures which occur during the devices's normal operating span.



LOT ACCEPTANCE TESTS

Quality control outgoing tests are performed as shown below:

HERMETIC PACKAGE

- Internal Visual Method 2010
- External Visual Method 2009
- Resistance to Solvents Method 2015
- Physical Dimensions Method 2016
- Gross Seal Test Method 1014 Condition C
- Fine Seal Test Method 1014 Condition A1
- Lead Integrity Method 2004
- Solderability Method 2003
- Final Electrical Test Per Device Specification

PLASTIC PACKAGE

- Internal Visual Method 2014
- External Visual Method 2009
- Resistance to Solvents Method 2015
- Physical Dimensions Method 2016
- Lead Integrity Method 2004
- Solderability Method 2003
- Final Electrical Test Per Device Specification

NOTES:

1. *Methods refer to MIL-STD-883*
2. *The following tests are optional:*
   - *Internal Water-Vapor Content Method 2014*
   - *Electrostatic Discharge Sensitivity Method 3015*
   - *Steady State Life Test Method 1005*
   - *Constant Acceleration Method 2001*
   - *Lid Torque Method 2024*
   - *Thermal Shock Method 1011*
   - *Temperature Cycling Method 1010*
   - *Mechanical Shock Method 2002*
   - *Vibration Variable Frequency Method 2007*
   - *Salt Atmosphere Method 1009*
   - *Burn-In Test Method 1015*

In summary, VTC's quality and reliability program is designed to provide a product that will conform to customer's requirements and continue to give useful service over a long period of time

NOTES

NOTES

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SECTION VI

ORDERING AND PACKAGING

INTRODUCTION: ORDERING AND PACKAGING

VTC offers its products in a wide variety of packages. Dimensions for these packages are shown on the following pages.

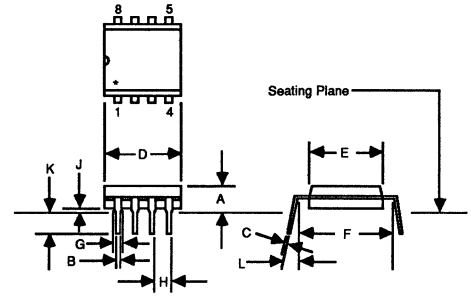
Package offerings include a range of pin counts in Plastic Dual-in-Line Packages (DIP), Ceramic DIPs (Cerdip), Side Brazed Ceramic DIPs, Flatpacks, Plastic Leaded Chip Carriers (PLCC), Ceramic Leadless Chip Carriers (LCC), Plastic SOICs, and Pin Grid Arrays.

Bipolar products are also available in TAB (Tape Automated Bonded) packages. Information concerning advantages and specifications for TAB packaging is available from authorized VTC representatives.

In addition to the above packages, VTC offers LSP products and others in die form. All dice are packaged in containers (die crates) with individual compartments which prevent damage to the die during shipping. Die are sold in multiples of 100.

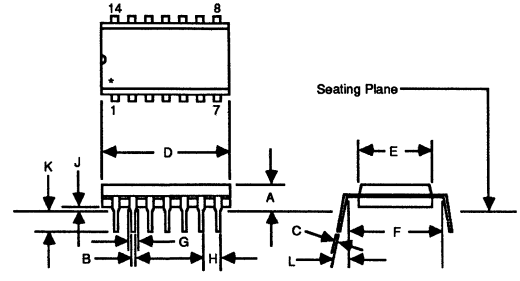
If package offerings given here do not meet the customer's requirements, VTC will address any special or unique package needs.

8 PIN PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	———	0.200	———	5.08
B	0.013	0.020	0.33	0.50
C	0.008	0.015	0.20	0.38
D	0.760	0.780	19.30	19.81
E	0.210	0.310	5.33	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



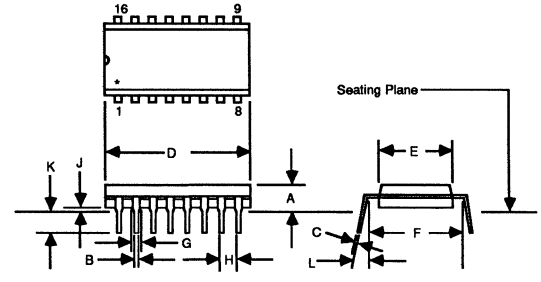
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

14 PIN PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	———	0.200	———	5.08
B	0.013	0.020	0.33	0.50
C	0.008	0.015	0.20	0.38
D	0.800	0.890	20.32	22.60
E	0.250	0.310	6.35	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

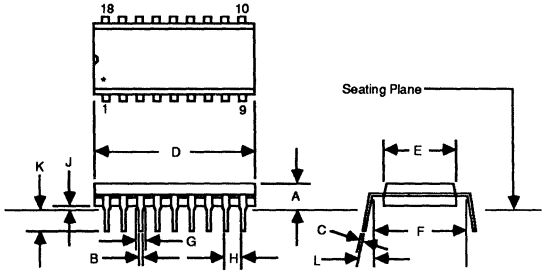
16 PIN PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	———	0.200	———	5.08
B	0.013	0.020	0.33	0.50
C	0.008	0.015	0.20	0.38
D	0.840	0.900	21.33	22.86
E	0.250	0.310	6.35	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

18 PIN PLASTIC DIP

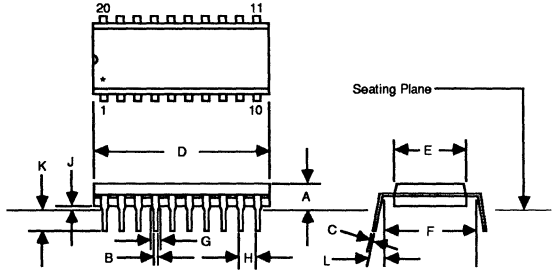
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.015	0.023	0.38	0.58
C	0.008	0.016	0.020	0.41
D	—	0.940	—	23.86
E	0.190	0.250	4.82	6.35
F	0.280	0.300	7.11	7.61
G	0.028	0.072	0.71	1.83
H	0.090	0.110	2.28	2.79
J	0.020	—	0.51	—
K	0.100	—	2.54	—
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

20 PIN PLASTIC DIP

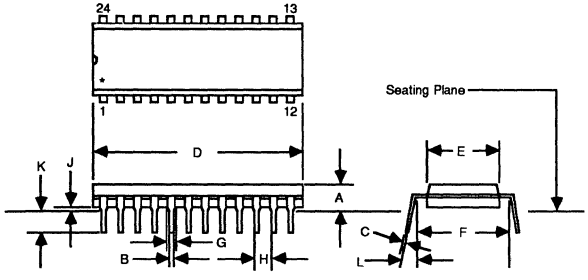
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.025	1.042	26.04	26.47
E	0.240	0.260	6.10	6.60
F	0.290	0.325	7.37	8.25
G	0.030	0.080	0.76	2.03
H	0.090	0.110	2.29	2.79
J	0.020	0.060	0.51	1.52
K	0.125	0.150	3.18	3.81
L	0°	10°	0°	10°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24 PIN SLIMLINE PLASTIC DIP

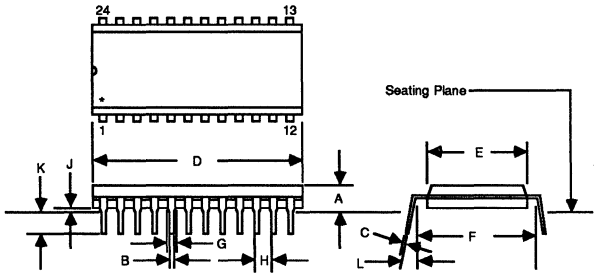
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.240	1.265	31.50	32.13
E	0.250	0.300	6.35	7.62
F	0.290	0.330	7.37	8.38
G	0.030	0.080	0.76	2.03
H	0.090	0.110	2.29	2.79
J	0.020	0.060	0.51	1.52
K	0.125	0.150	3.18	3.81
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24 PIN PLASTIC DIP

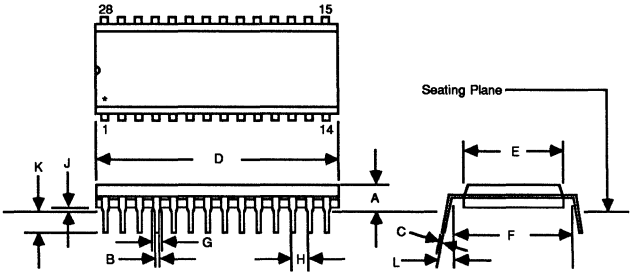
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	———	0.200	———	5.08
B	0.013	0.020	0.33	0.50
C	0.008	0.015	0.20	0.38
D	1.250	1.290	31.75	32.76
E	0.250	0.410	6.35	10.41
F	0.290	0.420	7.37	10.66
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

28 PIN PLASTIC DIP

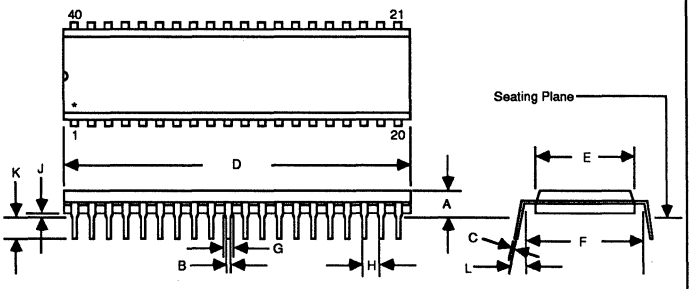
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.015	0.023	0.38	0.58
C	0.008	0.016	0.20	0.41
D	—	1.100	—	27.92
E	0.290	0.350	7.36	8.88
F	0.380	0.400	9.64	10.15
G	0.028	0.072	0.71	1.83
H	0.090	0.110	2.28	2.79
J	0.020	—	0.51	—
K	0.100	—	2.54	—
L	0°	10°	0°	10°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

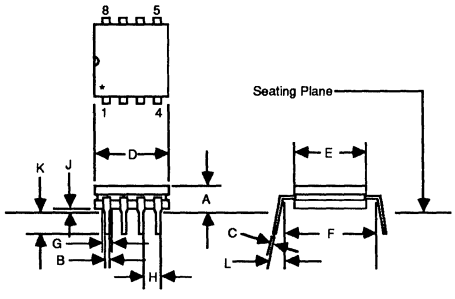
40 PIN PLASTIC DIP

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	———	0.200	———	5.08
B	0.013	0.020	0.33	0.50
C	0.008	0.015	0.20	0.38
D	2.035	2.085	51.68	52.95
E	0.250	0.310	6.35	7.87
F	0.280	0.320	7.11	8.12
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



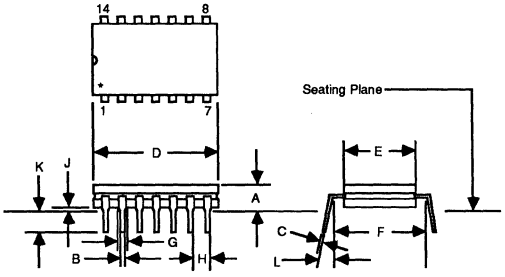
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

8 PIN CERAMIC DIP (Cerdip)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.015	0.023	0.38	0.58
C	0.008	0.015	0.20	0.38
D	—	0.400	—	10.15
E	0.220	0.280	5.58	7.11
F	0.290	0.310	7.36	7.87
G	0.026	0.070	0.66	1.78
H	0.090	0.110	2.28	2.79
J	0.020	—	0.51	—
K	0.100	—	2.54	—
L	0°	15°	0°	15°



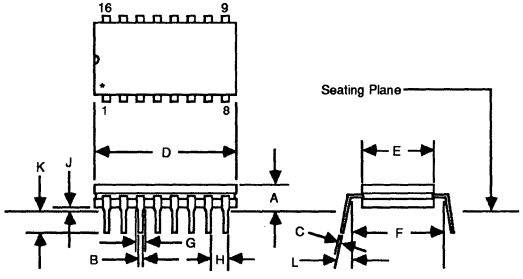
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

14 PIN CERAMIC DIP (Cerdip)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.750	0.770	19.05	19.55
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

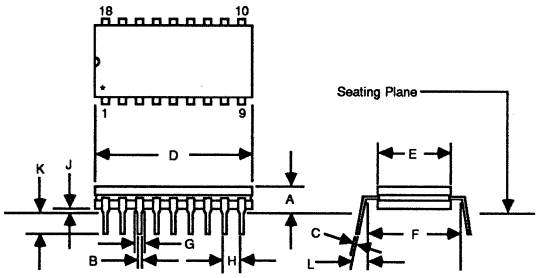
16 PIN CERAMIC DIP (Cerdip)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.750	0.770	19.05	19.55
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

18 PIN CERAMIC DIP (Cerdip)

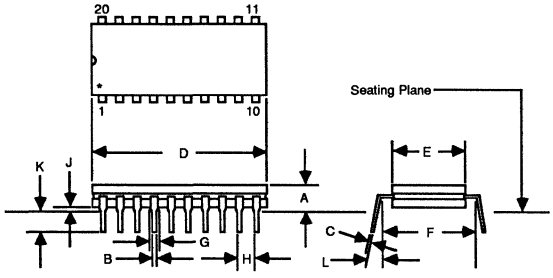
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	——	1.060	——	26.92
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

20 PIN CERAMIC DIP (Cerdip)

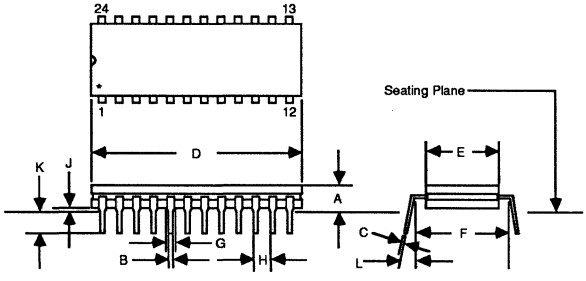
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.250	0.300	6.35	7.62
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

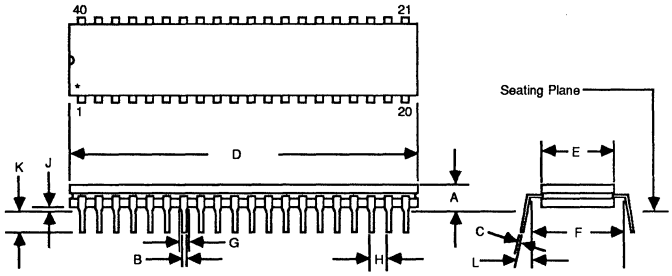
24 PIN CERAMIC DIP (Cerdip)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.250	0.300	6.35	7.62
E	0.220	0.410	5.59	10.41
F	0.290	0.420	7.37	10.66
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



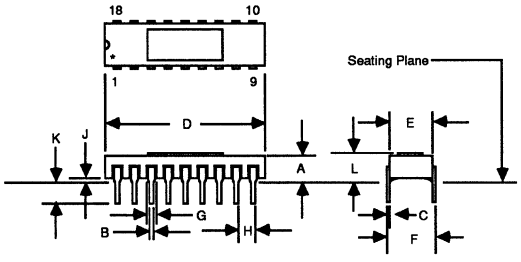
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

40 PIN CERAMIC DIP (Cerdip)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	2.025	2.075	51.43	52.70
E	0.530	0.600	13.46	15.24
F	0.540	0.610	13.71	15.49
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



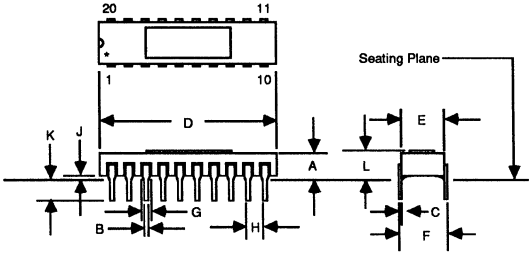
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

18 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.890	0.910	22.60	23.11
E	0.290	0.320	7.36	8.12
F	0.300	0.300	7.62	7.62
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	——	0.100	——	2.54



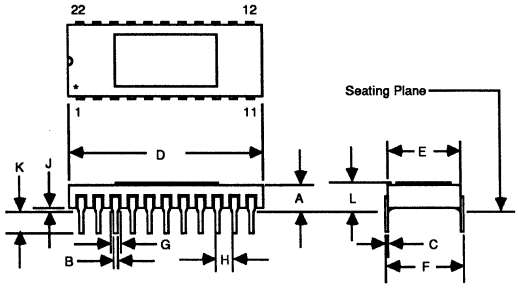
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

20 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	0.990	1.010	25.14	25.65
E	0.290	0.320	7.36	8.12
F	0.300	0.300	7.62	7.62
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	——	0.100	——	2.54



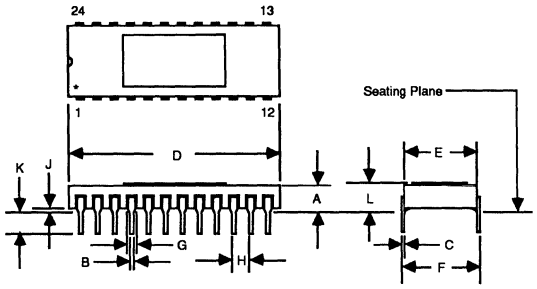
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

22 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.070	1.090	27.17	27.68
E	0.400	0.420	10.16	10.66
F	0.400	0.400	10.16	10.16
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	——	0.100	——	2.54



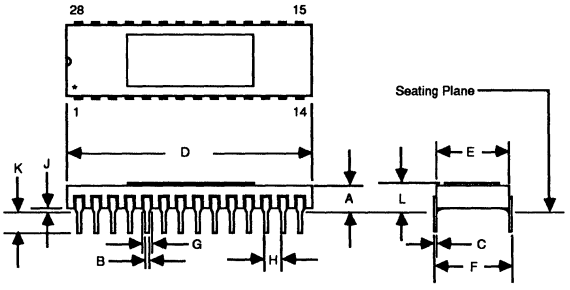
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

24 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.190	1.210	27.17	27.68
E	0.590	0.620	14.98	15.74
F	0.600	0.600	15.24	15.24
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	——	0.100	——	2.54



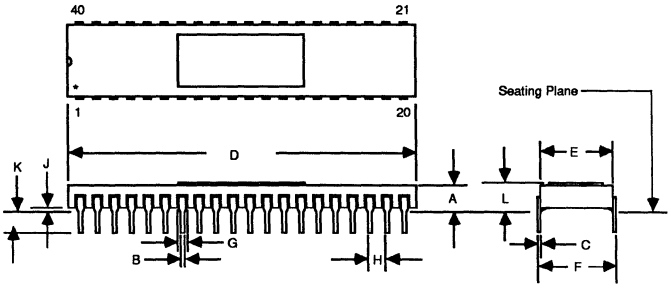
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

28 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.390	1.410	35.31	35.81
E	0.590	0.620	14.99	15.75
F	0.600	0.600	15.24	15.24
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



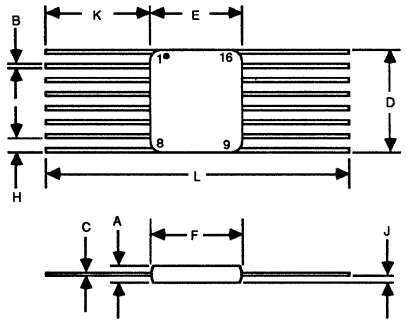
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

40 PIN SIDE BRAZED CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	——	0.200	——	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	1.950	2.050	49.53	52.07
E	0.570	0.600	14.47	15.24
F	0.580	0.620	14.73	15.74
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°

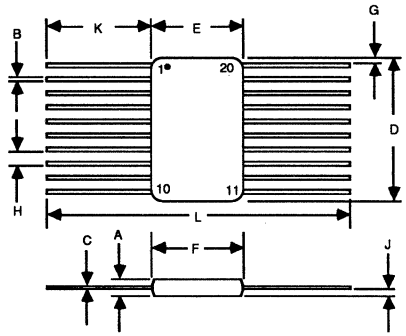


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

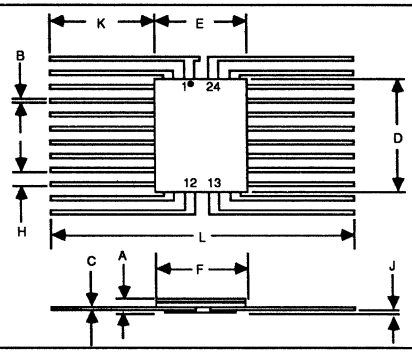
16 PIN FLATPACK				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.064	0.085	1.62	2.15
B	0.014	0.020	0.35	0.50
C	0.008	0.015	0.20	0.38
D	0.390	0.410	9.90	10.41
E	—	0.300	—	7.62
F	—	0.320	—	8.12
G	—	0.050	—	1.27
H	0.050	0.050	1.27	1.27
J	0.010	0.030	0.25	0.76
K	—	0.250	—	6.35
L	—	1.080	—	27.43



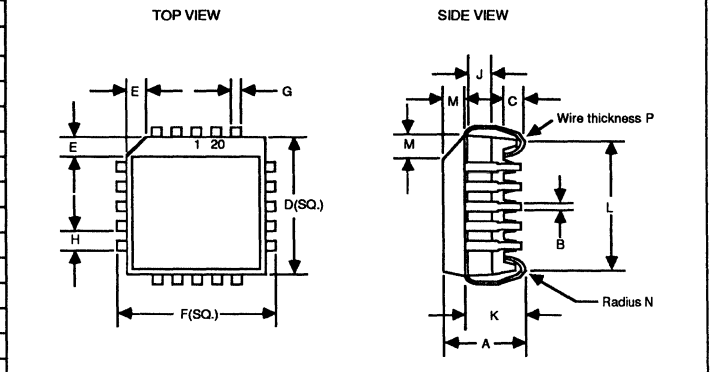
20 PIN FLATPACK				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.064	0.085	1.62	2.15
B	0.014	0.020	0.35	0.50
C	0.008	0.015	0.20	0.38
D	—	0.528	—	13.41
E	—	0.508	—	12.90
F	—	0.518	—	13.15
G	—	0.050	—	1.27
H	0.050	0.050	1.27	1.27
J	0.010	0.030	0.25	0.76
K	—	0.250	—	6.35
L	—	1.080	—	27.43



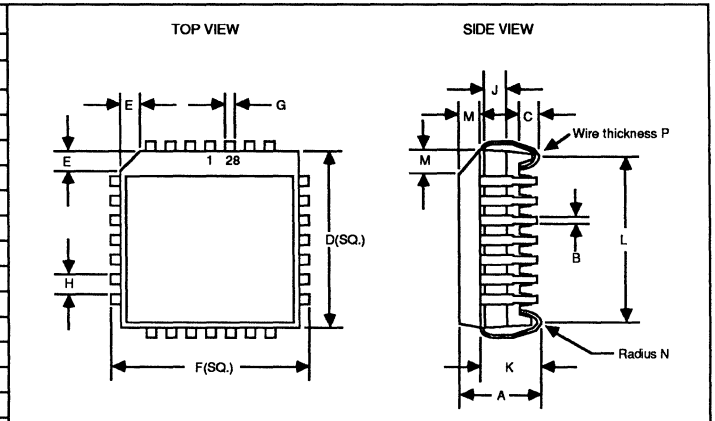
24 PIN FLATPACK				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.080	—	2.03
B	0.015	0.019	0.38	0.48
C	0.004	0.006	0.10	0.15
D	0.391	0.405	9.92	10.28
E	0.264	0.276	6.70	7.01
F	0.264	0.276	6.70	7.01
H	0.045	0.055	1.14	1.40
J	0.017	0.023	0.43	0.58
K	—	0.365	—	9.27
L	—	1.00	—	25.40



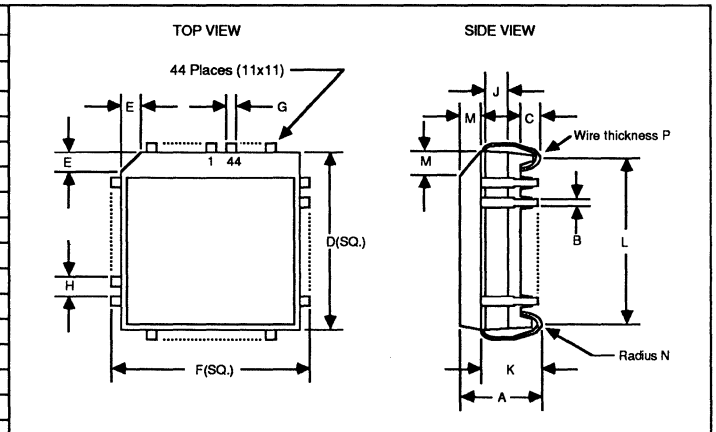
20 PIN PLASTIC LEADED CHIP CARRIER (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.19	4.57
B	0.013	0.021	0.33	0.53
C	0.020	—	0.508	—
D	0.350	0.356	8.89	9.04
E	0.042	0.048	1.06	1.21
F	0.385	0.395	9.77	10.03
G	0.026	0.032	0.66	0.81
H	0.050	0.050	1.27	1.27
J	0.040	0.050	1.01	1.52
K	0.095	0.125	2.41	3.17
L	0.290	0.330	7.36	8.38
M	0.042	0.056	1.06	1.42
N	0.020	0.040	0.50	1.01
P	0.004	0.012	0.10	0.30



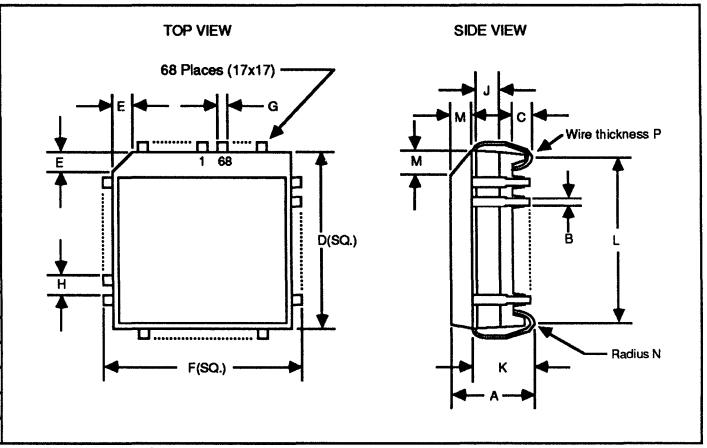
28 PIN PLASTIC LEADED CHIP CARRIER (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.191	4.572
B	0.013	0.021	0.330	0.533
C	0.020	—	0.508	—
D	0.450	0.456	11.43	11.58
E	0.042	0.048	1.066	1.220
F	0.485	0.495	12.41	12.58
G	0.026	0.032	0.660	0.813
H	0.050	0.050	1.27	1.27
J	0.040	0.050	1.016	1.270
K	0.095	0.125	2.413	3.175
L	0.390	0.430	9.906	10.93
M	0.042	0.056	1.066	1.423
N	0.020	0.040	0.508	1.015
P	0.004	0.004	0.102	0.102



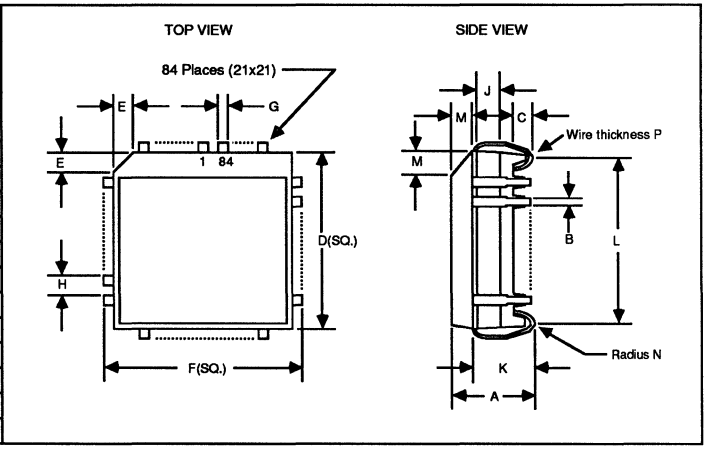
44 PIN PLASTIC LEADED CHIP CARRIER (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.19	4.57
B	0.013	0.018	0.33	0.53
C	0.020	—	0.50	—
D	0.650	0.656	16.51	16.66
E	0.042	0.048	1.06	1.21
F	0.685	0.695	17.39	17.65
G	0.026	0.032	0.66	0.81
H	0.050	0.050	1.27	1.27
J	0.040	0.060	1.01	1.52
K	0.095	0.125	2.41	3.17
L	0.600	0.630	15.24	16.00
M	0.042	0.056	1.06	1.42
N	0.020	0.040	0.50	1.01
P	0.004	0.012	0.10	0.30



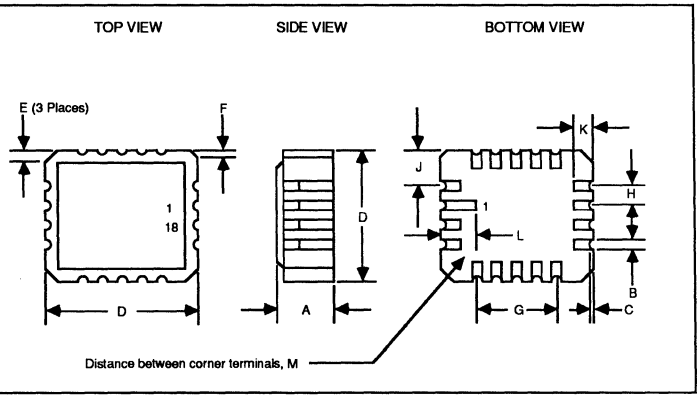
68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.191	4.572
B	0.013	0.021	0.330	0.533
C	0.020	—	0.508	—
D	0.950	0.956	24.13	24.28
E	0.042	0.048	1.066	1.220
F	0.985	0.995	25.02	25.27
G	0.026	0.032	0.660	0.813
H	0.050	0.050	1.27	1.27
J	0.040	0.050	1.016	1.270
K	0.095	0.125	2.413	3.175
L	0.910	0.930	23.11	23.62
M	0.042	0.056	1.066	1.423
N	0.020	0.040	0.508	1.015
P	0.004	0.004	0.102	0.102



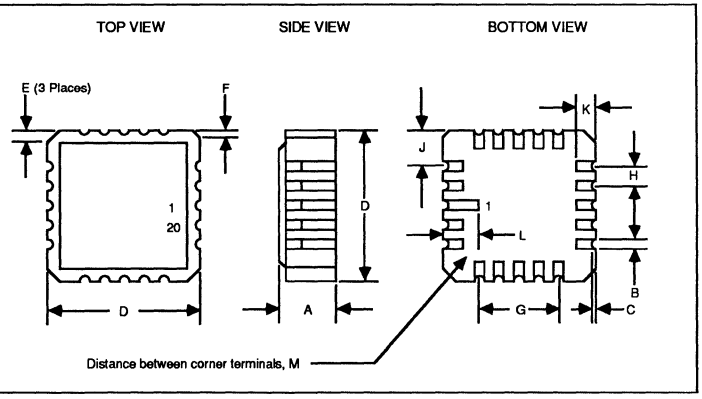
84 PIN PLASTIC LEADED CHIP CARRIER (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.191	4.572
B	0.013	0.021	0.330	0.533
C	0.020	—	0.508	—
D	1.150	1.156	29.21	29.36
E	0.042	0.048	1.066	1.220
F	1.185	1.195	30.10	30.35
G	0.026	0.032	0.660	0.813
H	0.050	0.050	1.27	1.27
J	0.040	0.050	1.016	1.270
K	0.095	0.125	2.413	3.175
L	1.110	1.130	28.19	28.70
M	0.042	0.056	1.066	1.423
N	0.020	0.040	0.508	1.015
P	0.004	0.004	0.102	0.102



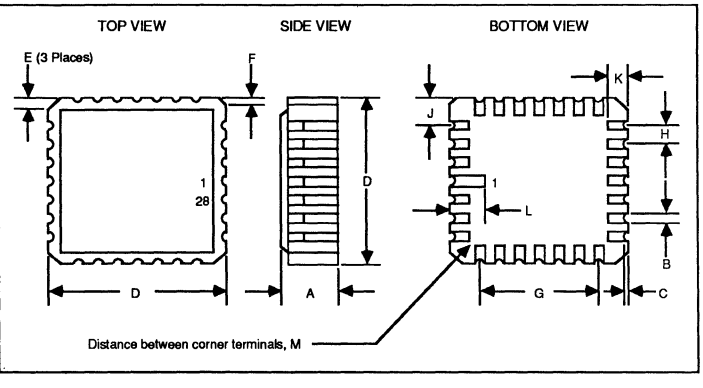
18 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.064	0.100	1.63	2.54
B	0.022	0.028	0.555	0.715
C	0.003	—	0.08	—
D	0.342	0.358	8.69	9.09
E	0.040	0.040	1.02	1.02
F	0.020	0.020	0.508	0.508
G	0.200	0.200	5.08	5.08
H	0.050	0.050	1.27	1.27
J	0.075	0.075	1.905	1.905
K	0.045	0.055	1.14	1.39
L	0.085	0.085	2.16	2.16
M	0.015	—	0.381	—



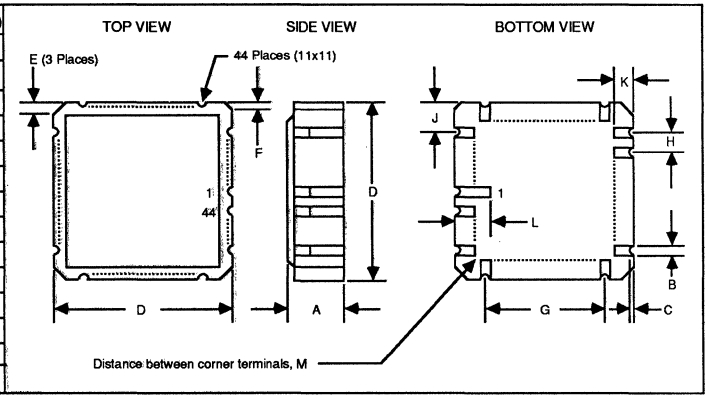
20 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.054	0.085	1.37	2.15
B	0.022	0.028	0.55	0.71
C	0.004	0.017	0.10	0.43
D	0.325	0.340	8.25	8.63
E	0.040	0.040	1.01	1.01
F	0.020	0.020	0.50	0.50
G	0.155	0.165	3.93	4.19
H	0.050	0.050	1.27	1.27
J	0.065	0.085	1.65	2.15
K	0.045	0.055	1.14	1.39
L	0.077	0.093	1.95	2.36
M	0.015	—	0.38	—



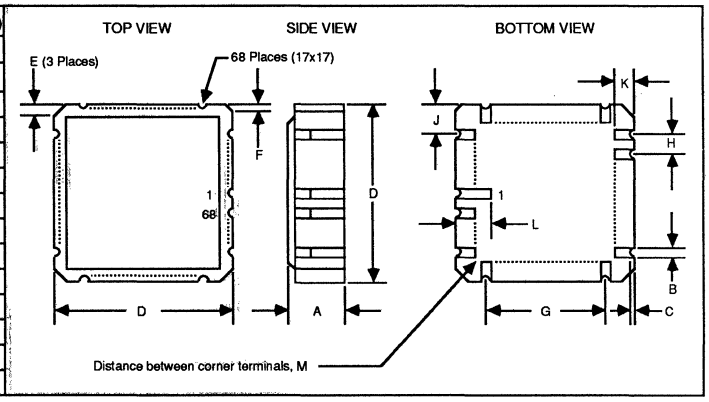
28 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.054	0.085	1.37	2.15
B	0.022	0.028	0.55	0.71
C	0.004	0.017	0.10	0.43
D	0.442	0.458	11.22	11.63
E	0.040	0.040	1.01	1.01
F	0.020	0.020	0.50	0.50
G	0.300	0.300	7.62	7.62
H	0.050	0.050	1.27	1.27
J	0.065	0.085	1.65	2.15
K	0.045	0.055	1.14	1.39
L	0.077	0.093	1.95	2.36
M	0.015	—	0.38	—



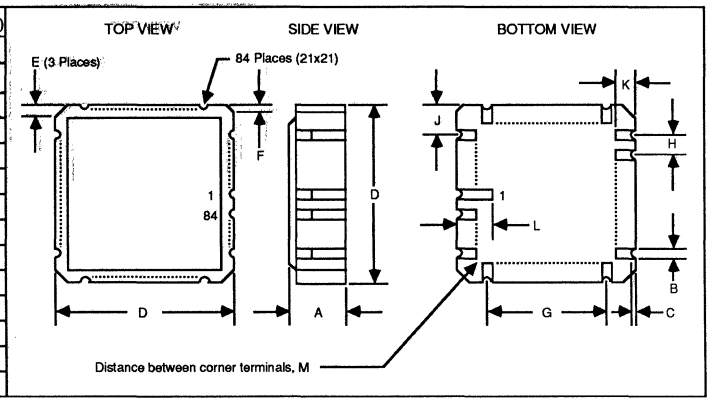
44 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.054	0.085	1.37	2.15
B	0.022	0.028	0.55	0.71
C	0.004	0.017	0.10	0.43
D	0.643	0.660	16.33	16.76
E	0.040	0.040	1.01	1.01
F	0.020	0.020	0.50	0.50
G	0.542	0.558	13.71	14.17
H	0.050	0.050	1.27	1.27
J	0.065	0.085	1.65	2.15
K	0.045	0.055	1.14	1.39
L	0.077	0.093	1.95	2.36
M	0.015	—	0.38	—



68 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.064	0.100	1.63	2.54
B	0.022	0.028	0.555	0.715
C	0.003	—	0.08	—
D	0.442	0.458	11.23	11.63
E	0.040	0.040	1.02	1.02
F	0.020	0.020	0.508	0.508
G	0.300	0.300	7.62	7.62
H	0.050	0.050	1.27	1.27
J	0.075	0.075	1.905	1.905
K	0.045	0.055	1.14	1.39
L	0.085	0.085	2.16	2.16
M	0.015	—	0.381	—

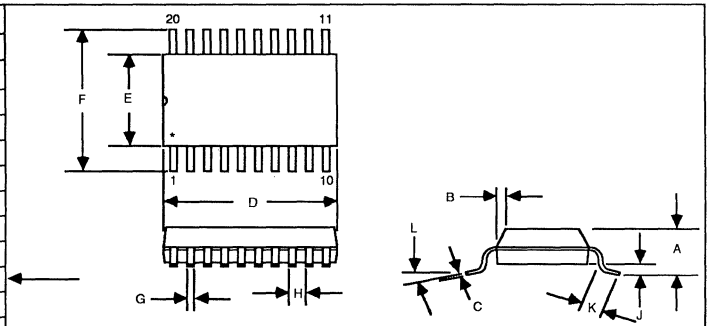


84 PIN CERAMIC LEADLESS CHIP CARRIER (LCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.064	0.100	1.63	2.54
B	0.022	0.028	0.555	0.715
C	0.003	—	0.08	—
D	0.442	0.458	11.23	11.63
E	0.040	0.040	1.02	1.02
F	0.020	0.020	0.508	0.508
G	0.300	0.300	7.62	7.62
H	0.050	0.050	1.27	1.27
J	0.075	0.075	1.905	1.905
K	0.045	0.055	1.14	1.39
L	0.085	0.085	2.16	2.16
M	0.015	—	0.381	—



20 PIN SOIC

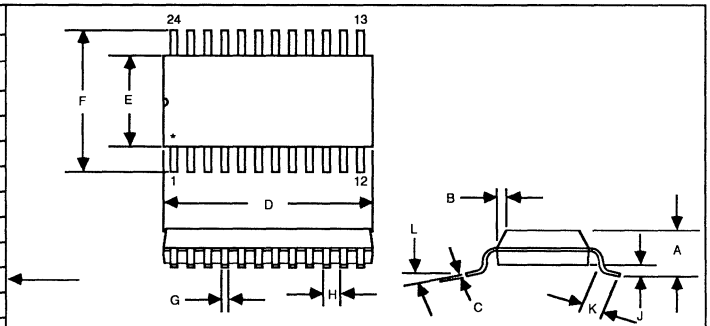
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.092	0.105	2.35	2.65
B	0.009	0.030	0.25	0.75
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.300	7.40	7.60
F	0.393	0.420	10.00	10.65
G	0.013	0.020	0.35	0.49
H	0.050	0.050	1.27	1.27
J	0.003	0.012	0.10	0.30
K	0.015	0.050	0.40	1.27
L	0°	8°	0°	8°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

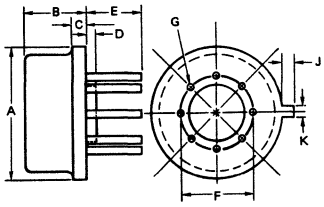
24 PIN SOIC

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.092	0.105	2.35	2.65
B	0.009	0.030	0.25	0.75
C	0.009	0.013	0.23	0.32
D	0.598	0.615	15.20	15.62
E	0.291	0.300	7.40	7.60
F	0.393	0.420	10.00	10.65
G	0.013	0.020	0.35	0.49
H	0.050	0.050	1.27	1.27
J	0.003	0.012	0.10	0.30
K	0.015	0.050	0.40	1.27
L	0°	8°	0°	8°

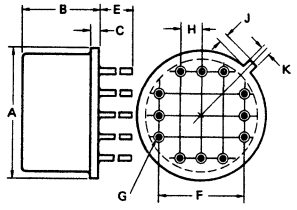


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

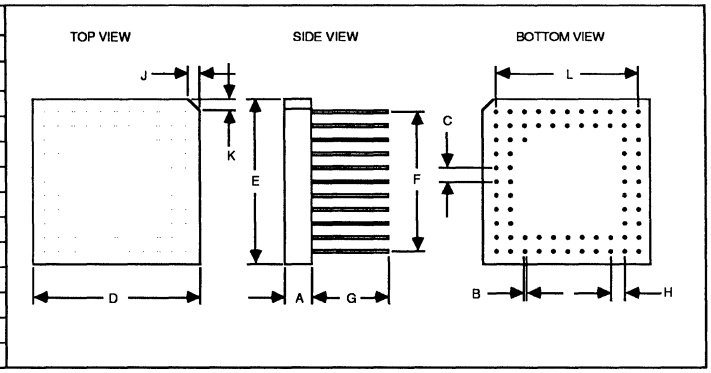
8 PIN METAL CAN (TO-99)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.345	0.365	8.76	9.27
B	0.165	0.185	4.19	4.70
C	0.020	0.040	0.51	1.02
D	0.010	0.045	0.25	1.14
E	0.500	0.550	12.70	13.97
F	0.200	BSC	5.08	BSC
G	0.016	0.021	0.41	0.53
J	0.027	0.045	0.69	1.14
K	0.027	0.034	0.69	0.86



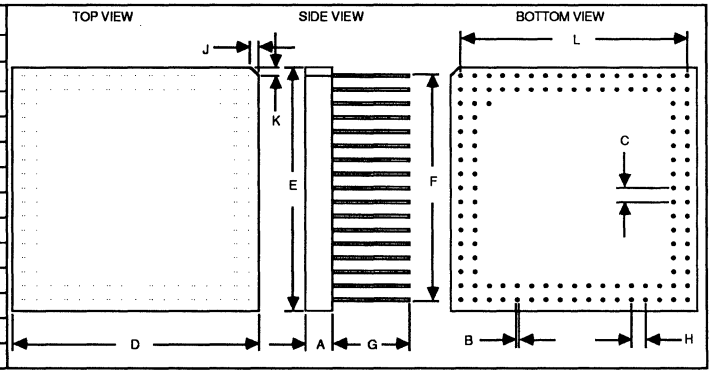
12 PIN METAL CAN (TO-8)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.585	0.615	14.86	15.62
B	0.130	0.150	3.30	3.81
C	—	0.040	—	1.02
D	—	—	—	—
E	0.500	0.550	12.70	13.97
F	0.400	BSC	10.16	BSC
G	0.016	0.021	0.41	0.53
H	0.100	BSC	2.54	BSC
J	0.027	0.045	0.69	1.14
K	0.027	0.034	0.69	0.86



72 PIN GRID ARRAY				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.067	0.090	1.70	2.28
B	0.016	0.020	0.40	0.50
C	0.100	0.100	2.54	2.54
D	1.089	1.111	27.66	28.21
E	1.089	1.111	27.66	28.21
F	0.990	1.010	25.14	25.65
G	0.139	0.161	3.53	4.08
H	0.100	0.100	2.54	2.54
J	0.050	0.050	1.27	1.27
K	0.050	0.050	1.27	1.27
L	0.990	1.010	25.14	25.65

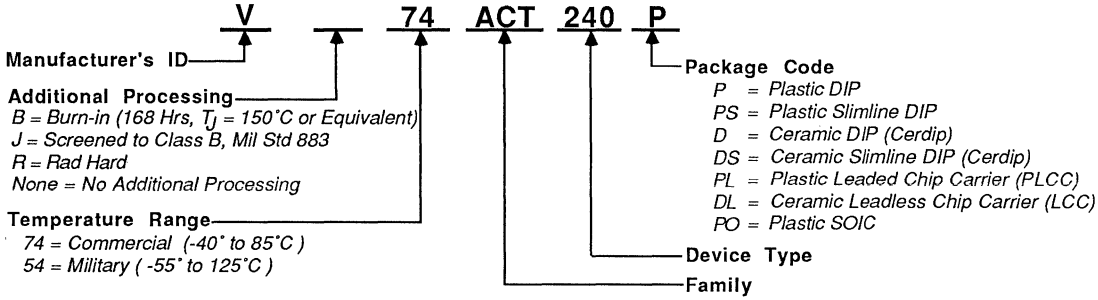


120 PIN GRID ARRAY				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.067	0.090	1.70	2.28
B	0.016	0.020	0.40	0.50
C	0.100	0.100	2.54	2.54
D	1.287	1.332	32.68	33.83
E	1.287	1.332	32.68	33.83
F	1.190	1.210	30.22	30.73
G	0.139	0.161	3.53	4.08
H	0.100	0.100	2.54	2.54
J	0.050	0.050	1.27	1.27
K	0.050	0.050	1.27	1.27
L	1.190	1.210	30.22	30.73

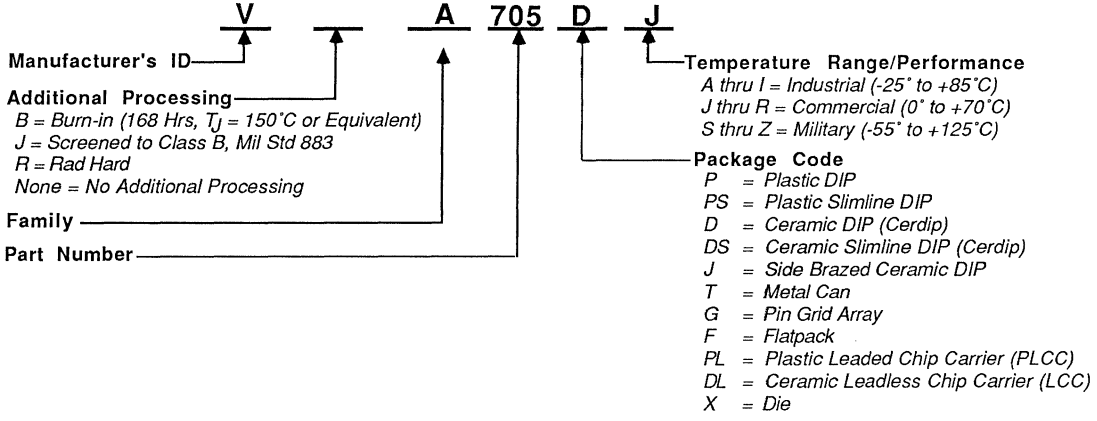


NOTES

ORDERING GUIDE FOR CMOS INTERFACE LOGIC:



ORDERING GUIDE FOR BIPOLAR PRODUCTS:



NOTES

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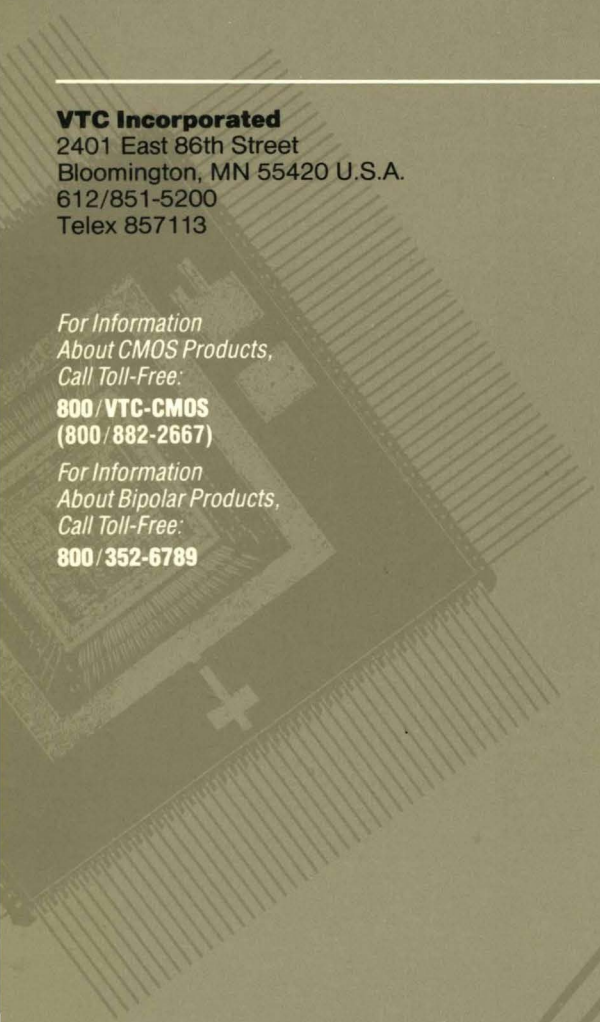

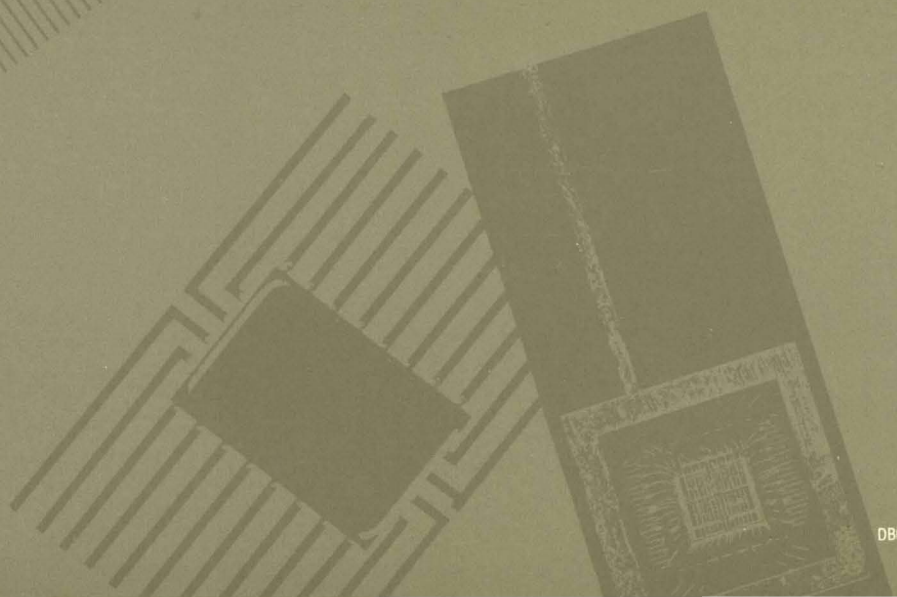

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