VITESSE

1992 Product Data Book

VITESSE
SEMICONDUCTOR CORPORATION

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$10.00

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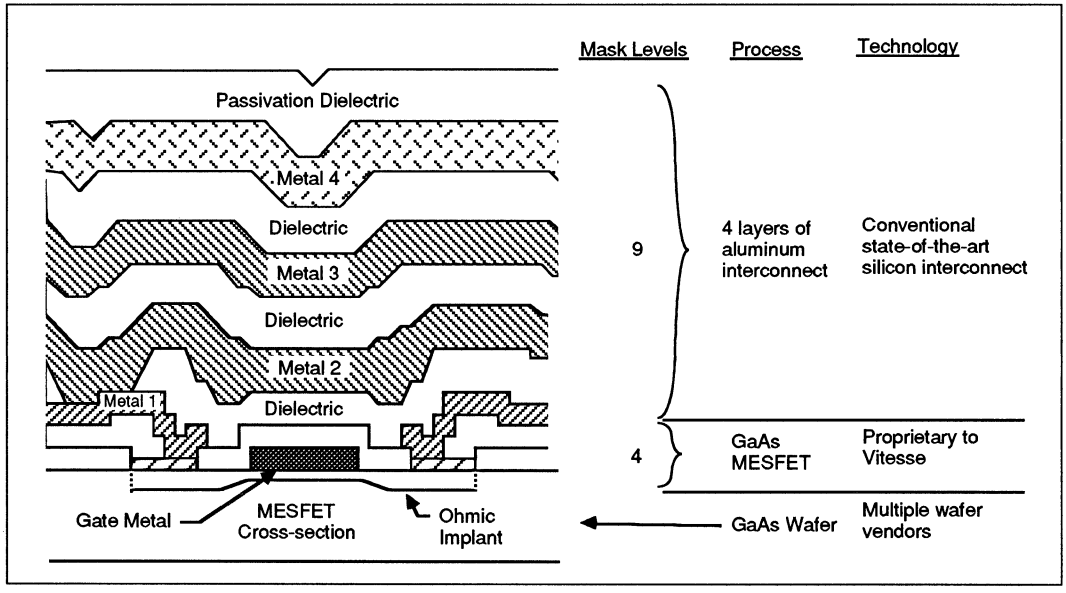
INTRODUCTION TO THE 1992 PRODUCT DATA BOOK

This 1992 Product Data Book contains the latest information on the entire range of products and services from Vitesse Semiconductor Corporation. We are pleased to present you with this compilation of information in one convenient source. This book includes complete product data sheets for all standard products, gate arrays, and foundry services. Supplementary information regarding packaging, applications, quality assurance and reliability is also included.

Vitesse Semiconductor Corporation is a proven leader in the design and manufacture of high performance digital LSI and VLSI GaAs ICs. The company, which was founded in 1984, has developed a revolutionary new process, allowing it to deliver the first affordable very large scale integrated circuits (VLSI) in gallium arsenide (GaAs). With the introduction of the FURY Gate Array family in 1988, Vitesse became the first company to deliver VLSI GaAs circuits into production systems. In 1991, Vitesse complemented its VLSI offerings with the introduction of the FX Gate Array family with integration reaching 350,000 gates.

The key to success for Vitesse has been the development of its unique H-GaAs manufacturing technology. Rather than developing a process based on existing GaAs microwave transistor technology as others in the GaAs industry had done, Vitesse chose to develop an entirely new process based on proven silicon MOS manufacturing methods. This strategy solved two major problems which had prevented GaAs ICs from receiving wide acceptance: low complexity and high cost. The result is a high yielding, proprietary process which produces circuits with a speed-power product unmatched by any other IC manufacturing technology.

The market for Vitesse's products is existing high performance silicon users. In order to compete in this marketplace, Vitesse chose to make its products look and feel exactly like silicon products, but with significant improvements in speed, complexity, and reduced power dissipation. The combination of GaAs performance and silicon MOS manufacturing techniques is the key Vitesse advantage. The results are families of IC products that set new performance standards at prices



equal to high performance silicon bipolar products and provide equal price/performance ratios to BiCMOS products.

Vitesse is committed to providing the highest performance integrated circuits in the world. Vitesse products have surpassed silicon ECL products in terms of performance and complexity, all at a lower price. Our next objective is to introduce an alternative to BiCMOS which provides equivalent complexity at far superior performance. The Vitesse manufacturing process has been designed to realize this objective with a combination of process innovations and proven MOS manufacturing techniques. The distinguishing features of the Vitesse process are: 1) excellent transistor electrical parameter control, 2) unprecedented manufacturing yields on VLSI complexity GaAs circuits, and 3) process simplicity and fast cycle time.

Vitesse has pioneered the now well-accepted concept of designing GaAs products that are compatible with existing silicon technologies. Input/output levels and power supplies found in TTL, ECL and CMOS are standard in the entire family of Vitesse products. In addition, standard ASIC (application specific IC) design tools allow designers to implement their circuits in a Vitesse gate array or cell based product exactly as they would with conventional silicon ASIC products. Synthesis tools, such as Synopsys™, are supported and facilitate retargetting a silicon design into GaAs technology with a minimum of effort and risk.

Memory

In addition to embedded RAM and register file capability in our ASIC products, Vitesse also offers several stand-alone RAM products. These products range in complexity from 1Kbits to 16Kbits. Some specialized functions, such as fast purging and self-timed or registered operation, are also available.

Datacommunications

The G-TAXIchips™ are a general purpose interface for very high speed point-to-point communications over coaxial or fiber-optic media. The G-TAXI transmitter and receiver are capable of two speed grades. The -1.2 parts are capable of handling serial data at rates up to 1.25 Gbits/sec. The -1.0 parts can handle up to 1.0625 Gbits/sec. The speed of the G-TAXI system is tuneable (±10%) from its center frequency to provide flexibility. The GTAXIchips are compatible with the ANSI X3T9.3 Fiber Channel Standard. The G-TAXIchips can also be used for proprietary links.

The G-TAXIchips consist of 4 devices: the VSC7101 Transmitter, VSC7102 Receiver, VSC7103 Multiplexer, and VSC7104 Demultiplexer. The G-TAXIchips provide simple point-to-point serial physical transport for parallel data. The G-TAXI Multiplexer/Transmitter (Mux/Tx) inputs originate in a sending host system, using a standard ready/strobe handshake for parallel data transfer. An output ready pulse from the G-TAXI Receiver/Demultiplexer (Rx/Dmx) indicates that data is available to the receiving host system.

The Mux and Dmx in the GTAXI chip implement the ANSI X3T9.3 8B/10B encoding scheme and make the full chip set compatible with this standard. Alternatively, the Tx and Rx chips can be used separately to implement a data link which uses any proprietary coding scheme which meets the minimum required data transition density.

Telecommunications

The family of telecommunications ICs from Vitesse are designed to address the needs of the newest generation of telecommunications systems incorporating data rates up to 2.5 Gigabits per second. These standard multiplexers and demultiplexers are available in 4, 8 and 12 channel configurations. These products feature very low power dissipation and ECL compatibility. The 8-channel mux/demux products are compatible with the Synchronous Optical Network (SONET) protocol for digital optical transmission. In addition, a 64 x 64 crosspoint chip capable of 200 Mb/s operation is available.

Semicustom Products

Vitesse offers four families of gate arrays. The gate array families include: the FX series, the FURY series, the PLR2KT array, and the HS se-

ries. The FX series offers unparalleled complexity and performance in a channeless array architecture. The FURY series features a balance between speed and power, which offers performance equal to or better than the best ECL bipolar technologies with only a fraction of the power dissipation. Vitesse arrays come in many convenient sizes ranging from 1500 to 350,000 gates. The FX and FURY families offer TTL, ECL or native GaAs signal interface for maximum flexibility. The HS series, made up of two arrays, feature a structured cell approach which combines very high speed source coupled FET logic (SCFL), with very low power direct coupled FET logic (DCFL) for maximum speed/power flexibility. The HS arrays feature ECL I/O interface and can handle data rates up to 2.5GHz.

Foundry Services

Vitesse has paved the way for designers wishing to realize their circuits in Gallium Arsenide by implementing a very simple, silicon-like MOS process. To this, enhancement/depletion (E/D) mode technology adds the flexibility of implementing a variety of logic families. Other important features of the process include: VLSI levels of complexity, self-aligned active devices, 0.6 micron minimum feature size, extended temperature range, resistance to ionizing radiation, and high yields. Vitesse offers an intensive three-day seminar to introduce the designer to digital GaAs IC design.

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VITESSE

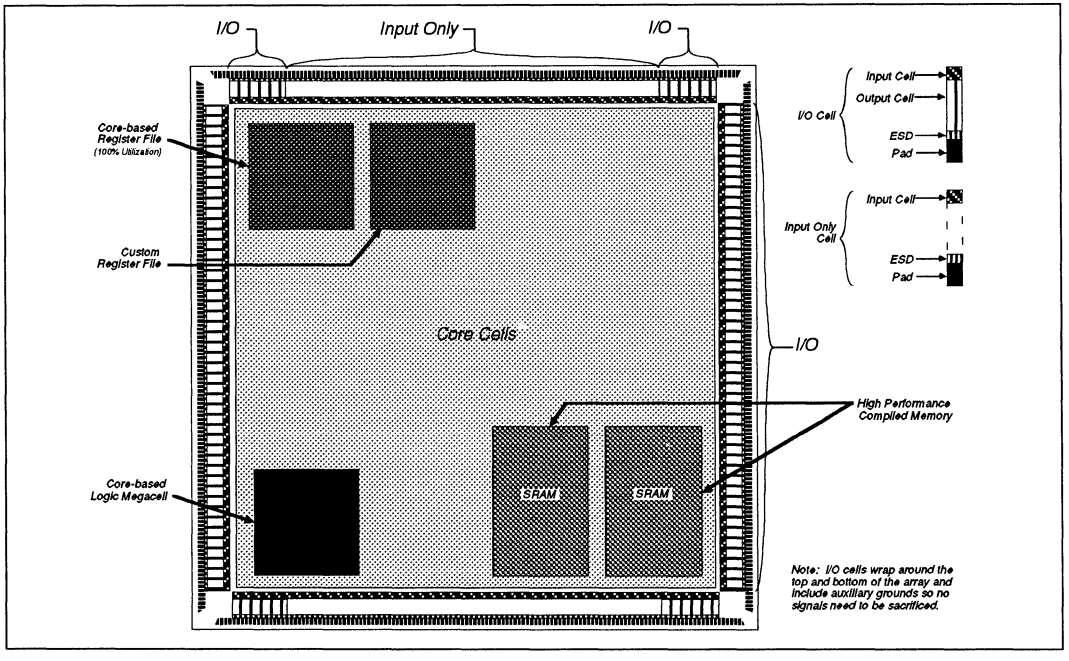
VGFX20K/VGFX40K/VGFX100K/ VGFX200K/VGFX350K

High Performance FX Family Gate Arrays

FEATURES

- Superior performance: High speed and low power dissipation
- Embedded custom functions and megacell options available
- Channelless array architecture and four layer metal for high density
- Custom RAM compiler for design flexibility
- Array performance:
  - Typical gate delay: 115 ps @ 0.20 mW *(Unbuffered 2-input NOR, F.O. = 1, 0.21 mm wire)*
  - Typical gate delay: 130 ps @ 0.7 mW *(Buffered 2-input NOR, F.O. = 3, 0.63 mm wire)*
- ECL, TTL, or mixed ECL/TTL compatible inputs/outputs
- 5 arrays from 20K to 350K gates
- Optional fixed clock distribution scheme for minimized clock skew
- Multiple buffering options for each macro function
- Schematic capture and simulation supported on MENTOR, CADENCE or VALID platforms
- Min/Max simulation supported with LASAR™
- VERILOG-XL™ behavioral modeling and simulation
- Logic synthesis supported with Synopsys Design Compiler™

TYPICAL FX ASIC IMPLEMENTATION



INTRODUCTION

The FX Series offers the integration level of BiCMOS gate arrays with speed performance exceeding that of ECL devices. Implemented using Vitesse's proprietary H-GaAs III process, the FX family of gate arrays is the first to combine ultra high integration with leading edge performance.

The H-GaAs III process represents the third generation of the H-GaAs technology developed by Vitesse to manufacture high yielding, LSI and VLSI digital GaAs circuits. This process features a 0.6 μm self-aligned gate MESFET and four levels of metal interconnect. The basic logic structure for the FX Series is a 2-input NOR gate implemented using direct coupled FET logic (DCFL). Millions of hours of life testing have proven the reliability of the H-GaAs process technology and the DCFL logic structure.

The FX array family incorporates a channelless array architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach avoids the need for pre-defined channels between columns of macros and therefore allows much greater density and flexibility than channelled gate array architectures. Due to an advanced four layer metal process, typical maximum array utilizations can be as high as 50% of the total available gates.

Capable of operating at well over 500 MHz, the FX Series arrays have been designed to provide the best speed - power performance of any gate array technology. The speed of leading edge ECL technology is achieved at a fraction of ECL's power. In addition, because of the frequency independent power consumption of H-GaAs technology, power dissipation levels comparable to, or lower than, similar density BiCMOS arrays can be achieved at frequencies above 50 MHz (see Vitesse Application Note 10, "Power Dissipation: BiCMOS vs. GaAs"). This power savings can add up to substantial cost savings to users in terms of overall cooling requirements.

The FX Family includes support for the creation of custom masterslices. Functions such as SRAMs, multiport register files, and others can be merged with FX arrays resulting in unique architectures and optimum performance.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL and ECL devices directly. The FX array family uses standard power supplies and is supported on the ASIC industry's most popular CAE platforms for schematic capture, behavioral modeling and logic synthesis.

APPLICATIONS

The FX Series of gate arrays can be used in a wide variety of applications including: mainframe computers, workstations and communications equipment. This family of high performance semicustom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

The ultra high integration that the FX arrays offer, combined with their high performance and low power consumption, makes them ideally suited for the implementation of high performance processors and processor support logic. Offering a big performance increase over BiCMOS technology and substantially lower power than ECL technology, the FX Series gate arrays are the perfect choice for systems with clock rates in excess of 50 MHz. Specific computer applications for FX arrays include integer arithmetic processing, floating-point processing, cache control, and bus interface functions.

Communications

Intelligent fiber optic communication links for voice and data transmission can be designed with the FX family. These applications can greatly benefit from the low power dissipation inherent in the FX arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of high-bandwidth tele-

communications standards. The implementation of large switching networks on a single chip is just one example of these applications.

ARCHITECTURE

The FX arrays contain three cell types: internal logic cells, input only cells, and input/output (I/O) cells. All input only and input/output cells contain undedicated logic which is used to incorporate logic functions in the I/O macrocells. There is enough configurable logic in these cells to implement moderately complex functions such as multiplexers and flip flops, allowing the arrays to conform to the JTAG boundary scan standard.

FX arrays can be designed to implement full custom megacells such as SRAM and pre-defined core based megacells such as register files. In addition, a proprietary compiler is available to customers wishing to incorporate custom RAM configurations in their designs. A depiction of a VGFX350K with megacells incorporated is shown on page 1. Table 1 is a summary of the internal cells, I/O and package options for arrays in the FX family.

Clock Distribution

A generic high-drive clock buffer and distribution scheme has been developed for each member of the FX family. This pre-defined clock tree minimizes clock skew to registered functions within the array. The clock tree is capable of driving between 820 and 11,000 flip-flops depending on the size of the array being implemented. Clock skew of less than 400 ps is achievable.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion-mode transistor and two enhancement-mode transistors which can be connected to make a 2-input NOR gate.

Input Only Cells

Input only cells are located predominantly on two edges of the periphery of the array. Input cells are also located in Input/Output cells. I/O macro-

ARRAY SPECIFIC FEATURES

Array Name	# of Internal Gates			# of Input Cells		# of I/O Cells		Max TTL Outputs/ Bidirects (B option)	Total Signal Pins		Package Options	
	Total Raw Gates	Usable Gates[1]	D - Flip Flops[1]	B²,T	E	B²,T	E		B²,T	E	B²,T	E
VGFX20K	20K	10K	1K	14	—	24	—	0	38	—	52 LDCC	—
				40	—	52	—	28	92	—	132 PGA	—
VGFX40K[3]	42K	21K	2.1K	44	—	96	—	96	140	—	184 PGA	—
VGFX100K	100K	50K	5K	74	—	100	—	48	172	—	211 PGA	—
				92	—	100	—	48	192	—	256 LDCC	—
VGFX200K	220K	110K	11K	84	—	172	—	172	256	—	415 PPGA	—
VGFX350K	350K	175K	17.5K	118[3]	128	230[3]	250	230[3]	348[3]	378	557 PPGA	557 PPGA

NOTES: T = TTL Only I/O: +2V, +5V, GND
E = ECL Only I/O: -2V, GND
B = TTL and/or ECL I/O: -2V, +3.3V, GND
(1) Based upon 50% utilization, 10 equivalent gates per flip flop.
(2) The number and placement of TTL I/O for B type arrays are specified in the Vitesse FX Gate Array Design Manual, version 2.0.
(3) Preliminary.

cells can incorporate logic functions by utilizing the 24 logic cells contained in the input cell. Input cells are compatible with TTL and ECL signals. Both signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels for efficient internal operation. These cells also provide ESD input protection.

Each input only cell has resources to form a JTAG-compatible boundary scan flip-flop. This feature allows a user to implement boundary scan without using core cells.

Input/Output (I/O) Cells

Input/Output cells are located on two edges of the periphery of the array. I/O cells can be configured as output drivers, input receivers, or bidirectional transceivers. TTL and ECL signal levels are supported on the same chip. I/O macrocells can incorporate logic functions by utilizing the 48 logic cells contained in the input/output cell. Boundary scan can be easily accommodated since each I/O cell can be configured as a scan flip-flop. When configured as an ECL driver, the output cell can interface with ECL 10KH or 100K receivers while driving a 50Ω load. Two output cells may be paralleled to drive a double-terminated ECL bus (25Ω DC load).

Power Supplies

The FX family uses industry standard power supplies. For an FX array requiring only ECL levels, -2.0V ± 5% is the only power supply required. For FX arrays requiring only TTL levels, 5.0V ± 5% and 2V ± 5% power supplies must be used. If both ECL and TTL levels are required, -2V ± 5% and 3.3V ± 5% are the specified power supplies.

MACRO LIBRARY

The FX Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells). The FX library includes functional equivalents for all FURY™ Series macros as well as optimized megacell functions. The table below is a representative list of the macrocells which are available for the FX arrays. Performance characteristics for selected macros are given on page 5. For a complete set of specifications, refer to the FX Design Manual.

FX FAMILY MACRO LIBRARY

Name	Description	Name	Description
Input/Output Macros			
BIE	Bidirectional ECL input/output buffer	BITOCK	Bidirectional TTL input/output buffer with open drain (+5.0V/+2.0V)
BIE25NR2	Bidirectional ECL input/25 Ω output buffer with 2-input NOR gate	IE1F	Inverting ECL input buffer
BIE25NR3	Bidirectional ECL input/25 Ω output buffer with 3-input NOR gate	IE1T	ECL input buffer (1x drive)
BIEJ	Bidirectional ECL input/output buffer with boundary scan register	IE2T	ECL input buffer (2x drive)
BIENR2	Bidirectional ECL input/output buffer with 2-input NOR gate	IEDIFF	Differential ECL Input (1x drive)
BIER	Bidirectional ECL input/output buffer with 3-input MUXed register	IEDIF2	Differential ECL Input (2x drive)
BIT	Bidirectional TTL input/output buffer (+3.3V/-2.0V)	IEJ1T	Non-inverting ECL input buffer with boundary scan register
BITK	Bidirectional TTL input/output buffer (+5.0V/+2.0V)	IER1T	Non-inverting ECL input buffer with 3-input MUXed register
BIT2K	Bidirectional TTL input/output buffer (+5.0V/+2.0V) (2x drive)	IT1T	TTL input buffer (1x drive) (+3.3V/-2.0V)
BITOC	Bidirectional TTL input/output buffer with open drain (+3.3V/-2.0V)	IT1TK	TTL input buffer (1x drive) (+5.0V/+2.0V)
		OE	ECL output buffer
		OE25	ECL 25Ω cut-off output driver
		OEJ	non-inverting ECL output buffer with boundary scan register
		OEMDF	ECL output buffer with scan register

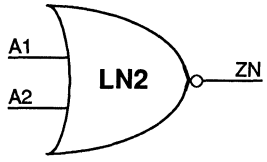
FX FAMILY MACRO LIBRARY (con't)

Name	Description
Input/Output Macros *(con't)*	
OENOR3	ECL output buffer with 3-input NOR
OER	Non-inverting ECL output buffer with 3-input muxed register
OESD	Single-ended ECL output buffer
OT	Non-inverting TTL output buffer with tri-state enable (+3.3V/-2.0V)
OTK	Non-inverting TTL output buffer with tri-state enable (+5.0V/+2.0V)
OT2K	Non-inverting TTL output buffer with tri-state enable (2x drive)
Adders	
LA1	Half adder
LA1U	Half adder (unbuffered)
LA2	Full adder (1x drive)
LA2B	Full adder (2x drive)
LA2U	Full adder (unbuffered)
LADD4	4-bit adder with inverted carry-out, block propagate, and block generate
Buffers	
CLK1	Clock buffer
LB3S	Inverter (unbuffered)
LDR1	Line driver/Inverting clock buffer (1x drive)
LDR3	Line driver/Inverting clock buffer (3x drive)
D Flip-Flops	
LFP1	Positive edge triggered D flip-flop (1x drive)
LFP1B	Positive edge triggered D flip-flop (2x drive)
LFP1U	Positive edge triggered D flip-flop (unbuffered)
LFP3	Positive edge triggered D F/F with asynchronous set & clear
LFP3U	Positive edge triggered D flip-flop with asynchronous set & clear (unbuffered)
LFP4	Positive edge triggered D F/F with 3-input OR and an asynchronous active high set
LFP5	Positive edge triggered D F/F with 4-input OR
LFP4	Positive edge triggered D flip-flop with 3-input OR and asynchronous set
LFP5	Positive edge triggered D flip-flop with 4-input OR
LSP1	Positive edge triggered D flip-flop with 2:1 mux input
LSP1U	Positive edge triggered D flip-flop with 2:1 mux input (unbuffered)
LSP2	Positive edge triggered scan register (1x drive)
LSP2B	Positive edge triggered scan register (2x drive)
LSP2U	Positive edge triggered scan register (unbuffered)
Latches	
LLP1	High transparent D latch
LLP1U	High transparent D latch (unbuffered)
LLP2	High transparent D latch with 2-input OR
LLP3	Muxed positive transparent D latch
Gates	
LAND	2-input AND
LANDU	2-input AND (unbuffered)
LN2	2-input NOR
LN2B	2-input NOR with 2x buffer
LN2US	2-input NOR (unbuffered)
LN3	3-input NOR
LN3U	3-input NOR (unbuffered)
LN4	4-input NOR (1x drive)
LN4B	4-input NOR (2x drive)
LN4U	4-input NOR (unbuffered)
LN6	6-input NOR gate
LN6U	6-input NOR gate (unbuffered)
LN9	9-input NOR (1x drive)
LN9B	9-input NOR (2x drive)
LN9U	9-input NOR (unbuffered)
LNA2	2-input NAND
LNA2U	2-input NAND (unbuffered)
LNA4	4-input NAND
LNA4U	4-input NAND (unbuffered)
LO2	2-input OR (1x drive)
LO2B	2-input OR (2x drive)
LO2U	2-input OR (unbuffered)
LO4	4-input OR (1x drive)
LO4B	4-input OR (2x drive)
LO4U	4-input OR (unbuffered)
LX1	2-input exclusive OR
LX1U	2-input exclusive OR (unbuffered)
LX2	2-input exclusive NOR
LX2U	2-input exclusive NOR (unbuffered)
OA4321	OR-AND gate
OA4321U	OR-AND gate (unbuffered)
Multiplexers	
LM1	2:1 multiplexer
LM1U	2:1 multiplexer (unbuffered)
LM3	4:1 multiplexer
LM3U	4:1 multiplexer (unbuffered)
Miscellaneous	
CNT1	Positive edge triggered 1-bit counter (toggle flip-flop)
LCAR4	4-bit cary-lookahead generator with inverted block propagation and block generate
LJP1	Implements JTAG boundary scan functionality in core logic
LOAD	1x diode load to V_{TT}
PD	Pull-down

SELECTED MACROCELL AC PERFORMANCE (Commercial arrays)

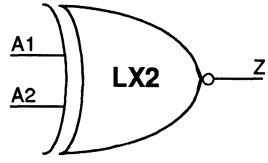
(V_{TT} = -2.0V, V_{CC} = V_{CCA} = GND, T_C = 25° C, Load: F.O. = Ø; Ø mm wire.)

LN2: Buffered 2-input NOR



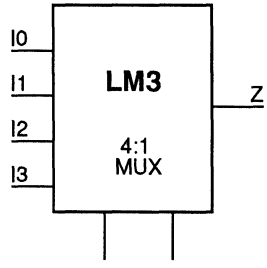
Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	50	—	81	ps
	Falling Signal	42	—	52	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	9	ps
	Falling Signal	5	—	6	ps
Delay/mm wire	*Rising Signal*	90	—	147	ps
	Falling Signal	67	—	84	ps
Power Dissipation		—	0.58	0.87	mW

LX2: 2-input XNOR



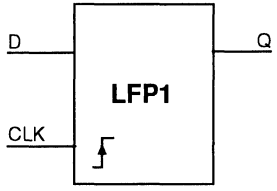
Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	112	—	343	ps
	Falling Signal	191	—	323	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	9	ps
	Falling Signal	6	—	8	ps
Delay/mm wire	*Rising Signal*	90	—	147	ps
	Falling Signal	85	—	106	ps
Power Dissipation		—	1.12	1.68	mW

LM3: 4:1 Multiplexer



Parameter		Min	Typ	Max	Units
Propagation Delay					
S0, S1 to Z	*Rising Signal*	130	—	364	ps
	Falling Signal	224	—	354	ps
I0 - I3 to Z	*Rising Signal*	130	—	212	ps
	Falling Signal	224	—	281	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	6	—	10	ps
	Falling Signal	6	—	8	ps
Delay/mm wire	*Rising Signal*	103	—	167	ps
	Falling Signal	85	—	106	ps
Power Dissipation		—	1.67	2.5	mW

SELECTED MACROCELL AC PERFORMANCE (con't)



LFP1: Positive Edge Triggered D Flip-Flop	Parameter		Min	Typ	Max	Units
	Propagation Delay					
	CLK to Q	*Rising Signal*	111	—	182	ps
		Falling Signal	241	—	302	ps
	t_{SET-UP}		62	—	104	ps
	t_{HOLD}		43	—	73	ps
	Load Dependent Delay					
	Delay/Fan-out	*Rising Signal*	5	—	9	ps
		Falling Signal	6	—	7	ps
	Delay/mm wire	*Rising Signal*	90	—	147	ps
		Falling Signal	81	—	102	ps
	Power Dissipation		—	2.03	3.05	mW

ABSOLUTE MAXIMUM RATINGS FOR ECL ONLY (-2V) AND MIXED ECL/TTL (-2V, +3.3V) POWER SUPPLY LEVELS (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -2.2 V to +0.5 V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... -0.5 V to +4.3 V
ECL Input Voltage Applied, ($V_{IN\ ECL}$) ..... +0.5 V to V_{TT}
TTL Input Voltage Applied, ($V_{IN\ TTL}$) ..... -0.5 V to V_{TTL} + 1.0 V
ECL or TTL Output Current, I_{OUT} ..... 50 mA
Case Temperature Under Bias, (T_C)(2). ..... -55° to +125°C
Storage Temperature, (T_{STG})(2) ..... -65°C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

RECOMMENDED OPERATING CONDITIONS FOR ECL ONLY (-2V) AND MIXED ECL/TTL (-2V, +3.3V) POWER SUPPLY LEVELS

ECL Supply Voltage, (V_{TT}) ..... -2.0 V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +3.3 V ± 5%
Commercial Operating Temperature Range, (T)(1). ..... 0° to 70°C
Industrial Operating Temperature Range, (T)(1). ..... -40° to 85°C

NOTES: (1) Lower limit is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS FOR -2V AND +3.3V POWER SUPPLY LEVELS

TTL Inputs/Outputs *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	—	0.4	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL}+1.0	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.4 V
I_{OZH}	3-state output OFF current HIGH	—	—	200	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.4 V
I_{OCZ}	Open collector output leakage current	—	—	200	µA	V_{OUT} = 2.4 V

NOTE: 1) Differential ECL output pins must be terminated identically.

ECL Inputs/Outputs *(Over recommended commercial operating conditions with internal V_{REF}, V_{CC} = V_{CCA} = GND, Output load 50Ω to -2.0 V)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IN} = V_{IH} (max)
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} (min)

ABSOLUTE MAXIMUM RATINGS FOR TTL ONLY (+2V, +5V) POWER SUPPLY LEVELS (1)

Power Supply Voltage, (V_{MM}) potential to GND ..... -0.5V to +2.5V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... -0.5V to +5.5V
TTL Input Voltage Applied, ($V_{IN\,TTL}$) ..... -0.5V to V_{TTL} + 1.0V
TTL Output Current, I_{OUT} (DC, output HI) ..... 50 mA
Case Temperature Under Bias, (T_C)(2). ..... -55°C to +125°C
Storage Temperature, (T_{STG})(2) ..... -65°C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

RECOMMENDED OPERATING CONDITIONS FOR TTL ONLY (+2V, +5V) POWER SUPPLY LEVELS

Supply Voltage, (V_{MM}) ..... +2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +5.0V ± 5%
Commercial Operating Temperature Range, (T)(1). ..... 0° to 70°C
Industrial Operating Temperature Range, (T)(1). ..... -40° to 85°C

NOTE: (1) Lower limit is ambient temperature and upper limit is case temperature.

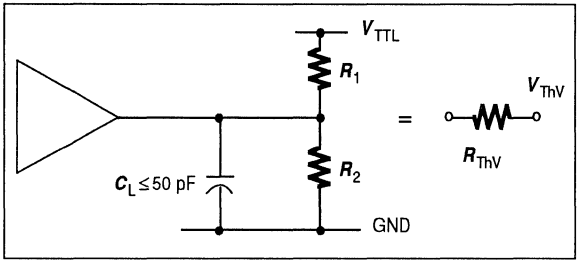
DC CHARACTERISTICS FOR TTL ONLY (+2V, +5V) POWER SUPPLY LEVELS

TTL INPUTS/OUTPUTS *(Over recommended commercial operating conditions, TTLGND = GND)*

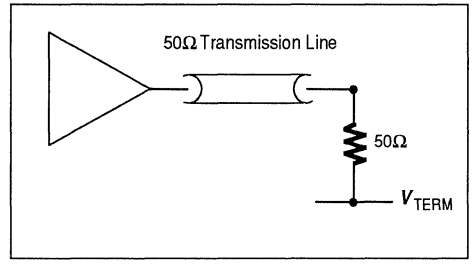
Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL} + 1.0	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	200	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-200	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	200	µA	V_{OUT} = 2.4 V

EQUIVALENT CIRCUITS FOR OUTPUT LOADS

TTL



ECL



Power Levels	R_1	R_2	R_{ThV}	V_{ThV}
+2, +5	467	301	183	1.96V
-2, +3.3	252	189	108	2.14V

OPTION DEVELOPMENT PROCEDURE

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by Vitesse design and implementation engineers:

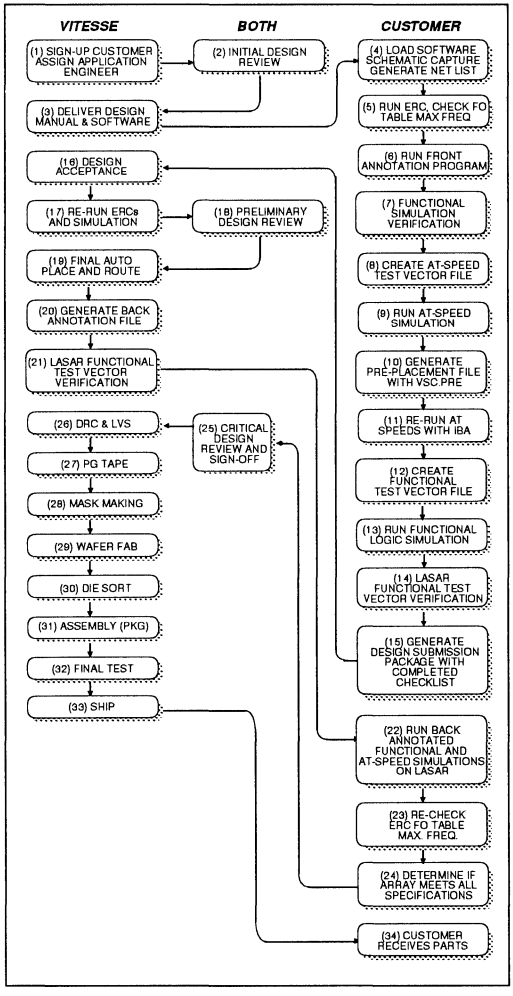
- Masterslice design
- Custom megacell design
- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule checking and layout vs schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart at right summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse.

CAD TOOLS/SUPPORT

FX designs are supported on MENTOR, VALID, SYNOPSYS, and VERILOG platforms. LASAR simulation software is used to verify the AC performance of the design by taking into account on-chip timing variations. Simulation libraries for VERILOG XL™ are also supported. The Vitesse Design Kit includes documentation and software which allow the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. To facilitate floorplanning and block pre-placement, Vitesse has an interactive graphical placement program that the customer may choose to use for their design. This program is supported in the X Windows™ environment. Cadence placement and routing tools are used for physical implementation.

GATE ARRAY DESIGN FLOW



TRAINING

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

1

VITESSE

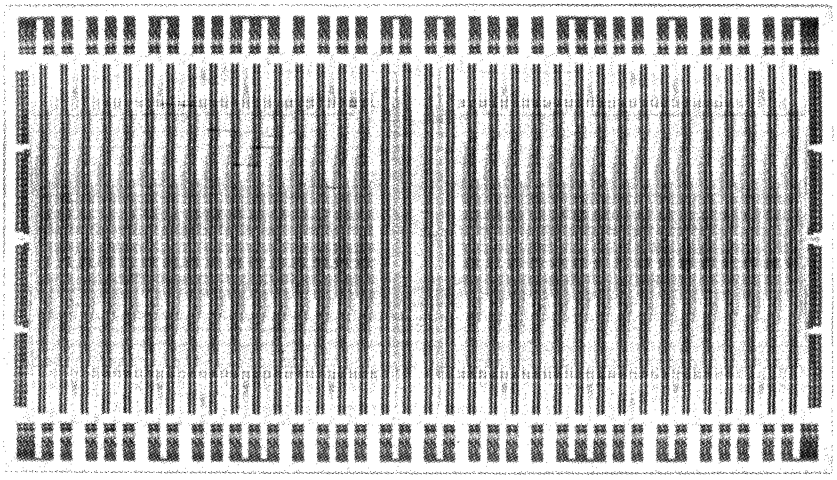
VSC3K/VSC5K/VSC10K/VSC15K/ VSC20K8R/VSC30K

High Performance FURY Series Gate Arrays

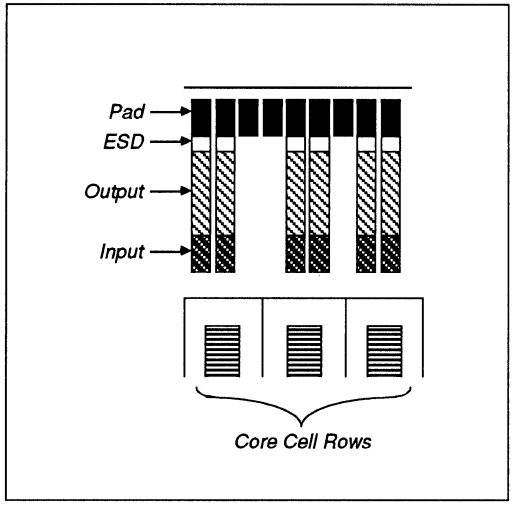
FEATURES

- Superior performance: High speed/low power
- High density channelled architecture (up to 100% utilization)
- Proven 0.8µ H-GaAs E/D MESFET process
- Array performance
  - D flip-flop toggle rates: >1 GHz
  - Typical gate delay: 177 ps @ 1.1 mW *(2-input NOR, F.O. = 3, 1.5 mm wire)*
  - ECL inputs/outputs at 650 MHz
  - TTL inputs/outputs at 100 MHz
  - Typical speed-power product: ~0.025 pJ *(2-input NOR)*
- SRAM performance
  - Cycle time: 3.5 ns (min)
  - Clock to Q: 1.5 ns (max)
  - Power dissipation: 0.55 W (Typical per 1K cell)
  - Normal and scan mode
  - Dedicated test circuitry
- ECL or TTL compatible inputs/outputs
- Choice of sizes: from VSC3K *(3,584 2-Input NOR gates)*, to VSC30K *(30,528 2-Input NOR gates)*
- Choice of buffered or unbuffered gates
- Three temperature ranges
  - Commercial: 0° to +70° C
  - Industrial: -40° to +85° C
  - Military: -55° to +125° C
- Multiple buffering options for macrocells
- Embedded SRAM and megacells available
- Mil-Std-883C, Level B screening and qualification available
- Schematic capture/simulation supported on MENTOR, CADENCE or VALID platforms
- Min/Max simulation supported with LASAR™
- VERILOG-XL™ behavioral modeling and simulation
- Logic synthesis supported with Synopsis Design Compiler™

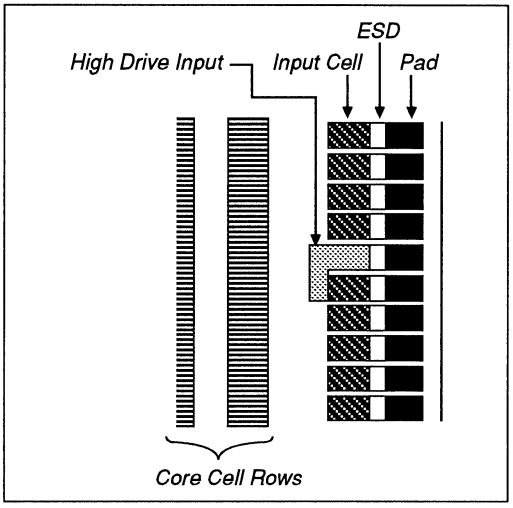
PHOTOMICROGRAPH OF THE FURY 30K ARRAY



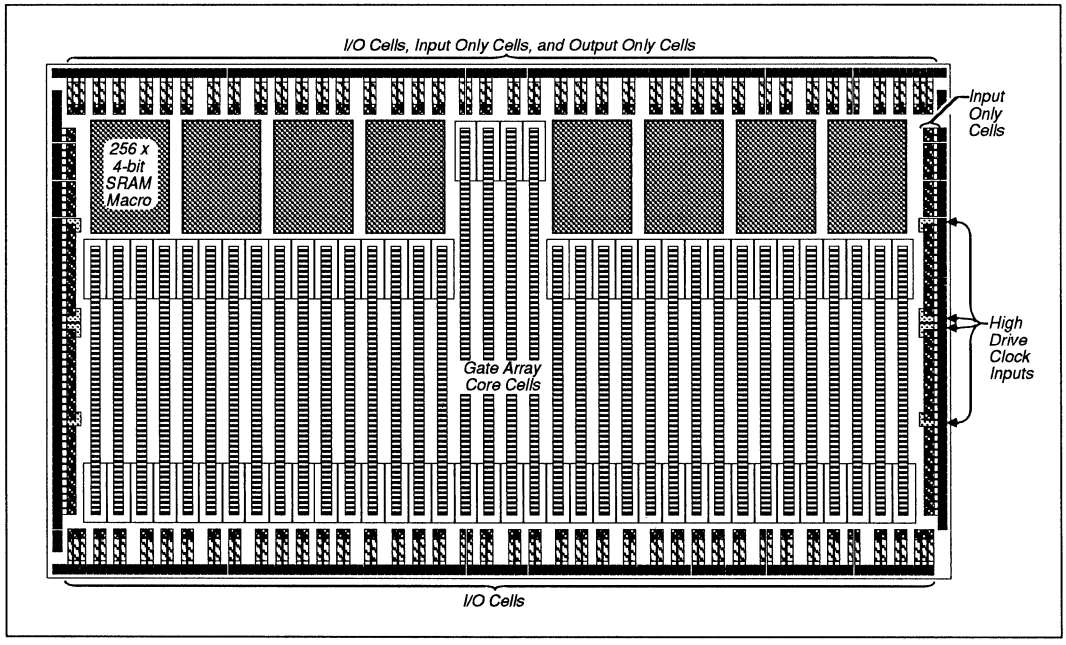
FURY I/O CELL DETAIL



FURY INPUT CELL DETAIL



ARCHITECTURE - THE VSC20K8R



INTRODUCTION

The VSC3K, VSC5K, VSC10K, VSC15K, VSC20K8R, and VSC30K are members of the FURY Series of high performance gate arrays. They are ideally suited for systems which require high density, state-of-the-art performance while maintaining low power dissipation. Vitesse uses a proprietary high yielding 0.8µ GaAs MESFET process to build the FURY Series gate arrays. These arrays interface with TTL and ECL technologies without adding any additional system requirements. The FURY family offers speed performance equal to or better than leading edge ECL gate arrays, while dissipating only 1/3 to 1/4 of the power. This can add up to substantial cost savings to users in terms of overall cooling requirements.

Input cells and output cells can be configured to contain a positive edge triggered D flip-flop and can support boundary scan designs. The combination of internal logic and I/O cells in the FURY Series provide the user with complexities ranging from 3,500 to over 30,000 equivalent gates.

APPLICATIONS

The FURY Series of gate arrays can be used in a wide variety of applications including computers, communications, test, and general instrumentation. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

Existing mainframe systems utilizing ECL or TTL technologies can improve speed and reduce power dissipation with the FURY arrays. Superminis using ECL arrays can increase system performance while reducing overall cooling requirements. Workstations using standard microprocessors can bring supercomputing power to their system by using the FURY arrays.

Communications

Fiber optic communication links for voice and data transmission can be designed with the

FURY ARRAY FEATURES

Array Name	# of Internal Gates			# of Input Cells		# of I/O Cells	# of Output Only Cells	Total Signal Pins	Package Options
	Total Raw Gates	Usable Gates	D - Flip Flops	TTL, ECL	Hi-Drive	TTL, ECL			
VSC3K	3,584	3,584	290	40	4	52	—	92	132 LDCC
VSC5K	6,400	6,400	520	52	4	68	—	120	149 PGA, 164 LDCC
VSC10K	13,376	13,376	1,100	74	8	100	—	174	211 PGA
				96	8	100	—	196	256 LDCC
VSC15K	16,896	16,896	1,408	74	8	100	—	174	211 PGA
				96	8	100	—	196	256 LDCC
VSC20K8R	20,736	20,736	1,728	74	8	132	19	256	344 LDCC
VSC30K	30,528	30,528	2,544	128	8	156	—	256	344 LDCC

FURY family. These applications can greatly benefit from the low power dissipation inherent in the FURY arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of telecommunications standards.

Architecture

The FURY arrays all contain four basic cell types: internal logic cells, input only cells, input/output (I/O) cells, and clock receivers. The VSC20K8R contains two additional cell types: the output only cell and the 256 x 4 bit SRAM macrocell. A photomicrograph of the VSC30K is shown on page 1-13 and the architecture of the VSC20K8R is shown on page 1-14. The table on page 1-15 is a summary of the internal cells, I/O, and package options for the FURY Series of gate arrays.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion transistor and two enhancement transistors which can be connected to make a 2-input NOR gate.

Input Cells

Input only cells are located on two sides of the periphery of the array. Input cells are also located in input/output cells. Input cells can be personalized as latches, flip-flops, or buffers and are compatible with TTL or ECL signals. All three signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels. These cells also provide ESD input protection.

Clock Receivers

A number of input cells in each array are configured as high-drive receivers intended for use as clock buffers. These special input cells can support up to 6x the drive capability of a standard input cell.

Input/Output (I/O) Cells

Input/output cells are located on two sides of the periphery of the array. I/O cells contain both input and output cells and can be configured as outputs, bidirectionals or inputs. I/O cells are compatible with TTL or ECL signals.

Output Cells

Output cells are located only in I/O cells. These cells can be configured as latches, flip-flops, 2- or 3-input ORs or NORs, or as inverting or non-inverting output buffers compatible with TTL or ECL signal levels. The output cells are capable of providing ECL 10K, 10KH, or 100K levels across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive.

SRAM Cells *(VSC20K8R only)*

8K bits of SRAM cells are embedded in the VSC20K8R for combined logic and RAM applications. The SRAM is organized into 8 blocks 256x4. The SRAM supports dedicated circuitry and a scan mode.

Output Only Cells *(VSC20K8R only)*

Output Only cells are located along the top of the array. These cells can be configured as latches, flip-flops, 2- or 3-input ORs or NORs, or as inverting or non-inverting output buffers compatible with TTL or ECL signal levels. The output cells are capable of providing ECL 10K, or 100K levels across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive.

MACRO LIBRARY

The FURY Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells). These macrocells define the optimized interconnection pattern of transistors in one or more cells which have been utilized to perform a logic function. The following page contains a representative list of macrocells which are available for FURY arrays.

Performance characteristics for selected macros are given on page 1-18. For complete specifications, refer to the FURY Series Gate Array Design Manual.

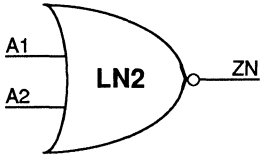
FURY MACROCELL LIBRARY

Name	Description
Input/Output Macros	
BIE	Bidirectional ECL Input/Output Buffer
BIE25NR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive
BIE25NR3	Bi-Directional ECL Input/25Ω Output Buffer with 3-input NOR Gate, 2x Drive
BIENR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive
BIT	Bidirectional TTL Input/Output Buffer
BITOC	Bidirectional TTL Input/Output - Open Drain
IE1F	Inverting ECL Input Buffer, 1x Drive
IE1T	ECL Input Buffer, 1x Drive
IE2T	ECL Input Buffer, 2x Drive
IECK3	ECL Input Buffer, 3x Drive
IEDIF2	Differential ECL Input, 2x Drive
IEDIF3	Differential ECL Input, 3x Drive
IEDIFF	Differential ECL Input, 1x Drive
IT1T	TTL Input Buffer
LB1UG	GaAs Input Buffer, 1x Drive
LB3UG	Inverting GaAs Input Buffer, 1x Drive
OE	ECL Output Buffer
OE25	ECL 25Ω Cut-off Output Buffer
OEMDF	ECL Output Buffer With Scan Register, 0.5x Drive
OENOR3	ECL Output Buffer With 3-input NOR
OESD	Differential ECL Output with Single-Ended Input
OT	TTL Output Buffer
Buffers	
CLK1	Clock Buffer
CLK1G	Clock Buffer with GaAs Input
LB3	Dual Inverter, 1x Drive
LDR1	Line Driver/Inverting Clock Buffer, 1x Drive
LDR3	Line Driver/Inverting Clock Buffer, 3x Drive
Flip-Flops	
CNT1	Toggle D Flip-flop
LFP1	Positive Edge Triggered D Flip-flop, 2x Drive
LFP1B	Positive Edge Triggered D Flip-flop, 3x Drive
LFP1U	Positive Edge Triggered D Flip-flop, 1x Drive
LFP3	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 2x Drive
LFP3U	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 1x Drive
LFP4	Positive Edge Triggered D Flip-flop with 3-Input OR and Asynchronous Set
LFP5	Positive Edge Triggered D Flip-flop with 4-Input OR
Flip-Flops (con't)	
LSP1	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 2x Drive
LSP1U	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 1x Drive
Logic Gates	
LA1	Half-adder, 1x Drive
LA1U	Half-adder, 2x Drive
LA2	Full-adder, 2x Drive
LA2B	Full-adder, 3x Drive
LA2U	Full-adder, 1x Drive
LAND	2-Input AND, 2x Drive
LANDU	2-Input AND, 1x Drive
LLP1	High Transparent D Latch, 2x Drive
LLP1U	High Transparent D Latch, 1x Drive
LLP2	High Transparent D Latch with 2-Input OR
LLP3	Multiplexed Positive Transparent D Latch
LM1	2:1 Multiplexer, 2x Drive
LM1U	2:1 Multiplexer, 1x Drive
LM3	4:1 Multiplexer, 2x Drive
LM3U	4:1 Multiplexer, 1x Drive
LN2	2-Input NOR, 2x Drive
LN2B	2-Input NOR, 3x Drive
LN2U	Dual 2-Input NOR, 1x Drive
LN3	3-Input NOR, 1x Drive
LN4	4-Input NOR, 2x Drive
LN4B	4-Input NOR, 3x Drive
LN4U	4-Input NOR, 1x Drive
LN9	9-Input NOR, 2x Drive
LN9B	9-Input NOR, 3x Drive
LN9U	9-Input NOR, 1x Drive
LNA2	2-Input NAND, 2x Drive
LNA2U	2-Input NAND, 1x Drive
LO2	2-Input OR, 1x Drive
LO2B	2-Input OR, 2x Drive
LO2U	2-Input OR, 0.5x Drive
LO4	4-Input OR, 2x Drive
LO4B	4-Input OR, 3x Drive
LO4U	4-Input OR, 1x Drive
LX1	2-Input Exclusive OR, 2x Drive
LX1U	2-Input Exclusive OR, 1x Drive
LX2	2-Input Exclusive NOR. 2x Drive
LX2U	2-Input Exclusive NOR, 1x Drive
R256X4	256 x 4 Bit SRAM
Miscellaneous	
PD	Pull Down

SELECTED MACROCELL AC PERFORMANCE (Commercial arrays)

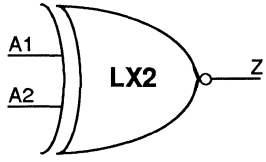
(V_{TT} = -2.0V, V_{TTL} = +5.0V, V_{CC} = V_{CCA} = GND, T_C = 25° C, Load: F.O. = Ø; Ø mm wire.)

LN2: Buffered 2-input NOR



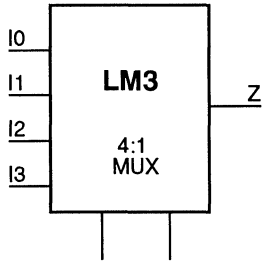
Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	68	—	111	ps
	Falling Signal	58	—	73	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	8	—	10	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	31	—	38	ps
Power Dissipation		—	1.1	1.8	mW

LX2: 2-input XNOR



Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	279	—	455	ps
	Falling Signal	349	—	437	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	11	—	12	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	40	—	49	ps
Power Dissipation		—	2.2	3.4	mW

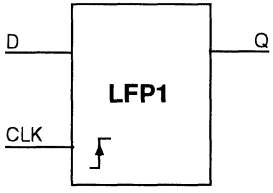
LM3: 4:1 Multiplexer



Parameter		Min	Typ	Max	Units
Propagation Delay					
S0, S1 to Z	*Rising Signal*	298	—	485	ps
	Falling Signal	382	—	478	ps
I0 - I3 to Z	*Rising Signal*	174	—	283	ps
	Falling Signal	307	—	385	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	10	—	15	ps
	Falling Signal	11	—	12	ps
Delay/mm wire	*Rising Signal*	59	—	96	ps
	Falling Signal	40	—	49	ps
Power Dissipation		—	3.1	5.1	mW

SELECTED MACROCELL AC PERFORMANCE (con't)

LFP1: Positive Edge Triggered D Flip-Flop



Parameter		Min	Typ	Max	Units
Propagation Delay					
CLK to Q	*Rising Signal*	155	—	253	ps
	Falling Signal	349	—	437	ps
t_{SET-UP}		—	—	146	ps
t_{HOLD}		—	—	104	ps
Toggle frequency		874	—	—	MHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	10	—	12	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	38	—	47	ps
Power Dissipation		—	3.9	6.2	mW

DC CHARACTERISTICS

TTL Inputs/Outputs

(Over recommended operating conditions, TTLGND = GND)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	V_{CC}	—	0.5	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	—	—	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	—	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

DC CHARACTERISTICS (con't)

ECL Inputs/Outputs

(Over recommended operating conditions with internal V_{REF}: $V_{CC} = V_{CCA} = GND$, Output load 50Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note:1) Differential ECL output pins must be terminated identically.

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (ECL), (V_{TT}) ..... -2.5V to +0.5V
Power Supply Voltage (TTL) (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), (V_{TTLIN}) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HI) ..... 50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage (1), (V_{TT}) ..... -2.1V to -1.9V
TTL Power Supply Voltage, (V_{TTL}) ..... +4.75V to +5.25V
Operating Temperature (2), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTES: 1) When using internal ECL 100K reference level.
2) Lower limit of specification is ambient temperature and upper limit is case temperature.

OPTION DEVELOPMENT PROCEDURE

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by Vitesse design and implementation engineers:

- Final placement and routing of the design
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- Design rule checking and layout vs schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart at right summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse.

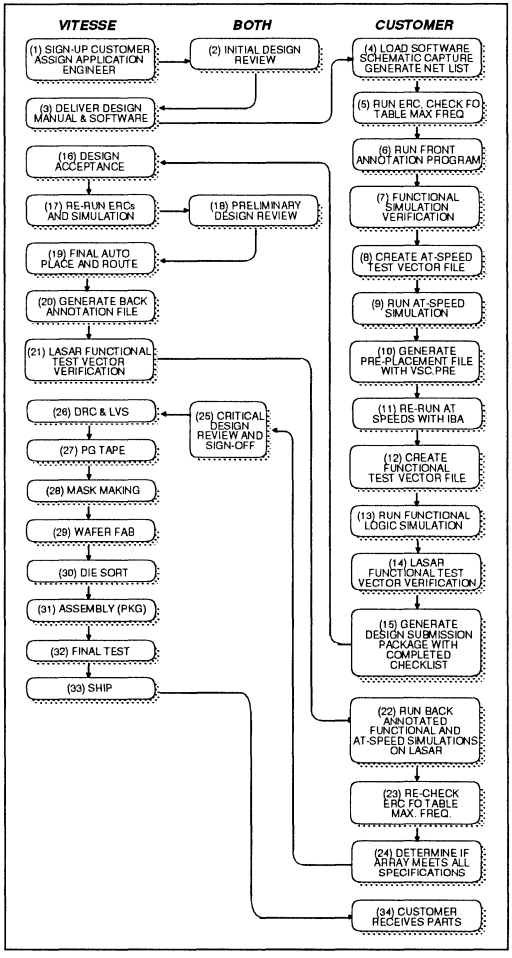
CAD TOOLS/SUPPORT

FURY designs are supported on MENTOR, VALID, SYNOPSYS, and VERILOG platforms. LASAR simulation software is used to verify the AC performance of the design by taking into account on-chip timing variations. Simulation libraries for VERILOG XL™ are also supported. The Vitesse Design Kit includes documentation and software which allow the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. To facilitate floorplanning and block pre-placement, Vitesse has an interactive graphical placement program that the customer may choose to use for their design. This program is supported in the X Windows™ environment. MERLYN-G placement and routing tools are used for physical implementation.

TRAINING

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

GATE ARRAY DESIGN FLOW



FEATURES

- Superior performance: high speed/low power
- Array performance:
  - D flip-flop toggle rates: >1 GHz
  - Typical gate delay: 177 ps @ 1.1 mW *(2-Input NOR, F.O. = 3, 1.5 mm wire)*
  - TTL/CMOS inputs/outputs to support up to 150 MHz state machine design
  - Typical speed-power product: ~0.025 pJ
- 2400 2-input NOR internal gates, 92 signal I/O (Up to 52 outputs or 92 inputs)
- Choice of buffered or unbuffered gates
- Direct PLD source file conversion using the SYNOPSYS Design Compiler™
- Schematic capture/simulation supported on MENTOR, CADENCE or VALID platforms
- Fault and Min/Max simulation supported with LASAR™
- VERILOG-XL™ behavioral modeling and simulation
- Compatible with +5 V only TTL systems (see application note on page 1-26)
- Typical power dissipation: 1.5 W
- Low Cost 132-pin Metal Quad flatpack (MQUAD)

INTRODUCTION

TTL signal interface, low power, and 150 MHz performance at very low cost makes the PLR2KT the perfect replacement for multiple programmable logic devices (PLDs) in high speed workstations and PCs. A proprietary high yielding, low power, 0.8μ GaAs MESFET process is used to build the PLR2KT gate array. This product has 2400 usable gates and the I/Os are TTL and CMOS compatible. The PLR2KT can replace 6 to 10 or more PLDs, depending on the application, and offers better performance than today's fastest TTL devices. The resulting reduction in part count can lead to a dramatic savings in power dissipation. The PLR2KT is the ideal replacement for TTL programmable logic devices.

APPLICATIONS

This array is designed to replace high speed TTL programmable logic devices or glue logic in a wide variety of applications in computers, workstations, communications and instrumentation. With 2400 usable gates, the PLR2KT offers outstanding utility for high performance TTL systems including such functions as peripheral control, communications, and data processing.

The PLR2KT is the ideal interface chip for high speed systems using state-of-the-art 32-bit RISC or CISC microprocessor architectures. Because of its outstanding flip-flop performance, fast state machines and counters can easily be realized in the PLR2KT. Also, functions such as cache memory control and bus arbitration can be implemented with minimum delay in this highly integrated, low cost solution.

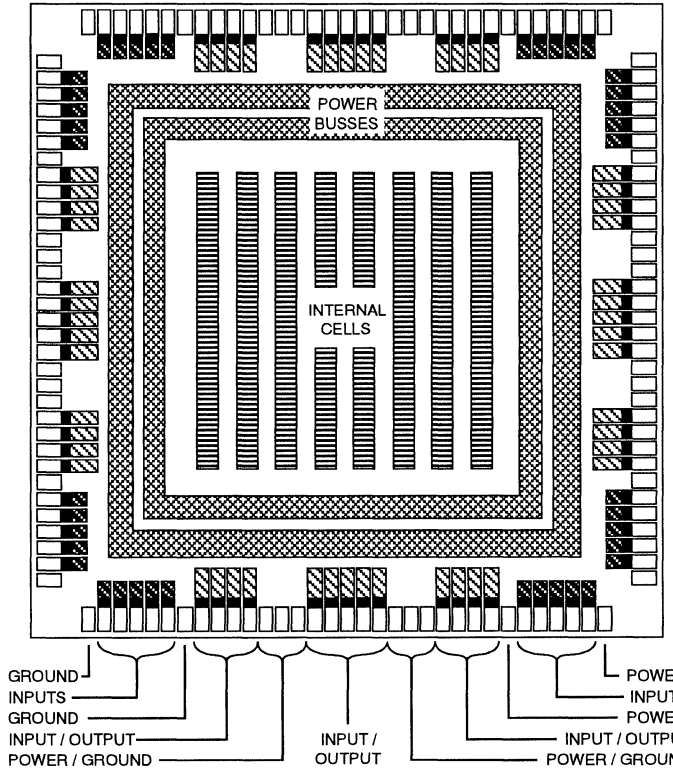
ARCHITECTURE

The PLR2KT array contains three cell types: internal logic cells, input only cells and input/output cells. The PLR2KT layout is shown on page 1-24.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion transistor and two enhancement transistors which can be connected to make a 2-input NOR gate.

PLR2KT ARRAY ARCHITECTURE



Input-Only Cells

Input-only cells are located on all four sides of the periphery of the array. Input-only cells can be configured to switch at either TTL or CMOS thresholds. All input cells contain ESD input protection.

Input/Output (I/O) Cells

Input/output cells are also located on all four sides of the periphery of the array. Each I/O cell contains a replica of an input-only cell as well as an output cell. Input/output cells can be configured as outputs, bidirectionals or inputs. Outputs are TTL compatible only.

MACRO LIBRARY

The PLR2KT Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells) available for the PLR2KT. These macrocells define the optimized interconnection pattern of transistors in one or more cells which have been utilized to perform a logic function. The following is a representative list of the internal macrocells which are available for the PLR2KT gate array. Performance characteristics for selected macros are given on page 1-27. For a complete set of macro specifications, refer to the PLR2KT Design Manual.

PLR2KT MACROCELL LIBRARY

Name	Description
Input/Output Macros	
BITK	Bidirectional TTL I/O, 1x drive
BITLK	Low Power Bidirectional TTL I/O, 1x drive
IC1TK	CMOS input buffer, 3x drive
IT1FK	Inverting TTL Input buffer, 1x drive
IT1TK	TTL Input buffer, 1x drive
ITK	TTL input buffer with true & complement outputs, 1x drive
OTK	TTL output
OTLK	Low power TTL output
Adders	
LA1	Half adder
LA1U	Half adder, unbuffered
LA2	Full adder
LA2B	Full adder with 2x buffer
LA2U	Full adder, unbuffered
Buffers	
CLK1	Clock buffer
LB3	Dual inverter, unbuffered
LDR1	Line driver/Inverting clock buffer, 1x drive
LDR3	Line driver/Inverting clock buffer, 3x drive
Flip-Flops	
LFP1	Positive edge triggered D flip-flop
LFP1B	Positive edge triggered D flip-flop with 2x buffer
LFP1U	Positive edge triggered D flip-flop, unbuffered
Logic Gates	
LAND	2-input AND
LANDU	2-input AND, unbuffered
LN2	2-input NOR
LN2B	2-input NOR with 2x buffer
LN2U	Dual 2-input NOR, unbuffered

Name	Description
Logic Gates	
LN4	4-input NOR
LN4B	4-input NOR, 2x drive
LN4U	4-input NOR, unbuffered
LN9	9-input NOR
LN9B	9-input NOR with 2x buffer
LN9U	9-input NOR, unbuffered
LNA2	2-input NAND
LNA2U	2-input NAND, unbuffered
LO2	2-input OR
LO2B	2-input OR, 2x drive
LO2U	2-input OR, 0.5x drive
LO4	4-input OR
LO4B	4-input OR with 2x buffer
LO4U	4-input OR, unbuffered
LX1	2-input exclusive OR
LX1U	2-input exclusive OR, unbuffered
LX2	2-input exclusive NOR
LX2U	2-input exclusive NOR, unbuffered
Latches	
LLP1	Positive transparent D latch
LLP1U	Positive transparent D latch, unbuffered
LLP2	Positive transparent D latch with 2-input OR
LLP3	Muxed positive transparent D latch
Multiplexers	
LM1	2:1 multiplexer
LM1U	2:1 multiplexer, unbuffered
LM3	4:1 multiplexer
LM3U	4:1 multiplexer, unbuffered
Miscellaneous	
CNT1	Toggle D flip-flop

ABSOLUTE MAXIMUM RATINGS (1)

Core Logic Supply Voltage, (V_{MM}) ..... +3.0V to -0.5V
TTL/CMOS Supply Voltage, (V_{TTL}) ..... +6.0V to -0.5V
TTL/CMOS Input Voltage Applied, ($V_{IN\,TTL}$) ..... -0.5V to V_{TTL}
TTL Output Current, I_{OUT}, (DC, output HI) ..... 50 mA
Storage Temperature, (T_{STG}) ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Core Logic Supply Voltage, (V_{MM}) ..... +2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +5.0V ± 5%
Operating Temperature Range, (T)(2). ..... 0° to 105°C

NOTES:(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS

TTL Inputs/Outputs: *(Over recommended operating conditions)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	—	—	0.5	V	I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0	—	—	V	Guaranteed HIGH for TTL inputs
V_{IL}	Input LOW voltage	—	—	0.8	V	Guaranteed LOW for TTL inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IH} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IL} = 0.0 V
I_{OZH}	3-state output OFF current HIGH	—	—	200	µA	V_{IN} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-200	—	—	µA	V_{IN} = 0.4 V

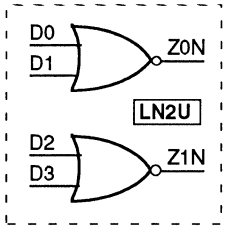
CMOS Inputs: *(Over recommended operating conditions)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage	3.5	—	—	V	Guaranteed HIGH for CMOS inputs
V_{IL}	Input LOW voltage	—	—	1.5	V	Guaranteed LOW for CMOS inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IH} = V_{TTL} - 1.0 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IL} = 0.0 V

SELECTED MACROCELL AC PERFORMANCE[1]

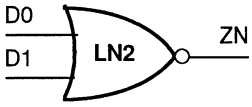
(Over Recommended Operating Conditions)

LN2U: Unbuffered Dual 2-input NOR



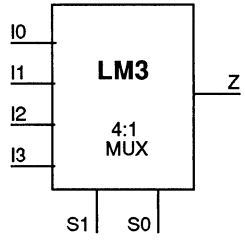
Parameter		Min	Typ	Max	Units
Propagation Delay					
(D0 - D1 to ZN0,	*Rising Signal*	30	—	91	ps
D2 - D3 to ZN1)	*Falling Signal*	20	—	73	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	26	—	88	ps
	Falling Signal	5	—	16	ps
Delay/mm wire	*Rising Signal*	161	—	542	ps
	Falling Signal	17	—	59	ps
Power Dissipation		—	0.67	1.0	mW

LN2: Buffered 2-input NOR



Parameter		Min	Typ	Max	Units
Propagation Delay					
D0, D1 to ZN	*Rising Signal*	40	—	141	ps
	Falling Signal	20	—	83	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	4	—	14	ps
	Falling Signal	2	—	6	ps
Delay/mm wire	*Rising Signal*	26	—	87	ps
	Falling Signal	8	—	27	ps
Power Dissipation		—	1.1	1.6	mW

LM3: 4:1 Multiplexer

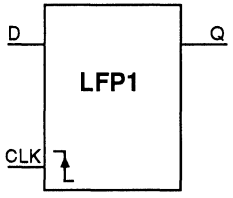


Parameter		Min	Typ	Max	Units
Propagation Delay					
S0, S1 to Z	*Rising Signal*	110	—	586	ps
	Falling Signal	150	—	570	ps
I0 - I3 to Z	*Rising Signal*	110	—	340	ps
	Falling Signal	150	—	460	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	15	ps
	Falling Signal	2	—	8	ps
Delay/mm wire	*Rising Signal*	29	—	96	ps
	Falling Signal	10	—	34	ps
Power Dissipation		—	3.1	4.6	mW

Note: 1) Macrocell AC performance is for user reference and is not explicitly measured.

SELECTED MACROCELL AC PERFORMANCE[1] (con't)

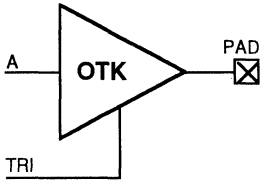
(Over Recommended Operating Conditions)

LFP1: Positive Edge Triggered D Flip-Flop	***Parameter***		***Min***	***Typ***	***Max***	***Units***
	Propagation Delay					
	CLK to Q	*Rising Signal*	90	—	313	ps
		Falling Signal	150	—	510	ps
	t_{SET-UP}		—	—	187	ps
	t_{HOLD}		—	—	135	ps
	Load Dependent Delay					
	Delay/Fan-out	*Rising Signal*	4	—	14	ps
		Falling Signal	2	—	8	ps
	Delay/mm wire	*Rising Signal*	26	—	87	ps
		Falling Signal	9	—	31	ps
	Power Dissipation		—	3.7	5.6	mW

Note: 1) Macrocell AC performance is for user reference and is not explicitly measured.

TTL OUTPUT AC PERFORMANCE[1]

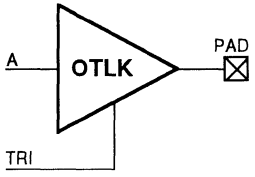
(Over Recommended Operating Conditions)

OTK: TTL Output Buffer	***Parameter***		***Min***	***Typ***	***Max***	***Units***
	Propagation Delay					
	A to PAD[2]	*Rising Signal*	1590	—	5350	ps
		Falling Signal	1530	—	5300	ps
	TRI to PAD	*Rising Signal*	1800	—	6060	ps
	(all cases)	*Falling Signal*	1800	—	6240	ps
	Load Dependent Delay					
	A to PAD	*Rising Signal*	15	—	51	ps/pF
		Falling Signal	20	—	68	ps/pF
	Edge Rates[2], [3]	*Rising Signal*	—	—	2	V/ns
		Falling Signal	—	—	2	V/ns
	Peak Current	*Rising Signal*	—	—	55	mA
		Falling Signal	—	—	65	mA
	Power Dissipation[4]		—	—	30	mW

Notes: 1) Macrocell AC performance is for user reference and is not explicitly measured.
2) With 50 pF load. 3) 0.5 - 2.4 Volts. 4) Output open circuit.

TTL OUTPUT AC PERFORMANCE[1] (con't)

(Over Recommended Operating Conditions)

OTK: TTL Output Buffer	Parameter		Min	Typ	Max	Units
	Propagation Delay					
	A to PAD[2]	*Rising Signal*	2100	—	7070	ps
		Falling Signal	2100	—	7280	ps
	TRI to PAD	*Rising Signal*	2400	—	8080	ps
	(all cases)	*Falling Signal*	2400	—	8320	ps
	Load Dependent Delay					
	A to PAD	*Rising Signal*	30	—	101	ps/pF
	(for loads beyond 50pf)	*Falling Signal*	38	—	135	ps/pF
	Edge Rates[2], [3]	*Rising Signal*	—	—	1	V/ns
		Falling Signal	—	—	1	V/ns
	Peak Current	*Rising Signal*	—	—	55	mA
		Falling Signal	—	—	65	mA
	Power Dissipation[4]		—	—	20	mW

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POWER DISSIPATION

The power dissipation is based on the utilization of the array's resources. The information below is meant to aid in the estimation of power dissipation. (Note: Power dissipation in the MQUAD package is limited to 2.8 Watts given the Recommended Operating Conditions specified in this data sheet.)

Power Characteristics for Array Resources

Parameters	Description	Min	Typ	Max	Units	Conditions
P_{DOUT}	TTL output power	—	—	30	mW	*Unloaded*
P_{DOUTL}	Low power TTL output power	—	—	20	mW	*Unloaded*
P_{DIN}	TTL input power	—	—	8	mW	
P_{DINC}	CMOS input power	—	—	8	mW	
P_{DCELL}	Core cell power	—	—	0.5	mW	

POWER ESTIMATION CALCULATION

Resources:

Total Signal Pads (Inputs and I/O pads)	=	92
Number of I/O Cells	=	52
Number of Input Cells	=	40
Number of Core Cells	=	2400

Calculation:

TTL/CMOS Inputs_____	x	8	= _____	mW
TTL Outputs_____	x	30	= _____	mW
Low Power TTL Outputs_____	x	20	= _____	mW
Core Cells_____	x	0.5	= _____	mW
Total Power			= _____	mW

OPTION DEVELOPMENT PROCEDURE

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by Vitesse design and implementation engineers:

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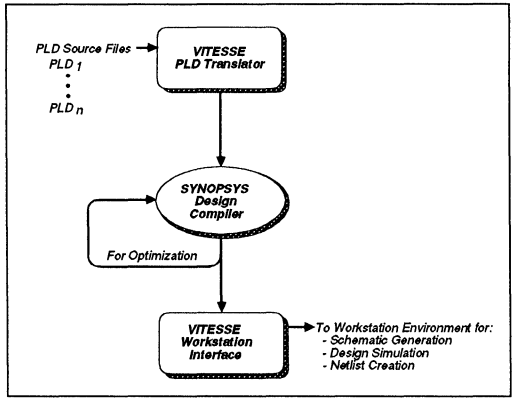
PLD CONVERSION METHODOLOGY

Through the use of the Synopsys Design Compiler™, Vitesse has created a direct path for the conversion of PLD source files into an optimized PLR2KT netlist. This procedure can be run at the customer site or by Vitesse and provides the necessary schematics and interconnect information for additional timing simulations as required. The PLD conversion process is outlined in the flowchart below.

PLD CONVERSION FLOW



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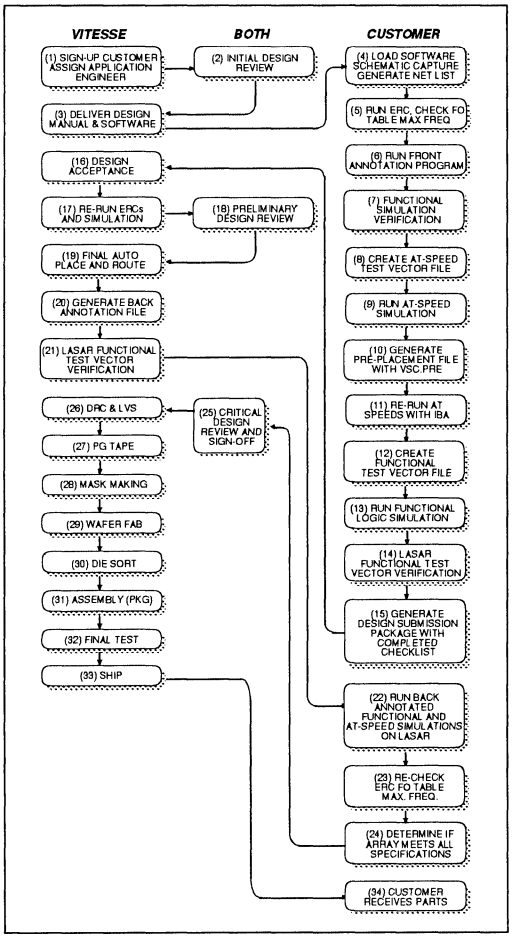
GATE ARRAY DESIGN FLOW



APPLICATION NOTE: GENERATION OF A +2V SUPPLY FROM A +5V SUPPLY

The PLR2KT gate array requires both +2 and +5 Volt power supplies. In the event that a +2 V supply is not available in the system, a simple method exists to generate the +2 V from a +5 V supply. This method involves the use of a low cost voltage regulator. Voltage regulator ICs are offered by several vendors including National Semiconductor Corp., Linear Technology Inc., and Advanced Micro Devices.

A voltage regulator IC, such as the LT117A made by Linear Technology, is a 3 terminal device. The LT117A develops a 1.25 V reference voltage between the ***OUT*** and the ***ADJ*** terminal (see figure 1). By placing a resistor, R_1, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Normally this current is the specified minimum load current of approximately 5 mA. An additional current, called I_{ADJ}, flows from the ***ADJ*** terminal and through R_2. This is a very small and constant current with a magnitude of approximately 50 µA.

It can be seen from the equation in figure 1 that the accuracy of the output voltage is limited by the accuracy of V_{REF} and the tolerance of the R_1 and R_2 resistors. The LT117A has a very tight initial tolerance of V_{REF} which permits the use of relatively inexpensive 1% film resistors for R_1 and R_2 while setting an output voltage tolerance which is compatible with the PLR2KT. If voltage regulators which have wider reference tolerance are used (such as industry standard LM117), a trim pot may be needed to set the exact value of the output voltage.

Figure 2 depicts the LT117A with the resistor values needed to generate the +2 V supply. The output current of the LT117A is limited to 1.5 Amps which is sufficient for any implementation of the PLR2KT. For systems which use several PLR2KT chips, regulation can be accomplished by devices such as the LT1038 (also from Linear Technology) which can handle an output current up to 10 Amps. The use of this larger regulator is identical to the LT117A.

FIGURE 1

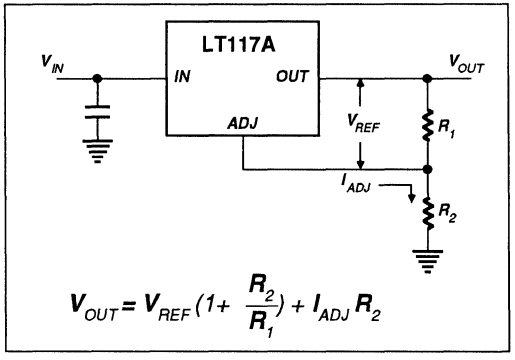
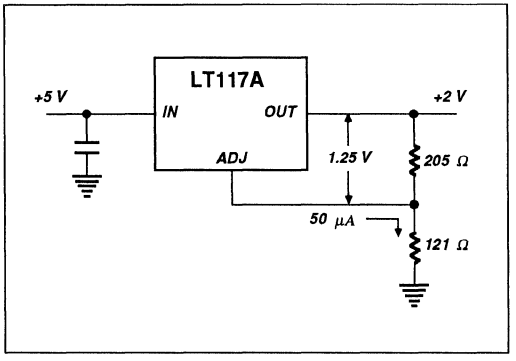


FIGURE 2



FEATURES

- Superior Performance: Supports clock rates up to 2.5 GHz in Mux/Demux applications
- Proven H-GaAs E/D MESFET process
- Array performance
  - Typical gate delay (high speed section): 150 ps @ 23 mW *(2-input XOR/XNOR, F.O. = 1, 0.5 mm wire)*
  - Typical gate delay (low power section): 330 ps @ 0.42 mW *(3-input NOR, F.O. = 1, 0.5 mm wire)*
  - High speed D Flip-flop toggle rate: > 3.3 GHz @ 64 mW
  - Low power D Flip-flop toggle rate: 500 MHz @ 4.1 mW
  - High speed differential I/Os up to 2.5 GHz
  - ECL 100K compatible I/Os up to 400 MHz
- Structured cell approach: High speed (SCFL) and low power (DCFL) cells for maximum performance and minimum power dissipation
- Up to 22 ECL inputs, 20 ECL outputs, 3 high speed differential inputs, 2 high speed differential outputs
- Power supplies: V_{EE} = -5.2 ± 0.26V, V_{TT} = -2.0 ± 0.1V
- Three temperature ranges:
  - Commercial: 0° to 70° C
  - Industrial: -40° to +85° C
  - Military: -55° to 125° C
- Power Dissipation: < 2.5W typical
- 52-pin leaded or leadless ceramic chip carrier
- Schematic capture/simulation supported on MENTOR, CADENCE or VALID platforms
- Min/Max simulation supported with LASAR™

INTRODUCTION

The VSC1520 is a 1520 gate GaAs structured cell array tailored for very high speed applications in systems requiring clock rates up to 2.5 GHz. The architecture utilizes a structured cell approach that combines both high speed source coupled FET logic (SCFL) and low power direct coupled FET logic (DCFL) cells to allow the user to obtain the optimum speed/power trade-off. The speed critical sections of the design use high speed SCFL cells, while the lower speed portion can be implemented with low power DCFL cells.

The VSC1520 is built using Vitesse's proprietary H-GaAs E/D MESFET process. The VSC1520 allows flexibility in design while providing very short turnaround time, without compromising overall circuit performance.

APPLICATIONS

The high speed I/O and fast internal gates make the VSC1520 ideally suited for mux/demux applications in fiber optic communications systems and computer backplanes. Other applications include critical paths in testers, LANs, and video graphics subsystems. In addition, the VSC1520 is ideally suited for implementing fast prescalers in PLL systems.

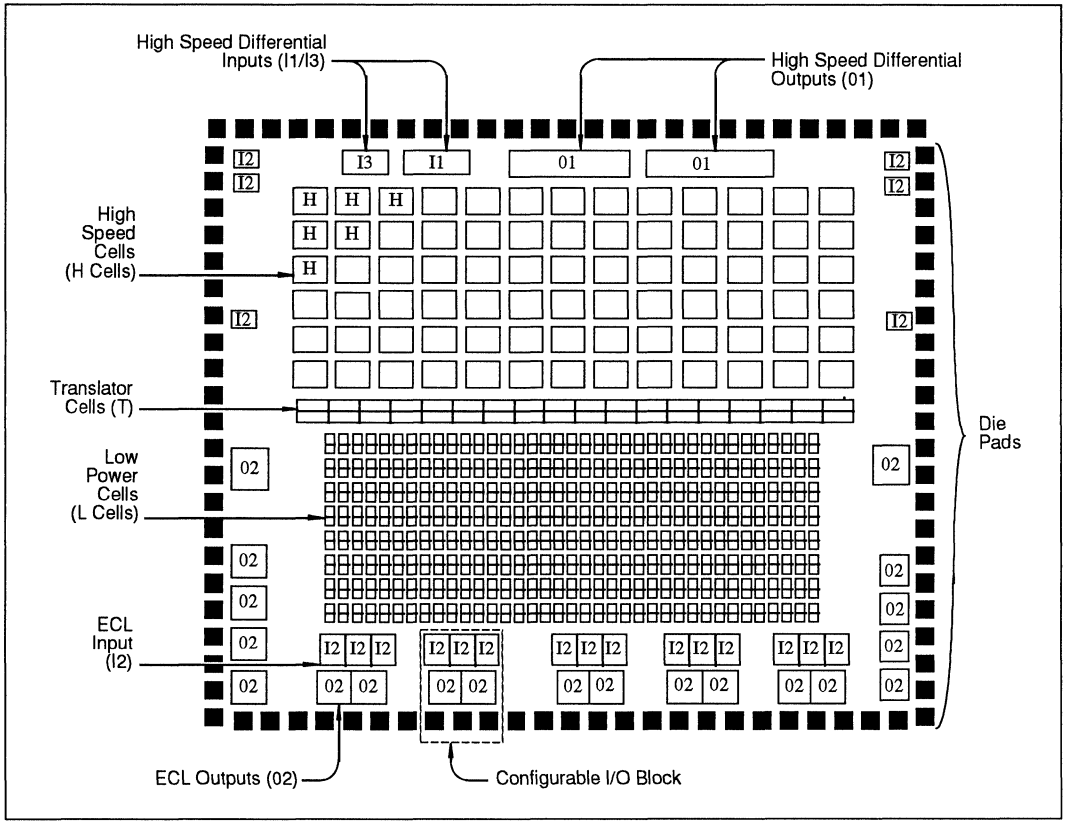
ARRAY ARCHITECTURE

The figure on page 1-34 shows the architecture of the VSC1520. The arrays contain input cells, output cells, high speed cells, low power cells, and translator cells. The various cell types are summarized in Table 1.

Input Cells

Input cells are used to bring signals onto the array. There are two types of input cells: high speed differential inputs, and ECL inputs.

VSC1500/1520 ACHITECTURE



High Speed Differential Inputs

There are three high speed differential inputs on these arrays. These inputs are designed to bring signals on-chip at rates up to 2.5 GHz. These inputs can also be used single-ended with an on-chip reference generator. The high speed inputs accept signals with a nominal 1V peak-to-peak swing. The high speed inputs are intended to be AC coupled, therefore strict adherence to ECL input specifications is not necessary.

ECL Inputs

There are 22 ECL input cells on these arrays. These inputs accept 100K ECL levels with an on-

Table 1: Cell Type Summary

Input Cells	
1. High speed differential inputs	3
2. ECL inputs	22
Output Cells	
3. High speed differential outputs	2
4. ECL outputs or	20
5. Differential ECL outputs	9
Internal Cells	
6. High speed cells	96
7. Low power cells	592
8. Translator cells	36

chip reference generator. ECL inputs can also be used as differential receivers. These inputs can be configured to yield up to nine differential ECL receivers. These inputs can handle frequencies up to 400 MHz.

Output Cells

Output cells are used to take signals off-chip. There are two types of output cells: high speed differential outputs and ECL outputs.

High Speed Differential Outputs

There are three high speed differential outputs on the 1520. These outputs are customized to take signals off-chip at rates up to 2.5 Gbits/sec. The high speed differential outputs can drive 50 ohm loads and provide a nominal 1V peak-to-peak signal swing.

ECL Outputs

There are 20 ECL outputs. These outputs can be configured to yield up to 9 differential ECL outputs. They provide 100K ECL levels and can drive 50Ω loads. ECL outputs can handle frequencies up to 600MHz.

ECL Input and Output Cell Utilization

There are 22 ECL input cells and 20 ECL output cells. One hundred percent utilization of ECL input and output cells is not possible since ECL outputs require VCCA pads. The ECL input and output cell combinations that can be used on these arrays are shown in Table 2.

Table 2: ECL I/O Combinations

If number of ECL inputs =	22	19	16	13	10	7
then number of ECL outputs =	10	12	14	16	18	20

INTERNAL CELLS

High Speed Cells

There are 96 high speed cells (H cells) which occupy about 60% of the internal core of the array. High speed cells can be used to implement speed critical portions of a design.

Each high speed cell is made up of E-mode and D-mode MESFETs and can be wired to perform a latch function. The circuit topology used is differential source coupled FET logic (similar to ECL) which results in ultra-high speed, high noise immunity macros. The H-cells use a -5.2V power supply.

Figure 2 shows a high speed cell personalized as a 2:1 multiplexer. The circuit is a two level series gated structure with a constant current generator, I_{CS}. SB, SBN are select inputs for the mux which selects the path for the current in the lower switch. A1, A1N and A2, A2N are differential data inputs for the upper current switch. At the outputs there are two constant current source followers which provide differential logic levels for the next stage and the current gain.

Figure 2: Simplified H-Cell (2:1 Multiplexer)

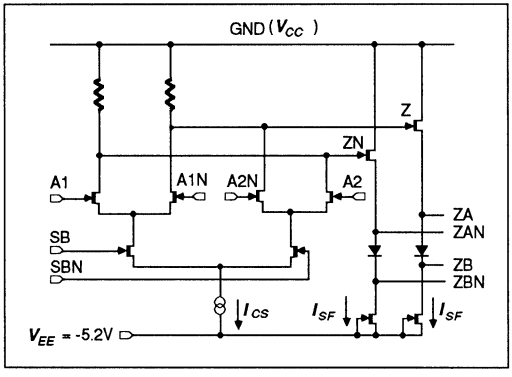
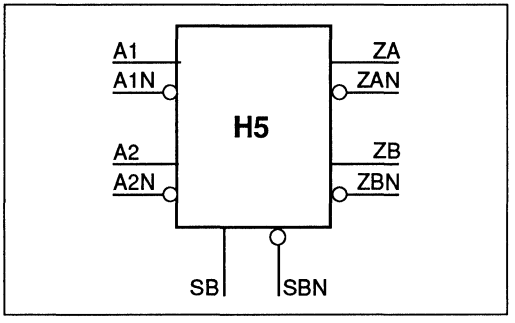


Figure 3 shows the symbol for a 2:1 Mux (Macro H5). ZA, ZAN outputs and ZB,ZBN outputs are logically equivalent, but ZB,ZBN levels are shifted down by a diode drop from ZA, ZAN outputs. ZA, ZAN are for the A-inputs of the loads and ZB, ZBN are for the B-inputs of the loads.

Figure 3: Symbol For Differential 2:1 Mux (Macro H5)



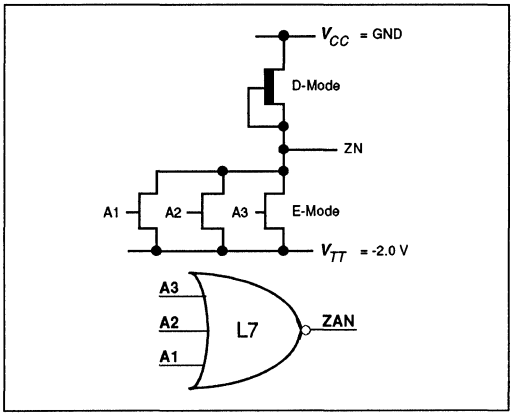
Low Power Cells

There are 592 low power cells (L cells) which occupy about 35% of the internal core of the array. These cells are used to implement non speed critical portions of a design and thus reduce overall power dissipation.

Each low power cell is made up of three enhancement mode transistors and one depletion mode transistor and can be wired to perform a 3-input NOR function. When all inputs A1, A2, and A3 are at logic 'LOW' level, output ZN is pulled HIGH. If at least one input goes HIGH, then output ZN is pulled LOW. Figure 4 shows the schematic and symbol for a 3-input NOR (Macro L7).

The circuit configuration used is Direct Coupled FET Logic (DCFL), which provides high speed, low power macros. The low power macrocells use a -2V supply.

Figure 4: Schematic and Symbol For a Low Power 3-input NOR (Macro L7)



Translator Cells

There are 18 T1 translators and 18 T2 translators. T1 translators convert H-cell logic levels to L-cell logic levels. T2 translators change L-cell levels to H-cell levels. These cells occupy 5% of the internal core of the array and are located between the H-cell and L-cell sections.

MACRO LIBRARY

Macros define the interconnection pattern of transistors in one or more cells which perform a logic function. A representative list of macros for the VSC1520 array are given below. For the complete set of macros, please refer to the macro library in the design manual.

HS MACROCELL LIBRARY

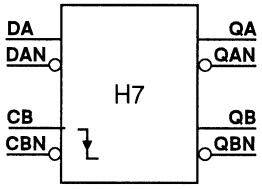
Name	Description
High Speed Macros	
H1	Inverter/buffer
H2	2-input OR/NOR
H3	2-input AND/NAND
H4	2-input XOR/XNOR
H5	2:1 multiplexer
H6	D-latch
H7	D flip-flop (negative edge triggered)
Low Power Macros	
L1	High fan-out buffer
L2	Medium fan-out buffer
L3	2-input NOR
L4	2:1 MUX
L5	D-latch
L6	High drive D flip-flop (negative edge triggered)
L6L	D flip-flop (negative edge triggered)
L7	3-input NOR
L8	4-input NOR
L9	2-input XNOR
L10	D flip-flop with synchronous reset
L11	D flip flop with asynchronous reset & set
L12	-2V pull-down
Input/Output Macros	
I1	High speed differential clock input
I2	ECL input
I3	High speed differential data input
O1	High speed differential output
O2	ECL output driver
Translator Macros	
T1	H-cell to L-cell signal translator
T2	L-cell to H-cell signal translator

MACROCELL AC PERFORMANCE CHARACTERSTICS (con't)

VSC1520 High Speed Macros

(Over recommended operating conditions:, Load: F.O. = 1; 0 mm wire).

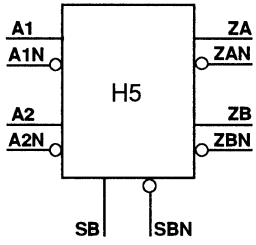
H7: D Flip-Flop



Parameter	*Min*	*Typ*	*Max*	*Units*
Propagation Delay CB, CBN to QA, QAN, QB, QBN Clock to Output	—	155	165	ps
Load Dependent Delay Delay/Fan-out Delay/mm wire	— —	15 70	16 74	ps ps
Set-up Time	—	110	135	ps
Hold Time	—	40	50	ps
Toggle Frequency	—	3.3*	—	GHz
Power Dissipation	32	45	64	mW

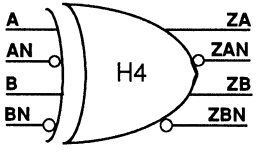
** Assumes 0.5 mm wire*

H5: 2:1 Multiplexer



Parameter	*Min*	*Typ*	*Max*	*Units*
Propagation Delay A1, A1N to ZA, ZAN, ZB, ZBN	—	115	122	ps
A2, A2N to ZA, ZAN, ZB, ZBN	—	115	122	ps
SB, SBN to ZA, ZAN, ZB, ZBN	—	145	155	ps
Load Dependent Delay Delay/Fan-out Delay/mm wire	— —	15 70	16 74	ps ps
Power Dissipation	16	23	32	mW

H4: 2-Input XOR/XNOR



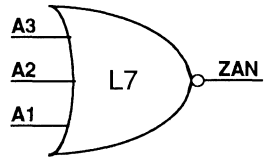
Parameter	*Min*	*Typ*	*Max*	*Units*
Propagation Delay A, AN to ZA, ZAN, ZB, ZBN	—	115	122	ps
B, BN to ZA, ZAN, ZB, ZBN	—	145	155	ps
Load Dependent Delay Delay/Fan-out Delay/mm wire	— —	15 70	16 74	ps ps
Power Dissipation	16	23	32	mW

MACROCELL AC PERFORMANCE CHARACTERSTICS

VSC1520 Low Power Macros

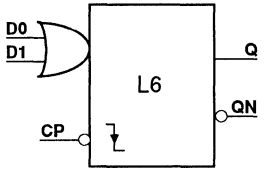
(Over recommended operating conditions:, Load: F.O. = 1; 0 mm wire).

L7: 3-Input NOR



Parameter	*Min*	*Typ*	*Max*	*Units*
Propagation Delay A1, A2, A3 to ZN	—	200	230	ps
Load Dependent Delay Delay/Fan-out Delay/mm wire	 — —	 55 260	 — —	 ps ps
Power Dissipation	0.28	0.42	0.56	mW

L6: High Drive D Flip-Flop



Parameter	*Min*	*Typ*	*Max*	*Units*
Propagation Delay CP to Q, QN	—	560	650	ps
Set-up Time	—	530	600	ps
Hold Time	—	—	—	ps
Toggle Frequency	—	650 *	—	MHz
Load Dependent Delay Delay/Fan-out Delay/mm wire	 — —	 30 130	 — —	 ps ps
Power Dissipation	2.7	4.1	5.4	mW

DC CHARACTERISTICS

ECL Inputs/Outputs:

(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, Output load 50Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	—	-600	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH for all ECL inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1620	mV	Guaranteed LOW for all ECL inputs
I_{IH}	Input HIGH current	—	10	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

NOTE: Differential ECL output pins must be terminated identically.

High Speed Inputs and Outputs:

(Over recommended operating conditions. V_{CC} = GND, Output load = 50Ω to -2.0V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Input reference level	—	-3.5	—	V	—
V_{OH}	Output HIGH voltage	—	-0.5	—	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load, 50Ω to -2.0 V

NOTES:1) Built in reference generator, the high speed inputs are designed for AC coupling.
2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed output pins must be terminated identically.
4) Limited ESD protection is provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (V_{TT}) ..... -3.0V to +0.5V
Power Supply Voltage (V_{EE}) ..... V_{CC} (GND) to -7.0V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5V to +0.5V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7V to V_{CC} + 0.7V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.0V ± 0.1V
Power Supply Voltage, (V_{EE}) ..... -5.20V ± 0.26V
Operating Temperature (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTES:1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2) V_{TT} must be applied before any input signal voltage (V_{ECLIN} and V_{HSIN}) must be greater than V_{TT} - 0.5V.
3) Lower limit of specification is ambient temperature and upper limit is case temperature.
4) When using internal ECL 100K reference level.

OPTION DEVELOPMENT PROCEDURE

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are normally performed by Vitesse design and implementation engineers:

- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule checking and layout vs schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart on page 1-42 summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse.

PACKAGING

A 52-pin multilayer ceramic leaded or leadless chip carrier is used for the VSC1520. It is a cavity down package with the heat spreader on top. Particular attention has been paid to reduce crosstalk of high speed signals and to keep the trace impedance at 50 ohms.

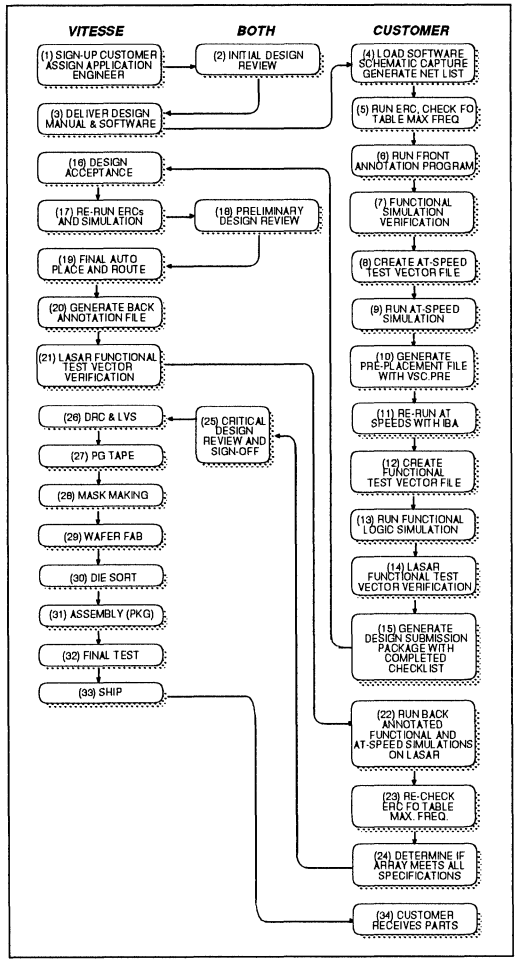
CAD TOOLS/SUPPORT

VSC1520 designs are supported on THE MENTOR platform. The Vitesse Design Kit includes documentation and software which allow the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. To facilitate floorplanning and block preplacement, Vitesse has an interactive graphical placement program that the customer may choose to use for their design. This program is supported in the X Windows™ environment. MERLYN-G placement and routing tools are used for physical implementation.

TRAINING

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

GATE ARRAY DESIGN FLOW



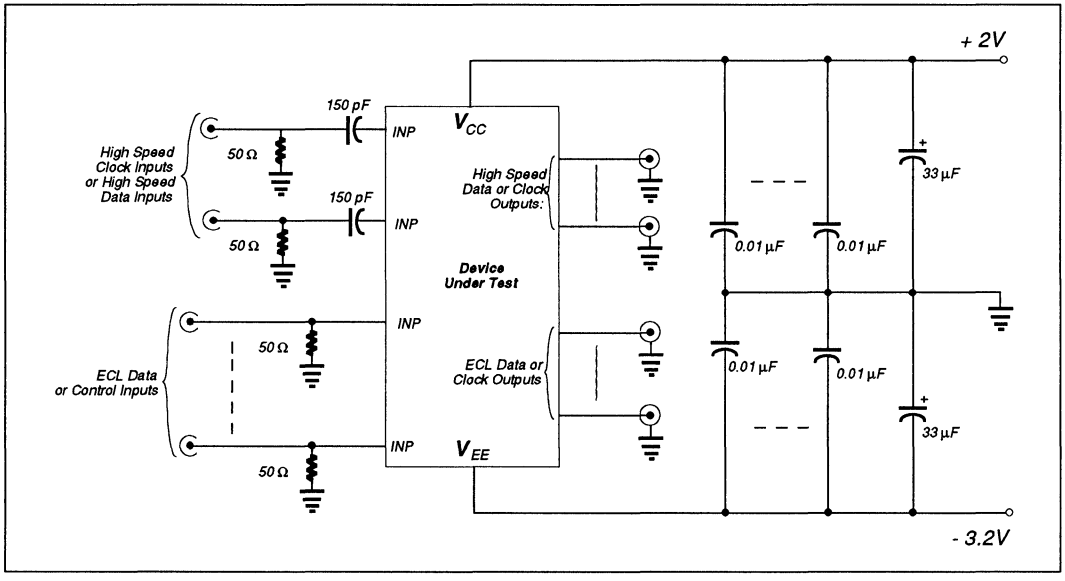
VSC1500 DUT BOARD

The VSC1500 DUT board is a special purpose circuit board which provides a test bed suitable for evaluating the performance characteristics of the VSC1500 in the 52 pin leadless chip carrier.

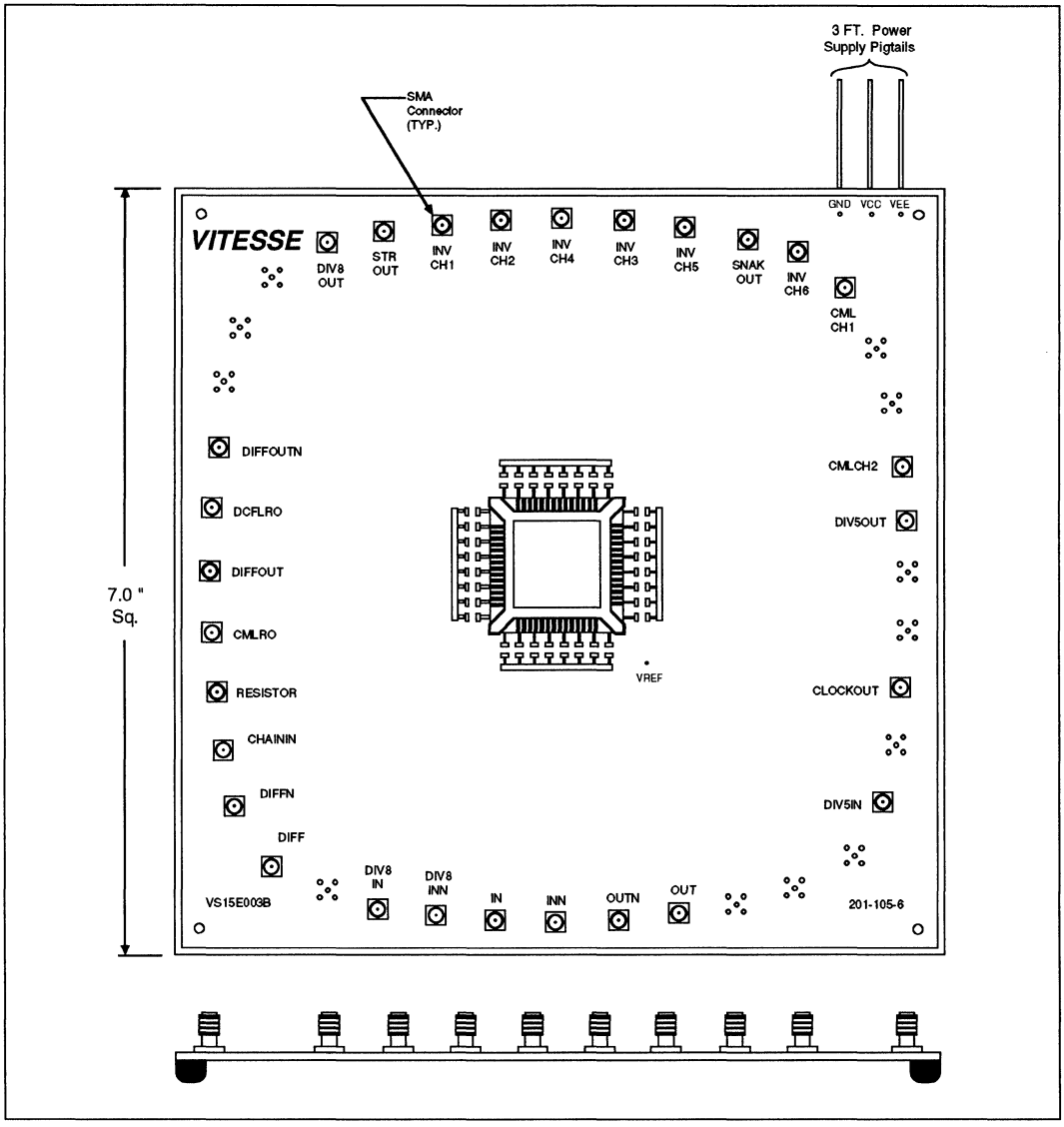
The figure below is a schematic representation of this circuit board. This board provides a controlled impedance transmission line for all signals and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VSC1500 circuit operates in an ECL environment with standard ECL power buses: 0V, -2V, -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus. The device to be tested is held in place with a pressure retaining fixture. The figure on the following page shows the physical dimensions and the connections labels for the evaluation board.

VSC1520 DUT SCHEMATIC



VSC1500DUT BOARD DIMENSIONS



G-TAXICHIP FEATURES

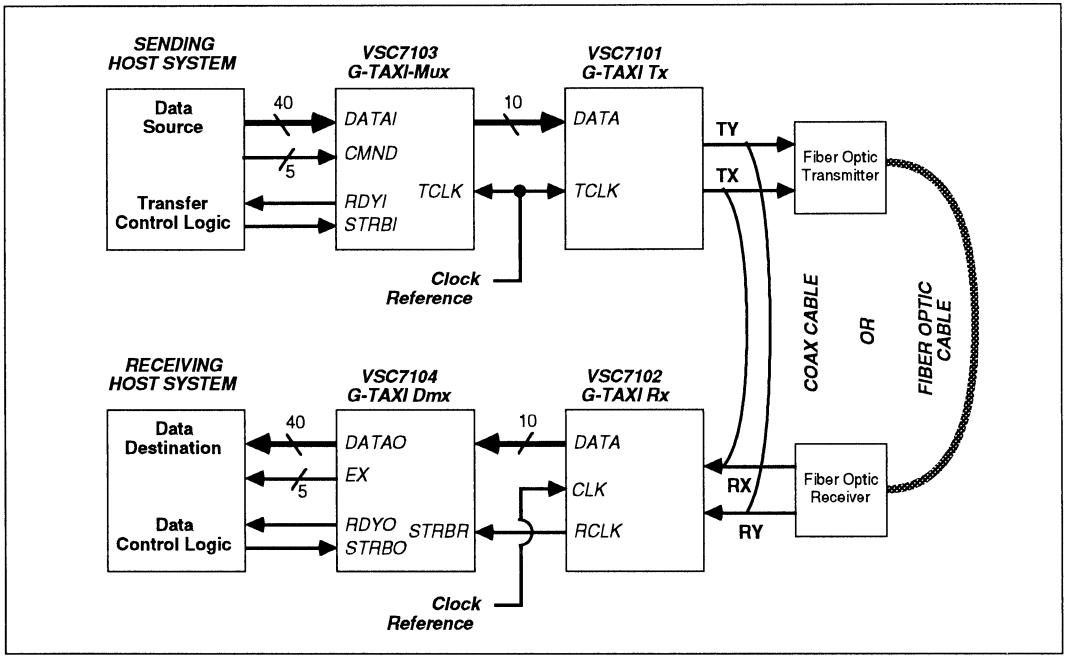
- Compatible with ANSI X3T9.3 Fiber Channel Standard
- Up to 1.25 Gbits/sec serial data rate
- 32 or 40-bit wide parallel TTL data bus input
- On-chip PLL (phase-locked loop) clock generation and recovery
- ANSI 8B/10B encoding
- Dedicated on-chip circuitry and pins to implement loopback testing
- Built-in test mode to facilitate factory testing
- Vitesse 0.8µ GaAs MESFET technology
- Small footprint surface mount packaging
- +5V and +2V power supply operation

GENERAL DESCRIPTION

The G-TAXIchips™ are a general purpose interface for very high speed point-to-point communications over coaxial or fiber-optic media. The G-TAXI transmitter and receiver are capable of two speed grades. The -1.2 parts are capable of handling serial data at rates up to 1.25 Gbits/sec. The -1.0 parts can handle up to 1.0625 Gbits/sec. The speed of the G-TAXI system is tuneable (±10%) from its center frequency to provide flexibility. The GTAXIchips are compatible with the ANSI X3T9.3 Fiber Channel Standard. The G-TAXIchips can also be used for proprietary links.

The G-TAXIchips consist of 4 devices: the VSC7101 Transmitter, VSC7102 Receiver, VSC7103 Multiplexer, and VSC7104 Demultiplexer. The G-TAXIchips provide simple point-to-

G-TAXICHIP SYSTEM BLOCK DIAGRAM



point serial physical transport for parallel data. The G-TAXI Multiplexer/Transmitter (Mux/Tx) inputs originate in a sending host system, using a standard ready/strobe handshake for parallel data transfer. An output ready pulse from the G-TAXI Receiver/ Demultiplexer (Rx/Dmx) indicates that data is available to the receiving host system.

The Mux and Dmx in the GTAXI chip implement the ANSI X3T9.3 8B/10B encoding scheme and make the full chip set compatible with this standard. Alternatively, the Tx and Rx chips can be used separately to implement a data link which uses any proprietary coding scheme which meets the minimum required data transition density.

APPLICATIONS

- High speed parallel data transfer at rates up to 1.25 Gbits/s (-1.2 speed grade)
- Data communications links that utilize standards such as the ANSI Fiber Channel X3T9.3, high performance parallel interface (HiPPI), or proprietary links
- High speed data links between groups of low to medium speed devices, such as CPUs and disk clusters
- Long distance time-multiplexing of multichannel video signals
- High bandwidth video such as HDTV
- Extended distance parallel data transmission to devices such as remote sensors and display terminals where data is moved in packets at a rate higher than 20 MBytes/sec
- High speed parallel data communication in a multi-processor system where multiple CPUs and multiple memory modules need to exchange data at high data rates with minimal latency
- Fiber optic industrial equipment control and data communications systems, where electrical and magnetic interferences make communications difficult using typical wire interconnect
- High speed control busses where interconnect hardware is critical or expensive such as military and avionics control systems using fiber optic technology
- Any high speed system which transports parallel data between devices using ribbon cable or a backplane bus

TRANSMITTER/RECEIVER (TX/RX) FEATURES

- Parallel data inputs registered into transmitter synchronous with TCLK
- Ten bit parallel PECL input
- Up to 1.25 Gbits/sec serial link data rate
- Up to 125 Mbits/sec parallel data rate
- Tuneable over a ±10% from center frequency (1.25 GHz or 1.0625 GHz) range by changing reference clock frequency at ***TCLK***
- +5V power supplies
- On chip Phase-Lock Loop (PLL)
- Dedicated pins to implement loopback testing
- Built-in test mode to bypass PLL
- Small footprint, surface mount 28 pin leaded ceramic chip carrier

G-TAXI TX FUNCTIONAL DESCRIPTION

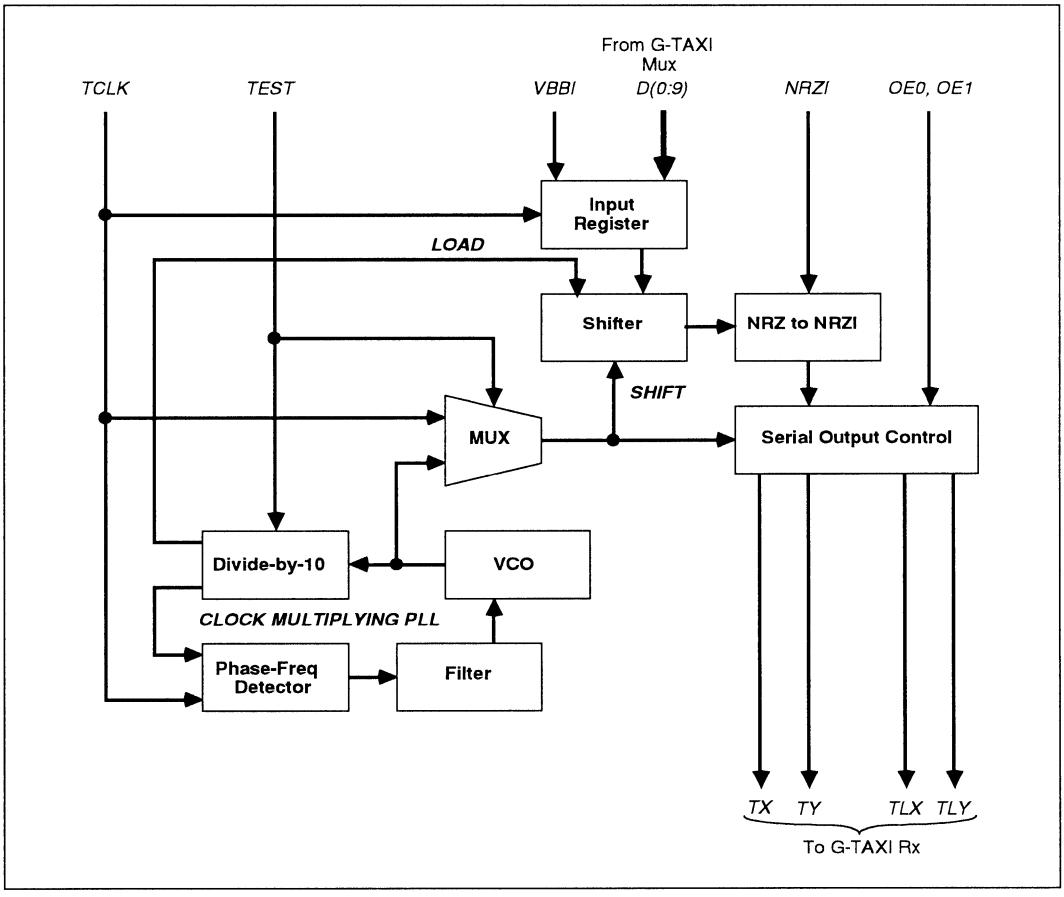
Normal Operation Mode

When data from the VSC7103 Mux has been latched into a VSC7101 Tx, it is serialized and shifted out onto the serial data link via the ***TX***, ***TY***, ***TLX***, ***TLY*** outputs at the internally generated high-speed clock rate.

Clock Requirement

The serial link speed is derived from an external master clock source and applied through the ***TCLK*** input pin on the Tx. This signal is used as a reference for the internal phase-locked loop (PLL) clock multiplying circuit in the Tx. This signal is also used synchronously to transfer bytes of data between the Mux and Tx. The absolute range of frequencies can be varied over a ±10% range offer-

G-TAXI TX (VSC7101) FUNCTIONAL BLOCK DIAGRAM



ing flexibility to the system designer. This master clock frequency is 1/10 of the serial link speed and four or five times the frequency of the input data bus depending on word width selection (32 or 40 bit) in the multiplexer chip. A 25 MHz 32-bit bus, for example, would require a 100 MHz clock source at ***TCLK*** to run the Mux and would result in a 1.00 Gbit/sec serial link output speed on the Tx.

In a typical synchronous setup, a crystal-controlled oscillator with PECL output drives the ***TCLK*** pin at G-TAXI Tx and ***TCLK*** pin at G-TAXI Mux. This clock frequency is divided by four or five and applied to the rest of the system. The input clock frequency required to achieve various rates on the serial link, and the resultant parallel input data transfer rate are shown in the table below.

Speed Grade	*TCLK Ref Freq (MHz)*	*Parallel Input Rate (ns/Byte)*	*Internal Clock Multiplying Ratio*	*Serial Data Rate (MBits/sec)*
-1.2	125.0	8.0	10	1250
-1.0	106.25	9.41	10	1062.5

Clock Multiplying PLL

The PLL multiplies the input frequency of the ***TCLK*** input by 10.

Input Register

Parallel data inputs, ***D(0:9)*** are clocked into the INPUT REGISTER by the rising edge of the external ***TCLK*** signal.

Shifter

The SHIFTER function is parallel loaded from the INPUT REGISTER by ***TCLK***, then serially shifted out at 10x ***TCLK***.

NRZ TO NRZI

The NRZ to NRZI conversion is enabled by the ***NRZI*** input if the system uses an NRZI transmission code.

Serial Output Control

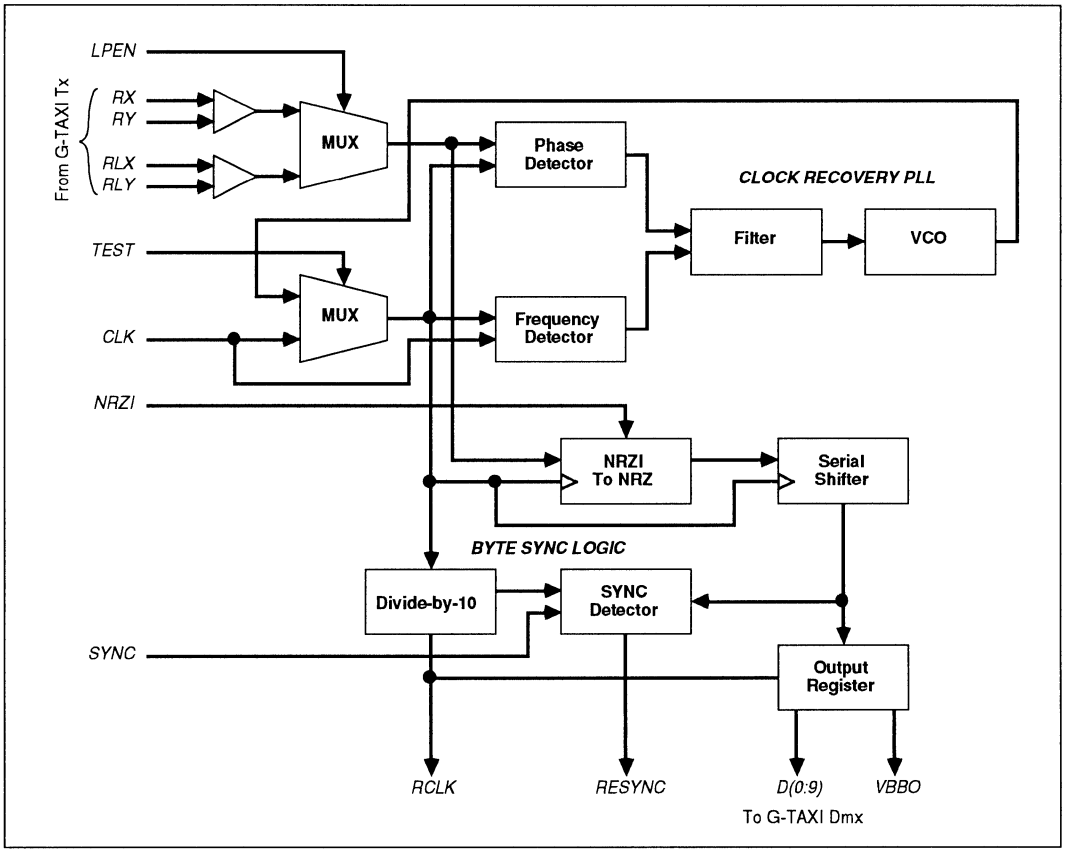
The differential transmitted outputs ***TX/TY*** and ***TLX/TLY*** carry the serial bit stream. These two pairs of outputs are controlled by ***OE0*** and ***OE1*** input pins. Both pins are asserted LOW, OE0 enables ***TX/TY*** outputs and ***OE1*** enables ***TLX/TLY*** outputs. ***TLX/TLY*** outputs are connected to the local ***RLX/RLY*** inputs of the G-TAXI Rx. These outputs are enabled during loopback diagnostic testing and are disabled during normal operation. ***TX/TY*** are forced to LOW/HIGH state when ***OE0*** = HIGH.

Test Mode

The ***TEST MODE*** input can be used to force the G-TAXI Tx into test mode. This will allow testing of the logic in the REGISTER and SHIFTER without having to first stabilize the PLL clock multiplier. When in TEST mode, the internal PLL clock is switched out and replaced by the ***TCLK*** input. The test mode is entered by floating the ***TEST*** signal. Normally the ***TEST*** is tied HIGH.

This switch makes the part a determinate and synchronous system. An automatic test system will be able to clock the part through its functional test patterns at any rate or sequence that is convenient.

G-TAXI RX (VSC7102) FUNCTIONAL BLOCK DIAGRAM



G-TAXI RX FUNCTIONAL DESCRIPTION

Normal Operation Mode

The VSC7102 accepts encoded serial data from the Tx on the ***RX/RY*** or ***RLX/RLY*** pins. This encoded data is loaded in parallel to the data outputs, ***D(0:9)***.

When the ***SYNC*** pattern is received, it causes the ***BYTE SYNC LOGIC*** to re-establish byte boundaries. During ***SYNC*** detection, the data outputs, ***D(0:9)***, hold their previous values and do not change until a new data pattern is received.

Clock Generation

The serial link speed is derived from a master frequency source at the transmitter. This frequency source is multiplied by 10 using the G-TAXI Tx clock multiplying PLL. When the serial data stream arrives at the G-TAXI Rx, the clock information is extracted from the encoded data by the use of a PLL circuit.

The clock recovery PLL in the G-TAXI Rx examines every transition (LOW-HIGH, HIGH-LOW) in the arriving serial data stream and aligns

its own VCO with these data transitions. The VCO provides the clock to operate all the data transfers in the receiver.

In order for the VCO in the G-TAXI Rx to maintain its correct phase relationship with the received data, an encoding scheme must ensure that the maximum run-length of the encoded data does not exceed 5 bits.

The signal that transfers data from serial to parallel is buffered to the ***RCLK*** output and can be used by other G-TAXIs for other circuit functions. This output is synchronous with the upstream G-TAXI Tx reference clock.

Data Synchronization

Parallel outputs from G-TAXI Rx are synchronous with ***RCLK***. ***RCLK*** is a buffered version of the signal which controls data transfers inside G-TAXI Rx on byte boundaries. Byte boundaries move when the G-TAXI loses and re-acquires ***SYNC***. To protect slave systems (which may use this output as a master clock) from having clocks which are too narrow, the internal logic will stretch an ***RCLK*** cycle when the output pulse would have been less than a byte time long. The partial data symbol being processed just prior to this re-acquisition of ***SYNC*** is lost.

Output ***RCLK*** will rise as the DATA changes. It will fall midway through the symbol.

PLL & Clock Circuit

The serial link speed is determined by the Tx VCO, but the Rx must know what data rate to expect. It must also have the ability to follow actual data rates, either faster or slower than the local reference clock.

This circuit follows the incoming data and allows the encoded clock and data stream to be decoded into separated clock and data patterns. Its center frequency is established by the reference at ***CLK*** and is capable of tracking data with frequency offsets of ±0.1%.

Media Interface

RX, ***RY*** inputs are driven by differential PECL voltages. These inputs carry the encoded serial data from the distant Tx. ***RLX*** and ***RLY*** are PECL serial data inputs carrying the loopback data stream from the local Tx ***TLX/TLY*** outputs.

NRZ_TO_NRZI

The NRZ_TO_NRZI conversion is enabled by the ***NRZI*** enable pin if the system uses an NRZI transmission code.

Serial Shifter

The shifter is serially loaded from the media interface using the recovered clock as a clock source.

Byte Sync Logic

The incoming data stream is a continuous stream of data bits without any companion signal which denotes byte boundaries. This logic will continuously monitor the data stream and upon detecting the reserved code used for ***SYNC***, it will signal byte boundaries.

BYTE SYNC LOGIC is responsible for re-alignment of ***RCLK*** signal for the parallel output register. Byte re-sync function can be disabled with the ***SYNC*** input.

Parallel Output Register

OUTPUT REGISTER is clocked by the recovered byte clock and will reflect the most recent data on the link.

Test Mode

TEST input is used to force the G-TAXI Rx into TEST mode. This will allow testing of the logic in the REGISTER and SHIFTER without having to first stabilize the PLL. The internal VCO is switched out and everything is clocked from the ***CLK*** input.

This switch makes the part a determinate, synchronous system, instead of a statistical, asynchronous one. An automatic test system will be able to clock the part through its functional test

patterns at any rate or sequence that is convenient.

When the logic has been verified, the part can be put back into the normal mode and the PLL functions can be verified using known good logic.

MUX/DMX FEATURES

- Parallel 32 or 40-bit wide TTL bus interface
- 32 or 40-to-8 mux — 8-to-32 or 40 demux
- Encode/decode functions and special characters are 8B/10B compliant (ANSI Std)
- ANSI Fiber Channel X3T9.3 compatible
- Parallel bus interface compatible with industry standard FIFO applications
- Asynchronous input to Mux with Ready/Strobe handshake
- Synchronous interface with the G-TAXI Rx/Tx is completely transparent to users
- 32/40-bit select pin
- 5 command bits for controlling the transmission of regular or special characters
- Exception pins for commands to receiver
- Up to 125 MBytes/sec parallel data rate
- +5V and +2V power supply operation
- 132 pin aluminum MQUAD™

GENERAL

The Mux-Dmx chipset serves as the interface used to simplify the design of control logic at the system bus. The Mux-Dmx chips also contain the logic used for the encoding and decoding of the transmission block code.

G-TAXI is the ideal product to make high-speed system-to-system communication interconnection with the bandwidth to accommodate even today's very fast computing machines. The G-TAXI reaches a serial data rate of 1.25 Gbits/sec, which translates into 125 Mbytes/sec at Mux/Dmx interfaces. Therefore, the G-TAXI Mux/Dmx data is clocked at rates up to 125 MHz at the Tx/Rx interfaces, 31 MHz (32-bit mode) and 25 MHz (40-bit mode) at the parallel bus (word) interfaces.

Normal Operation Mode

When the 32-bit or 40-bit data has been latched into a G-TAXI Mux, it is disassembled into 4 or 5 bytes (8-bit each), encoded into 10-bit codewords and transferred to the G-TAXI Tx, serialized and shifted out onto the serial transmission medium. The G-TAXI Rx at the other end of the serial link performs serial-to-byte conversion and transfers bytes to the G-TAXI Dmx for decoding and re-assembly into the original word-width. All operations are transparent to the bus user; data words seemingly are written into one end of the link and read from the other end.

In most data communications operations, maximum attainable bandwidth is desired. The G-TAXI Mux bus interface can be asynchronous, but highest throughput is only possible when it operates synchronously with the system clock. The ***CMND*** (command) inputs can be designated for ANSI 8B/10B communication control functions time-multiplexed into user data transmission (see 8B/10B CMND Input Special Function Table in Encode Tables section immediately preceding the G-TAXI Dmx functional description).

User Hardware Interface

There are two types of electrical interfaces on the G-TAXI Mux/Dmx. Bus parallel data and handshake signals are TTL compatible. Data and strobe interfaces to the G-TAXI Tx/Rx is single-ended 100K compatible ECL, referenced to +5.0V. This type of interface is called PECL. The chipset requires a PECL clock reference source at the "byte-rate" frequency.

Critical System Integration Issues (Mux)

One master frequency reference source is required for the G-TAXI Tx, and one is required for the G-TAXI Rx. The frequency reference for the G-TAXI Tx is used to generate the serial link data

rate. The frequency reference for the G-TAXI Rx is used to center its data recovery PLL circuits to an expected received data rate.

The external clock source must be crystal controlled and continuous. It is also used to control the byte rate transfer of data between the G-TAXI Mux and the G-TAXI Tx. In a system where the G-TAXI is synchronous to the 'host', it is more desirable to divide this "byte" clock down and use it as the master clock for the host system. The G-TAXI Mux provides this facility through its ***CLK45*** pin which carries the ***TCLK*** divided-by-4 or by-5 signal.

G-TAXI maintains link synchronization and word boundary alignment through the use of a special pattern. The G-TAXI Rx performs byte boundary realignment upon the arrival of an IDLE pattern. Therefore, when such operation is required, e.g. upon system initialization or at the beginning of a block transfer, the G-TAXI Mux ***STRBI*** input is held LOW for one or more ***CLK45*** cycles. Subsequently the Mux generates the IDLE pattern at its output. The IDLE pattern will be Muxed into the G-TAXI Tx for transmission to the receiving system. The IDLE pattern can also be generated by setting the CMND(4:0) to 10101.

In an asynchronous system where ***STRBI*** may stay inactive when no data is available to the G-TAXI chips, the G-TAXI Mux starts to force IDLEs to G-TAXI Tx when the MULTIPLEXER LATCH becomes empty.

Critical System Integration Issues (Dmx)

STRBO enables new data to be latched into the OUTPUT LATCH when available, ***RDYO*** will go HIGH when such transfer is READY. When the next data transfer from Dmx LATCH into BUFFER LATCH occurs before it is emptied, the previous content of the BUFFER LATCH will be overwritten and ***EX(4:0)*** outputs set to (11010) to indicate data overrun condition.

In a data overrun situation, the lost word cannot be recovered by any means.

When the ***DATAO*** bus of the G-TAXI Dmx is connected to the input port of an asynchronous buffer (FIFO), the ***RDYO*** can be used to transfer ***DATAO*** into the buffer by connecting it to the ***STRBO*** input.

When the G-TAXI Dmx receives illegal code pattern (a pattern which cannot be legally decoded by an 8B/10B encoder), this is flagged by ***EX(4:0)*** = (11101) to indicate to the receiving host system that at least one byte in the word is a G-TAXI code violation. The receiving host system can examine these Exception conditions and request re-transmission.

When the G-TAXI Dmx detects running disparity violation condition, it will be flagged by ***EX(4:0)*** = (11110) to indicate to the receiving host system that a disparity violation had occurred. The receiving host system can examine these Exception conditions and request re-transmission. It is important to know that, unlike a coding violation, a running disparity violation is not always flagged at the time when the error occurs. (See Fiber Channel Overview for running disparity details).

Dmx Word Alignment

Proper word boundaries need to be (re)established for the byte-to-word conversion. This is automatically accomplished with the IDLE sequence which is transmitted by G-TAXI Tx subsystem in order to maintain an inactive link.

In 32-bit G-TAXI Mux/Tx subsystem, IDLE is defined to be (K28.5 D21.4 D21.5 D21.5). In 40-bit G-TAXI Mux/Tx subsystem, IDLE is defined to be (K28.5 K28.5 D21.5 D21.5 D21.5). A full IDLE word, however, is not necessary for output word alignment. The first K28.5 immediately after any 2 or more valid data becomes the first byte of the next word and is output on D(39:32) in 40 bit configuration or D(31:24) in 32 bit configuration.

When the first IDLE word is not byte-aligned, there may only be one DXX.X decoded. Consequently, the second IDLE word cannot establish word alignment. The next two DXX.X's will come through and word alignment will occur at the transition to the third IDLE word.

Mux Data Synchronization and Handshake

In a synchronous system where host data is synchronized to the G-TAXI operating rate, the STROBE function can be achieved with synchronous logic in the sending host. When the ***STRBI*** is synchronous with the ***TCLK*** rate, the highest sustaining data throughput can be reached (e.g. ***CLK45*** tied back to ***STRBI***).

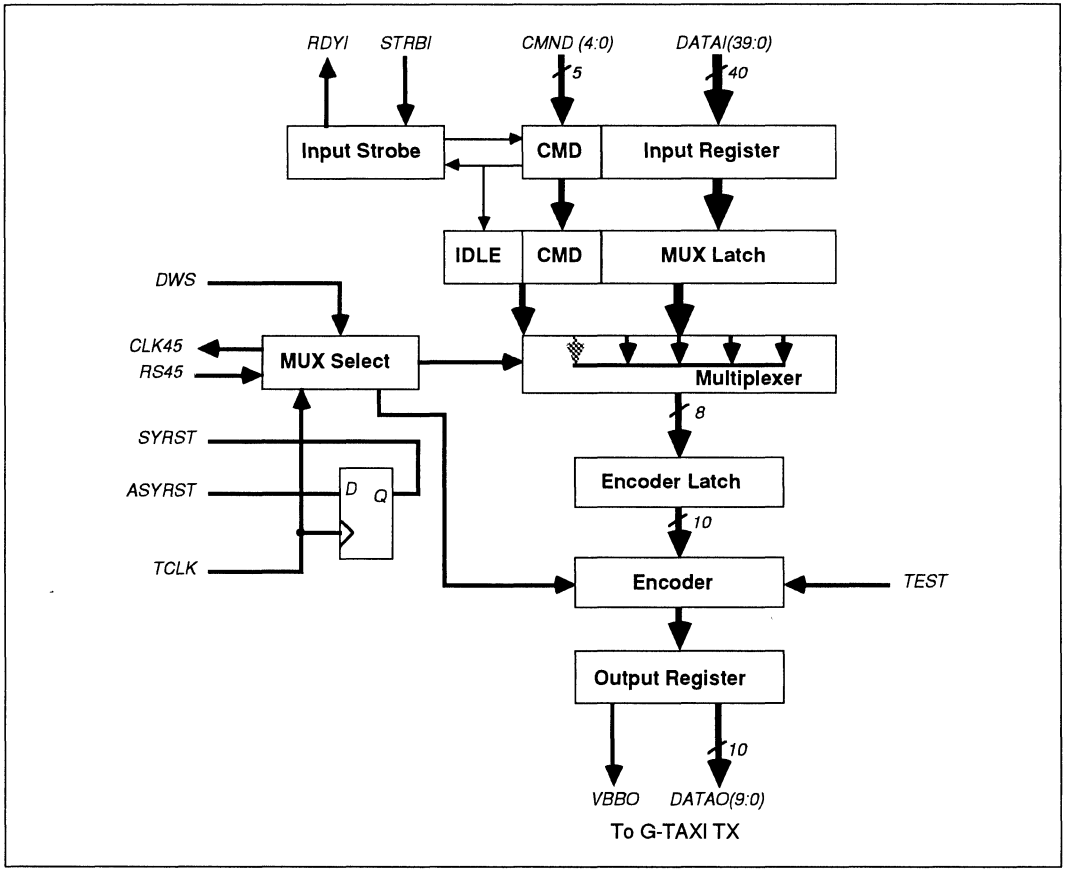
In systems where G-TAXI Mux inputs are strobed asynchronously with respect to the G-TAXI clock at ***TCLK*** pin, the ***RDYI*** signal must be used to determine the window for valid ***STRBI***. ***STRBI*** latches data into the INPUT REGISTER, and data transfer to the MULTIPLEXER LATCH will happen as it becomes empty. Data can be entered at rate which is less than the maximum transfer rate without regard to actual word boundaries.

Dmx Data Synchronization and Handshake

In general, buffers for received data are necessary if the host system cannot respond to the G-TAXI subsystem within single word cycle. The ***RDYO/STRBO*** handshake is compatible with most industry standard FIFOs for this purpose.

2

G-TAXI MUX (VSC7103) BLOCK DIAGRAM



G-TAXI MUX FUNCTIONAL DESCRIPTION

Input Register

DATAI(39:0) and ***CMND(4:0)*** inputs are latched into the INPUT REGISTER by an external ***STRBI*** signal. When empty, data is latched on the rising edge of ***STRBI*** (TTL Level).

Input Strobe Logic

When the INPUT REGISTER becomes empty, the ***RDYI*** is asserted and the next input ***STRBI*** will latch data into the INPUT REGISTER. However, if the previously latched data have not had time to be transferred to the MULTIPLEXER LATCH, then ***RDYI*** remains inactive and any ***STRBI*** input will be ignored.

Multiplexer Latch

Input to the MULTIPLEXER LATCH is clocked by an internal counter which is synchronous with the byte being sent out on to the G-TAXI Tx interface. Whenever a new output pattern is strobed into the ENCODER LATCH, the counter and Mux SELECT will be incremented. After four or five MULTIPLEXER transfers, the MULTIPLEXER LATCH is empty and ready to accept new data from the INPUT REGISTER.

Multiplexer

The MULTIPLEXER controls the sequence of the four or five bytes to be latched into the ENCODER LATCH. The MULTIPLEXER is controlled by the MUX SELECT logic.

Encoder Latch

The ENCODER LATCH is loaded from the MULTIPLEXER one byte at a time.

Encoder

Encodes the 8-bit data from the ENCODER LATCH according to the 8B/10B Encoding Table.

Mux Select Logic

Controls the sequence of the four or five bytes to be latched into the OUTPUT REGISTER. Also clears the MULTIPLEXER LATCH so that data from INPUT REGISTER could be transferred into MULTIPLEXER LATCH. The ***MUX SELECT LOGIC*** and ***DATA*** outputs are synchronous with ***TCLK*** (PECL Level). This block also generates ***CLK45*** from ***TCLK*** div-by-4 or div-by-5.

Output Register

The OUTPUT REGISTER is loaded from the ENCODER once every ***TCLK*** cycle, and then transferred to the outputs into a G-TAXI Tx (PECL Levels).

Multiple Mux Synchronization

The following signals are used to allow multiple Muxes to be synchronized with each other. A block diagram and timing diagram on pages 20-21 explains this configuration.

ASYRST *Asynchronous Reset (TTL Input)*

This input is used to reset the Muxes in multiple parallel Mux systems. Reset should only have to be performed during system initialization. In most applications, ASYRST can be hard-wired to GND. ASYRST is internally synchronized by ***TCLK***.

SYRST *Synchronized Reset (TTL Output)*

This output is the synchronized (by ***TCLK***) version of ASYRST. In multiple Mux systems, SYRST of one Mux should be connected to the ***RS45*** inputs of all Muxes in the system. This allows all Muxes to be reset from a common, synchronized source.

RS45 *Reset CLK45 (TTL Input)*

This input directly resets the internal MUX logic when it is HIGH. In multiple, parallel Mux systems it should be connected to the ***SYRST*** output of the MUX whose ***ASYRST*** input is being used. In most applications, ***RS45*** should be hard-wired to GND.

8B/10B CMND INPUT SPECIAL FUNCTION TABLE

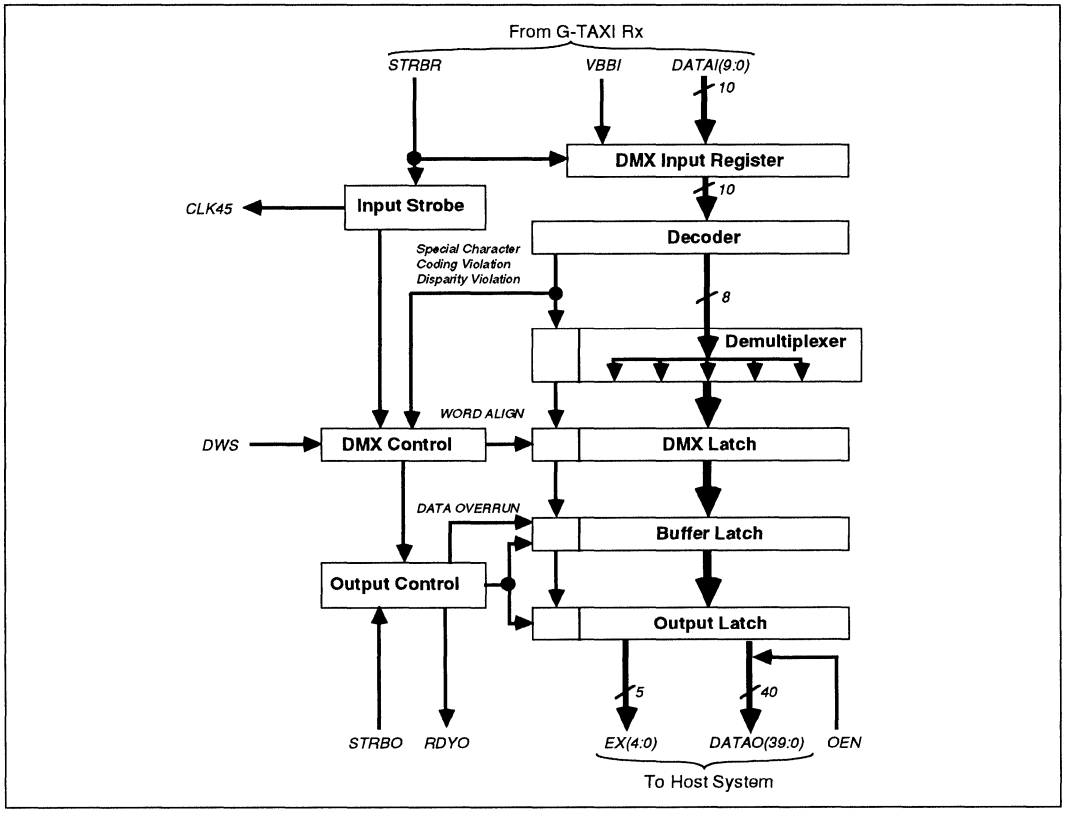
CMND		Bit Numbers				
43	210	39 – 32	31 – 24	23 – 16	15 – 8	7 – 0
00	000	(dataO)	data1	data2	data3	data4
00	001	(K28.5)	data1	data2	data3	data4
00	010	(K28.5)	K28.5	data2	data3	data4
00	011	(K28.5)	K28.5	K28.5	data3	data4
00	100	(K23.7)	K23.7	K23.7	data3	data4
00	101	(K27.7)	K27.7	K27.7	data3	data4
00	110	(K29.7)	K29.7	K29.7	data3	data4
00	111	(K30.7)	K30.7	K30.7	data3	data4
01	000	(K28.5)	K28.5	D10.4/5	D21.0	D21.0
01	001	(K28.5)	K28.5	D10.4/5	D21.1	D21.1
01	010	(K28.5)	K28.5	D10.4/5	D21.2	D21.2
01	011	(K28.5)	K28.5	D10.4/5	D21.3	D21.3
01	100	(K28.5)	K28.5	D10.4/5	D21.4	D21.4
01	101	(K28.5)	K28.5	D10.4/5	D21.5	D21.5
01	110	(K28.5)	K28.5	D10.4/5	D21.6	D21.6
01	111	(K28.5)	K28.5	D10.4/5	D21.7	D21.7
10	000	(K28.5)	K28.5	D21.4/5	D21.0	D21.0
10	001	(K28.5)	K28.5	D21.4/5	D21.1	D21.1
10	010	(K28.5)	K28.5	D21.4/5	D21.2	D21.2
10	011	(K28.5)	K28.5	D21.4/5	D21.3	D21.3
10	100	(K28.5)	K28.5	D21.4/5	D21.4	D21.4
10	101	(K28.5)	K28.5	D21.4/5	D21.5	D21.5*
10	110	(K28.5)	K28.5	D21.4/5	D21.6	D21.6
10	111	(K28.5)	K28.5	D21.4/5	D21.7	D21.7
11	000	(dataO)	data1	data2	data3	data4
11	001	(K28.5)	data1	data2	data3	data4
11	010	(K28.5)	K28.5	data2	data3	data4
11	011	(K28.5)	K28.5	K28.5	data3	data4
11	100	(K23.7)	K23.7	K23.7	data3	data4
11	101	(K27.7)	K27.7	K27.7	data3	data4
11	110	(K29.7)	K29.7	K29.7	data3	data4
11	111	(K30.7)	K30.7	K30.7	data3	data4

*Idle pattern.

NOTES:

1. *This table contains two identical sections, where CMND = (00xxx) and CMND=(11xxx). The G-TAXI Dmx decoder block which corresponds to CMND=(11xxx) is used for error reporting.*
2. *IDLE pattern can be generated automatically when STRBI becomes inactive. IDLE=K28.5 D21.4 D21.5 D21.5 in 32-bit mode and IDLE= K28.5 K28.5 D21.5 D21.5 D21.5 in 40-bit mode.*
3. *D10.4/5: always D10.5 when in 40-bit mode. When in 32-bit mode, the choice between D10.4 and D10.5 is made such that the disparity after this character will be negative.*
4. *D21.4/5: Always D21.5 when in 40-bit mode. When in 32-bit mode, the choice between D21.4 and D21.5 is made such that the disparity after this character will be negative.*

G-TAXI DMX (VSC7104) BLOCK DIAGRAM



G-TAXI DMX FUNCTIONAL DESCRIPTION

Input Register

DATAI(9:0) are latched into the INPUT REGISTER by the external ***STRBR*** signal on its rising edge.

Input Strobe Logic

When the ***STRBR*** signal goes active, the inputs at ***DATAI(9:0)*** are latched into the INPUT REGISTER. This logic also increments the DEMUX CONTROL counter.

Decoder

The DECODER converts the 10-bit input code into an 8-bit data byte.

Demultiplexer

DEMULTIPLEXER is controlled by the DEMUX CONTROL logic to perform 1-to-4 or 1-to-5 demultiplexing function from the DECODER into the DEMULTIPLEXER LATCH.

Demux Control Logic

Control the sequence of the four or five bytes to be latched into the DEMUX LATCH. Also signals the OUTPUT CONTROL logic so that the transfer from DEMUX LATCH to the BUFFER LATCH will happen at the earliest possible time.

Demultiplexer Latch

Whenever a new data pattern is strobed into the INPUT REGISTER, the counter in the DEMUX CONTROL is incremented and directs the DEMULTIPLEXER to the next available byte position in the DEMUX LATCH. After four or five DEMULTIPLEXER transfers, the DEMULTIPLEXER LATCH is full and will transfer its content to the BUFFER LATCH.

Buffer Latch

When the MULTIPLEXER LATCH accumulates a full word, it is transferred to the BUFFER LATCH immediately so the DEMULTIPLEXER LATCH can be ready for the next byte. If the transfer into BUFFER LATCH occurs before the previous word is sent to OUTPUT LATCH, then the error condition "data overrun" occurs and the previous word is overwritten and lost.

Output Latch

The OUTPUT LATCH is loaded from the BUFFER LATCH after an active ***STRBO*** edge.

Output Control

The ***RDYO*** is asserted when a full word is latched into the OUTPUT LATCH. ***STRBO*** input will clear ***RDYO*** and enable the next word transfer into the OUTPUT LATCH. An active ***STRBO*** without a previous ***RDYO*** is ignored by OUTPUT CONTROL logic.

FIBER CHANNEL OVERVIEW

The Fiber Channel provides a transport vehicle for the upper layer Intelligent Peripheral Interface (IPI) and Small Computer System Interface (SCSI) command sets, the High Performance Parallel Interface (HIPPI) data link layer, and other user-defined command sets. The Fiber Channel is capable of replacing the SCSI, IPI, and HIPPI physical interfaces with a protocol-efficient alternative that provides performance improvements in distance and/or speed. The maximum fiber channel serial link rate of 1.0625 Gbps is supported by the G-TAXI system.

IPI commands, SCSI commands, and HIPPI data link operations may all be intermixed on the Fiber Channel. Proprietary and other command sets may also use and share the Fiber Channel. Such usage is defined outside the standard.

The Fiber Channel is optimized for predictable transfers of large blocks of data such as those used in file transfers between processors (super, mainframe, super-mini, etc.), storage systems (disk and tape), communications, and output-only devices such as laser printers and raster scan graphics terminals.

The Fiber Channel standards are organized into four documents as follows:

- FC-3 is the highest layer in the Fiber Channel standards set. It defines the channel protocol, or mapping, between the lower layer FC standards and the IPI and SCSI command sets, applications which use the HIPPI data link layer, and other user-defined command sets.
- FC-2 defines the signalling protocol which includes the frame structure and byte sequences.
- FC 1 defines the transmission protocol, which includes the serial encoding and decoding rules, special characters, and error control.
- FC-O defines the physical portions of the Fiber Channel including the Fiber, connectors, and optical parameters for a variety of data rates. A serial copper version Is also discussed for limited distance applications.

The Fiber Channel protocol is simple in order to minimize implementation cost and enhance throughput. The transmission medium is isolated from the control protocol so that implementation of point-to-point links, multi-drop buses, rings, crosspoint switches, or other special implementations may be made in a technology best suited to the usage environment.

Transmission Order

Within the definition of the 8B/10B transmission code, the bit positions of the transmission characters are labeled a, b, c, d, e, i, f, g, h, and j. Bit "a" is transmitted first followed by bits "b," "c," "d," "e," "i," "f," "g," "h," and "j," in that order. (Note that bit "i" is transmitted between bit "e" and bit "f," rather than in the order that would be indicated by the letters of the alphabet.)

Characters within ordered sets (as specified in the section entitled "Special Functions") are transmitted sequentially beginning with the special character used to distinguish the ordered set (e.g., K28.5) and proceeding character by character from left to right within the definition of the ordered set until all characters of the ordered set are transmitted.

The contents of a frame (as specified by FC-2) are transmitted sequentially beginning with the ordered set used to denote the start of frame (the SOF delimiter) and proceeding character by character from left to right within the definition of the frame until the ordered set used to denote the end of frame (the EOF delimiter) is transmitted.

Valid and Invalid Transmission Characters

Valid data characters and valid special characters (K characters)are defined in the tables on pages 13-15. The tables are used for both generating valid transmission characters (encoding) and checking the validity of received transmission characters (decoding). In the tables, each data-byte or special-code entry has two columns that represent two (not necessarily different) transmission characters. The two columns correspond to the current value of the running disparity ("Current RD —" or "Current RD +"). Running disparity is a binary parameter with either the value negative (-) or the value positive (+).

The purpose of running disparity is to assure that, in the long run, just as many "zeros" have been transmitted as "ones". Data is periodically inverted based on the running disparity value to assure that condition.

After powering on, the transmitter assumes either a negative or positive value for its initial running disparity. Upon transmission of any transmission character, the transmitter calculates a new value for its running disparity based on the contents of the transmitted character.

After powering on, the receiver assumes either a negative or positive value for its initial running disparity. Upon reception of any transmission character, the receiver determines whether the transmission character is valid or invalid and calculates a new value for its running disparity based on the contents of the received character.

If the received character and subsequent characters were transmitted assuming the opposite starting running disparity, a running disparity violation will be reported and can be ignored. This violation is, of course, a product of chip initialization on power up and will disappear after a new correctly encoded character is received.

The following rules for running disparity are used to calculate the new running disparity value for transmission characters that have been transmitted (transmitter's running disparity) and that have been received (receiver's running disparity).

Running disparity for a transmission character is calculated on the basis of sub-blocks, where the first six bits (abcdei) form one sub-block (six-bit sub-block) and the second four bits (fghj) form the other sub-block (four-bit sub block). Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the last transmission character. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the beginning of the transmission character is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-block is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at

the end of the six-bit sub-block if the six-bit subblock is 000111 and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011

2. Running disparity at the end of any sub-block is negative if the sub-block contains more zero than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table is found for the data byte or the special code for which a transmission character is to be generated (encoded). The current value of the transmitter's running disparity is used to select the transmission character from its corresponding column. For each transmission character transmitted a new value of the running disparity is calculated. This new value is used as the transmitter's current running disparity for the next data byte or special code to be encoded and transmitted.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the receiver's running disparity is searched for the received transmission character. If the received transmission character is found in the proper column, then the transmission character is valid and the associated data byte or special code is determined (decoded). If the received transmission character is not found in that column, then the transmission character is a running disparity. If the character is then not located in the opposite column it is referred to as a code violation. Independent of the transmission character's validity, the received transmission character is used to calculate a new value of running disparity. The new value is used as the receiver's current running disparity for the next received transmission character.

VALID SPECIAL CHARACTERS

Special	Current RD -		Current RD +		
Code Name	HGF	EDCBA	abcdei	fghj	Conditions
K28.0	001111	0100	110000	1011	Reserved*
K28.1	001111	1001	110000	0110	Reserved*
K28.2	001111	0101	110000	1010	Reserved*
K28.3	001111	0011	110000	1100	Reserved*
K28.4	001111	0010	110000	1101	Reserved*
K28.5	001111	1010	110000	0101	Sync
K28.6	001111	0110	110000	1001	Reserved*
K28.7	001111	1000	110000	0111	Reserved*
K23.7	111010	1000	000101	0111	Reserved*
K27.7	110110	1000	001001	0111	Reserved*
K29.7	101110	1000	010001	0111	Reserved*
K30.7	011110	1000	100001	0111	Reserved*

Reserved - Valid transmission characters which are not defined for use by this standard.

VALID DATA CHARACTERS

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.0	000	000000	100111	0100	011000	1011
D1.0	000	000001	011101	0100	100010	1011
D2.0	000	000010	101101	0100	010010	1011
D3.0	000	000011	110001	1011	110001	0100
D4.0	000	000100	110101	0100	001010	1011
D5.0	000	000101	101001	1011	101001	0100
D6.0	000	000110	011001	1011	011001	0100
D7.0	000	000111	111000	1011	000111	0100
D8.0	000	001000	111001	0100	000110	1011
D9.0	000	001001	100101	1011	100101	0100
D10.0	000	001010	010101	1011	010101	0100
D11.0	000	001011	110100	1011	110100	0100
D12.0	000	001100	001101	1011	001101	0100
D13.0	000	001101	101100	1011	101100	0100
D14.0	000	001110	011100	1011	011100	0100
D15.0	000	001111	010111	0100	101000	1011
D16.0	000	010000	011011	0100	100100	1011
D17.0	000	010001	100011	1011	100011	0100
D18.0	000	010010	010011	1011	010011	0100
D19.0	000	010011	110010	1011	110010	0100
D20.0	000	010100	001011	1011	001011	0100
D21.0	000	010101	101010	1011	101010	0100
D22.0	000	010110	011010	1011	011010	0100
D23.0	000	010111	111010	0100	000101	1011
D24.0	000	011000	110011	0100	001100	1011
D25.0	000	011001	100110	1011	100110	0100
D26.0	000	011010	010110	1011	010110	0100
D27.0	000	011011	110110	0100	001001	1011
D28.0	000	011100	001110	1011	001110	0100
D29.0	000	011101	101110	0100	010001	1011
D30.0	000	011110	011110	0100	100001	1011
D31.0	000	011111	101011	0100	010100	1011

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.2	010	000000	100111	0101	011000	0101
D1.2	010	000001	011101	0101	100010	0101
D2.2	010	000010	101101	0101	010010	0101
D3.2	010	000011	110001	0101	110001	0101
D4.2	010	000100	110101	0101	001010	0101
D5.2	010	000101	101001	0101	101001	0101
D6.2	010	000110	011001	0101	011001	0101
D7.2	010	000111	111000	0101	000111	0101
D8.2	010	001000	111001	0101	000110	0101
D9.2	010	001001	100101	0101	100101	0101
D10.2	010	001010	010101	0101	010101	0101
D11.2	010	001011	110100	0101	110100	0101
D12.2	010	001100	001101	0101	001101	0101
D13.2	010	001101	101100	0101	101100	0101
D14.2	010	001110	011100	0101	011100	0101
D15.2	010	001111	010111	0101	101000	0101
D16.2	010	010000	011011	0101	100100	0101
D17.2	010	010001	100011	0101	100011	0101
D18.2	010	010010	010011	0101	010011	0101
D19.2	010	010011	110010	0101	110010	0101
D20.2	010	010100	001011	0101	001011	0101
D21.2	010	010101	101010	0101	101010	0101
D22.2	010	010110	011010	0101	011010	0101
D23.2	010	010111	111010	0101	000101	0101
D24.2	010	011000	110011	0101	001100	0101
D25.2	010	011001	100110	0101	100110	0101
D26.2	010	011010	010110	0101	010110	0101
D27.2	010	011011	110110	0101	001001	0101
D28.2	010	011100	001110	0101	001110	0101
D29.2	010	011101	101110	0101	010001	0101
D30.2	010	011110	011110	0101	100001	0101
D31.2	010	011111	101011	0101	010100	0101

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.1	001	000000	100111	1001	011000	1001
D1.1	001	000001	011101	1001	100010	1001
D2.1	001	000010	101101	1001	010010	1001
D3.1	001	000011	110001	1001	110001	1001
D4.1	001	000100	110101	1001	001010	1001
D5.1	001	000101	101001	1001	101001	1001
D6.1	001	000110	011001	1001	011001	1001
D7.1	001	000111	111000	1001	000111	1001
D8.1	001	001000	111001	1001	000110	1001
D9.1	001	001001	100101	1001	100101	1001
D10.1	001	001010	010101	1001	010101	1001
D11.1	001	001011	110100	1001	110100	1001
D12.1	001	001100	001101	1001	001101	1001
D13.1	001	001101	101100	1001	101100	1001
D14.1	001	001110	011100	1001	011100	1001
D15.1	001	001111	010111	1001	101000	1001
D16.1	001	010000	011011	1001	100100	1001
D17.1	001	010001	100011	1001	100011	1001
D18.1	001	010010	010011	1001	010011	1001
D19.1	001	010011	110010	1001	110010	1001
D20.1	001	010100	001011	1001	001011	1001
D21.1	001	010101	101010	1001	101010	1001
D22.1	001	010110	011010	1001	011010	1001
D23.1	001	010111	111010	1001	000101	1001
D24.1	001	011000	110011	1001	001100	1001
D25.1	001	011001	100110	1001	100110	1001
D26.1	001	011010	010110	1001	010110	1001
D27.1	001	011011	110110	1001	001001	1001
D28.1	001	011100	001110	1001	001110	1001
D29.1	001	011101	101110	1001	010001	1001
D30.1	001	011110	011110	1001	100001	1001
D31.1	001	011111	101011	1001	010100	1001

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.4	100	000000	100111	0010	011000	1101
D1.4	100	000001	011101	0010	100010	1101
D2.4	100	000010	101101	0010	010010	1101
D3.4	100	000011	110001	1101	110001	0010
D4.4	100	000100	110101	0010	001010	1101
D5.4	100	000101	101001	1101	101001	0010
D6.4	100	000110	011001	1101	011001	0010
D7.4	100	000111	111000	1101	000111	0010
D8.4	100	001000	111001	0010	000110	1101
D9.4	100	001001	100101	1101	100101	0010
D10.4	100	001010	010101	1101	010101	0010
D11.4	100	001011	110100	1101	110100	0010
D12.4	100	001100	001101	1101	001101	0010
D13.4	100	001101	101100	1101	101100	0010
D14.4	100	001110	011100	1101	011100	0010
D15.4	100	001111	010111	0010	101000	1101
D16.4	100	010000	011011	0010	100100	1101
D17.4	100	010001	100011	1101	100011	0010
D18.4	100	010010	010011	1101	010011	0010
D19.4	100	010011	110010	1101	110010	0010
D20.4	100	010100	001011	1101	001011	0010
D21.4	100	010101	101010	1101	101010	0010
D22.4	100	010110	011010	1101	011010	0010
D23.4	100	010111	111010	0010	000101	1101
D24.4	100	011000	110011	0010	001100	1101
D25.4	100	011001	100110	1101	100110	0010
D26.4	100	011010	010110	1101	010110	0010
D27.4	100	011011	110110	0010	001001	1101
D28.4	100	011100	001110	1101	001110	0010
D29.4	100	011101	101110	0010	010001	1101
D30.4	100	011110	011110	0010	100001	1101
D31.4	100	011111	101011	0010	010100	1101

VALID DATA CHARACTERS

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.3	011	000000	100111	0011	011000	1100
D1.3	011	000001	011101	0011	100010	1100
D2.3	011	000010	101101	0011	010010	1100
D3.3	011	000011	110001	1100	110001	0011
D4.3	011	000100	110101	0011	001010	1100
D5.3	011	000101	101001	1100	101001	0011
D6.3	011	000110	011001	1100	011001	0011
D7.3	011	000111	111000	1100	000111	0011
D8.3	011	001000	111001	0011	000110	1100
D9.3	011	001001	100101	1100	100101	0011
D10.3	011	001010	010101	1100	010101	0011
D11.3	011	001011	110100	1100	110100	0011
D12.3	011	001100	001101	1100	001101	0011
D13.3	011	001101	101100	1100	101100	0011
D14.3	011	001110	011100	1100	011100	0011
D15.3	011	001111	010111	0011	101000	1100
D16.3	011	010000	011011	0011	100100	1100
D17.3	011	010001	100011	1100	100011	0011
D18.3	011	010010	010011	1100	010011	0011
D19.3	011	010011	110010	1100	110010	0011
D20.3	011	010100	001011	1100	001011	0011
D21.3	011	010101	101010	1100	101010	0011
D22.3	011	010110	011010	1100	011010	0011
D23.3	011	010111	111010	0011	000101	1100
D24.3	011	011000	110011	0011	001100	1100
D25.3	011	011001	100110	1100	100110	0011
D26.3	011	011010	010110	1100	010110	0011
D27.3	011	011011	110110	0011	001001	1100
D28.3	011	011100	001110	1100	001110	0011
D29.3	011	011101	101110	0011	010001	1100
D30.3	011	011110	011110	0011	100001	1100
D31.3	011	011111	101011	0011	010100	1100

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.6	110	000000	100111	0110	011000	0110
D1.6	110	000001	011101	0110	100010	0110
D2.6	110	000010	101101	0110	010010	0110
D3.6	110	000011	110001	0110	110001	0110
D4.6	110	000100	110101	0110	001010	0110
D5.6	110	000101	101001	0110	101001	0110
D6.6	110	000110	011001	0110	011001	0110
D7.6	110	000111	111000	0110	000111	0110
D8.6	110	001000	111001	0110	000110	0110
D9.6	110	001001	100101	0110	100101	0110
D10.6	110	001010	010101	0110	010101	0110
D11.6	110	001011	110100	0110	110100	0110
D12.6	110	001100	001101	0110	001101	0110
D13.6	110	001101	101100	0110	101100	0110
D14.6	110	001110	011100	0110	011100	0110
D15.6	110	001111	010111	0110	101000	0110
D16.6	110	010000	011011	0110	100100	0110
D17.6	110	010001	100011	0110	100011	0110
D18.6	110	010010	010011	0110	010011	0110
D19.6	110	010011	110010	0110	110010	0110
D20.6	110	010100	001011	0110	001011	0110
D21.6	110	010101	101010	0110	101010	0110
D22.6	110	010110	011010	0110	011010	0110
D23.6	110	010111	111010	0110	000101	0110
D24.6	110	011000	110011	0110	001100	0110
D25.6	110	011001	100110	0110	100110	0110
D26.6	110	011010	010110	0110	010110	0110
D27.6	110	011011	110110	0110	001001	0110
D28.6	110	011100	001110	0110	001110	0110
D29.6	110	011101	101110	0110	010001	0110
D30.6	110	011110	011110	0110	100001	0110
D31.6	110	011111	101011	0110	010100	0110

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.5	101	000000	100111	1010	011000	1010
D1.5	101	000001	011101	1010	100010	1010
D2.5	101	000010	101101	1010	010010	1010
D3.5	101	000011	110001	1010	110001	1010
D4.5	101	000100	110101	1010	001010	1010
D5.5	101	000101	101001	1010	101001	1010
D6.5	101	000110	011001	1010	011001	1010
D7.5	101	000111	111000	1010	000111	1010
D8.5	101	001000	111001	1010	000110	1010
D9.5	101	001001	100101	1010	100101	1010
D10.5	101	001010	010101	1010	010101	1010
D11.5	101	001011	110100	1010	110100	1010
D12.5	101	001100	001101	1010	001101	1010
D13.5	101	001101	101100	1010	101100	1010
D14.5	101	001110	011100	1010	011100	1010
D15.5	101	001111	010111	1010	101000	1010
D16.5	101	010000	011011	1010	100100	1010
D17.5	101	010001	100011	1010	100011	1010
D18.5	101	010010	010011	1010	010011	1010
D19.5	101	010011	110010	1010	110010	1010
D20.5	101	010100	001011	1010	001011	1010
D21.5	101	010101	101010	1010	101010	1010
D22.5	101	010110	011010	1010	011010	1010
D23.5	101	010111	111010	1010	000101	1010
D24.5	101	011000	110011	1010	001100	1010
D25.5	101	011001	100110	1010	100110	1010
D26.5	101	011010	010110	1010	010110	1010
D27.5	101	011011	110110	1010	001001	1010
D28.5	101	011100	001110	1010	001110	1010
D29.5	101	011101	101110	1010	010001	1010
D30.5	101	011110	011110	1010	100001	1010
D31.5	101	011111	101011	1010	010100	1010

Data Byte	Data Bits		Current RD -		Current RD +	
Name	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.7	111	000000	100111	0001	011000	1110
D1.7	111	000001	011101	0001	100010	1110
D2.7	111	000010	101101	0001	010010	1110
D3.7	111	000011	110001	1110	110001	0001
D4.7	111	000100	110101	0001	001010	1110
D5.7	111	000101	101001	1110	101001	0001
D6.7	111	000110	011001	1110	011001	0001
D7.7	111	000111	111000	1110	000111	0001
D8.7	111	001000	111001	0001	000110	1110
D9.7	111	001001	100101	1110	100101	0001
D10.7	111	001010	010101	1110	010101	0001
D11.7	111	001011	110100	1110	110100	1000
D12.7	111	001100	001101	1110	001101	0001
D13.7	111	001101	101100	1110	101100	1000
D14.7	111	001110	011100	1110	011100	1000
D15.7	111	001111	010111	0001	101000	1110
D16.7	111	010000	011011	0001	100100	1110
D17.7	111	010001	100011	0111	100011	0001
D18.7	111	010010	010011	0111	010011	0001
D19.7	111	010011	110010	1110	110010	0001
D20.7	111	010100	001011	0111	001011	0001
D21.7	111	010101	101010	1110	101010	0001
D22.7	111	010110	011010	1110	011010	0001
D23.7	111	010111	111010	0001	000101	1110
D24.7	111	011000	110011	0001	001100	1110
D25.7	111	011001	100110	1110	100110	0001
D26.7	111	011010	010110	1110	010110	0001
D27.7	111	011011	110110	0001	001001	1110
D28.7	111	011100	001110	1110	001110	0001
D29.7	111	011101	101110	0001	010001	1110
D30.7	111	011110	011110	0001	100001	1110
D31.7	111	011111	101011	0001	010100	1110

EXception

*Priority**	*EXception: 4,3,2,1,0*	*Received and Demultiplexed Data*				
	00000	(data0)	data1	data2	data3	data4
	00001	(K28.5)	data1	data2	data3	data4
	00010	(K28.5)	K28.5	data2	data3	data4
	00011	(K28.5)	K28.5	K28.5	data3	data4
	00100	(K23.7)	K23.7	K23.7	data3	data4
	00101	(K27.7)	K27.7	K27.7	data3	data4
	00110	(K29.7)	K29.7	K29.7	data3	data4
	00111	(K30.7)	K30.7	K30.7	data3	data4
	01000	(K28.5)	K28.5	D10.4/5	D21.0	D21.0
	01001	(K28.5)	K28.5	D10.4/5	D21.1	D21.1
	01010	(K28.5)	K28.5	D10.4/5	D21.2	D21.2
	01011	(K28.5)	K28.5	D10.4/5	D21.3	D21.3
	01100	(K28.5)	K28.5	D10.4/5	D21.4	D21.4
	01101	(K28.5)	K28.5	D10.4/5	D21.5	D21.5
	01110	(K28.5)	K28.5	D10.4/5	D21.6	D21.6
	01111	(K28.5)	K28.5	D10.4/5	D21.7	D21.7
	10000	(K28.5)	K28.5	D21.4/5	D21.0	D21.0
	10001	(K28.5)	K28.5	D21.4/5	D21.1	D21.1
	10010	(K28.5)	K28.5	D21.4/5	D21.2	D21.2
	10011	(K28.5)	K28.5	D21.4/5	D21.3	D21.3
	10100	(K28.5)	K28.5	D21.4/5	D21.4	D21.4
	10101	(K28.5)	K28.5	D21.4/5	D21.5	D21.5**
	10110	(K28.5)	K28.5	D21.4/5	D21.6	D21.6
	10111	(K28.5)	K28.5	D21.4/5	D21.7	D21.7
	11000	Reserved				
	11001	Reserved				
3	11010	Data overrun, lack of STROBE_OUT				
6	11011	Partial word caused by new alignment				
5	11100	Out of place K-character detected				
2	11101	Word containing TAXI code violation(s), immediate error				
4	11110	Running disparity violation, non-immediate error				
1	11111	Both running disparity and coding violation				

**Priority required when more than one EXception condition occurs in the same byte.*
***Idle pattern.*
Data enclosed in () are disabled in 32-bit mode.

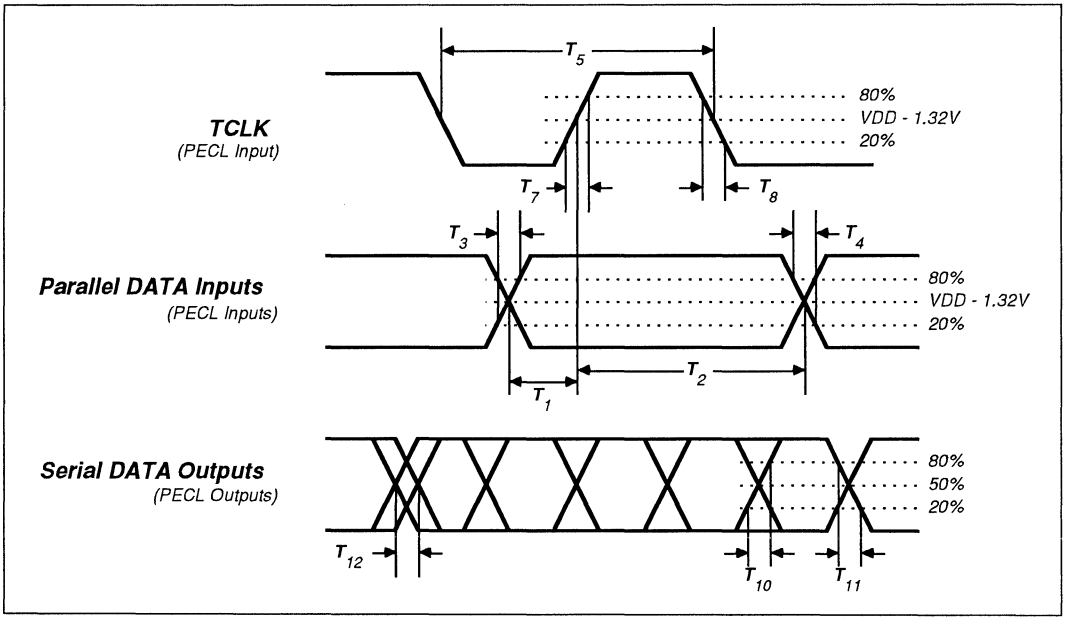
G-TAXI TX AC CHARACTERISTICS

(Guaranteed over recommended operating conditions).

Parameter	Description	Min	Typ	Max	Units	Conditions
T_1	Parallel Input Data Setup Time	1.0	—	—	ns	Measured in test mode
T_2	Parallel Input Data Hold Time	2.0	—	—	ns	Measured in test mode
T_3	Parallel Input Data Rise Time	—	—	2.0	ns	Test condition (a)
T_4	Parallel Input Data Fall Time	—	—	2.0	ns	Test condition (a)
T_5	TCLK Pulse Duty Cycle	40	—	60	%	V_{DD} - 1.32V
T_7	TCLK Pulse Rise Time	—	—	2.0	ns	Test condition (a)
T_8	TCLK Pulse Fall Time	—	—	2.0	ns	Test condition (a)
T_{10}	Serial Data Output Rise Time	—	—	300	ps	Test conditions (a), (b)
T_{11}	Serial Data Output Fall Time	—	—	300	ps	Test conditions (a), (b)
T_{12}	Serial Data Output Random Jitter (RMS)	—	—	20	ps	—
T_{12}	Serial Data Output Deterministic Jitter (Peak to Peak)	—	—	100	ps	—

Test conditions: a) 20%/80% for all PECL rise/fall measurements.
b) Load 2 = PECL load, 15 pF to ground 50Ω to V_{DD} - 2V.

GTAXI TX TIMING WAVEFORMS



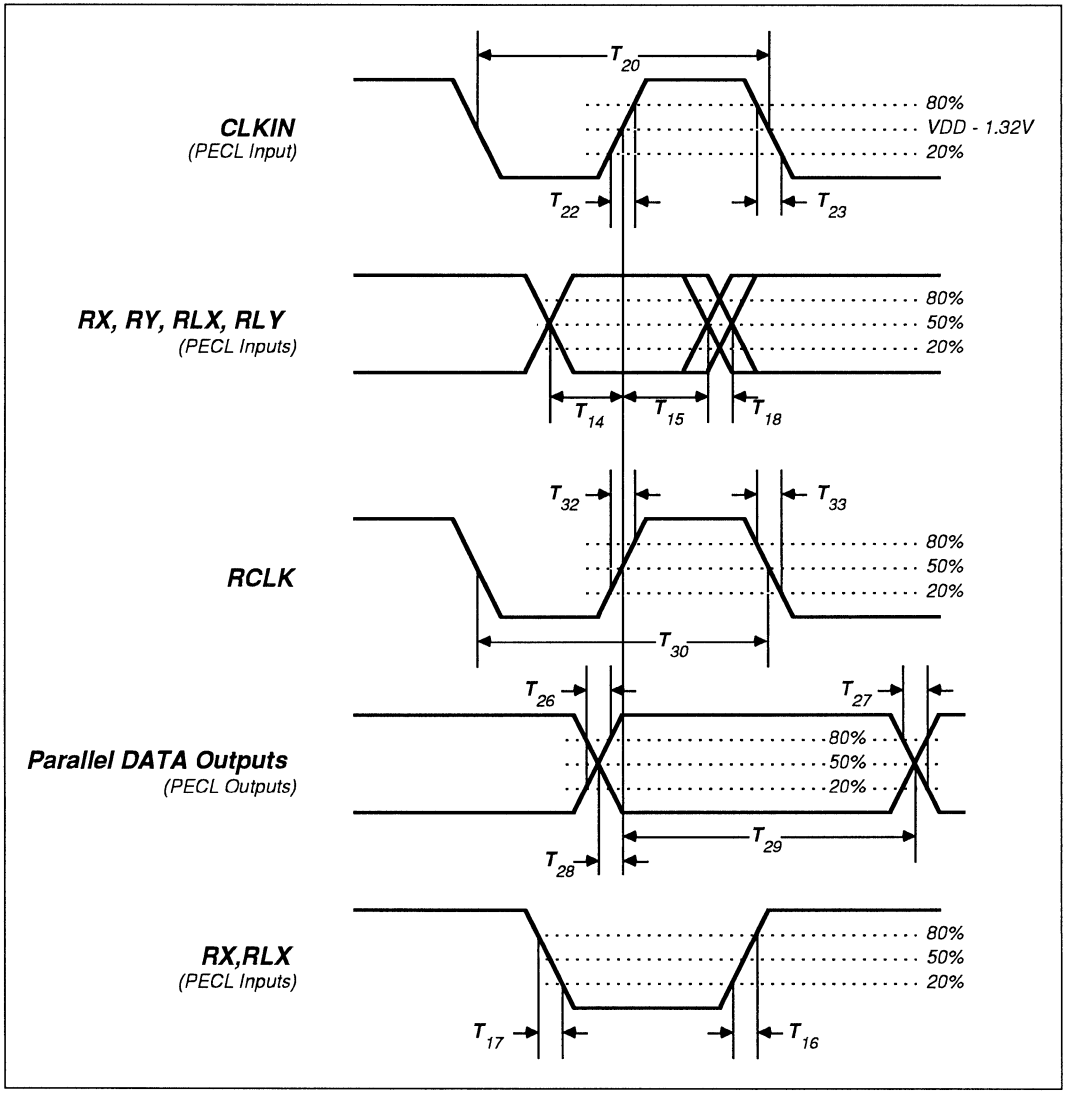
G-TAXI RX AC CHARACTERISTICS

(Guaranteed over recommended operating conditions).

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{14}	Serial Input Data Setup Time	1.0	—	—	ns	If PLL is bypassed
T_{15}	Serial Input Data Hold Time	2.0	—	—	ns	
T_{16}	Serial Input Data Rise Time	—	—	300	ps	Test condition (a)
T_{17}	Serial Input Data Fall Time	—	—	300	ps	Test condition (a)
T_{18}	Serial Data Input Random Jitter	—	—	TBD	ps	BER = 10^{-12}
T_{18}	Serial Data Input Deterministic Jitter (Peak to Peak)	—	—	TBD	ps	BER = 10^{-12}
T_{20}	CLK Pulse Duty Cycle	40	—	60	%	V_{DD} - 1.32V
T_{22}	CLK Pulse Rise Time	—	—	2.0	ns	—
T_{23}	CLK Pulse Fall Time	—	—	2.0	ns	—
—	Data Input and CLK Offset Freq.	—	—	0.1	%	f = 125 MHz or 106.25 MHz
T_{25}	Synchronization Time	—	—	100	µs	—
T_{26}	Parallel Data Output Rise Time	—	—	2.0	ns	Test conditions (a), (b)
T_{27}	Parallel Data Output Fall Time	—	—	2.0	ns	Test conditions (a), (b)
T_{28}	Data Valid to RCLK Rise	—	0	—	ns	Test condition (b)
T_{29}	Data Hold from RCLK Rise	4.0	—	—	ns	Test condition (b)
T_{30}	RCLK Pulse Duty Cycle	40	—	60	%	Test condition (b)
T_{32}	RCLK Pulse Rise Time	—	—	2.0	ns	Test conditions (a), (b)
T_{33}	RCLK Pulse Fall Time	—	—	2.0	ns	Test conditions (a), (b)

Test conditions: *(a) Measured at 20%/80%*
(b) Load 2 = PECL 15 pF to ground, 50Ω to V_{DD} - 2V.

G-TAXI RX TIMING WAVEFORMS



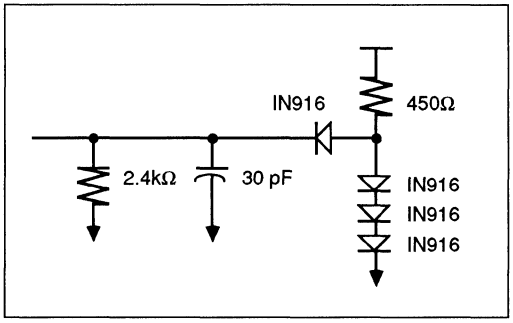
G-TAXI MUX AC CHARACTERISTICS

(Guaranteed over recommended operating conditions).

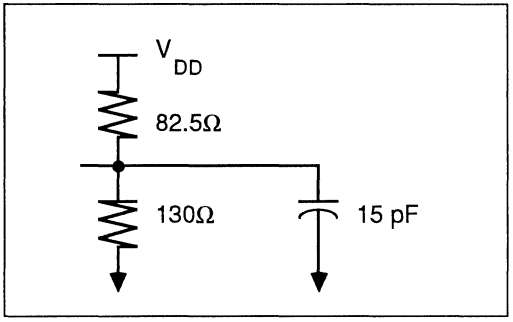
Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_1	TCLK Duty Cycle	40	—	60	%	V_{DD} - 1.32 V
T_2	TCLK Pulse Rise Time	—	—	2	ns	Test condition (a)
T_3	TCLK Pulse Fall Time	—	—	2	ns	Test condition (a)
T_4	TCLK to CLK45	—	8	—	ns	Test condition (b)
T_5	CLK45 Period	—	T_1xN	—	ns	M = 2 or 3 as determined by DWS input N = 4 or 5 as determined by DWS input
T_6	CLK45 Clock HIGH	—	T_1x2	—	ns	
T_7	CLK45 Clock LOW	—	T_1xM	—	ns	
T_8	STRBI Period	—	T_1xN	—	ns	
T_9	DATAI – STRBI T_{setup}	—	0	—	ns	DATAI = DATAI(39:0) and COMMAND(4:0) or DATAI(31:0) and COMMAND(4:0)
T_{10}	DATAI – STRBI T_{hold}	—	4	—	ns	
T_{11}	RDYI to STRBI Setup	—	0	—	ns	—
T_{12}	STRBI Rise to RDYI Fall	—	5	—	ns	Test condition (b)
T_{13}	STRBI Pulse Width HIGH	—	5	—	ns	Test condition (b)
T_{14}	RDYI Pulse Width LOW	—	15	—	ns	Test condition (b)
T_{16}	RDYI Rise Time	—	5	—	ns	Test condition (b)
T_{17}	RDYI Fall Time	—	5	—	ns	Test condition (b)
T_{16}	CLK45 Rise Time	—	5	—	ns	Test condition (b)
T_{17}	CLK45 Fall Time	—	5	—	ns	Test condition (b)
PECL Outputs:						
T_{20}	TCLK to DATAO Delay	—	5	—	ns	Test condition (c)
T_{23}	DATAO Output Rise Time	—	1	—	ns	Test condition (c)
T_{24}	DATAO Output Fall Time	—	1	—	ns	Test condition (c)

Test conditions: *(a) Measured at 20%/80%*
(b) Load 1 = TTL 30 pF to ground
(c) Load 2 = PECL 15 pF to ground, 50Ω to V_{DD} - 2V

Load 1 Used for TTL Outputs

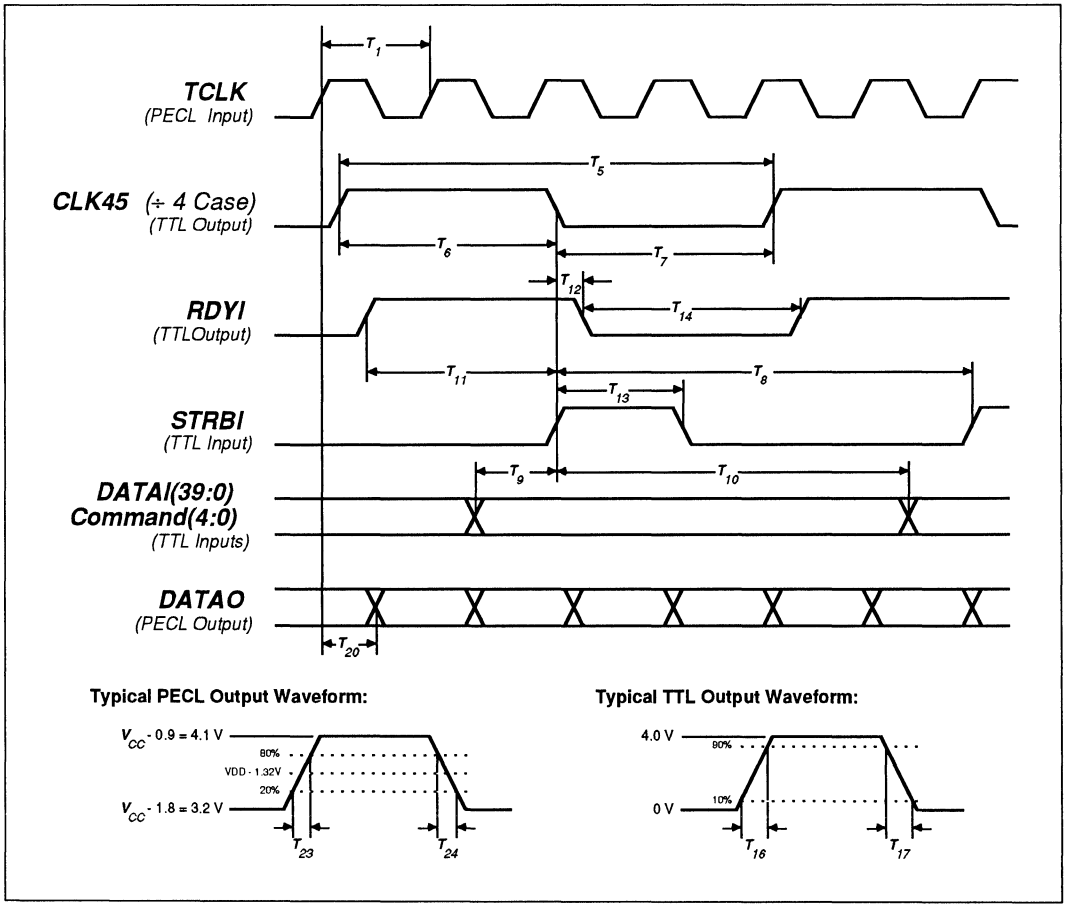


Load 2 Used for PECL Outputs

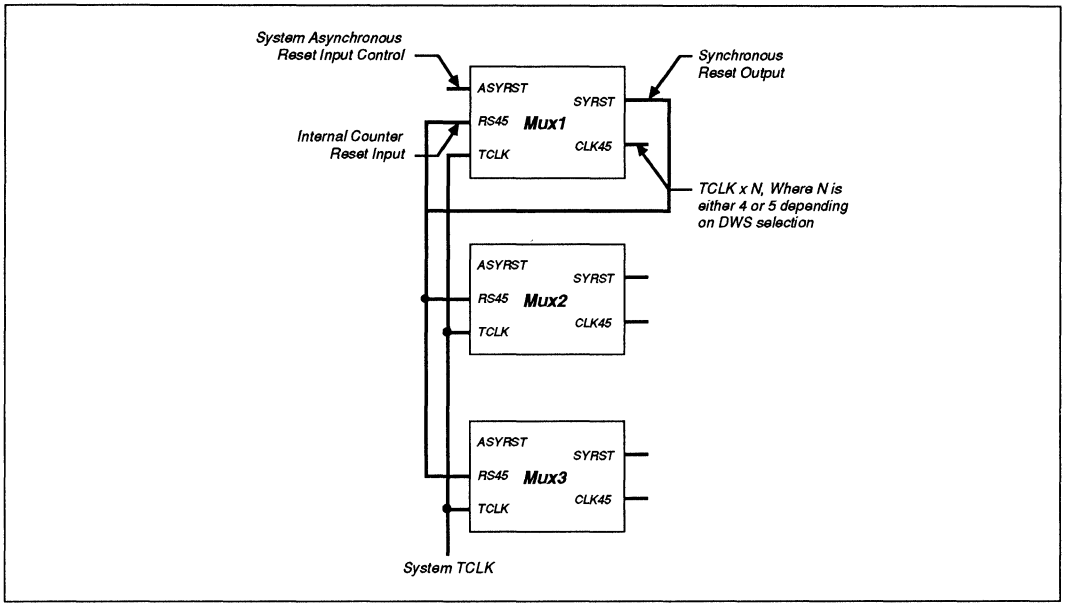


2

G-TAXI MUX TIMING WAVEFORMS



MULTIPLE MUX SYNCHRONIZATION

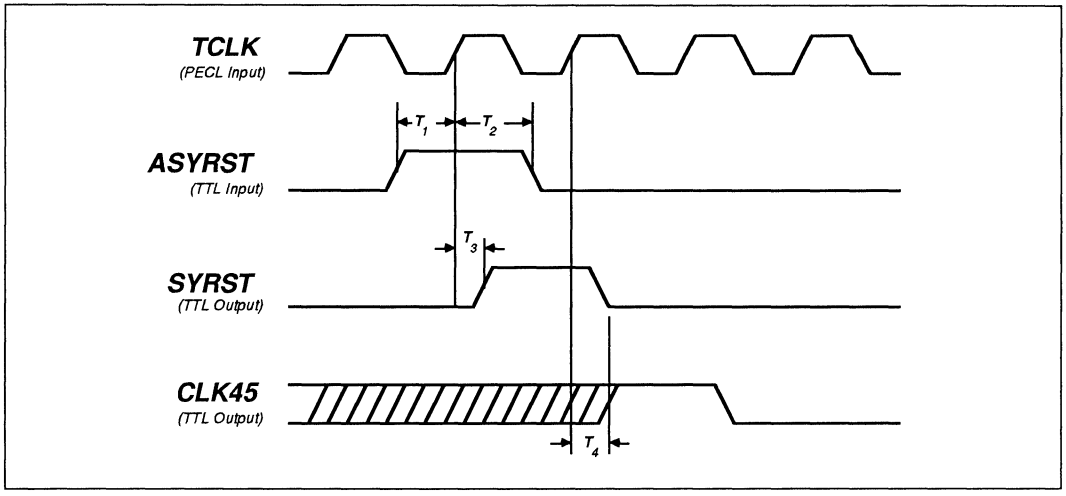


MULTIPLE MUX SYNCHRONIZATION AC CHARACTERISTICS

(Guaranteed over recommended operating conditions).

Parameter	Description	Min	Typ	Max	Units	Conditions
T_1	ASYRST to TCLK Setup	—	0	—	ns	—
T_2	ASYRST to TCLK Hold	—	2	—	ns	—
T_3	TCLK to SYRST Delay	—	6	—	ns	—
T_4	TCLK to CLK45 Delay	—	8	—	ns	—

MULTIPLE MUX SYNCHRONIZATION WAVEFORMS



G-TAXI DMX AC CHARACTERISTICS *(Guaranteed over recommended operating conditions).*

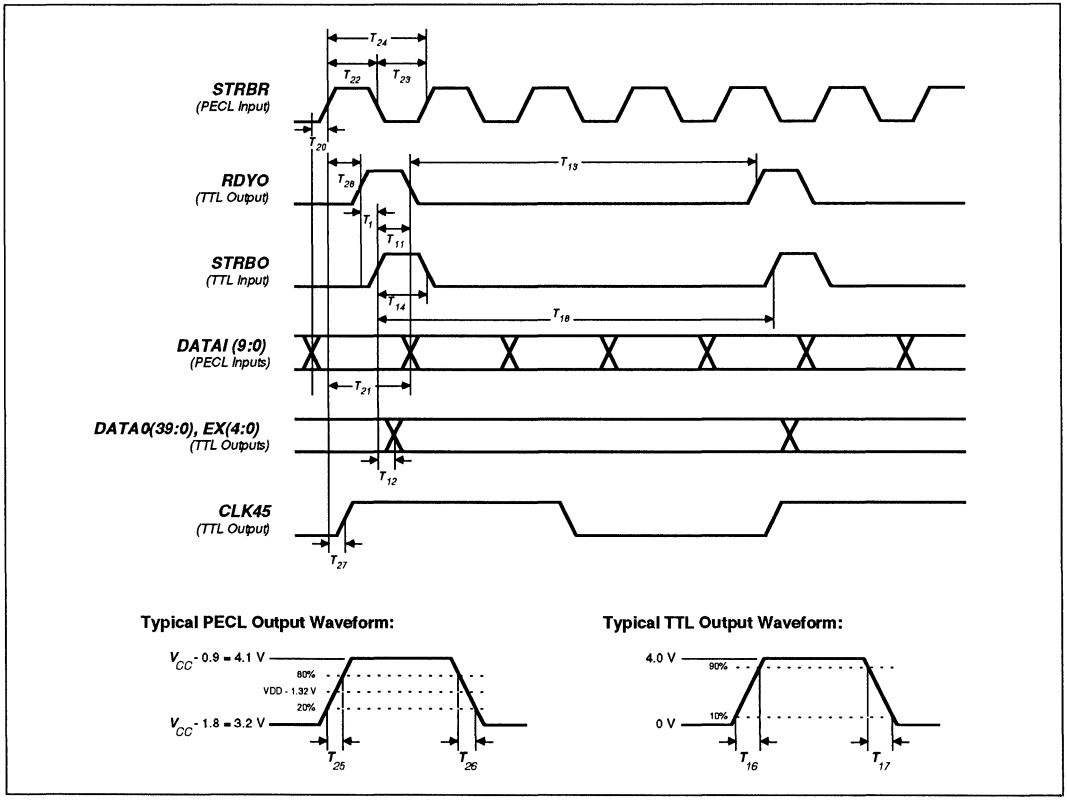
TTL I/O

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{20}	DATAI to STRBR Setup	—	0	—	ns	—
T_{21}	STRBR to DATAI Hold	—	4	—	ns	—
T_{22}	STRBR Pulse Width HIGH	—	4	—	ns	—
T_{23}	STRBR Pulse Width LOW	—	4	—	ns	—
T_{24}	STRBR Min Period	—	8	—	ns	—
T_{25}	DATAI Rise Time	—	1	—	ns	—
T_{26}	DATAI Fall Time	—	1	—	ns	Load 1 = TTL 30 pF load
T_{27}	STRBR to CLK45 delay	—	4	—	ns	—
T_{28}	STRBR to RDYO delay	—	5	—	ns	N=4 or 5 as determined by DWS input

PECL I/0

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{20}	DATAI to STRBR Setup	—	0	—	ns	—
T_{21}	STRBR to DATAI Hold	—	4	—	ns	—
T_{22}	STRBR Pulse Width HIGH	—	4	—	ns	Measured at V_{DD} - 1.32 V
T_{23}	STRBR Pulse Width LOW	—	4	—	ns	Measured at V_{DD} - 1.32 V
T_{24}	STRBR Min Period	—	8	—	ns	—
T_{25}	DATAI Rise Time	—	1	—	ns	—
T_{26}	DATAI Fall Time	—	1	—	ns	—
T_{27}	STRBR to CLK45 delay	—	4	—	ns	Load 1
T_{28}	STRBR to RDYO delay	—	5	—	ns	Load 1

G-TAXI DMX TIMING WAVEFORMS



ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +6.0V
Power Supply Voltage, (V_{MM}) ..... -0.5V to +3.0V
DC Input Voltage , (V_{IN}) ..... -0.5V to V_{DD}
DC Voltage Applied to Outputs for High Output State, ($V_{IN\,TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current, (I_{OUT}) , (DC, Output High) 50mA
PECL Output Current, (I_{OUT}) , (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +100°C
Storage Temperature, (T_{STG}) ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, (V_{DD}) ..... +5.0V ± 5%
Power Supply Voltage, (V_{MM}) ..... +2.0V ± 5%
Operating Temperature Range, (T) (2). ..... 0° to +100°C

Notes: *(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
(2) Lower limit is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS *(Guaranteed over recommended operating conditions).*

Power Supply (Tx/Rx)

		1.0		1.2			
Parameter	**Description**	**Typ**	**Max**	**Typ**	**Max**	**Units**	**Conditions**
$I_{DD(Tx)}$	Supply Current for Tx	310	—	368	—	mA	V_{DD} = 5.25 V Outputs open
$I_{DD(Rx)}$	Supply Current for Rx	500	—	620	—	mA	
$P_{D(Tx)}$	Power Dissipation for Tx	1.67	—	1.97	—	W	50% output HIGH and LOW
$P_{D(Rx)}$	Power Dissipation for Rx	2.75	—	3.38	—	W	

Power Supply (Mux/Dmx)

Parameters	**Description**	**Typ**	**Max**	**Units**	**Conditions**
$I_{DD(Mux)}$	V_{DD} Supply Current for Mux	100	150	mA	V_{DD} = 5.25 V
$I_{MM(Mux)}$	V_{MM} Supply Current for Mux	400	600	mA	V_{MM} = 2.1 V
$I_{DD(Dmx)}$	V_{DD} Supply Current for Dmx	40	60	mA	V_{DD} = 5.25 V
$I_{MM(Dmx)}$	V_{MM} Supply Current for Dmx	800	1200	mA	V_{MM} = 2.1 V

Single-Ended PECL I/O (Tx/Rx/Mux/Dmx)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	V_{DD} - 1.1	—	V_{DD} - 0.70	V	50 Ω to V_{DD} - 2V
V_{IL}	Input LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.54	V	
V_{BBI}	Reference Input	V_{DD} - 1.375	V_{DD} - 1.32	V_{DD} - 1.265	V	—
V_{OH}	Output HIGH voltage	V_{DD} - 1.020	—	V_{DD} - 0.70	V	50 Ω to V_{DD} - 2V
V_{OL}	Output LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.62	V	
V_{BBO}	Reference Output	V_{DD} - 1.375	V_{DD} - 1.32	V_{DD} - 1.265	V	
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ (min)

Differential PECL I/O (Tx/Rx)

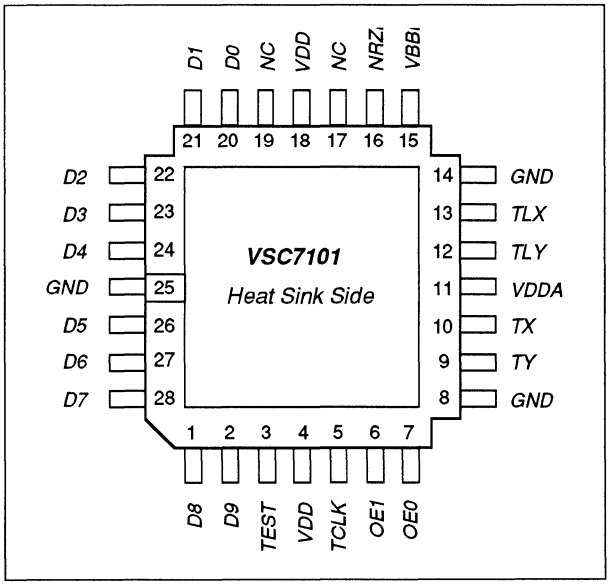
Parameters	Description	Min	Typ	Max	Units	Conditions
V_{DIF}	RX Input Differential voltage	0.2	—	1.2	V	$V_{ICM} = V_{DD}$ - 1.5V
V_{ICM}	RX Input Common Mode voltage	V_{DD} - 2.0	—	V_{DD} - 1.0	V	—
V_{OH}	TX Output High voltage	V_{DD} - 1.020	—	V_{DD} - 0.70	V	50 Ω to V_{DD} - 2V
V_{OL}	TX Output Low voltage	V_{DD} - 2.0	—	V_{DD} - 1.62	V	50 Ω to V_{DD} - 2V

TTL I/O (Mux/Dmx)

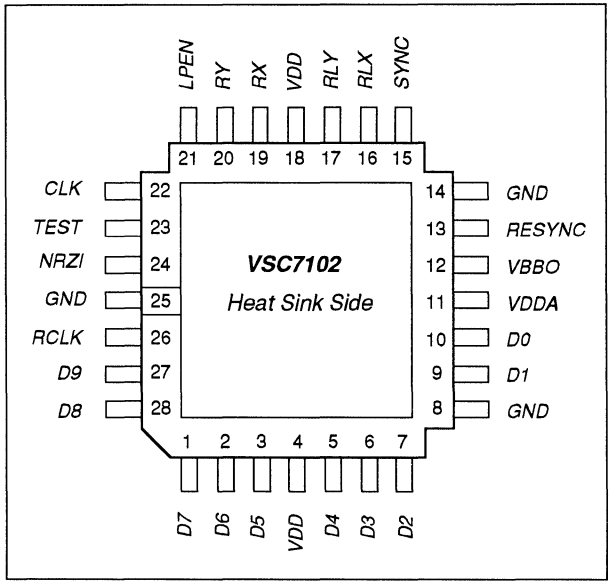
Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	2.0	—	—	V	—
V_{IL}	Input LOW voltage	—	—	0.8	V	
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5V
I_{IH}	Input HIGH current	—	—	200	µA	V_{IN} = 2.4V
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4mA
V_{OL}	Output LOW voltage	—	—	0.5	V	I_{OL} = 8mA

PIN CONNECTION DIAGRAMS

G-TAXI Tx Pin Connection Diagram



G-TAXI Rx Pin Connection Diagram



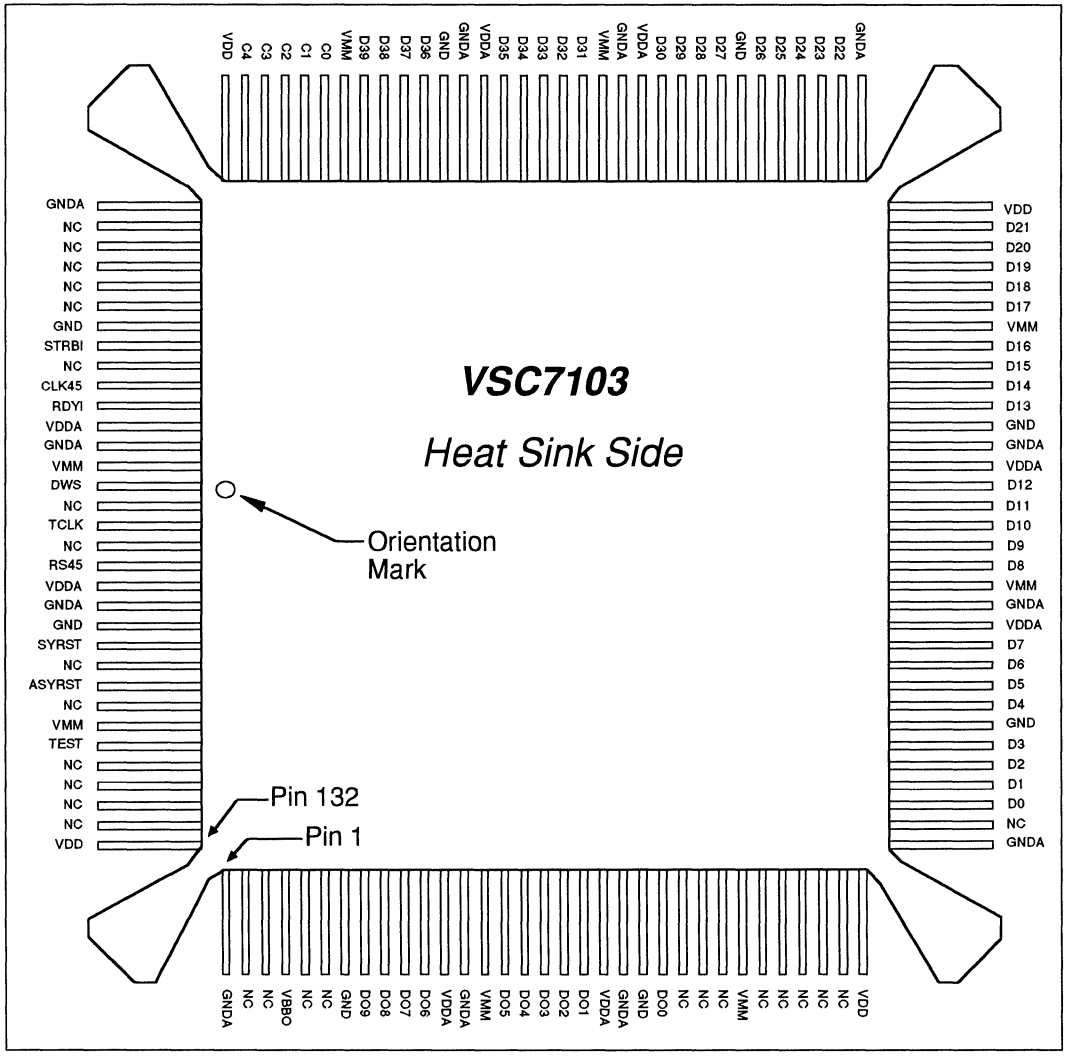
G-TAXI TX PIN DESCRIPTION

<table>
<tr><th>Pin #</th><th>Name</th><th>Description</th></tr>
<tr><td>20-24
26-28, 1, 2</td><td>D0:D9</td><td>Parallel Data Inputs. These inputs accept parallel data from the TAXI-MUX, to be latched by TCLK and transmitted serially, with D(9) first. (single-ended PECL inputs).</td></tr>
<tr><td>5</td><td>TCLK</td><td>Supplies the reference to the internal PLL clock multiplier. The internal state machine counters are synchronized to this signal. In TEST mode, this pin supplies the internal clock to the entire circuit when clock multiplying circuit is switched out. (single-ended PECL inputs)</td></tr>
<tr><td>7,6</td><td>OE0, OE1</td><td>Output Enable 0,1. These are PECL inputs. They control the PECL serial output pins according to the following:
<table><tr><th>OE0</th><th>OE1</th><th>TX/TY</th><th>TLX/TLY</th></tr><tr><td>Low</td><td>Low</td><td>active</td><td>active</td></tr><tr><td>Low</td><td>High</td><td>active</td><td>Low/High</td></tr><tr><td>High</td><td>Low</td><td>Low/High</td><td>active</td></tr><tr><td>High</td><td>High</td><td>Low/High</td><td>Low/High</td></tr></table>(single-ended PECL inputs)</td></tr>
<tr><td>16</td><td>NRZI</td><td><table><tr><th>NRZI</th><th>TX/TY, TLX/TLY</th></tr><tr><td>LOW</td><td>NRZ</td></tr><tr><td>HIGH</td><td>NRZI</td></tr></table>(PECL levels)</td></tr>
<tr><td>10,9</td><td>TX, TY</td><td>Differential serial transmitted data outputs. (differential PECL inputs)</td></tr>
<tr><td>13,12</td><td>TLX, TLY</td><td>Differential serial Transmitted Loopback outputs. When enabled, this pair of pins carries the same signal as TX/TY. They can be connected to RLX, RLY pins at the TAXI-Receiver to perform the system loopback diagnostic test. (differential PECL outputs)</td></tr>
<tr><td>3</td><td>TEST</td><td>TEST selects the normal and TEST mode function. The selection follows the following:
<table><tr><th>TEST</th><th>Select Function</th></tr><tr><td>VDD</td><td>Normal Mode</td></tr><tr><td>Floating</td><td>TEST Mode</td></tr></table>When in test mode, the internal clock multiplier circuit is switched out. The internal clock is supplied through the TCLK pin.</td></tr>
<tr><td>15</td><td>VBBI</td><td>VBB reference input. The voltage at this input defines the VBB for all single-ended PECL input signals. Typically connected to the VBBO pin from the TAXI-MUX.</td></tr>
<tr><td>11</td><td>VDDA</td><td>VDDA supplies current to the PECL output circuits. It is separated from VDD to reduce internal noise coupling, but will be connected to a common external +5V supply.</td></tr>
<tr><td>4,18</td><td>VDD</td><td>VDD supplies current to all other internal circuits. It can be connected to a common external +5V supply.</td></tr>
<tr><td>8,14,25</td><td>GND</td><td>GND should be connected to a common external ground reference.</td></tr>
<tr><td>17, 19</td><td>NC</td><td>Not connected.</td></tr>
</table>

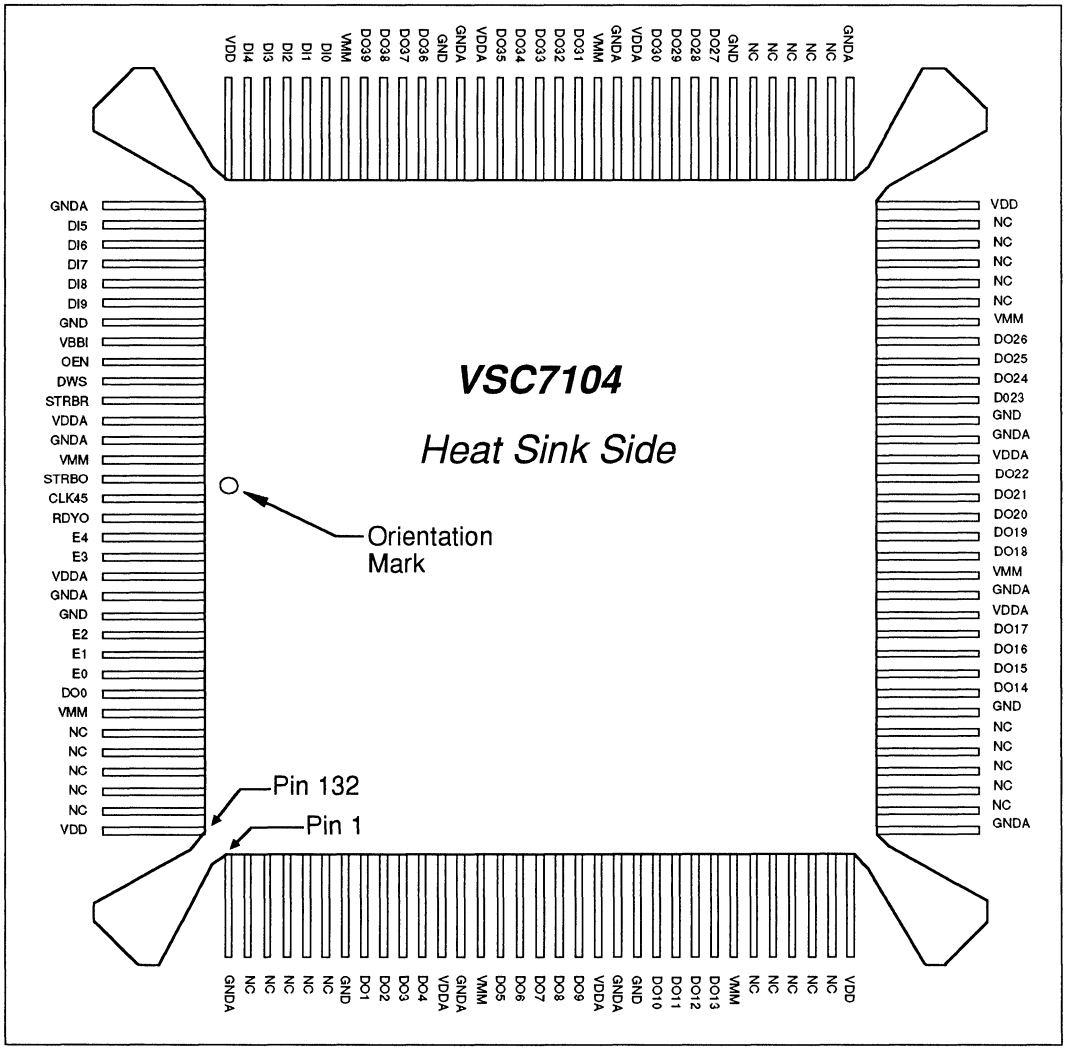
G-TAXI RX PIN DESCRIPTION

Pin #	Name	Description
10, 9, 7, 6, 5, 3, 2, 1, 28, 27	D0:D9	Parallel Data Outputs. These outputs are the most recent valid DATA symbol received by the G-TAXI. D(0) is the Least_Significant_Bit. D(9) is the Most_Significant_Bit. (PECL levels)
22	CLK	CLK is driven by an external frequency source at PECL levels. This signal is used as a frequency reference for the clock recovery PLL. Its frequency should be within 0.1% to that of the Tx TCLK.
24	NRZI	The NRZI enable allows the received data to be converted from NRZI into NRZ format. NRZI — TX/TY, TLX/TLY LOW — NRZ HIGH — NRZI
23	TEST	TEST input forces the chip into TEST mode when it is LOW (PECL level). During normal operation, TEST should be HIGH. (PECL level)
21	LPEN	LooP ENable input when LOW (PECL level) selects the serial data stream at RLX/RLY inputs as the received data. This is used in the system diagnostic loopback test. LPEN HIGH (PECL level) during normal operation.
15	SYNC	SYNC enable input allows the SYNC pattern (0011111010) to establish byte boundary for the data to follow. A new byte boundary will be established if the sync pattern is received. In a system with a different SYNC symbol, the SYNC detection function can be disabled with SYNC input LOW (PECL level) such that D(0:9) will be 'unframed'.
26	RCLK	This is a byte rate clock output from the data recovery PLL circuit. Its frequency is very close to that of the CLK input and synchronous with the serial transfer rate. D(0:9) are clocked out with the rising edges of RCLK (PECL levels).
13	RESYNC	RE-SYNC flag output is set HIGH (PECL level). When the receiver has received the SYNC character, RESYNC stays high only for one byte period. It observes the same timing as D(0:9).
19, 20	RX, RY	Differential serial received data inputs. (PECL level.).
16, 17	RLX, RLY	Differential serial Loopback data inputs. This pair of inputs should be connected to the TLX, TLY pins at the TAXI TX for system level diagnostic loopback test functions. (PECL levels)
12	VBBO	VBB reference output carries the VBB reference voltage for all the single-ended PECL signals (DATA and RCLK) originated from the G-TAXI Rx. It should be used to provide the logic level compatible with the circuits receiving these signals, typically connected to the VBBI pin of the TAXI-DMUX.
11	VDDA	VDDA supplies current to the PECL output circuits. It is separated from VDD to reduce internal noise coupling, but will be connected to a common external +5V supply.
4, 18	VDD	VDD supplies current to all other internal circuits. It will be connected to a common external +5V supply.
8, 14, 25	GND	GND should be connected to a common external ground reference.

G-TAXI MUX PIN CONNECTION DIAGRAM



G-TAXI DMX PIN CONNECTION DIAGRAM



G-TAXI MUX PIN SUMMARY

TTL Data Inputs ..... DATAI(39:Ø)
TTL Command Inputs ..... CMND(4:Ø)
TTL 32/40-bit Data Width Select Input ..... DWS
TTL Strobe Input ..... STRBI
TTL Ready Output ..... RDYI
TTL Divide by 4 or 5 Clock Output CLK45
TTL Asynchronous Reset Input ..... ASYRST
TTL Synchronous Reset Output ..... SYRST
Reset Clock 4 or Clock5 Input RS45
TEST Input ..... TEST
PECL Clock Input ..... TCLK
PECL Encoded Data Outputs ..... DATAO(9:Ø)
PECL VBB Reference Output ..... VBBO
PECL Power Supply pins ..... VDDA
TTL Power Supply pins ..... VDD
Logic Power Supply pins ..... VMM
PECL Ground pins ..... GNDA
TTL /Logic Ground pins ..... GND

G-TAXI MUX PIN DESCRIPTION

TTL Compatible I/O

Pin #	*Name*	*Description*
36-39, 41-44, 48-52, 56-59, 61-65, 68-72, 74-77, 81-85, 89-92	DATAI(39:Ø)	Parallel Data inputs. These 40 inputs accept parallel data from the host system bus. The incoming data is latched by STRBI, multiplexed, encoded, and clocked into the G-TAXI Transmitter. D(Ø) is within the Last Shifted Byte.
94-98	CMND(Ø:4)	Command (special character control) Inputs. A set of pre-defined special characters may be encoded using the CMND inputs. Refer to the CMND table on page 9.
114	DWS	Data Width Select input. When high, G-TAXI Mux accepts data in 40-bit mode and multiplexes it into 5 bytes for encoding. When low, G-TAXI Mux accepts data in 32-bit mode and multiplexes it into 4 bytes for encoding (DATAI(31:0) inputs are multiplexed and DATAI(39:32) are ignored).
107	STRBI	Strobe Input. The rising edge of this input causes the DATAI(39:0) and CMND(4:0) inputs to be latched into the INPUT REGISTER. The input latching will only occur when RDYI output rises — an indication that the previous data has been latched to the MULTIPLEXER LATCH.
110	RDYI	Ready output. This output rises after transfer of data from the INPUT REGISTER to the MULTIPLEXER LATCH is complete and the INPUT REGISTER is ready to accept the next 40-bit wide DATAI. If STRBI is asserted when RDYI is not ready, the data will not be latched into the Mux. RDYI falls in response to STRBI.
109	CLK45	Output Clock4 or Clock5 signal. This output clock is the PECL TCLK input signal divided-by-4 (2 TCLK cycle high, 2 TCLK cycle low) or divided-by-5 (2 TCLK cycle high, 3 TCLK cycle low) as defined by the DWS input. It can be used in a synchronous system as the master clock source at the 40-bit or 32-bit bus frequency. (TTL level).
124	ASYRST	Asynchronous Reset. This input is used to reset the Muxes in multiple parallel systems. Reset should only have to be performed during system initialization. In most applications, ASYRST can be hard-wired to GND. ASYRST is internally synchronized by TCLK.
122	SYRST	Synchronous Reset. This output is the synchronized (by TCLK) version of ASYRST. In multiple Mux systems, SYRST of one Mux should be connected to the RS45 inputs of all Muxes in the system. This allows all Muxes to be reset from a common, synchronized source.
118	RS45	Reset CLK45. This input directly resets the internal MUX logic when it is HIGH. In multiple, parallel Mux systems it should be connected to the SYRST output of the MUX whose ASYRST input is being used. In most applications, RS45 should be hard-wired to GND.
127	TEST	TEST input. TEST is used for setting positive running disparity during initialization. In most applications, TEST should be hard-wired to GND.

PECL Compatible I/O

Pin #	Name	Description
116	TCLK	Single-ended PECL Clock Input. This input is intended to receive the same clock that runs the G-TAXI Tx, which takes its input data from the G-TAXI Mux. At every TCLK cycle, a new byte of encoded data (10-bit) is presented at the DATAO(9:0) pins synchronously.
8-11, 15-19, 23	DATAO(0:9)	Single-ended PECL Data Outputs. These pins output mux'ed and encoded data at PECL voltage levels. They are connected to the DATA input pins of the G-TAXI Tx. New DATAO is presented at the output pins every TCLK cycle.
4	VBBO	VBB reference voltage output. This is the reference voltage for DATAO(9:0) outputs. When connected to G-TAXI Tx VBBI input, this voltage sets the VBB reference of all the input circuits on the G-TAXI Tx.

Power & Ground Pins

Pin #	Name	Description
12, 20, 45, 53, 78, 86, 111, 119	VDDA	VDDAs supply current to the I/O circuits. They are isolated from VDDs to reduce internal noise coupling, but will be connected to a common external +5V supply.
33, 66, 99, 132	VDD	VDDs supply current to all of the internal logic. They are isolated from VDDAs to reduce internal noise coupling, but will be connected to a common external +5V supply.
14, 27, 47, 60, 80, 93, 113, 126	VMM	VMMs supply current to all of the internal logic. They are connected to a common external +2V supply.
1, 13, 21, 34, 46, 54, 67, 79, 87, 100, 112, 120	GNDA	GNDAs are used by the I/O circuits. They are separated from GNDs to reduce internal noise coupling, but will be connected to a common external ground reference.
7, 22, 40, 55, 73, 88, 106, 121	GND	GNDs are used by all of the internal logic. They are separated from GNDAs to reduce internal noise coupling, but will be connected to a common external ground reference.
2, 3, 5, 6, 24-26, 28-32, 35, 101-105, 108, 115, 117, 123, 125, 128-131	NC	Not connected.

G-TAXI DMX PIN SUMMARY

TTL Data Outputs ..... DATAO(39:Ø)
TTL EXception Outputs ..... EX(4:Ø)
TTL 32/40-bit Data Width Select Input ..... DWS
TTL STROBE_Out Input ..... STRBO
TTL Ready Output ..... RDYO
TTL Data Output Enable ..... OEN
Output Clock4 or Clock5 Signal CLK45
PECL Data Inputs ..... DATAI(9:Ø)
PECL STRBR Input ..... STRBR
PECL VBB Reference Input ..... VBBI)
PECL Power Supply pins ..... VDDA
TTL Power Supply pins ..... VDD
Logic Power Supply pins ..... VMM
PECL Ground pins ..... GNDA
TTL /Logic Ground pins ..... GND

G-TAXI DMX PIN DESCRIPTION

TTL Compatible I/O

Pin #	*Name*	*Description*
125, 8-11, 15-19, 23-26, 41-44, 48-52, 56-59, 74-77, 81-85 89-92	DATAO(39:0)	Parallel DATA outputs, TTL-compatible tri-state output. These outputs carry parallel data to the receiving system. D(0) is within the Last Shifted Byte. DATAO(39:32) will be tri-stated in 32-bit mode.
122-124, 117, 118	EX(4:0)	EXception output pins. They indicate G-TAXI special conditions (errors or special K-character) that are received. EX(4:0) are timed the same way as DATAOs. EX(4:0) are never disabled. REFER TO EXCEPTION TABLE, p. 15.
109	DWS	Data Width Select input. When high, G-TAXI Dmx outputs data in 40-bit mode (5 bytes). When low, DATA0(39:32) are not used and DATA0(31:0) outputs carry the 4-byte data.
114	STRBO	Input strobe signal. The rising edge of this input causes the data transfer from BUFFER LATCH into the OUTPUT LATCH to happen as soon as OUTPUT LATCH has been read. This input should only be strobed when RDYO is active.
116	RDYO	Output READY output. This output rises after transfer of data from the BUFFER LATCH to the OUTPUT LATCH is complete and the DATA0(39:0) outputs are ready to be transferred. It falls in response to asserted STRBO input. If STROBE is asserted when RDYO is not ready, the OUTPUT LATCH will not be affected. RDYO falls in response to STRBO.
108	OEN	Data Output Enable. When low, the DATAO outputs are enabled. When high, DATAO outputs are in high impedance state.
115	CLK45	Output Clock4 or Clock5 signal. This output clock is the PECL STRBR input signal divided-by-4 (2 STRBR cycle high, 2 STRBR cycle low) or divided-by-5 (2 STRBR cycle high, 3 STRBR cycle low) as defined by the DWS input. It can be used in a synchronous system as the master clock source at the 40-bit or 32-bit bus frequency. (TTL level)

PECL Compatible I/O

Pin #	Name	Description\
94-98, 101-105	DATAI(Ø:9)	PECL data inputs. These inputs are driven by the G-TAXI Rx outputs at PECL voltage levels. The logic threshold is determined by VBBI voltage. They are connected to the DATA output pins at the G-TAXI Rx. New DATAI is presented at the input pins every time STRBR goes active at the G-TAXI Rx.
110	STRBR	PECL STROBE input. This input is connected to the RCLK output of the G-TAXI Rx and used by the G-TAXI DMX to transfer data from its DATAI(9:0) inputs into the INPUT REGISTER.
107	VBBI	VBB reference voltage input. This VBB is the reference voltage for DATAI(9:0) inputs. When connected to G-TAXI Rx VBBO output, this voltage sets the VBB reference of all the input circuits on the G-TAXI DMX.

Power & Ground Pins

Pin #	Name	Description
12, 20, 45, 53, 78, 86, 111, 119	VDDA	VDDAs supply current to the I/O circuits. They are isolated from VDDs to reduce internal noise coupling, but will be connected to a common external +5V supply.
33, 66, 99, 132	VDD	VDDs supply current to all of the internal logic. They are isolated from VDDAs to reduce internal noise coupling, but will be connected to a common external +5V supply.
14, 27, 47, 60, 80, 93, 113, 126	VMM	VMMs supply current to all of the internal logic. They are connected to a common external +2V supply.
1, 13, 21, 34, 46, 54, 67, 79, 87, 100, 112, 120	GNDA	GNDAs are used by the I/O circuits. They are separated from GNDs to reduce internal noise coupling, but will be connected to a common external ground reference.
7, 22, 40, 55, 73, 88, 106, 121	GND	GNDs are used by all of the internal logic. They are separated from GNDAs to reduce internal noise coupling, but will be connected to a common external ground reference.
2, 3, 5, 6, 24-26, 28-32, 35, 101-105, 108, 115, 117, 123, 125, 128-131	NC	Not connected.

FEATURES

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Set input on VS8001 synchronizes external and internal clocks
- Skip input on VS8002 for alignment of 12-bit output to word boundaries
- Standard ECL power supplies: V_{EE} = -5.2 V ± 0.26 V, V_{TT} = -2.0 V ± 0.1 V
- Available in commercial or industrial temperature ranges

FUNCTIONAL DESCRIPTION

Introduction

The VS8001 and VS8002 are data conversion devices capable of serial data rates up to 1.25 Gb/s, transforming 12-bit wide parallel data to serial data and serial data to 12-bit wide parallel data. Evaluation of the parts is facilitated by on-chip self-test circuitry.

The VS8001 and VS8002 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leadless or leaded chip carrier. Refer to Section 6, "Packaging" for a complete description of these packages.

VS8001

The VS8001 is a 12-bit parallel to serial data converter. A fully synchronous internal design receives 12 parallel single-ended ECL bit streams ***(D_0 - D_{11})*** and converts these to a single differential bit stream ***(MUXDATA, NMUXDATA)*** up to 1.25 Gb/s. To accommodate various system timing constraints, both the high frequency clock ***(CLK, NCLK)*** and low frequency divide by 12 clock ***(CLOCK12)*** are driven off chip. A synchronizing input ***(SET)*** allows alignment of the internal low frequency clock to an externally supplied clock ***(DCLOCK)***.

VS8002

The VS8002 is a serial to 12-bit parallel data converter. A fully synchronous internal design receives a single bit stream ***(MUXDATA, NMUXDATA)*** operating at data rates up to 1.25 Gb/s and converts it to 12 parallel single-ended ECL bit streams ***(D_0 - D_{11})***. The high frequency clock ***(CLK, NCLK)*** is externally supplied. The low frequency divide by 12 clock ***(DCLOCK)*** is driven off chip synchronous with the parallel data. An external signal ***(SKIP)*** may be used to slip the low frequency clock by one serial data bit for alignment of the 12-bit output to word boundaries. A ***SKIP*** input causes output to be invalid for up to 3 ***DCLOCK*** cycles.

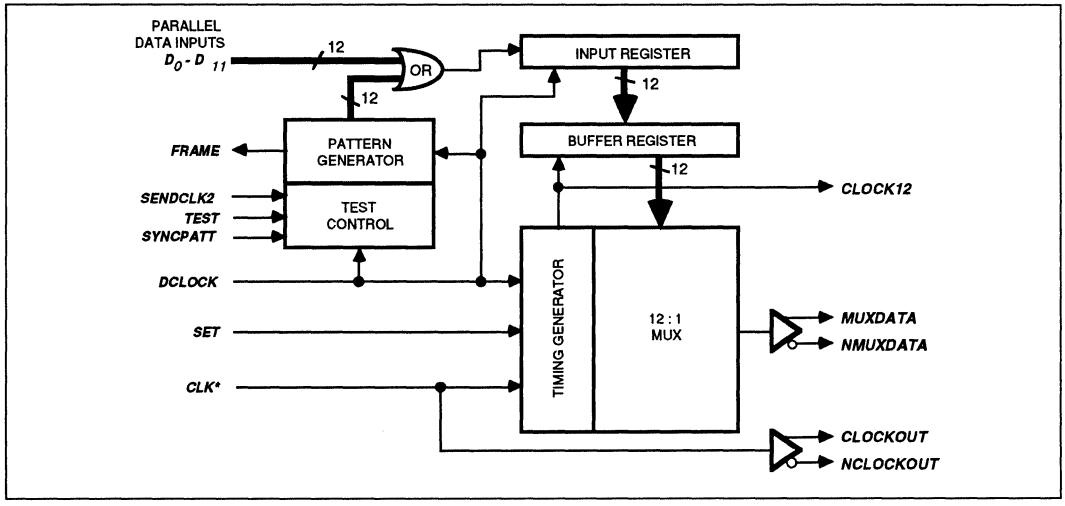
Self-Test Feature

In addition to normal parallel to serial and serial to parallel data conversion hardware, the VS8001 and VS8002 contain features which allow the user to fully evaluate the at-speed functionality of the devices. Given some simple enabling signals ***(TEST, SYNCPATT)***, built in hardware causes the VS8001 to transmit multiplexed internally generated data patterns via its high speed serial port to the high speed serial input on the VS8002. These signals allow the VS8002 to align itself to word boundaries and compare incoming data to its own internally generated, pseudo-random test patterns. Test enabling pins on the VS8002 consist of the ***TEST*** and ***SYNCPATT***. Test is confirmed on the ***ALIGNED, ERROR, FRAME*** and ***MATCH*** pins on the VS8002.

APPLICATIONS

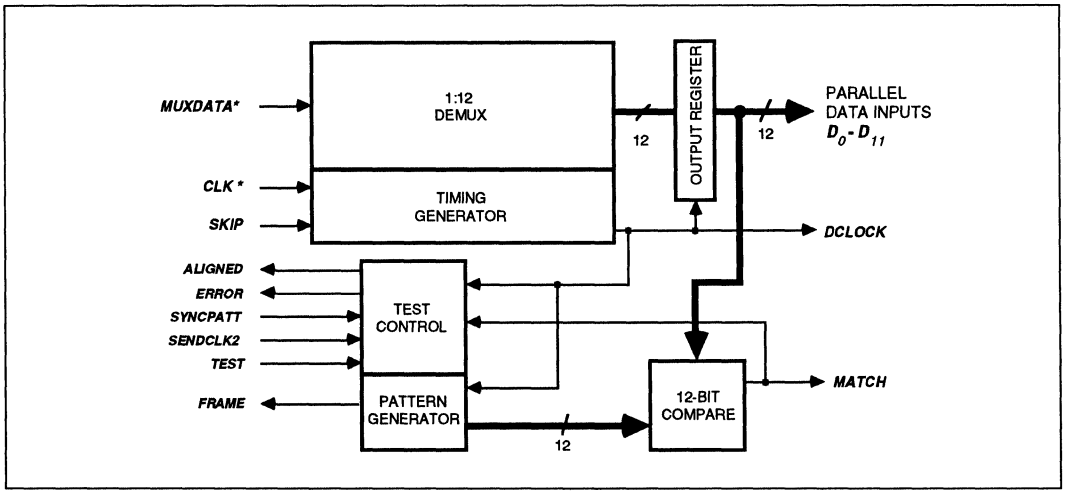
- High speed instrumentation and test equipment
- Fiber optic communication
- Local area networks
- Serialization of computer backplanes
- Computer to computer interfaces
- Serial control buses for aerospace environments

VS8001 12:1 MULTIPLEXER BLOCK DIAGRAM



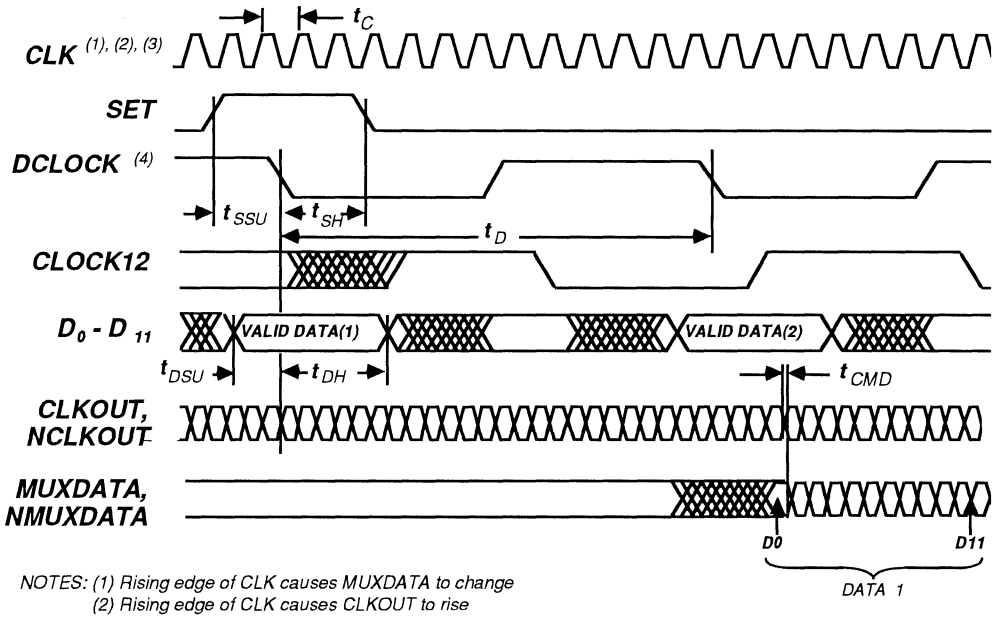
** **CLK** can be single ended or differential*

VS8002 1:12 DEMULTIPLEXER BLOCK DIAGRAM



** **MUXDATA** and **CLK** can be single ended or differential*

VS8001 12:1 MULTIPLEXER WAVEFORMS

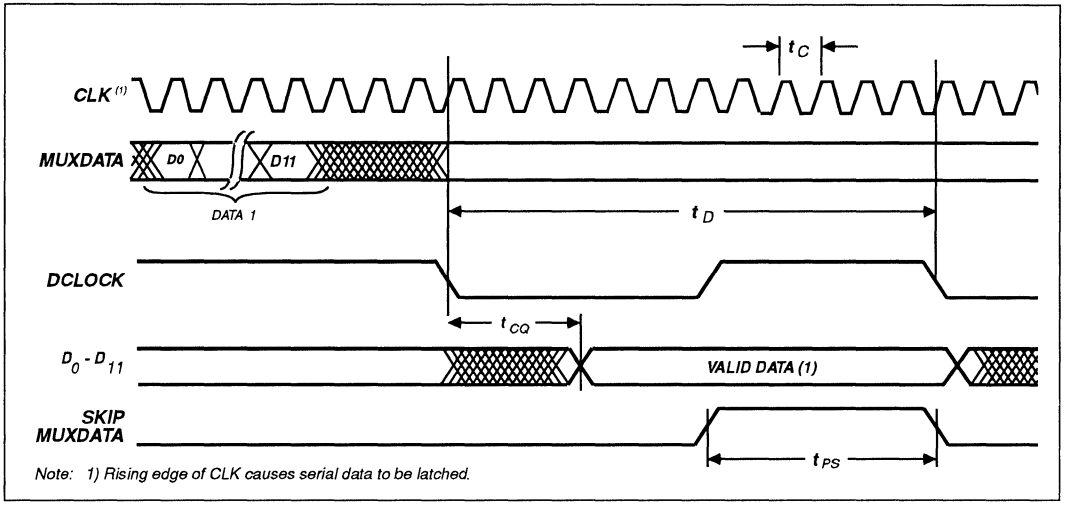


NOTES: (1) Rising edge of CLK causes MUXDATA to change
(2) Rising edge of CLK causes CLKOUT to rise
(3) Falling edge of CLK causes CLOCK12 to change
(4) Falling edge of DCLOCK latches parallel data

VS8001 AC CHARACTERISTICS *(Over recommended operating conditions.)*

Parameter	*Description*	*MIN*	*TYP*	*MAX*	*Units*
t_C	CLK period	0.80	—	—	ns
t_D	DCLOCK period	9.6	—	—	ns
t_{SSU}	Set set-up time	2.0	—	—	ns
t_H	Set hold time	3.0	—	—	ns
t_{DSU}	Data set-up time	2.0	—	—	ns
t_{DH}	Data hold time	3.0	—	—	ns
t_{CMD}	Clock output (CLKOUT, NCLKOUT) to muxed data output (MUXDATA, NMUXDATA) timing	-50	—	+150	ps
jitter	CLK to MUXDATA, NMUXDATA (max-min), (HIGH to LOW) same part, same pin as constant conditions	—	<50	—	ps

VS8002 1:12 DEMULTIPLEXER WAVEFORMS



Note: 1) Rising edge of CLK causes serial data to be latched.

VS8002 AC CHARACTERISTICS: *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units
t_C	CLK period	0.80	—	—	ns
t_D	DCLOCK period	9.6	—	—	ns
t_{CQ}	Clock to Q data	0.5	—	2.5	ns
t_{PS}	Minimum pulse skip	3.0	—	—	ns
Phase Margin	MUXDATA phase timing margin with respect to CLK input: $Phase\ Margin = \left(\frac{t_{SU} + t_H}{t_C}\right) 360^c$	135	—	—	degrees

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} + 0.7 V to -6.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature (3), (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage, (V_{TT}) ..... -2.0 V ± 0.1 V
Power Supply Voltage, (V_{EE}) ..... -5.2 V ± 0.26 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

3

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN} and V_{HSIN}) must be greater than V_{TT} - 0.5 V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS

ECL Inputs/Outputs

(Over recommended operating conditions with internal V_{REF}. V_{CC} = V_{CCA} = GND, Output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-700	mV	V_{IN} = V_{IH} (max)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min
V_{REF}	ECL input reference, V_{BB} (2)	—	-1.29	—	V	—

NOTE: 1) Differential ECL output pins must be terminated identically.
2) V_{REF} input is used to supply external V_{BB} on chip for ECL 10K ECL compatibility.

HIGH SPEED INPUTS/OUTPUTS

(V_{EE} = -5.2V, V_{CC} = GND, V_{TT} = -2.0V, T_C = 25°C. Input reference level (V_{REF}) = -3.5 V Typ.)
Complementary high speed output pins must be terminated equally.

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load: 50 Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	
ΔV_{OUT}	Output voltage swing	0.62	0.9	1.3	V	
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for all inputs

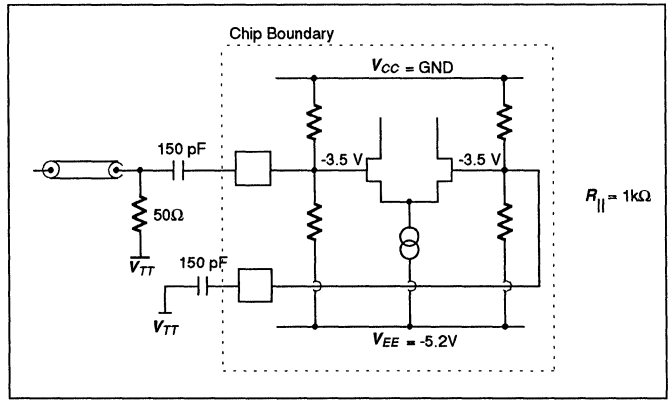
NOTES: *1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.*
2) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed output pins must be terminated identically.
4) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

POWER DISSIPATION *(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)*

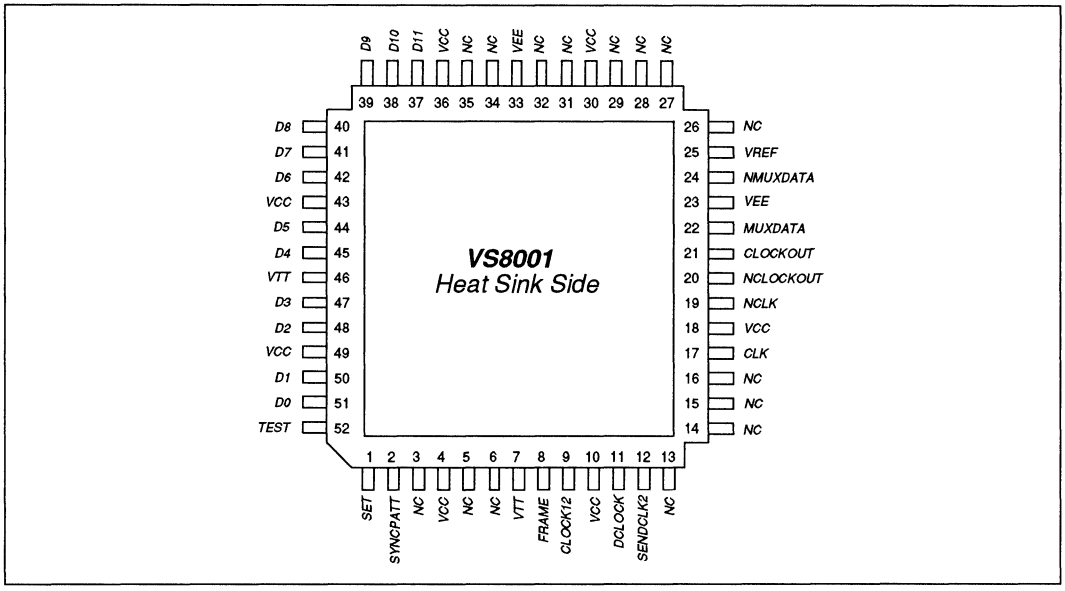
Parameter	Description	VS8001			VS8002			Units
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power supply current from V_{EE}	—	415	520	—	435	550	mA
I_{TT}	Power supply current from V_{TT}	—	200	300	—	270	400	mA
P_D	Power dissipation	—	2.6	3.5	—	2.8	3.9	W

HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated at right.



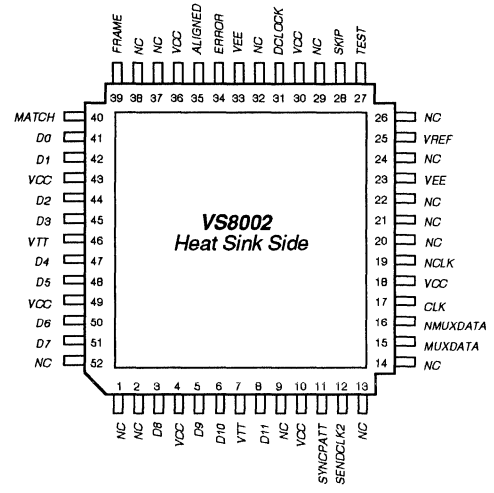
VS8001 PIN DIAGRAM



VS8001 PIN DESCRIPTION

Pin #	Name	I/O	Description
17, 19	***CLK, NCLK***	I	High speed clock input (capacitively coupled)
21, 20	***CLOCKOUT, NCLOCKOUT***	O	High speed clock output
22, 24	***MUXDATA, NMUXDATA***	O	High speed serial data output
37-42, 44, 45, 47, 48, 50, 51	***DO-D11***	I	Parallel data inputs (ECL)
9	***CLOCK12***	O	Internally generated divide by 12 clock output (ECL)
11	***DCLOCK***	I	External divide by 12 clock input (ECL)
1	***SET***	I	Synchronization input (ECL)
52	***TEST***	I	Test hardware enable (ECL input). LOW for normal operation.
8	***FRAME***	O	Test pattern repeat confirmation (ECL output). Float or VCC for normal operation.
2	***SYNCPATT***	I	Test pattern alignment enable (ECL input). LOW for nornal operation.
12	***SENDCLOCK2***	I	"CLK2" pattern enable (ECL input). LOW for normal operation.
25	V_{REF}		ECL reference level input.
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection.
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic.
23, 33	V_{EE}		-5.2 V supply for high speed logic.
3, 5, 6, 13-16, 26-29, 31, 32, 34, 35	***NC***		No connection.

VS8002 PIN DIAGRAM



VS8002 PIN DESCRIPTION

Pin #	Name	I/O	Description
17, 19	***CLK, NCLK***	I	High speed clock input (capacitively coupled)
15, 16	***MUXDATA, NMUXDATA***	I	High speed serial data input
41, 42, 44, 45, 47, 48, 50, 51, 3, 5, 6, 8	***DO-D11***	O	Parallel data outputs (ECL)
31	***DCLOCK***	I	Internally generated divide by 12 clock output (ECL)
28	***SKIP***	I	Causes one high speed serial bit to be skipped for word boundary shifting. A SKIP input causes data to become invalid for up to 3 DCLOCK periods. (ECL input)
35	***ALIGNED***	O	Indicates that the demux has found a match on three consecutive DCLOCK cycles (ECL output). Float or VCC for normal operation.
34	***ERROR***	O	Indicates that the internally generated pattern did not match the incoming data on at least one DCLOCK cycle since the error latch was reset (ECL output). Float or VCC for normal operation.
27	***TEST***	I	Test hardware enable (ECL input). LOW for normal operation.
39	***FRAME***	O	Test pattern repeat confirmation (ECL output). Float or VCC for nornal operation.
40	***MATCH***	O	Indicates that the internally generated pattern matched the incoming demultiplexed data (ECL output). Float or VCC for normal operation.
11	***SYNCPATT***	I	Test pattern enable (ECL input). LOW for nornal operation.
12	***SENDCLOCK2***	I	"CLK2" pattern enable (ECL input). LOW for normal operation.
25	V_{REF}	I	ECL reference level input.
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection.

VS8002 PIN DESCRIPTION (con't)

Pin #	Name	I/O	Description
7, 46	V_{TT}	I	-2.0 V supply for internal reference generation & low power logic.
23, 33	V_{EE}	I	-5.2 V supply for high speed logic.
1, 2, 9, 13, 14, 20-22, 24, 26, 29, 32, 38, 52	NC		No connection.

SELF-TEST FEATURE

Test Description

The following is a description of the circuitry and method used to implement the self-test feature incorporated in the VS8001 and VS8002.

Because of the difficulty and cost associated with manually generating and detecting high speed data streams, the VS8001 and VS8002 have been designed with circuitry which enables the user to perform an at-speed functional evaluation of the parts in a system environment by using a single external stimulus: the high speed clock. The test circuitry, distributed between the two parts, consists of two pattern generators, control logic, and a twelve-bit comparator. The multiplexer generates a serial data pattern, and the demultiplexer detects the pattern and compares it for correctness.

The pattern generator on the VS8001 creates twelve-bit patterns for the multiplexer, which then converts these twelve-bit words into a serial data stream. The serial output of the multiplexer is connected to the serial input of the demultiplexer. The demultiplexer converts this high speed serial data bit stream into twelve bit parallel data and compares the incoming data to patterns created by its own test pattern generator.

The pattern generators can make three different patterns: a synchronizing pattern (called *"SYNC"*), a transition pattern (called *"CLK2"*), and a pseudo-random pattern that repeats every 4095 words. The *SYNC* pattern is sent first to allow the demultiplexer to find word boundaries. During synchronization, the ***ALIGNED*** pin on the demultiplexer signals that the comparator has found a match on three successive words. This is followed by the *CLK2* pattern which signals the demultiplexer that the pattern is about to change to the 4095 word pseudo-random pattern. This allows the demultiplexer to start its pseudo-random pattern at the appropriate time to match the pattern being received on the incoming data stream from the multiplexer.

The incoming data pattern and the locally generated test pattern go to a twelve-bit comparator. The result of the comparison appears at the ***MATCH*** pin of the demultiplexer. A latch, which is reset upon entering the pseudo-random mode, detects any mismatch between the incoming data pattern and the locally generated test pattern. The latch state appears at the ***ERROR*** pin of the demultiplexer. On both parts, a one period pulse on the ***FRAME*** pin signals that the pseudo-random pattern is repeating.

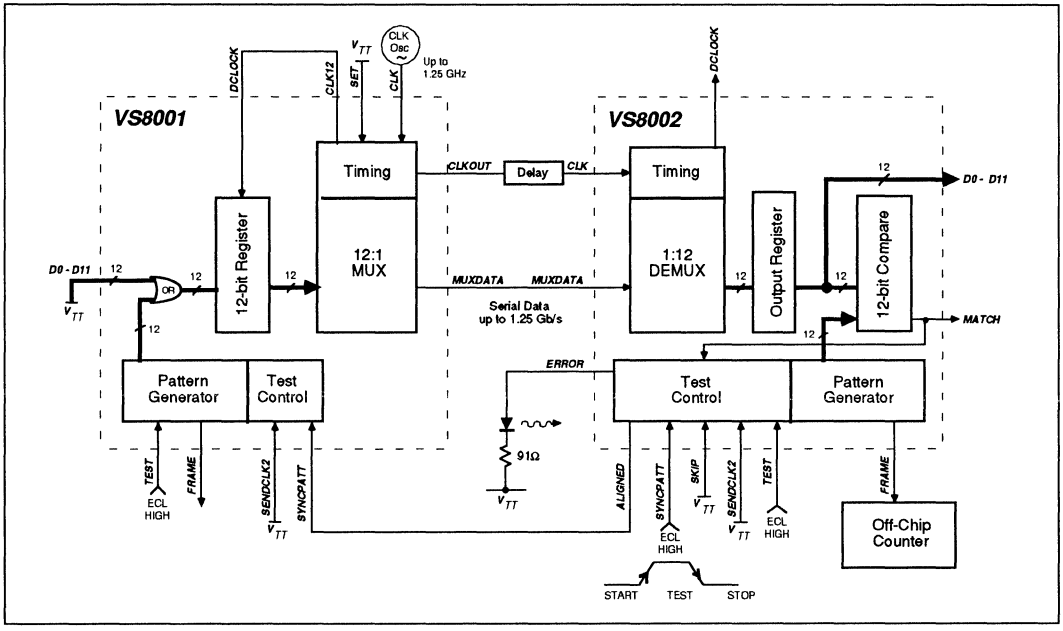
The test is controlled with the ***TEST*** and ***SYNCPATT*** pins on both parts. The diagram on the following page shows the self-test setup in more detail.

TEST HARDWARE BLOCKS

VS8001

The test hardware on the MUX consists of a 12-bit pattern generator with control logic. The individual blocks are described below.

SELF-TEST SETUP



Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the MUX pattern generator. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4095 ***DCLOCK*** cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the ***FRAME*** pin as a HIGH signal for one ***DCLOCK*** period out of every 4095 while in pseudo-random mode.

VS8002

The test hardware on the DEMUX consists of a 12-bit pattern generator with control logic and a 12-bit comparator. The individual blocks are described briefly below.

Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the DEMUX pattern generator. It also resets the error latch upon entering the pseudo-random test mode. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

Aligned FSM

When ***SYNCPATT*** is LOW and ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles, the ***ALIGNED*** signal will go HIGH on the next cycle. This is called the "aligned" state. Once aligned the ***ALIGNED*** pin will stay HIGH until ***SYNCPATT*** goes LOW, forcing a reset of the aligned state

machine. When aligned the DEMUX will not issue internally generated skip signals.

ERROR Latch

The ***ERROR*** latch is set if ***TEST*** is HIGH and ***MATCH*** is LOW. It is reset when entering the aligned state or when the ***TEST*** pin is LOW. The purpose is to latch any mismatch detected during the pseudo-random test.

SKIP Edge Generator FSM

If an internally generated skip is requested, this state machine translates the request to a rising edge and locks out internally generated skip signals for four ***DCLOCK*** cycles.

Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4095 ***DCLOCK*** cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the ***FRAME*** pin as a HIGH signal for one ***DCLOCK*** period out of each 4095 while in the pseudo-random mode.

TEST PINS

VS8001

There are 4 pins on the VS8001 which are used only for testing the part. The input pins used only for testing are ***TEST, SYNCPATT,*** and ***SENDCLK2.*** For normal operation, the ***TEST*** pin must be forced to ECL LOW or tied to V_{TT}. The one output pin used only for testing is ***FRAME.*** For normal operation, the termination of the ***FRAME*** pin is not critical. Usually, the output driver will be off. This pin may be properly terminated to V_{TT}, left floating, or tied to the V_{CC} supply. In test operations, all of the test pins should be properly terminated to V_{TT}.

TEST (ECL input pin)

The input, ***TEST,*** may be driven asynchronously. When ***TEST*** is LOW, all effects of the self-test hardware on the results of the MUX are asynchronously disabled. Explicitly, when the ***TEST*** pin is LOW, the output of the pattern generator is all zeros (000000000000).

When the ***TEST*** pin is HIGH and the high speed ***CLK*** and ***DCLOCK*** inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the MUX chip. In test mode the 12 parallel data input pins must be driven to ECL LOW or tied to the V_{TT} power supply.

SYNCPATT (ECL input pin)

The input pin, ***SYNCPATT,*** should be driven synchronously with respect to ***DCLOCK.*** When ***SYNCPATT*** is LOW, the pattern selector state machine will be forced to the zero state. If in test mode and ***SYNCPATT***= LOW, the MUX pattern generator will generate the *"SYNC"* pattern (100101010110). This pattern will appear at the high speed serial output port of the MUX (left bit first). The DEMUX expects to receive this pattern for word boundary alignment.

When in test mode and ***SYNCPATT*** goes HIGH, the MUX pattern generator will change the pattern on the next ***DCLOCK*** cycle. The *CLK2* pattern (101010101010) will be generated for 3 ***DCLOCK*** periods to signal a change in test mode. The next ***DCLOCK*** cycle will start a pseudo-random pattern that repeats every 4095 ***DCLOCK*** cycles. In test mode, the pseudo-random pattern sequence continues until ***SYNCPATT*** goes LOW or ***SENDCLK2*** goes HIGH.

In the intended test flow, the ***ALIGNED*** signal from the DEMUX is used to drive the ***SYNCPATT*** input on the MUX chip. This allows the DEMUX to determine the time necessary for alignment using the *SYNC* pattern before the MUX changes to the pseudo-random test mode.

SENDCLK2 (ECL input pin)

The input pin, ***SENDCLK2***, is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

FRAME (ECL output pin)

FRAME=HIGH indicates that the internally generated pattern (001010101010) was sent to the multiplexer's parallel data input register on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

VS8002

There are some pins on the VS8002 which are used only for testing the part. The input pins used only for testing are ***TEST, SYNCPATT***, and ***SENDCLK2***. For normal operation, the ***TEST*** pin must be forced to ECL LOW or tied to the V_{TT} supply. For normal operation, ***SYNCPATT*** and ***SENDCLK2*** may be left floating, forced to ECL LOW, or tied to the V_{TT} supply. The output pins used only for testing are ***MATCH***, ***ALIGNED***, ***ERROR***, and ***FRAME***. For normal operation, the termination of these output pins is not critical. Usually, the output drivers will be off. These pins may be properly terminated to V_{TT}, left floating, or tied to the V_{CC} supply. In test operations, all of the test pins should be properly terminated to V_{TT}

TEST (ECL input pin)

The input pin, ***TEST***, may be driven asynchronously. When ***TEST*** is LOW, all effects of the self-test hardware on the results of the DEMUX are asynchronously disabled. Explicitly, when the ***TEST*** pin is LOW, no ***SKIPs*** (word rotation) will be internally generated and the error latch input will be forced LOW.

When the ***TEST*** pin is HIGH and the high speed ***CLK*** inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the DEMUX chip.

SYNCPATT

The input pin, ***SYNCPATT***, should be driven synchronously with respect to ***DCLOCK***. When ***SYNCPATT*** is LOW, the pattern selector, word alignment selector, and ***SKIP*** edge generator state machines will all be forced to their zero states. In this state, the DEMUX pattern generator will generate the *SYNC* pattern (100101010110). This allows external word alignment using the ***MATCH*** output pin and the ***SKIP*** input pin.

When in test mode and ***SYNCPATT*** goes HIGH, the DEMUX pattern generator will continue to generate the *SYNC* pattern until certain conditions are met. If the generated pattern matches the demultiplexed input data, then ***MATCH*** will go HIGH. If no match is detected, then the DEMUX will issue itself a ***SKIP*** signal (through the ***SKIP*** edge generator state machine). After a ***SKIP*** has been issued in this manner, the ***MATCH*** signal will be ignored for four ***DCLOCK*** cycles so that transient data during word boundary rotation cannot cause an unintended ***SKIP*** to occur. In this state, the DEMUX will react normally to externally driven ***SKIP*** signals, so the ***SKIP*** pin should be held LOW for this test. Then, the DEMUX will issue ***SKIP*** signals until ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles. On the following ***DCLOCK*** cycle the ***ALIGNED*** signal will go HIGH. Call this the *"aligned"* state. Once aligned, the DEMUX will not issue internally generated ***SKIP*** signals unless the aligned state machine is reset by cycling the ***SYNCPATT*** input.

The expected test sequence is that the *SYNC* pattern will be received until the DEMUX is aligned. Then a *CLK* divide-by-2 pattern (101010101010) will be received for 3 ***DCLOCK*** cycles to signal a change in test mode. The next ***DCLOCK*** cycle will start a pseudo-random pattern that repeats every 4095 ***DCLOCK*** cycles. The DEMUX pattern selector state machine looks for ***ALIGNED*** to be HIGH and ***MATCH*** to be LOW.

This signals a change in test pattern on the input data stream. Notice the ***CLK2*** pattern is not specifically detected, only a mis-match. Thus, once aligned, an error in detecting the *SYNC* pattern will put the DEMUX in pseudo-random test mode.

SENDCLK2 (ECL input pin)

The input pin, ***SENDCLK2***, is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

MATCH (ECL output pin)

The ***MATCH*** pin is the registered output of the 12-bit comparator. ***MATCH***= HIGH indicates that the internally generated pattern matched the incoming demultiplexed data on the previous ***DCLOCK*** cycle.

ALIGNED (ECL output pin)

ALIGNED= HIGH indicates that the DEMUX has found a match on three consecutive ***DCLOCK*** cycles. When ***ALIGNED*** first goes HIGH the DEMUX is ready to transition to the pseudo-random pattern mode. In the intended test flow ***ALIGNED*** is used to drive the ***SYNCPATT*** input on the MUX chip.

ERROR (ECL output pin)

ERROR= HIGH indicates that the internally generated pattern did not match the incoming demultiplexed data on at least one ***DCLOCK*** cycle since the ***ERROR*** latch was reset.

FRAME (ECL output pin)

FRAME= HIGH indicates that the internally generated pattern (001010101010) was sent to the 12-bit comparator on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

VS8001/VS8002 DUT BOARDS

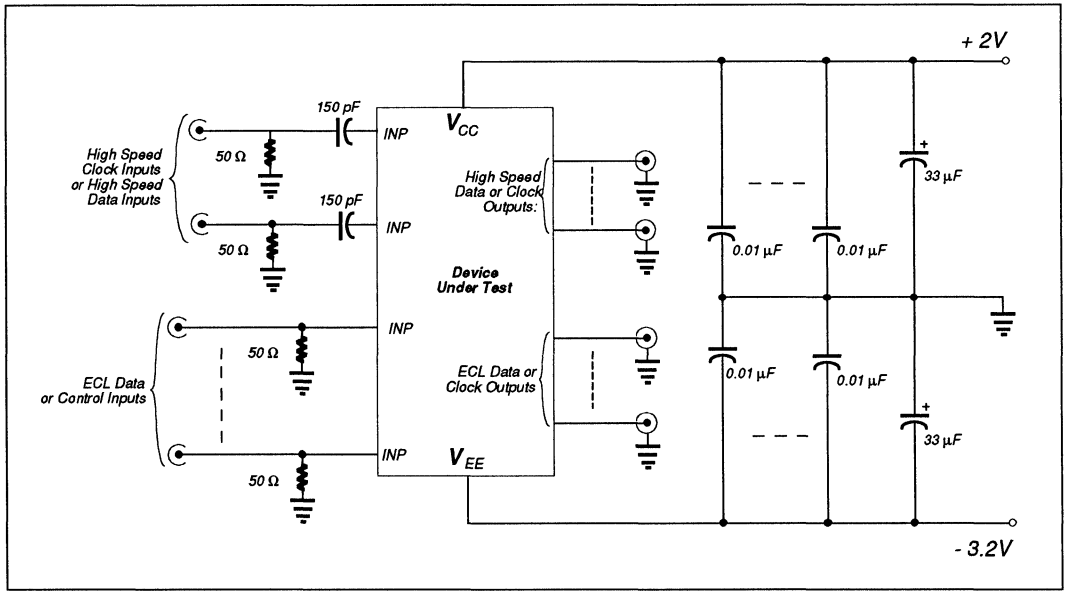
The VS8001DUT and VS8002DUT are circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8001 12:1 Multiplexer and the VS8002 1:12 Demultiplexer in 52 pin leadless chip carriers (LCC).

A schematic of the evaluation board is shown below. This board provides controlled impedance transmission lines for all signals and decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated with 50 Ω in the measuring instrument.

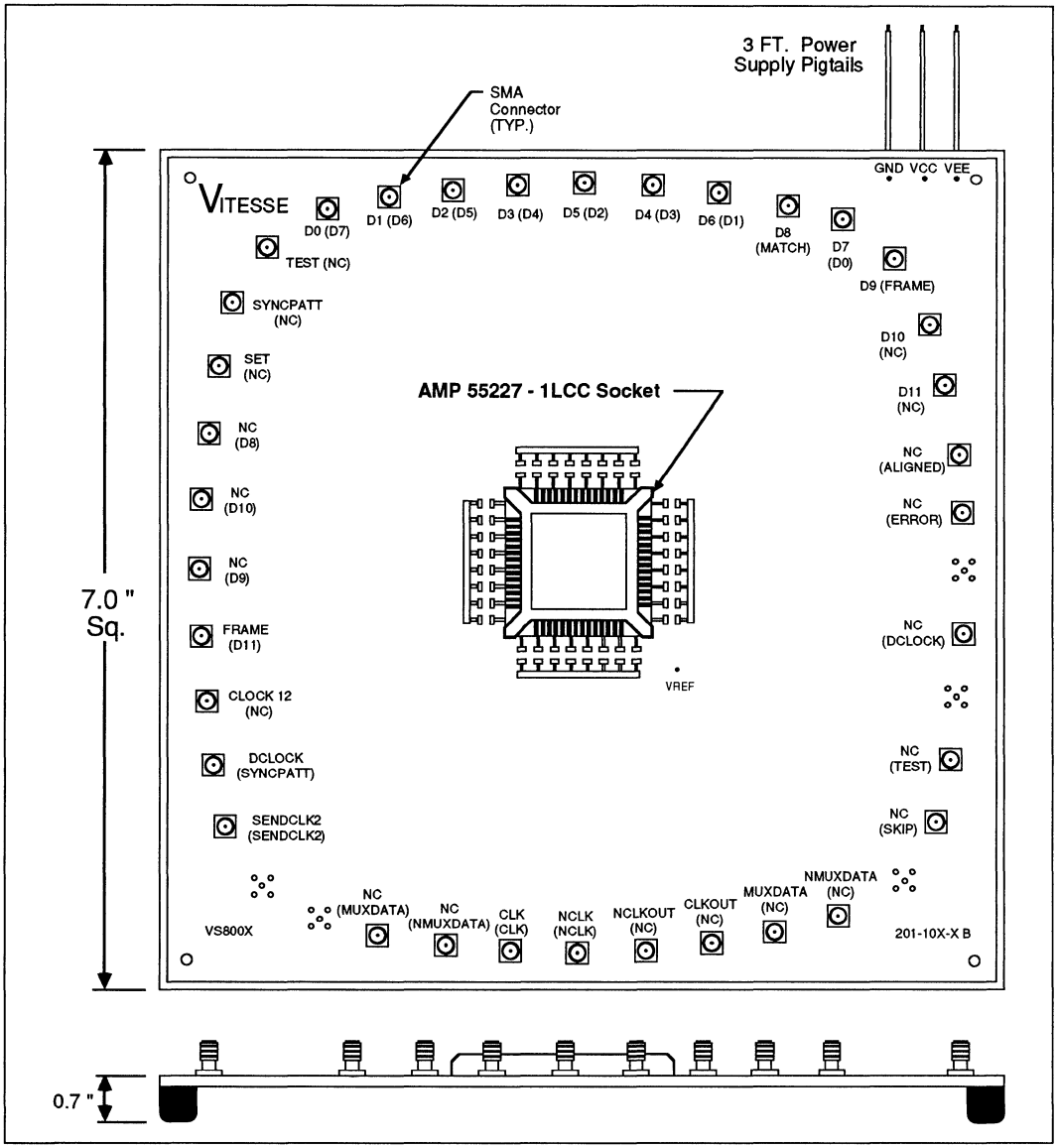
Normally, the VS8001 and VS8002 operate in an ECL environment with standard ECL power forms (Ø V, -2.0 V, and -5.2 V). In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device socket is an AMP 55227-1LCC socket and was chosen for minimum inductance and shortest possible stub length. The figures on the next page show the physical dimensions as well as the names of the connectors on the evaluation boards.

VS8001/VS8002 DUT BOARD SCHEMATIC



VS8001/VS8002 DUT BOARDS



NOTES: 1) This drawing represents both the VS8001 and VS8002 configurations.
(Connection labels given in parentheses are for the VS8002.)
2) NC = No connection.

FEATURES

- Superior performance: serial data up to 2.5 Gb/s
- ECL 100K compatible parallel data inputs/outputs
- Single ECL power supply: V_{EE} = -5.2 V ± 0.26 V
- Available in commercial or industrial temperature ranges
- Proven E/D mode GaAs technology
- Differential or single-ended inputs and outputs
- Low Power Dissipation 1.5 Watts (Typ)
- 28-pin leaded ceramic chip carrier

FUNCTIONAL DESCRIPTION

Introduction

The VS8004 and VS8005 are data conversion devices capable of serial data rates up to 2.5 Gb/s, transforming 4-bit wide parallel data to serial data and serial data to 4-bit wide parallel data.

The VS8004/VS8005 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 28-pin leaded chip carrier. Refer to Section 6, "Packaging" for a complete description of this package.

VS8004

The VS8004 is a high speed 4 bit parallel to serial data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The parallel inputs ***[D(0:3), ND(0:3)]*** accept data at rates up to 625 Mb/s. The differential serial data output ***(SDATA, NSDATA)*** presents the data sequentially from the parallel data inputs at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input ***(CLK, NCLK)***. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output ***(CLK4, NCLK4)***. This clock signal is provided so that incoming parallel signals can be synchronized to arrive at the input data registers simultaneously. An internal bias network is provided at all inputs to simplify capacitive coupling.

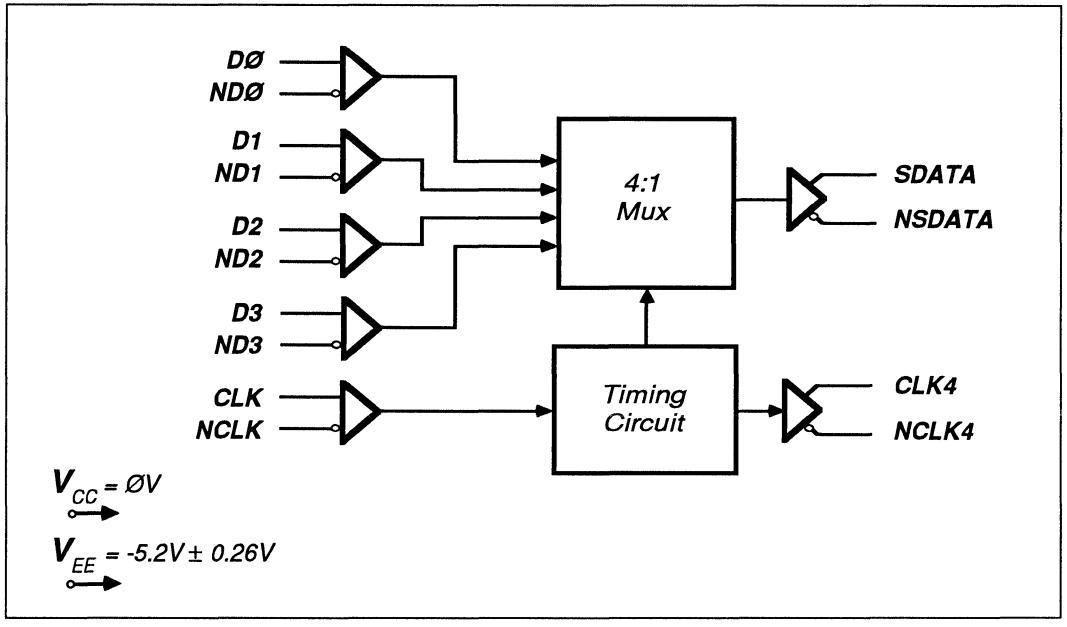
VS8005

The VS8005 is a high speed 4-bit serial to parallel data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The differential serial data inputs ***(SDATA, NSDATA)***accept data at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input ***(CLK, NCLK)***. The parallel outputs ***[D(0:3), ND(0:3)]*** present the data sequentially at rates up to 625 Mb/s. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output ***(CLK4, NCLK4)*** which is synchronous with the parallel data outputs. A control input ***(SKIP, NSKIP)*** is provided to allow realignment of the output parallel word boundaries.

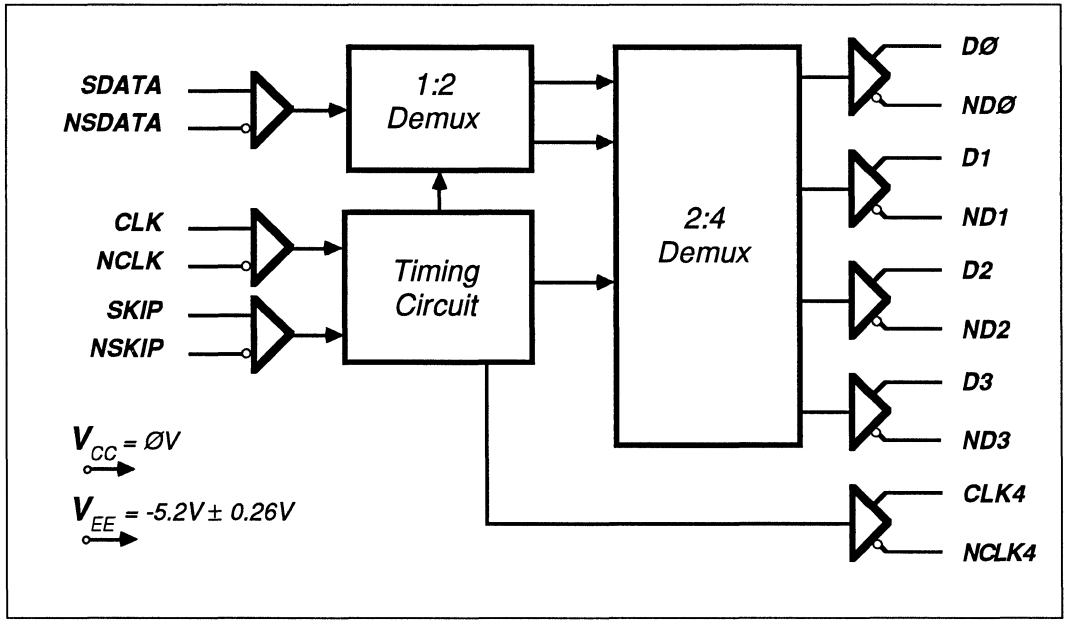
APPLICATIONS

- High speed instrumentation and test equipment
- Fiber-optic communication
- Local area networks
- Serialization of computer backplanes
- Computer to computer interfaces
- Serial control buses for aerospace environments

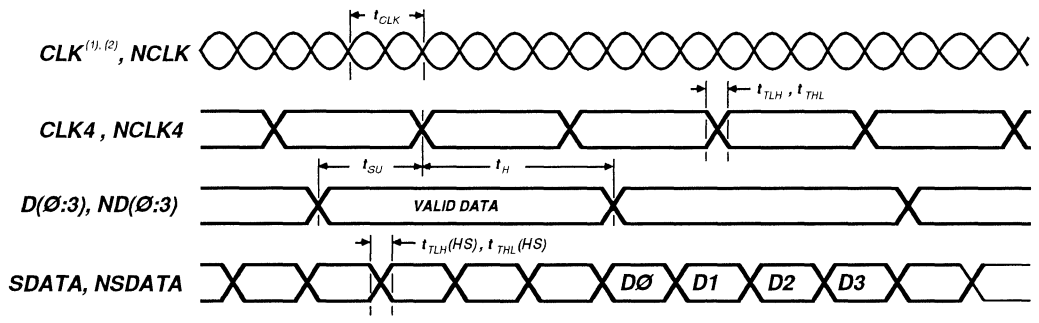
VS8004 BLOCK DIAGRAM



VS8005 BLOCK DIAGRAM



VS8004 WAVEFORMS



NOTES: (1) Falling edge of CLK causes SDATA to change
(2) Falling edge of CLK causes CLK4 to change

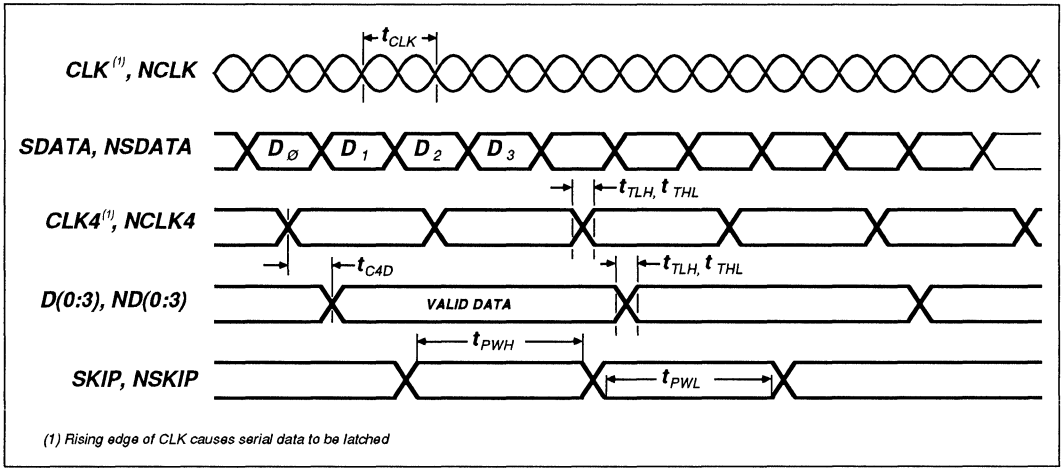
3

VS8004 AC CHARACTERISTICS

(Over recommend operating conditions.)

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High speed clock period	400	—	—	ps
t_{SU}	D(Ø:3), ND(Ø:3), set-up time with respect to CLK4, NCLK4	900	—	—	ps
t_H	D(Ø:3), ND(Ø:3), hold time with respect to CLK4, NCLK4	-300	—	—	ps
t_{TLH} (HS), t_{THL} (HS)	SDATA, NSDATA transition time (LO to HI, HI to LO) while driving 50Ω to -2.0V	—	150	—	ps
jitter	CLK, NCLK to SDATA, NSDATA (max-min), (HI to LO), same part, same pin at constant conditions	—	<50	—	ps
t_{TLH}, t_{THL}	ECL output transition time (LO to HI, HI to LO) while driving 50Ω (CLK4, NCLK4, D(0:3), ND(0:3)) to -2.0V	—	500	—	ps

VS8005 WAVEFORMS



(1) Rising edge of CLK causes serial data to be latched

VS8005 AC CHARACTERISTICS

(Over recommended operating conditions.)

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High speed clock period (CLK, NCLK)	400	—	—	ps
t_{C4D}	CLK4, NCLK4 to D(0:3), ND(0:3)	—	400	—	ps
t_{PWH}	SKIP, NSKIP pulse width (HIGH)	2	—	—	ns
t_{PWL}	SKIP, NSKIP pulse width (LOW)	2	—	—	ns
t_{TLH} t_{THL}	ECL output transition time (LOW to HIGH, & HIGH to LOW) for D(0:3), ND(0:3), and CLK4, NCLK4 (Driving 50Ω)	—	500	—	ps
Phase Margin	SDATA, NSDATA phase timing margin with respect to CLK, NCLK input: $Phase\ Margin = \left(\frac{t_{SU} + t_H}{t_C}\right) 360^c$	135	—	—	degrees

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage, (V_{EE}) ..... V_{CC} (GND) to - 6.0 V
ECL Input Voltage Applied, (V_{ECLIN})(2) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied, (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current (output HIGH), (I_{OUT}) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, (V_{EE}) ..... -5.2 V ± 0.26 V
Operating Temperature Range, (T) (3) ..... (Commercial) 0° to +70°C, (Industrial) -40° to +85°C

3

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without causing permanent damage, but are stress ratings only. Functionality at or above the values listed is not implied, and exposure to these values for extended periods may affect device reliability.
(2) V_{EE} must be applied before any input signal voltage (V_{ECLIN}).
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS

High Speed Inputs

(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal
V_{IL}	Input LOW Voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal

NOTES: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.
2) A reference generator is built in to each high speed input, and these inputs are intended to be AC coupled.
3) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and the power supply (V_{EE}).

DC CHARACTERISTICS (Con't)

High Speed Outputs

(Over recommended operating conditions. V_{CC} = GND, output load = 50Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	—	-0.9	—	V	Terminated to -2.0 V through 50Ω
V_{OL}	Output LOW Voltage	—	-1.8	—	V	Terminated to -2.0 V through 50Ω
ΔV_{OUT}	Output Voltage Swing	0.8	1.0	1.4	V	Output Load, 50Ω to -2V

NOTE: Differential high speed output pairs must be terminated identically

ECL Inputs and Outputs

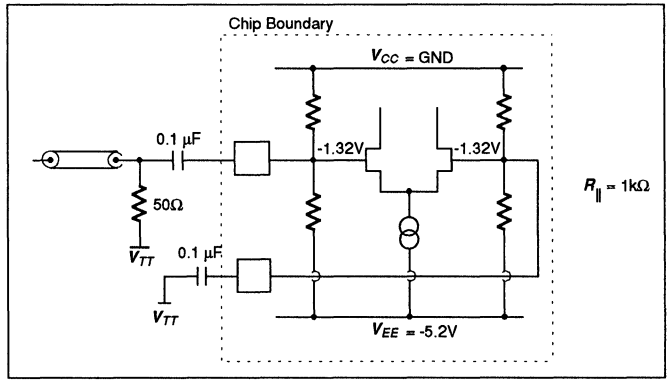
(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, output load = 50 Ω to -2.0 V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1020	—	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW Voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH Voltage	-1040	—	-600	mV	Guaranteed HIGH for ECL inputs
V_{IL}	Input LOW Voltage	-2000	—	-1600	mV	Guaranteed LOW for ECL inputs
I_{IH}	Input HIGH Current	—	500	1000	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW Current	-1000	-500	—	µA	$V_{IN} = V_{IL}$ (min)

NOTES: 1) Differential ECL output pairs must be terminated identically.
2) Leakage currents exceed ECL specifications due to the internal bias network which is connected to all inputs.

PARALLEL DATA, BYCLK INPUTS

ECL inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -1.32 Volts on both the true and complement inputs.



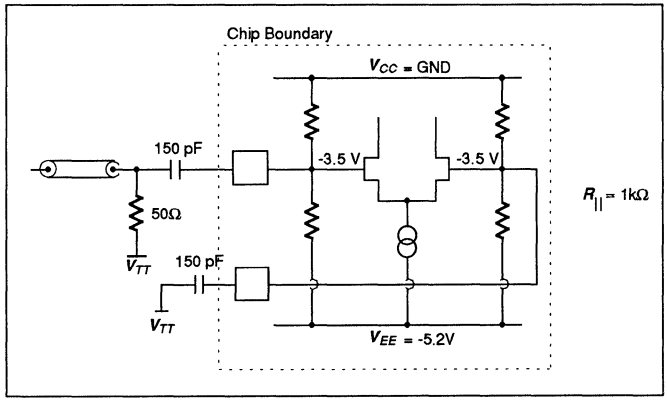
POWER DISSIPATION

(Over recommended operating conditions. V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8004			VS8005			Units
		MIN	TYP	MAX	MIN	TYP	MAX	Units
I_{EE}	Power supply current (V_{EE})	—	270	350	—	310	400	mA
P_D	Power dissipation	—	1.5	1.9	—	1.6	2.2	W

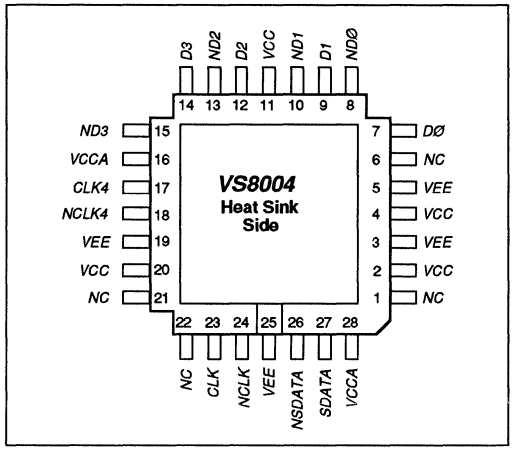
HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated at right.



3

VS8004 PIN DIAGRAM

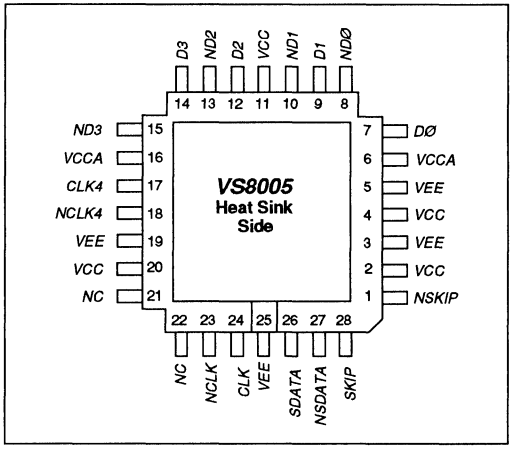


VS8004 PIN DESCRIPTION

Pin #	Name	I/O	Description
23, 24	***CLK, NCLK***	I	Differential high speed clock inputs
27, 26	***SDATA, NSDATA***	O	Differential high speed serial data outputs
17, 18	***CLK4, NCLK4***	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	***D(Ø:3), ND(Ø:3)***	I	Differential parallel data inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2 V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
16, 28	V_{CCA}		Ø V output ground connection
1, 6, 21, 22	***NC***		No connection

NOTE:
1) The heat sink is connected to V_{EE} (pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2 V normally), do not connect this heat sink to ground. (Ø V).

VS8005 PIN DIAGRAM



VS8005 PIN DESCRIPTION

Pin #	Name	I/O	Description
24, 23	***CLK, NCLK***	I	Differential high speed clock inputs
26, 27	***SDATA, NSDATA***	I	Differential high speed serial data inputs
17, 18	***CLK4, NCLK4***	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	***D(Ø:3), ND(Ø:3)***	I	Differential parallel data inputs (ECL)
28, 1	***SKIP, NSKIP***	I	Differential word boundary inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2 V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
6, 16	V_{CCA}		Ø V output ground connection
21, 22	***NC***		No connection.

NOTES:

1) *The heat sink is connected to V_{EE} (pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2 V normally), do not connect this heat sink to ground.*
2) *The falling edge of SKIP causes realignment of the parllel word boundary making parallel data invalid for three CLK4, NCLK4 (12 CLK, NCLK) periods.*

3

VS8004/VS8005 DUT BOARDS

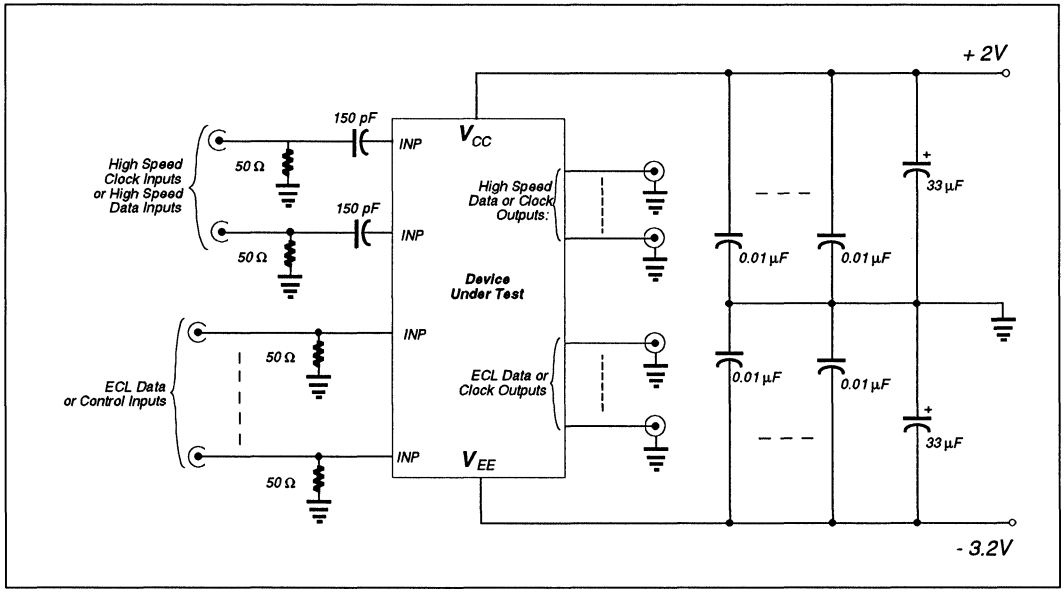
The VS8004FDUT/VS8005FDUT evaluation boards are special purpose circuit boards which provide a test bed suitable for evaluating the high performance characteristics of the VS8004 4:1 Multiplexer or the VS8005 1:4 Demultiplexer in the 28 pin leaded ceramic chip carrier.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument.

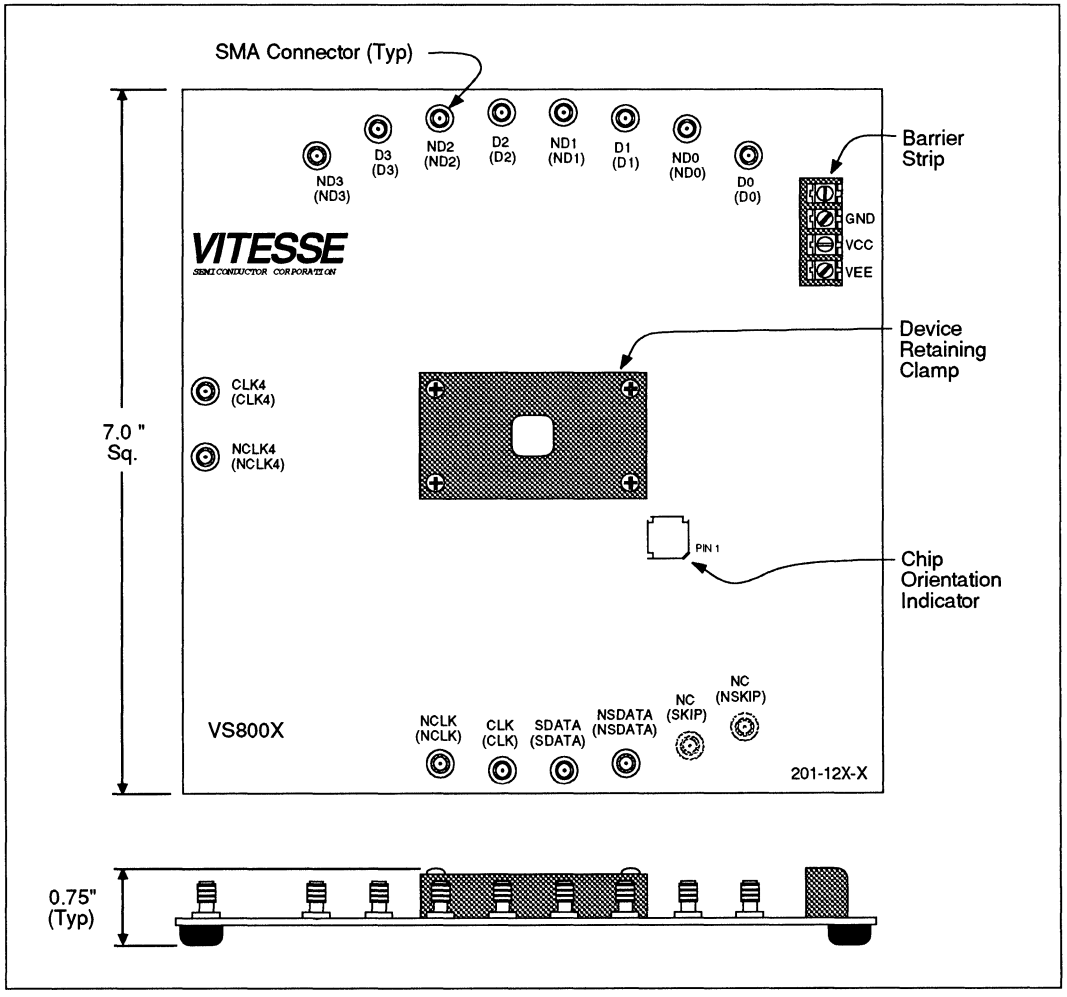
Normally, the VS8004 and VS8005 operate in an ECL environment with standard ECL power buses: ØV and -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device to be tested is held in place with a pressure retaining fixture. The figure on the following page shows the physical dimensions and the connection labels for the evaluation boards.

VS8004/VS8005 DUT BOARD SCHEMATICS



VS8004/VS8005 DUT BOARDS



NOTES: 1) This drawing represents both the VS8004FDUT and VS8005FDUT configurations. (Connection labels given in parentheses are for the VS8005.)
2) NC = No connection. Note: These connectors are omitted on the VS8004FDUT version of this evaluation board.

FEATURES

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Standard ECL power supplies: V_{EE} = -5.2 V ± 0.26 V, V_{TT} = -2.0 V ± 0.1 V
- VS8010: 8 bit Mux/Demux and SONET frame detection and recovery
- VS8011: 8 bit Mux
- VS8012: 8 bit Demux and SONET frame detection and recovery
- Compatible with STS-3 to STS-24 SONET applications

FUNCTIONAL DESCRIPTION

Introduction

The VS8010, VS8011 and VS8012 are high speed SONET compatible 8-bit data conversion devices capable of serial data rates up to 1.25 Gb/s. The VS8010 series can be used for STS-3 through STS-24 SONET applications.

The VS8010 Series are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52 pin leaded or leadless chip carrier. Refer to Section 6, "Packaging" to a complete description of this package.

VS8010

The VS8010 integrates an 8:1 multiplexer, 1:8 demultiplexer, and SONET frame detection and recovery circuitry all on one chip.

8:1 Multiplexer Circuit

The 8:1 multiplexer accepts 8 parallel ECL data inputs ***[D(1:8)]*** at rates up to 155 Mb/s and multiplexes them into a single bit stream at speeds up to 1.25 Gb/s. The parallel data inputs are clocked into the input registers with ***BYCLK***, an ECL input operating at up to 155 MHz. The high speed clock input ***(CLKI)*** is divided by 8 ***(CLK8)*** and used to synchronize the parallel data to the timing generator. ***CLK8*** then loads the parallel data into the buffer registers. An on-chip circuit detects internal set up and hold violations caused by improperly related ***BYCLK*** and ***CLK8*** falling edges. An external signal ***(SYNC)*** may be used to correct ***CLK8*** phase by 180°. ***SYNC*** is high. If a setup or hold violation has been detected, a ***SYNC*** input causes ***CLK8*** to be inverted on the next ***BYCLK*** falling edge, thereby guaranteeing a safe ***CLK8*** and ***BYCLK*** relationship. If no setup and hold violation has been detected ***SYNC*** has no impact on the circuit.

The high speed differential clock input is brought on-chip at ***CLKI, CLKIN***. The high speed differential serial data is provided at the ***DO, DON*** outputs. The high speed differential clock signal is transmitted off chip via the high speed outputs ***CO, CON***.

1:8 Demultiplexer Circuit

The 1:8 demultiplexer converts serial data at up to 1.25 Gb/s into an 8-bit parallel data stream at up to 155 Mb/s. The high speed differential serial input is at ***DI, DIN***. Valid parallel data is clocked out by the divide by 8 clock output ***BYCKO***. The demultiplexer also contains SONET frame detection and recovery circuitry.

Frame Recovery Circuit

The frame recovery circuits are enabled by a falling edge on the ***OOFN*** input. Once enabled, the frame recovery circuits start looking for the SONET framing sequence. Once the frame is detected, a confirmation signal is sent off-chip through the low power ECL output ***FP***. The frame detection confirmation signal also disables the frame recovery circuits.

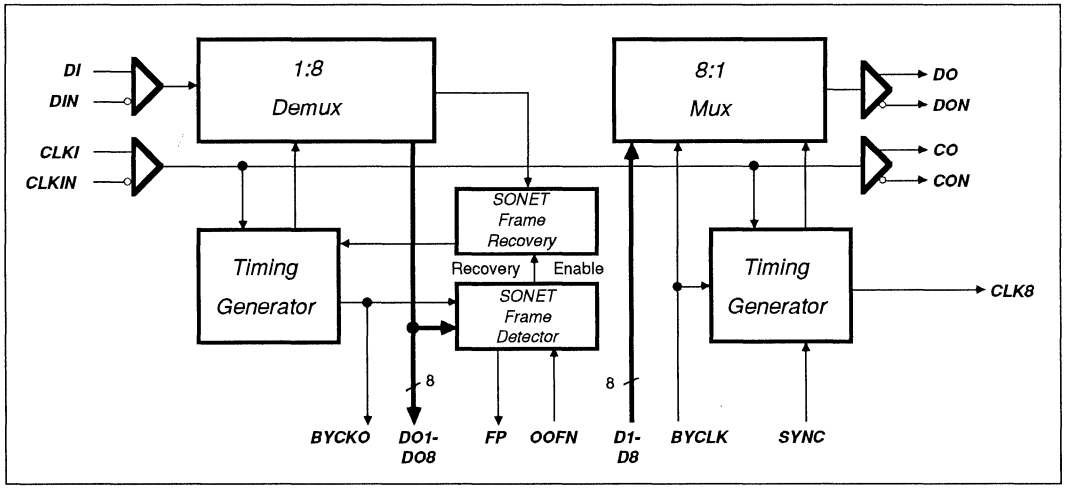
VS8011

The VS8011 is a high speed 8:1 multiplexer. The operation of the VS8011 exactly the same as that of the VS8010 8:1 Multiplexer circuitry described previously.

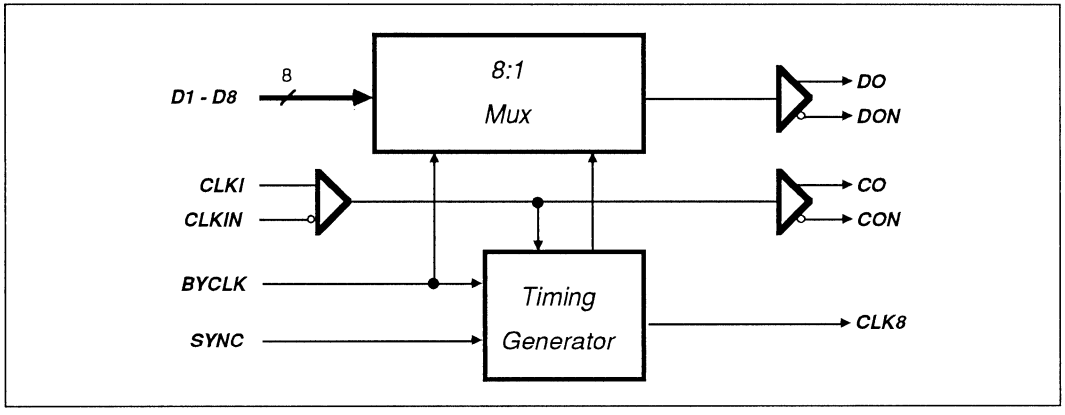
VS8012

The VS8012 integrates a 1:8 Demux and SONET frame recovery and detection circuitry on one chip. The operation of the VS8012 exactly the same as that of the VS8010 1:8 Demultiplexer and Frame Recovery circuits with the following exception. The frame recovery circuits are enabled by a falling edge on the ***OOFN*** ECL input when the additional ***FDIS*** ECL input is low. When the ***FDIS*** input is high the falling edge of ***OOFN*** disables the frame recovery circuit. The ***FDIS*** input is included to provide an alternative means of disabling the frame recovery circuit during device evaluation. In normal operation this input is wired to V_{TT} and the frame recovery circuit is disabled when serial F1's and F2's appear at the high speed differential serial data input ***(DI, DIN)***.

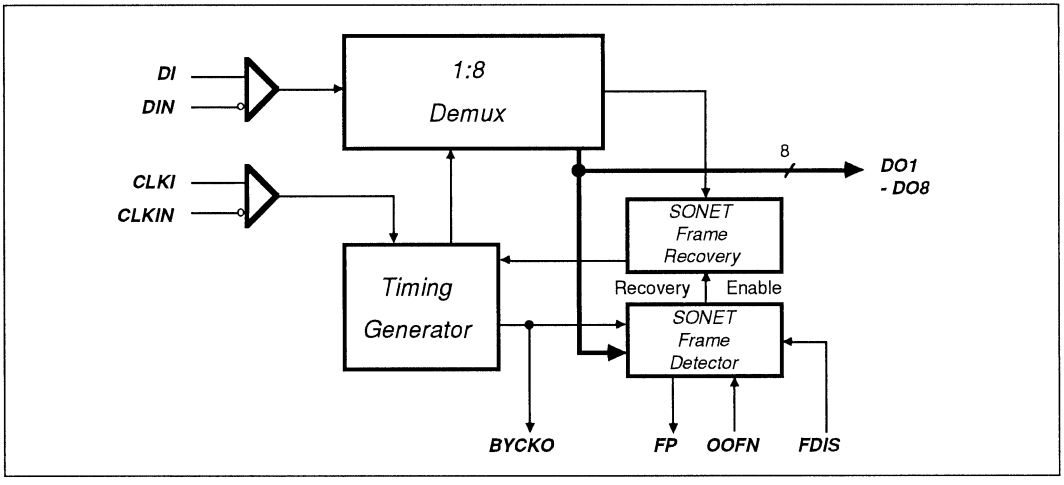
VS8010 BLOCK DIAGRAM



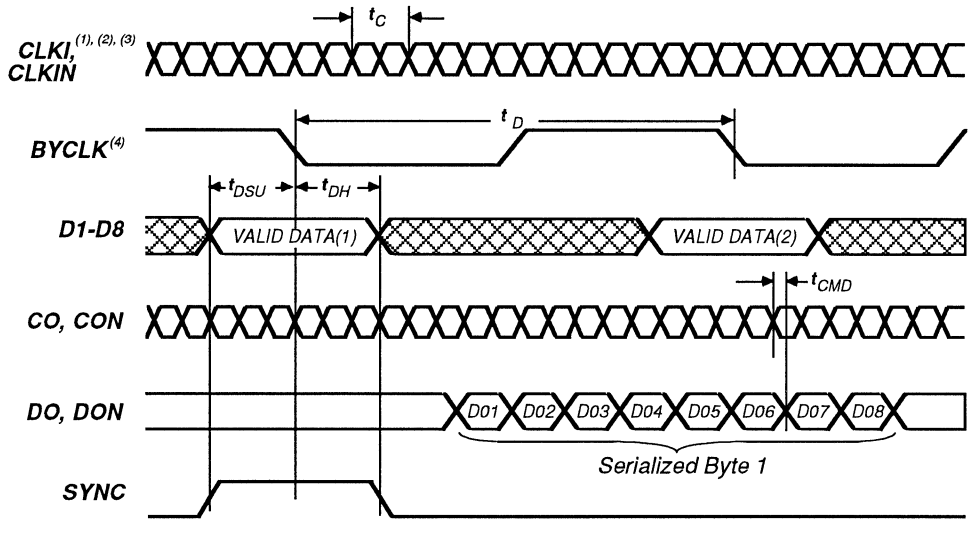
VS8011 BLOCK DIAGRAM



VS8012 BLOCK DIAGRAM



MULTIPLEXER WAVEFORMS (VS8010, VS8011)



NOTES:
(1) Falling edge of CLKI causes DO to change
(2) Falling edge of CLKI causes CO to fall
(3) Falling edge of CLKI causes CLK8 to change
(4) Falling edge of BYCLK latches parallel data

= Don't care

8 x clock period of CLKI = BYCLK period

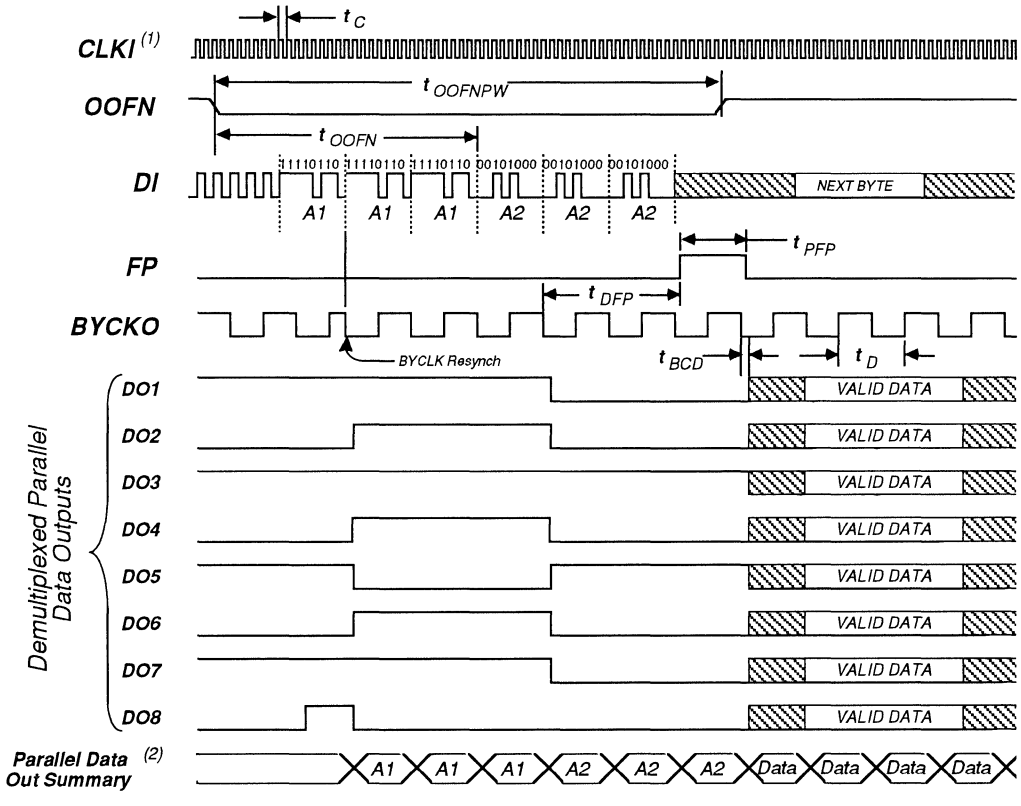
MULTIPLEXER AC CHARACTERISTICS (VS8010, VS8011)

(Over recommended operating conditions.)

Parameter	Description	Min	Typ	Max	Units
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period ($t_D = t_C$ x 8)	6.4	—	—	ns
t_{DSU}	Parallel data set-up time with respect to BYCLK	2.0	—	—	ns
t_{DH}	Data hold time with respect to BYCLK	1.0	—	—	ns
t_{CMD}	High speed clock output (CO, CON) to muxed data output (DO, DON) timing	—	500	—	ps
jitter	CLKI, CLKIN to DO, DON max-min, (HIGH to LOW), same part, same pin at constant conditions	—	<50	—	ps

** The parts are guaranteed by design to operate from DC to a maximum frequency of 1.25 GHz.*

DEMULTIPLEXER WAVEFORMS (VS8010, VS8012)



NOTES:
(1) Falling edge of CLK causes serial data to be latched
(2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above utilize an STS-3 framing sequence for convenience. Thus, in this example, valid data is output after the third A2 in the SONET framing sequence.

3

DEMULTIPLEXER AC CHARACTERISTICS (VS8010, VS8012)

(Over recommended operating conditions.)

Parameter	Description	Min	Typ	Max	Units
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period ($t_D = t_C \times 8$)	6.4	—	—	ns
t_{DFP}	FP rising edge from parallel data output change from F1 to F2 ($t_{DFP} = t_D \times 2$)	—	12.8	—	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	6.4	—	—	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D \times 4$)	—	25.6	—	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	6.4	—	—	ns
Phase Margin	Serial data phase timing margin with respect to high speed clock input: $Phase\ Margin = \left(\frac{t_{SU} + t_H}{t_C}\right) 360^c$	135	—	—	degrees
t_{BCD}	Falling edge of **BYCKO** to valid parallel data output	t_c	t_c+0.5	t_c+1.5	ns

** If t_C changes, all the remaining parameters change as indicated by the equations.*

VS8010/VS8012 SONET FRAME RECOVERY AND DETECTION

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit.

STS LEVEL	LINE RATE (Mb/S)	# OF A1 BYTES	# OF A2 BYTES
STS-3	155.520	3	3
STS-9	466.560	9	9
STS-12	622.080	12	12
STS-18	933.120	18	18
STS-24	1244.16	24	24
STS-48	2488.32	48	48

Example: STS-24 has 24 A1s and 24 A2s:
$A1_1A1_2A1_3$.....$A1_{24}A2_1A2_2A2_3$.....$A2_{24}$

Frame Recovery Circuit

The VS8010 Series SONET recovery circuits operate from STS-3 to STS-24. The frame recovery circuits look for 3 A1s followed by 3 A2s. The byte clock out ***(BYCKO)*** and parallel byte data out ***(DO_1-DO_8)*** become invalid on the falling edge of ***OOFN*** and become valid when A1 changes to A2. The frame recovery circuits align the received serial data on byte boundaries for demultiplexing by controlling the timing generator. The byte boundary alignment is based on specific A1 and A2 byte recognition.

The VS8010/12 have been designed to recognize 3 A1s followed by 3 A2s, and therefore recognize frames and align on byte boundaries for STS-3 through STS-24 line rates. As shown below, the framing sequence always contains 3 A1s followed by 3 A2s:

STS-24	(24 A1s & 24 A2s)
STS-18	(18 A1s & 18 A2s)
STS-12	(12 A1s &12 A2s)
STS-9	(9 A1s & 9 A2s)
STS-3	(3 A1s & 3 A2s)

The falling edge of ***OOFN*** must occur at least 4 byte clock periods before A1 changes to A2. The pulse width of ***OOFN*** must be at least 1 byte clock period.

Frame Detection Circuit

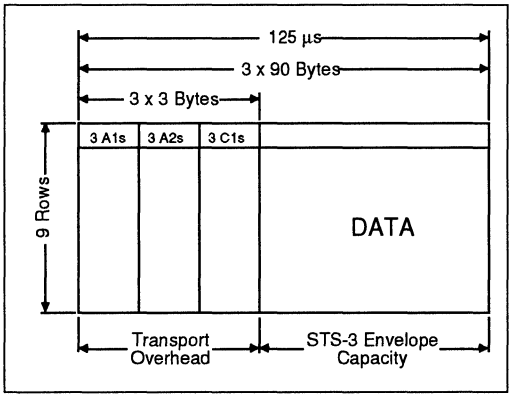
The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. If 3 A1 bytes followed by 3 A2 bytes are detected, then a frame confirmation signal is sent off-chip on the ECL output ***FP***. The rising edge of the ***FP*** pulse occurs 2 byte clock periods after A1 changes to A2 on the demultiplexer parallel data outputs. The ***FP*** pulse width is one byte clock period (refer to demultiplexer waveforms).

The frame detection circuitry also disables the frame recovery circuits once 3 A1 bytes are followed by 3 A2 bytes. The frame detector sends an ***FP*** pulse every frame when 3 A1s are followed by 3 A2s independent of the condition of the input ***OOFN***.

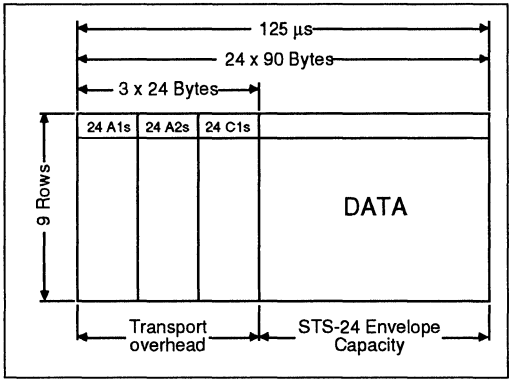
Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the ***OOFN*** ECL input with ***FDIS*** held low. The ***OOFN*** must be at least one byte clock period wide. It must occur at least 4 byte clock periods before the A1/A2 boundary. The circuit requires at least 2 A1 bytes followed by 2 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following A1 and 2 A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recovery and output alignment will occur only on the first A1 byte following a ***OOFN*** falling edge input. Frame recognition will occur for each word boundary aligned A1A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the ***FP*** ECL output pin. This ***FP*** pulse will appear one byte period after the second A2 byte appears on the parallel data output pins.

STS-3 FRAME



STS-24 FRAME



NOTE: A1s & A2s: SONET framing sequence
C1s: STS Frame ID

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} +0.7 V to -6.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature (3), (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage, (V_{TT}) ..... -2.0 V ± 0.1V
Power Supply Voltage, (V_{EE}) ..... -5.2 V ± 0.26 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN} and V_{HSIN}) must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS

ECL Inputs/Outputs

(Over recommended operating range with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-700	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min
V_{REF}	ECL input reference, V_{BB} (2)	—	-1.29	—	V	

NOTE: 1) Differential ECL output pins must be terminated identically.
2) V_{REF} input is used to supply external VBB on chip for ECL 10K ECL compatibility.

High Speed Inputs and Outputs: CLKI, CLKIN, DO, DON

(Over recommended operating conditions. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW for high speed inputs
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load, 50 Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50 Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.6	0.8	1.2	V	Output load, 50 Ω to -2.0 V

NOTES: 1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.
2) If a high speed input is used single-ended, a 150pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed outputs must be terminated identically.

3

HIGH SPEED DIFFERENTIAL CLOCK (C0,C0N) OUTPUTS (VS8010, VS8011)

V_{EE} = -5.2 ± 0.26 V, V_{CC} = GND, T_C = 0° to 70° C, Output load = 50 Ω to -2.0 V.)

The clock output swing at 1.25 GHz is 400 mVp-p from each output, centered at approximately -1.5 V
The clock output swing at DC is 1.0 Vp-p from each output, centered at approximately -1.5 V

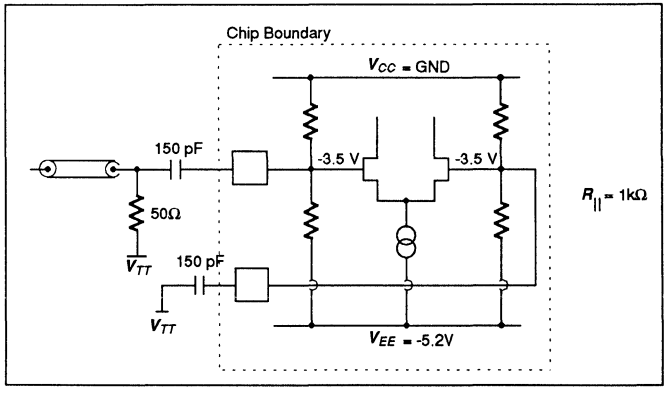
POWER DISSIPATION

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8010			VS8011			VS8012			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power supply current from V_{EE}	—	380	720	—	300	600	—	300	600	mA
I_{TT}	Power supply current from V_{TT}	—	450	900	—	110	220	—	125	250	mA
P_D	Power dissipation	—	2.9	5.8	—	1.9	3.7	—	2.0	3.8	W

HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated at right.



VS8010 EXAMPLE APPLICATION: STS-24 SYSTEM

The objective of the system is to multiplex and demultiplex 8 data channels at the STS-24 line rate with SONET frame recovery capability. In this example the system is implemented using the two VS8010s as follows:

8:1 Multiplexer

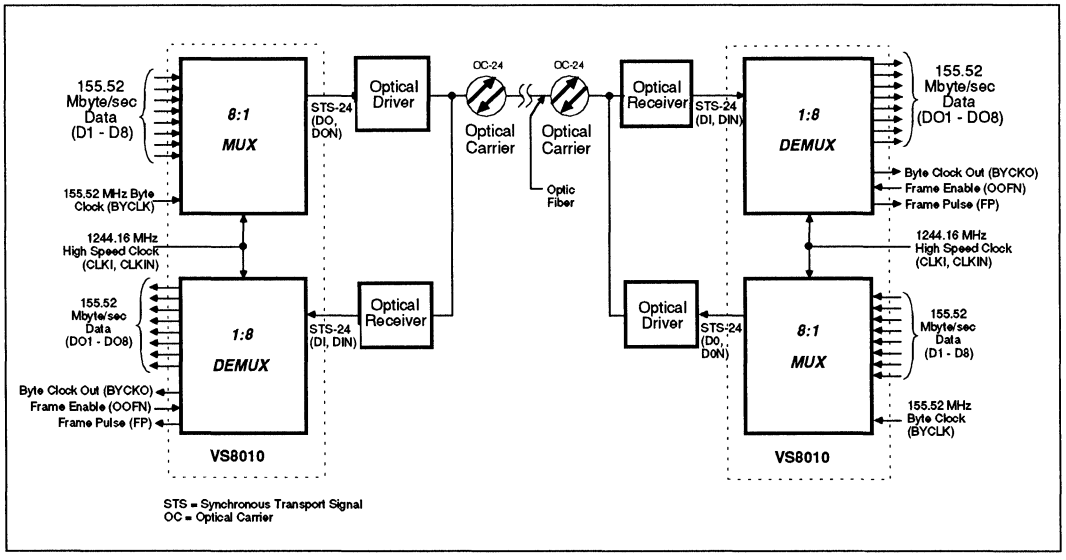
Data at a line rate of 155.52 Mbytes/sec is registered at the inputs using the 155.52 MHz byte clock. The 1244.16 MHz clock is used to generate timing signals for the mutiplexing function. The multiplexed output at 1244.16 Mbits/sec is generated at the serial data output (DO, DON) of the VS8010.

1:8 Demultiplexer

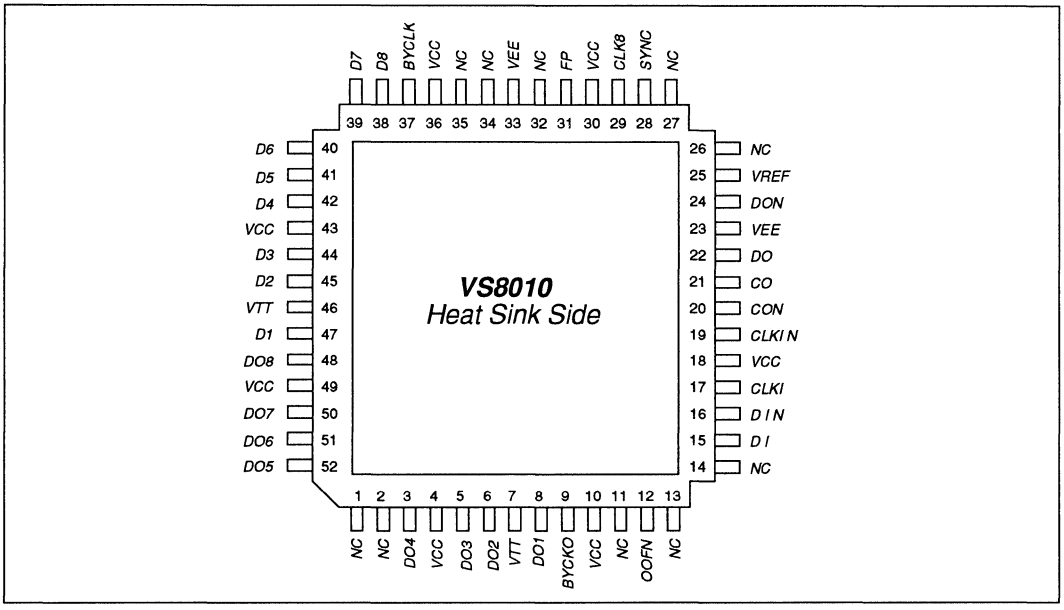
The 1:8 demultiplexer receives serial data at 1244.16 Mbits/sec and generates parallel data at 155.52 Mbytes/sec along with a byte clock output of 155.52 MHz. The demultiplexer also contains the SONET frame recovery and detection circuitry.

During system start-up the ***OOFN*** input receives a falling edge from the system control to recover the SONET frame and align on byte boundaries. Once the frame is aligned, the ***FP*** pulse is generated on every SONET frame. If for any reason the ***FP*** pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the ***OOFN*** input (HIGH to LOW) to recover the SONET frame and align on byte boundaries, thus bringing the system back to a synchronized condition. The ***FP*** pulse begins appearing again on every frame.

SONET STS-24 SECTION LEVEL NODE



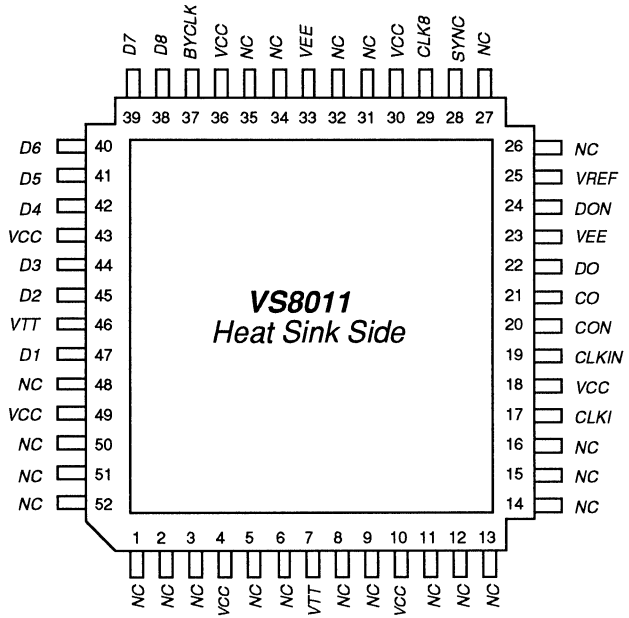
VS8010 PIN DIAGRAM



VS8010 PIN DESCRIPTION

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	***DO1 - DO8***	O	Parallel ECL data outputs
47, 45, 44, 42 - 38	***D1 - D8***	I	Parallel ECL data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
9	***BYCKO***	O	Divide by 8 clock ECL output
37	***BYCLK***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
29	***CLK8***	O	Mux divide by 8 clock ECL output
15, 16	***DI, DIN***	O	High speed differential serial data input
12	***OOFN***	I	Frame recovery enable ECL input
31	***FP***	O	Frame detection confirmation ECL output
28	***SYNC***	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 11, 13, 14, 26, 27, 32, 34, 35	***NC***		No connection

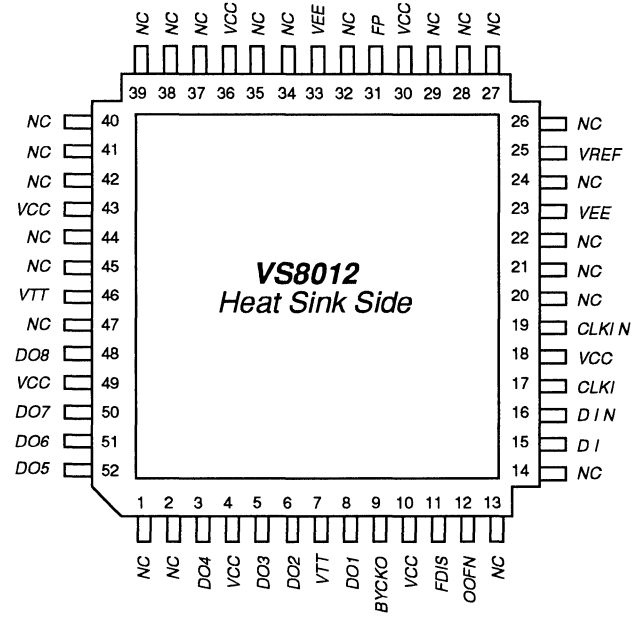
VS8011 PIN DIAGRAM



VS8011 PIN DESCRIPTION

Pin #	Name	I/O	Description
47, 45, 44, 42 - 38	***D1 - D8***	I	Parallel ECL data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
37	***BYCLK***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
29	***CLK8***	O	Mux divide by 8 clock ECL output
28	***SYNC***	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1 - 3, 5, 6, 8, 9, 11 - 16, 26, 27, 31, 32, 34, 35, 48, 50 - 52	***NC***		No connection

VS8012 PIN DIAGRAM



VS8012 PIN DESCRIPTION

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	***DO1 - DO8***	O	Parallel ECL data outputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
9	***BYCKO***	O	Divide by 8 clock ECL output
15, 16	***DI, DIN***	O	High speed differential serial data input
12	***OOFN***	I	Frame recovery enable ECL input
11	***FDIS***	I	Frame recovery disable ECL input
31	***FP***	O	Frame detection confirmation ECL output
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation and low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 13, 14, 20 - 22, 24, 26 - 29, 32, 34, 35, 37 - 42, 44, 45, 47	***NC***		No connection

VS8010DUT BOARD

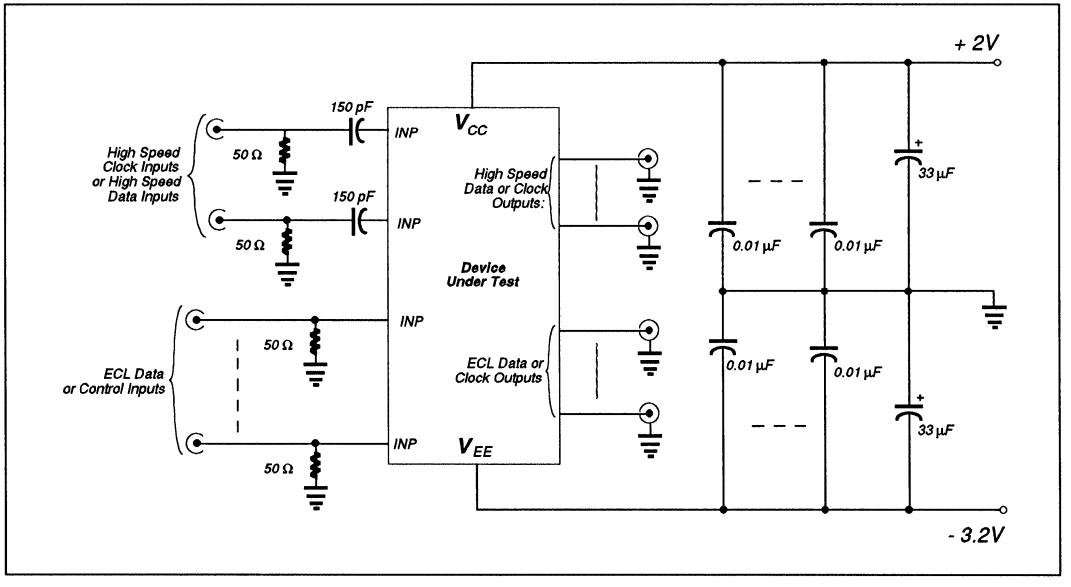
The VS8010DUT is a general purpose circuit board for the VS8010 series which provides a test bed suitable for evaluating the performance characteristics of the VS8010 series in the 52 pin LCC package. The evaluation board is generic to the VS8010 series, and is configured with I/Os which are specific to the VS8010 series.

The figure below is a schematic of this circuit board. This board provides a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

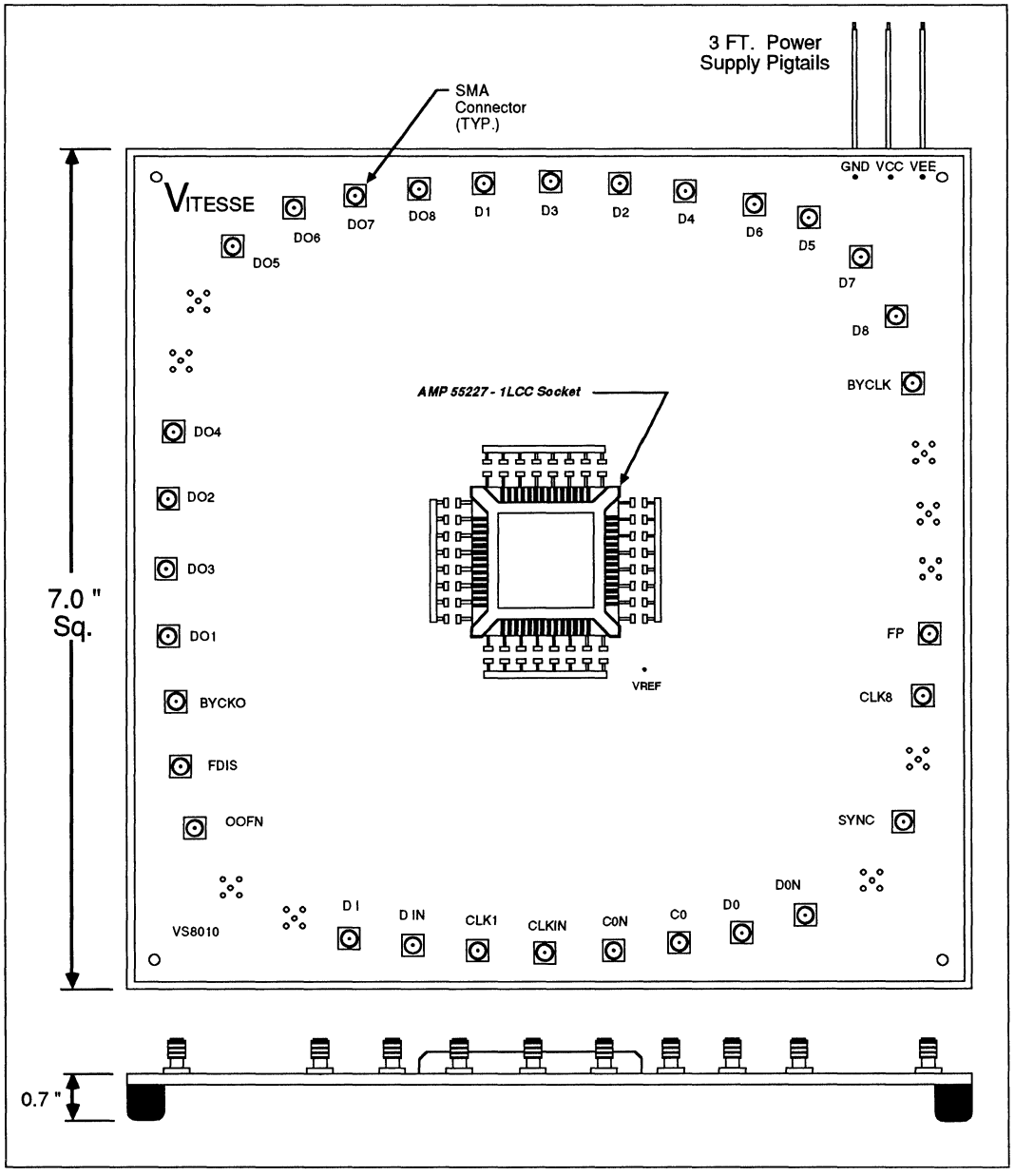
Normally, the VS8010 series operates in an ECL environment with standard ECL power buses: Ø V, -2 V, -5.2 V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device socket is an AMP 55227-1 LCC socket and was chosen for minimum inductance and shortest possible stub length. The figure on the next page shows the physical dimensions and the SMA connection labels for the VS8010DUT evaluation board.

VS8010DUT BOARD SCHEMATIC



VS8010DUT DIMENSIONS AND CONNECTION DIAGRAM



FEATURES

- Superior performance: serial data up to 2.5 Gb/s
- Compatible with SONET STS-3 to STS-48 applications
- 8-bit wide ECL 100K compatible parallel data I/Os
- Internal self-adjusting clock in the VS8021 for simple clock to parallel data alignment
- SONET frame recovery circuitry incorporated into the VS8022 demultiplexer
- Standard ECL power supplies: V_{EE} = -5.2 V, V_{TT} = -2.0 V
- All data and clock inputs and outputs are differential (inputs can be wired to be driven single-ended)
- 52-pin leaded ceramic chip carrier

FUNCTIONAL DESCRIPTION

The VS8021 and VS8022 are high speed SONET interface devices capable of handling serial data at rates up to 2.5 Gbits/second. These products can be used for STS-3 through STS-48 SONET applications.

These products are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded ceramic chip carrier. Refer to Section 6, "Packaging" for a complete description of this package. The following are individual descriptions of each product.

VS8021

The VS8021 contains an 8:1 multiplexer and a self-positioning timer. The 8:1 multiplexer accepts 8 parallel differential ECL data inputs ***(D1-D8, D1N-D8N)*** at rates up to 312.5 Mbits/sec and multiplexes them into a serial differential bit stream output ***(DO, DON)*** at rates up to 2.5 Gbits/sec.

The internal timing of the VS8021 is built around the high speed clock (up to 2.5 GHz) delivered onto the chip through a differential input ***(CLKI, CLKIN)***. This signal is subsequently echoed at the high speed differential output ***(CO, CON)***.

The parallel data inputs are clocked to on-chip input registers with an externally supplied differential ECL input ***(BYCLK, BYCLKN)*** operating at the same rate as the data inputs. An internal byte clock, which is a divide by 8 version of the high speed clock, is used to transfer the data to a set of buffer registers. This internal byte clock is brought off chip at the ECL output ***CLK8, CLK8N***.

Internal circuitry monitors the internal and external byte clocks and generates an ***ERR*** signal if a timing violation is detected. This signal can be connected directly to the ***SYNC*** input. An active ***SYNC*** input allows the VS8021 timing to shift, positioning it properly against the external byte clock, ***CLK8, CLK8N***.

Another divide by 8 version of the high speed clock is brought off chip at ***RCLK, RCLKN***. The phase of this clock is not affected by the self-adjusting circuitry, therefore it can be used as a system reference clock. ***RCLK, RCLKN*** can be used by the system designer to generate ***BYCLK, BYCLKN***. The self-positioning timer and ***RCLK, RCLKN*** allow for the creation of very tight parallel data timing for the VS8021.

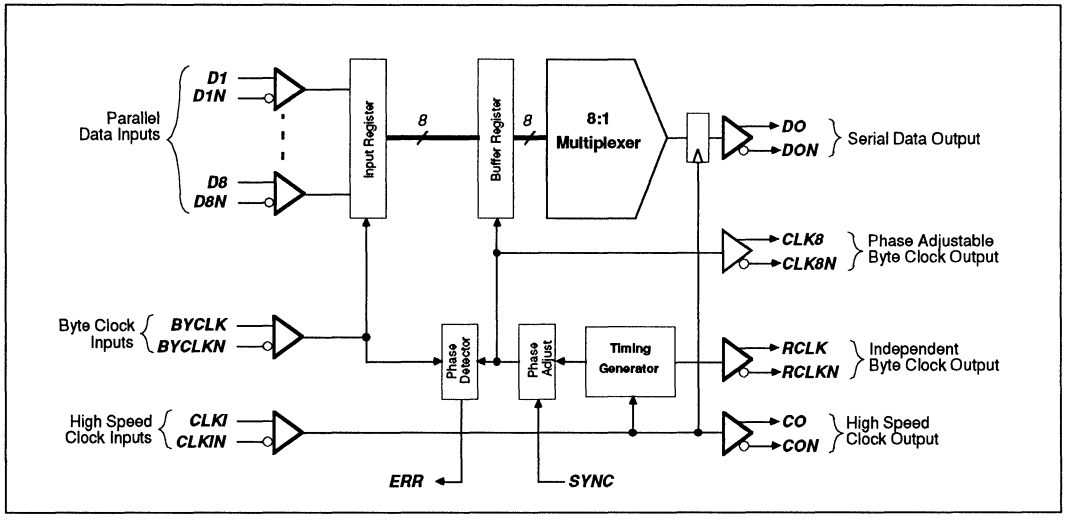
VS8022

The VS8022 contains both a 1:8 demultiplexer and SONET frame recovery circuitry. The 1:8 demultiplexer accepts a serial data input ***(DI, DIN)*** at rates up to 2.5 Gbits/second and converts it into 8 parallel differential ECL data outputs ***(D1-***

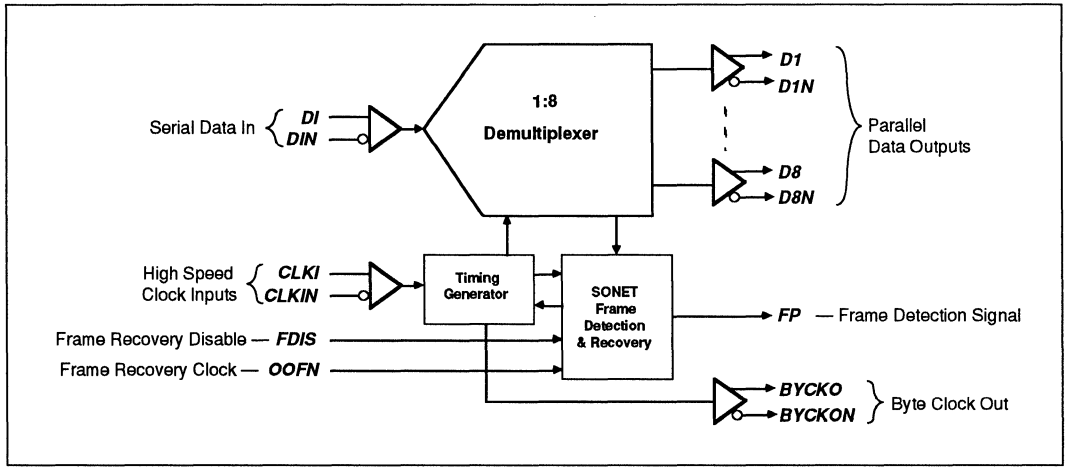
D8, D1N-D8N) at rates up to 312.5 Mbits/sec. Valid parallel data outputs are indicated by the divide by 8 differential clock outputs ***BYCKO***, ***BYCKON***.

The VS8022 also contains a SONET frame recovery circuit. The frame recovery circuits are enabled by a falling edge on the ***OOFN*** ECL input when the ***FDIS*** input is low. Once enabled the frame recovery circuit starts looking for the SONET framing sequence. Once the frame is detected, the word boundary is realigned, a confirmation signal is sent off-chip through the ***FP*** ECL output and the frame recovery circuits are disabled.

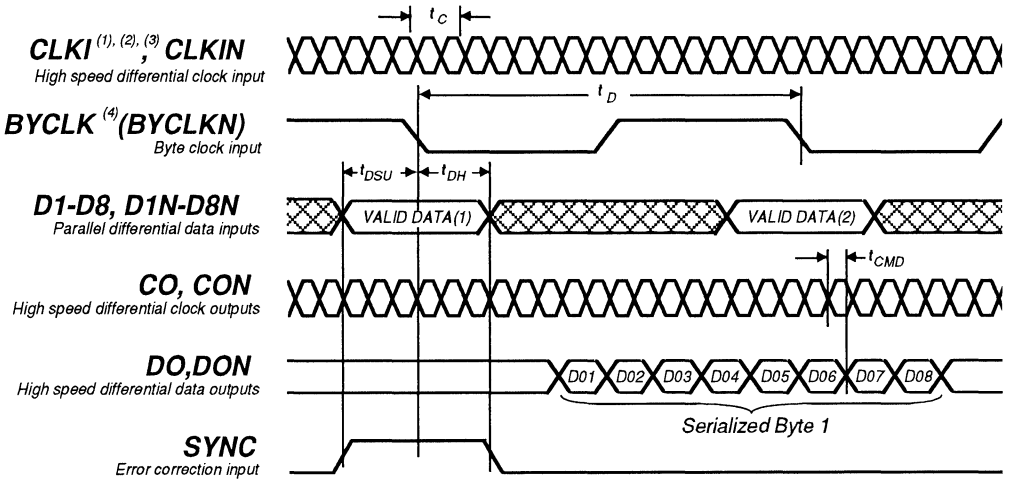
VS8021 BLOCK DIAGRAM



VS8022 BLOCK DIAGRAM



MULTIPLEXER WAVEFORMS (VS8021)



NOTES: (1) Falling edge of CLKI causes DO to change
(2) Falling edge of CLKI causes CO to fall
(3) Falling edge of CLKI causes RCLK, CLK8 to change
(4) Falling edge of BYCLK latches parallel data

CLKI (CLKIN) *period x 8 =* ***BYCLK (BYCLKN)*** *period.*

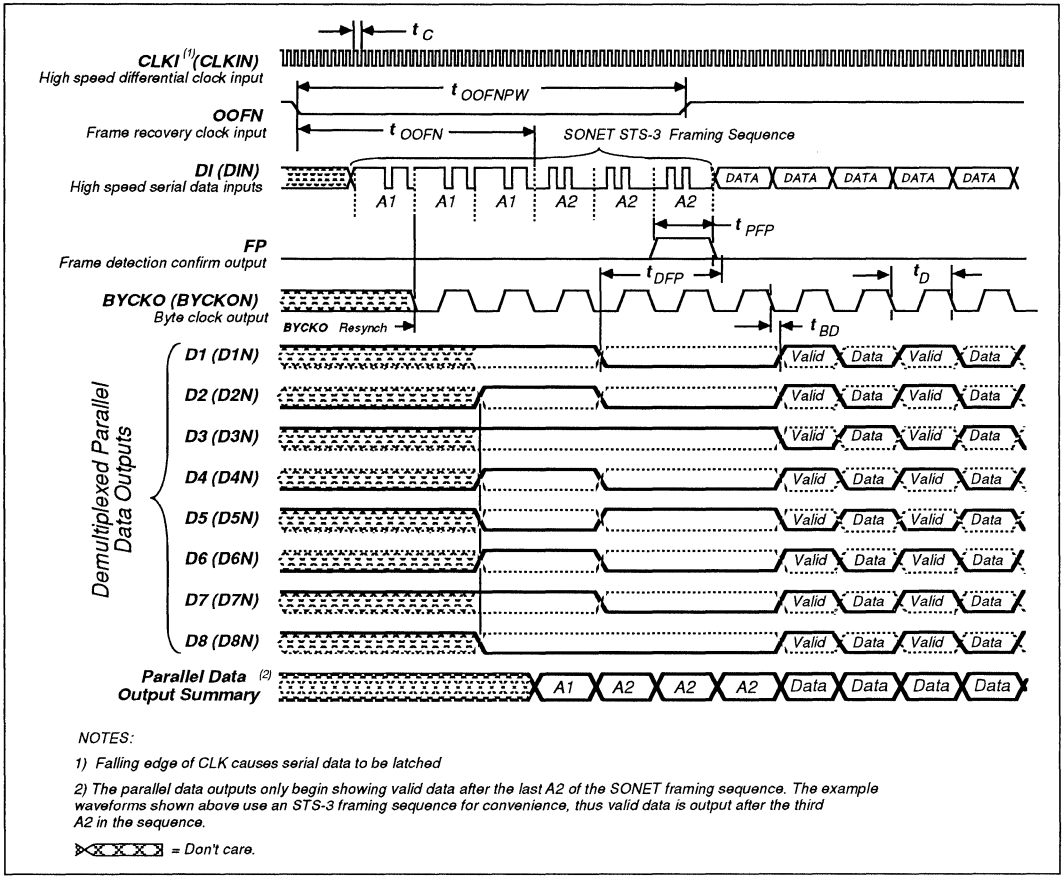
= *Don't care.*

MULTIPLEXER AC CHARACTERISTICS (VS8021): *Over recommended operating range*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t_C	Clock period *	400	—	—	ps
t_D	BYTE clock period	3.2	—	—	ns
t_{DSU}	Parallel data set-up time	1.0	—	—	ns
t_{DH}	Data hold time	1.0	—	—	ns
t_{CMD}	High speed clock output (CO, CON) to muxed data output (DO, DON) timing	220	—	350	ps
jitter	CLKI, CLKIN to DO, DON (max-min, (HIGH to LOW), same part, same pin at constant conditions	—	<50	—	ps

** The parts are guaranteed to operate from DC to a maximum frequency of 2.5 GHz.*

DEMULTIPLEXER WAVEFORMS (VS8022)



NOTES:

1) Falling edge of CLK causes serial data to be latched

2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above use an STS-3 framing sequence for convenience, thus valid data is output after the third A2 in the sequence.

⋈ = *Don't care.*

VS8022 DEMULTIPLEXER AC CHARACTERISTICS *(Over recommended operating range.)*

Parameter	Description	Min	Typ	Max	Units
t_C	Clock period *	400	—	—	ps
t_D	BYTE clock period ($t_D = t_C \times 8$)	3.2	—	—	ns
t_{BD}	BYTE clock output to valid data	0.5	1.0	2.0	ns
t_{DFP}	FP rising edge from parallel data output change from A1 to A2 ($t_{DFP} = t_D \times 2$)	—	6.4	—	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	3.2	—	—	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D \times 4$)	12.8	—	—	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	3.2	—	—	ns
Phase Margin	Serial data phase timing margin with respect to high speed clock: $Phase\ Margin = \left(\frac{t_{SU} + t_H}{t_C}\right) 360^c$	135	180	—	degrees

** If t_C changes, all the remaining parameters change as indicated by the equations.*

VS8022 SONET FRAME RECOVERY AND DETECTION

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit.

STS LEVEL	LINE RATE (Mb/S)	# OF A1 BYTES	# OF A2 BYTES
STS-3	155.520	3	3
STS-9	466.560	9	9
STS-12	622.080	12	12
STS-18	933.120	18	18
STS-24	1244.16	24	24
STS-48	2488.32	48	48

Example: STS-48 has 48 A1s and 48 A2s:
$A1_1A1_2A1_3$.....$A1_{48}A2_1A2_2A2_3$.....$A2_{48}$

Frame Recovery Circuit

The frame recovery circuit is designed to scan the serial data stream, looking for the A1 byte. When it finds the A1 pattern, it adjusts internal timing so that the serial data is properly demultiplexed onto the eight parallel outputs. Subsequently, the MSB of the A1 byte will appear in the D1 position and LSB of the A1 byte will appear in the D8 position. This word boundary alignment causes the ***BYCKO, BYCKON*** output to be resynchronized.

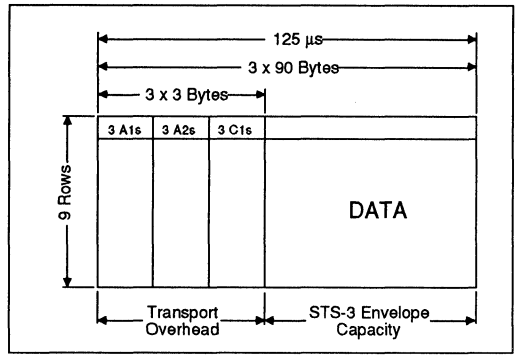
Frame Detection Circuit

The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. This circuit requires a minimum of 2 A2 bytes in order to generate a pulse on the ***FP*** output. This pulse on the ***FP*** output will reset the frame recovery circuit, so that no further resynchronization will occur.

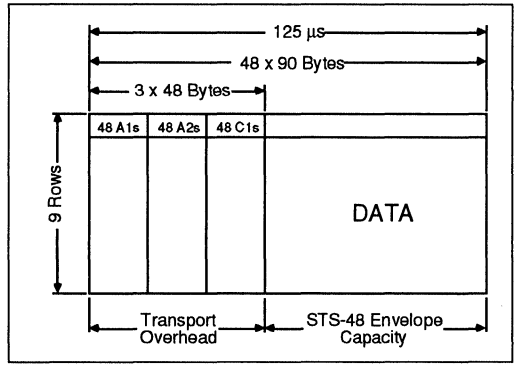
Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the ***OOFN*** ECL input with ***FDIS*** held low. The ***OOFN*** must be at least one byte clock period wide. It must occur at least 4 byte clock periods before the A1/A2 boundary. The circuit requires at least 2 A1 bytes followed by 2 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following A1 and 2 A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recovery and output alignment will occur only on the first A1 byte following a ***OOFN*** falling edge input. Frame recognition will occur for each word boundary aligned A1A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the ***FP*** ECL output pin. This ***FP*** pulse will appear one byte period after the second A2 byte appears on the parallel data output pins.

STS-3 FRAME



STS-48 FRAME



NOTE: A1s & A2s: SONET framing sequence
C1s: STS Frame ID

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} +0.7 V to -6.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature (3), (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.0 V ± 0.1 V
Power Supply Voltage, (V_{EE}) ..... -5.2 V ± 0.26 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

3

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN} and V_{HSIN}) must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.
(4) When using internal ECL 100K reference level.

DC CHARACTERISTICS

ECL Inputs/Outputs

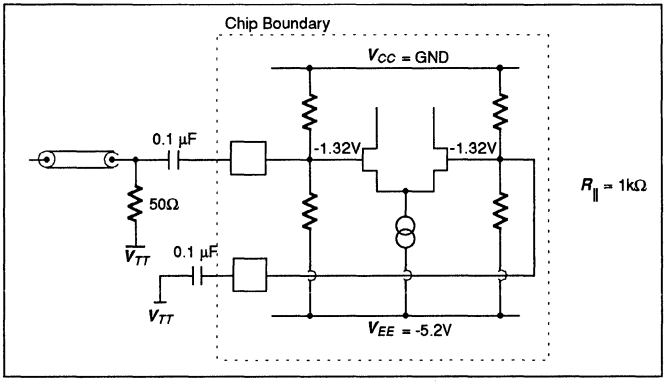
(Over recommended operating range with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load 50Ω to V_{TT}

NOTE: Differential ECL output pins must be terminated identically.

PARALLEL DATA, BYCLK INPUTS

ECL inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -1.32 Volts on both the true and complement inputs.



DC CHARACTERISTICS *(con't)*

High Speed Inputs and Outputs

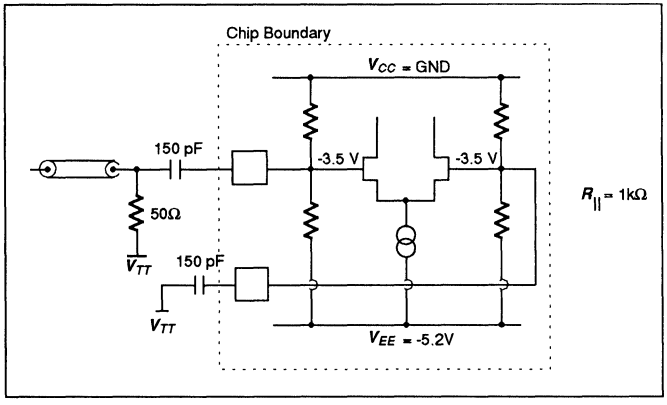
(Over recommended operating conditions. V_{CC} = GND, Output load = 50Ω to -2.0V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load, 50Ω to -2.0 V

NOTES: 1) Built in reference generator, the high speed inputs are designed for AC coupling.
2) If a high speed input is used single-ended, a 150pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed output pins must be terminated identically.
4) ESD protection is minimal for the high speed input pins, therefore, proper procedures should be used when handling this product.

HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -3.5 Volts on both the true and complement inputs. Single-ended, AC coupled operation is illustrated at right.



POWER DISSIPATION

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8021			VS8022			Units
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power supply current from V_{EE}	—	350	700	—	350	700	mA
I_{TT}	Power supply current from V_{TT}	—	100	200	—	100	200	mA
P_D	Power dissipation	—	2.2	4.3	—	2.2	4.3	W

EXAMPLE APPLICATION: STS-48 SONET SYSTEM LINK

The objective in this example is to multiplex/demultiplex 8 channels at the STS-48 line rate with SONET frame recovery capability. The system can be implemented using the VS8021 and VS8022 as follows:

8:1 Multiplexer

Data at a line rate of 311.04 Mbytes/sec is registered at the inputs using the externally provided 311.04 MHz byte clock. ***ERR*** is connected to ***SYNC*** for retiming of the input word. The 2488.32 MHz clock is used to generated timing signals for the mutiplexing function. The muxed output at 2488.32 Mbits/sec is generated at the serial data output of VS8021.

1:8 Demultiplexer

The 1:8 demultiplexer receives serial data at 2488.32 Mbits/sec and generates parallel data at 311.04 Mbytes/sec along with a byte clock output of 311.04 MHz. The demux also has the SONET frame recovery and detection circuitry.

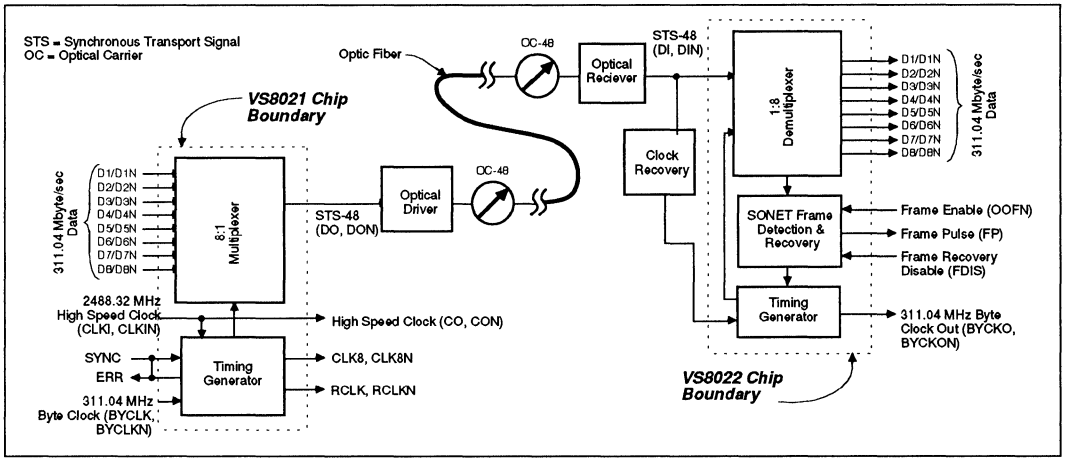
During system start-up ***OOFN*** input receives a falling edge from the system control to recover the SONET frame and align on byte boundaries. Once the frame is aligned, the ***FP*** pulse is generated on every SONET frame. If for any reason the ***FP*** pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the ***OOFN*** input (High to Low) to recover the SONET frame and align on byte boundaries, bringing the system back to a synchronized condition. After synchronization is achieved, the ***FP*** pulse starts again on every frame.

ESD Protection

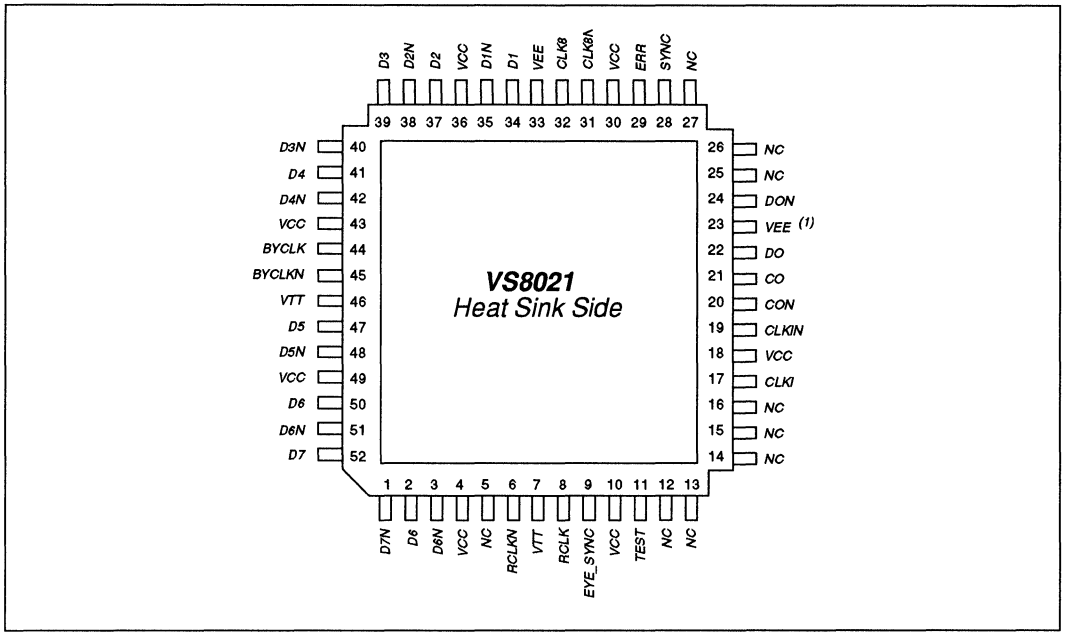
Electrostatic discharge protection is provided for ECL I/O's and high speed clock and data I/O's to the following minimum limits:

*ECL I/O's, High Speed Clock and Data O's..... **1000V***
*High Speed Clock and Data I's..... **500V***

STS-48 SONET SYSTEM LINK



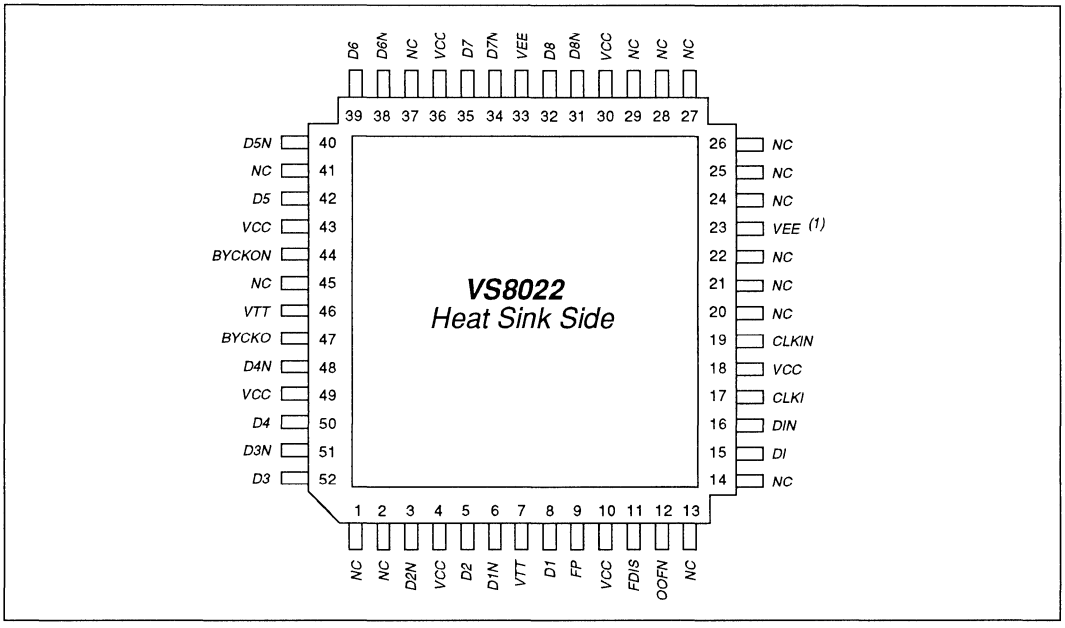
VS8021 PIN CONFIGURATION



NOTE: 1) Pin #23 on both parts is connected to the heat sink. Connect to VEE or most negative chip voltage.

Pin #	Name	I/O	Description
1-3,34,35,37-42,47,48,50-52	***D1-D8, D1N-D18***	I	Parallel ECL differential data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
44, 45	***BYCLK, BYCLKN***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
31, 32	***CLK8, CLK8N***	O	Phase adjustable ÷8 differential ECL clock output
6, 8	***RCLK, RCLKN***	O	Independent ÷8 differential ECL clock output
29	***ERR***	O	Error detection ECL output
28	***SYNC***	I	Error correction ECL input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic
23(1), 33	V_{EE}		-5.2 V supply for high speed logic
11	***TEST***		Test pin connection
9	***EYE_SYNC***		Synchronize internal test structure
5, 12 - 16, 25, 26, 27	***NC***		No connection

VS8022 PIN CONFIGURATION



NOTE: 1) Pin #23 on both parts is connected to the heat sink.Connect to VEE or most negative chip voltage.

Pin #	Name	I/O	Description
3,5,6,8,31,32, 34,35,38-40,42, 48, 50-52	***D1-D8, D1N-D8N***	O	Parallel ECL differential data outputs.
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs.
44, 47	***BYCKO, BYCKON***	O	Divide by 8 clock ECL outputs.
15, 16	***DI, DIN***	I	High speed differential serial data inputs.
12	***OOFN***	I	Frame recovery clock enable ECL input.
11	***FDIS***	I	Frame Disable. Disables framing circuitry when high.
9	***FP***	O	Frame Pulse. Recognizes in-frame A1A2A2.
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection.
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic.
23(1), 33	V_{EE}		-5.2 V supply for high speed logic.
1,2,9, 11, 13,14,20-22,24,25, 26-29, 37,41,45	***NC***		No connection.

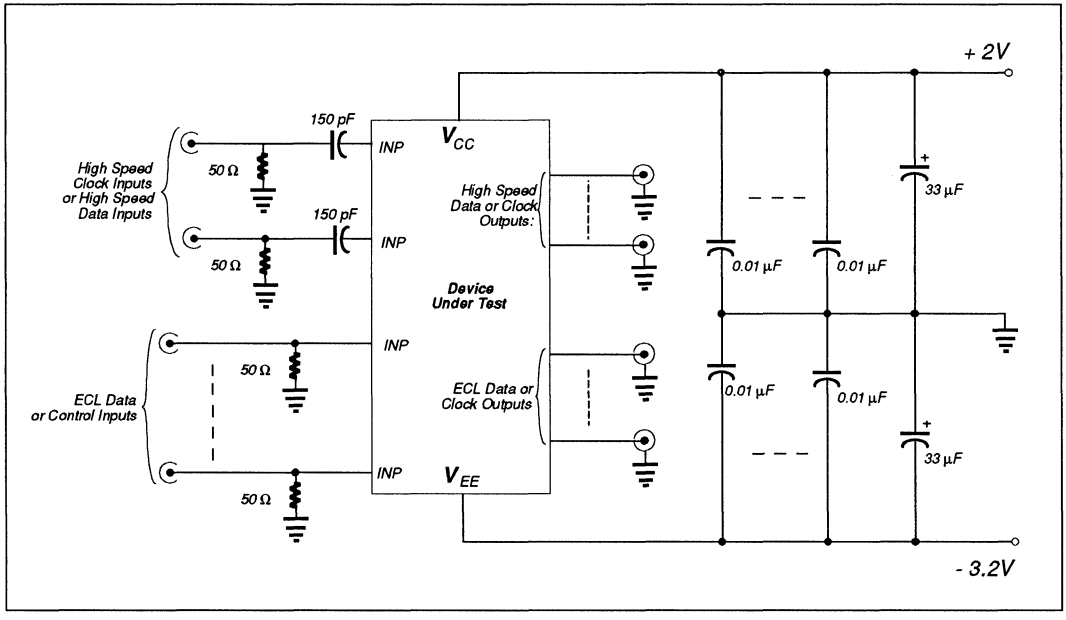
VS8021/VS8022 DUT BOARDS

The VS8021/VS8022 DUT boards are special purpose circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8021 8:1 Multiplexer or the VS8022 1:8 Demultiplexer in the 52 pin LDCC package.

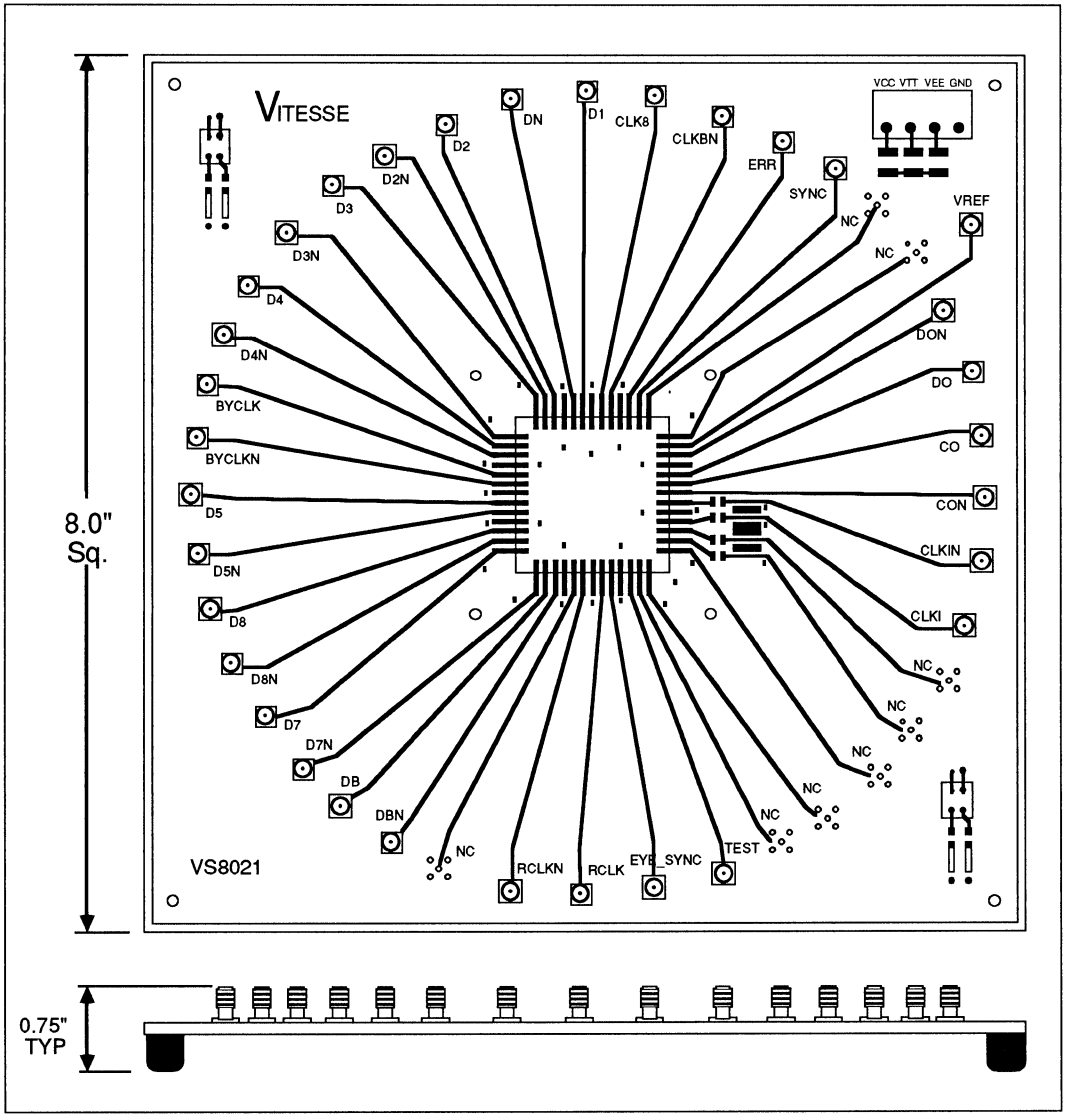
The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VS8021 and VS8022 circuits operate in an ECL environment with standard ECL power buses: 0V, -2V, -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus. The device to be tested is held in place with a pressure retaining fixture. The figures on the following pages shows the physical dimensions and the connections labels for the evaluation boards.

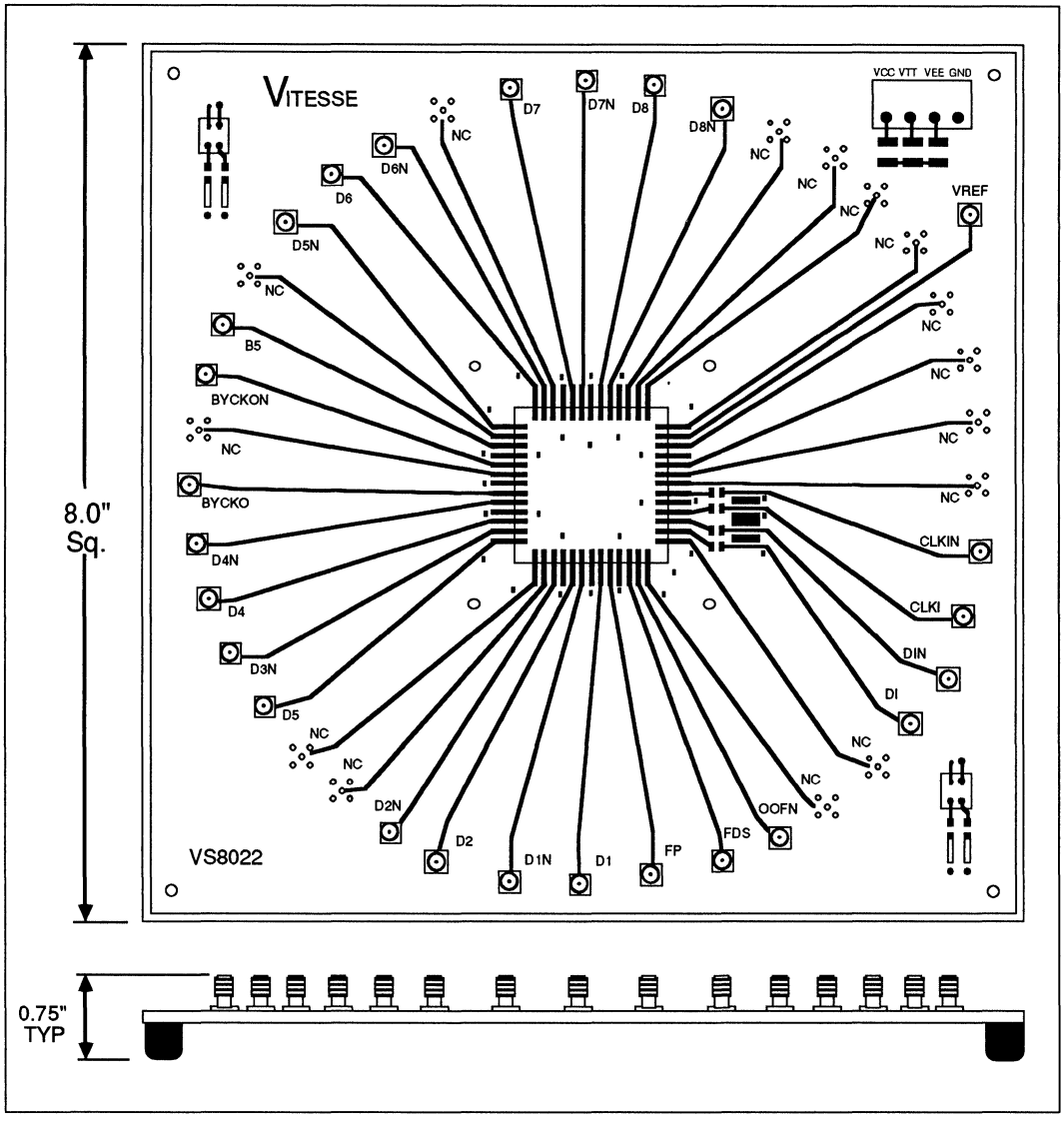
VS8021DUT/VS8022DUT BOARD SCHEMATIC



VS8021DUT DIMENSIONS AND CONNECTION DIAGRAM



VS8022DUT DIMENSIONS AND CONNECTION DIAGRAM



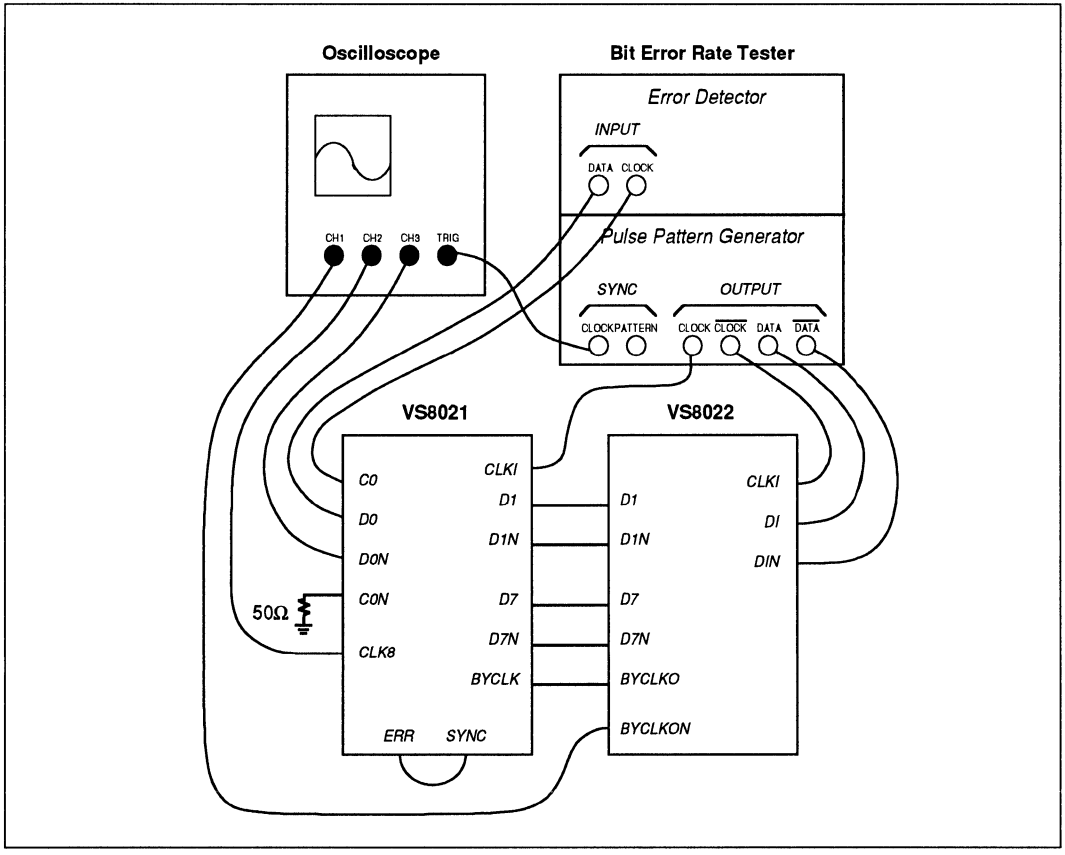
VS8021DUT/VS8022DUT TEST SETUP

Test equipment that is equal to or better than the following is recommended for testing the VS8021 and VS8022 DUT boards:

- 5 GHZ Oscilloscope
- 2.5 GHz Bit Error Rate Tester
- Power Supplies
  - 3.2V, 1 Amp per board
  - -2.0V, 1 Amp per board

The figure below shows one possible test setup for the VS8021 and VS8022 DUT boards. In this configuration the Bit Error Rate Tester sends a clock and serial bit pattern into the VS8022 DUT board. This data is demultiplexed into a byte wide pattern which is transferred via matched cables to the VS8021 DUT board where the byte wide data is multiplexed into a serial bit stream which is sent into the error detector. The bit error rate tester will verify that the bit stream that is sent out of the generator matches the bit stream that is fed back into the error detector. Always use matched delay cables between complementary signals and between data and clock signals. The oscilloscope can be used to view signal integrity of various signals and to monitor rise and fall times.

3



FEATURES

- Superior Performance: 200 Mb/s
- Duty-cycle Distortion @ 200Mb/s: ≤10%
- Operating Range: -40° to +85° C
- Power Dissipation: 10 Watts (Typical)
- Clocked or Flow-through Operation
- ECL F100K Compatible Inputs and Outputs
- Output to Output Skew: < 1500 ps
- Output Drive Capability: 25Ω
- Single Power Supply: -2 V ± 5%
- Package: 344-pin Ceramic LDCC
- Full Diagnostic Monitors
- Cascadable to Larger Systems

INTRODUCTION

The VSC864 is a 64 x 64 crosspoint switch intended for high speed (up to 200 Mb/s) digital data communications applications. This product has 64 data inputs and 64 data outputs. Any input can be multiplexed to any, some, or all outputs. High speed digital data up to 200 Mb/s can be switched with less than 10% pulse width distortion. In broadcast mode, any two outputs will exhibit less than 1500 ps of skew. All interfaces are fully compatible with ECL F100K logic levels. The VSC864 requires only a single -2 V power supply.

A separate Q bus is provided to allow observation of individual internal multiplexer address latches. Since the VSC864 outputs are capable of driving 25Ω double-terminated buses with cutoff drivers, the device can be cascaded to form larger crosspoint switches. The VSC864 Crosspoint Switch can be operated in either flow-through or synchronous mode by use of internal input and output data registers. In flow-through mode the data propagation delay is less than 6.5 ns.

The individual address registers in the VSC864 are double buffered. A local strobe signal is used to load an individual address for each output pin. A global strobe is used to simultaneously activate all 64 destination addresses.

This product is ideal for high speed digital applications including data distribution for telecommunications, computer network and multiprocessor switching, and test equipment. In a telecommunications SONET application, for example, the VSC864 can be used as an STS-3 protection switch, or in the fabric of a large switching system.

The VSC864 is packaged in a 344 pin ceramic LDCC package and typically dissipates less than 10 W. This product is fabricated using Vitesse's simple, high yielding, E/D GaAs MESFET process which achieves high speed coupled with low power dissipation.

FUNCTIONAL DESCRIPTION

The VSC864 may be used to connect any one of 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control latch.

During normal operation, signals flow from inputs (I_0 - I_{63}) to output channels (Z_0 - Z_{63}) through sixty-four, 64:1 multiplexers. The traffic pattern is controllable by data previously stored in sixty-four 7-bit control registers with each register corresponding to an output channel. The first 6 least significant bits in each control register are reserved for designating the MUX input which will be connected to its corresponding output, the most significant bit is used to tri-state this output if desired. The 6 LSBs are a binary numerical representation of the input channel selected (i.e.., 000000 corresponds to I_0, 000001 corresponds to I_1, etc.).

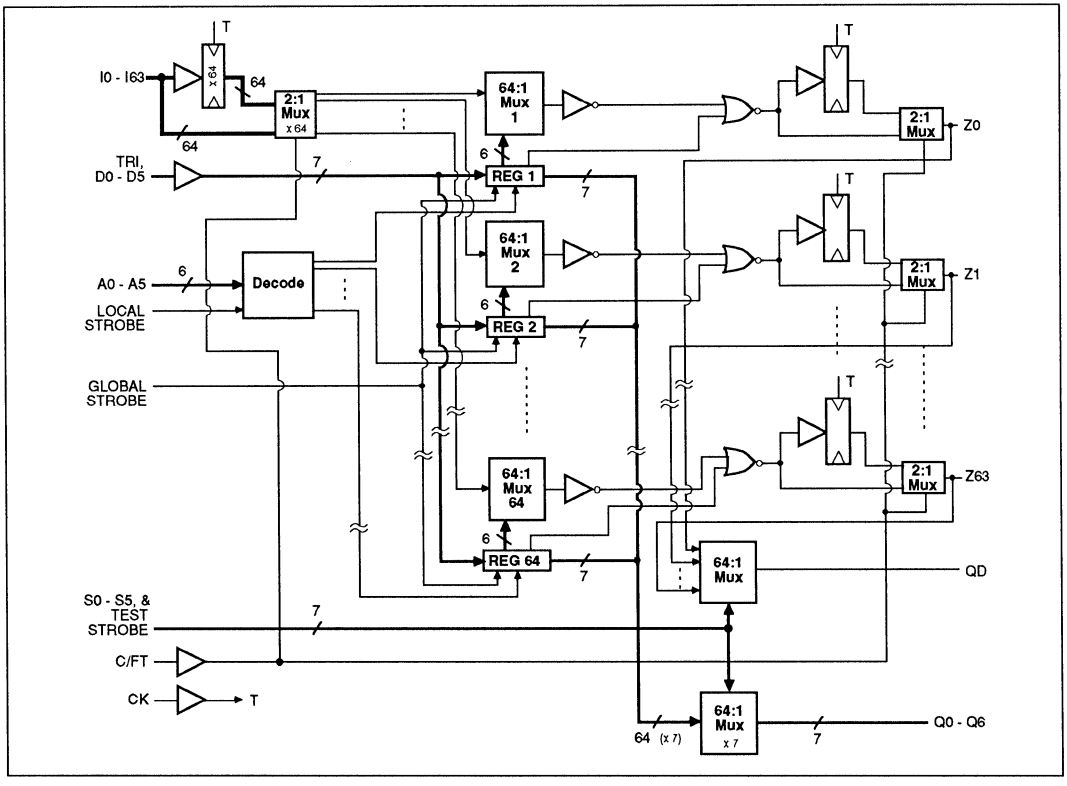
The Write mode is used to alter any one or all signal paths. During Write mode, inputs A_0 - A_5 select which output channel's control register will

be altered (also by a binary numerical representation). Inputs D_0- D_5 describe the new input signal to be selected for that channel. When a high pulse is applied to ***LOCAL STROBE***, D_0- D_5 and the ***TRI*** bit is transferred into a holding latch. After some or all control registers are programmed, a high pulse is applied to ***GLOBAL STROBE*** to transfer the information from the holding latch into all the control registers. In this way the entire crosspoint switch can be reconfigured simultaneously.

The Read mode is a diagnostic feature used to examine the data stored in any one control register and its corresponding 64:1 multiplexer output. The control register to be examined is selected by inputs S_0- S_5 (by a binary numerical representation). When a high pulse is applied to the ***TEST STROBE***, the contents of the selected control register will be displayed at the Q_0- Q_6 outputs and the corresponding 64:1 mux output will appear at the ***QD*** output. When ***TEST STROBE*** is "low" the Q bus has all low outputs (which is equivalent to being tri-stated).

The VSC864 can be configured to run in either synchronous clocked mode or asynchronous flow-through mode. This feature is controlled by the ***C/FT*** input. When ***C/FT*** is high, the chip is in clocked mode and will require an input clock at its ***CK*** pin. In this mode all input and output data is registered. When ***C/FT*** is low the chip is in flow-through mode and will ignore the ***CK*** input. In clocked mode, the outputs on the monitor bus (Q_0- Q_6, and ***QD***), and input data (I_0 - I_{63}) are registered by the master clock ***(CK)***.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -3.0V to +0.5V
Input Voltage Applied, $V_{E\,CLIN}$ ..... -2.5V to +0.5V
Output Current, I_{OUT},(DC, output HI) ..... 100 mA
Case Temperature Under Bias, T_C ..... -55° to +125°C
Storage Temperature (ambient), T_{STG} ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Supply Voltage, V_{TT} ..... -2.0V ± 0.1V
Commecial Operating Temperature Range, T (2) ..... 0° to 70°C
Industrial Operating Temperature Range, T (2) ..... -40° to 85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

3

DC CHARACTERISTICS

ECL Inputs/Outputs

(Over recommended commercial operating conditions. $V_{CC} = V_{CCA}$ = GND, Output load 25Ω to V_{TT}.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	$V_{IN} = V_{IH}$ (max)
V_{OL}	Output LOW voltage	V_{TT}	—	-1620	mV	or V_{IL} (min), V_{TT} = -2.0V
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min
I_{TT}	Supply current	—	4	7	A	V_{TT} = -2.10V

AC TIMING CHARACTERISTICS

(Over recommended operating conditions. V_{CC} = V_{CCA} = GND. Output load 25Ω to V_{TT}.)

Flow-Through Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
PW	Minimum data valid time	5	—	—	ns	—
t_{DR}	Propagation delay (rising)	3500	—	6500	ps	—
t_{DF}	Propagation delay (falling)	3500	—	6500	ps	—
—	Duty cycle distortion	—	10	—	%	at 200 Mb/s
skew	Output to output skew	—	—	2400	ps	on a given part
BER	Bit Error Rate	—	—	10^{-13}	—	—

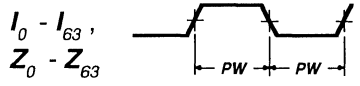
Clocked Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
f_{MAX}	Maximum clock rate	—	—	200	MHz	—
t_{ISU}	Input data set-up time	-500	—	—	ps	—
t_{IH}	Input data hold time	2800	—	—	ps	—
t_{CZR}	Clock to output delay (rising)	3500	—	6500	ps	—
t_{CZF}	Clock to output delay (falling)	3500	—	6500	ps	—
skew	Output to output skew	—	—	1500	ps	On a given part

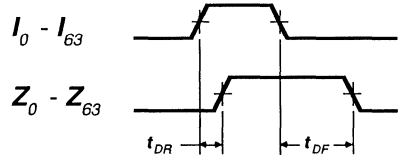
AC TIMING WAVEFORMS

Flow-Through Mode

Minimum Data Valid Time, ***PW***

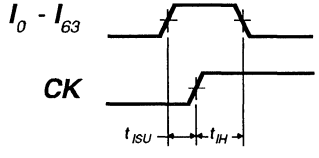


Propagation Delay

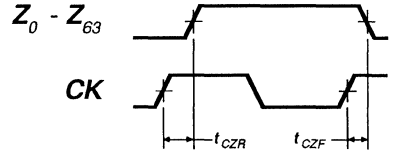


Clocked Mode

Input Data Set-up & Hold Times



Clock to Output Delay



AC TIMING CHARACTERISTICS *(continued):*

(Over recommended commercial operating conditions. V_{CC} = V_{CCA} = GND.

Write Mode

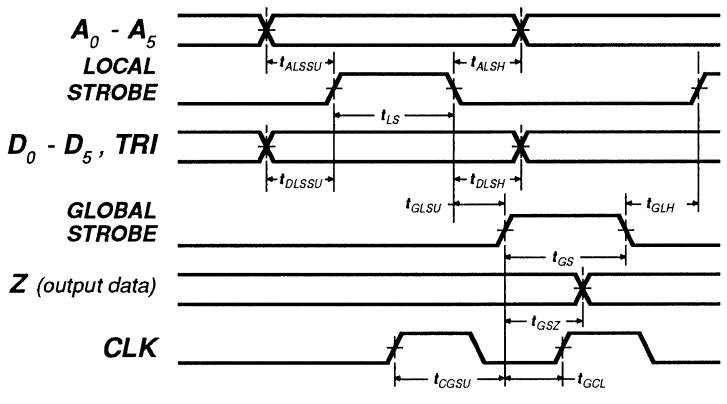
Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Condition*
t_{RECON}	Reconfiguration time	—	—	650	ns	64 channel reconfig
t_{ALSSU}	A bus to ***LOCAL STROBE*** set-up time	-100	—	—	ps	—
t_{ALSH}	A bus to ***LOCAL STROBE*** hold time	1600	—	—	ps	—
t_{DLSSU}	D bus to ***LOCAL STROBE*** set-up time	400	—	—	ps	—
t_{DLSH}	D bus to ***LOCAL STROBE*** hold time	2	—	—	ns	—
t_{GLSU}	***GLOBAL STROBE*** to ***LOCAL STROBE*** set-up time	5	—	—	ns	—
t_{GS}, t_{LS}, t_{TS}	***GLOBAL STROBE*** and ***LOCAL STROBE*** pulse widths	5	—	—	ns	—
t_{TS}	***TEST STROBE*** pulse width	10	—	—	ns	—
t_{GLH}	***GLOBAL STROBE*** to ***LOCAL STROBE*** hold time	5	—	—	ns	—
t_{GSZ}	***GLOBAL STROBE*** to valid output (flow-thrrough mode)	3.5	—	8.5	ns	—
t_{CGSU}	***CLK*** to ***GLOBAL STROBE*** set-up time (clocked mode)	5	—	—	ns	Data being clocked in at this time is invalid
t_{GCL}	***GLOBAL STROBE*** to ***CLK*** hold time (clocked mode)	5	—	—	ns	

Read Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{TSQ}	***TEST STROBE*** to valid Q output	—	—	10	ns	—
t_{TSBQ}	S bus to valid output	—	—	10	ns	—
t_{TSQT}	***TEST STROBE*** to tri-state condition on Q	—	—	10	ns	—

AC TIMING WAVEFORMS (con't)

Write Mode



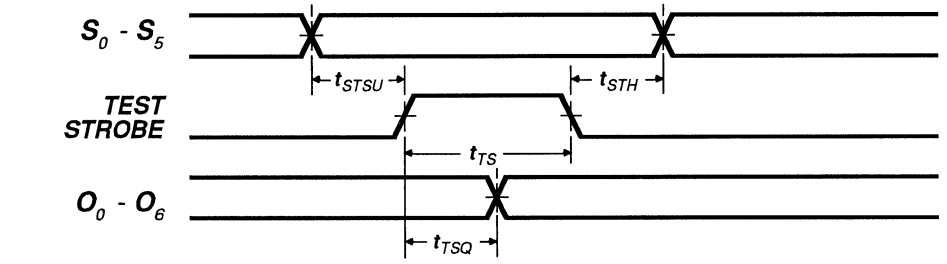
A address setup and hold relative to ***LOCAL STROBE***.

D data setup and hold relative to ***LOCAL STROBE***.

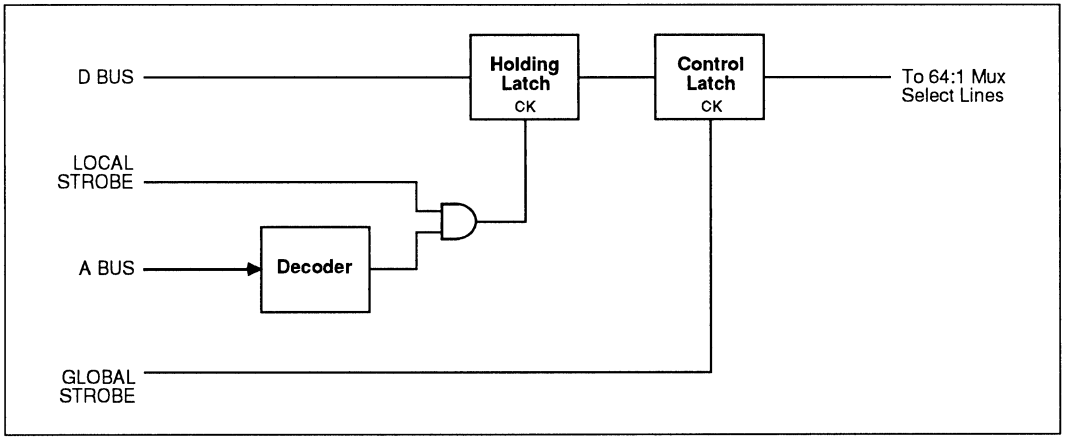
LOCAL STROBE to ***GLOBAL STROBE*** timing relationship.

CLOCKED MODE - ***GLOBAL STROBE*** to ***CLK*** timing relationship.

Read Mode



BLOCK DIAGRAM OF INTERNAL WRITE MODE CIRCUITS



PIN DESCRIPTION

Pin #	Name	I/O	Description
12-16, 20-30, 35-45, 49-53, 184-188, 192- 202, 207-217, 221-225	I_0 - I_{63}	I	The 64 ECL signal inputs.
11	TRI	I	ECL input containing Tristate data to be loaded into a 64:1 Mux holding latch. (Tristate = HIGH) Combined with a control register's destination address. Used to tristate the corresponding output.
5-10	D_0 - D_5	I	ECL inputs containing the destination address to be loaded into the 64:1 Mux holding latch.
178-183	A_0 - A_5	I	ECL inputs containing the address of the 64:1 Mux holding/control latch to be programmed.
177	LOCAL STROBE	I	Active HIGH, ECL input used to load the D0-D5 and TRI data into the 64:1 Mux holding latch.
34	GLOBAL STROBE	I	Active HIGH, ECL input used to load destination addresses to all 64:1 Mux control latches simultaneously from the data contained in their corresponding holding latches.
54-59	S_0 - S_5	I	ECL inputs containing the address of the control latch to be observed at the QD output when the TEST STROBE is HIGH.
60	TEST STROBE	I	Active HIGH, ECL input used to enable Test Mode and observation of a selected 64:1 Mux control latch's destination address.
206	C/FT	I	ECL input used to enable Clocked or Flow-through Mode (Clocked = HIGH / Flow-Thru = LOW).
203	CK	I	ECL clock input for Clocked Mode.
68, 71, 73, 78, 80, 83, 85, 88, 92, 95, 97, 100, 102, 107, 109, 112, 126, 129, 131, 136, 138, 141,143, 148, 150, 153, 155,158, 162, 165, 167, 170, 240, 243, 245, 250, 252, 255, 257, 260, 264, 267, 269, 272, 274, 279, 281, 284, 298, 301, 303, 308, 310, 313, 315, 320, 322, 325, 327, 330, 334, 337, 339, 342	Z_0 - Z_{63}	O	The 64 ECL signal outputs.
296	QD	O	ECL output used to observe the output of a selected 64:1 Mux in Test Mode.
114, 117, 121, 124, 286, 289, 293	Q_0 - Q_6	O	ECL outputs containing the selected 64:1 Mux control register's destination address and TRI bit in Test Mode.
3, 17, 32, 47, 61, 76, 90, 104, 118, 132, 146, 160, 175, 189, 204, 219, 233, 248, 262, 276, 290, 304, 318, 332	V_{CC}		ØV ground connection for internal logic.
2, 63, 69, 74, 81, 86, 93, 98, 103, 110, 115, 122, 127, 134, 139, 144, 151, 156, 163, 168, 174, 235, 241, 246, 253, 258, 265, 270, 275, 282, 287, 294, 299, 306, 311, 316, 323, 328, 335, 340	V_{CCA}		ØV 'dirty' ground connection for outputs.

PIN DESCRIPTION (cont.)

Pin #	Name	I/O	Description
4, 18, 33, 48, 62, 77, 91, 105, 119, 133, 147, 161, 176, 190, 205, 220, 234, 249, 263, 277, 305, 319, 333	V_{TT}		-2V supply connection.
291	V_{SUB}		-2V supply connection to substrate (most negative supply).
1, 19, 31, 46, 64-67, 70, 72, 75, 79, 82, 84, 87, 89, 94, 96, 99, 101, 106, 108, 111, 113, 116, 120, 123, 125, 128, 130, 135, 137, 140, 142, 145, 149, 152, 154, 157, 159, 164, 166, 169, 171-173, 191, 218, 226-232, 236-239, 242, 244, 247, 251, 254, 256, 259, 261, 266, 268, 271, 273, 278, 280, 283, 285, 288, 292, 295, 297, 300, 302, 307, 309, 312, 314, 317, 321, 324, 326, 329, 331, 336, 338, 341, 343, 344	NC		No connection

PIN IDENTIFICATION

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin#	Name	Pin #
I_0	12	I_{22}	26	I_{44}	41	D_2	7	Z_6	85	Z_{28}	162	Z_{50}	303
I_1	225	I_{23}	211	I_{45}	196	D_3	8	Z_7	88	Z_{29}	165	Z_{51}	308
I_2	13	I_{24}	27	I_{46}	42	D_4	9	Z_8	92	Z_{30}	167	Z_{52}	310
I_3	224	I_{25}	210	I_{47}	195	D_5	10	Z_9	95	Z_{31}	170	Z_{53}	313
I_4	14	I_{26}	28	I_{48}	43	A_0	183	Z_{10}	97	Z_{32}	240	Z_{54}	315
I_5	223	I_{27}	209	I_{49}	194	A_1	182	Z_{11}	100	Z_{33}	243	Z_{55}	320
I_6	15	I_{28}	29	I_{50}	44	A_2	181	Z_{12}	102	Z_{34}	245	Z_{56}	322
I_7	222	I_{29}	208	I_{51}	193	A_3	180	Z_{13}	107	Z_{35}	250	Z_{57}	325
I_8	16	I_{30}	30	I_{52}	45	A_4	179	Z_{14}	109	Z_{36}	252	Z_{58}	327
I_9	221	I_{31}	207	I_{53}	192	A_5	178	Z_{15}	112	Z_{37}	255	Z_{59}	330
I_{10}	20	I_{32}	35	I_{54}	49	S_0	54	Z_{16}	126	Z_{38}	257	Z_{60}	334
I_{11}	217	I_{33}	202	I_{55}	188	S_1	55	Z_{17}	129	Z_{39}	260	Z_{61}	337
I_{12}	21	I_{34}	36	I_{56}	50	S_2	56	Z_{18}	131	Z_{40}	264	Z_{62}	339
I_{13}	216	I_{35}	201	I_{57}	187	S_3	57	Z_{19}	136	Z_{41}	267	Z_{63}	342
I_{14}	22	I_{36}	37	I_{58}	51	S_4	58	Z_{20}	138	Z_{42}	269	Q_0	114
I_{15}	215	I_{37}	200	I_{59}	186	S_5	59	Z_{21}	141	Z_{43}	272	Q_1	117
I_{16}	23	I_{38}	38	I_{60}	52	Z_0	68	Z_{22}	143	Z_{44}	274	Q_2	121
I_{17}	214	I_{39}	199	I_{61}	185	Z_1	71	Z_{23}	148	Z_{45}	279	Q_3	124
I_{18}	24	I_{40}	39	I_{62}	53	Z_2	73	Z_{24}	150	Z_{46}	281	Q_4	286
I_{19}	213	I_{41}	198	I_{63}	184	Z_3	78	Z_{25}	153	Z_{47}	284	Q_5	289
I_{20}	25	I_{42}	40	D_0	5	Z_4	80	Z_{26}	155	Z_{48}	298	Q_6	293
I_{21}	212	I_{43}	197	D_1	6	Z_5	83	Z_{27}	158	Z_{49}	301		

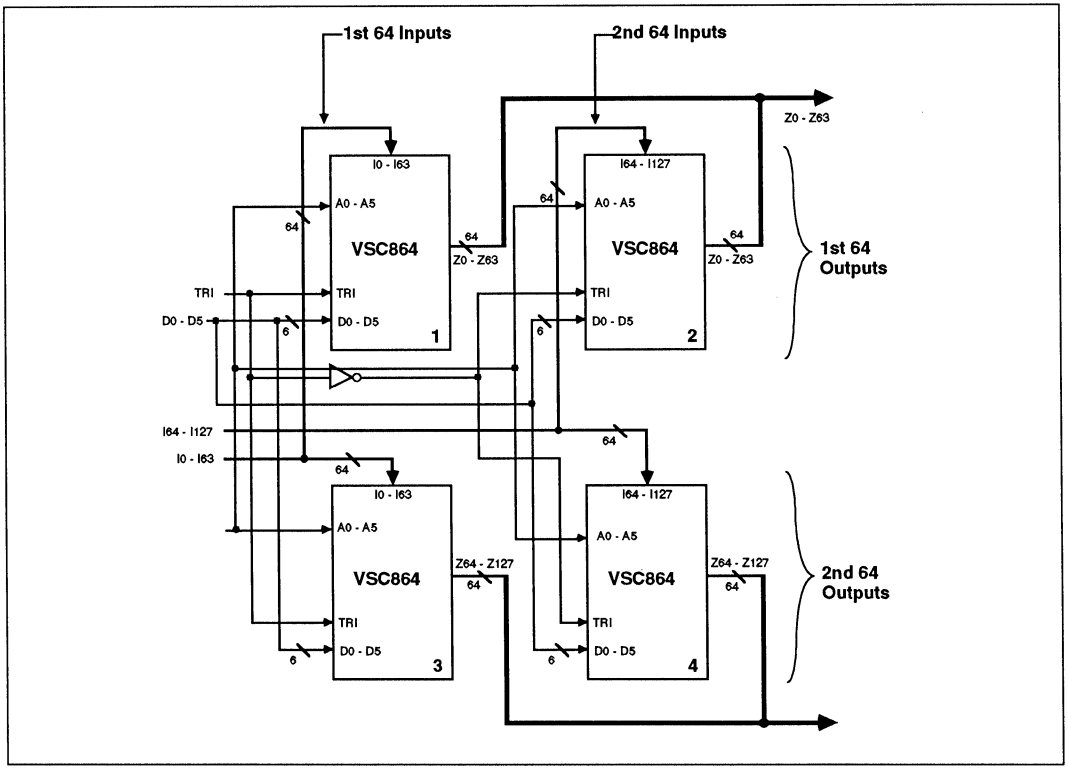
EXPANDABILITY

The VSC864 can be expanded to larger crosspoint switches by configuring it so that any input can be multiplexed to any output. The figure below is an example of a 128 x 128 crosspoint switch. The top two VSC864s (1&2) correspond to the first 64 outputs and the bottom two VSC864s (3&4) correspond to the last 64 outputs. The VSC864s on the left (1&3) correspond to the first 64 inputs, and the two VSC864s on the right (2&4) correspond to the last inputs. All like outputs are then joined to form a 128 bit Z output bus. The ability of the VSC864 to tri-state its outputs will prevent contention on the Z bus.

The ***TRI*** input is configured such that when it is active on the left hand chips (which are responsible for routing the first 64 inputs) it is inactive on the two right hand chips (which are responsible for routing the last 64 inputs). The TRI input thus functions as the MSB of a 7-bit channel address word (A-bus plus TRI). Chips can share A-bus information. The destination (D) bus can be shared among the four chips with the local strobe for each device being used to select which output address gets reconfigured.

The layout and placement of the VSC864 is such that inputs are on the top and bottom of the chip and outputs are to the right and left. In this way a PC board design for a large crosspoint is facilitated.

In the read mode tri-stateability on the Q-bus can be controlled with the ***TEST STROBE*** input. A "low" level on this input will tri-state its corresponding Q-bus. In this way the Q-bus from all chips can be wire-OR'ed. Individual ***TEST STROBE*** signals to each chip, however, are required.



FEATURES

- 256 words by 4-bit static RAM for cache and control store applications
- Very fast: Choice of 4, 5, and 6 ns maximum address access times
- TTL compatible inputs and outputs
- Single +5.0 Volt power supply
- Very low sensitivity to radiation
- Standard 22-pin DIP
- Fully static operation - equal access and cycle times
- Pin compatible with standard silicon -422 and -122 products

FUNCTIONAL DESCRIPTION

The Vitesse VS12G422T is a very high speed, fully decoded 1024-bit read write static random access memory organized as 256 words by 4 bits. All inputs and outputs of this RAM are TTL compatible and operation is from a standard +5.0 Volt power supply.

Fully static asynchronous internal circuits are used, which require no clocks or refreshing for operation. Memory expansion is provided by an active LOW chip select input ($\overline{CS}_1$), an active HIGH chip select input (CS_2) and three-state outputs. Due to its static operation, the VS12G422T offers equal read and write cycle times, which further simplifies system design.

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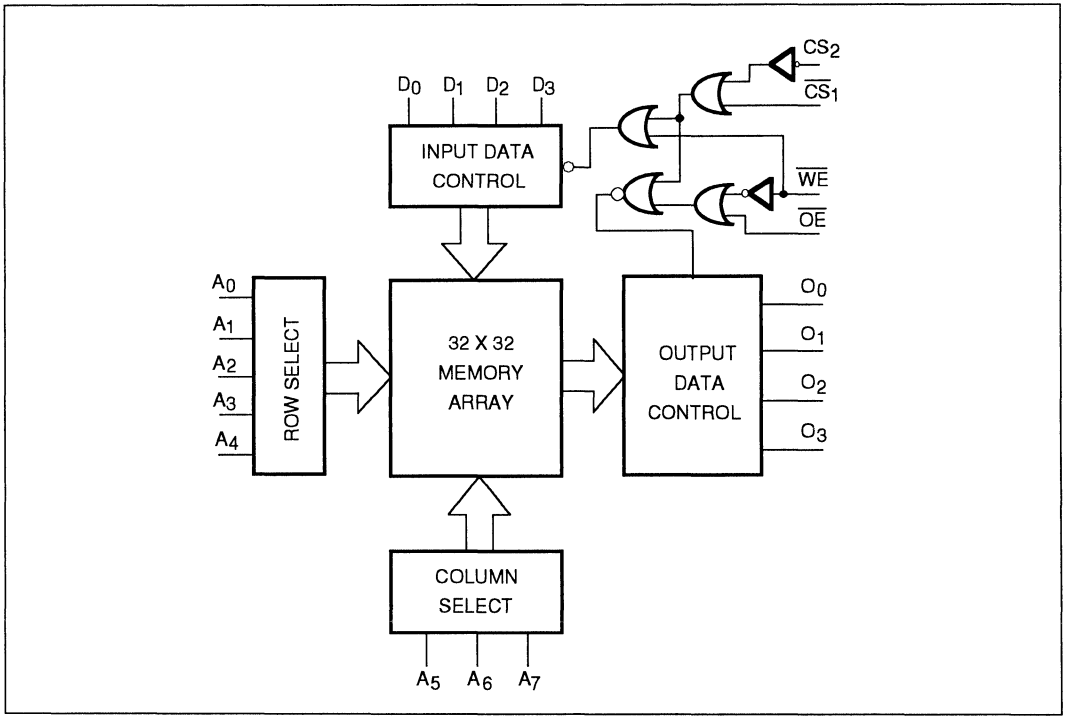
BLOCK DIAGRAM



TRUTH TABLE

Inputs				Output	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$		
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V) *X = Don't Care (HIGH or LOW)*
L = LOW Voltage Level (0.4 V) *HIGH Z = High-Impedence*

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage *(V_{CC})* ..... -0.5 V to +6.0 V
Input Voltage Applied, *(V_{IN})* ..... -1.0 V to +7.0 V
Input Current, *(I_{IN})*, (DC, output LOW) ..... -30 to +30 mA
Output Current, *(I_{OUT})*, (DC, output LOW) ..... 20 mA
Case Temperature Under Bias, *(T_C)* ..... -55° to +125°C
Storage Temperature(2), *(T_{STG})* ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, *(V_{CC})* ..... 4.75 to 5.25 V
Operating Temperature Range (2). ..... 0° to +70°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS *(Over recommended operating conditions)*

Parameters	Description	Commercial Range				Test Conditions
		5,6 ns		4 ns		
		Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	2.4 V	—	2.4 V	—	V_{CC} = MIN, I_{OH} = -5.2 mA
V_{OL}	Output LOW voltage	—	0.5 V	—	0.5 V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0 V	—	2.0 V	—	—
V_{IL}	Input LOW voltage	—	0.8 V	—	0.8 V	—
I_{IX}	Input LOAD current	-100 µA	100 µA	-100 µA	100 µA	V_{IN} = 3.3 V
I_{OZ}	Output current (HIGH-Z)	-1.0 mA	1.0 mA	-1.0 mA	1.0 mA	$V_{OL} \leq V_{OUT} \leq V_{OH}$ *Output Disabled*
I_{CC}	Power supply current (from V_{CC})	—	300 mA	—	300 mA	V_{CC} = MAX, I_{OUT} = 0 mA

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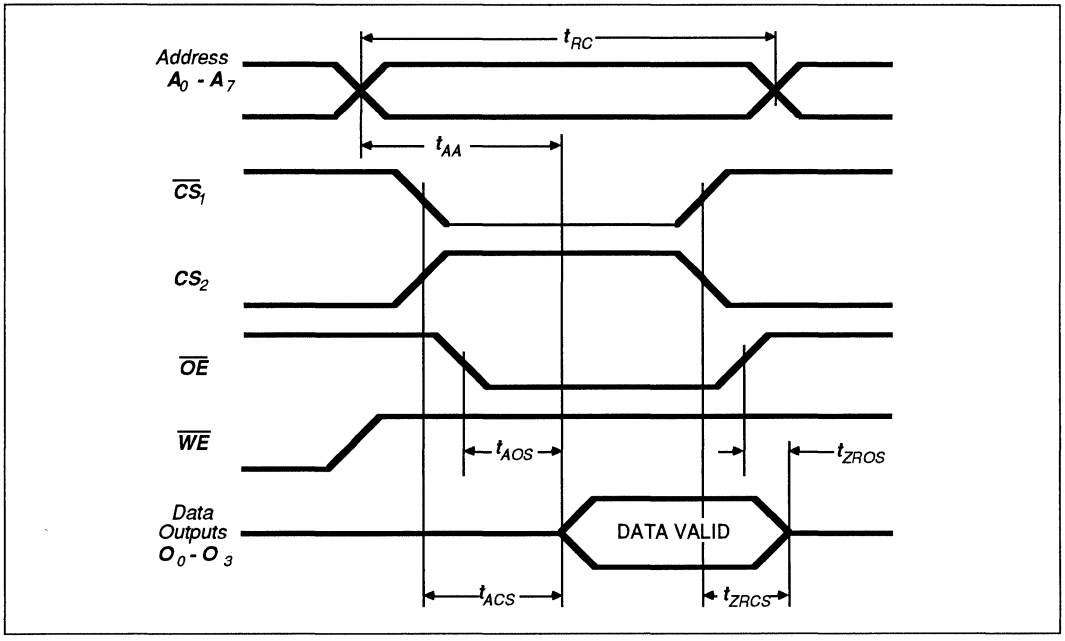
AC PERFORMANCE CHARACTERISTICS (1)

(Over guaranteed operating conditions, GND = 0 V)

Read Mode



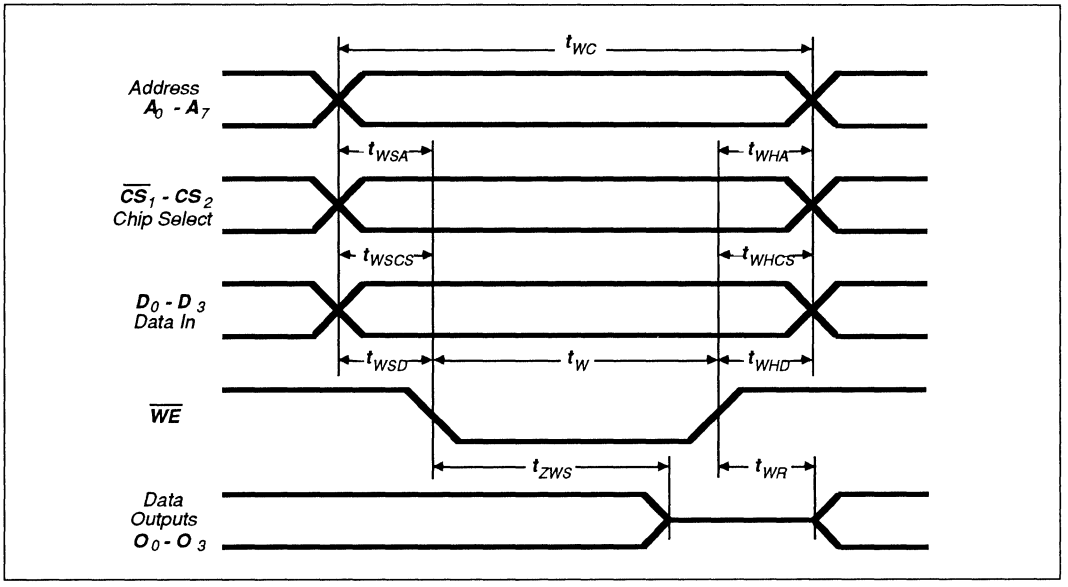
Parameters	Description	6 ns		5 ns		4 ns		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	6	—	5	—	4	—	ns
t_{ACS}	Chip select time	—	4	—	3.5	—	2.5	ns
t_{ZRCS} (2)	Chip select to HIGH Z	—	5	—	4	—	3.5	ns
t_{AOS}	Output enable time	—	4	—	3.5	—	2.5	ns
t_{ZROS} (2)	Output enable to HIGH Z	—	5	—	4	—	3.5	ns
t_{AA}	Address access time	—	6	—	5	—	4	ns

NOTES: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in Figure 1 on ***page X.***
2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in Figure 1 on ***page X.***

AC PERFORMANCE CHARACTERISTICS (con't) [1]

(Over guaranteed operating conditions, GND = 0V)

2. Write Mode



Paramters	Description	6 ns		5 ns		4ns		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	6	—	5	—	4	—	ns
t_{ZWS} [2]	Write disable to HIGH Z	—	5	—	4	—	3.5	ns
t_{WR}	Write recovery time	—	4.5	—	3.5	—	3	ns
t_W [3]	Write pulse width	4	—	3	—	2.5	—	ns
t_{WSD}	Data setup time prior to write	0	—	0	—	0	—	ns
t_{WHD}	Data hold time after write	2	—	2	—	1.5	—	ns
t_{WSA} [3]	Address setup time	0	—	0	—	0	—	ns
t_{WHA}	Address hold time	2	—	2	—	1.5	—	ns
t_{WSCS}	Chip select setup time	0	—	0	—	0	—	ns
t_{WHCS}	Chip select hold time	2	—	2	—	1.5	—	ns

NOTES: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in Figure 1 on ***page X***
2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in Figure 1 on ***page X***
3) t_W measured at t_{WSA} = min; t_{WSA} measured at t_W = min

FIGURE 1: AC TEST LOADING CONDITION

The following conditions apply to the "AC Performance Characteristics" indicated on **pages X and X.**

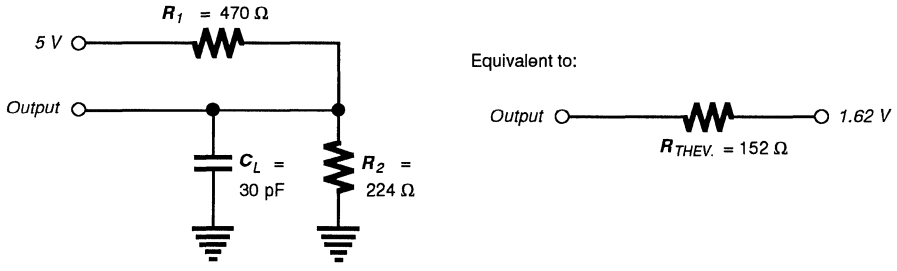
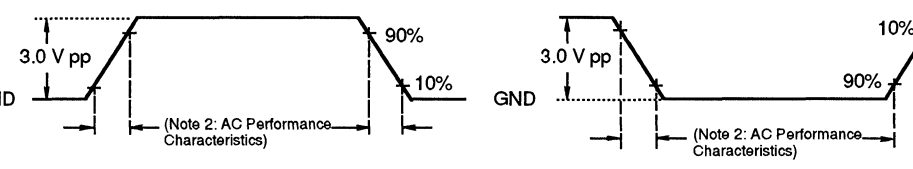


FIGURE 2: AC TEST INPUT LEVELS

The following conditions apply to the "AC Performance Characteristics" indicated on **pages X and X.**

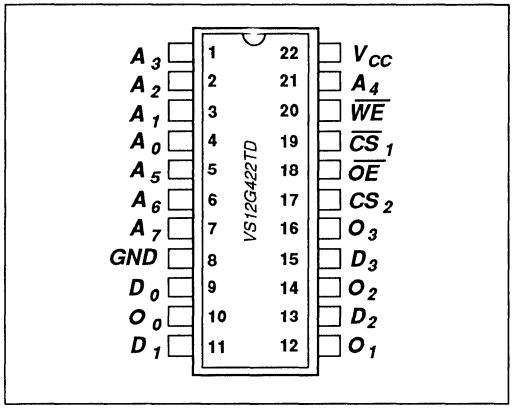


ADDRESS DESIGNATORS

Address Name	*Address Function*	*Pin # (22-pin DIP)*
A_0	AX_0	4
A_1	AX_1	3
A_2	AX_2	2
A_3	AX_3	1
A_4	AX_4	21
A_5	AY_5	5
A_6	AY_6	6
A_7	AY_7	7

CONNECTION DIAGRAM

(22-pin DIP - Top View)



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PIN DESCRIPTION

Pin #	Name	I/O	Description
1-7, 21	A_0 - A_7	I	Address inputs
9, 11, 13, 15	D_0 - D_3	I	Data Inputs
19	$\overline{CS}_1$	I	Chip select input (Active LOW)
10, 12, 14, 16	O_0 - O_3	O	Data outputs
17	CS_2	I	Chip select input (Active HIGH)
20	$\overline{WE}$	I	Write enable input (Active LOW)
18	$\overline{OE}$	I	Output enable input (Active LOW)
22	V_{CC}		5.0 V supply connection
8	GND		Ground connection (0 V)

2K x 2 Self-Timed RAM with Purge

FEATURES

- 2048 words x 2-bit Static RAM, ideal for fast cache or control store applications
- Functionally compatible with national NM100492 (with the addition of an output latch enable)
- Very fast: read/write cycle time 5, 6 or 7 ns (Max)
- Full chip bit purge in 4 cycles
- 100K ECL compatible inputs and outputs
- Power dissipation: ≤ 1 W (typical)
- Single power supply, V_{TT} = -2.0 V ± 5%
- 28-pin ceramic leaded chip carrier (LDCC)
- Diagnostic serial scan mode
- Self-timed operation

INTRODUCTION

The VS12G478 is a high speed, fully decoded 4096-bit read write self-timed static random access memory organized as 2048 words by 2 bits. This RAM is intended for use in high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and addressable translation lookaside buffers. This device is I/O compatible with standard F100K ECL logic, allowing trouble free interfacing in high performance ECL systems. Operation is from a standard -2.0 Volt power supply, and all inputs are registered and all outputs are latched.

The SRAM features a 4 cycle "clear-all-bits-to-zero" purge function. The purge function is especially useful in multitasking systems with cache tags which require a validity bit purge in a very short time. On-chip circuitry creates an inter-

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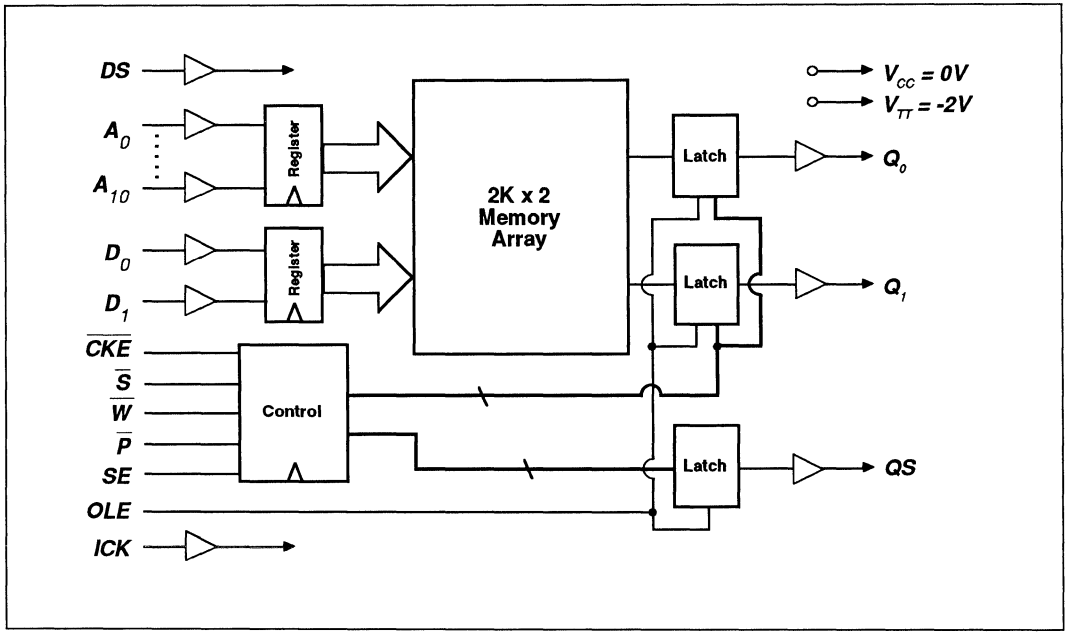
BLOCK DIAGRAM



nal write pulse intended to ease system timing. A diagnostic serial scan mode is also supported. The scan function allows examin–ation and modification of internal register states.

The VS12G478 is available with a 5 or 7 ns worst case cycle time, and either a read or a write operation can be performed in one cycle. Total power dissipation for the chip is less than 1 W, and it is packaged in a 28-pin leaded ceramic chip carrier. The VS12G478 is fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation.

TRUTH TABLES

Normal Operation *(SE Low for Current and Previous Cycle)*

Inputs						Output	Description
$\overline{CKE}$	$\overline{P}$	$\overline{S}$	$\overline{W}$	AN	DN	Q	
H	X	X	X	X	X	NC	No operation
L	L	X	X	X	X	L	PURGE*
L	H	H	H	X	X	L	Deselect (READ)
L	H	L	H	V	X	V	READ
L	H	H	L	X	X	NC	WRITE inhibit
L	H	L	L	V	V	NC	WRITE (Hidden), outputs remain held during write.

** PURGE starts a 4 cycle RAM clear operation. During the next 4 cycles, all other inputs except SE are ignored.*

Scan Mode Operation

Inputs				Outputs		Description
Prior SE	Current SE	Registered $\overline{CKE}$	DS	Q	QS	
L	L	X	X	X	DI	Normal operation
L	H	X	V	NC	DO	Enter SCAN, do first shift. DS scanned in.
H	H	X	V	NC	V	SCAN mode
H	L	L	V	L/V/NC	V	Exit SCAN. Shift, then perform Scanned Instruction*
H	L	H	V	V	V	Exit SCAN, NOP. Update Output Latches to Scanned in Values

** If PURGE instruction is scanned in, then the PURGE will start at the scanned in purge machine state.*

DC CHARACTERISTICS

ECL Inputs/Outputs

(Over recommended operating conditions with external V_{REF} (1). $V_{CC} = V_{CCA} = GND$, Output load 50Ω to V_{TT}.)

Parameter	Description	Min	Max	Units	Conditions
V_{IH}	Input HIGH Voltage	-1140	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW Voltage	-2000	-1500	mV	Guaranteed LOW for all inputs
V_{OH}	Output HIGH Voltage	-1020	-700	mV	Output load = 50 Ω to -2 V
V_{OL}	Output LOW Voltage	-2000	-1620	mV	Output load = 50 Ω to -2 V
I_{IH}	Input HIGH Current	—	+200	µA	$V_{IN} = V_{IH}$max
I_{IL}	Input LOW Current	-50	—	µA	$V_{IN} = V_{IL}$max
I_{IHP}	Input Pulldown Current ($\overline{CKE}$, CS, SE, DS)	0	+500	µA	

Note: (1) External reference = -1.32V ± 25 mV.

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POWER DISSIPATION *(Over recommended operating conditions, V_{CC} = GND, outputs open circuit.)*

Parameter	Description	Min	Max	Units	Conditions
I_{TT}	Power Supply Current	-600	—	mA	T_{CYCLE} = 5 ns
P_D	Power Dissipation	—	1.05	W	T_{CYCLE} = 5 ns

ABSOLUTE MAXIMUM RATINGS (1)

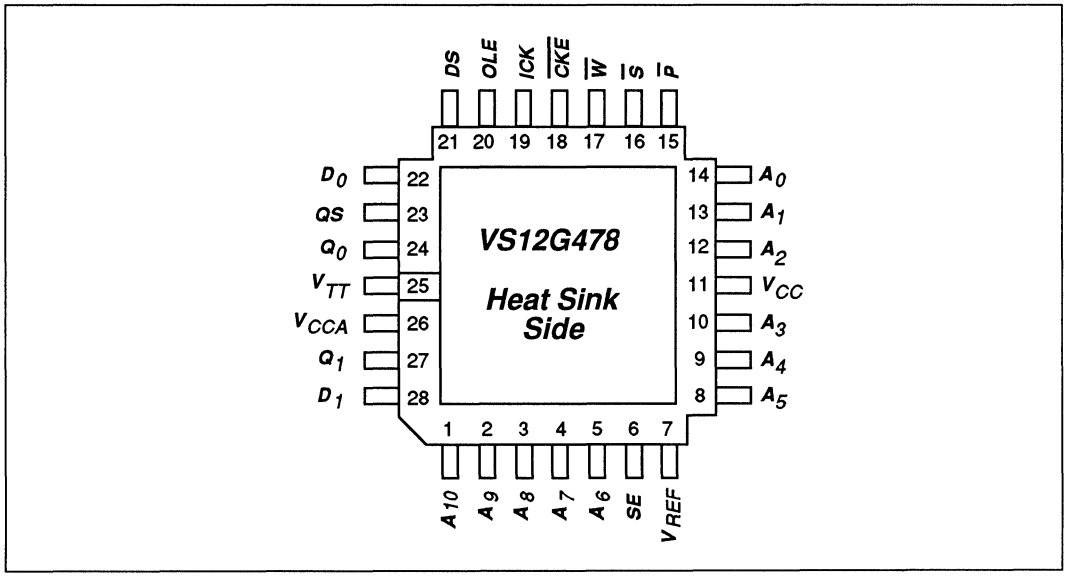
Power Supply Voltage, V_{TT} potential to GND ..... -2.5V to +0.5V
Input Voltage Applied, V_{IN} (2). ..... +0.5V to V_{TT}
Output Current, I_{OUT} (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, T_C ..... -55°C to +125°C
Storage Temperature, T_{STG} (3). ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{TT} ..... -2.0V ± 5%
Operating Temperature Range, T (3). ..... 0° to 70°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{IN}) and V_{IN} must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

PIN DESCRIPTION



ADDRESS DESIGNATORS

Address Name	Address Function
A_0	X_0
A_1	X_2
A_2	X_1
A_3	X_3
A_4	X_5
A_5	X_4
A_6	Y_0
A_7	Y_2
A_8	Y_1
A_9	Y_3
A_{10}	Y_4

PIN DESCRIPTION

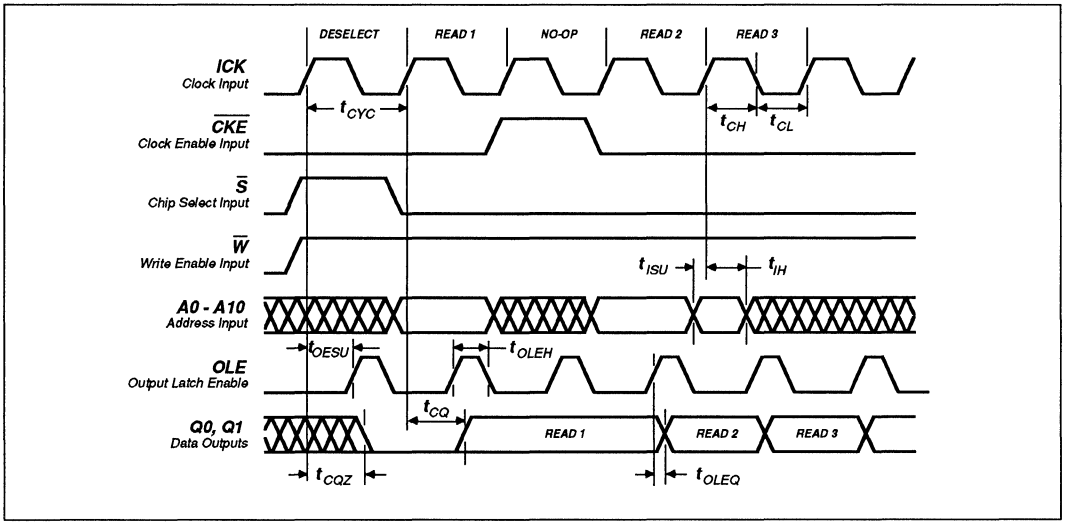
Name	I/O	Description
A_0 - A_{10}	I	Address inputs used to select the memory locations for storing or retrieving data.
D_0, D_1	I	Data inputs stored in the specified address location during a write operation.
$\overline{CKE}$	I	Clock Enable input. Allows normal operation when LOW. Holds outputs and disables writes and purges when HIGH. Upon exiting SCAN mode, causes chip to either execute scanned-in instruction ($\overline{CKE}$ LOW), or transfer scan contents to outputs and do a no-op ($\overline{CKE}$ HIGH).
$\overline{P}$	I	Purge input. Clocking in a LOW input will start a 4 cycle reset of all bits in the RAM. During the purge operation all inputs except Scan Enable are ignored. Outputs are disabled for the duration of the purge.
$\overline{S}$	I	Chip Select input. When active (LOW) allows normal read and write cycles to occur. When inactive, and when Write Enable is also inactive, a de-selected read operation will disable the outputs. Writes are disabled when the chip is de-selected.
$\overline{W}$	I	Write Enable input. When active (LOW), causes a write operation to occur. Outputs are held in previous state during writes.
ICK	I	Input Clock. All inputs except **OLE** are registered on the rising edge of **ICK**.
OLE	I	Output Latch Enable. HIGH transparent latch enable signal to the output latches.
DS	I	Serial Data input. Scan shift register input.
SE	I	Scan Enable input. Enables the serial scan diagnostics mode. During all cycles when this pin is active (HIGH) the scan registers shift once. Writes and purges are disabled and the Data Outputs are held.
Q_0, Q_1	O	Data Outputs. Latched RAM data outputs.
QS	O	Serial Data Output. Scan data output.
V_{TT}		Negative supply (-2V).
V_{CC}		Positive supply (GND).
V_{CCA}		Positive supply (GND) for output buffers only.
V_{REF}		ECL reference level input when not using internally generated reference level.

AC PERFORMANCE CHARACTERISTICS: *(Over recommended operating conditions, V_{CC} = V_{CCA} = GND)*

Read Mode

A read cycle is performed when the following conditions are present at the rising edge of ***ICK:*** $\overline{CKE}$ = LOW, S = LOW, $\overline{W}$ = HIGH, SE = LOW and was LOW for the previous cycle, $\overline{P}$ = HIGH and no purge in progress. (i.e. $\overline{P}$ has been high for the previous 4 cycles and Scan Mode was not exited into a purge that is still in progress.)

Read Mode Waveforms



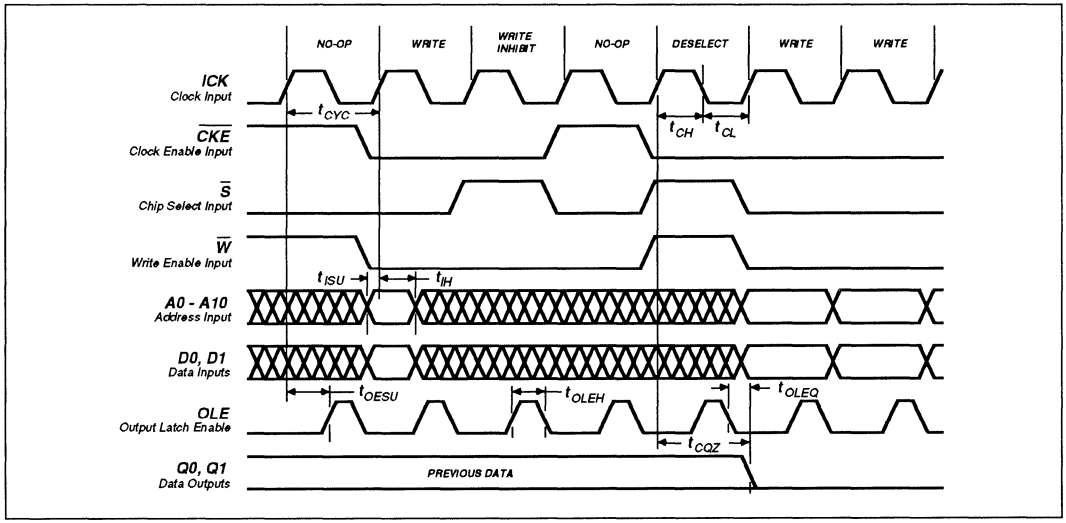
Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQ}	Access Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	2.0	—	2.5	—	ns	
t_{CL}	Clock LOW Time	2.0	—	2.5	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

AC PERFORMANCE CHARACTERISTICS (con't) *(Over recommended operating conditions, V_{CC} = V_{CCA} = GND)*

2. Write Mode

A write cycle is performed when the following conditions are present at the rising edge of ***ICK:*** $\overline{CKE}$ = LOW, $\overline{S}$ = LOW, $\overline{W}$ = LOW, ***SE*** = LOW and was LOW for the previous cycle, $\overline{P}$ = HIGH and no purge in progress. (i.e. $\overline{P}$ has been high for the previous 4 cycles and Scan Mode was not exited into a purge that is still in progress.)

Write Mode Waveforms



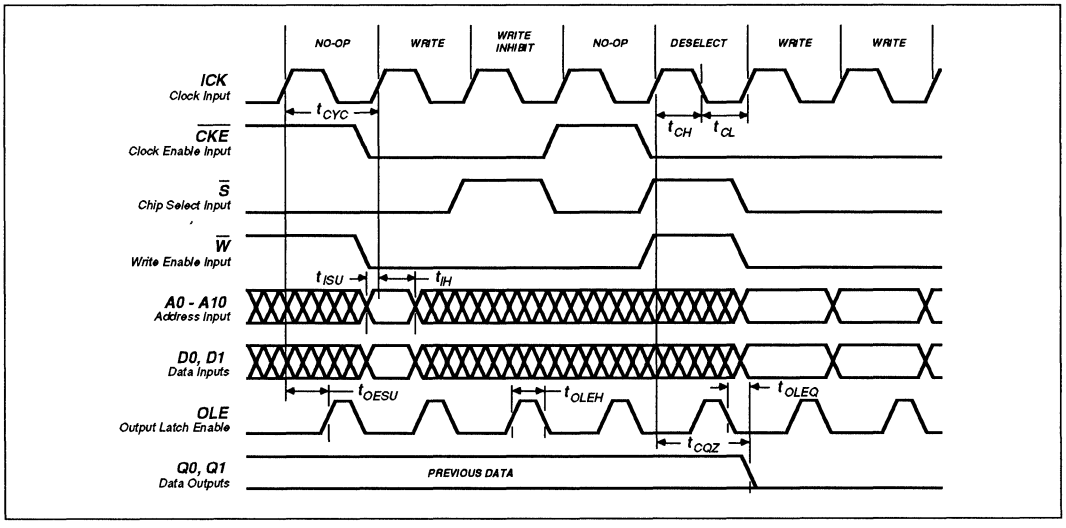
Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	2.0	—	2.5	—	ns	
t_{CL}	Clock LOW Time	2.0	—	2.5	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

AC PERFORMANCE CHARACTERISTICS (con't) *(Over recommended operating conditions, V_{CC} = V_{CCA} = GND)*

3. Purge Mode

A full chip reset begins when the following conditions are present at the rising edge of ***ICK***: $\overline{CKE}$ = LOW, ***SE*** = LOW and was LOW for the previous cycle, $\overline{P}$ = LOW. Once started, the purge cycle takes 4 cycles to complete. During this time, all inputs except SE are ignored and outputs are disabled.

Purge Mode Waveforms



Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time (except $\overline{P}$)	500	—	500	—	ps	
$t_{ISU\overline{P}}$	Purge Input Setup Time	750	—	750	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	2.0		2.5	—	ns	
t_{CL}	Clock LOW Time	2.0	—	2.5	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

4. Scan Mode

Scan Mode is entered when ***SE*** is brought high. When in Scan Mode, the input registers are reconfigured as shift registers and each rising edge of ***ICK*** causes them to shift. The state of ***DS*** is shifted in and the state of ***QS*** is updated. ***QS*** is latched by ***OLE*** like the regular outputs. While ***SE*** is high, Writes to the array are disabled and the outputs are held. On the first clock cycle when ***SE*** is brought low, the rising edge of ***ICK*** causes the registers to shift and conditionally execute the scanned in instruction. If the scanned in $\overline{CKE}$ is low, the instruction executes with normal timing; if $\overline{CKE}$ is high, the outputs update to the values scanned into the Q scan bits and the RAM performs a 'NO-OP'. If a purge machine cycle number other than zero is scanned in, however, the outputs will be disabled and purge will continue regardless of the state of $\overline{CKE}$. Note: If a purge state other than zero is scanned in, the $\bar{P}$ register should be scanned in to a zero.

The purge state machine consists of 3 bits; a registered $\bar{P}$ signal and a 2 bit counter. Purge will begin anytime the $\bar{P}$ register is LOW and the $\overline{CKE}$ register is LOW. On the next ***ICK*** rising edge, the counter will increment to 1 and all inputs except ***SE*** will be ignored until the counter wraps around to 0 again. If a non-zero value is scanned into the purge state machine (which is included in the scan loop) then the purge will continue from that point on exit from Scan Mode regardless of the state of $\overline{CKE}$. The scan sequence is input ***DS,*** to ***Q0, D0*** $\overline{CKE}$, $\overline{W}$, $\overline{S}$, $\bar{P}$, *PURGE LSB, PURGE MSB,* ***A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, D1, Q1,*** to ***QS*** out.

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Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{OLEQS}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$

VSC7100EVAL2

Evaluation Board for the G-TAXI Chipset

G-TAXI EVALUATION BOARD

The G-TAXI evaluation board is a special purpose circuit board which provides a test bed suitable for evaluating the performance characteristics of the G-TAXI chipset; the VSC7101, VSC7102, VSC7103 and VSC7104.

The board is of multilayer construction and provides a 50 ohm controlled impedance transmission line environment for all high speed signals. High speed signals are launched onto the circuit board and removed by means of SMA coaxial connectors. Slower speed TTL compatible signals use a 96 pin DIN eurocard edge connector.

The board contains a socket for optional optical transmitter and receiver modules. These components are not provided with the evaluation board, but can be purchased and installed to modify the board for optical link transmission.

The multiplexer-transmitter portion of the board is physically isolated from the receiver-demultiplexer portion. In fact, the center of the board is perforated and may be separated into transmitter and receiver functions.

Each section of the evaluation board has a 125 MHz (or 106.25 MHz) crystal controlled oscillator which provides TCLK input to the G-TAXI multiplexer and transmitter and the CLK input to the receiver. In addition, two SMA clock input ports are provided. Two PECL level clock sources within 0.1% in frequency can be connected to these ports to evaluate the frequency range of the chipset. In addition the board contains LM317 voltage regulators needed to provide the +2V supply required by the multiplexer and demultiplexer chips; in this way a single +5V (5A) external supply is needed to operate the evaluation board. With the exception of the oscillators and regulators, all other components on the evaluation board are passive.

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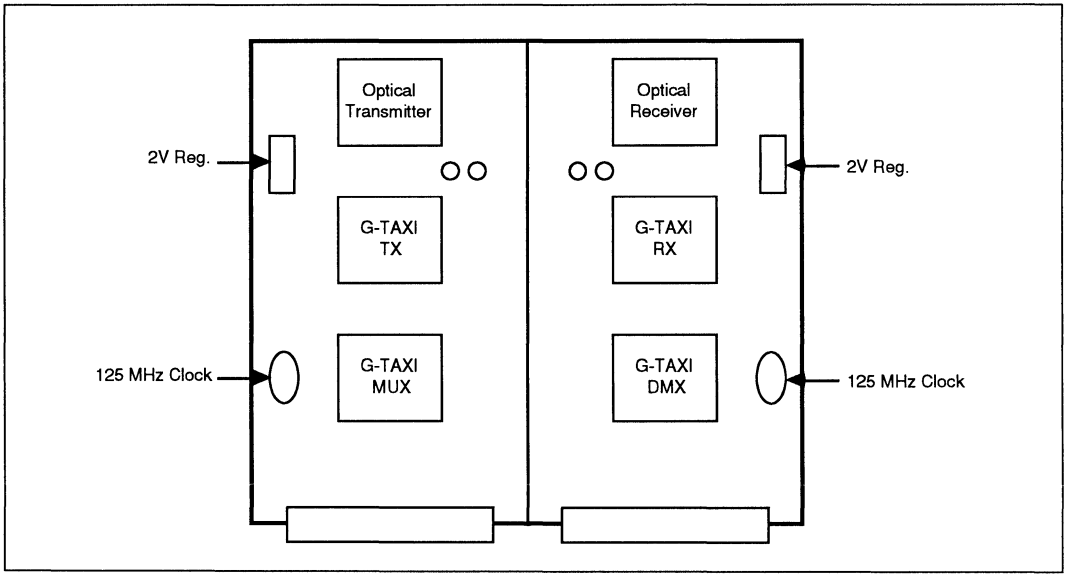
SIMPLIFIED BOARD DIAGRAM



VSP465

32-Bit Flow-Thru Error Detection and Correction Unit

FEATURES

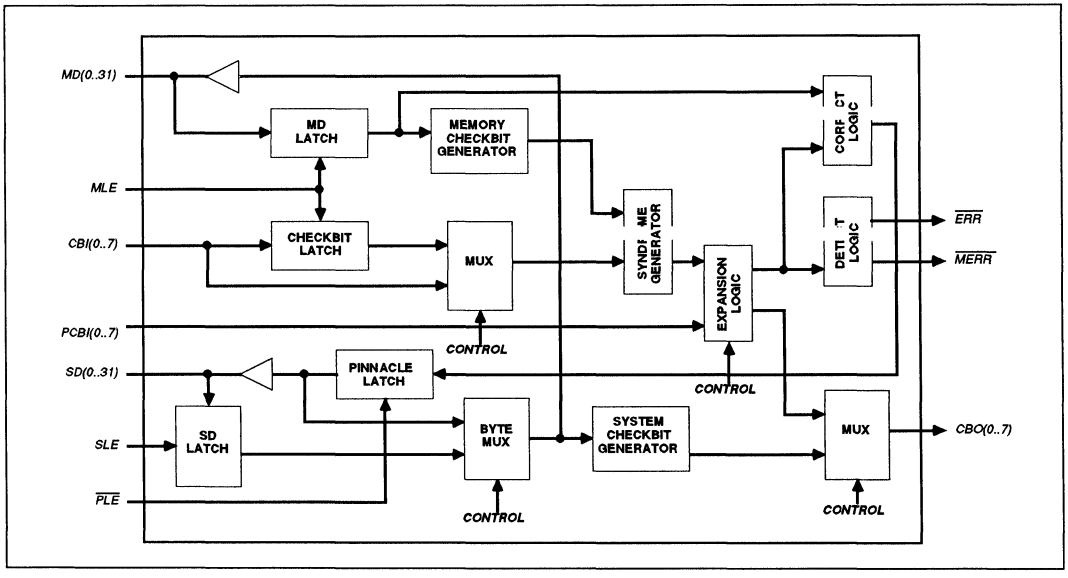
- 32-bit wide Flow-through EDC unit
- Expandable to 64 bits
- Single-chip 64-bit Generate mode
- Separate system and memory busses
- On-chip pipeline latch with external control
- Supports bi-directional and common I/O memories
- Corrects all single-bit errors
- Detects all double-bit errors, some multiple-bit errors
- Error Detection Time — 6 ns
- Error Correction Time — 9 ns
- Internal Syndrome register
- Four-bit error counter and error-data register on-chip
- Parity generation and checking on system data bus
- 211 pin PGA package

GENERAL DESCRIPTION

The VSP465 is a 32-bit, two-data bus, Flow-thru EDC unit. The chip provides single-error correction and multiple-error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading 2 units, without the need for additional external logic. The flow-thru EDC has been optimized for speed and simplicity of control.

The EDC unit has been designed to be used in either of two configurations in an error correcting memory system. The bi-directional configuration is most appropriate for systems using bi-directional memory buses. A second system configuration utilizes external octal buffers and is particularly well suited for systems using memory with separate I/O buses.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



VSA1201

High Speed 12-Bit Multiplexed Layout D/A Converter

FEATURES

- 12 bit resolution
- ECL 100K compatible
- Fully monolithic
- 52 pin LDCC package
- Drives 50Ω loads directly
- High yield H-GaAs E/D MESFET process

PRODUCT DESCRIPTION

The VSA1201 is a very fast 12 bit D/A converter designed for high performance applications such as high resolution graphics, direct digital synthesis, and arbitrary waveform generation.

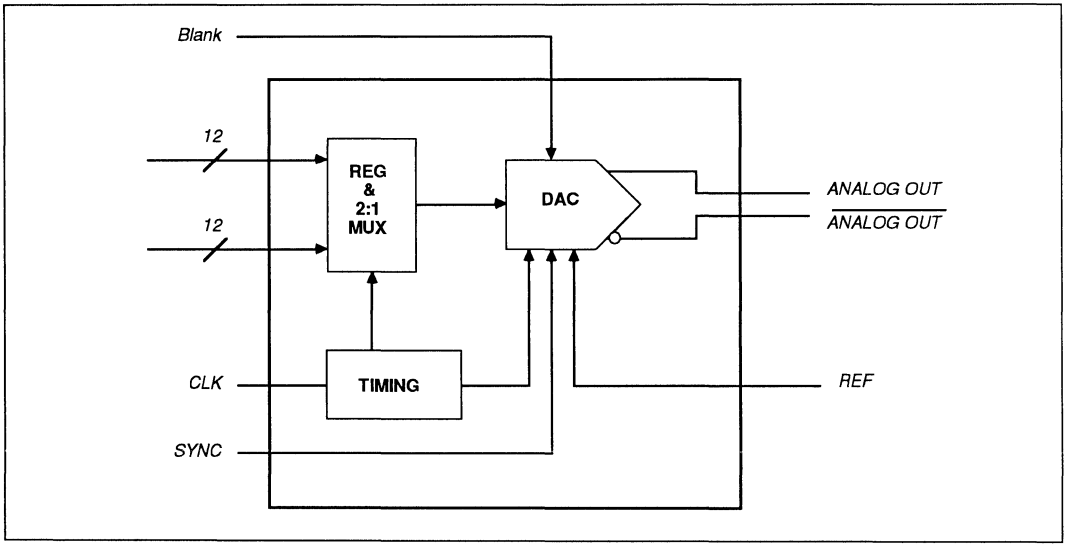
Multiplexed inputs enable data to be latched into the VSA1201 at half the output rate. The VSA1201 has outstanding AC linearity. Due to current segmentation circuitry which minimizes glitch impulse, the device is capable of near theoretical total signal to noise ratio (SNR).

The VSA1201 selects 12 bit ECL level inputs and produces true and complementary proportional current outputs (1LSB = 10μA).

The VSA1201 is physically divided into two main current source arrays: an MSB array and an LSB array. The MSB contains the three significant bits and the LSB is broken into a master-slave array. The segmentation generation for the three most significant bits reduces the resistance matching and tracking requirements so that implanted resistors are adequate. An on-chip operational amplifier provides closed loop reference tracking. Video Blank and Sync signals are inputs enabling use of the VSA1201 in high resolution video applications. The low spurious response and glitch impulse characteristics of this part make it appropriate for high fidelity waveform generation and direct digital frequency synthesizers.

The VSA1201 is a fully monolithic component packaged in a high performance 52 pin ceramic LDCC.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



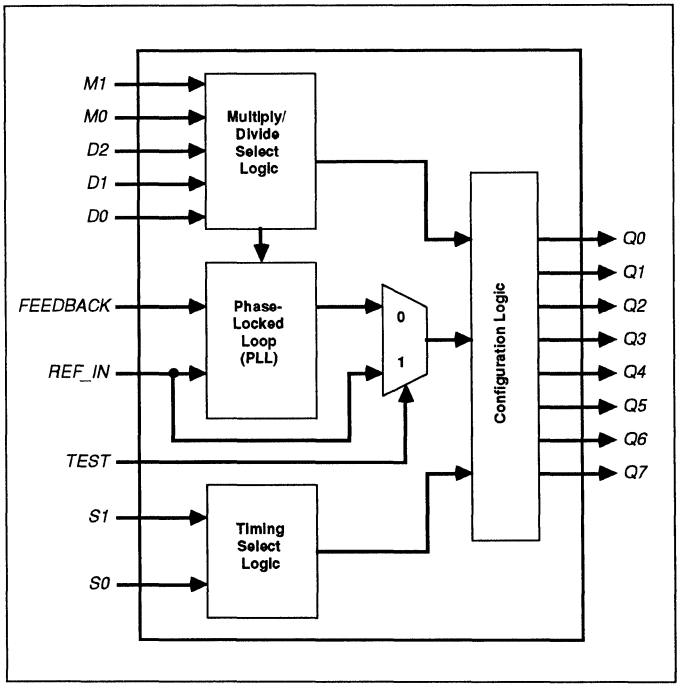
VSL4485

High Performance Clock Distribution Chip

FEATURES

- Six outputs (Q) with maximum output-to-output skew of 500 ps
- Duty cycle: 50% ± 10%
- Input reference clock frequency range from 25 to 100 MHz
- Additional outputs: Q6, Q7 at 1X, 2X, 4X the Q0-Q5 frequency
- TTL compatible inputs and outputs
- I_{OL} = 24 mA at V_{OL} = 0.5V, I_{OH} = -24mA at V_{OH} = 3.0V
- Single +5V supply
- 400 mA supply current (max)
- 0°C to 70°C ambient operating temperature
- 28 pin MQUAD™ package
- 200 ps effective delay

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The VSL4485 clock driver chip is a Low-Skew TTL I/O Clock Driver which controls the phase and frequency of the output clocks through the use of an internal Phase-Locked-Loop (PLL) which operates at between 6X and 24X the input reference clock frequency. By feeding back one of the output clocks (to the FEEDBACK input), the PLL can maintain a fixed relationship between the input reference clock (REF_IN) and all outputs. The VSL4485 can also be used as a 2X and 4X frequency multiplier by using one of the Q0-Q5 outputs as the FEEDBACK input and configuring the multiplier pins (***M1, M0***). The ***Q6, Q7*** outputs will then run at multiples of the REF_IN frequency. The VSL4485 can also generate multiple phase relationships between the clocks. These output phase relationship configurations can be selected by the choice of the output used as the feedback input and the state of the select pins (***S1, S0***). In addition, the width of the phase increment can be varied from 4% to 16% of the Q output clock period by using the divider pins (***D2:D0***).

The VSL4485 is ideal for providing and distributing system clocks in advanced microprocessor based systems requiring clock frequencies in excess of 50MHz.

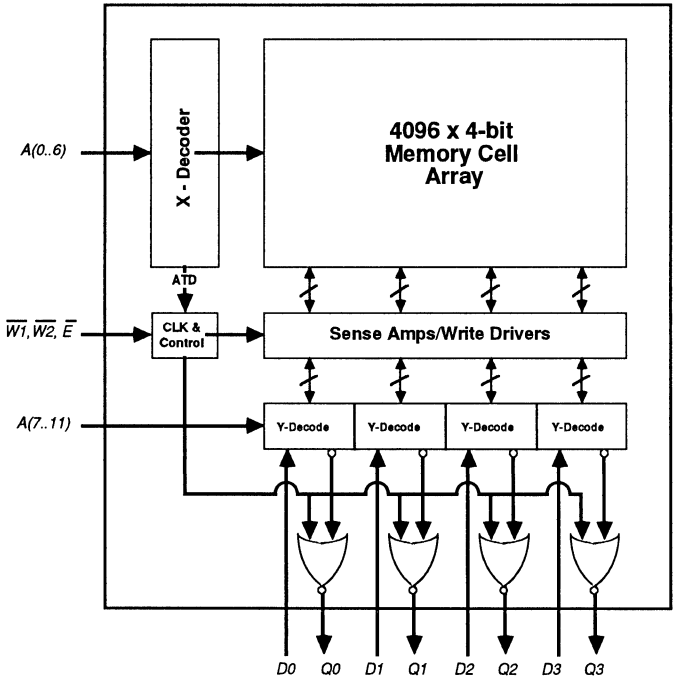
FEATURES

- 4096 words x 4-bit Static RAM, ideal for fast cache or control store applications
- Pin compatible with industry standard 100484 (except V_{TT})
- Very fast: Address access time = 5 ns (Max)
- 100K ECL compatible inputs and outputs
- Power dissipation ≤ 2 W (Typ)
- Single power supply, V_{TT} = -2.0 V ± 5%
- 28-Pin MQUAD™ package
- Edge triggered write

FUNCTIONAL DESCRIPTION

The VSM12G484 is a fully decoded 16,384 bit ECL compatible GaAs SRAM designed for extremely fast control and buffer storage applications. The device is organized as 4096 words by 4-bits, and is pin for pin compatible with industry standard 100484 with the exception that V_{EE} has been replaced by V_{TT} (-2V) for power reduction. To ease system timing requirements, the write pulse is internally generated, resulting in balanced read/write cycle times. The 12G484 is fabricated in GaAs using Vitesse proprietary E/D MESFET technology, offering an uncompromised speed/power combination which uses very few elements per logic function.

BLOCK DIAGRAM



FEATURES

- Enhancement/depletion GaAs process
- VLSI complexity
- Self-aligned active devices
- 0.8 micron effective gate length
- 4 inch diameter GaAs wafers
- Sub-100 ps gate delays
- Four interconnect levels
- Extended temperature range operation
- Radiation resistant
- Mil 883C processing

GaAs ADVANTAGES

Gallium arsenide is the clear IC technology choice where either speed alone or speed and power are the critical design parameters. GaAs derives its superiority from a variety of factors, including a high electron mobility which results in very fast MESFETs, and an inherent hardness to ionizing radiation. To these, enhancement/depletion (E/D) mode technology adds compatibility with logic families which require relatively small numbers of active devices per function implemented.

GaAs E/D technology allows the designer the flexibility of implementing a variety of logic families, including the ones available in D-mode technology. Some of the well known families open to use in E/D GaAs are Direct-Coupled FET Logic (DCFL), Source-Coupled FET Logic (SCFL), Buffered Direct-Coupled FET logic (BDCFL), Buffered FET logic (BFL) and Schottky diode FET Logic (SFL). Each family has unique power dissipation, gate delay, and load drive characteristics. Any and all of these logic families can be mixed in the same circuit to optimize performance.

THE H-GaAs II PROCESS

Vitesse offers a second generation NMOS-like, planar process for the fabrication of digital and mixed analog-digital integrated circuits.

H-GaAs II is a scaled version of the process first implemented by Vitesse in 1986. The high yield and manufacturability of this approach has been established through volume shipment of VLSI complexity circuits for use in a wide array of applications.

The H-GaAs II process employs up to four levels of metallization requiring as little as eleven mask levels to produce self-aligned MESFETs and diodes. H-GaAs II is currently used by Vitesse to implement standard and semi-custom products including the FURY Series of gate arrays, proprietary high performance processor chip sets, and static RAMs.

The use of a tungsten-based refractory metal for gates and local interconnects ensures stability during high temperature processing. As in VLSI silicon processing, an aluminum alloy is used for the four levels of global interconnects. Dry etching of metals and dielectrics is used throughout in order to maximize yields.

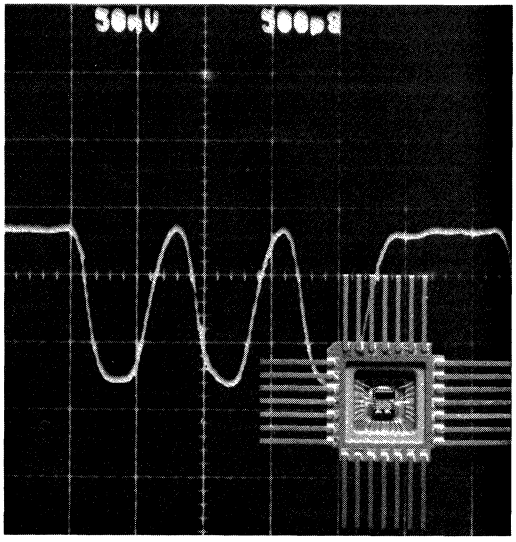
QUALITY ASSURANCE

Quality control mechanisms are built into every step of Vitesse's fabrication process, from wafer acquisition to final testing. These mechanisms, like the models and design tools, are continually refined through use in the production of Vitesse's standard products.

The assurance of the quality of finished wafers begins before the wafers are received at

H-GaAs II METAL PITCHES

Metal	*Line Width*	*Spacing*
Gate	0.8	1.5
Metal 1	1.5	2
Metal 2	2	2
Metal 3	3	3
Metal 4	Unpatterned	



The Vitesse process can be used to implement circuits which operate at clock rates well above 1 GHz. The 4:1 multiplexer shown above uses SCFL circuitry and operates at 2.5 Gb/s.

Vitesse's facility. Four inch diameter semi-insulating GaAs wafers are used exclusively for H-GaAs II processing. Careful screening has already reduced the number of vendors from which Vitesse acquires its wafers to a relative few. These suppliers have been provided with a proprietary set of requirements specifying how Vitesse's wafers must be prepared, cleaned, tested, and packaged for our use.

Wafers in process are inspected at 33 points, tested in processing, and tested again after final passivation.

The H-GaAs process currently uses 5x steppers with a maximum reticle size of 13mm x 13mm. Each reticle contains a process control monitor (PCM) for use in parametric screening and quality control. At each of the metallization steps, the devices within the PCM are inspected and measured. In addition to other parameters, transistor quality, transistor-to-transistor variation, and metal connections (shorts/opens) are checked.

Final results of the measurement of PCMs at various positions on the wafer determine whether a wafer will be released to the customer. The results of the PCM measurements are released to the customer with the wafers.

CUSTOMER SUPPORT

Vitesse offers the designer an array of design tools and support services developed specifically for custom designs. These tools and services have been assembled to provide a designer with a high degree of confidence to implement high performance circuits which will function correctly the first time.

Before any instruction or design has begun, a joint review of the customer's requirements is performed and a Vitesse project manager is assigned to support and track each foundry program. This project manager is provided to insure timely response to a customer's needs during the program and to report the status of the customer's wafers at any time during the fabrication cycle.

The Vitesse Foundry Design Manual, a proprietary publication which is released to the customer on a non-disclosure basis, provides a road map through the design and fabrication process. This manual, when combined with the design training course offered by Vitesse, provides a comprehensive method by which designers can familiarize themselves with the process, rules, aids, and tools, as well as specific examples of Vitesse's digital GaAs IC design process.

The guide provides complete instructions for designing custom cells compatible with the Vitesse standard cell library. In addition, it contains information on testing and packaging, including test vector formats and assembly/build diagrams for the entire line of Vitesse high-speed packages.

Vitesse supports the HSPICE* circuit simulator for use in full custom design projects. HSPICE is one of the most popular commercially available simulators and is characterized by excellent convergence and pre- and post-processing facilities.

SCFL

MACRO	DELAY	DELAY/ F.O.	WIRE DELAY	P_D
Inverter	140ps	15ps	70ps/mm	23mW
D Flip-flop	230ps	15ps	70ps/mm	45mW
2:1 Mux Select→ Output	160ps	15ps	70ps/mm	23mW

DCFL

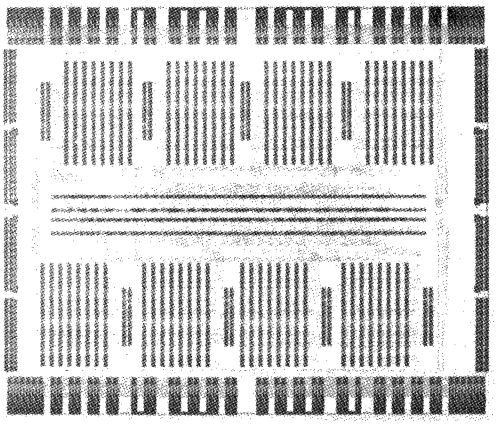
FUNCTION	DELAY	DELAY/ F.O.	WIRE DELAY	P_D
Inverter	90ps	13ps	80ps/mm	1.0mW
D Flip-flop	400ps	13ps	80ps/mm	3.9mW
2:1 Mux Select→ Output	300ps	13ps	80ps/mm	2.1mW

The parameters shown above are provided as a quick reference to the performance of two commonly used logic families implemented using Vitesse's proprietary process. The data reflects the fact that the choice of logic depends heavily on the circuit — or portion of a circuit — being produced (more than one logic type may be mixed in a given design).

These parameters are based on worst case characteristics, and 70° C operation. All of the delay values assume unit fan-out and no metal loading. All D-mode devices were used to implement the two level series gated SCFL example. The nominal supply voltage for SCFL is -5.2V. Both E-mode and D-mode devices were employed to implement the DCFL circuits. The nominal supply voltage for DCFL is -2V.

**HSPICE is a product of Meta-Software*

Photomicrograph of a 22K gate chip implemented in H-GaAs II



Vitesse, in conjunction with Meta-Software, has developed a model which accurately reflects the characteristics of MESFETs fabricated in the H-GaAs II process. The temperature dependent model includes backgating, short and narrow channel effects, and velocity saturation.

Parameter files that represent device performance shifts due to process variations are supplied by Vitesse for use with the HSPICE simulator. With the aid of HSPICE, the designer can simulate circuit performance over all process corners, thereby simplifying performance/yield trade-offs.

Several other software tools are also provided, including ECAD-compatible files for physical layout design rule checking, electrical design rule checking, and layout-vs-schematic checking.

Design consultation with Vitesse senior circuit designers is included as part of the standard foundry program package, and an optional classroom course is offered for in-depth review of the design, testing, and packaging of VLSI GaAs circuits. Use of Vitesse's design center is also optionally available. Final design results can be submitted in the form of GDS II or CIF format tapes.

OPTIONAL SERVICES

Assembly and testing are provided as customer options. This includes functional and critical path testing at both the wafer level and for packaged parts. Vitesse has a full complement of IC test equipment including a Teradyne J953 high pin count tester and Teradyne J386 memory tester. The J953 can accommodate up to 256 I/O signals with a maximum data rate of 50MHz. The edge placement accuracy on both inputs and outputs is ± 250psec. The J386 has an algorithmic pattern generator for the generation of regular bit patterns. That system is capable of functional pattern generation at a maximum rate of 100MHz, and has an input signal

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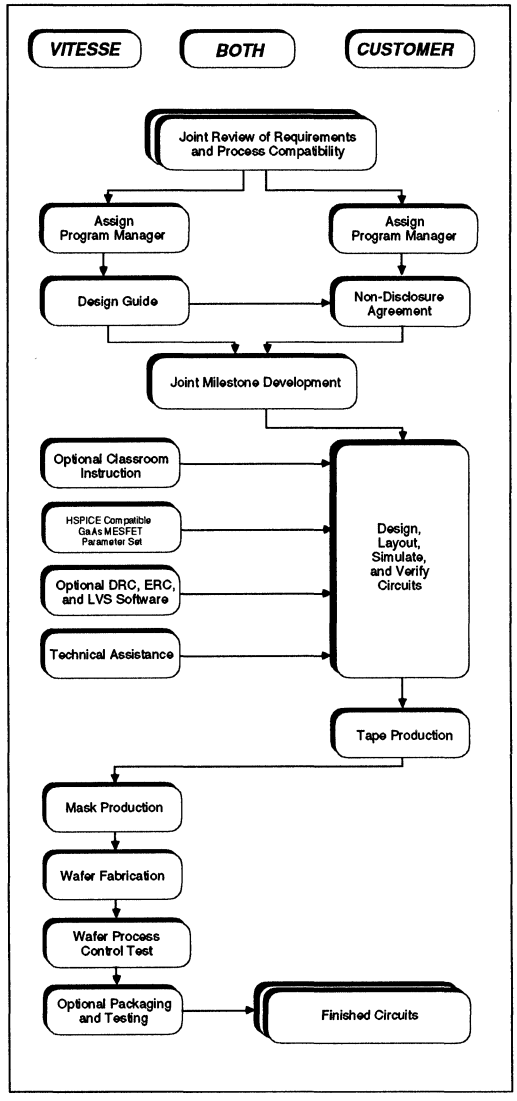
rise/fall time of under 400ps. AC parameters for the tester include a 1GHz bandwidth, 50ps resolution, and 200ps measurement accuracy. More detailed specifications of its capabilities are available upon request.

Assembly and packaging services are available. Ceramic chip carriers, DIPs, and pin grid arrays capable of supporting edge rates of 150ps are the standard package forms; custom package development will be considered as a special quote. Vitesse can provide Mil 883 compliant chips to customer specifications.

TURNAROUND

In a typical IC development program most of the time is spent on design and layout, which is the responsibility of the customer. The primary goal of Vitesse's consulting services and software tools is to minimize that portion of the schedule. Once the design and layout are complete, the time from mask procurement to tested wafers usually requires six to seven weeks. This includes one week for mask making, three to four weeks for fabrication and two weeks for assembly and test.

VITESSE FOUNDRY DESIGN FLOW



Vitesse Standard Packages

INTRODUCTION

This section contains the outlines for all of the standard packages currently offered by Vitesse. Most of these packages are cavity down, multilayer ceramic packages with Cu-W heat spreaders for efficient cooling. This arrangement results in controlled impedance on signals, good cross talk control, low impedance power supply leads and low thermal resistance from junction to case. In addition to the ceramic packages, Vitesse offers the28-pin J-lead MQUAD™ and the 132-pin MQUAD which are both low cost, high volume packages. Two plastic packages are offered as well: the 415 plastic PGA and the 557 plastic PGA.

In most ASIC designs, the size of the die and package are dictated by the number of signal I/O and/or equivalent gates. Table 1 summarizes the standard packages with the corresponding die size and maximum signal I/O that can be accomodated. Vitesse has complete assembly facilities, and die can be assembled in non-Vitesse packages. New packages may be currently under development based on new standard products and customer designs. If none of the packages listed in the table meet your requirements, contact Vitesse for the latest information on package availability.

Table 2 summarizes Vitesse's standard products and the packages which are available for each. Also listed is the page on which the package drawing appears.

TABLE 1: VITESSE STANDARD PACKAGES

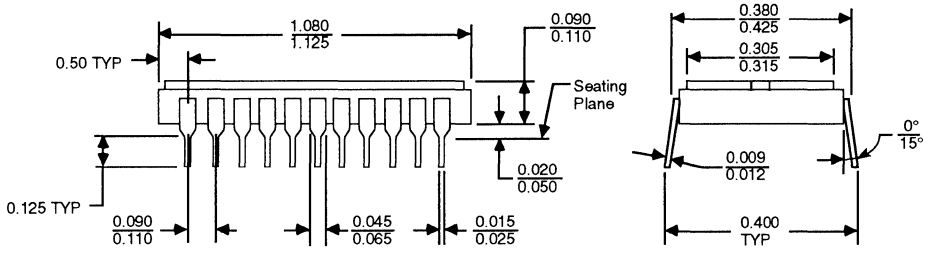
Package	*# of I/O (Max. Outputs)*	*Die Size (μm)*
22 pin Ceramic DIP	20	2160 x 2450 2880 x 2450
24 pin Ceramic DIP	22	2880 x 2450 4325 x 3675
28 pin LDCC or LCC	26	2160 x 2450 2880 x 2450
52 pin LDCC or LCC, or	41	2880 x 3671
52 pin J-lead MQUAD	41	4325 x 3675
132 pin LDCC or MQUAD	92	3440 x 5540
149 pin PGA	120	4325 x 7350
164 pin LDCC	120	4325 x 7350
211 pin PGA	174	8650 x 7350
256 pin LDCC	196	8650 x 7350
344 pin LDCC	256	13780 x 7730
415 pin PPGA	172	12970 x 9930
557 pin PPGA	250	14950 x 14750

TABLE 2: PRODUCT VS. PACKAGE SUMMARY

Product	*Description*	*Packages*	*Page*
VS8001/VS8002	12:1 Multiplexer/1:12 Demulti plexer Chip Set	52 pin Ceramic LDCC or LCC	7-6
VS8004/VS8005	4:1 Multiplexer/1:4 Demultiplexer Chip Set (2.5 Gb/s)	28 pin Ceramic LDCC or LCC	7-4
VS8010/VS8011/ VS8012	SONET - High Speed 8 Bit Mux/Demux Products	52 pin Ceramic LDCC or LCC	7-6
VS8021/VS8022	SONET - 2.5 Gb/s Chip Set 8-Bit Mux/Demux	52 pin Ceramic LDCC or LCC	7-6
VS12G422T	256 x 4 Static RAM (TTL)	22 pin Ceramic DIP	7-3
VS12G478 w/Purge	2K x 2 Self-Timed Static RAM	28 pin Ceramic LDCC	7-4
VS12G484	4K x 4 Self-Timed Static RAM	28 Pin Ceramic LDCC	7-4
VSC1520	HS Series, 1500 Gate Structured Cell Array (2.5GHz)	52 pin Ceramic LDCC or LCC	7-6
VSC864	64 x 64 Crosspoint Switch	344 pin Ceramic LDCC	7-17
VSC7101/7102	1.25 Gb/s Data Communications Transmitter/Receiver	28 pin Ceramic LDCC	7-4
VSC7103/7104	1.25 Gb/s Data Communications Mux/Demux	132 pin J-Lead MQUAD	7-8
VSC3K	FURY Series, 3500 Gate Array	132 pin Ceramic LDCC	7-9
VSC5K	FURY Series, 6400 Gate Array	149 pin Ceramic PGA 164 pin Ceramic LDCC or LCC	7-11 7-12
VSC10K	FURY Series, 13000 Gate Array	211 pin Ceramic PGA 256 pin Ceramic LDCC	7-14 7-15
VSC15K	FURY Series, 17000 Gate Array	211 pin Ceramic PGA 256 pin Ceramic LDCC	7-14 7-15
VSC30K	FURY Series, 30,000 Gate Array	344 pin Ceramic LDCC	7-17
PLR2KT	2400 Gate TTL Compatible GaAs Gate Array	132 pin MQUAD	7-8
FX20K	FX Series, 20,000 Gate Array	52 pin Ceramic LDCC 132 pin Ceramic LDCC	7-6 7-9
FX40K [2]	FX Series, 40,000 Gate Array	184 pin Ceramic PGA[1]	—
FX100K	FX Series, 100,000 Gate Array	211 pin Ceramic PGA 256 pin Ceramic LDCC	7-14 7-15
FX200K [2]	FX Series, 220,000 Gate Array	415 Plastic PGA	7-18
FX350K [2]	FX Series, 350,000 Gate Array	557 Plastic PGA	7-20

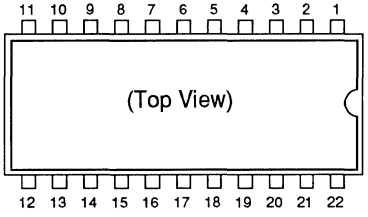
NOTES:
1) In development
2) Preliminary

22 PIN CERAMIC DIP PACKAGE

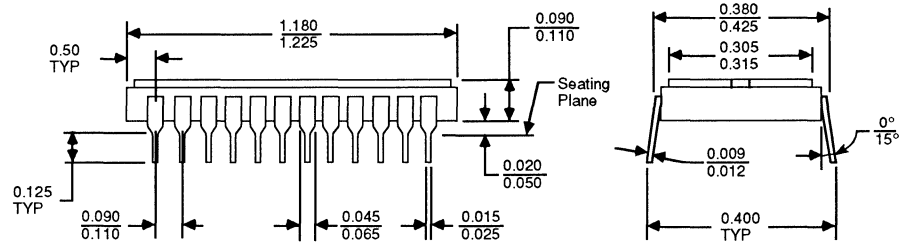


22-pin leaded (400 mil) sidebraze dual in-line package

Pin	*Function*
1-7	Input/Output
8	– Supply
9-21	Input/Output
22	+ Supply

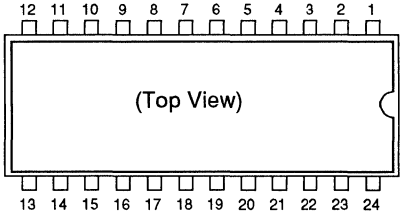


24 PIN CERAMIC DIP PACKAGE



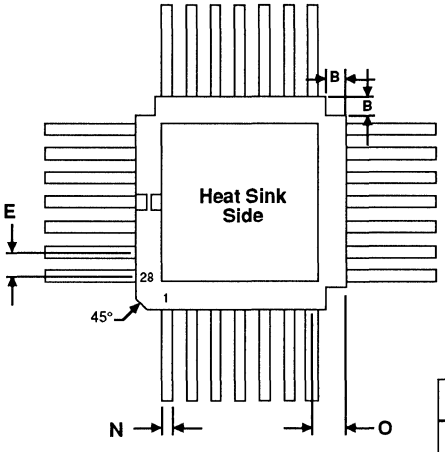
24-pin leaded (400 mil) sidebraze dual in-line package

Pin	*Function*
1-5	Input/Output
6	+ Supply
7	Extra Supply or I/O
8-17	Input/Output
18	– Supply
19-24	Input/Output

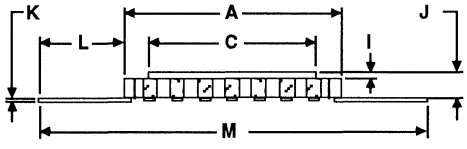


NOTES: *1) Drawings not to scale.*
2) All dimensions given in inches.
3) Max. and min. tolerance are indicated.
4) Package: Ceramic (alumina); Heat sink: Copper-tungsten; Leads: Alloy 42 with gold plating.

28 PIN CERAMIC LDCC AND LCC PACKAGES

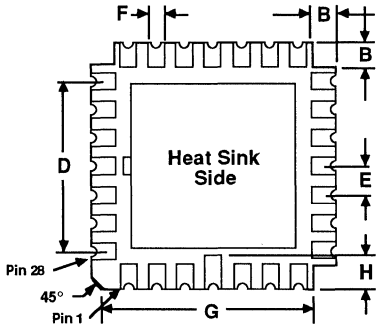


28-Pin Leaded Ceramic Package (LDCC)

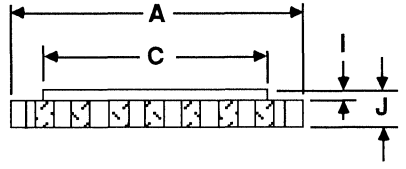


28 Pin LDCC or LCC Pin Functions

Pin	*Function*	*Pin*	*Function*
1-3	Input/Output	18	Supply or I/O
4	Supply or I/O	19-24	Input/Output
5-10	Input/Output	25	- Supply (Substrate)
11	Supply or I/O	26-28	Input/Output
12-17	Input/Output		

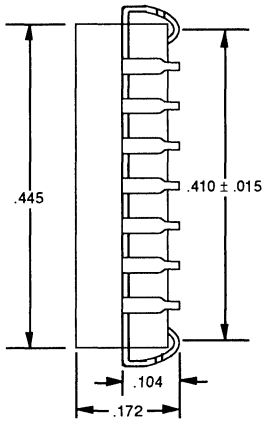


28 Pin Leadless Ceramic Package (LCC)

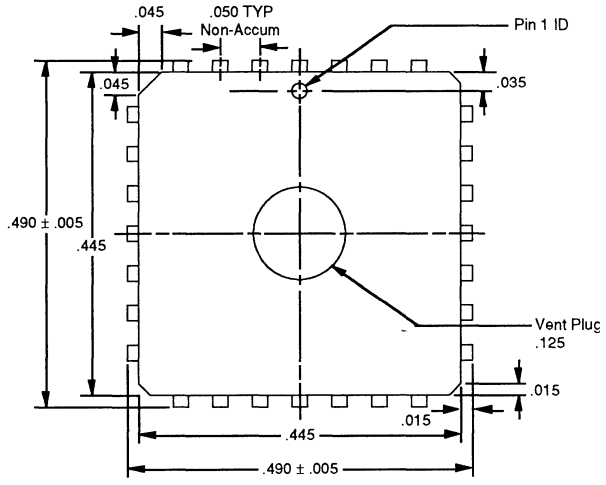


Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	11.176/11.682	0.440/0.460	I	0.406/0.610	0.016/0.024
B	1.016/1.524	0.040/0.060	J	1.715/2.223	0.075/0.095
C	9.652/10.160	0.300 TYP	K	0.090/0.242	0.004/0.008
D	7.493/7.747	0.300 TYP	L	5.842/6.858	0.230/0.270
E	1.143/1.397	0.050 TYP	M	22.860/25.398	0.900/1.000
F	0.762/1.016	0.035 TYP	N	0.356/0.559	0.014/0.022
G	9.271	0.365	O	1.525/2.287	0.075 TYP
H	1.778	0.070			

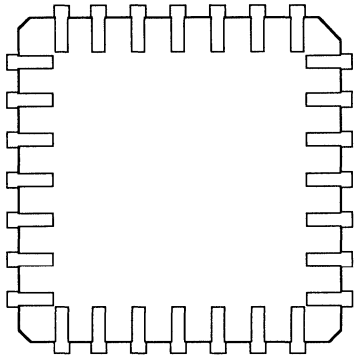
28 PIN J-LEAD MQUAD™ PACKAGE



SIDE VIEW



TOP VIEW

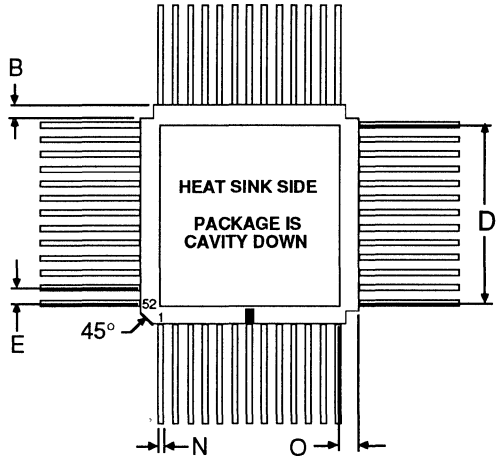


BOTTOM VIEW

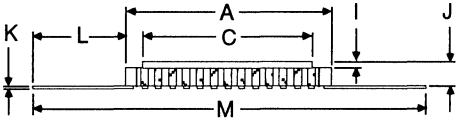
NOTES: *1) All non-toleranced dimensions are shown at nominal.*
2) All dimensions in inches.
3) Drawing not to scale.
4) Package is black annodized Aluminum.Leads are copper alloy.

7

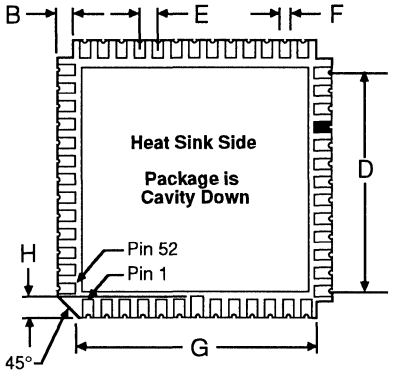
52 PIN CERAMIC LDCC AND LCC PACKAGES



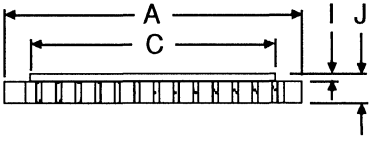
52 Pin Leaded Ceramic Package (LDCC)



Pin	Function
1-3, 5-6, 8-9, 11-17	Input/Output
19-22, 24-29, 31-32	Input/Output
34-35, 37-42, 44-45	Input/Output
47-48, 50-52	Input/Output
4,10,18,30,36,43,49	GND
7,46	(-) Supply 1
33	Supply 2
23	(substrate)



52 Pin Leadless Ceramic Package (LCC)

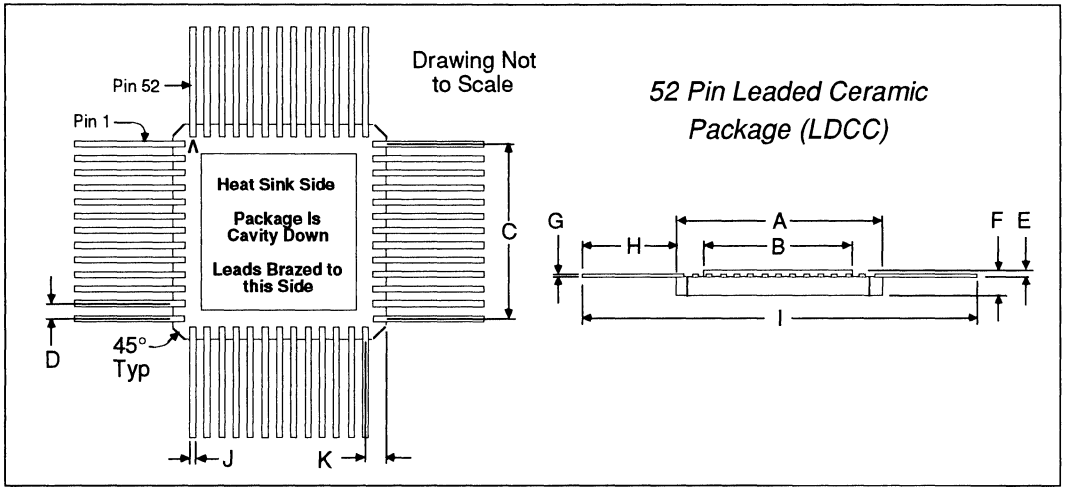


Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	18.54/19.56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.83/5.08	0.190/0.200
E	1.27 TYP	0.050 TYP	M	29.46 TYP	1.160 TYP
F	0.76/1.02	0.030/0.040	N	0.36/0.56	0.014/0.022
G	16.94 TYP	0.667 TYP	O	1.75/1.90	0.069/0.075
H	1.91/2.41	0.075/0.095			

** At package body.*

NOTES:
1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

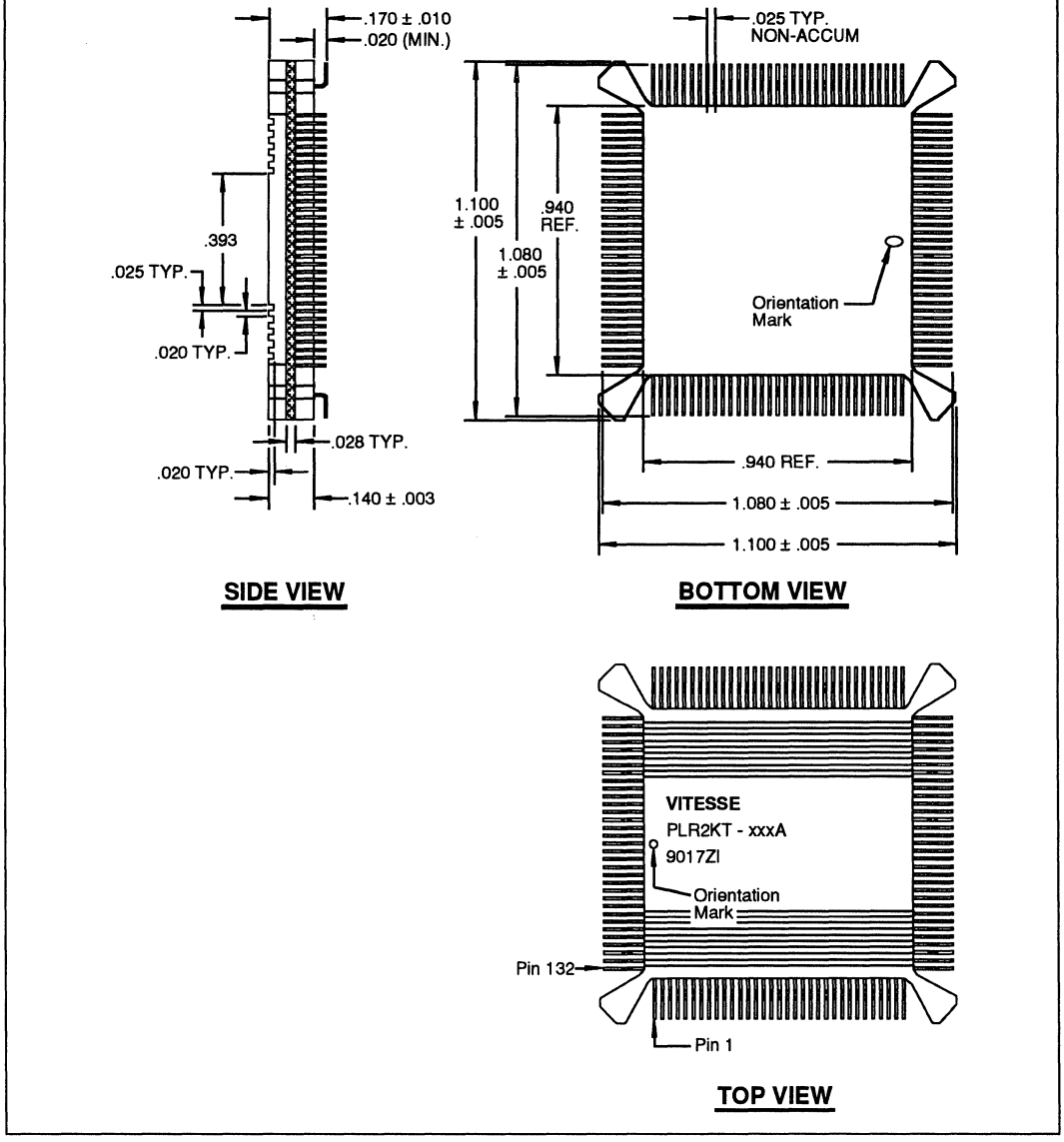
52 PIN CERAMIC LDCC PACKAGE (FOR FURY VSC3K ONLY)



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	18.54/19.56	0.730/0.770	G	0.09/0.24	0.003/0.009
B	12.700/13.208	0.500/0.520	H	5.84/6.10	0.230/0.240
C*	15.24 TYP	0.600 TYP	I	31.75 TYP	1.25 TYP
D*	1.27 TYP	0.050 TYP	J	0.36/0.56	0.014/0.022
E	0.41/0.61	0.016/0.024	K*	1.75/1.90	0.069/0.075
F	2.03/2.79	0.080/0.110			

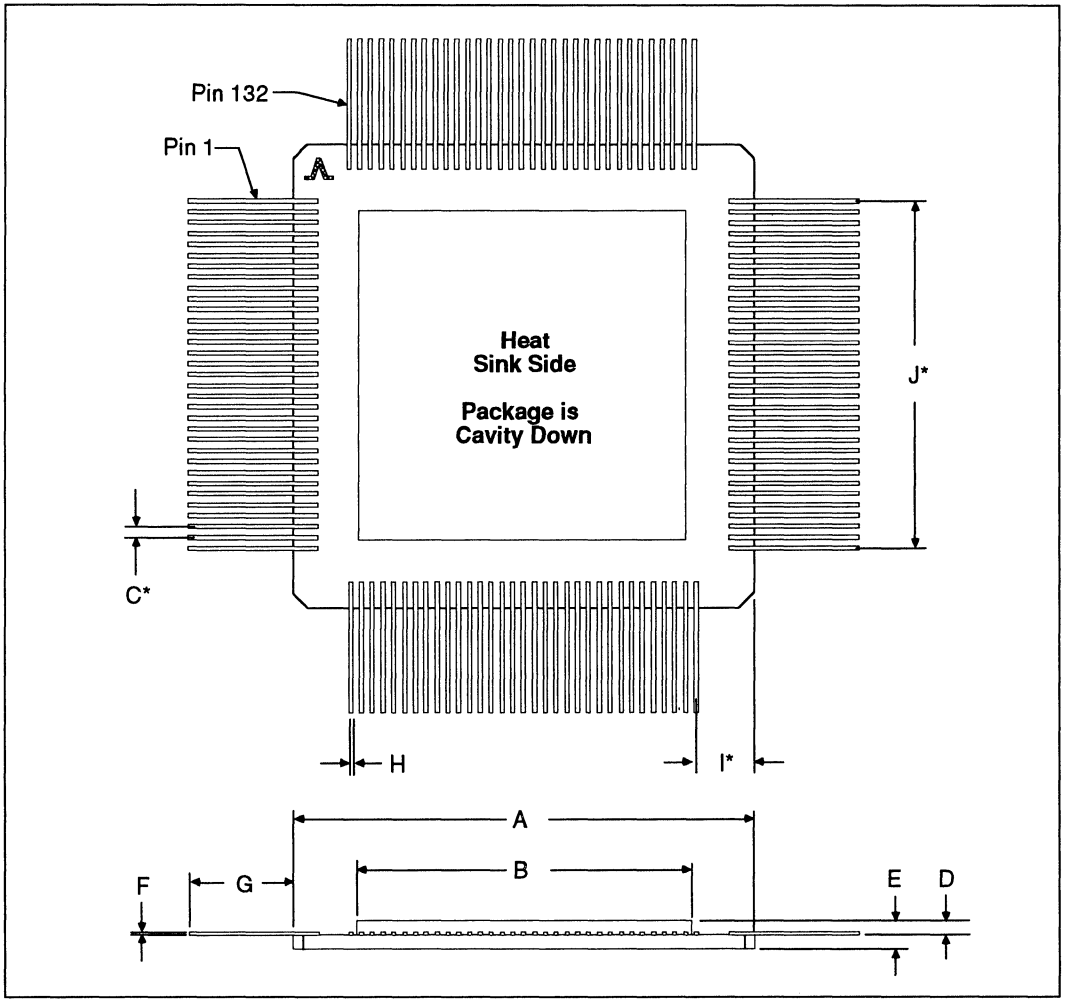
* At package body.

132 LEAD MQUAD™ FLATPACK PACKAGE



NOTES: 1) Drawing not to scale.
2) All non-toleranced dimensions are shown at nominal and tolerance is ± .010 unless otherwise noted.
3) Package is black annodized Aluminum. Leads are copper alloy.

132 PIN CERAMIC LDCC PACKAGE



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	23.75/24.51	0.935/0.965	F	0.09/0.24	0.004/0.008
B	18.67/19.43	0.750 TYP	G	5.08/7.62	0.200/0.250
C*	0.64 TYP	0.025 TYP	H	0.15/0.26	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	1.91 TYP	0.075 TYP
E	2.16/2.52	0.085/0.115	J*	20.32 TYP	0.800 TYP

** At package body.*

NOTES:
1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

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132 PIN CERAMIC LDCC PIN IDENTIFICATION*

Input/Output Pins	*Power/GND Pins*
1, 2, 6-15, 17-27, 31-33, 35, 36, 38-40, 44-46, 48-51, 53-55, 59-61, 63, 64, 66-68, 72-81, 84-93, 97-99, 101, 102, 104-106, 110-112, 114-117, 119-121, 125-127, 129, 130, 132	3, 4, 5, 16, 17, 28, 29, 30, 34, 37, 41, 42, 43, 47, 52, 56, 57, 58, 62, 65, 69, 70, 71, 82, 83, 94, 95, 96, 100, 103, 107, 108, 109, 113, 118, 122, 123, 124,128, 131

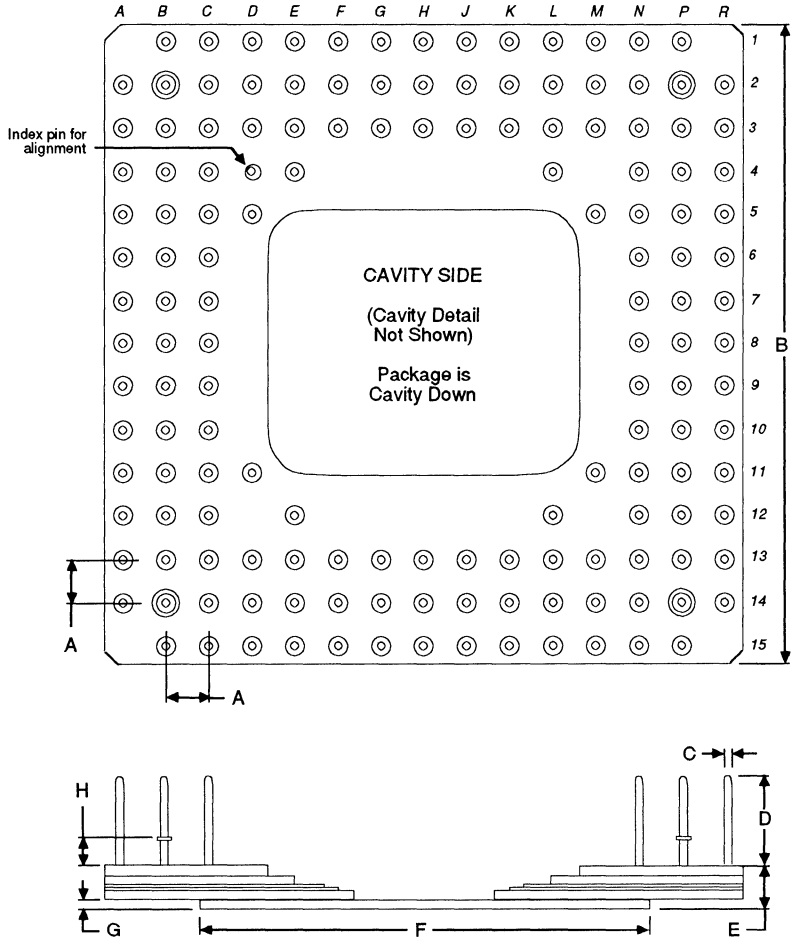
**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

149 PIN CERAMIC PGA PIN IDENTIFICATION*

Input/Output Pins	*Power/GND Pins*
A2-A14, B1-B15, C1-C5, C11-C15, D1-D3, D13-D15, E1-E3, E13-E15, F1, F2, F14, F15, G1, G2, G14, H1, H2, H14, H15, J1, J2, J14, J15, K1, K2, K14, K15, L1-L3, L13-L15, M1-M3, M13-M15, N1-N5, N11-N15, P1-P15, R2-R14	C6, C7, C8, C9, C10, D4 D5, D11, E4, E12, F3, F13, G3, G13, H3, H13, J3, J13, K3, K13 L4, L12, M5, M11, N6, N7, N8, N9, N10

**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

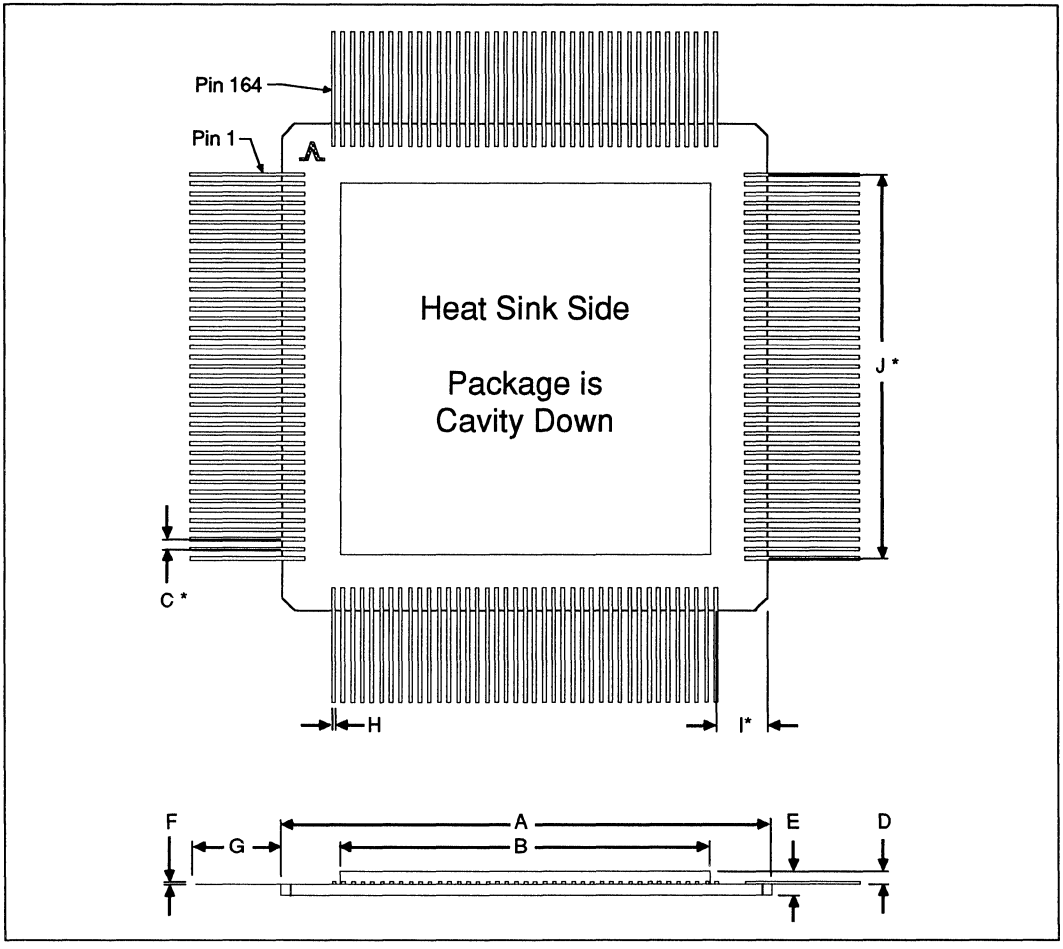
149 PIN CERAMIC PGA PACKAGE



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	2.54 TYP	0.100 TYP	E	2.25/2.92	0.085/0.115
B	37.85/38.61 SQ	1.490/1.520 SQ	F	27.40 TYP (Heatsink)	1.08 TYP (Heatsink)
C	0.41/0.51 DIA	0.016/0.020 DIA	G	0.38/0.63	0.015/0.025
D	4.45/4.95	0.175/0.195	H	1.14/1.40 (4 Plcs)	.050 TYP

Notes: 1) Drawing not to scale.
2) Package: Ceramic (alumina); Heat sink: Copper-tungsten; Leads: Alloy 42 with gold plating

164 PIN CERAMIC LDCC PACKAGE



Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	28.58/29.84 SQ	1.130/1.170	F	0.09/0.22	0.004/0.008
B	Ref 24 SQ	Ref 0.95 SQ	G	5.08/7.62	0.200/0.300
C*	0.64 TYP	0.025 TYP	H	0.15/0.25	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	Ref 1.91 TYP	Ref 0.075 TYP
E	2.16/2.92	0.085/0.115	J*	25.40 TYP	1.00 TYP

* At package body

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

164 PIN CERAMIC LDCC PIN IDENTIFICATION*

Input/Output Pins	*Power/GND Pins*
1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 16, 18-20, 22-24, 26, 27, 29, 30, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45, 48-53, 55-61, 63-69, 71-76, 79, 80, 82, 83, 85, 86, 88, 89, 91, 92, 94, 95, 97, 98, 100-102, 104-109, 111, 112, 114, 115, 117, 118, 120, 121, 123, 124, 126, 127, 130-135, 137-143, 145-151, 153-158, 161, 162, 164	2, 5, 8, 11, 14, 17, 21, 25, 28, 31, 34, 37, 40, 43, 46, 47, 54, 62, 70, 77, 78, 81, 84, 87, 90, 93, 96, 99, 103, 107, 110, 113, 116, 119, 122, 125, 128, 129, 144, 159, 163

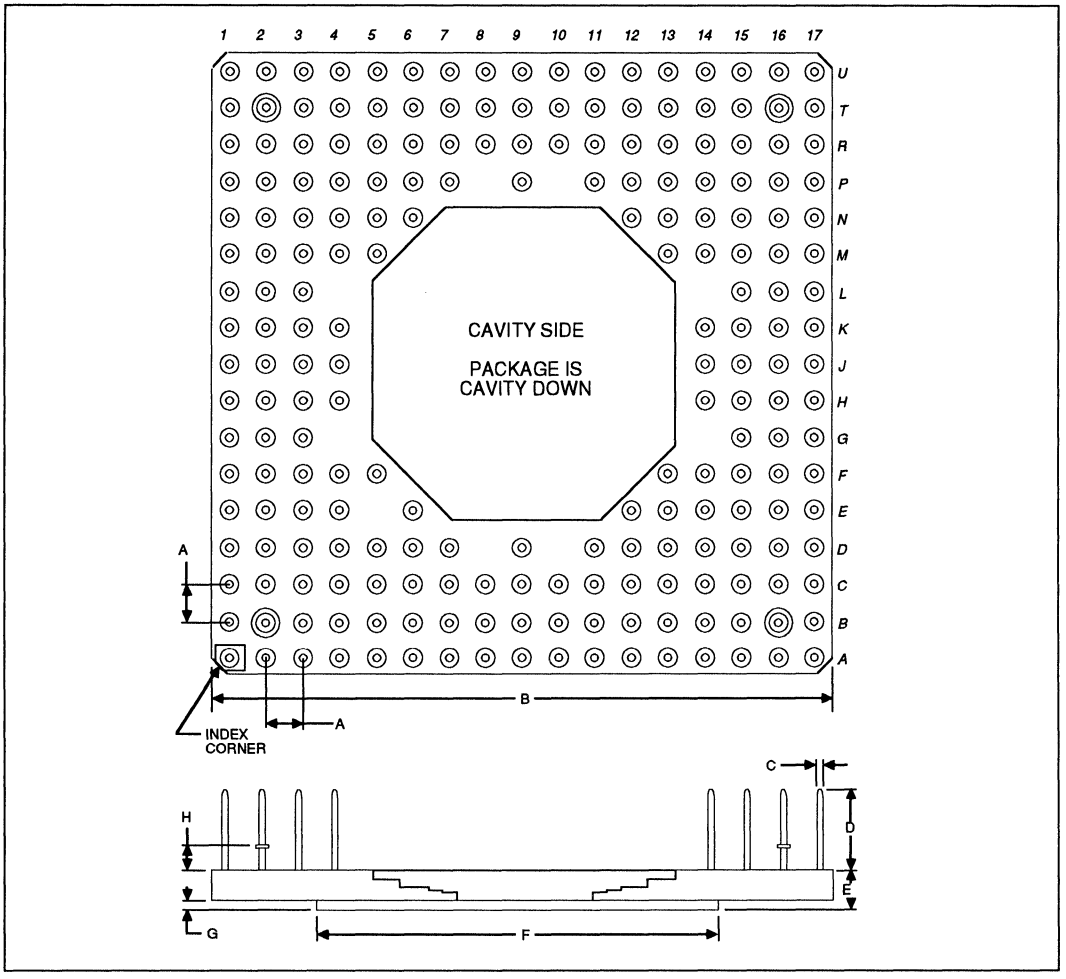
**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

211 PIN CERAMIC PGA PIN IDENTIFICATION*

Input/Output Pins	*Power/GND Pins*
A1-A17, B1-B17, C1-C17, D1-D3, D6, D12, D14-D17, E1-E3, E13, E15-E17, F1-F3, F15-F17, G1-G3, G15-G17, H1-H3, H15-H17, J1-J3, J15-J17, K1-K3, K15-K17, L1-L3, L15-L17, M1-M3, M15-M17, N1-N3, N5, N15-N17, P1-P3, P6, P12, P15-P17, R1-R17, S1-S17, V1-V17	D4, D5, D7, D9, D11, D13, D14, E4, E6, E12, E14, F4, F5, F13, F14, H4, H14, J4, J14, K4, K14, M4, M5, M13, M14, N4, N6, N12, N13, N14, P4, P5, P7, P9, P11, P13, P14

**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

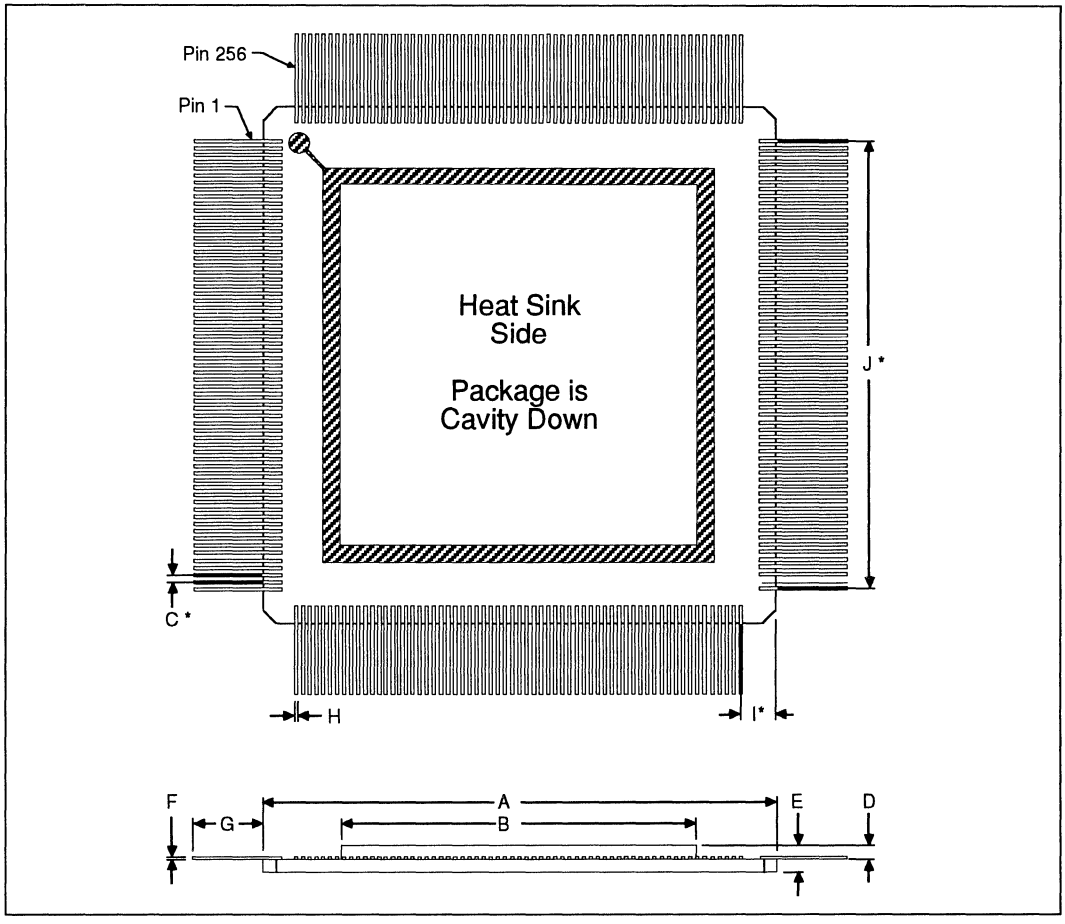
211 PIN CERAMIC PGA PACKAGE



Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	2.54 TYP	0.100 TYP	E	2.16/2.92	0.085/0.115
B	42.42/43.69	1.670/1.710	F	27.4 REF (Heatsink)	1.08 REF (Heatsink)
C	0.41/0.51 DIA	0.016/0.020 DIA	G	0.38/0.63	0.015/0.025
D	4.45/4.95	0.175/0.195	H	1.14/1.40 (4 Plcs)	.050 TYP

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

256 PIN CERAMIC LDCC PACKAGE



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	36.57/37.59 SQ	1.440/1.480 SQ	F	0.09/0.216	0.004/0.008
B	TYP 28 SQ	TYP 1.00 SQ	G	5.08/7.62	0.200/0.300
C*	0.51 TYP	0.020 TYP	H	0.15/0.25	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	REF 2.54 TYP	REF 0.100 TYP
E	2.16/2.92	0.085/0.115	J*	32.00 TYP	1.26 TYP

** At package body*

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

256 PIN CERAMIC LDCC PIN IDENTIFICATION*

Input/Output Pins	*Power/GND Pins*
3-5, 7-10, 12-15, 19-23, 25-28, 30, 31, 34, 35, 37-40, 42-45, 46, 50-53, 55-58, 60-62, 65-67, 71-86, 89-104, 107-122, 126-128, 131-133, 135-138, 140-143, 147-151, 153-156, 158, 159, 162, 163, 165-168, 170-174, 178-181, 183-186, 188-190, 193-195, 199-214, 217-232, 235-250, 254-256	1, 2, 6, 11, 16, 17, 18, 24, 29, 32, 33, 36, 41, 47, 48, 49, 54, 59, 63, 64, 68, 69, 70, 87, 88, 105, 106, 123, 124, 125, 129, 130, 134, 139, 144, 145, 146, 152, 157, 160, 161, 164, 169, 175, 176, 177, 182, 187, 191, 192, 196, 197, 198, 215, 216, 233, 234, 251, 252, 253

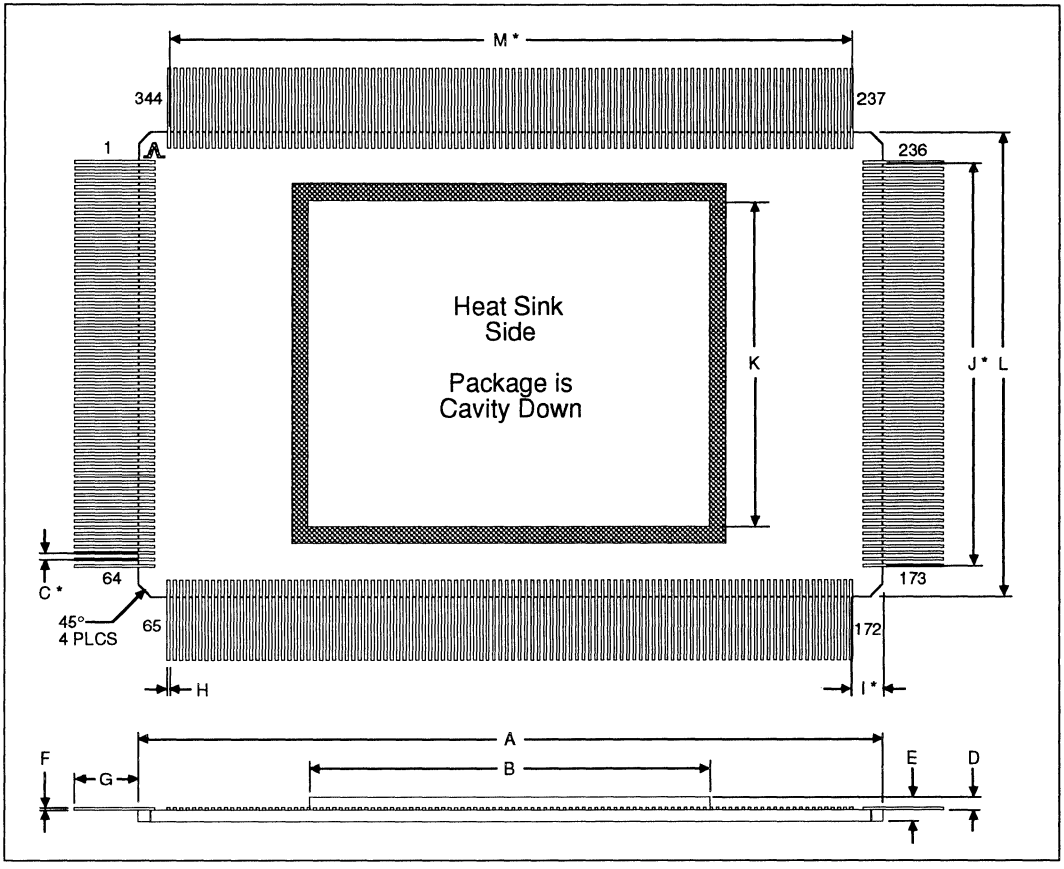
**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

344 PIN CERAMIC LDCC PIN IDENTIFICATION*

Input Only Pins	*Input/Output Pins*	*Power/GND Pins*
5-16, 19-31, 34-46, 49-60, 177-188, 191-203, 206-218, 221-232	1, 64-68, 70-73, 75, 78-80, 82-85, 87-89, 92, 94-97, 99-102, 106-109, 111-114, 116-117, 120, 121, 123, 124, 125, 126, 128-131, 135-138, 140-143, 145, 148-150, 152-155, 157-159, 162, 164-167, 169-173, 236-240, 242-245, 247, 250-252, 254-257, 259-261, 264, 266-269, 271-274, 278-281, 283-286, 288, 289, 292, 293, 295-298, 300-303, 307-310, 312-315, 317, 320-322, 324-327, 329-331, 334, 336-	2, 3, 4, 17, 18, 32, 33, 47, 48, 61, 62, 63, 69, 74, 76, 77, 81, 86, 90, 91, 93, 98, 103, 104, 105, 110, 115, 118, 119, 122, 127, 132, 133, 134, 139, 144, 146, 147, 151, 156, 160, 161, 163, 168, 174, 175, 176, 189, 190, 204, 205, 219, 220, 233, 234, 235, 241, 246, 248, 249, 253, 258, 262, 263, 265, 270, 275, 276, 277, 282, 287, 290, 291, 294, 299, 304, 305, 306, 311, 316, 318, 319, 323, 328, 332, 333, 335, 340

**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

344 PIN CERAMIC LDCC PACKAGE

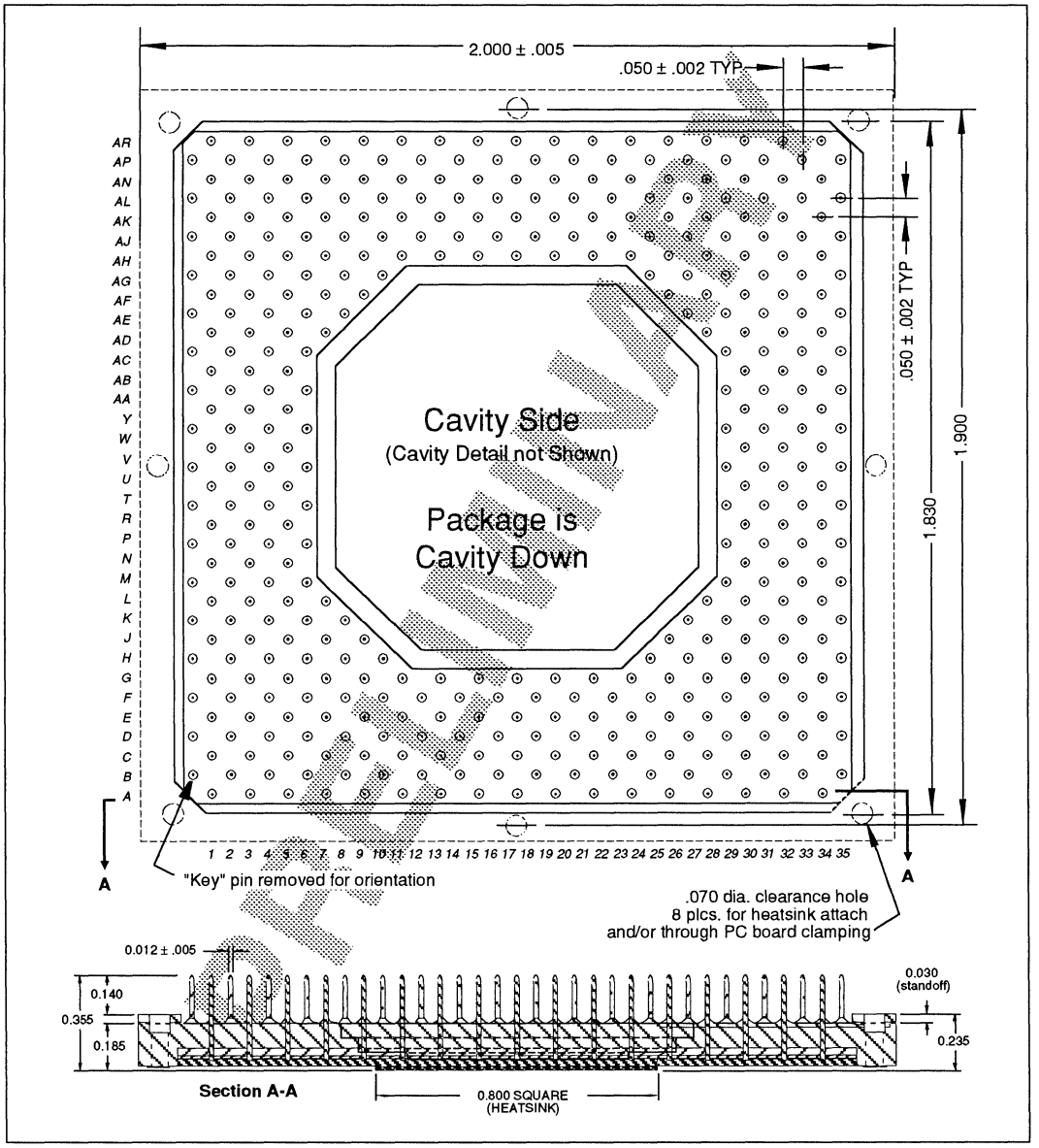


Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	58.93/59.94	2.320/2.340	H	0.15/0.25	0.006/0.010
B	35.54 TYP	TYP 1.36 SQ	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.08 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59 SQ	1.440/1.480
F	0.09/0.216	0.004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300			

** At package body*

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

415 PIN PLASTIC PGA PACKAGE



NOTES: *1) Drawing not to scale.*
2) All dimensions are nominal and in inches unless otherwise stated.
3) All non-toleranced dimensions are shown at nominal.
4) Plastic portion is RTP 1400 Ar15 Kevlar filled Polyethersulphone, black. Pins are Phos-Bronze, plated Ni/Au. Substrate is multilayer polymer/glass and copper.

415 PIN PLASTIC PGA PIN IDENTIFICATION*

Input Only Pins	*Input/Output Pins*	*Power/GND Pins*
A10, A14, A16, A18, A20, A22, A26, A28, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B35, C2, C8, C12, C14, C18, C22, C24, C34, D17, D19, D23, D33, E4, E18, E32, F5, F15, F21, F31, G8, H7, H29, J10, AG26, AH29, AJ28, AK15, AK21, AK31, AL18, AL32, AM13, AM17, AM19, AN12, AN14, AN18, AN22, AN24, AN28, AN34, AP9, AP11, AP13, AP15, AP17, AP19, AP21, AP23, AP25, AP27, AR8, AR10, AR14, AR16, AR18, AR20, AR22, AR26	A6, A8, A30, B3, B5, B31, B33, C4, C6, C28, C30, C32, D3, D7, D11, D13, D25, D29, E2, E6, E8, E10, E26, E28, E30, E34, F1, F3, F7, F11, F25, F29, F33, F35, G4, G10, G26, G28, G32, H1, H3, H9, H27, H33, H35, J2, J4, J6, J26, J30, J32, J34, K1, K5, K7, K29, K31, K35, L2, L4, L32, L34, M3, M33, N2, N4, N6, N30, N32, N34, P1, R2, R4, R32, R34, T1, T3, T33, T35, U2, U4, U6, U30, U32, U34, W2, W4, W6, W30, W32, W34, Y1, Y3, Y33, Y35, AA2, AA4, AA32, AA34, AB1, AB35, AC2, AC4, AC6, AC30, AC32, AC34, AD3, AD33, AE2, AE4, AE32, AE34, AF1, AF5, AF7, AF29, AF31, AF35, AG10, AG2, AG4, AG6, AG30, AG32, AG34, AH1, AH3, AH9, AH27, AH33, AH35, AJ10, AJ26, AJ32, AJ4, AJ8, AK1, AK3, AK7, AK11, AK25, AK29, AK33, AK35, AL2, AL6, AL8, AL10, AL26, AL28, AL30, AL34, AM7, AM11, AM23, AM25, AM29, AM33, AN30, AN32, AN4, AN6, AN8, AP3, AP5, AP31, AP33, AR6, AR28, AR30	A2, A4, A12, A24, A32, A34, B7, B29, C10, C16, C20, C26, D1, D5, D9, D15, D21, D27, D31, D35, E12, E14, E16, E20, E22, E24, F9, F13, F17, F19, F23, F27, G2, G6, G12, G14, G16, G18, G20, G22, G24, G30, G34, H5, H11, H25, H31, J8, J28, K3, K9, K27, K33, L6, L8, L28, L30, M1, M5, M7, M29, M31, M35, P3, P5, P7, P29, P31, P33, R6, R30, T5, T7, T29, T31, V1, V3, V5, V7, V29, V31, V33, V35, Y5, Y7, Y29, Y31, AA6, AA30, AB3, AB5, AB7, AB29, AB31, AB33, AD1, AD5, AD7, AD29, AD31, AD35, AE6, AE8, AE28, AE30, AF3, AF9, AF27, AF33, AG8, AG28, AH5, AH11, AH25, AH31, AJ2, AJ6, AJ12, AJ14, AJ16, AJ18, AJ20, AJ22, AJ24, AJ30, AJ34, AK9, AK13, AK17, AK19, AK23, AK27, AL12, AL14, AL16, AL20, AL22, AL24, AM1, AM5, AM9, AM15, AM21, AM27, AM31, AM35, AN10, AN16, AN20, AN26, AP7, AP29, AP35, AR2, AR4, AR12, AR24, AR32, AR34

**For comprehensive pin identification, refer to the appropriate Vitesse gate array design manual.*

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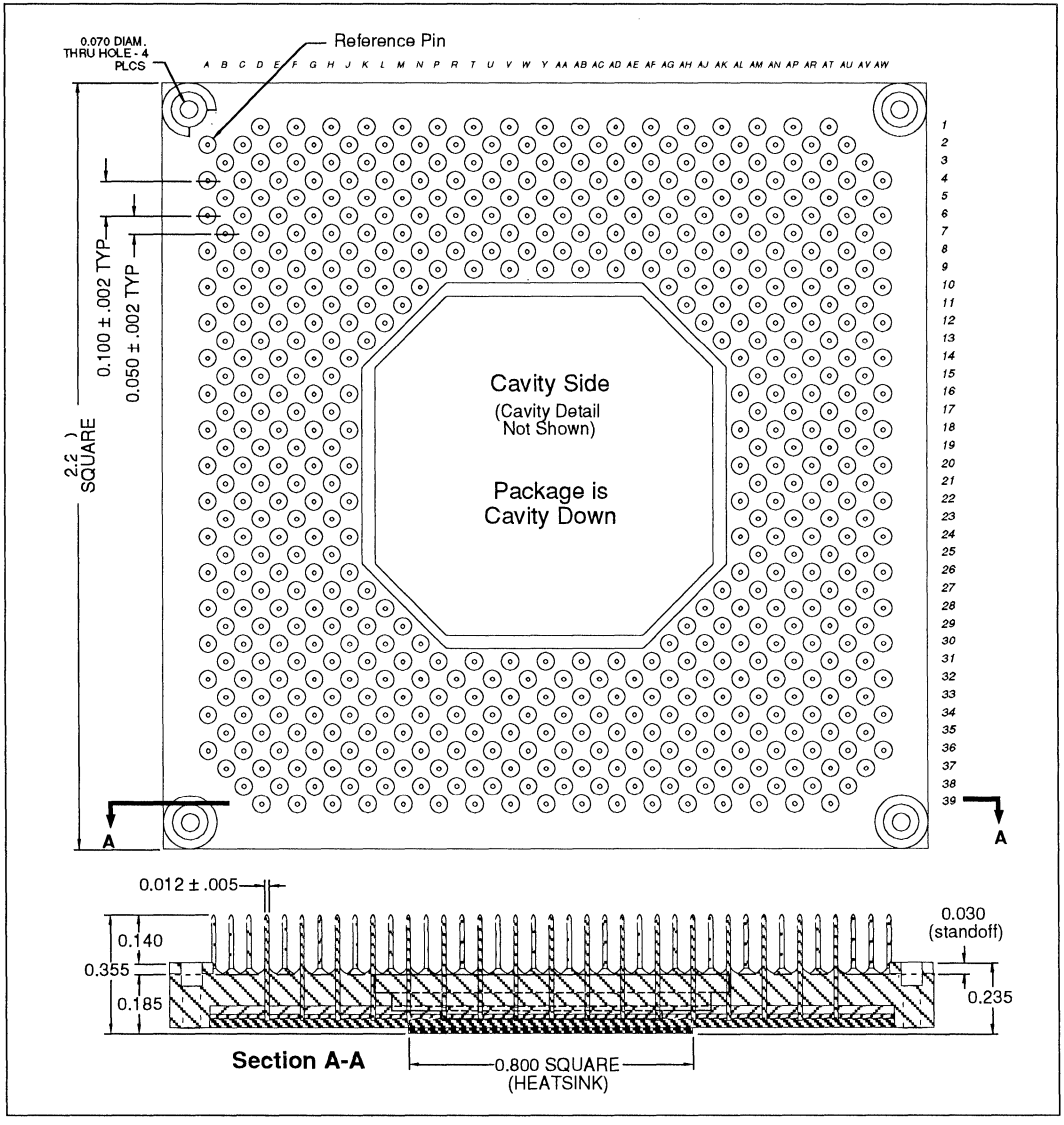
557 PIN PLASTIC PGA PACKAGE



NOTES: *1) Drawing not to scale.*
2) All dimensions are nominal and in inches unless otherwise stated.
3) All non-toleranced dimensions are shown at nominal.
4) Plastic portion is RTP 1400 Ar15 Kevlar filled Polyethersulphone, black. Pins are Phos-Bronze, plated Ni/Au. Substrate is multilayer polymer/glass and copper.

INTRODUCTION

Several important considerations must be taken into account when high speed GaAs (or ECL) ICs are interconnected on printed circuit boards. Chief among them is the need to properly terminate signal trace interconnections and the maintenance of low impedance ground and power supply connections.

This application note reviews some of the popular design techniques which are utilized to insure the integrity of high frequency signals on a printed circuit board. While these techniques have been used in ECL systems for some time, they may not be familiar to designers accustomed to CMOS circuits.

In general, signal traces on circuit boards should be treated as transmission lines if the propagation delay of the trace is more than one-tenth of the rise time of the signal. In the event that the propagation delay of the trace is short with respect to the rise time of the signal, any reflections caused by unterminated transmission lines are masked during the relatively slow transition and are not seen as overshoot or ringing.

Because most CMOS circuits have a high ratio of signal rise time to trace propagation delay, several inches of unterminated signal trace can be used without signal distortion. Since edge speeds in GaAs components are faster, the trace lengths must be considered as transmission lines and must be terminated properly to retain signal integrity.

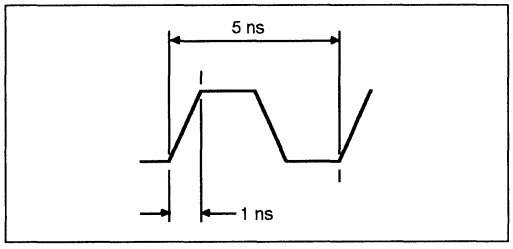


Figure 1: 200 MHz Signal

WHY ARE PROPERLY TERMINATED TRANSMISSION LINES NEEDED?

Rapidly changing signals require fast edge rates. A 200 MHz 50% duty cycle clock signal, for example, has a total period of 5ns. This period must accomodate a rise time, a fall time and some pulse width duration. As seen in Figure 1, this signal can result in rise and fall times of approximately 1ns because of the desire to maintain the pulse signal integrity. Since GaAs circuits are designed to support signal rates beyond 200 MHz, both ECL compatible and 'native' GaAs compatible output drivers are designed for sub-nanosecond rise and

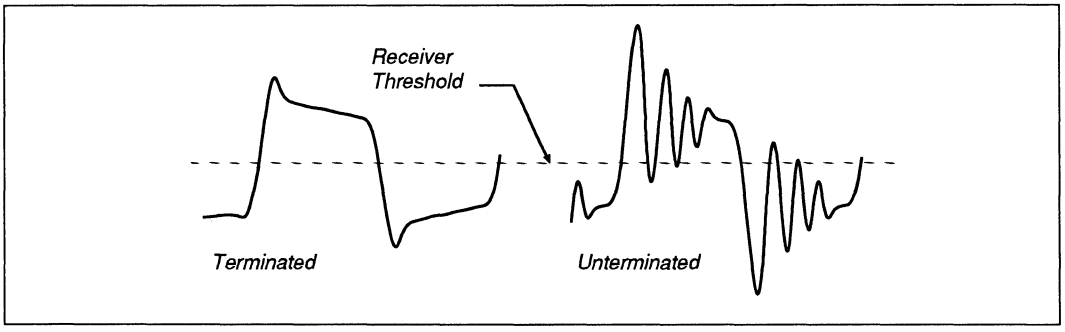


Figure 2: Signals at Terminated and Unterminated Signal Traces

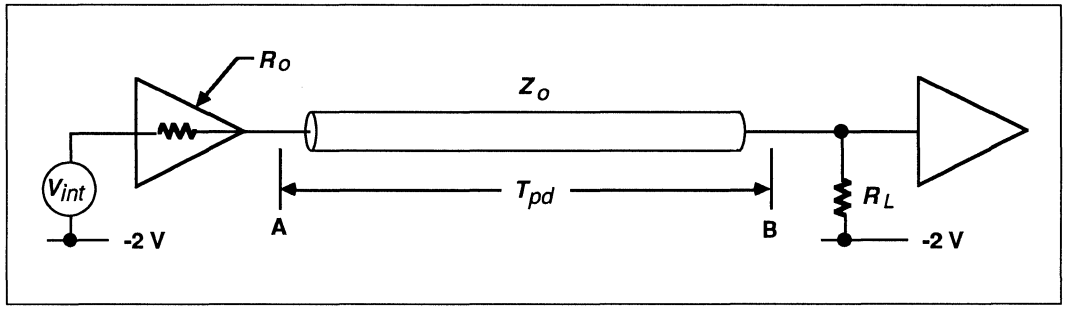


Figure 3: Parallel Terminated Line Model

fall times.

Such fast rise and fall time signals require that board signal traces are terminated transmission lines. Anytime that the propagation delay of a signal trace is longer than one-tenth the rise or fall time of the signal, an unterminated trace will result in voltage reflections which can cause degradations in the signal integrity.

Figure 2 shows the difference in signals observed in terminated and unterminated environments. As seen, unterminated signal lines can result in substantial overshoot and ringing which are caused by voltage reflections.

These voltage reflections can cause a ringing signal which can be interpreted as several faster signals by the receiver. Terminated transmission lines eliminate voltage reflections and therefore produce clean waveforms. Generally, signals with sub-nanosecond rise and fall times must be terminated if the signal trace length is longer than 0.5 in. This is because the propagation velocity of a typical signal trace is approximately 2ns/ft.

TRANSMISSION LINE THEORY

Transmission line theory is important to an understanding of the methods used to terminate GaAs signal lines. Figure 3 shows a signal trace with typical loads at both ends. Usually, the signal trace delay is long when compared with the signal rise or fall time and reflections will appear at their full amplitude. The output voltage swing at point A, (V_A), is given by:

$$V_A = (V_{int})\left[\frac{Z_O}{R_O + Z_O}\right]$$

where V_{int} is the internal voltage swing, R_O is the chip output impedance and Z_O is the line impedance.

Since R_O is small compared to the line impedance, the output swing is nearly the same as the internal transition. The internal swing is approximately 1.4 V and the typical output swing is 1.3 V. The signal propagates down the line and is seen at point B some time, T_{pd}, later. The voltage reflection coefficient at the load end of the line, *rc*, is a function of the line characteristic impedance and the load impedance and is given by:

$$rc = \frac{(R_L - Z_O)}{(R_L + Z_O)}$$

where R_L is the termination load resistance and Z_O is the line impedance (both in ohms). If $R_L = Z_O$, there is no reflection. For any value of R_L close to Z_O, the reflection is small.

PRACTICAL TRANSMISSION LINES

The key to maintaining signal integrity in practical high frequency digital systems is the utilization of properly terminated, controlled impedance transmission lines. Controlled impedance transmission lines can be realized in several ways.

For signal transmission over long distances, coaxial cables or twisted pairs are popular. Some common types of coaxial cable have characteristic impedances of 50, 75, 93 or 125 ohms. Twisted pairs can be made from AWG 24-28 hook-up wire twisted about 30 turns per foot. Such twisted pairs have a characteristic impedance of about 110 ohms.

For signal transmission within a circuit board, Striplines and Microstrip lines are usually used. A Microstrip line is shown in Figure 4. It is constructed with a strip conductor for the signal line separated from a ground plane by a dielectric. The signal line is made by etching away the unwanted copper using photoresist techniques. If the thickness, width of the line, and the distance from the ground plane are controlled, the line will exhibit a predictable characteristic impedance that can be controlled to within 5%. The characteristic impedance, Z_0, of a Microstrip Line can be approximated by:

$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

where e_r is the relative dielectric constant of the board material (which is typically 5 for FR-4 fiberglass epoxy boards), and w, h and t are the dimensions indicated in Figure 4 in inches.

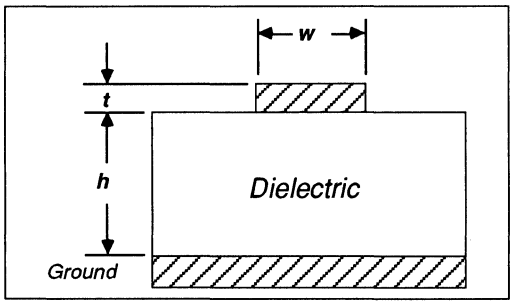


Figure 4: Microstrip

The propagation delay of the line may be approximated by:

$$T_{pd} = 1.017\sqrt{0.475\,e_r + 0.67}\ ns/ft$$

Note that the propagation delay of the line is dependent only on the dielectric constant and is not a function of line width or spacing. For FR-4 fiberglass epoxy boards, the propagation delay of the Microstrip line is approximately 1.8 ns/ft.

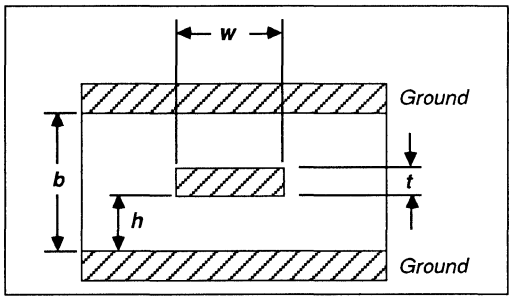


Figure 5: Stripline

A Stripline is shown in Figure 5. It consists of a copper ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the dielectric constant medium, and the distance between the ground planes are all controlled, the line will exhibit a characteristic impedance that can be held constant within 5%. The characteristic impedance of a Strip Line is given by:

$$Z_0 = \frac{60}{\sqrt{e_r}} \ln\left[\frac{4b}{0.67\pi w\,(0.8 + t/w)}\right]$$

where e_r is the relative dielectric constant of the medium and b, t, and w are the dimensions shown in Figure 3. This equation proves accurate for:

$$\frac{w}{(b - t)} < 0.35 \text{ and } \frac{t}{b} < 0.25$$

and the propagation delay of the line is:

$$t_{pd} = 1.017\sqrt{e_r}\ ns/ft$$

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For FR-4 fiber-glass epoxy, the propagation delay of the Stripline is about 2.27 ns/ft. Note that in both Striplines and Microstrip, the propagation delay is not a function of the width or spacing.

PARALLEL TERMINATED LINES

Parallel terminated lines such as the one shown in Figure 3 are used for fastest circuit performance. Standard output drivers on Vitesse's GaAs products can drive 50 ohm lines. ASIC products also allow for up to 25 ohm drive capability. In each case the term "line" refers to a signal transmission line, terminated at the receiving end through a resistor of the characteristic line impedance to -2 Volts. With parallel terminated lines, the line termination supplies the output pull-down current for the open source-follower output FET. Thus, no other pull-down resistor is required at the output of the driving gate.

POWER DISTRIBUTION

Power distribution is an important factor in system design. The loss of noise margin dueto reduced power supply voltage or noise on the power supply lines means a reduction in the circuit tolerance to crosstalk and ringing. Points to consider for overall system operation include total circuit and termination power, voltage drops on the power busses, and noise induced on the power distribution lines by the circuits and by external sources.

Vitesse GaAs circuits are designed to interface with each other over a power supply voltage range of ± 5% from the nominal -2 Volts without a loss of noise margin. However, if two chips are at different supply voltages or on the same power supply with a voltage offset between them, there will be a predictable loss of noise margin.

The main causes of V_{TT} power supply offsets between circuits are:

- Inadequate power busses to handle the necessary current
- Separate supplies with common positive terminals at slightly different potentials
- Separate positive grounded supplies with an inadequate number of interconnection ground bus bars

Power supply requirements for Vitesse GaAs circuits must take into account the fact that a 50 ohm ECL compatible output sources about 22 mA in a logic HIGH state and no current in a logic LOW state. The 22 mA differential between the two states can produce a significant power supply current fluctuation. Such an effect should be considered when specifying the power supply.

Current fluctuations are by no means insurmountable. Brief current changes are smoothed by bypass capacitors at the power supplies. Also, the typical 50% distribution of output logic levels (e.g., HIGH and LOW states) tends to minimize current changes.

High frequency noise and ripple from the power supply should be avoided. These effects produce differences in voltage levels among sections of a system and lead to loss of noise margin. As a rule of thumb, noise can be considered "high frequency" whenever the mean wave length of the noise (in units of time) is not more than 2 times greater than the propagation delay of the longest power line. For implementations which use GaAs ICs, it is recommended that high frequency power supply noise be held to under 25 mV of total signal variation.

When multiple power supplies are used, the positive terminals should be connected together with a large bus and the output voltages maintained as equal as possible. It is desirable to keep the power supply levels within 25 mV of one another.

To achieve the requirements imposed by GaAs circuits on power supply distribution, printed circuit boards with large ground and power planes are commonly used. Power supply bypass capacitors are used on the circuit boards to handle the current transients required by the outputs.

Typically, a 1 to 10 microfarad capacitor is placed on the board at the power supply inputs and a 0.1 to 0.01 microfarad capacitor is connected between ground and -2 V on every V_{TT} package pin. RF type capacitors are recommended because of their low inductance.

INTRODUCTION

Vitesse GaAs products are designed to interface to external circuits with standard ECL and TTL signal levels. In some cases, however, slight differences exist between the signal levels produced by these compatible parts and actual silicon ECL or TTL components.

Although Vitesse components use GaAs DCFL circuitry internally, the I/O is designed to interface directly with industry standard ECL and TTL levels. In addition, the FURY Series of gate arrays, the VCB50K Standard Cells and the VS12G476 4K SRAM can send and receive signals at Vitesse's own internal GaAs levels, thus allowing one device to "talk" directly to another device with no translation delays. Figure 1 shows the model used to specify system noise margins.

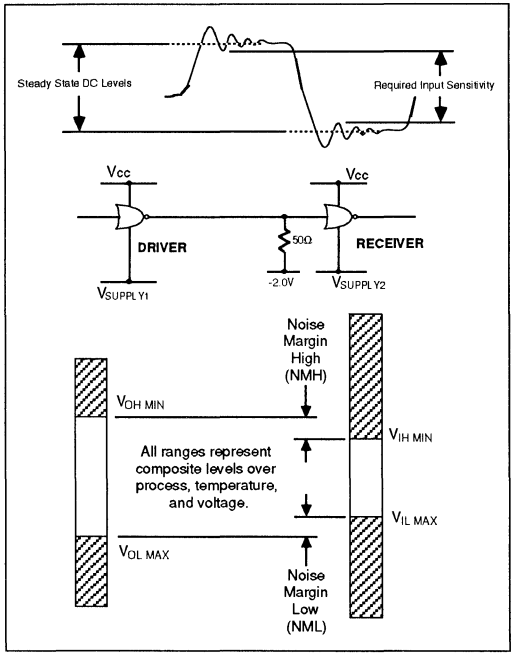

Figure 1: Noise Margin Model

ECL I/O

Industry standard ECL I/O signal levels are based on voltage levels that result naturally from the characteristics of bipolar logic families. In order to interface with standard ECL logic, Vitesse components use buffered level translators at the input and output pads. The input translator consists of a differential current switch which drives a level shifter. The reference voltage for the differential pair can be provided in one of three ways:

1. Internal Reference

This option uses the internal reference on the chip. No additional pins are required. Noise margins for this scheme are shown in Table 1.

2. External Band-Gap Diode

This option is shown in Figure 2 and involves the use of an LM185 diode in conjunction with a gate array or standard cell product. The user must connect the LM185 to the external reference pin on the GaAs device. Use of the external diode reference provides improved input noise margins (see Table 2) over a wider V_{TT} range of -2.0V ± 10%.

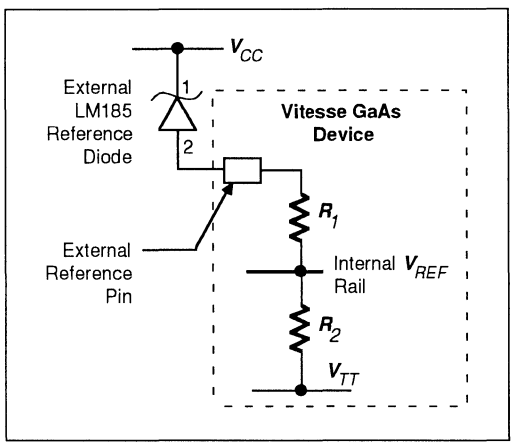

Figure 2: External Band-Gap Diode Reference

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Noise Margin	*ECL Device Driving Vitesse Device*		*Vitesse Device Driving ECL Device*	
	ECL 100K	ECL 10KH	ECL 100K	ECL 10KH
HIGH	75 mV	80 mV	145 mV	150 mV
LOW	80 mV	60 mV	145 mV	140 mV

Table 1: ECL Noise Margins Using the Internal Reference

Noise Margin	*ECL Device Driving Vitesse Device*		*Vitesse Device Driving ECL Device*	
	ECL 100K	ECL 10KH	ECL 100K	ECL 10KH
HIGH	100 mV	105 mV	145 mV	150 mV
LOW	110 mV	90 mV	145 mV	140 mV

Table 2: ECL Noise Margins Using an External Diode Reference

Noise Margin	*ECL Device Driving Vitesse Device*		*Vitesse Device Driving ECL Device*	
	ECL 100K	ECL 10KH	ECL 100K	ECL 10KH
HIGH	140 mV	145 mV	145 mV	150 mV
LOW	145 mV	125 mV	145 mV	140 mV

Table 3: ECL Noise Margins Using a Full External Reference

NOTES:
1) Worst case noise margins over nominal conditions.
2) Source for ECL 100K DC characteristics: Fairchild F100K DC Family Specifications.
3) Source for ECL 10KH DC characteristics: Motorola MECL 10KH DC Family Specifications.

3. Full External Reference

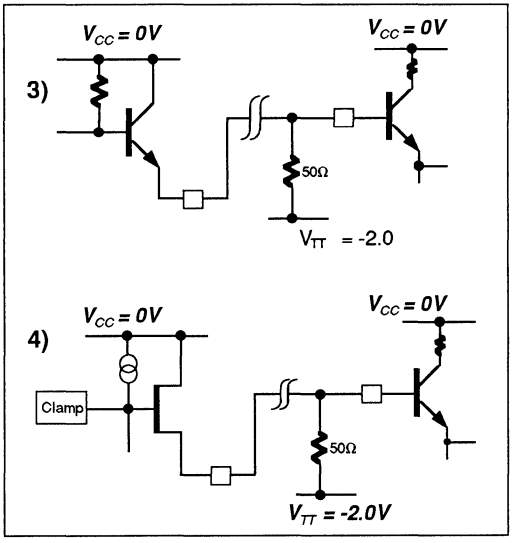
The user may provide an external reference voltage of -1.32V ± 25 mV to the external reference pin. (See table 3 for noise margins.) AN-8 discusses the creation of an external reference using the LM185.

Different but equally important issues arise when interfacing Vitesse components' output (or any "non-bipolar" ECL output) with a silicon bipolar ECL circuit input. Figures 3 & 4 illustrate this situation. In Figure 3, an ECL input is the base of an NPN bipolar transistor whose collector is connected to V_{CC} (0 Volts). In order not to degrade the switching characteristics of this input, it is essential that this input transistor be kept out of saturation, which means that the base collector diode must not become forward biased. This condition is assured when driving this input with a bipolar ECL output, since the emitter follower output cannot go more positive than one diode drop below V_{CC}.

The situation is different when the output emitter follower is replaced with a FET such as in Figure 4. Vitesse's ECL output driver incorporates clamp circuitry to ensure that the output high level does not go more positive than -700mV.

One major difference between Vitesse ECL compatible outputs and silicon ECL outputs is that Vitesse outputs are "cutoff" drivers which have an

output low voltage equal to the V_{TT} supply. In this way, a logic low is also a high impedance state and several outputs can be bussed together.



Figures 3 & 4: Bipolar & GaAs ECL outputs driving an ECL input

TTL I/O

Vitesse ASICs support TTL inputs and outputs in addition to ECL I/O. The standard minimum input swing specification at a TTL input is ≥1.2 V (0.8 - 2.0 V) compared to 310 mV for ECL. Figure 5 shows the guaranteed worst case TTL I/O levels in Vitesse components. The TTL inputs source a worst case current of -500 µA.

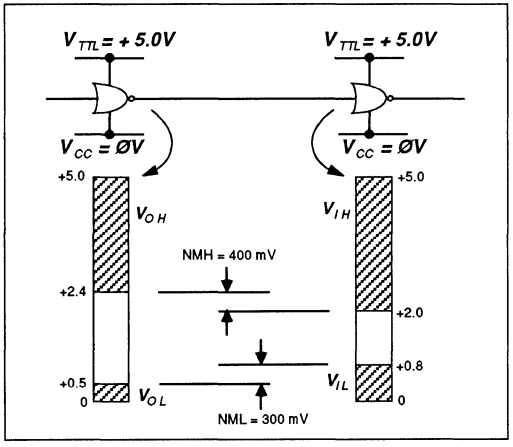
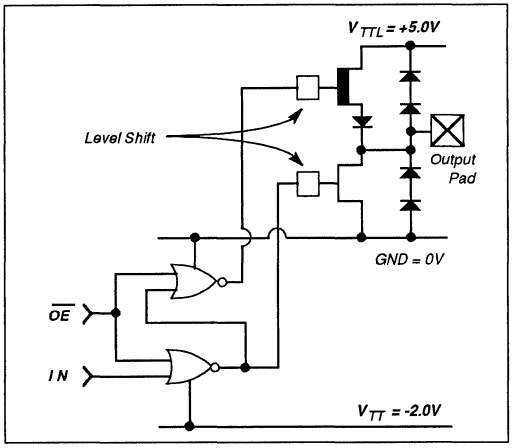


Figure 5: Worst Case TTL I/O Levels for Vitesse Products

TTL compatible outputs impose certain constraints on the user. Figure 6 is a schematic representation of the TTL output buffer with tri-state capability.



Figures 6: TTL Output Buffer Schematic

One difference between the Vitesse TTL totem-pole output and typical silicon TTL is that the high level (V_{OH}) typically goes higher in the Vitesse output. The high level can be one diode drop below V_{TTL} (+5.0 V), whereas in standard

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TTL, the output generally does not exceed 3.8 Volts. The low level (V_{OL}) is similar to standard TTL (≥ 0.4 Volts) with the rated sinking current (8 mA).

The TTL output tri-state current voltage characteristics are also different from typical silicon bipolar devices. Figure 7 shows the TTL output tri-state I-V curve. Note that the tri-state leakage current, I_{OZ}, shows a sharp increase near 3.5 Volts. This voltage is low, but well beyond the TTL valid high level of 2.4 Volts.

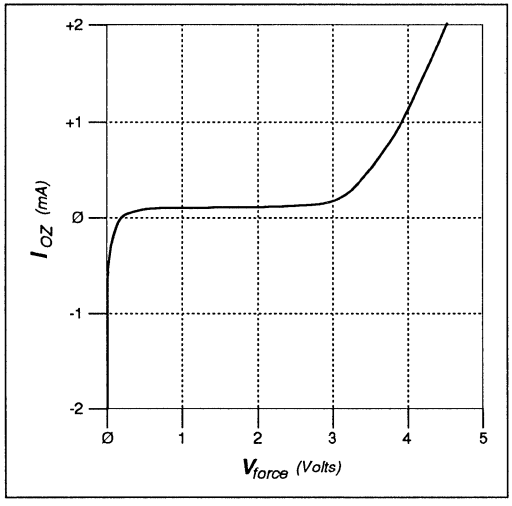

Figure 7: TTL Output Tri-State I-V Curve

In a typical system application, there may be many TTL outputs from the Vitesse component bussed together with either CMOS or TTL open collector outputs. The output high level on the bus equilibriates at an operating point (Q point) consistent with the I-V characteristics shown in Figure 7 and the current sourcing capability of the driving device.

The output edge rates in the Vitesse TTL outputs are intrinsically fast (see Figure 8). With 30 pF capacitive load, the edge rates are about 3 ns. Handling very fast edge rates on TTL circuit boards is difficult due to the severe ringing that fast edges produce. To control the ringing on the circuit board, it is helpful to buffer the TTL outputs with a silicon bus interface chip such as the 74244.

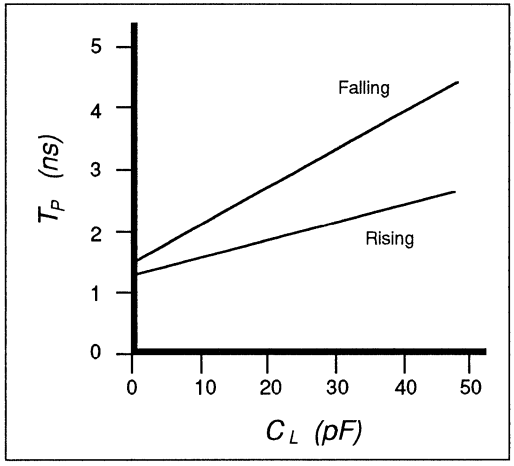

Figure 8: Capacitive Loading Effect onVitesse TTL Output Buffers

DC SPECIFICATIONS

The following tables (4-8) taken from the FURY Series Gate Array Design Manual are representative of all of Vitesse's GaAs devices. Tables 4, 5 and 6 give DC specifications for the ECL I/O cells using the internal reference, an external diode reference, or a full external reference, respectively. DC specifications for TTL I/Os are in Table 7. Following the tables are specified Recommended Operating Conditions and Absolute Maximum Ratings.

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs

NOTES: Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.

Table 4: DC Characteristics for ECL I/O Cells Using Internal Reference

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1125	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1510	mV	Guaranteed LOW for all inputs

NOTES: Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.

Table 5: DC Characteristics for ECL I/O Cells Using External Diode Reference

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1165	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1475	mV	Guaranteed LOW for all inputs

NOTES:Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.
External reference = -1.32V ± 0.025V.

Table 6: DC Characteristics for ECL I/O Cells Using Full External Reference

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Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL}	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	$V_{IN} = V_{TTL}$
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OH}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

Table 7: DC Characteristics for TTL I/O Cells (Over recommended operating conditions, TTLGND = GND)

ABSOLUTE MAXIMUM RATINGS (1)

Potential Pin to Ground, (V_{TT}) ..... -2.5V to +0.5V
Potential Pin to Ground, (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), ($V_{IN\ ECL}$) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), ($V_{IN\ TTL}$) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HIGH) ..... 50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature (3), (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.
3) Lower limit of specification is ambient temperature and upper limit is case temperature.

RECOMMENDED OPERATING CONDITIONS

ECL Supply Voltage (V_{CC}), (V_{TT}) ..... -2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +5.0V to +5%
Operating Temperature (2), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTES:1) When using internal ECL 100K reference level.
2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Application Note 4

Generation of a -2 Volt Supply From a +5 Volt Supply

DESCRIPTION

Some Vitesse ASIC products need both -2V and +5V power supplies. This application note describes a method of generating a -2V supply from a +5V supply. It is possible to generate the -2V supply from a standard +5V supply, commonly found in TTL systems, by using a switching regulator IC such as the LT1070 from Linear Technology Corp. (Milpitas, CA).

The LT1070 is a monolithic high power switching regulator which can be configured with the aid of a few external components to create a positive input - negative output Flyback Converter. The schematic below depicts a Flyback Converter configuration capable of +5V to -2V conversion. In addition to the LT1070, the circuit includes a standard LM124 op-amp from National Semiconductor Corp. (Santa Clara, CA) and a PE-65108 Transformer from Pulse Engineering (San Diego, CA). Such a circuit is capable of delivering up to 4 Amps of continuous current at -2 Volts and has line regulation of 0.05%/V.

Additional information on the LT1070 and the Output Flyback Converter configuration can be obtained from Linear Technology Corp. (408/432-1900) in their Application Note # 19.

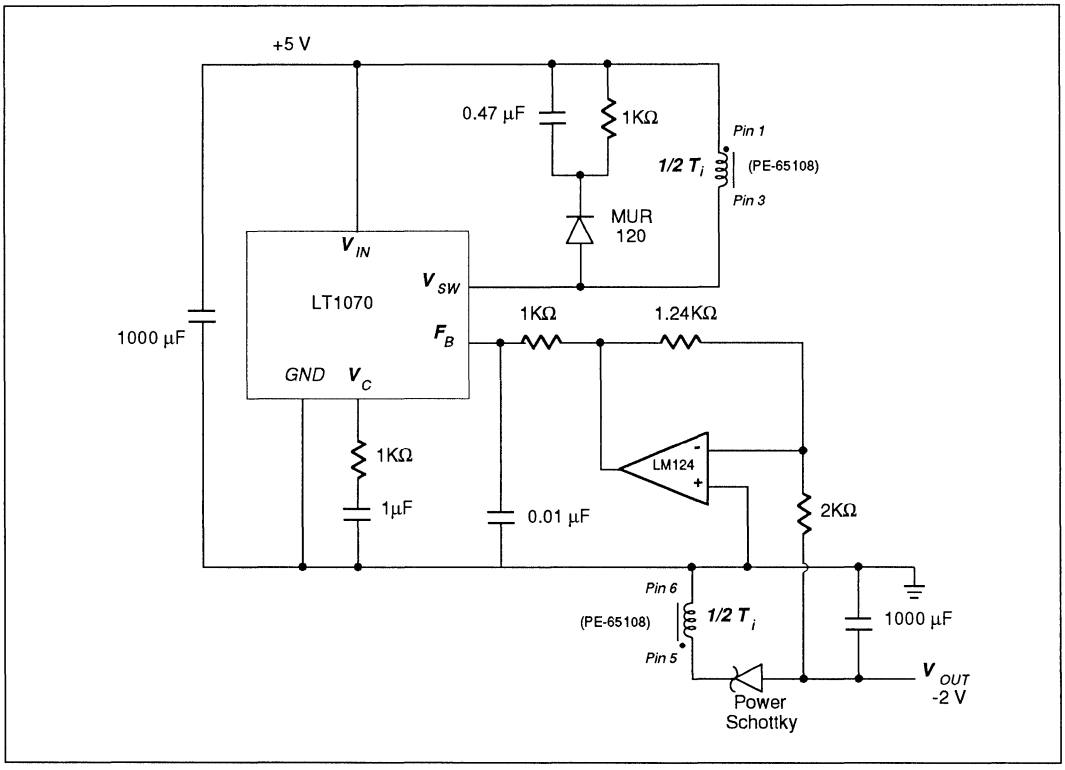

Figure 1: Flyback Converter Configuration

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INTRODUCTION

This application note describes the SONET (Synchronous Optical NETwork) transmission standard and how the VS8010 Series of ICs can be used to implement SONET. Background information is included on both SONET and the VS8010 Series. A detailed description of SONET conventions and their interface with the features of the VS8010 product family is included as well. A list of specific optical transmitters and receivers which are compatible with the VS8010 Series multiplexers and demultiplexers is also provided.

THE VS8010 SERIES

The VS8010 series of integrated circuits are a set of high speed GaAs multiplexers and demultiplexers intended for applications in optical fiber telecommunication links which are intended to comply with the Synchronous Optical NETwork (SONET) transmission standard. The series is comprised of three chips. They are: the VS8011 multiplexer, VS8012 demultiplexer and frame recovery circuit, and the VS8010 which combines the multiplexer, demultiplexer and frame recovery circuits into one monolithic entity.

These chips are the result of a collaborative research agreement between Vitesse Semiconductor Corporation and Bell Communications Research (Bellcore). Each chip represents a different personalization of the Vitesse VSC1500 gate array. The VSC1500 is an ASIC device which is optimized for multiplexer or demultiplexer applica-

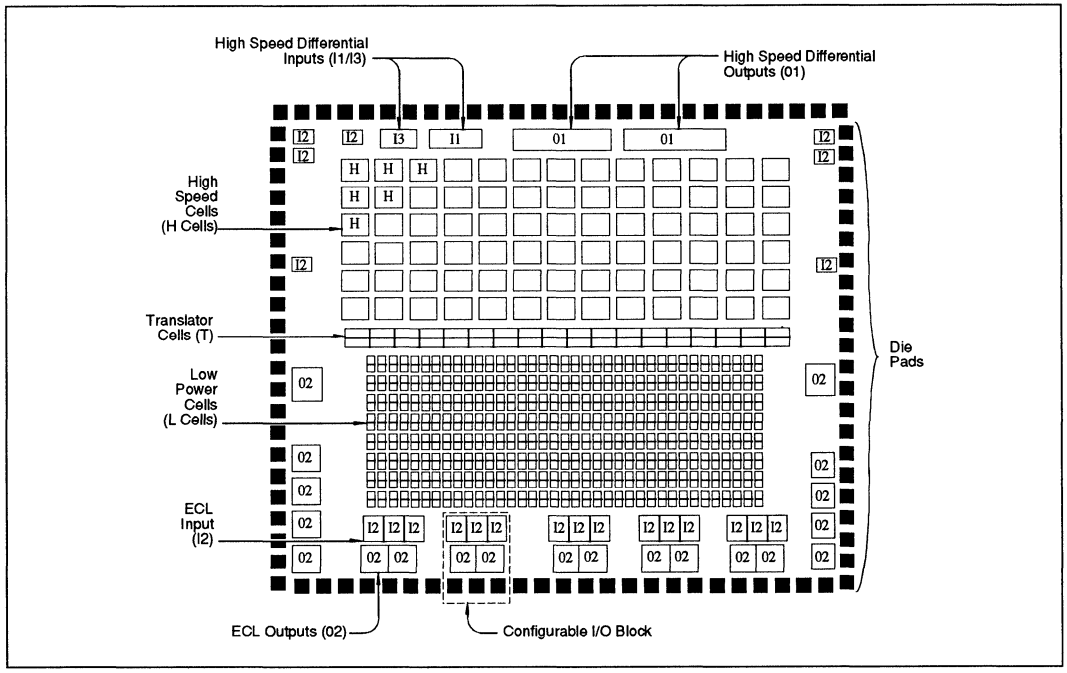

Figure 1: VSC1500 Gate Array Architecture

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tions. Figure 1 depicts the internal architecture of the VSC1520. As seen, the array is divided between two sections. The top section contains ultra high-speed cells capable of flip-flop toggle rates in excess of 2 GHz. This section is typically used for data serialization and de-serialization in communications systems applications. The lower section contains moderate speed cells capable of ultra low power dissipation. These low power cells are typically used for data processing, storage and manipulation subsequent to de-serialization or prior to serialization.

THE SONET STANDARD

The SONET transmission standard was developed by the American National Standards Institute (ANSI) and the T-1 Committee of the Exchange Carriers Standards Association. Over 200 individual contributions from more than 40 companies helped to complete the SONET specification. This effort establishes, for the first time in history, an international telecommunications protocol for digital optical transmission.

The basic SONET signal, which operates at 51.84Mbit/s, is called Synchronous Transport Signal 1 (STS-1). It is comprised of digital frames, each 125 microseconds long. Each STS-1 signal is divided into two portions, one assigned for transport overhead and another which contains the actual data to be transported. The portion of the frame containing

the data is called the Synchronous Payload Envelope (SPE). The SPE can be used to transport a variety of digital data including telecommunications DS3 signals, video data, or a number of lower rate telephone services such as DS1, DS1C or DS2 signals. The transport overhead information is used to maintain the integrity of the digital link and contains bytes associated with identifying frame boundaries, data parity, maintenance, frequency justification, orderwire, channel identification, and user specific functions. Figure 2 illustrates the STS-1 frame which is arranged into 9 rows of 90 bytes each (each row is a sequential 90 byte segment of the STS-1 frame). In each row 87 bytes are reserved for the SPE and 3 bytes are associated with transport overhead.

A primary goal of the SONET standard is to define a synchronous optical hierarchy with sufficient flexibility to carry many different capacity signals. This is accomplished by a byte interleaved multiplexing scheme which results in a family of standard rates and formats which are integer multiples of the basic STS-1 rate of 51.84Mbit/s. Since some signals which need to be transported are greater than the basic rate (such as broadband ISDN) a technique of linking several basic signals together to build a transport signal of varying capacity has also been defined. In general, however, higher rate SONET signals are created by interleaving bytes of lower rate SONET signals and modifying the appropriate layer of transport overhead.

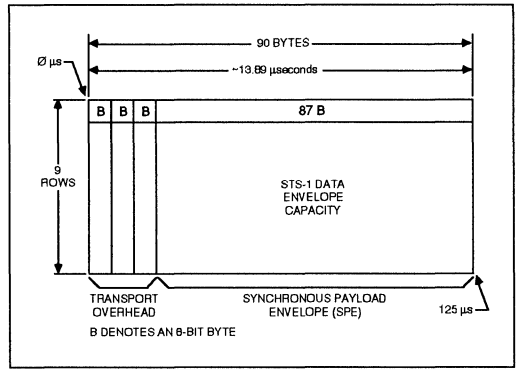

Figure 2: STS-1 Frame

The SONET standard only recognizes certain whole number multiples of the basic STS-1 signal as valid higher rate signals. The multiplier values allowed are 1, 3, 9, 12, 18, 24, 36, and 48. Table 1 lists the standard rates and corresponding STS levels which are permissible. The rates which have gained the greatest popularity in the telecommunications community are STS-1, STS-3, STS-

12, STS-24 and STS-48. In addition to providing overhead functions, the SONET standard facilitates clock recovery in a digital link by requiring that all bytes in a SONET signal be scrambled by a frame synchronous scrambler of a sequence length of 127 and a generating poynomial of $1+x^6+x^7$. Certain overhead bytes such as the ones identifying frame boundaries are exempt from this requirement. The scrambling operation causes the data to be exclusive OR'ed with a pseudo random bit sequence (127 bits long) and thereby provide data transitions in the transmitted signal. These transitions are utilized by clock recovery circuits to extract the clock from the data stream in the receiver. Scrambling is necessary because transition-poor data (all 1's or 0's for example) could cause the clock recovery circuits difficulty in performing their function.

Additional information on the details of the SONET standard can be found in ANSI document T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification".

USING THE VS8010, VS8011, AND VS8012

As seen from the previous description, the SONET standard imposes an array of fairly complex requirements on a compliant system. Most of SONET's requirements for composing the basic STS-1 frames can be accomodated in pedestrian CMOS technology because of the relatively low data rates involved. The business of interleaving these basic signals to form the high speed STS-3 to STS-24 frames is much more challenging because it involves the use of a circuit technology which can handle the 155 Mbits/s to 1.24 Gbits/s data rates required.

In order to maximize the utility of GaAs technology to the user while minimizing overall system power dissipation, the VS8010 series ICs implement only those functions which necessitate data manipulation at the fast line rate. These functions are bit serialization and de-serialization, and SONET frame recognition and byte alignment. Most other required functions (byte interleaving, overhead byte alteration, data scrambling, etc.) can be accomplished at speeds lower than the line rate, and are more appropriately delegated to an external, low power, gate array. Data scrambling, for example, can quite easily be accomplished at the byte rate with the circuit shown in Figure 3. In this parallel scrambler, D1 is assumed to be transmitted first and D8 is assumed to be transmitted last. When ENABLE is LOW the scrambler is off and inputs are equal to outputs. In addition, S1N to S7N are in the state which is the correct initial 8-bit scramble sequence according to the SONET specification. When ENABLE is HIGH the resulting output is a scrambled version of the input and is ready for bit serialization via the VS8010 or VS8011 as appropriate to the application.

STS Level	Line Rate (Mbit/s)
STS-1	51.840
STS-3	155.520
STS-9	466.560
STS-12	622.080
STS-18	933.120
STS-24	1244.160
STS-36	1866.240
STS-48	2488.320

Table 1: Standard SONET Line Rates

For line rates up to STS-3 the external gate array used to implement functions not provided on the VS8010 can be a CMOS device. For line rates between STS-12 and STS-24 Vitesse offers the FURY or LP Series of gate arrays which feature

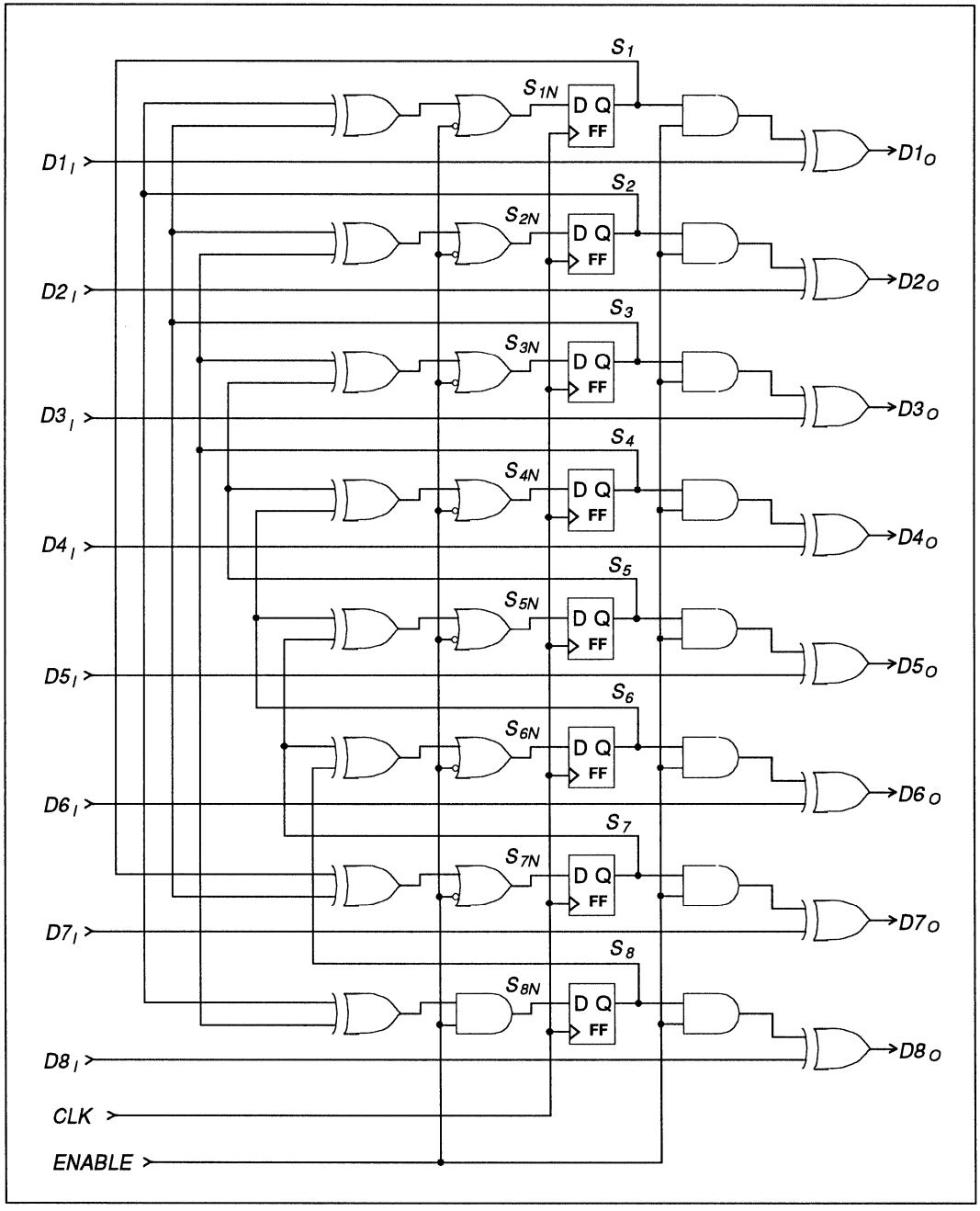

Figure 3: SONET Parallel Scrambler

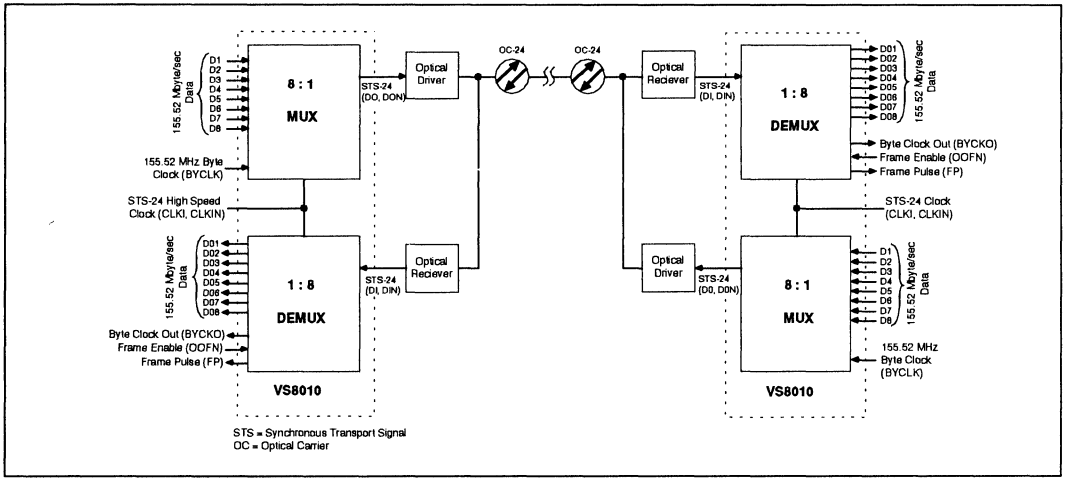

Figure 4: SONET Section Level Node (STS-24 Line Rate)

ultra low power dissipation and the ability to interface both with the VS8010 series chips via ECL logic levels and to slower systems utilizing TTL logic levels. These lower power devices can be used since the VS8010 series ICs are capable of reducing the effective data rate by a factor of eight.

In applications where the multiplexer and demultiplexer are co-located (such as a SONET section level node) the VS8010 chip can be used to realize the complete transceiver function. Figure 4 shows a block diagram of a SONET Add-Drop MUX capable of STS-24 rates. In the event that the multiplexer and demultiplexer functions are not located on the same printed circuit board, a more appropriate configuration would use the VS8011 for the multiplexing function and the VS8012 for the demultiplexing function. The power dissipation of these individual chips is approximately half of the power dissipation of the VS8010 which combines both functions.

FRAME RECOVERY

The primary capability of the VS8010 series ICs which makes them appropriate for SONET

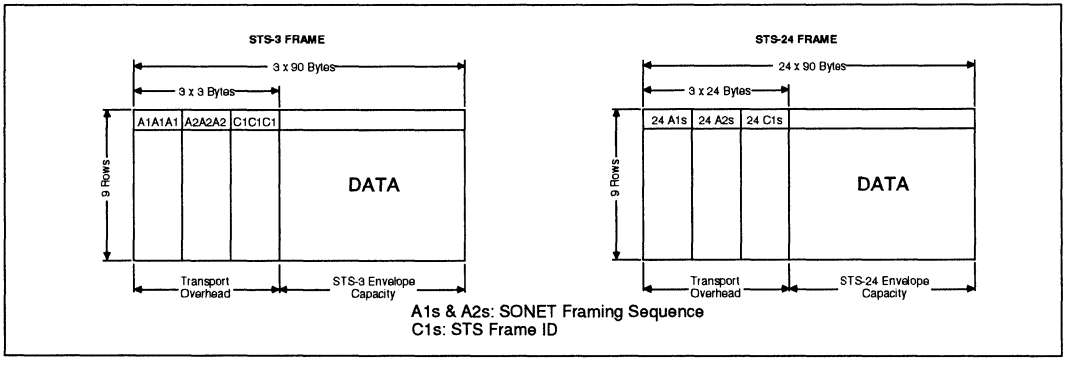

Figure 5: STS-3 and STS-24 Frames

applications is their ability to detect the boundary of SONET frames from the framing overhead bytes and to align the subsequently demultiplexed information to the frame boundary. This operation is difficult to implement after information has been demultiplexed and generally requires circuits which operate at the transmission line rate. Since SONET protocol insists on byte wide multiplexing to form higher rate signals, the relative location of overhead information is maintained in any SONET frame. Figure 5 depicts both an STS-3 and an STS-24 frame. Although both frames are 125 microseconds long, the amount of information in the STS-24 frame is much greater due to the higher (1.24 GHz) data rate. Note that in all cases a SONET frame begins with a framing sequence. The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes (A1 = 11110110 and A2 = 00101000). Table 2 shows the number of A1 and A2 bytes in each SONET frame for different line rates.

STS Level	Line Rate (Mbit/s)	# of A1 Bytes	# of A2 Bytes
STS-3	155.520	3	3
STS-9	466.560	9	9
STS-12	622.080	12	12
STS-18	933.120	18	18
STS-24	1244.160	24	24
STS-48	2488.320	48	48

Table 2: A1 and A2 Bytes in SONET Frame

Figure 6 shows the functional block diagrams for the VS8010, VS8011 and VS8012 chips. The frame recovery circuits in the VS8010 and VS8012 are enabled on the falling edge of the OOFN input. Once enabled, the frame recovery circuits start looking for the SONET framing sequence. The VS8010 and VS8012 recovery circuits operate from STS-3 to STS-24. The frame recovery circuits look for 3 A1s followed by 3 A2s. The byte clock (BYCKO) and parallel byte data output (DO1-DO8) become invalid on the falling edge of OOFN and become valid when A1 changes to A2. The frame recovery circuits align the received serial data on byte boundaries for demultiplexing by controlling the timing generator. The byte boundary alignment is based on the specific A1 and A2 byte recognition. The falling edge of OOFN must occur at least 4 byte clock periods before A1 changes to A2. The pulse width of OOFN must be at least 1 byte clock period.

The SONET frame detector monitors the incoming data stream. If 3 A1 bytes followed by 3 A2 bytes are detected, a frame confirmation signal is sent off-chip on the output called FP. The rising edge of the FP pulse occurs 2 byte clock periods after A1 changes to A2 on the demultiplexer parallel data outputs. The FP pulse width is one byte clock period. The frame detection circuitry also disables the frame recovery circuits once 3 A1s are

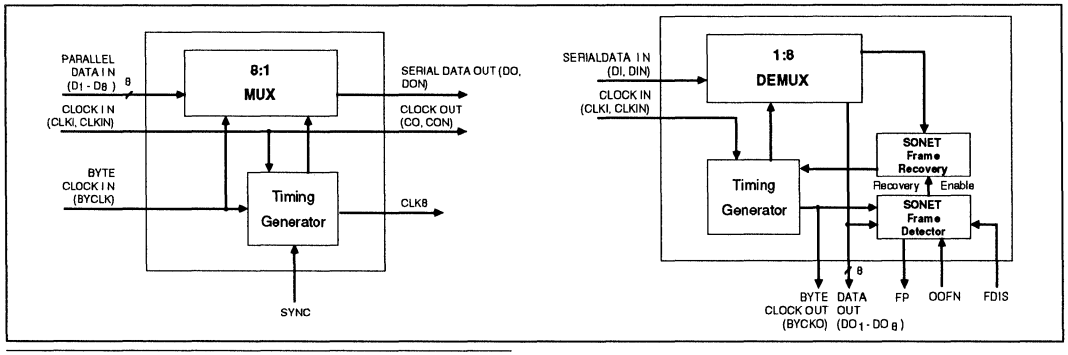

Figure 6: a) 8:1 Multiplexer and **b)** 1:8 Demultiplexer

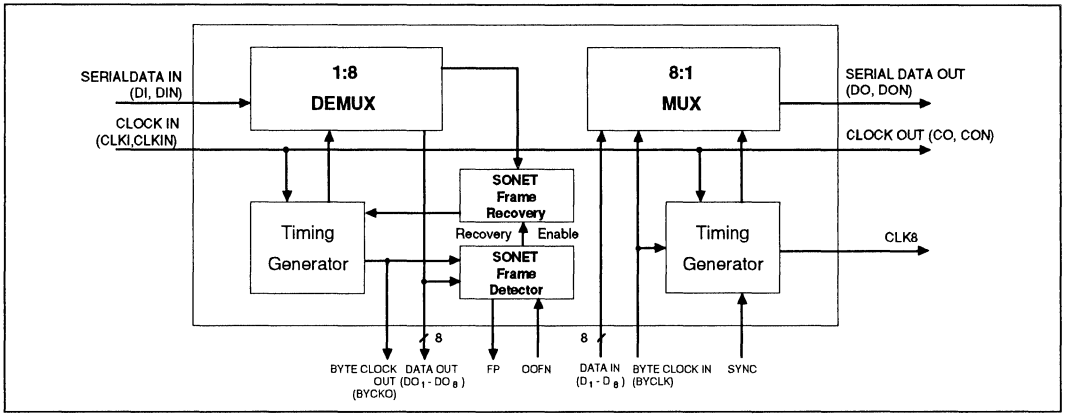

Figure 7: VS8010 - 8 Bit Mux/Demux with SONET Frame Recovery

followed by 3 A2s. This is done to avoid a false FP signal in the unlikely event that the data payload contains data which is identical to the framing sequence. It is the systems responsibility to reactivate the frame detector every 125 microseconds (the length of a SONET frame). Once the frame is aligned, the FP pulse is generated on every SONET frame. If for any reason the FP pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the OOFN input (HIGH to LOW) to recover the system back to a synchronized condition. If the FP pulse does not start up again a link failure may have occurred. Figure 7 shows the timing relationships between important signals in the demultiplexing and frame recovery operation.

INTERFACES

Most inputs and outputs on the VS8010 series chips are fully compatible with ECL circuits. Exceptions to this general rule are the very high speed inputs and outputs assigned to receiving and transmitting serial data and high speed line-rate clock. These interfaces are capable of accepting or transmitting data at rates in excess of 1.5 GHz. Since ECL circuits are not capable of speeds of such magnitude, the high speed I/O of the VS8010 series interfaces with AC coupled signals which could be generated by oscillators or high speed optical receivers/transmitters.

In a typical application the high speed clock (CLKIN) and data (DIN) inputs have an external chip capacitor connected in series between the input and the terminated transmission line carrying the high speed signal. Internal circuitry is responsible for level shifting the AC coupled signal to the appropriate DC levels needed for internal operation. The AC coupled signals should have peak-to-peak amplitudes between 800mV and 1.2V. The DC levels required at these high speed inputs, in the event of DC coupling, are shown in Table 3.

High speed outputs CO, CON and DO, DON on the VS8010 and VS8011 deviate slightly from standard ECL levels. The guaranteed signal levels are also shown in table 3. Note that the peak-to-peak amplitude of these signals is between 620mV and 1.3V.

SUPPORT CIRCUITS

In the design of an actual SONET compliant digital optical link, many additional circuits are needed to support the VS8010 series ICs. They include optical transmitters and receivers, clock recovery circuits, high speed clock generation cir-

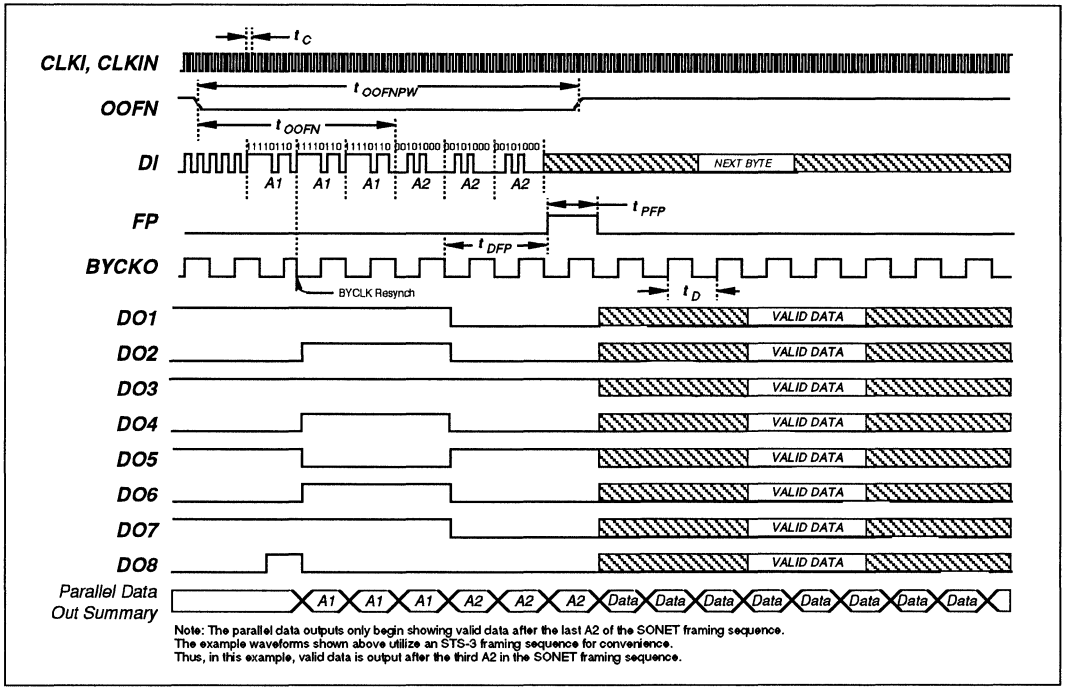

Figure 7: Timing Waveforms for Demultiplexing and Frame Recovery

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Reference level	—	-3.5	—	V	
V_{OH}	Output HIGH voltage	-1.1	—	-0.7	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	-2.0	—	-1.72	V	Output load, 50Ω to -2.0 V

NOTES:1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.
2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed outputs must be terminated identically.

Table 3: High Speed Input and Output Levels *(Over recommended operating conditions. V_{CC} = GND, output load = 50Ω to -2.0V.)*

cuits, frame formatting and byte multiplexing circuits. A list of optical transmitters and receivers which are compatible with the VS8010 family are listed below.

OPTICAL TRANSMITTERS

Company	*Model Number*	*Performance*
BT&D	XMT 1100	up to 1.4 Gb/s - 1mW output power
BT&D	XMT 1300	up to 1.4 Gb/s - 200μW output power
AT&T	ASTROTEC 1218	up to 1.0 Gb/s
Ortel	3510A	up to 3.0 Gb/s
Ortel	3510B	up to 6.0 Gb/s
TACAN	TX1250	up to 1.25 Gb/s

OPTICAL RECEIVERS

Company	*Model Number*	*Performance*
BT&D	RCV1101-50	up to 50 Mb/s
BT&D	RCV1101-150	up to 150 Mb/s
AT&T	ASTROTEC 1306A	up to 1.7 Gb/s
Ortel	3510A	up to 3.0 Gb/s
Ortel	3510B	up to 6.0 Gb/s
TACAN	RX1250	up to 1.25 Gb/s

Key to Optical Transmitter/Receiver Vendors:

Ortel Corporation
2015 West Chestnut St.
Alhambra, CA 91803

AT&T Technologies
555 Union Blvd.
Allentown, PA 18103

TACAN Corp.
2330 Faraday Ave.
Carlsbad, CA 92008

BT&D
2 Righter Parkway
Wilmington, DE 19083

INTRODUCTION

This application note describes the fundamentals of metastability as well as a method of characterizing metastable behavior. The results of the characterization are applied to a general failure rate formula to predict the reliability of data synchronizers implemented using GaAs DCFL registers.

METASTABILITY THEORY

In any system where a single flip-flop (or latch) is used to resolve the timing conflicts between two asynchronous digital circuits, this flip-flop is subject to marginal triggering behavior.[1] In recent years, this general phenomenon has been given the name "metastability". The theory and characterization of metastable behavior is of particular concern in determining the reliability (failure rate) of synchronizer circuits.

A metastable condition can occur when the setup and hold specifications of a register are violated. In Figure 1, Case 1 shows a transition of the asynchronous data which satisfies the setup time requirements of the synchronizing register. A logic "1" is therefore transferred to the register output. Case 2 in Figure 1 shows data which is stable for a sufficient period of time to satisfy the hold time requirements of the register. In Case 3, however, the asynchronous data and the clock transition concurrently, thus causing the output of the register to be indeterminate (neither a logic "1" or a logic "0") for a period of time. The amount of time required for the register output to transition from this indeterminate state to a valid logic state is commonly referred to as the "walk-out" time. The actual window of time where an indeterminate condition can occur is normally much smaller than the specified setup and hold time window for a given flip-flop.

Metastable behavior can also be perceived in terms of its effect on flip-flop delay [2]. As seen in Figure 2, the flip-flop has a normal propagation

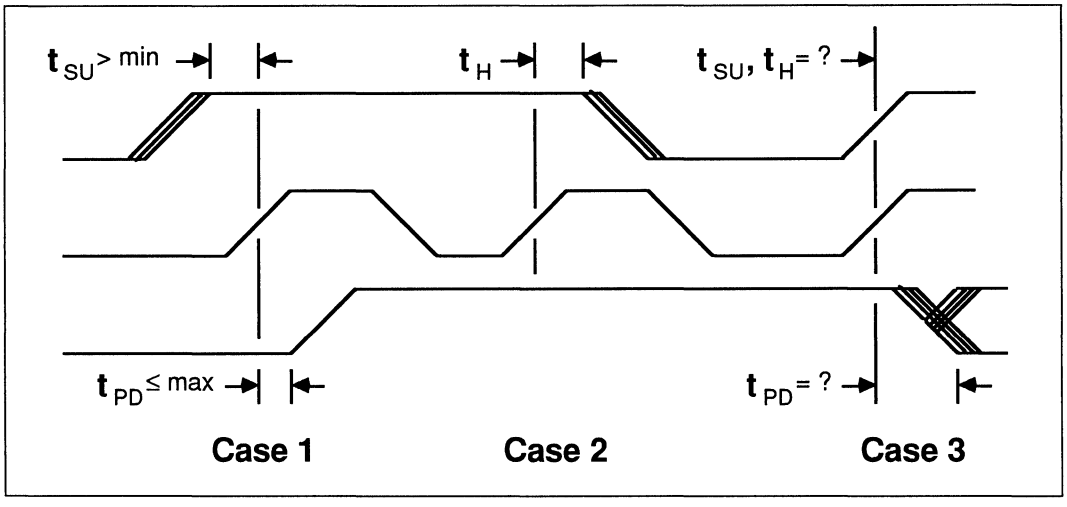

Figure 1: Data and Clock Relationships for Bi-Stable Elements

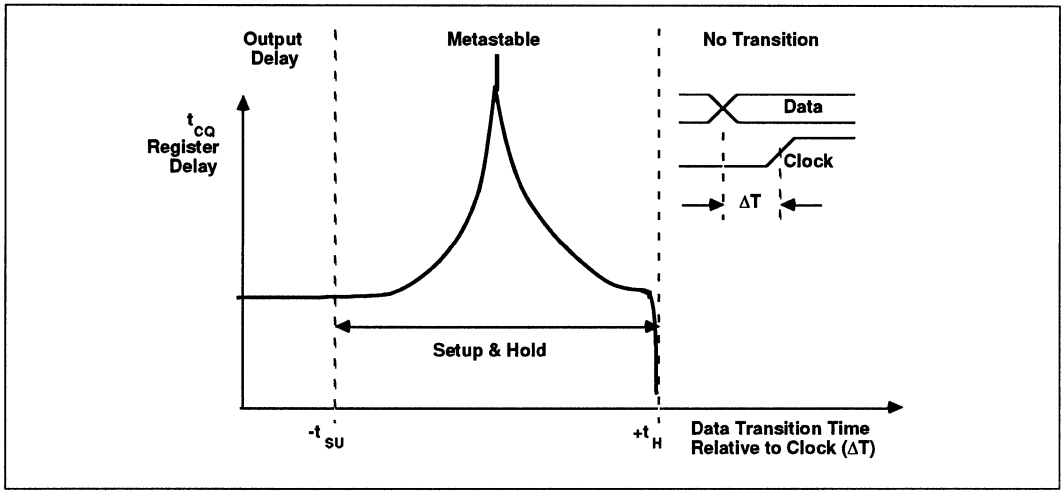

Figure 2: Metastable Delay

delay, t_{CQ}, when the setup time specification is met. As the data input transition moves closer to the clock transition, however, the delay of the flip-flop increases - reaching its maximum value when the clock and data transitions occur simultaneously. As the data input transition moves past the hold time, no output transition occurs.

Perhaps the most important concept in understanding metastable behavior is that the walk-out time is *always* a probabilistic phenomenon. A "maximum" walkout time for a given register does not exist. Rather, for a certain flip-flop there exists a relationship between a given walk-out time and the probability that this walk-out time will occur. Empirical studies have shown that the mean time between events where the synchronizer flip-flop is still unresolved at time t_w, MTBF(t_w), is: [2,3]

$$MTBF(t_w) = \frac{exp(t_w/K2)}{(K1)(f_{CLK})(f_{DATA})} \qquad (1)$$

for $t_w > h$

where:

t_w is the time the flip-flop has been allowed to resolve after the clock transition.

K1, *K2*, and *h* are parameters associated with a particular register and are functions of the circuit design and construction.

The total walk-out or indeterminate time can be viewed as two time periods: the amount of time taken for random noise to "push" the output just outside of the metastable state (T_M), and the recovery time (T_R) from time T_M until a valid logic state is achieved.

METASTABILITY CHARACTERIZATION

Metastable behavior can be observed using many different methods. Analog circuit simulators such as SPICE cannot accurately characterize metastable behavior in a bistable element unless an accurate noise model is incorporated into the simulation. Given the random and often complex origins of noise in actual circuits, accurate noise models are quite difficult to create. Metastable behavior can also be observed in the lab using fine resolution

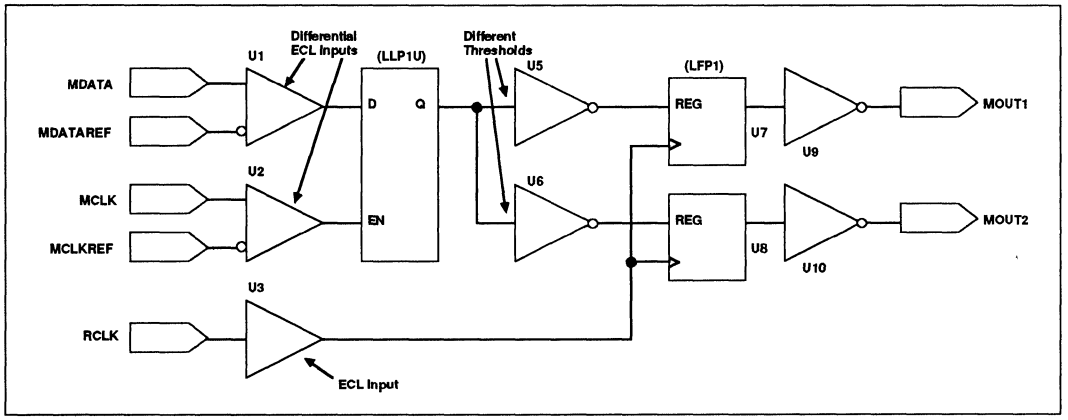

Figure 3: Metastability Circuit Schematic

delay lines to vary the relationship between clock and data until an indeterminate condition is observed using a triggered oscilloscope. Because metastability is a probabilistic phenomenon, however, it is impossible to obtain the *K1*, *K2*, and *h* constants for a given register using either of the above methods.

The most direct and accurate method of characterizing the metastable behavior of a flip-flop is to construct a synchronizer using that flip-flop and gather statistical data on that flip-flop's failure rate as a function of the settling time allowed. This characterization method readily yields the *K1*, *K2*, and *h* constants necessary to predict synchronizer failure rates. To shorten the duration of the tests, random data transitions can be confined to a small window of time surrounding the active clock transition.

TEST SETUP

In order to characterize the metastable properties of GaAs DCFL registers, a synchronizer circuit was implemented on a FURY VSC10K gate array. The circuit schematic is shown in Figure 3. In order to simplify the testing, a latch (LLP1U) was used rather than a flip-flop. The LLP1U is an unbuffered DCFL latch. The clock and data signals are brought onto the chip through differential ECL compatible inputs. The clock (enable) signal was inverted to cause the circuit to latch on a positive clock, again to simplify the test. The output of the latch drives two DCFL inverters, U5 and U6. A difference in switching thresholds between the two inverters is created by using twice the standard D-mode FET width on inverter U5 and twice the E-mode FET width on inverter U6. This threshold window is approximately 130 mV in magnitude centered around the nominal inverter threshold. When the output of the latch is in the indeterminate region, therefore, the output of U5 will be high and the output of U6 will be low. The outputs of U5 and U6 are registered using flip-flops U7 and U8 and are driven off-chip through ECL outputs U9 and U10.

The bench setup shown in Figure 4 was used to conduct the metastability testing. An EH SPG2000 4-channel pulse generator was used to provide the "raw" clock and data signals (MCLK and MDATA) to the latch as well as the RCLK signal to registers U7 and U8. In order to accurately control the relationship between the clock and data signals to the latch, the ECL differential input buffers, U1 and U2), were used as verniers. The MDATAREF signal was set to a fixed voltage to

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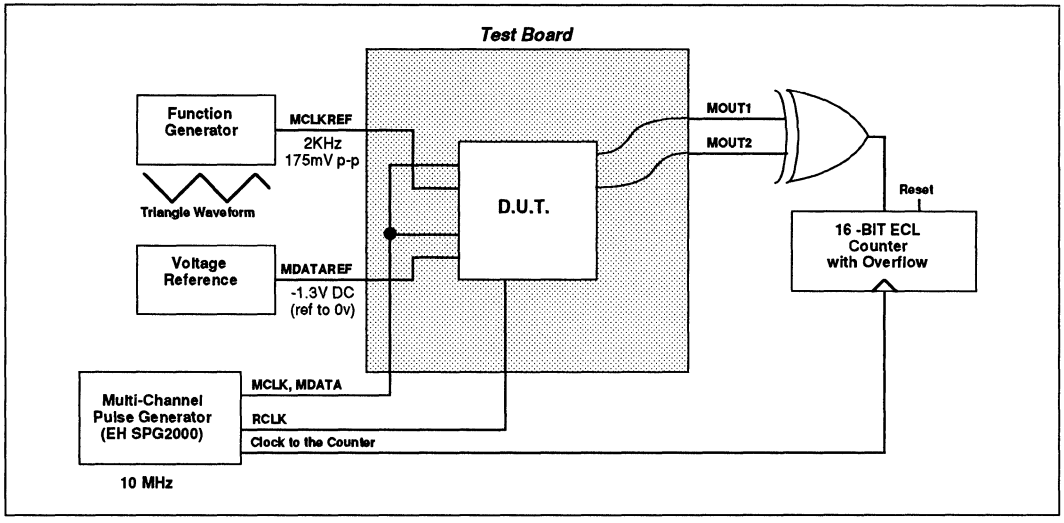

Figure 4: Metastability Bench Setup

adjust the clock and data signals so that metastable events per unit time were maximized. A triangle waveform was driven onto the MCLKREF pin in order to sweep the latch back and forth through its entire window of metastability. The size of the actual window was determined empirically to be about 15 ps. However, a 350 ps sweep window was chosen (by adjusting the amplitude of the triangle waveform) to ensure that the entire period where metastable events occurred was covered even if the MDATAREF input voltage drifted. Because the slew rate of the MCLK/MDATA signal was set to 0.5 V/ns, a peak-to-peak voltage of 175 mV was used for The register output signals, MOUT1 and MOUT2, drive an off-chip exclusive-OR which in turn drives a 16-bit ECL counter with over-flow. For a given test the walkout time, t_w, is controlled by setting the delay between the MCLK and RCLK signals. The time between trials (each trial being a latching edge on MCLK) is set by varying the internal period on the SPG2000 pulse generator. For all of the tests summarized in this document, a period of 100 ns was used which corresponds to a clock rate of 10 MHz. For each part, errors were counted over a specific period of time for various values of walkout time.

All of the testing was performed at room temperature with no air flow applied to the part. A case temperature of 52 ± 2°C was measured for these conditions. A nominal supply voltage of -2.0 Volts was applied to the device under test. Prior to the actual MTBF testing, the output of the latch was observed directly using a sampling oscilloscope to ensure that metastable conditions could be induced by the test setup.

TEST RESULTS

Figure 5 shows ln(MTBF raw) versus the walkout time. This data is an average of testing done on two devices and is considered to be typical. For both parts, the data taken fit the theoretical model described in equation (1). The value of the experimental constant, *h*, which represents the minimum value of t_w for which equation (1) holds, was not determined but appears to be less than 1 ns. Further testing is required to establish the worst case MTBF for a given walkout time. Vitesse recommends guardbanding the settling time al-

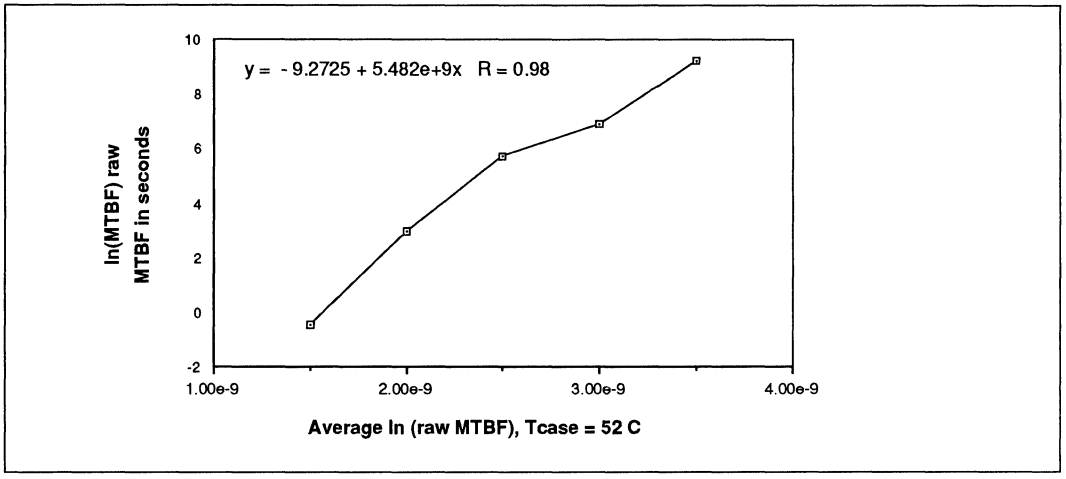

Figure 5: ln(raw MTBF) as a Function of Walkout Time

lowed by at least 1 ns to meet the typical MTBF values specified.

The values for *K1* and *K2* are derived from the experimental data using the following relationships:

$$K1 = exp(-ln((f_{CLK})(f_{DATA})) - b) \quad (2)$$

$$K2 = 1/m \quad (3)$$

where:

f_{CLK} = clock frequency to the latch (10 MHz)

f_{DATA} = effective data frequency (1.43 GHz)

m,b = the slope and y-intercept of the linear fit of ln(MTBF) vs. t_w

The effective data rate of 1.43 GHz is achieved by limiting data transitions to the 350 ps sweep window around the clock. Because only a single rising edge occurs in this window, however, the effective data period is twice the sweep window. Using the slope and y-intercept from Figure 5, the values of *K1* and *K2* are:

K1 = 7.44E-13/sec

K2 = 1.82E-10 (dimensionless)

Figure 6 charts the MTBF as a function of walkout time for a data frequency of 100 MHz and a clock frequency of 75 MHz. Data is given for both a GaAs DCFL circuit and a typical ECL register. Table 1 shows the typical MTBF for various combinations of f_{CLK}, f_{DATA}, and t_w. The user should note that these MTBF values are for a single flip-flop. In order to calculate the MTBF for a dual-stage synchronizer, the MTBF of the first stage must be calculated first. This MTBF then becomes the data rate for the next stage when calculating the cumulative MTBF of the two registers in series.

SYNCHRONIZER APPLICATIONS

Knowledge of the metastable behavior of registers in a given technology is crucial to the design of synchronizers. The VMEbus, for example, is an entirely asynchronous bus[2]. Because no timing is specified for bus arbitration signals, decision points such as the bus arbiter, the bus-

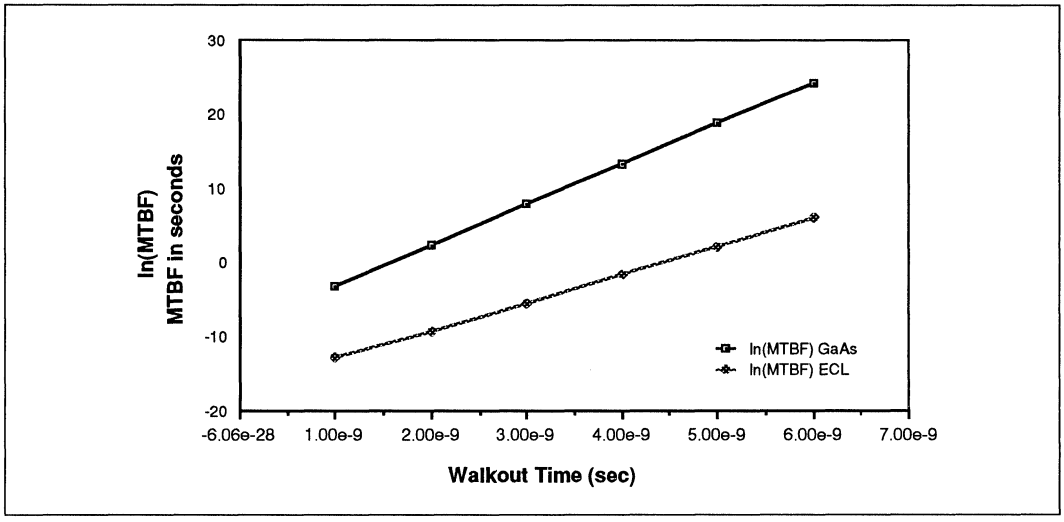

Figure 6: MTBF vs Walkout Time for GaAs and ECL

grant daisy chain, and the interrupt-acknowledge daisy chain must contain synchronizers to resolve timing conflicts. Given that the system clock rate is a known value and the frequency of events to be synchronized can be estimated for the system, the MTBF for the synchronizer can be established based on the MTBF equation for that register. For example, a dual register synchronizer clocked at 100 MHz synchronizing data at 50 MHz will exhibit a mean time between failures of approximately 90 million years, allowing 1 ns for setup time and 1 ns for guardband. If the MTBF for a given amount of settling time is tolerable, a single DCFL register can be used to synchronize random events. For a single register, 100 MHz clock, and 50 MHz data, allowing an additional 5 ns of delay yields a typical MTBF of about 7 years.

CONCLUSIONS

Compared with previously published results, initial testing indicates that GaAs DCFL registers are superior to ECL registers in terms of the mean time between failure due to metastable conditions. This result is likely attributable to the fast intrinsic delays of DCFL gates as well as the shorter feedback path inherent in DCFL latches. Past studies show that the trend is for the value of *K2* to be lower for newer and faster technologies [2]. Further testing will allow the variations in metastable behavior with respect to process to be determined. Testing over temperature and voltage variations is also scheduled although past research indicates that variations in *K1* and *K2* due to temperature and voltage are minimal compared to variations due to process [2].

f_data (Hz)	f_clk (Hz)	t_walk (seconds)	MTBF Expressed in:			
			Seconds	Hours	Days	Years
1.00E+07	2.00E+07	4.00E-08	1.15E+93	3.18E+89	1.33E+88	3.64E+85
2.50E+07	5.00E+07	1.80E-08	7.69E+39	2.14E+36	8.99E+35	2.44E+32
5.00E+07	1.00E+08	8.00E-09	2.99E+15	8.31E+11	3.46E+10	9.48E+07
1.00E+08	2.00E+08	4.50E-09	3.47E+06	9.65E+02	4.02E+01	1.10E-01
3.30E+07	6.60E+07	1.42E-08	3.04E+30	8.43E+26	3.51E+25	9.63E+22

Table 1: MTBF as a Function of f_{DATA}, f_{CLK}, and Walkout Time

References

1 Chaney, Thomas J., "Measured Flip-Flop Responses to Marginal Triggering", *IEEE Transactions on Computers*, Vol. C-32, No. 12, pp. 1207-1209, December 1983.

2 Beaston, John and R. Scott Tetrick, "Designers Confront Metastability in Boards and Busses", *Computer Design*, pp 67-71, March 1, 1986.

3 Chaney, T. J. and F. U. Rosenberger, "Characterization and Scaling of MOS flip-flop Performance in Synchronizer Applications", in *Proc. Conf. Very Large Scale Integration Architecture, Design, Fabrication*, California Instit. Technol., pp. 357-374, 22-24 Jan. 1979.

8

INTRODUCTION

For several years, Gallium Arsenide ICs have proven extremely useful in high-speed linear applications such as microwave amplifiers and fiber optic drivers. Within the past five years, however, improvements in processing technology coupled with the use of advanced design techniques have made the production of VLSI GaAs integrated circuits a reality. Vitesse Semiconductor Corporation has developed a tightly controlled GaAs enhancement/depletion mode (E/D) process. This process in conjunction with its direct-coupled FET logic (DCFL) design technique has enabled Vitesse to produce and ship ASIC circuits with complexities of over 100,000 gates. The performance of these circuits and the available ECL-compatible I/O structures allow GaAs DCFL ASICs to serve as a viable alternative to ECL gate arrays or standard cells at the system level. This application note describes the similarities and differences in structure and implementation of GaAs DCFL and Bipolar ECL/TTL ASIC devices.

WHAT IS DIRECT-COUPLED FET LOGIC?

Direct-coupled FET logic (DCFL) is a technique used to design logic structures from enhancement and depletion mode FETs. DCFL has been in use since the mid-1970's to build nMOS circuits and is widely recognized for its density and simplicity in the creation of large integrated circuits.

On paper, GaAs DCFL logic looks virtually identical to nMOS with the exception that nMOS uses MOSFETs while GaAs DCFL uses MESFETs. MOSFETs have an oxide insulated gate which prevents the flow of gate current, while MESFETs contain a Schottky barrier diode in the gate-source junction which allows the gate to source current supplied from the previous stage of logic. The gate diode also clamps the internal V_{OH} level to about -1.3 V, or one diode drop above V_{TT}.

Figure 1 shows a 2-input NOR driving an inverter. The depletion mode FETs (*Q1* & *Q4*) have their gates shorted to their drains and act like current sources. When both *D0* and *D1* are low, *Q2* and *Q3* are off, allowing *ZN1* to rise and turn on *Q5*. The current from *Q1* in this case will flow through the gate of *Q5*. If either *D0* or *D1* are pulled high, the *Q1* current is shunted through *Q2* and/or *Q3*, pulling *ZN1* low.

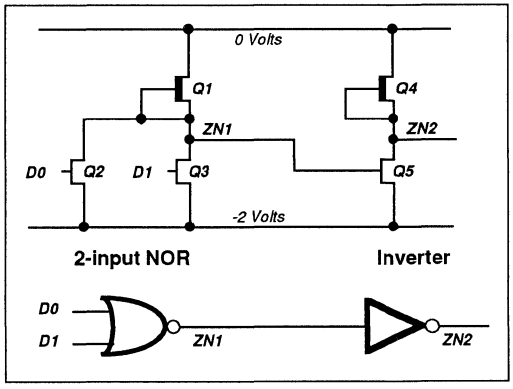

Figure 1: DCFL 2-input NOR and Inverter

DCFL Features

The key advantages of DCFL are circuit simplicity and the ability to switch very quickly using a small supply voltage. The 2-input NOR gate shown in Figure 1, uses only three transistors (resistors are not necessary). GaAs DCFL can operate reliably on a 1.1 V power supply, in contrast to bipolar ECL which requires either 4.5 or 5.2 V. Unlike ECL, no internal reference voltages are needed for GaAs DCFL circuits. All logic switches around the enhancement-mode FET threshold (about 250 mV above the source voltage, V_{TT}).

On the flip side, however, GaAs DCFL does not allow the use of series-gated structures, wire-ORs, or collector-dotting (all features of ECL).

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This is offset by the higher circuit density and corresponding shorter device interconnection lengths found in GaAs DCFL. Virtually all logic structures which have been created for Vitesse ASIC products ars constructed from simple inverters or two to four input NOR gates. Figure 2 depicts a full adder macro implemented in GaAs DCFL. The logic portion of this macro is built from three 2-input NORs, five 3-input NORs, and one 4-input NOR. Vitesse incorporates a proprietary buffer on the outputs which effectively drive large capacitive loads with very little skew between the rising and falling edges. Table 1 is a comparison of the GaAs DCFL full adder macro with an equivalent version implemented in silicon bipolar ECL technology. Note that the GaAs DCFL version has a significantly shorter propagation delay, dissipates less than 30% of the power and uses only 70% of the space needed by its silicon counterpart.

Parameter	GaAs DCFL	Silicon ECL
A/B → SUM	836 ps	1125 ps
$C_{in} \rightarrow C_{out}$	587 ps	1338 ps
Power (typ)	4.8 mW	16.58 mW
Area	21236 μm^2	31750 μm^2

Table 1: GaAs DCFL vs. Silicon ECL: Full Adder Macro Comparison

BUFFERING TRADEOFFS

Many ECL ASIC products allow for a tradeoff between speed and power. This is generally accomplished by allowing the designer to select different switch and emitter follower current values by paralleling resistors using the metal personalization. Generally, the resistors necessary for at least two different speed/power versions of many functions are included in the basic cell. In GaAs DCFL, however, the trade-offs involved in buffering are somewhat different. In Vitesse's FURY and FX Series' of gate arrays, internal macrocells can have unbuffered, 1x drive, or 2x drive outputs. The trade-offs involved with this choice of buffering involve speed, power, and density. Moreover, the speed/power versus density tradeoffs will vary depending on the complexity of the macro function. In general, the presence (or absence) of buffering

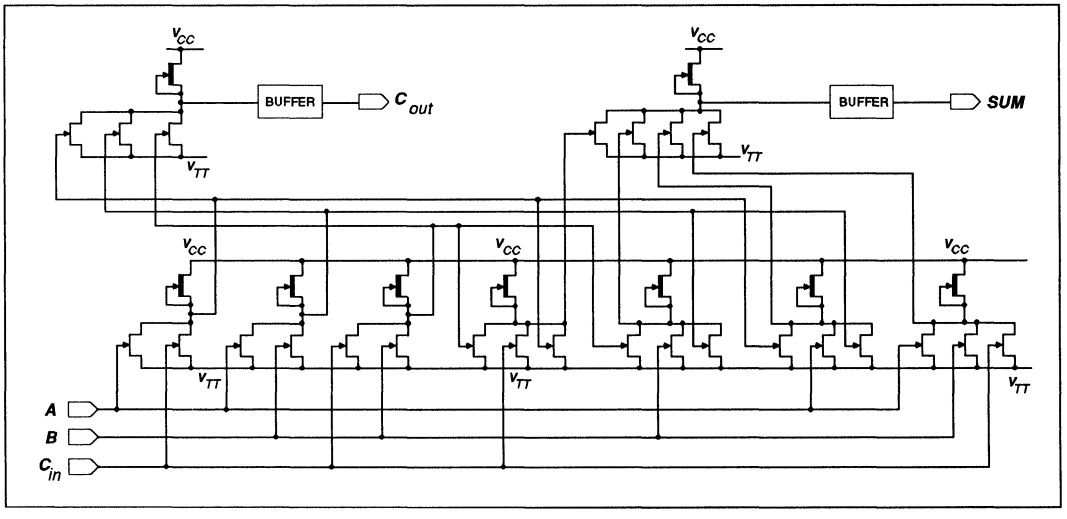

Figure 2: Full Adder Implemented in GaAs DCFL

affects the intrinsic delay of the macro very little. Buffering will increase the driving ability of the macro output in terms of both DC drive limitations and AC performance. On the other hand, buffering requires additional depletion and enhancement mode devices which could otherwise be used for logic and also consumes additional power. The more complex the macro function, the less the price paid for the buffer in terms of percentage area and power. Figures 3 and 4 depict the buffering tradeoffs for a 4-input NOR and a D flip flop in the FX Series macrocell library.

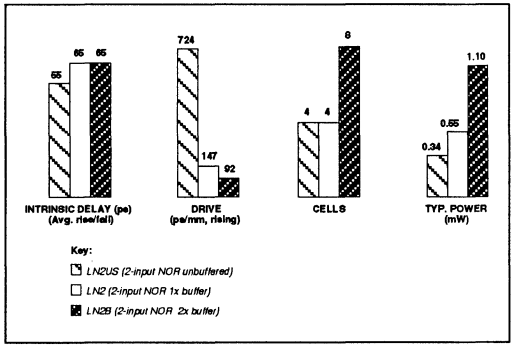

Figure 3: FX Macro Buffering Options for a 2-input NOR Gate

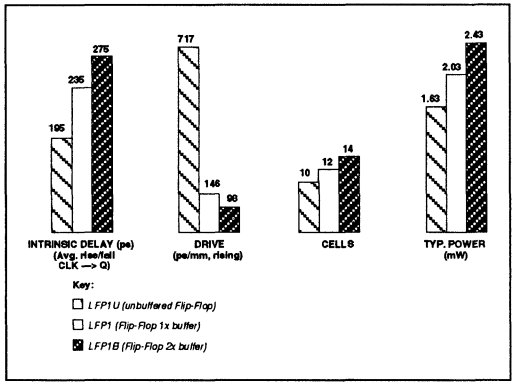

Figure 4: FX Macro Buffering Options for a D Flip-Flop

FURY GATE ARRAY ARCHITECTURE

Like most third generation ECL gate arrays, the Vitesse FURY Series of gate arrays employ a channeled architecture. Metal 1 is used to route within macrocells and in the vertical channels between macrocell columns reserved for routing. Metal 2 channels run horizontally over the entire core area. A third layer of metalization is used for fixed power and ground distribution in the macrocell columns. Figure 5 shows the layout of the FURY VSC15K array.

The I/O ring contains 96 input-only buffers on the sides of the array and 100 input/output buffers on the top and bottom for a total of 196 I/O pads. A D-latch or buffer can be implemented in the input-only cells and a D-flip flop or a 2 or 3-input OR/NOR gate may be placed in the output cell structure. In addition, each FURY array contains a small number of high-drive input cells which are used for distributing large fanout signals, such as clocks, to local buffers in different areas of the core.

Each cell column in the core is composed of a large number of "slices" (192 in the case of the VSC15K). A slice consists of four cells in a 2 by 2 configuration. A cell is equivalent to an unbuffered 2-input NOR (two enhancement-mode FETs and one depletion-mode FET). The minimum addressable unit (MAU) in a FURY array is two cells (six FETs). By contrast, the typical ECL gate array MAU contains 10 to 19 transistors and an equal number of resistors. The finer granularity of the FURY MAU minimizes the number of wasted transistors in a given macrocell implementation allowing for virtually 100% use of the core cells.

To the IC designer, a Vitesse GaAs DCFL gate array appears much the same as its present ECL counterpart. Both have internal and I/O macrocells and both generally use channeled architectures with two layers of user metal and one layer of power/ground metal.

FX ARRAY ARCHITECTURE

The FX Series offers the integration level of BiCMOS gate arrays with speed performance exceeding that of ECL devices. Implemented using Vitesse's proprietary H-GaAs III process, the FX family of gate arrays is the first to combine ultra high integration with leading edge performance.

The FX array family incorporates a channelless array architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach avoids the need for pre-defined channels between columns of macros and therefore allows much greater density and flexibility than channelled gate array architectures. Due to an advanced four layer metal process, typical maximum array utilizations range from 50% to 67% of the total available gates.

Capable of operating at well over 500 MHz, the FX Series arrays have been designed to provide the best speed - power performance of any gate array technology. The speed of leading edge ECL technology is achieved at a fraction of ECL's power. In addition, because of the frequency independent power consumption of H-GaAs technology, power dissipation levels comparable to, or lower than, similar density BiCMOS arrays can be achieved at frequencies above 50 MHz (see Vitesse Application Note 10, "Power Dissipation: BiCMOS vs. GaAs"). This power savings can add up to substantial cost savings to users in terms of overall cooling requirements.

The FX Family includes support for the creation of custom masterslices. Functions such as SRAMs, multiport register files, and others can be merged with FX arrays resulting in unique architectures and optimum performance.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL and ECL devices directly. The FX array family uses standard power supplies and is supported on the ASIC industry's

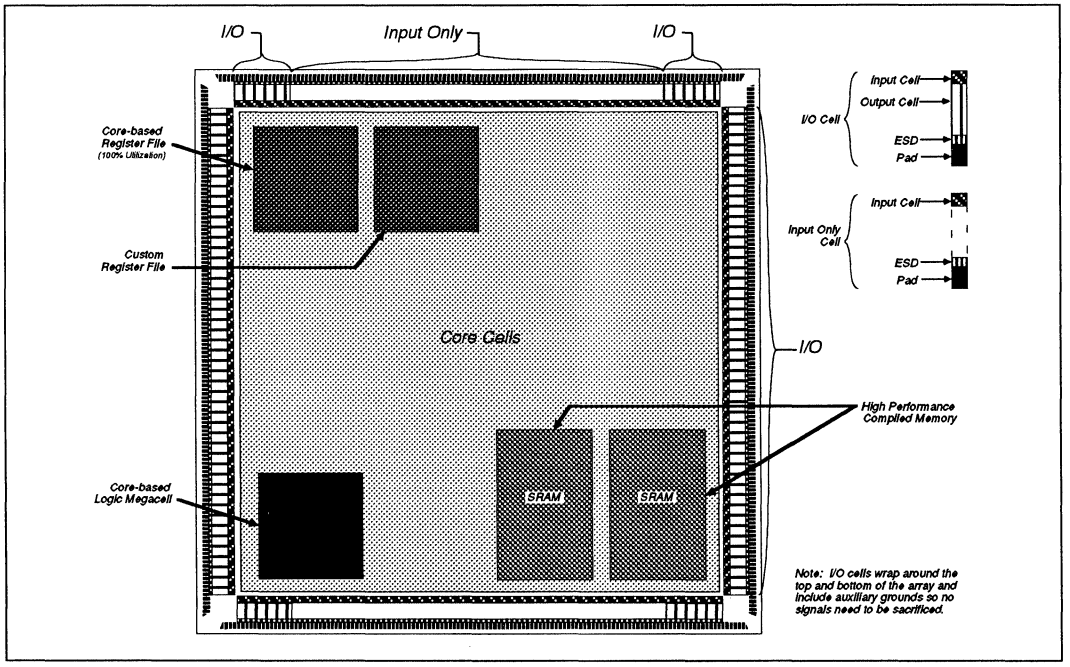

Figure 6: FX Array

most popular CAE platforms for schematic capture, behavioral modeling and logic synthesis.

The FX arrays contain three cell types: internal logic cells, input only cells and input/output (I/O) cells. All input only and input/output cells contain undedicated logic which the user may personalize. There is enough configurable logic in these cells to implement moderately complex functions such as mux'es and flip flops, allowing the arrays to conform to the JTAG boundary scan standard.

FX arrays can be designed to implement full custom megacells such as SRAM and pre-defined core based megacells such as register files. In addition, a proprietary compiler is available to customers wishing to incorporate custom RAM configurations in their designs. A depiction of a VGFX350K with megacells incorporated is shown in Figure 6.

RAM/ROM Megacells

As with ECL standard cell architectures, the FX gate arrays allow for the inclusion of custom, hand-packed "megacell" blocks. Unlike newer ECL standard cell technologies which use BiCMOS for the implementation of dense RAM, the FX arrays use the same GaAs E/D process and design rules for RAM and ROM blocks that are used for standard DCFL logic.

SYSTEM CONSIDERATIONS

At the system level (i.e., looking at a packaged part as a black box), Vitesse GaAs ASICs are virtually identical to ECL ASICs. ECL I/O buffers as well as TTL buffers are supported on all FURY and FX ASIC products. In implementing a board design which includes a Vitesse ASIC, however, the designer should be aware of ECL I/O differences and power supply requirements.

ECL I/O

Vitesse ASICs support ECL 100K input and output levels. Unlike standard ECL 100K, however, the GaAs V_{OL} min is always equal to V_{TT} because the ECL outputs are cutoff in the low state. This is not a problem in digital applications, but may necessitate the use of a higher V_{TT} (approximately -1.7 Volts) when driving a DAC because of potential analog feed-through problems associated with the larger input swings. Also, the -2.0 Volt supply must be controlled to ±5% to ensure that adequate noise margins are maintained using the internal V_{BB} reference generator. If such regulation is not feasible, or if the design must receive 10KH levels (which vary with temperature), then an external V_{BB} reference should be supplied.

Power Supply Considerations

Nearly all Vitesse ASICs use -2 V as the primary supply voltage. In fact, for an ECL-only interface, -2 V is the only supply required. Although the power dissipated by GaAs DCFL circuits is relatively small, the -2 V regulator must be capable of supplying a large amount of current (up to 4 Amps in the case of a fully utilized VSC15K gate array). When TTL interfaces are needed, a +5 V is required. Some gate arrays can be configured to a +5V, +2V supply environment for TTL only operation.

CONCLUSION

Though the internal logic structures and raw materials used to construct GaAs DCFL ASICs are somewhat different from those used to build ECL ASICs, the two technologies are virtually identical at the system level. The density and performance of GaAs DCFL ASICs make them attractive alternatives to ECL ASICs in many systems. With the advent of the FX family, the system designer now has the flexibility to more fully reap the benefits of GaAs DCFL technology. The major advantage of GaAs DCFL technology is the ability to produce ASIC devices which offer better density and performance than ECL while dissipating only 1/4 to 1/5 of the power.

INTRODUCTION

The use of multiple ECL (or ECL-compatible GaAs) ASIC devices on a circuit board may require the addition of an externally generated ECL input reference voltage (V_{BB}). Providing this reference ensures that the input receivers of the ECL devices will all switch at the same threshold voltage independent of power supply or temperature variations.

This application note describes a method for providing an external ECL input reference (-1.32 Volts) from a standard -2.0 Volt ECL supply using an adjustable micropower voltage reference and three resistors.

REFERENCE CIRCUIT DESCRIPTION

The reference circuit employs three resistors and an LM185, LM285, or LM385, which are 3-terminal adjustable band-gap voltage reference devices available from National Semiconductor Corporation. The LM185 is rated for operation over a -55°C to 125°C temperature range, while the LM285 is rated from -40°C to 85°C and the LM385, from 0°C to 70°C. A block diagram of the LM185/285/385 is shown in Figure 1. The circuit shown in Figure 2 is used to create the voltage reference.

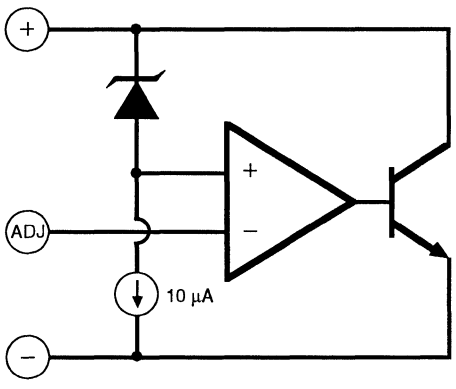

Figure 1: Block Diagram of the LM185/285/385

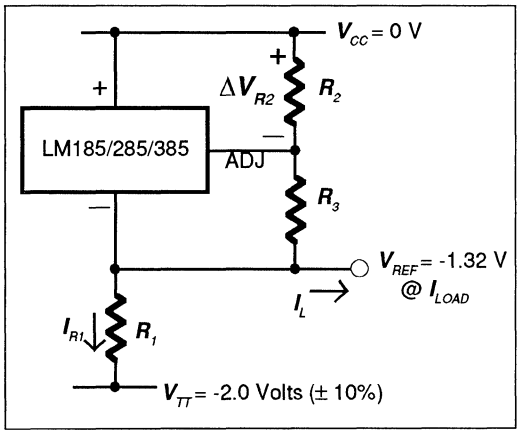

Figure 2: ECL Reference Circuit

The reference circuit shown in Figure 2 uses V_{TT} and V_{CC} as external voltages to produce the reference voltage, V_{REF}. In order to create a reference which can be used with Vitesse ECL-compatible ASIC parts, the values for R_1, R_2, and R_3 must be chosen under the following operating conditions:

- Supply Voltage,(V_{TT}) -2.0 Volts (± 10 %)
- Current through LM185/285/385 from + to —, (I_D) 0.10 to 20 mA
- ADJ Current through LM185/285/385, (I_A) ≤ 10 nA (guaranteed by LM185/285/385 specs)
- Current to each Vitesse ECL compatible input cell from V_{REF}, (I_{Input}) ≤ 5 µA
- Potential between V_{CC} and ADJ, (ΔV_{R2}) 1.24 Volts (reference voltage produced by the LM385)

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The values for R_2 and R_3 must satisfy the following condition:

$$V_{REF} = -1.24 \left(\frac{R_3}{R_2} + 1\right) \quad [1]$$

By equation [1], the following commonly available resistor values can be used for R_2 and R_3 to create a -1.32 Volt ± 10mV reference:

$R_2 = 16K\,\Omega$
$R_3 = 1K\,\Omega$

The stability of V_{REF} depends on the tolerances of these two resistors. If k is the maximum normalized value and p is the minimum normalized value of the resistors R_2 and R_3 expressed as decimals, then the variation in V_{REF} is given by the following equation:

$$\Delta V_{REF} = \frac{\frac{R_3}{R_2}\left(\frac{k}{p} - 1\right)}{\frac{R_3}{R_2} + 1} \quad [2]$$

Assuming that the resistors have a 5% tolerance and substituting values into the equation, we can then solve the equation:

$$\Delta V_{REF} = \frac{\frac{1K\Omega}{16K\Omega}\left(\frac{1.05}{0.95} - 1\right)}{\frac{1K\Omega}{16K\Omega} + 1} \quad [3]$$

$\Delta V_{REF} = 0.6\%$ or ~8mV

Although use of 5% resistors gives a tight V_{REF}, it is advisable to use 1% metal film resistors instead of the commonly available 5% carbon composition resistors to minimize aging effects and to compensate for the tolerance on the 1.24 Volt bandgap reference voltage.

R_1 determines the no load regulator current. Assuming worst case power supply and 175µA total regulator current, then:

$$R_1 = \frac{1.8\text{-}1.32}{175\mu A} = 2.7\ k\Omega$$

Since the regulator can source up to 20mA, as many as 4000 Vitesse ECL inputs can be supported. Thus, a single regulator circuit, as shown in Figure 3, can be used on a circuit board to supply ECL input reference for many Vitesse IC's. A typical Vitesse compatible external V_{REF} pad is shown in Figure 4. The exact number of IC's is dependent upon the number of ECL inputs per IC. The load current per input cell is ≤ 5µA, with an additional 100µA ESD diode leakage current per chip. For example, if 3 ASIC devices with 40 inputs each are serviced by the external V_{REF} circuit, then:

$I_L = (3x40x5\mu A) + (3x100\mu A)$
$= 900\mu A$

When more than 40 inputs are connected to the reference, the value of the bleeder resistor R_1 becomes relatively unimportant and, for example, can be made equal to R_2 (16KΩ) in order to reduce parts inventory.

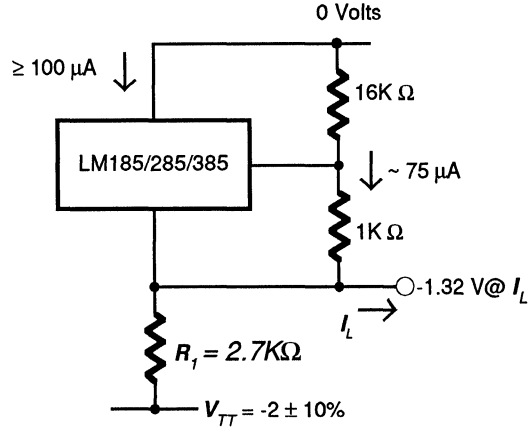

Figure 3: Implementation of Reference Circuit

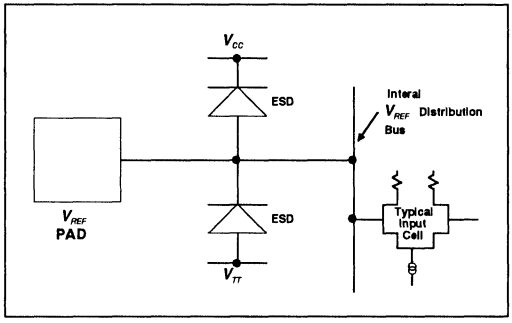

Figure 4: Typical Vitesse External V_{REF} Pad

Notes

1. In order to use this reference generation scheme, the Vitesse ASIC product (gate array or standard cell) must be specified with an external ECL reference.
2. Vitesse recommends the use of a 0.001 to 0.01 µF bypass capacitor at the reference input pin of each array. Refer to the design manual for the particular ASIC product for the location of the input reference pins.
3. Care must be taken to account for the effect of IR drop in the refer ence net on the PC board.

INTRODUCTION

CMOS and BiCMOS have traditionally been viewed as low power technologies. This reputation stems from the fact that unlike other technologies which have preceded them (TTL, ECL, NMOS, etc.) the power dissipated by a CMOS or a BiCMOS gate is dependent on the frequency of its operation. When CMOS or BiCMOS gates are not toggling they dissipate almost no power. As operational frequencies in the gates increase, however, the amount of power dissipated proportionately increases. At these higher frequencies, GaAs Direct Coupled FET Logic (DCFL), which is capable of faster gate delays, dissipates less power than BiCMOS.

The purpose of this application note is to show how both BiCMOS and DCFL GaAs power dissipation is calculated and to examine and compare the two technologies with regard to power dissipation.

POWER CALCULATIONS FOR BICMOS

There is little or no static power dissipated in most practical topologies of BiCMOS gates since current is used exclusively to charge and discharge load capacitance. BiCMOS ASIC design manuals instruct the user to compute the internal cell power dissipation by multiplying a factor, whose units are microwatts/(gate-MHz), by the frequency of operation. This result is then multiplied by the total number of cells in a given design derated by an arbitrary fraction representing the number of gates switching. This latter derating factor ranges from 0.2 to 0.4 depending on the design at hand. The composite power is calculated using the following formula:

$$P_{internal} = F A_V G P_{gm} \quad (1)$$

Where:

F = the highest frequency in MHz for gates in the design

A_V = average fraction of the gates which are switching at a given time

G = the total number of gates in the design

P_{gm} = the power per gate-MHz (typically between 20 and 40 microwatts/gate-MHz)

To obtain accurate results from a particular design, however, it would be a mistake to use the A_V

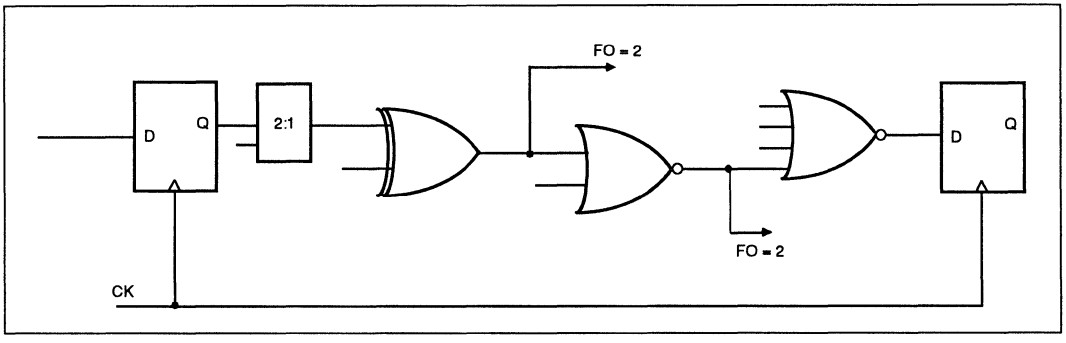

Figure 1: Benchmark Circuit. *This circuit is analyzed in the text to compare its power dissipation vs. frequency when implemented in BiCMOS and GaAs.*

estimation factor blindly. Not using any derating factor could also result in an incorrect estimate of the power dissipated in a sequential circuit. Between two successive registers in a sequential circuit there may be several levels of logic. As a result, the effective frequency seen by any one gate in the chain of gates between registers can be substantially lower than the clock frequency applied to the registers. For small designs it is practical to explicitly calculate the effective frequency of operation of each gate and obtain an accurate understanding of power dissipation.

As an example please refer to the benchmark circuit of Figure 1. Here several stages of logic are placed between two flip-flops. The maximum frequency seen by any gate other then the flip-flops is one half of the flip-flop frequency. This is due to the fact that the output of a flip-flop can only toggle at one-half its clock frequency. In addition, there is a statistical probability of 0.5 that the output of a given gate or flip-flop will remain at its previous logic state (assuming an equal number of ones and zeros in the incoming data stream) in which case no power is dissipated since a transition did not occur.

We can split the problem into two; the power dissipated in the flip-flops and the power dissipated in the gates. For the flip-flops the power can be estimated by:

$$Power = F(0.5)GP_{gm} \quad (2)$$

and for the gates in between:

$$Power = F(0.5)(0.5)GP_{gm} \quad (3)$$

POWER CALCULATION FOR DCFL GAAS CIRCUITS

Unlike CMOS or BiCMOS, DCFL GaAs circuits have a power dissipation which is independent of logic state or frequency of operation. The reason for this can be seen by examining Figure 2 which depicts a typical DCFL NOR gate driving an inverter. The DCFL structure is composed of a pull up depletion FET and one or more pull down enhancement FETs. The NOR operation is possible because when both pull down FETs are off (corresponding to a logic low at each input) the logic gate's output voltage rises to a valid logic high. However, when one or more pull down FETs are on (corresponding to a logic high at their input) the pull down FET sinks all of the pull up FET current while maintaining a very small Vds. As a result a valid logic low is created at the gate's output.

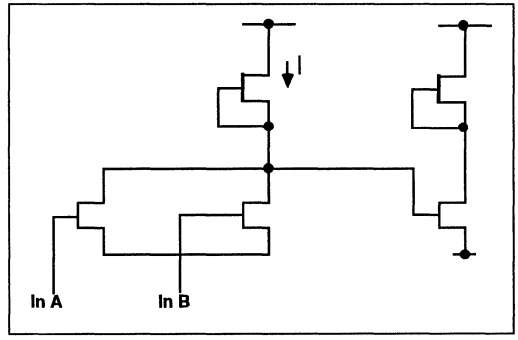

Figure 2: DCFL Logic

GaAs FETs, unlike silicon MOS devices, do not have an insulator between the gate and channel region. Instead they employ the depletion region of a schottky barrier junction to modulate drain to source current. This schottky diode will conduct current between the gate and source when forward biased.

In normal DCFL operation, a valid logic high voltage is determined by the forward biased voltage of the gate to source diode. As a result the load current, I, of a DCFL gate will be used to forward bias the gate to source diode of a subsequent logic gate.

In normal operation the current consumption of a DCFL logic gate is constant. Current is simply steered either into the pull down FET in a logic low condition or into the gate to source diode of a subsequent logic gate in a logic high condition. For high speed logic this situation is ideal because current, and subsequent voltage, "spiking" on power supply lines is eliminated.

Therefore, when calculating the power dissi-

pation of a DCFL based chip, the power dissipation reported for an individual logic macro is valid for any frequency at which it can operate.

BENCHMARK CIRCUIT

To get an idea of the range of speeds and power dissipations achievable in both BiCMOS and GaAs technology we turn our attention again to the benchmark circuit of Figure 2. Table 1 shows the delay for each macro in both BiCMOS and GaAs technology. For the BiCMOS portion of this analysis the NEC BiCMOS-5 design manual was used. The Vitesse FURY manual was used for the GaAs portion.

As seen from Table 1 the delays for both rising and falling output waveforms were calculated. Because NOR gates cause signal inversion the worst case delay through a network must be calculated by evaluating all realistic propagations through the cascade of gates taking signal inversions into account. The worst case path for each situation is designated by arrows in Table 1.

MACRO	DELAY (BICMOS)		DELAY (GaAs)	
	Rising	Falling	Rising	Falling
F/F CLK» Q	2.75	2.59	0.59	0.36
2:1 MUX (Fo = 1)	1.93	2.10	0.61	0.28
2 Input XOR (Fo = 3)	1.66	2.10	1.34	0.45
2 Input NOR (Fo = 3)	1.26	0.50	1.15	0.56
4 Input NOR (Fo = 1)	2.88	0.45	0.49	0.26
F/F Setup Time	0.25	0.25	0.14	0.14
Rising Delay	9.97 nS		3.73 nS	
Falling Delay	9.98 nS		3.20 nS	
Max Operating Freq.	100.2MHz		268.1 MHz	

Table 1: Macro Delay

Table 1 indicates that, for the benchmark circuit, the maximum frequency attainable in BiCMOS is 100.2 MHz. GaAs technology is capable of a 268.1 MHz frequency. The GaAs macros selected for this particular analysis are optimized for low power dissipation. As a result a factor of 2.7 improvement in speed is observed between GaAs and BiCMOS. A greater investment in power could yield speed improvement factors of between four and five.

Table 2 and the corresponding graph in Figure 3 (following page) depict the power dissipated by each technology as a function of frequency for the benchmark circuit. The power for the BiCMOS circuit was calculated using equations (2) and (3). The Pgm value NEC attributes to their BiCMOS-5 process is 0.038 mW/MHz.

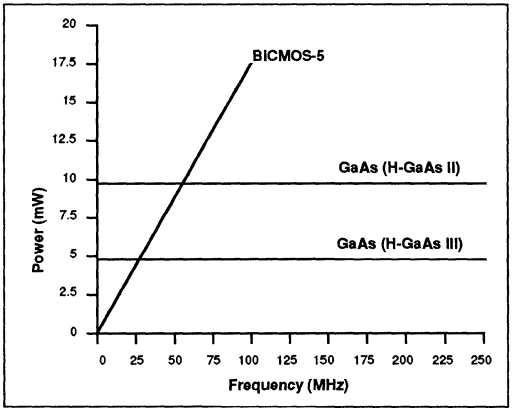

Table 2: Macro Power

As seen in Figure 3, the crossover point between the linear BiCMOS power curve and the constant GaAs power curve occurs at about 60 MHz with the H-GaAs II process and at about 30 MHz with the H-GaAs III process. Since, for the circuit in question, BiCMOS is limited in frequency to about 100 MHz one can only speculate about the power it would dissipate if capable of higher frequencies. However, since the curve is linearly increasing it is safe to say that at frequencies above 150 MHz BiCMOS power dissipation is unreasonably high.

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BiCMOS

FUNCTION	BICMOS-5 MACRO NAME	POWER DISSIPATION (mW)			
		25MHz	50MHz	80MHz	100MHz
Flip-Flop	F641	1.42	2.85	4.56	5.7
2:1 MUX	F571	0.47	0.95	1.52	1.9
2-Input XOR	F511	0.47	0.95	1.52	1.9
2-Input NOR	F202	0.24	0.475	0.76	0.95
4-Input NOR	F204	0.24	0.475	0.76	0.95
Flip-Flop	F641	1.42	2.85	4.56	5.1
		4.26	**8.55**	**13.68**	**17.1**

GaAs

FUNCTION	FURY MACRO NAME	POWER (mW)	
		H-GaAs II	H-GaAs III
Flip-Flop	LFPIU	3.1	1.55
2:1 MUX	LMIU	1.3	0.65
2-Input XOR	LXIU	1.7	0.85
2-Input NOR	LN2U	0.33	0.16
4-Input NOR	LN4U	0.33	0.16
Flip-Flop	LFPIU	3.1	1.55
		9.86	**4.92**

Source: NEC BiCMOS-5 Design Manual, Oct. '89
Vitesse FURY Design Manual, v. 3.0

Figure 3: Power Dissipation vs. Frequency for Benchmark Circuit

CONCLUSION

BiCMOS, which has earned a reputation as a low power technology, earns that reputation at low frequencies only. Since its power dissipation increases linearly with frequency, GaAs technology actually dissipates less power at frequencies above 60-70 MHz. This capability coupled with the fact that GaAs technology is capable of speeds which range between a factor of 3 to 5 faster than BiCMOS positions GaAs as the dominant technology for any high speed digital application.

Application Note 11

The Effects of Simultaneously Switching Outputs in GaAs Devices

INTRODUCTION

When one or more outputs of a semiconductor device switch, a change in voltage is effected on the driven signal lines. This change in voltage is in turn received by any inputs connected to those signal lines and interpreted as a change in logic state. Switching a group of outputs simultaneously, however, may cause undesirable effects on the operation of a circuit. These unwanted consequences are generally referred to as simultaneously switching output (SSO) effects. Features have been incorporated into the design of all Vitesse devices (die and packages) which minimize the deleterious effects of SSO's. These effects have been characterized by Vitesse using a test chip personalization of the FURY VSC10K gate array packaged in a multilayer ceramic 211 pin grid array.

The purpose of this application note, therefore, is to help the system designer minimize the probability of device or board level problems associated with SSO's. This will be accomplished by presenting the designer with some of the physics associated with output switching phenomena as well as some of the methods used to alleviate the effects of SSO's.

STATEMENT OF PROBLEM

Simultaneously switching outputs can cause the following effects:

- Additional output delay
- Ground or power supply noise at the device
- Ground or power supply noise in the system
- Noise on adjacent signal pins which share supply or ground pins

ELECTRICAL EFFECTS OF OUTPUT SWITCHING: A BASIC MODEL

Figure 1 shows an ECL source-follower output driving a capacitive load and a 50Ω resistor. Figure 2 demonstrates the relationship between the drain voltage of the output FET (node A) and the source voltage of the output FET (node B) as a pulse is propagated through the ECL output. When the output switches from a logic low state to a logic high state, a substantial gate to source voltage is applied to the output FET causing its source-drain conductance to increase dramatically.

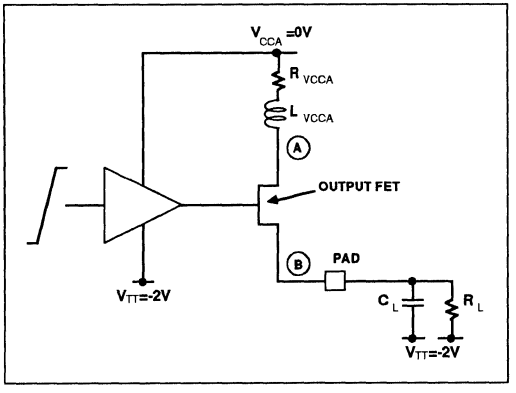

Figure 1: ECL SSO Model

As the transient current is conducted through the device to charge the capacitive load, an instantaneous demand for current is placed on the VCCA (output ground) supply terminal of the output node A. If inductance is present in the VCCA supply path (as shown in Figure 1), the voltage at node A will drop until the inductor is energized and necessary current can be supplied to the output FET. A falling output edge conversely creates a positive transient voltage on the VCCA node. Increasing the inductance in the tends to impede the transient current flow and increase the size of the SSO noise pulses

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shown in Figure 2. At the system level, these effects are manifested as degradations in the pin-to-pin delay of a device. In addition, if sufficient noise is coupled from the VCCA pins to the logic elements in the device, the states of synchronous elements (registers or latches) in the core of the device may be altered causing the circuit to logically fail.

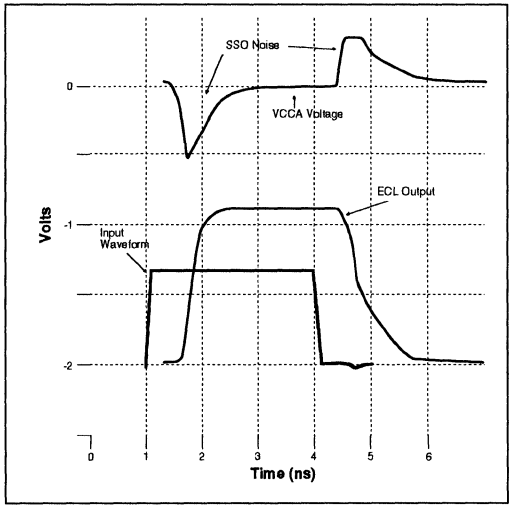

Figure 2: Power Supply Noise

ASIC DEVICE AND PACKAGE FEATURES TO ALLEVIATE SSO PROBLEMS

All of Vitesse's high-performance packages are designed to minimize the electrical problems associated with simultaneously switching outputs. The power and ground pads on each device are fixed. These pads are bonded to separate planes in the multi-layer ceramic package. In order to isolate critical asynchronous inputs (such as clock and reset signals) from noise generated by output switching, outputs on Vitesse devices are confined to the top and bottom of the die (see Figure 4). Signals which are sensitive to noise can then be brought onto the device though input buffers on the left and right sides of the die. This not only isolates the inputs and outputs on the die itself but also minimizes mutual coupling (crosstalk) between output and input bond wires by placing them at 90° with respect to one another.

SSO TEST CHIP DESCRIPTION

Output Registers

In order to gain an empirical understanding of the effects of switching large groups of outputs on a large device, Vitesse has designed and produced a test chip specifically designed to examine these effects. The schematic of the test chip is shown in Figure 3. The SSO test chip, or SSOTC, is implemented using a Vitesse FURY VSC10K gate array in a 211 PGA package. The test circuitry consists of 80 shift registers grouped into four banks of 20 registers each. Each shift register contains four D flip-flops. The four Bank Scan signals allow data on the SDAT (scan data) bus to be clocked into the shift registers on a bank by bank basis. The input CLOCK serves as the system clock for both scanning and shifting operations. To reset all the registers at once, the RESET signal can be asserted. The BZ bus signals allow the user to force the outputs of given bank to logic low without resetting the registers in the bank. Using the scan inputs, patterns which switch anywhere from one up to 80 outputs can be scanned in and clocked to the Z outputs.

As with all FURY gate arrays, the power and ground pins are in fixed locations. In order to minimize the undesirable effects of simultaneous output switching, every four outputs typically share a ground, or VCCA, pad. The VCCA pads are in turn bonded to conductor planes in the 211 PGA package.

Upset Structures

In order to monitor the coupling of noise back into the SSO test chip, eight upset structures are interspersed around the periphery of the gate array as shown in Figure 4. Each upset structure consists of a D flip flop (FURY LFP3 macrocell) configured so that it will toggle on an active clock edge. The

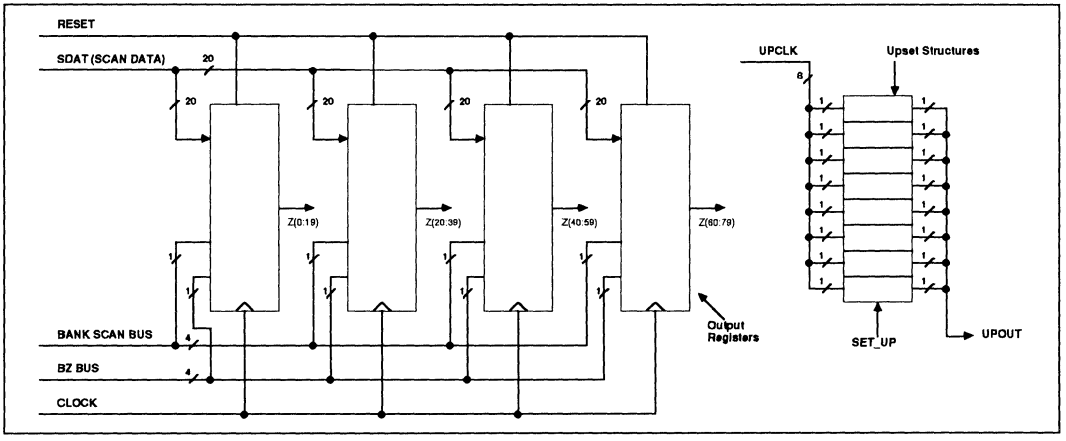

Figure 3: SSO Test Chip Schematic

clock inputs of these structures (UPCLK bus) are driven by ECL input pins. The outputs of these structures are connected directly to ECL outputs (UPOUT bus). If the noise generated by the simultaneous output switching is sufficiently coupled to the upset structure input, the flip-flop will toggle, thus signifying an upset failure.

SSO TEST RESULTS

Characterization of SSO effects was performed on a Teradyne J953 VLSI tester. In order to execute a given test, all the shift registers are first reset and then logic highs are shifted into the registers whose outputs are to switch. The master clock is then used to shift the pattern to the outputs causing first a group of simultaneous rising edges and then a group of simultaneous falling edges.

Simultaneous Switching Delay

The effects of concurrent switching on output delay were measured by connecting both the CLK signal and one of the Z outputs, to a high speed oscilloscope while the test chip is in the Teradyne test fixture. The tester was then used to force various switching patterns on the part while the relative delay was monitored. During the initial testing, it was determined that most of the observed SSO delay was due to the device test fixture. The test fixture was re-worked to minimize the impedance to the VCCA pins. Subsequent testing showed a minimal delay degradation as increasing numbers of outputs sharing the same VCCA pin were switched. Analysis of the delay data showed the following typical delay per output switched:

$$T_{pd}(SSO) = 15\ ps/SSO$$

for ECL outputs which share a common VCCA pad.

A maximum total delay degradation of approximately 100 ps was observed when switching up to six ECL outputs sharing the same VCCA pad. Increasing the number of outputs switching beyond six, however, appeared to have a negligible effect on the output delay.

SIMULTANEOUS SWITCHING NOISE

A second phase of testing was performed to characterize the coupling of SSO noise to input pins. For these tests, various combinations of the Z outputs were switched and the states of the upset structure outputs (UPOUT bus) were monitored. No upset structure failures were observed when switching up to 40 outputs simultaneously. Results

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for more than 40 outputs switching were inconclusive due to the noise inherent in the VLSI test environment.

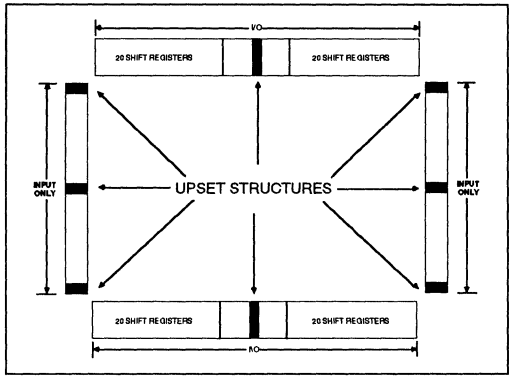

Figure 4: SSO Test Chip Block Diagram

As previously noted, however, SSO noise in the device appeared to be primarily a localized effect. The design of the pad ring on the FURY 10K as well as the design of the 211 PGA itself appears to accommodate the switching of all 100 ECL outputs on the device simultaneously with no effect on internal logic states.

SYSTEM DESIGN RECOMMENDATIONS FOR MINIMIZING SSO EFFECTS

To minimize the possibility of SSO related problems in a given system, precautions should be taken in the arrangement of the inputs and outputs on the ASIC as well as in the construction of the board on which the integrated circuit(s) will reside. The following guidelines summarize these precautions.

ASIC and Board Design Guidelines

1. Place all clock, set, or reset signals on the ASIC at least six pads away from any output.
2. When designing a custom pad ring,a) a VCCA pad should be allotted for each set of four ECL or GaAs outputs, and b) two VCCA pads and a VTTL (+5 V) pad should be allotted for each set of eight TTL outputs.
3. A large power plane should be used on the PC for distribution of VCCA (Figure 5).
4. The peak switching current should be estimated for the worst case number of SSOs per device and adequate bypass capacitance should be added to satisfy the transient VCCA and VTTL current needs.

Bypass Capacitor Recommendations

Bypass capacitors must be used in high frequency (>100MHz) designs to filter out high frequency variations in the power supply voltages at the device power inputs and on the board. The following bypassing is recommended.

1. A 0.01μF high frequency capacitor should be placed between ground (VCCA) and each V_{TT} (-2Volt) pin as close to the V_{TT} pin as possible.
2. A 1 to 10 μF capacitor should be placed on the board at the power supply inputs to filter out variation in the power supply with longer time constants (e.g. power supply noise at the system clock frequency.)

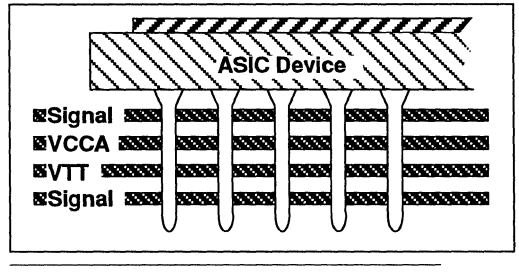

Figure 5: Recommended Ground Distribution

INTRODUCTION

This application note describes a general method for converting a design implemented in one technology into another technology using the Synopsys Design Compiler™. Specific guidelines are given for converting a "non-GaAs" design (e.g. CMOS, BiCMOS, ECL) into a Vitesse gate array or standard cell implementation. This document also contains specific information on converting PLD equation-based designs into Vitesse ASICs.

TECHNOLOGY TRANSLATION BASICS

The low speed-power product and high integration level possible with current Vitesse H-GaAs technology has created a need to translate designs from various Silicon-based technologies into Gallium Arsenide Direct-Coupled FET Logic (DCFL). Prior to committing to a redesign, high performance systems houses need a method to evaluate the performance, power, and size of their existing designs were they to be re-implemented in GaAs. Until recently, such translations could only be accomplished by either manually swapping logic functions from one technology to another on a workstation or by redesigning from the ground up using the alternate vendor's library. Both of these methods involve a great deal of effort and are prone to errors. Logic synthesis tools such as the Design Compiler™ from Synopsys, however, remove most of the manual tasks and result in virtually error-free design conversions.

GENERAL TRANSLATION FLOW

Figure 1 shows the sequence of events and the files involved to translate a design from one technology to another. Two alternate paths are shown - the left path is used if an EDIF netlist is not available. The actual translation is carried out by the Synopsys Design Compiler™ using the **link** command. Figure 2 shows the libraries needed for translation.

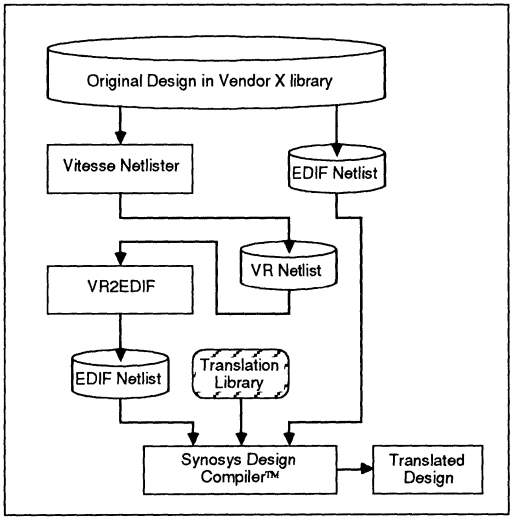

Figure 1: Design Transition Flow

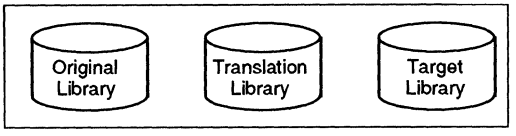

Figure 2: Translation Libraries

Original Library

This library contains all of the cells which are referenced in the original design. This may be a library from another (non-Vitesse) vendor or may be a Vitesse ASIC library (e.g. FURY gate array). If this library does not exist it can readily be created for the subset of cells which are used in the original design. Refer to the Synopsys Library Compiler Reference Manual for information on creating Synopsys libraries.

Translation Library

This library contains designs (cell descriptions) which are named after the sequential and tri-

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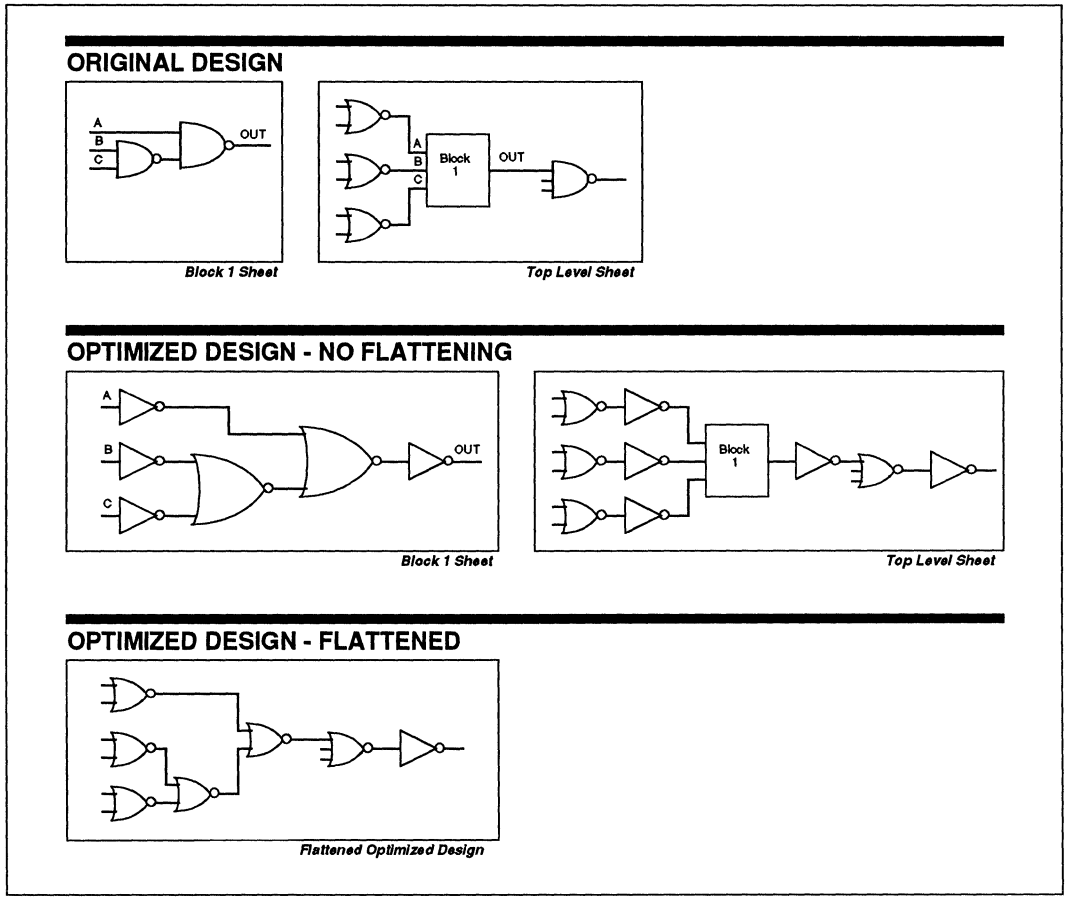

Figure 3: Optimizing a Hierarchical Design

state elements from the original library, but are described using cells from the desired Vitesse library. The user should note that all non-combinatorial functions as well as any tri-state functions in the original library must be mapped into the Vitesse library by creating entries in the translation library. Combinatorial functions such as AND gates, multiplexers, etc. need not be mapped explicitly by the user because the Synopsys Design Compiler™ can automatically (and unambiguously) map such functions between technologies.

TRANSLATING HIERARCHICAL DESIGNS

Designs may be converted from another technology into a Vitesse ASIC-based implementation regardless of whether the designs are hierarchical or flat. The conversion methodology used, however, depends upon the user's desire to preserve the original hierarchy present in the design after it has been converted. In making this choice, the following issues should be considered:

- *How large is the design?*
  If the design is in excess of 10,000 gates, the user may wish to convert hierarchical blocks individually and then link them in the Design Compiler™ at the end of the conversion. This not only preserves some of the original hierarchy in the design, but also requires far less computing resource (e.g. RAM and disk space) than converting the entire design at once.
- *Do optimized designs for some of the blocks already exist?*
  The design may contain, for instance, a 32-bit adder implemented using CMOS NAND-based structures. Several versions of 32-bit adders optimized for Vitesse GaAs DCFL implementations already exist. Thus, the user may choose not to convert this block at all and opt to use an existing block can be provided by Vitesse.
- *Will preserving the hierarchy produce a less than optimal design?*
  In certain designs, the original hierarchy (especially at the lowest levels) may make the application of optimization algorithms such as (DeMorgan equivalent circuits) difficult if not impossible. Figure 3, for example, shows an original hierarchical design and two different optimizations - one without flattening and one with flattening. The optimal design in terms of speed, power, and area is the flattened version. Keeping the hierarchy intact, however, will produce an optimized design similar to the one shown in the center of the figure.

Figure 4 shows the conversion flow for a hierarchical design. Note that some of the steps in this flow are not necessary if the user can provide a hierarchical EDIF netlist to Synopsys.

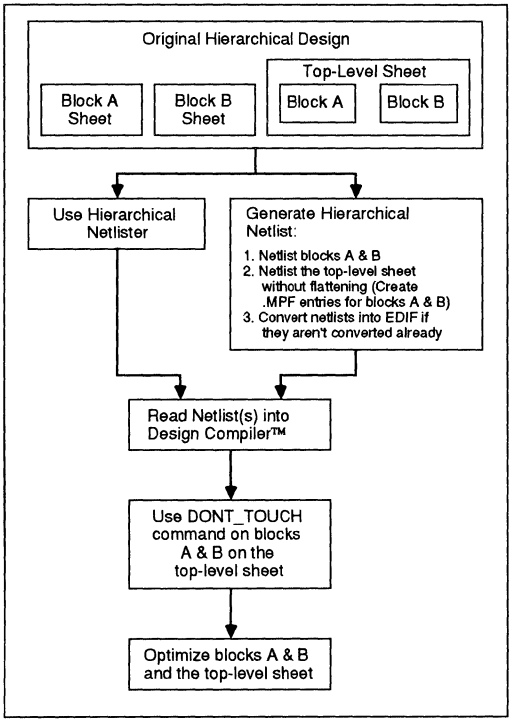

Figure 4 Hierarchical Conversion Flow

CONVERSION EXAMPLE

Figure 5 shows a 4-bit counter design in Vendor A's technology which is to be implemented as a Vitesse FURY gate array. The following steps are used to translate this design:

1. *Create the translation library.*
   The translation library is generated by creating representations of the sequential elements (D flip-flops, latches, etc.) and tri-state elements (tri-state outputs and internal buffers) in the Vitesse FURY library. In this example, Vendor A's library contains a D flip flop with Q and QN outputs not present in the FURY library. Therefore, the

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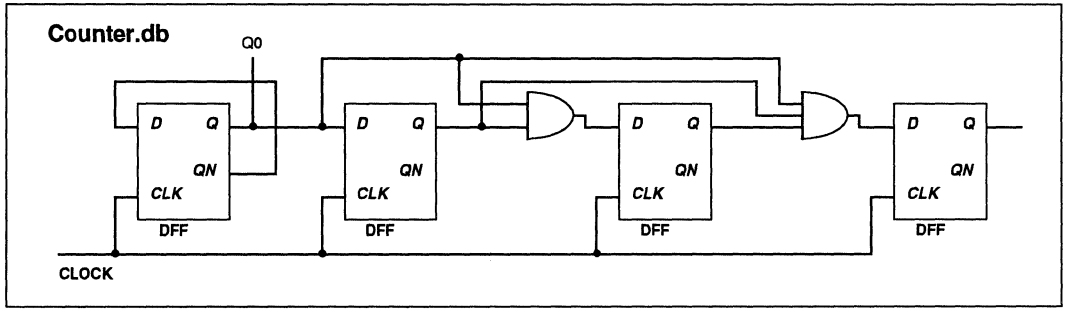

Figure 5: Four Bit Counter in Vendor A's Technology

design shown in Figure 6 must be created to represent the Vendor A's flip flop named DFF. In FURY library elements, an LFP1 D flip flop and an LDR1 inverter are combined to create Vendor A's DFF. (Note that the mapping of the LPF1 to the DFF flip flop would be necessary even if the two flip-flops were functionally identical.) The design *must* be named `DFF.db` and the port names *must* match the port names in Vendor A's cell.

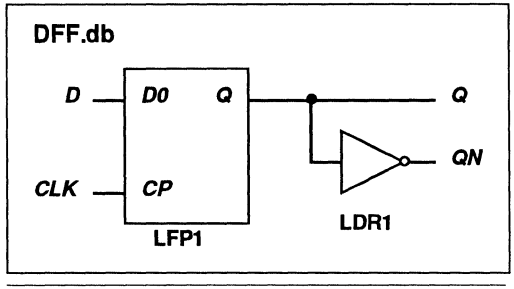

Figure 6: Vendor A's DFF Macro Mapped into FURY

2. *Create the link path.*
   To create the link path, we issue the following statement on the Design Compiler™ command line:

```
link_path = {translation_lib.db,
vendor_a.db, fury.db}
```

   This statement assumes that the translation library which contains our newly created `DFF.db` is named `translation_lib.db` and Vendor A's Synopsys technology library is named `vendor_a.db`. The `fury.db` library will reference Vitesse's FURY library. The `search_path` statement in the `.synopsys` startup file should contain the path or paths where all these libraries are located.

3. *Read in the top level of the original design.*
   In our example, the counter only has one level of hierarchy so we read in the design as follows:

   read counter.db

4. *Translate the design using the `link` command.*
   The `link` command resolves the references to the non-combinatorial elements using the translation library we have created. These non-boolean elements (such as our DFF) are resolved in exactly the same way the Design Compiler™ resolves any hierarchy.

```
link;
```

   At this point, the design is represented in a mix of Vendor A's technology library (the boolean elements) and the Vitesse FURY

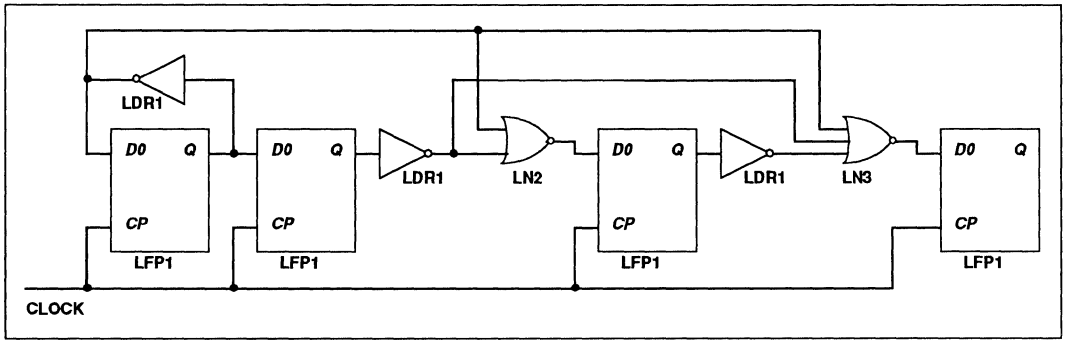

Figure 7: Four-Bit Counter Translated into FURY

technology library (the LFP1 flip flop).

5. *Compile the design to complete the translation.*
   Now we must issue the `compile` command to translate the boolean elements and eliminate the extra level of hierarchy that the **`link`** command created.

```
compile -no_flatten -
no_structure - map_effort low;
```

Note that the flattening and structuring functions in the Design Compiler™ are turned off and the mapping effort is reduced to its minimum level. This causes the design to be mapped without any logic optimization. Given the CPU time and disk space normally involved with the translation of a large design, this is highly recommended. Figure 7 shows the original design after it has been translated into the FURY gate array library.

6. *Write the translated design.*
   Use the `write` command to save the translated design in the Synopsys .db format.

```
write;
```

DESIGN OPTIMIZATION

Merely mapping the design into GaAs DCFL ignores tremendous gains in terms of circuit speed and area which can be realized by using the optimization capabilities of the Synopsys Design Compiler™. The **compile** command allows the user to control the optimization process by designating different optimization routines and amounts of computational resources. Design optimization is also controlled by setting constraint variables (e.g. **max_area**, **max_delay**, etc.) to their desired values. Further details on the design optimization

```
current_design = "TOP";
current_library = "vendorA.db";
translate_library = "vendorA_to_FURY.db";
target_library = "fury.db";
link_path = { translate_library current_library target_library };
link;
compile -no_flatten -no_structure -map_effort low;
```

Figure 8: Example Translation Script

process can be found in the Synopsys Design Compiler™ Reference Manual. Figure 9 shows an example of a script which optimizes a design for minimum area. Area optimization is generally the easiest type of optimization to perform because the desired goal (i.e. zero area!) is the easiest to describe.

```
current_design = "TOP";
link_path = { fury.db };
target_library = { fury.db };
max_area 0.0;
```

Figure 9: Example Min. Area Optimization Script

CONVERTING A PLD-BASED DESIGN INTO A VITESSE ASIC DESIGN

Vitesse supports the conversion of various PLD descriptions into Vitesse ASIC designs. The conversion is accomplished using the Synopsys Design Compiler™ in conjunction with specific software developed by Vitesse. PLD file conversion is provided as a service by Vitesse and may be a part of a full turnkey development or a "standard" customer design. This section covers the PLD conversion flow and the PLD file types currently supported.

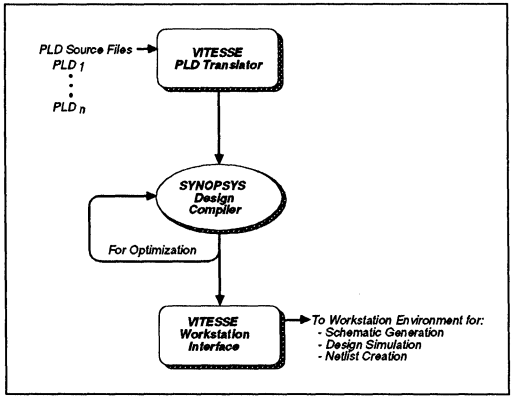

Figure 10: PLD Conversion Flow

Conversion Flow

Figure 10 shows the general flow for PLD conversion. The customer supplies files for one or more PLD devices to Vitesse. These files are combined and then translated into two files used as input for the Synopsys Design Compiler™:

- Equation File - This file describes the combinatorial logic which feeds the state elements in the design.
- EDIF Frame File - This EDIF schematic file contains a reference to the combinatorial block described by the equation file as well as connectivity information for all the registers, buffers, and I/O cells in the design.

The equation file is read into the Synopsys Design Compiler™ and is compiled and optimized using customer provided area and speed constraints, if any. The EDIF frame file is then read into the Synopsys Design Compiler™ and mapped into the VITESSE ASIC library. The two descriptions are then linked and the output files are produced in one of two formats depending on the design flow.

Customer Input Files and Design Information Required

This section summarizes the input files and information required by Vitesse to perform a PLD design conversion. The specific file formats indicate those currently supported by Vitesse. PLD conversion support is constantly being reviewed and upgraded, and the user is urged to contact Vitesse if the conversion of file types other than those listed is desired. All of the file informationshould be supplied on one of the following computer media:

Computer Media Supported

- IBM PC, XT, or AT 5.25" floppy disk - any density
- Apple Macintosh 3.5" floppy disk - any density

- SUN cartridge tape
- Mentor cartridge tape

PLD Design Input

1. ***PLD file(s)*** The customer must supply Vitesse with one or more files which describe the functionality of the PLDs to be converted. These must be on one of the types of computer media named above. Vitesse currently supports the following input file formats for PLD conversion:

- ABL DOC - Equations should be in the format produced by the document module of the ABL compiler. All comments and other extraneous data such as line feeds, form feeds, etc. should be stripped from this file. The file should only contain equations. The following is an example of an equation in ABL DOC file format.

```
SIGOUT1 := IN1 & !IN2 & C0 &
!STOP & GO &
# MAYBE & BARNEY & WILMA &
DINO & !BAMBAM
# BEDROCK & !SIGOUT;
```

The := signifies that SIGOUT1 is a registered output. An equal sign with no colon denotes a purely combinatorial output. The ampersand (&) is a logical AND, the pound sign (#) is a logical OR, an exclamation point (!) represents an inversion, and a semicolon (;) ends the equation. No line continuation character is required.

- CUPL DOC - The stipulations listed for ABL DOC files also apply here. The file should only contain CUPL "DOC" format equations. The following is an example of an equation in the CUPL DOC format.

```
OUT1.d => !IN1 & IN2 &
CYCLE1 & CYCLE2 & CYCLE3
 # OLD_DOG & POOCH &
 !MUTT & !OUT1 & PUP
```

As in the ABL DOC format, the ampersand represents a logical AND while the pound sign signifies a logical OR. Unlike the ABL format, however, a '.d' suffix is used to denote a registered output. The assignment operator is an equal sign followed by the greater than symbol (=>). There is no semicolon at the end of an equation.
Vitesse prefers that the customer supply the PLD description as one file. For instance, if the customer wants to implement a state machine, the preferred PLD input format is a single equation file which describes the combinatorial logic feeding the state elements as if it were written for one large PAL. If multiple equation files are supplied to Vitesse, all of the names must be unique unless the user want those signals shorted together.

2. ***I/O Designation*** The customer must also provide a file which lists all of the primary inputs, outputs, and bidirectionals in the "target" design. The following is an example of the I/O designation file:

```
I/O Designation File Format
.inputlist
IN1
IN2
DATA1
DATA2
.outputlist
OUT1
OUT2
OUT3
Q0
Q1
Q2
.bidirlist
BID1
BID2
```

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3. ***PLD Connectivity File*** - If multiple sets of equations are provided to Vitesse, the customer must also supply a netlist which describes the connectivity of the PLDs in question. The preferred formats are EDIF or VR (Vitesse internal format). Most workstations provide EDIF netlisting capabilities. Otherwise, if the board design containing the PLDs has been captured on the Mentor or VALID, then a VR netlist can be obtained by running the Vitesse netlister. The customer should also provide a hard copy schematic which shows the connectivity visually.

PLD Conversion Example

Figure 11 shows an example CUPL DOC file for a 4-bit up counter. The pld2synopsys translator is used to convert this file into the two files (equation file and EDIF file) needed by the Design Compiler™ for conversion of the PLD. The usage of the command is:

```
pld2synopsys
[-cupl | -abl ]
[-pad] [-oe] input_file
```

where:

-cupl | -abl denotes the input file format: -cupl for a CUPL DOC file and -abl for an ABL DOC file.

-pad causes the translator to add input and output buffers to the design. The -pad switch should be omitted if several PLDs are incorporated in a single conversion.

-oe causes any output enable signals to appear as outputs to the PLD core if the -pad switch is not chosen. If the -pad switch is chosen, then the output enable signals are connected to the output enable inputs of the tri-state outputs.

input_file is the ABL or CUPL input file name

```
**************************************************************************
                                  COUNTER
**************************************************************************

CUPL            3.00 Serial# 999999999
Device          p20r6 Library DLIB-h-24-10
Created         Wed May 16 15:32:49 1990
Name            COUNTER
Partno          none
Revision        1
Date            4/23/90
Designer        George Jetson
Company         Spacely Sprockets
Assembly        none
Location U1
--------------------------------------------------------------------------------
                            Expanded Product Terms
--------------------------------------------------------------------------------
Q1.d =>
      !Q1
Q2.d =>
      Q1
Q3.d =>
      Q1 & Q2
Q4.d =>
      Q1 & Q2 & Q3
--------------------------------------------------------------------------------
                              Symbol Table
--------------------------------------------------------------------------------
Pin  Variable                                    Pterms  Max    Min
Pol  Name              Ext     Pin     Type      Used    Pterms  Level
---  --------          ---     ---     ----      ----    -----   -----

     Q1                        21      V         -       -       -
     Q1                D       21      X         1       1       1
     Q2                        20      V         -       -       -
     Q2                D       20      X         1       1       1
     Q3                        19      V         -       -       -
     Q3                D       19      X         1       1       1
     Q4                        18      V         -       -       -
     Q4                D       18      X         1       1       1
     CLK                       1       V         -       -       -

LEGEND:    F : field          D : default variable       M : extended node
           N : node           I : intermediate variable  T : function
           V : variable       X : extended variable      U : undefined
```

Figure 11: CUPL DOC File for a 4-bit Counter

The following command was used to translate the PLD equations in the example into an EDIF and equation file for subsequent reading into the Design Compiler™:

```
pld2synopsys -cupl counter.doc
```

Figure 12 shows a plot of the converted design produced by the Design Compiler™. Note that in this case, the design was synthesized for minimum area as opposed to the design shown in Figure 7 which is optimized for speed.

SUMMARY

Vitesse can supply both the guidelines and software necessary for converting a design from a Silicon (Bipolar ECL, CMOS, or BiCMOS) implementation into a GaAs DCFL implementation. The conversion may be performed at the customer loca-

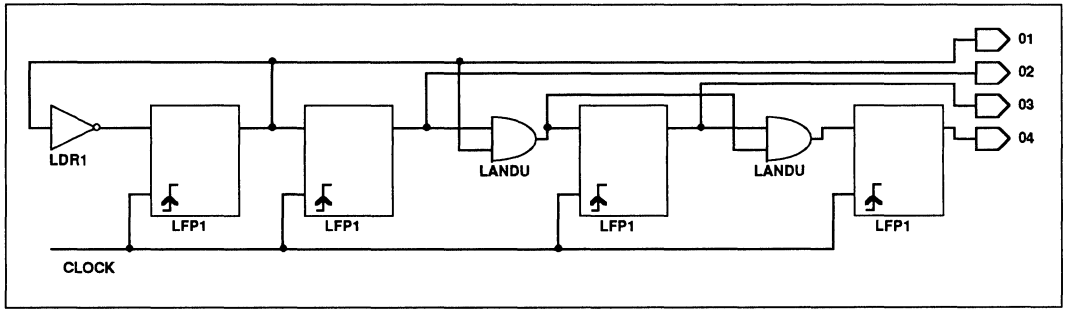


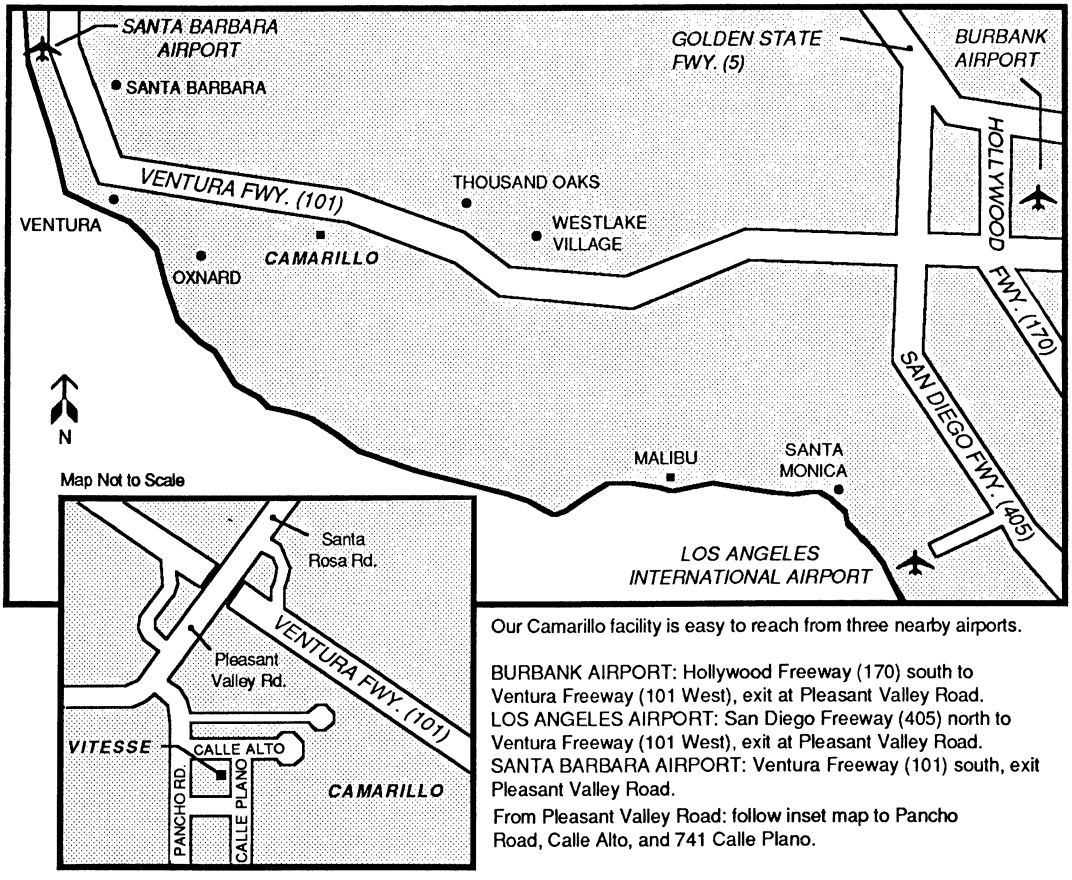
Figure 12: 4-bit Counter in FURY Synthesized from CUPL Equations

tion or in-house by Vitesse. For more detailed information on the capabilites of the Synopsys Design Compiler™, the following sources are recommended:

Synopsys™ Design Compiler™ Reference Manual. Synopsys, Inc. Version 1.2, October 30, 1989.

Synopsys™ Design Compiler™ Commands Reference. Synopsys, Inc. Version 1.2, November 30, 1989.

Synopsys Technical Applications Note #2: "Technology Translation Applications Note", Cynthia Collart, Revision 1.0, April 13, 1989.



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LOS ANGELES AIRPORT: San Diego Freeway (405) north to Ventura Freeway (101 West), exit at Pleasant Valley Road.
SANTA BARBARA AIRPORT: Ventura Freeway (101) south, exit Pleasant Valley Road.
From Pleasant Valley Road: follow inset map to Pancho Road, Calle Alto, and 741 Calle Plano.

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The following is a list of some convenient hotels and motels you may choose to stay in when visiting the Camarillo Headquarters of Vitesse Semiconductor Corporation.

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Hwy 101 at Ventu Park Road exit
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The Days Inn
Tel: 805/375-1431
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The Hyatt Westlake Plaza*
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Hwy 101 at Westlake Boulevard
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The Courtyard by Marriott*
Tel: 805/388-1020
Hwy 101 at Santa Rosa Road
in Camarillo (North)

** Recommended*

ORDERING INFORMATION

Vitesse products are available in a variety of packages and operating ranges. The order number is formed by using a combination of the following: *Device Type, Package Type, Operating Temperature Range, Speed Option,* and *I/O Type.*

Specific ordering numbers are listed for each standard product family below and on the next page. Please consult with a Vitesse sales representative to determine device availability.

VS8000 FAMILY - STANDARD LOGIC

VS8001 L I

Device Type

VS8001: 1.25 Gb/Sec 12:1 Multiplexer
VS8002: 1.25 Gb/Sec 1:12 Demultiplexer
VS8004: 2.5 Gb/Sec 4:1 Multiplexer
VS8005: 2.5 Gb/Sec 1:4 Demultiplexer
VS8010: SONET - 1.25 Gb/Sec 8-bit Mux/ Demux with Frame Synchronization
VS8011: SONET - 1.25 Gb/Sec 8-bit Multiplexer
VS8012: SONET - 1.25 Gb/Sec 8-bit Demultiplexer with Frame Synchronization
VS8021: SONET - 2.4 Gb/Sec 8-bit Multiplexer
VS8022: SONET - 2.4 Gb/Sec 8-bit Demultiplexer

Temperature

C: Commercial (0° to 70°C)
I: Industrial (-40° to +85°C)

Package Type

L: Leadless Chip Carrier (LCC)
F: Leaded Chip Carrier (LDCC)

VS12G00 FAMILY - RAMS

VS12G422T L C - 5

Device Type

VS12G422T: 256 x 4-bit TTL Static RAM
VS12G478: 2K x 2-bit ECL SRAM

Speed Range

VS12G422T: 4, 5, and 6 ns
VS12G478: 5 and 6 ns

Package Type

D: 22- and 24-pin DIP
L: 28-pin Leadless Chip Carrier (LCC)
F: 28-pin Leaded Chip Carrier (LDCC)

Temperature

C: Commercial (0 to 70°C)
M: Military (-55 to +125°C) (1)

(1) Contact Vitesse for availability of military temperature range parts.

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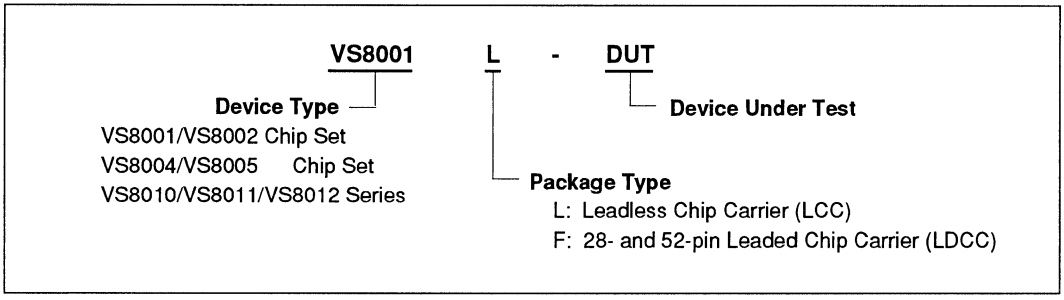
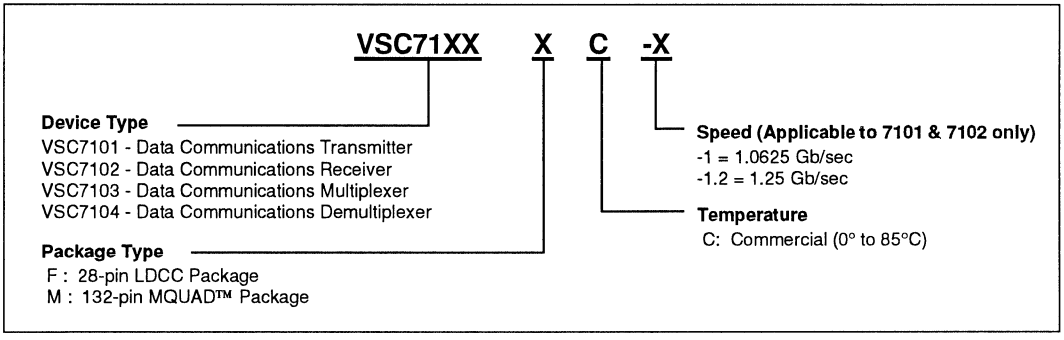


G-TAXICHIPS - DATACOMMUNICATIONS



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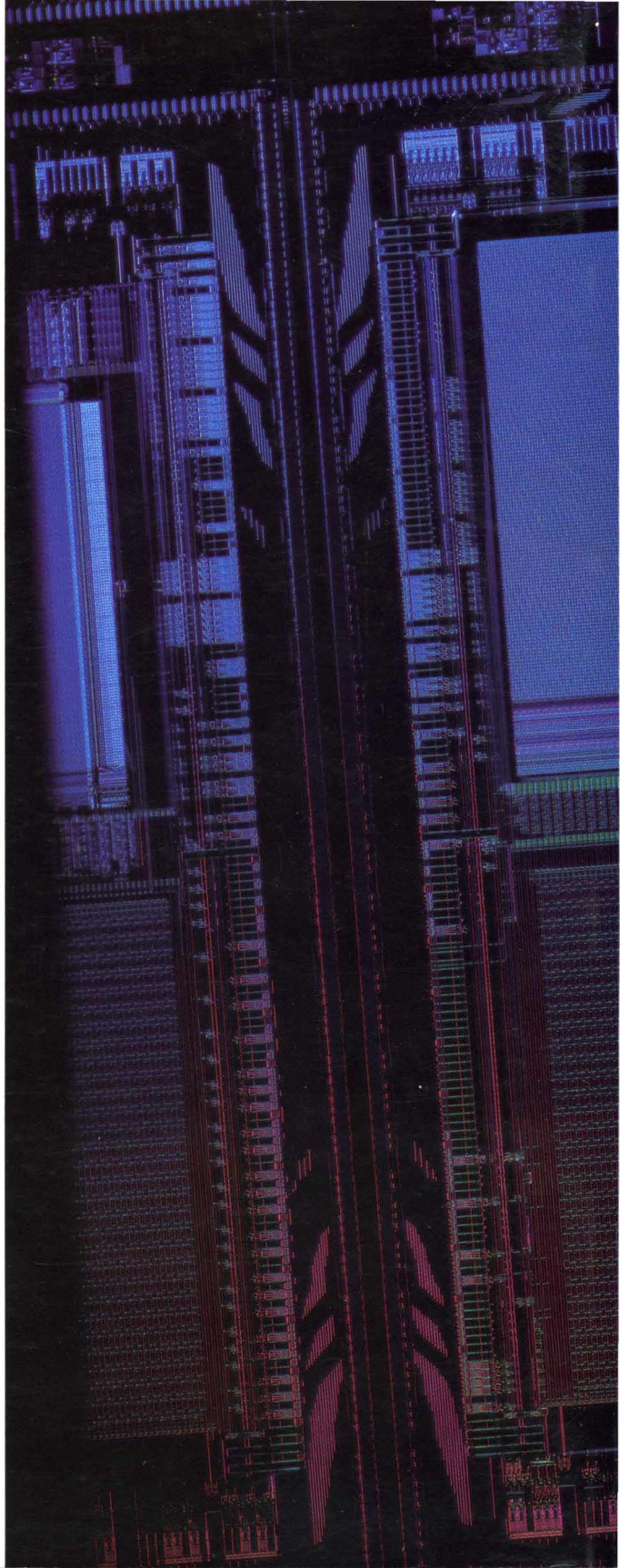

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